Control Art of Switching Converters

Thesis by

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Dedicated to My Mother Wanhua Ma

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Abstract

Switching Flow-Graph Model

The Switching Flow-Graph is a unified graphical model of large-signal, small-signal and steady-state behavior of pulse-width-modulated (PWM) switching converters. Switching branches are introduced into the flow-graph to represent the switches of the PWM switching converters. The Switching Flow-Graph model is easy to derive, and it provides a visual physical understanding of switching converter systems. The small-signal Switching Flow-Graph generates analytical transfer functions and the large-signal Switching Flow-Graph is compatible with the TUTSIM simulation program. The Switching Flow-Graphs of PWM switching converters reveal a regular pattern, and they predict right-half-plane (RHP) zeros, caused by the imbalanced effects of the duty-ratio control signal on the output of the switching converters. Criteria are found for the design of damping circuits that are capable of eliminating RHP zeros. General models are derived for current-mode controlled switching converters. In addition, the large-signal model and the small-signal model are verified by experiments.

One-Cycle Control Technique

The One-Cycle Control technique is conceived to control the duty-ratio d of the switch in real time such that in *each cycle* the average of the chopped waveform at the switch output is *exactly* equal to the control reference. Implementation circuits are found for any type of switch, constant frequency, constant ON-time, constant OFF-time, and

variable. One-Cycle Control fully rejects the input signal, and linearly all passes the control signal. This technique turns a nonlinear switch into a linear one. Experiments were conducted using the One-Cycle Control technique on the buck converter and the Ćuk converter. One-Cycle Control was found to reject input perturbations and input filter dynamics. The diode voltage of One-Cycle Controlled converters follows the control reference instantaneously in one cycle. One-Cycle Control takes advantage of the pulsed and nonlinear nature of switching converters to achieve instantaneous control of the average value of the diode voltage. This technique is suitable for large-signal control of PWM switching converters and quasi-resonant converters.

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Chapter 1

Introduction

1.1 Object

Switching converters, as shown in Fig. 1.1, are power processing units that utilize lossless components, switches, inductors, and capacitors to convert input power to output power with 100 percent efficiency in the ideal case. The input power is generally AC or DC, whereas the output power can be AC , DC, or any desired function. The conversion capability for a particular application is established by the topology of the converter, while the function and quality of the output waveform depends on the control-loop design.

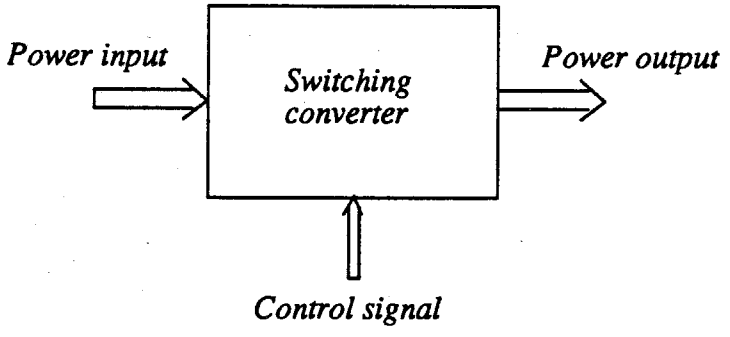


Figure 1.1: Switching Converter. It is a power processing unit. The input power may be AC or DC, the output power may be AC, DC or any desired functions.

In recent years power electronics has been a very active discipline. Many new switching converter topologies have been and are being discovered in both the pulse-width-

modulation (PWM) converter family and the quasi-resonant converter family [1]. The circuits are becoming more complicated; therefore, the modelling tools and the control techniques are confronting new challenges.

Switching converters are pulsed and nonlinear dynamic systems. There has been no standard way to model and control nonlinear systems. People usually avoid the pulsed and nonlinear nature by linearizing the governing equations to obtain small-signal models. Linear feedback control structures are used to control nonlinear systems. If a system is very simple, a satisfactory control loop may be obtained through the use of a small-signal model, a linear control scheme, some previous design experience and a lot of trial and error. However, if the circuit is more complicated, this approach may never achieve a workable solution. First of all, a small-signal model provides only the local dynamic information around the operating point; if the system is perturbed, enough to leave the operating point, the system may not converge. On the other hand, since switching converters are pulsed and nonlinear in nature, their capability is greatly restricted if linear feedback control is applied.

The work in this thesis takes advantage of the pulsed and nonlinear nature of switching converter systems rather than avoiding it. The goal here is to find a suitable way to achieve switching nonlinear control. The motivation is that a switching system under pulsed nature nonlinear control should be more robust, have faster dynamic response and better input perturbation rejection than the same system under linear control.

In Part I, a new unified nonlinear modelling tool, the Switching Flow-Graph technique, is developed and used to reveal the global and local dynamic properties of switching converters. In Part II, a new pulsed nature nonlinear control technique, One-Cycle Control, is conceived based on the understanding gained from the model. The One-Cycle Control technique provides fast dynamic response and good input perturbation rejection.

It can be used to control PWM converters and quasi-resonant converters. A buck converter and a Ćuk converter were built to test both the One-Cycle Control technique and the Switching Flow-Graph model.

1.2 Background

A brief review of the previous work on modelling and control techniques of switching converters is given below for comparison to the present work.

Small-Signal Modeling Techniques

The state-space averaging method [2] is widely used in industry. This method averages and linearizes the pulsed and nonlinear trajectories in state space. This model provides small-signal predictions with very good accuracy when the signal frequency is lower than half the switching frequency.

The sampled-data modelling method [3] is another small-signal modelling tool that provides better accuracy at high frequency. However, the mathematics are much more complicated than for the state-space averaging method.

The small-signal frequency response theory [4] provides an exact solution to the frequency response problem of DC-to-DC converter systems; however, it is valid only in the small-signal limit.

The small-signal models are linear and hence easily applied to most practical design problems. However, because of the small-signal assumption, these models do not describe the behavior of the switching converter during large transients.

Large-Signal Modelling Techniques

Robert Erickson developed a large-signal model for state-feedback switching regulators [5]. The model is provided in two forms, a discrete-time equation for use in com-

puter simulations and an analytical matrix expression to enhance physical understanding. However, the model does not provide a general form for large-signal, small-signal, and steady-state analysis.

Control Techniques

PWM feedback control is a linear error control technique. The output voltage of the switching converter is compared with a control reference. The error between the control reference and the output voltage is amplified and compared with a saw-tooth waveform to adjust the duty-ratio in the direction required to reduce the error. In order to obtain good input perturbation rejection and fast dynamic response to the control reference, the loop-gain must be very high. Unfortunately, high loop-gain may cause circuit instability.

The current-mode control technique, [6][7], includes some pulsed nature control concepts. The switch current is sensed and compared with a control reference. The transistor is turned ON at clock pulses and is turned OFF when the switch current reaches the control reference. This method is equivalent to state-feedback control. A stabilizing ramp is necessary when the system operates at a duty-ratio larger than 0.5. If the slope of the ramp is equal to the falling slope of the inductor currents which flow through the transistor when it is ON, this control technique will reject input perturbations. However, only the buck converters with constant output voltage satisfy this condition.

Sliding-mode control [8][9] is based on pulsed and nonlinear nature. A sliding line is defined through the operating point. The switch is turned ON when the trajectories reach the lower limit, and is turned OFF when the trajectories reach the upper limit. The system motion is restricted along the sliding line and within the hysteresis, $\Delta < \sigma < \Delta$, as shown in Fig. 1.2. Therefore, the system order is reduced by one. However, the switch operates at a variable frequency.

If a variable hysteresis is used to envelope the system motion, as shown in Fig. 1.3,

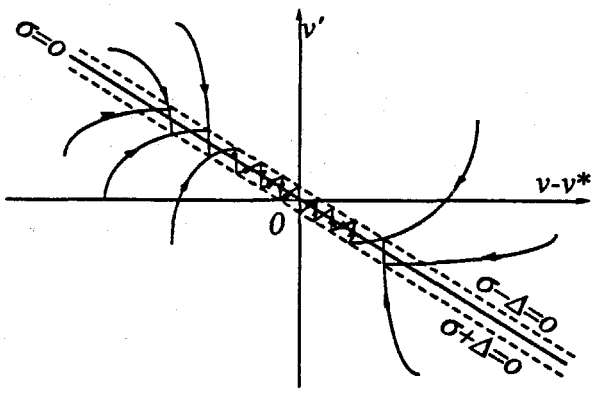


Figure 1.2: Sliding-Mode Control Concept. A sliding line is defined through the operating point. The switch is turned ON when the trajectories reach the lower limit, and is turned OFF when the trajectories reach the upper limit. Therefore, the system motion is restricted along the sliding line and within the hysteresis, $\Delta < \sigma < \Delta$.

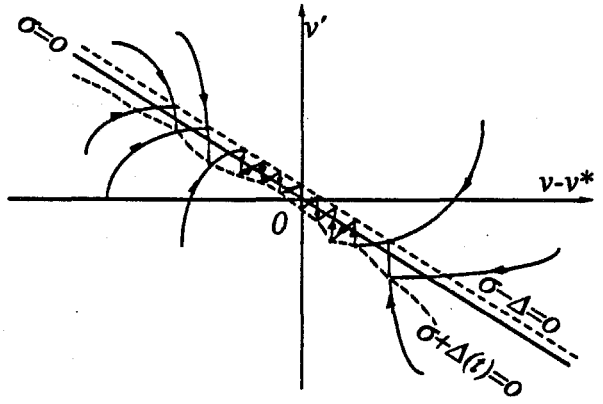


Figure 1.3: Constant Frequency Sliding-Mode Control. A variable hysteresis is used to envelope the system motion. The switch is turned ON by the clock pulse, and turned OFF when the trajectories reach the upper limit.

the switching frequency is fixed [10]. In this case, the switch is turned ON by the clock pulse, and turned OFF when the trajectories reach the upper limit. This control function is similar to the one used for current-mode control.

Sliding-mode control is possible only when both the reaching condition and the converging condition are satisfied. When the system order is higher than two, a sliding surface is very hard to find that satisfies both the reaching condition and the converging condition.

1.3 Outline of the Thesis

This thesis contains two parts. The Switching Flow-Graph model is discussed in Part I and the One-Cycle Control technique is presented in Part II. Each Part of the thesis includes both theory and experiments.

Part I. Switching Flow-Graph Model

The Switching Flow-Graph technique provides a unified graphical representation of the large-signal nonlinear model, the small-signal model and the steady-state model for any PWM switching converter.

This technique utilizes some concepts from state-space averaging, and is an extension of linear circuit flow-graph theory. Though a switching converter is a nonlinear system, it is equivalent to a linear circuit, the ON-circuit, when the switch is in the ON state, and it is equivalent to another linear circuit, the OFF-circuit, when the switch is in the OFF state. The On-circuit and the OFF-circuit can be described by their respective flow-graphs. The Switching Flow-Graph is obtained by combining the flow-graphs of the ON-circuit and the OFF-circuit through the use of switching branches. The switching branches are the only nonlinear components in the Switching Flow-Graph; therefore,

the modelling work is reduced to the switching branches. Large-signal, small-signal and steady-state representations of the switching branches are given. The Switching Flow-Graph model is very easy to obtain, and it provides a visual means for the physical understanding of switching converter systems. It can predict the large-signal, the small-signal, and the steady-state behavior of switching converter systems. The details are described in Chapter 2.

In Chapter 3, the Switching Flow-Graph modelling technique is used to model the most commonly used PWM switching converters in the second-order and fourth-order families. The Switching Flow-Graphs reveal a regular pattern, and generate deeper physical insight into the function of switching converters. The large-signal model is compatible with the TUTSIM simulation program [11]. Users enter the branch transmittances, the node connections, the initial conditions, and the simulation step size. The small-signal model gives visual graphs and analytical transfer functions. The Switching Flow-Graph technique is used to predict the global and local dynamic behavior of switching converters. Experiments were conducted to verify the large-signal model and the small-signal model. The measured and the predicted dynamic response are very close.

In Chapter 4, the Switching Flow-Graph model is used to develop a physical explanation of right-half-plane (RHP) zero problems. The duty-ratio control reference has imbalanced effects on the output of the switching converters, which causes the RHP zeros. Design criteria are found, for the damping circuit, to eliminate the RHP zeros. The model can analytically predict the conditions under which the RHP zeros will appear and therefore reveals how to eliminate them. Experiments were conducted to generate and remove the RHP zeros. The experimental results verified the theoretical predictions.

The general model for current-mode controlled switching converters is derived, in Chapter 5, using the Switching Flow-Graph technique. The current-mode control-loop

does not affect the zeros in the transfer function of the switching converters, while it rearranges the system poles, which is, however, not fully controllable, since the state-feedback coefficients are restricted by the current-mode control function. Current-mode control may convert RHP zeros into RHP poles; therefore, the loop may oscillate. Experiments verified the predictions.

Part II. One-Cycle Control Technique

The One-Cycle Control technique is conceived to control the duty-ratio d of the switch in real time such that in *each cycle* the average of the chopped waveform at the switch output is *exactly* equal to the control reference. With One-Cycle Control, a switching converter can rejects the effects of the input voltage, and follows the control reference quickly. This technique is suitable for large-signal control of PWM switching converters and quasi-resonant converters.

The general concept of One-Cycle Control can be summarized as follows: The effective value of the chopped waveform at the switch output is its average when the signal frequency is lower than half of the switching frequency. A real-time integrator is employed to integrate the chopped waveform. If the integrated value of the chopped waveform in one cycle is exactly equal to the integrated value of the control reference in one cycle, then the average of the chopped waveform is exactly equal to the control reference in one cycle. The implementation circuits are found for any type of switch, constant frequency, constant ON-time, constant OFF-time, and variable. The key component of One-Cycle Control is the real-time integrator. For a constant-frequency switch example, the real-time integrator starts integrating at the instant when the switch is turned on, and when the integrated value reaches the control reference, the controller shuts OFF the switch. Therefore, the output signal of the switch is exactly equal to the control signal. The details of the One-Cycle Control theory and its implementation are

described in Chapter 6.

In Chapter 7, the One-Cycle Control technique is used to control the PWM buck converter. The control processes are analyzed to see exactly how the circuit rejects the input voltage and the load current perturbations, and how it follows the control reference. When the converter has an input filter, the dynamics of the input filter do not affect the dynamic response of the output. The One-Cycle Controlled buck converter with input filter behaves like a second-order system. This control scheme is compared with the PWM feedback control technique and the current-mode control technique. Experiments were conducted to verify the theory.

In Chapter 8, the dynamic behavior of the One-Cycle Controlled system is investigated, with the Ćuk converter as an example. The diode voltage of the Ćuk converter is instantaneously controlled by the control reference; therefore, one would assume that the control-loop has infinite loop-gain. The Switching Flow-Graph model is employed to study the large-signal stability and small-signal behavior of the One-Cycle Controlled system. The One-Cycle Controlled Ćuk converter is not globally stable. However, the limitation of the switching duty-ratio may prevent the system from operating in the unstable region. It is also found that the One-Cycle Control loop-gain is below $0db$! The system dynamics must obey physical laws; therefore, the transients of the capacitor voltage and the inductor current are not instantaneously controlled. One-Cycle Control takes advantage of the pulsed and nonlinear nature of the system to achieve instantaneous control over the average value of diode voltage.

The physical limitations, the discontinuous current operating condition, and the design of the real-time integrator are discussed in Chapter 9.

The conclusions and some further discussion are given in Chapter 10.

Part I

Switching Flow-Graph Model

Chapter 2

Switching Flow-Graph Modelling Technique

A new modelling tool for switching converters, the Switching Flow-Graph Modelling Technique, is introduced in this chapter. This technique is developed based on experience with the state-space averaging method and the linear circuit flow-graph method. This new technique can be utilized to create the large-signal nonlinear model, the small-signal linear model, and the steady-state model.

A brief background of flow-graph is reviewed in Section 2.1. The Switching Flow-Graph is introduced in Section 2.2. The switching functions, constant frequency, constant ON-time, constant OFF-time, and variable, are discussed for the switching branches in Section 2.3. The large-signal, steady-state, and small-signal representations of the Switching Flow-Graph are obtained in Section 2.4, Section 2.5, and Section 2.6, respectively. The linear circuit extra-element theory is extended to the use in flow-graphs and Switching Flow-Graphs in Section 2.7.

2.1 Flow-Graph Background

Flow-graph [18] is a symbolic language for the description of dynamic systems that provides a graphic representation of the signal flow within the system. The flow-graph construction breaks a system into virtually all of its basic components, and thereby clearly illustrates the effects of input and/or parameter changes upon its signals at all points in the system. Flow-graphs may be reduced, using standard procedures, to obtain

transfer characteristics between arbitrary points in the system. Once the basic concepts of this technique are understood, the flow-graph can be easily constructed from the system equations or directly from the electrical circuit.

The signals are represented by nodes, which are schematically represented by small circles in the diagrams. The nodes are connected by branches, line segments with arrows. The signals flow only in the direction of the arrow on each branch. Each branch has a transmittance or gain indicated next to it and the signals passing along that branch are multiplied by the branch transmittance. The signal at a node is the sum of all signals entering the node. Source nodes, nodes with outputs only, represent independent variables. Sink nodes, nodes with inputs only, always represent dependent variables. A mixed node has both inputs and outputs.

The procedure for constructing the flow-graph of a system is straightforward. First each variable of interest is assigned a node on the flow-graph. Next the nodes are interconnected as required by the specific system configuration. Once all of the nodes are properly connected, the flow-graph is complete.

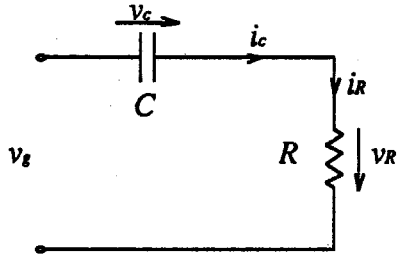


Figure 2.1: The RC Circuit. v_g is the input voltage, v_C is the voltage cross the capacitor, i_C is the capacitor current, i_R is the resistor current and v_R is the output voltage.

Consider a simple RC circuit as an example. Fig. 2.1 depicts an RC circuit, where v_g is the input voltage, v_C is the voltage across the capacitor, i_C is the capacitor current, i_R is the resistor current, and v_R is the output voltage. To create the flow-graph for this

RC circuit, first assign five nodes from left to right to denote v_g, v_C, i_C, i_R, and v_R, respectively, as shown in Fig. 2.2 (a). From Kerchhoff's law, it is found that:

$$v_C = v_g - v_R \tag{2.1}$$

$$i_C = CSv_C \tag{2.2}$$

$$i_R = i_C \tag{2.3}$$

$$v_R = Ri_R \tag{2.4}$$

where C is the capacitance, R is the resistance, and S is the Laplace complex number $S = \sigma + j\omega$. These relations are used to connect the nodes in Fig. 2.2 (a), to produce the flow-graph shown in Fig. 2.2 (b). The node that represents the input voltage v_g is

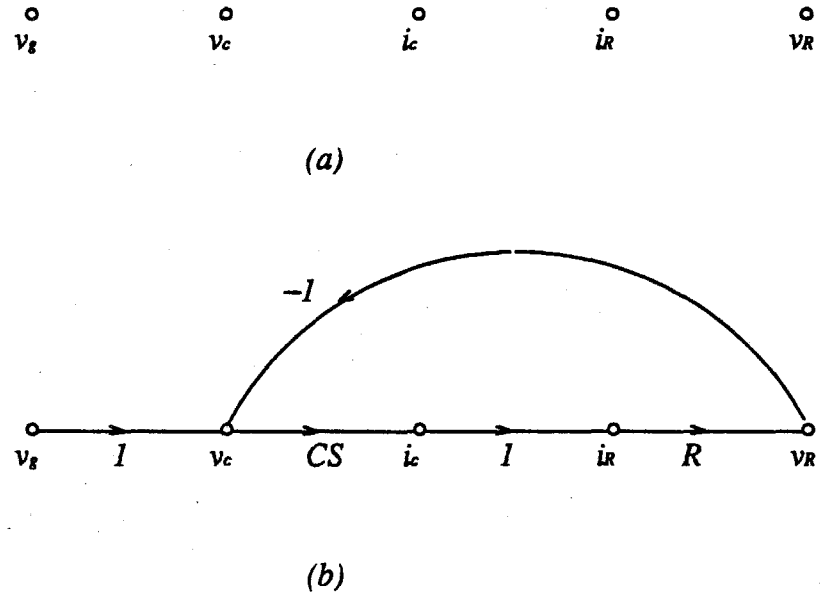


Figure 2.2: Flow-Graph of the RC Circuit. (a) Five nodes are assigned to the circuit variables: v_g, v_C, i_C, i_R, and v_R. (b) The nodes are connected according to the circuit equations (2.1), (2.2), (2.3) and (2.4).

a source node, while the other nodes are mixed nodes. From the flow-graph, it is very

easy to obtain the transfer function for the circuit.

$$v_o = v_R \tag{2.5}$$

$$= \frac{RCS}{1+RCS} v_g \tag{2.6}$$

2.2 Switching Flow-Graph

Flow-graph is a very useful tool for the design and analysis of linear circuits. This tool is extended to study the dynamic behavior of switching converters.

Switching converters are nonlinear dynamic systems; however, deeper insight reveals that switching converters are systems with variable structure. A switching converter, in continuous mode, contains two linear subcircuits. The subcircuits share common elements, such as inductors, capacitors and resistors, connected in different topologies. The switch of the converter operates at a frequency, either constant or variable, and alters the system between the two linear subcircuits. This conceptual view provoked the motivation to model these two linear subcircuits using flow-graphs, then to relate the flow-graphs to each other using switching branches.

Suppose a switching converter operates at a frequency $f_s(t) = \frac{1}{T_s(t)}$. When $0 < t < T_{ON}$ the switch S is ON, and when $T_{ON} < t < T_s$, the switch S is OFF. For the two positions of the switch S, in the switching converter, the two switched subcircuits are obtained. It is clear that a change in the topological structure occurs within each period as the circuit configuration is periodically changed from the ON-circuit to the OFF-circuit. Both switched subcircuits are linear by themselves, while the converter itself is a nonlinear circuit due to the periodic structure change. The fact that both subcircuits are linear enables them to be modelled using the flow-graph technique.

During the time when the switch S is in the ON position, $0 < t < T_{ON}$, the converter is switched to the ON-circuit. Nodes are assigned to each variable, according to the

ON-circuit configuration, and are connected to form a flow-graph $\mathcal{G}_{ON}$. During the time when the switch S is in the OFF position, $T_{ON} < t < T_s$, the converter is switched to the OFF-circuit. The OFF-circuit contains the same circuit elements as those in the ON-circuit; therefore, it preserves the same variables. The same nodes, which were used for the ON-circuit, are used to represent the OFF-circuit variables. However, the nodes are connected according to the OFF-circuit configuration to form a flow-graph $\mathcal{G}_{OFF}$.

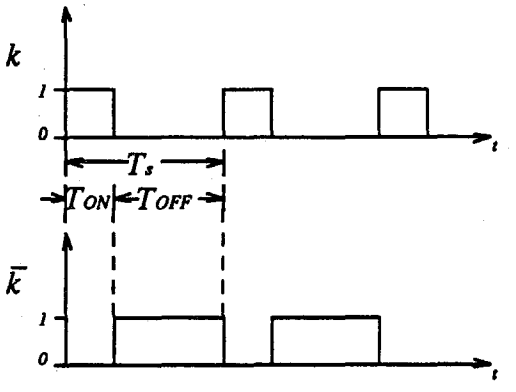


Figure 2.3: Switching Functions. The k function has a value of "1," when $0 < t < T_{ON}$, and has a value "0," when $T_{ON} < t < T_s$. The $\overline{k}$ function has a value of $1 - k$.

The two flow-graphs, $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$, have exactly the same nodes. However, some connections that exist in $\mathcal{G}_{ON}$ may not exist in $\mathcal{G}_{OFF}$, and some branches that exist in $\mathcal{G}_{OFF}$ may not exist in $\mathcal{G}_{ON}$. Consider the switching functions k and $\overline{k}$ as shown in Fig. 2.3. The k function has a value "1," when $0 < t < T_{ON}$, and has a value zero, when $T_{ON} < t < T_s$. The $\overline{k}$ function has a value of $1 - k$. With these two switching functions, the two flow-graphs $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$ can be topologically merged by the following equation:

$$\mathcal{G} = k\mathcal{G}_{ON} + \overline{k}\mathcal{G}_{OFF} \tag{2.7}$$

Two switching branches, the k-branch and its complementary $\overline{k}$-branch, are thus

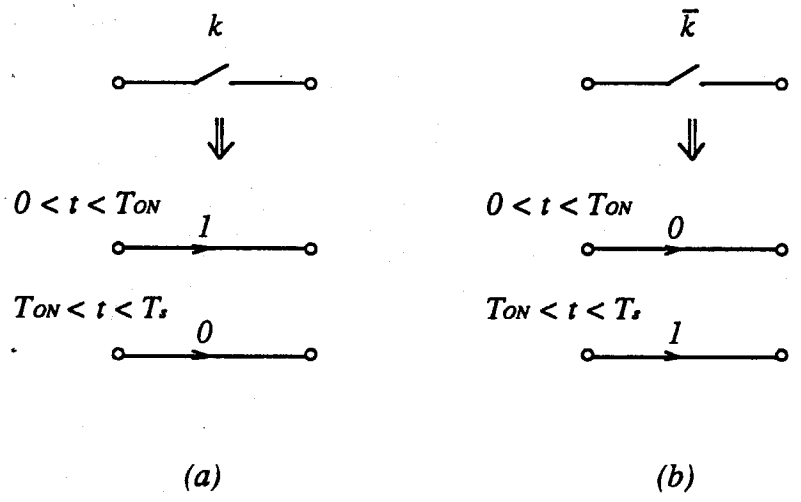


Figure 2.4: The Switching Branches: k and $\bar{k}$. During the time $0 < t < T_{ON}$, the k-branch has a transmittance of "1," and the $\bar{k}$-branch has a transmittance of "0." During the time $T_{ON} < t < T_S$, the k branch has a transmittance of "0," and the $\bar{k}$-branch has a transmittance of "1."

introduced, as shown in Fig. 2.4. The transmittances of the two branches are time dependent. During the time $0 < t < T_{ON}$, the k-branch has a transmittance of "1," and the $\bar{k}$-branch has a transmittance of "0." During the time $T_{ON} < t < T_S$, the k branch has a transmittance of "0," and the $\bar{k}$-branch has a transmittance of "1." These switching branches physically unite the two flow-graphs, $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$, into one flow-graph $\mathcal{G}$. $\mathcal{G}$ is the graphical representation of the switching converter. The flow-graph $\mathcal{G}$ contains switching branches, the k-branch and the $\bar{k}$-branch, therefore, it is defined as a Switching Flow-Graph . The switching control signals are injected into the converter through these switching branches.

Consider the buckboost converter, shown in Fig. 2.5 (a), as an example, where v_g is the input voltage, L is the inductor, C is the capacitor, R is the load, R_L is the parasitic resistance of the inductor, and S is the switch. Define v_L, v_{R_L}, and v_o as the inductor voltage, the parasitic-resistor voltage, and the output voltage respectively.

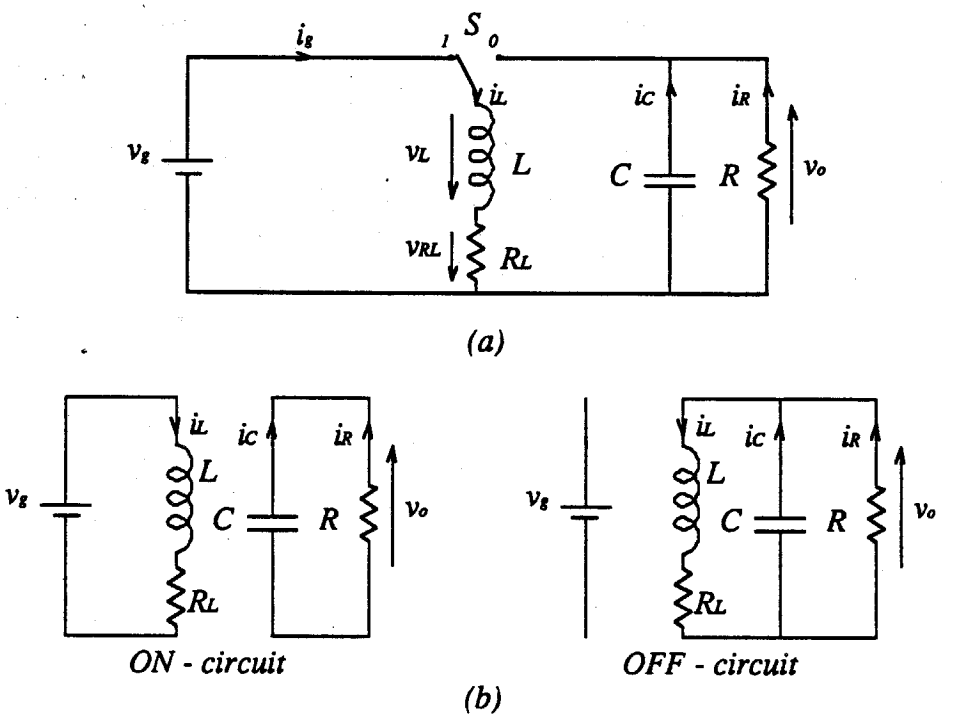


Figure 2.5: The Buckboost Converter and its Subcircuits. (a) The buckboost converter. (b) The two subcircuits: ON-circuit and OFF-circuit.

Define i_g, i_L, and i_o as the input current, the inductor current, and the output current flowing in the same direction as v_g, v_L, and v_o respectively. The quantity i_o is the sum of the load current and the capacitor current i_C. The two subcircuits, the ON-circuit and the OFF-circuit, are shown in Fig. 2.5 (b). When the switch is ON, the buckboost converter is equivalent to its ON-circuit, and when the switch is OFF, it is equivalent to its OFF-circuit.

The two subcircuits can be described by their flow-graphs, $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$, shown in Fig. 2.6 (a). These two flow-graphs share the same nodes and share some of the same branches. By overlapping $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$, it is easily seen that some branches exist in both $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$, while other branches exist only in one of them. The branches that exist in $\mathcal{G}_{ON}$ but not in $\mathcal{G}_{OFF}$ are replaced by k-branches, and the branches that

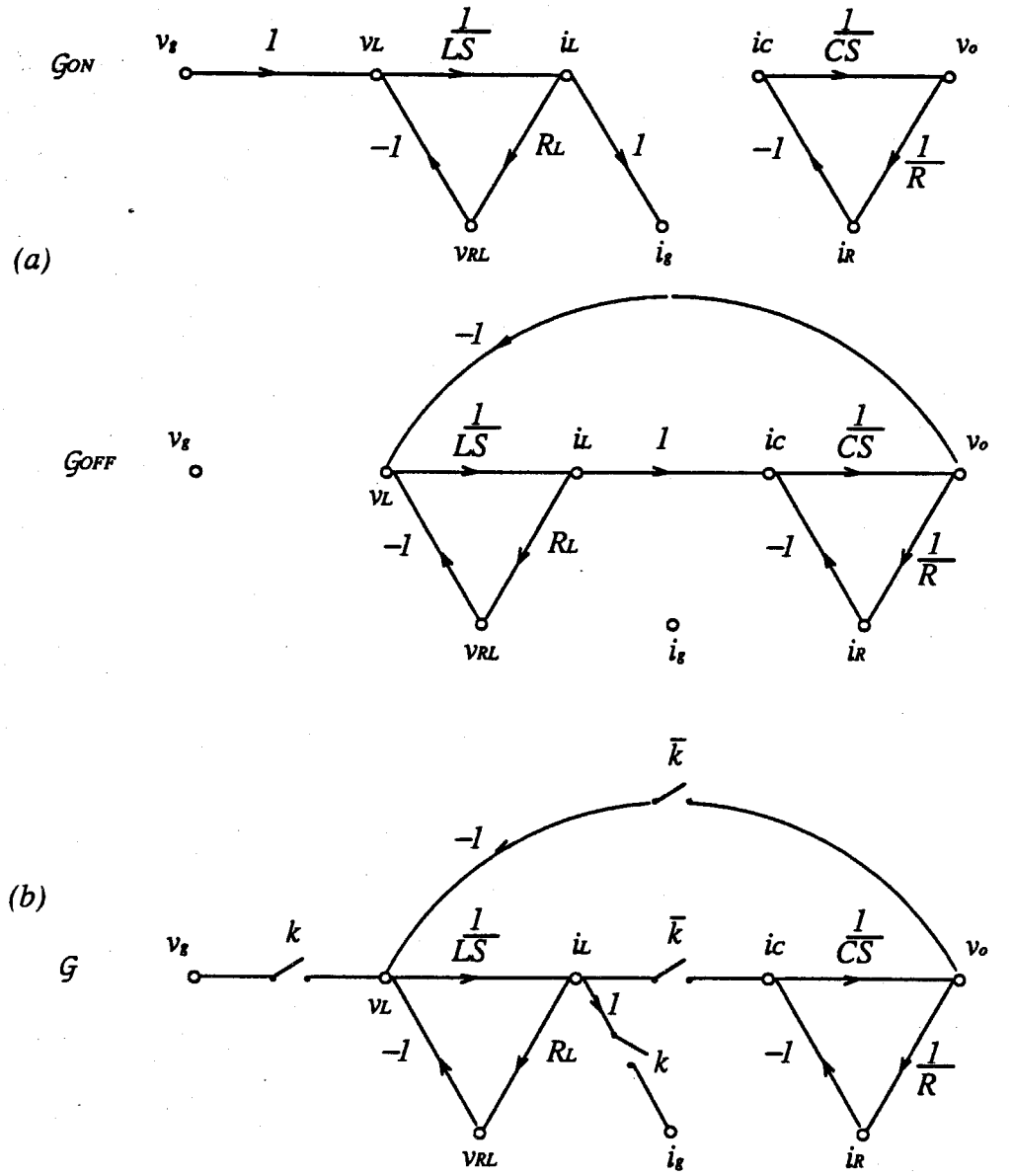


Figure 2.6: The Switching Flow-Graph of the Buckboost Converter. (a) The flow-graph $\mathcal{G}_{ON}$ for the buckboost ON-circuit and the flow-graph $\mathcal{G}_{OFF}$ for the buck-boost converter OFF-circuit. (b) The Switching Flow-Graph $\mathcal{G}$ for the buckboost converter.

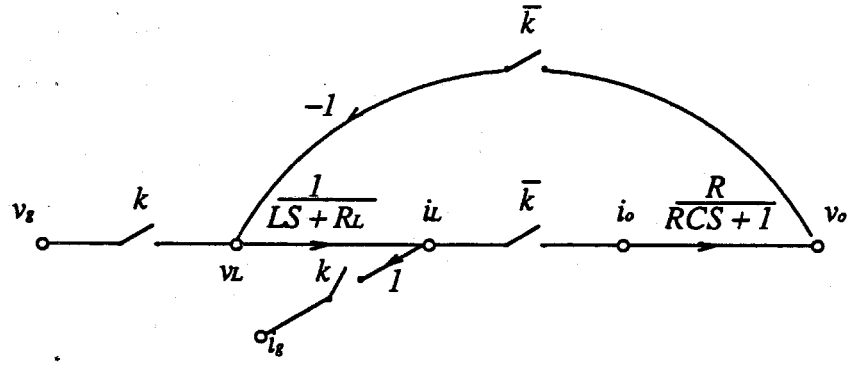


Figure 2.7: The Simplified Switching Flow-Graph of the Buckboost Converter.

exist in $\mathcal{G}_{OFF}$ but not in $\mathcal{G}_{ON}$ are replaced by $\overline{k}$-branches. Therefore, $\mathcal{G}_{ON}$ and $\mathcal{G}_{OFF}$ are combined to form one Switching Flow-Graph $\mathcal{G}$, shown in Fig. 2.6 (b). In addition, the Switching Flow-Graph $\mathcal{G}$ of the buckboost converter can be simplified, as shown in Fig. 2.7, using the algebraic rules in Appendix A.

2.3 Switches

The Switching Flow-Graph $\mathcal{G}$ is linear except for the switching branches. The switching branches are the signal-flow representations of the real switches. The real switches in the switching converter have very different behavior depending on their voltage, current, and load conditions. Therefore, it is very difficult to make a general model for the real switches. However, when switching converters are transferred into Switching Flow-Graphs, the switches are transferred into generalized switching branches: k-branches and $\overline{k}$-branches. The k-branches represent the active switches, whereas the $\overline{k}$-branches represent the passive switches. The active switching branch and the passive switching branch are complementary.

Switches are classified, according to their operating function, as constant frequency switches, constant ON-time switches, constant OFF-time switches, and variable switches.

The constant frequency switch operates at a switching frequency $f_s = \frac{1}{T_s}$. The switch remains in the ON state for a variable time duration $T_{ON}(t)$ and remains in the OFF state for a variable time duration $T_{OFF}(t)$, where $T_{ON}(t) + T_{OFF}(t) = T_s$, as shown in Fig. 2.8.

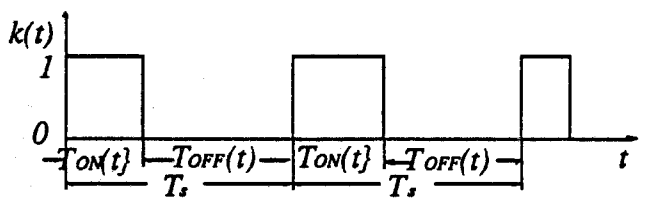


Figure 2.8: The Constant Frequency Switch. The constant frequency switch operates at a switching frequency $f_s = \frac{1}{T_s}$.

The constant ON-time switch operates at a variable switching frequency $f_s(t) = \frac{1}{T_s(t)}$. The switch remains in the ON state for a constant period T_{ON} and remains in the OFF state for a variable time duration $T_{OFF}(t)$, where $T_{ON} + T_{OFF}(t) = T_s(t)$, as shown in Fig. 2.9.

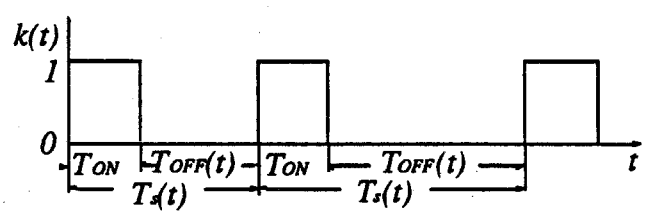


Figure 2.9: The Constant ON-Time Switch. The constant ON-time switch operates at a variable switching frequency $f_s(t) = \frac{1}{T_s(t)}$. The switch remains in the ON state for a constant duration T_{ON} and remains in the OFF state for a variable time duration $T_{OFF}(t)$.

The constant OFF-time switch operates at a variable switching frequency $f_s(t) =$

$\frac{1}{T_s(t)}$. The switch remains in the ON state for a variable time duration $T_{ON}(t)$ and remains in the OFF state for a constant time duration T_{OFF} as shown in Fig. 2.10.

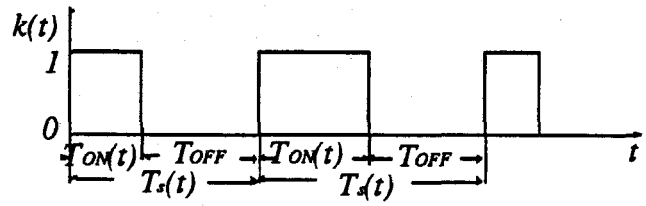


Figure 2.10: The Constant OFF-Time Switch. The constant OFF-time switch operates at a variable switching frequency $f_s(t) = \frac{1}{T_s(t)}$. The switch remains in the ON state for a variable time duration $T_{ON}(t)$ and remains in the OFF state for a constant time duration T_{OFF}.

The variable switch operates at a variable switching frequency $f_s(t) = \frac{1}{T_s(t)}$. The switch remains in the ON state for a variable time duration $T_{ON}(t)$ and remains in the OFF state for a variable time duration $T_{OFF}(t)$ as shown in Fig. 2.11.

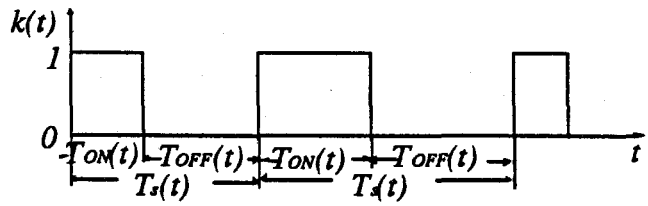


Figure 2.11: The Variable Switch. The variable switch operates at a variable switching frequency $f_s(t) = \frac{1}{T_s(t)}$. The switch remains in the ON state for a variable time duration $T_{OFF}(t)$ and remains in the OFF state for a variable time duration $T_{OFF}(t)$.

2.4 Large-Signal Model of Switching Converters

Suppose that the signal entering the k-branch is $x(t)$, and that the the output signal of the switching branch is $y(t)$. The input signal $x(t)$ is chopped by the switch function, as shown in Fig. 2.12. The output signal $y(t)$ of the switching branch is a chopped waveform with an envelope equal to the input signal $x(t)$, a pulse frequency equal to the switch frequency f_s, and a pulse width equal to T_{ON}.

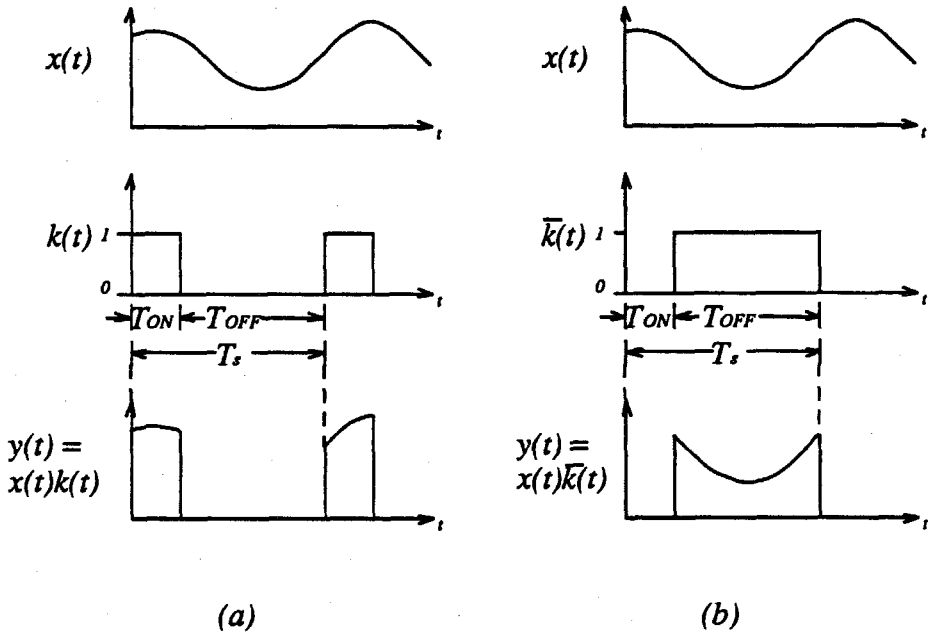


Figure 2.12: The Signal Flow of the Switching Branches. The input signal $x(t)$ is chopped by the switch function $k(t)$ and $\overline{k}(t)$. The effective signal carried in the output signal is $y(t)$. (a) The signal flow of the k-branch. (b) The signal flow of the $\overline{k}$-branch.

Assume that the small ripple condition is satisfied; therefore, the switch frequency is attenuated in the circuit. Also, assume that the signal frequency is much lower than the switch frequency. The effective signal carried at the k-branch output is equal to its

average value over a switch cycle:

$$y(t) = \frac{1}{T_s(t)} \int_0^{T_{ON}(t)} x(t)dt \tag{2.8}$$

$$\approx x(t)\frac{1}{T_s(t)} \int_0^{T_{ON}(t)} dt \tag{2.9}$$

$$= x(t)\frac{T_{ON}(t)}{T_s(t)} \tag{2.10}$$

$$= x(t)d(t) \tag{2.11}$$

Similarly for the $\overline{k}$-branch, the input signal $x(t)$, and output signal $y(t)$ have the relation:

$$y(t) = \frac{1}{T_s(t)} \int_{T_{ON}(t)}^{T_S(t)} x(t)dt \tag{2.12}$$

$$\approx x(t)\frac{1}{T_s(t)} \int_{T_{ON}(t)}^{T_s(t)} dt \tag{2.13}$$

$$= x(t)\frac{T_{OFF}(t)}{T_s(t)} \tag{2.14}$$

$$= x(t)d^{'}(t) \tag{2.15}$$

where $d(t)$ and $d'(t)$ are the averages of the switch functions $k(t)$ and $\overline{k}(t)$ respectively, and they represent the duty-ratio of the switch.

$$d(t) = \frac{T_{ON}(t)}{T_s(t)} \tag{2.16}$$

$$d^{'}(t) = \frac{T_{OFF}(t)}{T_s(t)} \tag{2.17}$$

$$d'(t) = 1 - d(t) \tag{2.18}$$

Switches are controlled by their duty-ratio function $d(t)$. The duty-ratio functions are found for the constant frequency switches, the constant ON-time switches, the constant OFF-time switches, and the variable switches:

$$d(t) = T_{ON}(t)f_s \qquad \text{for the constant frequency switches} \tag{2.19}$$

$$d(t) = T_{ON}f_s(t) \qquad \text{for the constant ON-time switches} \tag{2.20}$$

$$d(t) = 1 - T_{OFF}f_s(t) \qquad \text{for the constant OFF-time switches} \tag{2.21}$$

$$d(t) = T_{ON}(t) f_s(t) \qquad \text{for the variable switches} \qquad (2.22)$$

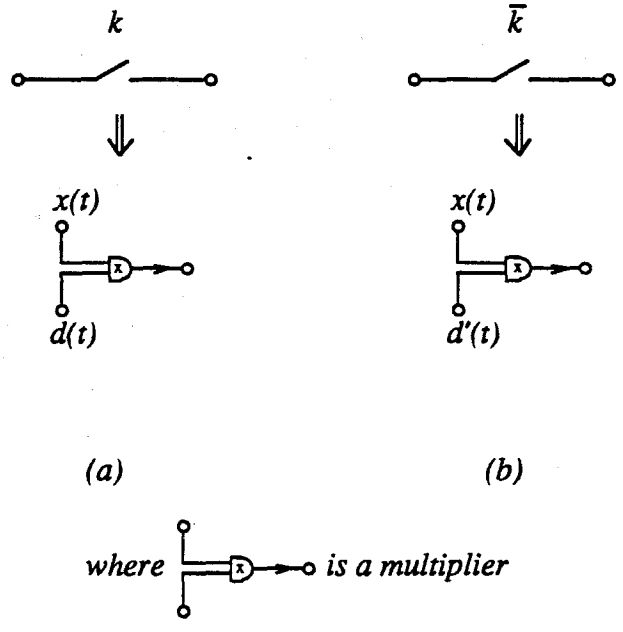


Figure 2.13: The large-signal Models of the Switching Branches. (a) The Large-signal model of the k-branch. (b) The Large-signal model of the $\overline{k}$-branch.

Equations (2.11) and (2.15) indicate that the output signal $y(t)$ from the switching branches is the product of the input signal $x(t)$ and the duty-ratio control signal $d(t)$ or $d'(t)$, thus it is directly affected by the input signal $x(t)$ and controlled by the duty-ratio $d(t)$ or $d'(t)$. Therefore, the large-signal models of the switching branches are represented by a single multiplier, as shown in Fig. 2.13. The large-signal model of a switching converter is obtained by replacing the switching branches with the large-signal models of the switching branches in the Switching Flow-Graph $\mathcal{G}$.

Large-signal models are necessary for studying the global dynamic behavior of the switching converter systems. Global knowledge makes it possible to design a switching converter system that operates in the desirable converging region of state space. Inside this desired converging region, the small-signal model can be employed to investigate the

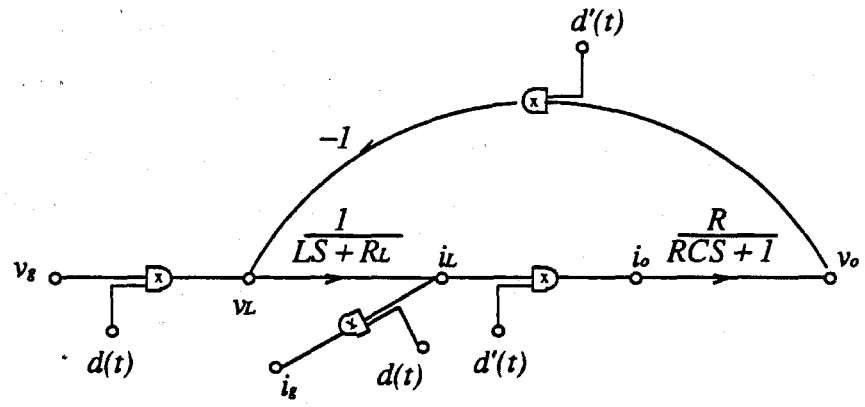


Figure 2.14: The Large-Signal Model of the Buckboost Converter. The large-signal model of the buckboost converter is obtained by replacing the switching branches with the large-signal models of the switching branches in the Switching Flow-Graph $\mathcal{G}$.

local frequency response for small-signals.

The large-signal model is shown in Fig. 2.14 for the same buckboost converter discussed in the previous section. The input to output large-signal response can be obtained by injecting a signal into node v_g, and observing the output at the node v_o. In addition, the input impedance can be determined by detecting the signal at node i_g. Injecting a signal into node $d(t)$ and detecting the output at node v_o generates the control to output large-signal-response. Injecting a signal into the node v_o, one can detect the signal at node i_o to get the output impedance.

It is very easy to obtain the global view of the dynamic behavior of the system by entering the model into a computer simulation program. From the study of the large-signal dynamic behavior, a desired stable operating region is found. Inside this region, the system can be linearized in the neighborhood of the operating point to obtain the small-signal frequency response.

2.5 Steady-State Model

The large-signal models of the k-branch and the $\overline{k}$-branch, derived in the previous section, can be modified to generate a steady-state model of the switching branches. Assume that the input signals and the duty-ratio control signals, $x(t)$, $d(t)$, and $d'(t)$, entering the switching branches are constant. That is:

$$x(t) = X \tag{2.23}$$

$$d(t) = D \tag{2.24}$$

$$d'(t) = D' \tag{2.25}$$

Then the output signal $y(t)$ of the switch is also constant:

$$y(t) = Y \tag{2.26}$$

Therefore, the switching branches degenerate to standard branches, as shown in Fig. 2.15. In the steady-state, the k-branch has only one input signal, X; the transmittance of the branch is D and the output signal is Y. Similarly, for the $\overline{k}$-branch, the input signal is X, the transmittance of the branch is D' and the output signal is Y.

Substitution of these steady-state models into the Switching Flow-Graph $\mathcal{G}$ of the switching converter for the switching branches and assuming $S \rightarrow 0$, immediately yields the steady-state model of the switching converter. The steady-state model of the buck-boost converter is shown in Fig. 2.16.

Relations between state variables, such as the input-to-output gain, the DC relations between the state variables, and the efficiency, etc., can be read directly off the steady-state flow-graph model.

$$\frac{V_o}{V_g} = \frac{D/D'}{1+\frac{R_L}{RD'^2}} \tag{2.27}$$

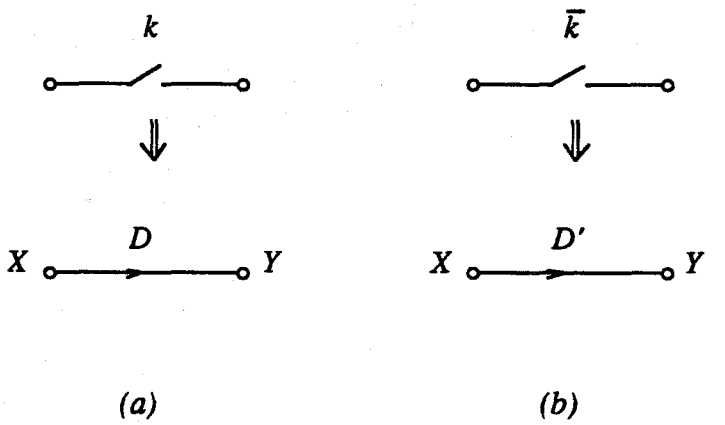


Figure 2.15: The Steady-State Models of the Switching Branches. (a) The steady-state model of the k-branch. (b) The steady-state model of the $\overline{k}$-branch.

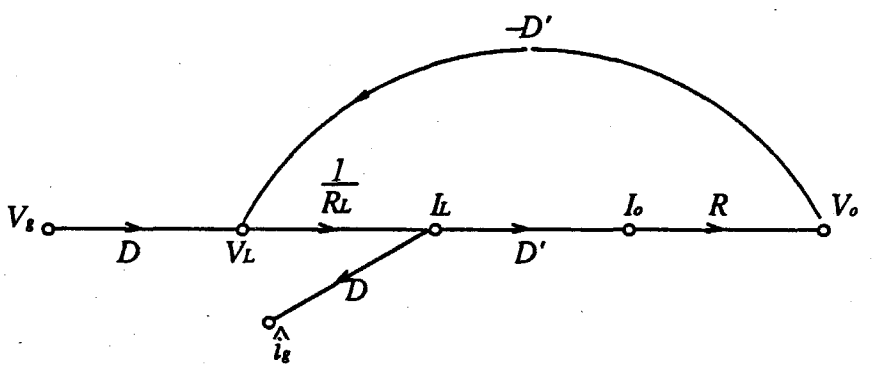


Figure 2.16: The Steady-State Model of the Buckboost Converter. Substitution of the steady-state models into the Switching Flow-Graph $\mathcal{G}$ of the buckboost converter for the switching branches and assuming $S \rightarrow 0$, immediately yields the steady-state model of the buckboost converter.

$$\frac{I_L}{V_g} = \frac{D}{R_L + D'^2 R} \tag{2.28}$$

$$\frac{I_C}{V_g} = \frac{DD'}{R_L + D'^2 R} \tag{2.29}$$

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}} \tag{2.30}$$

2.6 Small-Signal Model

For the k-branch and the $\overline{k}$-branch, in the large-signal environment, the input and output signals have the relationships:

$$y(t) = x(t)d(t) \qquad \text{for the } k\text{-branch} \tag{2.31}$$

$$y(t) = x(t)d'(t) \qquad \text{for the } \overline{k}\text{-branch} \tag{2.32}$$

Define the operating point by X, D and Y, and the associated small-signal perturbations by $\hat{x}(t)$, $\hat{d}(t)$, and $\hat{y}(t)$, where:

$$d(t) = D + \hat{d}(t) \tag{2.33}$$

$$d'(t) = D' - \hat{d}(t) \tag{2.34}$$

$$1 = D + D' \tag{2.35}$$

$$x(t) = X + \hat{x}(t) \tag{2.36}$$

$$y(t) = Y + \hat{y}(t) \tag{2.37}$$

Inserting Equations (2.33), (2.34), (2.36) and (2.37) into the large-signal switching branch relations (2.31) and (2.32), yields the equations for the small-signal perturbations.

$$\begin{aligned} Y + \hat{y}(t) &= (X + \hat{x}(t))(D + \hat{d}(t)) \\ &= XD + D\hat{x}(t) + X\hat{d}(t) + \hat{x}(t)\hat{d}(t) \end{aligned} \tag{2.38}$$

for the k-branch and

$$Y + \hat{y}(t) = (X + \hat{x}(t))(D' - \hat{d}(t))$$

$$= XD' + D'\hat{x}(t) - X\hat{d}(t) - \hat{x}(t)\hat{d}(t) \tag{2.39}$$

for the $\overline{k}$-branch.

At the operating point, the k-branch and the $\overline{k}$-branch satisfy:

$$Y = XD \qquad \text{for the } k\text{-branch} \tag{2.40}$$

$$Y = XD' \qquad \text{for the } \overline{k}\text{-branch} \tag{2.41}$$

Neglecting the second-order perturbations, yields the small-signal switching branch equations:

$$\hat{y}(t) = D\hat{x}(t) + X\hat{d}(t) \qquad \text{for the } k\text{-branch} \tag{2.42}$$

$$\hat{y}(t) = D'\hat{x}(t) - X\hat{d}(t) \qquad \text{for the } \overline{k}\text{-branch} \tag{2.43}$$

The small-signal models of the switching branches are shown in Fig. 2.17. Substitution

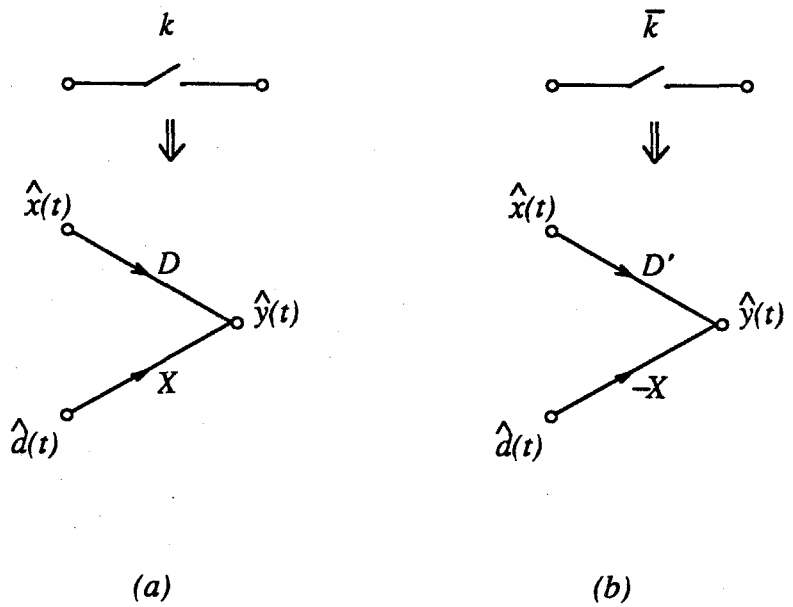


Figure 2.17: The Small-Signal Models of the Switching Branches. (a) The small-signal model of the k-branch. (b) The small-signal model of the $\overline{k}$-branch.

of the small-signal models for the switching branches in the Switching Flow-Graph immediately generates the small-signal model.

The small-signal dynamic model is shown in Fig. 2.18 for the same buckboost converter discussed in the last section. The small-signal model of the buckboost converter,

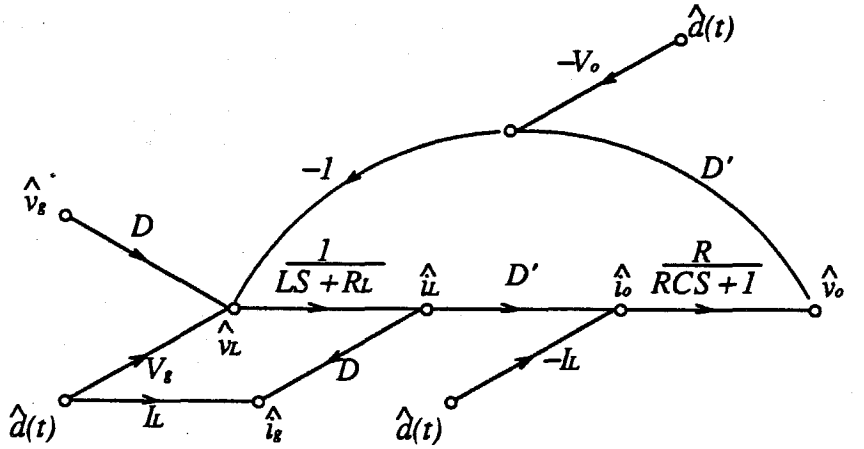


Figure 2.18: The Small-Signal Model of the Buckboost Converter. Substitution of the small-signal models for the switching branches in the Switching Flow-Graph of the buckboost converter, immediately generates the small-signal model.

shown in Fig. 2.18, can be further simplified to Fig. 2.19 using the flow-graph algebraic rules in Appendix A. The analytic forms of the transfer functions for the buckboost converter are easily obtained from Fig. 2.19.

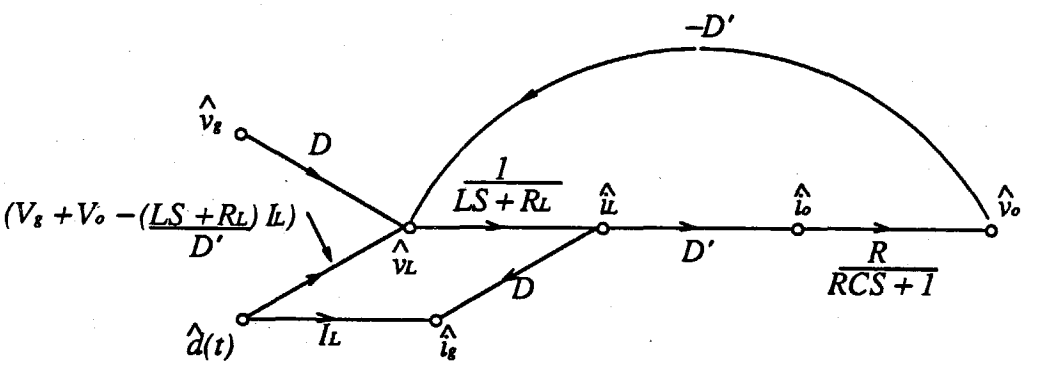


Figure 2.19: The Simplified Small-Signal Model of the Buckboost Converter. The small-signal model of the buckboost converter can be simplified using the flow-graph algebraic rules in Appendix A.

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_g + V_o - \frac{LS+R_L}{D'} I_L}{D'((1+\frac{R_L/R}{D'^2}) + \frac{R_L C + L/R}{D'^2} S + \frac{LC}{D'^2} S^2)} \tag{2.44}$$

$$\frac{\hat{v}_o}{\hat{v}_g} = \frac{\frac{D}{D'}}{(1+\frac{R_L/R}{D'^2}) + \frac{R_L C + L/R}{D'^2} S + \frac{LC}{D'^2} S^2} \tag{2.45}$$

The transfer function, shown in Equation (2.44), which represents the relationship between the small-signal control $\hat{d}(t)$ and the output $\hat{v}_o$, can be simplified using the steady-state relations of Equation (2.27) and (2.28).

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_g(1 + \frac{D(RD'-R_L/D')}{R_L+RD'^2} - \frac{LD/D'}{R_L+RD'^2} S)}{D'((1+\frac{R_L/R}{D'^2}) + \frac{R_L C + L/R}{D'^2} S + \frac{LC}{D'^2} S^2)} \tag{2.46}$$

The small-signal transfer functions, obtained using the Switching Flow-Graph technique, are the same as those obtained using the state-space averaging technique; however, the Switching Flow-Graph technique provides a more visible and faster way to obtain the small-signal models for switching converters. The Switching Flow-Graph models generate a more physical understanding of the signal processing in switching converters. For example, it is evident from Fig. 2.7 that a right-half-plane (RHP) zero exists in the control-to-output frequency response. The physical insight necessary to make this observation of the RHP zero is further discussed in Chapter. 4.

In addition, the Switching Flow-Graph facilitates the determination of the input and output impedances:

$$\begin{aligned} \hat{z}_{in} &= \frac{\hat{v}_g}{\hat{i}_g} \\ &= \frac{R\frac{D'^2}{D^2}((1+\frac{R_L/R}{D'^2}) + \frac{R_L C + L/R}{D'^2} S + \frac{LC}{D'^2} S^2)}{1 + RCS} \end{aligned} \tag{2.47}$$

$$\begin{aligned} \hat{z}_{out} &= \frac{\hat{v}_o}{\hat{i}_R|_{v_g=0}} \\ &= \frac{R_L(1+\frac{L}{R_L}S)}{D'^2((1+\frac{R_L/R}{D'^2}) + \frac{R_L C + L/R}{D'^2} S + \frac{LC}{D'^2} S^2)} \end{aligned} \tag{2.48}$$

2.7 Extra-Element Theory of the Flow-Graph

The extra-element theory [12] can be applied to the flow-graph and the Switching Flow-Graph. Suppose $\mathcal{B}_i$ is i-th branch of the Switching Flow-Graph $\mathcal{G}$. The branch $\mathcal{B}_i$ represents an electrical element Z_i of the original circuit. If an extra-element Z_E is to be inserted into the original circuit in parallel with the element Z_B, as shown in Fig. 2.20, then the extra-element $Z_E = 1/C_E S$ shares the current with the original element Z_B. Therefore, Z_d and Z_n can be determined by injecting a current signal into the current node of branch $\mathcal{B}_i$ and detecting the voltage at the voltage node of branch $\mathcal{B}_i$, as shown in Fig. 2.20. Let $v_g = 0$, $v_o = v_R$,

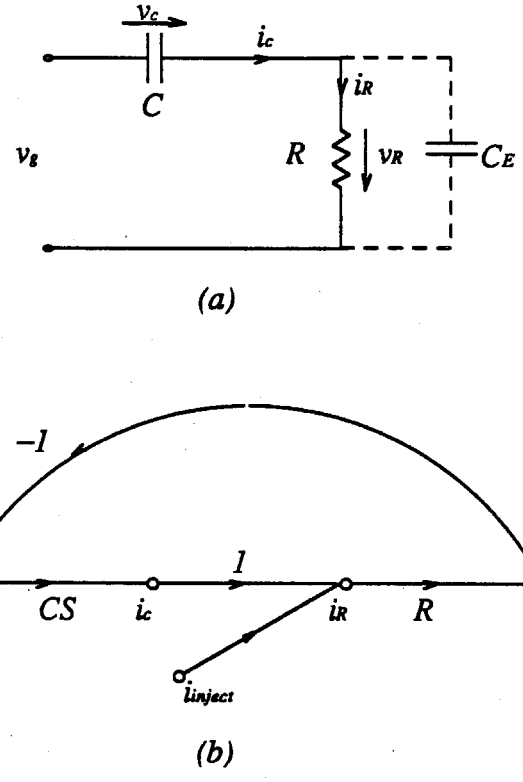


Figure 2.20: The Parallel Extra-Element. Z_d and Z_n can be determined by injecting a current signal into the current node of branch $\mathcal{B}_i$ and detecting the voltage at the voltage node of branch $\mathcal{B}_i$.

$$Z_d = \frac{v_{test}}{i_{inject}}|_{v_g=0} \tag{2.49}$$

$$= \frac{R}{1+RCS}. \tag{2.50}$$

Adjust i_{inject} such that $v_o = 0$,

$$Z_n = \frac{v_{test}}{i_{inject}}|_{v_0=0} \tag{2.51}$$

$$= 0. \tag{2.52}$$

The gain $\frac{v_o}{v_g}$ with the extra-element Z_E is:

$$\frac{v_o}{v_g}|_{Z_E} = \frac{v_o}{v_g}|_{Z_E=\infty} \frac{1+\frac{Z_n}{Z_E}}{1+\frac{Z_d}{Z_E}} \tag{2.53}$$

$$= \frac{RCS}{1+R(C+C_E)S}. \tag{2.54}$$

If an extra-element Z_E is inserted into the circuit in series with the element Z_B, as shown in Fig. 2.21, then the extra element $Z_E = L_E S$ shares the voltage with the original element Z_B. Therefore, Z_d and Z_n can be determined by injecting a voltage signal in to the current node of branch $\mathcal{B}_i$, and detecting the current at the current node of branch $\mathcal{B}_i$, as shown in Fig. 2.21. Let $v_g = 0$ and $v_o = v_R$,

$$Z_d = \frac{v_{inject}}{i_{test}}|_{v_g=0} \tag{2.55}$$

$$= \frac{1+RCS}{CS}. \tag{2.56}$$

Adjust i_{inject} such that $v_o = 0$,

$$Z_n = \frac{v_{inject}}{i_{test}}|_{v_0=0} \tag{2.57}$$

$$= \infty. \tag{2.58}$$

The gain $\frac{v_o}{v_g}$ with the extra-element Z_E is:

$$\frac{v_o}{v_g}|_{Z_E} = \frac{v_o}{v_g}|_{Z_E=0} \frac{1+\frac{Z_E}{Z_n}}{1+\frac{Z_E}{Z_d}} \tag{2.59}$$

$$= \frac{RCS}{1+RCS+L_E CS^2}. \tag{2.60}$$

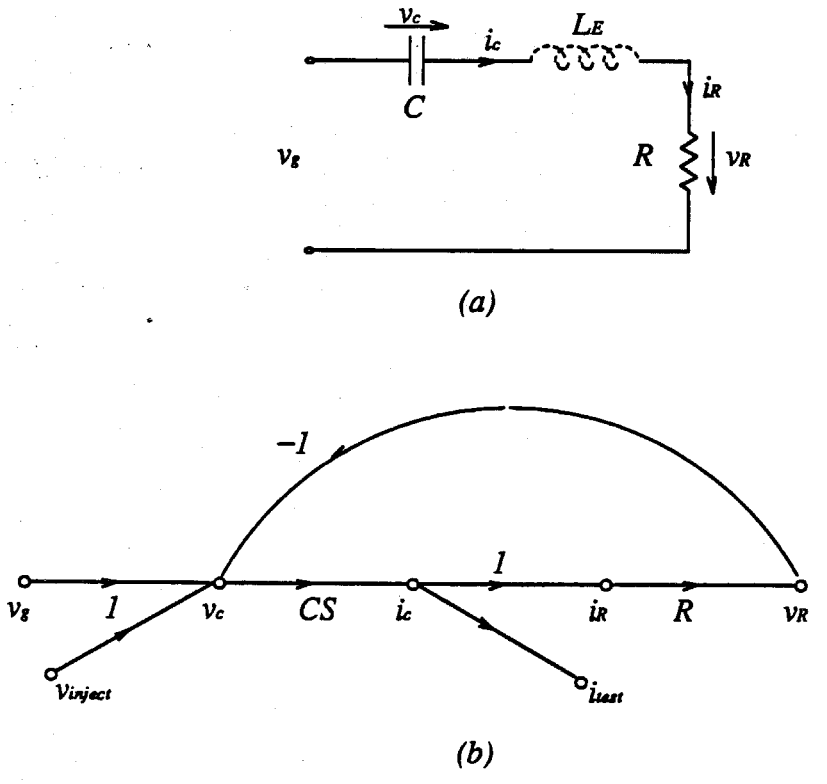


Figure 2.21: The Series Extra-Element. Z_d and Z_n can be determined by injecting a voltage signal into the voltage node of branch $\mathcal{B}_i$, and detecting the current at the current node of branch $\mathcal{B}_i$.

For simple circuits such as those shown in Fig. 2.20 and Fig. 2.21, there is not much advantage in using the extra-element theory. However, the extra-element theory is of tremendous help when the circuit is very complicated.

2.8 Summary

The Switching Flow-Graph technique is an easily implemented graphic modelling tool for switching converter design and analysis. This technique provides a large-signal model, a small-signal model, and a steady-state model. The large-signal model gives a global view of the switching converter, thus it can be used to find the convergent operating

region and to design a converter that operates in a desired region. The steady-state model yields the steady-state relations, which are useful in determining the efficiency and other steady-state properties of switching converters. The small-signal model gives the transfer functions from one arbitrary state variable to another arbitrary state variable, such as the input-to-output gain, the control-to-output gain, the input and output impedances, etc. The Switching Flow-Graph is a graphic realization of the circuit that contains all the information about the circuit, provides physical insight into the operation of the circuit and is very easy to obtain.

Chapter 3

Modelling Pulse-Width-Modulated Switching Converters

The Switching Flow-Graph technique is applied to model the most commonly used pulsed-width-modulated (PWM) converters in the second-order family in Section 3.1 and the fourth-order family in Section 3.2. The algebraic rules, outlined in Appendix A, are employed to simplify the small-signal Switching Flow-Graphs in Section 3.3. Experiments, described in Section 3.4, were conducted to verify both the large-signal and the small-signal models.

3.1 Modelling Second-Order PWM Switching Converters

The Switching Flow-Graph technique is used to study the dynamic behavior of standard second-order PWM converters, such as the buck converter, the boost converter, and the buckboost converter, shown in Fig. 3.1. L is the inductor, C is the capacitor, and R is the load resistor. A transistor and a diode are employed to implement the switch S. When the transistor is ON the diode is OFF and when the transistor is OFF the diode is ON. Define v_g, v_L, v_o as the input voltage, the inductor voltage, and the output voltage, respectively. Assume that the input current i_g, the inductor current i_L, and the output current $i_o = i_C + i_R$ are in the same direction as v_g, v_L, and v_o.

The Switching Flow-Graphs, shown in Fig. 3.2, for the buck converter, the boost

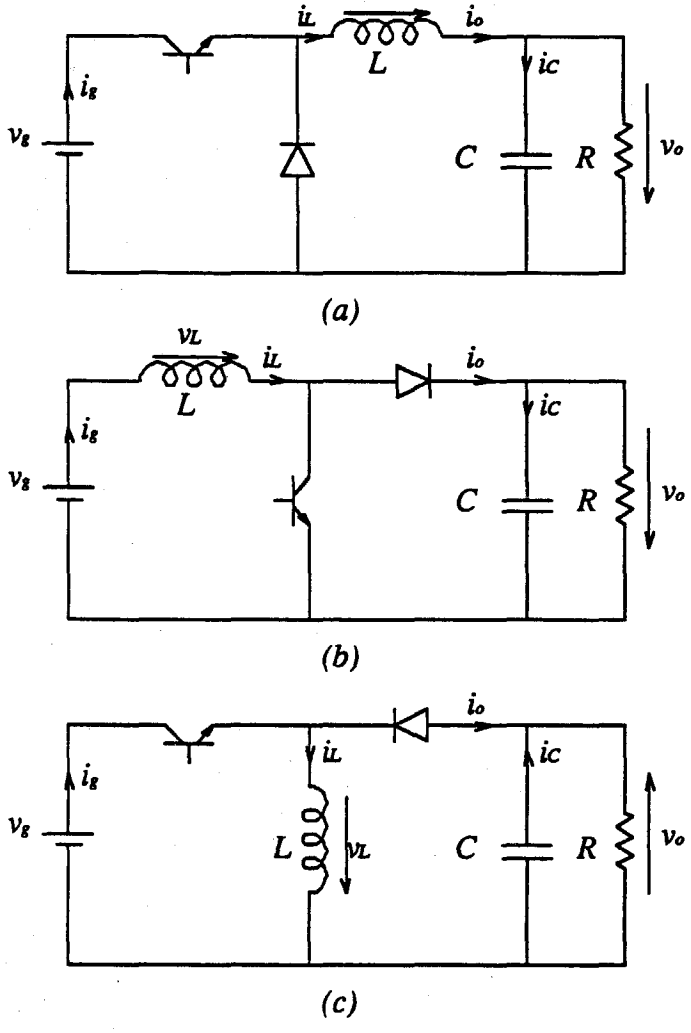


Figure 3.1: The Basic Second-Order PWM Converter. (a) The buck converter. (b) The boost converter. (c) The buckboost converter.

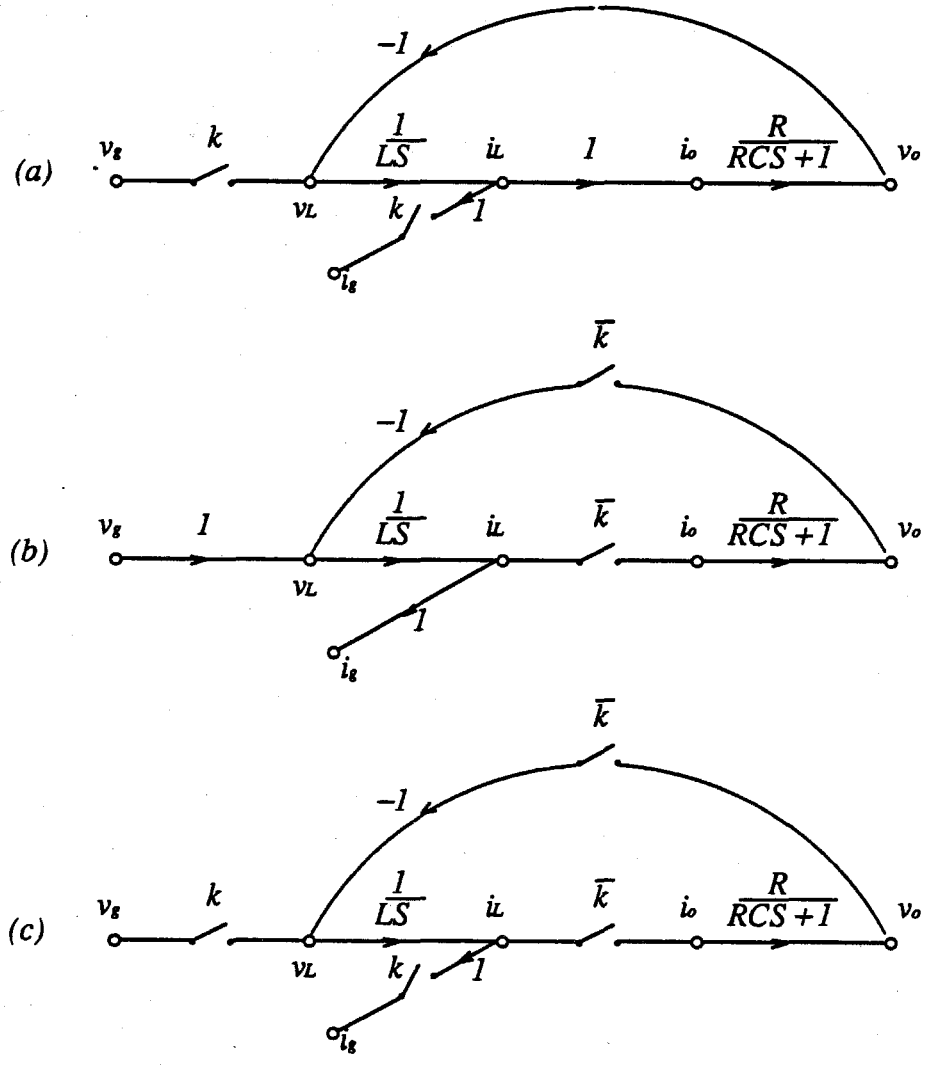


Figure 3.2: The Switching Flow-Graphs of the Second-Order PWM Converters. The Switching Flow-Graph for the buck converter (a), the boost converter (b), and the buckboost converter (c).

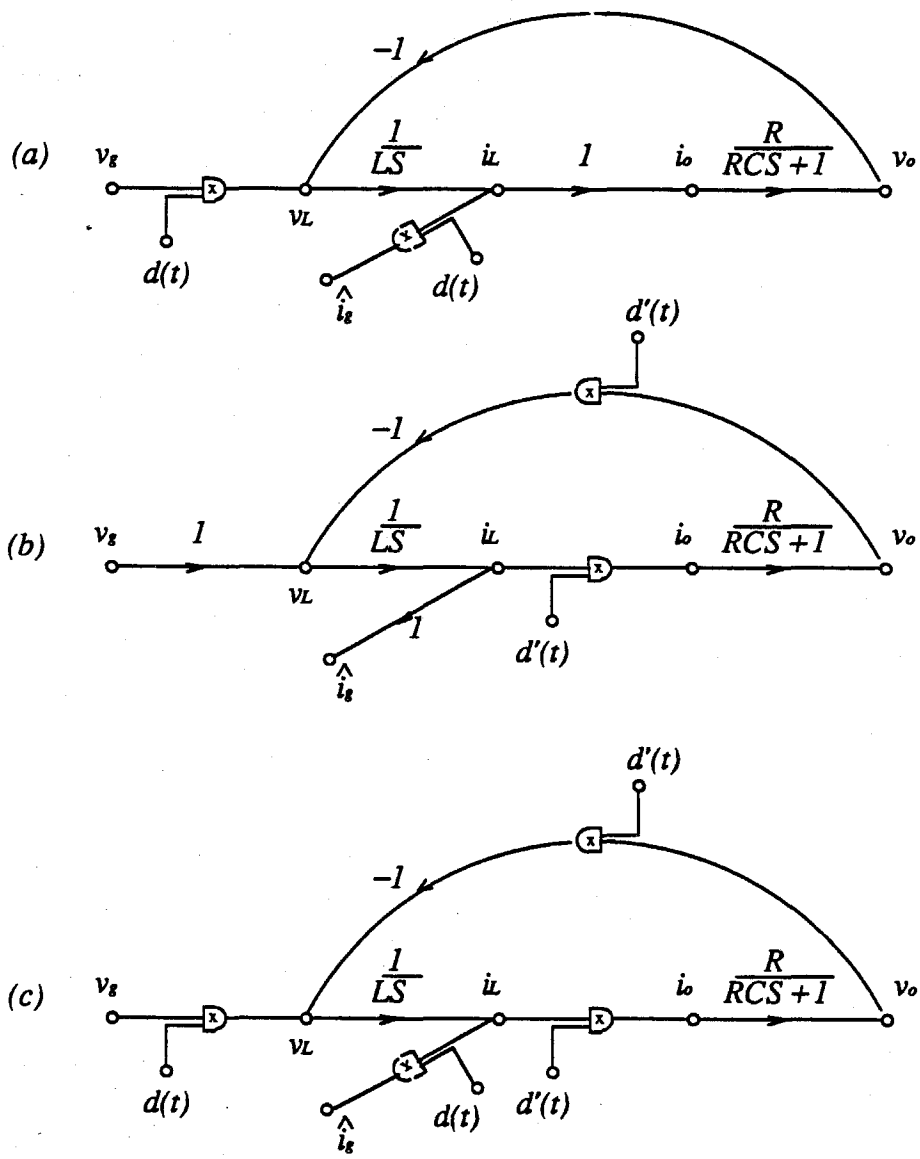


Figure 3.3: The Large-Signal Models of the Second-Order PWM Converters. The large-signal model for the buck converter (a), the boost converter (b), and the buckboost converter (c).

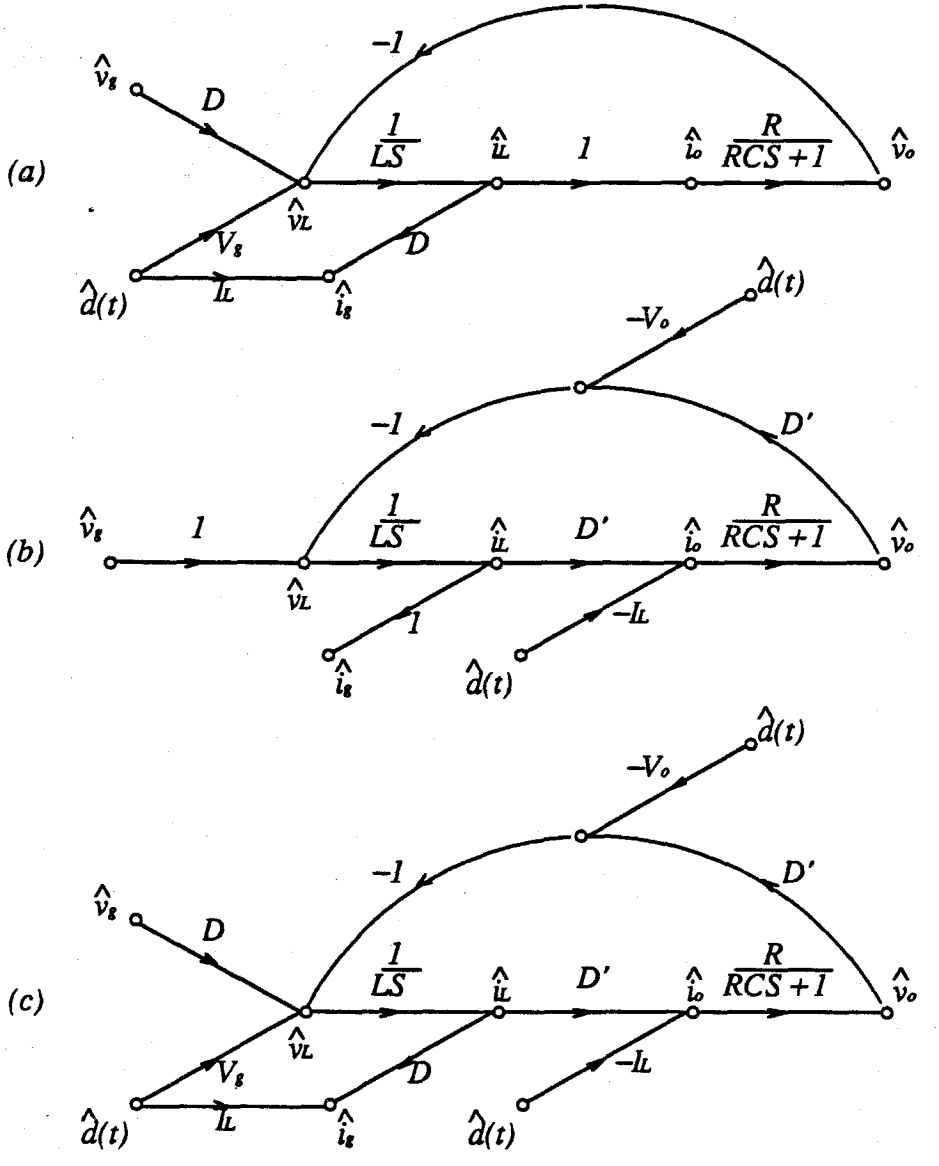


Figure 3.4: The Small-Signal Models of the Second-Order PWM Converters. The small-signal model for the buck converter (a), the boost converter (b), and the buckboost converter (c).

converter, and the buckboost converter are very similar. The Switching Flow-Graphs exhibit an interesting regularity. The k-branches appear in pairs and the $\overline{k}$-branches appear in pairs. In all cases, one switching branch of a given pair is in the voltage path, while the other is in the current path. The buck converter has only one pair of k-branches, the boost converter has only one pair of $\overline{k}$-branches, and the buckboost converter has both a k-branch pair and a $\overline{k}$-branch pair.

The large-signal models are shown in Fig. 3.3. Relations between the various state variables are obtained by simulation. The small-signal models are shown in Fig. 3.4. Small-signal transfer functions between state variables are read directly from the small-signal Switching Flow-Graph. Fig. 3.4 also indicates that the duty-ratio signal $\hat{d}$ injected into the current path has a negative effect on the output voltage $\hat{v}_o$. This negative effect raises the problem of right-half-plane (RHP) zeros that is discussed in Chapter 4.

3.2 Modelling Fourth-Order PWM Converters

The Switching Flow-Graph technique is also well suited for the study of the dynamic behavior of fourth-order systems, such as the buck converter with input filter, the d^2 converter, the Ćuk converter, and the Lambda converter, as shown in Fig. 3.5. L_1 and L_2 are the input and output inductors, C_1 and C_2 are the input and output capacitors, and R is the load resistor. In each circuit, a transistor and one or more diode(s) are used to implement the switch S. When the transistor is ON, diode "1"s are ON and diode "0"s are OFF. When the transistor is OFF, diode "1"s are OFF and diode "0"s are ON. Define v_g as the input voltage, v_{L1} and v_{L2} as the voltages across L_1 and L_2, v_{C1} as the voltage across C_1, and v_o as the output voltage. Define i_g as the input current, i_{L1} and i_{L2} as the currents through L_1 and L_2, i_{C1} as the current through C_1, and $i_o = i_{L2} = i_R + i_{C2}$ as the output current. All currents flow in the same direction as

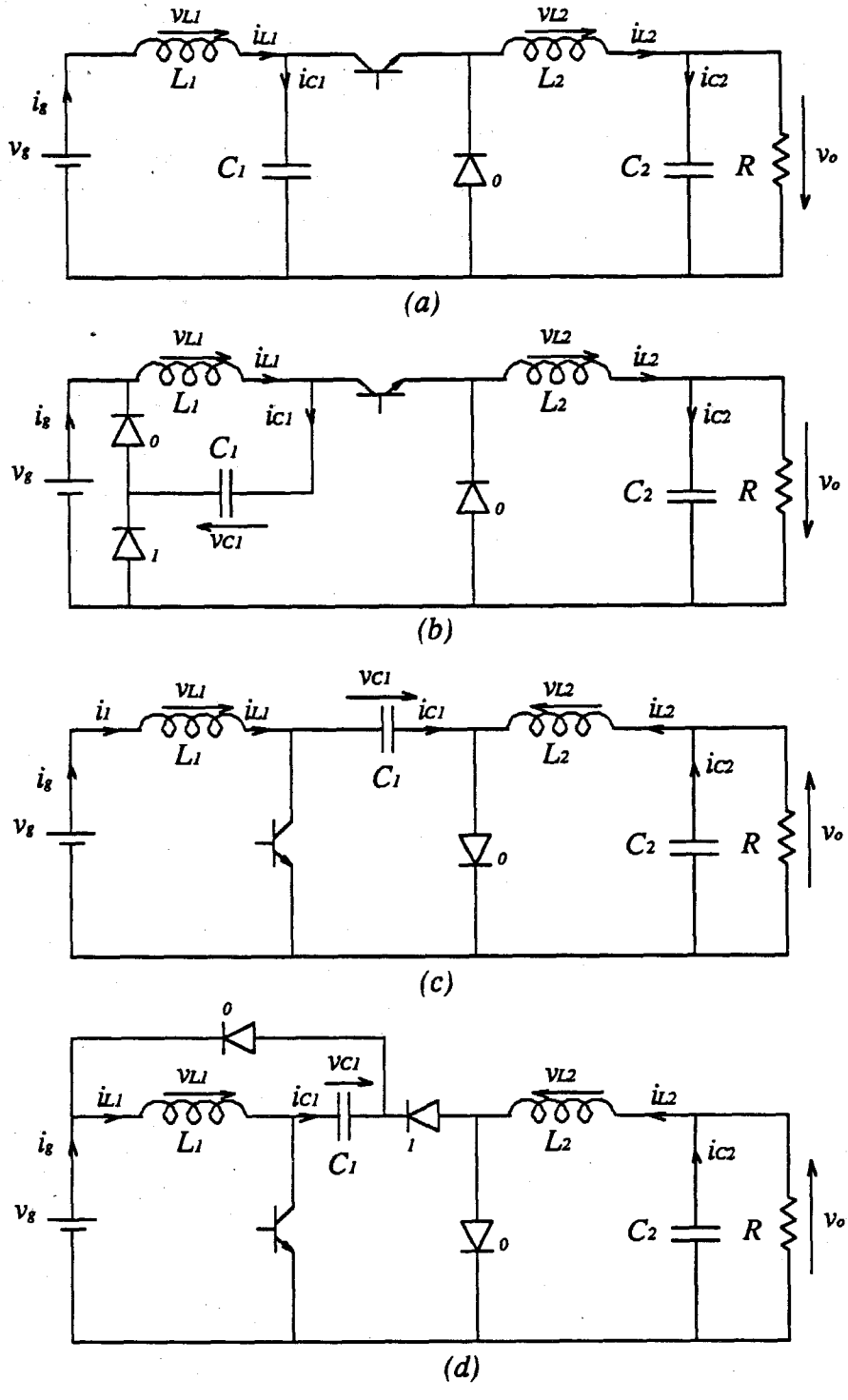


Figure 3.5: The Fourth-Order PWM Converters. (a) The buck converter with input filter. (b) The d^2 converter. (c) The Ćuk converter. (d) The Lambda converter.

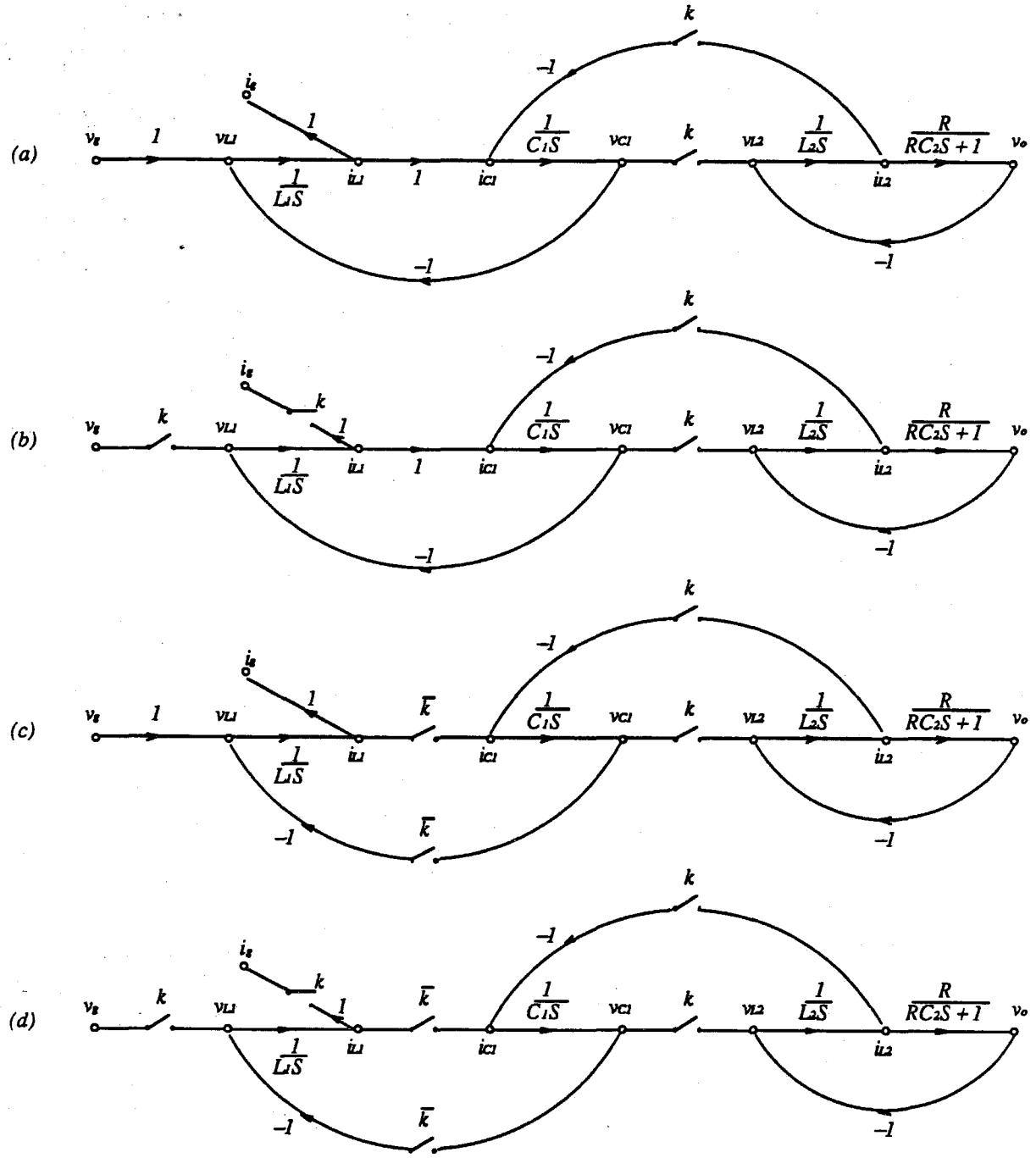


Figure 3.6: The Switching Flow-Graphs of the Fourth-Order PWM Converters. The Switching Flow-Graph for the buck converter with input filter (a), the d^2 converter (b), the Ćuk converter (c), and the Lambda converter (d).

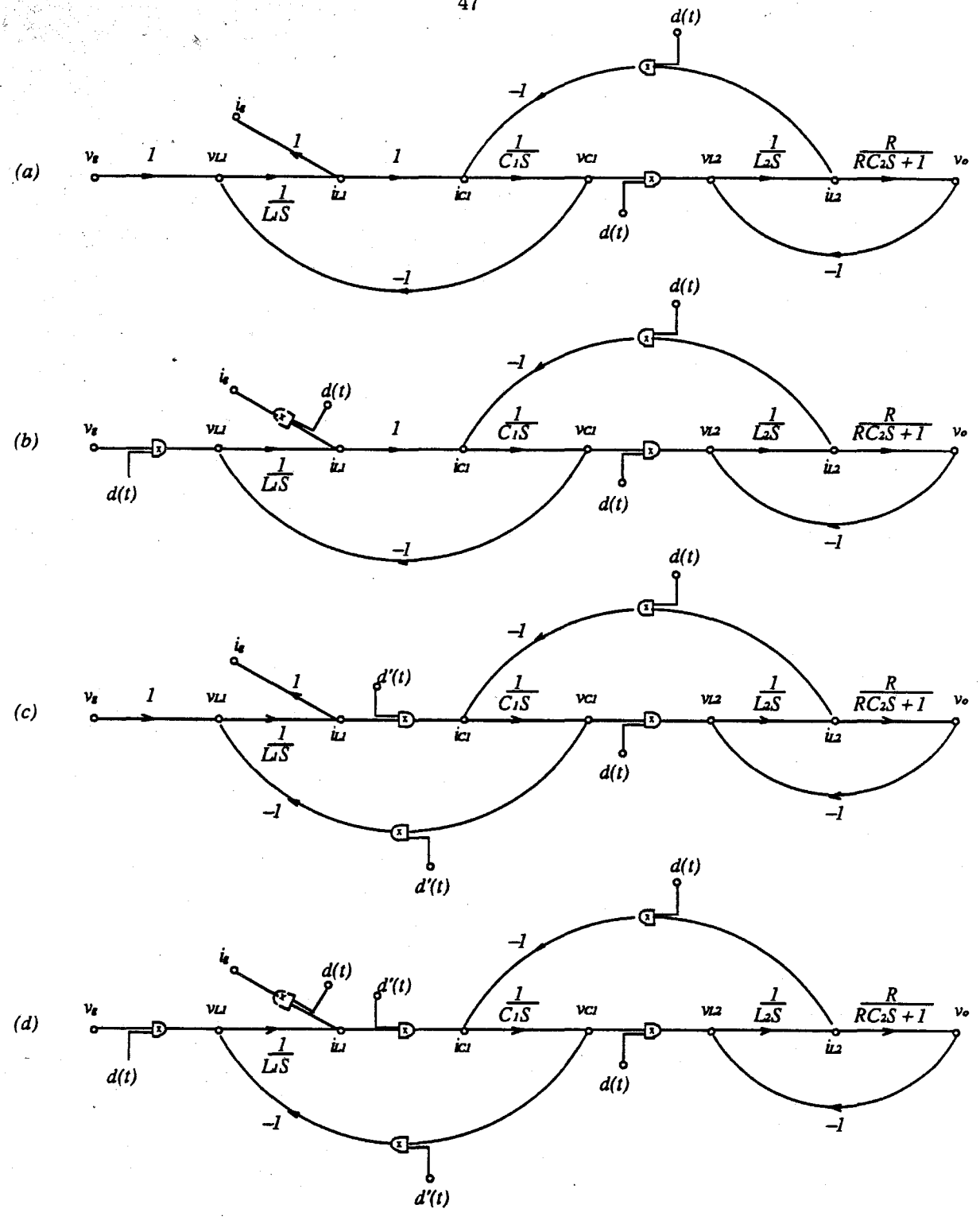


Figure 3.7: The Large-Signal Models of the Fourth-Order PWM Converters. The large-signal model for the buck converter with input filter (a), the d^2 converter (b), the Ćuk converter (c), and the Lambda converter (d).

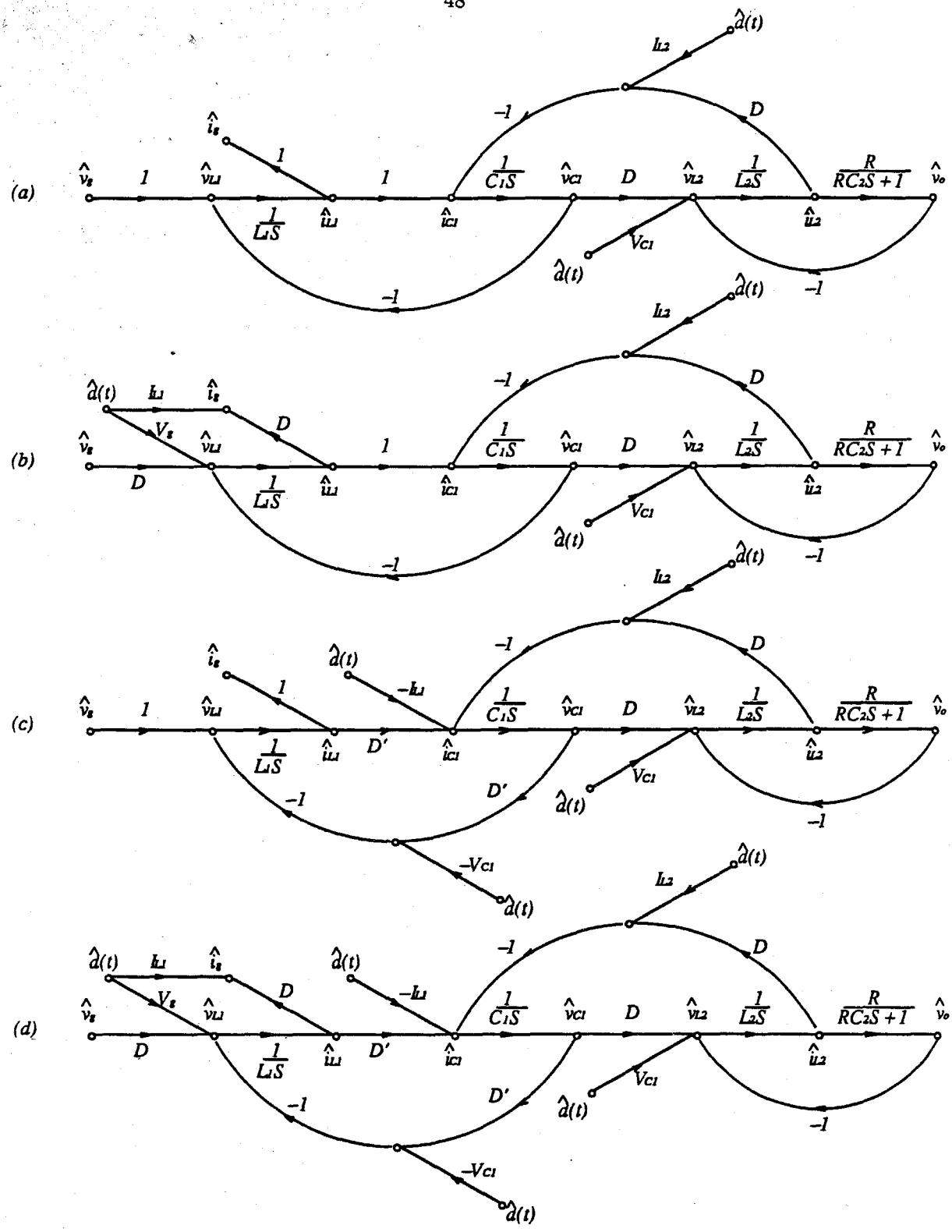


Figure 3.8: The Small-Signal Models of the Fourth-Order PWM Converters. The small-signal model for the buck converter with input filter (a), the d^2 converter (b), the Ćuk converter (c), and the Lambda converter (d).

their associated voltages.

The Switching Flow-Graphs obtained for the fourth-order converters are shown in Fig. 3.6. The Switching Flow-Graphs illustrate the same regular pattern as seen in the second-order converters. The k-branches appear in pairs, and the $\overline{k}$-branches appear in pairs. In all cases, one switching branch of a given pair is in the voltage path and the other is in the current path. A loop contains at most one type of switching branch. If a loop has switching branches, it always has two, one in the forward path and the other in the feedback path. If two adjacent loops both have switching branches, they have different types. Converters with DC gain $\frac{D^m}{D^n}$ have m pairs of k-branches and n pairs of $\overline{k}$-branches in their Switching Flow-Graphs.

The large-signal models in Fig. 3.7 and the small-signal models in Fig. 3.8 are given to demonstrate the ease with which this Switching Flow-Graph technique can be applied to generate deeper insight into the operation of PWM converters.

3.3 Simplification of the Small-Signal Switching Flow-Graphs

The Switching Flow-Graph small-signal models are linear. Hence all the linear flow-graph reducing techniques are applicable, such as the Flow-Graph algebraic rules, shown in Appendix A, the Mason Formula, etc. The algebraic rules are visual; therefore, they are more straightforward. The algebraic rules are used here to simplify the Switching Flow-Graph small-signal models, shown in Fig. 3.4 and Fig. 3.8 to obtain the input-to-output, the control-to-output transfer functions.

To demonstrate the procedure, the buck converter with input filter in the fourth-order family, as shown in Fig. 3.8(a), is used as an example. First, label all the $\hat{d}(t)$ control branches, as shown in Fig. 3.9(a). Second, move all the $\hat{d}(t)$ control branches to one node, for example the $\hat{v}_{L1}$ node. Branch #1 must be moved forward to node $\hat{i}_{C1}$

and then backward along the Switching Flow-Graph path from node $\hat{i}_{C1}$ to node $\hat{v}_{L1}$; therefore, the transmittance of Branch #1 is changed after the move. According to the algebraic rules, a factor of $-\frac{1}{L_1 S}$, which is the total gain of the path to be crossed, must be divided into the original transmittance. The transmittance of Branch #1 becomes $-I_{L2}L_1S$. In order to move Branch #2 to node V_{L1}, it must cross a local loop that has a gain $\frac{D}{1+C_1L_1S^2}$. Therefore the transmittance of Branch #2 becomes $V_{C1}\frac{1+C_1L_1S^2}{D}$. By superposition, Branch #1 and #2 can be combined into one branch with a transmittance N_d, as shown in fig. 3.9(b).

$$N_d = V_{C1}\frac{1+C_1L_1S^2}{D} - I_{L2}L_1S \tag{3.1}$$

The third step in the simplification involves reshaping of the $\hat{i}_{L2}$ feedback branch. Move the feedback point from node $\hat{i}_{L2}$ to node $\hat{v}_o$, and move the injection point from node $\hat{i}_{C1}$ to node $\hat{v}_{L1}$, that yields a feedback transmittance of $-\frac{DL_1}{R}S(1+RC_2S)$, as shown in Fig. 3.9(c). Last, reshape the two local feedback loops. The left loop is reduced to a branch with transmittance $\frac{1}{1+C_1L_1S^2}$, and the right loop is reduced to a branch with transmittance $\frac{1}{1+\frac{L_2}{R}S+L_2C_2S^2}$, as shown in Fig. 3.9(d).

The input-to-output transfer function and the control-to-output transfer function of the buck converter with input filter are read from Fig. 3.9(d).

$$\frac{\hat{v}_o}{\hat{v}_g} \approx \frac{D}{(1+\frac{D^2L_1}{R}S+\frac{1}{L_1C_1}S^2)(1+\frac{L_2}{R}S+\frac{1}{L_2C_2}S^2)} \tag{3.2}$$

$$= \frac{K_g}{(1+\frac{1}{Q_1\omega_1}S+\frac{1}{\omega_1^2}S^2)(1+\frac{1}{Q_2\omega_2}S+\frac{1}{\omega_2^2}S^2)} \tag{3.3}$$

$$\frac{\hat{v}_o}{\hat{d}} \approx \frac{V_g(1-\frac{D^2L_1}{R}S+L_1C_1S^2)}{(1+\frac{D^2L_1}{R}S+\frac{1}{L_1C_1}S^2)(1+\frac{L_2}{R}S+\frac{1}{L_2C_2}S^2)} \tag{3.4}$$

$$= \frac{K_d(1+\frac{1}{Q_0\omega_0}S+\frac{1}{\omega_0^2}S^2)}{(1+\frac{1}{Q_1\omega_1}S+\frac{1}{\omega_1^2}S^2)(1+\frac{1}{Q_2\omega_2}S+\frac{1}{\omega_2^2}S^2)} \tag{3.5}$$

where

$$K_g = D \tag{3.6}$$

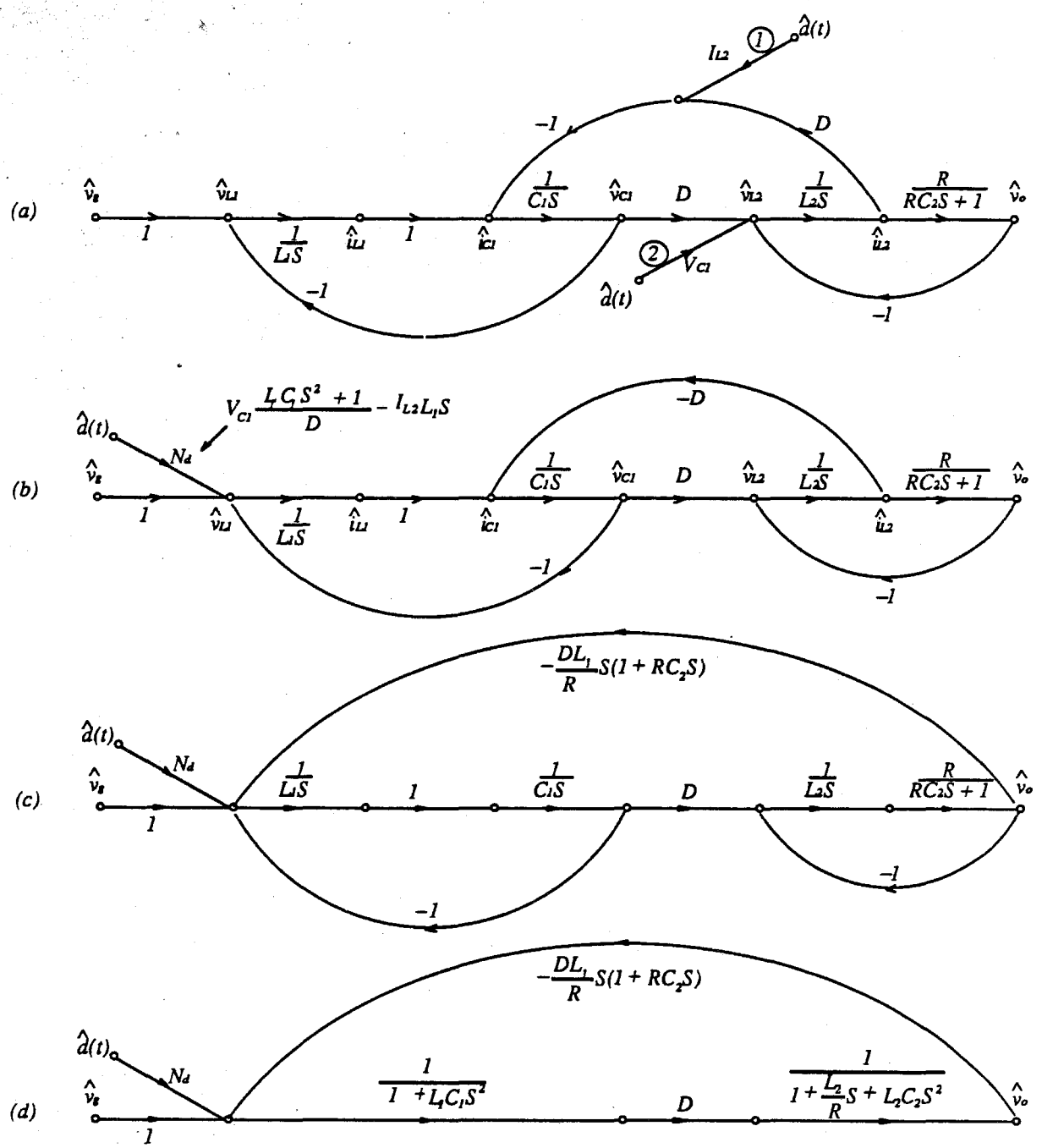


Figure 3.9: Reduce the Switching Flow-Graph of the Buck Converter with Input Filter. (a) The original Switching Flow-Graph of the Buck Converter with Input Filter. (b) Move all $d(t)$ control branch to one node. (c) Reshape the i_{L2} feedback branch. (d) Reduce two local feedback loops.

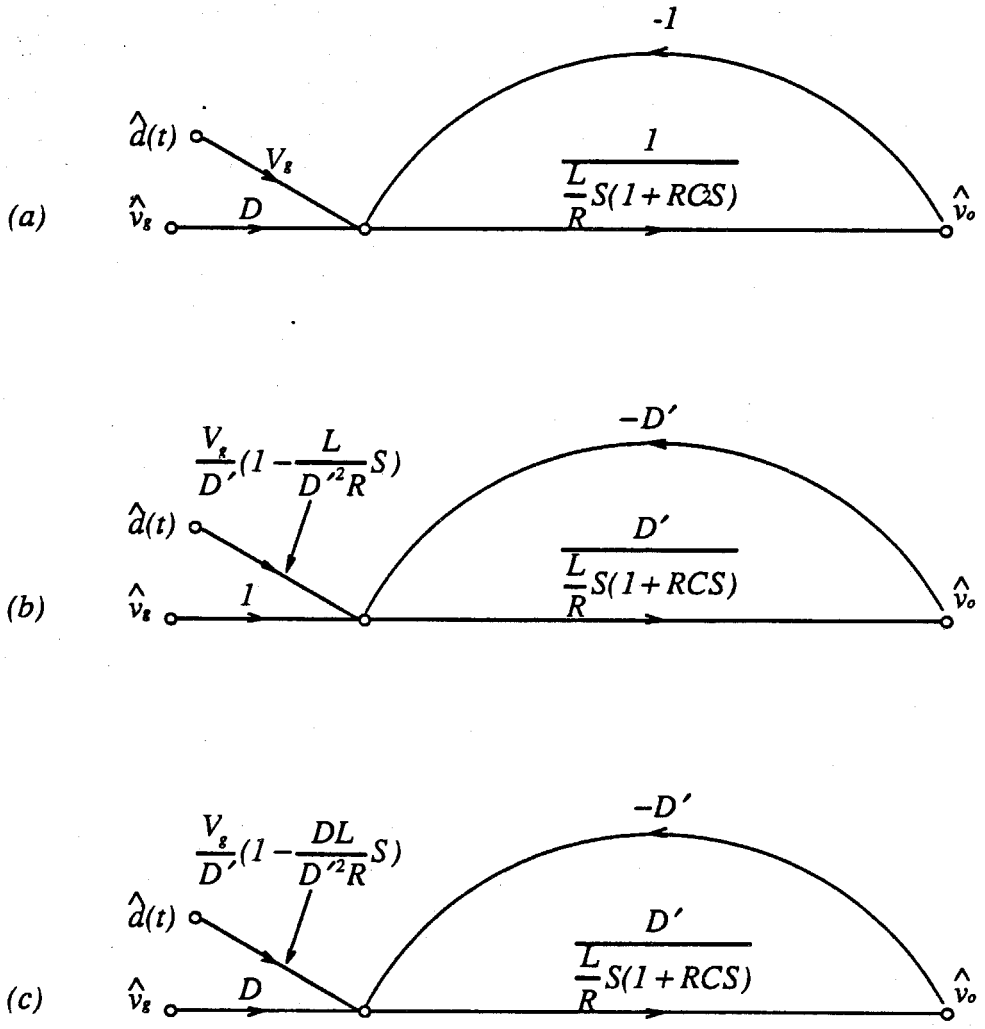


Figure 3.10: The Small-Signal Transfer Functions of the Second-Order PWM Converters. The small-signal transfer function for the buck converter (a), the boost converter (b), and the buckboost converter (c).

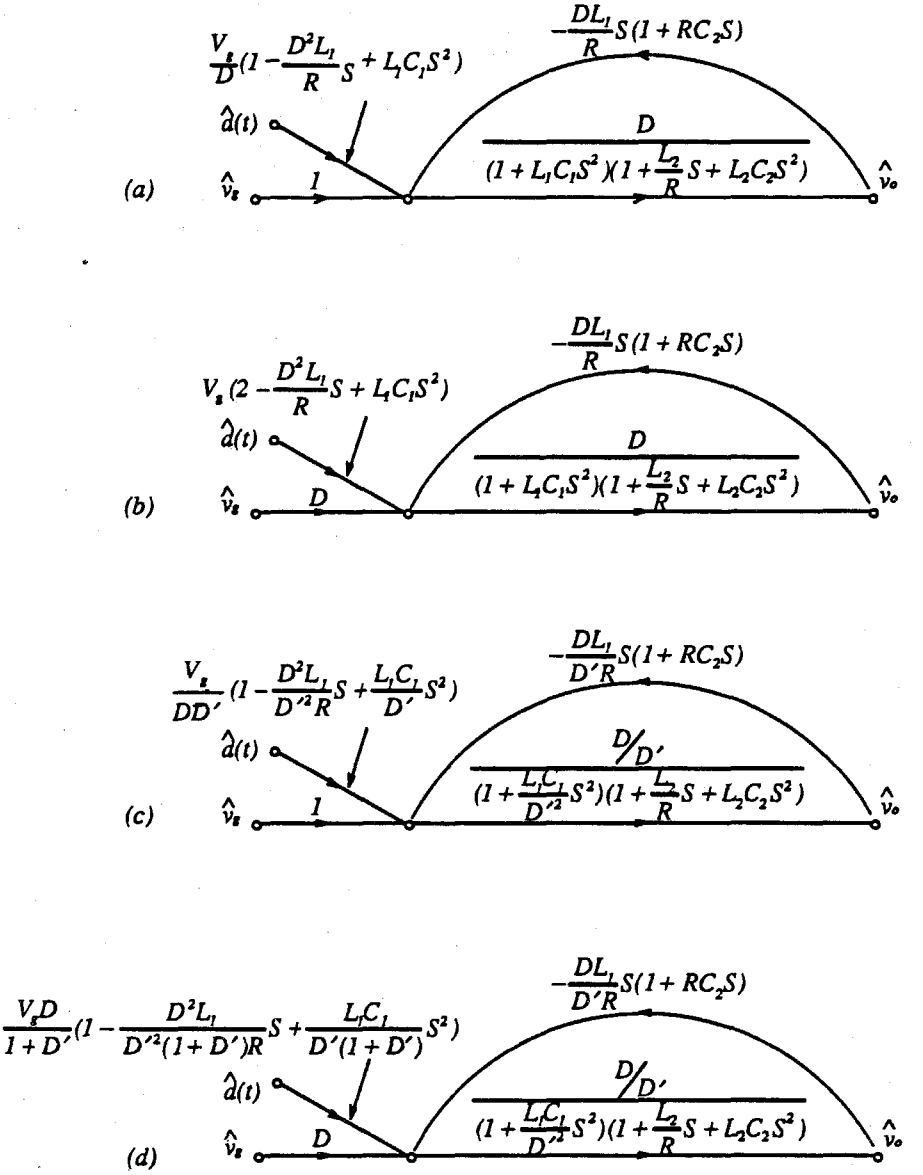


Figure 3.11: The Small-Signal Transfer Functions of the Fourth-Order PWM Converters. The small-signal transfer function for the buck converter with input filter (a), the d^2 converter (b), the Ćuk converter (c), and the Lambda converter (d).

$$K_d = V_g \tag{3.7}$$

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{3.8}$$

$$Q_0 = -\frac{R}{D^2}\sqrt{\frac{C_1}{L_1}} \tag{3.9}$$

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}} \tag{3.10}$$

$$Q_1 = \frac{R}{D^2}\sqrt{\frac{C_1}{L_1}} \tag{3.11}$$

$$\omega_2 = \frac{1}{\sqrt{L_2 C_2}} \tag{3.12}$$

$$Q_2 = R\sqrt{\frac{C_2}{L_2}} \tag{3.13}$$

Since $Q_0 > 0.5$, the duty-ratio d to output voltage v_o transfer function of the buck converter with input filter has a pair of RHP zeros:

$$\mathcal{N}(S) = 1 - \frac{D^2 L_1}{R} S + L_1 C_1 S^2 \tag{3.14}$$

The output filter of the buck converter has no effect on the RHP zeros, while the input inductor L_1, the energy transfer capacitor C_1, and the load R actually determine the RHP zeros.

The transfer functions are also found for the buck converter, the boost converter and the buckboost converter in the second-order family, the d^2 converter, the Ćuk converter, and the lambda converter in the fourth-order family, using the same simplification technique. The simplified small-signal models are given in Fig. 3.10 and Fig. 3.11. The small-signal models show that all the converters, except the basic buck converter, have RHP zeros. The RHP zero problem is discussed further in Chapter 4.

3.4 Experimental Verification

The Switching Flow-Graph large-signal models and small-signal models were obtained in Section 3.3 for the second-order family and the fourth-order family. Do these models

predict the dynamic behavior of the real converters? Experiments were conducted to verify the models; the results are discussed below.

3.4.1 The Experimental Circuit

The simplest converter, the basic buck converter, does not have RHP zeros and it is a second-order system, as shown in Section 3.1. Therefore, it should always be stable. In practice, however, a buck converter may oscillate when a feedback loop is applied. The oscillation is due to the fact that the input power source is usually obtained from rectified line power with an output filter. The output filter of the input voltage source is equivalent to the input filter of the buck converter. The buck converter with input filter is a fourth-order converter with two RHP zeros, as predicted in Section 3.2. A fourth-order converter with two RHP zeros is difficult to stabilize when the loop is closed. The buck converter with an input filter, as shown in Fig. 3.12, was chosen for the experiment.

3.4.2 The Large-Signal Model

The large-signal model for the buck converter with input filter, shown in Fig. 3.12, is shown in Fig. 3.13. To verify the large-signal model, the results obtained from computer simulations were compared to the results obtained from experiments. The commercially available simulation program, TUTSIM, is flow-graph oriented. The large-signal model, as shown in Fig. 3.13, can be entered directly to the TUTSIM simulation program. Users specify the transmittance and the inputs for each branch, define the injecting function of the duty-ratio, and give the initial condition, the simulation step size and the starting and stopping time. The file to simulate the step response is shown in Fig. 3.14.

The circuit parameters are as follows: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

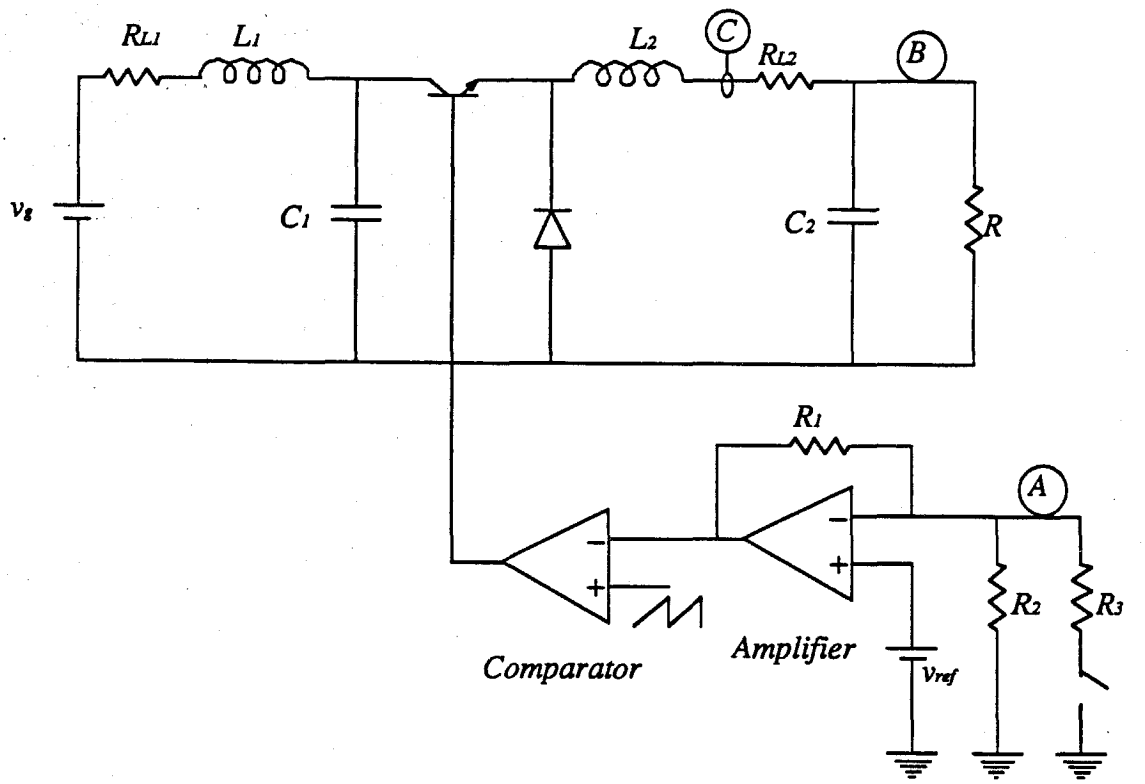


Figure 3.12: The Experimental Buck Converter with an Input Filter. The experimental circuit contains the power stage and the modulator. An electronic switch is used for injecting the step exciting signals. Point A is the signal injecting point, Point B and Point C are test points for v_o and i_{L2}.

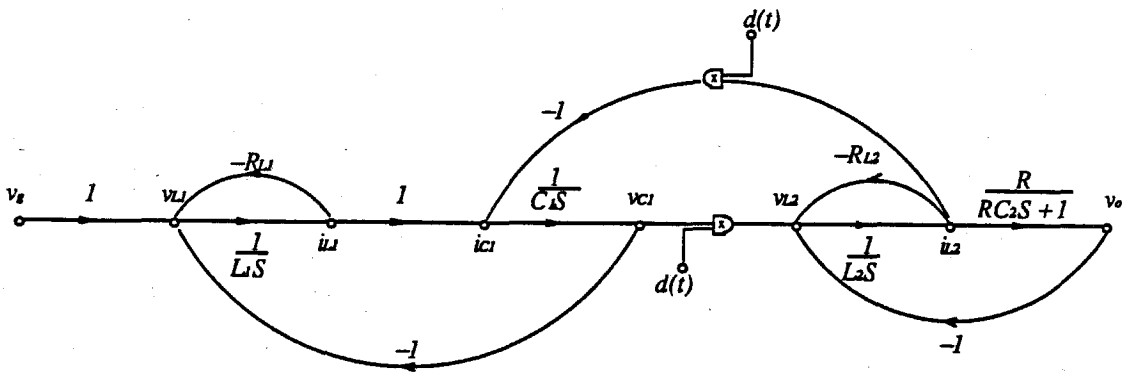


Figure 3.13: The Large-Signal Model of the Buck Converter with an Input Filter. In this model, two parasitic resistor are considered, R_{L1} and R_{L2}.

```
Model File: bfstp596.c10
Date:     4 / 22 / 1990
Time:     2 : 22
Timing: 300.000E-09 ,DELTA  ;    0.0050000   ,RANGE
PlotBlocks and Scales:
Format:
        BlockNo, Plot-MINimum,    Plot-MAXimum; Comment
Horz:        0 ,     0.0000   ,    0.0050000  ; Time
 Y1:        12 ,     0.0000   ,   20.0000     ; VO=VC2
 Y2:        10 ,     0.0000   ,    5.0000     ; IL2
 Y3:           ,              ,               ;
 Y4:           ,              ,               ;


   15.0000        1 CON                       ;Vg
    0.3550000     2 CON                       ;D_o
    0.0010000     3 PLS                       ;D_delta
    0.0100000
    0.3350000
                  4 SUM          2     3      ;D_o+D_delta
                  5 MUL          4    10      ;PWM SWITCH
  430.000E-06     6 L      1    -6    -7      ;IL2
    0.1731870
    0.2700000     7 R      6                  ;R11
   10.400E-06     8 C      6    -5            ;VC1
   14.9541
                  9 MUL    8     4            ;PWM SWITCH
  480.000E-06    10 L      9   -12   -11      ;IL2
    0.4854770
    0.6000000    11 R     10                  ;RL2
   10.3000       12 FIO   10                  ;VO=VC2
  309.000E-06
    5.0103
```

Figure 3.14: The Input Format of the TUTSIM Program. The Switching Flow-Graph Model can be directly entered to the TUTSIM simulation program. Users specify the transmittance and the inputs for each branch, define the duty-ratio step function, and give the initial condition, the simulation step size and the starting and stopping time.

An electronic switch was built to inject the duty-ratio step excitation at Point A. The Tektronix oscilloscope 2440 was used to measure the transient responses of the converter at Point B, for the output voltage v_o, and Point C, for the inductor current i_{L2}. The single shot mode was used, with the external signal from point A, to trigger the data acquisition to record the transients.

Experiment 3.1 For a large step duty-ratio jump, from $d = 0.355$ to $d = 0.69$, the output voltage jumped from $5V$ to $9.7V$, and the current jumped from $0.48A$ to $0.93A$.

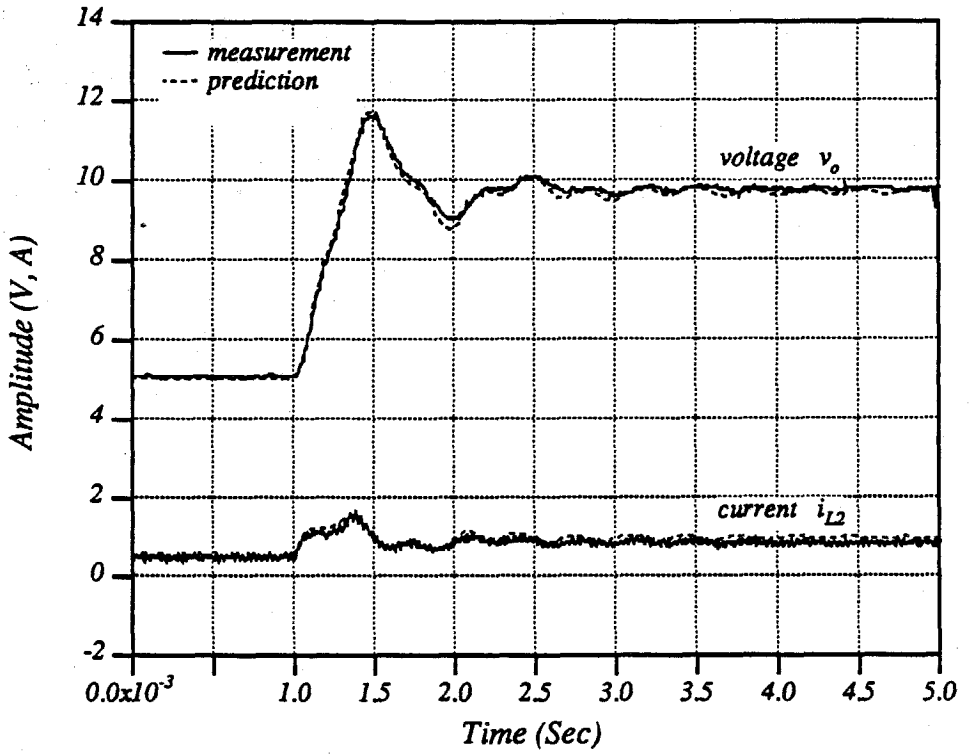


Figure 3.15: The Predicted and Measured Large-Signal Step Response. When the duty-ratio stepped up from $d = 0.355$ to $d = 0.69$, the output voltage v_o jumped from $5V$ to $9.7V$, and the current jumped from $0.48A$ to $0.93A$. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

The measured data and the simulation data are plotted in the same figure as shown in Fig. 3.15. The measured large-signal response and the prediction match very closely.

Experiment 3.2 The input capacitor was changed from $10.4\mu F$ to $31.4\mu F$, and other conditions remained the same. The measured data and the simulation data are plotted together in Fig. 3.16. The prediction and the measurement coincide with each other.

Experiment 3.3 The input inductor was changed from $0.43mH$ to $1.45mH$, and other

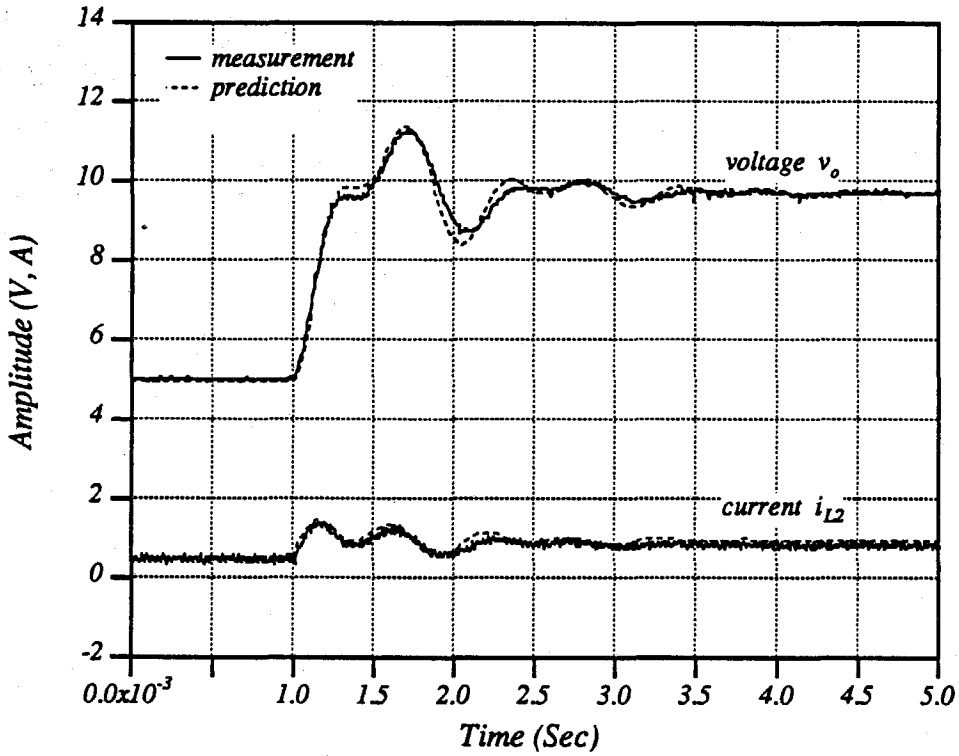


Figure 3.16: The Predicted and Measured Large-Signal Step Response. When the duty-ratio stepped up from $d = 0.355$ to $d = 0.69$, the output voltage v_o jumped from $5V$ to $9.7V$, and the inductor current $\hat{i}_{L2}$ jumped from $0.48A$ to $0.93A$. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 31.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

conditions remained the same as Experiment 3.2. The measured data and the simulation data are plotted together in Fig. 3.17. The prediction and the measurement are very close.

The experiments verified the Switching Flow-Graph large-signal model. This model can be utilized to predict the large-signal behaviors of the PWM switch converters, and to provide global stability information.

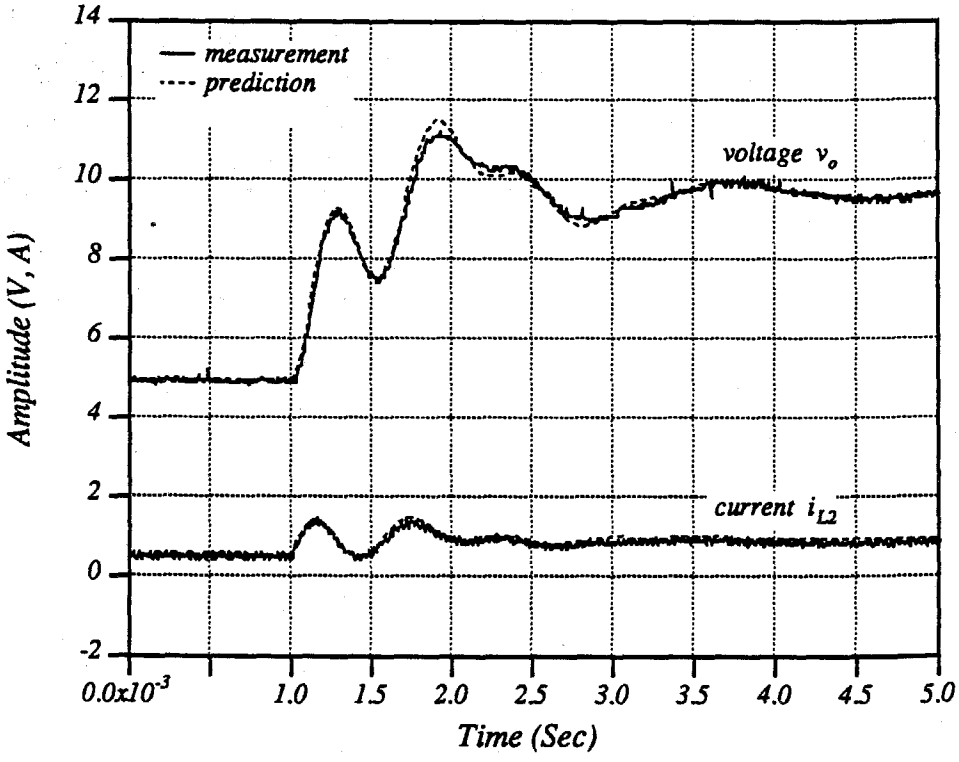


Figure 3.17: The Predicted and Measured Large-Signal Step Response. When the duty-ratio stepped up from $d = 0.355$ to $d = 0.69$, the output voltage v_o jumped from $5V$ to $9.7V$, and the inductor current $\hat{i}_{L2}$ jumped from $0.48A$ to $0.93A$. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 1.45mH$, $L_2 = 0.48mH$, $C_1 = 31.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

3.4.3 The Small-Signal Model

The small-signal linearized model plays an important role in the study of local Small-Signal dynamical behavior. For the buck converter with input filter, consider the two parasitic resistors, the small-signal model is shown in Fig. 3.18. The small-signal model predicts the input-to-all state frequency responses.

$$\frac{\hat{v}_{C1}}{\hat{d}} = \frac{N_3(S)}{D(S)}$$

$$\approx -\frac{\frac{DV_gR_{L1}}{R}(1+\frac{L_1}{R_{L1}}S)(2+(\frac{L_2}{R}+RC_2)S+L_2C_2S^2)}{D(S)} \tag{3.15}$$

$$= \frac{K_{C_1}(1+\frac{1}{\omega_3}S)(1+\frac{1}{Q_4\omega_4}S+\frac{1}{\omega_4}S^2)}{D(S)} \tag{3.16}$$

$$\frac{\hat{v}_o}{d} = \frac{N_4(S)}{D(S)}$$

$$\approx \frac{V_g(1+(C_1R_{L1}-\frac{D^2L_1}{R})S+L_1C_1S^2)}{D(S)} \tag{3.17}$$

$$= \frac{K_d(1+\frac{1}{Q_0\omega_0}S+\frac{1}{\omega_0^2}S^2)}{D(S)} \tag{3.18}$$

$$D(S) \approx (1+\frac{D^2L_1}{R}S+L_1C_1S^2)(1+\frac{L_2}{R}S+L_2C_2S^2) \tag{3.19}$$

$$= (1+\frac{1}{Q_1\omega_1}S+\frac{1}{\omega_1^2}S^2)(1+\frac{1}{Q_2\omega_2}S+\frac{1}{\omega_2^2}S^2) \tag{3.20}$$

where

$$K_{C1} = \frac{2V_gR_{L1}}{R(1+\frac{D^2R_{L1}}{R+R_{L2}})} \tag{3.21}$$

$$K_d = \frac{V_g(1-\frac{D^2R_{L1}}{R})}{1+\frac{R_{L2}+d^2R_{L1}}{R}} \tag{3.22}$$

$$\omega_0 = \frac{1}{\sqrt{L_1C_1}} \tag{3.23}$$

$$Q_0 = \frac{1}{R_{L1}\sqrt{\frac{C_1}{L_1}}-\frac{D^2}{R}\sqrt{\frac{L_1}{C_1}}} \tag{3.24}$$

$$\omega_1 = \frac{1}{\sqrt{L_1C_1}} \tag{3.25}$$

$$Q_1 = \frac{R}{D^2}\sqrt{\frac{C_1}{L_1}} \tag{3.26}$$

$$\omega_2 = \frac{1}{\sqrt{L_2C_2}} \tag{3.27}$$

$$Q_2 = R\sqrt{\frac{C_2}{L_2}} \tag{3.28}$$

$$\omega_3 = \frac{R_{L1}}{L_1} \tag{3.29}$$

$$\omega_4 = \frac{1}{\sqrt{\frac{L_2C_2}{2}}} \tag{3.30}$$

$$Q_4 = \frac{\sqrt{2}}{\frac{1}{R}\sqrt{\frac{L_2}{C_2}} + R\sqrt{\frac{C_2}{L_2}}} \tag{3.31}$$

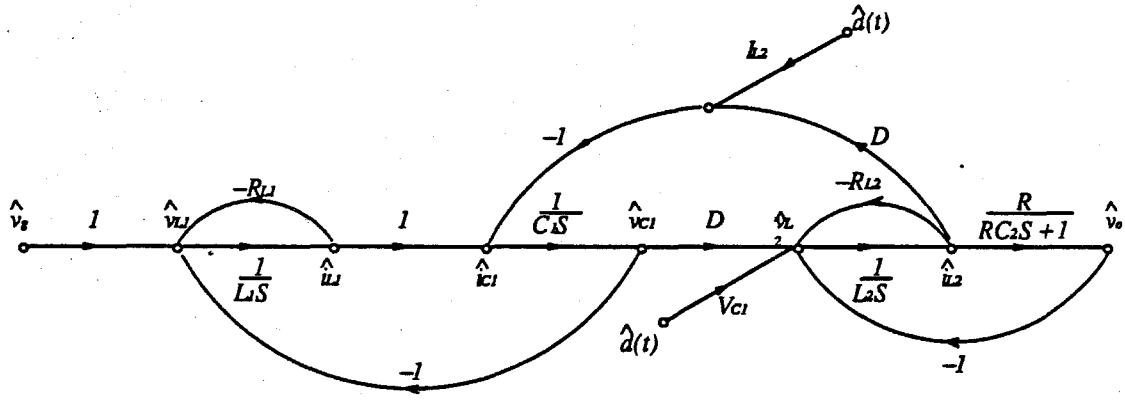


Figure 3.18: The Small-Signal Model of the Buck Converter with an Input Filter. In this model, two parasitic resistors are included, R_{L1} and R_{L2}.

Two experiments were conducted to verify the prediction. The HP 3577 network analyzer was used to measure frequency response. A frequency sweeping signal was injected at Point A. The responses at Point B were detected to determine the transfer function $\frac{\hat{v}_o}{\hat{d}}$, and the frequency responses at Point C were detected to determine the transfer function $\frac{\hat{i}_{L2}}{\hat{d}}$. An IBM AT was connected to the analyzer through the HPIB interface to take the measurement data.

Experiment 3.4 A frequency sweeping signal, ranged from $5Hz$ to $30KHz$, was injected at Point A. The responses at Point B were detected to determine the transfer function $\frac{\hat{v}_o}{\hat{d}}$. For the circuit parameter $V_g = 15V$, $f_s = 30kHz$, $D = 0.27$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 31.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$. The model predicts two RHP zeros, when the duty-ratio $D > 0.24$. The measured transfer function and the predicted transfer function are plotted in Fig. 3.19. The predicted and the measured response match closely. Both the prediction and the measurement show that the phase shifts 540° at $2.4kHz$. The measurement proved the prediction.

Experiment 3.5 A frequency sweeping signal, ranged from $5Hz$ to $30KHz$, was in-

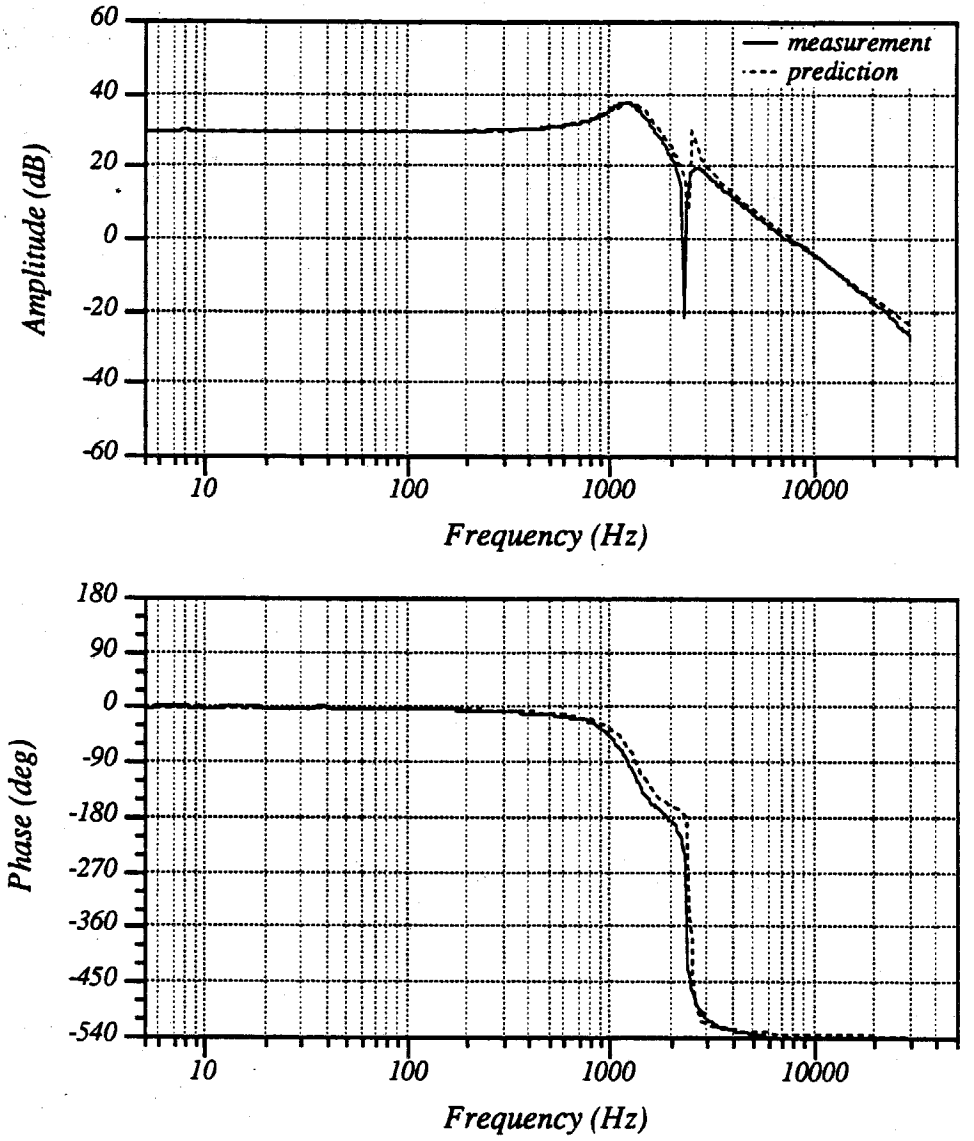


Figure 3.19: The Predicted and Measured Frequency Response of $\frac{\hat{v}_o}{d}$. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 31.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

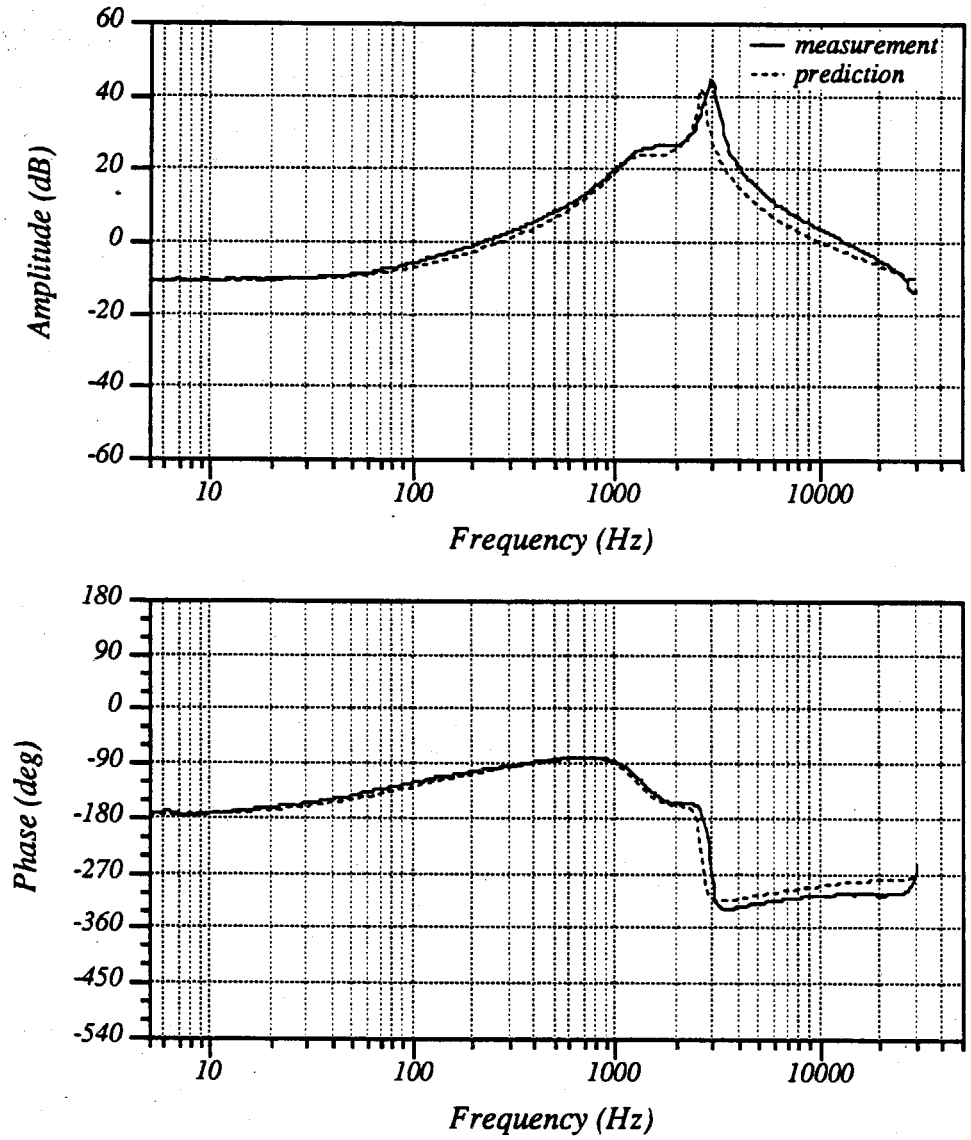


Figure 3.20: The Predicted and Measured Frequency Response of $\frac{\hat{i}_{L2}}{d}$. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $D = 0.27$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 31.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

jected at Point A. The responses at Point C were detected to determine the transfer function $\frac{\hat{i}_{L2}}{\hat{d}}$. For the same circuit parameters as that of Experiment 1, the predicted and the measured frequency responses are plotted in Fig. 3.20. The prediction and the measurement are very close.

3.5 Summary

The Switching Flow-Graphs are found for the commonly used converters in the second-order and the fourth-order families. A regularity exists in the Switching Flow-Graphs of the PWM switching converters. This regularity provides a visual and physical understanding of the switching converters. The large-signal Switching Flow-Graphs are compatible with the TUTSIM simulation program. The user simply specifies the transmittance and the inputs for each branch, defines the duty-ratio step function, and gives the initial conditions, the simulation step size, the starting and the stopping time. The TUTSIM program automatically simulates the dynamic transients. The small-signal Switching Flow-Graph models can be simplified by the flow-graph algebraic rules, shown in Appendix A. The analytical small-signal transfer function of the switching converters can be directly read from the Switching Flow-Graph. The Experiments proved that the large-signal Switching Flow-Graph model and the small-signal Switching Flow-Graph model are very accurate.

Chapter 4

Right-Half-Plane Zero Study

Most pulse-width-modulated (PWM) converters, such as the boost converter and the buckboost converter in the second-order converter family, and all the converters in the fourth-order converter family, have right-half-plane (RHP) zeros, as described in the last chapter. It is very difficult to close the feedback loop for PWM control or current-mode control of converters, especially fourth-order converters with two pairs of complex poles located close to each other and RHP zeros.

In Section 4.1, a physical interpretation of RHP zeros is revealed by the Switching Flow-Graph. Imbalanced effects are found for the duty-ratio control signal $d(t)$ to the output voltage v_o, which induce the RHP zeros in the small-signal frequency response. Experiments were conducted to detect the predicted RHP zeros. The results, discussed in Section 4.2, are in good agreement with the theory. Proper damping circuit design criteria are found, in Section 4.3, to eliminate the RHP zeros . By first understanding and then eliminating the RHP zeros, the fourth-order converters achieve very good close-loop dynamical response. Experiments verified the theory.

4.1 The Physical Interpretation of Right-Half-Plane Zeros

The Switching Flow-Graph models were found for the second-order converters and the fourth-order converters, as shown in Fig. 3.4 and Fig. 3.8. The Switching Flow-Graphs exhibit a unique regularity. The duty-ratio control signals are injected into the

converters through the switching branches. The duty-ratio control signals injected into a k-branch have a positive effect on the output voltage v_o if the k-branch is in the forward path, and have a negative effect the output voltage if the k-branch is in the feedback path. The duty-ratio control signals injected into a $\overline{k}$-branch have a negative effect on the output voltage v_o if the $\overline{k}$-branch is in the forward path, and have a positive effect on the output voltage if the $\overline{k}$-branch is in the feedback path. Further observation indicates that the duty-ratio control signals injected into a switching branch in the current path have a negative effect on the output, and the duty-ratio control signal injected into a switching branch in the voltage path have a positive effect on the output. The positive and negative effects of the duty-ratio control signals reach the output voltage through different dynamic processes; therefore, they are not balanced. The RHP zeros, in the small-signal models, are the result of this imbalance.

The imbalance affects the second-order family and the fourth-order family in different ways. To explain how this imbalance affects the performance of a switching converter in the second-order family, the boost converter, shown in Fig. 4.1, is utilized as an example. The small-signal model of the boost converter shows that the duty-ratio control signal $d(t)$ is injected into two nodes, the i_o node and the v_L node. The duty-ratio signal injected at the i_o node has a negative transfer function to the output voltage v_o:

$$\frac{\frac{-I_L L}{D'^2}S}{1+\frac{L}{RD'^2}S+\frac{LC}{D'^2}S^2} \tag{4.1}$$

Whereas the duty-ratio signal injected at the node v_L has a positive transfer function to the output voltage v_o:

$$\frac{V_o}{1+\frac{L}{RD'^2}S+\frac{LC}{D'^2}S^2} \tag{4.2}$$

According to linear-circuit superposition, these two effects of the duty-ratio can be added

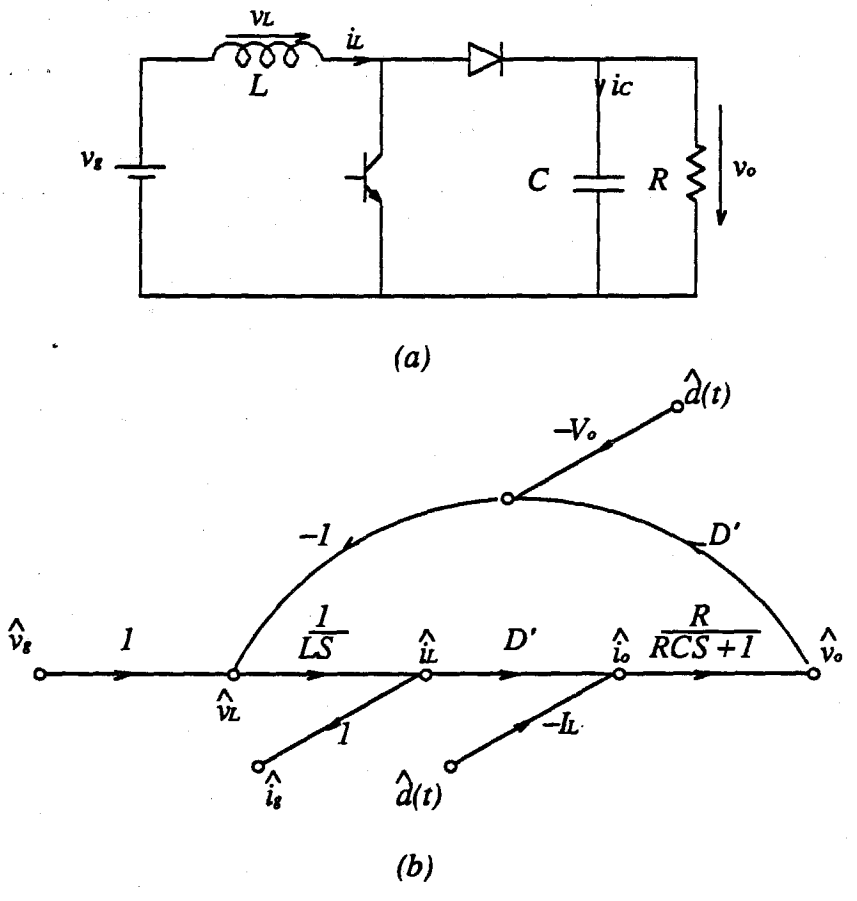


Figure 4.1: The Boost Converter and its Small-Signal Model. (a) The boost converter. (b) The Switching Flow-Graph small-signal model.

together to get the whole transfer function:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_o - \frac{I_L L}{D'^2} S}{1 + \frac{L}{RD'^2} S + \frac{LC}{D'^2} S^2} \tag{4.3}$$

It is easy to see that there is a RHP zero.

From Fig. 4.1 (b), it is clear that the negative duty-ratio signal injected at the node i_o is closer, in the signal path, to the output signal v_o than the positive duty-ratio signal injected at the node v_L. Therefore, the negative duty-ratio signal injected at the node i_o affects the output voltage v_o faster, by a factor of LS, than the positive duty-ratio signal injected at the node v_L. The Switching Flow-Graph physically demonstrates that

if the duty-ratio increases, then the time duration for the energy to discharge from the inductor to the output is reduced. The increase in the duty-ratio directly reduces the output voltage. On the other hand, when the duty-ratio increases, the time duration for the energy from the input voltage to charge the inductor increases, which increases the inductor current and eventually increases the output voltage. However, this process takes longer than the effect acting to reduce the output voltage because this process requires two steps.

When the duty-ratio $\hat{d}(t)$ is at a low frequency, the output voltage $\hat{v}_o$ is not phase shifted. However, when the duty-ratio $\hat{d}(t)$ is at a high frequency, the output voltage $\hat{v}_o$ is phase shifted by 90°.

To explain how this imbalance affects the performance of a switching converter in the fourth-order family, the buck converter with input filter, shown in Fig. 3.5, is utilized as an example. The small-signal model of the buck converter with input filter, Fig. 3.18, shows that the duty-ratio signal is injected into two nodes, the i_{C1} node and the v_{L2} node. The duty-ratio injected at the i_{C1} node has a negative effect on the output voltage v_0, while the duty-ratio injected at v_{L2} has a positive effect on the output voltage v_0. Physically, when the duty-ratio increases, the charging time of the inductor L_2 increases, which tends to increase the output voltage. However, the increased duty-ratio reduces the current that charges the capacitor C_1, which tends to reduce the output voltage. This imbalance causes the RHP zeros in the small-signal model of the buck converter.

The existence of RHP zeros in the PWM converter makes the control-loop design very difficult. The closed-loop is very hard to stabilize.

4.2 Detection of the Right-Half-Plane Zeros

For a given buck converter with input filter, as shown in Fig. 3.12, the open-loop transfer function has a numerator:

$$N(S) = ((1 - \frac{R_1 D}{R}) + (R_{L1}C_1 - \frac{D^2 L_1}{R})S + L_1 C_1 S^2) \tag{4.4}$$

$$= 1 + \frac{1}{Q_0 \omega_0} S + \frac{1}{\omega_0^2} S^2 \tag{4.5}$$

$$\tag{4.6}$$

where $\frac{R_1 D}{R} << 1$, therefore,

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{4.7}$$

$$Q_0 = \frac{1}{R_{L1}\sqrt{\frac{C_1}{L_1}} - \frac{D^2}{R}\sqrt{\frac{L_1}{C_1}}}. \tag{4.8}$$

When

$$R_{L1}\sqrt{\frac{C_1}{L_1}} > \frac{D^2}{R}\sqrt{\frac{L_1}{C_1}}, \tag{4.9}$$

the buck converter has left-half-plane (LHP) zeros, while when

$$R_{L1}\sqrt{\frac{C_1}{L_1}} < \frac{D^2}{R}\sqrt{\frac{L_1}{C_1}}, \tag{4.10}$$

the LHP zeros change to RHP zeros.

$$R_{L1}C_1 = \frac{D^2 L_1}{R} \tag{4.11}$$

Equation (4.11) is the critical condition. If the circuit parameters are constant while the duty-ratio D is varying, a critical duty-ratio D_{crit} can be found at which the LHP zeros change to RHP zeros.

$$D_{crit} = \sqrt{\frac{R_{L1} R C_1}{L_1}} \tag{4.12}$$

For the given value of $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$, the critical duty-ratio

D_{crit} is 0.24. Therefore, if $D < 0.24$ there are no RHP zeros; whereas, if $D > 0.24$ a pair of RHP zeros appears. Experiments were conducted, using the circuit shown in Fig. 3.12, to detect the RHP zeros.

Experiment 4.1 The HP 3577 network analyzer was used to measure the frequency response. A frequency sweeping duty-ratio modulation signal was injected at Point A. The response was detected at Point B to determine the transfer function $\frac{\hat{v}_o}{\hat{d}}$. The duty-ratio D was varied from a small value to a large value, $D(1) = 0.2$, $D(2) = 0.23$, $D(3) = 0.27$, and $D(4) = 0.4$. In all cases, the values for v_g, f_s, L_1, L_2, C_1, C_2, R_{L1}, R_{L2}, and R were held constant. When the duty-ratio $D = 0.2$, far below the critical duty-ratio D_{crit}, the frequency response is only phase shifted by 180°; therefore, the converter has no RHP zeros. The measured data and the predicted results are plotted together in Fig. 4.2. The experimental data match the theoretical prediction very closely. When the duty-ratio $D = 0.23$, which is a little below the critical duty-ratio D_{crit}. The phase shift of the frequency response still did not exceed 180°. The measured and the predicted results are plotted together in Fig. 4.3. Therefore, the converter does not have any RHP zeros; however, the Q value is higher. The duty-ratio was further increased to exceed the critical duty-ratio D_{crit}, $D = 0.27$. The measured and the predicted results are plotted together in Fig. 4.4. The phase shift dramatically crosses over 180° and reaches 540°. Two RHP zeros appear and the Q value is very high. When the duty-ratio $D = 0.4$, which was far above the critical duty-ratio D_{crit}. The phase shift reaches to 540°, with a more gradual falling slope than the case for $D = 0.27$. The measured and the predicted results are plotted together in Fig. 4.5. As predicted, the converter has two RHP zeros with a lower Q value than the case when $D = 0.27$.

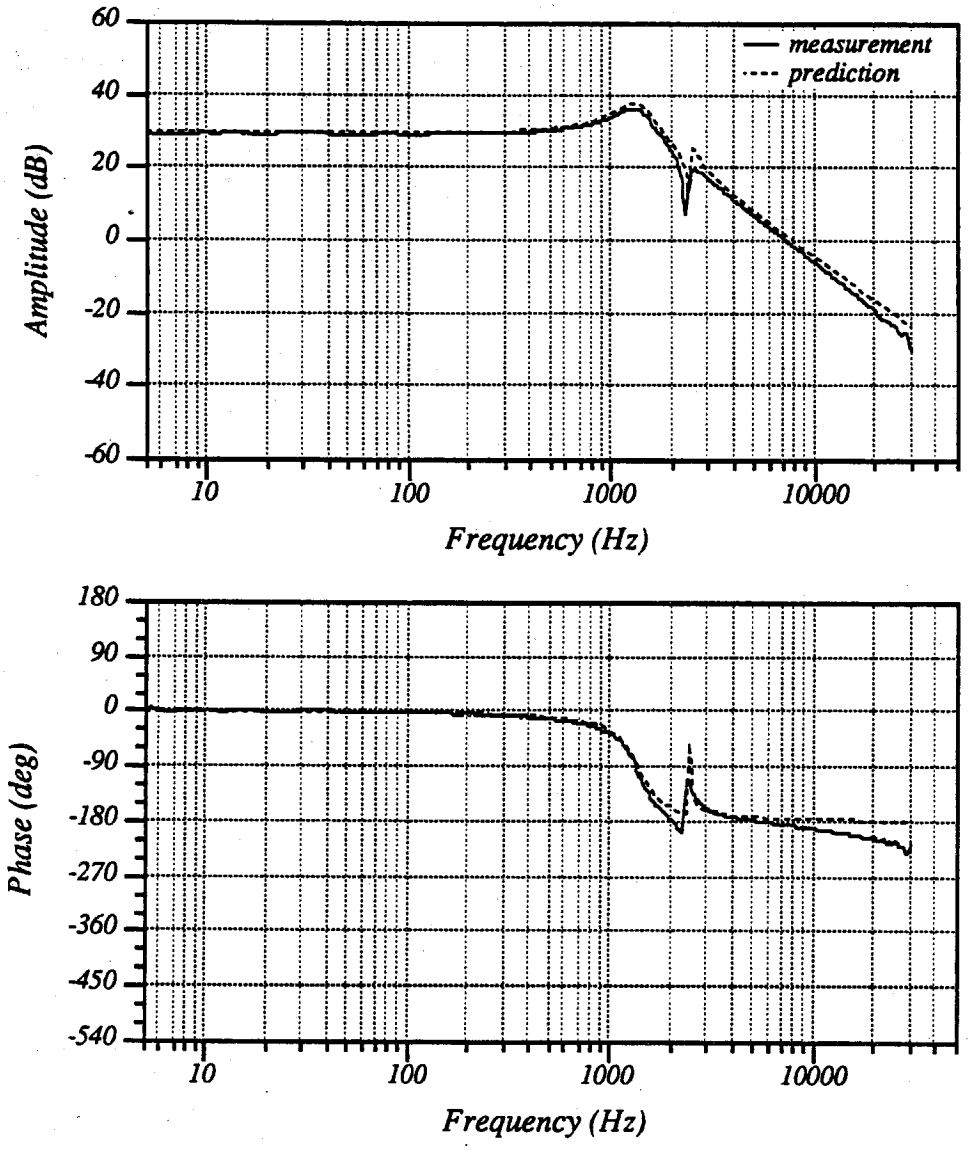


Figure 4.2: The Predicted and Measured Frequency Response when D=0.2. The duty-ratio D is much smaller than the critical duty-ratio D_{crit}; there is no RHP zero. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

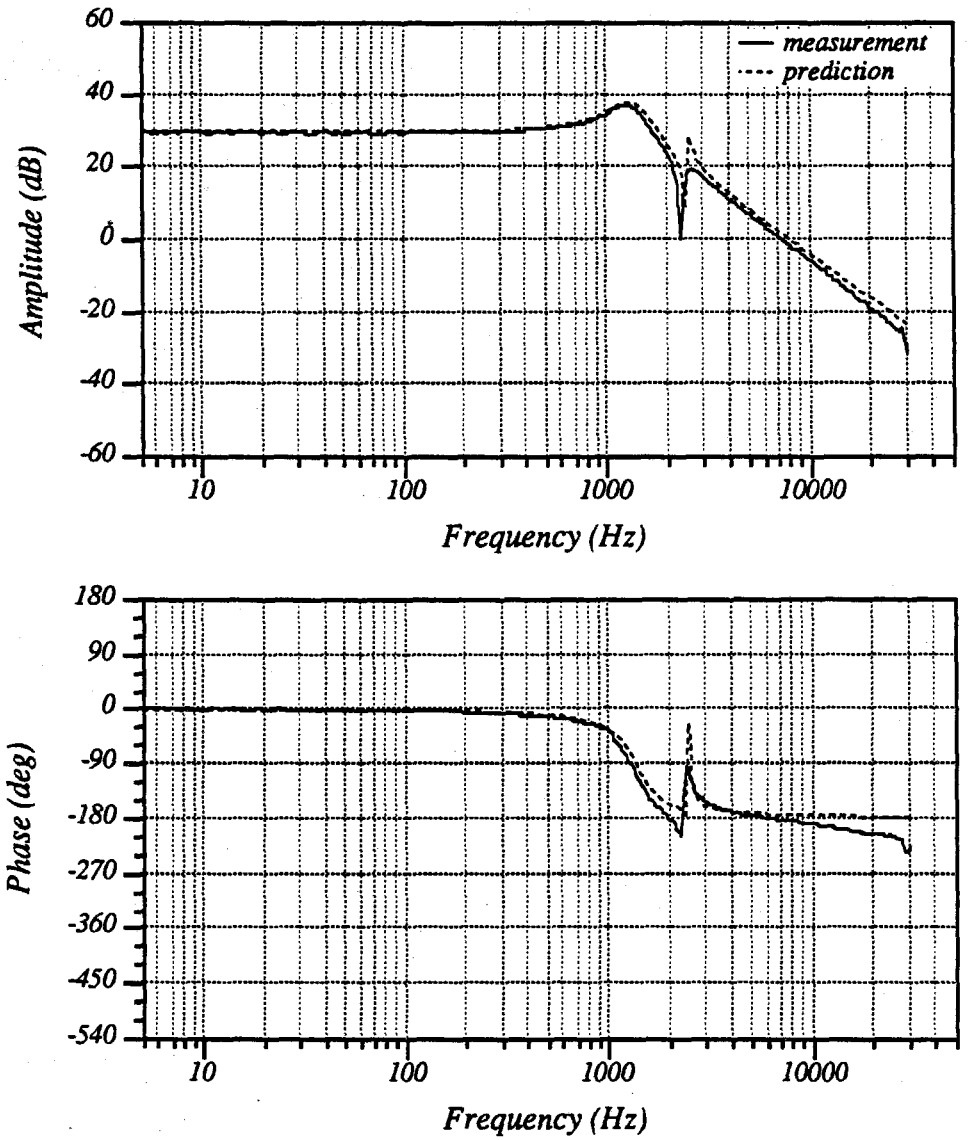


Figure 4.3: The Predicted and Measured Frequency Response when D=0.23. The duty-ratio D is a little smaller than the critical duty-ratio D_{crit}; there is still no RHP zero. However, the duty-ratio D is very close to D_{crit}; the Q value is very high. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

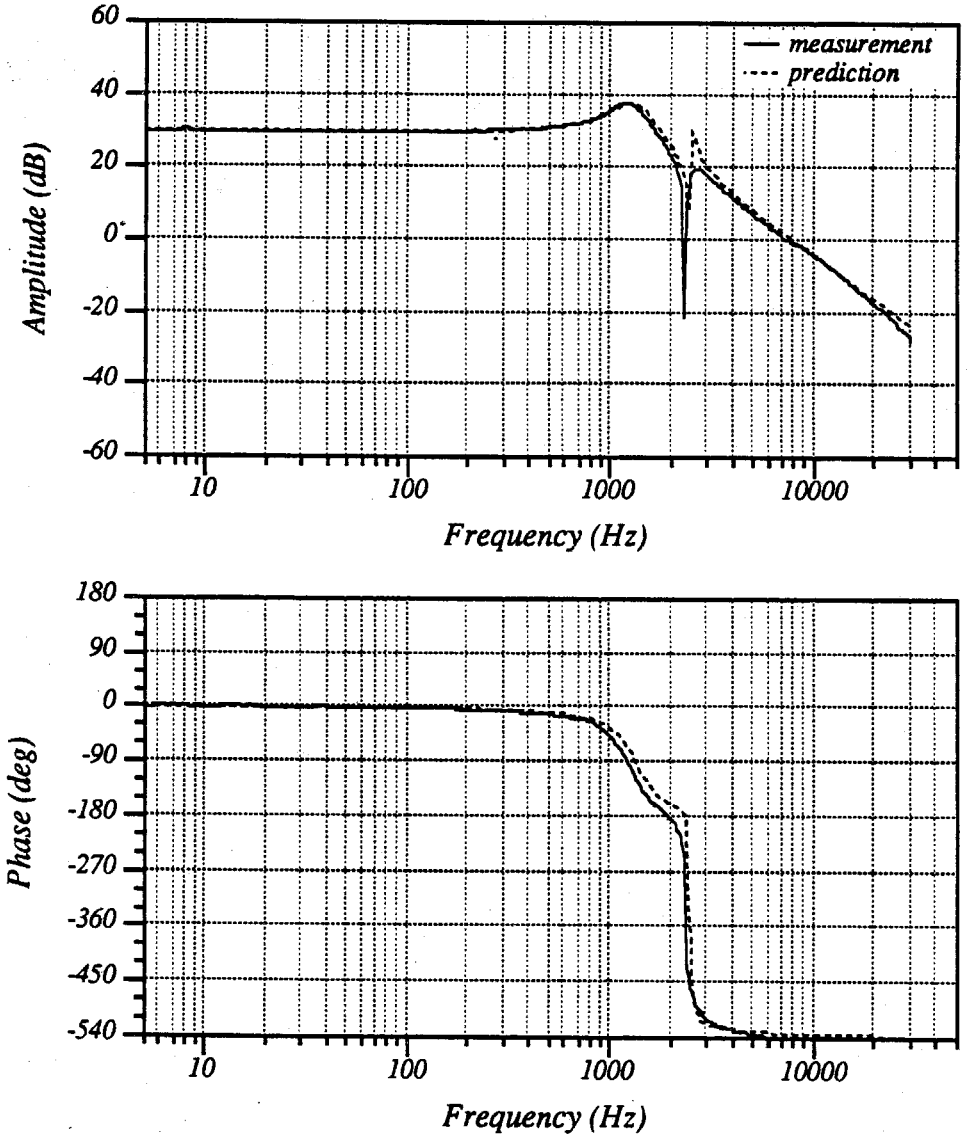


Figure 4.4: The Predicted and Measured Frequency Response when D=0.27. The duty-ratio D is just above D_{crit}; the RHP zeros appear. Since the duty-ratio D is very close to the critical duty-ratio D_{crit}; the Q is very high. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

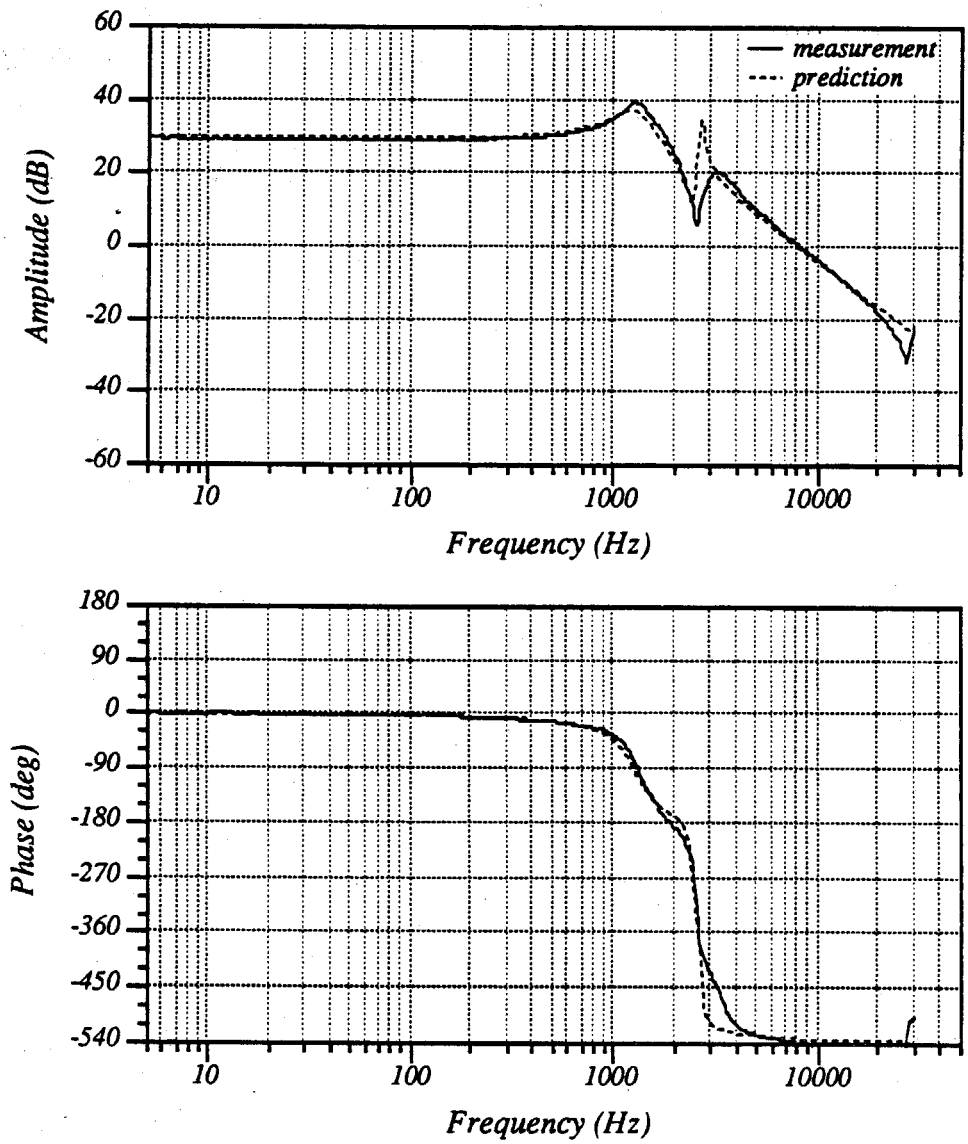


Figure 4.5: The Predicted and Measured Frequency Response when D=0.4. The duty-ratio D is much larger than the critical duty-ratio D_{crit}; there are two RHP zeros. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

4.3 Damping Technique to Eliminate the Right-Half-Plane Zeros

In this section, the damping technique is used to eliminate the RHP zeros and therefore improve the dynamic properties of the PWM converter.

For a real switching converter, the input voltage source always has impedance, and the parasitic resistance of the inductor is always present. The whole input resistance provides some damping to the RHP zeros. To have controllable damping, an effective engineering method to eliminate the RHP zeros is to add a damping circuit to the energy-transfer capacitor.

4.3.1 The Input Resistor Damping

In Section 4.2, the condition is derived for an input resistance that is capable of eliminating the RHP zeros of the buck converter with input filter, shown in Equation(4.11). The same condition are also found for the d^2 converter, the Ćuk converter, and the Lambda converter.

$$R_{L1} > \frac{D^2 L_1}{RC_1} \quad \text{for the input filter buck} \tag{4.13}$$

$$R_{L1} > \frac{D^2 L_1}{RC_1} \quad \text{for the } d^2 \text{ converter} \tag{4.14}$$

$$R_{L1} > \frac{D^2 L_1}{D'C_1 R} \quad \text{for the Ćuk converter} \tag{4.15}$$

$$R_{L1} > \frac{D^2 L_1}{D'C_1 R} \quad \text{for the Lambda converter} \tag{4.16}$$

In practice, however, the converter circuit is designed to minimize the input resistance in order to increase the power processing efficiency. Therefore, input resistance damping is usually not enough to eliminate the RHP zeros, and even if the RHP zeros are damped out, the Q value of the LHP zeros may be very high, as discussed in Section 4.2.

4.3.2 The Energy-Transfer Capacitor Damping

A capacitor damping circuit for the buck converter with input filter is shown in Fig. 4.6. The capacitor damping circuit contains a resistor R_D and a capacitor C_D. To

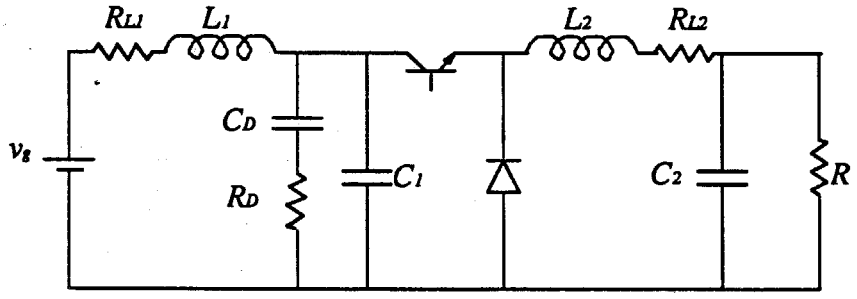


Figure 4.6: The Damping Circuit for the Buck Converter. A capacitor C_D and a resistor R_D compose a damping circuit.

examine the effect of this damping, neglect the parasitic resistance R_{L1} for a moment. The transfer function $\frac{\hat{v}_o}{\hat{d}}$ has a numerator:

$$N(S) = 1 - \frac{D^2 L_2}{R} S + L_1 C_1 S^2 \tag{4.17}$$

Let:

$$C_1 S \rightarrow \frac{C_D S(1 + C_1 R_D S)}{1 + C_D R_D S}, \tag{4.18}$$

in Equation(4.17). Therefore, Equation(4.17) becomes

$$\mathcal{N}_{damp}(S) = 1 + (C_D R_D - \frac{D^2 L_1}{R})S + (L_1 C_D - \frac{D^2 L_1 C_D R_D}{R})S^2 + L_1 L_2 C_2 C_2 S^3. \tag{4.19}$$

Apply Ruth's law to $\mathcal{N}_{damp}(S)$; the criterion to have all zeros in the LHP is obtained:

$$\frac{D^2 L_1}{R C_D} < R_D < (1 - \frac{C_1}{C_D})\frac{R}{D^2} \tag{4.20}$$

If the damping circuit is designed with this criterion, all the RHP zeros of the Lambda converter will be moved to the LHP. Similarly, the damping criteria for the D^2 converter,

the Ćuk converter, and the Lambda converter are

$$\frac{D^2L_1}{RC_D} < R_D < (1-\frac{C_1}{C_D})\frac{R}{D^2} \quad \text{for the input filter buck} \quad (4.21)$$

$$\frac{D^2L_1}{2RC_D} < R_D < (1-\frac{C_1}{C_D})\frac{R}{D^2} \quad \text{for the } D^2 \text{ converter} \quad (4.22)$$

$$\frac{D^2L_1}{D'^2RC_D} < R_D < (1-\frac{C_1}{C_D})\frac{D'R}{D^2} \quad \text{for the Ćuk converter} \quad (4.23)$$

$$\frac{D^2L_1}{D'^2(1+D')RC_D} < R_D < (1-\frac{C_1}{C_D})\frac{D'R}{D^2} \quad \text{for the Lambda converter} \quad (4.24)$$

These conditions are derived when the input resistance $R_{L1} = 0$; therefore, this is not exact if the input resistance R_{L1} is not zero.

4.3.3 Experimental Verification

The buck converter with input filter, as shown in Fig. 4.6, with the same circuit parameters given in Section 4.2, has RHP zeros when the duty-ratio $D = 0.4$, as predicted and detected in Section 4.2.

If the damping capacitor is chosen to be $C_D = 100\mu F$; the damping condition for $R_{L1} = 0$ is

$$0.7\Omega < R_D < 56\Omega. \quad (4.25)$$

For the real circuit, there is a parasitic input resistance $R_{L1} = 0.25$; therefore, this condition is not exact.

Experiment 4.2 A damping resistor $R_D = 51\Omega$ was used, which was inside the condition region. The RHP zeros of the buck converter with input filter should be changed to LHP zeros. The experimental result is shown in Fig. 4.7. The measured phase shift is 180°; hence, the measured frequency response shows that no RHP zeros exist; as predicted. The damping resistor was increased to $R_D = 82\Omega$, which is outside the condition region. The theory predicts that the RHP zeros of the buck converter may come back.

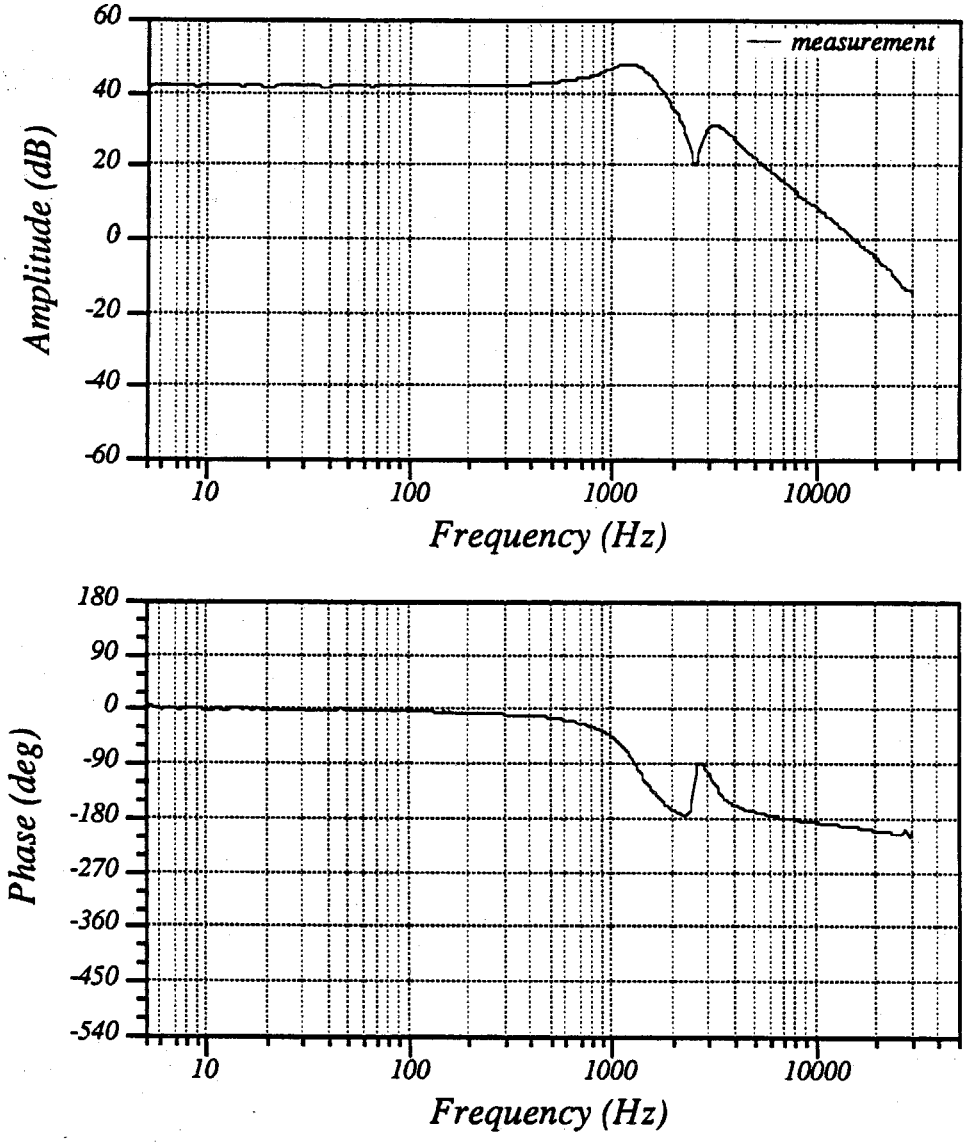


Figure 4.7: The Measured Frequency Response when the Damping Condition is Satisfied. The damping capacitor $C_D = 100\mu F$, and the damping resistor $R_D = 51\Omega$. As predicted there is no RHP zero. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

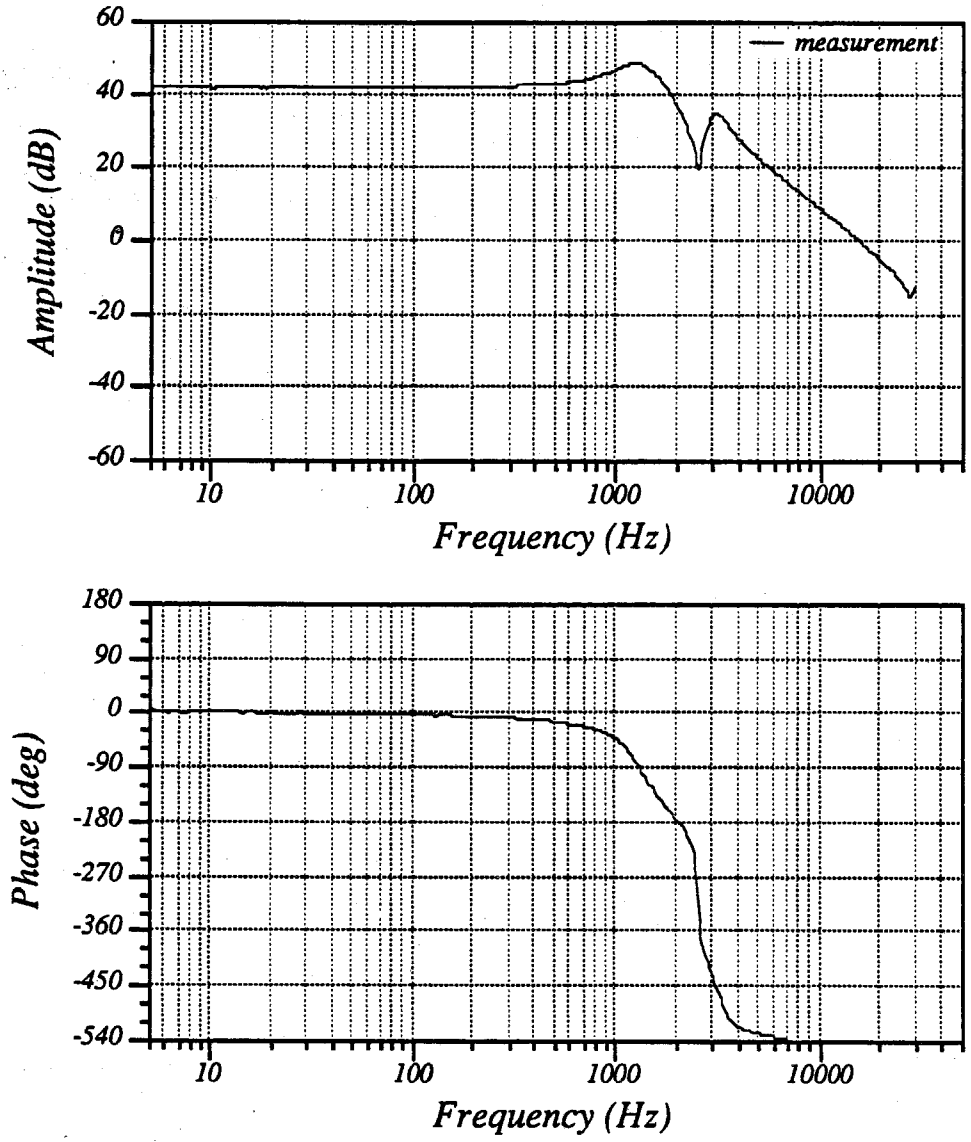


Figure 4.8: The Measured Frequency Response when the Damping Condition is not Satisfied. The damping capacitor $C_D = 100\mu F$, and the damping resistor $R_D = 82\Omega$. As predicted there are RHP zeros. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

The experimental result is shown in Fig. 4.8. The phase shift crosses over 540°; therefore, the RHP zeros show up in the measured frequency response as predicted.

4.4 Summary

The duty-ratio control signal $d(t)$ is injected into switching converters through the switching branches. The Switching Flow-Graph model physically revealed two imbalanced effects that the duty-ratio control signal was exerting on the output voltage. This imbalance is the reason for RHP zeros in the small-signal transfer functions. The Switching Flow-Graph model provides analytical predictions of the RHP zeros, which directs the designer to choose proper circuit parameters to avoid the RHP zeros. The damping criterion, which is a useful tool for eliminating the RHP zeros, is derived from the Switching Flow-Graph model. Experiments were conducted to verify the theoretical predictions.

Chapter 5

General Model for Converters with Current-Mode Control

The current-mode control technique is widely used to improve the dynamic properties of switching converters. A general model of the current-mode control is given in this chapter. The model physically describes how the current-mode control loop affects the dynamics of the switching converters, and it explains why the right-half-plane (RHP) zeros are not removed by the current-mode control loop and under which conditions loop oscillations will occur. Section 5.1 describes the dynamic structure for a converter power stage. In Section 5.2 the feedback function is discussed for current-mode control. In Section 5.3 the general model is found for the current-mode control switching converters. In Section 5.4 the general model is used to predict the stability of the switching converters with experimental verification.

5.1 Switching Converter Power-Stage

Consider an nth-order converter, shown in Fig. 5.1, that has n_L inductors, L_1, L_2, ..., L_{n_L}, and n_C capacitors, C_1, C_2, ..., C_{n_C}, where $n_C + n_L = n$. Suppose that $\hat{i}_k$, $1 \leq k \leq n_L$, is the current flowing through inductor L_k, and $\hat{v}_j$, $1 \leq j \leq n_C$, is the voltage across capacitor C_j.

By apply the Switching Flow-Graph modelling technique, the small-signal transfer

functions are obtained for control-to-all-states. Let the inductor currents and the capacitor voltages be the n state variables. State symbols with hats represent the small-signal perturbation of the associated states. The transfer functions for the converter power stage are

$$\frac{\hat{i}_k}{\hat{d}} = \frac{c_{kn}S^{n-1} + c_{kn-1}S^{n-2} + \cdots + c_{k1}}{S^n + a_nS^{n-1} + \cdots + a_1} \qquad k = 1, \ldots, n_L \tag{5.1}$$

$$\frac{\hat{v}_j}{\hat{d}} = \frac{c_{jn}S^{n-1} + c_{jn-1}S^{n-2} + \cdots + c_{j1}}{S^n + a_nS^{n-1} + \cdots + a_1} \qquad j = 1, \ldots, n_C \tag{5.2}$$

$$\hat{v}_o = \hat{v}_{n_C}, \tag{5.3}$$

where $a_i \geq 0$ are the coefficients in the denominator and c_{ki}, c_{ji} are arbitrary coefficients in the numerator. For some converters, the numerator $c_{in}S^{n-1} + c_{in-1}S^{n-2} + \cdots + c_{i1}$, $i = 1, \ldots, n$, may contain RHP zeros.

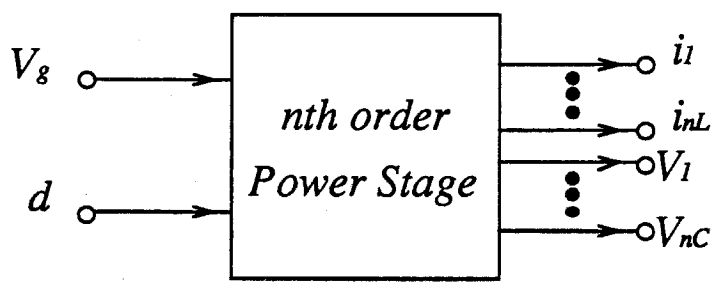


Figure 5.1: The nth-Order Power Stage. It has n_L inductors, L_1, L_2, ..., L_{n_L}, and n_C capacitors, C_1, C_2, ..., C_{n_C}, where $n_C + n_L = n$. Suppose that $\hat{i}_k$, $1 \leq k \leq n_L$, is the current flowing through inductor L_k, and $\hat{v}_j$, $1 \leq j \leq n_C$, is the voltage cross capacitor C_j.

5.2 Current-Mode Control Loop

A schematic diagram of current-mode control is shown in Fig. 5.2. The switch is turned ON by a fixed frequency clock. The switch current i_s is sensed and compared with a current reference i_{ref}. The duty-ratio d of the switch is determined by the time at which the switch current reaches the current reference. Therefore, the current reference

i_{ref}, the inductor currents i_L, the rising and falling ramp of the inductor current m_1 and m_2, and the stabilizing ramp m_c directly control the duty-ratio d.

$$d = F(i_{ref}, i_L, m_1, m_2, m_c) \tag{5.4}$$

The inductor current i_L is the sum of the inductor currents that flow through the active

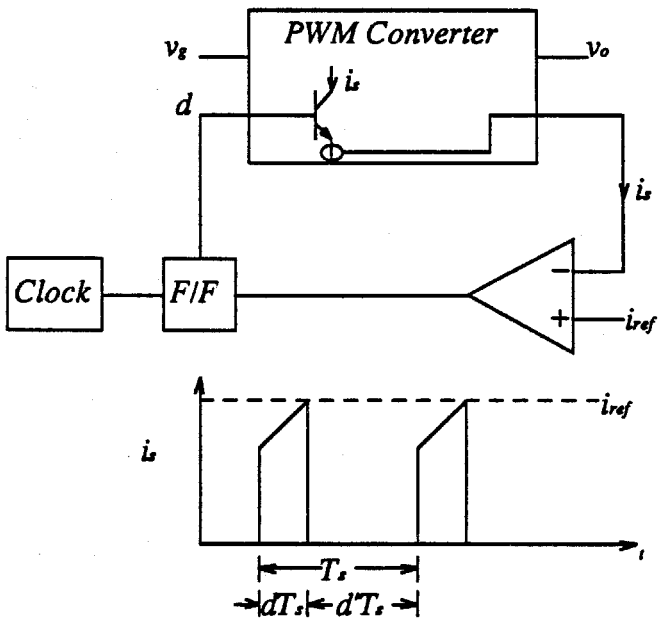


Figure 5.2: Block Diagram of Current-Mode Control. The switch is turned ON by a fixed frequency clock. The switch current i_s is sensed and compared with a current reference i_{ref}. The switch duty-ratio d is determined by the time at which the switch current reaches the current reference.

switch, transistor, during the time when the transistor is ON. The rising and falling ramps m_1 and m_2 of the inductor current are functions of the input voltage v_g and the voltages across the capacitors v_j, $j = 1, \ldots, n_C$. The small-signal model of current-mode control is obtained by linearizing Equation (5.4) around the operating point.

$$\hat{d} = F_o \hat{i}_{ref} - \sum_{k=1}^{n_L} f_k \hat{i}_k - \sum_{j=1}^{n_C} f_{n_L+j}\ \hat{v}_j \tag{5.5}$$

F_o is the control gain and f_i, $1 \leq i \leq n$, is the feedback coefficient of the ith state variable. The small-signal model of current-mode control is equivalent to the state-feedback control function. Since the feedback coefficients f_i, $1 \leq i \leq n$ are generated by Equation (5.4), they are not independent. The only control parameters that vary the feedback coefficients are the stabilizing ramp m_c and the switch period T_s.

There are several different analog approximations that yield the small-signal model [13] [14]. The model given in [14] is not defined when the artificial ramp is zero. Therefore, the small-signal model suggested in [13] is used as the example in this chapter.

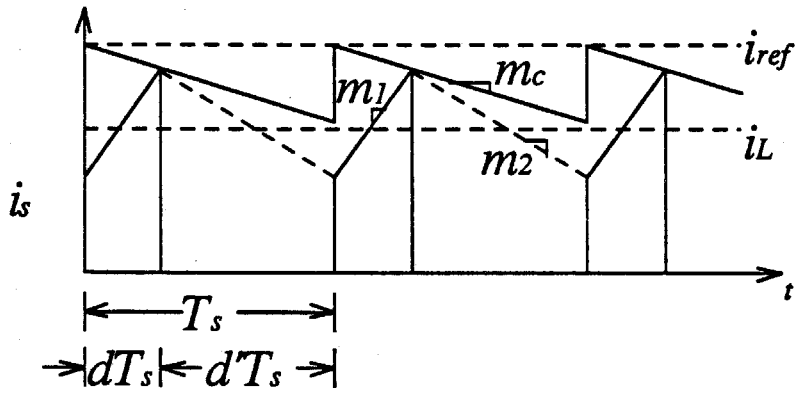


Figure 5.3: The Geometric Function of Current-Mode Control. m_1 is the rising slope of the switch current, m_2 is the falling slope of the inductor current associated with the switch current, and m_c is the stabilizing ramp.

The geometrical relationship shown in Fig. 5.3 reveals the function of current-mode-control:

$$i_L + m_1 \frac{dT_s}{2} = i_{ref} - m_c dT_s \tag{5.6}$$

i_L is the inductor current, m_1 is the rising slope of the inductor current, d is the duty-ratio, T_s is the switch period, i_{ref} is the current control reference, and m_c is the slope of the stabilizing ramp. For small-signal operation, suppose the steady-state values are I_L,

M_1, D, and I_{ref} and the associated perturbations are $\hat{i}_L$, $\hat{m}_1$, $\hat{d}$, and $\hat{i}_{ref}$.

$$i_L = I_L + \hat{i}_L \tag{5.7}$$

$$m_1 = M_1 + \hat{m}_1 \tag{5.8}$$

$$d = D + \hat{d} \tag{5.9}$$

$$i_{ref} = I_{ref} + \hat{i}_{ref} \tag{5.10}$$

The small-signal perturbation model is obtained by linearizing Equation (5.6):

$$\hat{d} = \frac{2}{nM_1T_s}(\hat{i}_{ref} - \hat{i}_L) - \frac{D}{nM_1}\hat{m}_1 \tag{5.11}$$

where

$$n = 1 + \frac{2m_c}{M_1}. \tag{5.12}$$

The rising slope of the inductor current m_1 is a linear function of the voltage variables, i.e., the input voltage and the capacitor voltages. The inductor current i_L is a linear combination of the inductor currents. For example, the boost converter has

$$m_1 = \frac{v_g}{L} \tag{5.13}$$

$$i_L = i_{L1}. \tag{5.14}$$

The lambda converter has

$$m_1 = \frac{v_g}{L_1} + \frac{v_{C1} - v_{C2}}{L_2} \tag{5.15}$$

$$i_L = i_{L1} + i_{L2}. \tag{5.16}$$

Consequently, the duty-ratio perturbation $\hat{d}$ is a linear combination of the state variables of the controlled converter.

5.3 General Model of Current-Mode Control

To study the dynamic properties of the general current-mode control system, the state space analysis tool is employed. For mathematical simplicity, a set of intermediate

state variables $x_1, x_2, \ldots, x_n$ are used

$$x_1 = x \tag{5.17}$$

$$x_2 = x' \tag{5.18}$$

$$\vdots \tag{5.19}$$

$$x_n = x^{(n-1)}. \tag{5.20}$$

These intermediate states are related to the standard circuit states $\hat{i}_k$ and v_j,

$$x_1 = \frac{1}{S^n + a_n S^{n-1} + \cdots + a_1}\hat{d} \tag{5.21}$$

$$\hat{i}_k = (c_{kn}S^{n-1} + c_{kn-1}S^{n-2} + \cdots + c_{k1})x \qquad k = 1, \ldots, n_L \tag{5.22}$$

$$\hat{v}_j = (c_{jn}S^{n-1} + c_{jn-1}S^{n-2} + \cdots + c_{j1})x \qquad j = 1, \ldots, n_C. \tag{5.23}$$

This relation can be expressed in state space, as shown in Fig. 5.4.

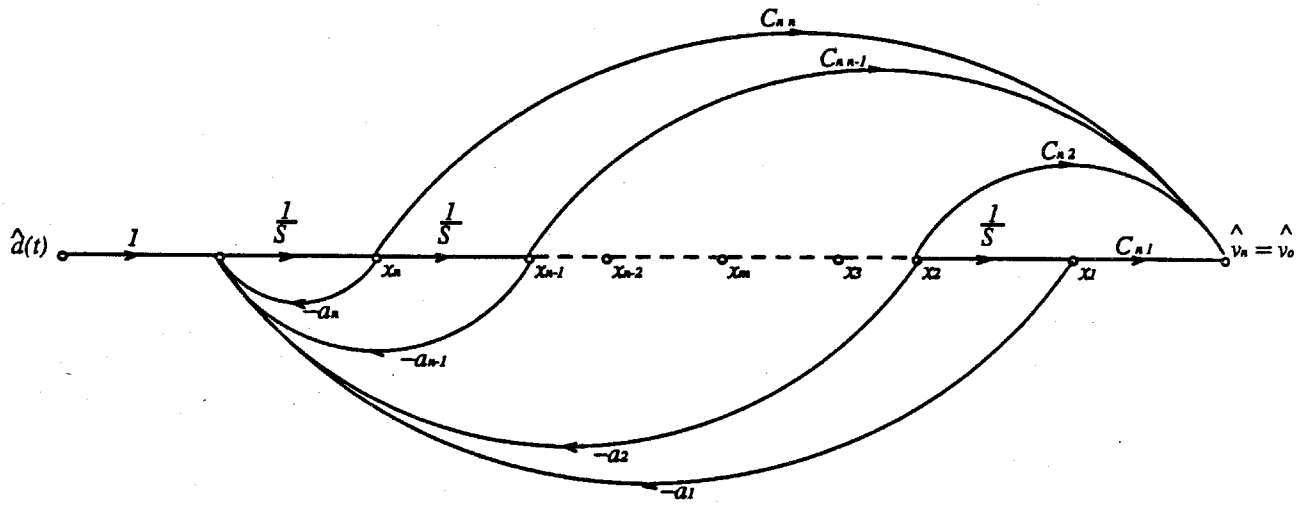


Figure 5.4: The Converter System. $x_1, x_2, \ldots, x_n$ are n independent intermediate state variables. The inductor currents $\hat{i}_k$, $1 \le k \le n_L$, the capacitor voltage $\hat{v}_j$, $1 \le j \le n_C$, can be expressed by a linear combination of the n states x_i, $1 \le i \le n$.

Let

$$X = \begin{bmatrix} x_1 & x_2 & \cdots & x_n \end{bmatrix}^T \tag{5.24}$$

$$Y = \begin{bmatrix} \hat{i}_1 & \cdots & \hat{i}_{n_L} & \hat{v}_1 & \cdots & \hat{v}_{n_C} \end{bmatrix}^T. \tag{5.25}$$

The n states x_1, x_2, ..., x_n are independent; therefore, the inductor currents $\hat{i}_k$, $1 \leq k \leq n_L$, the capacitor voltage $\hat{v}_j$, $1 \leq j \leq n_C$, can be expressed by a linear combination of the n states x_i, $1 \leq i \leq n$.

$$X' = AX + B\hat{d} \tag{5.26}$$

$$Y = CX \tag{5.27}$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ .. & .. & .. & \cdots & .. \\ 0 & 0 & 0 & \cdots & 1 \\ -a_1 & -a_2 & -a_3 & \cdots & -a_n \end{bmatrix} \tag{5.28}$$

$$B = \begin{bmatrix} 0 & 0 & \cdots & 0 & 1 \end{bmatrix}^T \tag{5.29}$$

$$C = \begin{bmatrix} c_{11} & c_{12} & \cdots & c_{1n} \\ c_{21} & c_{22} & \cdots & c_{2n} \\ .. & .. & \cdots & .. \\ c_{n1} & c_{n2} & \cdots & c_{nn} \end{bmatrix}. \tag{5.30}$$

The system feedback is:

$$\hat{d} = F_o\hat{i}_{ref} + FY \tag{5.31}$$

$$= F_o\hat{i}_{ref} + FCX \tag{5.32}$$

$$= F_o\hat{i}_{ref} + F^*X \tag{5.33}$$

where

$$F = \begin{bmatrix} -f_1 & -f_2 & \cdots & -f_n \end{bmatrix} \tag{5.34}$$

$$F^* = \begin{bmatrix} -f_1^* & -f_2^* & \cdots & -f_n^* \end{bmatrix} \tag{5.35}$$

$$f_k^* = \sum_{i=1}^{n} f_i c_{ik}. \tag{5.36}$$

Therefore, the closed-loop system is

$$X' = AX + B\hat{d} \tag{5.37}$$

$$= AX + BF^*X + BF_o\hat{i}_{ref}$$

$$= (A + BF^*)X + BF_o\hat{i}_{ref}$$

$$= A^*X + B^*\hat{i}_{ref} \tag{5.38}$$

where

$$A^* = \begin{bmatrix} 0 & 1 & \cdots & 0 \\ 0 & 0 & \cdots & 0 \\ .. & .. & \cdots & .. \\ -(a_1 + f_1^*) & -(a_2 + f_2^*) & \cdots & -(a_n + f_n^*) \end{bmatrix} \tag{5.39}$$

$$B^* = \begin{bmatrix} 0 & 0 & \cdots & F_o \end{bmatrix}. \tag{5.40}$$

The transfer function for the closed-loop system becomes

$$\frac{\hat{i}_k}{\hat{d}} = \frac{c_{kn}S^{n-1} + c_{kn-1}S^{n-2} + \cdots + c_{k1}}{S_n + (a_n + f_n^*)S^{n-1} + \cdots + (a_1 + f_1^*)} \qquad k = 1, \ldots, n_L \tag{5.41}$$

$$\frac{\hat{v}_j}{\hat{d}} = \frac{c_{jn}S^{n-1} + c_{jn-1}S^{n-2} + \cdots + c_{j1}}{S_n + (a_n + f_n^*)S^{n-1} + \cdots + (a_1 + f_1^*)} \qquad j = 1, \ldots, n_C \tag{5.42}$$

$$\frac{\hat{v}_o}{\hat{d}} = \frac{\hat{v}_{nC}}{\hat{d}}. \tag{5.43}$$

The transfer function for the closed-loop system has the same numerator as the transfer function for the open-loop system; therefore, current-mode control does not affect the system zeros. However, the poles of the closed-loop system are changed. Notice that the coefficients of the denominator changed from a_i to a_i^*.

$$\begin{aligned} a_i^* &= a_i + f^* \\ &= a_i - \sum_{k=1}^{n} f_k c_{ki} \qquad i = 1, \ldots, n \end{aligned} \tag{5.44}$$

where $a_i \geq 0$. While the value of f_k depends on the current-mode control equation, it could be positive or negative. If the converter power stage has RHP zeros, c_{ki} may be negative. Consequently, a_i^* may be negative; that means RHP POLES!

Furthermore, suppose the system transfer functions are

$$\frac{\hat{i}_1}{\hat{d}} = \frac{N_1(S)}{D(S)} \tag{5.45}$$

$$\cdots \tag{5.46}$$

$$\frac{\hat{i}_{n_L}}{\hat{d}} = \frac{N_{n_L}(S)}{D(S)} \tag{5.47}$$

$$\frac{\hat{v}_1}{\hat{d}} = \frac{N_{n_L+1}(S)}{D(S)} \tag{5.48}$$

$$\cdots \tag{5.49}$$

$$\frac{\hat{v}_{n_C}}{\hat{d}} = \frac{N_n(S)}{D(S)} \tag{5.50}$$

The control-to-output transfer function of the current-mode control system are expressed as

$$\frac{\hat{v}_o}{\hat{i}_{ref}} = \frac{F_o N_n(S)}{D(S) + f_1 N_1(S) + f_2 N_2(S) + \cdots + f_n N_n(S)} \tag{5.51}$$

$$= \frac{\frac{F_o N_n(S)}{D(S)}}{1 + \frac{f_1 N_1(S)}{D(S)} + \frac{f_2 N_2(S)}{D(S)} + \cdots + \frac{f_n N_n(S)}{D(S)}}. \tag{5.52}$$

where $\frac{f_i N_i(S)}{D(S)}$ is the loop-gain of the i-th state variable feedback loop, $i = 1, \ldots, n$. There are chances for RHP poles to occur for current-mode control. Since the state feedback

coefficients are determined by Equation (5.11), one cannot choose f_i, $1 \leq i \leq n$, freely; therefore, the pole rearrangement is rather restricted. If N_i, $1 \leq i \leq n$, has RHP zeros, and the associated feedback coefficient f_i is negative, the RHP zeros may transfer to RHP poles.

From the general model of current-mode control, it is evident that: Property 1. Current-mode control does not change the numerator of the transfer function for the converter.

Property 2. Current-mode control rearranges the pole positions of the converter. However, the rearrangement is restricted by the current-mode control function. Current-mode control does not necessarily improve the dynamic response of the system; in some cases, current-mode control may cause system oscillations.

5.3.1 Applying the General Model to Obtain the Closed-Loop Transfer Functions

The analysis discussed above also provides an efficient tool for finding the transfer function for the current-mode control loop.

The Buck Converter

A buck converter is shown in Fig. 5.5(a), and its small-signal model is shown in Fig. 5.5(b).

From the small-signal model, one finds:

$$\frac{\hat{i}_L}{d} = \frac{\frac{V_g}{R}(1+RCS)}{1+\frac{L}{R}S+LCS^2} \tag{5.53}$$

$$\frac{\hat{v}_o}{d} = \frac{V_g}{1+\frac{L}{R}S+LCS^2}. \tag{5.54}$$

Current-mode control yields the state-feedback function:

$$\hat{d} = F_o\hat{i}_{ref} - f_1\hat{i}_L - f_2\hat{v}_o \tag{5.55}$$

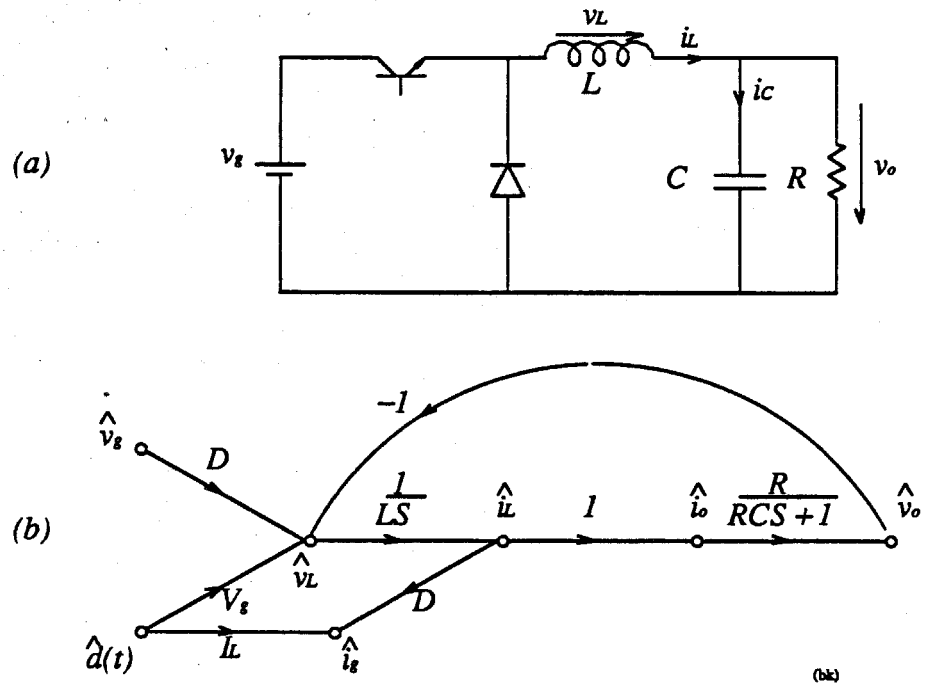


Figure 5.5: The Buck Converter and its Small-Signal Model. (a) The buck converter. (b) The small-signal model for the buck converter.

$$f_1 = +F_o \tag{5.56}$$

$$= \frac{2L}{nD'T_sV_g} \tag{5.57}$$

$$f_2 = -\frac{D}{nD'V_g} \tag{5.58}$$

The closed-loop transfer function of current-mode control is

$$\frac{\hat{v}_o}{\hat{i}_{ref}} = \frac{V_g}{1+\frac{L}{R}S+LCS^2+f_1\frac{V_g}{R}(1+RCS)+f_2V_g} \tag{5.59}$$

$$= \frac{V_g}{(1+f_1\frac{V_g}{R}+f_2V_g)+(\frac{L}{R}+f_1V_gC)S+LCS^2} \tag{5.60}$$

$$= \frac{V_g}{(1+\frac{2L}{nD'T_sR}-\frac{D}{nD'})+(\frac{L}{R}+\frac{2LC}{nD'T_s})S+LCS^2}. \tag{5.61}$$

Equation (5.55) shows that current-mode control actually introduces some positive feedback through f_2, and negative feedback through f_1. Since $| f_1c_{11} | \gg | f_2c_{21} |$, the positive feedback effect is negligible. Current-mode control improves the frequency response of

the buck converter.

The Boost Converter

The boost converter, shown in Fig. 4.1, has transfer functions of control-to-states:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{\frac{V_g}{D'^2}(1-\frac{L}{D'^2R}S)}{1+\frac{L}{D'^2R}S+\frac{LC}{D'^2}S^2} \tag{5.62}$$

$$\frac{\hat{i}_L}{\hat{d}} = \frac{\frac{2V_g}{RD'^3}(1+\frac{RC}{2}S)}{1+\frac{L}{D'^2R}S+\frac{LC}{D'^2}S^2}. \tag{5.63}$$

The current-mode control function for the boost converter is

$$\hat{d} = F_o i_{ref} - f_1\hat{i}_L - f_2\hat{v}_o \tag{5.64}$$

$$f_1 = F_o \tag{5.65}$$

$$= \frac{2L}{nT_sV_g} \tag{5.66}$$

$$f_2 = 0. \tag{5.67}$$

Notice that the only feedback state is the inductor current $\hat{i}_L$. The control-to-$\hat{i}_L$ does not have RHP zeros; therefore, current-mode control of the boost converter will not have RHP Poles. The closed-loop transfer function for current-mode control is

$$\frac{\hat{v}_o}{d} = \frac{\frac{V_g}{D'^2}(1-\frac{L}{D'^2R}S)}{1+\frac{L}{D'^2R}S+\frac{LC}{D'^2}S^2+f_1\frac{2V_g}{RD'^3}(1+\frac{RC}{2}S)} \tag{5.68}$$

$$= \frac{\frac{V_g}{D'^2}(1-\frac{L}{D'^2R}S)}{(1+f_1\frac{2V_g}{D'^3R})+(\frac{L}{D'^2R}+f_1\frac{V_gC}{D'^3})S+\frac{LC}{D'^2}S^2} \tag{5.69}$$

$$= \frac{\frac{V_g}{D'^2}(1-\frac{L}{D'^2R}S)}{(1+\frac{4L}{nT_sD'^3R})+(\frac{L}{D'^2R}+\frac{2LC}{nT_sD'^3})S+\frac{LC}{D'^2}S^2}. \tag{5.70}$$

Current-mode control breaks the high Q complex pole pair; hence, it improves the dynamic behavior of the system. However, the RHP zeros still remain.

5.4 Current-Mode Control of Converters with RHP Zeros

For a current-mode-controlled buck converter with input filter, as shown in Fig. 5.6, the power stage has control-to-state transfer functions:

$$\frac{\hat{i}_{L2}}{\hat{d}} = \frac{N_2(S)}{D(S)} = \frac{\frac{V_g}{DR}(1+RC_2S)(1+(C_1R_{L1}-\frac{D^2L_1}{R})S+L_1C_1S^2)}{D(S)} \tag{5.71}$$

$$\frac{\hat{v}_{C1}}{\hat{d}} = \frac{N_3(S)}{D(S)} = -\frac{\frac{V_gR_{L1}}{R}(1+\frac{L_1}{R_{L1}}S)(2+(\frac{L_2}{R}+RC_2)S+L_2C_2S^2)}{D(S)} \tag{5.72}$$

$$\frac{\hat{v}_o}{\hat{d}} = \frac{N_4(S)}{D(S)} = \frac{\frac{V_g}{D}(1+(C_1R_{L1}-\frac{D^2L_1}{R})S+L_1C_1S^2)}{D(S)} \tag{5.73}$$

The control-to-output transfer function has two RHP zeros. The control-to-i_{L2} transfer

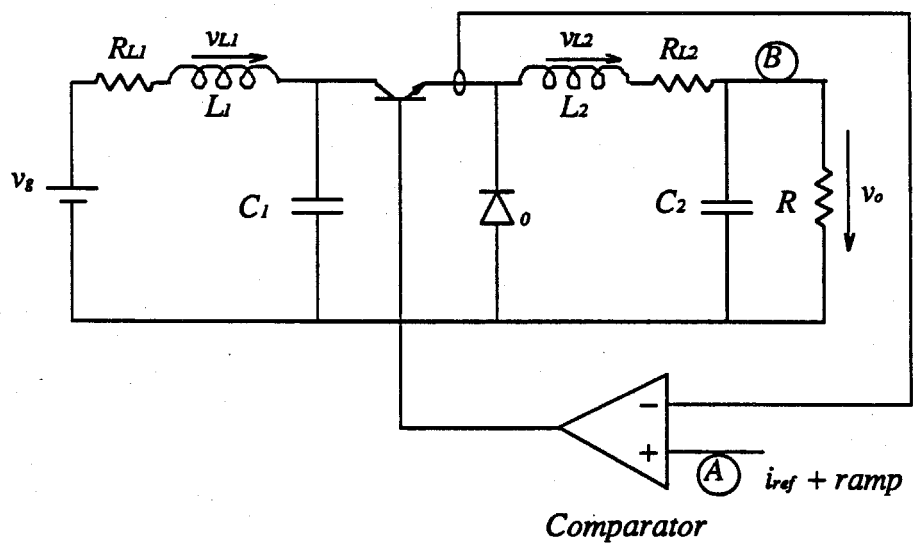


Figure 5.6: The Current-Mode-Controlled Buck Converter with Input Filter. The two access points, Point A and Point B, are used to inject the control signal and to detect the output signal, respectively.

function has two RHP zeros. The control-to-v_{C1} transfer function is negative.

The current-mode control yields the feedback equation

$$\hat{d} = F_o\hat{i}_{ref} - f_2\hat{i}_{L2} - f_3\hat{v}_{C1} - f_4\hat{v}_o \tag{5.74}$$

$$f_2 = F_o \tag{5.75}$$

$$= \frac{2}{nM_1T_s} \tag{5.76}$$

$$f_3 = -f_4 \tag{5.77}$$

$$= \frac{D}{nM_1L_2}. \tag{5.78}$$

States $\hat{i}_{L2}$, $\hat{v}_{C1}$, and v_o are fed back, with feedback coefficients, f_2, f_3, and f_4. The closed-loop transfer function is

$$\frac{\hat{v}_o}{\hat{i}_{ref}} = \frac{\frac{F_oN_4(S)}{D(S)}}{1 + \frac{f_2N_2(S)}{D(S)} + \frac{f_3N_3(S)}{D(S)} + \frac{f_4N_4(S)}{D(S)}}. \tag{5.79}$$

The loop-gain of the current i_{L2} feedback loop, the capacitor-voltage v_{C1} feedback loop, and the output-voltage v_0 feedback loop are:

$$T_2|_{S=0} = \frac{f_2N_2(S)}{D(S)}|_{S=0} \tag{5.80}$$

$$= \frac{2V_g}{nM_1T_sDR} \tag{5.81}$$

$$T_3|_{S=0} = \frac{f_3N_3(S)}{D(S)}|_{S=0} \tag{5.82}$$

$$= \frac{2V_gR_{L1}D}{nM_1L_2R} \tag{5.83}$$

$$T_4|_{S=0} = \frac{f_4N_4(S)}{D(S)}|_{S=0} \tag{5.84}$$

$$= \frac{V_g}{nM_1L_2} \tag{5.85}$$

For the circuit parameters $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

$$\frac{T_2|_{S=0}}{T_3|_{S=0}} = \frac{L_2}{D^2T_s} = 160 \tag{5.86}$$

$$\frac{T_2|_{S=0}}{T_4|_{S=0}} = \frac{2L_2}{DRT_s} = 9.2 \tag{5.87}$$

The loop-gain of the current feedback loop is much higher than the loop-gain of the voltage feedback loops. Therefore, the current feedback is dominant among all the state feedbacks of current-mode control. Current-mode control of the buck converter with an input filter is approximately equivalent to feedback control of the output inductor current with a feedback coefficient of $\frac{2}{nM_1T_s}$. This approximation is also true for other converters. Fig. 5.7 shows that the precise prediction, which considers all the state feedbacks, and the approximate prediction, which considers only the feedback of the output inductor current, are very close.

The control-to-v_{C1} transfer function is negative, and f_3 is also negative; therefore, the local v_{C1} feedback loop has positive feedback. The transfer functions $\hat{i}_{L2}/\hat{d}$ and $\hat{v}_o/\hat{d}$ have RHP zeros, these RHP zeros contribute to the closed-loop pole positions. However, the main effect of current-mode control is the feedback of the output inductor current. The closed-loop transfer function is approximately

$$\frac{\hat{v}_o}{\hat{i}_{ref}} = \frac{N_4(S)}{D(S) + f_2N_2(S)}. \tag{5.88}$$

Prediction 1. For the given parameters, when the duty-ratio $D < 0.24$, both $N_4(S)$ and $N_2(S)$ do not have RHP zeros. Consequently, the closed-loop transfer function $\frac{\hat{v}_o}{\hat{i}_{ref}}$ does not have RHP zeros or RHP poles.

Prediction 2. When the duty-ratio $0.24 < D < 0.3$, both $N_4(S)$ and $N_2(S)$ have RHP zeros. Consequently the closed-loop transfer function $\frac{\hat{v}_o}{\hat{i}_{ref}}$ has RHP zeros. Since the negative term of $N_2(S)$ is not very big, $D(S) + f_2N_2(S)$ cancels the negative term. Therefore, the closed-loop transfer function $\frac{\hat{v}_o}{\hat{i}_{ref}}$ does not have any RHP Poles.

Prediction 3. When the duty-ratio $D > 0.3$, both $N_4(S)$ and $N_2(S)$ have RHP zeros, and the negative term of $N_2(S)$ cannot be cancelled in $D(S) + f_2N_2(S)$. Consequently,

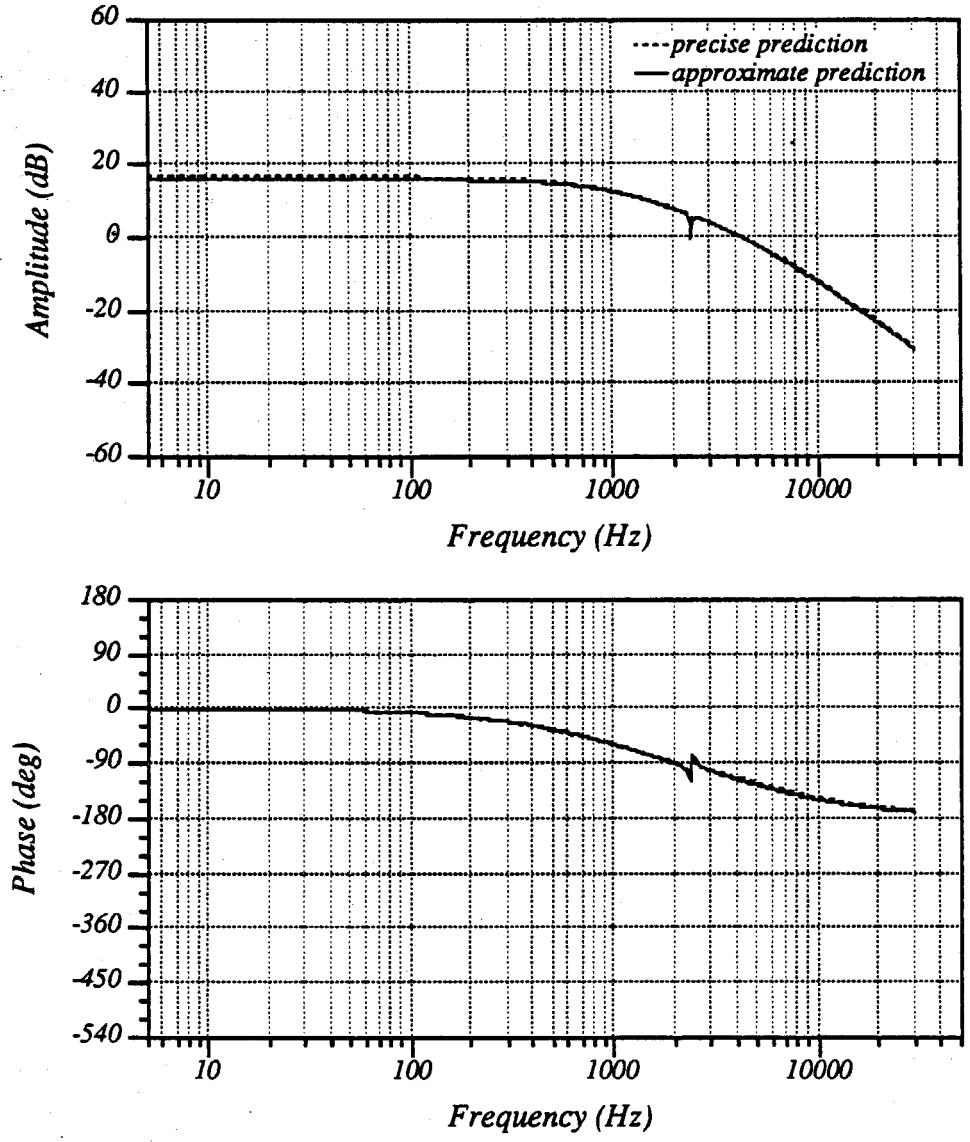


Figure 5.7: Frequency Response of the Current-Mode-Controlled Buck Converter with Input Filter. The approximate prediction and the precise prediction, when $D = 0.2$. The operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

the closed-loop transfer function $\frac{\hat{v}_o}{i_{ref}}$ has RHP zeros and RHP poles. The system is not stable.

Prediction 4. If the damping circuit is used to eliminate the RHP zeros of $N_4(S)$ and $N_2(S)$, the closed-loop transfer function $\frac{\hat{v}_o}{i_{ref}}$ will not have RHP zeros or RHP poles.

Experiments were conducted to verify the predictions for the current-mode controlled buck converter with an input filter. The HP 3577 network analyzer was used to measure the frequency response. A frequency sweeping signal, from $5Hz$ to $30kHz$, was injected at Point A and the responses at Point B were detected to determine $\frac{\hat{v}_o}{i_{ref}}$.

Experiment 5.1 The measured and the predicted frequency response, for the circuit parameters $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$, and $D = 0.2$, are plotted in Fig. 5.8. Both the measurement and the prediction show that no RHP zeros exist, therefore, the system is stable.

Experiment 5.2 For the same circuit parameters, the duty-ratio D was increased to 0.29. The measured and the predicted frequency response are plotted in Fig. 5.9. Both the measurement and the prediction illustrate the existence of two RHP zeros. Since there is no RHP pole, the system is stable. The window in which the RHP zeros were detected was very small, from $D = 0.24$ to $D = 0.3$.

Experiment 5.3 For the same circuit parameters, the duty-ratio D was further increased. When $D > 0.3$, the prediction shows two RHP zeros and two RHP poles. The real circuit oscillated.

Experiment 5.4 A damping circuit was added to the experimental circuit shown as Fig. 4.6. $C_D = 100\mu F$ and $R_D = 51\Omega$. The open-loop buck converter does not have any RHP zeros, as predicted and detected in Chapter 4. The prediction and measurement,

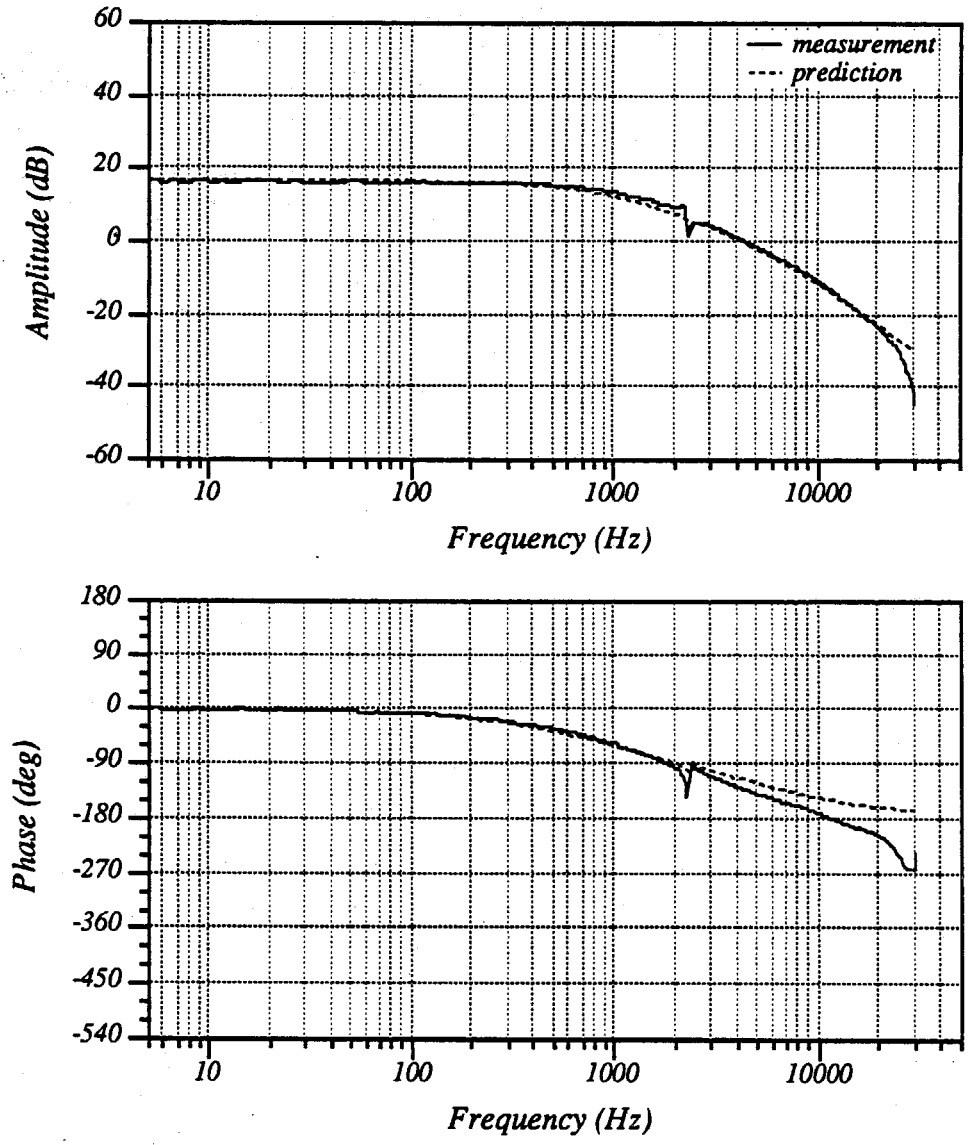


Figure 5.8: The Frequency Response of the Current-Mode-Controlled Buck Converter with Input Filter. The measurement and prediction, when $D = 0.2$. The operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

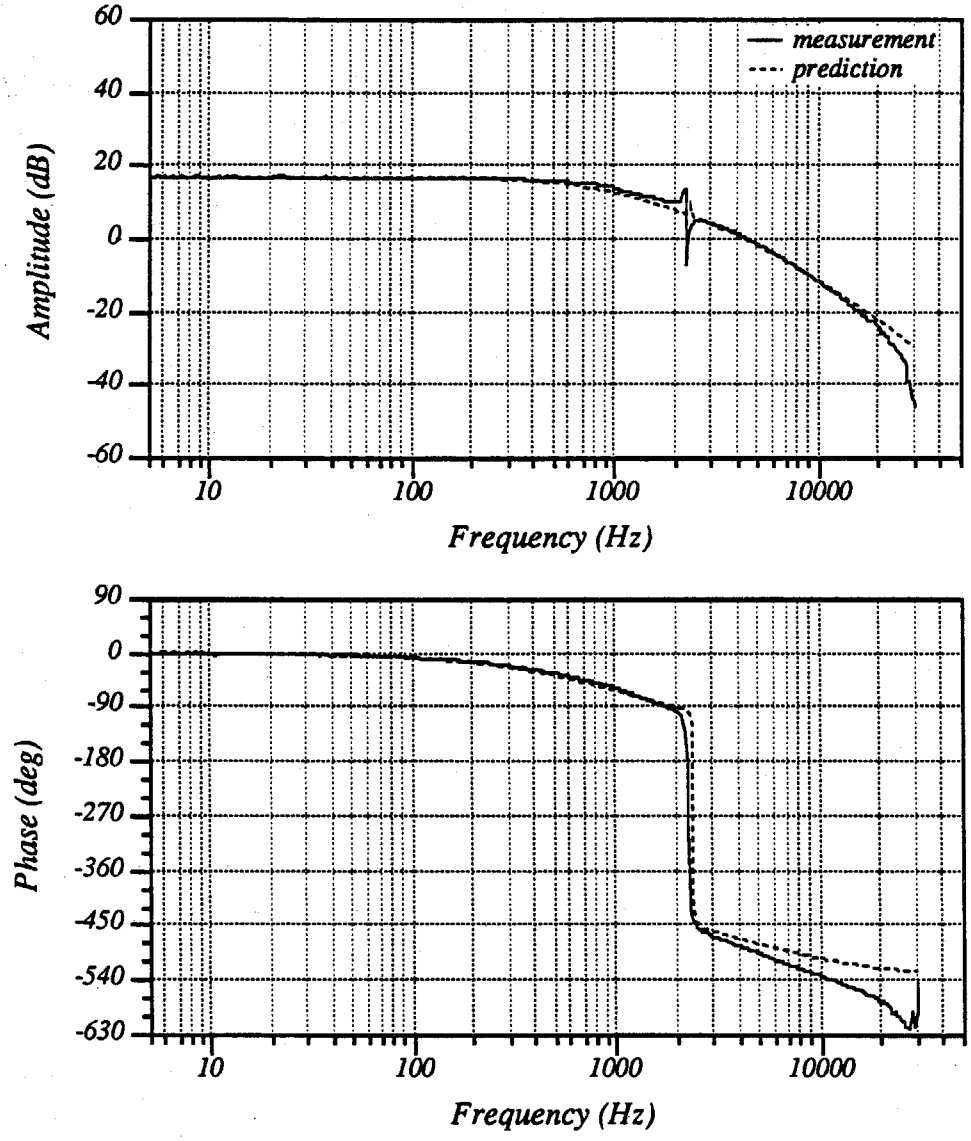


Figure 5.9: The Frequency Response of the Current-Mode Controlled Buck Converter with Input Filter. The measurement and prediction when $D = 0.29$. The operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

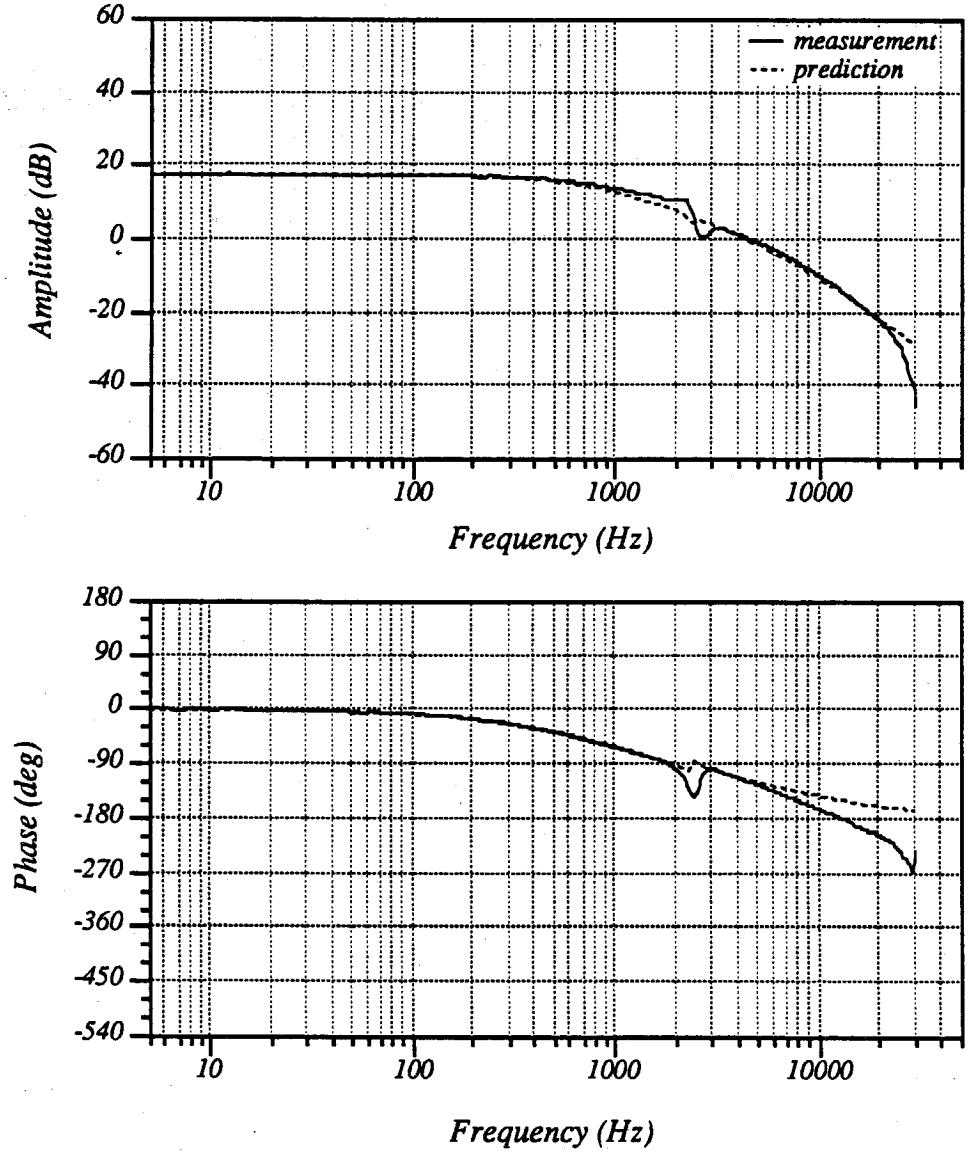


Figure 5.10: The Frequency Response of the Current-Mode Controlled Buck Converter with Input Filter. The measurement and prediction, when $D = 0.44$. The operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 10.4\Omega$.

Fig. 5.10, show that the closed-loop transfer function $\frac{\hat{v}_o}{\hat{i}_{ref}}$ does not have RHP zeros or RHP poles when the duty ratio $D > 0.44$.

The experiments verified the theoretical predictions. Conclusion: For a converter in the fourth-order family, if the operating region requires a very small D such that the resistor of the input inductance is large enough to eliminate the RHP zeros, then the current-mode control loop is stable. If the operating region requires a large D such that the input resistor cannot eliminate the RHP zeros, the current-mode control loop may oscillate. However, if a damping circuit is used to eliminate the RHP zeros, the current-mode control loop is stable, even when D is large.

5.5 Summary

The small-signal model of current-mode control is equivalent to the state-feedback control function. The RHP zeros of the switching converters are not removed with current-mode control. The poles of the switching converters are relocated. However, the poles can not be relocated to arbitrary positions, because the choice of the coefficients is restricted by the control functions. Among all the feedback states, the switch-current feedback is dominant, whereas others can be ignored for quantitative understanding. The RHP zeros in the transfer functions of control-to-inductor currents may be converted to RHP poles, by increasing the feedback coefficient. The RHP poles cause loop oscillations. Hence, if the RHP zeros are eliminated by a damping circuit using the damping criteria found in Chapter 4, switching converters with current-mode control loops can be made stable. Experiments verified the prediction.

Part II

One-Cycle Control Technique

Chapter 6

One-Cycle Control Technique

Switches are pulsed and non-linear elements, yet they have found wide use in the signal processing and the power processing, that is because digital signal processing has a much better signal-to-noise ratio than analog signal processing, and because switching power supplies have much lower power losses than analog power supplies. Switches are very important components in science and technology applications.

Switches usually operates at a much higher frequency than the information signal or the power signal that they modulate. The effective signal, the average signal, carried in the switch output is the product of the input signal and duty-ratio control signal; therefore, switches are non-linear components. In this chapter, a new switching technique is conceived, which fully rejects the input signal and linearly all-passes the duty-ratio control signal. This new switching technique changes the dynamics of the switching circuits. It can be applied to power processing and may be useful for signal processing as well.

The general concept of One-Cycle Control is introduced in Section 6.1. The implementation technique is discussed for the constant frequency switches, the constant ON-time switches, the constant OFF-time switches and the variable switches in Section 6.2. Among these four switches, the constant frequency switch is most commonly used; therefore, it is used as an example to further describe the One-Cycle Control process in Section 6.3 in order to achieve deeper physical understanding.

6.1 General Concept of One-Cycle Control

A switch, constant frequency, constant ON-time, constant OFF-time, or variable, as defined in Chapter 2, operates according to the switch function $k(t)$.

$$k(t) = \begin{cases} 1 & 0 < t < T_{ON} \\ 0 & T_{ON} < t < T_s \end{cases} \tag{6.1}$$

In each cycle, the switch stays ON for a time duration of T_{ON} and stays OFF for a time duration of T_{OFF}. The duty-ratio $d = \frac{T_{ON}}{T_s}$ is modulated by an analog control signal $v_{ref}(t)$. The input signal to the switch is $x(t)$. The switch chops the input signal. The frequency and the pulse width of $y(t)$ is the same as that of the switch function $k(t)$, while the envelope of $y(t)$ is $x(t)$, as shown in Fig. 6.1.

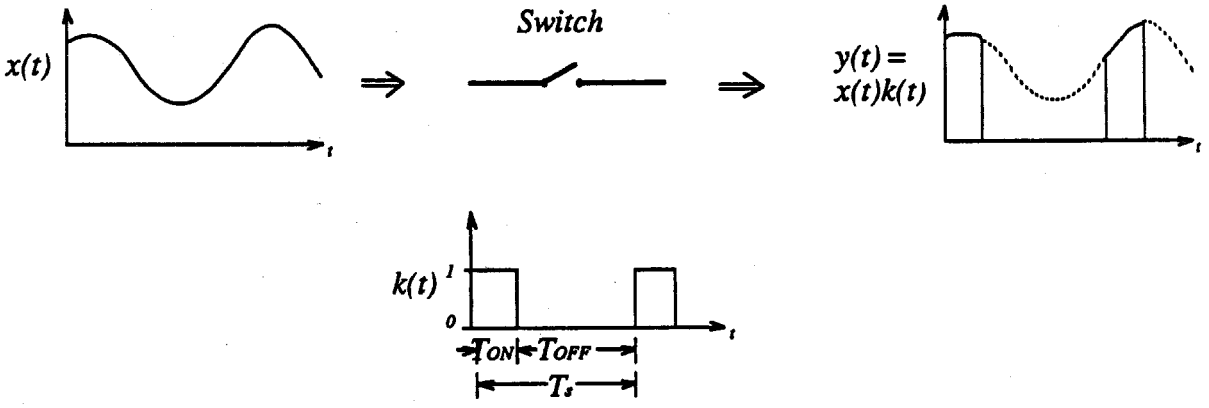


Figure 6.1: The Switch. The input signal to the switch is $x(t)$ and the switch chops the input signal. Therefore, the output signal of the switch is $y(t) = k(t)x(t)$.

Suppose the switch frequency f_s is much higher than the frequency bandwidth of either the input signal $x(t)$ or the control signal $v_{ref}(t)$. According to the analysis in Chapter 2, the effective signal carried in the switch output is

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)dt \tag{6.2}$$

$$\approx x(t)\frac{1}{T_s}\int_0^{T_{ON}} dt \tag{6.3}$$

$$= x(t)d(t) \tag{6.4}$$

$$= x(t)v_{ref}(t) \tag{6.5}$$

The output signal $y(t)$ of the switch is the product of the input signal $x(t)$ and the control signal $v_{ref}(t)$; therefore, the switch is nonlinear. If the control signal $v_{ref}(t)$ is constant, for example $v_{ref}(t) = D$, the output signal of the switch is $Dx(t)$, which is the case when the switch is used for digital signal processing. In power processing applications, for example a power amplifier, the input $x(t)$ usually represents the power, while the control signal $v_{ref}(t)$ represents the signal to be amplified. In ideal case the input power $x(t)$ is constant X; therefore, the output signal $y(t) = Xv_{ref}(t)$. However, in reality there are always perturbations in the input power $x(t)$, hence the output signal $y(t)$ contains the power disturbance signal as well.

If the duty-ratio of the switch is modulated such that in each cycle the integration of the chopped waveform at the switch output is exactly equal to the integration of the control signal, ie.

$$\int_0^{T_{ON}} x(t)dt = \int_0^{T_s} v_{ref}(t)dt, \tag{6.6}$$

then the average value of the chopped waveform at the switch output is exactly equal to the average value of the control signal in each cycle.

$$\frac{1}{T_s}\int_0^{T_{ON}} x(t)dt = \frac{1}{T_s}\int_0^{T_s} v_{ref}(t)dt. \tag{6.7}$$

Therefore, the output signal is instantaneously controlled within one cycle, ie.

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)dt = \frac{1}{T_s}\int_0^{T_s} v_{ref}(t)dt = v_{ref}(t) \tag{6.8}$$

The technique to control switches according to this concept is defined as the One-Cycle

Control technique. With One-Cycle Control, the effective output signal of the switch is

$$y(t) = v_{ref}(t). \tag{6.9}$$

The switch fully rejects the input signal and linearly all-passes the control signal v_{ref}; therefore, the One-Cycle Control technique turns a non-linear switch into a linear switch.

6.2 One-Cycle Controlled Switches

The implementation circuits are found for any type of switch, constant frequency, constant ON-time, constant OFF-time, and variable.

6.2.1 One-Cycle Control of Constant Frequency Switches

For a constant frequency switch, T_s is constant. The object of One-Cycle Control is to adjust the switch ON-time T_{ON} in each cycle, such that the integrated value of the chopped waveform is constant.

The implementation circuit for One-Cycle Control of constant frequency switches is shown in Fig. 6.2. The key component of the One-Cycle Control technique is the real-time integrator. The real-time integration is started the moment when the switch is turned ON by the fixed frequency clock pulse. The integration value, $v_{int} = \frac{1}{T_s}\int_0^t x(t)dt$, is compared with the control signal $v_{ref}(t)$ in real time. At the instant when the integration value v_{int} reaches the control signal $v_{ref}(t)$, the controller sends a command to the switch, which forces the switch to change from the ON state to the OFF state. At the same time, the controller resets the real-time integrator to zero to prepare for the next cycle. The duty-ratio d of the present cycle is determined by the following equation:

$$\frac{1}{T_s}\int_0^{dT_s} x(t)dt = v_{ref}(t) \tag{6.10}$$

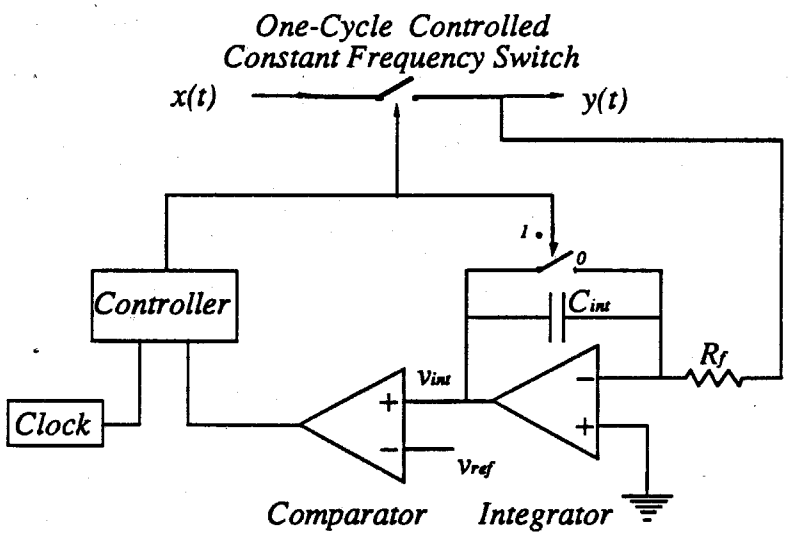


Figure 6.2: The One-Cycle Controlled Constant Frequency Switches. This circuit contains a real-time integrator, a comparator, a constant frequency clock, and a controller. The controller can be implemented by an RS Flip-Flop. The real-time integrator is the key component.

Since the switch period T_s is constant and the duty-ratio is controlled, the average value of the waveform at the switch output $y(t)$ is guaranteed to be

$$y(t) = \frac{1}{T_s}\int_0^{dT_s} x(t)dt = v_{ref}(t) \tag{6.11}$$

in each cycle. Fig. 6.3 shows the operating waveforms of the circuit.

6.2.2 One-Cycle Control of Constant ON-Time Switches

For a constant ON-time switch, T_{ON} is constant. The object of One-Cycle Control is to adjust the OFF-time T_{OFF} in each cycle, such that the average value of the chopped waveform is constant.

The implementation circuit for One-Cycle Control of constant ON-time switches is shown in Fig. 6.4. The real-time integration is started at the moment when the switch

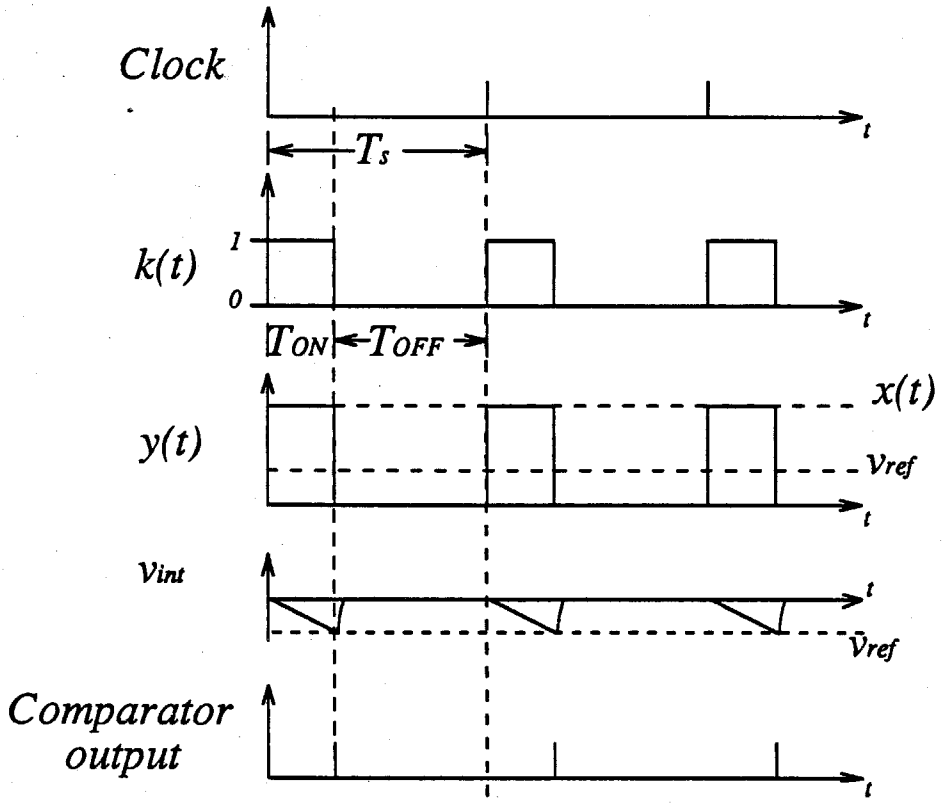


Figure 6.3: The Waveform of One-Cycle Controlled Constant Frequency Switches. The real-time integration is started at the moment when the switch is turned ON by the fixed frequency clock pulse. The integration value $v_{int} = \frac{1}{T_s}\int_0^t x(t)dt$ is compared with the control signal $v_{ref}(t)$ in real time. At the instant when the integration value v_{int} reaches the control signal $v_{ref}(t)$, the controller sends a command to the switch that forces the switch to change from the ON state to the OFF state. At the same time, the controller resets the real-time integrator to zero to prepare for the next cycle.

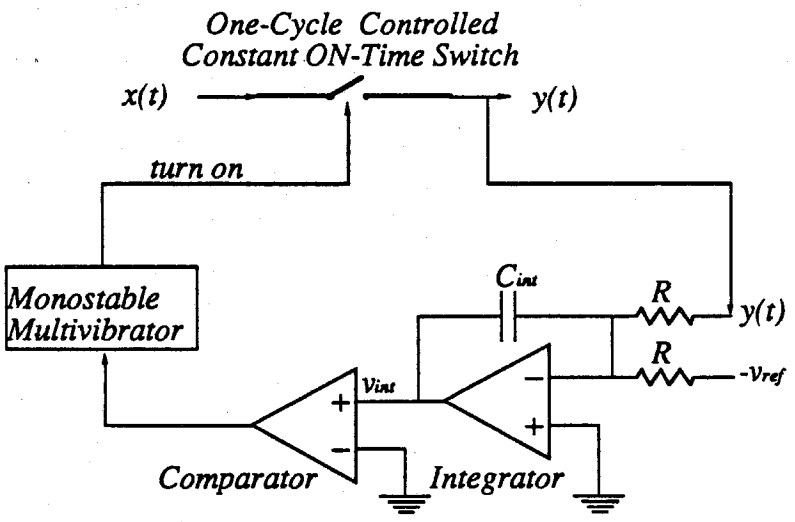


Figure 6.4: The One-Cycle Controlled Constant ON-Time Switches. This circuit contains a real-time integrator, a comparator, and a monostable multivibrator. The real-time integrator is the key component.

is turned ON. From $t = 0$ to $t = T_{ON}$, the switch is ON, so the integration value

$$v_{int} = \int_0^t v_{ref}(t)dt - \int_0^t x(t)dt \tag{6.12}$$

deceases. The monostable multivibrator has a constant pulse width. When the monostable multivibrator changes its state from high to low, the switch is turned OFF. From $t = T_{ON}$ to T_s, the switch is OFF, so the integration value

$$v_{int} = \int_0^t v_{ref}(t)dt - \int_0^{T_{ON}} x(t)dt \tag{6.13}$$

increases. At the instant when v_{int} reaches zero, the comparator changes its state from low to high, which triggers the monostable multivabrator to high and turns the switch ON. The present switching cycle is completed. The switch starts the next cycle.

The OFF-time T_{OFF} of the present cycle is determined by the following equation:

$$\int_0^{T_{ON}} x(t)dt = (T_{ON} + T_{OFF})v_{ref}(t) \tag{6.14}$$

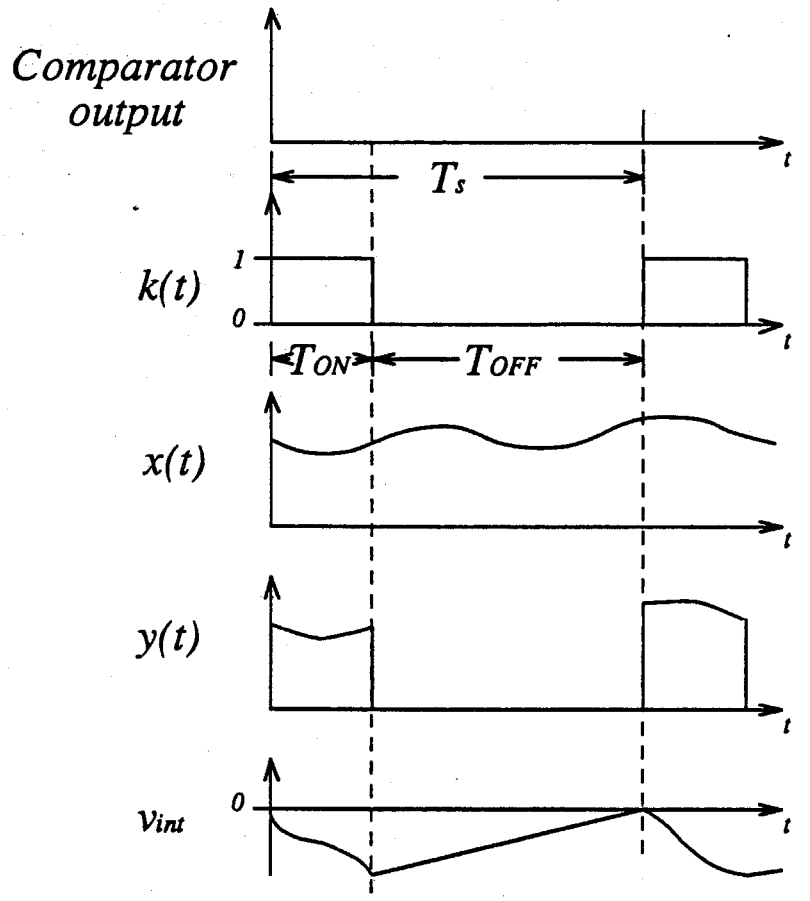


Figure 6.5: The Waveform of One-Cycle Controlled Constant ON-Time Switches. The real-time integration is started the moment when the switch is turned on. The integration value $v_{int} = \int_0^t x(t)dt - \int_0^t v_{ref}(t)dt$ starts to decrease. The monostable multivibrator has a constant pulse width. When the monostable multivibrator changes its state from high to low, the switch is turned OFF. Then the integration value $v_{int} = \int_0^t v_{ref}(t)dt - \int_0^{T_{ON}} x(t)dt$ increases. At the instant when v_{int} reaches zero, the comparator changes its state from low to high, which triggers the monostable multivibrator to high and turns the switch ON. The switch starts the next cycle.

The waveform at the switch output $y(t)$ is guaranteed to be

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)dt = v_{ref}(t). \tag{6.15}$$

where T_s is time dependent and T_{ON} is constant. Fig. 6.5 shows the operating waveforms of the circuit.

6.2.3 One-Cycle Control of Constant OFF-Time Switches

For a constant OFF-time switch, T_{OFF} is constant. The object of One-Cycle Control is to adjust the ON-time T_{ON} in each cycle, such that the average value of the chopped waveform is constant.

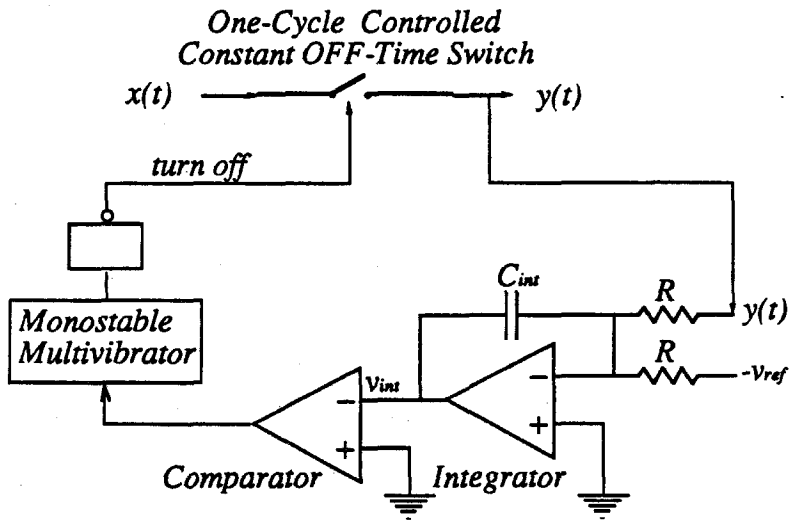


Figure 6.6: The One-Cycle Controlled Constant OFF-Time Switches. This circuit contains a real-time integrator, a comparator, and a monostable multivibrator. The real-time integrator is the key component.

The implementation circuit for One-Cycle Control of constant OFF-time switches is shown in Fig. 6.6. The real-time integration is started the moment when the switch is turned OFF. From $t = 0$ to $t = T_{OFF}$, the integration value

$$v_{int} = \int_0^t v_{ref}(t)dt \tag{6.16}$$

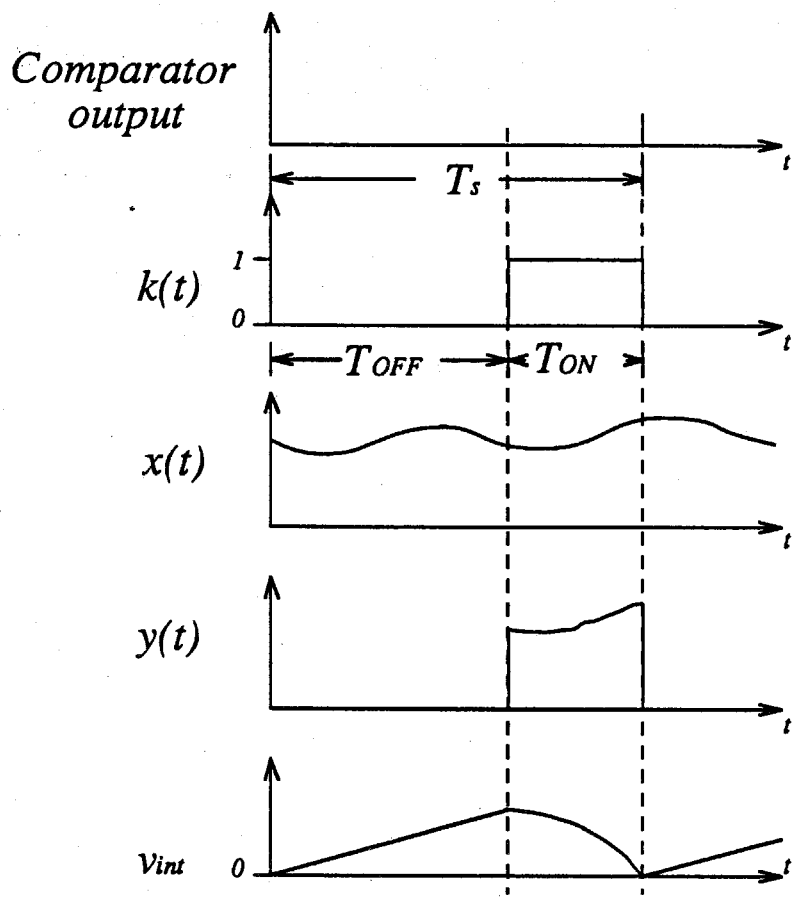


Figure 6.7: The Waveform of One-Cycle Controlled Constant OFF-Time Switches The real-time integration is started the moment when the switch is turned off. The integration value $v_{int} = \int_0^t v_{ref}(t)dt$ starts to grow. The monostable multivibrator has a constant pulse width. When the monostable multivibrator changes its state from high to low, the switch is turned ON. The integration value $v_{int} = \int_0^t v_{ref}(t)dt - \int_{T_{OFF}}^{T_{OFF}+t} x(t)dt$ is compared with zero in real-time. At the instant when v_{int} reaches zero, the comparator changes its state from low to high, which triggers the monostable multivibrator to high and turns the switch OFF. The switch starts the next cycle.

grows. The monostable multivibrator has a constant pulse width. When the monostable multivibrator changes its state from high to low, the switch is turned ON. From $t = T_{OFF}$ to $t = T_s$, the integration value

$$v_{int} = \int_0^t v_{ref}(t)dt - \int_{T_{OFF}}^{T_{OFF}+t} x(t)dt \tag{6.17}$$

decreases. At the instant when v_{int} reaches zero, the comparator changes its state from low to high, which triggers the monostable multivabrator to high and turns the switch OFF. The present switching cycle is completed. The switch starts the next cycle.

The ON-time T_{ON} of the present cycle is determined by the following equation:

$$\int_0^{dT_s} x(t)dt = (T_{ON} + T_{OFF})v_{ref}(t) \tag{6.18}$$

Since the OFF-time T_{OFF} of the switch is constant and the ON-time T_{ON} is controlled, the average value of the waveform at the switch output $y(t)$ is guaranteed to be

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)dt = v_{ref}(t) \tag{6.19}$$

in each cycle. Fig. 6.7 shows the operating waveforms of the circuit.

6.2.4 One-Cycle Control of Variable Switches

For a variable switch, there are two adjustable dimensions, T_{ON} and T_{OFF}. Usually, one dimensions is governed by the particular application. If a particular application requires the ON-time vary in a particular pattern, then the One-Cycle Control can be implemented in an approach similar to the one described for the constant ON-time switches. If a particular application restricts the OFF-time by some function, then the One-Cycle Control can be implemented in an approach similar to the one described for the constant OFF-time switches.

6.3 One-Cycle Control Operating Process

The most commonly used constant frequency switch is used as an example to demonstrate the operating process of One-Cycle Control. The principle control function can be described by a speed, time, and distance triangle rule, as shown in Fig. 6.8.

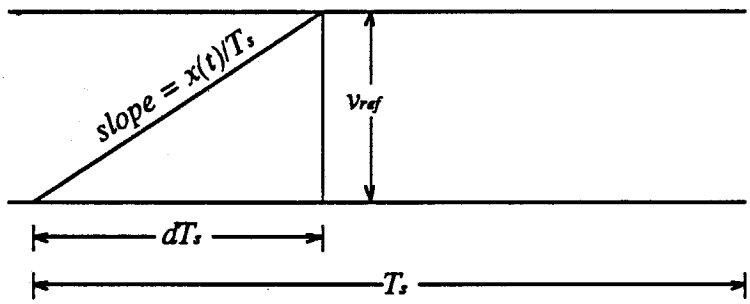


Figure 6.8: The Triangle Rule of Constant Frequency One-Cycle Control. The amplitude of the input signal $x(t)$ determines the slope, which is the speed of the integration. The control signal v_{ref} determines the distance that the integration value must travel to reach the control signal. The speed and the distance determine the time dT_s required for the integration to reach the control signal.

Suppose the control signal is constant while the input signal changes. The waveform at the switch output is the same as the input signal, when the switch is in the ON state; and the signal at the switch output is zero, when the switch is in the OFF state. Any input signal perturbation that occurs during the ON state immediately influences the slope of the real-time integration. Consequently, it affects the speed at which the integration value reaches the control signal. Since the control signal is constant, the time dT_s, for the real-time integration value to reach the control signal, is directly controlled by the input signal. No matter how the input signal changes, the chopped waveform at the switch output has a constant average value that is equal to the control signal in each cycle, as shown in Fig. 6.9.

Suppose the input signal is constant, and the control signal changes; for example,

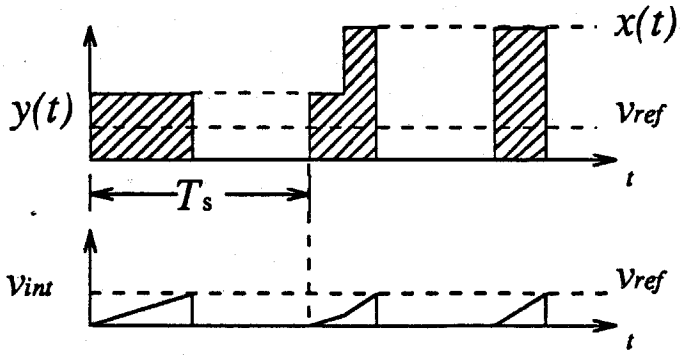


Figure 6.9: Input Signal Perturbation is Rejected by One-Cycle Control. The input signal perturbation directly controls the slope of the real-time integration and consequently controls the time dT_s for the integration value to reach the control signal. The average value of the chopped waveform is always equal to the control signal. It rejects the input signal perturbation in one cycle.

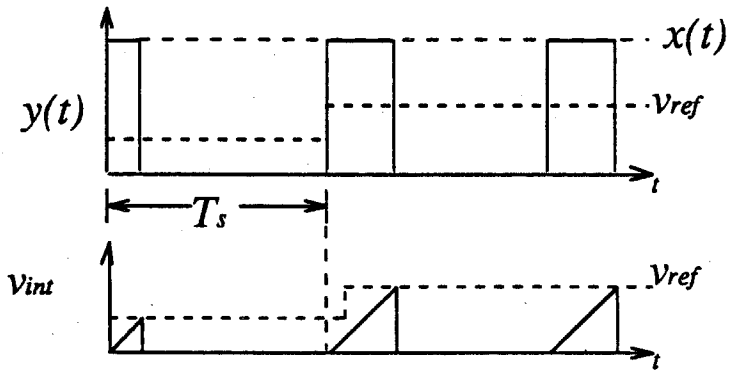


Figure 6.10: Follow the Control Signal in One Cycle. When the control signal steps up, the integration value takes a longer time to reach the control signal. The duty-ratio d is determined when the integration value reaches the control signal, so that the average value of the chopped waveform keeps up with the new control signal in one cycle.

a step up. The real-time integration keeps the same slope since the input signal is constant; therefore, the speed at which the integration value reaches the control signal is constant. However, when the control signal changes to a higher value, the distance that the integration value must travel to reach the control signal is increased. As a result, a longer time dT_s is required for this cycle. The average value of the chopped waveform, in this cycle, is exactly equal to the stepped-up control signal. No matter how the control signal changes, the average value of the chopped waveform follows the control signal immediately, within one cycle, as shown in Fig. 6.10.

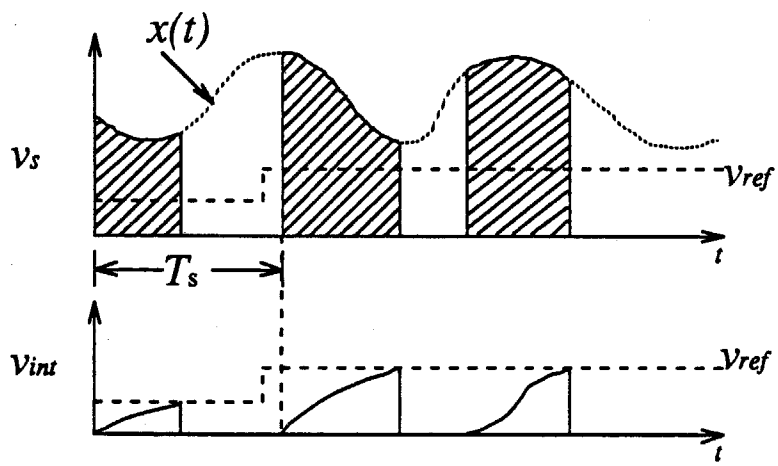


Figure 6.11: Follow the Control Signal and Reject the Input Signal Perturbation. The control signal steps up. Under the circumstance the input signal is perturbed. The slope of the integration is changing with time. When the integration value reaches the new control signal value, the switch changes its state. The average value of the chopped waveform $y(t)$ is changed such that is remains exactly equal to the new control signal.

Suppose both the input signal and the control signal are varying. According to the triangle rule of One-Cycle Control, both the speed and the distance are varying. The average value of the chopped waveform is not affected by the input signal perturbation, and it follows the control signal in one cycle, as shown in Fig. 6.11. One-Cycle Control

completely rejects input disturbances and enables the output to immediately follow the control signal within one cycle.

The pulse width of the One-Cycle Controlled constant frequency switch is modulated by a combined effect of the control signal $v_{ref}(t)$ and the input signal $x(t)$. The One-Cycle Controlled switch fully rejects the input signal $x(t)$, and all passes the modulation signal $v_{ref}(t)$. As a result, the control signal and the output signal of One-Cycle Controlled switches are linearly related.

6.4 Summary

The general concept of One-Cycle Control is to adjust the duty-ratio in real time such that the average value of the chopped waveform at the switch output is exactly equal to the control reference in each cycle. The implementation technique is found for any type of switch, constant frequency switches, constant ON-time switches, constant OFF-time switches, and variable switches. The One-Cycle Control technique converts a nonlinear switch into a linear switch that fully rejects the input signal and all-passes the control signal.

The most direct applications of the One-Cycle Control technique are found for the control of switching converters, both the pulse-width-modulated (PWM) converters and the quasi-resonant converters.

The One-Cycle Controlled switch is a useful component for power amplifiers. The perturbations from the power supply would be fully rejected, and the control signal would be linearly transfered to the switch output.

The One-Cycle Controlled switches would also be very useful for motor driving. The input power would be converted to a pulsed voltage for the motor. The pulse voltage would carry a signal exactly equal to the control signal $v_{ref}(t)$. The switching frequency

harmonics would be attenuated by the armature inductance. Any perturbation from the power line would be fully rejected.

One-Cycle Control might also find some use in signal processing systems.

Chapter 7

One-Cycle Control of Pulse-Width-Modulated Switching Converters

The most direct applications of the One-Cycle Control technique are found in the control of switching converters, which includes both the pulse-width-modulated (PWM) converters and the quasi-resonant converters. According to the analysis in Chapter 6, any switches operating with a switching function $k(t)$ can be One-Cycle Controlled. For a given switching converter, the diode-voltage and the transistor current naturally satisfy this condition. In this chapter, the One-Cycle Control technique is used to control the constant frequency PWM switching converters, with the buck converter as the example. The most desirable properties of the control loop are described in Section 7.1; these are the goals of control-loop design in the following sections. The One-Cycle Controlled buck converter is analyzed, in Section 7.2. The effects of the input filter on the One-Cycle Control function are discussed in Section 7.3, and the effects of the output filter on One-Cycle Control function are discussed in Section 7.4. In Section 7.5, the One-Cycle Control function is compared with the PWM feedback control and the current-mode control schemes. Section 7.6 outlines the experimental results.

7.1 Task of Control Loops

The capability to reject input-voltage perturbations, to recover from load disturbances, and to follow the control reference are the most important evaluations of the control technique of switching converters.

Most electrical equipment uses DC power that is converted from the line power, which contains perturbations, such as line-frequency harmonics, neighbor-load transients, and/or high frequency electromagnetic field disturbances, etc. A desirable switching converter must have the capability to reject the input-voltage perturbations so that its loads are not subjected to input perturbations. This rejection is especially important for power supplies used in scientific experiments. For example, a particle accelerator ring uses magnetic fields to provide centripetal force which enables the particle beams to travel around the ring. The ring needs very stable DC power supplies for its magnets. Any ripple in the output of the power supplies will generate perturbations in the magnetic field. These perturbations cause the particles to become unstable inside the accelerator tube. Consider a switching converter that has power conversion $v_o = M(d)v_g$, where v_o is the output voltage, v_g is the input voltage, and $M(d)$ is the DC gain that is a function of the duty-ratio d. If the input voltage v_g is perturbed, the duty-ratio d should be adjusted such that the output voltage v_o is not disturbed. To reject an input voltage perturbation, the control circuit must diagnose the perturbation quickly before it sends its command to the duty-ratio. Since switching converters are dynamical systems, the design of the control circuit is very subtle. Different control schemes have very different rejection capabilities.

In many applications, the output voltage of the switching converters needs to be controlled. For example, the output power of the DC power supplies for the magnets of the particle accelerator must be increased as the particles gain energy in order to keep

the particles inside the beam tube.

Load disturbance rejection is another important aspect of a switching power supply. Some loads, such as computers, have pulsed current that influences the output of the switching power supply. A good control technique should enable the output voltage to recover from load disturbances quickly.

The One-Cycle Control technique is conceptually different from the classical PWM feedback control and the current-mode control. With One-Cycle Control, a converter is able to reject the input-voltage perturbations, to quickly follow the control reference, and to recover from a load disturbance.

7.2 One-Cycle Control

The simplest configuration, buck converter, shown in Fig. 7.1, is used as an example to study the features of One-Cycle Controlled PWM converters. The switch S is operated repetitively with constant frequency f_s. It is in position 1, defined to be the ON state, for a fraction d of the period $T_s = \frac{1}{f_s}$. Consequently, a voltage equal to the DC line input voltage v_g appears at the switch output. When the switch is in position 0, defined to be the OFF state, the voltage at the switch output is zero. The DC line-input voltage is chopped by the switch S resulting in a chopped waveform v_s at the switch output. The average, or DC, of this waveform is V_s.

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s dt = \frac{1}{T_s}\int_0^{dT_s} v_s dt \tag{7.1}$$

The LC low-pass filter transmits this value to the output while rejecting most of the undesired switch frequency f_s. Therefore, the output voltage contains the desired DC value dv_g and a small residual switch ripple. Here d is defined as the duty-ratio. The buck converter has a conversion rate equal to its duty-ratio d. By controlling the duty-ratio d, the output DC voltage is controlled, as shown in Fig. 7.2.

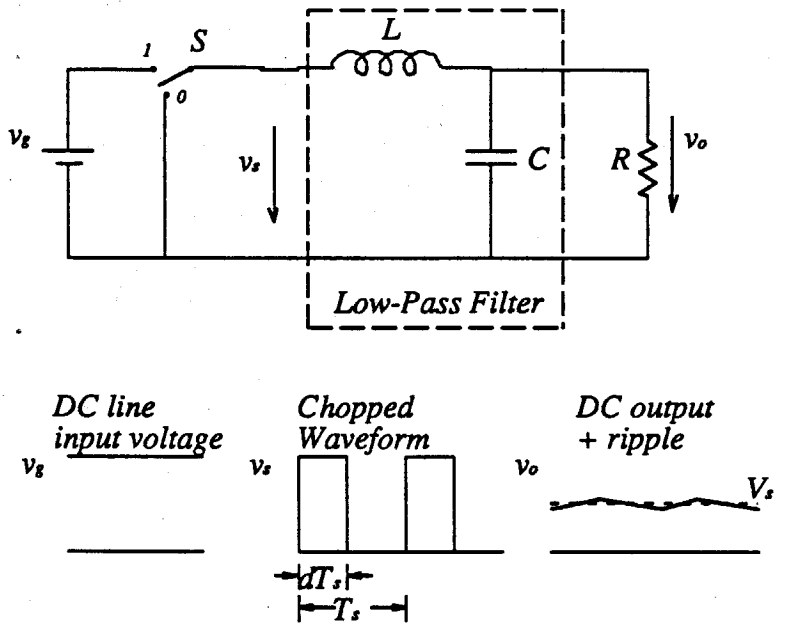


Figure 7.1: The Buck Converter. The DC line input voltage is v_g. The Switch S is operated at a fixed frequency f_s and with a duty-ratio d. The waveform at the switch output is v_s. The inductor L and the capacitor C compose a low-pass filter. The output voltage is v_o.

The buck converter has one switch in its signal path, from the duty-ratio control signal to the output voltage, as shown in Fig. 3.2. This signal switch is implemented by a transistor and a diode in the real circuit. The input signal of the switch is the input voltage. The output signal of the switch is the diode-voltage. One-Cycle Control is designed to control the duty-ratio d in real time, such that in *each cycle* the average value of the diode-voltage is *exactly* equal to the control reference.

Fig. 7.3 shows the One-Cycle Controlled buck converter. The diode-voltage is fed back to the real-time integrator. The integration is started when the clock turns the transistor ON. The integration value is compared with the control reference in real time. When the output voltage of the integrator reaches the control reference, the transistor is turned OFF. Fig. 7.4 shows the chopped waveform at the switch output, which is the

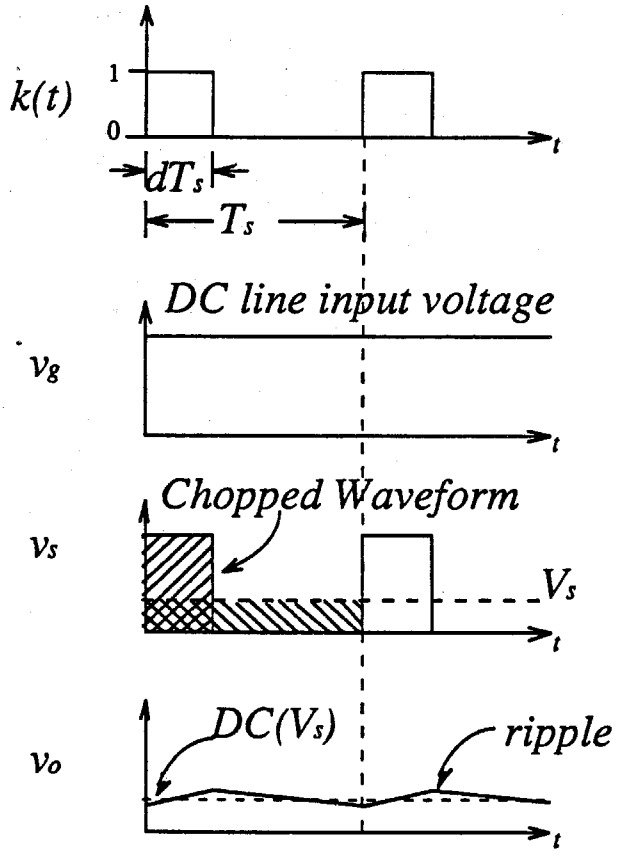


Figure 7.2: The Working Waveforms of the Buck Converter. The switch operating duty-ratio is d. The input voltage waveform is v_g. The switch pulsed waveform is v_s with its average waveform V_s in the dashed line. The output voltage v_o equals V_s.

voltage across the diode v_s. When the transistor is on, the diode is off, and the diode-voltage v_s is equal to the input voltage. When the transistor is off, the diode is on, and the diode-voltage v_s is zero.

In each cycle, the diode-voltage waveform may be different; however, as long as the area under the diode-voltage waveform in each cycle is the same as the control reference signal, the instantaneous control of the diode-voltage v_s is achieved, as shown in Fig. 7.4.

The control strategy is as follows: The transistor is turned ON at the clock pluse and it is shutted OFF when the diode-voltage integration reaches the reference value, i.e.,

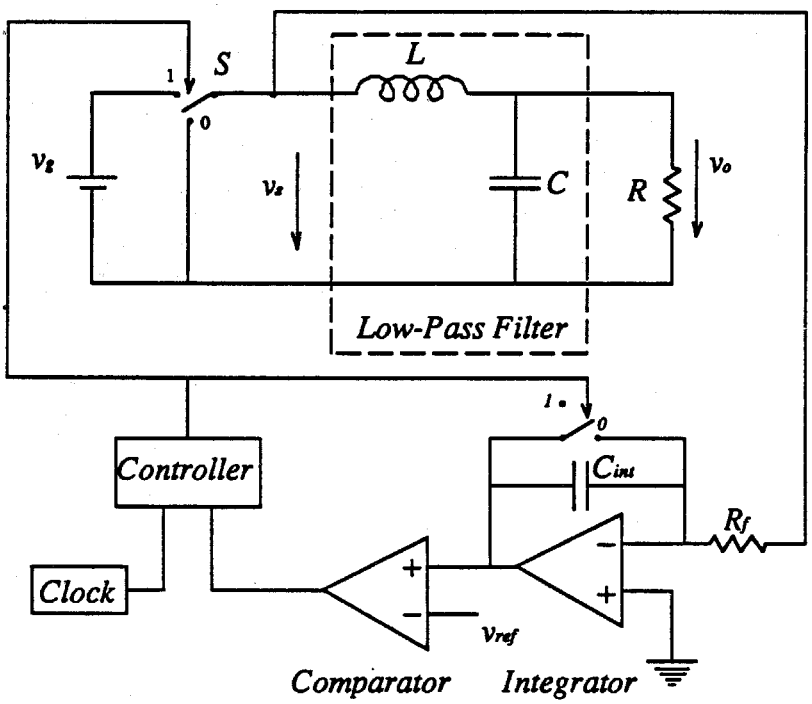


Figure 7.3: One-Cycle Control Buck Converter. The diode-voltage is fed back to the real-time integrator. The integration is started when the clock turns the transistor ON. The integration value is compared with the control reference in real time. When the output voltage of the integrator reaches the control reference, the transistor is turned OFF.

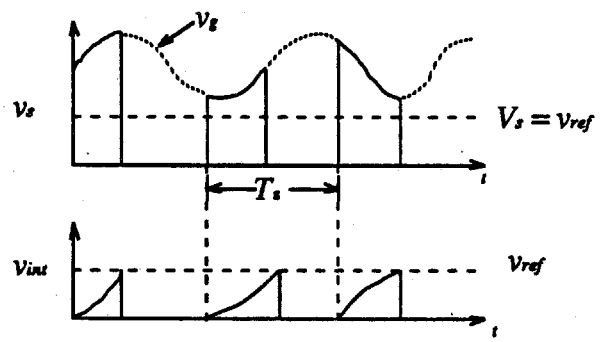


Figure 7.4: Diode-Voltage Waveform of the Buck Converter. When the transistor is on, the diode is off, and the diode-voltage v_s is equal to the input voltage. When the transistor is off, the diode is on, and v_s is zero.

$v_{int} = v_{ref}$. The integration is immediately reset to zero when the transistor turns OFF, to prepare for the next cycle.

7.2.1 The Input-Voltage Perturbation Rejection

Suppose the control reference and the load are constant. When the input voltage v_g is perturbed, by an arbitrary pattern, the diode-voltage is equal to the input voltage while the transistor is ON. This changing diode-voltage is integrated in real time. The slope of the integrated diode-voltage changes exactly and immediately corresponding to changes in the diode-voltage. The input voltage directly and instantly adjusts the duty-ratio d such that the integration of the diode-voltage is constant in each cycle as shown in Fig. 7.5. In Fig. 7.5(a) the input voltage is changed twice while the transistor

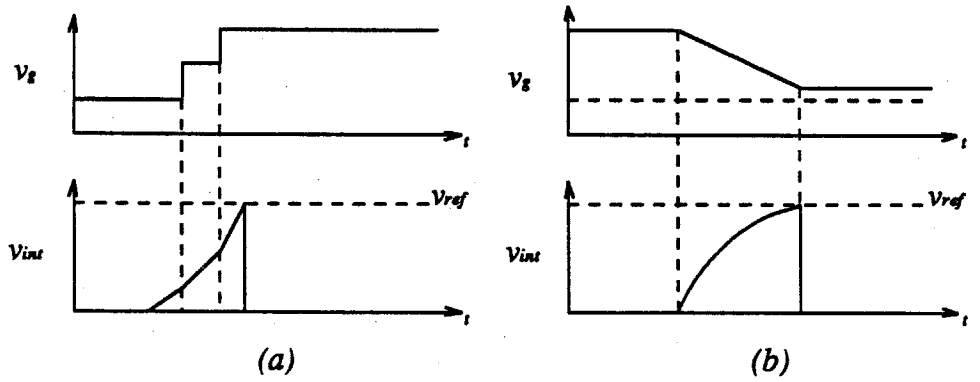


Figure 7.5: Rejection of Input-Voltage Perturbations. (a). The input voltage jumps twice while the transistor was ON. The slope of the integration immediately changes; therefore, the speed to reach the control reference is adjusted instantaneously in order to keep the integration value of the diode-voltage the same as the control reference. (b). The input voltage decreases linearly during the time when the transistor is ON. The integrator adjusts its integration slope continuously to adjust the duty ratio so that the integration of the diode-voltage is equal to the control reference.

is ON. The slope of the integration immediately changes; therefore, the speed to reach the control reference is adjusted instantaneously in order to keep the integrated value of

the diode-voltage the same as the control reference. In Fig. 7.5(b) the input voltage is decreased linearly during the time when the transistor is ON. The integrator adjusts its integration slope continuously in order to adjust the duty-ratio so that the integration of the diode-voltage is equal to the control reference. No matter how the input-voltage changes, the output voltage does not see the input perturbation. Theoretically, this control technique completely rejects input-voltage perturbations. Since the integrator adjusts its integration slope in real time, the One-Cycle Control technique is able to reject all frequency perturbations, even perturbations at frequencies higher than the switch frequency, as shown in Fig. 7.6.

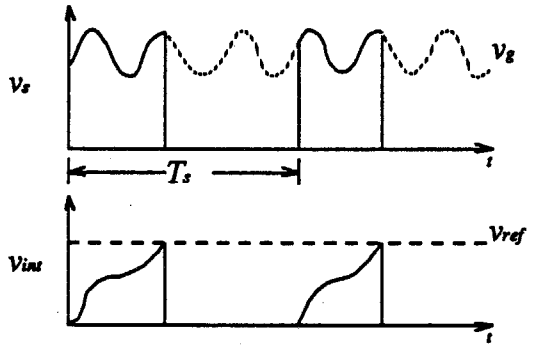


Figure 7.6: High Frequency Input-Perturbation Rejection. Since the integrator adjusts its integration slope in real time, the One-Cycle Control rejects all frequency perturbations, even perturbations with frequencies higher than the switch frequency.

One-Cycle Control of buck converter can also be understood as a feedforward buck converter with special designed feedforward circuit, as shown in Fig. 7.7. The motivation behind the feedforward method is that the input voltage directly controls the duty ratio before the output voltage error occurs. When the input voltage steps up, the saw-tooth becomes steeper and the duty-ratio changes immediately in an attempt to reject the input voltage perturbation. The input voltage is sensed and integrated to generate the saw-tooth. When the input voltage is perturbed, the so called "saw-tooth" is no longer

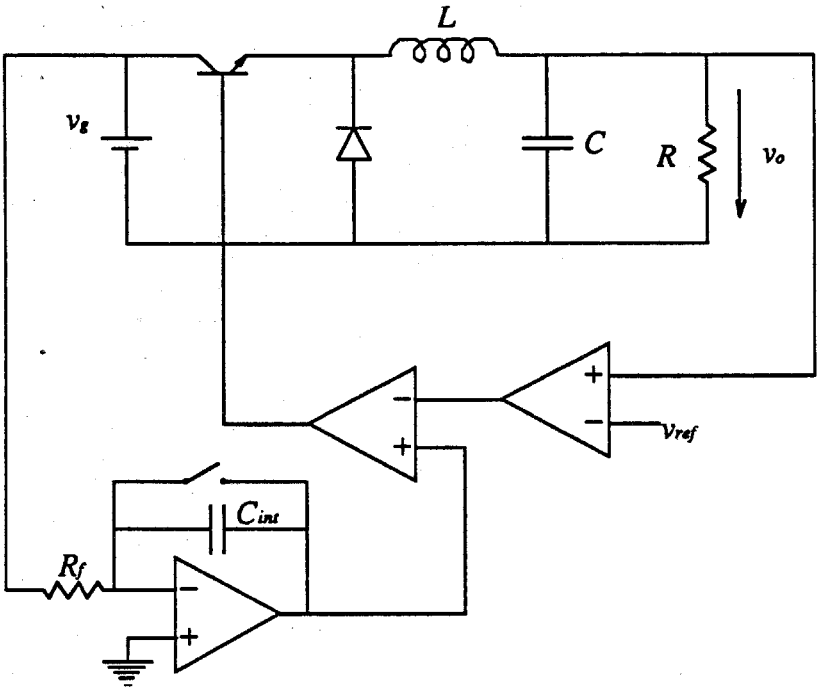


Figure 7.7: Integrated Input Voltage Feedforward Control of Buck Converter. The input voltage directly controls the duty ratio before the output voltage error occurs. When the input voltage steps up, the saw-tooth becomes steeper and the duty-ratio changes immediately in an attempt to reject the input voltage perturbation.

linear as shown in Fig. 7.8.

For feedforward control of the buck converter, the slope of the saw-tooth is determined by the integration of the input voltage.

$$Saw = \int_0^t v_g dt \qquad 0 < t < T_s \tag{7.2}$$

When the saw-tooth and the voltage reference cross each other, the transistor is turned off. The duty-ratio is determined such that the input voltage integration in each cycle is constant. This function is identical to the One-Cycle Control technique. However, this feedforward scheme does not work for other types of switching converters.

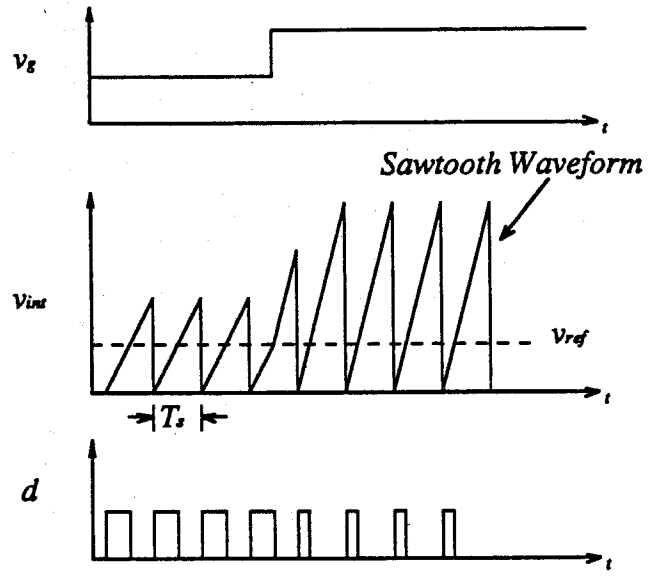


Figure 7.8: The Saw-Tooth of Feedforward Buck Converter. The input voltage is sensed and integrated to generate the saw-tooth. When the input voltage is perturbed, the so called "saw-tooth" is no longer linear.

7.2.2 Load-Disturbance Rejection

Suppose the control reference and the input voltage are constant, whereas the load current is perturbed. If the input voltage source has some output impedance, the amplitude of the diode-voltage will be perturbed because the disturbing current generates a voltage disturbance across the input impedance. This disturbance is equivalent to the case when the input voltage is perturbed. One-Cycle control completely rejects load disturbances at the diode-voltage, and keeps the average of the diode-voltage constant. However, the output voltage is disturbed because the dynamics of the output filter. The effect of the output filter is discussed in more detail in Section 7.4.

7.2.3 Following the Control Reference

Suppose the input voltage and the load are constant, while the control reference changes sinusoidly. Since the input voltage is constant, the slope of the real-time inte-

gration remains constant; however, the integrated value, at which the transistor is shut OFF, is exactly equal to the sinusoid control reference, in each cycle . Therefore, the average of the diode-voltage follows the control signal immediately, within one cycle, as shown in Fig. 7.9.

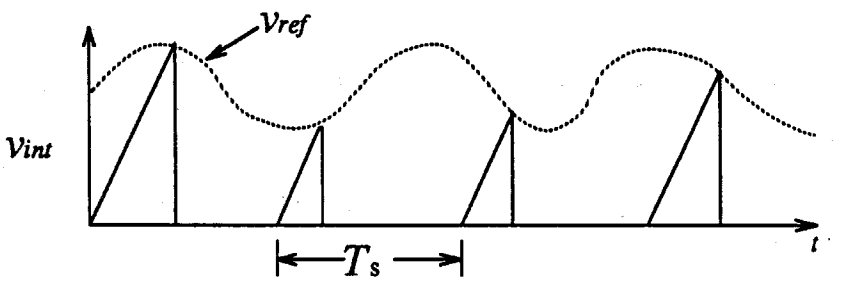


Figure 7.9: Following the Control Signal in One Cycle. When the control reference changes sinusoidly, the integration value follows the control reference in each switching cycle. The duty-ratio d is determined when the integration value reaches the control signal, so that the average value of the diode-voltage keeps up with the sinusoid control reference in one cycle.

Suppose the input voltage and the control reference are changing at the same time. For example, the input voltage has a step up perturbation while the control reference changes sinusoidly. The integration changes its slope as the amplitude of the input voltage changes. The slope becomes steeper after the input voltage steps up. No matter how the integration slope changes, the integration value still keeps up with the sinusoid control reference in each cycle. Therefore, the average value of the diode-voltage does not see the input perturbation and it follows the control reference in one cycle, as shown in Fig. 7.10.

Suppose the load resistance suddenly steps up, and the control reference is changing

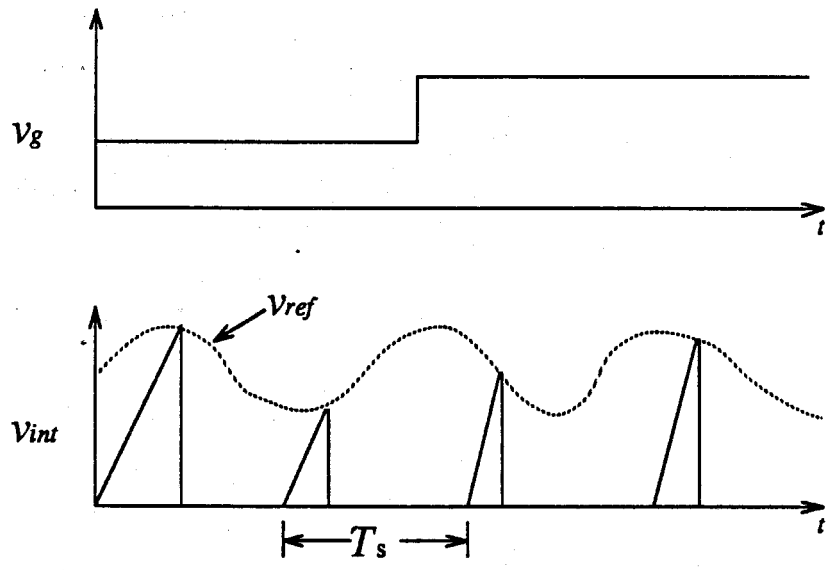


Figure 7.10: Following the Control Signal and Rejecting the Input Voltage Perturbation. The input voltage is perturbed with a step up function and the control reference changes sinusoidly. The slope of the integration is changing according to the input voltage. When the integration value reaches the control signal value, the switch changes its state. The average value of the diode-voltage is exactly equal to the sinusoid control reference.

with time in a sinusoid pattern. Due to the input impedance of the converter, the envelope of the diode-voltage changes. Therefore, the slope of the integration changes corresponding to the load change. The integration value keeps up with the sinusoid control reference. Hence, the average of the diode-voltage is fully controlled by the control reference, as shown in Fig. 7.11.

7.3 The Effect of the Input Low-Pass Filter

The pulsed input current of the basic buck converter produces electromagnetic disturbances on the line power. In order to prevent the line power from pulse current pollution, a low-pass input filter is necessary in practice, as shown in Fig. 7.12.

The input current for the buck converter with input filter is continuous. The am-

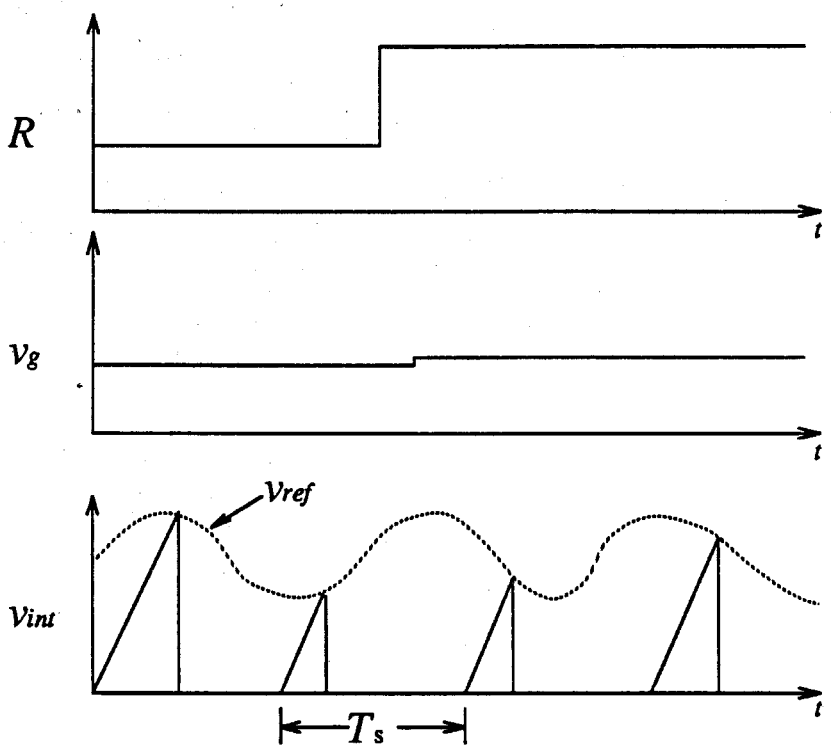


Figure 7.11: Following the Control signal and Rejecting the Load Disturbance. The load resistance is stepped up, and the control reference changes sinusoidly. The slope of the integration changes due to the change of the envelope voltage of the diode caused by the load resistance change. When the integration value reaches the new control signal value, the switch changes its state. The average value of the diode-voltage is exactly equal to the sinusoid control reference.

plitude of the diode-voltage v_s, when the switch is ON, is no longer the same as the input voltage; therefore, the input voltage does not directly control the amplitude of the diode-voltage. However, the relationship in Equation (7.1) is still preserved. The working waveform of the buck converter with input filter is shown in Fig. 7.13.

One-Cycle Control of buck converter with an input low-pass filter is shown in Fig. 7.14. The input filter L_1C_1 of the buck converter can be considered as the output filter of the line input voltage v_g; then the capacitor voltage v_{C1} can be considered the input voltage of the buck converter. One-Cycle Control of the buck converter, with v_{C1} as its input voltage, has the same structure as the one discussed in Fig. 7.3 of Section 7.2. Any

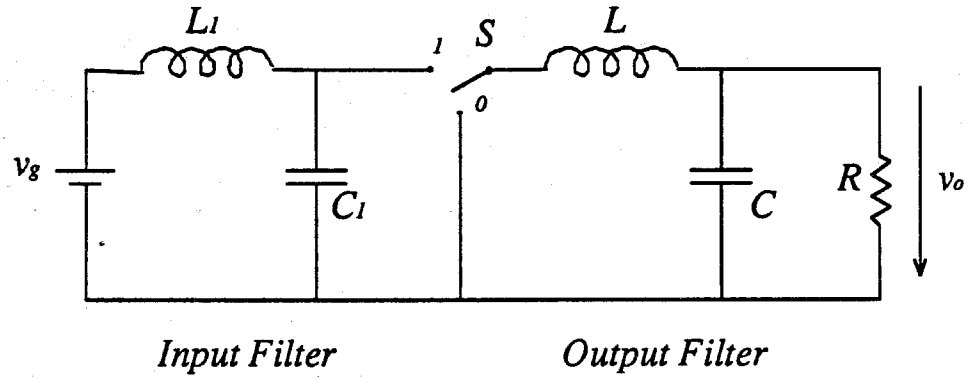


Figure 7.12: Buck Converter with Input Filter. A low-pass filter L_1C_1 is used to prevent the line power from electromagnetic disturbances. The system becomes fourth order.

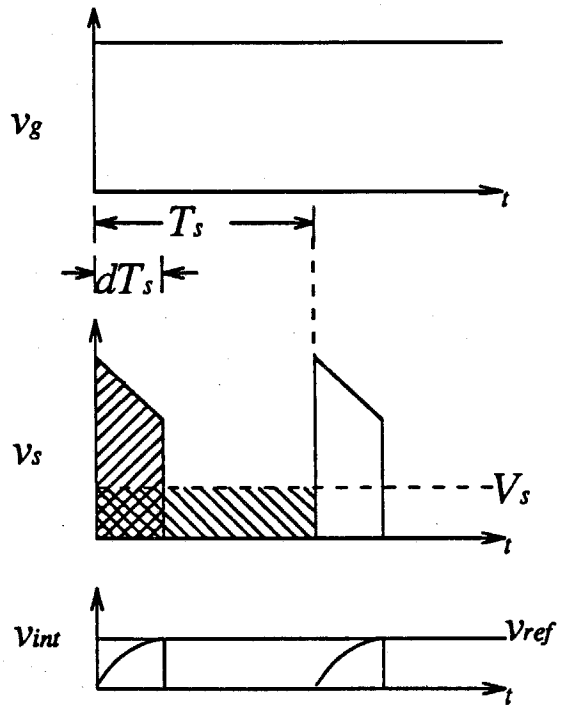


Figure 7.13: The Working Waveform of the Buck Converter with Input Filter. The amplitude of the diode-voltage, when the switch is ON, is no longer the same as the input voltage. However, the relationship in Equation. 7.1 is still preserved.

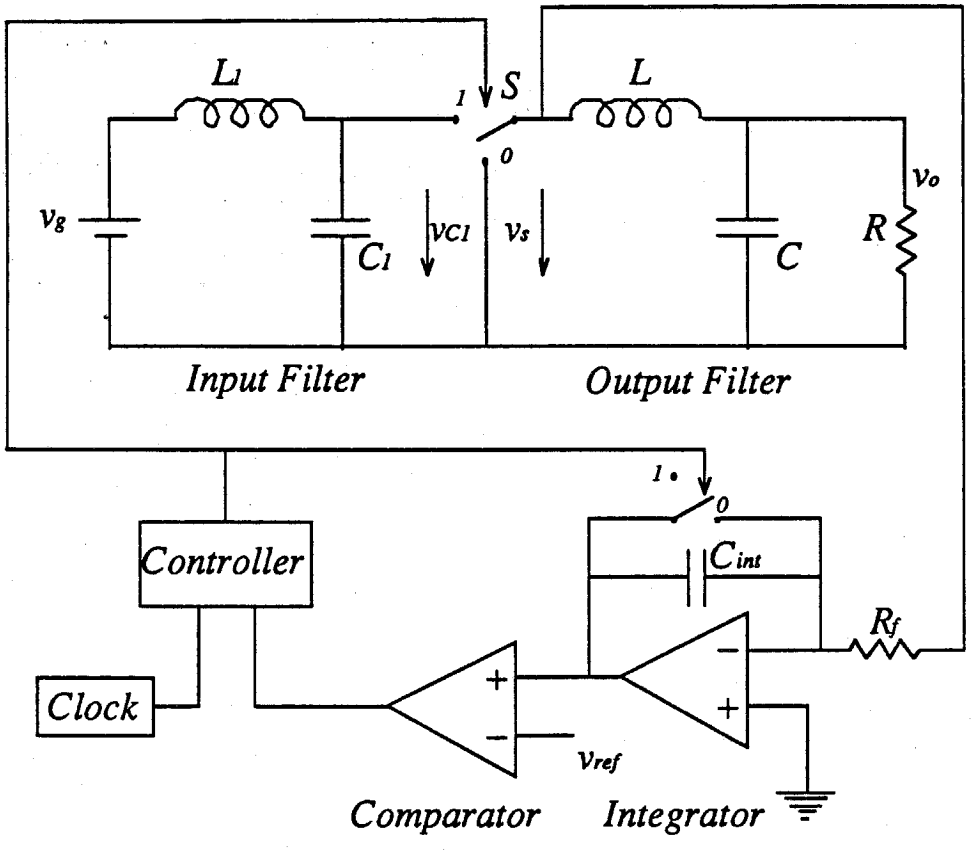


Figure 7.14: One-Cycle Control of the Buck Converter with Input Low-Pass Filter. The input filter of the buck converter can be considered as the output filter of the input line voltage v_g. Therefore One-Cycle Controlled buck converter with the capacitor voltage v_{C1} as its input voltage has the same structure as the circuit discussed in Section 7.2.

perturbation of the input voltage v_g causes a dynamic response in the capacitor voltage v_{C1}. According to the analysis in Section. 7.2, One-Cycle Control of the buck converter rejects any perturbation in v_{C1}; therefore, it also rejects any perturbation of the input voltage v_g. The average value of the diode-voltage at the switch output rejects the load perturbation and follows the control reference instantaneously within one cycle. The input low-pass filter does not have dynamic effect on the One-Cycle Controlled buck converter.

7.4 The Effect of the Output Low-Pass Filter

As discussed in the last section, the diode-voltage of the buck converter with One-Cycle Control is instantaneously controlled by the control reference in one cycle. Therefore, the diode-voltage is equivalent to a controllable voltage source that provides desired DC and undesired switching frequency AC. The LC low-pass output filter of the buck converter is designed to block the switch frequency, as shown in Fig. 7.15. However, the

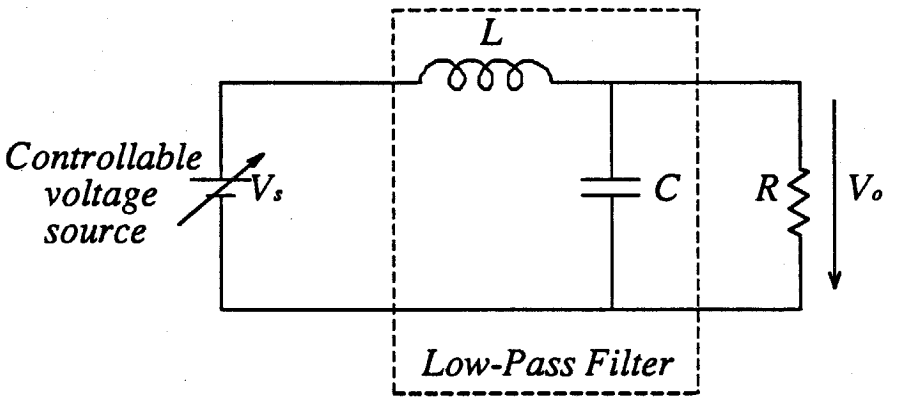


Figure 7.15: The Equivalent Circuit for Buck Converter with One-Cycle Control. The diode-voltage of buck converter with One-Cycle Control is equivalent to a controllable voltage source with desired DC and undesired AC. The low-pass filter is designed to block the undesired AC. The whole system behaves like a second-order linear system.

existence of the low-pass filter introduces an additional frequency response from the v_{ref} controlled voltage source V_s to the output voltage v_o. The whole system behaves like a second-order linear system:

$$\frac{v_o}{V_s} = 1 + \frac{L}{R}S + LCS^2 \tag{7.3}$$

The input-voltage perturbation does not have effect on the output voltage v_o, since it is rejected by the One-Cycle Control loop. Though the load change does not have any effect on the DC value V_s of the diode-voltage, it does perturb the output voltage

v_o because of the energy storage elements in the low-pass filter that prevent the load current and/or voltage from changing suddenly, as shown in Fig. 7.16. Although the control reference v_{ref} is able to adjust the average of the diode-voltage instantaneously, the output voltage still has a second-order transient response to the control reference because of the low-pass filter, as shown in Fig. 7.16.

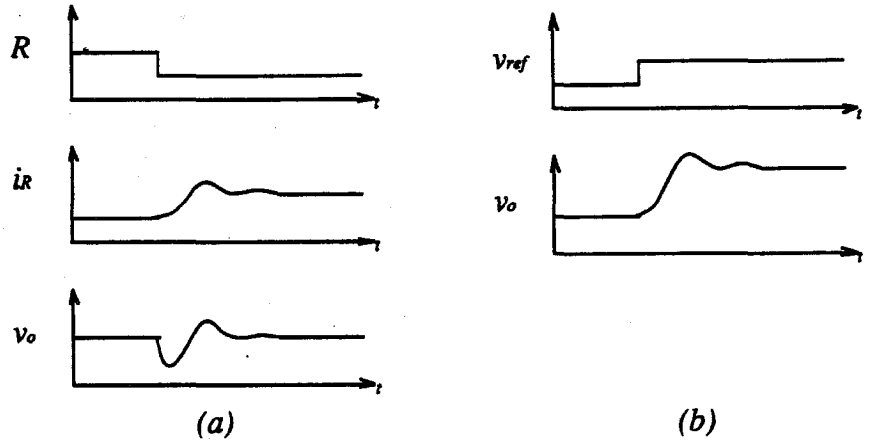


Figure 7.16: Second-Order System Responses. a) When the load resistance R steps down. The load current i_R does not change to its new steady state immediately and the output voltage v_o is disturbed. b) When the control reference v_{ref} changes, the output voltage v_o has a second-order response.

From the above analysis, it is clear that the input-voltage perturbations and the dynamic response of the input low-pass filter are isolated by the One-Cycle Control loop so that they do not affect the output voltage. The dynamics of the output low-pass filter remain the same. Therefore, a One-Cycle Controlled buck converter is equivalent to a linear controllable voltage source with an output low-pass filter.

7.5 Comparison with Pulse-Width-Modulation and Current-Mode Control

The open-loop PWM buck converter has nonlinear dynamics from its input voltage and duty-ratio control signal to its output voltage.

$$\mathcal{L}(v_o) = \frac{\mathcal{L}(d\ v_g)}{1 + \frac{L}{R}S + LCS^2} \tag{7.4}$$

where the symbol $\mathcal{L}$ represents the Laplace transformation. From above equation, it is clear that the open-loop PWM buck converter does not have any capability to reject the input voltage perturbation. When the input voltage is constant, the output voltage has a second-order response to the duty-ratio control signal. If the buck converter has an input filter, the dynamics of the converter become more complicated. The converter does not reject the input perturbation. In addition, the existence of the input filter produces the right-half-plane (RHP) zeros. Details are discussed in Chapter 3.

The PWM feedback buck converter is shown in Fig. 7.17. The transistor and the diode operate at a fixed frequency. During the time $0 < t < dT_s$, the transistor is ON and the diode is OFF. During the time $dT_s < t < T_s$, the transistor is OFF and the diode is ON. The buck converter has input voltage v_g and output voltage v_o. The conversion of the buck converter is the same as its duty-ratio:

$$v_o = dv_g \tag{7.5}$$

The control circuit contains an output voltage sensor, a control reference, an error controller, and a PWM modulator. The error controller is a PID (proportion, integration, and/or differential) amplifier that is designed to improve the frequency response of the closed-loop system. The PWM modulator is a saw-tooth comparator that adjusts the duty ratio in each cycle by comparing the control signal with the saw-tooth wave.

The output voltage v_o is sensed and compared with the control reference to generate the error signal $v_e = v_{ref} - v_o$. If the error signal is zero the duty-ratio remains unchanged. If the error is not zero, the controller sends a control signal to the modulator to change the duty-ratio d in the direction necessary to reduce the error signal. The modulator compares the control signal v_c with the saw-tooth wave and generates a square-wave drive signal with an adjustable duty-ratio d.

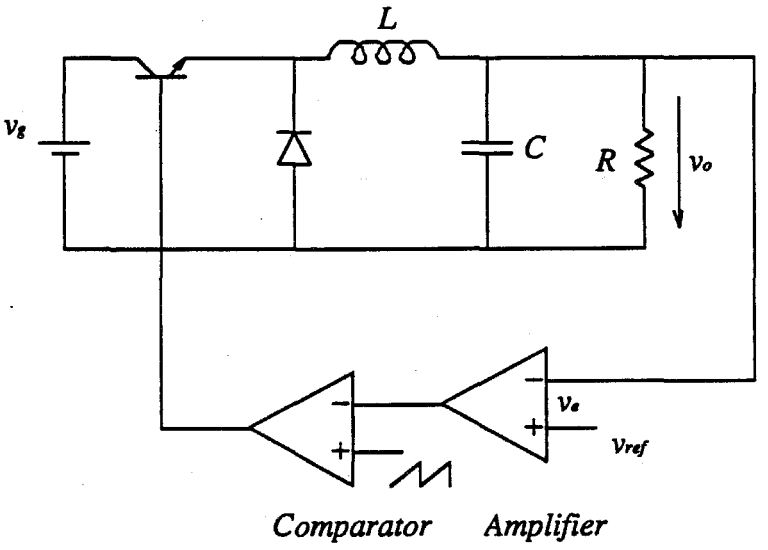


Figure 7.17: Feedback Control of The Buck Converter. The buck converter has input voltage v_g, output voltage v_o, and conversion rate d. The output voltage is sensed and compared with the control reference v_{ref}, and the error signal $v_e = v_{ref} - v_o$ is processed to control the duty-ratio d.

To examine the capability of the circuit to reject input-voltage perturbations, suppose that the load and the control reference are constant. When the input voltage is perturbed, for example by a large step up, the duty-ratio controller does not see the change instantaneously since the error signal must change first. Therefore, the output voltage jumps up. The feedback signal is compared with the reference, and the error between the reference and the feedback signal is amplified to control the duty-ratio. The

duty ratio is then adjusted, through a number of switching periods, to the new steady-state value that provides the correct conversion ratio to regulate the output voltage. The duration of the transient is dictated by the loop-gain bandwidth and by the converter's output impedance. Large changes in the input voltage cause large changes in the duty-ratio as well. The duty-ratio is corrected by the output voltage error; therefore,

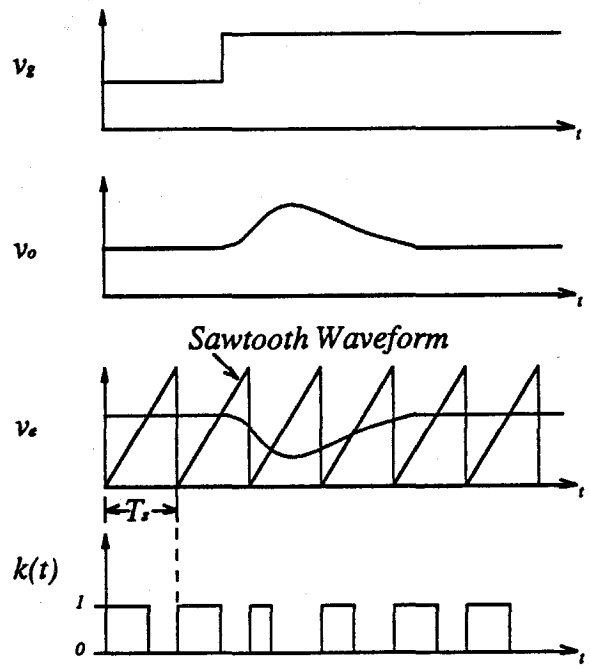


Figure 7.18: Transient Response Caused by Input-Voltage Perturbation. The duty-ratio is corrected by the output-voltage error; therefore, the output voltage is always influenced by the input-voltage perturbation.

the output voltage is always influenced by the input-voltage perturbation. The control process is shown in Fig. 7.18. In addition, input voltage perturbations also perturb the loop-gain and cause some nonlinear frequency response.

If the buck converter has a low-pass input filter, (see analysis in Chapter 3) the dynamic model of the system is shown in Fig. 3.11. The system is nonlinear, its linearized small-signal model has RHP zeros. The control loop is very difficulty to stabilize.

Current-mode control utilizes some pulse and nonlinear nature of the switching con-

verter. The switch current is sensed and compared with the control reference. The clock pulse, which runs at constant frequency, turns the transistor on. When the switch current reaches the control reference the comparator changes its state and turns the transistor off. There is no PWM modulator in the control loop, because the pulse signal in the circuit controls the duty-ratio directly. A schematic of current-mode control of the buck converter is shown in Fig. 7.19. The control function for this circuit is shown in Fig. 7.20.

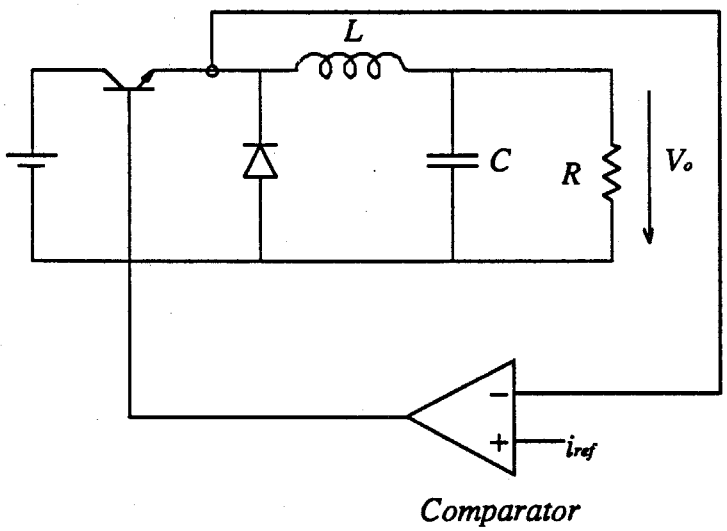


Figure 7.19: Current-Mode Control of the Buck Converter. The current-mode control loop of the buck converter contains a current reference i_{ref}, a comparator, and a switch current sensor.

When the input voltage is perturbed, by a step up for example, the current ramp immediately increases to control the duty-ratio. The duty-ratio correction is dependent not only on the current ramp, but also on the last state of the current; the transient is shown in Fig. 7.21. Suppose the input voltage changes from v_{g1} to v_{g2}. In order to maintain a constant output voltage, the duty-ratio d must change from its old steady state $d_{old} = \frac{v_o}{v_{g1}}$ to a new steady state $d_{new} = \frac{v_o}{v_{g2}}$. The duty-ratio d jumps from d_{old} to

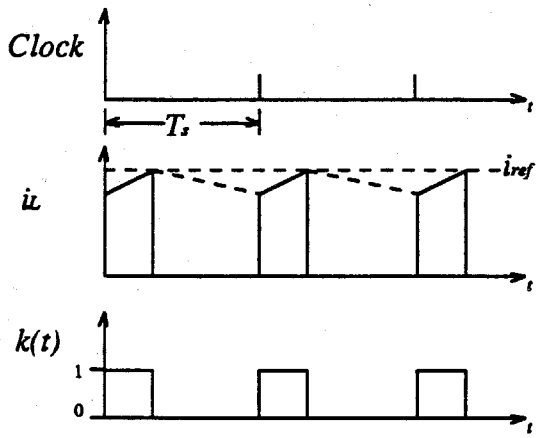


Figure 7.20: Current-Mode Control Function. The switch current is sensed and compared with the control reference. The clock pulse, which runs at constant frequency and turns the transistor on. When the switch current reaches the control reference the comparator changes its state and turns the transistor off.

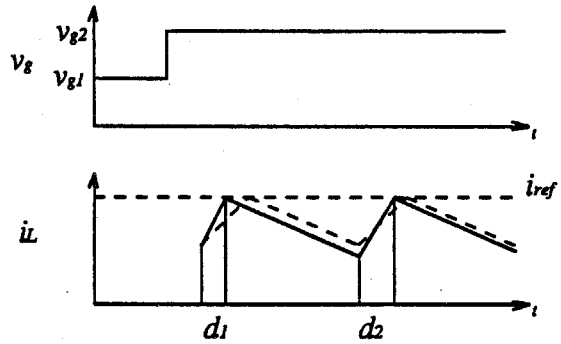


Figure 7.21: The Response of Current-Mode Control to the Input Perturbation. When $\frac{v_o}{v_g} < 0.5$, the transient process converges, however, it takes several cycles for the system to reach the new steady state. When $\frac{v_o}{v_g} > 0.5$, the transient process does not converge; the system oscillates. Nevertheless, an artificial ramp can be employed to stabilize the system.

d_1 immediately in the first cycle. The transient can be found as

$$d_{n+1} - d_n \approx -\frac{v_o}{v_G - v_o}(d_n - d_{n-1}) \tag{7.6}$$

$$d_n|_{n=\infty} = \begin{cases} d_{new} & \frac{v_o}{v_g} < 0.5 \\ oscillates & \frac{v_o}{v_g} > 0.5 \end{cases} . \tag{7.7}$$

When $\frac{v_o}{v_g} < 0.5$, the transient process converges, however, it takes several cycles for the system to reach the new steady state. When $\frac{v_o}{v_g} > 0.5$, the transient process does not converge; the system oscillates. Nevertheless, an artificial ramp can be employed to stabilize the system. In addition, if the artificial ramp is chosen to be exactly equal to the falling slope s_f of the switch current, the system fully rejects the input voltage perturbations. However, only the buck converter operating at a constant output voltage satisfies this condition. Fig. 7.22 shows how the artificial ramp affects the function of the current-mode control. The falling slope of the switch current of the buck converter is determined by the output voltage:

$$s_f = \frac{v_o}{L} \tag{7.8}$$

where L is the output filter inductance. When the output voltage changes, the artificial ramp must change accordingly, such that $s_f = \frac{v_o}{L}$. For converters other than the buck converter, however, the falling slope of the switch current may be a function of the input voltage, the voltage across the energy-transfer capacitor, and/or the output voltage. Therefore, the falling slope of the switch current dynamically responses to the input voltage, and the artificial ramp can no longer match the falling slope of the switch current. Due to this mismatch, current-mode control is unable to reject input-voltage perturbations.

Current-mode control is equivalent to state-feedback control. Therefore, it rearranges pole positions of the system. Current-mode control may improve the dynamic response

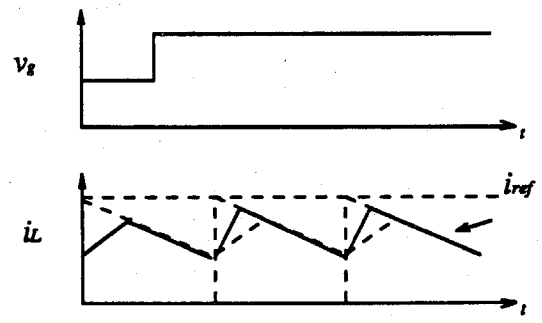


Figure 7.22: Current-Mode Control of Buck Converter with Artificial Ramp. If the artificial ramp is chosen to be exactly equal to the falling slope s_f of the switch current, the system will fully reject the input voltage perturbation. However, only the buck converter working at a constant output voltage satisfies this condition.

of a converter. It is necessary to have an output voltage feedback control. With output-voltage feedback control, the system is still an error amplified system. Therefore, the ability of the converter to follow the control reference is similar to that of the PWM feedback converter.

7.6 Experiments of One-Cycle Controlled Buck Converter

The experimental One-Cycle Controlled buck converter is shown in Fig. 7.23. The clock triggers the RS flip-flop at a constant frequency to turn ON the transistor. The diode-voltage is integrated and compared with the reference voltage v_{ref}. When the integrated value of the diode-voltage reaches the control reference, the comparator changes its state, which resets the RS flip-flop and consequently turns off the transistor. A junction FET is used to reset the integrator when the transistor turns off. Five access points are set. Point A, Point B, and Point C are used to inject the control signal, the load disturbance, and the input perturbations, respectively. Point B, Point D, and Point E are used to detect the output voltage, the diode-voltage, and the integrated diode-voltage.

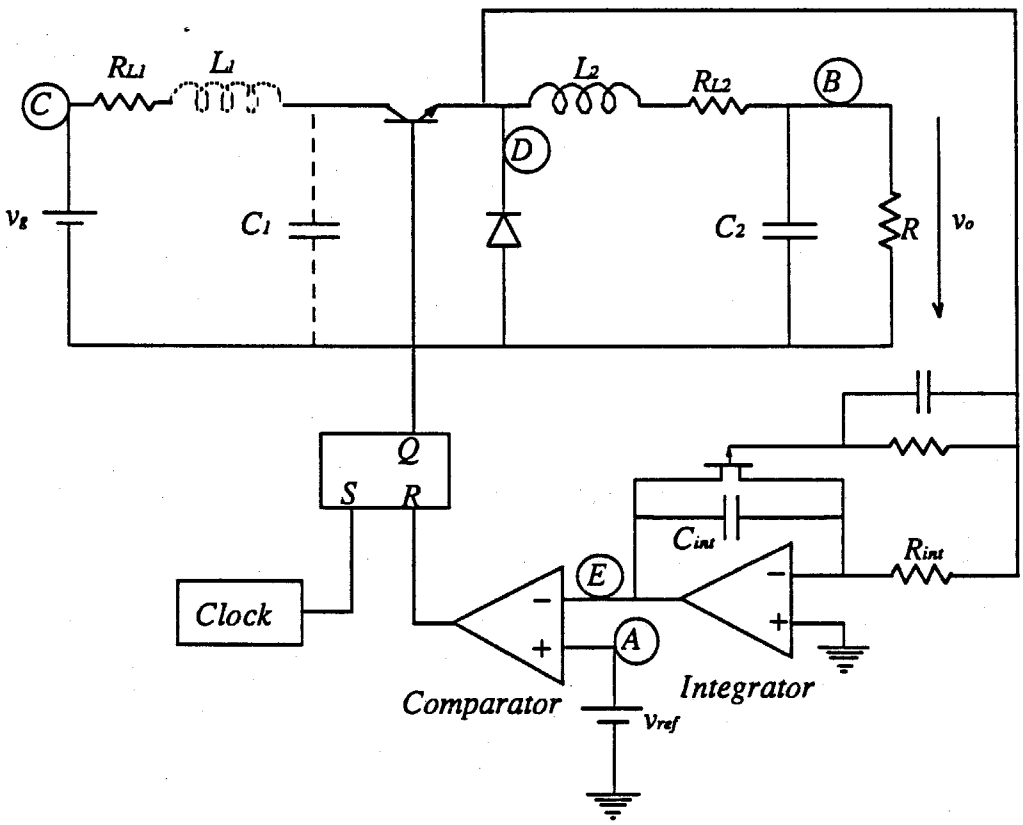


Figure 7.23: The Experimental Buck Converter with One-Cycle Control. Five access points are set. Point A, Point B, and Point C are used to inject the control signal, the load disturbance, and the input perturbations, respectively. Point B, Point D, and Point E are used to detect the output voltage, the diode-voltage and the integrated diode-voltage.

Experiment 7.1 Measure the ability of the diode-voltage to follow a step change in the control reference. A step-up function from $3V$ to $4.6V$ was injected into the control reference at Point A, while the input voltage and the load were held constant. The output response of the integrator was measured at Point E. The experimental results are shown in Fig. 7.24. Since the load and the input voltage are constant, the integration slope is also constant. When the control reference stepped up, the integration took a longer time to reach the control reference. Therefore, the duty-ratio was increased and the average value of the diode-voltage jumped to its new steady state in one cycle.

Experiment 7.2 Measure the response of the diode-voltage to a step-up perturbation of the input voltage. A step-up function from $10V$ to $20V$ was injected into the input voltage at Point B, while the load and the control reference were constant. The output response of the integrator was measured at Point E. The experimental results are shown in Fig. 7.25. There are spikes on the input voltage, because the buck converter has pulsed input current and the output impedance of the power source is not zero. These spikes did not influence the average value of the diode-voltage, because the spikes also contributed to the integration that kept the average value of the diode-voltage constant. The input voltage stepped up while the transistor was on. The slope of the integration of that cycle immediately changed; therefore, the duty-ratio was adjusted instantaneously.

Experiment 7.3 Measure the response of the diode-voltage to a sinusoid perturbation in the input voltage. A sinusoid wave $v_g = 20 + 7sin\omega t$, $f = 10kHz$, was injected into the input voltage at Point B, while the control reference and the load were held constant. The integrator output response was measured at Point E. The experimental results are shown in Fig. 7.26. Since the input voltage was not constant, the slope of the integration was changing all the time. Near the peak value of the input voltage the integration took

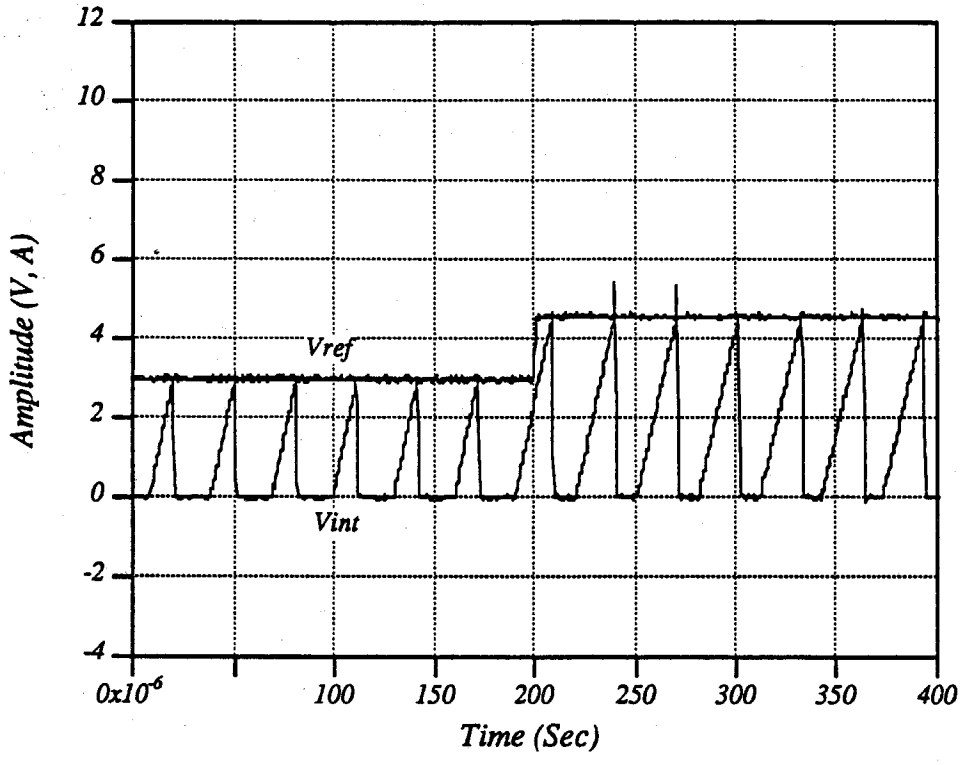


Figure 7.24: The Response of the Buck Converter to a Step-Up of the Control Reference. A step-up function from $3V$ to $4.6V$ was injected into the control reference at Point A; the integrator output response was detected at Point E. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0mH$, $L_2 = 0.48mH$, $C_1 = 0\mu F$, $C_2 = 30\mu F$, $R_{L1} = 1.8\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

about $10\mu sec$, whereas near the valley of the input voltage the integration took about $20\mu sec$. The average value of the diode-voltage was constant in each cycle.

Experiment 7.4 Measure the capability of the diode voltage to reject a step-up input voltage perturbation while following a sinusoid varying control reference. A step-up function from $10V$ to $20V$ was injected into the input voltage at Point B, while the control reference was varied with a sinusoid wave $v_g = 3.1 + 1.2sin\omega t$, $f = 10kHz$, at

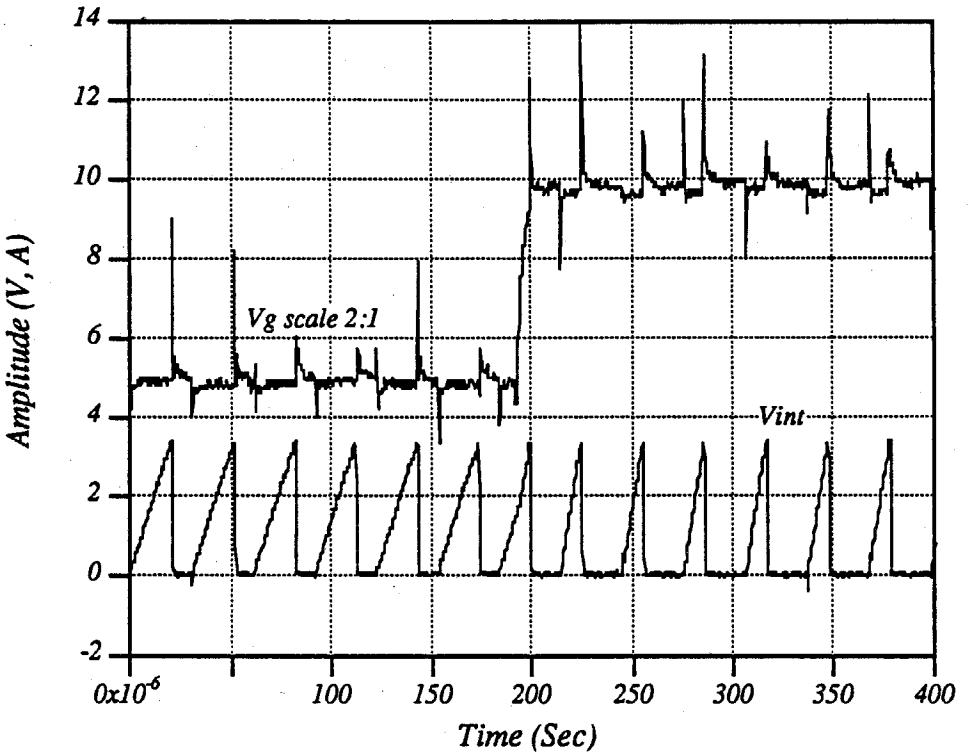


Figure 7.25: Buck Converter Rejects a Step-Up in the Input Voltage. A step-up function from $10V$ to $20V$ was injected into the input voltage at Point B, the integrator response was measured at Point E. Note that the input voltage has been reduced by a factor of two in order to fit it into the plot. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0mH$, $L_2 = 0.48mH$, $C_1 = 0\mu F$, $C_2 = 30\mu F$, $R_{L1} = 1.8\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

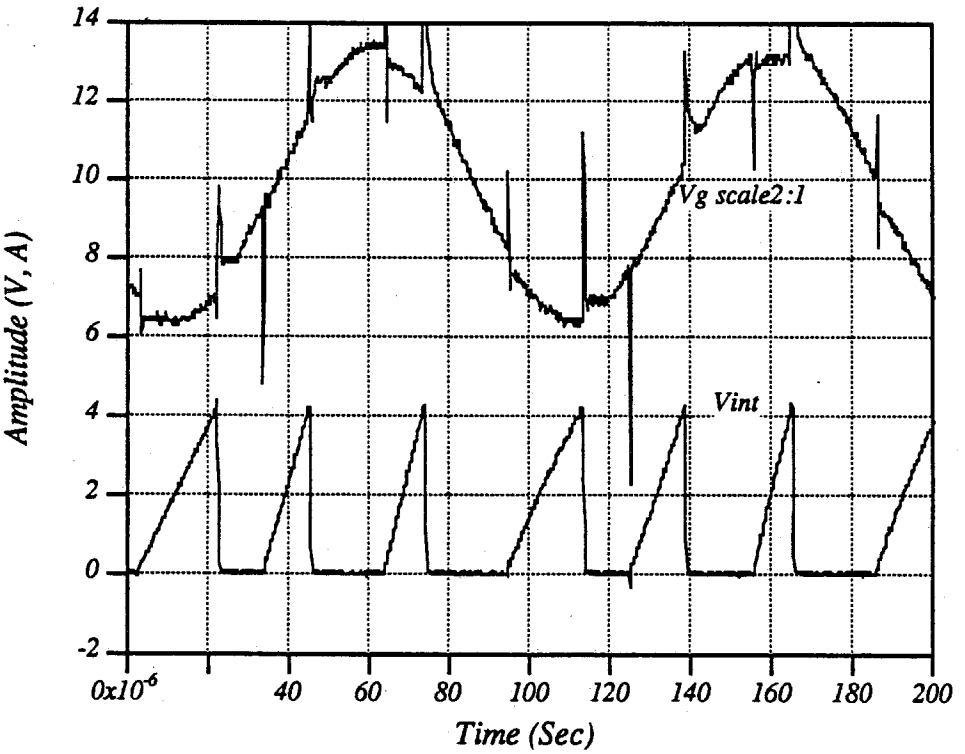


Figure 7.26: Buck Converter Rejects a Sinusoid Change in the Input Voltage. A sinusoid wave $v_g = 20 + 7sin\omega t$, $f = 10kHz$, was injected into the input voltage at Point B. The integrator output response was measured at Point E. Note that the input voltage has been reduced by a factor of two in order to fit it into the plot. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0mH$, $L_2 = 0.48mH$, $C_1 = 0\mu F$, $C_2 = 30\mu F$, $R_{L1} = 1.8\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

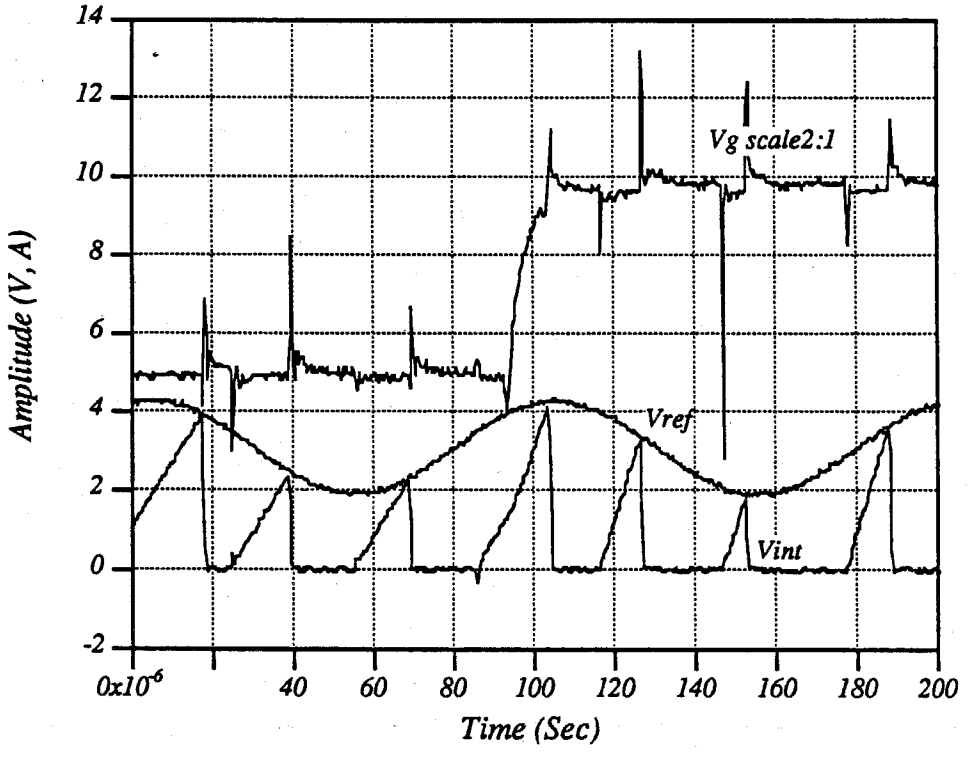


Figure 7.27: Buck Converter Response to a Step-Up in the Input Voltage and a Sinusoid Change in the Control Reference. A step up function from $10V$ to $20V$ was injected into the input voltage at Point B, while the control reference was varied with a sinusoid wave $v_g = 3.1 + 1.2sin\omega t$, $f = 10kHz$, at Point A. The integrator output response was measured at Point E. Note that the input voltage has been reduced by a factor of two in order to fit it into the plot. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0mH$, $L_2 = 0.48mH$, $C_1 = 0\mu F$, $C_2 = 30\mu F$, $R_{L1} = 1.8\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

Point A. The integrator output response was measured at Point E. The experimental results are shown in Fig. 7.27. The slope of the integration changed immediately when the input voltage stepped up. The envelope of the integration waveform kept up with the control reference exactly. Therefore, the average of the diode-voltage was not influenced by the input disturbance and was fully controlled by the control reference.

Experiment 7.5 Measure the capability of the diode-voltage to simutaneously reject an input voltage perturbation and a load disturbance. A sinusoid wave $v_g = 20 + 7sin\omega t$, $f = 10kHz$, was injected into the input voltage at Point B, while the load resistor was changed from 25Ω to 7.1Ω. The integrator output response was measured at Point E, while the control reference was constant. The experimental results are shown in Fig. 7.28. When the resistance stepped up, at $t = 200\mu sec$, the input current became smaller. As a result, the spikes on the input voltage, caused by the pulse input current going through the input impedance, became smaller. However, the average value of the diode-voltage was not affected.

Experiment 7.6 Measure the control-to-diode-voltage frequency response. A sweeping frequency signal was injected at Point A, while the diode-voltage response was measured at Point D. Since the average value of the diode-voltage was fully controlled by the control reference, it was predicted that the frequency response of the diode-voltage to the control reference was flat. The detected frequency response had a very flat amplitude response and phase lag. There was a bump at $f = 2.4kHz$ that was the corner frequency of the input filter. Since the diode-voltage was not exactly zero when the transistor was ON, as a result, the frequency response was not completely flat. The experimental result is plotted in Fig. 7.29.

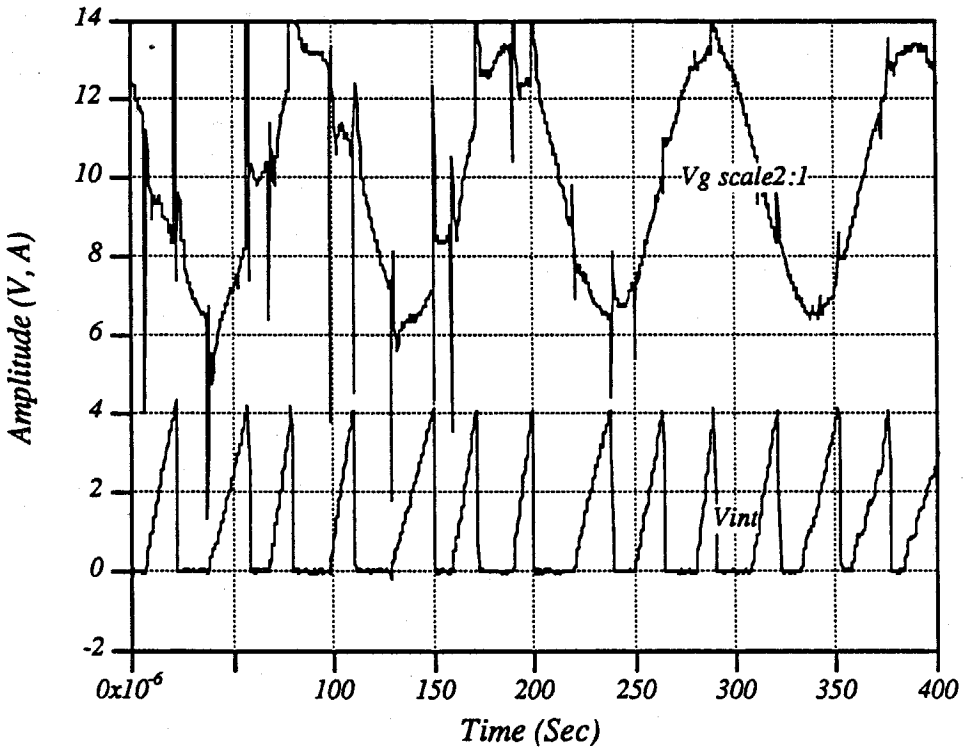


Figure 7.28: The Response of the Buck Converter to a Sinusoid Change in the Input Voltage and a Step-up in the Load Resistance. A sinusoid wave $v_g = 20 + 7sin\omega t$, $f = 10kHz$, was injected at Point B to the input voltage and the load resistor was changed from 25Ω to 7.1Ω, at $t = 200\mu sec$. The integrator output response was measured at Point E. Note that the input voltage has been reduced by a factor of two in order to fit it into the plot. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0mH$, $L_2 = 0.48mH$, $C_1 = 0\mu F$, $C_2 = 30\mu F$, $R_{L1} = 1.8\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

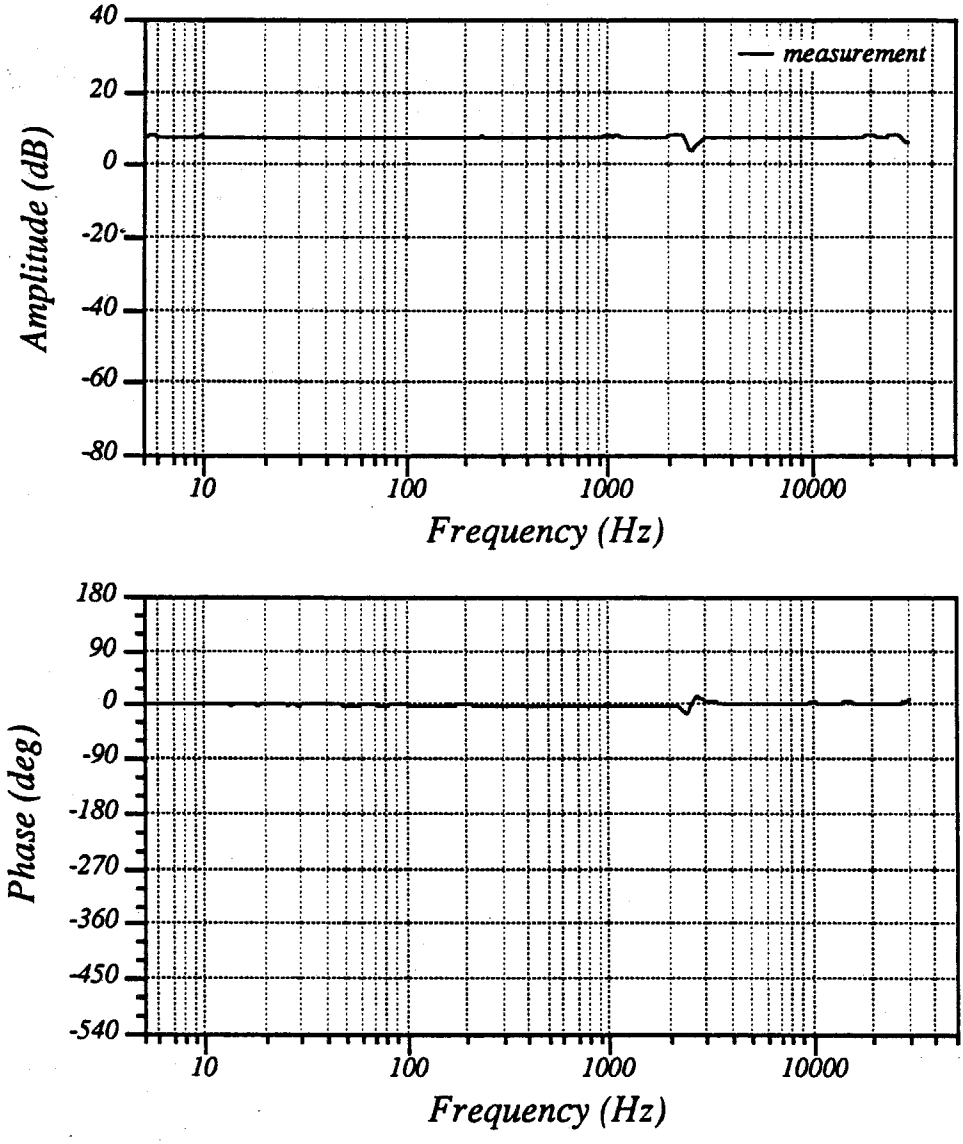


Figure 7.29: Control-to-Diode-Voltage Frequency Response of Buck Converter with Input Filter. A sweeping frequency signal was injected at Point A and the diode-voltage response was measured at Point D. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

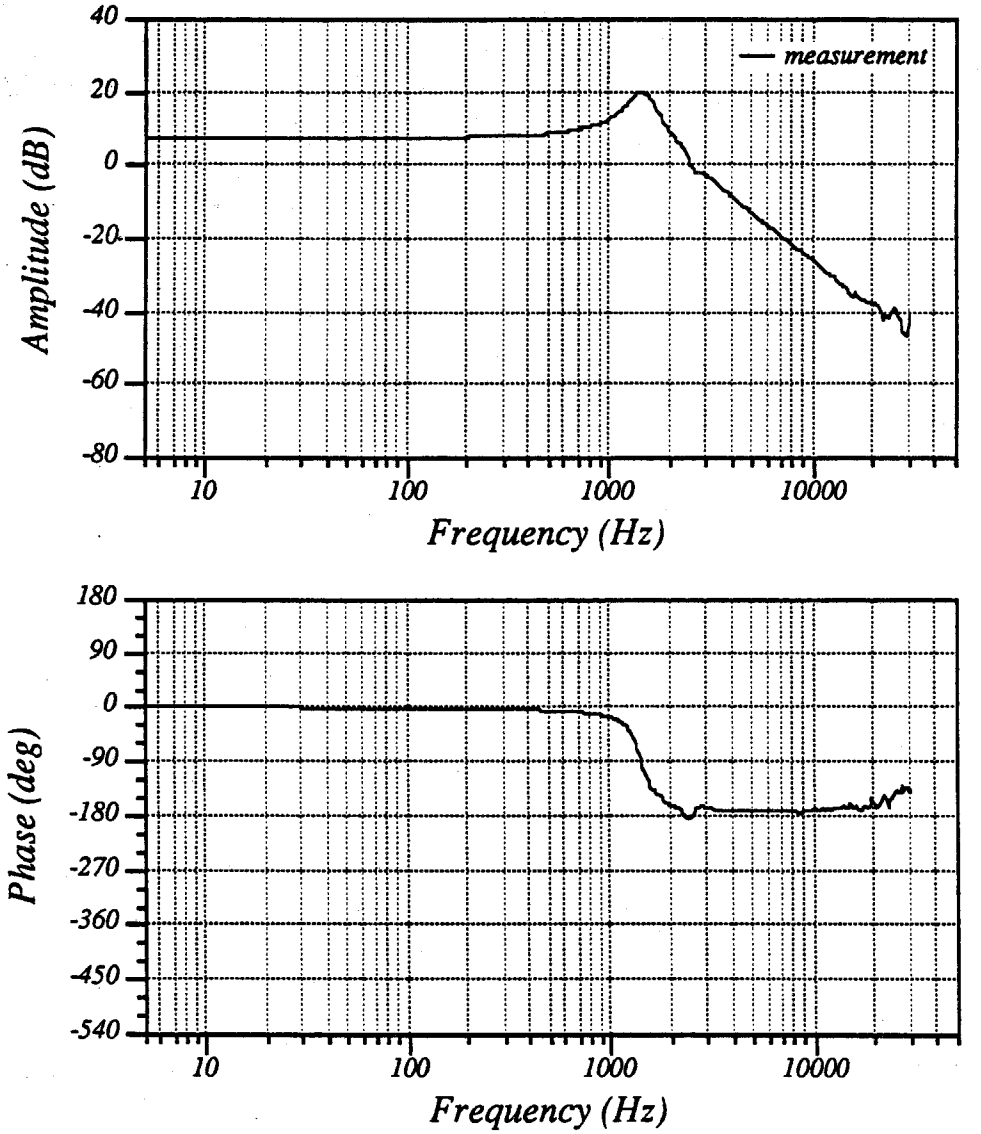


Figure 7.30: Control-to-Output Frequency Response of Buck Converter with Input Filter. A sweeping frequency signal was injected at Point A and the output voltage response was measured at Point B. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

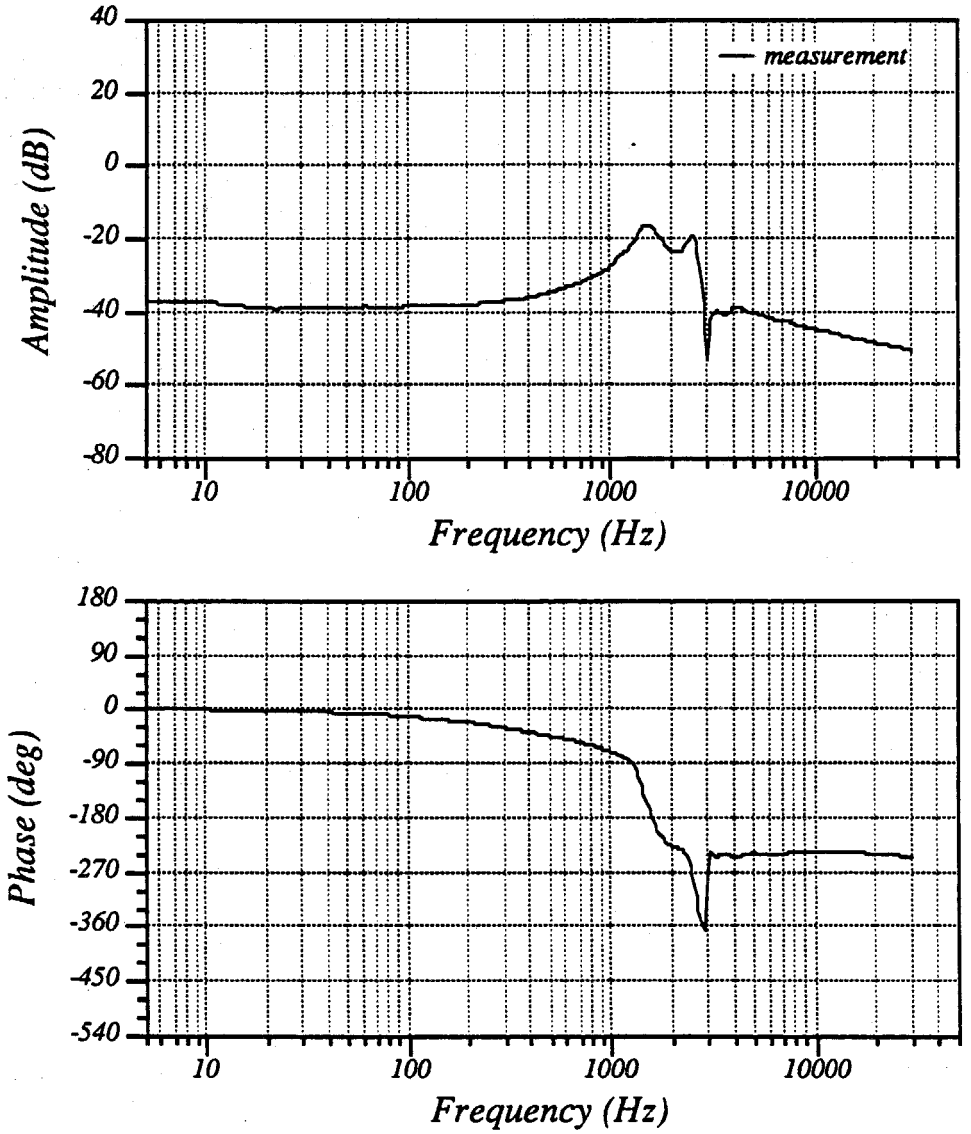


Figure 7.31: Input-to-Output Frequency Response of Buck Converter with Input Filter. A sweeping frequency signal was injected at Point C and the output voltage response was measured at Point B. Operating condition: $V_g = 15V$, $f_s = 30kHz$, $L_1 = 0.43mH$, $L_2 = 0.48mH$, $C_1 = 10.4\mu F$, $C_2 = 30\mu F$, $R_{L1} = 0.25\Omega$, $R_{L2} = 0.6\Omega$, $R = 25\Omega$.

Experiment 7.7 Measure the control-to-output frequency response. A sweeping frequency signal was injected at Point A, and the output voltage response was measured at Point B. The experimental result is plotted in Fig. 7.30. As predicted in the previous section, the frequency response of the buck converter with input filter is equivalent to a second-order system.

Experiment 7.8 Measure the input-to-output frequency response. A sweeping frequency signal was injected at Point C, while the output voltage response was measured at Point B. The experimental result is plotted in Fig. 7.31. It was expected that the system should completely reject the input voltage perturbation. However, the experimental data show that there were leakages of the input perturbation, especially when the sweeping frequency was near the corner frequency of the input filter. This leakage is caused by the fact that the real diode has a non-zero conducting resistance, and also because the wire wrap circuit has some AC coupling.

7.7 Summary

The buck converter with PWM feedback is an error control system. A high loop-gain is required in order to have fast response and good input-perturbation rejection. However, this high gain may cause oscillations due to the influence of the input filter. The current-mode control may improve the system dynamics. When the stabilizing ramp is equal to the falling slope of the switching current, the buck converter can reject input-voltage perturbations; however, this is only possible when the output voltage is constant.

The One-Cycle Control technique is used to control the constant frequency PWM buck converter. The diode-voltage of the buck converter is One-Cycle Controlled. The diode-voltage follows the control reference instantaneously and rejects the input-voltage

perturbations and the load disturbances quickly. The dynamics of the input filter are blocked by One-Cycle Control, while the dynamics of the output filter remains the same. The Buck converter with One-Cycle Control behaves like a controllable voltage source with an output filter. Experiments verified the theoretical predictions.

Chapter 8

Stability of One-Cycle Controlled Pulse-Width-Modulated Converters

For a given switching converter, suppose the diode-voltage is One-Cycle Controlled, the diode-voltage instantaneously responds to the control reference and fully rejects input perturbations. One might assume that this system has infinite loop-gain, however, a physical system is usually unstable with infinite loop-gain. How does the One-Cycle Control loop work? This chapter explains the stability problem of One-Cycle Control. A Ćuk converter is used as an example. The Switching Flow-Graph model is derived for the One-Cycle Control Ćuk converter, in Section 8.1. The global dynamic behavior of the One-Cycle Controlled Ćuk converter is examined in Section 8.2 and the small-signal loop-gain is studied in Section 8.3. Experimental results are discussed in Section 8.4.

8.1 One-Cycle Controlled Switch in Converters

The One-Cycle Control technique converts a non-linear switch into a linear switch, as discussed in Chapter 6. A converter sometimes contains more than one switch in its signal path, as shown in Fig. 3.6. All the signal switches are either synchronized or complementary since they are implemented by one transistor and one or more diode in the real circuit. Therefore, only one signal switch can be One-Cycle Controlled. The other switches are turned ON and OFF according to the state of the One-Cycle Controlled

switch. A basic buck converter, discussed in Chapter 7, has only one signal switch in the signal path from the control reference to the output voltage. Therefore, this basic converter can be completely One-Cycle Controlled. However, a Ćuk converter contains four switches in its signal path, yet only one can be chosen as the One-Cycle Controlled switch. If the signal switch, in the path from Node v_{C1} to the Node v_{L2}, is chosen as the One-Cycle Controlled switch, the forward signal path is broken into two. The resulting system is decoupled into two second-order systems, the input loop and the output loop, as shown in Fig. 8.1. The output of the One-Cycle Controlled switch is the diode-voltage; hence, this is One-Cycle Control of the diode-voltage.

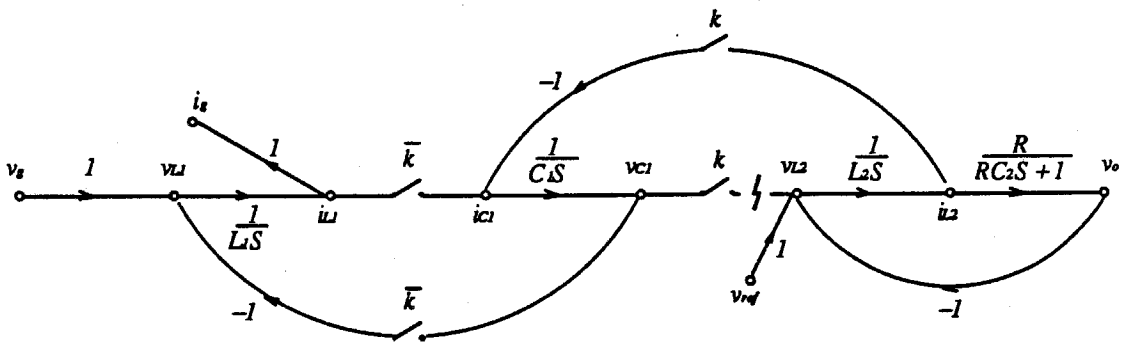


Figure 8.1: Diode-Voltage One-Cycle Control. The signal switch, in the path from Node v_{C1} to the Node v_{L2}, is chosen as the One-Cycle Controlled switch. The forward signal path will be broken into two. The resulting system is decoupled into two second-order systems, the input loop, and the output loop. The output of the One-Cycle Controlled switch, the diode-voltage, is instantaneously controlled within one cycle.

The output loop is fully controlled by the control reference. Any dynamics changes in the input loop are blocked by the One-Cycle Controlled switch. It is equivalent to a linear second-order system from the control reference to the output voltage. The output loop has some influence on the input loop through the switch in the path from Node i_{L2} to Node i_{C1}. Since the signal i_{L2} is independent of the input loop dynamics, the path

from Node i_{L2} to Node i_{C1} is not inside the loop. Hence, the stability of the input loop is not affected by the dynamics of the output loop.

8.2 Global Stability of the One-Cycle Controlled Ćuk Converter

The One-Cycle Control breaks the Ćuk converter into two second-order systems, the input loop and the output loop; therefore, the stability of the One-Cycle Controlled Ćuk converter depends on the stability of the two loops. The output loop, which is a second-order linear system, is always stable. The input loop is a non-linear second-order system.

From the large-signal switch model, it is found that

$$v_d = dv_{C1}. \tag{8.1}$$

Since the One-Cycle Controlled switch all passes the control reference v_{ref} and fully rejects its input signal v_{C1}, that is

$$v_d = v_{ref}. \tag{8.2}$$

Therefore, the duty-ratio of the One-Cycle Controlled switch is modulated by the following equation:

$$d = \frac{v_{ref}}{v_{C1}} \tag{8.3}$$

The duty-ratio signal of the One-Cycle Controlled switch is a nonlinear function of the voltage across the input capacitor. Since all the other switches are either synchronized or complementary with the One-Cycle Controlled switch, their duty-ratio is determined by the non-linear feedback signal $d = \frac{v_{ref}}{v_{C1}}$. The input loop and the output loop have the structure shown in Fig. 8.2. The system state-space equations are obtained from Fig. 8.2.

$$L_1 \frac{di_{L1}}{dt} = v_g - R_1 i_1 - (1-d)v_{C1} \tag{8.4}$$

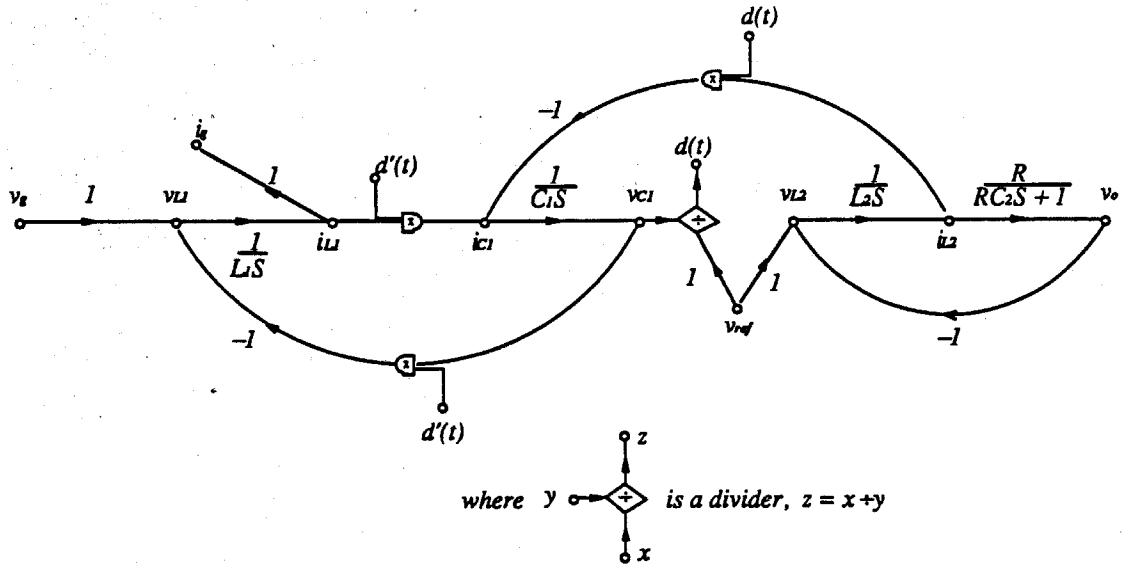


Figure 8.2: The Large-Signal Model of the One-Cycle Controlled Ćuk converter. The duty-ratio signal of the One-Cycle Controlled switch is a nonlinear function of the voltage across the input capacitor. Since all the other switches are either synchronized or compensated with the One-Cycle Controlled switch, their duty-ratio is determined by the non-linear feedback signal $d = \frac{v_{ref}}{v_{C1}}$.

$$C_1 \frac{dv_{C1}}{dt} = (1-d)i_{L1} - di_{L2} \tag{8.5}$$

$$d = \frac{v_{ref}}{v_{C1}} \tag{8.6}$$

Let Equation (8.4) and (8.5) equal zero, that is

$$v_g - R_1 i_1 - (1-d)v_{C1} = 0 \tag{8.7}$$

$$(1-d)i_{L1} - di_{L2} = 0 \tag{8.8}$$

$$d = \frac{v_{ref}}{v_{C1}} \tag{8.9}$$

Equation (8.6), (8.7) and (8.8) generate two singular points, P_1 and P_2, and a singular region $v_{C1} = 0$.

The global dynamic behavior, simulated by TUTSIM program, is shown in Fig. 8.3. There are two singular points, $P_1 = (V_1, I_1)$ and $P_2 = (V_2, I_2)$, and a singular region, the whole i_{L1}-axis. P_1 is a stable spiral point. P_2 is an unstable saddle point. The lower

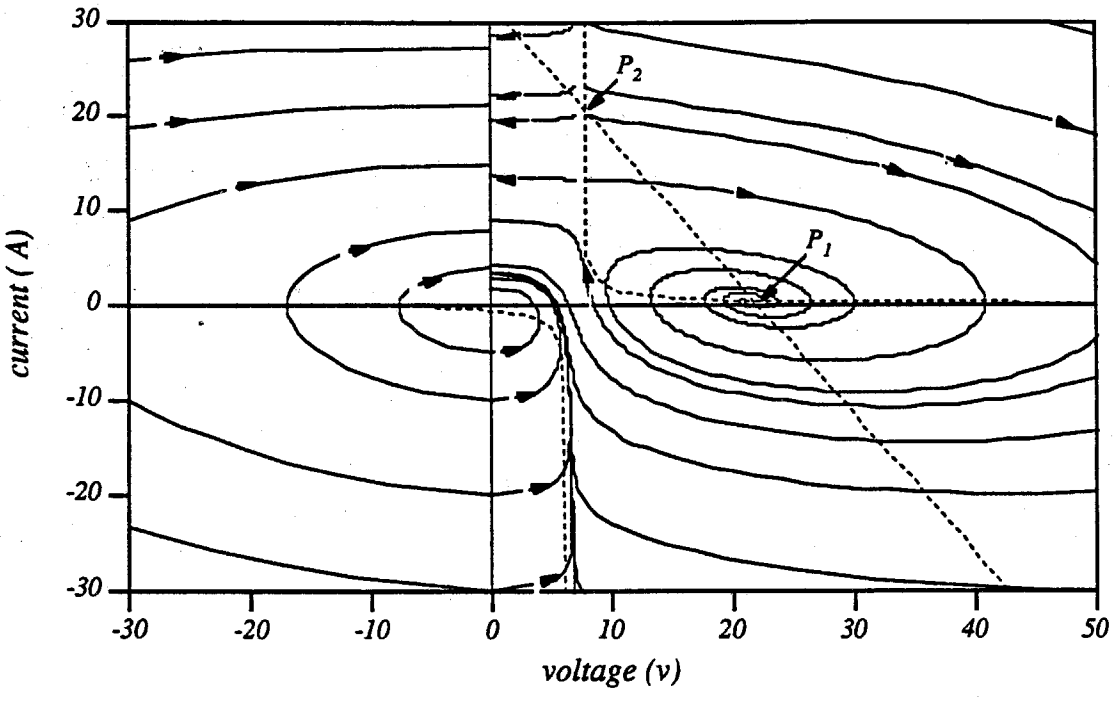


Figure 8.3: The Global Dynamic Behavior of the One-Cycle Controlled Ćuk Converter. The global dynamics is simulated by TUTSIM program. The x-axis represents the voltage across the input capacitor and the y-axis represents the input inductor current i_{L1}. There are two singular points, P_1 and P_2, and a singular region, the whole y-axis. P_1 is a stable spiral point. P_2 is an unstable saddle point. And the lower part of the y-axis is an unstable region, and the upper part of the i_{L1}-axis is stable. The system is not globally stable. The region around the spiral point P_1 is the desired working region.

part of the i_{L1}-axis is an unstable region, and the upper part of the i_{L1}-axis is stable. The system is not globally stable. The region around the spiral point P_1 is the desired working region.

In practice, there is physical restrictions on the duty-ratio, $D_{min} \leq d \leq D_{max}$. When $v_{C1} \leq \frac{v_{ref}}{D_{max}}$, the system operates at the maximum duty-ratio D_{max}; therefore, the system becomes a linear system:

$$L_1 \frac{di_{L1}}{dt} = v_g - R_1 i_1 - (1 - D_{max}) v_{C1} \tag{8.10}$$

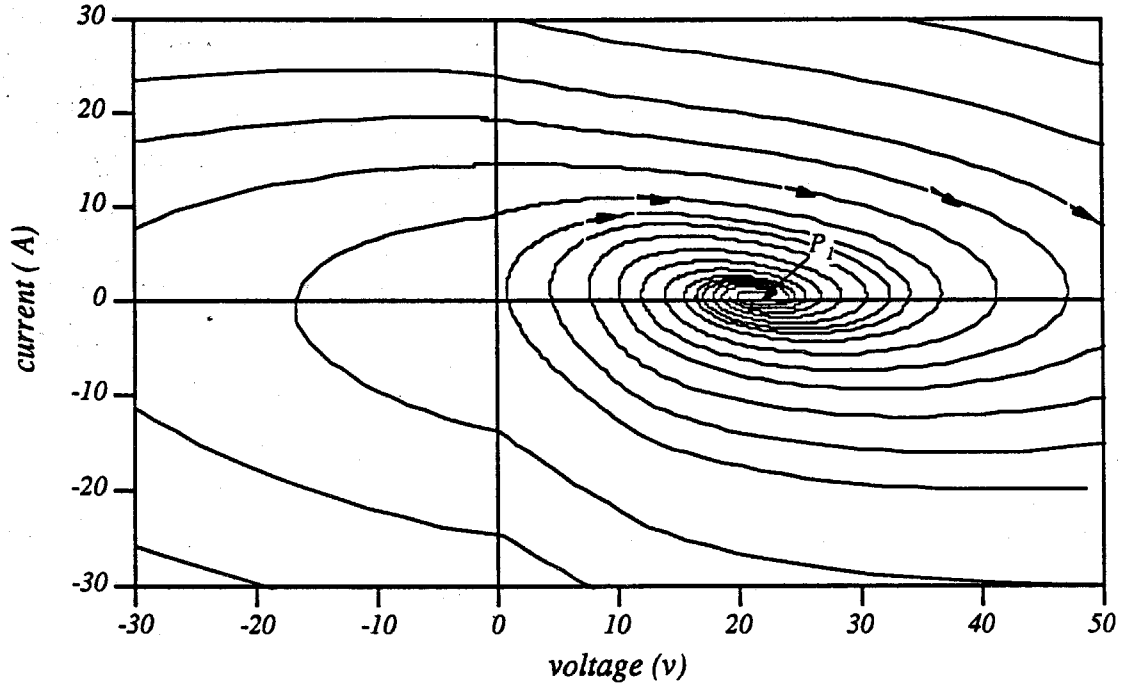


Figure 8.4: The Global Dynamic Behavior with Duty-Ratio Limitation. The x-axis represents the voltage across the input capacitor and the y-axis represents the input inductor current. When $v_{C1} \leq \frac{v_{ref}}{D_{max}}$, or $v_{C1} \geq \frac{v_{ref}}{D_{min}}$, the system becomes a linear second-order system. If the maximum duty-ratio is artificially restricted such that $D_{max} < \frac{v_{ref}}{V_2}$, the unstable saddle point $P_2 = (V_2 < I_2)$ is avoided. Therefore, the system will be globally stable.

$$C_1 \frac{dv_{C1}}{dt} = (1 - D_{max}) i_{L1} - D_{max} i_{L2} \tag{8.11}$$

When $v_{C1} \geq \frac{v_{ref}}{D_{min}}$, the system operates at the minimum duty-ratio d_{min}; therefore, the system becomes a linear system:

$$L_1 \frac{di_{L1}}{dt} = v_g - R_1 i_1 - (1 - D_{min}) v_{C1} \tag{8.12}$$

$$C_1 \frac{dv_{C1}}{dt} = (1 - D_{min}) i_{L1} - D_{min} i_{L2} \tag{8.13}$$

If the maximum duty-ratio is artificially restricted such that $D_{max} < \frac{v_{ref}}{V_2}$, the unstable saddle point $P_2 = (V_2 < I_2)$ is avoided. Therefore, the system will be globally stable. The

global dynamics is found by TUTSIM program as shown in Fig. 8.4. The small-signal model is obtained to study the local dynamic behavior.

8.3 Local Dynamic Behavior

For a linear feedback system, an infinite loop-gain is required in order to have instantaneous control over some variables. In practice, all physical systems have limited band width. Consequently, when the loop-gain is higher than certain value, the loop becomes unstable. Therefore, it is impossible to have instantaneous control for a linear feedback control system.

However, instantaneous control does exist in One-Cycle Controlled converters. For the One-Cycle Controlled Ćuk converter, the average value of the diode-voltage actually has an instantaneous response to the control reference. To further understand One-Cycle Control, a study of the linearized local dynamic behavior and the loop-gain is necessary. The large-signal model of the One-Cycle Controlled switch, from Equation (8.3), is rewritten as follows:

$$d = \frac{v_{ref}}{v_{C1}} \tag{8.14}$$

Suppose the One-Cycle Controlled switch operates around the steady-state point, V_{ref}, V_{C1}, and D with small-signal perturbation, $\hat{v}_{ref}$, $\hat{v}_{C1}$, and $\hat{d}$.

$$v_{ref} = V_{ref} + \hat{v}_{ref} \tag{8.15}$$

$$v_{C1} = V_{C1} + \hat{v}_{C1} \tag{8.16}$$

$$d = D + \hat{d} \tag{8.17}$$

The linearized small-signal model of the One-Cycle Controlled switch is:

$$\hat{d} = \frac{1}{V_{C1}}\hat{v}_{ref} - \frac{D}{V_{C1}}\hat{v}_{C1} \tag{8.18}$$

The duty-ratio signal of the input loop is determined by the control reference and the feedback of the voltage across the input capacitor, as shown in Equation (8.18). The output loop does not contain any switching branch therefore, it is a stable linear second-order system. The linearized small-signal model of the One-Cycle Controlled Ćuk converter is shown in Fig. 8.5.

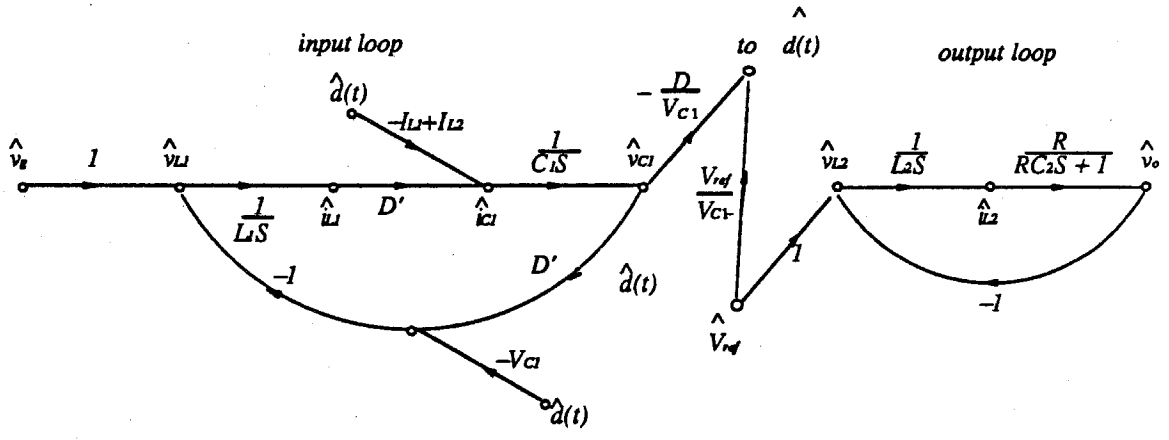


Figure 8.5: The Small-Signal Model of One-Cycle Controlled Ćuk Converter. The duty-ratio signal of the input loop is determined by the control reference and the feedback of the voltage across the input capacitor, $\hat{d}(t) = \hat{d} = \frac{1}{V_{C1}}\hat{v}_{ref} - \frac{D}{V_{C1}}\hat{v}_{C1}$. The output loop does not contain any switching branch, therefore, it is a stable linear second-order system.

Consider the parasitic resistance of the input inductor and the the input capacitor, the linearized small-signal transfer function of the One-Cycle Controlled Ćuk converter is found

$$G = \frac{D(RD'^2 - R_1 D)}{RD'^3} \frac{(1 - \frac{DL_1 S}{RD'^2 - R_1 D})(1 + C_1 R_2 S)}{1 + \frac{C_1(R_1 + D'^2 R_2)}{D'^2} S + \frac{L_1 C_1}{D'^2} S^2} \tag{8.19}$$

A digital injector [15] was built to measure the loop-gain. The predicted and the measured loop-gains are plotted in Fig. 8.6. The loop-gain of the One-Cycle Controlled Ćuk converter is not infinite; it is actually lower than $0db$!

One-Cycle Control instantaneously controls the average value of the diode-voltage.

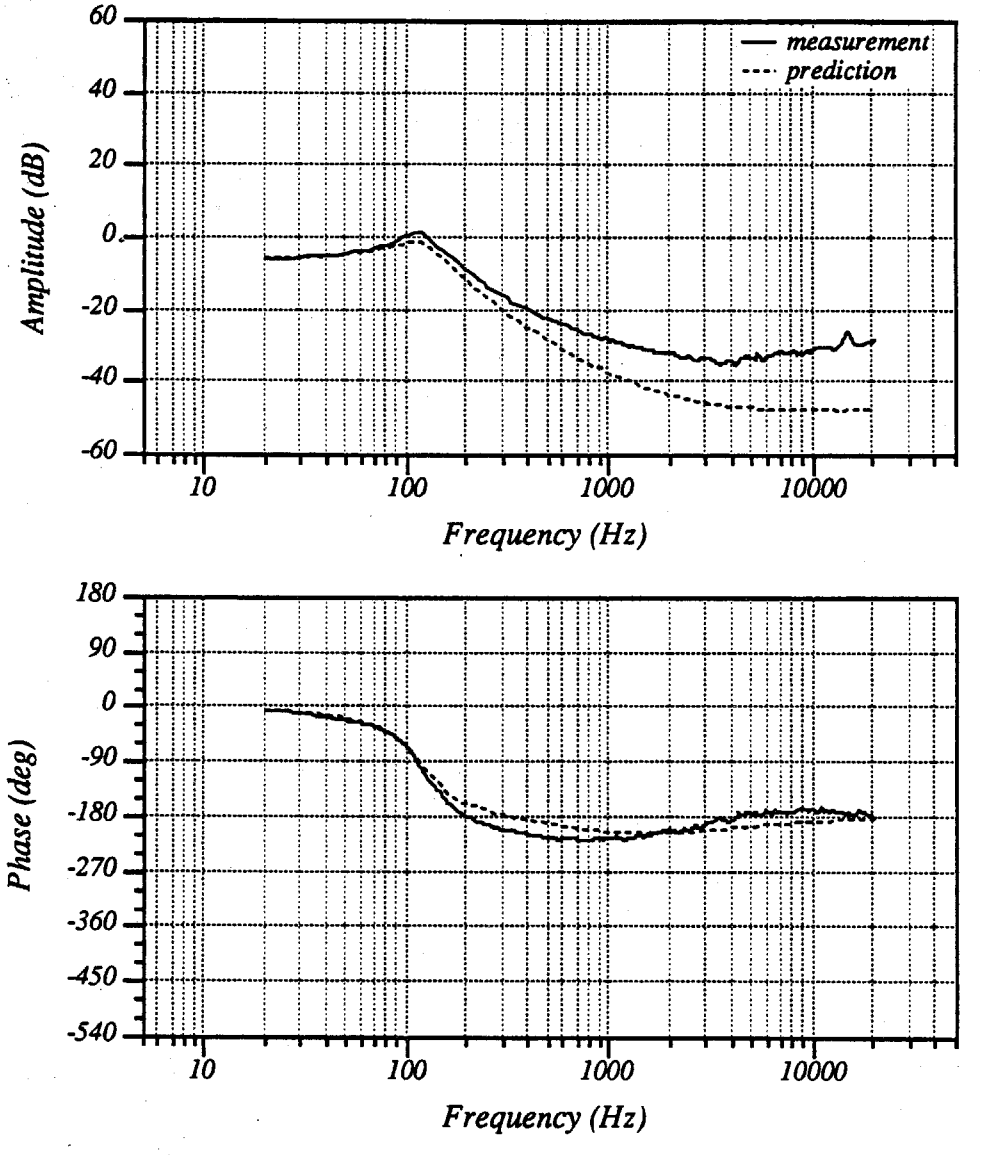


Figure 8.6: The Loop-Gain of the One-Cycle Controlled Ćuk Converter. The prediction is obtained by the Switching Flow-Graph model. The experimental data were measured with the digital injector. It is surprising that the loop-gain is less than zero *db*, though the diode-voltage has instantaneous response to the control reference.

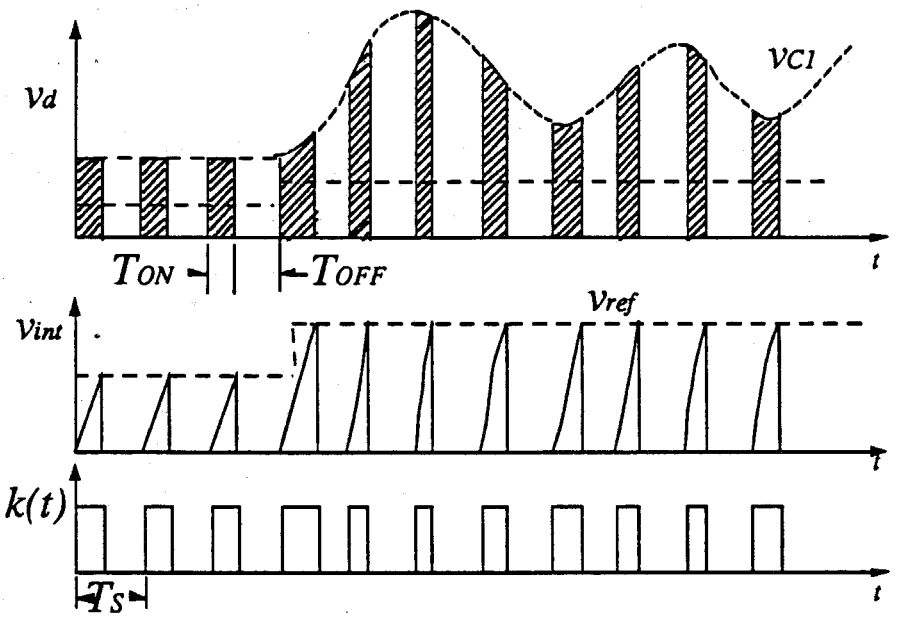


Figure 8.7: Take Advantage of the Pulsed and Nonlinear Nature. When the control reference steps up, the voltage across the input capacitor undergoes an attenuating oscillation. The input signal of the One-Cycle Controlled switch is the capacitor voltage v_{C1}. The output signal of the One-Cycle Controlled switch is the diode-voltage v_d, which has an envelope equal to the capacitor voltage v_{C1}. One-Cycle Control takes advantage of the pulsed and nonlinear nature of the switching converter, and adjusts the average value of the diode-voltage instantaneously. The real transient of the diode-voltage is not instantaneously controlled.

Nevertheless, the loop-gain is not infinite. All the other state variables inside the loop obey the physical laws. The variables actually move along the state-space trajectory shown in Fig. 8.4. As a matter of fact, the voltage across the diode has a finite transient. One-Cycle Control takes advantage of the pulsed and nonlinear nature of the switching converter, and adjusts the average value of the diode-voltage instantaneously. For example, when the control reference steps up, the voltage across the input capacitor undergoes an attenuating oscillation. The input signal of the One-Cycle Controlled switch is the capacitor voltage v_{C1}. The output signal of the One-Cycle Controlled switch is

the diode-voltage v_d, which has an envelope equal to the capacitor voltage v_{C1}. The real-time integrated value is compared with the control reference in each cycle. Therefore, the duty-ratio is precisely adjusted such that the average of the diode-voltage is exactly equal to the control reference. The real transient of the diode-voltage is not instantaneously controlled, as shown in Fig. 8.7.

8.4 Experiments

The experimental One-Cycle Controlled Ćuk converter is shown in Fig. 8.8. The clock triggers the RS flip-flop with constant frequency to turn ON the transistor. The diode-voltage is integrated and compared with the reference voltage v_{ref}. When the integrated value of the diode-voltage reaches the control reference, the comparator changes its state, which resets the RS flip-flop and consequently turns OFF the transistor. A junction FET is used to reset the integrator when the transistor turns off. Five access points are set. Point A, Point B and Point C are used to inject the control signal, the load disturbance, and the input perturbations, respectively. Point B, Point D, and Point E are used to detect the output voltage, the diode-voltage and the integration of the diode-voltage.

Experiment 8.1 Measure the effect of a step response of the control reference on the diode-voltage. A step up function from $2.3V$ to $5V$ was injected into the control reference at Point A, while the input voltage and the load were constant. The integrator output responses were detected at Point E. The experimental results are shown in Fig. 8.9. Since the load and the input voltage are constant, the integration slope is constant. When the control reference stepped up, the integration took longer to reach the control reference. The average value of the diode-voltage jumped to its new steady state in one cycle.

Experiment 8.2 Measure the response of the diode-voltage to a sinusoid wave of the control reference. A sinusoid wave $v_{ref} = 3.4 + 2.2sin\omega t$, $f = 10kHz$, was injected

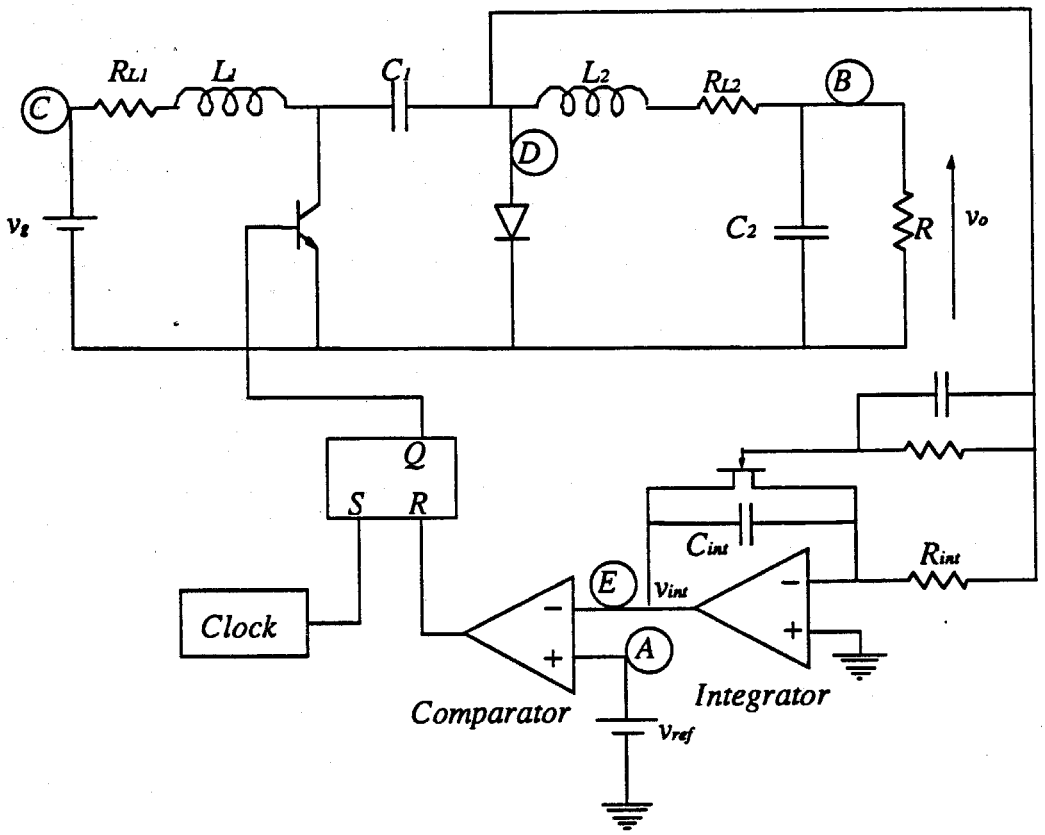


Figure 8.8: The Experimental Ćuk Converter with One-Cycle Control. Point A, Point B and Point C are used to inject the control signal, the load disturbance, and the input perturbations, respectively. Point B, Point D, and Point E are used to detect the output voltage, the diode-voltage and the integration of the diode-voltage.

into the input voltage at Point A, while the input voltage and the load were constant. The integrator output response was measured at Point E. The experimental results are shown in Fig. 8.10. Since the input voltage and the load are constant, the slope of the integration is constant. The integration time is changing with the sinusoid waveform, as a result, the average value of the diode-voltage changes sinusoidly.

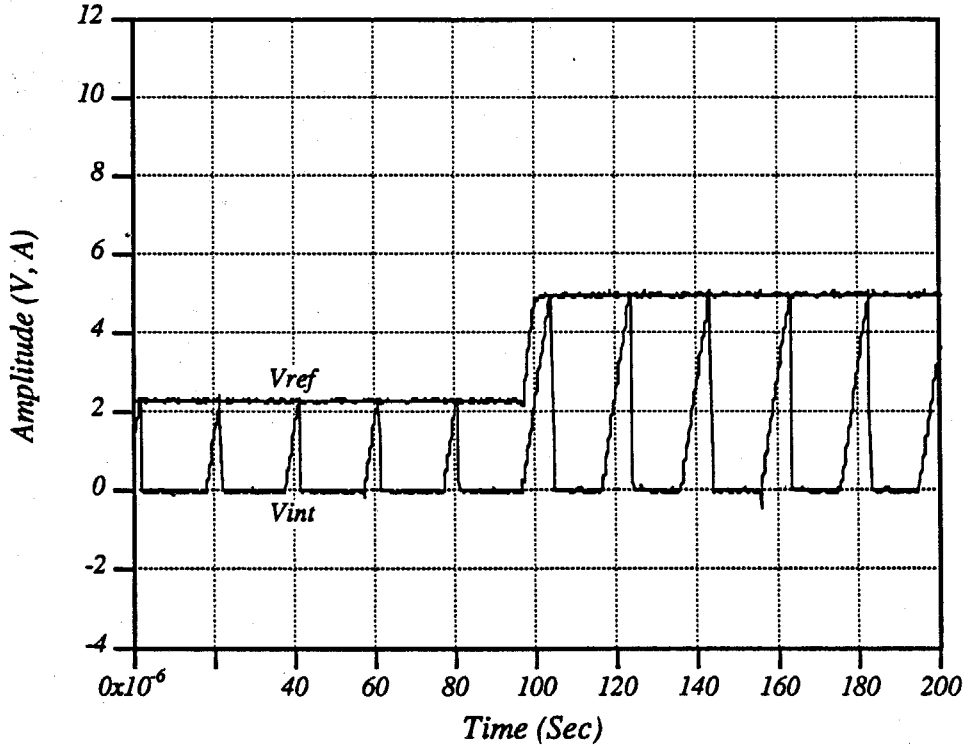


Figure 8.9: Ćuk Converter Follows Step-up of the Control Reference. A step up function from $2.3V$ to $5V$ was injected into the control reference at Point A, and the integrator output responses were detected at Point E. The input voltage and the load were constant. Operating condition: $V_g = 20V$, $f_s = 50kHz$, $L_1 = 2.39mH$, $L_2 = 2.34mH$, $C_1 = 100\mu F$, $C_2 = 1000\mu F$, $R_{L1} = 1\Omega$, $R_{L2} = 1\Omega$, $R = 10\Omega$.

Experiment 8.3 Measure the control-to-diode-voltage frequency response. A sweeping frequency signal was injected to the control reference at Point A, while the diode-voltage response was measured at Point D. The experimental result is plotted in Fig. 8.11. Since the average value of the diode-voltage was fully controlled by the control reference, it was predicted that the frequency response of the diode-voltage to the control reference should be flat. The detected frequency response has a very flat amplitude response and phase lag. Since the diode-voltage is not exactly zero when the transistor is ON, the

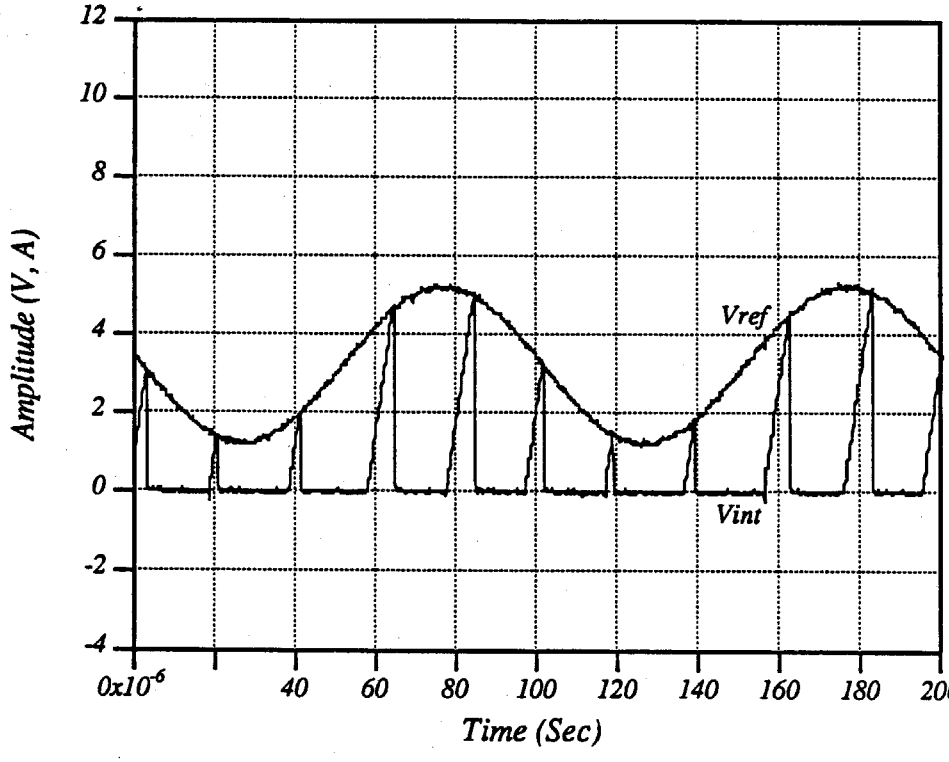


Figure 8.10: Ćuk Converter Follows Sinusoid Change of Control Reference. A sinusoid wave $v_{ref} = 3.4 + 2.2sin\omega t$, $f = 10kHz$, was injected into the input voltage at Point A and the integrator output response was measured at Point E. The input voltage and the load were constant. Operating condition: $V_g = 20V$, $f_s = 50kHz$, $L_1 = 2.39mH$, $L_2 = 2.34mH$, $C_1 = 100\mu F$, $C_2 = 1000\mu F$, $R_{L1} = 1\Omega$, $R_{L2} = 1\Omega$, $R = 10\Omega$.

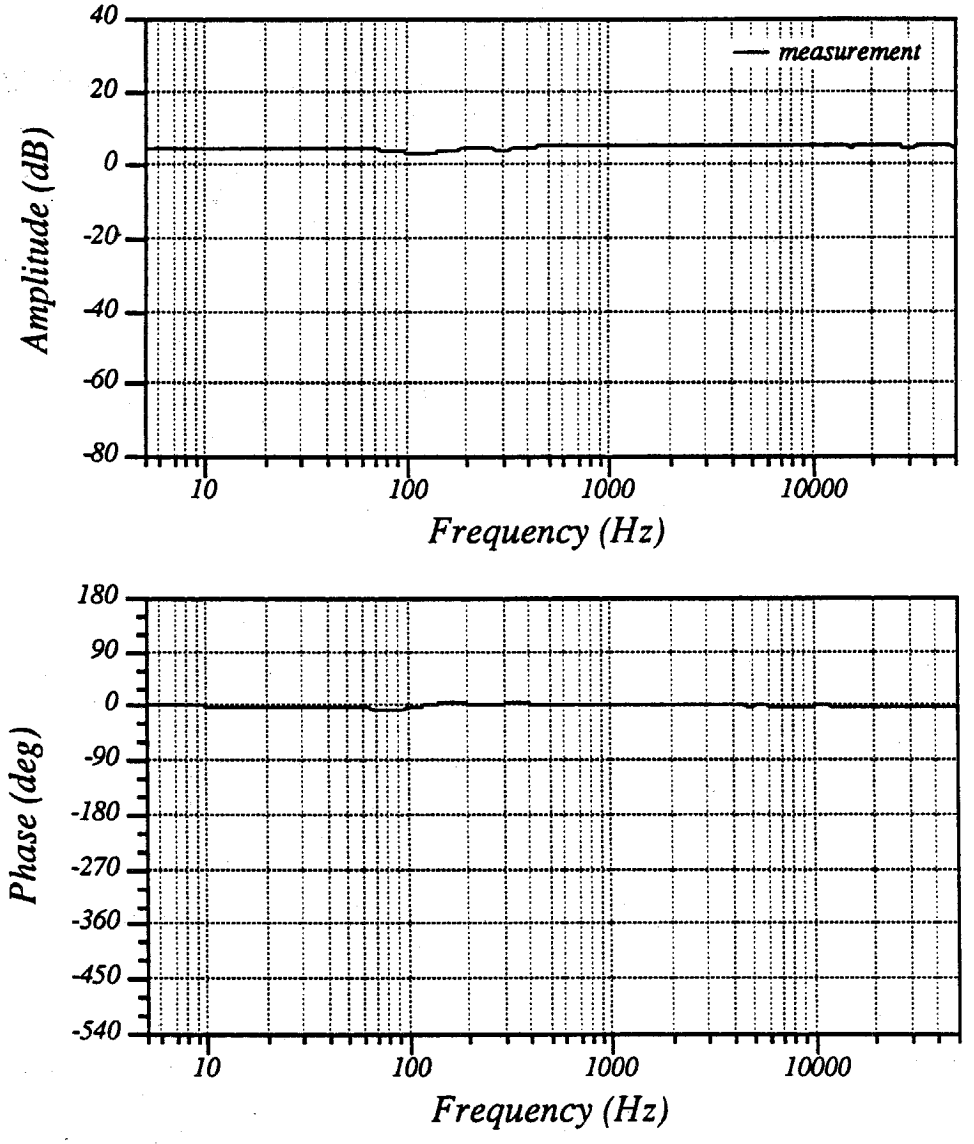


Figure 8.11: The Control-to-Diode-Voltage Frequency Response of the One-Cycle Controlled Ćuk Converter. A sweeping frequency signal was injected to the control reference at Point A, and the diode-voltage response was measured at Point D. Operating condition: $V_g = 20V$, $f_s = 50kHz$, $L_1 = 2.39mH$, $L_2 = 2.34mH$, $C_1 = 100\mu F$, $C_2 = 1000\mu F$, $R_{L1} = 1\Omega$, $R_{L2} = 1\Omega$, $R = 10\Omega$.

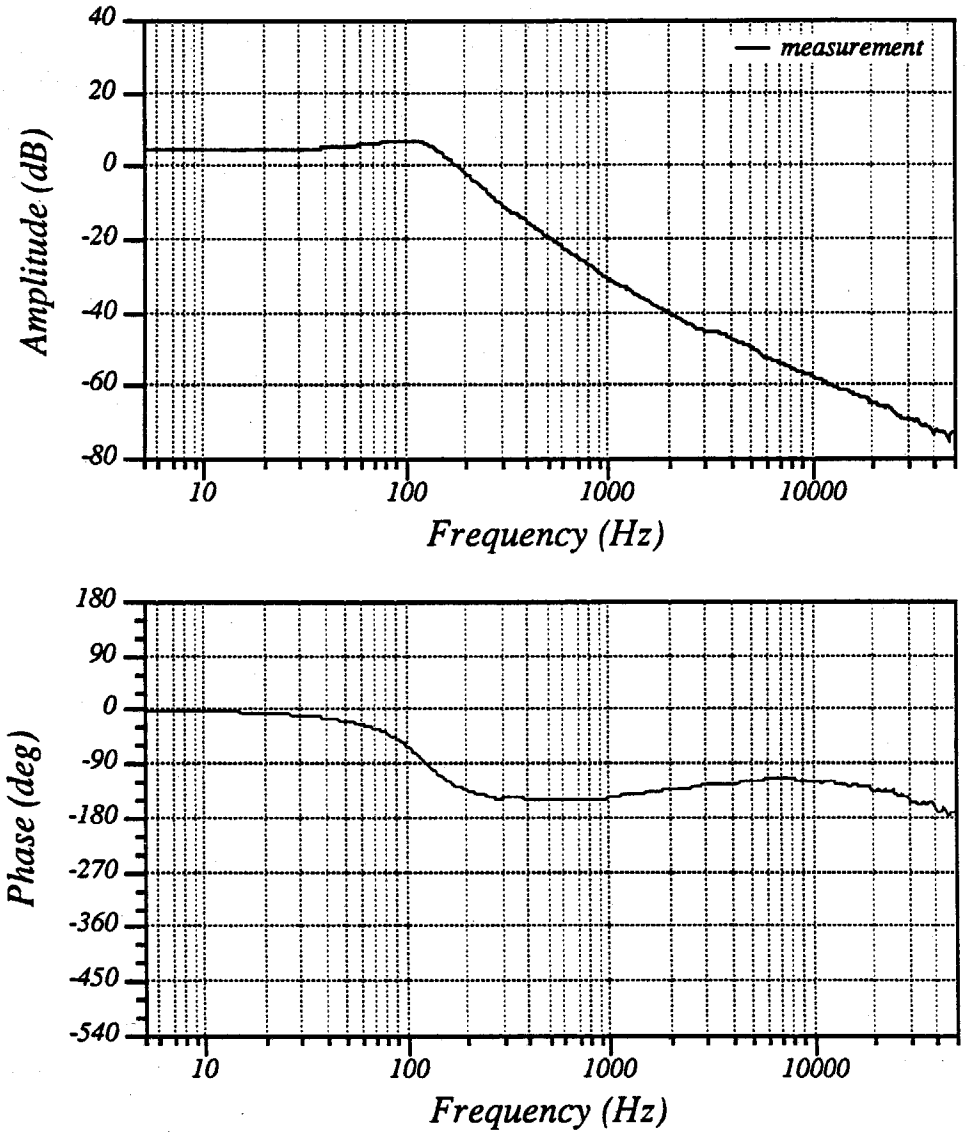


Figure 8.12: The Control-to-Output Frequency Response of the One-Cycle Controlled Ćuk Converter. A sweeping frequency signal was injected to the control reference at Point A, and the output-voltage response was measured at Point B. Operating condition: $V_g = 20V$, $f_s = 50kHz$, $L_1 = 2.39mH$, $L_2 = 2.34mH$, $C_1 = 100\mu F$, $C_2 = 1000\mu F$, $R_{L1} = 1\Omega$, $R_{L2} = 1\Omega$, $R = 10\Omega$.

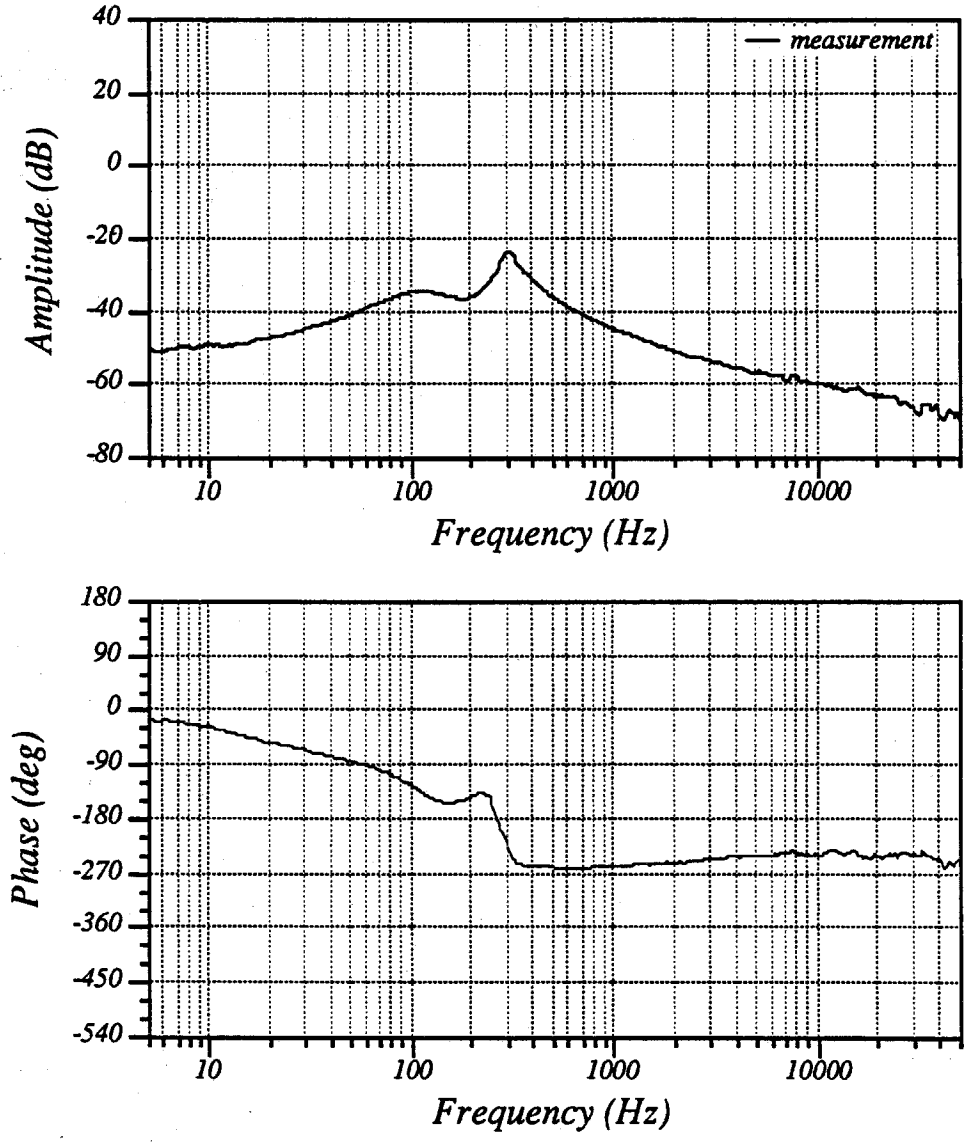


Figure 8.13: The Input-to-Output Frequency Response of the One-Cycle Controlled Ćuk Converter. A sweeping frequency signal was injected to the input voltage at Point C, and the output-voltage response was measured at Point B. Operating condition: $V_g = 20V$, $f_s = 50kHz$, $L_1 = 2.39mH$, $L_2 = 2.34mH$, $C_1 = 100\mu F$, $C_2 = 1000\mu F$, $R_{L1} = 1\Omega$, $R_{L2} = 1\Omega$, $R = 10\Omega$.

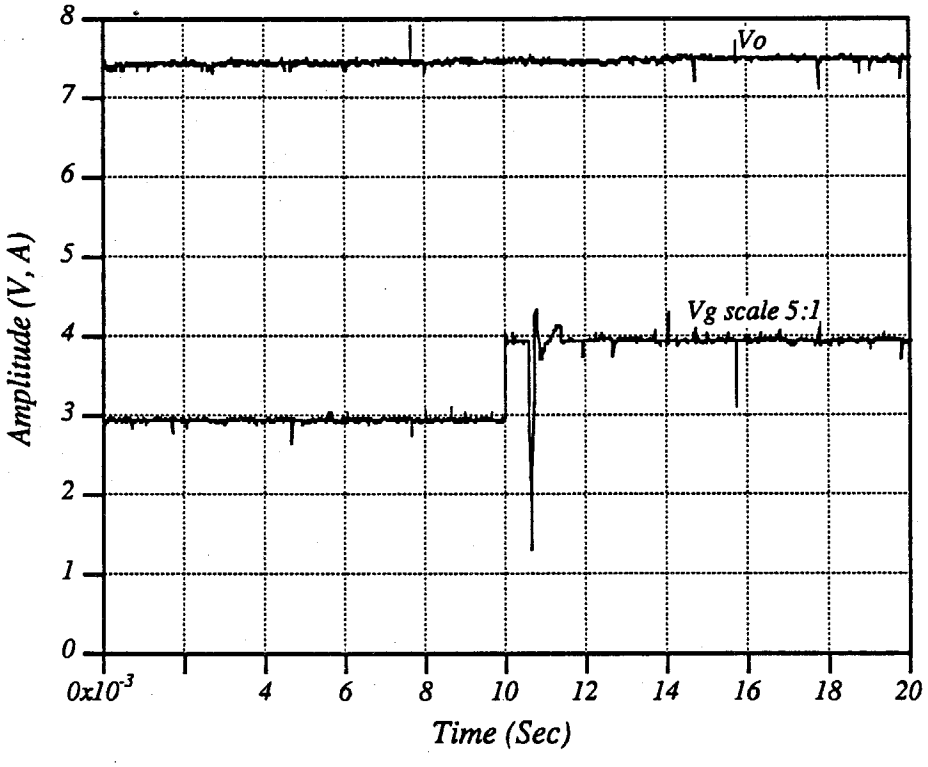


Figure 8.14: The Input-to-Output Step Up Response of the One-Cycle Controlled Ćuk Converter. The input voltage v_g was stepped up from $15V$ to $20V$. The output voltage of the Ćuk converter was almost not affected. Note that the input voltage has been reduced by a factor of five in order to fit it into the plot. Operating condition: $V_g = 20V$, $f_s = 50kHz$, $L_1 = 2.39mH$, $L_2 = 2.34mH$, $C_1 = 100\mu F$, $C_2 = 1000\mu F$, $R_{L1} = 1\Omega$, $R_{L2} = 1\Omega$, $R = 10\Omega$.

frequency response is not completely flat.

Experiment 8.4 Measure the control-to-output frequency response. A sweeping frequency signal was injected to the control reference at Point A, and the output-voltage response was measured at Point B. The experimental result is plotted in Fig. 8.12. As predicted in the previous section, the frequency response of the One-Cycle Controlled Ćuk converter is equivalent to a second-order system.

Experiment 8.5 Measure the input-to-output frequency response. A sweeping frequency signal was injected to the input voltage at Point C, while the output-voltage response was measured at Point B. The experimental result is plotted in Fig. 8.13. It was expected that the system should completely reject the input-voltage perturbation. However, the experimental data show that there were leakages of the input perturbation, especially when the sweeping frequency was near the corner frequency, $300Hz$, of the input filter. This was because the real diode has a non zero conducting resistance, and also because the wire wrap circuit had some AC coupling.

Experiment 8.6 Measure the input-to-output step response of the One-Cycle Controlled Ćuk converter. A step-up function, from $v_g = 15V$ to $v_g = 20V$, was exerted on the input-voltage at Point C, while the output-voltage response was detected at point B. The experimental result is plotted in Fig. 8.14. The One-Cycle Control Ćuk converter has very good input-voltage rejection.

8.5 Summary

The Switching Flow-Graph model is employed to study the large-signal stability and small-signal behavior of the One-Cycle Controlled system. The large-signal dynamic simulation shows that the system is not globally stable. However, if the duty-ratio

limitation is properly set, the system will be globally stable. The small-signal model shows that the One-Cycle Control loop-gain is below $0db$! The fact is that the system dynamics must obey the physical laws. The transients of the capacitor voltage and the inductor current are not instantaneous. The One-Cycle Control takes advantage of the pulsed and non-linear nature and achieves the instantaneous control over the average value of the diode-voltage.

The experiments show that the One-Cycle Controlled Ćuk converter is stable with the duty-ratio limitation. The diode-voltage follows the control reference instantaneously, and has good rejection of the input perturbations. The input dynamics are blocked by the One-Cycle Control. The system is equivalent to a second-order system.

Chapter 9

One-Cycle Control Circuit Design

In practice, the components of the electrical circuits are not ideal. For example, the turn-on time and the turn-off time of transistors and diodes are not instantaneous. Also, the transistors and diodes have non-zero conducting resistances, the operational amplifiers have limited bandwidth, and the comparators have finite speed. In addition, the circuit layout may have AC coupling, etc. Some practical design aspects are discussed in this chapter. The possible effects caused by the physical limitation of the duty-ratio is analyzed in Section 9.1. The condition of discontinuous conduction of switching converters is discussed in Section 9.2. The design procedure for the key component, the real-time integrator, of the One-Cycle Control technique is described in Section 9.3.

9.1 Limitation of the Switching Duty-Ratio

In practice, the duty-ratio d has physical limitations that is

$$0 \leq d \leq 1. \tag{9.1}$$

If the switch turn-on and turn-off time are taken into consideration, the duty-ratio limitation is more limited. In addition, the control circuit must be designed to avoid the unstable operating regions, as the Ćuk converter in Chapter 8. As a result, the duty-ratio limits are

$$D_{min} \leq d \leq D_{max}. \tag{9.2}$$

Therefore, the One-Cycle Control function disappears when the input signal $x(t)$ and the control signal v_{ref} of the switch exceed the limits of Equation (9.2), that is

$$\frac{v_{ref}}{x(t)} > D_{max}, \quad or \quad \frac{v_{ref}}{x(t)} < D_{min}. \tag{9.3}$$

Take the basic buck converter as an example. If the required output voltage is constant, the allowable variation of the input voltage is found from Fig. 9.1. The integration slope is

$$Slope = \frac{v_g}{T_s}. \tag{9.4}$$

The maximum slope and the minimum slope are determined by the limitation of the duty-ratio limitations:

$$Slope_{max} = \frac{v_{ref}}{D_{min}T_s} \tag{9.5}$$

$$Slope_{max} = \frac{v_{ref}}{D_{max}T_s} \tag{9.6}$$

If the input voltage is higher than $\frac{v_{ref}}{D_{min}}$, the time for the integration to reach the control

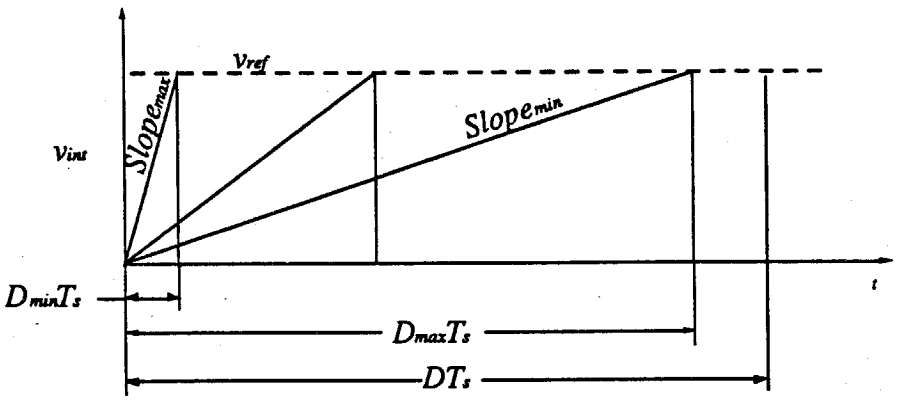


Figure 9.1: The Allowable Operating Range of the Input Voltage of Buck Converter. One-Cycle Control is possible, when the input voltage is inside this range.

reference is shorter than $D_{min}T_s$. In this case, the transistor does not turn OFF until $t = D_{min}T_s$. If the input voltage is lower than $\frac{v_{ref}}{D_{max}}$, the time for the integration to

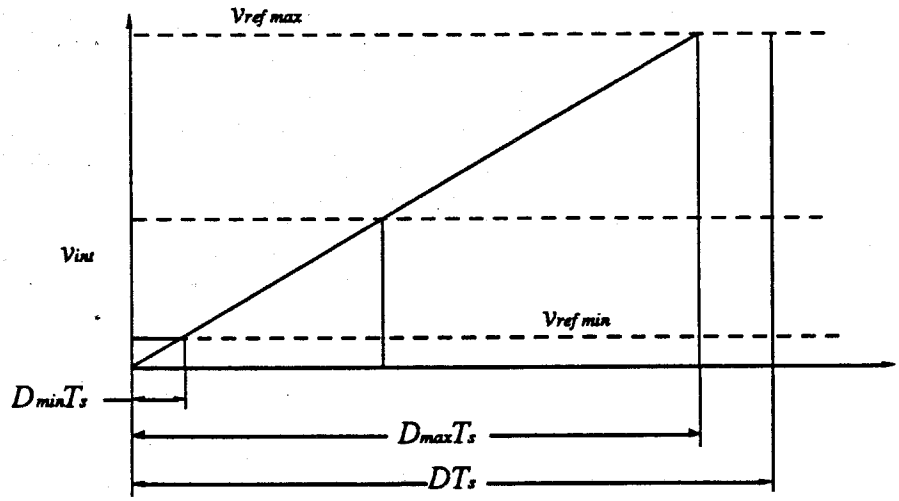


Figure 9.2: The Allowable Range of the Control Reference of Buck Converter. Suppose the input voltage is constant, the control reference has a finite range of variation. If the control reference is outside this range, it can not be attained.

reach the control reference is longer than $D_{max}T_s$. Hence, the transistor turns OFF at $t = D_{max}T_s$; which is before the integration reaches the control reference. Therefore, the allowable range of the input voltage for One-Cycle Control is

$$\frac{v_{ref}}{D_{max}} < v_g < \frac{v_{ref}}{D_{min}}. \tag{9.7}$$

One-Cycle Control is possible when the input voltage is inside this range. If the input voltage is outside this region, the One-Cycle Control no longer exists.

If the input voltage is constant, the control reference has a finite range of variation, as shown in Fig. 9.2.

$$D_{min}v_g < v_{ref} < D_{max}v_g \tag{9.8}$$

When the control reference is lower than $D_{min}v_g$, the integration reaches the control reference before $t = D_{min}T_s$, however, the transistor does not turn OFF until $t = D_{min}T_s$. When the control reference is higher than $D_{max}v_g$ the transistor turns OFF at $t = D_{max}T_s$, before the integration value reaches the control reference. Therefore

it is not possible to obtain the desired output if v_{ref} is outside the range specified in Equation (9.8). The allowable operating region for One-Cycle Control of buck converter is shown in Fig. 9.3.

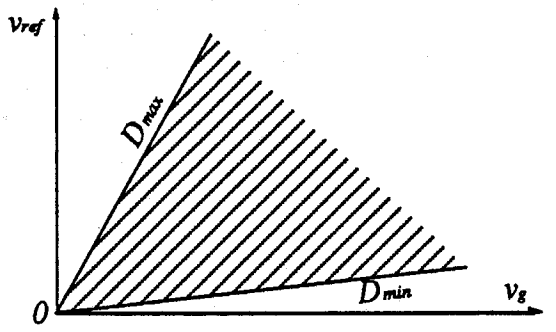


Figure 9.3: One-Cycle Control Operation Region of Buck Converter. One-Cycle Control is possible within this region.

For some converter, such as the Ćuk converter or the buck converter with input filter, the input signal of the One-Cycle Controlled switch is a dynamic function of the other variables in the circuit. For example, the input signal of the One-Cycle Controlled switch of the Ćuk converter is the voltage across the input capacitor v_{C1} that is nonlinearly fed back to control the duty-ratio of other signal switches. Therefore, the voltage of the input capacitor has nonlinear dynamics. If the changes of the control reference and/or the input voltage are to fast or to large, that will cause a dynamics on the voltage across the input capacitor. If $v_{C1} < \frac{v_{ref}}{D_{max}}$, the converter is restricted by its maximum duty-ratio D_{max}, as shown in Fig. 9.4. If $v_{C1} > \frac{v_{ref}}{D_{min}}$, the converter is restricted by its minimum duty-ratio D_{min}, as shown in Fig. 9.5. In these two cases, it takes more than one cycle for the diode-voltage to follow the control reference or to reject the input voltage perturbation.

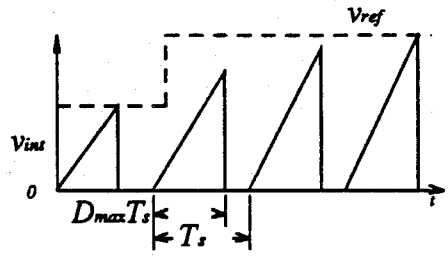


Figure 9.4: One-Cycle Controlled Ćuk Converter Operates under the Maximum Duty-Ratio. When the control reference steps up too fast, the integrated value v_{int} may not reach the control reference in one cycle. Therefore, the maximum duty-ratio limitation shuts the transistor OFF at $t = D_{max}T_s$. The input voltage of the One-Cycle Control switch increases gradually, which causes the slope of the integration to increase. After several cycle, the integrated value reaches the control reference.

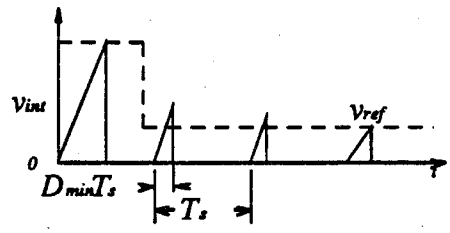


Figure 9.5: One-Cycle Controlled Ćuk Converter Operates under the Minimum Duty-Ratio. When the control reference steps down too fast, the integrated value v_{int} may reach the control reference before $t = D_{min}T_s$. Therefore, the minimum duty-ratio limitation keeps the transistor ON until $t = D_{min}T_s$. The input voltage of the One-Cycle Control switch decreases gradually, which causes the slope of the integration to decrease also. After several cycle, the integrated value reaches the control reference.

9.2 Condition of Discontinuous Conduction

One-Cycle Control is still preserved, when the converter operates under the condition of discontinuous conduction, provided the diode-voltage is used to control the reset switch. Take the buck converter, shown in Fig. 7.23 as an example. The diode-voltage in the discontinuous mode is shown in Fig. 9.6. At $t = t_1$, the transistor is turned OFF, the

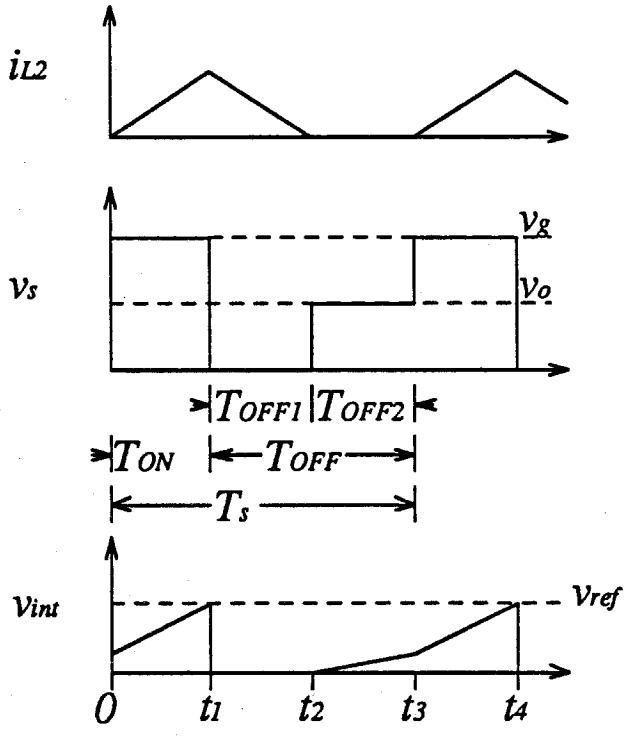


Figure 9.6: One-Cycle Control of Buck Converter at Discontinuous Conducting Condition. The transistor is turned OFF as $t = t_1$, the inductor current starts to decrease, the diode is conducting, therefore, the diode-voltage is zero. At $t = t_2$, the inductor runs out of current, the transistor is still OFF, the diode current drops to zero; therefore, the voltage of the diode is equal to the output voltage. The integration is started no sooner than the inductor current drops to zero. At $t = t_3$, the transistor is turned ON by the clock and the diode-voltage jumps to the input voltage level. The integration slope jumps up accordingly. When the integration value reaches the control reference, the transistor is turned OFF. Any voltage across the diode is integrated.

inductor current starts to decrease. During the time from t_1 to t_2, the diode conducts;

therefore, the diode-voltage is $v_s = 0$. At $t = t_2$, the inductor runs out of current, while the transistor is still OFF. During the time from t_2 to t_3, the diode-voltage is equal to the output voltage. The integration is started immediately after the inductor current drops to zero. At $t = t_3$, the transistor is turned ON by the clock, the diode-voltage jumps to the input voltage level, and the integration slope jumps up accordingly. When the integrated diode-voltage reaches the control reference, the transistor is turned OFF.

$$v_{int} = \frac{1}{T_s}\left(\int_{t_2}^{t_3} v_o dt + \int_{t_3}^{t_4} v_g dt\right) \tag{9.9}$$

$$= v_{ref} \tag{9.10}$$

The output voltage v_0 equals the average value of the diode-voltage over the switch cycle; therefore, One-Cycle Control remains valid even if the switching converter operates in the discontinuous mode.

9.3 Integrator Design

The real-time integrator is the key component in the One-Cycle Control technique. Fig. 9.7 shows an integrator for the One-Cycle Control of constant frequency switches. The integrator is composed of an operational amplifier, a resistor R_{int} and a capacitor C_{int}. The switch output signal v_s is integrated and the integrated value is v_{int}. The choice of the operational amplifier is very important, because it directly influences the accuracy of the integration. Suppose the operational amplifier is ideal, ie. the bandwidth and the DC gain are infinite, then the transfer function of the integrator is

$$\frac{v_{int}(S)}{v_d(S)} = \frac{1}{R_{int}C_{int}S}. \tag{9.11}$$

In the time domain the relationship is

$$v_{int} = \frac{1}{R_{int}C_{int}}\int_0^t v_d(t)dt. \tag{9.12}$$

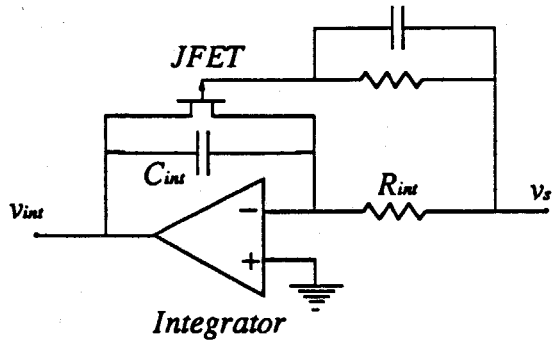


Figure 9.7: The Real-Time Integrator. The operational amplifier, the resistor R_{int} and capacitor C_{int} compose an integrator. The switch output signal v_s is integrated and the integrated value is v_{int}. The junction FET is used to reset the integrator in each cycle.

However, the real operational amplifier has finite gain and finite bandwidth, ie. the transfer function of the operational amplifier is:

$$A(S) = \frac{A_0}{1 + \frac{S}{\omega_0}} \tag{9.13}$$

where A_0 is the DC gain and ω_0 is the corner frequency. Therefore, the transfer function of the integration becomes

$$\frac{v_{int}(S)}{v_d(S)} = \frac{1}{R_{int}C_{int}S} \frac{1}{(1 + \frac{S}{A_0\omega_0} + \frac{1}{A_0R_{int}C_{int}S})}. \tag{9.14}$$

where $\frac{S}{A_0\omega_0}$ is due to the finite bandwidth ω_0 and $\frac{1}{A_0R_{int}C_{int}S}$ is caused by the finite gain A_0. The finite bandwidth affects the integration accuracy at high frequency, whereas finite gain affects the integration accuracy at low frequency. At low frequency, the transfer function of the integration is

$$\frac{v_{int}(S)}{v_d(S)} = \frac{1}{R_{int}C_{int}S} \frac{1}{(1 + \frac{1}{A_0R_{int}C_{int}S})}. \tag{9.15}$$

The step response in the time domain is

$$v_{int} = A_0(1 - e^{-\frac{t}{A_0R_{int}C_{int}}}) \tag{9.16}$$

$$\approx \frac{t}{R_{int}C_{int}} - \frac{t^2}{2A_0R_{int}^2C_{int}^2}. \tag{9.17}$$

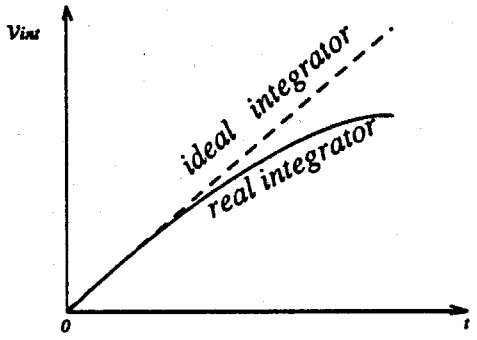


Figure 9.8: Integration Error due to Finite DC Gain. The finite DC gain of the operational amplifier causes non-linear behavior of the integration.

The step response of the integrator is shown in Fig. 9.8. The maximum integrating time of the One-Cycle Control circuit is $D_{max}T_s$; therefore, the integration error is

$$\Delta v_{int} = \frac{D_{max}T_s}{2A_0R_{int}C_{int}}. \tag{9.18}$$

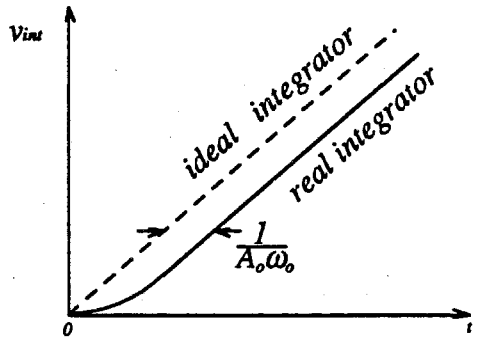


Figure 9.9: Integration Error due to Finite Bandwidth. The finite bandwidth of the operational amplifier causes the integration delay.

At high frequency, the transfer function of the integration is

$$\frac{v_{int}(S)}{v_d(S)} = \frac{1}{R_{int}C_{int}S}\frac{1}{(1+\frac{S}{A_0\omega_0})}. \tag{9.19}$$

The time domain frequency response is

$$v_{int} \approx \frac{1}{R_{int}C_{int}}(t - \frac{1}{A_0\omega_0}). \tag{9.20}$$

The step response of the integrator is shown in Fig. 9.9. The finite bandwidth causes a time delay $\frac{1}{A_0\omega_0}$; therefore, the integration error is

$$\Delta v_{int} = \frac{1}{D_{max}T_sA_0\omega_0}. \tag{9.21}$$

Further consider the input impedance R_i of the operational amplifier, the step response of the integrator is:

$$v_{int} = \frac{t}{R_{int}C_{int}} - \frac{t^2}{2A_0(R_{int} \parallel R_i)R_{int}C_{int}^2} \tag{9.22}$$

The error is found

$$error = \frac{D_{max}T_s}{2A_0(R_{int} \parallel R_i)C_{int}}. \tag{9.23}$$

If the resistor $R_{int} > 10R_i$, the error due to the finite input impedance can be ignored.

From the above analysis, it is clear that the operational amplifier must have high input impedance, high DC gain, and high bandwidth. The operational amplifier must satisfy the following conditions.

$$R_i > 10R_{int} \tag{9.24}$$

$$A_o > \frac{D_{max}Ts}{2R_{int}C_{int}\Delta v_{int}} \tag{9.25}$$

$$\omega_0 > \frac{1}{D_{max}T_s\Delta v_{int}} \tag{9.26}$$

A low loss capacitor and a low inductance resistor are required for the integrator.

The junction FET is used to reset the integrator each cycle. In order to achieve a fast reset, a junction FET with low conducting resistance must be used. It is necessary to complete the reset before the transistor turns ON for the next cycle. Therefore, the on-resistance R_{on} of the junction FET must be

$$R_{on}C_{int} < T_s(1 - D_{max}). \tag{9.27}$$

The reset control signal comes directly from the diode-voltage; therefore, One-Cycle Control still functions when the switching converter is operating in discontinuous mode. For different polarity of the diode-voltage, different type of junction FET is used. For positively biased diode-voltage, a P-channel junction FET is required, whereas for the negatively biased diode-voltage, a N-channel junction is required.

9.4 Summary

In a real circuit design, the operating condition of the switching converter and the physical limitations of the electrical elements affects the quality of the One-Cycle Control. One must aware that One-Cycle Control may not function properly if the circuit is operating near its duty-ratio limits. One-Cycle Control function is still preserved even if the switching converter is in discontinuous mode, provided the reset switch is designed such that the reset signal comes directly from the diode-voltage. For the integrator design, the choice of operational amplifier is very important. High input impedance, high DC gain, and high frequency bandwidth of the operational amplifier yield high accuracy.

Chapter 10

Conclusion

The work in this thesis was directed toward the developement of the Switching Flow-Graph modelling tool and the conception of the One-Cycle Control technique.

The Switching Flow-Graph technique provides a unified graphical representation of the large-signal non-linear model, the small-signal model, and the steady-state model for any given pulse-width-modulated (PWM) switching converter. The graphic models are very easy to obtain and they yield a visual and physical understanding of switching converter systems. The large-signal model and the small-signal model are verified by experiments. The measurements and the theoretical predictions are very close. This technique can be used to model very complicated switching converters, such as the coupled inductor converter, linear feedback systems, and nonlinear feedback systems, etc.

The modelling procedures are as follows: First, find the two subcircuits, the ON-circuit, switch ON, and the OFF-circuit, switch OFF, for the given switching converter. Second, draw the flow-graphs for the two subcircuits and combine them using the switching branches. Then, replace the switching branches with the large-signal model to obtain the large-signal Switching Flow-Graph, replace the switching branches with the small-signal model to obtain the small-signal Switching Flow-Graph, or replace the switching branches with the steady-state model to obtain the steady-state Switching Flow-Graph. Finally, the algebraic rules of the flow-graph can be used to simplify the small-signal model or the steady-state model.

With this Switching Flow-Graph model, one can easily obtain the input-output gain and the power processing efficiency for the steady-state design. The large-signal model is compatible with the TUTSIM simulation program. By simply entering the flow-graph branches, the interconnections, the step size for the simulation, and the initial conditions, the program automatically generates the large-signal dynamical responses. The large-signal model gives a global view of the system dynamics, which enables the designer to understand the limits of the system, and helps the designer to achieve robust control. The small-signal model provides the analytic and graphic frequency response relations between each variable. This enables the designer to do small-signal performance adjustments. These procedures may need to be repeated before a satisfactory closed-loop switching converter design is obtained. However, the approach using Switching Flow-Graph technique is faster, easier, and more robust than any other modelling tool.

The One-Cycle Control technique is designed to control the duty-ratio d of the switch in real time, such that in *each cycle* the average of the chopped waveform at the switch output is *exactly* equal to the control reference. With One-Cycle Control, a switching converter rejects the input voltage perturbations, and can follow the control reference quickly. Implementation circuits are found for any type of switch, constant frequency, constant ON-time, constant OFF-time, and variable. Therefore, the One-Cycle Control technique is suitable for large-signal robust control of PWM switching converters and quasi-resonant converters, inverters, and rectifiers. This technique may also useful for signal processing and other applications.

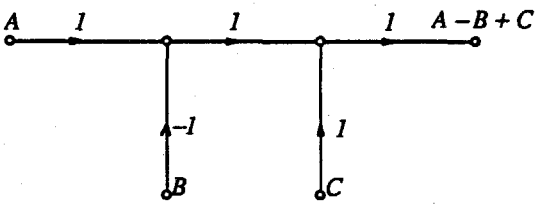
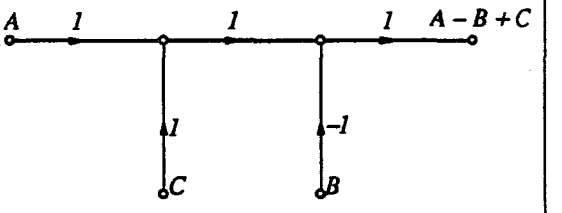
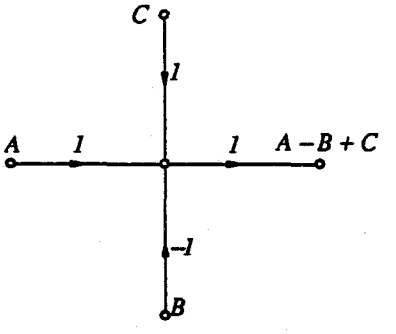
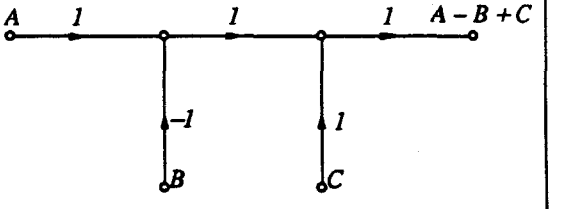
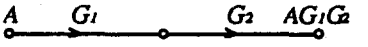
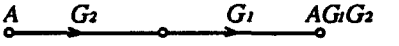
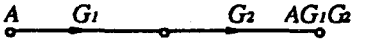
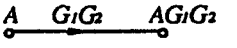
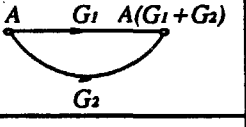
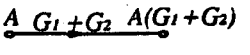
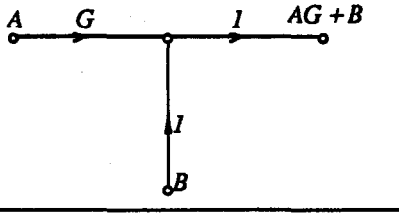
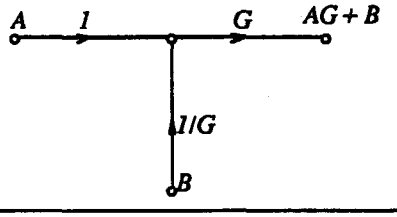
Under ideal conditions, converters with One-Cycle Control are capable of rejecting the input-voltage perturbations, and the diode-voltage is able to follow the control signal instantaneously, within one cycle. Therefore, the One-Cycle Controlled converter is

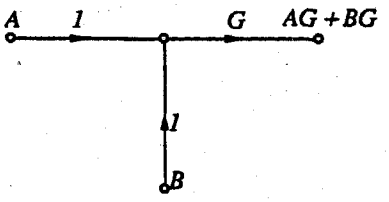
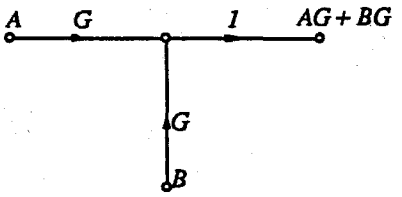
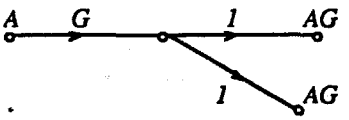
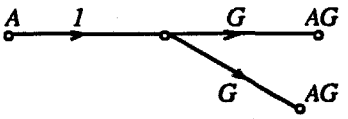
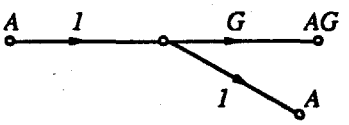
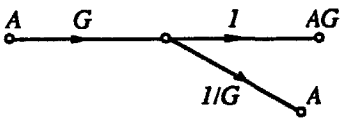
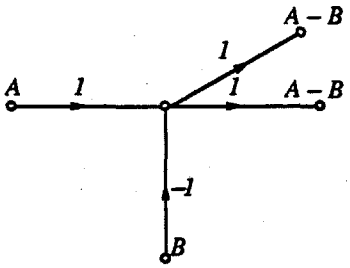
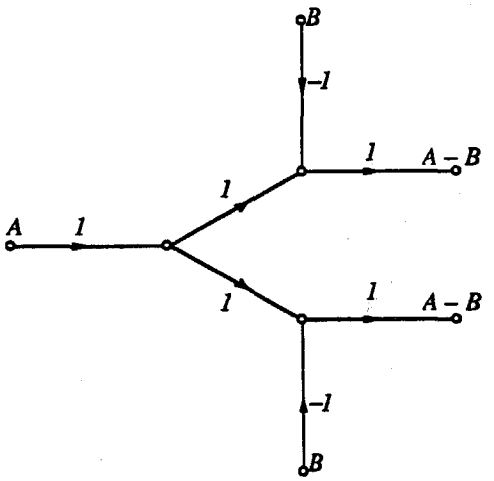
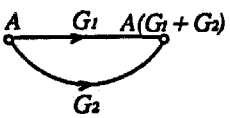
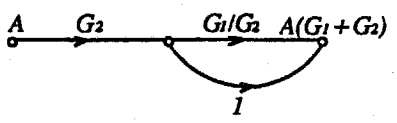
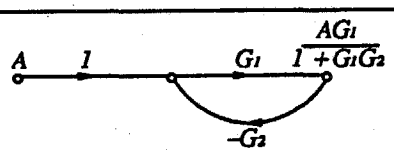
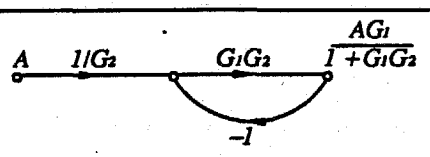
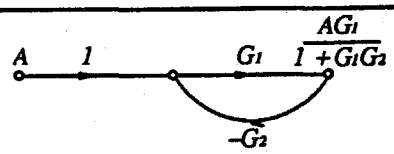
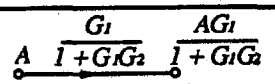
equivalent to a controllable voltage source with an output filter. However, in practice, the switches, the transistors, and the diodes are not ideal switches. Also the integration is not instantaneous. Therefore, the accuracy of One-Cycle Control is greatly dependent on the circuit design. The experimental circuits of a buck converter and a Ćuk converter in this work show a very close match between the measurements and the theoretical predictions. The dynamic behavior, for both the large-signal and the small-signal cases, of One-Cycle Control is analyzed for the Ćuk converter. The Switching Flow-Graph model shows that the One-Cycle Control Ćuk converter is not globally stable. However, imposing a limitation on the duty-ratio $D_{min} \leq d \leq D_{max}$ prevents the converter from operating in the unstable region. As a result, the system is globally stable and behaves like a second-order linear system.

The One-Cycle Control concept is straightforward and its implementation circuits are simple; yet it provides very good control of switching converters.

Appendix A

The Algebraic Rules of the Flow-Graph

	ORIGINAL	EQUIVALENT
(1)		
(2)		
(3)		
(4)		
(5)		
(6)		

(7)		
(8)		
(9)		
(10)		
(11)		
(12)		
(13)		

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