Frequency Generation Techniques for Integrated Applications

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Faciendi plures libros nullus est finis frequensque meditatio carnis afflictio est.

Liber Ecclesiastes 12,12

Venite ad me omnes qui laboratis et onerati estis et ego reficiam vos.

Evangelium Secundum Matthaeum 11,28

Abstract

This thesis presents novel oscillator topologies and passive structures that demonstrate improvements in performance compared to existing devices in CMOS. The contributions of this work include the development of original topologies and concepts together with practical implications in the area of integrated frequency generation.

A noise-shifting differential Colpitts oscillator topology is proposed. It is less sensitive to noise generated by the active devices than commonly used integrated oscillator topologies such as NMOS- or PMOS-only, and complementary cross-coupled. This is achieved through cyclostationary noise alignment while providing a fully differential output and large loop gain for reliable start up. An optimization strategy is derived for this oscillator that is used in the implementation of a CMOS prototype. The performance of this oscillator is compared to traditional topologies and previously published integrated oscillators achieving lower phase noise and some of the highest figures of merit, respectively.

A new circular-geometry oscillator topology is introduced. It allows the implementation of slab inductors for high-frequency and low-phase noise oscillator applications. Slab inductors present an attractive alternative for monolitic applications where low loss, low impedance, and high self-resonance integrated inductors are required. A general methodology to ensure the proper oscillation mode when several oscillator cores are coupled in a circular-geometry as well as to achieve a stable dc bias point is offered. Several circular-geometry CMOS integrated oscillator prototypes are presented as a proof of concept and their performances are compared to previously published high frequency oscillators achieving some of the best figures of merit.

Theoretical limits for the capacitance density of integrated capacitors with combined lateral and vertical field components are derived. These limits are used to investigate the efficiency of various capacitive structures such as lateral flux and quasi-fractal capacitors.

This study leads to two new capacitor structures with high lateral-field efficiencies. These new capacitors demonstrate larger capacities, superior matching properties, tighter tolerances, and higher self-resonance frequencies than the standard horizontal parallel plate and previously reported lateral-field capacitors, while maintaining comparable quality factors. These superior qualities are verified by simulation and experimental results.

Finally, three phase-locked-loops (PLL) are presented. A 6.6GHz PLL for applications in a concurrent dual-band CMOS receiver is described. Careful frequency planning allows the generation of the three local oscillator signals required by the entire receiver using only one PLL, reducing power consumption and chip area considerably. The design issues of an ultra-low-power PLL prototype implemented in a sub-micron CMOS process are also discussed. The design of a low-power 3.2GHz PLL implementing a phase-compensation technique for fractional-N frequency synthesis is described. It uses an on-chip delay-locked-loop tuning scheme that attenuates the fractional spur independent of the output frequency and process variations.

Table of Contents

List of Tables

Chapter 8: Conclusion

List of Figures

Chapter 1: Introduction

Chapter 2: Frequency Generation Fundamentals

Chapter 3: A Noise Shifting Colpitts VCO

Chapter 4: Circular-Geometry Oscillators

Chapter 5: Quadrature Signal Generation

Chapter 6: Capacity Limits and Matching Properties of Integrated Capacitors

Chapter 7: Closed Loop Frequency Generation

Chapter 8: Conclusion

Chapter 1 Introduction

The end of the twentieth century and the beginning of the twenty-first century will be remembered by the tremendous growth of mobile communications. Driven by economical and technological forces, small and low-cost handheld devices have invaded the market. For instance, mobile phone sales totaled 115 million units in the second quarter of 2003, where as the 2004 global cell phones sales is expected to top 500 million units. This is mainly because of the demand for mobile phones with E-mail and Internet access capabilities, and models with integrated digital cameras, FM tuners, MP3 music players, personal digital assistants (PDA) and other commodities [1].

Technology improvements and market growth have been pushing for higher quality of service in transmission and reception of information at faster data rates. For example, third generation (3G) communication systems enable high-speed data communication, mobile Internet, E-mail, video on demand, and E-commerce. Also, short-range wireless local area networks (WLAN) have emerged, leading to standards such as the IEEE802.11a and its European counterpart HIPERLAN, that target for 54Mbps at 5GHz, while the IEE802.11b and the recent IEEE802.11g enable data rates of 11Mbps and 22-50Mbps, respectively, at 2.4GHz. The variety of wireless standards and communication methods will continue to present major challenges for telecommunication design engineers.

1.1 Motivation

Economy of sale forces the phone manufacturers to integrate as many of the elements as possible. This reduces both cost and size via a reduction on the number of components, making the wireless handheld devices small, affordable, and user-friendly. This evolution

continues ultimately towards the single-chip mobile radio. To accomplish this, architectural and technological integration innovations are required.

There are several benefits obtained from a higher degree of integration. The absence of external nodes reduces package parasitics, interference, noise, and signal coupling. Fewer external nodes translate to a smaller package size with less pin number count, thus leading to an smaller system. Lower power consumption is also achieved since there is no need for off-chip signal buffering. Higher predictability and repeatability are an important benefit of higher levels of integration. Additionally, higher integration reduces the number of external components that lower the manufacturing costs considerably.

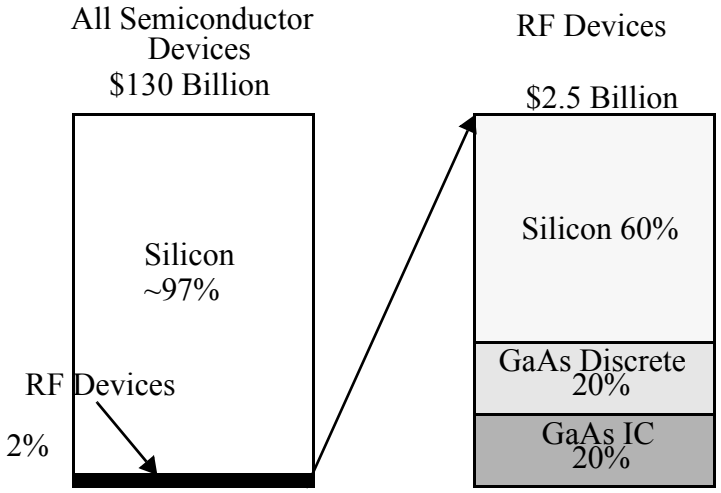


Figure 1.1: Breakdown of silicon and GaAs technologies in the total and RF semiconductor revenue.

Although GaAs technology has been used to implement RF circuits, CMOS technology *can* be applied to RF circuits [2]-[4]. The higher yield and reliability of silicon technologies increases the number of available transistor on a single chip, generating new possibilities not conceivable in GaAs or other III-V technologies. CMOS technology is particularly promising as the wafer manufacturing costs of CMOS are much lower than GaAs. Moreover, fierce competition between CMOS foundries is expected, which will further reduce these costs. These are mainly because over 97% of the total semiconductor

devices produced worldwide are manufactured in CMOS technology [5] (Figure 1.1). On the other hand, GaAs only occupies about 1% of the market share. Therefore, aggressive cost reduction and heavy competition has been experienced by silicon technology over the last several years and is expected to continue.

For certain RF applications, pure CMOS technology may not be suitable. For some of these applications, technologies such as SiGe-BiCMOS have been introduced as alternatives for applications that require higher performances. These more specialized processes increase the manufacturing costs by 10% to 50% due to the extra processing steps required for the availability of NPN transistors, MIM capacitances, resistors, and thick top metal layers [6]. Although the NPN transistors available in SiGe-BiCMOS technology can be faster, the lack of competition in this industry compared to CMOS would make it unlikely that the price will decrease resulting in a solution not as cost-effective as CMOS technology.

One of the major challenges towards the integration of the CMOS-only radio is the frequency generation block. The spectral purity of the local oscillator signals is one of the most critical parameters affecting the reliability and quality for the transfer of information in this radio [7][8]. Unfortunately, there are several obstacles that can deteriorate the performance of CMOS oscillators. The transistor devices readily available in these process technologies generate high active device noise due to short channel and hot electron effects [9]. Therefore, these circuits suffer from a worse noise performance than modules fabricated using discrete components. Also, the driving force in CMOS technologies are digital applications, therefore, these technologies are not optimized for analog or RF applications. Furthermore, to avoid latch up of the digital circuits, the silicon substrate is fairly conductive and increases the signal loss because of the energy coupled, both inductively and capacitivelly, into the substrate, resulting in lossy passive components.

With the goal of overcoming these drawbacks of CMOS technology, novel circuit topologies and passive structures will be presented in this dissertation. These new structures demonstrate significant improvements in performance compared to existing devices in CMOS.

1.2 Organization of the Dissertation

After reviewing the traditional frequency generation fundamentals, a brief overview of the coherent indirect frequency synthesis basics will be explained in Chapter 2. We will then focus on the spectral purity of phase-locked-loops (PLL) and local oscillators as well as the integration challenges imposed by silicon technology with further detail.

Chapter 3 compares the existing oscillator topologies with an emphasis on the cyclostationarity of noise sources and presents the design evolution leading to a topology that lowers the phase noise through cylostationary noise alignment. This new topology provides a fully differential output and a large loop gain for reliable start up. A design strategy is also devised for this oscillator and the phase noise performance of a CMOS prototype is compared to previously published integrated oscillators achieving some of the highest figures of merit.

A new circular-geometry oscillator topology that allows the implementation of slab inductors for high frequency integrated applications is presented in Chapter 4. Slab inductors present an attractive alternative for monolitic applications where low impedance and high quality factor integrated inductors are required. A general methodology to ensure the proper oscillation mode when several oscillator cores are coupled in a circular-geometry is also introduced. Several circular-geometry CMOS integrated oscillator prototypes are presented as a proof of concept and their performance is compared to previously published high frequency oscillators achieving some of the best figures of merit.

An overview of the existing methods for generating on-chip in-phase and quadrature (IQ) signals is presented in Chapter 5 with an emphasis on coupled oscillators. The trade-off between the phase noise performance and the quadrature and in-phase signal accuracy will be investigated and a general design methodology is devised to optimally couple quadrature oscillators. A CMOS oscillator prototype optimized using this methodology is fabricated and its phase noise enhancement is verified experimentally.

Capacitors are essential components in several analog integrated circuits as well as radio frequency (RF) building blocks. In many of these applications, the capacitor tolerance and matching properties play an essential role in determining their performance. In some other of these applications, capacitors with large values are needed. Often, off-chip capacitors are required as the integrated on-chip capacitor would consume a large die area. In Chapter 6, theoretical limits for the capacitance density of integrated capacitors with combined lateral and vertical field components are derived. These limits are used to investigate the efficiency of various capacitive structures such as lateral flux and quasi-fractal capacitors. This study leads to two new capacitor structures with superior matching properties and high lateral-field efficiencies. These new capacitors demonstrate larger capacities, superior matching properties, tighter tolerances, and higher self-resonance frequencies than the standard horizontal parallel plate and previously reported lateral-field capacitors, while maintaining comparable quality factors. These superior qualities are verified by simulation and experimental results.

Integrated phase-locked-loops will be presented in Chapter 7. First, the implementation of a triple-frequency output PLL will be presented. A frequency planning scheme that allows the generation of three local oscillator signals using only one PLL will be discussed. These three local oscillator signals are required for simultaneous downconversion to base band in a dual-band CMOS concurrent receiver [9]. Then, the design challenges in the design of an ultra-low-power PLL prototype implemented in a sub-micron CMOS processes will be addressed. Finally, a phase-compensation technique

will be introduced that attenuates the fractional spur in an integrated fractional-N PLL for low-power integrated applications.

A summary of the results presented in this dissertation as well as suggestions for future work are offered in Chapter 8.

Chapter

2

Frequency Generation Fundamentals

An indispensable building block required for both the receive and transmit path in modern communications systems is the phase-locked-loop (PLL). PLLs can be used to maintain a well-defined phase and frequency relation between two signal sources. Therefore, they can provide a stable local oscillator output required for frequency translation, modulation, and demodulation. Due to their remarkable versatility, PLLs are usually preferred over other methods of maintaining phase lock, as will be discussed shortly.

Local oscillator's short-term instabilities directly affect the quality and reliability of the information being transferred. It is therefore important to review some of the underlying properties of the local oscillator noise and their effect in the transmit and receive path.

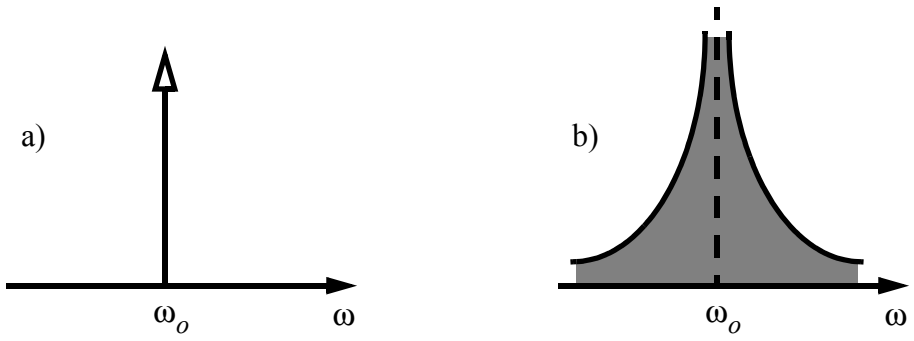


Figure 2.1: Oscillator output spectrums, a) ideal, b) typical.

Local oscillators are susceptible to noise injected either by its constituting devices or by external sources. These noise sources would influence both the frequency or phase and amplitude of the output. Ideally, the output of the local oscillator can be expressed as:

$$V_{out}(t) = V_o \cdot \cos(\omega_o t + \phi_o) \tag{2.1}$$

where the amplitude V_o, frequency ω_o and phase ϕ_o are all constants. The one-sided spectrum of this ideal oscillator consists of an impulse at frequency ω_o, as depicted in Figure 2.1a. However, due to the abovementioned random fluctuations, the output of a real oscillator can be more generally expressed as:

$$V_{out}(t) = V_o \cdot [1 + A(t)] \cdot f[\omega_o t + \phi(t)] \tag{2.2}$$

where $A(t)$ and $\phi(t)$ are both functions of time and f represents the periodic waveform of the steady-state output of the oscillator. If $f(t)$ is not a pure sinusoid, the oscillator spectrum has components around the harmonics of ω_o. What is more, due to the fluctuations represented by $A(t)$ and $\phi(t)$, the spectrum of the oscillator has side bands close to the frequency of oscillation ω_o, as shown in Figure 2.1b. These skirts in the spectrum are generally referred to as phase noise side bands. To help us understand the importance of phase noise, consider a generic RF transceiver shown in Figure 2.2. It consists of a low noise amplifier (LNA), power amplifier (PA), filters, mixers, and a frequency synthesizer that provides the carrier signal (local oscillator) for both the receiver and transmit paths.

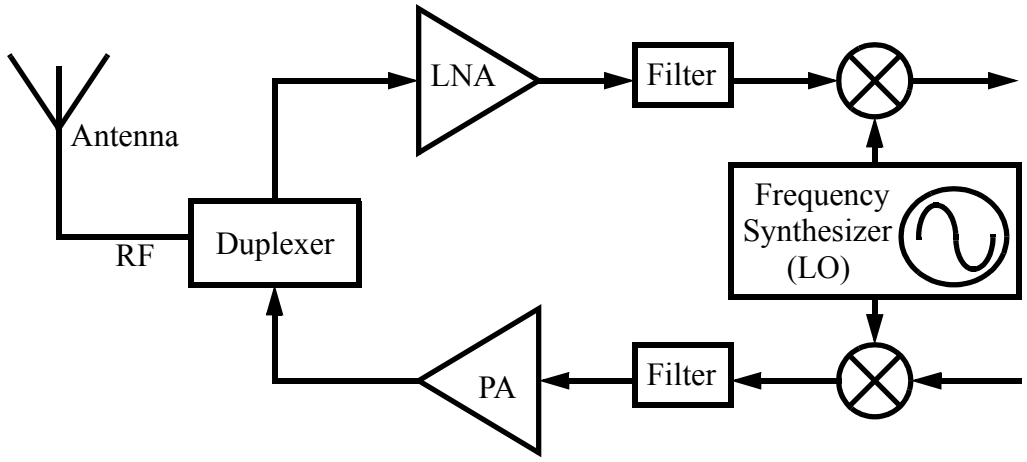


Figure 2.2: Simplified model of a generic transceiver.

If the local oscillator output has a large phase noise, the up- and down-converted signals are corrupted. Suppose the signal of interest is to be received in the presence of a strong interferer in the form of an adjacent channel. Consequently, some downconversion of these two signals will occur in the receive path. The resulting spectra will consist of two overlapping signals, as depicted in Figure 2.3. As can be seen, the desired signal can get

buried under the interferer which can significantly degrade the dynamic range of the receiver.

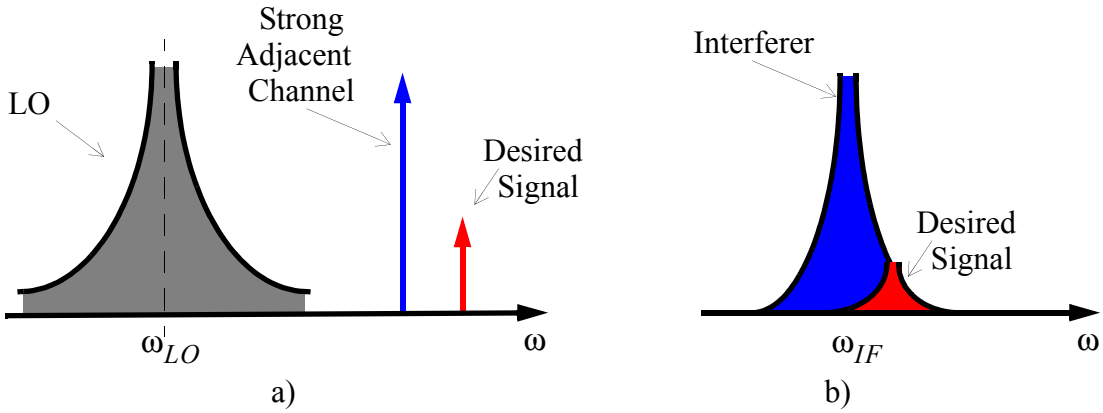


Figure 2.3: Downconversion by a noisy oscillator, a) RF spectrum, b) IF spectrum.

As for the transmit path, the phase noise will generate interference around the local oscillator output frequency, corrupting the neighboring channels, as depicted in Figure 2.4. Therefore, improving the phase noise of the local oscillator improves the performance of both receiver and transmitter.

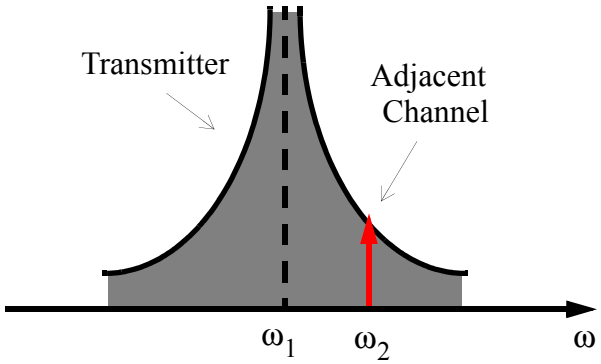


Figure 2.4: Effect of phase noise in transmitters.

In this chapter, we will start with a brief overview of the traditional frequency generation techniques. Then, the basics of the coherent indirect frequency synthesis will be covered. Finally, we will review the spectral purity of phase-locked-loops (PLLs) and voltage controlled oscillators.

2.1 Frequency Synthesis Techniques

The term *frequency synthesis* was first introduced by Finden in 1943 [11]. The first generation of frequency synthesizers used an incoherent method. In this approach, the frequencies were synthesized by manually switching and mixing several crystal oscillators and filters [12], as shown in Figure 2.5.

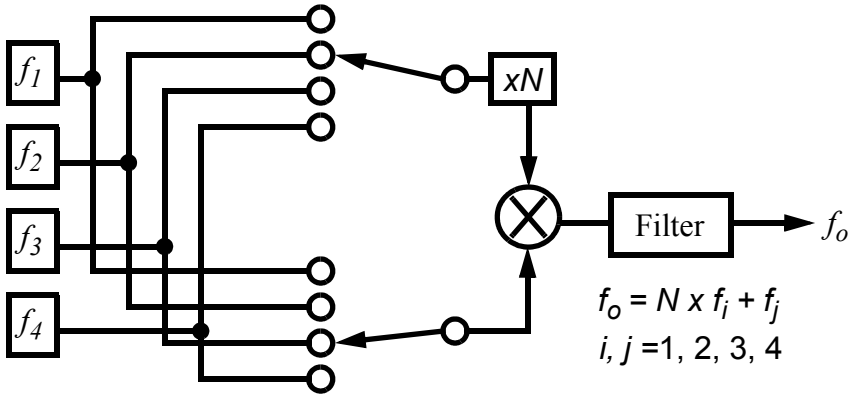


Figure 2.5: Incoherent frequency synthesis method.

The ever increasing need for frequency generation schemes with higher accuracy, stability, and versatility than the incoherent method have resulted in three options for frequency synthesis in todays communication systems, namely, table-look-up, coherent and indirect frequency synthesis (phase-lock) [12].

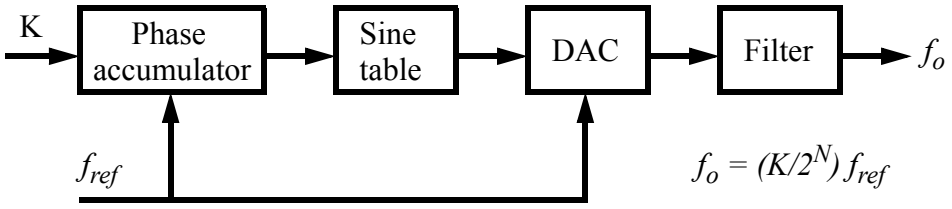


Figure 2.6: Direct digital synthesis.

In a digital synthesizer (table-look-up), the output sinusoid is generated using the digital values of the waveform stored in a memory, as depicted in Figure 2.6. The signal is generated in the form of a series of digital numbers with clock frequency f_{ref} and a

digital-to-analog converter (DAC) is required to process the data from the memory containing the sine or cosine values. These values are set by the accumulator and 2^N clock cycles are required for completion of one full cycle. Thus, corresponding to an output frequency of $f_{ref}/2^N$ with an N-bit accumulator. Here, the accumulator capacity determines the frequency resolution. A low pass filter is usually required to remove the high-frequency spurs generated by this digital process. The table-look-up method features fine frequency resolution, very fast settling time, and low harmonic and spur content. However, it suffers from the limited speed of the memory and the resolution and speed of the digital-to-analog converter. Also, the output frequency is always lower than half the reference frequency based on the Nyquist criterion. All these issues limit their use to few hundreds of megahertz for fully integrated applications [13]-[15]. Hence, high frequency of operation is not feasible.

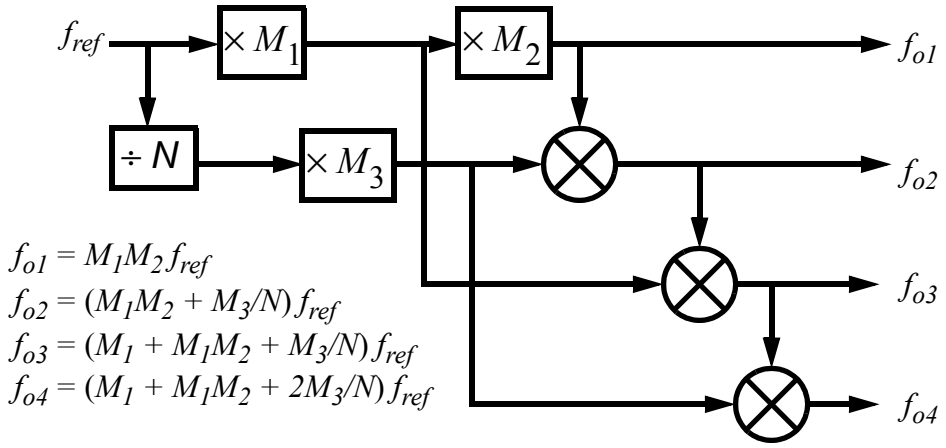


Figure 2.7: Coherent frequency synthesis method.

The coherent frequency synthesis method shown in Figure 2.7 has also been used in the past. In this approach, various output frequencies are generated with the combination of frequency multipliers, dividers, and mixers. Thus, high frequency accuracy is attainable. Ideally, the stability and accuracy of the output frequencies are the same as those of the reference signal. However, undesired sidebands and high cross-talk between stages are a serious problem for practical monolitic implementations that directly impact the spectral purity of the output. Another disadvantages are the stringent filtering

requirements and the large number of blocks and components, which causes the direct synthesizer to be bulky and power hungry. These drawbacks limit its practical use for integrated applications.

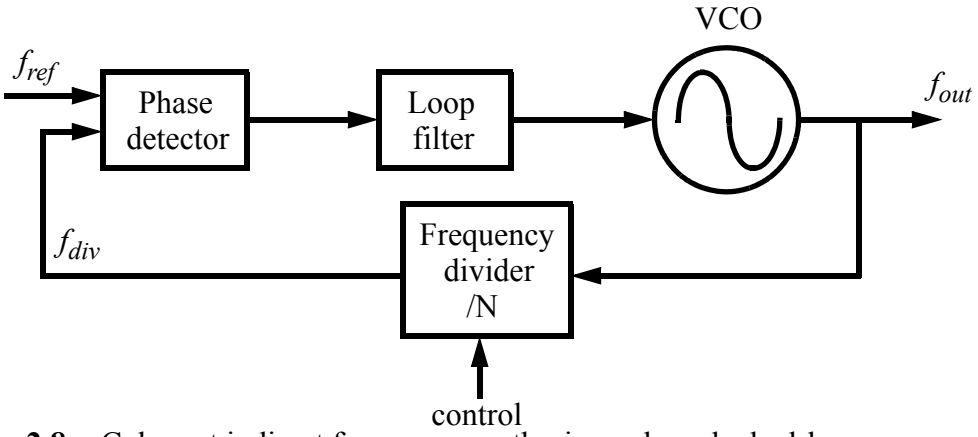


Figure 2.8: Coherent indirect frequency synthesis or phase-locked-loop.

Modern frequency synthesizers for portable applications use an indirect method known as a phase-lock technique shown schematically in Figure 2.8. This coherent indirect frequency synthesis generates the output by phase-locking the divided output to a reference signal and has the potential of combining high frequency and low power and is well suited for integration in low-cost CMOS processes.

2.2 Coherent Indirect or Phase-Locked-Loop Frequency Synthesis

Monolitic PLLs have been widely used in wired and wireless communications, as well as digital and control systems. Their applications span from frequency synthesis, modulation and demodulation of signals, data and signal recovery, and clock generation and distribution among others. The first description of a phase-locked-loop was provided by H. de Bellescize in 1932 [16]. In this work, an architecture consisting of an oscillator, mixer and amplifier was proposed for demodulating and receiving AM signals. The local oscillator was required to be tuned at exactly the same frequency as that of the incoming

carrier. Thus, it was essential for the local oscillator to be in phase with the carrier for maximum output. In other words, this local oscillator had to be phase-locked by a phase-locked-loop. Some other early applications that use PLLs include synchronization of the image and color bursts for TVs, and tuning of stations in FM radios.

2.2.1 Phase-Locked-Loop Basics

In this section, a brief overview of some of the basic properties of PLLs is offered. A general PLL consists of four basic components, namely the phase detector (PD), loop filter with transfer function $G_{lf}(s)$, voltage controlled oscillator (VCO) and an optional frequency divider, as depicted in Figure 2.8. In this scheme, the output frequency of the VCO is divided by N in the frequency divider block. The divided signal phase is then compared in the phase detector block to that of the reference. This reference signal is usually generated by an external source which has a high signal-to-noise ratio and is very clean and stable. Under the locked condition, the negative feedback adjusts the control voltage of the VCO in such a way that the reference and the divided signal have a constant phase difference. Therefore, these two signals have the same frequencies.

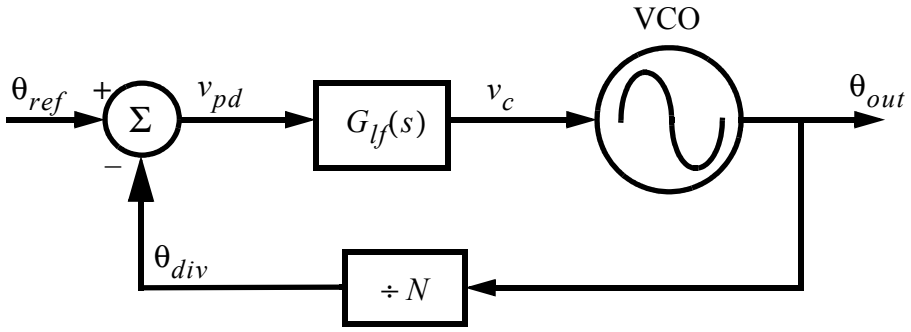


Figure 2.9: Phase-locked-loop state variable diagram.

When the phase relationship between f_{ref} and f_{div} is constant, the PLL is in lock and the output frequency equals the divided frequency, *i.e.,* $f_{div} = f_{ref}$ or,

$$f_{out} = N \cdot f_{ref} \tag{2.3}$$

Even though the phase-locked-loop is a non-linear system, it can be modeled quite accurately as a linear time-invariant system when in lock [17]-[21]. This is mainly because the phase detector transfer characteristic is linear in phase domain under lock. A simple way to analyze this system is by using the phases of the reference and the output of the VCO signals as loop variables, as shown in Figure 2.9.

The input signal and the output of the PLL have phases $\theta_{ref}(t)$ and $\theta_{out}(t)$, respectively. The divider block divides the VCO frequency by a factor *N*, therefore, it also divides its phase by the same factor:

$$\theta_{div}(t) = \frac{\theta_{out}(t)}{N} \tag{2.4}$$

When the loop is locked, or close to be locked, the phase detector output voltage is proportional to the phase difference between its inputs, *i.e.,*

$$v_{pd}(t) = K_{pd} \cdot [\theta_{ref}(t) - \theta_{div}(t)] \tag{2.5}$$

where K_{pd} is the phase detector gain and has units of [*V/rad*]. This phase difference or error, v_{pd}, is filtered by the low-pass transfer function of the loop filter $G_{lf}(s)$, which attenuates noise and high frequency components. $G_{lf}(s)$ has an important effect on the noise characteristics of the loop as will be discussed shortly.

The output frequency of the VCO is proportional to its control voltage, v_c. Since the phase is the integral of the frequency, the VCO acts as an ideal integrator for the input voltage v_c. The output phase can then be found by integrating the VCO output frequency, *i.e.*,

$$\theta_{out}(t) = \int^{t} K_{vco} \cdot v_c(t) \cdot dt \tag{2.6}$$

where K_{vco} is the VCO gain factor with units [*rad/V s*]. By applying the Laplace transform to (2.6), we obtain:

$$\theta_{out}(s) = \frac{K_{vco} \cdot V_c(s)}{s} \tag{2.7}$$

The phase domain equivalent system of the PLL depicted in Figure 2.9 can be viewed as a standard feedback system with a forward transfer function $G(s) = K_{pd} \cdot G_{lf}(s) \cdot K_{VCO}/s$ and a feedback gain, $H(s) = 1/N$. The phase domain transfer function of this PLL is then:

$$\frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{G(s)}{G(s) \cdot H(s) + 1} = \frac{N \cdot K_{pd} \cdot K_{VCO} \cdot G_{lf}(s)}{K_{pd} \cdot K_{VCO} \cdot G_{lf}(s) + N \cdot s} \tag{2.8}$$

2.3 Phase-Locked-Loop Spectral Purity

Although there are several ways to quantify the frequency instabilities of a local oscillator, we will focus on the most common measure for their spectral purity, namely phase noise. The single sideband noise spectral density is defined as,

$$L\{\Delta\omega\} = 10 \cdot \log_{10}\left(\frac{P_{sideband}(\omega_o + \Delta\omega, 1Hz)}{P_{carrier}}\right) \tag{2.9}$$

where $P_{sideband}(\omega_o + \Delta\omega, 1Hz)$ is the noise power in the band at an offset frequency $\Delta\omega$ from the carrier, per unit bandwidth, as depicted in Figure 2.10

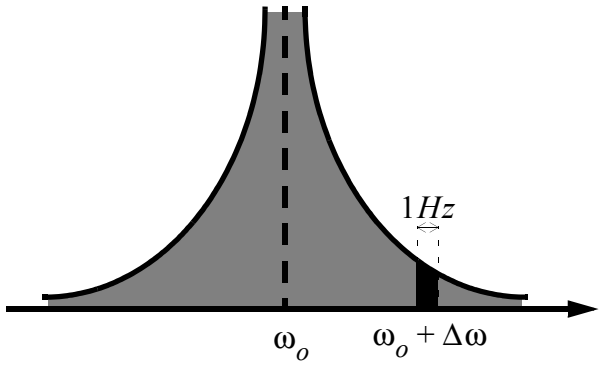


Figure 2.10: Frequency representation of oscillator phase noise.

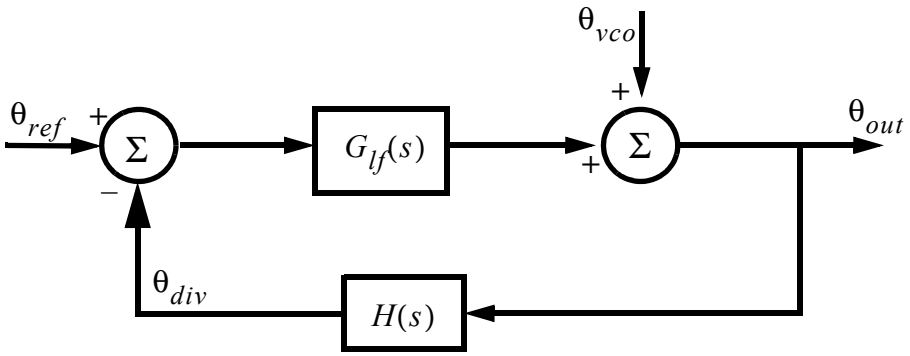


Figure 2.11: Phase-locked-loop feedback system.

The noise in the phase-locked-loop of Figure 2.9 is mainly determined by two factors, the noise generated in the VCO, $\theta_{vco}(s)$, and the noise from the reference signal, $\theta_{ref}(s)$. Modelling the VCO noise as an additive noise, as shown in Figure 2.11, the closed loop response to $\theta_{vco}(s)$ is as follows,

$$\frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{1}{G(s)\cdot H(s)+1} = \frac{N\cdot s}{N\cdot s + K_{pd}\cdot K_{vco}\cdot G_{lf}(s)} \tag{2.10}$$

On the other hand, the closed-loop response to $\theta_{ref}(s)$ is,

$$\frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{G(s)}{G(s)\cdot H(s)+1} = \frac{N\cdot K_{pd}\cdot G_{lf}(s)\cdot K_{vco}}{N\cdot s + K_{pd}\cdot G_{lf}(s)\cdot K_{vco}} \tag{2.11}$$

To obtain some insight on how both noise contributions are transferred to the output, let us consider the most elementary loop filter with a constant transfer function, *i.e.*, $G_{lf}(s) = K_{lf}$. Equations (2.10) and (2.11) can be calculated for a constant loop filter as follows:

$$\frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{1}{\frac{K_{pd}\cdot K_{lf}\cdot K_{vco}}{N\cdot s}+1} = \frac{s}{s+\omega_c} \tag{2.12}$$

$$\frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{\frac{K_{pd} \cdot K_{lf} \cdot K_{vco}}{N}}{\frac{K_{pd} \cdot K_{lf} \cdot K_{vco}}{N \cdot s} + 1} = N\frac{\omega_c}{s + \omega_c} \tag{2.13}$$

In these equations, ω_c can be defined as the cross-over frequency of the PLL where the open loop gain has a magnitude equal to one, *i.e.,*

$$\omega_c = \frac{K_{pd} \cdot K_{lf} \cdot K_{vco}}{N} \tag{2.14}$$

Two important observations can be made from equations (2.12) and (2.13). The noise transfer function from the VCO to the output has a high-pass characteristic. This is because the feedback action of the loop is too weak to suppress high frequency noise components. At lower frequencies, the loop feedback becomes stronger, successfully suppressing the low frequency VCO noise components. On the other hand, the noise from the reference has a low-pass characteristic with the same cross-over frequency ω_c. However, within the PLL bandwidth, this noise is amplified by N (the division factor). ω_c is the 3-*dB* frequency for these actions.

The output noise power spectral density of an integrated oscillator demonstrates three regions with slopes of $1/\omega^3$, $1/\omega^2$ and a flat region, as shown in Figure 2.12a with a dashed line [22]. At high frequencies, a flat noise floor is observed. From this point, the phase noise increases quadratically with offset frequencies closer to the carrier. This noise originates from the white active device noise upconverted around the carrier and harmonics. And finally, closest to the carrier, the $1/f$ noise upconversion shapes the $1/\omega^3$ region. The power spectral density of the output of the PLL is also shown in

Figure 2.12a with a solid line. For frequencies beyond ω_c, the noise of the voltage controlled oscillator dominates the shape of the PLL output noise.

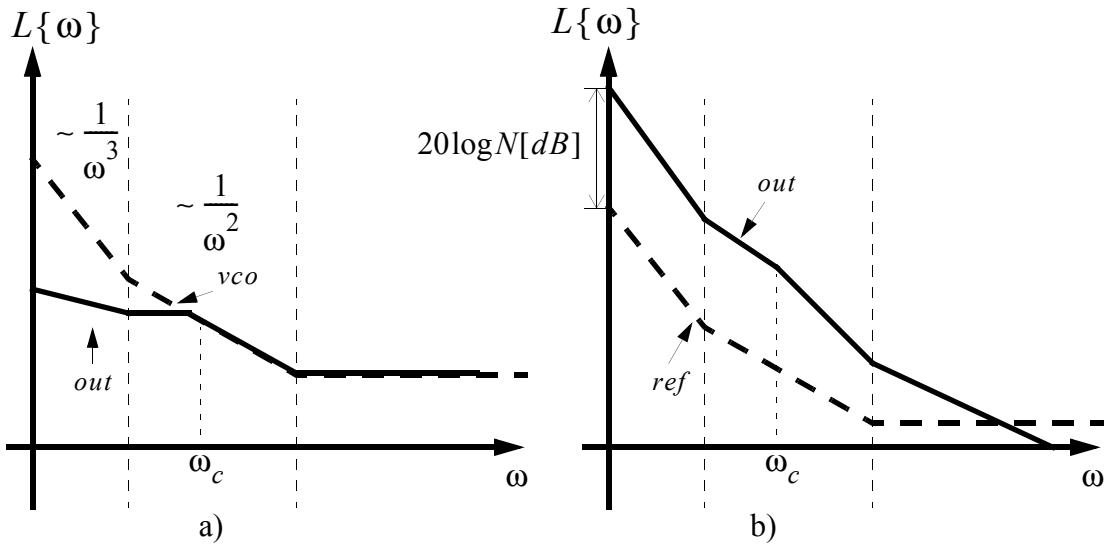


Figure 2.12: Phase-locked-loop phase noise transfer characteristics, a) VCO noise, b) reference noise

Typically, the reference noise also exhibits the same curve as that of the VCO noise with three distinctive regions as depicted in Figure 2.12b with a dashed line. The resulting noise power spectral density of the PLL output is also depicted in Figure 2.12b with a solid line. For frequencies below ω_c, the noise of the reference signal is amplified by N and dominates the shape of output noise.

The noise from the other PLL building blocks will also be low-passed to the output with a transfer function dependent in their respective position in the loop. However, these building blocks can be designed in such a way to minimize their noise contributions [19][21].

In this context, it is desirable to use as large a cross-over frequency, ω_c, as possible in the design of a PLL to suppress the VCO close-in phase noise. In practice, however, ω_c has to be smaller than the reference frequency to provide enough stability to the loop [18]-[21]. The cut off frequency is often chosen to be at least 10 to 20 times smaller than the reference frequency for loop stability, *i.e.,*

$$\omega_c \leq \frac{2\pi}{10 \cdot f_{ref}} \tag{2.15}$$

For typical mobile applications, the input reference signal is generated by crystal resonators that show very stable and high-quality output signals. However, crystal resonators with frequencies in excess of 20MHz are very hard to find and usually are more expensive [23]. The availability of crystal resonator with frequencies below 20MHz and (2.15) pose a practical upper limit of ω_c to about $2\pi \times 10^6 \left[\frac{rad}{sec}\right]$.

Although the developments in this section were derived for a simple loop filter with a constant transfer function, they can be generalized for a first-order or second-order low-pass loop filter as well [17].

2.4 Oscillator Phase Noise

In an oscillator, the total single-sideband phase noise in the $1/f^2$ region of the spectrum is given by [22]:

$$L\{\Delta\omega\} = \frac{\overline{i_n^2}/\Delta f}{2q_{max}^2} \cdot \frac{\Gamma_{eff,\,rms}^2}{\Delta\omega^2} \tag{2.16}$$

where $\Delta\omega$ is the offset frequency from the carrier, $\overline{i_n^2}/\Delta f$ is the power spectral density of the current noise source in question, $\Gamma_{eff,\,rms}$ is the root-mean-square value of the *effective impulse sensitivity function* (ISF) associated with that noise source, and q_{max} is the maximum charge swing across the current noise source. The effective ISF is the product of the ISF and the *noise modulating function* (NMF), as defined in [22], *i.e.,*

$$\Gamma_{eff}(\omega t) = \Gamma(\omega t) \cdot \alpha(\omega t) \tag{2.17}$$

where the ISF, denoted as $\Gamma(\omega t)$, represents the time varying sensitivity of the oscillator's phase to perturbations and the NMF, shown as $\alpha(\omega t)$, describes the modulation of the noise power spectrum with time for the noise source in question.

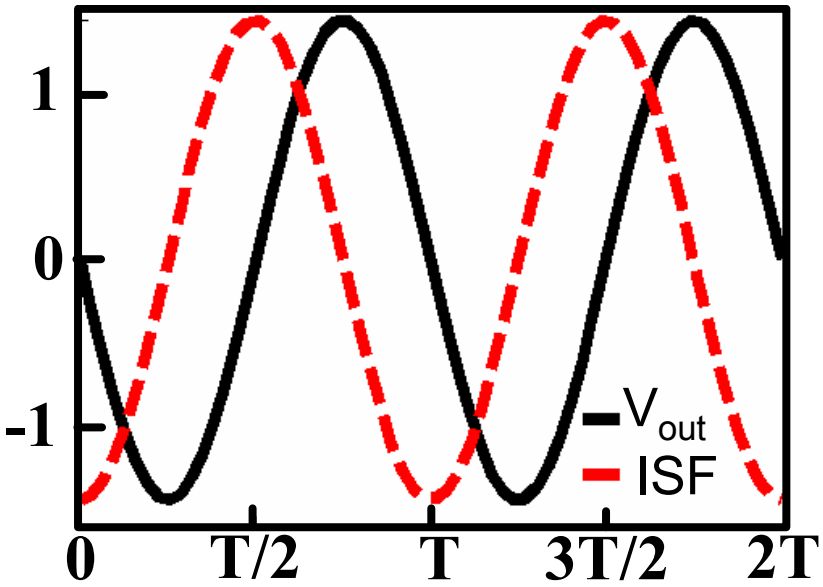


Figure 2.13: ISF and output voltage waveforms of a typical LC oscillator.

As an example, Figure 2.13 shows the ISF with a dashed red line together with the output voltage waveform with a solid black line, of a typical *LC* oscillator. As can be seen, there are regions on the oscillation cycle where the oscillator is more sensitive and less sensitive to perturbations

In practice, an active device creates an energy restoring mechanism to compensate for the losses of the tank and thus sustain the oscillation. This device acts as a means to transfer the energy from the dc power supply to the resonant tank. Unfortunately, during this energy transfer process, the active device also injects noise into the tank, which in turn becomes phase noise.

As another example, Figure 2.14 shows the drain current and a sample of the channel noise in a MOS transistor.

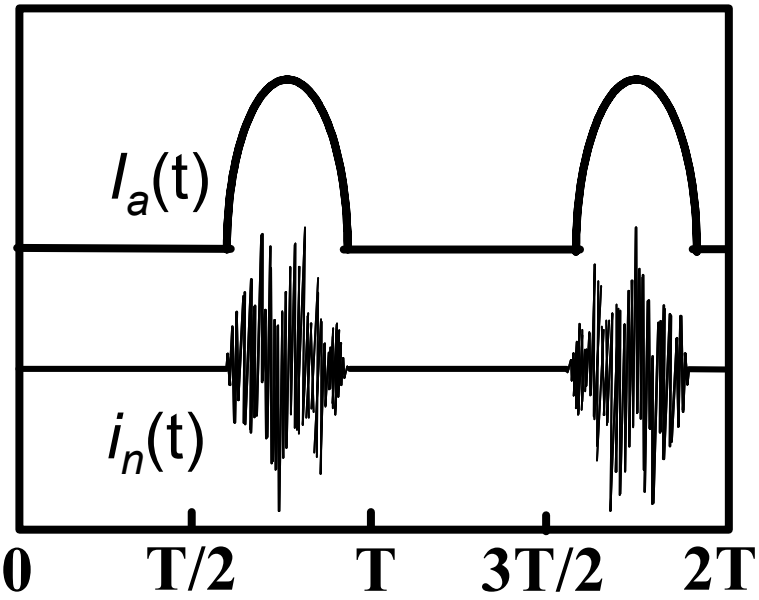


Figure 2.14: Drain current and a sample of the channel noise in a MOS transistor.

These two effects combined are captured by the effective ISF, which is the product of the ISF and the NMF. The NMF describes the noise amplitude modulation of the active sources, which are the dominant factor in degrading the oscillator's phase noise [22][24]. The relative timing of the cyclostationary noise sources with respect to the ISF can drastically change the effect of these noise sources; therefore, it is highly desirable for the cyclostationary noise sources to have their maximum power at the minimum sensitivity point. In essence, (2.16) states quantitatively the way the phase noise is affected by these processes.

As previously discussed, active device noise (and not the resonator noise) dominates the phase noise of most CMOS oscillators. In a properly designed oscillator, the quality factor, Q, of the resonant tank plays a central role in the phase noise, *indirectly*. The best

phase-noise-power trade-off is usually achieved at the borderline between the current and voltage limited regimes [24][25]. These two regions are depicted in Figure 2.15.

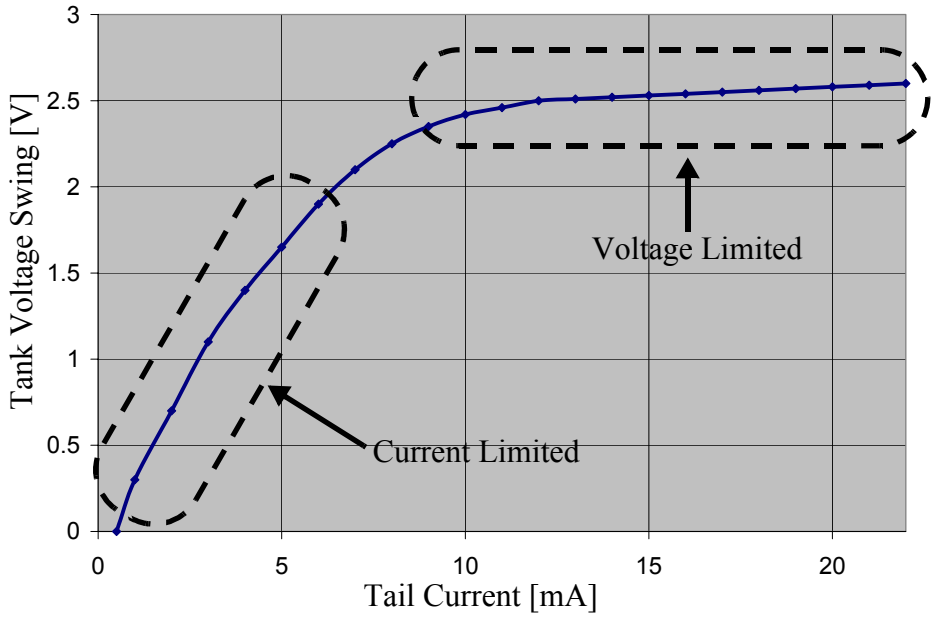


Figure 2.15: Oscillator tank voltage vs. bias current of a typical LC oscillator.

For sufficiently large bias currents, the oscillator tank voltage starts to clip due to the inability to grow beyond the supply voltage, and thus the tank amplitude reaches a plateau. On the other hand, the tank amplitude is proportional to $I_{bias} \cdot R_{tank}$ at the current limited regime (and also at the edge of the voltage-limited regime), where I_{bias} is the oscillator dc bias current and R_{tank} is the equivalent tank parallel resistance [25]. A higher tank Q translates to a larger effective tank parallel resistance, R_{tank}. This, in turn, allows the designer to lower the oscillator's bias current, I_{bias}, while maintaining the full voltage swing necessary for operation at the edge of the voltage-limited regime. The lower bias current decreases the noise from the active devices, which is the dominant contributor to phase noise. This explains the well-established fact that higher tank quality factor can be used to improve oscillator phase noise.

2.5 Challenges in Integrated Oscillator Design

There are several issues in the design of local oscillators in CMOS technologies. Firstly, the transistor devices readily available in these process technologies generate more active device noise due to short channel and hot electron effects [9], hence suffering from a worse phase noise performance than oscillator modules fabricated using discrete components. Moreover, the *1/f* noise corner in these devices is quite high, on the order of hundreds of kilohertz to several megahertz for sub-micron silicon technologies, posing another challenge for low noise oscillator design due to the up-conversion of this noise to close-in phase noise around the carrier. Secondly, as the driving force in CMOS technologies are digital applications, these technologies are not optimized for analog or RF applications. Furthermore, to avoid latch up of the digital circuits, the silicon substrate is fairly conductive and increases the signal loss because of the energy coupled (both, inductively and capacitivelly) into the lossy substrate. Therefore, the quality factors of the passive components available are quite low. Integrated capacitors present low capacitance densities and large bottom plate capacitances that would degrade their RF performance and worsen their effective loss. In addition, on-chip inductors suffer from high ohmic losses from the thin metal layers available in CMOS technologies. This is exacerbated by the skin effect, which causes a non-uniform current distribution in a conductor at high frequencies. The consequence is a reduction in the effective inductor cross-section, decreasing the metal conductance and hence, increasing the loss. What is more, due to the proximity to the substrate, there will be energy coupled in to the substrate degrading the inductor quality factor significantly.

2.6 Summary

Local oscillators are an essential building block in modern communications systems. The close-in phase noise in a phase-locked-loop is determined by the reference signal,

however, the far-out phase noise is determined by the spectral purity of the voltage controlled oscillator and ultimately impacts the performance for such communication systems. There are several challenges in oscillator design towards their integration in silicon technologies, namely active device noise generation and low quality passives. We will propose new architectures and topologies to overcome such issues in the following chapters of this dissertation.

Chapter 3

A Noise Shifting Colpitts VCO

Integrated voltage controlled oscillators (VCOs) are essential building elements of all kinds of communication systems in general, and in particular, for the implementation of a single chip radio in today's communication systems. The ever-growing demand for higher numbers of channels keeps imposing tighter phase noise performance specifications for local oscillators.

Recently, many different approaches have been used to improve the performance of integrated *LC* VCOs [24]-[49]. Cross-coupled oscillators have been preferred over other topologies due to their ease of implementation, relaxed start-up condition, and differential operation. However, in cross-coupled oscillators the noise generation by the active devices occurs when the oscillator is quite sensitive to perturbations [22] degrading the phase noise considerably. On the other hand, the Colpitts oscillator [31][40] has superior cyclostationary noise properties and can hence potentially achieve lower phase noise [50]. Despite these advantages, single-ended Colpitts oscillators are rarely used in today's integrated circuits due to their higher required gain for reliable start-up and single-ended nature that makes them more sensitive to parameter variations and common-mode noise sources, such as substrate and supply noise.

This chapter presents a new oscillator that overcomes these issues. This topology improves the phase noise performance by cyclostationary noise alignment while providing a fully differential output and a large loop gain for reliable start-up.

3.1 Oscillator Topology Comparison

In this section, several oscillator topologies will be compared with an emphasis on their cyclostationary noise properties and energy transfer efficiencies to obtain essential understanding of their effect on the oscillator's phase noise. This comparison is carried out in the context of the oscillator impulse sensitivity and noise modulating functions introduced in Section 2.4.

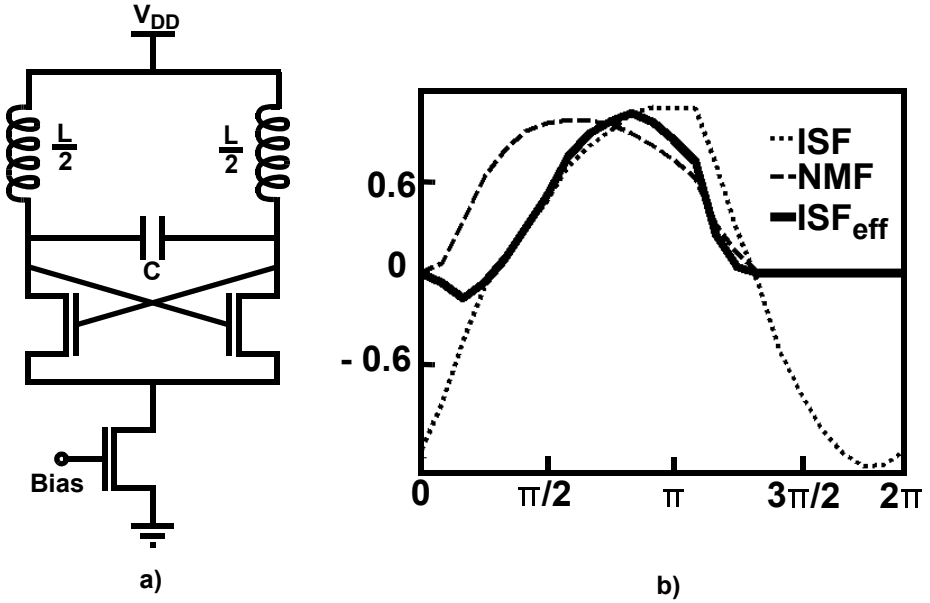


Figure 3.1: NMOS-only cross-coupled oscillator: a) Circuit schematic, b) ISF, NMF and effective ISF waveforms.

Figure 3.1a shows the NMOS-only cross-coupled oscillator topology, widely used in high-frequency integrated circuits due to the ease of implementation and differential operation. Figure 3.2a shows the complementary version using both NMOS and PMOS transistors. This topology provides a larger tank amplitude for a given tail current in the current limited regime [25]. Finally, Figure 3.3a depicts the single-ended Colpitts oscillator topology, which is a commonly used in single-ended design [31][51][52].

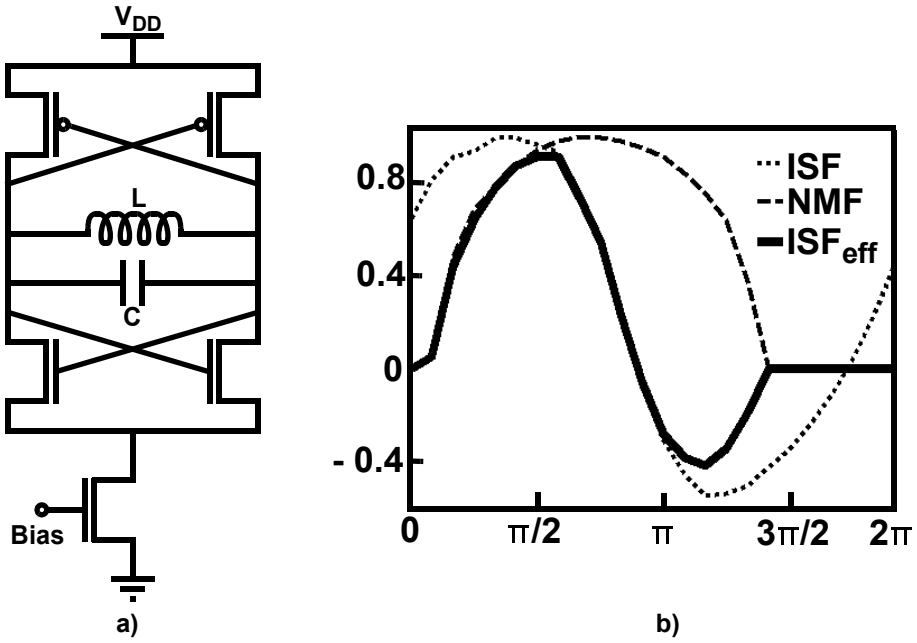


Figure 3.2: Complementary cross-coupled oscillator: a) Circuit schematic, b) ISF, NMF and effective ISF waveforms.

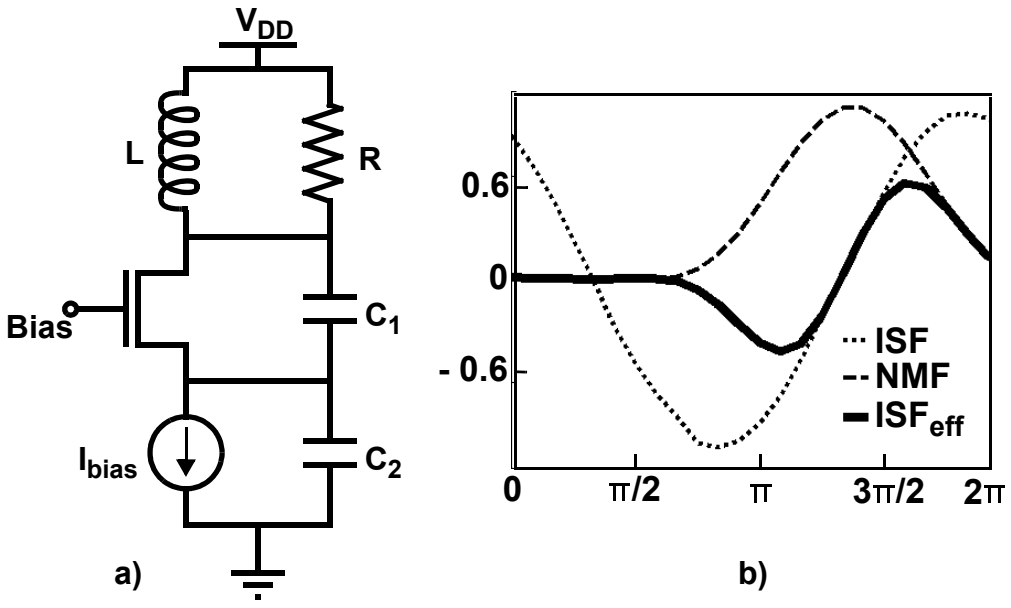


Figure 3.3: Single-ended Colpitts oscillator topology: a) Circuit schematic, b) ISF, NMF and effective ISF waveforms.

To simulate the ISF and NMF waveforms of the abovementioned oscillators, the *direct impulse response measurement* method of [22] is implemented in Spice [53]. In order to compare these oscillator topologies, these three oscillators are simulated using the same tank inductance and are tuned to oscillate at a center frequency of 1.8GHz, while maintaining a tuning range of at least 20%. The inductors have a quality factor of 5 at 1.8GHz. Finally, the oscillators draw the same bias current and operate in the current limited regime.

Figure 3.1b shows the simulated impulse sensitivity function, $\Gamma(\omega t)$, noise modulating function, $\alpha(\omega t)$, and the effective impulse sensitivity function, $\Gamma_{eff}(\omega t)$, of the NMOS transistor channel noise in the NMOS-only cross-coupled topology of Figure 3.1a. In this oscillator topology, the maximum noise generated by the active devices appears when the oscillator is quite sensitive to perturbations. This can be noticed in Figure 3.1b, where the maximums of the NMF and ISF almost overlap, resulting in a large effective ISF and thus worsening the phase noise for a given resonator quality factor and bias current.

Figure 3.2b shows the simulated waveforms for the PMOS transistors in the complementary cross-coupled oscillator of Figure 3.2a. The waveforms of the NMOS transistors are comparable and are omitted without loss of generality. Similar to the NMOS-only cross-coupled topology discussed previously, the noise generated by the active devices of the complementary cross-coupled oscillator of Figure 3.2a is maximum when the oscillator's phase is quite sensitive to perturbations. Moreover, in this topology the noise generated by both PMOS and NMOS transistors add to the overall active noise of the oscillator. Nevertheless, the complementary cross-coupled oscillator shows a better phase noise performance when compared to the NMOS- or PMOS-only cross-coupled oscillators for the same supply voltage and bias current when operating at the current limited regime, as demonstrated experimentally in [25]. This is mainly because the complementary cross-coupled oscillator of Figure 3.2a presents a larger maximum charge

swing, q_{max}, than that of the NMOS- or PMOS-only cross-coupled oscillators which overall enhances its phase noise performance, as will be discussed shortly. In these two oscillator topologies, each of the cross-coupled transistors operate fully switching over half of the oscillation period. Thus, in the ideal case, their noise modulating function would be a square wave. However, these transistors require some time to switch completely and hence, show noise modulating functions depicted in Figure 3.1b and Figure 3.2b. In other words, the noise generation in these cross-coupled oscillator topologies occurs over the entire oscillation cycle, worsening their phase noise performance for a given resonator quality factor and bias current.

Noise Source	Contribution
Drain current	87%
Inductor	6%
Tail Current	5%
Varactor	2%

Table 3.1: Phase noise contribution of each noise source.

It is instructive to compare the contributions of each of the noise sources to the total phase noise in the complementary cross-coupled topology of Figure 3.2a. Table 3.1 shows the simulated phase noise contributions of different noise sources at 600KHz offset from a 1.8GHz carrier of the cross-coupled oscillator depicted in Figure 3.2a. It can be clearly seen that most of the circuit noise is generated by the drain current noise of the cross-connected transistors, while the combined contributions of the other noise sources accounts for less than 13% of the total phase noise power. For example, if the noise injected by the tail device could be completely removed, the total phase noise would only show an improvement of 0.22 dB in this oscillator.

On the other hand, the single-ended Colpitts oscillator of Figure 3.3a has better cyclostationary noise properties, as exhibited in the simulated $\Gamma(\omega t)$, $\alpha(\omega t)$, and $\Gamma_{eff}(\omega t)$ waveforms depicted in Figure 3.3b. In this topology, the maximum noise

generation instant is aligned with the oscillator's minimum sensitivity point and can hence potentially achieve lower phase noise. Also, the Colpitts oscillator presents a smaller rms and dc value of its effective ISF than that of the NMOS- or PMOS-only and complementary cross-coupled oscillators of Figure 3.1a and Figure 3.2a, respectively. A more symmetrical effective ISF will significantly reduce the up-conversion of the low frequency noise of the transistor [22]. It is noteworthy that in the single-ended Colpitts oscillator of Figure 3.3a, the conduction angle of the main transistor is determined by the C_2/C_1 ratio, and thus it is highly desirable to minimize this conduction time. In practice, this conduction time has an optimum when this ratio is about 4 [54]. Fortunately, in this oscillator topology, the maximum of the core transistor current conduction (or the maximum of the noise power generation) occurs at the oscillator minimum sensitivity point.

As previously discussed, while the better cyclostationary properties of an oscillator alone would enhance the phase noise performance, a large oscillation charge swing results in an increase in the tank stored energy. The tank energy E_{tank} in an oscillator is given by $E_{tank} = CV_{tank}^2/2$, where V_{tank} is the tank voltage amplitude. Moreover, if the oscillator operates in the current limited regime, V_{tank} can be expressed in terms of the bias current I_{bias} and the effective parallel tank resistance R_{tank}, *i.e.*,

$$V_{tank} = \beta R_{tank} I_{bias} \tag{3.1}$$

where β is the oscillation amplitude constant. The *energy transfer efficiency,* η, which is defined as the ratio of the energy stored in the resonator's tank E_{tank} to the total dc energy P_{dc} dissipated in one period can be expressed as:

$$\begin{aligned}\eta &= \frac{E_{tank}}{P_{dc}T} \\ &= \frac{CV_{tank}^2 f_{osc}}{2V_{dc}I_{bias}} \\ &= \frac{Q_{tank}^2 \beta^2 I_{bias}}{4\pi V_{dc}} \cdot \sqrt{\frac{L}{C}}\end{aligned} \tag{3.2}$$

where $T = \frac{1}{f_{osc}} = 2\pi\sqrt{LC}$ is the oscillation period and V_{dc} is the supply voltage. Also, it is assumed that the quality factor of the tank is given by $Q = R_{tank}/2\pi f_{osc}L$.

Equation (3.2) shows the well-established fact that increasing the tank's quality factor will improve the energy transfer efficiency and enhance the phase noise of the oscillator. However, this energy transfer efficiency can also be increased if the oscillator has a larger oscillation amplitude for a given bias current (*i.e.,* larger β). To illustrate this, Table 3.2 compares the oscillation amplitude constant β for the NMOS- and PMOS-only, complementary cross-coupled and Colpitts VCOs of Figure 3.1a, Figure 3.2a, and Figure 3.3a, respectively.

Oscillator	**Amplitude**	**Oscillation amplitude constant, β**	**Energy transfer efficiency, η**
NMOS- or PMOS-only cross-coupled	$\frac{2}{\pi}R_{tank}I_{bias}$	$2/\pi$	$\frac{1}{\pi^2}\cdot\frac{Q_{tank}^2 I_{bias}\sqrt{L/C}}{\pi V_{dc}}$
Complementary cross-coupled	$\frac{4}{\pi}R_{tank}I_{bias}$	$4/\pi$	$\frac{4}{\pi^2}\cdot\frac{Q_{tank}^2 I_{bias}\sqrt{L/C}}{\pi V_{dc}}$
Single-ended Colpitts	$2R_{tank}I_{bias}$	2	$1\cdot\frac{Q_{tank}^2 I_{bias}\sqrt{L/C}}{\pi V_{dc}}$

Table 3.2: Oscillator comparison.

It can be easily seen that the Colpitts oscillator presents a higher output voltage swing and higher energy transfer efficiency than that of the NMOS- or PMOS-only and

complementary cross-coupled oscillators for a given bias current, which will further enhance its phase noise. It is also noteworthy that the efficiency is proportional only to the square-root of the L/C ratio. Interestingly, in the case of integrated spiral inductors, reducing the L results in a stronger improvement in the Q^2 term compared to the $\sqrt{L/C}$, as discussed in more details in [24].

Despite these advantages, single-ended Colpitts oscillators are rarely used in today integrated circuits, due to the higher required gain for reliable start-up and their single-ended nature that makes them more susceptible to common-mode noise sources such as substrate and supply noise. In the following section we will present a new topology that remedies these problems. Most of the discussed properties of the single-ended Colpitts oscillator of Figure 3.3a are applicable to the oscillator topology presented next.

3.2 Design Evolution

In this section, starting from the single-ended Colpitts oscillator of Figure 3.3a, we will show the design evolution that leads to a topology that overcomes the start-up issues while providing a low-noise fully-differential output.

A differential output can be provided by coupling two identical Colpitts oscillators and sharing their source-to-ground capacitors, C_2, as shown on Figure 3.4a. Since the center node where both C_2 capacitors are connected together is a differential virtual ground, the original operation of the oscillators remains unchanged when the two sides oscillate $180°$ out of phase. The differential operation will be guaranteed if the center node is left floating and is not grounded. To illustrate this effect, Figure 3.4b shows the simulated voltage and current waveforms of this topology.

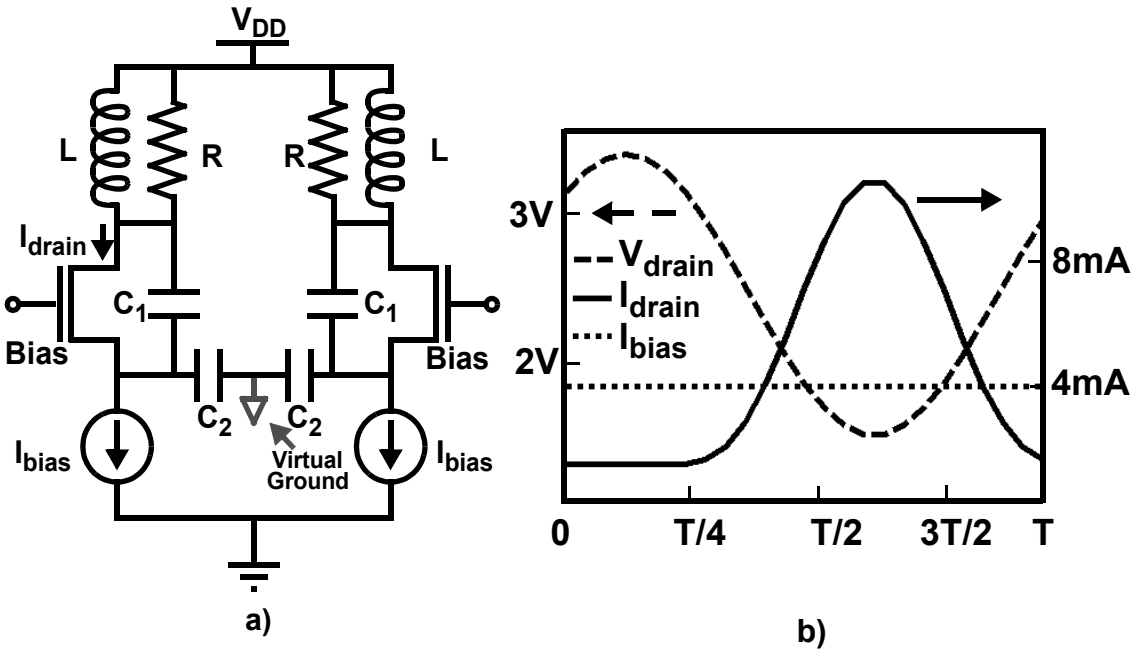


Figure 3.4: Differential Colpitts oscillator a) Circuit topology, b) Simulated voltage and current waveforms.

This differential topology is insensitive to any extra parasitic inductance and capacitance due to the metal lines and wire bonds used to provide the ground and supply voltage to the oscillator. On the other hand, this topology increases the power consumption by a factor of two, if the same start-up condition is to be met. Nevertheless, the power transfer efficiency remains constant, as the output voltage swing of this differential topology is twice that of the single-ended Colpitts oscillator of Figure 3.3a.

Noting that the current through the main transistor in each of the Colpitts oscillators of Figure 3.4a flows for less than half of the oscillation period, as shown in the simulated voltage and current waveforms of Figure 3.4b. It is, therefore, possible and favorable to replace the source-to-ground dc current source by the same dc current source and a timed switch which alternates the current between the two sides of the oscillator at the frequency of oscillation, as shown in Figure 3.5a.

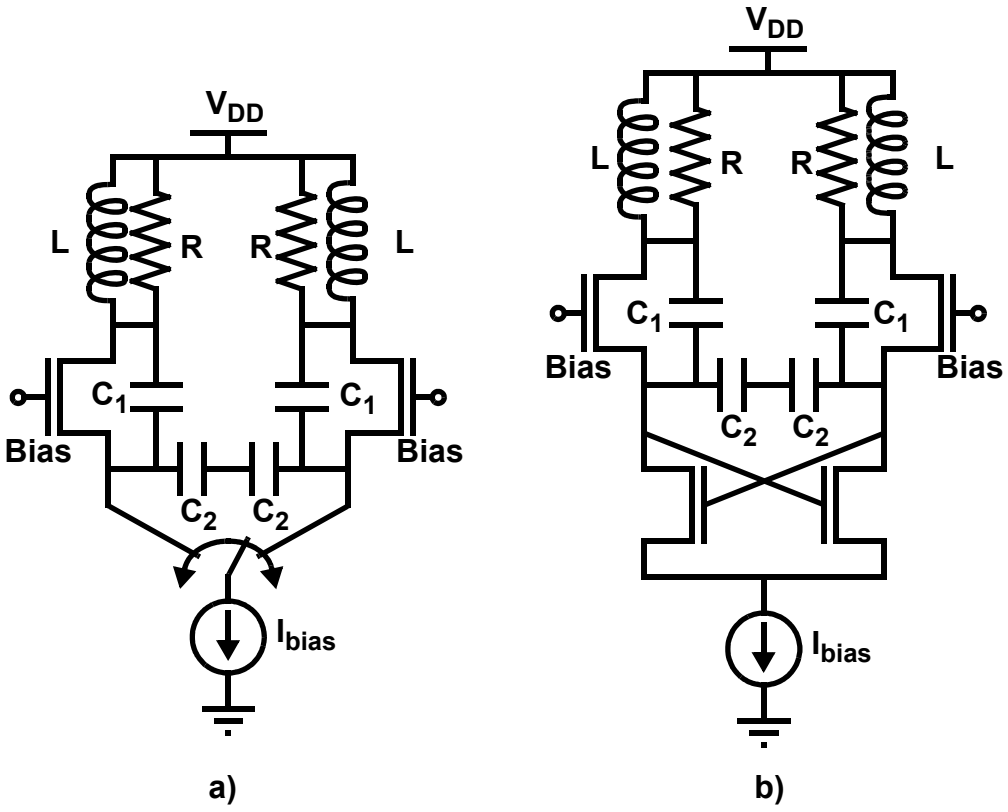


Figure 3.5: Current switching topology evolution a) Timed switch implementation b) NMOS transistors implementation.

The switching has to occur in a synchronized manner and can be achieved by using a pair of NMOS transistors to switch the current from one side to the other, as shown in Figure 3.5b. Moreover, the negative resistance of this tail cross-coupled pair provides a very effective means to enhance the small-signal loop gain, improving the start-up condition.

Finally, to add frequency tuning capabilities to the proposed oscillator topology, it is possible to include two varactors connected in parallel with the tank inductor. Also, the two shared C_2 capacitors connected in series can be replaced by an equivalent capacitor with half the value. The final oscillator topology is shown in Figure 3.6a and the simulated ISF, NMF, effective ISF and voltage waveforms for the core transistor are depicted in

Figure 3.6b. In this configuration, the transistor channel noise is maximum when the oscillator is the least sensitive to perturbations, reducing the effective ISF considerably. Therefore, this topology takes full advantage of the cyclostationary noise shaping of the core transistors. The NMOS cross-coupled transistors of Figure 3.6a operate mostly between ohmic and cut-off regions and hence have smaller noise contribution. Moreover, this noise contribution is attenuated by the capacitive voltage divider formed by C_1 and C_2. This voltage divider has the primarily function to provide a positive feedback path and enhance the small-signal loop gain of the oscillator.

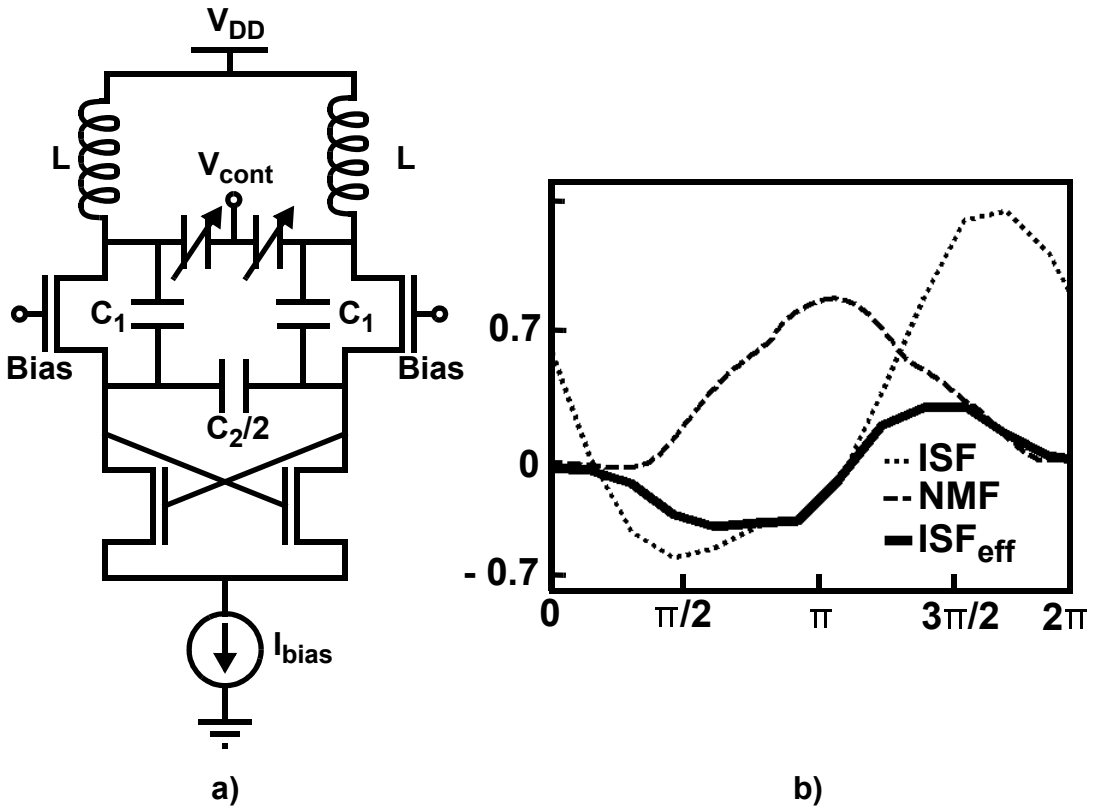


Figure 3.6: Noise shifting differential Colpitts VCO a) Final topology, b) ISF, NMF and effective ISF waveforms for the core transistor.

3.3 Design Example

In this section, we will discuss the design issues for the optimization and implementation of a test oscillator prototype in a CMOS process technology in order to evaluate the performance of the topology proposed in Section 3.2.

Subsection 3.3.1 describes the oscillator tank optimization procedures. In Subsection 3.3.2, we will analyze the oscillator topology in question and design constraints are imposed in terms of frequency tunability, start-up gain and minimum oscillation amplitude. The graphical method for the optimization for these constraints is explained in Subsection 3.3.3 together with the inductance selection strategy. Although a few parameters in this optimization are considered for a specific process technology, this methodology is generally applicable.

3.3.1 Inductor and Varactor Optimization

In typical silicon-based fully-integrated *LC* oscillators, spiral inductors are used, which have relatively low quality factors (Q~5) [55]. The inductance value of these inductors is dependent on the physical geometries of the spiral and the process technology of interest, while the loss mechanisms are the ohmic series resistance of the metal layer and the capacitive coupling to the conductive substrate. For this oscillator prototype the software package ASITIC was used, which is 2.5D field solver that calculates the second order coupling effects through Green functions [55]. This simulator was chosen due to the ability to simulate several square spiral inductors while varying their size and metal width in a time efficient manner, and thus, being able to find the structure with the highest Q (or lowest loss) achievable for a given inductance value.

The frequency of an *LC* oscillator can be tuned by using variable capacitors which are readily available in silicon technologies. Ideally, these varactors should simultaneously

offer a high quality factor, large capacitance variation, a control voltage range compatible with supply voltage, and uniform capacitance variation over the control voltage range.

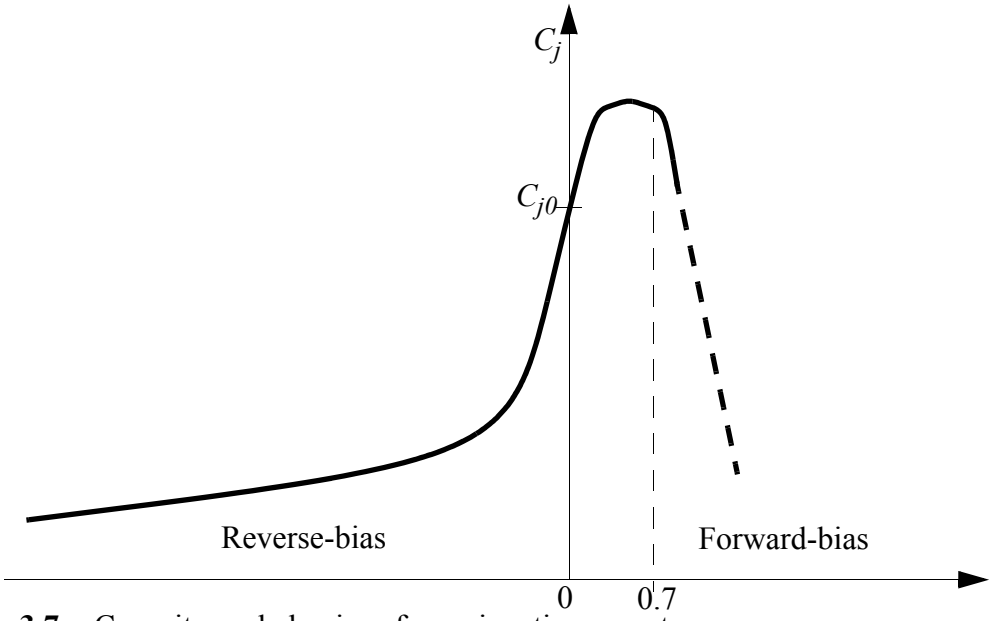


Figure 3.7: Capacitance behavior of a pn-junction varactor.

Varactor diodes, or varicaps, have been typically realized in standard bipolar process technology using reversed biased diodes and base-emitter junctions. Figure 3.7 shows a general characteristic of the capacitance variation vs. the bias voltage exhibited by a pn junction capacitor. The capacitance decreases gradually from C_{j0}, the zero-bias value, as the reverse bias increases. This is because the depletion region widens continuously until the junction avalanches due to the high junction electric field. On the other hand, the capacitance of a forward-biased junction increases, as the depletion region narrows while the external bias counteracts the junction built in potential. When the forward-bias approaches this built in potential, the depletion region collapses and the junction capacitance decreases drastically. This region of operation is not particularly useful, because forwarded-bias junctions conduct current. Even small forward bias voltages as low as 0.3V will create noticeable current conduction leading to additional loss. Therefore, these types of varactors are not well suited for our oscillator application.

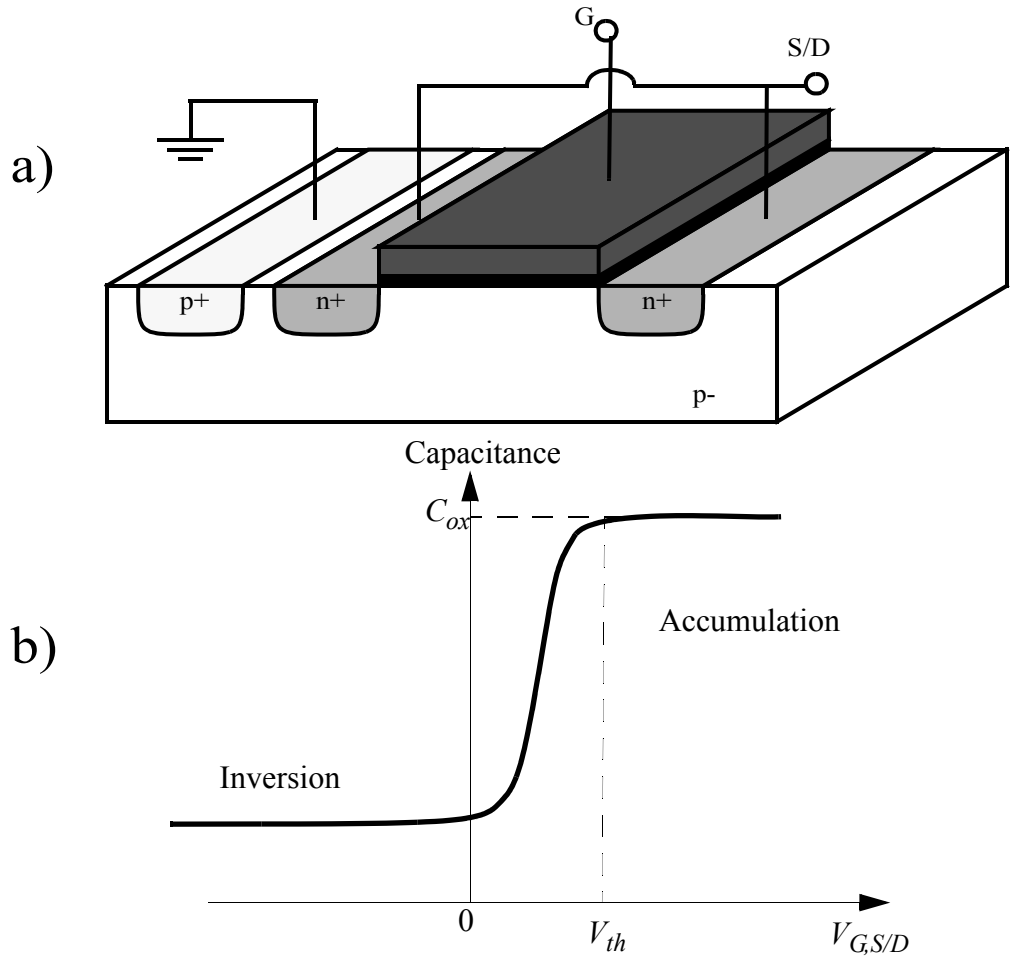


Figure 3.8: MOS varactor a) cross section of a NMOSCAP, b) capacitance behavior vs. $V_{G,S/D}$.

A MOS transistor with drain and source connected together can be used as a variable capacitor, or MOSCAP, with a capacitance value dependent on the voltage between the gate and the drain-source terminals. Figure 3.8a depicts a NMOS transistor configured as a MOSCAP while Figure 3.8b shows its capacitance curve. Electrons generated in the n+ region are accumulated beneath the gate when $V_{G,\,S/D} > V_{th}$. This region is called accumulation and the capacitance of the device in this region is equal to:

$$C_{ox} = \frac{\varepsilon_{ox} \cdot A_t}{t_{ox}} \tag{3.3}$$

where ε_{ox} is the permittivity of the oxide, A_t is the transistor channel area, and t_{ox} is the oxide thickness. As the $V_{G,S/D}$ voltage is decreased, the silicon surface beneath the gate is less accumulated becoming charge-free and eventually, the surface undergoes depletion. Therefore, the capacitance varies from a maximum to a minimum value as depicted in Figure 3.8b. Many efforts have been made to accurately model the MOS varactors in these different modes of operation and is an active area of research [56]-[59].

Although the abovementioned arguments were limited to a NMOS transistor configured as a MOSCAP, they are equally applicable to a MOS varactor using an PMOS transistors. However, NMOS transistors present higher *Q*, or lower loss, when compared to their PMOS counterparts due to the higher mobility of the electrons when compared to holes [56].

The quality factor in a MOSCAP is mainly determined by the channel and gate resistance of the MOS transistor. The use of short- and multi-fingered gate electrodes can reduce the gate resistance to some extend. The channel resistance can be decreased by using a smaller channel length. Ultimately, the minimum MOSCAP channel length is set by the process technology of interest. However, this smaller gate increases the gate resistance which can become the dominant factor in determining the *Q*. On the other hand, the effective tunability of the MOSCAP is limited by the overlap capacitance between the gates of the MOS transistor and the source-drain diffusions. Therefore, to increase the tunability of the MOSCAP, a larger channel length is required.

NMOS transistors were considered as the tuning element in our VCO due to their higher *Q* when compared to the PMOS transistors while being compatible with a purely CMOS process technology. Extensive device simulations were carried out for different channels lengths and the best trade-off quality factor versus capacitance variation was found when the transistor channel length is 1μm with multi fingered gate electrodes of 2.5μm width. For this case, the varactor quality factor was about 30 at 2GHz, which is well above typical values of spiral on-chip inductor's quality factor in silicon process

technologies [55]. This varactor presents a maximum to minimum capacitance ratio ($C_{v,max}/C_{v,min}$) of 3.1.

It is noteworthy that Figure 3.7 and Figure 3.8 show the capacitance vs. voltage characteristics for a very small signal superimposed on the bias voltage of the varactors. On the other hand, *LC* VCOs have a large oscillation amplitude to comply with the minimum tank voltage constraints, therefore, the instantaneous value of the varactor capacitance varies over the signal period. Nevertheless, the average of the capacitance in a varactor is still a function of the control voltage, but the tuning characteristic of the VCO would deviate from the ideal $f_{osc} = 1/2\pi\sqrt{L \times C(V)}$ [60]-[62].

3.3.2 Process Technology, Design Equations and Constraints

The technology chosen for the integration of the oscillator prototype was Conexant's BC35 [63]. Although this is a BiCMOS process technology, only the MOS transistor were used. The MOS transistors have a minimum channel length of 0.35μm. To be able to analyze and gain insight into the design issues of the proposed oscillator topology, it is necessary to model the transistor gain, output conductances and capacitances as a function of the transistor width and the bias current [9][64][65]. These transistor elements are shown in the model depicted in Figure 3.9 while their dependence in the transistor width, *w,* and bias current, I_{bias}, is summarized in Table 3.3. To achieve fast transistor switching and to lower the parasitic capacitances, the minimum transistor channel length was used for the derivation of Table 3.3.

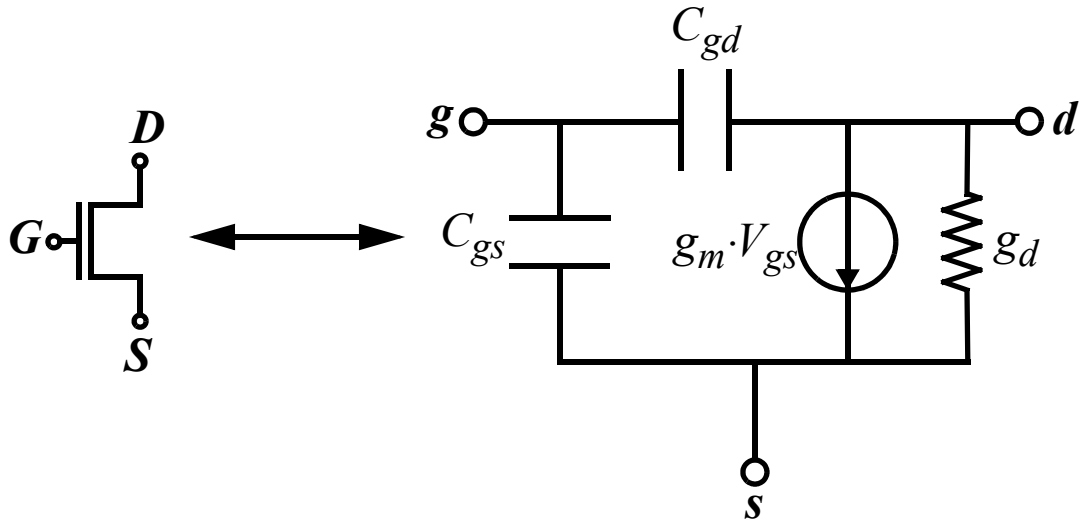


Figure 3.9: NMOS transistor model.

Element	Value
g_m	$150 \cdot w[1/\Omega]$
g_d	$0.157 \cdot I_{bias}^{0.6} \cdot w^{0.4}[1/\Omega]$
C_{gs}	$1.51 \cdot w[nF]$
C_{gd}	$0.36 \cdot w[nF]$

Table 3.3: NMOS transistor model values

NMOS transistors operating in inversion mode are used as varactors for the frequency tuning of the oscillator. They are modelled by a variable capacitor C_v in series with a resistor R_v and capacitances to the substrate, as depicted in Figure 3.10.

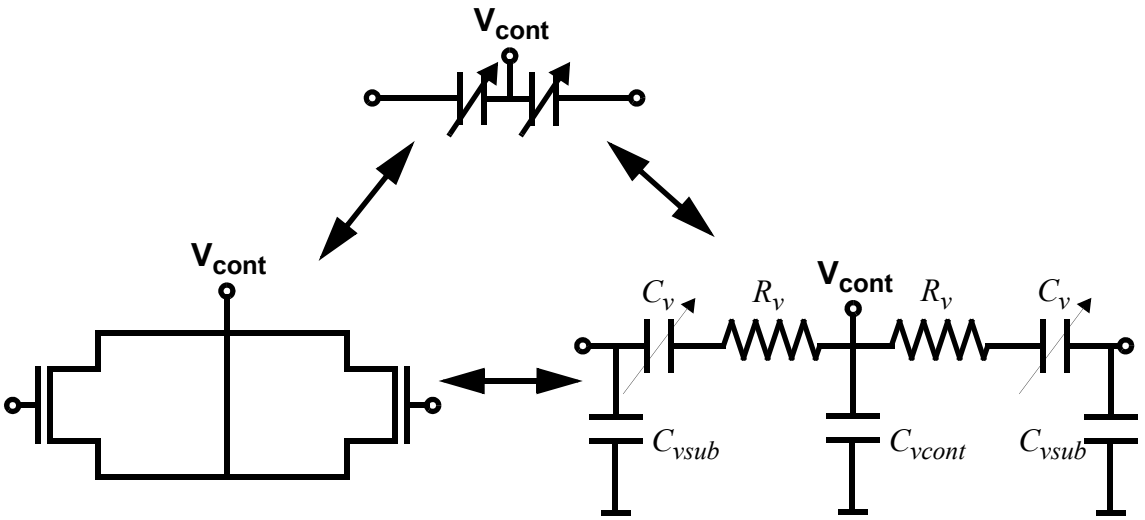


Figure 3.10: MOS varactor equivalent circuit model

The integrated spiral inductors are modelled using the symmetrical π-circuit model proposed in [66] which is depicted in Figure 3.11.

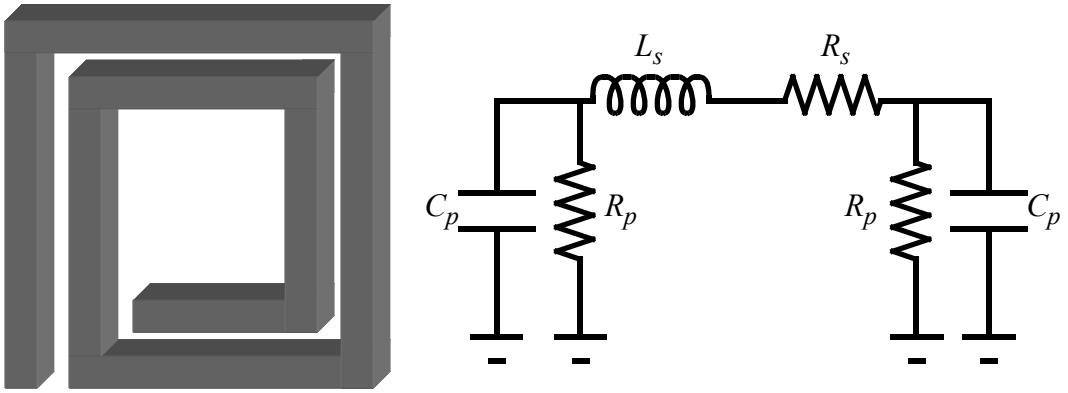


Figure 3.11: Integrated spiral inductor model.

Initially, there are thirteen design variables that are associated with this oscillator topology, namely, the parameters for the on-chip spiral inductor model (L_s, R_s, C_p, R_p), the minimum and maximum capacitance values of the varactors ($C_{v,\,min}$, $C_{v,\,max}$) and its series resistance (R_v), the core and cross-coupled MOS transistors dimensions (w, w'), the voltage divider capacitances (C_1, C_2), the load capacitance (C_{load}) and the oscillator

bias current (I_{bias}). These design variables are shown in Table 3.4. The cross-coupled transistor elements will be differentiated with a prime throughout the reminder of this section.

Circuit Elements	Variables
Spiral Inductor	L_s, R_s, C_p, R_p
Varactors	$C_{v,\,min}$, $C_{v,\,max}$, R_v
Transistors	w, w'
Capacitors	C_1, C_2, C_{load}
Oscillator Current	I_{bias}

Table 3.4: Initial design variables.

The equivalent circuit model for the noise shifting differential Colpitts oscillator of Figure 3.6 is depicted in Figure 3.12, where the dashed line represents either the ground or the common mode.

In this schematic, $C^{\dagger}_{load}$ is the parallel combination of the parasitic capacitances of the core transistor, the integrated inductor and the loading capacitance from the next stage, *i.e.,*

$$C^{\dagger}_{load} = C_{load} + C_p + C_{vsub} + C_{db} + C_{gd} \tag{3.4}$$

and $C^{\dagger}_2$ is the parallel combination of the parasitic capacitances of the core and cross-coupled transistor as well as the capacitor's voltage divider C_2*, i.e.,*

$$C^{\dagger}_2 = C_2 + C_{gs} + C_{sb} + C'_{db} + C'_{gb} + C'_{gs} + 4 \cdot C'_{gd} \tag{3.5}$$

Even though most of the circuit parameters vary with the operating point of the MOS transistors (g_m, g_d and parasitic capacitances) through the oscillation cycle [9][65], we can still use the values from Table 3.3 to allow an analytical treatment of the design constraints.

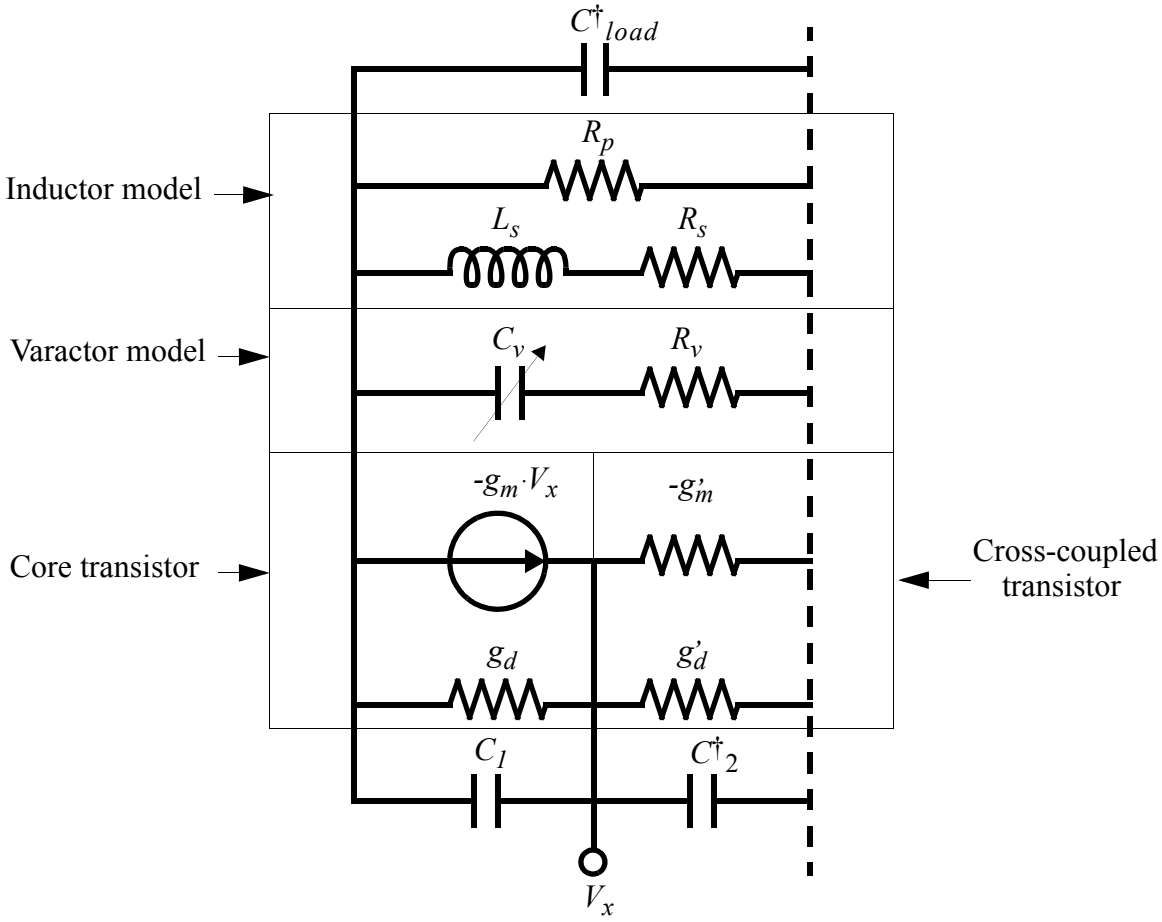


Figure 3.12: Equivalent noise shifting differential Colpitts oscillator model.

There are four primary parameters that are closely related to the oscillator behavior and will be helpful in the derivation of the constraints. These parameters are the effective tank conductance (or loss) g_{tank}, the effective negative conductance g_{active}, the tank capacitance C_{tank}, and the tank inductance L_{tank} [64]. The tank conductance is the parallel combination of the inductor loss, varactor loss and the equivalent output conductances of the core and cross-coupled transistors referred to the tank output, *i.e.,*

$$\begin{aligned} 2 \cdot g_{tank} &= g_L + g_v + g_{d,eq} + g'_{d,eq} \\ &= \left(\frac{1}{R_p} + \frac{R_s}{(L\omega)^2}\right) + (\omega \cdot C_v)^2 \cdot R_v + g_d \cdot \left(\frac{k}{k+1}\right)^2 + \frac{g'_d}{(k+1)^2} \end{aligned} \tag{3.6}$$

where the capacitor voltage divider ratio k was introduced to simplify the previous equation, *i.e.,*

$$C^{\dagger}_{2} = k \cdot C_{1} \tag{3.7}$$

The effective negative device conductance is the combination of the core and cross-coupled transistor gain referred to the output tank, *i.e.,*

$$2 \cdot g_{active,\,eq} = g_{active} + g'_{active} = g_{m} \cdot \left(\frac{k}{k+1}\right)^{2} + \frac{g'_{m}}{(k+1)^{2}} \tag{3.8}$$

The total tank capacitance is the parallel combination of $C^{\dagger}_{load}$, the equivalent capacitance voltage divider $C_{12,eq}$ and the varactor capacitance, *i.e.,*

$$C_{tank} = C^{\dagger}_{load} + C_{12,\,eq} + C_{v} = C^{\dagger}_{load} + C_{1} \cdot \frac{k}{k+1} + C_{v} \tag{3.9}$$

As the varactor capacitance varies from its minimum to maximum capacitance range ($C_{v,min}$ to $C_{v,max}$), the tank conductance and tank capacitance will vary accordingly as well, we will denote them as $g_{tank,min}$, $g_{tank,max}$, $C_{tank,min}$,and $C_{tank,min}$, respectively.

After developing equations (3.6) through (3.9), we are now able to formulate the design constraints over power dissipation, tank amplitude, frequency tuning, and minimum start up conditions for the noise shifting differential Colpitts VCO (Figure 3.6).

A minimum oscillator tank amplitude is required to provide large enough voltage swing for the next stage, which is the first constraint:

$$V_{tank} = \frac{I_{bias}}{g_{tank,\,max}} \geq V_{tank,\,min} \tag{3.10}$$

where the worst-case scenario g_{tank} is considered in the last equation. Secondly, the minimum small signal gain can be expressed as follows:

$$g_{active} \geq \kappa_{min} \cdot g_{tank,\,max} \tag{3.11}$$

where κ_{min} usually has a value of 2 to 3 to guarantee reliable start-up.

Finally, the oscillator output frequency has to meet the minimum and maximum specified by the tuning range, *i.e.,*

$$\frac{1}{\sqrt{L_{tank} \cdot C_{tank,\,max}}} \leq \omega_{osc,\,min} \tag{3.12}$$

$$\frac{1}{\sqrt{L_{tank} \cdot C_{tank,\,min}}} \geq \omega_{osc,\,max} \tag{3.13}$$

It is usually the case that the frequency tuning constraints are given in terms of oscillation center frequency, f_{center} and tuning range in percentage, f_{tune}. The minimum and maximum oscillation frequencies can be easily calculated as follows:

$$\omega_{osc,\,max} = 2\pi \cdot f_{center} \cdot \left(1 + \frac{f_{tune}}{2}\right) \tag{3.14}$$

$$\omega_{osc,\,min} = 2\pi \cdot f_{center} \cdot \left(1 - \frac{f_{tune}}{2}\right) \tag{3.15}$$

3.3.3 Graphical Optimization Methods and Inductance Selection

Due to the existence of multiple variables to optimize in this oscillator topology, graphical methods were chosen to find an optimum design after [24]. To facilitate this optimization, a reduction of the design variables from 13 (as shown in Table 3.4) can be accomplished by making some simplifying assumptions.

First, as the phase noise performance has a direct relationship with the power stored in the tank, the power consumption constraint is tight and we can set $I_{bias} = I_{max}$, which is the maximum allowed bias current in the constraints. Second, the capacitor voltage divider ratio k defined in (3.7) is set to 4 to exploit the better cyclostationary properties of the oscillator after [54]. Third, the ratio $C_{v,\,max} / C_{v,\,min}$ for the optimized varactors is around 3.1 and remains constant for a scalable layout. This varactor achieves a minimum quality factor of 30 and thus, we can calculate the worse case-scenario varactor series resistance R_v. Fourth, as the output buffer of the oscillator can be pre-designed, and thus, the loading

capacitance from this stage (C_{load}) can be known *a priori*. Finally, the spiral inductor parameters (L_s, R_s, C_p, R_p) are calculated for the particular inductor used. Therefore, it is possible to reduce the set of independent variables to four, as shown in Table 3.5.

Circuit Elements	Variables
Varactors	$C_{v,\,max}$
Transistors	w, w'
Capacitors	C_1

Table 3.5: Reduced set of design variables.

To demonstrate a typical design problem, specific design constraints are imposed to the oscillator topology of Figure 3.6 and are summarized in Table 3.6.

Specification	Variable	Value
Center frequency	f_{center}	2.1GHz
Frequency tuning	f_{tune}	25%
Supply voltage	V_{supply}	2.5V
Minimum oscillation amplitude	$V_{tank,\,min}$	2.0V
Bias current	I_{bias}	4mA
Minimum start up gain	κ_{min}	2.5

Table 3.6: Specific design constraints.

Although there are four variables in the design space (Table 3.5), we can get some insight by setting C_1 and w' to a specific value and plot equations (3.10) through (3.13) in the $C_{v,\,max}$ and w plane as shown in Figure 3.13.

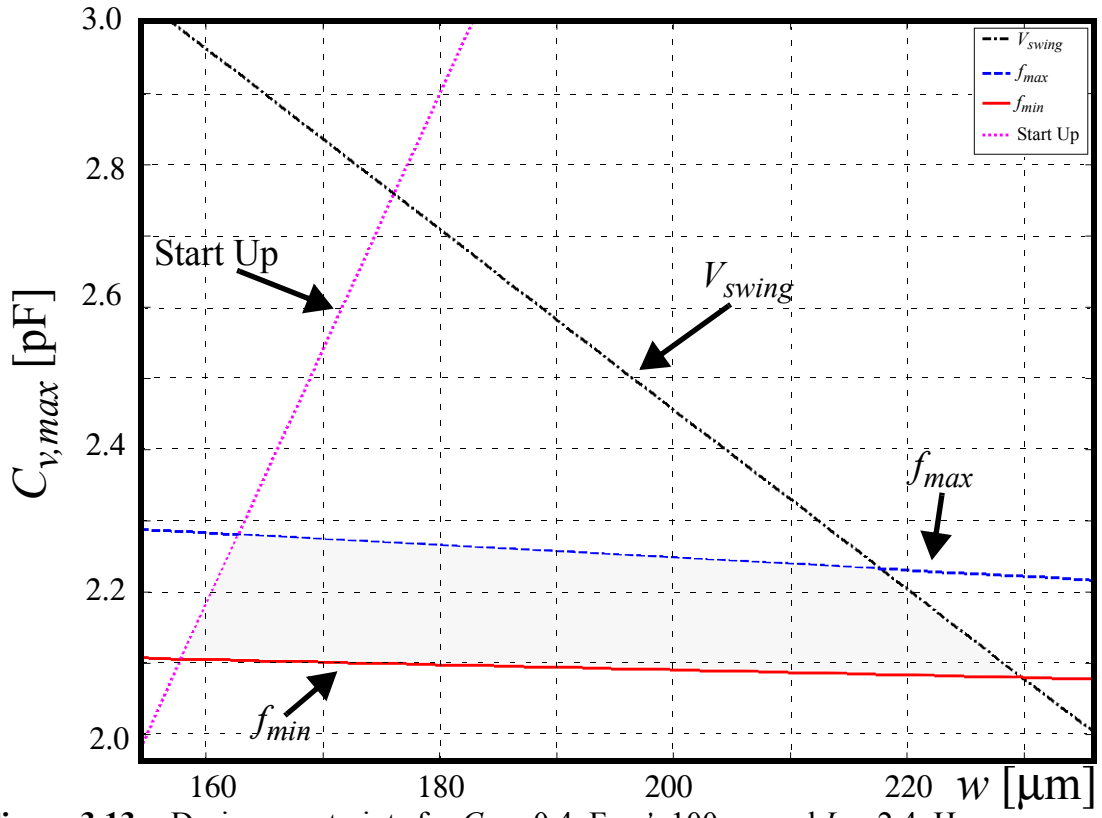


Figure 3.13: Design constraints for C_1 = 0.4pF, w'=100µm and L_s= 2.4nH.

This figure is considered for the case where C_1 = 0.4pF and w'=100µm and L_s= 2.4nH. The loci of the points below the tank amplitude depicted with dashed-doted black line results in a tank amplitude of $V_{tank} \geq 2.0V$ using (3.10). The dotted cyan line is obtained from (3.11) and represents the small-signal gain of $\kappa_{min} = 2.5$. The points laying on the right-hand side of this line will satisfy the minimum start-up condition. A center frequency of 2.1GHz and a tuning range of at least 25% is achieved by the design points below the dashed blue line and above the solid red line, these two lines signify the minimum (3.12) and maximum (3.13) oscillation frequencies, respectively. This graphical method is useful to obtain an intuition about the effect on these constraints from the C_1 and w' variables.

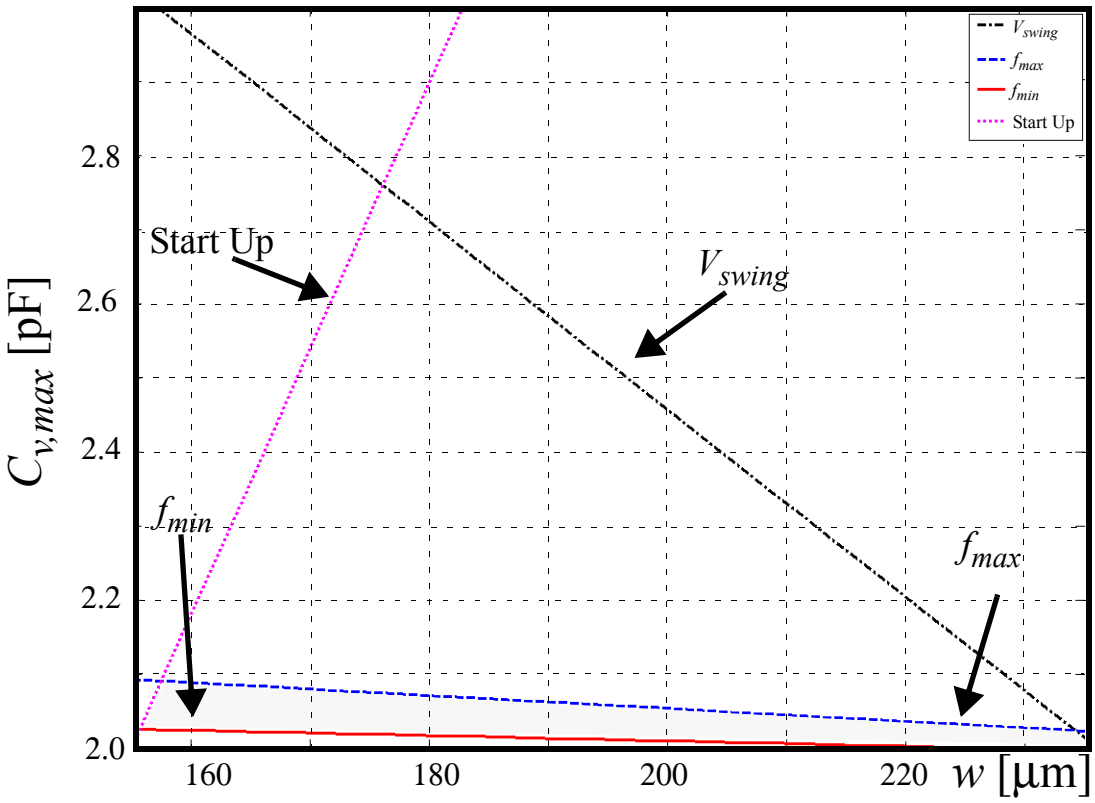


Figure 3.14: Design constraints for C_1 = 0.6pF, w'=100µm and L_s= 2.4nH.

For instance, Figure 3.14 shows these design constraints for the case where C_1 = 0.6pF and w'=100µm and L_s= 2.4nH. An increase in C_1 will translate into a tighter design locus for the tuning rage. As another example, Figure 3.15 shows the design constraints for the case where C_1 = 0.4pF and w'=300µm and L_s= 2.4nH. In this case the start up condition is relaxed by a having a wider cross-coupled transistor.

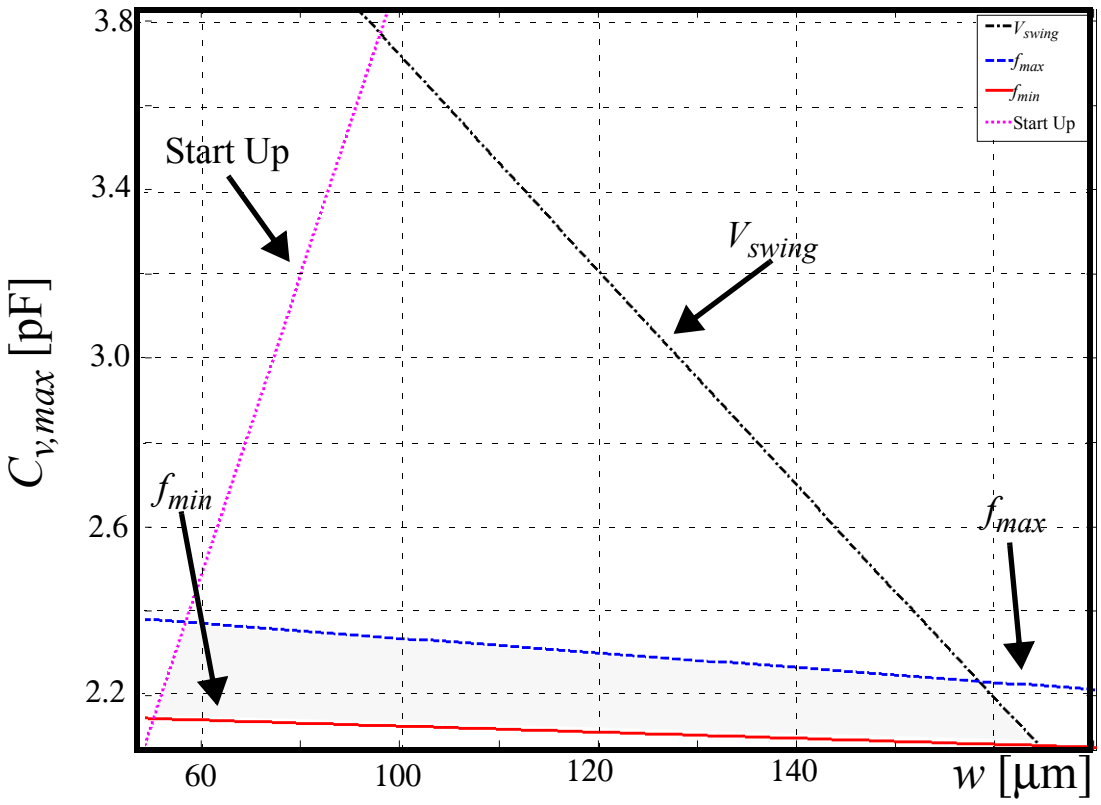


Figure 3.15: Design constraints for C_1 = 0.4pF, w'=300µm and L_s= 2.4nH.

As discussed in Chapter 2, the quality factor of the tank has a substantial impact on the phase noise performance of *LC* oscillators indirectly. A higher *Q* for the tank translates to a lower bias current that decreases the noise from the active devices while improving the energy transfer efficiency. Also, for a given oscillation frequency, it is possible to decrease the kT/C noise of the parallel resonator by using an inductor with smaller value as explained in more detail in [24]. Therefore, the optimization strategy for this oscillator prototype can be summarized as follows: Set the bias current to I_{max} and pick the highest *Q* inductor for an initial guess of the inductance value. An inductor library can be obtained using simulation tools such as ASITIC [55]. Plot the design constraints in the $C_{v,max}$-w plane for a proper range of C_1 and w' values and pick the feasible design points. These points are compared using a transient, ISF_{eff}, and phase noise simulation. This process is

repeated for a smaller inductance value L until the design constraints cannot be met. Finally, choose the design point that shows the best phase noise performance.

3.4 Experimental Results

The design methodology described in the previous section was used for the implementation of a noise shifting differential Colpitts VCO prototype. The complete circuit schematic for this topology is depicted in Figure 3.16. The final values of the components and transistor sizes for this schematic are shown in Table 3.7. Open drain transistors are used as buffers and are designed to drive a 50Ω load at 0dBm. Figure 3.17 shows the die photo of the test VCO, where the main blocks of the oscillator are highlighted.

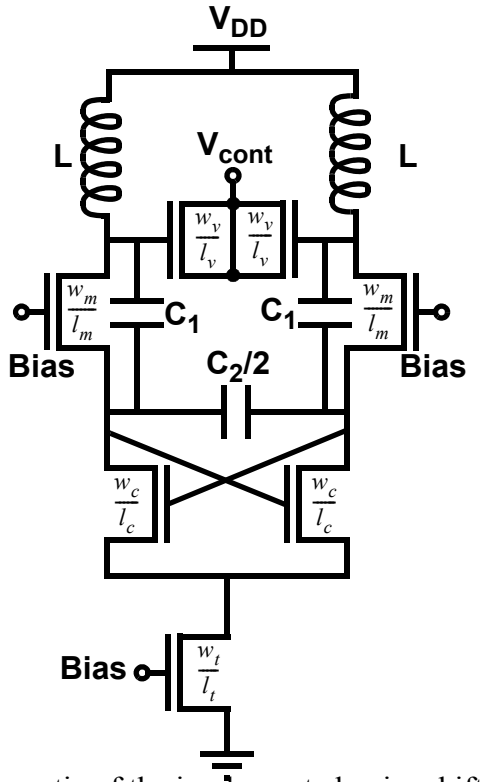


Figure 3.16: Circuit schematic of the implemented noise shifting differential Colpitts oscillator.

Variable	Value
L	3.6nH
C_1	600fF
C_2	2.1pF
w_v	250µm
l_v	1.0µm
w_m	130µm
l_m	0.35µm
w_c	80µm
l_c	0.35µm
w_t	300µm
l_t	0.95µm

Table 3.7: Component values for the implemented noise shifting differential Colpitts VCO.

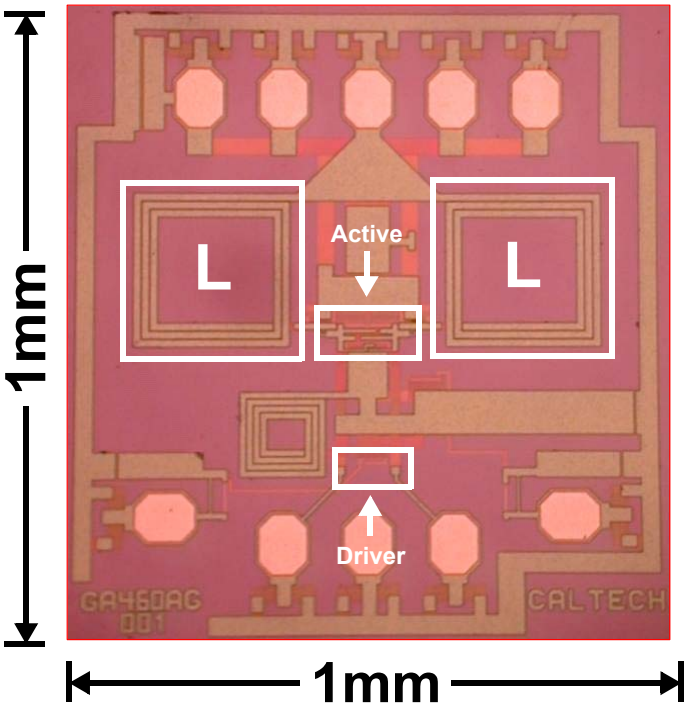


Figure 3.17: Differential Colpitts oscillator die micrograph.

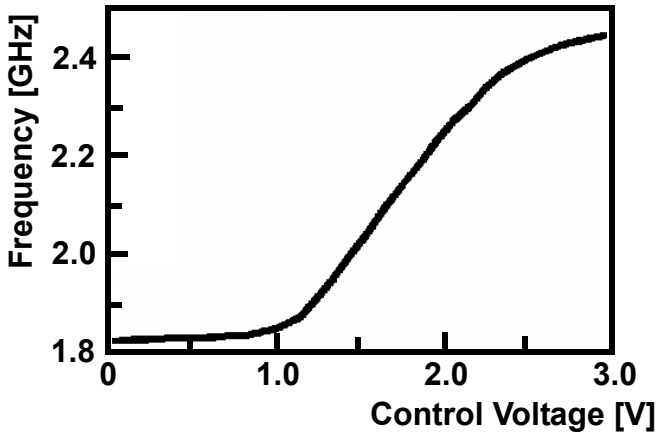


Figure 3.18: Differential Colpitts oscillator frequency tuning.

The oscillator operates from 1.8GHz to 2.45GHz, which corresponds to a center frequency of 2.12GHz and a tuning range of 30.5%, as shown on Figure 3.18. It can be noted that the voltage to frequency transfer function of the VCO is very linear over more than 500MHz, which corresponds to 80% of the frequency tuning of the VCO. The oscillator phase noise is measured using an NTS-1000 phase noise analyzer with a DRC 14000 down converter as well as an HP8563 spectrum analyzer with phase noise measurement utility.

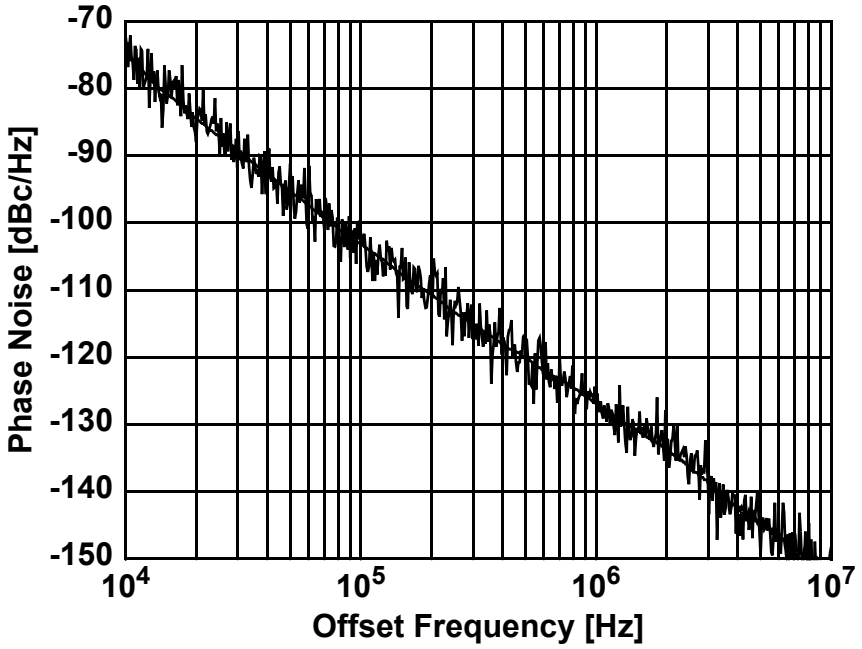


Figure 3.19: Measured phase noise vs. offset frequency at 1.8GHz

Figure 3.19 shows the plot of the phase noise versus the offset frequency from the 1.8GHz carrier. The oscillator shows a phase noise of -139dBc/Hz at 3MHz offset using low inductor *Q* of 6, while drawing 4mA from a 2.5V supply.

To compare the performance of the noise shifting differential Colpitts VCO to the widely used complementary cross-coupled oscillator, Table 3.8 shows the performance measures of the complementary cross-coupled VCO presented in [24] along with those of this oscillator prototype. These two oscillator were fabricated in the same process technology and optimized using graphical methods. Moreover, they are biased at the exactly same voltage and current, and have comparable center frequencies and tuning ranges. This noise shifting differential Colpitts oscillator shows 8dB better phase noise at 3MHz offset than the complementary cross-coupled oscillator of [24] under the same conditions.

Oscillator	**Noise Shifting Differential Colpitts**	**Complementary Cross-coupled [24]**
Technology	BC35	BC35
Optimization	Graphical Methods	Graphical Methods
Supply voltage	2.5V	2.5V
Bias current	4mA	4mA
Center frequency	2.1GHz	2.3GHz
Tuning range	30.5%	26%
Phase noise at 3MHz offset	-139 dBc/Hz	-131 dBc/Hz

Table 3.8: Oscillator comparison.

To evaluate the performance of our oscillator one step further, the unit-less *power-frequency-normalized* and the unit-less *power-frequency-tuning -normalized* figures of merit:

$$PFN = 10 \cdot \log\left(\frac{kT}{P_{sup}} \cdot \left(\frac{f_{osc}}{f_{off}}\right)^2\right) - L\{f_{off}\} \tag{3.16}$$

$$PFTN = 10 \cdot \log\left(\frac{kT}{P_{sup}} \cdot \left(\frac{f_{tune}}{f_{off}}\right)^2\right) - L\{f_{off}\} \tag{3.17}$$

defined in [24] were calculated to recently published results and are shown in Figure 3.19 [24]-[47].Using these figures, this oscillator has the fourth largest *PFN* and the largest *PFTN* among these oscillators.

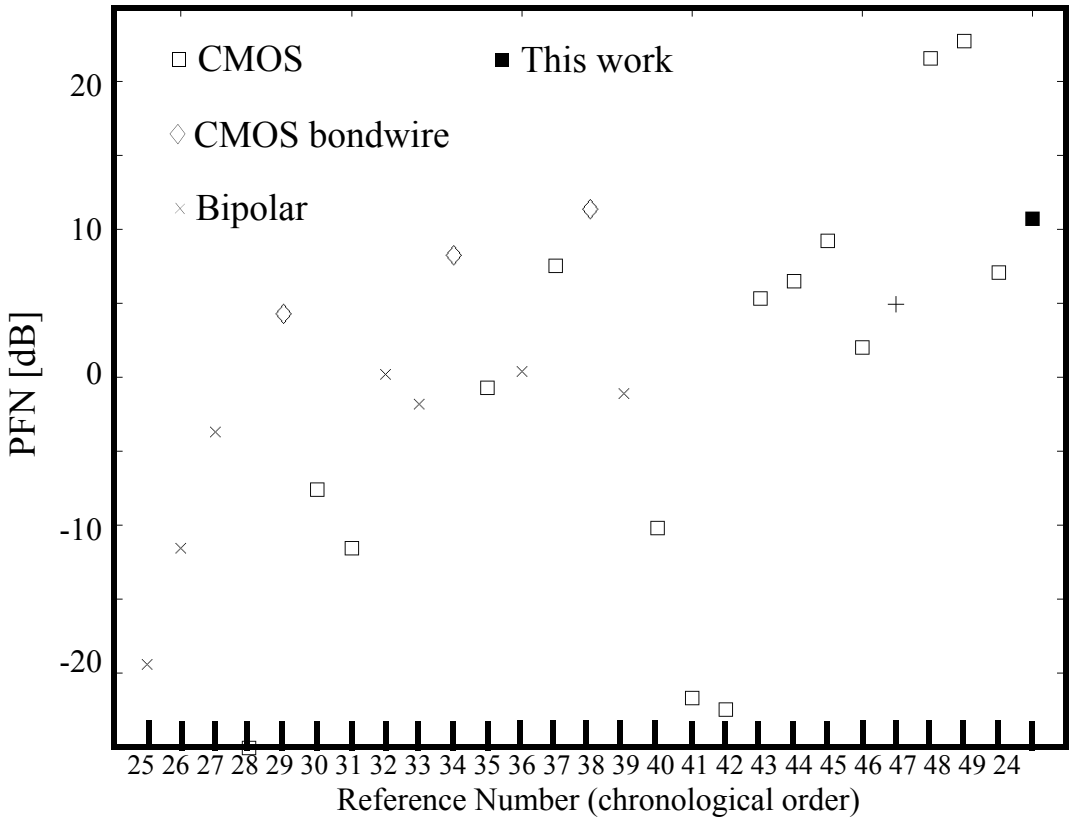


Figure 3.20: *PFN* for previously published oscillators.

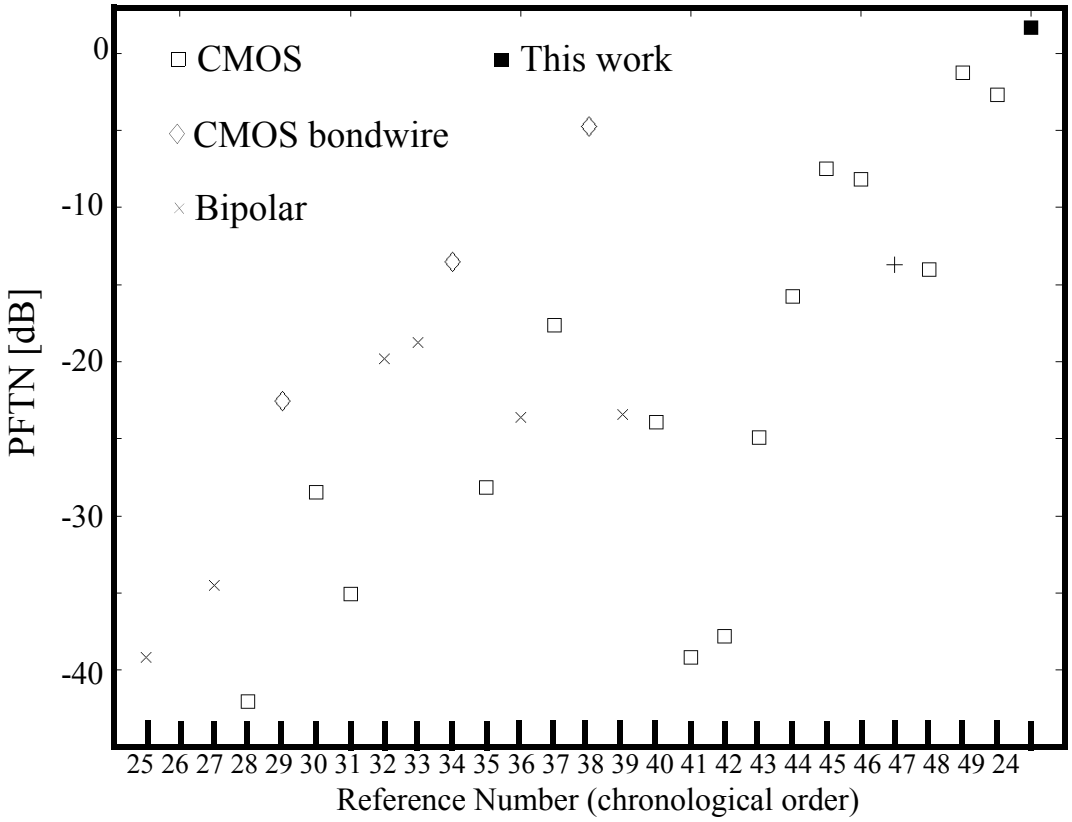


Figure 3.21: *PFTN* for previously published oscillators.

3.5 Summary

A new noise-shifting differential Colpitts VCO topology is introduced. It uses current-switching to lower the phase noise by cyclostationary noise alignment and improve the start-up condition. A general methodology is also devised for the optimization of this oscillator. The superior performance of this topology is demonstrated through measurement results of a CMOS implementation of a VCO prototype and achieves 8dB better phase noise at 3MHz offset than the complementary cross-coupled

oscillator under the same conditions. This test VCO achieves the largest *PFTN* and the fourth largest *PFN* among previously published integrated oscillators.

Chapter 4

Circular-Geometry Oscillators

The ever-increasing demand for faster data rates is pushing low-cost CMOS integrated circuits for operation at higher frequencies, while tighter jitter and phase noise requirements for the local oscillators are required for data re-timing and more available number of channels in the wired and wireless market, respectively.

As discussed in Section 2.4, the quality factor, Q, of the resonant tank plays a central role in the phase noise of an integrated oscillator. A higher tank Q translates to a a lower oscillator's bias current for a given voltage swing. The lower bias current decreases the noise from the active devices, which is the dominant contributor to phase noise [24].

In typical high-frequency integrated applications, the resonator quality factor is mainly determined by the inductor quality factor, Q_{ind}, whose main sources of degradation are the ohmic and substrate losses. For a given oscillation frequency in a parallel LC tank, it is desirable to use as small inductance L possible to minimize the kT/C noise of the resonator [24]. Also, to operate at higher frequencies, the tank's LC product must decrease, however, the loading from the next stage, parasitic capacitance of the active devices, and the stringent constraints on the tuning capability of the oscillator do not scale down resulting in a choice of an inductor with a smaller inductance value L.

In this chapter, a new oscillator topology is introduced. It allows the use of high quality factor slab inductors for high frequency and low noise applications. An overview of the different integrated inductors is presented in Section 4.1. Section 4.2 describes the design evolution leading to the circular-geometry oscillators, that uses magnetic coupling extensively. This coupling can be used to extract the output of the oscillator, as will be

discussed in Section 4.3. The performance measures of two test oscillators are presented in Section 4.4 as a proof of concept.

4.1 On-chip Inductors

There are three choices for the implementation of on-chip inductors, namely multi-turn spiral, single-turn spiral, and slab (Figure 4.1), while substrate and ohmic losses degrade the performance of these silicon integrated RF inductors. Due to the low resistivity of the silicon substrate (in comparison with GaAs or SOI), capacitive coupling through the substrate allows the current to flow not only in the metal conductor, but also through the silicon substrate. Inductive coupling is another important source of substrate loss. Due to the planar geometry of the inductor, magnetic fields penetrate deep into the silicon substrate, inducing current loops and related losses. In addition, on-chip inductors suffer from high ohmic losses due to the thin metal layers available in CMOS technologies and the skin effect that causes a non-uniform current distribution in a conductor at high frequencies. The consequence is a reduction in the effective inductor cross-section, decreasing the metal conductance significantly and hence, increasing the loss.

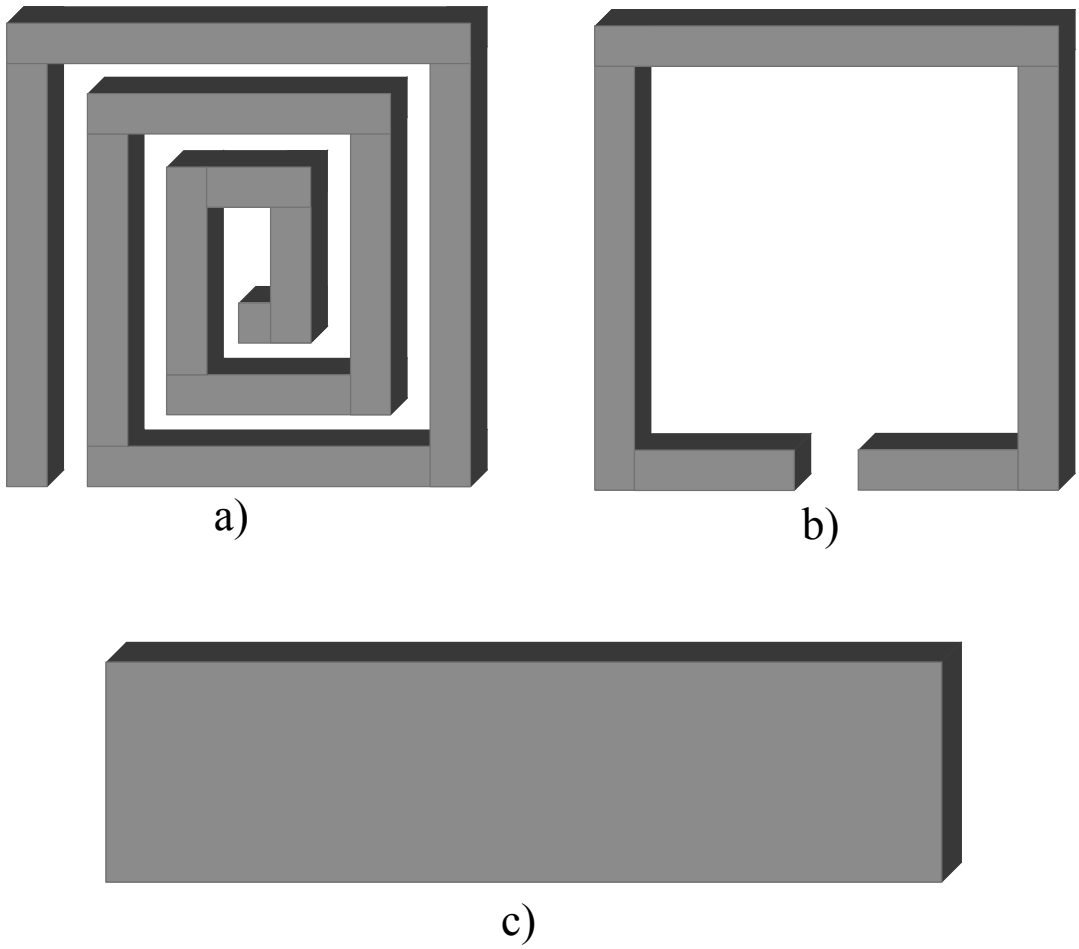


Figure 4.1: Different choices of integrated inductors, a) multi-turn spiral, b) single-turn spiral, c) slab.

Multi-turn spiral inductors benefit from the positive mutual coupling between the adjacent segments of the spiral, which enhances their inductance L for a given area. Therefore, it is usually the case that multi-turn spiral inductors result in the highest Q (or lower loss) among the three choices of integrated inductor for high inductance values. On the other hand, multi-turn spiral inductors are *not* the most efficient inductors in terms of quality factor for small inductance values. This is because the area of the spiral has to shrink for an inductor with smaller value while the spiral segments have to widen in order to decrease the inductance per length. Therefore, the overall quality factor is deteriorated

due to the extra substrate coupling and the generation of eddy currents in the innermost turns of the spiral that increase their effective series resistance significantly [40] [55].

On the other hand, single-turn spiral and slab inductors achieve the highest quality factor for inductors with small inductance value L [67]. For a given L and metal width w, the slab inductor length is shorter than the perimeter of the single turn spiral loop of the same inductance as shown in Figure 4.2. This is due to the negative mutual inductance between the segments on the opposite sides of the single-turn spiral. Moreover, the shunt resistance through the substrate between the two terminals of the slab inductor is higher when compared to that of the single-turn spiral due to the larger distance between them. Because of these, slab inductors have smaller series and substrate losses and present a significantly higher Q when compared to the single-turn spiral. In addition, the slab inductor is easier to model and optimize due to its inherently simpler geometry.

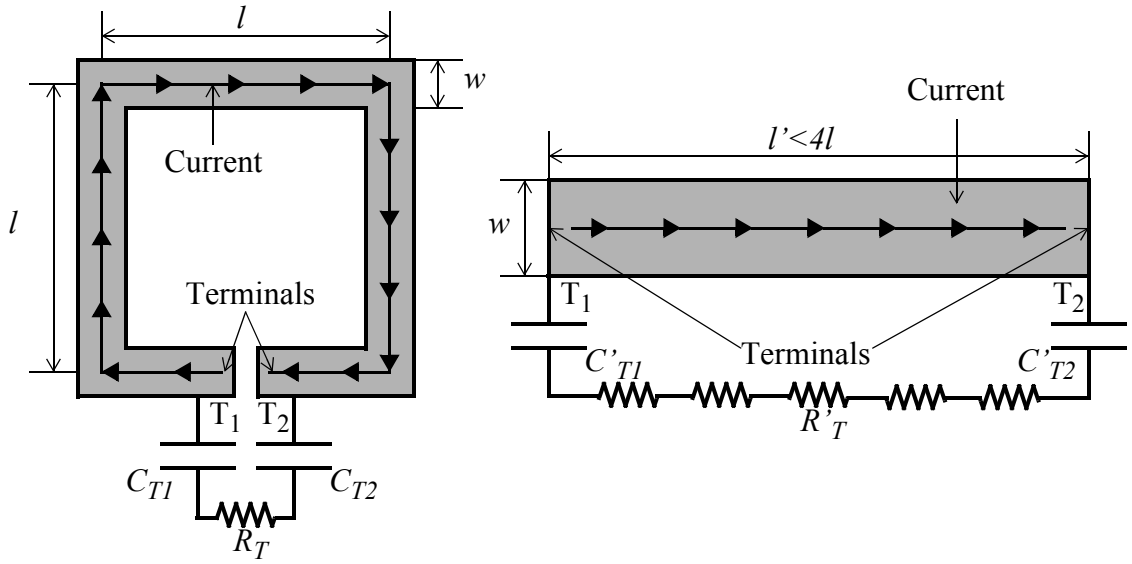


Figure 4.2: Single-turn and slab inductor comparison.

To visualize these trade-offs, Figure 4.3 shows the simulated quality factor and self-resonance frequencies as a function of the inductance L for the multi-turn spiral inductor with a dashed line, the single-turn spiral inductor with a dotted line, and the slab inductor with a solid line, respectively. This simulations were carried out using ASITIC [55] and correspond to the inductor with the highest achievable quality factor for the given

inductance value L and to a specific process technology whose parameters are shown in Table 4.1. This simulations are considered for single- and multi-turn square inductors that occupy an area of up to 500μm by 500μm, and slab inductors with lengths of up to 1300μm.

Description	Value
Metal Thickness	4μm
Metal Resistance	7mΩ/sq.
Metal Type	Cu
Oxide Thickness	11.6μm
Oxide ε_r	4.2
Substrate Thickness	700μm
Substrate ε_r	11.9
Substrate Resistivity	13.5Ω/cm

Table 4.1: Typical silicon process technology.

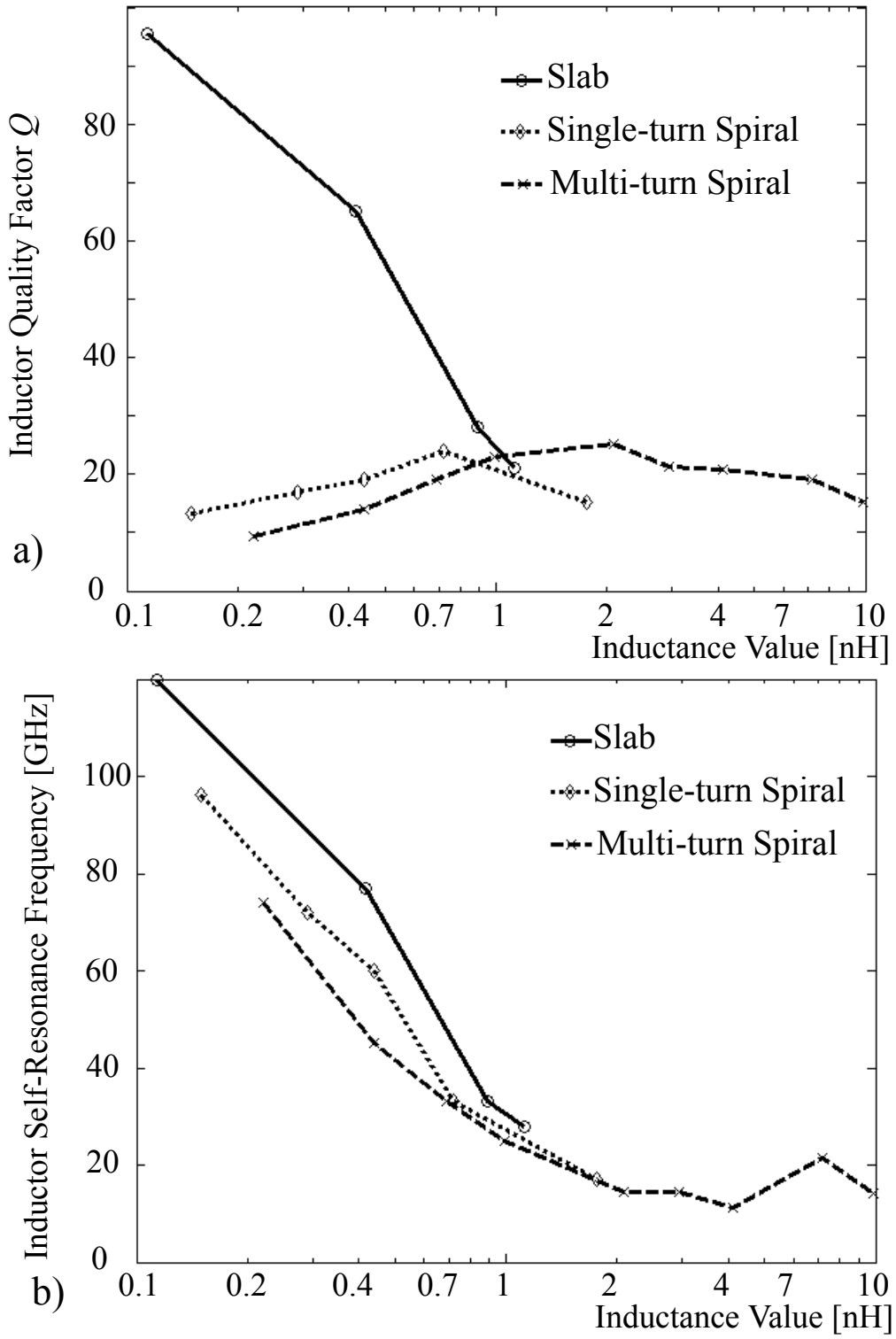


Figure 4.3: Inductor comparison vs. inductance value, a) quality factor Q, b) self-resonance frequency.

Interestingly enough, the slab inductors show the highest quality factor among all these integrated inductors for small inductance values. Moreover, they attain the highest self-resonant frequencies. This is because the slab inductor length is shorter than the perimeter of the single turn spiral loop of the same inductance *L* and metal width *w*, which translates to smaller capacitive coupling to the substrate. Also, the multi-turn spiral inductor suffers from a larger parasitic capacitance between adjacent turns and thus, lowers its self-resonant frequency, hindering its use for high-frequency applications.

Despite these advantages, slab inductors are not commonly used in integrated oscillators because of the intrinsic topological constraints for the interconnection of its terminals in the layout. The slab inductor terminals must be connected to the resonating capacitor *C* and to the oscillator core as shown in Figure 4.4. These interconnections add additional inductance and loss that can defeat the purpose. In other words, these interconnections lead to a configuration similar to that of a single-turn spiral inductor, which degrades its performance in terms of quality factor and self-resonance frequency.

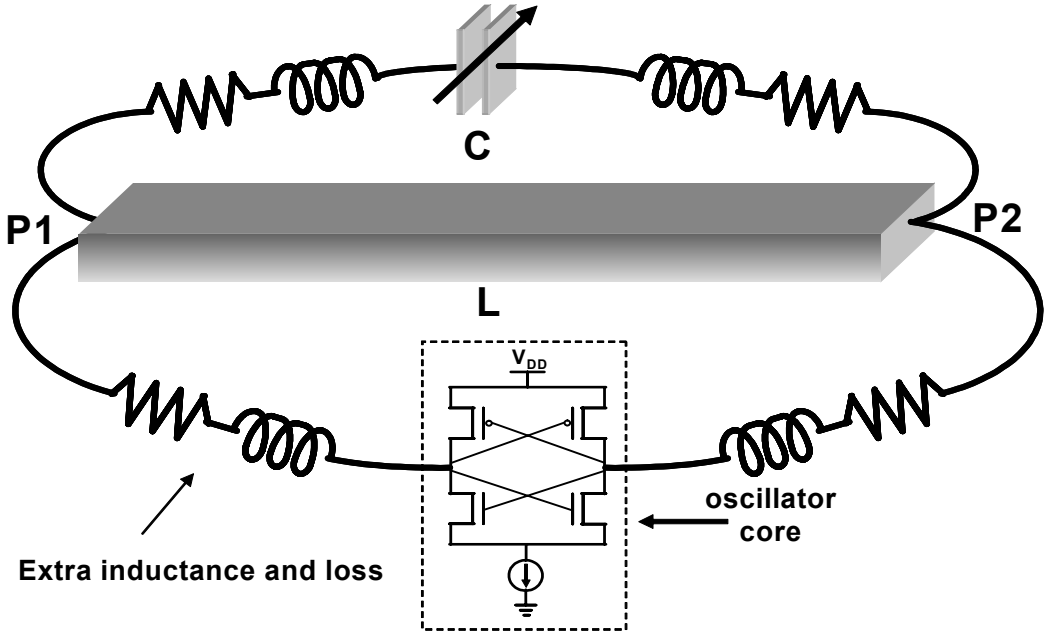


Figure 4.4: Slab inductor terminal connection issues.

4.2 Circular Geometry Oscillators

To overcome these issues, individual oscillator cores using slab inductors are laid out adjacent to one another and in a circular configuration, similar to that used to implement a power amplifier in [67] (Figure 4.4). In this implementation, the individual oscillators share two slab inductors with the neighboring oscillator cores. In the desired mode of operation, the slab inductor terminals oscillate at opposite phases. Therefore, an ideal connection of the active oscillator core across the slab inductor can be imitated by connecting the active cores to two adjacent terminals of neighboring slabs. This will work when the slabs are placed in a circular geometry, as in Figure 4.5.

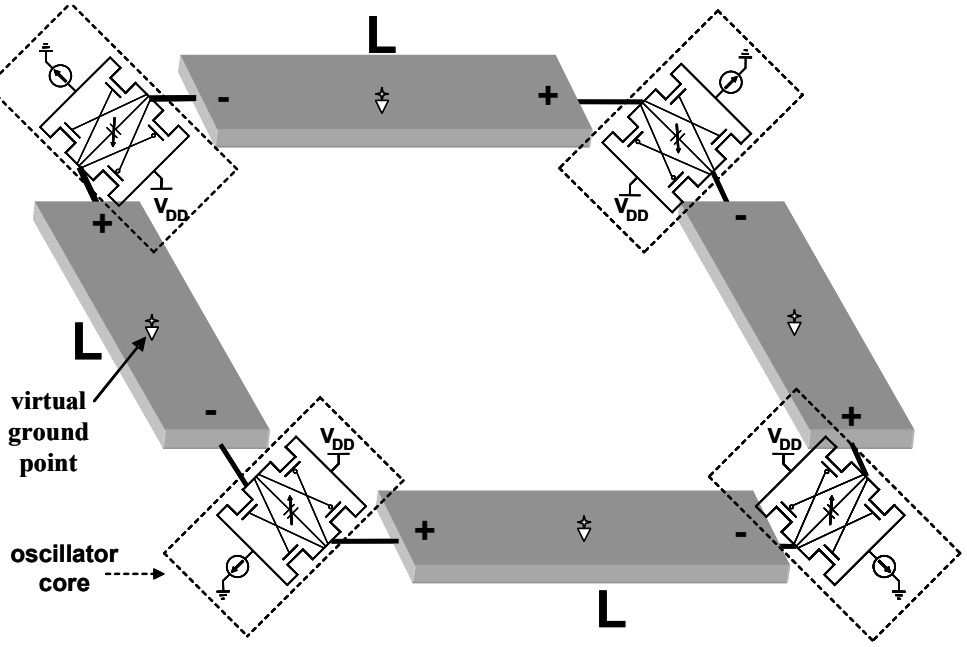


Figure 4.5: Proposed oscillator topology.

While very effective in principle, this approach can suffer from parasitic modes of oscillation and self-induced dc latching problems, in the absence of safeguards against

these phenomena. For instance, Figure 4.6 shows a possible stable dc solution of the topology, as from a dc standpoint, it is nothing but four latches connected in a loop.

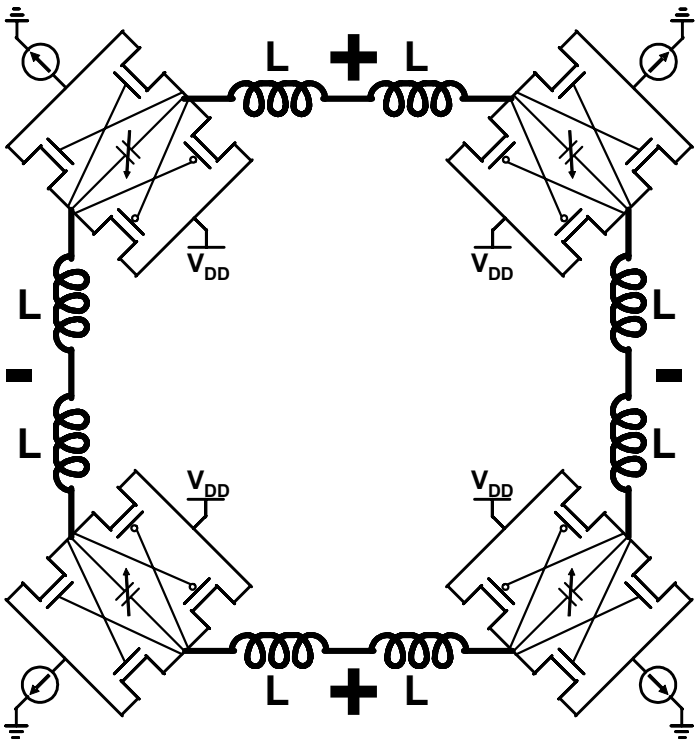
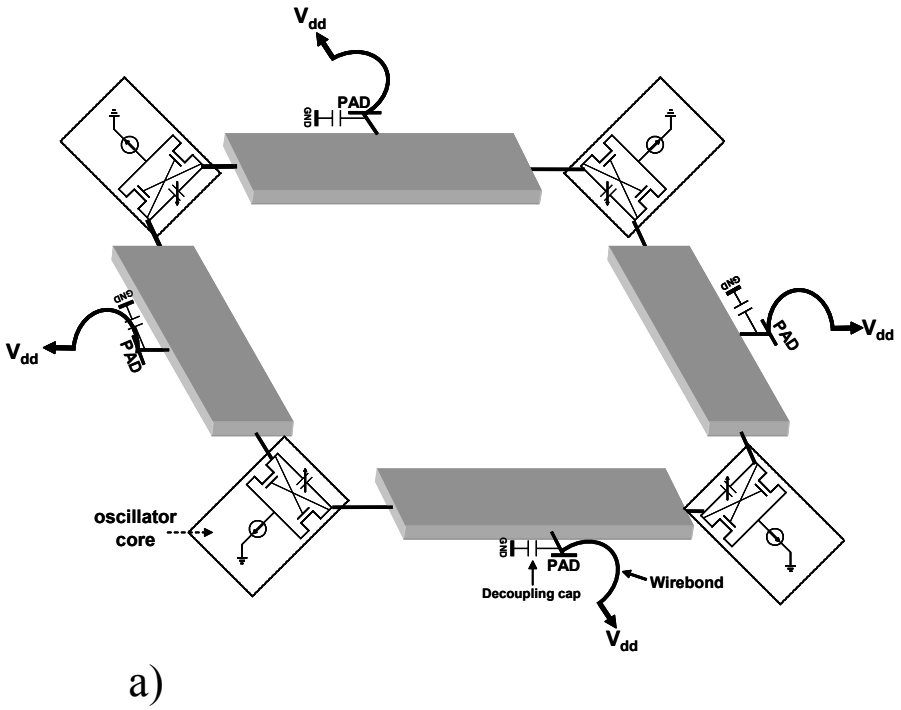


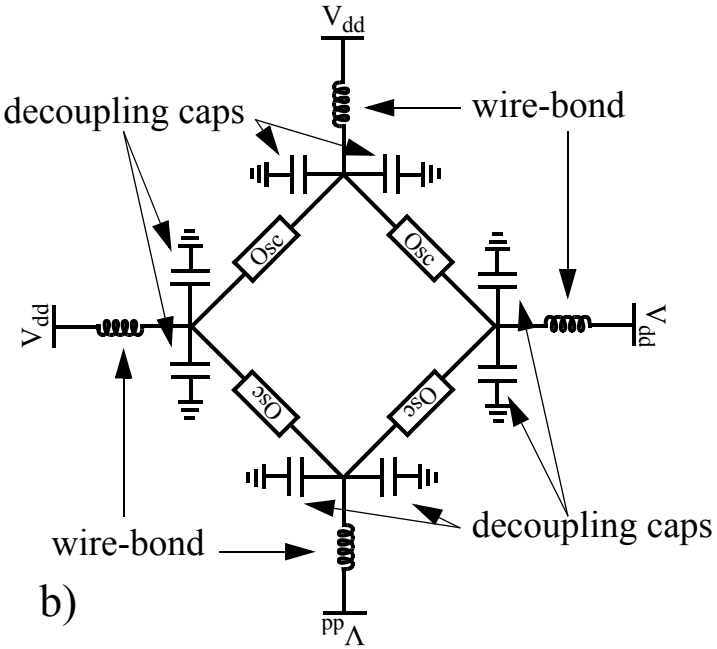
Figure 4.6: dc latching issues.

A less obvious example is depicted in Figure 4.7a. In this configuration, the oscillator core comprises four NMOS-only cross-coupled cores with a slab center connection to V_{DD}. If the on-chip decoupling capacitances and the inductance of the wire-bonds are taken into account, there would be an oscillation mode related to these components. For typical values of wire-bonds and decoupling caps, the oscillation frequencies associated with these components would be of few hundred of megahertz. At these frequencies, the slab inductors have a very small impedance and behave practically as a short. Figure 4.7b shows the equivalent circuit for this configuration where the four oscillator cores are

effectively connected in parallel and a high gain-high Q oscillation mode would be associated with these parasitic components.



a)



b)

Figure 4.7: Undesirable oscillation modes, a) block diagram, b) equivalent schematic.

Interestingly, at the desired oscillation mode, the slab inductor middle points are at virtual ground. Thus, connecting them in dc would suppress the undesired dc and parasitic modes of oscillation, while it will not affect the desired mode of operation. This can be done in a symmetric fashion by introducing a cross, connecting the mid-points of the slab inductors at the center of the oscillator, as shown in Figure 4.8 [68]. This would short the outputs of the oscillator cores at low frequencies and even harmonics avoiding any possible dc latching. In addition to eliminating the dc latch issue, the cross loads the outputs of the oscillators with a small impedance decreasing the start-up gain of the parasitic oscillation modes.

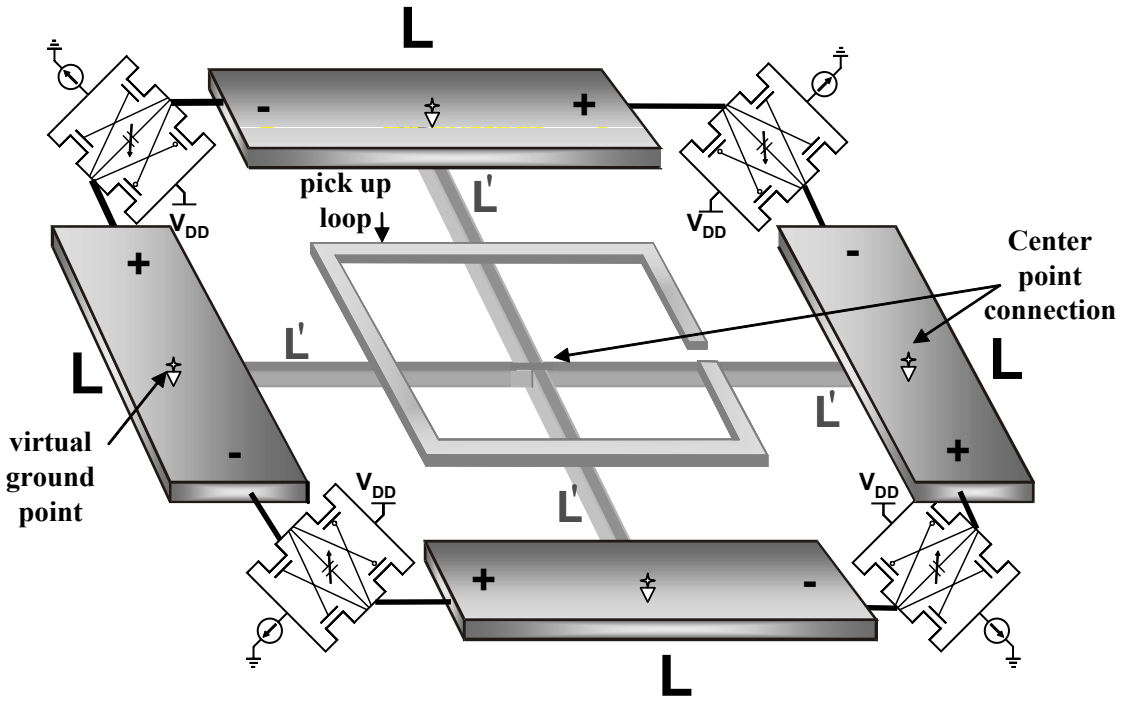


Figure 4.8: Proposed oscillator topology.

4.3 Magnetic Coupling

Due to the geometry, it is possible to extract the output of the oscillators by introducing a one turn metal strip in the middle of the circular-geometry oscillator to act as a magnetic pick-up as shown in Figure 4.8. The internal metal loop harnesses the induced

magnetic field to generate a voltage between its terminals. This is particularly useful, as the pick-up loop allows to load each corner evenly, and thus, a high degree of symmetry in the circular-geometry oscillator can be achieved.

The output voltage of the pick-up loop can be buffered, amplified, or further processed depending on the application. It can also be connected directly to a 50Ω load with a properly designed output matching network [67].

4.4 Design examples

This oscillator topology can be implemented using any number of corners and with a variety of active cores, such as the PMOS- or NMOS-only cross-coupled oscillators or the noise shifting differential Colpitts oscillator discussed in the previous chapter. It can also be used to implement oscillators with differential tanks, such as the complementary cross-coupled oscillator.

As a proof of concept, single frequency and voltage controlled circular-geometry oscillators with four corners were implemented using 0.18μm CMOS transistors. For these prototypes, the complementary cross-coupled oscillator cores were used due to its higher oscillation amplitude and low voltage of operation. Full electromagnetic simulations were carried out to model the high frequency behavior of the slab inductors and the coupling between them. The frequency dependent s-parameters were fit to a broad band lumped circuit model adequate for circuit optimizations. NMOS transistors were

used as varactors. The oscillators were designed using the optimization strategies of Chapter 3.

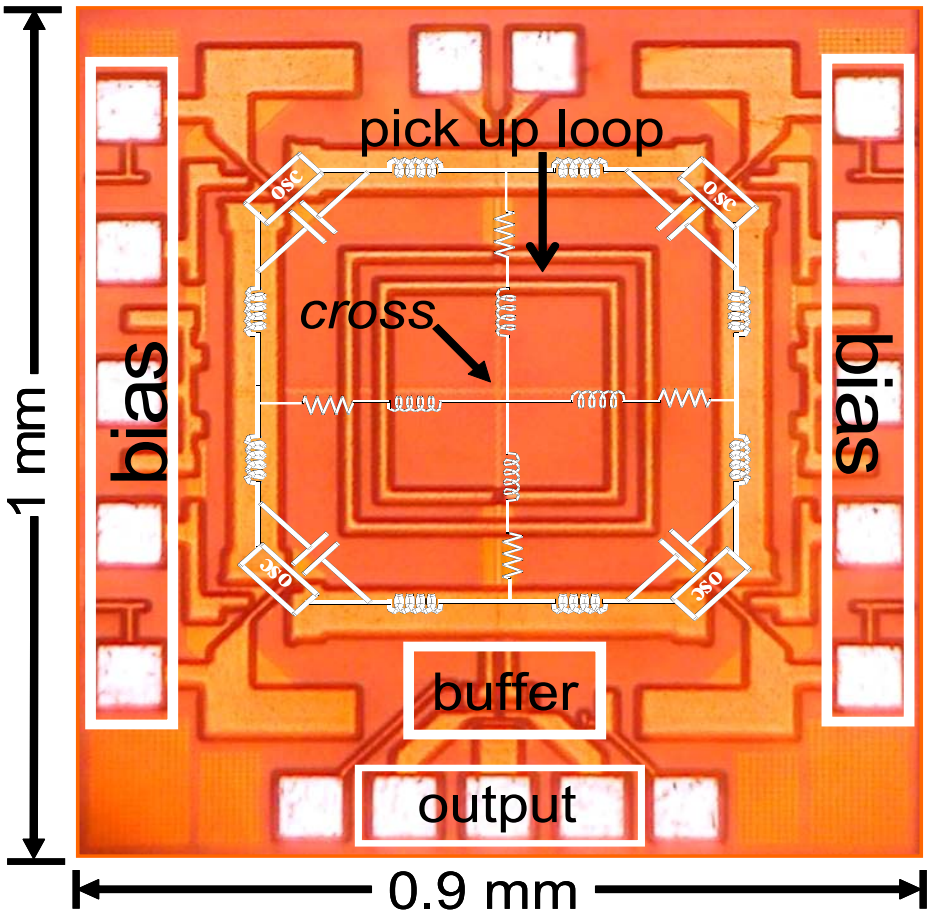


Figure 4.9: Single-frequency circular-geometry oscillator die micrograph.

Figure 4.9 shows the die photo of the single frequency circular-geometry oscillator prototype, where the main blocks of the oscillator are highlighted. It operates at 5.33GHz and shows a phase noise of –147.3dBc/Hz at 10MHz offset from the carrier while drawing 10mA from a 1.4V supply. The oscillator phase noise is measured using an NTS-1000 phase noise analyzer with a DRC 14000 downconverter as well as an HP8563 spectrum

analyzer with phase noise measurement utility. Figure 4.10 shows the phase noise plot for this oscillator.

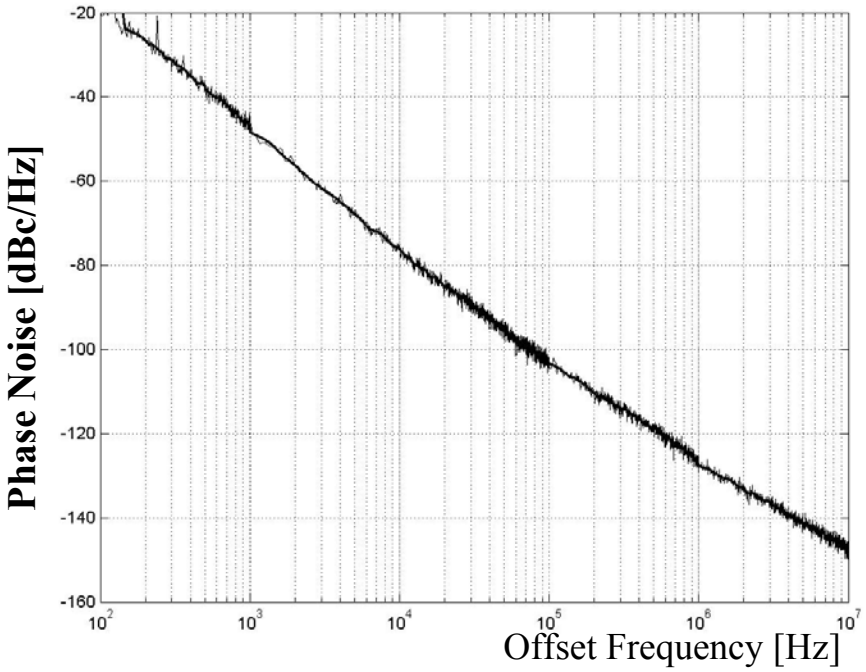


Figure 4.10: Single-frequency Circular-Geometry oscillator phase noise plot at f_{osc}=5.35GHz

The voltage controlled circular-geometry oscillator operates from 4.9GHz to 5.8GHz, which corresponds to a center frequency of 5.36GHz and a tuning range of 8.1%, as shown in Figure 4.11.

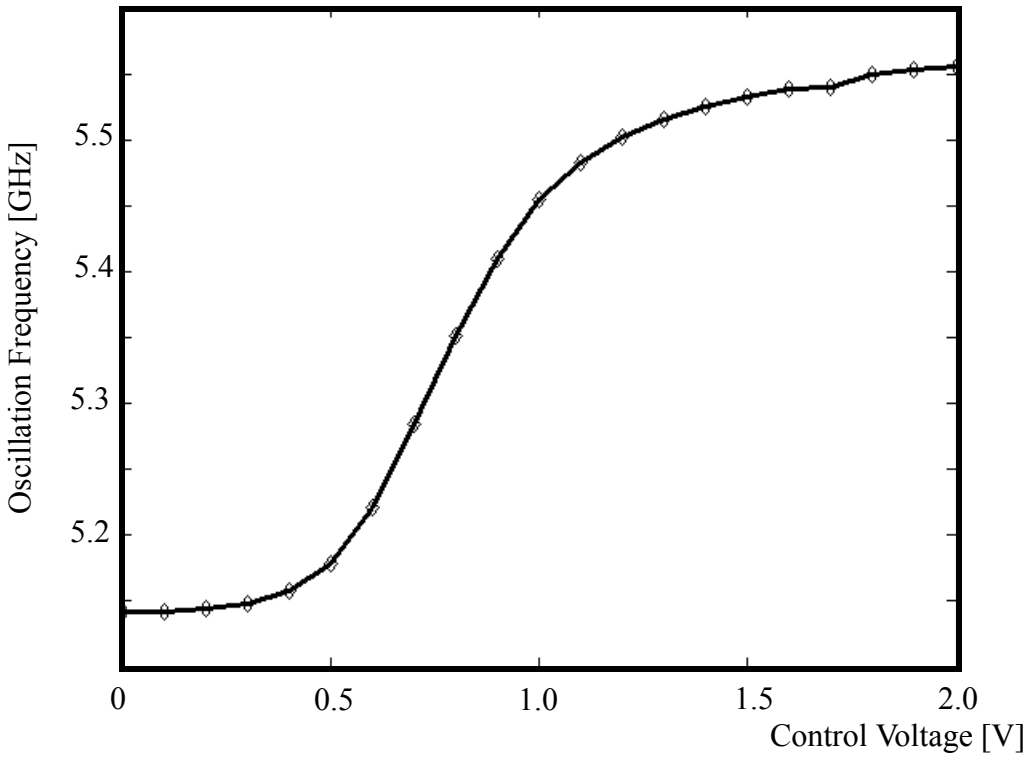


Figure 4.11: Voltage controlled circular-geometry oscillator frequency tuning.

The voltage controlled circular-geometry oscillator shows a phase noise of –142.2dBc/Hz at 10MHz offset from the carrier, drawing 12mA from a 1.8V supply. The lower phase noise of the fixed frequency oscillator compared to the VCO is primarily due to the low quality factor of the varactors at higher frequencies. The summary of the measurements for these oscillators is reported in Table 4.2.

Circular-Geometry Oscillator	Single Frequency	VCO
Technology	IBM SiGe 7HP (CMOS transistors only)	
Channel Length	0.18μm	
Center Frequency	5.33GHz	5.36GHz
Frequency Tuning	NA	8.3%
Output Power	1dBm	
V_{DD}	1.4V	1.8V
I_{bias}	10mA	12mA
Phase Noise @10MHz offset	-147.3dBc/Hz	-142.2dBc/Hz

Table 4.2: Circular-geometry oscillators performance summary.

To evaluate the performance of the newly proposed topology, the unit-less power-frequency-normalized and power-frequency-tuning-normalized figures of merit [24] are calculated for the best recently published fully-integrated oscillators and are shown in Table 4.3. As the slab inductors present better quality factor and self resonance frequencies for small inductance values (or high oscillation frequencies) when compared to the multi- and single-turn spiral inductors, only oscillators above 4GHz are considered in Table 4.3. The single frequency circular-geometry oscillator achieves the best PFN, while the circular-geometry VCO achieves the sixth largest PFN and the third largest PFTN.

Reference	Technology	Frequency [GHz]	Power	PFN	PTFN
This work Single-Frequency	**SiGe 0.18 μm**	**5.33**	**14mW**	**16.5**	**NA**
This work VCO	**SiGe 0.18 μm**	**5.15**	**21.6mW**	**9.6**	**-12**
[69]	CMOS 0.24 μm	7.3	2.4mW	16.3	4.2
[75]	NA	10	2.93mW	11.5	NA
[73]	CMOS 0.18 μm	12	1.4mW	11.03	-18.4
[74]	CMOS 0.18 μm	5.5	3.6mW	10.4	-2.8
[70]	CMOS 0.25 μm	17	10.5mW	8.75	-12.7
[71]	CMOS 0.25 μm	50	13mW	8.0	-25.1
[72]	CMOS 0.12 μm	50	1mW	5.4	-27.2
[47]	CMOS 0.35 μm	10	35mW	4.9	-13.7

Table 4.3: Oscillators above 4GHz comparison.

4.5 Summary

A new circular-geometry oscillator topology has been presented. It allows the use of slab inductors for high frequency-low phase noise oscillator applications. These inductors present a significantly higher quality factor and self-resonance frequencies when compared to single- and multi-turn spiral inductors for small inductance values required for high frequency operation. A general methodology to suppress the undesired oscillation modes and achieve a stable dc bias point has been devised and its efficacy proven experimentally. This topology is general and can be used to implement oscillators with any number of corners and with a variety of active cores. Two test oscillator have been fabricated as a proof of concept and achieve some of the largest figures of merit among previously published high frequency oscillators.

Chapter 5 *Quadrature Signal Generation*

Quadrature signals are typically required in many receiver and transmitter architectures [76], where the accuracy of such quadrature signals would determine the image rejection [76][77]. In this chapter we will discuss the three main quadrature generation techniques used in integrated applications.

The importance of the in-phase and quadrature signals will be discussed in Section 5.1. In Section 5.2, an overview the challenges of the generation of these signals trough frequency division will be presented. Section 5.3 analyzes the coupling between two identical oscillators to produce quadrature signals. The implication of the strength of this coupling on the phase noise, phase and amplitude accuracy of the quadrature signals are explored and verified experimentally. A design strategy is also devised for optimum coupling of two identical *LC* oscillators for phase noise performance. Polyphase networks can also be used for quadrature generation, Section 5.4 briefly covers the design issues and trade-off between quadrature accuracy and the matching properties of the *RC* components of the filter.

5.1 Introduction

Achieving a large image rejection poses a major challenge towards the full integration of superheterodyne wireless receivers with on-chip circuits. Zero-IF receivers require a moderate image rejection (about 10dB) for a good signal-to-noise ration (SNR) as the image of one half of the channel is the other half of the same channel. However, flicker noise and dc offsets are serious problems in this architecture and usually require the removal of spectral energy of the downconverted signal around dc, and thus, lead to a loss

of signal-to-noise. On the other hand, low-IF and image-reject architectures downconvert the desired signals to frequencies beyond the flicker noise corner. Now, the image frequency is located two times the intermediate frequency, f_{IF}, from the desired channel. Unfortunately, large interferers can exist at that frequency and requires a suppression of up to 80dB. This image channel suppression can be achieved by filtering prior to downconversion and/or by signal cancellation. Unfortunately, it is extremely difficult to build on-chip filters with sufficient selectivity and dynamic range at the frequencies of interest. The practical approach to cancel the image is by mixing quadrature phases of the local oscillation with the RF signal followed by a Hilbert transform as shown in Figure 5.1.

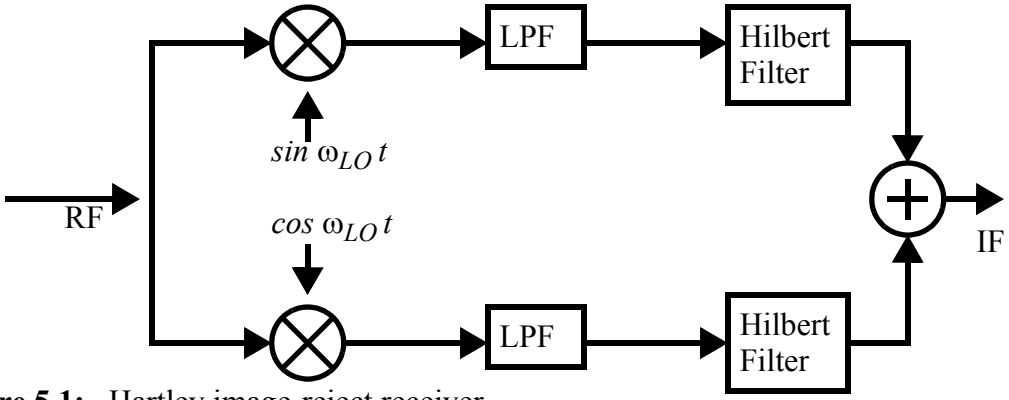


Figure 5.1: Hartley image-reject receiver.

It is noteworthy that a complex representation of the signal follows the Hilbert filter, and after downconversion, the signal and its image lie at the same frequency with complex representation. An extension of the Hartley receiver is the Weaver architecture depicted in Figure 5.2. It uses four mixers with local oscillator signals in quadrature phases. In these

architectures, the ultimate image rejection is limited by the quadrature accuracy of the mixer input phases and the gain matching of the mixers.

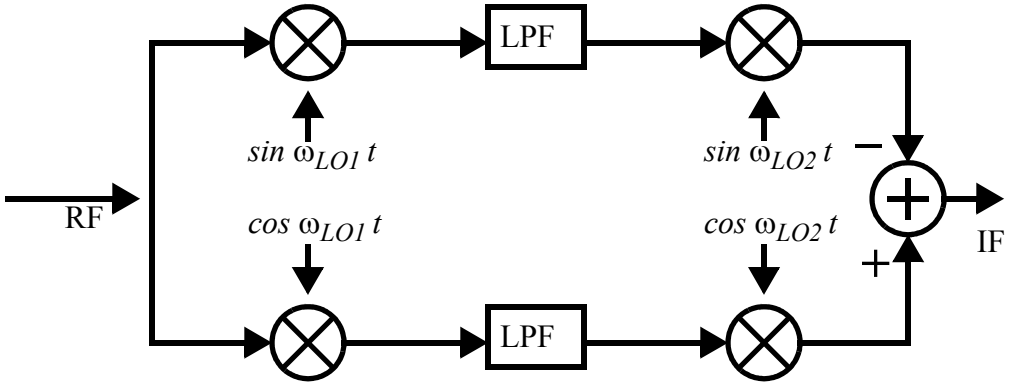


Figure 5.2: Weaver image-reject receiver.

5.2 IQ Generation by Frequency Division

In-phase and quadrature signals can be generated by using a VCO operating at twice the frequency of interest and a divide by two circuit. Figure 5.3a shows this implementation with two master-slave flip-flops. In this scheme, the outputs of a set of divide-by-two flip-flops are triggered by opposite phases of a 50% duty cycle clock, the outputs are in quadrature but at half the clock frequency. Important drawbacks of this scheme are the significant increase of power consumption, an oscillator running at twice the desired output frequency, and the need for accurate 50% duty cycle in the oscillator output. The dependence of the duty cycle translates directly to the quadrature accuracy as can be appreciated in the time diagram shown in Figure 5.3b. The dependency on the duty cycle can be eliminated by running the oscillator at four times the desired frequency ($4 \cdot f_{out}$) and a divide-by-four block, but this imposes yet more stringent demands on the digital divider, specially at high frequencies. At IF frequencies, this is a very popular solution, but for higher signal frequencies, the $4 \cdot f_{out}$ requirement typically exceeds device capabilities.

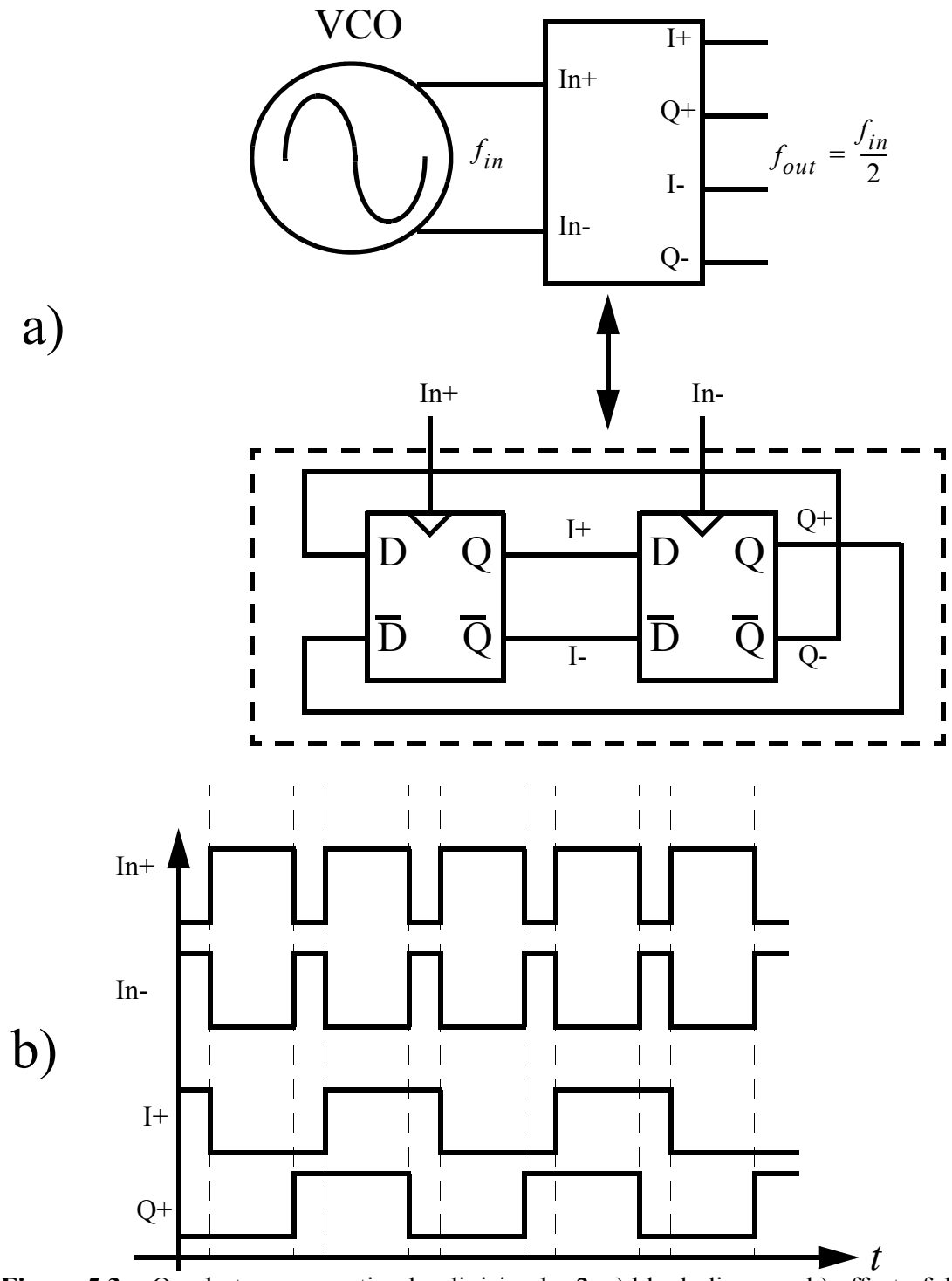


Figure 5.3: Quadrature generation by division by 2, a) block diagram, b) effect of duty cycle mismatch on the quadrature accuracy.

A comparator with an adjustable threshold in front of the divide-by-two can adjust the clock's duty cycle toward highly accurate quadrature outputs; the threshold is computed with a feedback loop which measures the quadrature error [81]. This scheme suffers from a factor of two speed penalty, but is also limited by the accuracy of the quadrature phase measurement. Power consumption, feedback stability and settling time impose additional limitations.

5.3 Quadrature Coupled Oscillators

Two identical oscillators can be coupled in such a way that their outputs are forced to oscillate $90°$ out of phase. Figure 5.4a shows the typical approach to practically couple two NMOS-only cross-coupled oscillators [82]. This configuration has the disadvantage of requiring twice the area and power than that of a single *LC* oscillator.

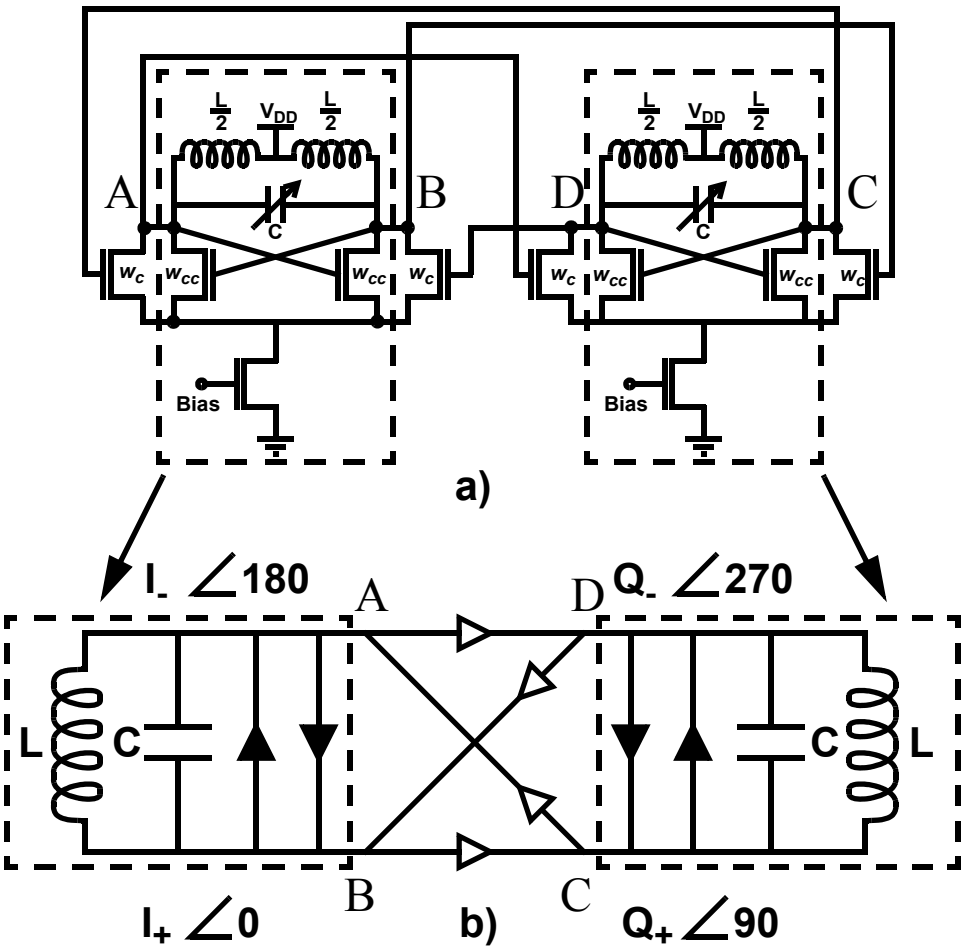


Figure 5.4: Quadrature-coupled LC VCO, a) circuit topology, b) block diagram.

To get some intuition on how this coupling works, Figure 5.4b depicts the block diagram of the circuit shown in Figure 5.4a. The four output nodes, namely, I_+, Q_+, I_- and Q_-, have the same amplitude and frequency but are shifted 90° out of phase, respectively. The solid triangles signify the cross-coupled pair of NMOS transistors, while the hollow triangles denote the coupling transistors between the two oscillators. Under normal operation conditions, the cross-coupled transistors operate fully switching and provide 180° phase shift from input to output (solid triangles, Figure 5.4b). Due to the symmetry of the circuit configuration and as the oscillator would oscillate in the state of equilibrium, the coupling transistors (hollow triangles, Figure 5.4b) operate providing 90° phase shift

between the input to output. In other words, for instance if one assumes that the oscillator on the left hand side is $90° + \Delta$ ahead of the one on the right, one can argue that looking at the mirror image of the oscillator we will see that the left hand side is $90° - \Delta$ ahead. Assuming that both sides are identical, we should have $90° + \Delta = 90° - \Delta$, and thus $\Delta = 0$.

To gain more insight into the system of Figure 5.4, it can be noted that if oscillation exists, the voltages will be purely sinusoidal at one frequency. Therefore, this system can be approximated in frequency domain, as in Figure 5.5.

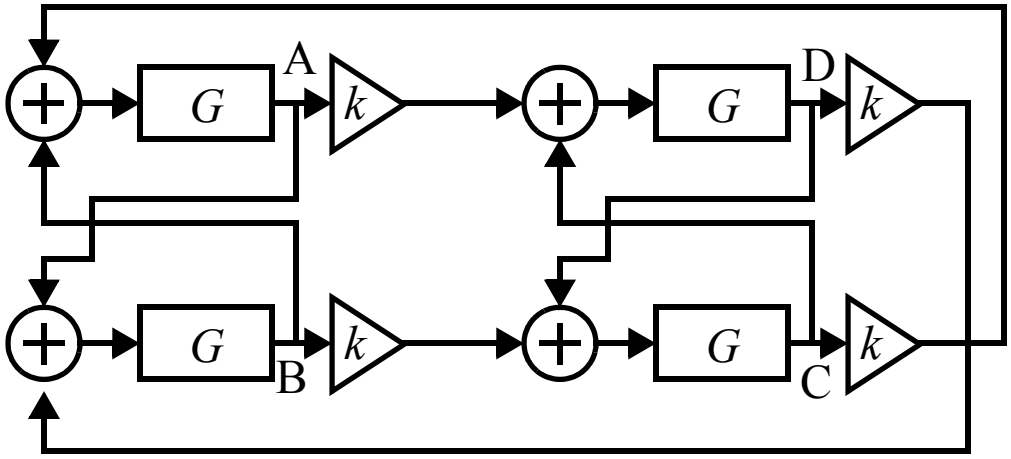


Figure 5.5: Quadrature-coupled oscillator system.

$G(j\omega)$ is the transfer function of the subsystem and k is a real constant that represents the amount of coupling between the two identical oscillators. The constituting equations for this system are as follows:

$$(F_B + k \cdot F_C) \cdot G = F_A \tag{5.1}$$

$$(F_A + k \cdot F_D) \cdot G = F_B \tag{5.2}$$

$$(F_D + k \cdot F_B) \cdot G = F_C \tag{5.3}$$

$$(F_C + k \cdot F_A) \cdot G = F_D \tag{5.4}$$

(5.1) through (5.4) are a set of linear homogeneous equations and can be rewritten in the following form.

$$\begin{bmatrix} -1 & G & k\cdot G & 0 \\ G & -1 & 0 & k\cdot G \\ 0 & k\cdot G & -1 & G \\ k\cdot G & 0 & G & -1 \end{bmatrix} \cdot \begin{bmatrix} F_A \\ F_B \\ F_C \\ F_C \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.5}$$

This system would have a non-trivial solution if and only if the determinant of (5.5) is zero, *i.e.,*

$$1 + 2\cdot G^2 - 4\cdot k^2\cdot G^3 + (1-k^4)\cdot G^4 = 0 \tag{5.6}$$

thus, the roots of (5.6) are as follows:

$$G(j\omega) = \frac{1}{1\pm k}, \frac{-1}{1\pm jk} \tag{5.7}$$

for $k^2 \neq 1$, and

$$G(j\omega) = \frac{1}{2}, \frac{-1\pm j}{2} \tag{5.8}$$

for $k^2 = 1$. The two real roots of G are ruled out as they lead to a solution in which the four output nodes of Figure 5.5 (A, B, C, D) are all in phase.

To gain further intuition, the complex transfer function of (5.7) can be implemented using a simple *RC* circuit model (Figure 5.6). This *RC* circuit can be used to express equations (5.1) through (5.4). Each of these equations correspond to the same order as the indexes of *F*, respectively, as exemplified in Figure 5.5.

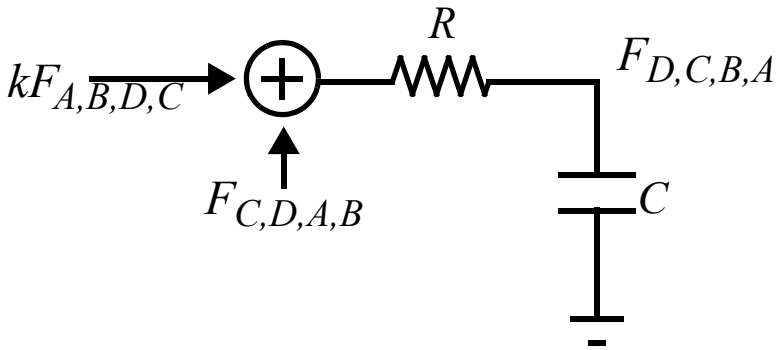


Figure 5.6: *RC* circuit implementation.

The state equations of the system depicted in Figure 5.6 can be expressed in the following form:

$$\frac{d}{dt}F(t) = \frac{1}{RC}AF(t) \tag{5.9}$$

where $F(t) = [F_A(t), F_B(t), F_C(t), F_D(t)]$ and

$$A = \begin{bmatrix} -1 & -1 & -k & 0 \\ -1 & -1 & 0 & -k \\ 0 & -k & -1 & -1 \\ -k & 0 & -1 & -1 \end{bmatrix} \tag{5.10}$$

The matrix A has the eigenvalues $\lambda_{1,2} = -2 \pm k, \pm jk$ and hence, $F(t)$ will be a 4x4 matrix whose elements are a linear combination of $e^{-(k+2)t/(RC)}$, $e^{-(k-2)t/(RC)}$, $\cos\left(\frac{kt}{RC}\right)$, and $\sin\left(\frac{kt}{RC}\right)$. A simple solution can be obtained for the case when the initial condition is $F(0) = [1, 0, 0, 0]^T$, in this case $F(t)$ is as follows:

$$F_A(t) = \frac{1}{4}\left[e^{(k-2)t/(RC)} + e^{-(k+2)t/(RC)} + 2\cos\left(\frac{kt}{RC}\right)\right] \tag{5.11}$$

$$F_B(t) = \frac{1}{4}\left[e^{(k-2)t/(RC)} + e^{-(k+2)t/(RC)} - 2\cos\left(\frac{kt}{RC}\right)\right] \tag{5.12}$$

$$F_C(t) = \frac{1}{4}\left[-e^{(k-2)t/(RC)} + e^{-(k+2)t/(RC)} + 2\sin\left(\frac{kt}{RC}\right)\right] \tag{5.13}$$

$$F_D(t) = \frac{1}{4}\left[-e^{(k-2)t/(RC)} + e^{-(k+2)t/(RC)} - 2\sin\left(\frac{kt}{RC}\right)\right] \tag{5.14}$$

If $0 < |k| < 2$, the exponential terms will decay to zero in the steady state, and the four output signals are a sinusoid, equal in amplitude and $90°$ apart in phase, as expected earlier.

Although this is a particular example, the previous study points us in the direction of evaluating the effect of the coupling transistors in the quadrature *LC* oscillator system of Figure 5.4. For this purpose, the circuit topology of Figure 5.4a is simulated. For this set

of simulations, the VCO is designed to oscillate at 1.8GHz while having more than 20% of frequency tuning and operating at the current limited regime. The inductors have a quality factor of 5. The coupling factor κ is defined as the ratio of the width of the coupling transistor, w_c, to the width of the cross-connected transistor, w_{cc}, *i.e.*, $\kappa = w_c / w_{cc}$.

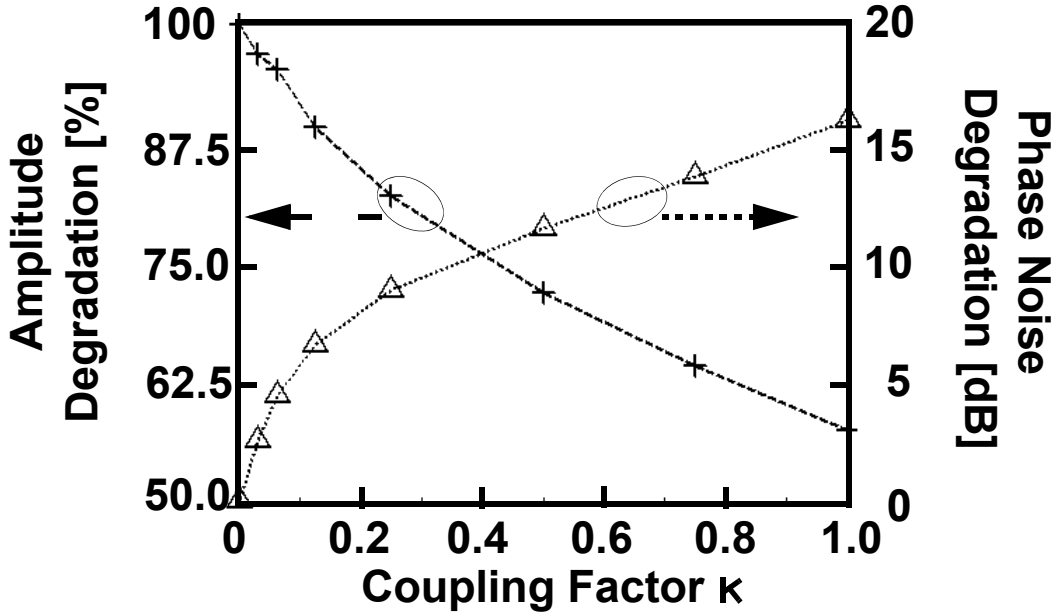


Figure 5.7: Amplitude and phase noise degradation vs. the coupling factor.

If the size of the coupling transistors is on the same order of magnitude as the cross-coupling transistors, their effective g_m would load the tank significantly, reducing the output voltage swing and thus worsening the phase noise. The simulation results showing the *amplitude degradation* versus the coupling factor κ are depicted in Figure 5.7 with the dashed line. Amplitude degradation can be defined as the ratio of the amplitude of the quadrature *LC* oscillator of Figure 5.4a to that of the same oscillator when there is no coupling, *i.e.* $\kappa = 0$. As can be seen, the oscillation amplitude decreases for larger coupling ratios. For instance, the oscillation amplitude is degraded by more than 40% for $\kappa = 1$. The *phase noise degradation* of the oscillator versus κ is also depicted in Figure 5.7 with a dotted line. Phase noise degradation is defined as the excess of phase noise when compared to the oscillator with no coupling, *i.e.* $\kappa = 0$. For this example, the

simulated phase noise is measured at 600KHz offset from a 1.8GHz carrier. As expected, the phase noise is degraded for higher coupling ratios being as much as 16 dB for $\kappa = 1$. It is noteworthy that not only the amplitude reduction of the quadrature *LC* oscillator of Figure 5.4a contributes to the worse phase noise performance for larger coupling ratios, but also the coupling transistors generate noise in proportion to the coupling factor κ. This noise in turn becomes phase noise and accounts for the extra degradation of the phase noise for larger κ. The amount of amplitude and phase noise degradation for a given quadrature *LC* oscillator and a given κ will depend on the effective loading of the coupling transistors to the oscillator tank.

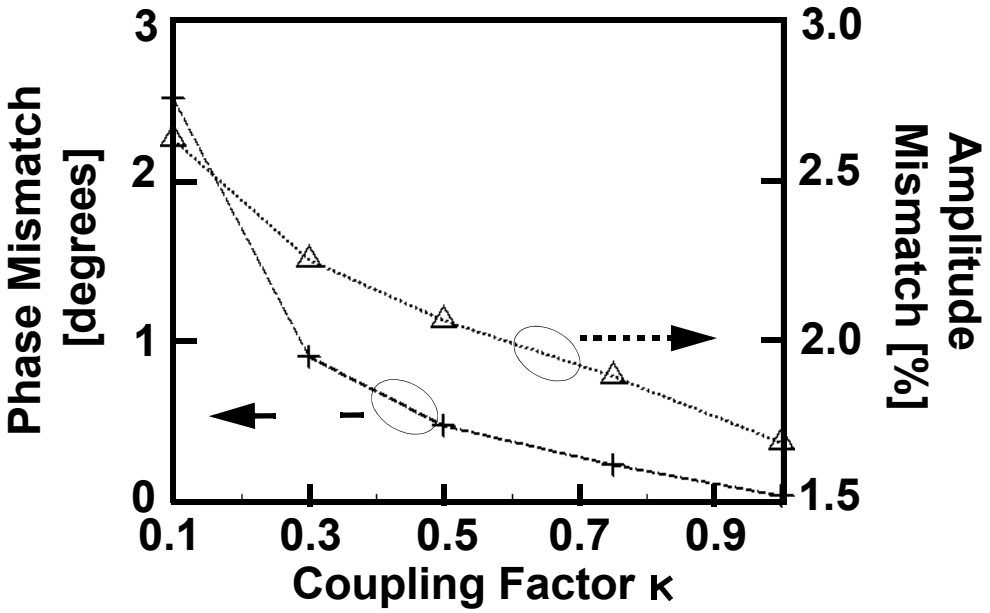


Figure 5.8: Amplitude and phase mismatch vs. the coupling factor for a tank referred capacitor of 2%.

To evaluate the effect of component mismatch on the phase and amplitude accuracy of the quadrature *LC* oscillator of Figure 5.4a, a *tank referred* capacitor is inserted between one of the output nodes of the oscillator and ground. This capacitor is introduced to imitate any unbalanced loading produced by the following stages of the oscillator, such as buffers/amplifiers and mixers, or by any asymmetry in the layout. The capacitance value of the tank referred capacitor corresponds to that of the tank capacitance expressed in

percentage. Thus, a tank referred capacitor of 5% corresponds to an extra loading capacitor whose value is 0.05 times that of the tank capacitance. For the second set of simulations, a tank referred capacitor of 2% is added to one of the outputs of the quadrature *LC* oscillator of Figure 5.4a. The simulation results showing the phase and amplitude mismatch versus the coupling factor, κ, for the quadrature oscillator of Figure 5.4a are depicted in Figure 5.8, with dashed and dotted lines, respectively. It can easily be seen that the phase and amplitude accuracy of the quadrature outputs is compromised for smaller coupling factors, and this degradation is inversely proportional to κ.

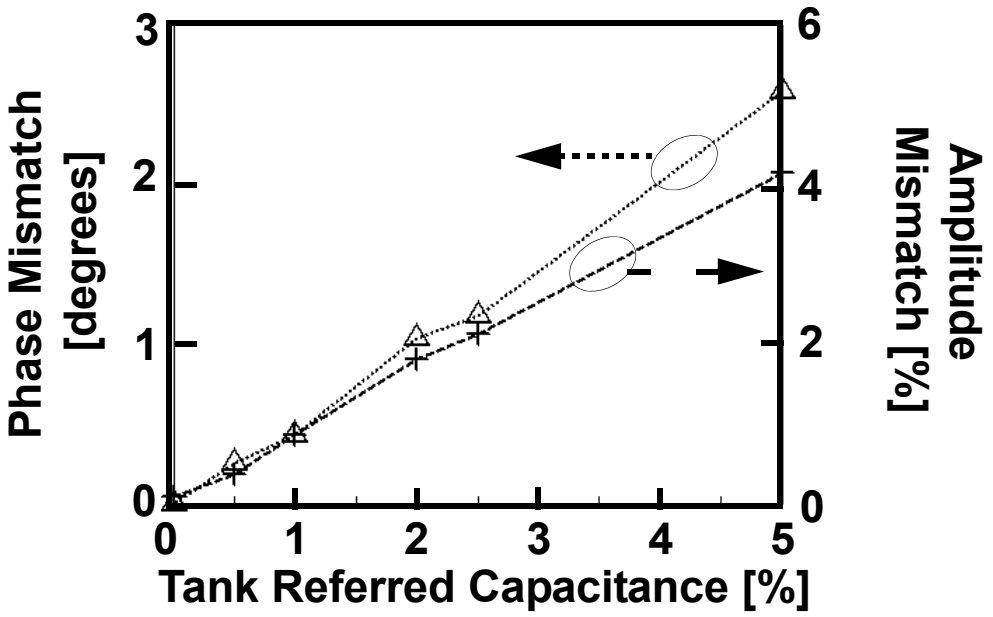


Figure 5.9: Amplitude and phase mismatch vs. the tank referred capacitor for $\kappa = 0.3$.

To visualize this trade off further, Figure 5.9 depicts the simulation results showing the phase and amplitude mismatch for different values of a tank referred capacitor for the oscillator of Figure 5.4a with a coupling factor of $\kappa = 0.3$ with dashed and dotted lines, respectively. As expected, the phase and amplitude accuracy of the quadrature *LC* oscillator of Figure 5.4a is degraded for larger capacitance unbalance. However, it is

noteworthy that for a tank referred capacitor as high as 2% of the tank capacitance, the phase mismatch is smaller than $1°$ and the amplitude mismatch is less than 2%, as shown in Figure 5.9.

Quadrature *LC* oscillators also suffer from mismatches of other components due to process variations such as transistor gain and tank inductance value. However, due to the nonlinear behavior and gain compression mechanisms of the oscillator, the transistor mismatch has a smaller effect on the accuracy of the quadrature signals. Also, uncertainties in the inductance value can be small as it is determined by lithographic processes which are quite accurate in nowadays process technologies.

Based on these arguments, a design strategy can be summarized for improving the amplitude and phase accuracy for the quadrature *LC* oscillator of Figure 5.9 as follows:

1) Find the maximum tank capacitance that satisfies the oscillator design specifications, such as frequency tuning, tank amplitude and start up. This will decrease the effect of capacitive mismatch on the amplitude and phase accuracy of the quadrature signals.

2) Compensate any asymmetric loading on the nodes of the quadrature oscillator. Layout the oscillator with a high degree of symmetry while balancing any extra interconnecting capacitance. Also, equalize the length and the differential capacitance of the connecting metal lines of the quadrature *LC* oscillator.

If the phase noise performance is of primary concern, decrease the ratio of the coupling transistors. However, this will increase the amplitude and phase mismatch of the quadrature outputs limiting its practical use to compensating any unbalanced capacitances.

Although the arguments presented in this section were limited to the coupling of the NMOS-only cross-coupled VCO, they are equally applicable to the complementary cross-coupled oscillator [25] and the differential noise-shifting Colpitts oscillator [87] using similar lines of argument. It is noteworthy that the first design strategy is in good

agreement with the optimization presented in Chapter 3 and in [24] for phase noise performance of integrated *LC* VCOs.

5.3.1 Experimental Results

A test chip implementing the quadrature NMOS-only cross-coupled VCO of Figure 5.4a, was fabricated in a 0.18μm BiCMOS process technology using the NMOS transistors only. For this design, the oscillator is designed for a center frequency of 1.8GHz and NMOS transistors operating in inversion mode are used as varactors. The design strategies and methodologies presented in Chapter 3 were closely followed in the design of this oscillator.

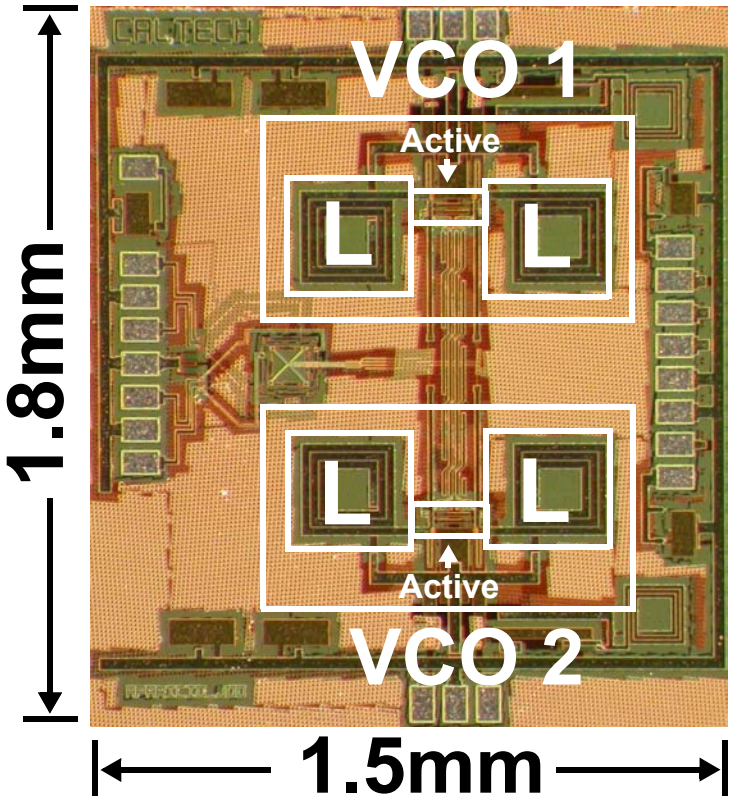


Figure 5.10: Quadrature NMOS-only cross-coupled oscillator die photo.

The implemented quadrature *LC* VCO is aimed to evaluate the effect of the relative coupling on the phase noise of the quadrature oscillator. Therefore, very special care is taken to layout the VCO. Figure 5.10 shows the quadrature *LC* VCO test chip photograph.

The quadrature oscillator draws a total of 4mA of current from a 1V supply and operates from 1.72GHz to 2.02GHz. These correspond to a current consumption of 2mA per *LC* oscillator, a center frequency of 1.87GHz and a tuning range of 16%. The voltage to frequency transfer function of the oscillator is depicted in Figure 5.11.

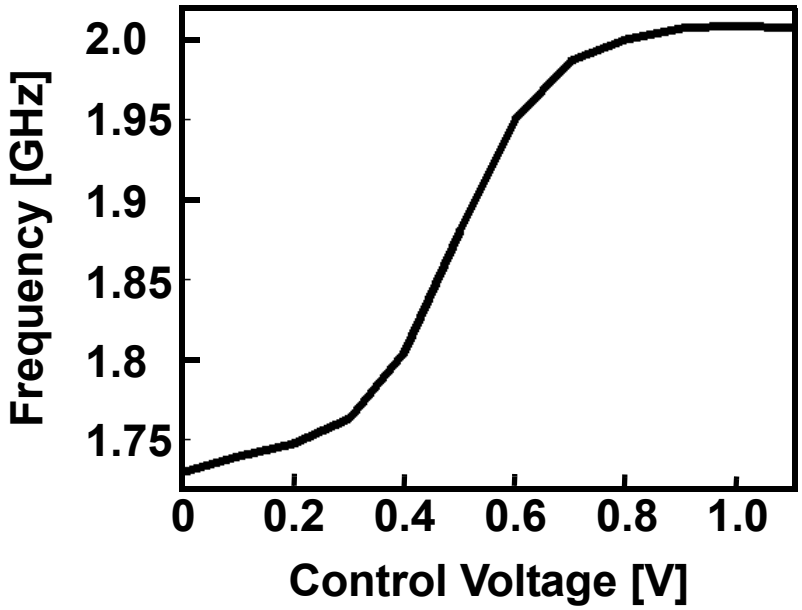


Figure 5.11: Quadrature NMOS-only cross-coupled oscillator frequency tuning.

Phase noise is measured using an NTS-1000 phase noise analyzer with a DRC 14000 down converter as well as an HP8563 spectrum analyzer with phase noise measurement utility. The quadrature *LC* oscillator shows a phase noise of -100.7 dBc/Hz at 600Khz offset from a 1.72GHz carrier for a coupling factor of $\kappa = 0.35$. To evaluate the effect of the relative coupling of the oscillator on its phase noise, the coupling factor can be modified to $\kappa = 0.05$ by means of a laser trim. The measured phase noise for a coupling factor $\kappa = 0.05$ is -113.5 dBc/Hz at 600Khz offset from a 1.72GHz carrier. Figure 5.12 shows a plot of phase noise versus the offset frequency. It is shown experimentally that the

phase noise is enhanced by 12.7dB by having a smaller coupling factor κ while maintaining the same supply voltage and bias current.

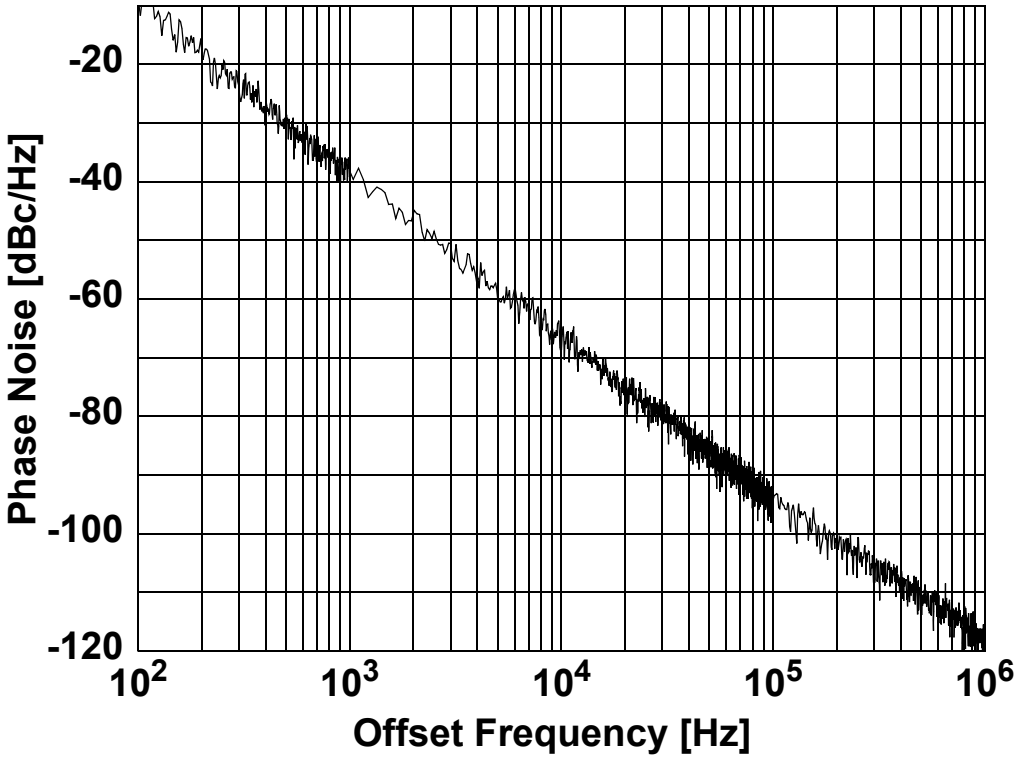


Figure 5.12: Measure phase noise vs. offset frequency at 1.72GHz.

To estimate the phase accuracy of the VCOs quadrature outputs, a polyphase network is also integrated on the same chip. The polyphase schematic and terminal interconnections are depicted in Figure 5.13.

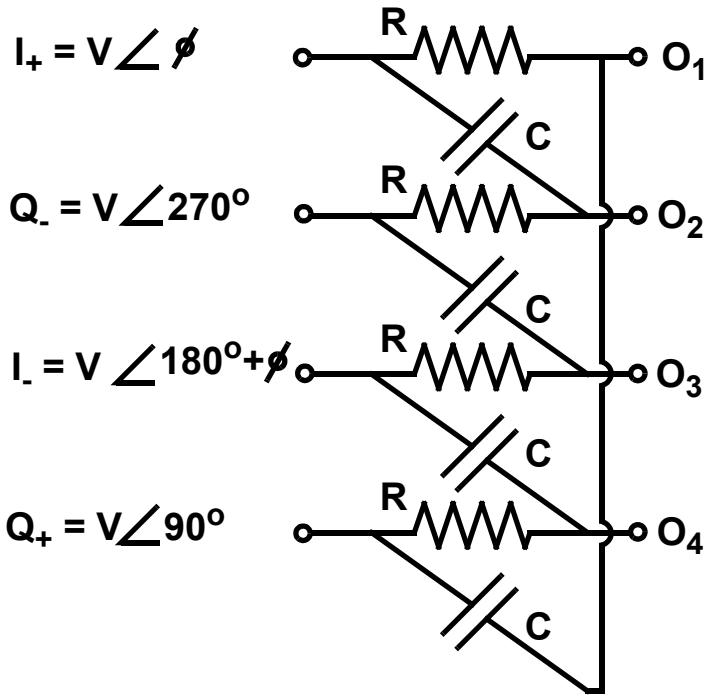


Figure 5.13: RC polyphase network.

If the inputs to the polyphase are in quadrature and have an amplitude V, but with a phase mismatch of ϕ degrees, the magnitude of *any* output of the polyphase at $2\pi f = 1/RC$ can be shown to be:

$$\left|O_{1-4}\right| = V \cdot 2\sqrt{2}\left|\sin\frac{\phi}{2}\right| \tag{6}$$

Therefore, the phase error can be extrapolated by measuring the output voltage amplitude of the polyphase filter. Buffers are required to prevent excessive loading to the polyphase and drive the 50Ω load of the measurement equipment. Microwave coplanar probes are used to probe the RF output pads of the buffers. An HP 8563E spectrum analyzer is used to measure the output power. Using the simulated values for the buffers gain, the extrapolated phase error ϕ is found to be less than $1°$ degree in both cases.

5.4 Polyphase Filter Quadrature Signal Generation

Polyphase networks can be used to generate balanced quadrature signals from a differential input. A polyphase filter is a *RC-CR* network that in the ideal case, shifts its outputs by ±90° degrees with respect to one another. Figure 5.14 shows this configuration. Unfortunately, this phase shift occurs only in a narrow frequency range. For instance, in the single stage polyphase of Figure 5.14, a frequency variation of ±1.7% translates to a phase variation of ±1°. Moreover, non-sinusoid input waveforms contain odd harmonics. These harmonics will pass through the polyphase with completely different gain and phase than the fundamental distorting the duty cycle of the output waveform. Although cascading several stages of stagger-tuned polyphase filters can alleviate these problems [80], unwanted additional loss adds quickly with cascading, requiring amplifiers/buffers to compensate for loss of the filter, at the extra penalty of higher power consumption. Also, additional loss translates to higher noise that can corrupt the signal.

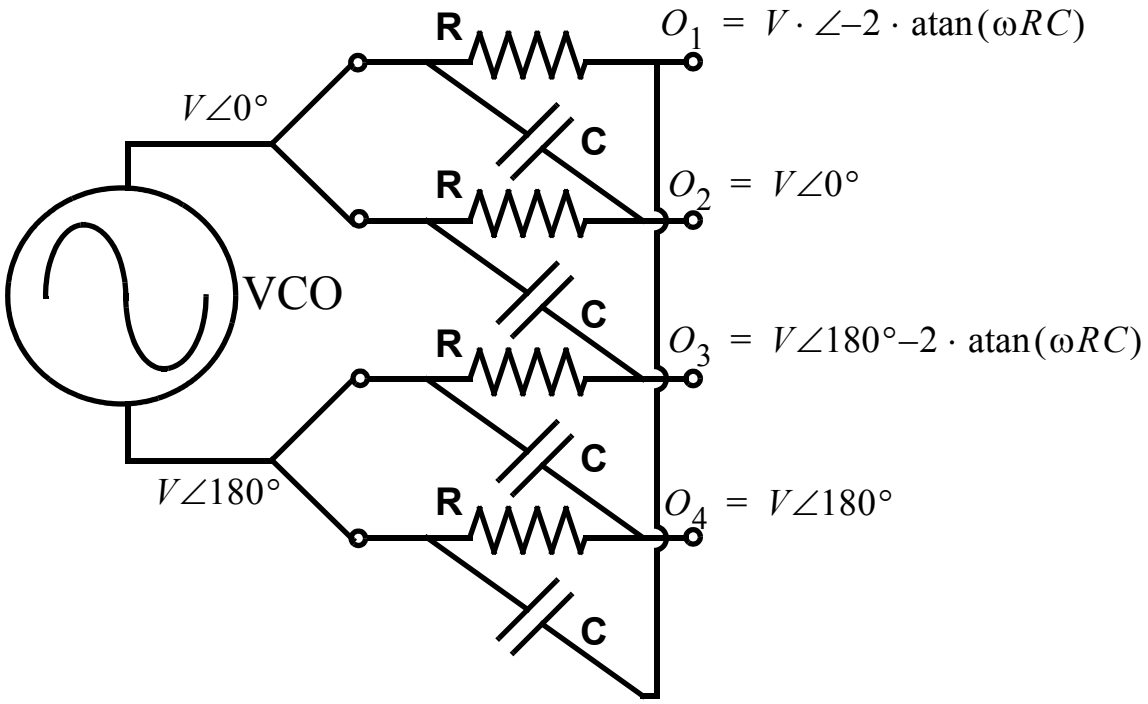


Figure 5.14: Polyphase filter used as quadrature signal generator.

Another drawback of polyphase filters is that the accuracy of the in phase and quadrature signals is strongly dependent on the on-chip component matching. Assuming a relative resistor mismatch of α and capacitor mismatch of β, the phase shift ϕ in the vicinity of $\omega = 1/RC$ can be expressed as follows:

$$\begin{aligned}\phi &= \frac{\pi}{2} - [\operatorname{atan}\{R(1+\alpha)\cdot C(1+\beta)\cdot\omega\} - \operatorname{atan}\{RC\omega\}] \\ &= \frac{\pi}{2} - \operatorname{atan}\frac{RC\omega\cdot(1+\alpha)(1+\beta) - RC\omega}{1+(RC\omega)^2\cdot(1+\alpha)(1+\beta)} \\ &\approx \frac{\pi}{2} - \operatorname{atan}\frac{\alpha+\beta}{2} \\ &\approx \frac{\pi}{2} - \frac{\alpha+\beta}{2}\end{aligned} \tag{5.1}$$

Thus, for a resistor and capacitor matching of 1%, the phase shift would be $0.6°$. Resistors matching can be increased easily with larger area for a given resistor value [83]. This is mainly because the resistance value is proportional to the resistivity of the material, ρ, and the resistor length, l, and inversely proportional to the resistor width, w, *i.e.* $R = \rho\cdot\frac{l}{w}$. Therefore, for a given resistor value and material resistivity, a higher matching can be achieved by increasing l and w by the same factor. On the other hand, integrated capacitors suffer from the inability to trade area with capacitance density to achieve better matching for a given capacitor value. Although common-centroid structures can alleviate this problem to a certain extend [84], resistors achieve better matching and the dominant source of performance degradation is the capacitor matching. These issues will be extensively studied in the next Chapter.

5.5 Summary

An overview of the different on-chip quadrature signal generation methods has been presented. The trade-off between the amount of coupling, phase noise, amplitude matching and the in-phase and quadrature signal accuracy for the *LC* quadrature coupled

oscillator topology has been shown. A design strategy is also devised aimed to enhancing the phase noise performance of quadrature *LC* oscillators.

Chapter 6

Capacity Limits and Matching Properties of Integrated Capacitors

In this chapter, theoretical limits for the capacitance density of integrated capacitors with combined lateral and vertical field components are derived. These limits are used to investigate the efficiency of various capacitive structures such as lateral flux and quasi-fractal capacitors. This study leads to two new capacitor structures with high lateral-field efficiencies. These new capacitors demonstrate larger capacities, superior matching properties, tighter tolerances, and higher self-resonance frequencies than the standard horizontal parallel plate and previously reported lateral-field capacitors, while maintaining comparable quality factors. These superior qualities are verified by simulation and experimental results.

In Section 6.1, the desired qualities of integrated capacitors are introduced. Section 6.2 illustrates some of the improvements in other properties of integrated capacitors, due to higher capacitance density. It is shown in Section 6.3 that the density of any arbitrary capacitor can be decomposed as the sum of the individual capacitance contributions of the lateral and vertical electric field components. This decomposition will be used to derive new theoretical limits for the capacitance density of integrated capacitors. These theoretical limits lead to two new capacitor structures introduced in Section 6.4. These new capacitors demonstrate superior densities, matching, tolerances, and self-resonance frequencies when compared to previously reported lateral-field and quasi-fractal capacitors, while maintaining a comparable quality factor. The superior capacitance density of the new structures will be corroborated in Section 6.5. Experimental results verifying the superior area efficiency, higher self-resonance frequency, tighter tolerance, and better matching properties of these new capacitors are presented in Section 6.6. In the end, a summary will be given in Section 6.7.

6.1 Introduction

Capacitors are essential components in integrated circuits, such as sample and holds, analog-to-digital (A/D) and digital-to-analog (D/A) converters, switched-capacitor and continuous-time filters, as well as many radio frequency (RF) building blocks. In many of these applications, capacitors consume a large fraction of the chip area. Therefore, capacitors with higher capacitance density are very desirable. In analog applications the other desired properties for capacitors are close matching of adjacent capacitors, linearity, small bottom-plate capacitor, and the absolute accuracy of the value (*i.e.*, tolerance). In RF applications, it is essential for the capacitors to have self-resonance frequencies well in excess of the frequency of interest and large quality factors Q. Excellent matching and tolerance properties would translate to enhanced performance in RF circuits such as polyphase filters or high accuracy and repeatability in the center frequency of resonant networks, respectively. Good linearity and large breakdown voltage are the other two desired properties for a good RF capacitor.

Several approaches have been taken to improve the area efficiency of capacitors. Nonlinear capacitors with high capacitance density such as junction or gate oxide capacitors have been used for a long time in applications where the linearity, breakdown voltage, and the quality factor, Q, are not important. Unfortunately, these capacitors need a dc bias and are strongly process and temperature dependent. Thus, in high precision

circuits, such as data converters, their use is limited to bypass and coupling capacitors, or varactors in RF circuits.

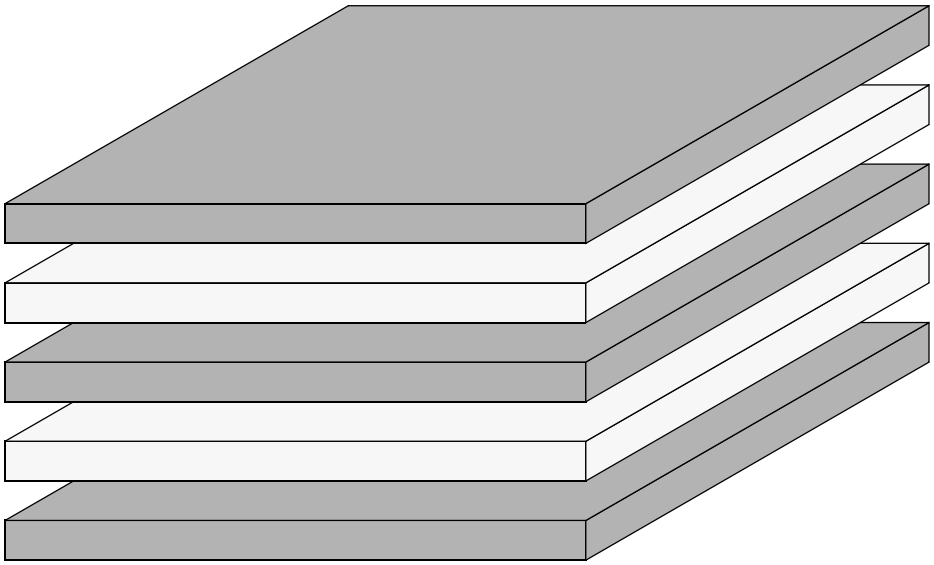


Figure 6.1: *Parallel Plate* capacitor.

On the other hand, metal-to-metal and metal-to-poly capacitors have very good linearity and quality factors. However, they suffer from a low capacitance density which mainly arises from the large metal-to-metal or metal-to-poly vertical spacing that determines the capacitance in the multiple parallel plate structure of Figure 6.1. Unfortunately, in today's process technologies, this vertical spacing does not shrink as fast as the lateral separation to avoid excessive crosstalk between the digital metal lines in different layers; Thus, the parallel plate capacitors consume a larger fractional die area. Although an extra processing step to deposit a thin layer of insulator between two metal or poly layers can mitigate this problem to some extent [89], this extra step is not available in many of the standard silicon-based technologies and often suffer from low breakdown voltages. Even if such special capacitor layers were available, the parallel plate structure does not necessarily result in the highest possible capacitance density, as will be shown later in this chapter.

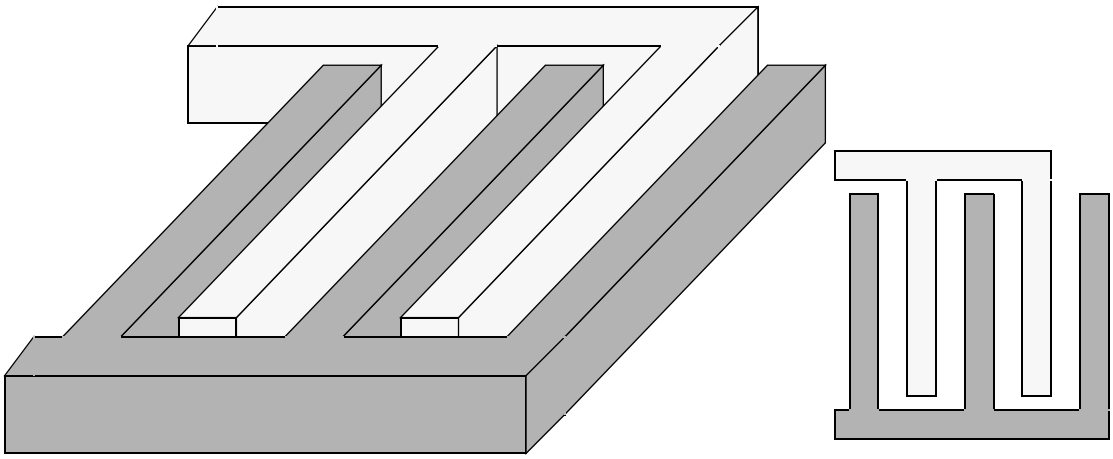


Figure 6.2: *Parallel Wires* configuration.

The capacitance density can be improved by exploiting both lateral and vertical electric field components. A well-known example of such structures is the interdigitated or *Parallel Wires* (*PW*) structure shown in Figure 6.2 [90]-[94]. Recently, several new structures, such as *quasi-fractal* and *woven* structures were suggested as methods of obtaining higher capacitance per unit area [93]. These structures essentially demonstrate the same linearity as parallel plate metal-to-metal and metal-to-poly capacitors and but with higher capacitance densities. They also provide lower bottom-plate capacitance since more field lines terminate on the adjacent metal lines as opposed to the substrate.

Despite these advantages, lateral-flux and quasi-fractal capacitors have not been widely used in the signal path of analog and RF circuits, as predicting their absolute value can be complicated and time-consuming. Also, it is not clear if they are always advantageous over the more regular structures such as the *Parallel Wires* structure shown in Figure 6.2. This chapter addresses some of these issues by focusing on the fundamental properties of the capacitance densities of integrated capacitors.

6.2 The Effect of the Density on Other Capacitor Properties

A higher capacitance density and hence a smaller physical size for a given capacitance will automatically result in a few important improvements in other properties of the capacitor. This higher capacitance density can be achieved in many different ways, such as using a material with higher dielectric constant [89] or using the lateral field components [90]-[96]. For a given capacitor value, smaller physical dimensions will result in a smaller series inductor, since the average ac current path is shorter. Hence, a higher self-resonance frequency can be obtained. Also a smaller area usually translates to shorter metal lengths which in turn result in a smaller series resistance and therefore, a higher quality factor Q. The bottom-plate capacitor also shrinks automatically in a capacitor with a smaller area due to the smaller area of the bottom plate itself. On the other hand, it is believed that a capacitor with a smaller size usually results in a larger fractional variations in the exact value of the capacitor. We will investigate the validity of these statements experimentally in Section 6.6.

It has been proposed to use lateral field components to enhance the capacity of the standard parallel plate structure shown in Figure 6.1 [90]-[96]. Lateral electric fields are particularly useful as the minimum lateral spacing of metal layers shrinks quickly with process scaling, while the vertical spacing does not scale down as fast. Inter-digitated structures similar to those shown in Figure 6.2 have been proposed to enhance the density and lower the bottom plate capacitance [90]-[94]. These structures combine the lateral and the vertical field components very tightly. This has an undesirable effect on the matching properties of the capacitor, as will be demonstrated later in this paper, and thus should be avoided.

Increasing the periphery of a lateral field capacitor has been suggested as a means to enhance the capacitance density [93]. Quasi-fractal structures have been considered as one such alternative. Unfortunately, these structures are time consuming to generate.

Furthermore, they are difficult to predict and simulate in a time efficient manner. They also suffer from the same strong coupling between the vertical and lateral field components which can degrade their matching and tolerance as will be discussed later.

From these different approaches to capacitance optimization, it is not clear which structure results in the best capacitors. Therefore, it is essential to form a deeper understanding of the underlying capacity limits for integrated capacitors to be able to identify the best capacitive structure for any given application. We study these limits in the following section.

6.3 Capacity Limits

To gain more insight into the trade offs in using the lateral and vertical field components, we now set the basis for the capacitance decomposition, starting from the relationships between the capacitance and the electric field in three dimensions. This decomposition leads to theoretical upper bounds on the maximum capacitance of rectangular (*Manhattan*) structures. This can be done by noting that the total electrostatic energy, U_E, in a capacitor, C, is given by

$$U_E = \frac{C \cdot \Delta V^2}{2} \tag{6.1}$$

where ΔV is the voltage drop across its two terminals. The capacitance of an arbitrary structure can be calculated by integrating the electrostatic energy density, u, over the entire dielectric volume to obtain the total stored electrostatic energy, U_E, for a given voltage drop, ΔV, between the two terminals of the capacitor, *i.e.*,

$$C = \frac{2 \cdot U_E}{\Delta V^2} = \frac{2}{\Delta V^2} \int_{Vol} u(\boldsymbol{r}) dv \tag{6.2}$$

where $\boldsymbol{r}$ is the position vector and dv is the differential unit of volume. For an isotropic dielectric material, the electrostatic energy density is given by

$$u(\boldsymbol{r}) = \frac{\boldsymbol{E}(\boldsymbol{r}) \cdot \boldsymbol{D}(\boldsymbol{r})}{2} = \frac{\varepsilon_r \varepsilon_o}{2} \boldsymbol{E}^2(\boldsymbol{r})$$
$$= \frac{\varepsilon_r \varepsilon_o}{2} [E_x^2(\boldsymbol{r}) + E_y^2(\boldsymbol{r}) + E_z^2(\boldsymbol{r})] = u_x(\boldsymbol{r}) + u_y(\boldsymbol{r}) + u_z(\boldsymbol{r}) \tag{6.3}$$

where $\boldsymbol{E}$ and $\boldsymbol{D}$ are the electric and displacement vectors, ε_o is the permittivity of free space, ε_r is the relative permittivity of the dielectric, and u_x, u_y, and u_z are the electrostatic energy densities due to the electric field components along the three cartesian axes, namely, E_x, E_y, and E_z, respectively. Therefore, the density (capacitance per unit volume) can be calculated by integrating the sum of the three electrostatic field energy density components over the dielectric volume, *i.e.,*

$$c = \frac{C}{Vol} = \frac{1}{Vol} \cdot \frac{2}{\Delta V^2} \left[\int_{Vol} u_x(\boldsymbol{r}) dv + \int_{Vol} u_y(\boldsymbol{r}) dv + \int_{Vol} u_z(\boldsymbol{r}) dv \right] = c_x + c_y + c_z \tag{6.4}$$

where c is the capacitance density of the structure (in Farad per cubic meter) and c_x, c_y, and c_z are the capacitance densities due to the electric field components E_x, E_y, and E_z, respectively.

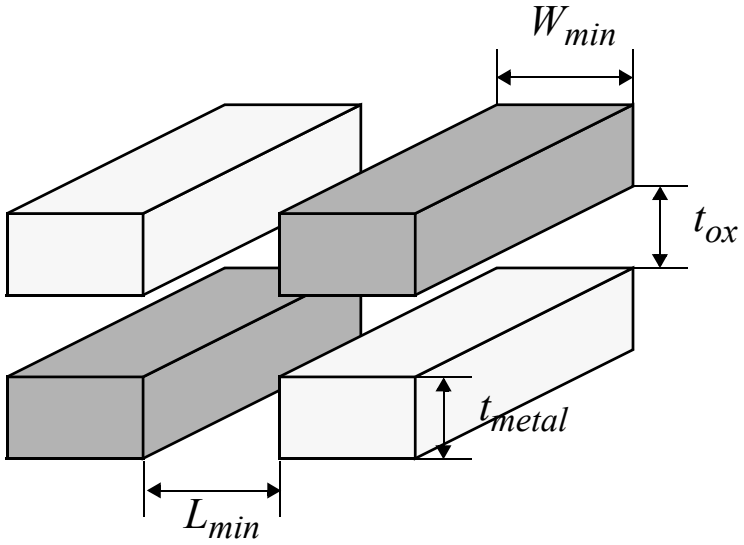


Figure 6.3: Dimensions of the metal lines.

As mentioned earlier, we are interested in maximizing the capacitance density, c, for integrated capacitor structures. Let us consider a process technology with a minimum

lateral spacing of L_{min}, minimum metal width of W_{min}, a vertical spacing between two adjacent metal layers, t_{ox}, and a metal thickness, t_{metal}, as shown in Figure 6.3. We would like to determine the maximum achievable capacitance density, c, for such process technology.

The total capacitance density, c, cannot exceed the sum of the maximums of its individual components, namely, $c_{x,max}$, $c_{y,max}$, and $c_{z,max}$. In other words, we have to maximize the capacitance density due to each component of the electric field separately, to obtain an upper bound on the density.

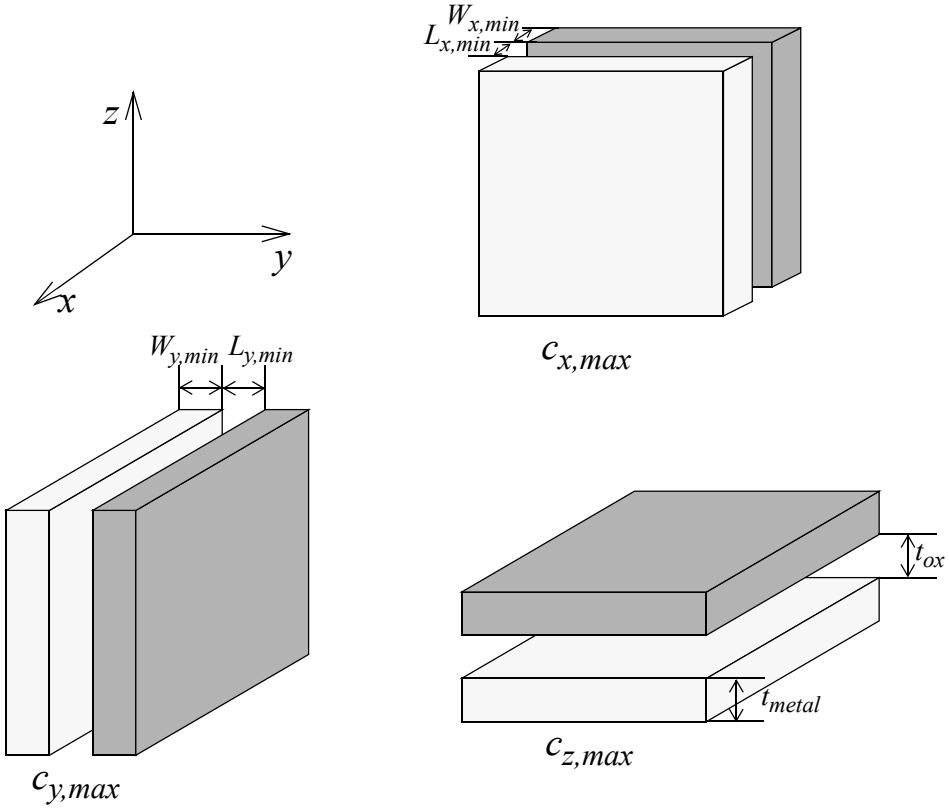


Figure 6.4: *Parallel Plate* structures normal to the cartesian axis.

We can maximize the capacitance contribution of the electric field along the x axis, c_x, (with no constraint on the contributions of other field components) by using a parallel plate structure with minimum plate width, $W_{x,min}$, and minimum spacing, $L_{x,min}$, perpendicular to the x axis. The capacitive components along the y, and z axes can be

maximized in a similar fashion by using minimum spacing and minimum width parallel plate structures normal to these axes, as shown in Figure 6.4. Therefore, an upper bound on the total capacitance density can be obtained by adding the individual maximums of the capacitance density components, *i.e.,*

$$c_{max} = c_{x,max} + c_{y,max} + c_{z,max}$$
$$= \varepsilon_r \varepsilon_o \left[\frac{1}{L_{x,min}(L_{x,min} + W_{x,min})} + \frac{1}{L_{y,min}(L_{y,min} + W_{y,min})} + \frac{1}{t_{ox}(t_{ox} + t_{metal})} \right] \quad (6.5)$$

where $L_{x,min}$, $L_{y,min}$, $W_{x,min}$, and $W_{y,min}$ represent the minimum lateral spacing and metal width along the x and y axis, respectively. Equation (6.5) reduces to

$$c_{max} = \varepsilon_r \varepsilon_o \left[\frac{2}{L_{min}(L_{min} + W_{min})} + \frac{1}{t_{ox}(t_{ox} + t_{metal})} \right] \quad (6.6)$$

for $L_{x,min} = L_{y,min} \equiv L_{min}$ and $W_{x,min} = W_{y,min} \equiv W_{min}$, which is often the case. This is a capacitance per unit volume, and can be easily translated to capacitance per unit area for a known number of metal layers. This maximum in the capacitance density will be referred to as *Theoretical Limit 1 (TL1)*.

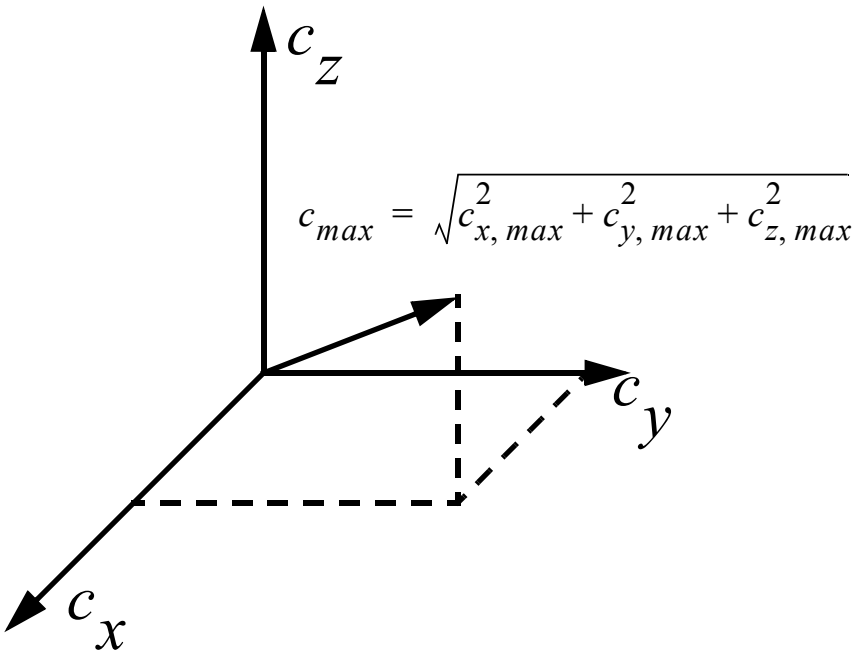


Figure 6.5: Ortho-normal decomposition into lateral and vertical parallel plates.

Although the horizontal and vertical parallel plate capacitor structures of Figure 6.4 have the maximum horizontal and vertical field usage, respectively, they cannot be implemented in the same spatial location simultaneously. This makes it impossible to achieve the maximum electric field usage in the *x*, *y*, and *z* dimensions at the same time, and therefore (6.5), while being correct, is too conservative. The orthogonality of the electric field components implies that the horizontal and vertical parallel plate capacitance densities, c_x, c_y, and c_z *may* form an orthogonal basis for decomposition of capacitance densities as visualized in Figure 6.5. This orthogonal decomposition can be used to obtain a new tighter upper bound for the capacitance density of structures with rectangular (*Manhattan*) boundaries. Noting that the maximum capacitance is given by the magnitude of the vector sum of $c_{x,max}$, $c_{y,max}$, and $c_{z,max}$ (Figure 6.5), we hypothesize that the maximum capacitance density for any given process technology will be given by:

$$c_{max} = \sqrt{c_{x,max}^2 + c_{y,max}^2 + c_{z,max}^2}$$
$$= \varepsilon_o \varepsilon_r \sqrt{\frac{2}{L_{min}^2 (L_{min} + W_{min})^2} + \frac{1}{t_{ox}^2 (t_{ox} + t_{metal})^2}} \quad (6.7)$$

for $L_{x,min} = L_{y,min} \equiv L_{min}$ and $W_{x,min} = W_{y,min} \equiv W_{min}$. The verification of the validity of this hypothesis through simulations will be done shortly.

These theoretical limits can be very helpful for integrated circuit designers, as they set an upper bound for the minimum attainable die area for a given value of capacitance and for a specific process technology. In practice, for a given capacitive structure, c_x, c_y, and c_z are correlated and cannot be maximized all at the same time, therefore, the ratios of the capacitance density of any given structure to these theoretical limits can be defined as figures of merit for the capacitor of interest and used for comparison of various structures.

6.4 Purely-Lateral Field Capacitive Structures

The theoretical limits shown in (6.6) and (6.7) demonstrates an inverse square law dependence on the minimum lateral and vertical dimensions of the process technology. In today's standard process technologies, the minimum lateral dimensions, L_{min} and W_{min}, are smaller than the vertical dimensions, t_{ox} and t_{metal}. Therefore, in properly designed capacitors the lateral component of the capacitance density should be the dominant contributor to the overall density. Furthermore, this maximization of the lateral field component leads to further improvements in the density with process technology advancements. Additionally, the processes used in the back-end metallization allow the

lateral dimensions to be controlled more accurate and repeatable (*e.g.,* lithography and etching) when compared to the vertical dimensions (*e.g.,* deposition).

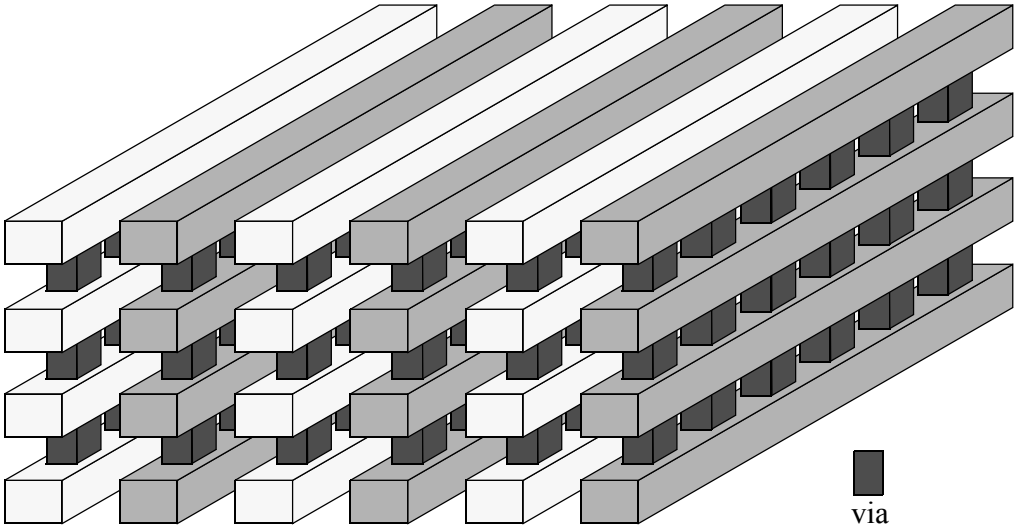


Figure 6.6: *Vertical Parallel Plates* structure.

Therefore, (6.6) and (6.7) directs us in the direction of structures with purely lateral capacitance component and no vertical component. Figure 6.6 shows the first of these structures, called *Vertical Parallel Plates*, or *VPP* for short [95][96]. It consists of metal slabs connected vertically using multiple vias to form vertical plates. This structure takes full advantage of the lateral dimension scaling. Note that different shadings are used to distinguish the two terminals of the capacitor throughout this paper.

It is noteworthy that while each via may present a reasonably large series resistance, a large number of them are connected in parallel in each plate. This large number of parallel small capacitors will reduce the series resistance significantly, which in turn, will reduce the loss of the structure. In other words, very little ac current flows through each via, reducing the effective series resistance of the capacitor. This statement will be verified experimentally in Section 6.6.

Although the fabrication of the *VPP* structure relies on stacked vias which may not be available in all process technologies, close approximations to this structure can be fabricated by interleaving vias. Also, long electromagnetic capacitance simulations are

rather unnecessary as the capacitance of the *VPP* structure can be predicted using simple expressions for parallel plate structures with fringing [97].

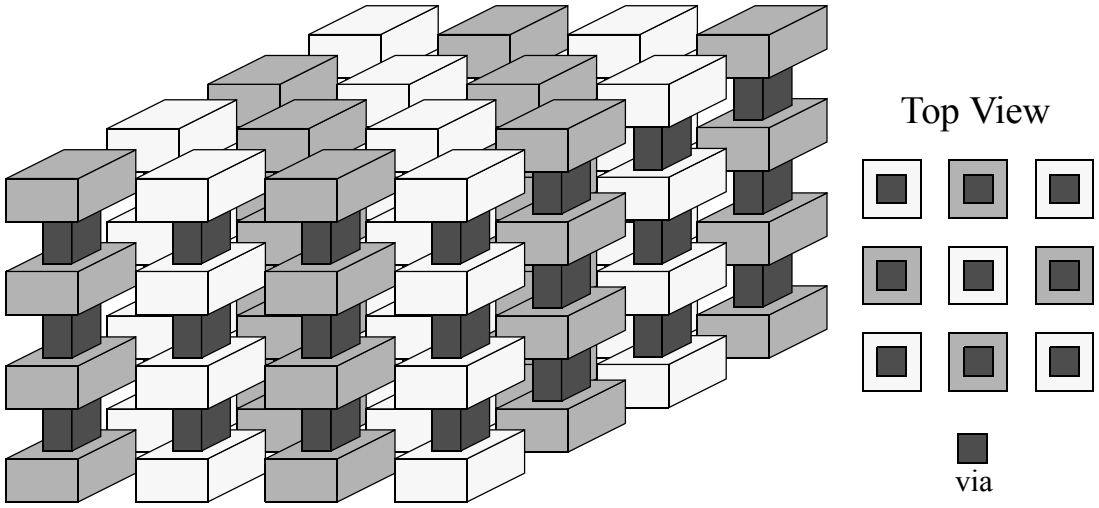


Figure 6.7: *Vertical Bars* structure.

We can take this maximization one step further by using both lateral dimensions in the *Vertical Bars* structure, or *VB* for short, shown in Figure 6.7 [95][96]. It consists of vertical bars made out of metal squares and vias. The length of the bars is limited by the number and thickness of metal layers. This structure utilizes the electric field in both lateral dimensions and has even higher capacitance density than the *VPP* structure. In practice, the interconnection of the bars to the terminals of the capacitor require the use of at least one metal layer, reducing the effective volume of the capacitor. Therefore, in certain process technologies the overall capacitance of the *VB* structure will be smaller than that of the *VPP*.

The *VB* structure can show a larger series resistance compared to the *VPP* capacitor. However, the series resistance of the *VB* structure is mainly determined by the via resistance. Again a large number of small capacitors in parallel form the total capacitance and hence the overall series resistance is the parallel combination of these resistors, which will be much smaller than an individual via. The choice between *VPP* and *VB* will depend on the application. A compromise between the higher quality factor of the *VPP* and the

larger capacitance density of the *VB* structures can be achieved by extending the widths of the vertical bars in one dimension, as shown in Figure 6.8. In the limiting case, this intermediate structure will become the *VPP* capacitor.

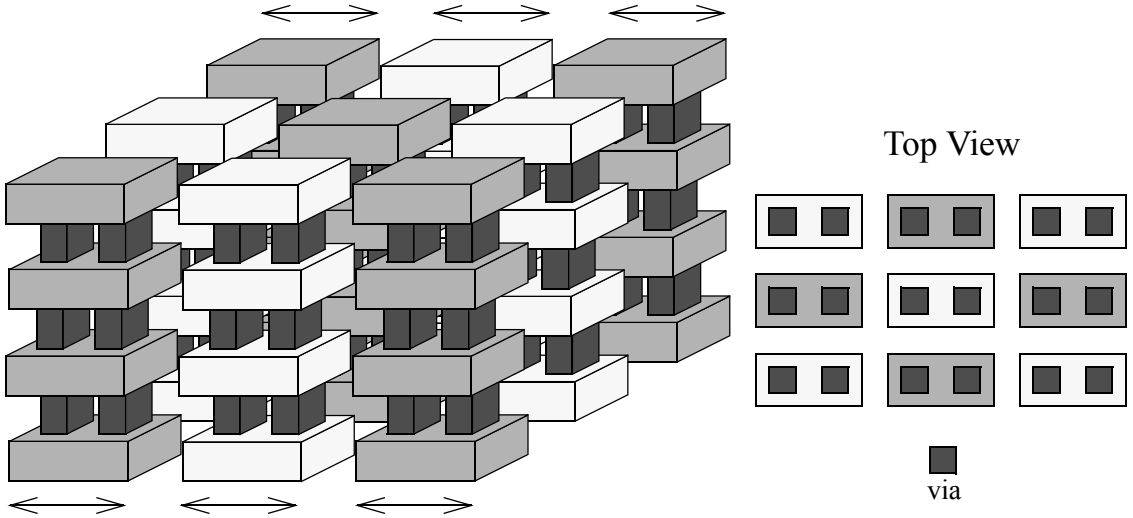


Figure 6.8: Modified *Vertical Bars* structure.

In some process technologies the minimum lateral spacing between different metal layers may vary significantly. To achieve the highest capacitance density in such processes we can use a modified version of the *VPP* structure, shown in Figure 6.9. This structure consists of multiple vertical parallel plate capacitors placed orthogonally and connected through interleaved vias. In the limiting case, reduces to the woven structure [93] discussed in the next section. This configuration takes advantage of all the available metal

layers and hence achieve higher capacitance density at the extra cost of combining vertical fields which will degrade the matching properties of the structure as will be seen next.

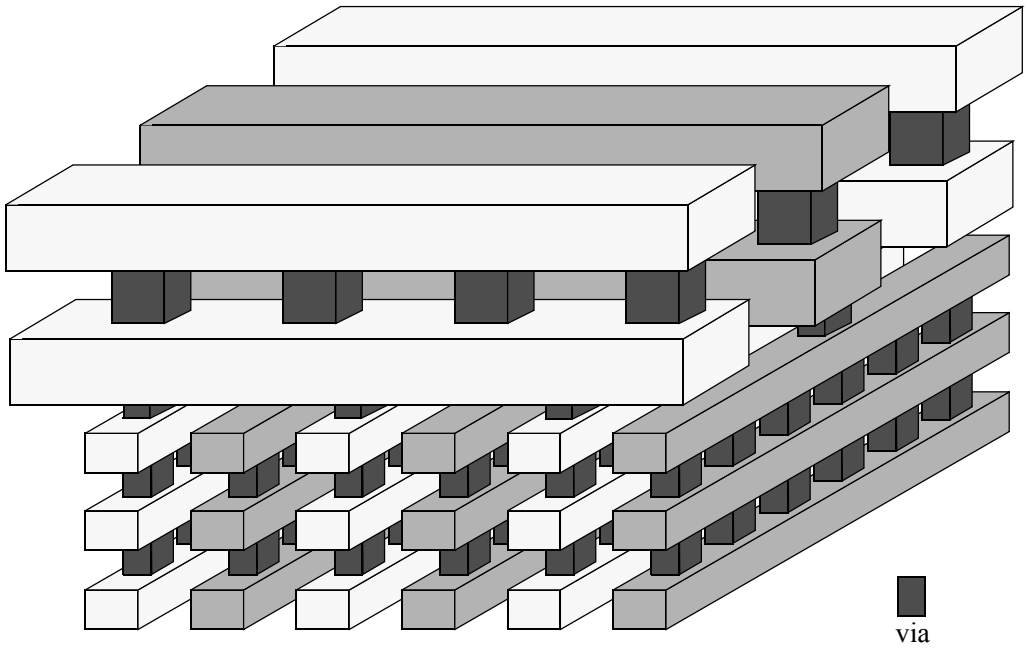


Figure 6.9: Modified *Vertical Parallel Plates* structure.

The value of the standard parallel plate capacitor of Figure 6.1 is primarily determined by the oxide thickness. On the other hand, the exact values of the *VPP* and *VB* capacitors are determined by lithography and etching. These two processes are quite accurate in today's process technologies. It is therefore reasonable to suspect that the lateral component of the capacitor should be more repeatable and has a smaller variation across the wafer. In this case, it is clear that any structure combining the lateral and vertical field components will suffer from the worse accuracy of the vertical capacitance component, which will lead to inferior matching and tolerance properties. Practically, all of the existing integrated capacitive structures use the vertical fields and hence cannot achieve the best possible accuracy. This hypothesis will be verified in Section 6.6.

6.5 Capacitance Comparison

In this section, we will demonstrate the superior capacitance density of the new proposed structures through capacitance simulations. Several previously known structures which exploit lateral and vertical fields will be compared to the *VPP* and *VB* structures under different conditions.

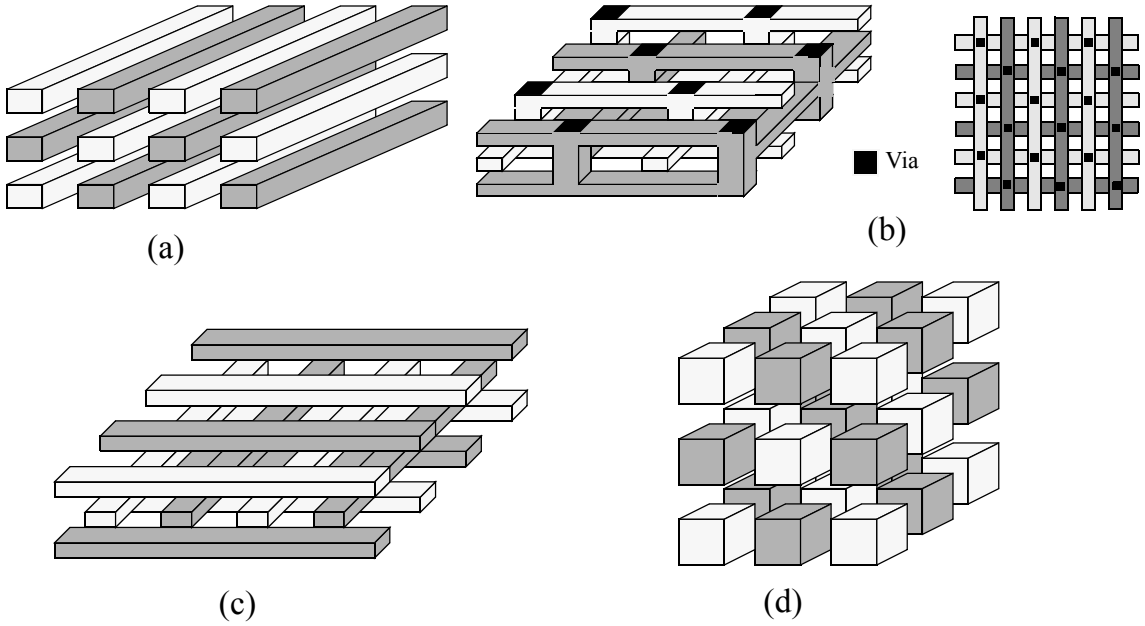


Figure 6.10: Manhattan capacitor structures: a) Parallel Wires (*PW*), b) Woven, c) Woven no Via, and d) Cubes 3-D.

Some of the more uniform structures, which we will refer to as lateral flux capacitors are shown in Figure 6.10. Three examples of structures using more random patterns mostly inspired by fractal geometries that will be referred to as quasi-fractal structures after [93] are depicted in Figure 6.11. While not exclusive, the structures in Figure 6.10

and Figure 6.11 are chosen to reflect a wide range of possible rectangular (*Manhattan*) geometries alternatives to the horizontal parallel plate of Figure 6.1.

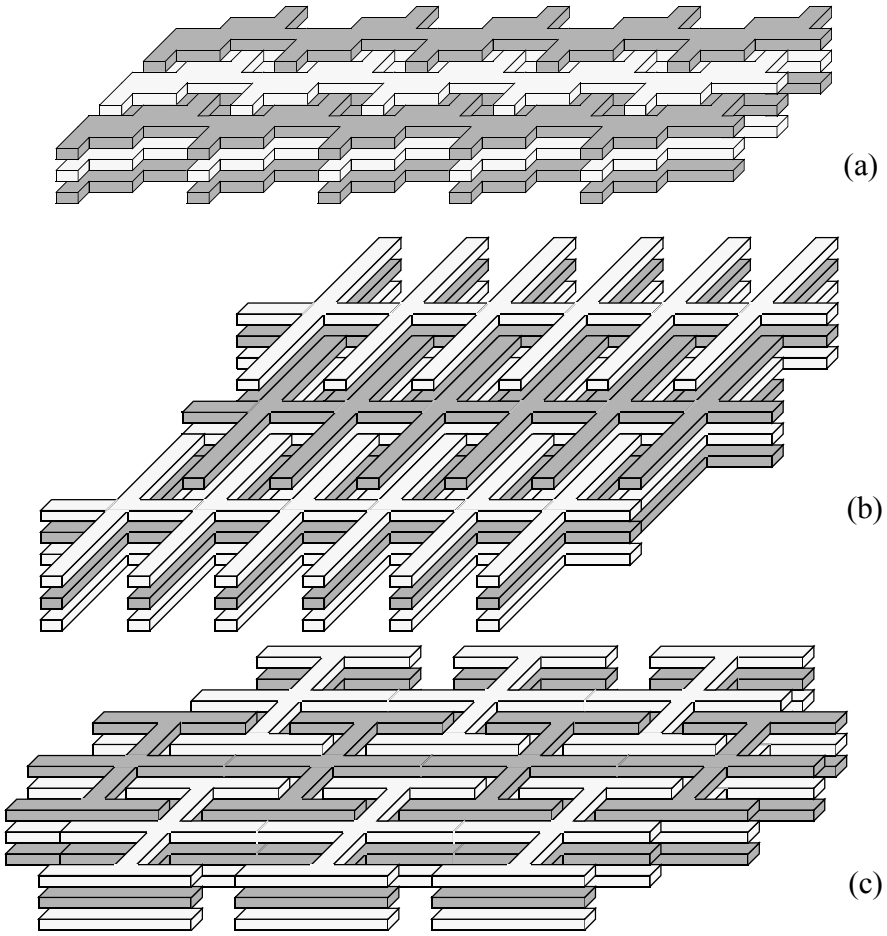


Figure 6.11: Quasi-fractal capacitor structures.

Figure 6.10a shows the interdigitated metal slabs or *Parallel Wires* used for high-frequency bypassing and coupling in integrated circuits [93]-[97]. Figure 6.10b shows the top view and the three-dimensional (3-D) perspective of the woven structure mentioned in [93]. A no-via variation of this structure is illustrated in Figure 6.10c for comparison purposes. This structure will be mainly used to determine the effect of vias in the regular woven structure. Figure 6.10d depicts minimum-sized cubes spaced at minimum lateral spacing and cross-connected three-dimensionally to maximize the fringe fields. It is noteworthy that this structure is only used for comparison and cannot be

fabricated in reality due to lack of means to maintain every other cube at the same potential.

As mentioned before, the structures in Figure 6.11 are intended to imitate segments of quasi-fractal structures. The structure in Figure 6.11a is aimed at maximizing the vertical field usage, enhanced by moderate lateral fields. On the other hand, the capacitive structures of Figure 6.11b and Figure 6.11c are more aggressive with the lateral field and try to use both vertical and lateral fields more equally.

In odder to accurately predict the capacitance of any capacitive structure, we have developed a special purpose field solver working based on an enhanced relaxation algorithm. The simulator brakes the simulation volume into discrete grid points, the grid size in each direction can be different and is set by the user. The information of the physical location of the metal lines is introduced in a 3-dimensional (3D) matrix, which determines the boundary conditions. Then the poisson's equation is solved in the entire dielectric volume. The electric field and the electrostatic energy density are then computed, and finally, the capacitance is obtained by integrating the electrostatic energy density over the entire volume. It is noteworthy that a finer grid can be achieved by exploiting the symmetry of the structure and carefully using a basic simulation cell.

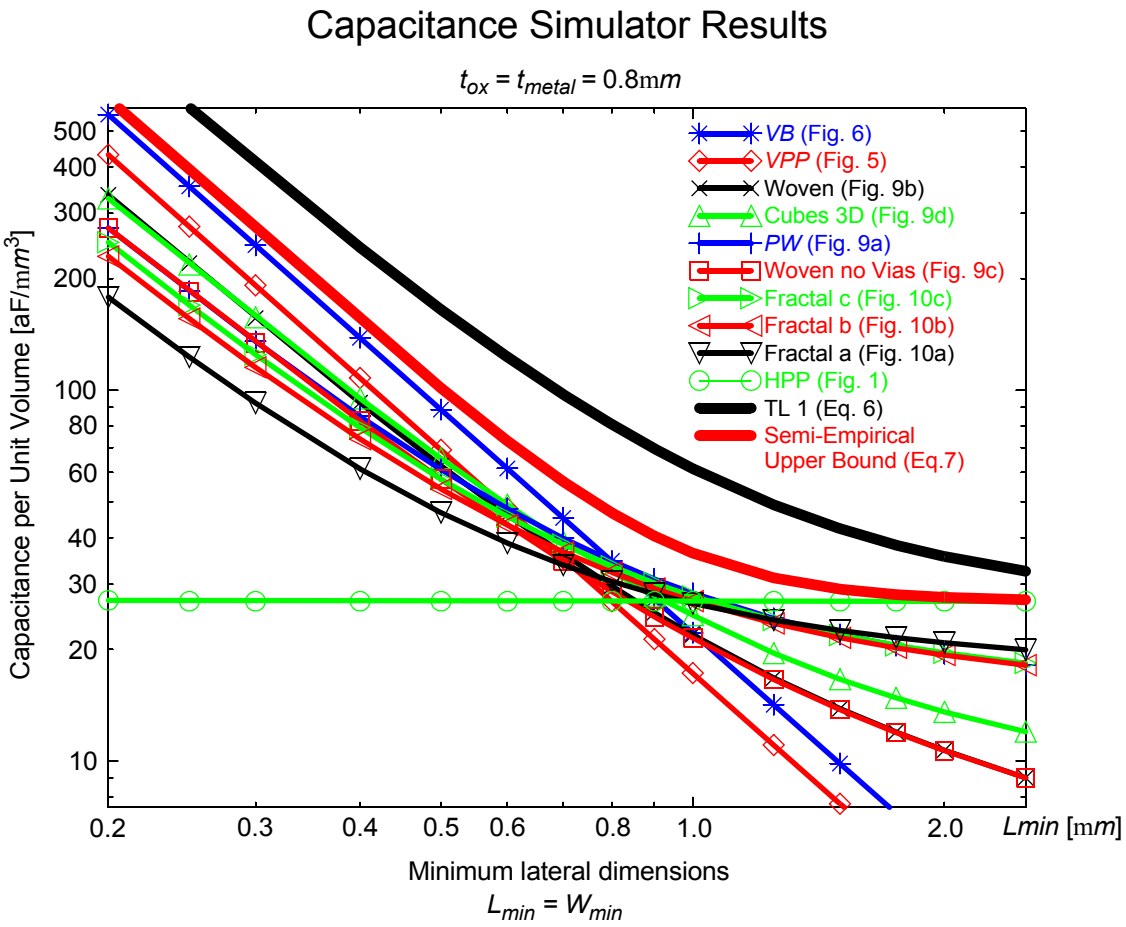


Figure 6.12: Capacitance density vs. minimum lateral dimensions for $t_{ox} = t_{metal} = 0.8\mu m$.

Capacitance density simulations are performed for metal configurations of Figure 6.10 and Figure 6.11, as well as the two new proposed structures. In the first set of simulations both, t_{ox} and t_{metal} are kept constant at $0.8\mu m$. It is also assumed that $L_{min} = W_{min}$. The equality of L_{min} and W_{min} is common in contemporary process technologies and hence will be used in this comparison. The simulation results showing the capacitance density per unit volume versus the minimum lateral spacing, L_{min}, for the structures of Figure 6.1, Figure 6.6, Figure 6.7, Figure 6.10, and Figure 6.11 are depicted in Figure 6.12. Although this graph is for a t_{ox} and t_{metal} of $0.8\mu m$, it can be easily used for other vertical spacings

through a simple scaling, as long as $t_{ox} = t_{metal}$ and $L_{min} = W_{min}$. This property can be traced back to the scale invariance of electrostatic equations [104].

It is instructive to investigate the behavior of the capacitance density for very small and very large lateral spacings in Figure 6.12. For large lateral spacings (right hand side of the graph), the capacitance densities reach plateaux as the lateral fields become inconsequential and the capacitance is dominated by the vertical fields. The horizontal parallel plate structure of Figure 6.1, has the best performance in this region due to its optimal usage of vertical fields. Also note that the capacitance densities of the *VPP* and *VB* structures continuously diminish due to the lack of any vertical field component. Other structures fall in between these two extremes and reach a capacity limit controlled by their vertical-to-lateral field usage efficiency.

At the other extreme, when the minimum lateral spacing becomes much smaller than the vertical separation (left hand side of the graph), the capacitance density becomes inversely proportional to L_{min}^2 because the lateral plate spacing decreases linearly with L_{min} resulting in a linear increase in the capacitance per plate. Also the number of plates per unit volume grows linearly with decreasing L_{min} due to smaller metal width and spacing. This dual dependence results in an inverse L_{min}^2 dependence, as predicted by (6.6). In this region, the *VB* structure shows the maximum capacitance density followed by the *VPP* structure due to their optimum usage of lateral fields. The later structure benefits from shrinking in one lateral-dimension only, while the former makes the most of the two lateral-dimensions shrinkage. On the other hand, the horizontal parallel plate structure has the worst performance in this region, due to lack of any lateral-field components. It is also noted that the vias enhance the lateral-flux density in the dielectric/oxide inter-layer separation. As an example, the woven structure of Figure 6.10b shows an advantage over that of Figure 6.10c, due to the lateral field enhancement caused by the vias. This is another very important characteristic of the two new proposed structures, as they use vias

that maximize the lateral field usage in the vertical inter-layer dielectric separation between different metal layers.

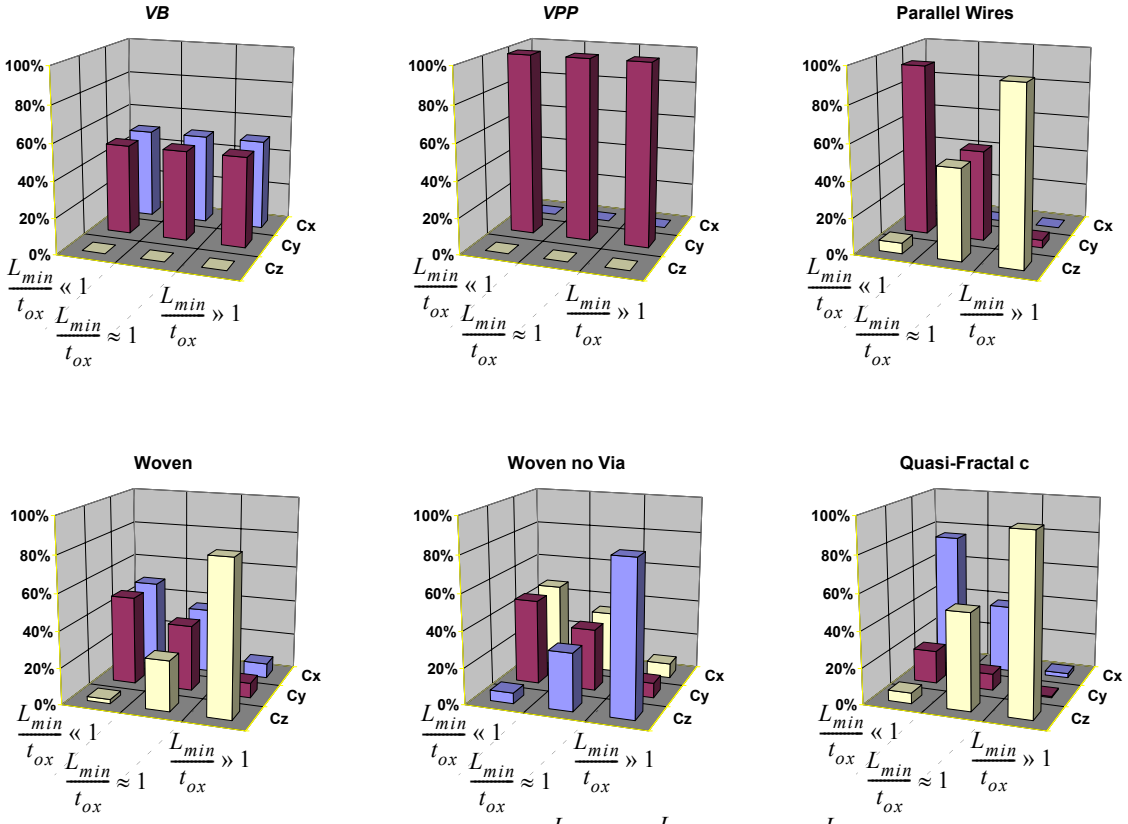


Figure 6.13: Field usage efficiencies for $\frac{L_{min}}{t_{ox}} \ll 1$, $\frac{L_{min}}{t_{ox}} = 1$ and $\frac{L_{min}}{t_{ox}} \gg 1$.

To gain more insight into the contributions of the capacitance components to the overall density, the *field usage efficiency* of different structures are plotted in three different regions of the $\frac{L_{min}}{t_{ox}}$ ratios in Figure 6.13. *Field usage efficiency* can be defined as the ratio of each of c_x, c_y, and c_z to the total capacitance density, which represent the percentage of energy stored in each component of the electric field. For the $\frac{L_{min}}{t_{ox}} \ll 1$ region, the lateral components are the main contributor to the total capacitance. In

contrast, for the $\frac{L_{min}}{t_{ox}} \gg 1$ region, the vertical component forms the main portion of the total capacitance.

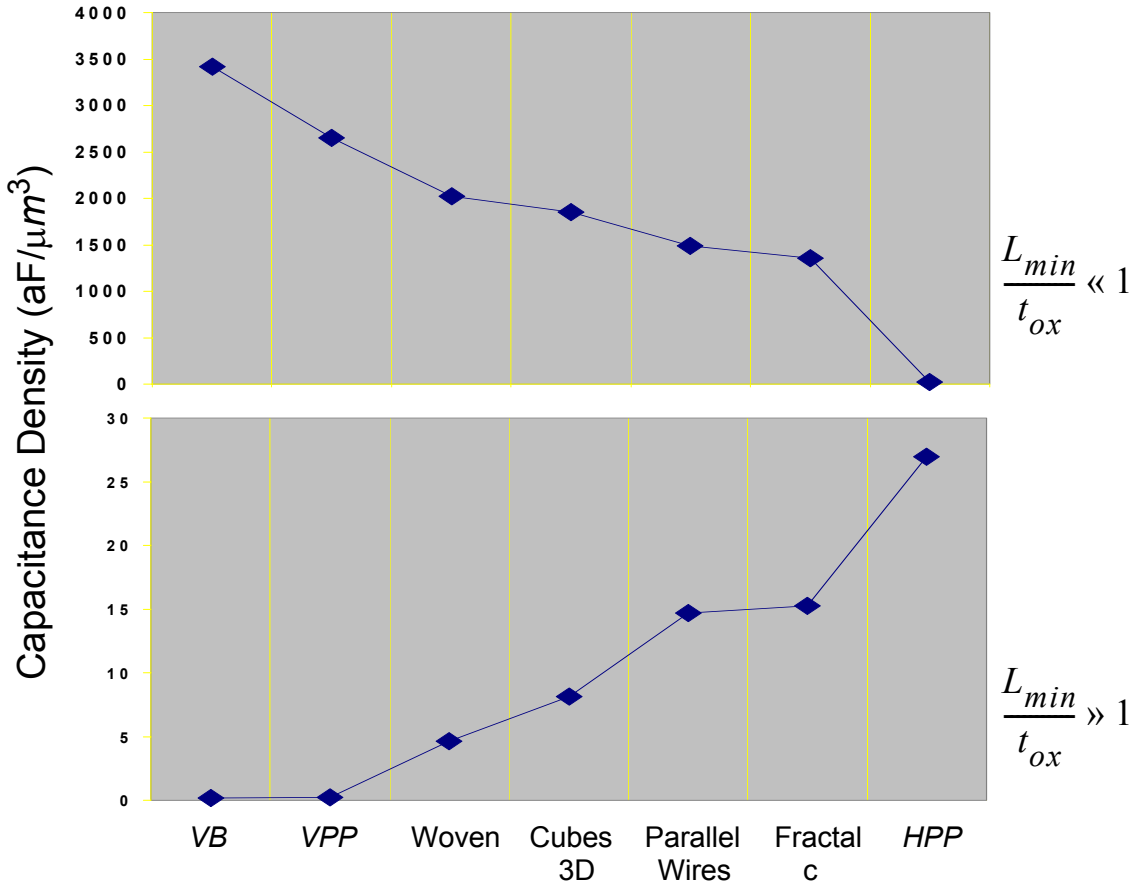


Figure 6.14: Capacitance densities for $\frac{L_{min}}{t_{ox}} \ll 1$ and $\frac{L_{min}}{t_{ox}} \gg 1$.

To visualize this trade off further, the capacitance density of different structures are plotted in Figure 6.14 for the $\frac{L_{min}}{t_{ox}} \ll 1$ and $\frac{L_{min}}{t_{ox}} \gg 1$ regions. Interestingly, the order almost completely reverses when going from small to large $\frac{L_{min}}{t_{ox}}$ ratios, *i.e.*, the best structures become the *worst* and vise versa. This can be explained by the inherent trade-off between lateral and vertical field utilization, as lateral field usage can only be increased by introducing dielectric regions between metal lines in the same layer, which in turn results in loss of some vertical component.

Structure	Ratio to TL1	Ratio to Semi-Empirical Upper Bound
VB	64%	91%
VPP	50%	71%
Woven	38%	54%
Cubes 3-D	35%	49%
Parallel Wires	28%	40%
Woven no vias	28%	40%
Quasi-Fractal c	25%	36%
Quasi-Fractal b	23%	33%
Quasi-Fractal a	18%	25%
HPP	0.5%	0.7%

Table 6.1: Capacitance comparison.

Finally, Table 6.1 compares the simulated capacitance densities of all the structures discussed so far. These results are normalized to the *Theoretical Limit 1* and *Semi-Empirical Upper Bound,* and are considered for $L_{min} = W_{min} = 0.1\mu m$ and $t_{ox} = t_{metal} = 1\mu m$ (or for any other case where the minimum lateral dimensions are ten times smaller than the vertical dimensions). The two new proposed structures attain the highest capacitance density among these structures. The *VB* and *VPP* achieve a capacitance density of 91% and 71% when compared to the *Semi-Empirical Upper Bound*, respectively, while the woven and quasi-fractal structures attain 54% and 25%, respectively.

6.6 Measurement Results

Two sets of test capacitors were fabricated in two different process technologies. The first set of test capacitors were fabricated in a 3 metal layer process with two thin metal layers and an additional thick metal layer. For this process the dielectric material is silicon dioxide and the metal material is aluminum. The two lower metal layers have $L_{min} = W_{min}$

= 0.5µ*m*, t_{ox} = 0.95µ*m*, and t_{metal} = 0.63µ*m*. The fabricated structures in this process include the *VPP* (Figure 6.6), interdigitated (*Parallel Wires* or *PW*) (Figure 6.2) and horizontal parallel plate (*HPP)* (Figure 6.1) capacitors that occupy 0.12mm^2, 0.33mm^2 and 0.19mm^2, respectively, as shown in Figure 6.15.

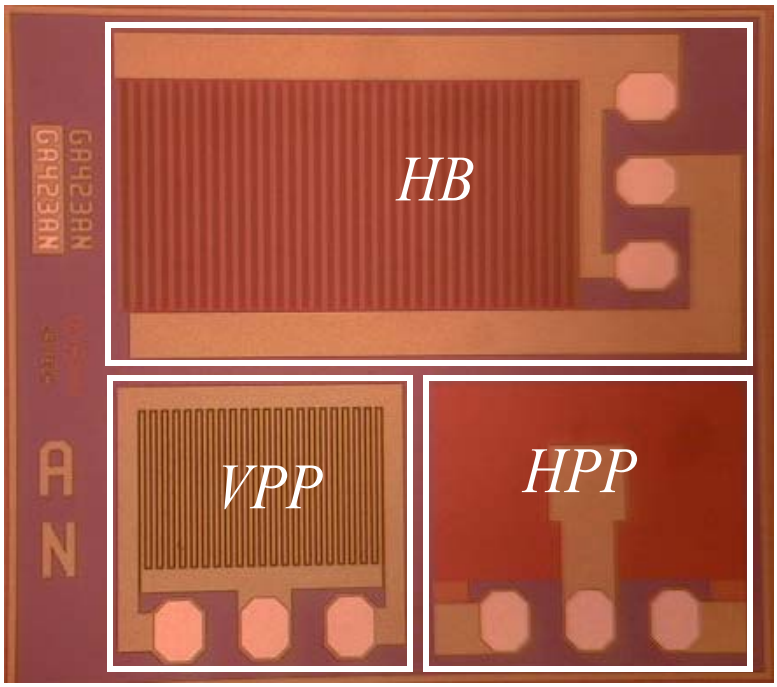


Figure 6.15: Die micrograph of the first test capacitor for $L_{min} = W_{min} = 0.5\mu m$

The performance numbers for these structures are summarized in Table 6.2. The *VPP* capacitor achieves a factor of 4.4 capacitance density improvement over the standard *HPP* using only two metal layers, but also *for equal capacitance values* demonstrate a higher self-resonance frequency than the *HPP* structure. This is based on the size-normalized self-resonance frequencies of the structures listed in Table 6.2. In terms of series resistance, the *VPP* capacitor has a series resistance, r_s, of 0.57Ω comparable to r_s of 1.1Ω and 0.55Ω for the *HPP* and *PW* capacitors, respectively. It is noteworthy that the commonly used interdigitated (or *PW*) structure of Figure 6.2 is inferior to the newly introduced *VPP* capacitor, in capacitance density, quality factor, and self-resonance frequency.

Structure	Cap. Density (c) [aF/μm^2]	Ave. (C_{ave}) [pF]	Std. Dev. (σ_c) [fF]	$\frac{\sigma_c}{C_{ave}}$	f_{res} [GHz]	Q @ 1GHz	f_{res} (fixed L)[a] (C=6.94pF) [GHz]	f_{res} (scaled L)[b] (C=6.94pF) [GHz]	Rs (Ω)	Break-Down [Volts]
VPP	158.3	18.99	103	0.0054	3.65	14.5	6.04	9.99	0.57	355
PW	101.5	33.5	315	0.0094	1.1	8.6	2.42	5.31	0.55	380
HPP	35.8	6.94	427	0.0615	6.0	21	6.0	6.0	1.1	690

Table 6.2: Measurement results - first set.

a. Normalized self-resonance frequency calculated for a capacitance of 6.94pF (the value of the *HPP*) assuming that only the capacitor changes and that the inductor does not scale.

b. Normalized self-resonance frequency calculated for a capacitance of 6.94pF (the value of the *HPP*) scaling both the capacitor and the inductor with size.

To investigate the tolerance properties of the *VPP* capacitor, the capacitance of these three structures were measured across 22 different sites at different locations on two quarters of two different 8-inch wafers. A histogram showing the relative capacitance value distribution across one of the quarter-wafers is shown in Figure 6.16. The standard deviations of the capacitance normalized to the average value for these three structures are also shown in Table 6.2. It can be easily seen that the absolute capacitance accuracy of the *VPP* capacitor is approximately an order of magnitude better than the conventional *HPP*. Comparison of the measurements on two different wafers also shows that wafer-to-wafer capacitance variation of the purely lateral structures is also improved significantly due to the higher repeatability of the lithography. Finally, due to the high breakdown voltage of the dielectric, the measured breakdown voltage of the implemented capacitors are in excess of 350V, as shown in Table 6.2.

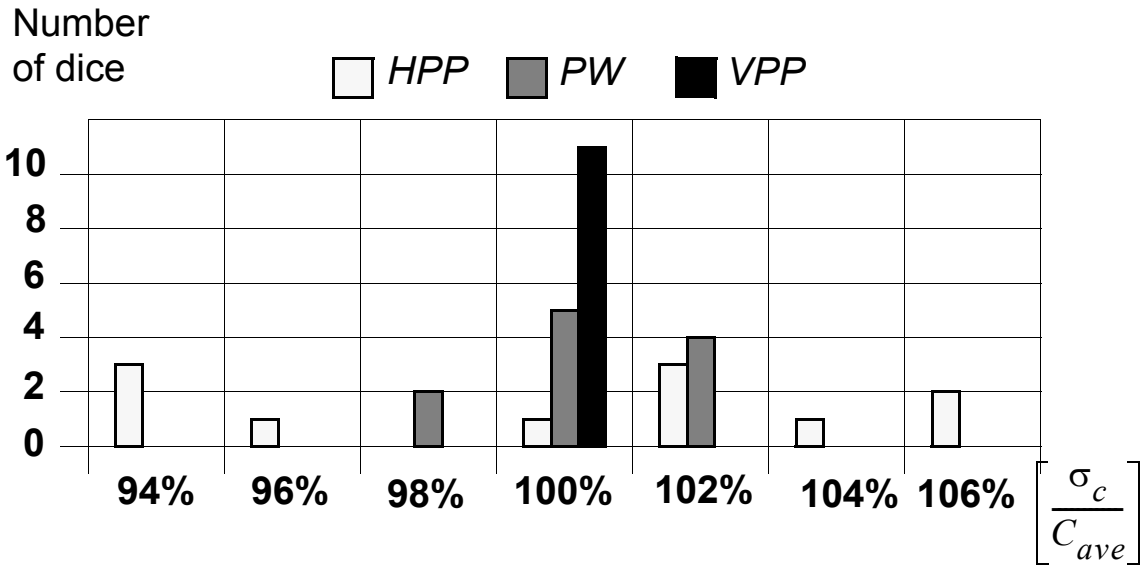


Figure 6.16: Capacitance distribution of the *VPP*, *PW,* and *HPP* structures.

The second set of test capacitors were fabricated in a purely digital CMOS 7-metal layer process technology with $L_{min} = W_{min} = 0.24\mu m$, $t_{ox} = 0.7\mu m$, and $t_{metal} = 0.53\mu m$ for the bottom five layers. For this process the dielectric material is silicon dioxide and the metal material is aluminum. The implemented capacitors include a 5 metal layer *HPP*, a 5 metal layer *VPP,* and a 4 metal layer modified *VB* structures as shown in Figure 6.1, Figure 6.6, and Figure 6.7, respectively. To perform a fair comparison the value of the three different capacitor types are designed to be equal. A 1pF and a 10pF version of each structure were fabricated in the same die to provide an unbiased comparison of the

structures' capacitance density, self-resonant frequency, tolerance and matching properties. Figure 6.17 shows the capacitor test chip photograph.

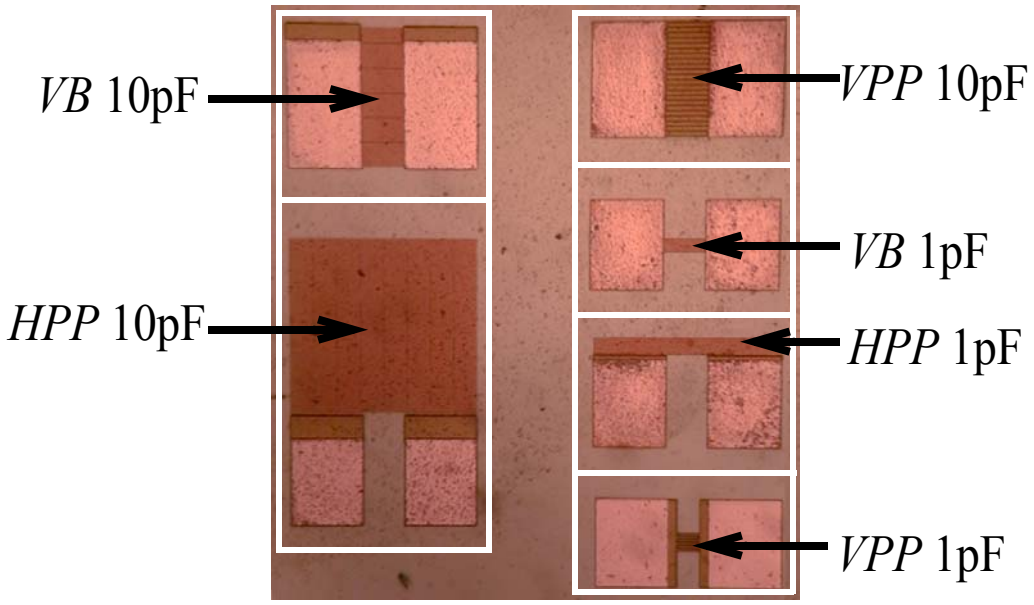


Figure 6.17: Die micrographs of the second test capacitors for $L_{min} = W_{min} = 0.24\mu m$.

The summary of the measurements for the 1pF capacitors is presented in Table 6.3. For the sake of comparison, the performance measures of a 1pF MIM capacitor is also included in this table. Due to the lack of any MIM capacitor in the purely digital CMOS technology used, these performance measures are obtained from the design manual information for an MIM capacitor of a very similar process technology with $L_{min} = 0.28\mu m$ and mixed signal capabilities.

Structure	Cap. Density (c) [aF/μm^2]	Ave. (C_{ave}) [pF]	Area [μm^2]	Cap. Enhance-ment	Std. Dev. (σ_c) [fF]	$\frac{\sigma_c}{C_{ave}}$	f_{res} [GHz]	Measured Q @ 1GHz	Break-Down [Volts]
VPP	1512.2	1.01	669.9	7.4	5.06	0.0050	>40	83.2	128
VB	1281.3	1.07	839.7	6.3	14.19	0.0132	37.1	48.7	124
HPP	203.6	1.09	5378.2	1.0	26.11	0.0239	21	63.8	500
MIM	1100	1.05	960.9	5.4			11	95	

Table 6.3: Measurement results - second set (1pF).

Due to the high lateral field efficiency of the new proposed structures, the *VPP* and *VB* capacitors show 7.43 and 6.29 times more capacitance density than the standard multi-plate *HPP* of Figure 6.1, respectively, which are the highest reported to date. This corresponds to a capacitance density of 1.51fF/μm^2. Moreover, the capacitance density of the *VPP* capacitor is even 37% higher than the capacitance density of the MIM capacitor.

Because of the multiple via connections and the large number of vertical plates connected in parallel, the *VPP* structure presents a quality factor even higher than the *HPP*, whereas the quality factor of the *VB* structure is relatively lower because of the rather high via resistance of the process technology, as summarized in Table 6.3.

As the proposed structures attain higher capacitance densities, their physical dimensions are smaller and hence show higher self-resonance frequencies. The admittance versus frequency measurement of Figure 6.18 shows a self-resonance frequency in excess of 40GHz for the 1pF *VPP* capacitor. This is twice the self-resonance frequency of the *HPP* capacitor, and 4 times higher than that of the MIM capacitor.

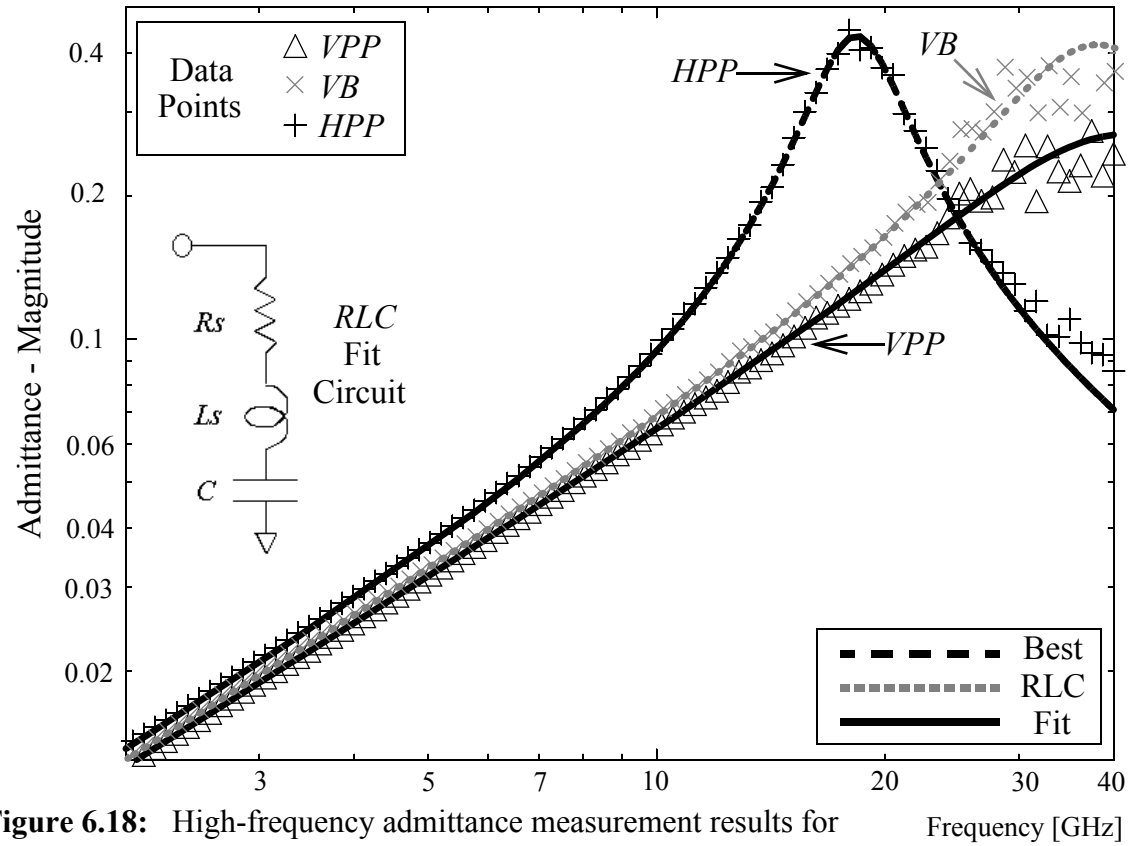


Figure 6.18: High-frequency admittance measurement results for the *HPP*, *VB,* and *VPP* structures.

To verify our earlier hypothesis of better tolerance and matching properties of the purely lateral structures, the capacitance of capacitors of same values implemented using different structures were measured across 37 usable sites of an 8-inch wafer. The standard deviation normalized to the average value of each 1pF structure is shown in Table 6.3. As can be seen, the *VPP* structure presents almost 5 times better capacitance tolerance than the *HPP* structure across the wafer.

Although the tolerance of capacitors is an important property to quantify, in many analog applications, the parameter of more significance is the ratio between two adjacent capacitors. To confirm the better matching properties of the new structures, the ratio of adjacent 10pF and 1pF capacitors of the same type on the same site were compared across the wafer. The variations of this ratio normalized to its average, namely σ_r / r_{ave}, is a

better measure to quantify matching. The *VPP, VB,* and *HPP* capacitors show a σ_r / r_{ave} of 0.6%, 1%, and 1.3%, respectively. Due to the higher accuracy of the lithography process, the two new lateral field structures present better matching properties than the standard horizontal parallel plate capacitor, as suggested earlier. It is noteworthy that in practice, an accurately defined ratio is achieved by using multiple parallel capacitors of the same size and shape.

Structure	Cap. Density (c) [aF/μm^2]	Ave. (C_{ave}) [pF]	Area [μm^2]	Cap. Enhan-cement	Std. Dev. (σ_c) [fF]	$\frac{\sigma_c}{C_{ave}}$	f_{res} [GHz]	Measured Q @ 1GHz	Break-Down [Volts]
VPP	1480.0	11.46	7749	8.0	73.43	0.0064	11.3	26.6	125
VB	1223.2	10.60	8666	6.6	73.21	0.0069	11.1	17.8	121
HPP	183.6	10.21	55615	1.0	182.14	0.0178	6.17	23.5	495
MIM	1100	10.13	9216	6.0			4.05	25.6	

Table 6.4: Measurement results - second set (10pF).

Finally, the summary of the measurements for the 10pF capacitors are shown in Table 6.4. For the sake of comparison, it also includes the estimated performance measures of a 10pF MIM capacitor. The *VPP* and *VB* capacitors show 8.0 and 6.6 times more capacitance density than the 10pF standard multi-plate *HPP* of Figure 6.1. This corresponds to a 34% higher capacitance density of the *VPP* capacitor when compared to the MIM. The self-resonance frequencies of the proposed structures are in excess of 11GHz, which is almost twice the self-resonance frequency of the *HPP* capacitor, and approximately 3 times higher than that of the MIM of the same value. Finally, the 10pF *VPP* and *VB* capacitors presents almost 3 times better capacitance tolerance than the *HPP* structure across the wafer.

6.7 Summary

A new theoretical framework which shows the capacity limits of integrated capacitors was presented. This new framework can be used to evaluate the performance of the existing capacitive structures and leads to two purely lateral capacitors. These structures demonstrate: higher capacitance density, better matching and tolerance properties, and higher self-resonance frequency than previously reported capacitor structures, MIM and standard *HPP* capacitors, while maintaining a comparable quality factor. These two new structures are standard CMOS compatible and do not need an extra processing step, as is the case with special MIM capacitors.

Chapter 7 *Closed Loop Frequency Generation*

After looking into the phase-locked-loop (PLL) basics, local oscillators and in-phase and quadrature signal generation methods, in this Chapter, three phase-locked-loops will be presented. A 6.6GHz PLL for application in a concurrent dual band receiver will be addressed in Section 7.1. The design issues for an ultra-low power 6.3GHz PLL will be covered in Section 7.2. In Section 7.3, a phase compensation technique is implemented to reduce the fractional reference spur in a 3.2GHz Fractional-*N* PLL.

7.1 A 6.6GHz Phase-Locked-Loop for Concurrent Dual-Band Receiver Applications

Recently, multi-band receivers have been introduced to increase the functionality and flexibility of modern wireless applications [105]-[111]. These multi-band receivers switch between two or more different bands to receive one band at a time. While switching between bands improves the versatility of the receiver, such as multi-band cellular phones, this is not sufficient as in the case where more than one band needs to be received simultaneously, as in the case of a multi functionality transceiver (e.g., a multi-band cellular phone with a global position system (GPS), Bluetooth interface, wireless LAN, etc.). Hashemi *et al* [112] has recently introduced a new concurrent receiver architecture that is capable of simultaneous operation at two-different frequencies without dissipating twice as much power or a significant increase in cost and die area. In this Section, the implementation of the frequency generation for such system will be presented.

7.1.1 Receiver Architecture and Frequency Planning

The simultaneous detection of two different frequency bands is accomplished by the dual-band antenna [113]-[115], dual-band filter [116] and dual-band LNA [112] depicted in the dual-band receiver architecture of Figure 7.1.

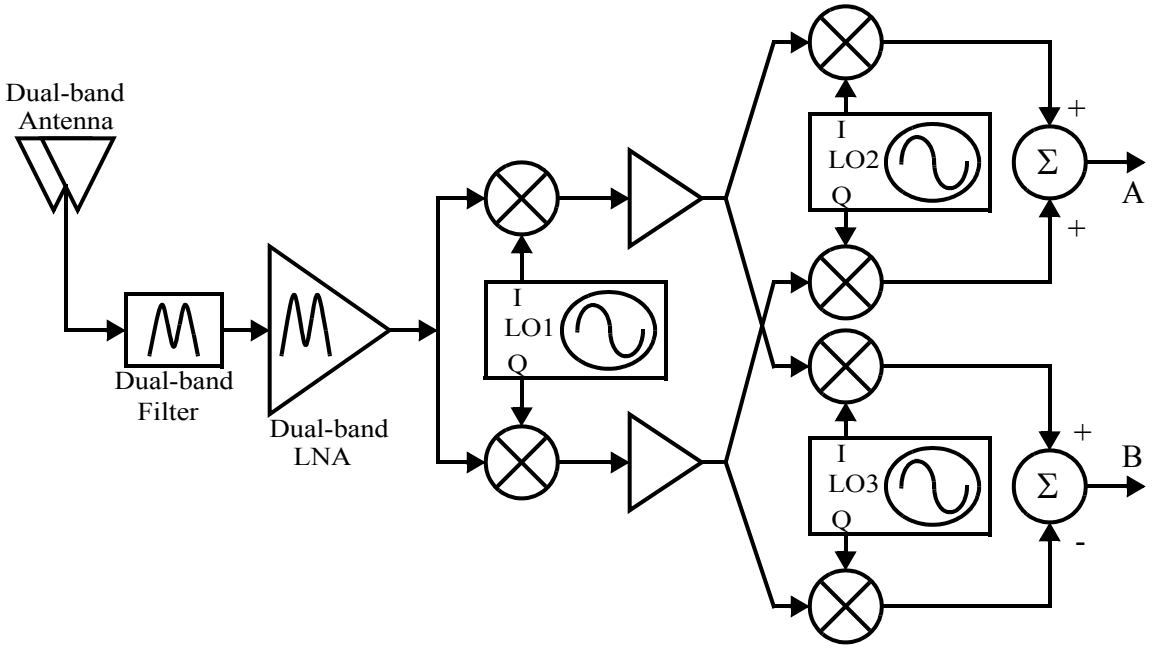


Figure 7.1: Dual-band receiver architecture.

A dual-band image-rejection downconversion scheme is necessary to translate the different information-carrying signals to baseband. This is accomplished by the combination of the mixing of the three local oscillator frequencies, amplification and filtering [112] as shown in Figure 7.1.

Frequency planning plays an essential role in the design of such dual-band receiver system. It is highly desirable that the first LO frequency is such that the image of the first band at the frequency f_A falls at the notch of the front-end transfer function (f_{IA}), and that

the image of the second band at the frequency f_B falls at the outside of the pass-band of the front end (f_{IB}) as depicted in Figure 7.2.

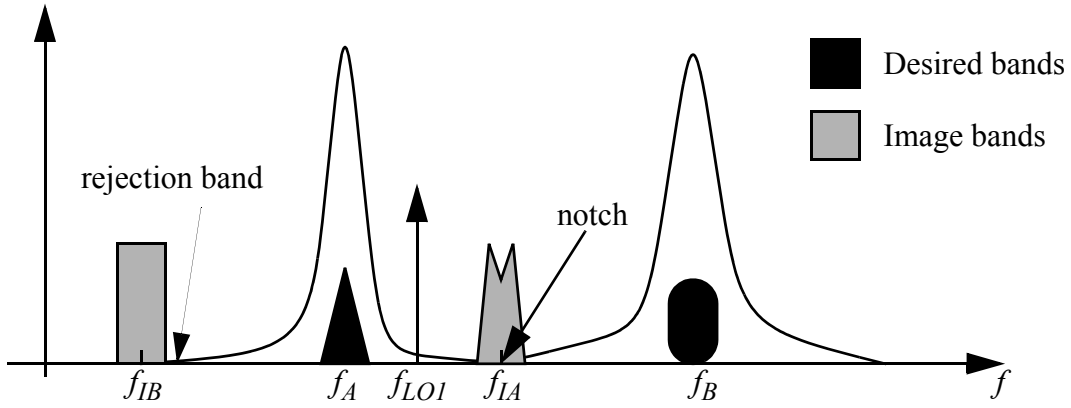


Figure 7.2: Frequency allocation and planing for the dual-band receiver.

The notch and out-of-band rejection is determined by the combined attenuation of the dual-band antenna, dual-band-filter and dual-band LNA. This receiver architecture can act as the first half of a single-sideband image reject architecture if quadrature phases of the LO are available, similar to that proposed by Weaver [117]. Two separate paths have to be used in order to demodulate two bands simultaneously and independently. Each path is comprised by the second half of an image rejection architecture.

Since the power consumption of high-frequency PLLs is quite high and PLLs occupy large fraction of the die, it is highly desirable that all the local-oscillator signals would be generated from a single PLL and frequency divider stages. Thus, the power consumption and area of two PLLs can be saved. For this particular application, f_A =2.45GHz and f_B = 5.25GHz. These two frequencies correspond to two unlicensed ISM bands. For this frequency allocations, the notch in the LNA can be easily tuned at 4.15GHz, thus, $f_{LO1} = \frac{f_{IA}+f_A}{2} = 3.3GHz$, and $f_{IB} = 2 \cdot f_{LO1} - f_B = 1.35GHz$. The image frequency of the second band (f_{IB}) is approximately a factor of two lower than f_A and will have enough attenuation. If the center of the desired bands (f_{CA} and f_{CB}) are downconverted to 250MHz, which corresponds to downconvert the beginning of the two bands to dc, thus $f_{LO2} = f_{CA} + f_{LO1} - f_A = 1.1GHz$ and $f_{LO3} = f_{CB} - f_{LO1} + f_B = 2.2GHz$. This

frequency allocation plan allows the generation of f_{LO2} from the division by two of f_{LO3}, *i.e.,* $f_{LO3} = \frac{f_{LO2}}{2}$. f_{LO1} and f_{LO3} can both be derived from a 6.6GHz source by a division by 2 and 3, respectively, *i.e.,* $f_{LO1} = \frac{f_{LO}}{2}$ and $f_{LO3} = \frac{f_{LO}}{3}$. Table 7.1 summarizes the frequency allocation for the proposed plan.

f_{LO}	$f_{LO1}=f_{LO}/2$	$f_{LO2}=f_{LO}/3$	$f_{LO3}=f_{LO2}/2$
6.6GHz	3.3GHz	2.2GHz	1.1GHz
f_A	$f_{IF1}=f_{LO1}-f_A$	$f_{IA}=f_{IFA}-f_{LO1}$	$f_{BBA}=f_{IFA}-f_{LO2}$
2.45GHz	0.85GHz	4.15GHz	250MHz
f_B	$f_{IF2}=f_B-f_{LO1}$	$f_{IB}=f_{LO1}-f_{IFB}$	$f_{BBB}=f_{IFB}-f_{LO3}$
5.25GHz	1.95GHz	1.35GHz	250MHz

Table 7.1: Concurrent receiver frequency planning.

7.1.2 PLL Building Blocks

Due to the frequency allocation plan discussed previously, all the necessary LO frequencies are derived from a single 6.6GHz PLL, the general block diagram of which is shown in Figure 7.3. The feedback action in the loop causes the two input signals of the phase detector to lock. For this implementation a series of nine flip-flop based divide-by-two provide total frequency division of N=512, therefore, a reference frequency of 12.89MHz is required for proper operation.

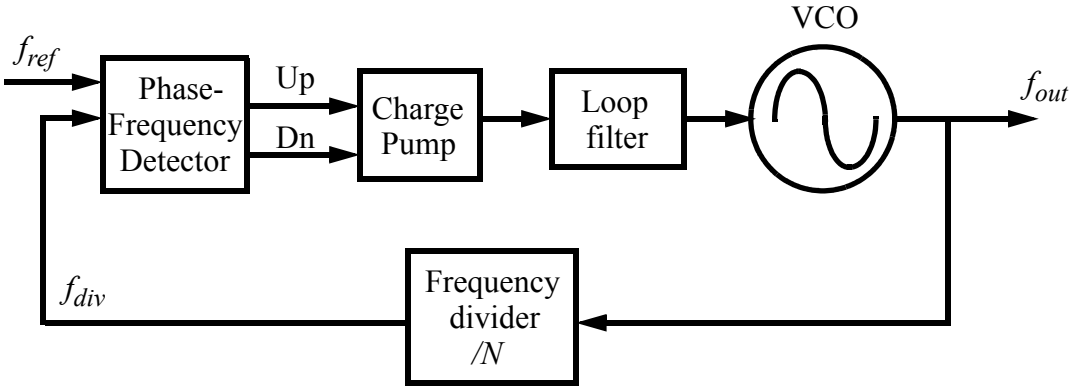


Figure 7.3: 6.6GHz PLL block diagram.

7.1.2.1 Voltage Controlled Oscillator

The voltage controlled oscillator circuit schematic is shown in Figure 7.4. It uses a cross-coupled differential pair core with a center-tapped inductor for the resonator. NMOS transistors are used as varactors. The strategies discussed in Chapter 3 for the optimization of the *LC* tank and oscillator core were implemented for this VCO. The oscillator is designed to have a center frequency of 6.6GHz and 15% of frequency tuning while drawing 7mA of current.

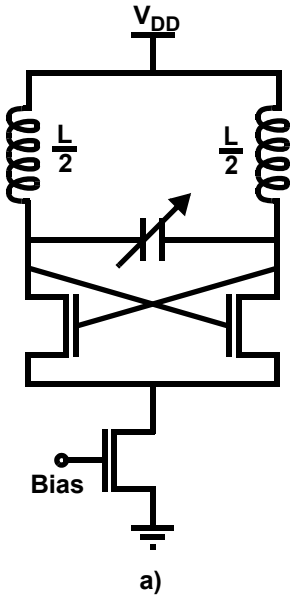


Figure 7.4: NMOS-only cross-coupled voltage controlled oscillator.

7.1.2.2 Frequency Dividers

A master-slave configuration of edge triggered flip-flops are used as a divide-by-two circuit and hence achieve frequency division by a factor of two. Their block diagram is shown in Figure 7.5a and the circuit schematic of the flip-flops is depicted in Figure 7.5b.

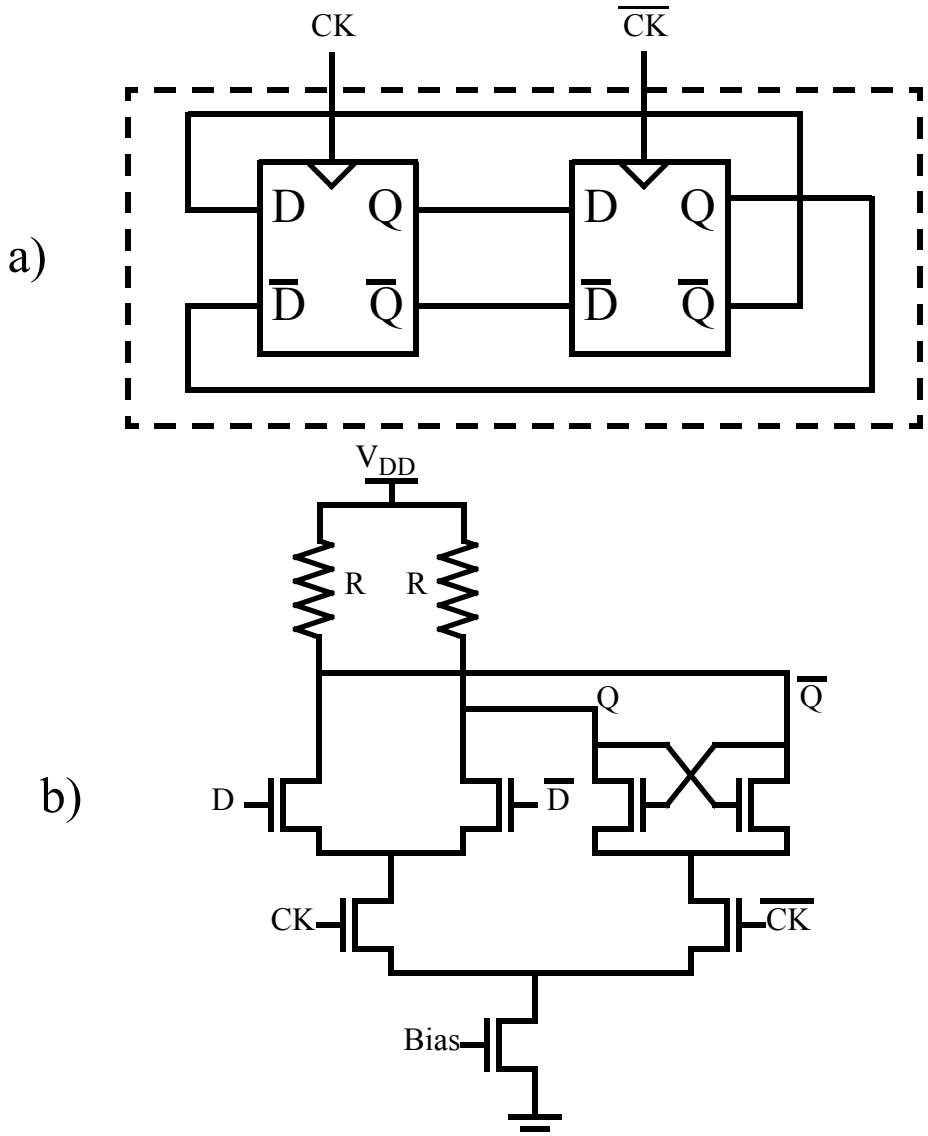


Figure 7.5: Divide-by-two master-slave flip-flop, a) block diagram, b) circuit schematic.

7.1.2.3 Phase Detector and Charge Pump

The phase-frequency detector schematic is depicted in Figure 7.6. It is the commonly employed topology that adds pulses on the up and down outputs of a certain minimum

width, even when the phase difference is zero. This eliminates the dead-zone problem of the other types of PLL [17][118].

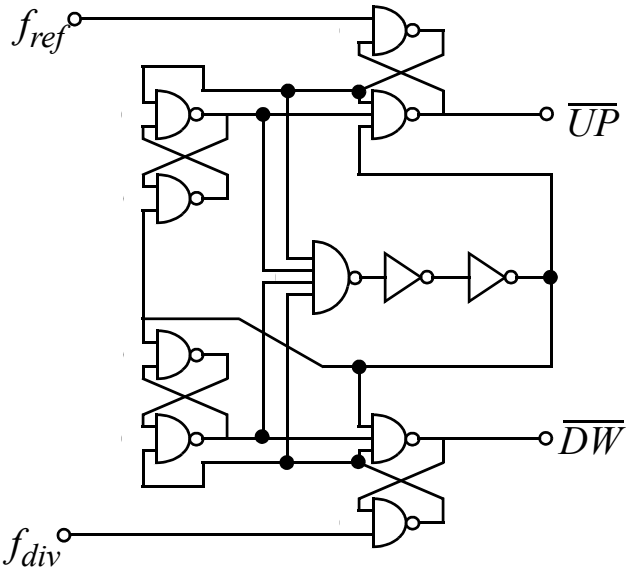


Figure 7.6: Phase-frequency detector schematic.

The charge-pump circuit is depicted in Figure 7.7. The up and down current can be either connected to the output or connected to a dummy reference voltage. To minimize the feed through of the control signal, all the switches are implemented by equal size NMOS and PMOS transistors. Each of them has their own separate control signal. To generate these eight control signals from the two outputs of the phase-frequency detector, both signals are passed through a inverter chain. These paths have even and odd number of inverter stages, respectively, but with the same global delay, so that the control signals of

the NMOS and PMOS transistor pair switch at the same instant, and thus cancelling charge injection. This is because the two control signals are of opposite sign.

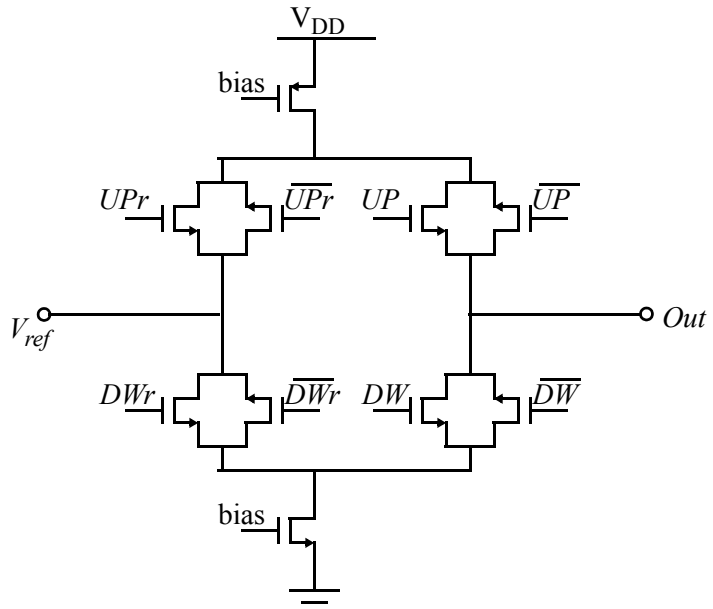


Figure 7.7: Charge-pump circuit schematic.

Ideally, the current should be steered at the same instant, from the right path (output) to the left path (dummy reference voltage) and vice versa. In practice however, there will be a short time when the switches from both sides will be conducting, due to the finite time required for a transistor to fully switch from conducting to non-conducting and vice versa. Therefore, a second control circuit adjusts the control signals to the charge-pump switches so that the switches in the left branch open before the switches in the right branch close, and close after the switches in the right branch open.

7.1.2.4 Loop Filter

Capacitors usually consume a large fraction of the die area and thus, loop filters are notorious for their large foot print size. The loop filter chosen for this design is comprised of two capacitors and one resistor and is shown in Figure 7.8. It presents the best trade-off between number and size of capacitors while providing a loop gain zero and a pole that guarantee stability as will be discussed next.

The open loop gain can be calculated after (2.8) as follows:

$$G(s) \cdot H(s) = \frac{I_{qp} \cdot K_{VCO}}{2\pi \cdot N} \times \frac{1 + \alpha_z \cdot s}{s^2 \cdot (C_z + C_p) \times (1 + \alpha_p \cdot s)} \tag{7.1}$$

where $\alpha_z = R_z \cdot C_z$ is an open loop zero and $\alpha_p = R_z \cdot \left(\frac{1}{C_z} + \frac{1}{C_p}\right)$ is an open loop pole. The cross-over frequency can be approximated as:

$$\omega_c \approx \frac{I_{qp} \cdot K_{VCO} \cdot R_z}{2\pi \cdot N} \tag{7.2}$$

If the loop gain zero is placed below ω_c by a factor of four and the pole is factor of four above ω_c, the loop will have a a phase margin of approximately $60°$. The loop filter elements can be calculated as follows:

$$R_z = \frac{2\pi \cdot N}{I_{qp} \cdot K_{VCO}} \times \omega_c \tag{7.3}$$

$$C_z = \frac{I_{qp} \cdot K_{VCO}}{2\pi \cdot N} \times \frac{4}{\omega_c^2} \tag{7.4}$$

$$C_p = \frac{I_{qp} \cdot K_{VCO}}{2\pi \cdot N} \times \frac{1}{4 \cdot \omega_c^2} \tag{7.5}$$

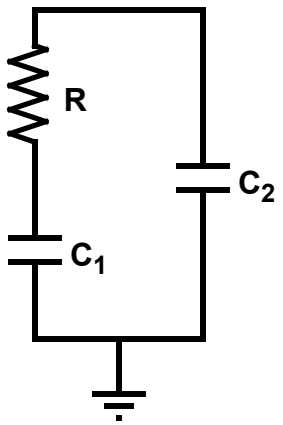


Figure 7.8: Loop filter schematic.

7.1.3 Experimental Results

A dual-band concurrent receiver was implemented in a 0.35μm BiCMOS process technology using the CMOS transistors only [119]. The chip occupies an area of 2.4mm x 2.4mm. Figure 7.9 is the die photo with the main blocks depicted in Figure 7.1 highlighted.

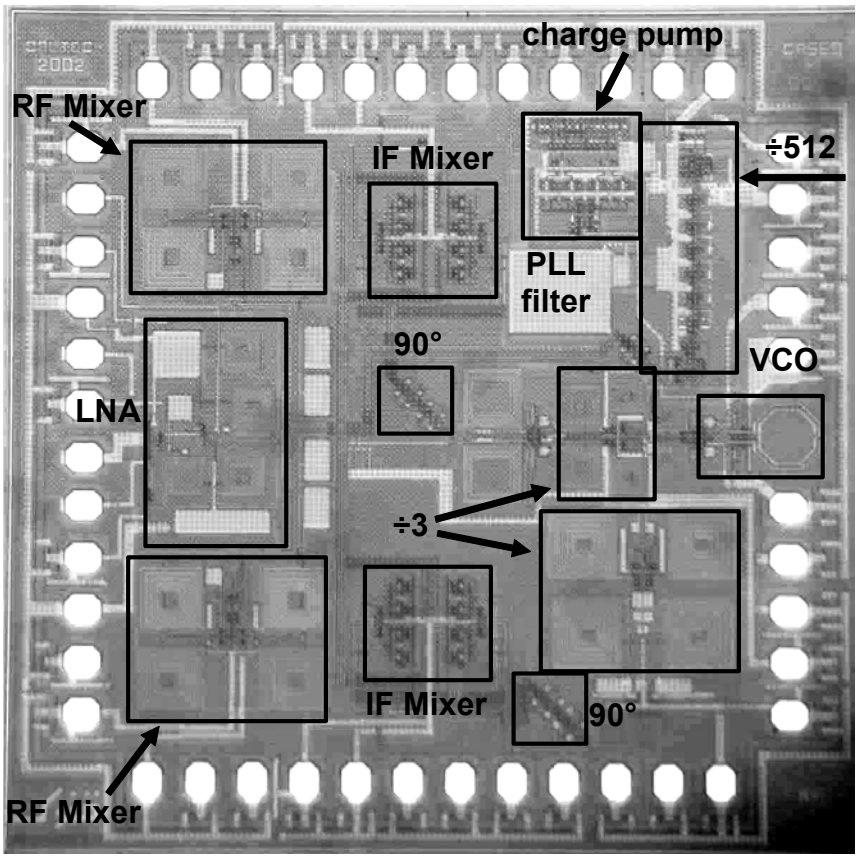


Figure 7.9: Dual-band concurrent receiver die photo.

This receiver was designed for a 3-metal layer version of the process technology with a 3μm thick top metal. Unfortunately, the chip was fabricated in a 4-metal layer version of the same process instead due to an oversight by the foundry. The thickness of the third metal layer in the fabricated chip is approximately one fifth of the original one, and thus, the quality factor of all inductors is severely reduced. Even so, the oscillator was able to start but with a significantly smaller oscillation amplitude. The output of the VCO was

extracted using tuned buffers with a gain smaller than one and fed to the frequency dividers. The low quality factor of the implemented inductors compromised the buffers gain even further. Due to these two combined effects, the master-slave flip-flops used to implement the frequency divider of Figure 7.5 were unable to lock to the input. This unfortunate mistake made it impossible to test the PLL and no further evaluation was performed.

7.2 An Ultra-Low-Power 6.4GHz PLL

Major advances in low-power RF system design have enabled a large span of new wireless applications such as high performance systems that communicate voice, data, and multimedia. As process technologies scale down, the energy costs of computation will also scale down, and fewer gains are expected in power consumption. It is possible to perform more computation to reduce the time of communication. However, the basic architectures and circuit blocks should me optimized for low power at the lowest level possible. In this section, an ultra low power 6.4GHz PLL is presented. This power reduction is possible by reducing the operating voltage.

7.2.1 System Blocks

The PLL diagram is the same as that shown in Figure 7.3. For this implementation, the division ratio is N=128 and the reference frequency is f_{ref} = 50MHz.

To achieve low-power consumption, a supply voltage of 1.0V was chosen. For this application, the complementary cross-coupled oscillator topology was chosen and NMOS transistors were used as varactors. The strategies discussed in Chapter 3 for the optimization of the *LC* tank and oscillator core were implemented for the VCO. The oscillator is designed to have a center frequency of 6.4GHz and 20% of frequency tuning, while drawing 3mA of current from a 1.0V supply.

A master-slave configuration of edge triggered flip-flops are also used as a divide-by-two circuit (Figure 7.5a and Figure 7.5b). Each divider in the chain is optimized for the low voltage of operation while minimizing the current consumption. The total power consumption of the divider chain is 2.88mW.

The phase-frequency detector and charge pump are similar to those shown in Figure 7.6 and Figure 7.7. The second order loop filter shown in Figure 7.8 was designed for a loop bandwidth of 1MHz.

7.2.2 Simulation Results and Power Consumption Comparison

This PLL has been submitted for fabrication in a 80nm CMOS process technology. Due to the extra processing time associated with state of the art technologies, the low power PLL chip is still being fabricated. Table 7.2 summarizes the simulated performance measures of the integrated PLL and Table 7.3 compares its power consumption with previously published low power PLL works. This integrated PLL is expected to attain the lowest power consumption.

Frequency	6.4GHz
Power Consumption	6.5mW
Supply Voltage	1.0V
Reference Spur	48dB down
PLL bandwidth	1MHz
Phase noise @10MHz offset	-120.1dBc/Hz
Settling time	<10μsec.

Table 7.2: Low power 6.4GHz PLL performance summary.

Reference	Frequency	Power consumption
This work	6.6GHz	6.5mW
[120]	1.2GHz	9.12mW
[121]	1.5GHz	10mW
[122]	1GHz	10mW
[123]	900MHz	18mW
[124]	13.4GHz	28mW

Table 7.3: Fully integrated low-power PLLs comparison.

7.3 A Phase-Compensated Fractional-*N* PLL

Fractional-*N* synthesis allows phase-locked-loops to have a frequency resolution finer than the phase detector frequency. This method originates from the digiphase technique introduced in [125]. The commercial version of this technique is referred to as fractional-*N* [126] and its block diagram is shown in Figure 7.10a. The fractional division is obtained by periodically modulating the control input of the dual-modulus divider. For instance, to achieve a $N+\frac{1}{4}$ division ratio, a *N*+1 division is carried out after every three *N* divisions. Thus, a {...,0001,0001,0001,0001,...} sequence of the control signal is required, in this case the *N*+1 division ratio corresponds to 1 and *N* division corresponds to 0. Figure 7.10b shows the timing diagram for the $N+\frac{1}{4}$ division.

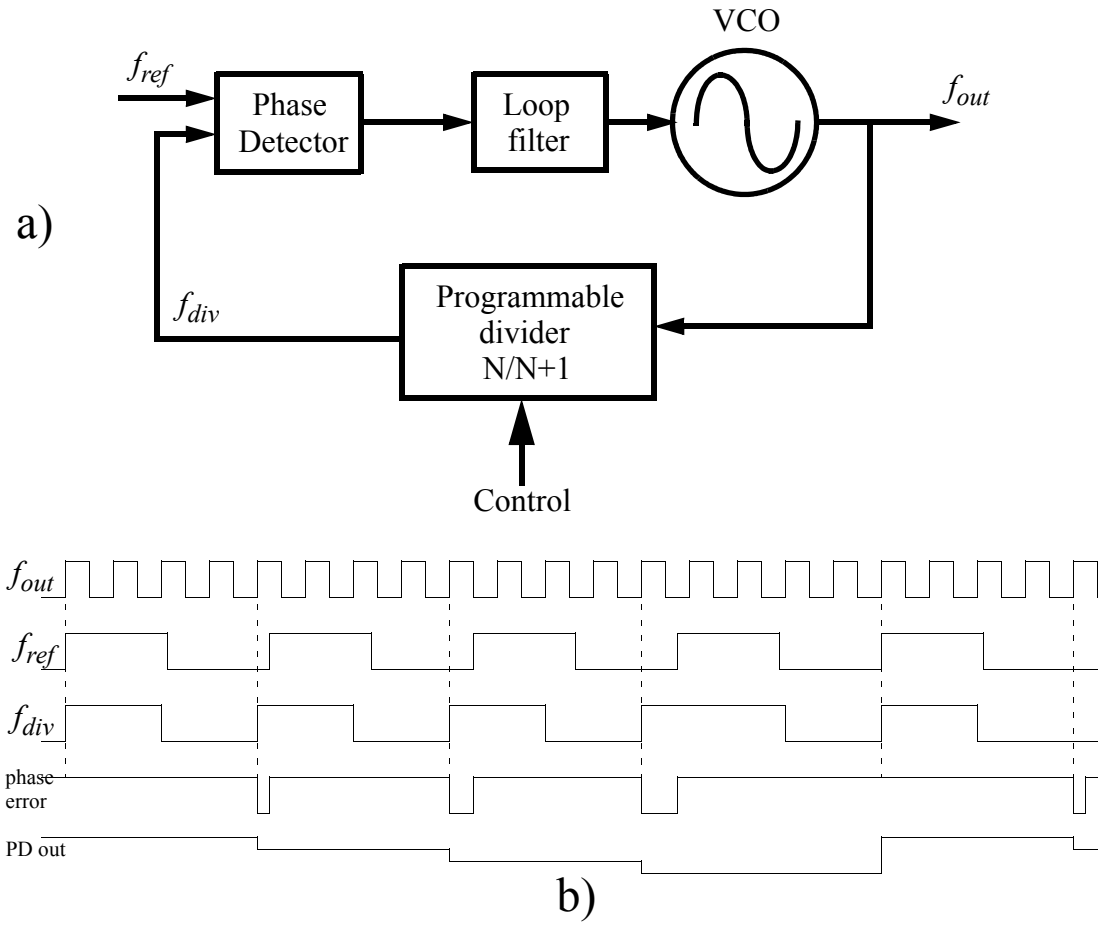


Figure 7.10: Fractional-N frequency synthesis, a) block diagram, b) timing diagram for $N + 1/4$ division.

Since the reference frequency f_{ref} is higher than the frequency resolution in fractional-*N* frequency synthesis, the loop bandwidth of the PLL is not limited by the frequency resolution [17]. However, for low-cost and low-power integrated circuits, the fractional spur limits the overall performance.

7.3.1 Spur Reduction Techniques in Fractional-*N* Frequency Synthesis

The main drawback of the fractional-*N* synthesis is the generation of unwanted spurs in addition to the reference spur. Unless these fractional spurs are suppressed, this method is not useful in practice. Several techniques have been proposed to alleviate this problem.

An oversampling Δ–Σ modulator can be used to interpolate the control signal of the programmable divider of Figure 7.10a [127][128]. This modulator randomizes the choice of the modulus such that the average division factor remains constant. This technique converts the systematic fractional spurs to random noise. The Δ–Σ modulator shapes the resulting noise spectrum such that most of its energy appears at large frequency offsets and thus, the noise in the vicinity of the carrier is small and the noise at higher offsets is suppressed by the low-pass filter after the feedback signal is translated to dc by the phase detector. Although this is a commonly used method for integrated applications, the design complexity is considerably increased. Moreover, Δ–Σ modulators are power hungry and occupy most of the PLL die area [127]-[130].

The phase error cancellation using a digital-to-analog converter (DAC) is the traditional method employed in the digiphase synthesizer to reduce the periodic tones [131]. Figure 7.11 shows the basic architecture and its operation is as follows. The value of the accumulator carries the information of the spurious beat tone, which allows the DAC to predict the phase error for cancellation. Since the phase error is compensated in the voltage domain, this method suffers from analog errors and mismatches. The mismatch results primarily from limited DAC resolution and accuracy.

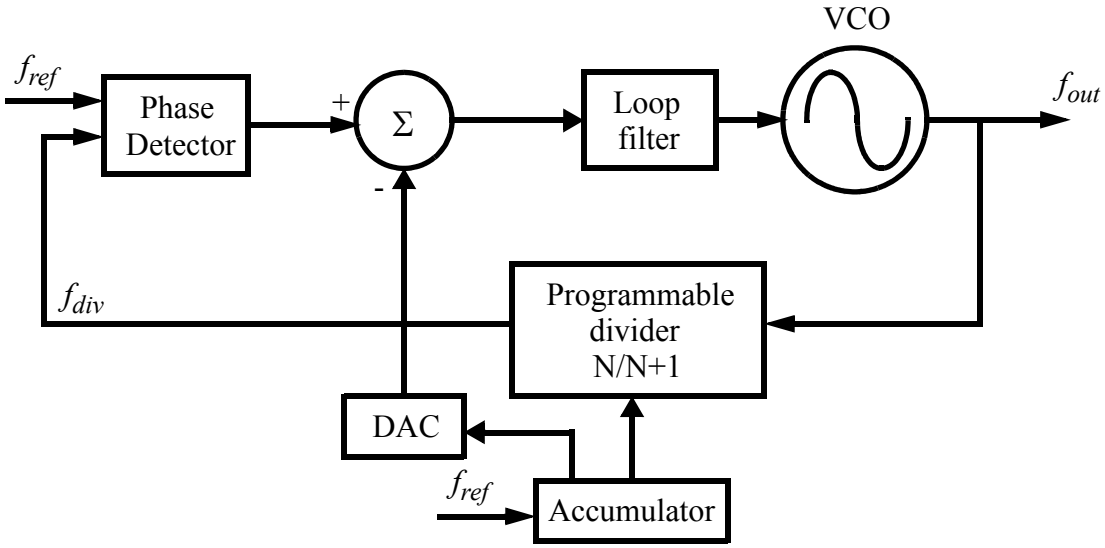


Figure 7.11: DAC estimation method.

A similar approach to compensate for the instantaneous phase errors can be achieved in time domain. Different from the DAC cancellation method, the phase compensation is carried out before the phase-frequency detector as depicted in Figure 7.12a [132]. The on-chip tuning circuit tracks the different amount of phase interpolation as the output frequency varies. A detailed time diagram of the phase interpolation and the on-chip tuning is shown in Figure 7.12b. For the sake of argument, the modulo-4 operation is assumed with a 2-bit accumulator. The output frequency f_{VCO}, with the reference frequency f_{ref} are related as follows,

$$f_{VCO} = f_{ref} \times \left(N + \frac{1}{4}\right) \tag{7.6}$$

thus, the period T_{ref} can be calculated as,

$$T_{ref} = T_{VCO} \times \left(N + \frac{1}{4}\right) = N \cdot T_{VCO} + \frac{T_{VCO}}{4} \tag{7.7}$$

The instantaneous timing error due to the divide-by-*N* is determined by

$$\Delta t_N = T_{ref} - N \cdot T_{VCO} = \frac{1}{4} T_{VCO} \tag{7.8}$$

similarly, the instantaneous timing error due to the divide-by-*N+1* is given by,

$$\Delta t_{N+1} = T_{ref} - (N+1) \cdot T_{VCO} = -\frac{3}{4} T_{VCO} \tag{7.9}$$

Therefore, the timing error sequence is $\{..., \frac{1}{4}T_{VCO}, \frac{1}{4}T_{VCO}, \frac{1}{4}T_{VCO}, -\frac{3}{4}T_{VCO}, ...\}$ for the division ratio of $N + 1/4$. In a similar way, the error sequences for a division ratio of $N + 1/2$ and $N + 3/4$ are $\{..., \frac{1}{2}T_{VCO}, -\frac{1}{2}T_{VCO}, \frac{1}{2}T_{VCO}, -\frac{1}{2}T_{VCO}, ...\}$ and $\{..., \frac{3}{4}T_{VCO}, \frac{3}{4}T_{VCO}, \frac{3}{4}T_{VCO}, -\frac{1}{4}T_{VCO}, ...\}$, respectively. Since the timing error sequence can be predicted from the input of the accumulator, the timing correction is possible if the right phase is added with the opposite direction of the timing error sequence.

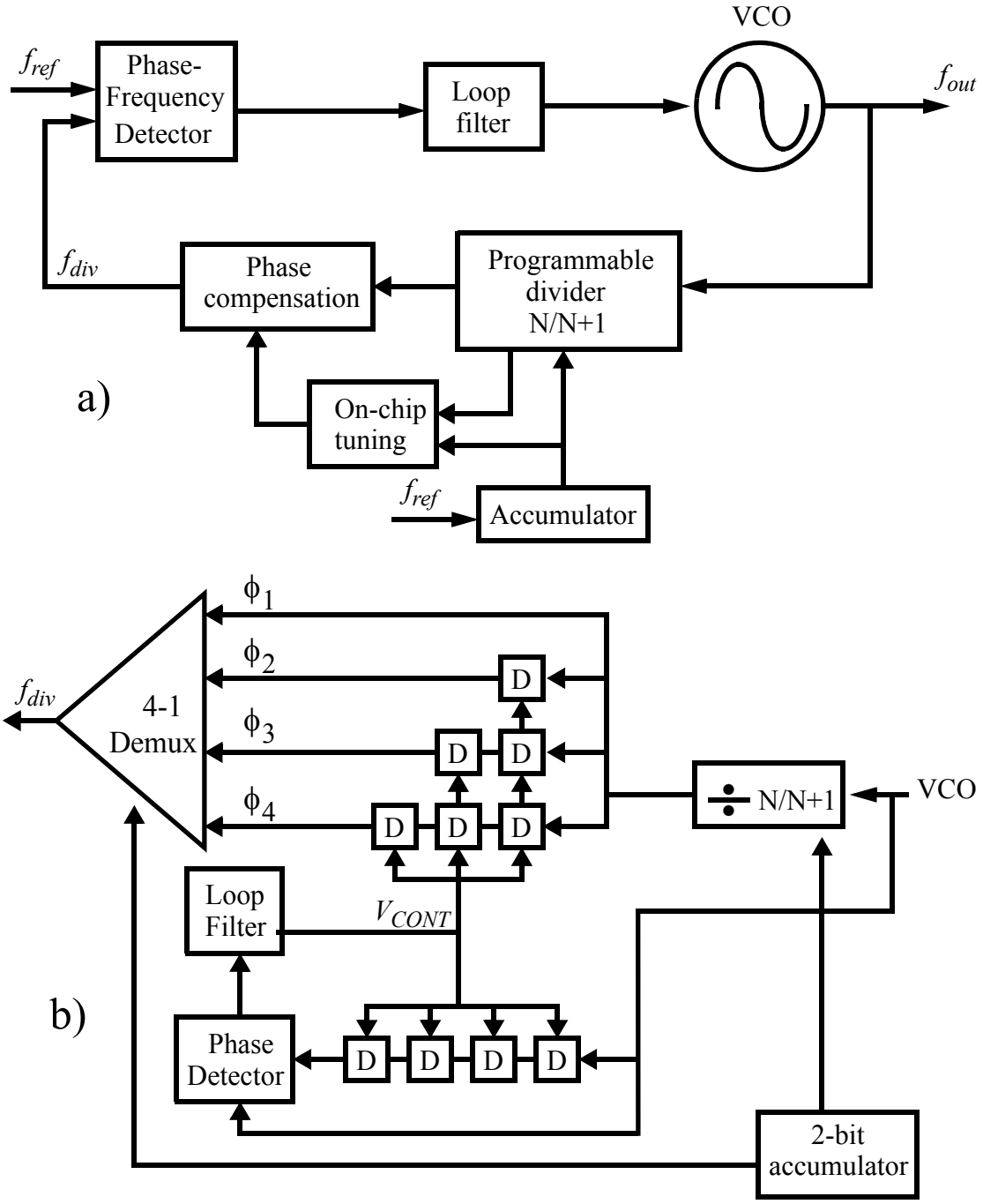


Figure 7.12: Phase compensation method, a) block diagram, b) on-chip tuning achieved with a DLL.

By selecting the phase edge periodically among the interpolator outputs from ϕ_1 to ϕ_4 as shown in Figure 7.12b, the selected clock will be phase-locked to the reference clock without generating instantaneous phase error.

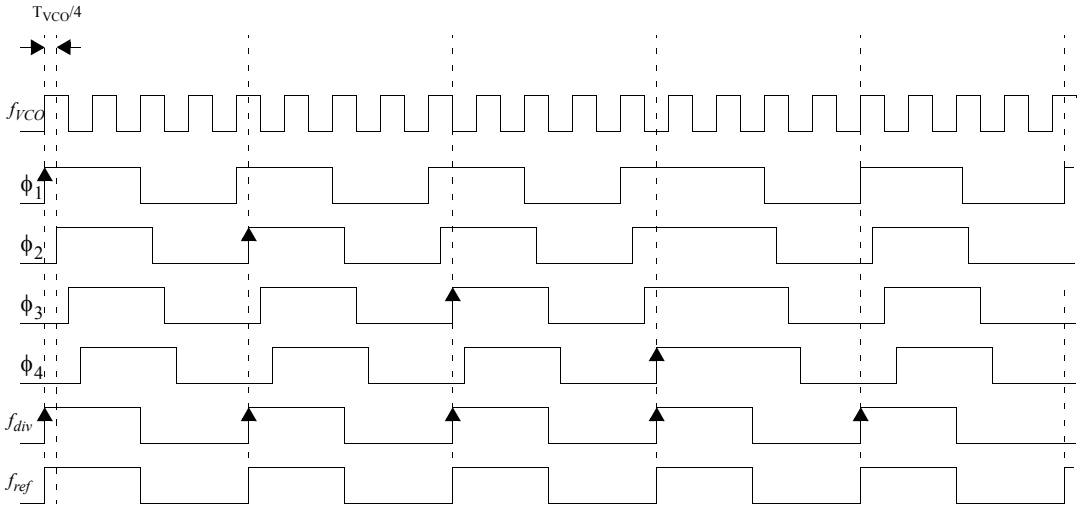


Figure 7.13: Phase-compensated PLL timing diagram for $4 + 1/4$ division.

As an example, the timing diagram for a division ratio of $4 + 1/4$ is depicted in Figure 7.13. A fixed delay element would not offer enough cancellation since the timing error Δt_N and Δt_{N+1} depend on the output frequency. Therefore, a delay-locked-loop, or DLL, should be employed to adjust the delay depending on the output frequency. It would also provide a delay that is immune to process and temperature variations.

7.3.2 A 3.2GHz Phase Compensated Fractional-*N* PLL

In the following subsections, the circuit building blocks for the phase compensated PLL will be discussed. For this particular implementation, a PLL frequency of 3.2GHz is targeted and a division ratio of 64+1/4 is intended for the demonstration of this technique. To achieve low power consumption, a supply voltage of 1.0V was chosen.

7.3.2.1 Delay Locked Loop

In principle, the DLL would operate at the PLL frequency, thus, the power consumption is quite high as it requires the delay elements to operate at full rate. It is possible to decrease the power consumption of the DLL by using the in-phase and quadrature outputs of a divide-by-four stage as shown in Figure 7.14. In this approach, the DLL operates at one fourth of the PLL frequency decreasing the DLL power consumption by almost a factor of 4. Also, three delay cells instead of five can be used of the generation of the phases ϕ_1 to ϕ_4 if their fan out is kept the same.

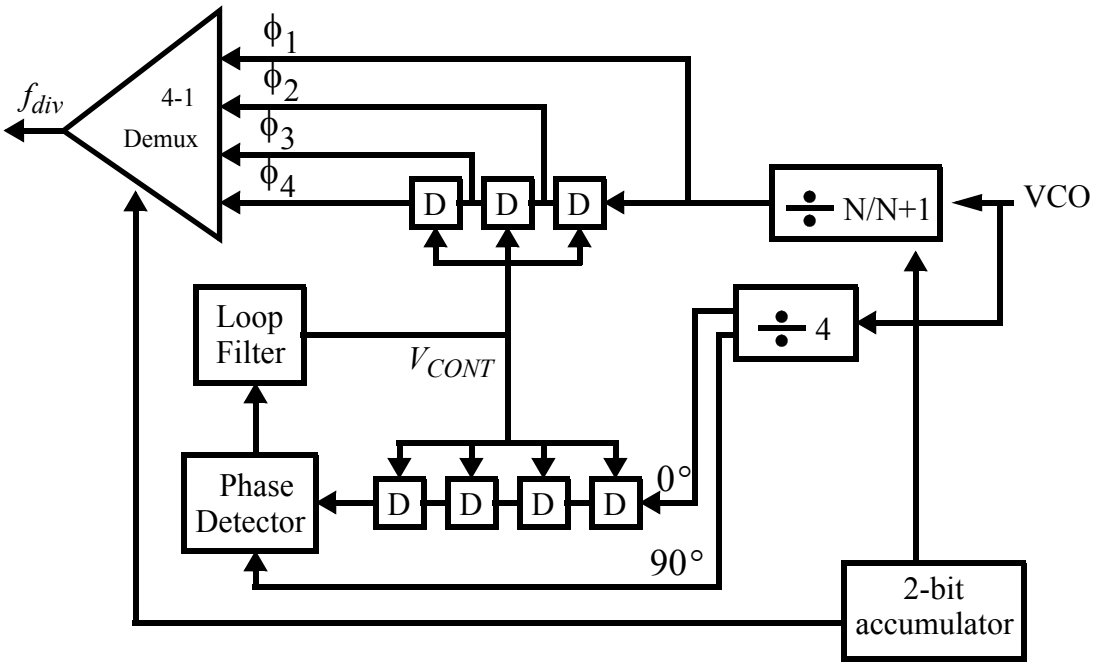


Figure 7.14: Modified DLL block diagram operating at one fourth the data rate.

The delay elements are comprised by two CMOS inverters with a variable *RC* load (Figure 7.15). MOS transistors are used as capacitors and an NMOS transistor operating mostly in triode region is used as a variable resistor changing the *RC* time constant and thus, modifying the effective delay of the cell. The second inverter serves as a buffer to re-shape the distorted output from the loaded first inverter. To compensate for process and

temperature variations, the tunability of the delay in this cell is designed to cover 50% to 200% of the required delay. In order to have the same signal delay in each of the cells of Figure 7.14, the loading at the output of each delay cell must be equal and the input waveform should have the same shape and rise and fall times. Therefore, dummy loading stages and capacitors have been added to equalize any mismatch in the output loading or extra parasitic capacitances in the layout.

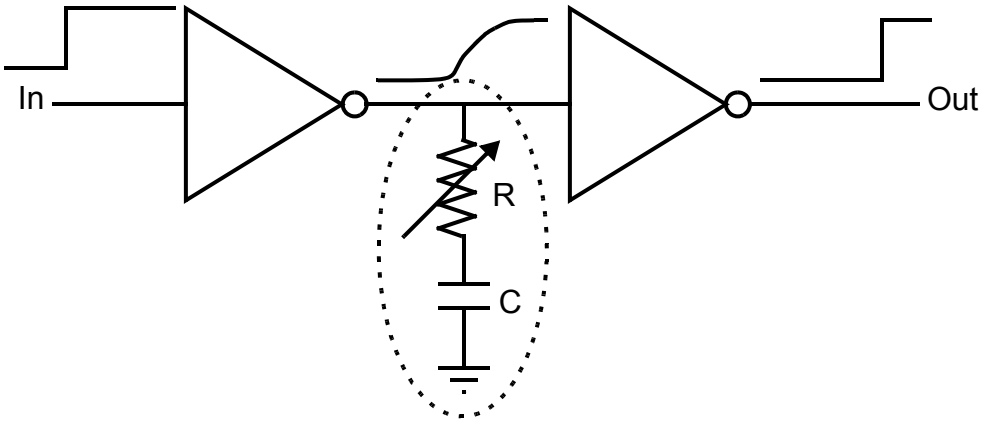


Figure 7.15: Delay element block diagram.

As the comparison rate in the DLL is $f_{VCO}/4$, a digital phase-only detector is implemented with a fast-switching current steering charge pump. The total power consumption of the DLL including the divide-by-four circuit is 2.1mW.

7.3.2.2 PLL Building Blocks

For this application, the complementary cross-coupled oscillator topology was chosen and NMOS transistors were used as varactors. The strategies discussed in Chapter 3 for the optimization of the *LC* tank and oscillator core were implemented for the VCO. The oscillator is designed to have a center frequency of 3.2GHz and 20% of frequency tuning, while drawing 2mA of current from a 1.0V supply.

A 64/65 prescaler is comprised by a synchronous divide-by-4/5 part and an asynchronous divide-by-16 part as shown in Figure 7.16. The extra gates are embedded

into their respective synchronous edge-triggered latches to achieve high frequency of operation. Master-slave flip-flops are used as the asynchronous divide-by-two circuits. The total power consumption of the prescaler is 2.6mW.

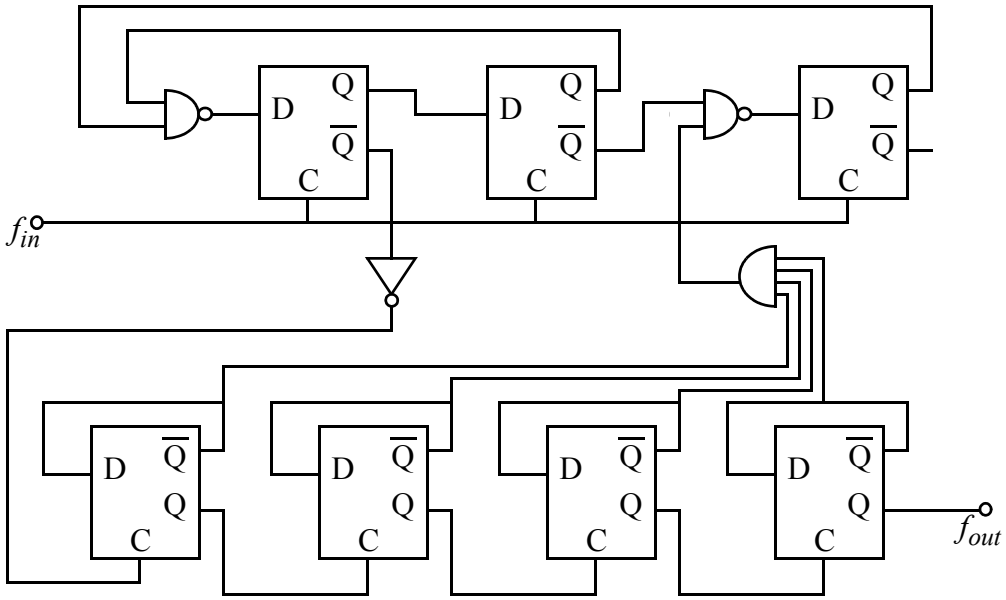


Figure 7.16: Dual-modulus prescaler architecture.

The phase-frequency detector and charge pump are the same as the 6.6GHz PLL presented in Section 7.2. They operate at the same frequency ranges and 1.0V supply. The second order loop filter shown in Figure 7.8 was designed for a loop bandwidth of 1MHz.

7.3.3 Simulation Results and Comparison

This PLL has been submitted for fabrication in a 80nm CMOS process technology. Similar to the ultra-low-power PLLL presented in the previous subsection, the phase compensated fractional-*N* PLL chip is being still fabricated. Table 7.4 summarizes the simulated performance measures of the integrated PLL.

It is shown in simulations that using this technique, a 25dB fractional-*N* spur reduction can be achieved.

Frequency	3.2GHz
Power Consumption (PLL+DLL)	10mW
Supply Voltage	1.0V
Reference Spur	53dB down
Fractional Spur	58dB down
Fractional Spur with out phase compensation	33dB down
Phase noise @10MHz offset	-128.5dBc/Hz
PLL bandwidth	1MHz
Settling time	<10μsec.

Table 7.4: 3.2GHz phase-compensated PLL performance summary.

7.4 Summary

The design and implementation of three integrated phase-locked-loops were described in this Chapter. First, a 6.6GHz PLL for application in the first concurrent dual band CMOS receiver [10] was presented. Diligent frequency planning allows the generation of three local oscillator signals using only one PLL in the entire receiver, thereby reducing chip area and power consumption significantly. The design issues of an ultra-low-power PLL prototype implemented in a sub-micron CMOS processes were also discussed. The design of a low-power 3.2GHz PLL implementing a spur reduction technique in fractional-N frequency synthesis was also introduced. It uses on-chip delay-locked-loop tuning scheme that attenuates the fractional spur independent of the output frequency and process variations.

Chapter 8 *Conclusion*

The design of fully-integrated low-noise oscillators has been one of the major challenges towards the implementation of the single-chip CMOS-only radio. Unfortunately, the driving forces behind CMOS technology are digital applications and thus, are not optimized for analog or RF circuits. In these process technologies, the silicon substrate is fairly conductive and increases the signal loss because of the energy coupled into the substrate. Moreover, the thin metal layers readily available in these technologies present high ohmic loss, which is exacerbated due to the skin effect at high frequencies. These result in lossy passive components. Also, the transistor devices available in these process technologies generate high active device noise. Therefore, fully-integrated CMOS oscillator circuits suffer from a worse noise performance than modules fabricated using discrete components.

With the goal of overcoming these drawbacks of CMOS technology, novel oscillator circuit topologies and passive structures have been presented in this dissertation. These new structures demonstrate significant improvements in performance compared to existing devices in CMOS. The contributions of our study included the development of original topologies and concepts together with practical implications in the area of integrated frequency generation.

8.1 Summary

A new noise-shifting differential Colpitts VCO topology was presented. It is less sensitive to the noise generated by the active devices through cyclostationary noise alignment, while improving the start-up condition. A general methodology has been

devised for the optimization of this oscillator. The superior performance of this topology is demonstrated through measurement results of a CMOS VCO prototype that achieves 8dB better phase noise at 3MHz offset than the complementary cross-coupled oscillator topology presented in [24] under similar conditions. This test VCO achieves the largest *PFTN* and the fourth largest *PFN* among previously published integrated oscillators.

A novel circular-geometry oscillator topology has been introduced that allows the use of slab inductors for high-frequency and low-phase noise oscillator applications. These inductors present significantly higher quality factors and self-resonance frequencies when compared to single- and multi-turn spiral inductors for small inductance values required for high frequency operation. A general methodology to suppress the undesired oscillation modes and achieve a stable dc bias point has been devised and its efficacy proven experimentally. This topology is general and can be used to implement oscillators with any number of corners and with a variety of active cores. Two test oscillator have been fabricated as a proof of concept and achieve some of the largest figures of merit among previously published high frequency oscillators.

The trade-off between the phase noise performance and the quadrature and in-phase signal accuracy has been investigated and a general design methodology was devised to optimally couple quadrature oscillators. A CMOS oscillator prototype optimized using this methodology is fabricated and its phase noise enhancement was verified experimentally.

The design and implementation of three integrated phase-locked-loops were described. First, a 6.6GHz PLL for application in the first concurrent dual band CMOS receiver [10] was presented. Diligent frequency-planning allows the generation of the three local oscillator signals required by the entire receiver using only one PLL. Thereby reducing chip area and power consumption significantly. The design issues of an ultra-low-power PLL prototype implemented in a sub-micron CMOS process was also discussed. The design of a low-power 3.2GHz PLL implementing a spur reduction

technique in fractional-N frequency synthesis was introduced. It uses an on-chip delay-locked-loop tuning scheme that attenuates the fractional spur independent of the output frequency and process variations.

A theoretical framework which shows the capacity limits of integrated capacitors was also offered. This new framework can be used to evaluate the performance of existing capacitive structures and leads to two new purely lateral capacitors. These structures demonstrate: higher capacitance density, better matching and tolerance properties, and higher self-resonance frequency than previously reported capacitor structures, MIM and standard *HPP* capacitors, while maintaining a comparable quality factor. These two new structures are standard CMOS compatible and do not need an extra processing step, as is the case with special MIM capacitors.

8.2 Recommendations for Future Investigations

The oscillator topologies presented in this work can be further explored for different frequencies and process technologies. A promising circular-geometry oscillator implementation using the noise shifting differential Colpitts topology as an oscillator core has the potential of achieving even better phase noise performance than the oscillator prototypes presented in Chapter 4.

Using conventional silicon CMOS technologies, it should be possible to implement circular-geometry oscillators for frequencies of 50GHz and beyond using 0.12μm technology or technologies with finer channel length. These high frequency oscillators can be superior in terms of phase noise and figures of merit than conventional oscillators implemented with single-turn spiral inductors [71][72].

Another promising application of the circular-geometry oscillators is that of a high-power oscillator. In this application, the oscillator output can directly drive a 50Ω load with output power in the watts range. A similar impedance-transformation method to

that presented in [133] can be used in order to combine the power of several oscillator cores (or oscillator corners) to achieve high output powers.

Recently, it has been proposed the use of magnetically coupled resonators to enhance the effective quality factor of the tank [134]-[136]. The new oscillator topologies presented in this dissertation can benefit from this higher effective resonator quality factor and achieve lower phase noise. Due to geometry, low impedance and high quality factor coupled slab inductors can be easily laid out in the circular-geometry oscillator topology presented in Chapter 4. The center point connection, or *cross*, can also be used to suppress the undesired modes of oscillation associated with the set of coupled inductors.

There are still some remaining issues in the context of purely lateral field capacitor structures. Increasing the lateral separation of the VPP and VB structures beyond the minimum metal separation allowed by the process technology would decrease the capacitance density of such structures. However, the variations on the periphery of the metal layers and vias remain constant as it is determined by the process technology of interest. This would translate to smaller fractional variations of the capacitance of these structures across the wafer that would enhance their tolerances and matching properties. Therefore, the trade offs between capacitance density versus matching properties have to be explored further and verified experimentally. Another interesting scenario occurs when the capacitance density of these structures is compromised by using plates and bars that are wider than the minimum specified by the process technology of interest and with more than one via rows. This in turn would decrease the series resistance associated to the structures achieving lower loss and hence, higher quality factors. In this context, the trade offs between capacitance density and quality factor can also be explored and verified experimentally.

As a summary, the work presented in this dissertation has opened some directions for future research in the fields of low noise and high frequency oscillator topologies and the optimization of passive structures.

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