NONLINEAR ELECTRICAL PROPERTIES OF ONE-DIMENSIONAL NANOSTRUCTURES

Thesis by

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Abstract

A general method is first reported for reliably fabricating highly-ordered conventional superconductor nanowire arrays, with good control over nanowire cross section (down to 10 nm by 11 nm) and length (up to 200 microns). Nanowire size effects are systematically studied through electrical measurements and explained with theories. A comprehensive investigation of influence of nanowire length on superconductivity is reported for the first time.

We further demonstrate the preparation and electrical properties of high-temperature superconductor nanowires. We find that high-temperature superconductivity can be retained in nanowires ~10 nm in width and >100 microns in length. All nanowires exhibit a superconducting transition above liquid nitrogen temperature, and a transition temperature width that depends strongly upon the nanowire dimensions.

The experience gained from the above projects has allowed for the fabrication of superconductor films patterned with ultrahigh-density (pitch ~30 nm) two-dimensional arrays of nano-holes. Significantly enhanced critical currents are observed in such systems.

We then describe a method for the assembly of nanoparticles into granular solids that can be tuned continuously from two dimensions to one dimension, and establish how electron transport evolves between these limits. We find that the energy barriers to transport increase in the one-dimensional limit, in both the variable-range-hopping and

sequential-tunneling regimes. Furthermore, in the sequential-tunneling regime, we find an unexpected relationship that is peculiar to one-dimensional systems, between the temperature and the voltage at which the conductance becomes appreciable. These results are explained by extrapolating existing theories to one dimension.

We also describe an approach to combine the geometric confinement of a Si nanowire and the electric field confinement from an array of ultrahigh-density top gates to form a concatenated array of coupled quantum dots. Reproducible confinement and coupling effects are observed.

We have achieved single-atomic resolution in our scanning tunneling microscopy studies of graphene sheets on SiO_2 substrates, from which we discovered significant changes in electronic states for bended regions in graphene sheets. We have also carried out the first systematic study on local conductance variations in graphene. Our results suggest large local variations in both the morphology and the electrical properties of graphene.

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Chapter 1

Thesis Overview

One-dimensional (1D) nanostructures have attracted widespread research interests for their novel physical properties and potential applications in nanoelectronic circuits. Quantum mechanical effects become important in such systems due to geometric confinement in the lateral dimensions (size effects), and new physics emerges and dominates their properties. The very small length scales and energy scales of such systems, however, make the investigation of such new physics challenging. In particular, 1D systems with highly nonlinear (non-ohmic) electrical properties (e.g., superconductors and granular conductors) have proven to be difficult to investigate. These problems are addressed in this thesis through the development of precisely controlled nano-fabrication techniques and low temperature electrical measurements. Experimental results are also systematically compared and explained with theories. Three major research areas are discussed in this thesis, each of which further contains several different research projects.

Quasi-One-Dimensional Superconductors.

When prepared as sufficiently narrow diameter (~10 nm) nanowires, superconductors become quasi-one-dimensional and exhibit unique properties. Such nanowires are an ideal test-bed for the investigation of size effects on superconductivity, and have potential applications in nanoelectronic circuits. Quite different from normal-

metal or semiconductor nanowires, precise controls over nanowire length and cross sectional area are both crucial for achieving a quantitative understanding of such systems. However, previous studies on superconductor nanowires have only achieved limited dimensional and positional control and very limited materials flexibility. In particular, the class of high-temperature superconductors has been unavailable for study as nanowires.

A general method is reported in Chapter 2 for reliably fabricating highly-ordered superconductor nanowire arrays, with good control over nanowire cross section (down to 10 nm by 11 nm) and length (up to 200 μm), and with full compatibility with device processing methods. Nanowire size effects are systematically studied through electrical measurements, and quantitatively explained with theories. In particular, for conventional superconductor nanowires, a comprehensive investigation of influence of nanowire length on superconductivity is reported for the first time, from which characteristic quasiparticle diffusion lengths are extracted.[1]

We further demonstrate in Chapter 3 the preparation and electrical properties of high-temperature superconductor nanowires for the first time. We find that high-temperature superconductivity can be retained in nanowires ~10 nm in width and >100 μm in length. All nanowires exhibit a superconducting transition above liquid nitrogen temperature, and a transition temperature width that depends strongly upon the nanowire dimensions. These nanowires can function as superconducting nanoelectronic components over much wider temperature ranges as compared to conventional superconductor nanowires. We also demonstrate the applicability of phase-slip theories in explaining the size effects in high-temperature superconductor nanowires for the first time.[2]

The experience we gained from the above two projects has recently allowed for the fabrication of superconductor films patterned with ultrahigh-density two-dimensional arrays of nano-holes. Because the hole-to-hole distances in the film are extremely small (~30 nm), the holes effectively act as pinning centers for supercurrent vortices, and drastically enhanced critical currents are observed comparing to unpatterned films. These results are discussed in Chapter 6.

One-Dimensional Granular Conductors and Quantum Dot Arrays.

Sufficiently small (<100 nm) nanoparticles exhibit charge and energy quantization and are often called ‘‘quantum dots’’, referring to the quantum confinement in all three spatial dimensions. Granular conductors are solids comprised of densely-packed quantum dots, and their electrical properties are determined by the size, composition, and packing of the composite quantum dots. The ability to control these properties in two- and three-dimensional granular conductors (2D and 3D quantum dot arrays) has made such systems prototypes for investigating new physics. In contrast, attempts to assemble quantum dots into ordered 1D (single-file nanoparticle arrays/chains) or quasi-1D granular structures have only achieved limited success, largely due to the difficulty in obtaining continuously connected 1D superstructures.

A novel approach is reported in Chapter 4 for assembling closest-packed arrays of 5 nm and larger quantum dots that permits a continuous, precise tuning of the resultant granular solid from 2D to 1D. We report on the electrical properties of the novel 1D granular solids, and systematically establish how electron transport through these systems

evolves from the 2D limit to the strictly 1D limit. We find the electrical properties of 1D granular conductors are fundamentally different from 2D systems. In the low-voltage variable-range-hopping regime, we experimentally determine the relevant dimensional factor that describes the 2D-1D transition. In the high-voltage sequential-tunneling regime, we find an unexpected sublinear relationship between the conductance onset voltage and the temperature, which appears peculiar to strictly 1D systems. These results are explained by extrapolating existing granular conductor theories to 1D.[3]

Chapter 5 describes a different approach to study 1D arrays of quantum dots, in which an array of ultrahigh-density metal nanowires (serving as top gate electrodes) is fabricated perpendicular to and on top of an individual Si nanowire. The combination of geometric confinement from the width of the underlying Si nanowire and the electric field confinement from the ultrahigh-density top gates has for the first time allowed for the controlled formation of a concatenated 1D array of small (17 nm) quantum dots coupled in series along the length of the Si nanowire. Reproducible confinement and coupling effects are observed with large energy scales (~10 meV) through low-temperature electrical measurements, and compared with theory.[4]

Graphene.

Graphene is the name given to a flat monolayer of carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice, and is a basic building block for graphitic materials of all other dimensionalities. As a newly discovered material,

graphene has attracted widespread research interests for its outstanding electrical and mechanical properties.

Chapter 7 contains a short discussion on my ongoing research on graphene, including studies towards the fabrication of nano-ribbon arrays for potential applications in nanoelectronic circuits, and scanning tunneling microscopy (STM) studies of graphene sheets on SiO_2 substrates. Single-atomic resolution is achieved in our STM studies, from which we discovered significant changes in electronic states for bended regions in graphene sheets. We have also carried out the first systematic study on local conductance variations in graphene, the results of which indicate coupling effects from the underlying SiO_2 substrate. Our results suggest large local variations in both the morphology and the electrical properties of the same graphene sheet, challenging previous assumptions.

Other Research Projects.

During my graduate study, I also worked on several other projects through close collaboration with other lab members and participation in the synergetic projects in the lab, including size-dependent transport and thermoelectric properties of bismuth nanowires,[5] azidation of silicon(111) surfaces,[6] ultrahigh-density molecular electronic memory circuits,[7] and switching kinetics of bistable [2]rotaxanes.[8] These, however, will not be discussed in detail in this thesis. Interested readers are referred to the respective publications and the theses by A. Boukai, J. E. Green, and J. W. Choi.

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#: Indicates equal contributions.

Chapter 2

Quasi-One-Dimensional Conventional Superconductor Nanowire Arrays

The contents presented in this chapter are based on K. Xu and J. R. Heath, "Controlled fabrication and electrical properties of long quasi-one-dimensional superconducting nanowire arrays," *Nano Letters*, 8, 136-141 (2008). (Ref. [1])

2.1 Introduction

A superconductor wire becomes quasi-one-dimensional (quasi-1D) when its diameter is comparable to or smaller than the material-dependent superconducting coherence length ξ (~100 nm for elemental superconductors) and magnetic penetration depth λ (~40 nm for elemental superconductors). In such systems, the Ginzburg–Landau complex order parameter ψ (and consequently, the local density of superconducting electrons, $|\psi|^2$,) becomes constant over the cross section,[2,3] and is only a function of the position x along the wire. Quasi-1D superconductors provide an ideal test-bed for investigating superconductivity in finite size. In a strictly 1D system, superconductivity is not possible.[4]

Below the superconducting transition temperature, T_c, the electrical resistance of a bulk superconductor quickly drops to zero, while the resistance in a quasi-1D system decreases more gradually (Fig. 2-1A). This finite resistance at $T<T_c$ is a consequence of

Thermally Activated Phase Slip (TAPS) and Quantum Phase Slip (QPS) processes.[2,5,6] For TAPS, thermodynamic fluctuations (~kT) stochastically and instantaneously depress $|\psi|$ to zero at a random point along the wire, resulting in a local non-superconducting state. Because ψ is constant over the cross section, the local non-superconducting state blocks the entire cross section, and so a superconducting current (supercurrent) cannot pass through (Fig. 2-1B). A measurable resistance thus appears. In contrast, although thermodynamic fluctuations may also lead to instantaneous local non-superconducting states (~ξ in size) in bulk superconductors, supercurrents can always find alternative paths to bypass (get around) such local states (Fig. 2-1C), and zero-resistance can still be achieved.

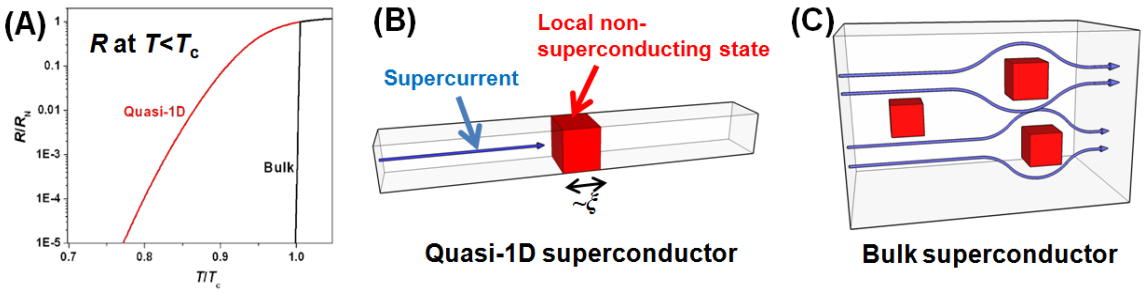

Figure 2-1. Schematics of quasi-one-dimensional (quasi-1D) superconductors in comparison with bulk superconductors. (A): Schematics of the temperature dependence of resistance for a quasi-1D superconductor and a bulk superconductor. The resistance (R) is normalized by the normal state resistance, R_N. (B): Schematics showing the appearance of a local non-superconducting state that blocks the passage of a supercurrent in a quasi-1D superconductor. (C): Schematics showing that supercurrents can bypass local non-superconducting states in a bulk superconductor.

Formally, the depression of local $|\psi|$ to zero allows for a sudden change of 2π in the phase of ψ and a finite voltage drop across the wire. Such processes are thus named "phase slips".[2] The energy required to locally depress $|\psi|$ is

$$\Delta F = \frac{8\sqrt{2}}{3}\frac{H_c^2}{8\pi}A\xi \qquad (1)$$

H_c is the thermodynamic critical field of the superconductor, and A is the cross-section area of the wire. Equation (1) represents the superconducting condensation energy within a wire segment of length $\sim\xi$, and suggests thinner wires have a smaller energy barrier for phase-slip processes and therefore a slower decrease of resistance for $T<T_c$. This can be seen from the resistance formula

$$R_{\mathrm{TAPS}} = \frac{\pi\hbar^2\Omega}{2e^2kT}e^{-\Delta F/kT} \qquad (2)$$

where $\Omega = (L/\xi)(\Delta F/kT)^{1/2}(1/\tau_{GL})$, L is wire length, and $\tau_{GL} = \pi\hbar/8k(T_c - T)$ is the Ginzburg–Landau relaxation time. Equation (2) predicts zero resistance when T approaches zero since $kT<<\Delta F$. Even then, however, ΔF might[6-9] be tunneled via quantum fluctuations, leading to QPS and a finite resistance when T approaches zero.

Because both $\xi(T) \approx \xi(0)(1-T/T_c)^{-1/2}$ and $\lambda(T) \approx \lambda(0)[1-(T/T_c)^4]^{-1/2}$ are large for T close to T_c, quasi-1D superconductivity was first reported in micron-size filaments within several millikelvins just below T_c.[2,3,10,11] However, for lower temperatures ξ and λ both rapidly reduce to their zero-temperature limits. For pure metals, $\lambda(0)$ is ~40 nm, while $\xi(0)$ varies from ~1 μm to 40 nm. Consequently, for $T<T_c$, strong quasi-1D behavior requires nanowires (NWs) with diameters substantially below 40 nm. This is beyond the limits of conventional lithographic fabrication methods, and necessitates non-traditional

fabrication methods. In early studies, Giordano *et al.* obtained superconducting In and PbIn NWs ~50 nm in diameter with limited dimensional control basing on a step-edge technique, and modeled their results within the context of TAPS and QPS.[7,12]

Recently, Bezryadin *et al.* developed a new method to produce superconducting NWs, based on the sputter deposition of MoGe or Nb onto suspended carbon nanotube (CNT) or DNA molecule templates.[13-15] This method can produce NWs ~10 nm in diameter and ~100 nm in length, but is only applicable to the limited types of materials that wet the templates. Other materials form disconnected beads along the template.[16,17] The method relies on the stochastic bridging of CNT/DNA templates onto predefined trenches, and the location and dimensions of the NWs are thus hard to control. The suspended structure also limits the length of the NWs to be ~200 nm. This leads to two potential problems: 1) Cooper pairs from the superconducting contacts may tunnel through the very short NW channel and result in proximity-induced superconductivity, even when the NW itself is a normal material. Indeed, superconductivity has been observed in *uncoated* CNTs ~300 nm in length bridging superconductive Re, Ta or Nb contacts.[18,19] 2) The difficulties in producing NWs of varied lengths also complicate the discussion of whether there is a well-defined critical NW size limit beyond which superconductivity cannot be retained. Some experiments suggest that superconductivity disappears if the normal state resistance of the NW, R_N, is larger than $R_q = h/4e^2 = 6.5$ kΩ.[13,20,21] This argument implies two superconducting NWs with R_N just below R_q would lose their superconductivity when connected in series (as now $2R_N > R_q$), and suggests that superconductivity is hard to achieve in long NWs.

Tian *et al.* and Michotte *et al.* fabricated embedded superconducting NW arrays by electrodeposition into porous membranes.[22-26] This method can produce NWs >20 nm in diameter and ~10 μm in length, but is only applicable to the limited types of metals that can be electrodeposited. The wire-to-wire diameter variation for the obtained NWs in the same array is relatively large (~10 nm).[23] Also, transport measurements on embedded arrays are typically limited to two-point measurements, and the number of NWs being measured is uncertain.[23,25]

Starting from a ~100 nm-wide Al wire, Zgirski *et al.* monitored the evolution of superconductivity of the wire between subsequent thin-down sessions, down to a width of ~8 nm, where superconductivity disappears.[8] Dimensions are difficult to control with this method, and the non-selective physical thin-down process results in serious etching of the substrate, making the method incompatible with other circuits on the substrate.

Altomare *et al.* fabricated superconducting NWs ~10 nm in diameter by depositing Al onto a thin InP edge obtained by selective etching of the side edge of a GaAs wafer that has a molecular-beam epitaxy (MBE) grown InP layer.[9,27] This method bears a resemblance to our previous work on Pt NWs.[28-30] However, without a subsequent pattern transfer step, NWs thus fabricated are on the very thin side edges of GaAs wafers close to the surface (< 2 μm),[27] making subsequent processing difficult. In addition, highly directional evaporation of the superconductor material is required for the method, which is not available for many superconductor materials.

To sum up, previous experiments have together painted an incomplete picture of quasi-1D superconductors. Issues such as proximity effects, the lack of 4-point contacts, limited materials flexibility and limited NW dimensional control are unresolved.

In this chapter, we describe[1] a general method for reliably fabricating quasi-1D superconductor nanowire arrays, with good control over nanowire cross section and length, and with full compatibility with device processing methods. As shall be discussed in Chapter 3, this method is generally applicable, including to high T_c materials, as long as a thin film of the material is available. Nearly atomically straight Nb NWs with widths ranging from bulk-like to 10 nm and aspect ratios approaching 10^4 are prepared. Four-point electrical measurements indicate the NWs are uniform and defect-free, and good reproducibility is found between NWs with the same *designed* cross sections. Thinner NWs exhibit a slower relative decrease of resistance below T_c, and more pronounced contributions from QPS in the low-temperature limit. The ability to fabricate very long (up to 100 μm) NWs with different lengths but identical cross sections has for the first time allowed for the investigation of length's sole influence on superconductivity in NWs, from which characteristic quasiparticle diffusion lengths are extracted. All results are interpreted within the context of phase-slip models.

2.2 Fabrication of conventional superconductor nanowire arrays

Superconducting NW Arrays were prepared using Superlattice Nanowire Pattern Transfer (SNAP), which translates the atomic control over the film thicknesses of a superlattice into control over the width and spacing of metal and semiconductor NWs.[28-

[30] In this method, Pt NWs are obtained by directional e-beam evaporation onto the raised edges of a differentially etched edge of a GaAs/$Al_xGa_{(1-x)}As$ superlattice (cf. Fig. 2-3A), and transferred onto a substrate.

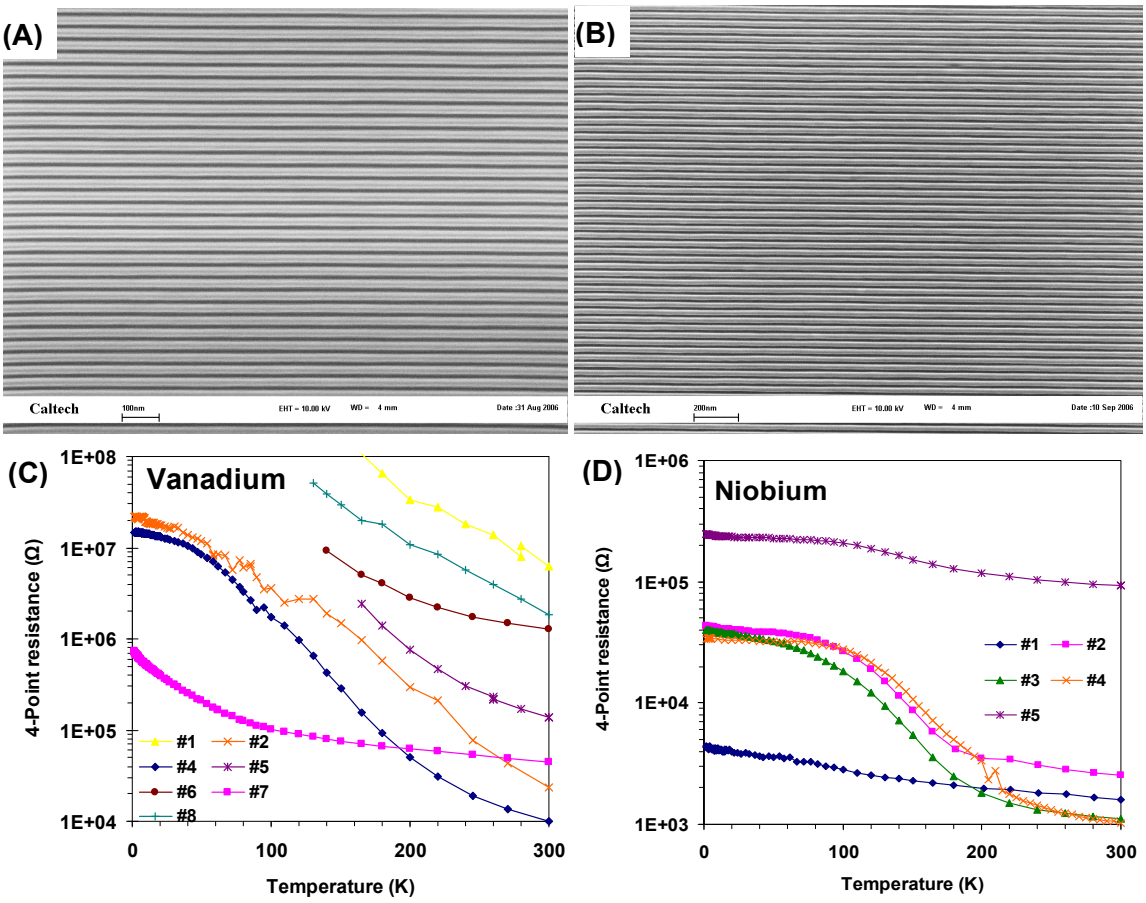

Figure 2-2. Vanadium and niobium nanowire (NW) arrays fabricated by direct application of the SNAP process, using the corresponding metals to replace Pt for the directional e-beam evaporation step. (A): Scanning electron microscope (SEM) image of an array of 20 nm wide vanadium NWs. Scale bar: 100 nm. (B): SEM image of an array of 20 nm wide niobium NWs. Scale bar: 200 nm. (C): Four-point resistance measured on different vanadium NW arrays similar to those shown in (A). (D): Four-point resistance measured on different niobium NW arrays similar to those shown in (B).

We initially attempted to replace Pt with the superconducting materials vanadium (V) and niobium (Nb). Highly ordered NWs were obtained (Fig. 2-2A,B), but none of those NWs were superconducting. All arrays have increased resistance at low temperature (Fig. 2-2C,D). In fact, e-beam evaporated thin *films* of V and Nb were also found non-superconducting, presumably due to inflated lattice parameters.[31]

Thus we prepared the superconducting NW arrays in a fashion analogous to how Si NW arrays are fabricated[29,32,33] – i.e., SNAP is utilized to prepare a Pt NW array mask on top of a superconducting thin film, and directional dry etching is utilized to translate the Pt NW pattern into the film to produce superconducting NWs. Superconducting materials are in general not as stable as Si, so the protocol used for Si was modified accordingly. In particular, the superconducting film was protected with a thin SiO_2 layer deposited prior to the SNAP procedure. This layer also ensured the superconducting NWs were well-insulated from the Pt NW mask. The resultant on-chip NWs can be readily integrated with microcircuits on the same substrate (e.g., 4-point contacts made out of either the same superconducting film or a different material), in comparison with other methods where NWs are obtained as suspended[6,13-15,21,34-36] or embedded[23,25,26] structures, or on the very thin edges of substrates.[9,27] We chose Nb as a first demonstration here, but as shall be discussed in Chapter 3, this method is generally applicable, including to high T_c materials, as long as a thin film of the material is available. The detailed fabrication processes are described below.

Si substrates with a 300 nm thick SiO_2 or Si_3N_4 top layer were cleaned in a piranha solution (H_2SO_4/H_2O_2) and rinsed thoroughly with deionized water. SiO_2, Si_3N_4 and Si substrates were all compatible with the fabrication procedure, and consistent

results were observed on SiO_2 and Si_3N_4 substrates (Si substrates are not tested due to the large current through the Si channel). Fully functional thin Pt/Ti (5 nm/2 nm) contact electrodes with thick Au/Ti (50 nm/10 nm) wire-bonding pads were fabricated on some of the substrates by electron-beam lithography (EBL).

Superconducting Nb films were prepared in a Denton Vacuum Discovery 550 multi-cathode DC/RF magnetron sputter deposition system. Substrates were loaded onto a rotating stage and the chamber was pumped down overnight to achieve a base pressure of 10^{-7} Torr (1 Torr ~ 133 Pa). Ultrahigh-purity argon (99.999%+) was introduced into the system as the sputtering gas at 15 sccm (standard cubic centimeters per minute) and kept at 2.5 mTorr. Nb films were deposited at ~0.8 nm/s by DC sputtering from a 3-inch Nb target (99.96%, Plasmaterials, Livermore, CA), after an extensive (>30 minutes) pre-sputtering with a shield between the substrates and the target to clean the surface of the target thoroughly and getter-absorb the residual background gases in the chamber. Without breaking the vacuum, 4 nm SiO_2 was immediately RF sputtered from a 3-inch silicon dioxide target (99.995%, Kurt J. Lesker, Livermore, CA) to cover the films.

An array of Pt SNAP NWs was obtained by e-beam evaporation onto the raised edges of a differentially etched edge of a $GaAs/Al_xGa_{(1-x)}As$ superlattice wafer (IQE, Cardiff, UK).[28] In this way, the atomic control over the film thicknesses of the superlattice stack was translated into control over the width and spacing of NWs (Fig. 2-3A). The array of Pt SNAP NWs was then stamped (as an ink) onto a SiO_2-coated superconductor (Nb) thin film and securely bonded to the surface (Fig. 2-3B) with a thin layer of epoxy (EpoxyBond 110, Allied High Tech, Rancho Dominguez, CA). The

superlattice was then released by a selective wet etch, leaving the highly-ordered array of Pt nanowires on the surface (Fig. 2-3C).

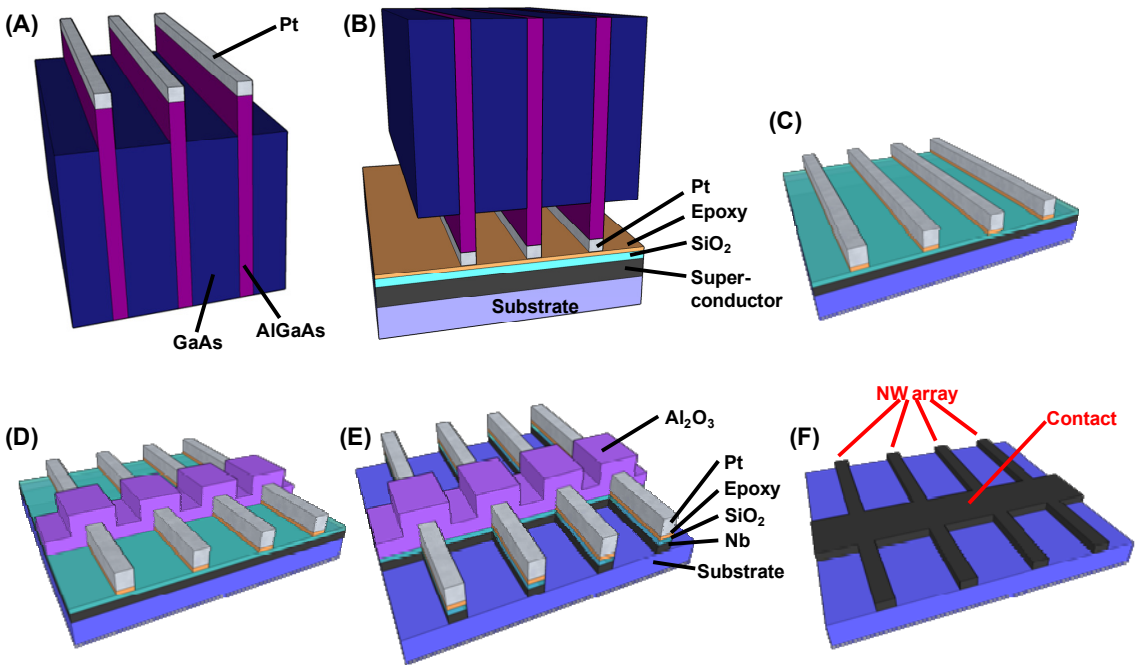

Figure 2-3. Process flow for the fabrication of superconducting nanowire (NW) array devices. (A): An array of Pt SNAP NWs is obtained on the raised edges of a differentially etched edge of a GaAs/$Al_xGa_{(1-x)}As$ superlattice wafer. (B): The array of Pt NWs is stamped onto a SiO_2-coated superconductor (Nb) thin film and bonded to the surface. (C): The superlattice is released by a selective wet etch, leaving the highly-ordered array of Pt NWs on the surface. (D): Al_2O_3 is deposited as a pattern for the contact electrodes. (E): A monolithic (all Nb) NW array circuit is obtained after the pattern is translated with a directional dry etch. (F): The resultant NW array circuit is drawn here. In practice, it is protected by the SiO_2 cover layer.

For substrates with pre-defined contact electrodes, Pt NW arrays were aligned perpendicular to and across the underlying electrodes with ~1 μm registration.[29] For

substrates without pre-defined contact electrodes, Pt NW arrays were put down at the center of the substrate, and EBL was used to pattern a 40 nm thick Al_2O_3 mask for the contact electrodes (Fig. 2-3D). The Pt NW array and Al_2O_3 electrode masks were translated into the underlying Nb film by highly directional reactive-ion etching (RIE) in a 40 MHz Unaxis SLR parallel-plate RIE system with CF_4/He (20/30 sccm, 5 mTorr, 40 W).

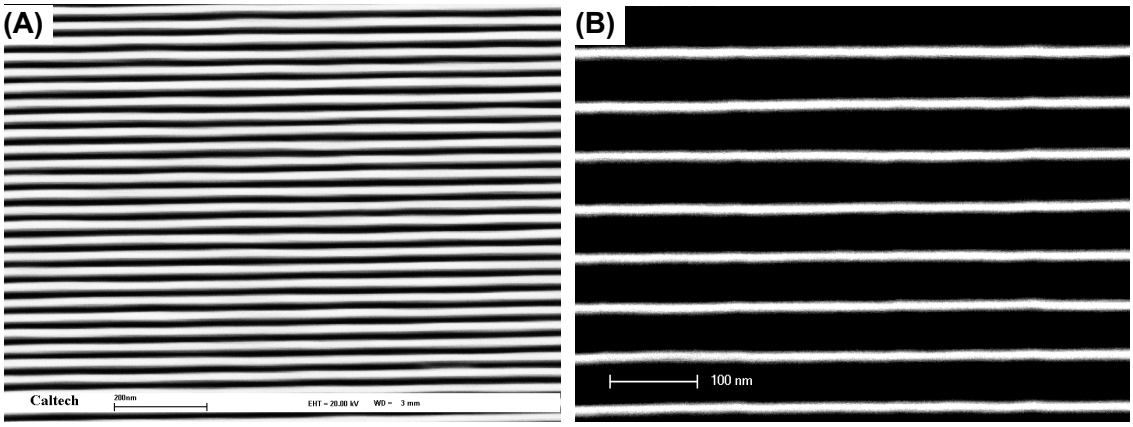

Figure 2-4. Scanning electron microscope (SEM) images of representative Nb nanowire arrays. (A) 16 nm wide nanowires with 33 nm pitch (periodicity). Scale bar: 200 nm. (B) 10 nm wide nanowires with 60 nm pitch. Scale bar: 100 nm. Both sets of Nb nanowires are 11 nm high.

Devices are ready for measurement after the pattern translation: for substrates with predefined electrodes, the Nb NWs are contacted by the underlying Pt electrodes, while for substrates without predefined electrodes, the Nb NWs are seamlessly connected to the contacts made out of the *same* superconducting film, forming monolithic Nb NW array circuits defined by the Pt NW and Al_2O_3 contact electrode masks (Fig. 2-3E and 1-3F). With this careful design, the obtained Nb NWs are well insulated from the Pt NW

masks above by the SiO_2 and epoxy layers (Fig. 2-3E), and the whole structure is covered and protected by the SiO_2 layer on the top and the very thin fluorocarbon polymer films coated on the sidewalls during the dry etching step.[37] Representative images of the fabricated Nb NW arrays are presented in Fig. 2-4.

2.3 Electrical properties of conventional superconductor nanowire arrays at low current levels

The electrical properties of the fabricated superconducting NW array devices aHre measured in a pumped ^{4}He system (Quantum Design MPMS-XL; base temperature ~1.7 K) with standard DC or AC lock-in techniques at low frequency. Low-current measurements were first performed, in which a sufficiently small current is used to probe the equilibrium properties without causing significant perturbations to the system.

Fig. 2-5 presents the measured electrical properties of Nb nanowire arrays at low current levels. A *total* current level of ~100 nA is typically used in the low-current measurements. Because there are typically ~100 parallel NWs in each array, the current level corresponds to ~1 nA per individual NW. This is well below the current limit beyond which the *V*-*I* relationship is expected to become nonlinear for a NW, $I_0 = 4ekT/h = 13\ \text{nA}\cdot(T/\text{K})$,[2] which is ~20 nA for the base temperature of our system. As a result, Ohmic (linear) *V*-*I* curves are observed at all temperatures (Fig. 2-5B). Low-current-limit resistance is then calculated from linear fits to such *V*-*I* curves, and plotted as a function of temperature (Fig. 2-5A).

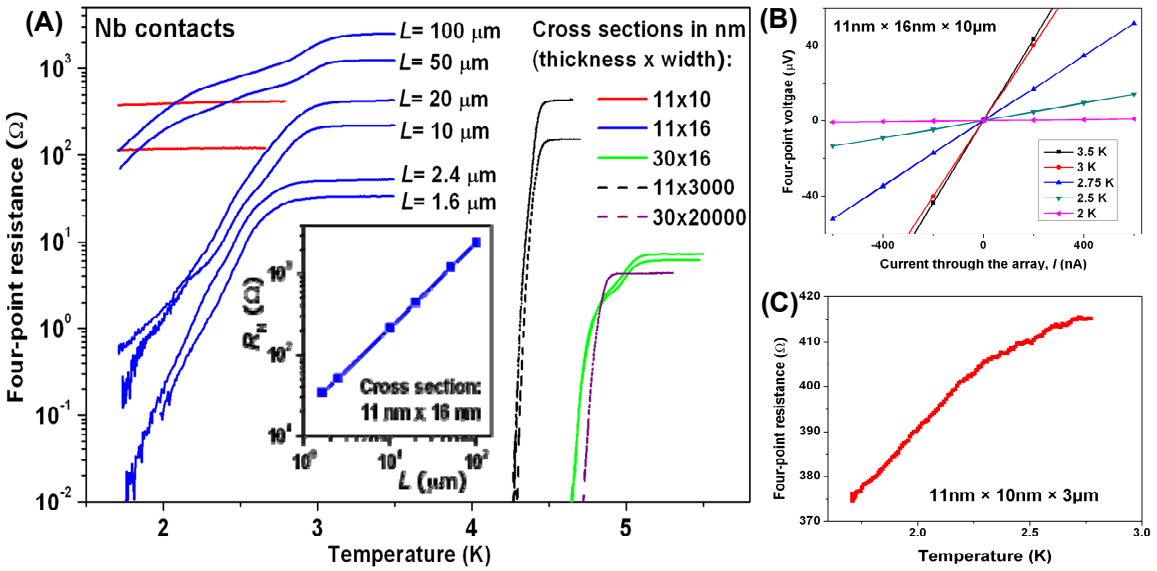

Figure 2-5. Measured electrical properties of Nb nanowire arrays at low current levels. (A): Temperature dependence for the four-point resistance of Nb NW arrays and films contacted with monolithic Nb contacts. Red lines: arrays of 12 NWs of cross section 11nm × 10nm and length *L* (From top to bottom) = 3 and 0.9 μm. Blue lines: arrays of 100 NWs of cross section 11nm × 16nm and *L* = 100, 50, 20, 10, 2.4, and 1.6 μm. Green lines: arrays of 250 NWs of cross section 30nm × 16nm and *L* = 1.5 and 1.3 μm. Black dashed lines: 11 nm thick films with width of 3 μm, *L* = 60 and 20 μm. Purple dashed line: a 30 nm thick film with width of 20 μm, *L* = 2.5 μm. Inset: Length dependence of the normal-state resistance for arrays of 100 NWs of cross section 11nm × 16nm. (B): Representative four-point *V-I* curves in the low-current limit for an array of 100 Nb NWs of cross section 11nm × 16nm and *L* = 10 μm. (C): A close-up of the temperature dependence for the four-point resistance of an array of 12 NWs of cross section 11nm × 10nm and *L* = 3 μm.

Superconductivity is observed on all NW arrays (Fig. 2-5A). Here we've followed the criterion for superconductivity used in previous NW studies, i.e., whether the

resistance decreases significantly (near exponentially) when the temperature is reduced below a device-dependent T_c.[6,13,36] Although not clear from Fig. 2-5A, the thinnest NWs do show the onset of superconductivity at ~2.5 K, and the resistance continues to drop when the temperature is lowered (Fig. 2-5C). 10% of total resistance vanishes at the base temperature (1.7 K).

Remarkably, superconductive behavior is observed in long (100 μm) NWs with normal state resistance R_N = 245 kΩ for each individual NW. As discussed previously in Introduction, basing on results in short NWs, some researchers have speculated that superconductivity may not be retained in a NW if $R_N > R_q$ ~6.5 kΩ, the quantum resistance for Cooper pairs.[13,21] This suggests the observed superconductivity could be proximity-induced by superconducting contacts[18,19,38,39] and is difficult to retain in long (high R_N) NWs. In agreement with recent experiments,[6,9] our results indicate $R_N > R_q$ should not be the criterion for the superconductor-insulator transition in NWs: superconductivity is intrinsic to NWs and can be maintained in long (and hence high R_N) NWs.

To further demonstrate that the observed superconductivity is intrinsic to the NWs (as opposed to proximity-induced superconductivity from superconducting contacts), we also examined NW arrays contacted with normal-state leads (Fig. 2-6). Such device structures are difficult to achieve using other NW fabrication methods. A clear resistance drop is observed with T_c ~ 3.5 K, but the superconductivity is partially suppressed by the normal-state contacts, as evidenced by a drop in T_c (T_c ~3.5 K as compared with T_c ~5 K for Nb-contacted NWs of similar dimensions) and a substantial residual resistance at low temperature. For the two sets of data, the shorter NW array has a slightly lower T_c due to

stronger suppression from the contacts. Although the longer array has a considerably larger normal state resistance (proportional to the length), an identical residual resistance of 18 Ω is obtained for both arrays at low temperature. This is indicative of a resistive superconducting-normal mixed state localized at the contact interfaces.[40] The Pt-contacted NW arrays provide unambiguous evidence of the intrinsic origin of superconductivity in NWs, but the strong suppression of superconductivity by the contacts is undesirable. Consequently, we shall focus on Nb-contacted arrays in the discussions below.

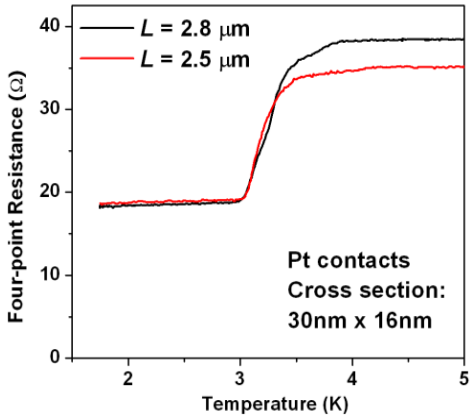

Figure 2-6. Measured temperature dependence for the four-point resistance of two Nb NW arrays contacted using normal-state Pt. The NWs in both arrays have the same cross section (30nm × 16nm), but different lengths (*L*) as labeled in the graph.

Note from Fig. 2-5 the consistency, for both T_c and the log(R)-T slopes, between data collected from different arrays with the same NW cross sections. The qualitatively different behavior found in the two longest arrays will be discussed later. Data from NWs of different cross sections are clearly different. Lower T_c is found for thinner NWs, with the cross-section dependence of T_c in general agreement with data on CNT-templated

NWs.[14] According to equations (1) and (2), the log(R)-T slope (~ΔF) is proportional to A but independent of L. Consequently, the similar slopes in the four 11nm × 16nm arrays of varying lengths testify to the uniform cross section of the NWs. Moreover, the slope for these NW arrays is ~3-fold smaller than for the 30nm × 16nm arrays.

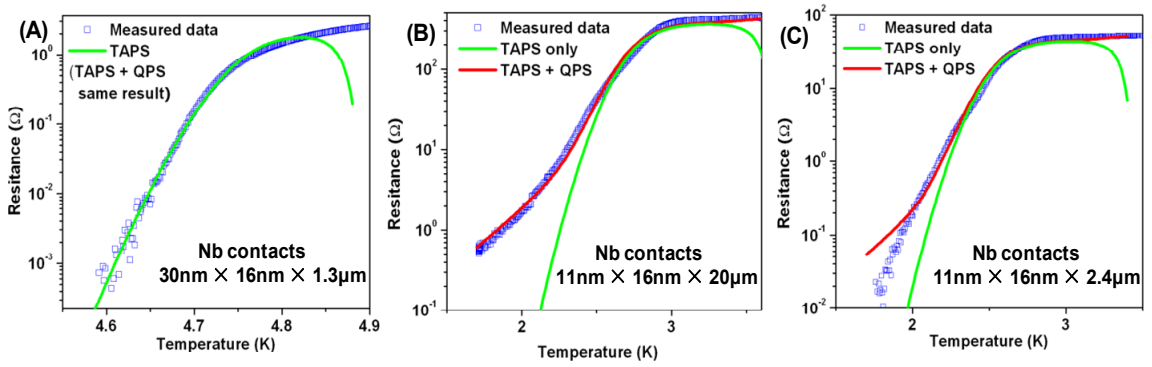

Figure 2-7. Fitting of the measured *R*(*T*) data to phase-slip theories. (A): The $R(T)$ data collected on an array of NWs of cross section 30nm × 16nm × 1.3μm, fitted to TAPS theory. TAPS + QPS gives an indistinguishable result. (B): The 11nm × 16nm × 20μm data fitted to the theories. (C): The 11nm × 16nm × 2.4μm data fitted to the theories.

Three representative sets of the measured $R(T)$ data shown in Fig. 2-5A are fitted to theories (Fig. 2-7). According to equation (2), $\log(R_{TAPS}) \sim -\Delta F/kT$. Because $H_c \sim(T_c-T)$ and $\xi \sim (T_c-T)^{-1/2}$, equation (1) gives $\Delta F\sim(T_c-T)^{3/2}$. This means a higher ΔF and therefore a faster drop in $\log(R_{TAPS})$ at lower T. This behavior is observed in the thicker NWs (Fig. 2-7A), and the data fit well to TAPS theory.[6]

Thinner NW arrays deviate from TAPS fits by having resistance higher than predicted in the low-T limit (Fig. 2-7B,C). Such behavior has been previously ascribed to

QPS processes[6-9,23] – i.e., the acquisition of phase slips by tunneling through ΔF. We use the formulation adapted by Tinkham to account for QPS:[6,7]

$$R_{\mathrm{QPS}} = B\frac{\pi\hbar^2\Omega_{\mathrm{QPS}}}{2e^2(\hbar/\tau_{\mathrm{GL}})}e^{-a\Delta F\tau_{\mathrm{GL}}/\hbar} \qquad (3)$$

where $\Omega_{\mathrm{QPS}} = (L/\xi)[\Delta F/(\hbar/\tau_{\mathrm{GL}})]^{1/2}(1/\tau_{GL})$, and B and a are fitting parameters of order unity. Because $R_{\mathrm{QPS}} << R_{\mathrm{TAPS}}$ when T is close to T_c, the contribution from QPS is unimportant in thicker NWs (Fig. 2-7A).

In contrast, thinner NWs have wider transitions with respect to temperature, and $R_{\mathrm{QPS}} << R_{\mathrm{TAPS}}$ may no longer hold at low temperature. Because $\Delta F \sim (T_c - T)^{3/2}$ and $\tau_{GL} \sim (T_c - T)^{-1}$, $\log(R_{\mathrm{QPS}}) \sim -a\Delta F\tau_{\mathrm{GL}}/\hbar \sim (T_c - T)^{1/2}$ has a weaker-than-linear dependence on T, and drops more slowly at low T relative to $\log(R_{\mathrm{TAPS}})$. Therefore, R_{QPS} is expected to dominate the total phase-slip resistance in the low-temperature limit. Such behavior is observed in the 11nm × 16nm × 20μm sample (Fig. 2-7B). For similar but shorter NWs, an improved fit is obtained by taking into account both TAPS and QPS. However, a nearly constant $\log(R)$-T slope is observed in the low-temperature limit (Fig. 2-7C), deviating from QPS prediction. Such behavior has been reported in short NWs,[6,8,13,14,36] while long NWs typically show the expected QPS behavior,[7,9,23] in agreement with our results. Because precise control of length and cross section has been difficult in previous studies, these observations have been inconclusive. We believe our data indicate that QPS can be partially suppressed in short NWs in the low-temperature limit due to contact effects, e.g., a local enhancement of ψ, as will be discussed further later.

The two longest NW arrays show a wide shoulder feature around 2.5 K (Fig. 2-5A) that cannot be explained with TAPS and QPS theories. A similar feature was recently reported in an Al NW 100 μm in length, and was accounted for by assuming the NW to be composed of segments of two different cross section areas with different T_c.[9] This argument, however, cannot explain why the shoulder is not observed in an Al NW 10 μm in length[27] or in any of the $L \leq 20$ μm NW arrays with the *same* cross section in our experiment. Also, it is hard to imagine why our 50 and 100 μm long arrays of 100 Nb NWs would both contain segments of exactly *two* different cross sections such as was proposed for the single Al NW. This "abnormal" behavior of long NW arrays in comparison with the consistent results found on the other four shorter arrays implies the shoulder feature should have a sole mechanism that depends only upon the length of the NWs. This mechanism will be discussed in detail later.

2.4 Electrical properties of conventional superconductor nanowire arrays at high current levels

While low-current limit measurements reflect the equilibrium properties of the NWs, the high-current limit represents different physics, since the current itself causes the breakdown of superconductivity, and so can address how large a supercurrent can be sustained in a NW (array). In addition, true quasi-1D superconductors provide for an ideal system to study the current-induced nonequilibrium phenomena.[3] However, a systematic study on this topic with varied dimensions of NWs has been lacking. In this regime, we observe three qualitatively different behaviors when the dimensions of the NWs are varied by design (Fig. 2-8).

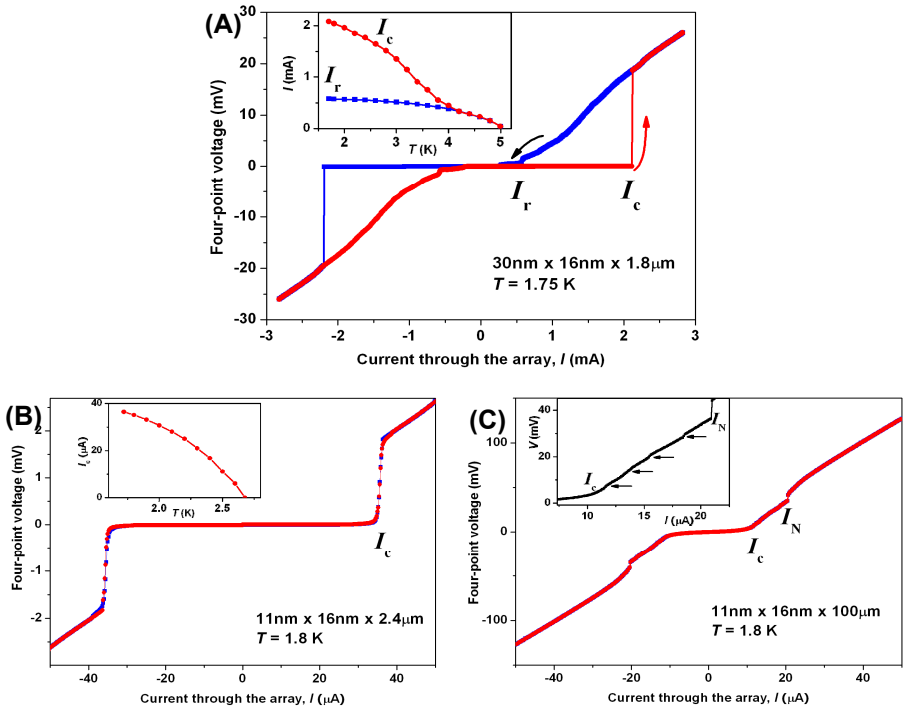

Figure 2-8. Four-point *V-I* curves for three representative arrays of Nb NWs, measured with increasing (red) and decreasing (blue) current bias at the base temperature. (A): An array of 250 NWs of cross section 30nm × 16nm and L = 1.8 μm. I_c denotes the critical current, i.e., the highest supercurrent that can be sustained when the applied current is swept up from zero, while I_r denotes the retrapping current, i.e., the current level at which the array returns to the superconducting state when the current is swept back down. Inset: Temperature dependence of I_c and I_r. (B): An array of 100 NWs of cross section 11nm × 16nm and L = 2.4 μm. Inset: Temperature dependence of I_c. (C): An array of 100 NWs of cross section 11nm × 16nm and L = 100 μm. Inset: An expanded plot of the intermediate state region ($I_c < I < I_N$); arrows point to voltage jumps.

Strong hysteresis is found in the *V-I* responses of thicker NWs at base temperature (Fig. 2-8A): the transition between the superconducting and normal states happens at different current levels for decreasing and increasing current. Such hysteresis is

characteristic of single NWs,[9,14,34,41] but has not been observed in NW arrays before,[23,25,26] presumably due to the large (~10 nm[23]) NW-to-NW diameter variation. The observed clear hysteresis, as well as the fact that the I_c per NW (2.1mA/250 = 8.4 μA) is comparable to a CNT-templated short Nb NW of similar width[14] suggests the uniformity and high quality of our NWs, so the collective behavior of the array retains the traits of individual NWs. Because we have more than 100 NWs per array, the resultant total I_c = 2.1 mA is more than 10^2 higher than those previously reported in individual NWs or small NW arrays. This large I_c in our on-chip arrays could find applications in carrying high levels of low-dissipation current, while the strong hysteresis effect could be potentially tailored into an information storage or switching mechanism with a high on-off ratio and low power dissipation. Both I_c and I_r drop when temperature is raised, but I_r drops slower so the hysteresis weakens and eventually disappears at high temperature (Fig. 2-8A inset), in agreement with results on individual NWs.[34] The hysteresis is not found in the thinner NWs at low temperature (Fig. 2-8B and 1-8C) due to the larger residual resistance, again agreeing with results on single NWs.[41] I_c is significantly reduced compared to the thicker NWs, consistent with previous experiments.[35]

Qualitatively different behaviors are also found for NWs with the same cross section but different lengths. In comparison with a single jump between the superconducting and normal states at I_c for shorter NWs (Fig. 2-8B), longer NWs first enter an intermediate state at I_c, and jump to the normal state at a higher current level, I_N ~$2I_c$ (Fig. 2-8C). This intermediate region exhibits multiple voltage jumps (Fig. 2-8C inset). Such behavior is characteristic of long quasi-1D superconductors, and each

voltage jump is associated with the emergence of a localized resistive "phase-slip center" (PSC) along the wire.[2,3,11]

In contrast to the stochastic TAPS and QPS events, PSCs are stable and have fixed locations within the NW for a constant driving current. The core of each PSC (~2ξ in length) quickly oscillates between the superconducting and normal states, and this leads to a finite resistance. Each PSC has a characteristic interaction length of ~2Λ, where Λ ~10 μm is the quasiparticle diffusion length. The number of PSCs a wire can accommodate should thus be ~L/2Λ. Theory[2,42] predicts that a single PSC emerges at the center of the NW at I_c (Fig. 2-9), resulting in the first voltage jump step in the V-I curve. Additional PSCs appear as the applied current increases, leading to additional voltage jump steps. When a new PSC emerges, all PSCs reorganize to distribute evenly along the nanowire, until the number of PSCs exceeds ~L/2Λ (Fig. 2-9).[2,42]

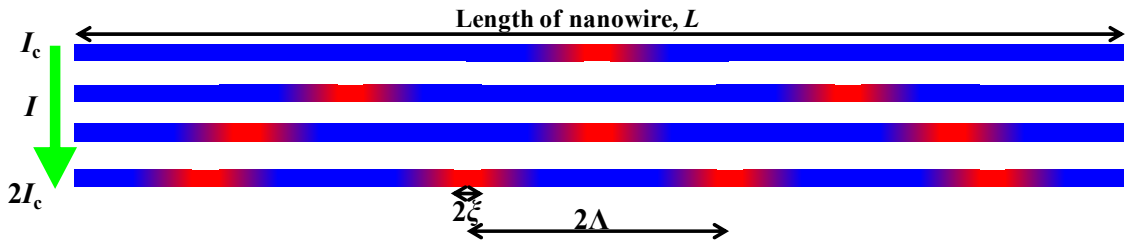

Figure 2-9. The expected distribution of phase-slip centers (PSCs; shown as red) along a quasi-1D superconductor nanowire of length *L*, as the applied current (*I*) is varied from I_c to $2I_c$. New PSCs emerge as *I* increases, and all PSCs rearrange to distribute evenly along the length of the nanowire.

The evolution of PSCs have been extensively studied in microbridges and submicron "whiskers"[3] very close to T_c and mesoscopic (~100 nm) nanoribbons,[43] but

results on NWs, which are truly quasi-1D superconductors at any temperature, have been limited. For example, in electrodeposited Sn NW arrays, PSCs are pinned down at local defects, and the number of PSCs observed is independent of the length of the arrays.[23]

We have charted the evolution of PSCs in our (11nm × 16nm) NW arrays with L= 2-100 μm, by plotting dV/dI, so that each PSC-related voltage jump in the V-I curve appears as a peak.[43] These features evolve reproducibly as a function of temperature and applied magnetic field (Fig. 2-10). In the low-temperature limit, 4 and 2 peaks are found for L=100 μm and L=50 μm NWs, respectively, between I_c (~12 μA) and I_N (~24 μA). NWs with $L \leq$ 20 μm exhibit no peak lines. The faint features found on the two shortest arrays are attributed to contact-induced PSCs.[44] Theory predicts[2,42] that for an *absolutely uniform* filament of length L, approximately $L/2\Lambda$ steps should occur between I_c and $2I_c$. The length of each PSC in our NWs can thus be estimated to be $2\Lambda \sim 25$ μm, comparable to the 10-50 μm values found in various materials.[11,26,45] Three small branching features are observed close to I_c for the 20 μm NWs (Fig. 2-10D), while the 10 μm NWs have one such feature (Fig. 2-10E), suggesting PSCs can still appear in NWs slightly shorter than 2Λ when the energy provided by temperature and current is sufficiently high. Such branching is not seen in the 2.4 μm (Fig. 2-10F) and 1.6 μm (not shown) arrays where $L << 2\Lambda$. The clear and consistent length dependence of PSCs' behavior revealed in the above discussions supports our conclusions that the NWs are uniform and effectively defect-free (defects would act as pinning centers for PSCs). The collective behavior of 100 NWs agrees with that expected for a single homogeneous quasi-1D superconductor.[42]

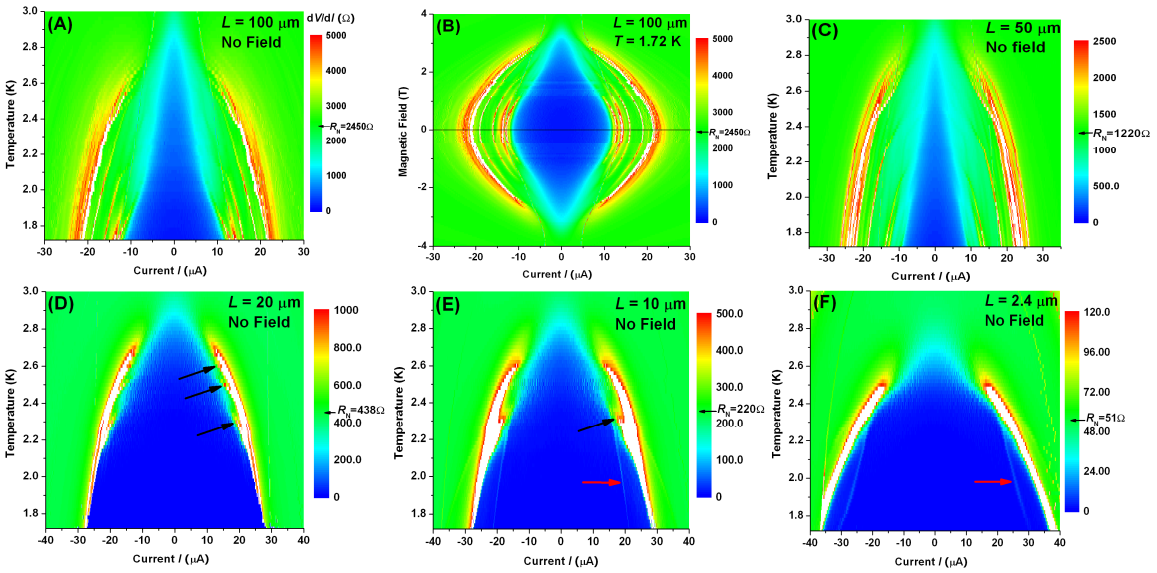

Figure 2-10. Differential resistance d*V*/d*I* of arrays of 100 NWs of cross section 11 nm × 16 nm, as a function of current, temperature and applied magnetic field. (A) and (C)-(F): temperature is varied at zero field. (B): Applied magnetic field is varied at constant temperature T = 1.72 K. The lengths of the arrays are labeled on each plot. Black arrows point to the small branching features observed close to I_c at higher temperatures for arrays of intermediate lengths, and red arrows point to the very faint (light blue) peak lines found only on the two shortest arrays.

The characteristic lengths revealed above should also be relevant to the equilibrium properties of the NWs. In particular, consider the shoulder feature observed ~2.5 K in the low-current *R*-*T* curves of the 50 μm and 100 μm arrays (Fig. 2-5A). This feature deviates from TAPS and QPS models, but coincides with the onset of stable PSC peak lines (Fig. 2-10A,C). Such features are not observed in shorter NWs that exhibit no PSC peak lines in the high-current limit. NWs longer than ~2Λ could allow for multiple phase-slip events in each NW for the same instant, which is not considered in the TAPS and QPS models.[6,8,46] A resistance higher than predicted (i.e., the shoulder feature)

would thus be observed. Shoulder features were observed in early experiments on long tin whiskers[2,10] near T_c, but were attributed to contact effects,[2] which is clearly not the case for our results. As discussed earlier, the faint features found on the *shortest* arrays (Fig. 2-10E,F) may arise from contact effects, but the corresponding local enhancement of ψ is found to suppress QPS and result in *smaller* residual resistances in comparison with theory (cf. Fig. 2-7C and related discussions).

2.5 Conclusion

In this chapter, we have reported[1] on the fabrication and properties of superconducting nanowire arrays with good control over both cross section and length. The nanowires are compatible with device processing, allowing for the establishment of 4-point electrical contacts. We investigated Nb nanowires with individual nanowire cross sectional areas that range from bulk-like to 10 × 11 nm, and with lengths from 1 to 100 micrometers. Electrical measurements in the low-current and high-current limits indicate the nanowires obtained are uniform and effectively defect-free. Size effects on superconductivity are systematically studied; in particular, the ability to fabricate very long nanowires with identical cross sections allows for the first systematic investigation of length's sole influence on superconductivity in nanowires, from which characteristic quasiparticle diffusion lengths are extracted. All results are interpreted within the context of phase-slip models.

The fabrication method demonstrated with Nb nanowires in this chapter is broadly applicable to various thin film superconductors. In the next chapter, we will

discuss how similar fabrication methods were further harnessed to produce high-quality high-temperature superconductor nanowires.

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Chapter 3

Long, Highly-Ordered High-Temperature Superconductor Nanowire Arrays

The contents presented in this chapter are based on K. Xu and J. R. Heath, "Long, highly-ordered high-temperature superconductor nanowire arrays," *Nano Letters,* 8, 3845-3849 (2008). (Ref. [1])

3.1 Introduction

As discussed in Chapter 2, a superconducting wire becomes quasi-one-dimensional (quasi-1D) when its width w is reduced to be comparable to or smaller than the Ginzburg-Landau (GL) coherence length ξ and magnetic penetration depth λ.[2,3] For $w < \sim\xi$, the GL order parameter ψ (and the density of Cooper pairs, $|\psi|^2$) is constant over the cross section and is only a function of the position x along the wire. For $w < \sim\lambda$, a current passed through the wire should spread uniformly over the cross section. The electrical resistance R of a quasi-1D superconductor decreases to zero gradually below the superconducting transition temperature T_c due to phase-slip processes (Chapter 2).[2,4] Phase-slip processes may also result in resistive or insulating behaviors for thin (~10 nm) wires when temperature approaches zero.[4,5]

Both conditions for quasi-1D superconductivity are met for elemental superconductors when $w < \sim\lambda$, because they are typically type I, satisfying $\xi > \sqrt{2}\lambda$

(except for Nb, which has $\xi \approx \lambda$). Phase-slip theories were first validated in micron-size filaments within several millikelvins below T_c because both $\xi(T) \approx \xi(0)(1-T/T_c)^{-1/2}$ and $\lambda(T) \approx \lambda(0)[1-(T/T_c)^4]^{-1/2}$ are large close to T_c.[2,3] Recent nanotechnology advances have allowed for the fabrication of elemental superconductor nanowires (NWs) with w down to ~10 nm < $\lambda(0)$ (~40 nm[6]).[7-13] These NWs are strictly quasi-1D for any $T<T_c$, and phase-slip theories have been verified in these systems.

Alloy and compound superconductors are typically type II superconductors, satisfying $\xi < \sqrt{2}\lambda$. Many of these materials are in the extreme type II limit, with ξ ~1 nm and λ ~100 nm. The current fabrication limit for superconductor NWs is w ~10 nm, satisfying $\xi << w << \lambda$ for these materials. In this region, because $w < \lambda$, transport currents are still expected to be homogeneous over the NW cross section, but because $w > \xi$, ψ may vary over the NW cross section. Recent experiments suggest that, in this regime, phase-slip theories may still be applicable. For example, phase-slip theories give excellent fits for MoGe NWs when $w \sim 4\xi << \lambda$[4,5,14] and NbN strips when $w \sim 25\xi < \lambda$.[15] Recent studies on $NbSe_2$ NWs have also suggested the appearance of phase-slip centers and other quasi-1D characteristics when $10\xi < w < \lambda$.[16,17]

With ξ~2 nm and λ~150 nm, cuprate-based high-temperature superconductors (HTS) are all in the extreme type II limit.[18] Also, the underlying mechanism of high-temperature superconductivity is fundamentally different from the BCS Cooper pair mechanism for conventional superconductors, and is one of the major unsolved problems of theoretical condensed matter physics as of 2009.[19-21] It is therefore of fundamental interest to understand (1) whether high-temperature superconductivity can be retained in

NWs at all, and, (2) if it is retained, whether phase-slip theories, which have been widely applied to conventional superconductor NWs, still apply to HTS NWs.

In addition, strong suppression of superconductivity by phase-slip processes has been observed in previous studies on quasi-1D NWs made from elemental superconductors[10-13] and from the binary alloy MoGe.[4,5,22] The very low T_c (typically below liquid helium temperature) also limits their potential applications as zero-electrical resistance conductors or active components in nanoelectronic circuits.[22-26] The short ξ (~2 nm) that characterizes HTS materials may reduce the influence on superconductivity of phase slip processes in HTS NWs, and the expected significantly higher T_c should uniquely enable applications of HTS NW materials.

However, achieving high-temperature superconductivity in NWs requires achieving the correct stoichiometry *and* the correct perovskite-like crystal structures of the HTS materials. This renders many superconductor NW fabrication methods[5,10,12,16,27] inapplicable, and so little has been reported in this area.

Short HTS NWs (w ~50 nm) have been synthesized, but superconductivity was only tested through magnetization measurements of powders of these materials.[28,29]

Patterning HTS NWs from epitaxially grown HTS thin films is also challenging: HTS materials are unstable towards processing steps involving acid, water, or moderately elevated temperatures. In addition, for patterning, HTS films are resistive to directional dry etching, and no selective chemical dry etch for HTS materials has been reported. For physical dry etching, HTS films exhibit slower etching rates than typical etch-mask materials. As a result, HTS thin films have only been patterned into short submicron

bridges, and property measurements of those bridges have yielded inconsistent results.[30-34] Bonetti *et al.* reported substantial broadening of the transition temperature width and telegraph-like resistance fluctuations in a w = 250 nm $YBa_2Cu_3O_{7-\delta}$ (YBCO) bridge,[33] but their findings were not confirmed by others in similar or narrower bridges.[30-32,34] Mikheenko *et al.* studied YBCO bridges of several different widths, and observed broadening of transition temperature width in a w = 500 nm bridge.[34] The broadening was modeled with phase-slip theories, but unrealistic fitting parameters were obtained because $w > \lambda >> \xi$, and also no clear trend was found as the width of the bridges was varied.

In summary, no clear size effects have been studied for HTS bridges (or wires) in the $w << \lambda \sim$100 nm region.

We have significantly modified the superlattice nanowire pattern transfer (SNAP) technique[35-37] to overcome the limitations of previous studies. We report[1] for the first time that arrays of HTS NWs can be produced down to w = 10 nm ($<< \lambda$) and up to 200 μm in length, achieving aspect ratios of $>10^4$. Through four-point electrical measurements, we find high-temperature superconductivity is retained in these NWs: all nanowires exhibit a superconducting transition above liquid nitrogen temperature, and a transition temperature width that depends strongly upon the nanowire dimensions. Nanowire size effects are systematically studied, and we demonstrate for the first time the applicability of phase-slip theories in explaining the size effects in high-temperature superconductor nanowires. These nanowires can function as superconducting nanoelectronic components over much wider temperature ranges as compared to conventional superconductor nanowires.

3.2 Fabrication of high-temperature superconductor nanowire arrays

As discussed in Chapter 2, we have previously developed the fabrication methods to prepare high-quality elemental (Nb) superconductor NWs, basing on pattern translation of Pt NWs through directional dry etching.[13] HTS materials are very unstable relative to Nb. Thus, a water-free process that avoided temperatures above 120^{o}C was developed to accommodate the fragility of HTS thin films. Because HTS materials can only be patterned by slow physical dry etching (~10 times slower than the mask Pt NWs), a slow-etching SiO_2 layer was sandwiched between the HTS thin film and the Pt NW array. Reactive-ion etching translated the Pt NW features into the SiO_2 layer, which then served as a mask for an Ar+O_2 physical dry etch of the HTS film. O_2 helped maintain the correct oxygen stoichiometry in the HTS material,[38] and ~10 second etch cycles were separated by 1 minute cool-down periods to prevent heat accumulation within the HTS film.

HTS materials react with many metals and form highly resistive contacts.[39] Thus, four-point probe contacts were made to the HTS NW array out of the *same* HTS film by patterning on top of the SiO_2 layer before pattern translation of the Pt NWs. Metal contacts for wirebonding were connected to the HTS layer far away from the NW array. The detailed fabrication processes are described below.

An array of Pt SNAP NWs was obtained by e-beam evaporation onto the raised edges of a differentially etched edge of a GaAs/$Al_xGa_{(1-x)}$As superlattice wafer (IQE, Cardiff, UK).[35] The array of Pt SNAP NWs was then stamped onto a HTS thin film that is pre-coated with a ~50 nm thick SiO_2 layer. For the YBCO HTS NWs discussed in this

chapter, a 30 nm *c*-axis oriented epitaxial YBCO HTS film (E-type, THEVA, Ismaning, Germany) was used. A thin (~10 nm) layer of chemically-modified heat-curable epoxy (EpoxyBond 110, Allied High Tech, Rancho Dominguez, CA. Modified with dibutyl phthalate.) was used to securely bond the Pt NW array to the surface. The superlattice/NW array/epoxy/SiO_2/HTS assembly was baked on a hot plate at 120 °C for 5 min, and the superlattice was then released by a selective wet etch. 5% I_2 in anhydrous methanol was used as the etchant, which was found to effectively dissolve the superlattice without degrading the HTS film. After the residual epoxy was etched away with an oxygen plasma, a highly-ordered array of Pt NWs was obtained on top of the SiO_2-covered HTS film (Fig. 3-1a).

Metal (Au/Ti) contact pads for wirebonding were lithographically defined far away from the NW array, and CF_4 reactive ion etching (RIE) was used to remove the SiO_2 layer before metal was deposited, so the metal contact pads were directly connected to the HTS layer (Fig. 3-1b). An additional Ti/Pt bilayer was deposited onto the Au-Ti metal pads to prevent complete removal of Au in the subsequent dry etching steps. E-beam lithography was then used to pattern a 40 nm thick Al_2O_3 mask on top of the SiO_2 layer to define the four-point probe contacts (Fig. 3-1c). The Pt NW array and Al_2O_3 electrode masks were first translated into the SiO_2 layer by highly directional RIE in a 40 MHz Unaxis SLR parallel-plate RIE system with CF_4/He (20/30 sccm, 5 mTorr, 40 W) (Fig. 3-1d).

The patterns in the SiO_2 layer (Fig. 3-1d) then served as a mask for an Ar+O_2 physical dry etching (18/2 sccm, 10 mTorr, 190 W) of the HTS film (Fig. 3-1e). O_2 was used with Ar in this etching step to help maintain the correct oxygen stoichiometry in the

HTS thin film,[38] and ~10 second etch cycles were separated by 1 minute cool-down periods to prevent heat accumulation within the HTS film. The top-lying platinum nanowires were also removed in this step.

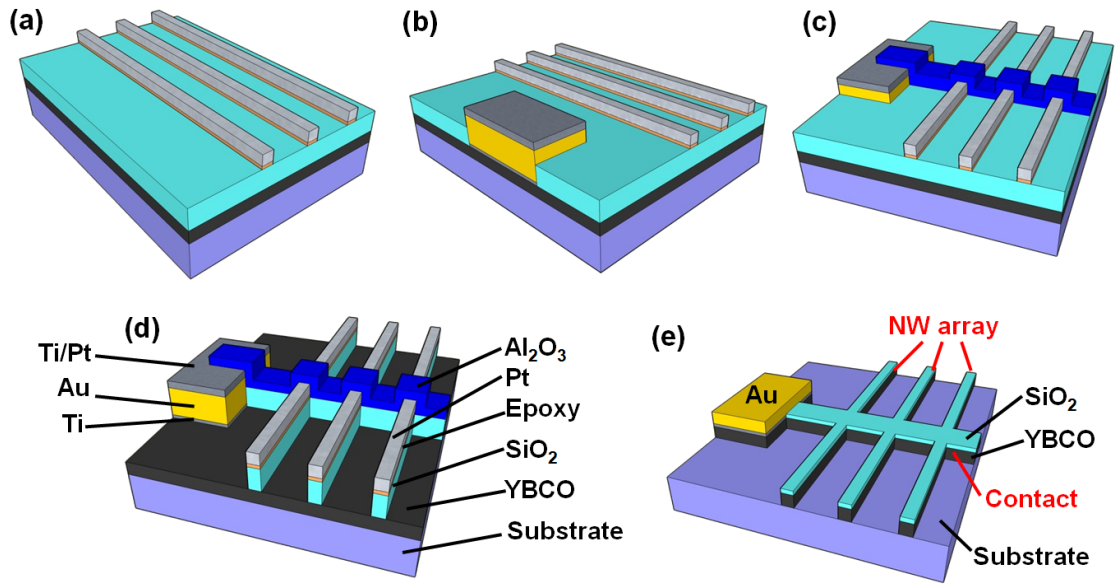

Figure 3-1. Process flow schematics for the fabrication of high-temperature superconductor nanowire array devices. (a): Pt SNAP nanowires are deposited onto a SiO_2-coated high-temperature superconductor (HTS) thin film. (b): Au-Ti metal pads are deposited and connected to the HTS layer far away from the nanowire array, after the underneath SiO_2 layer is removed using dry etching. An additional Ti/Pt bilayer is deposited onto the Au-Ti metal pads to prevent complete removal of Au in the subsequent dry etching steps. (c): Al_2O_3 is lithographically patterned to define the contact electrodes. (d): The nanowires and contact patterns are translated into the SiO_2 layer with selective reactive-ion etching. (e): The nanowires and contact patterns defined in the SiO_2 layer are translated into the HTS film with $Ar+O_2$ physical dry etching. This also removes the top-lying Pt nanowires. The final structure is a single crystal HTS nanowire array device protected by a thin SiO_2 film, with nanowires seamlessly connected to the contacts made from the *same* HTS film.

The final structure is a monolithic, single crystal HTS nanowire array device protected by a thin SiO_2 film, with nanowires seamlessly connected to the contacts made from the *same* HTS film (Fig. 3-1e).

HTS NW arrays of various dimensions were fabricated. Fig. 3-2 presents representative images of the YBCO NWs discussed in this chapter. Three 10 micrometer wide strips of YBCO films underwent the same fabrication and testing as the NWs, and independent electrical measurements of these strips produced overlying resistance-temperature (*R*-*T*) curves (Fig. 3-3a). The strips exhibit a T_c of 85 K, a sharp transition width of ~3 K, and a critical current density of 0.83 MA/cm^2 at 77 K. These values agree with those measured from the starting film. Thus the different behaviors observed in the NWs are attributed to size effects.

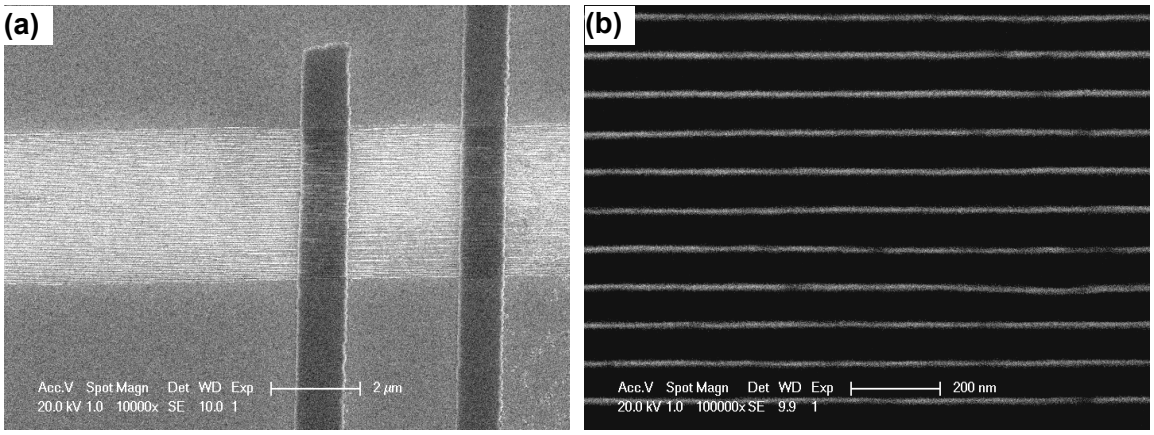

Figure 3-2. Scanning electron microscope images of representative $YBa_2Cu_3O_{7-\delta}$ nanowire arrays. (a): Scanning electron microscope image showing an $YBa_2Cu_3O_{7-\delta}$ nanowire array and two contacts. Scale bar: 2 μm. (b): High-magnification micrograph of an $YBa_2Cu_3O_{7-\delta}$ nanowire array (nanowires width = 10 nm). Scale bar: 200 nm.

3.3 Electrical properties of high-temperature superconductor nanowire arrays at low current levels

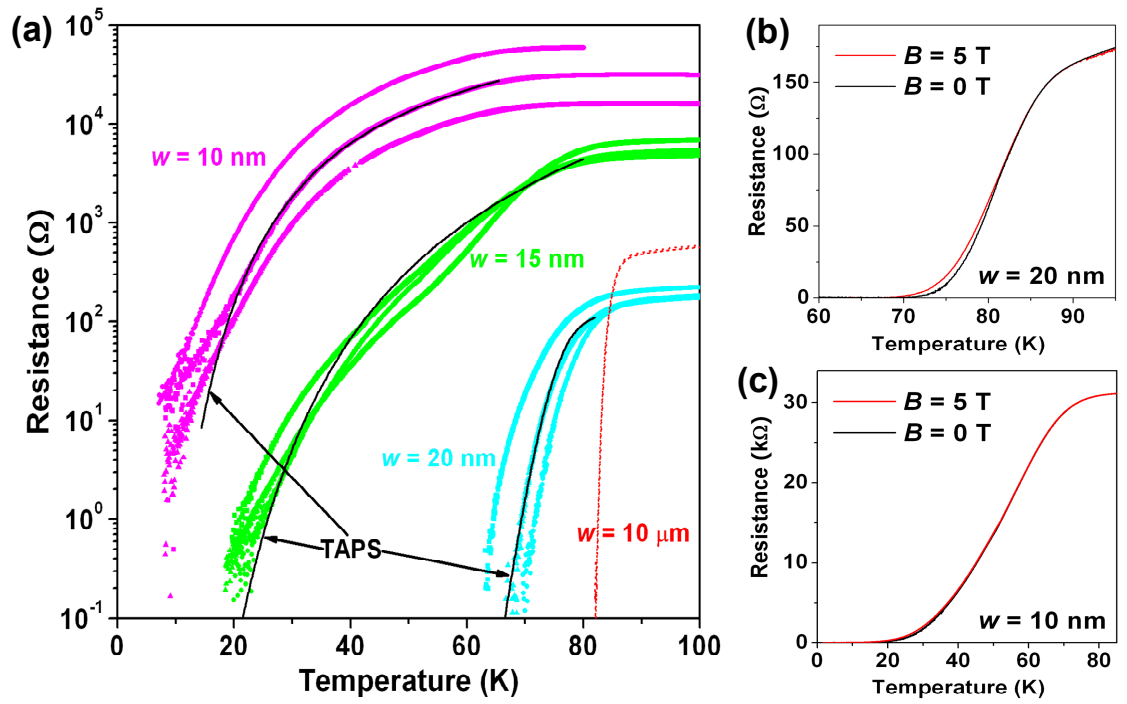

Figure 3-3. Temperature and magnetic field dependence for the four-point resistance of $YBa_2Cu_3O_{7-\delta}$ nanowire arrays in the low-current limit. (a): Temperature dependence of resistance for nanowire arrays and films with various dimensions at zero magnetic field. Pink: arrays of 100 nanowires, width w = 10 nm and length L (from top to bottom) = 200, 100, and 50 μm. Green: arrays of 150 nanowires, w = 15 nm and L = 35, 30, and 27 μm. Light blue: three arrays of 400 nanowires each, with w = 20 nm and L = 5 μm. Red dot lines: three geometrically identical strips fabricated through the same process, w = 10 μm and L = 50 μm. Black lines are fits of the nanowire data to thermally activated phase slip (TAPS) models. (b): The resistance-temperature relationship for a 400 nanowire array with w = 20 nm and L = 5 μm, with and without an applied 5 T magnetic field. (c): The resistance-temperature relationship for an array of 100 nanowires with width w = 10 nm and L = 100 μm, with and without an applied 5 T magnetic field.

R-T data, taken in the low-current limit (~1 nA per NW) (Fig. 3-3), reveals that high-temperature superconductivity is retained in all NWs, as characterized by a significant drop in resistance when temperature is reduced below T_c ~80 K. Consistent trends are found for NWs with the same widths, whereas thinner NWs exhibit broader transitions with respect to temperature. T_c for the NWs is close to that of the starting film. For the thicker (w = 20 nm) NWs, the resistance drops by an order of magnitude at liquid nitrogen temperature (77 K). It drops below the measurement limit at ~69 K (Fig. 3-3a,b), higher than the triple point of nitrogen (63 K). This implies that YBCO NWs thicker than ~20 nm could operate as fully superconducting nanoelectronic components in a pumped liquid nitrogen system. Thinner NWs have significantly broadened transition temperature widths, and the resistance drops to effectively zero at ~20 and ~10 K for w = 15 and 10 nm NWs, respectively. Even these temperatures are considerably higher than those found in conventional superconductor NWs of similar widths, which are typically below liquid helium temperature (4.2 K). The very broad (>50 K, comparing to a few Kelvins for conventional superconductor NWs) transition temperature widths observed in these NWs could found applications in NW-based nano-SQUIDs,[22] in which the quantum-interference-induced resistance oscillations of a pair of superconductive, yet resistive, NWs are monitored for local magnetic field measurements.

The broadened transition temperature widths in the HTS NWs can be captured by the same phase-slip theories[2,4] that have been applied to elemental superconductor NWs. As discussed in the Introduction, although phase-slip theories were originally derived for NWs with w comparable to or smaller than both ξ and λ, recent studies on binary compound superconductor NWs and submicron bridges have suggested that they may

still be applicable in our case in which $\xi < w < \lambda$.[4,15] For thermally activated phase slip (TAPS) processes, thermodynamic fluctuations (~kT) instantaneously suppress superconductivity at a random point along the NW, resulting in a measurable resistance. The energy required to locally suppress superconductivity is (note: the exact form here is different from eqn. 1 in Chapter 2, because now SI units is used, which is more convenient for the discussions here):

$$\Delta F(T) = \frac{8\sqrt{2}}{3}\frac{B_c^2(T)}{2\mu_0}A\xi(T) \qquad (1)$$

B_c is the thermodynamic critical field and A is the cross-section area of the NW. The resultant resistance then follows an Arrhenius-like equation with respect to temperature, $R_{TAPS} \sim \exp(-\Delta F/kT)$. Thinner NWs have smaller A and therefore smaller energy barriers to overcome to acquire resistance. As a result, the resistance of thinner NWs drops more gradually below T_c, and those NWs have wider transition temperature widths.

As shown in Fig. 3-3a, the R-T relationship observed in our experiment can be satisfactorily modeled with TAPS theory using reasonable fitting parameters. The difficulty in directly applying Eq. (1) to obtain ΔF for data fitting lies in the fact that both B_c and ξ depend on T and may be different from the bulk. In previous studies on conventional superconductor NWs, Tinkham *et al.* derived a formula to estimate the zero-temperature limit $\Delta F(0)$ using Ginzburg-Landau relations, and $\Delta F(T)$ was then estimated using Eq. (1) and the relationships that $B_c \sim (T_c - T)$ and $\xi \sim (T_c - T)^{-1/2}$ when $T \sim T_c$, thus:[4,40]

$$\Delta F(0) \approx 0.83\frac{L}{\xi(0)}\frac{R_q}{R_N}kT_c \quad (2a) \qquad \Delta F(T) \approx \Delta F(0)(1 - T/T_c)^{3/2} \quad (2b)$$

In this way, ΔF is estimated from the known normal state resistance R_N and the NW length L, whereas the cross section A becomes *implicit* in data fitting. $\xi(0)$ and T_c are fitting parameters. This approach applies only to the "dirty limit", i.e., the mean free path ℓ << BCS coherence length ξ_0, so $\lambda \approx \lambda_L\left(1+\xi_0/\ell\right)^{1/2} \approx \lambda_L\left(\xi_0/\ell\right)^{1/2}$ (and thus B_c) is correlated with ℓ and therefore R_N.

With ℓ ~10 nm and ξ_0 ~1 nm, HTS materials are in the opposite, "clean limit",[18] so $\lambda \approx \lambda_L$ is not correlated with R_N, and Eq. (2a) is no longer applicable. For the w = 20 nm NWs, the transition temperature width is small ($T \sim T_c$), and so we've assumed a T-dependence of ΔF as in Eq. (2b). We then used A *explicitly* from the NW geometry, $\xi(0)$ ~2 nm for YBCO from literature,[6] and $B_c(0)$ as the fitting parameter to estimate $\Delta F(0)$ from Eq. (1). A reasonable fit (Fig. 3-3a) is thus obtained with $B_c(0) \approx 0.25$ T. This value is slightly lower than the bulk YBCO value, $B_c(0)$ ~0.5-2 T.[6] This could be due to uncertainties and/or approximations in the fitting model,[10,41] size effects,[42] or surface effects (e.g., loss of oxygen) that reduce the effective w to < 20 nm.

For the w = 10 nm and 15 nm arrays, the transitions are too broad and no simple analytical approximation of $\lambda(T)$ [and therefore $B_c(T)$] is expected to hold over the whole range.[2] On the other hand, because $w << \lambda$, B_c is correlated with the critical current density J_c by:[2,43]

$$J_c = a\frac{B_c}{\mu_0 \lambda} \qquad (3)$$

where a is a constant of order unity, depending on the criterion used for the calculation. For example, the free-energy criterion gives a = 1, whereas Ginzburg-Landau theory

gives $a = (2/3)^{3/2} = 0.544$.[2,43] Using this relationship, Tinkham demonstrated that $\Delta F(T)$ is directly proportional to the critical current $I_c(T)$:[40]

$$\Delta F(T) = \frac{1}{a}\frac{4}{3}\left(\frac{\hbar}{2e}\right) I_c(T) \quad (4)$$

We measured $I_c(T)$ directly, and estimated $\Delta F(T)$ by fitting to Eq. (4), with a as the single fitting parameter. Satisfactory fits were obtained (Fig. 3-3a) with reasonable fitting parameters, $a = 0.95$ and 0.76 for w =10 nm and 15 nm NWs, respectively. These values are quite reasonable, considering that a is the *only* parameter used in fitting. Larger values of a are expected if we take into account that the measured I_c could be less than predicted by Eq.(3) due to heating effects, but such effects may not be significant,[8] considering the very high T_c and the fact that our nanowires are epitaxially anchored to the substrate and in equilibrium with a helium gas during measurement. The deviation of the fits in the low-T limit agrees with the fact that TAPS was originally developed for $T \sim T_c$ and should not be expected to hold at $T \ll T_c$. We, however, cannot completely dismiss the possibility that surface impurities might contribute to the broadening of superconducting transition widths for thinner NWs.

In addition to the much higher T_c, HTS NWs are also less susceptible to suppression of superconductivity from applied magnetic field than are conventional superconductors.[12,13] As shown in Fig. 3-3b and c, a 5-T magnetic field only slightly perturbs the R-T curves of the YBCO NWs. This is because HTS have higher upper critical magnetic fields comparing to conventional superconductors, and also our NWs have $w \ll \lambda \sim 150$ nm.

3.4 Electrical properties of high-temperature superconductor nanowire arrays at high current levels

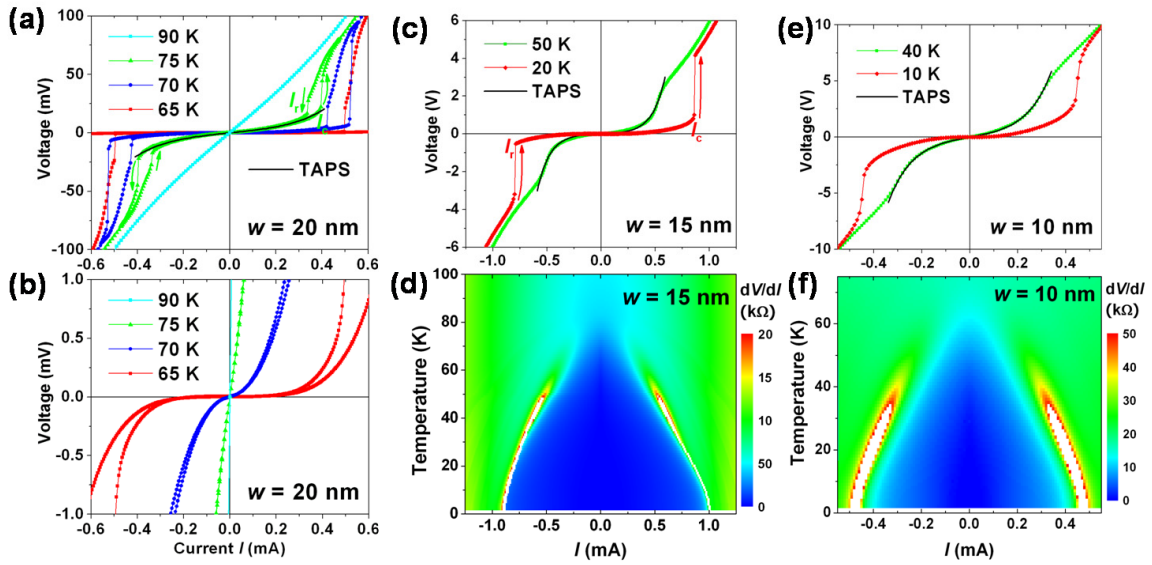

Figure 3-4. Electrical properties of $YBa_2Cu_3O_{7-\delta}$ nanowire arrays in the high-current limit. (a): Four-point *V*-*I* curves for an array of 400 nanowires, *w* = 20 nm and *L* = 5 μm. Measured with both increasing and decreasing current bias (arrows). I_c denotes the critical current, i.e., the highest supercurrent that can be sustained when the applied current is swept up from zero, whereas I_r denotes the retrapping current, i.e., the current level at which the array returns to the superconducting state when the current is swept back down. (b): Expansion of the plot in (a) in the low voltage range. (c) and (d): *V*-*I* curves and d*V*/d*I* as a function of *I* and *T* for an array of 150 nanowires, *w* = 15 nm and *L* = 27 μm. Current sweep is from negative to positive. (e) and (f): *V*-*I* curves and d*V*/d*I* as a function of *I* and *T* for an array of 100 nanowires, *w* = 10 nm and *L* = 50 μm. Black lines are TAPS fits to *V*-*I* curves.

The electrical properties of the HTS NW arrays are also investigated in the high-current limit (Fig. 3-4). We address whether a dissipationless supercurrent can be sustained in HTS NWs. For the w = 20 nm NW array (Fig. 3-4a), at 75 K, although residual resistance is still present (cf. Fig. 3-3a,b), a significant part of the current is already carried by supercurrent, so the voltage drop across the NWs is much smaller than when the NWs are in the normal state (90 K). Sweeping up from zero current, the *V*-*I* relationship in this regime can be modeled with TAPS,[2,12] before the NWs suddenly enter the highly-resistive normal state at critical current I_c. When the current is swept down, the NWs return to the superconducting state at a lower current level, I_r. Such hysteresis has been reported in conventional superconductor NWs (Chapter 2).[13,16,44] At lower T, a larger portion of the current is carried by the supercurrent, resulting in smaller voltage drops, and I_c increases steadily. At 70 K, where the low-current-limit resistance is very close to zero (cf. Fig. 3-3a,b), dissipationless (characterized by a zero voltage drop) supercurrent starts to emerge (Fig. 3-4b). At 65 K, which is still higher than the triple point of nitrogen (63 K), the low-current-limit resistance has dropped below a measureable value, and a dissipationless supercurrent is sustained up to ~0.2 mA.

Similar trends are found for the thinner NWs (Fig. 3-4c,e). Dissipationless supercurrent occurs below the temperature at which the low-current-limit resistance drops to effectively zero (red curves), which is ~20 and ~10 K for w = 15 and 10 nm NWs, respectively. These temperatures are still considerably higher than conventional superconductor NWs. As with NWs of conventional superconductors,[13,44] hysteresis in the *V*-*I* curves is less prominent for thinner NWs.

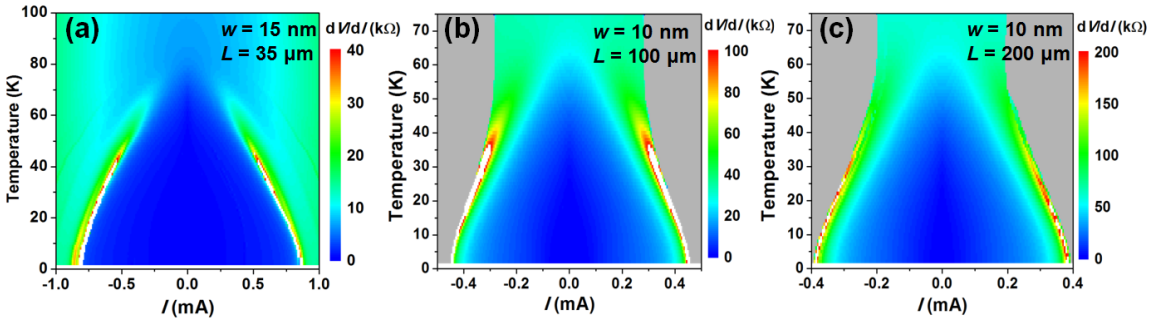

Figure 3-5. Additional differential resistance maps measured on $YBa_2Cu_3O_{7-\delta}$ nanowire arrays. Plotted are d*V*/d*I* as a function of *I* and *T* for (a): an array of 150 nanowires, *w* = 15 nm and *L* = 35 μm, (b): an array of 100 nanowires, *w* = 10 nm and *L* = 100 μm, and (c): an array of 100 nanowires, *w* = 10 nm and *L* = 200 μm. Grey areas in (b) and (c) indicate unmeasured regions in which the voltage level would be too high (> ~20 V) to be safe for our experimental setup. For example, for *R* = 60 kΩ and I = 0.4 mA, *V* = *IR* = 24 V.

The wide superconducting transition-temperature width found in the thinner NWs is further studied by plotting the differential resistance d*V*/d*I* as a function of *I* and *T* (Fig. 3-4d,f). At $T<T_c$, a gap of low differential resistance opens up at low current due to supercurrent, and the width of this gap ($I_c + I_r$) increases steadily with decreasing temperature. Transitions between the superconducting and normal states sharpen, and regions with effectively zero differential resistance start to appear at finite current. In contrast to arrays of conventional superconductor NWs, no peak lines or branching features are observed in the d*V*/d*I*-*T* plots. Similarly clean and featureless d*V*/d*I* plots were obtained for all our YBCO NW devices of various dimensions (Fig. 3-5).

As discussed in Chapter 2, peak line features in d*V*/d*I*-*T* plots are typical for long, conventional superconductor NWs, and reflect multiple voltage-jump steps in *V*-*I* curves.

Each such voltage-jump step is associated with the emergence of a localized resistive "phase-slip center" (PSC) along the NW.[2] Each PSC has characteristic interaction length of ~2Λ, where Λ is the quasiparticle diffusion length (~10 μm for elemental superconductors). Theory predicts that for a uniform filament of length L, approximately $L/2\Lambda$ steps should occur between I_c and $2I_c$,[2,45] and we've previously verified this prediction in Nb NW arrays (Chapter 2).[13] HTS materials have extremely small Λ (<~10 nm for YBCO[46]), so all the NWs investigated in this work satisfy $L>>2\Lambda$, and in this limit PSC steps are not expected to be resolvable.[45] Voltage-jump steps have been previously observed in several studies on HTS micron- and submicron- bridges,[33,34,47] but they are not obviously a consequence of PSCs.[33]

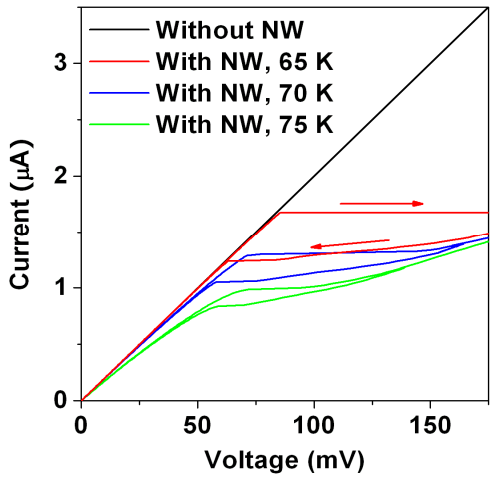

Figure 3-6. High-temperature superconductor nanowire as a current limiter. Simulated current-limiting behavior of an individual YBCO nanowire (width =20 nm) basing on the experimental data shown in Fig. 3-4a. The NW is connected in series with a load resistance of 50 KΩ.

Besides the emerging applications of superconductor NWs in nano-SQUIDs,[22] single-photon detectors,[26] and quantum computing,[23-25] another possible application for HTS NWs is to function as current limiters[48] in nanoelectronic circuits. We simulated the current-limiting behavior of an individual YBCO NW (w = 20 nm) basing on the data shown in Fig. 3-4a (Fig. 3-6). At 75 K, the NW limits the current at high bias voltages, but because the NW is not fully superconducting, at low biases the NW consumes some energy. At T = 65K, the NW is fully superconducting and the current limiter is close to perfect: when $I < I_c$, the NW is a zero-resistance conductor and the I-V characteristics of the circuit is uninfluenced by the NW. When the current in the circuit reaches I_c, the NW transits into the highly-resistive normal state, thus limiting the current to I_c and protecting the circuit. Unlike a standard fuse, this process is fully reversible, so an individual HTS NW could fulfill the function of an automatically recoverable current limiting device, which otherwise is complicated to build with semiconductor circuits. Such devices could be integrated with nanoelectronic circuits while occupying a very small footprint. The limiting current I_c may be varied via the working temperature, the NW dimensions, or numbers of the NWs used.

3.5 Conclusion

In this chapter, we have reported[1] for the first time the preparation and electrical properties of high-temperature superconductor nanowire arrays. We demonstrated that arrays of highly-ordered high-temperature superconductor nanowires can be produced down to w = 10 nm ($<< \lambda$) and up to 200 μm in length, achieving aspect ratios of $>10^4$.

Through four-point electrical measurements on the $YBa_2Cu_3O_{7-\delta}$ nanowire arrays, we found high-temperature superconductivity is retained in these nanowires. All nanowires exhibit a superconducting transition above liquid nitrogen temperature, and a transition temperature width that depends strongly upon the nanowire dimensions. The *w* = 20 nm NWs become fully superconducting and are capable of carrying dissipationless current at pumped liquid nitrogen temperatures. For thinner nanowires, the transition temperature widths are significantly broadened to ~60 K, and complete superconductivity is achieved at ~20 and ~10 K for *w* = 15 and 10 nm nanowires, respectively. In high-current measurements, voltage-jump steps are not observed due to the small quasiparticle diffusion length.

We have also demonstrated for the first time the applicability of phase-slip theories in explaining the size effects in high-temperature superconductor nanowires. All experimental results are modeled satisfactorily using phase-slip theories that generate reasonable parameters. Furthermore, these nanowires can function as superconducting nanoelectronic components with broader working temperature ranges as compared to conventional superconductor nanowires.

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Chapter 4

The Crossover from Two Dimensions to One Dimension in Granular Electronic Materials

The contents presented in this chapter are based on K. Xu, L. Qin, and J. R. Heath, "The crossover from two dimensions to one dimension in granular electronic materials," *Nature Nanotechnology,* advanced online publication; digital object identifier: 10.1038/nnano.2009.81 (2009). (Ref. [1])

4.1 Introduction

A particularly rich area of nanoscale science is the investigation of low-dimensional systems, such as two-dimensional (2D) thin films,[2] one-dimensional (1D) nanowires,[3,4] and zero-dimensional (0D) quantum dots (QDs).[5-7] In such systems, the electronic structure of the material and the statistical distribution of charge transport pathways are strongly influenced by the dimensionality. An equally rich area, but one that is more difficult to investigate, is the physics associated with dimensional cross-over.

Granular electronic materials,[8] in principle, provide the flexibility for investigating such dimensional cross-overs. Granular electronic materials are solids comprised of densely-packed conductive nanoparticles (particles ~10 nm in diameter), and their electrical properties are determined by both the nature of the composite nanoparticles and by their packing arrangement.[8] Through separate control over the

constituent grains and over the grain organization, granular electronic materials provide a unique framework for manipulating and understanding solid-state electrical properties. In particular, because the constituent nanoparticle properties[9] are independent of how they are assembled, pure packing-arrangement effects, including dimensional effects, can be studied.

Indeed, granular materials self-assembled from monodisperse, chemically synthesized colloidal QDs (sufficiently small nanoparticles exhibit charge and energy quantization and are often called QDs, referring to the quantum confinement in all three spatial dimensions)[5-7] into highly ordered 3D and 2D architectures[7,10-13] have provided a laboratory for investigating new physics, including, for instance, the long-range resonance transfer of electronic excitations in 3D QD solids[7] and the metal-to-insulator transition in 2D QD superlattices.[10,11] In contrast, attempts to assemble nanoparticles into ordered 1D (single-file nanoparticle arrays/chains) or quasi-1D granular structures have only achieved limited success,[14-19] largely due to the difficulty in obtaining continuously connected 1D superstructures.

In this chapter, we describe[1] a novel method for the assembly of 5 nm and larger nanoparticles into granular solids that can be tuned continuously from 2D to 1D. We report on the electrical properties of the novel 1D granular solids, and systematically establish how electron transport through these systems evolves from the previously studied 2D limit to the strictly 1D limit. We find the electrical properties of 1D granular systems are fundamentally different from 2D systems. The energy barriers to transport increase in the 1D limit, in both the variable-range-hopping (low-voltage) and sequential-tunneling (high-voltage) regimes. In the variable-range-hopping regime, we

experimentally determine the relevant dimensional factor that describes the 2D→1D transition. In the sequential-tunneling regime, we find an unexpected relationship between the temperature, and the voltage at which the conductance becomes appreciable - a relationship that appears peculiar to 1D systems. These results are explained by extrapolating existing granular conductor theories to 1D.

4.2 Assembly of quantum dots into one-dimensional and quasi-one-dimensional granular electronic materials

We employed a template-directed approach to align QDs into densely packed 1D superstructures, utilizing surface interactions between nanopatterned substrates and QD solutions. Similar methods have been employed to fabricate ordered nano/micro sphere assemblies over the particle size range from microns to 50 nm.[20-22] In this study, ordered QD 1D assemblies were achieved by precisely controlling the widths of nanopatterned 1D trenches (the templates), to within ~1 nm, utilizing QDs characterized by a narrow size distribution, and controlling the QD/trench chemical interface.

Arrays of SiO_2 nanotrenches were fabricated using superlattice nanowire pattern transfer (SNAP)[23,24], which, as discussed in Chapter 2, translates the atomic control over the film thicknesses within a GaAs/$Al_xGa_{1-x}As$ superlattice into control over the width and spacing of nanotrenches. The nanotrench surfaces were chemically functionalized with hexamethyldisilazane. The resultant hydrophobic substrate was dip-coated in a toluene solution of QDs (Fig. 4-1a,b). A wetting meniscus was formed in the process.

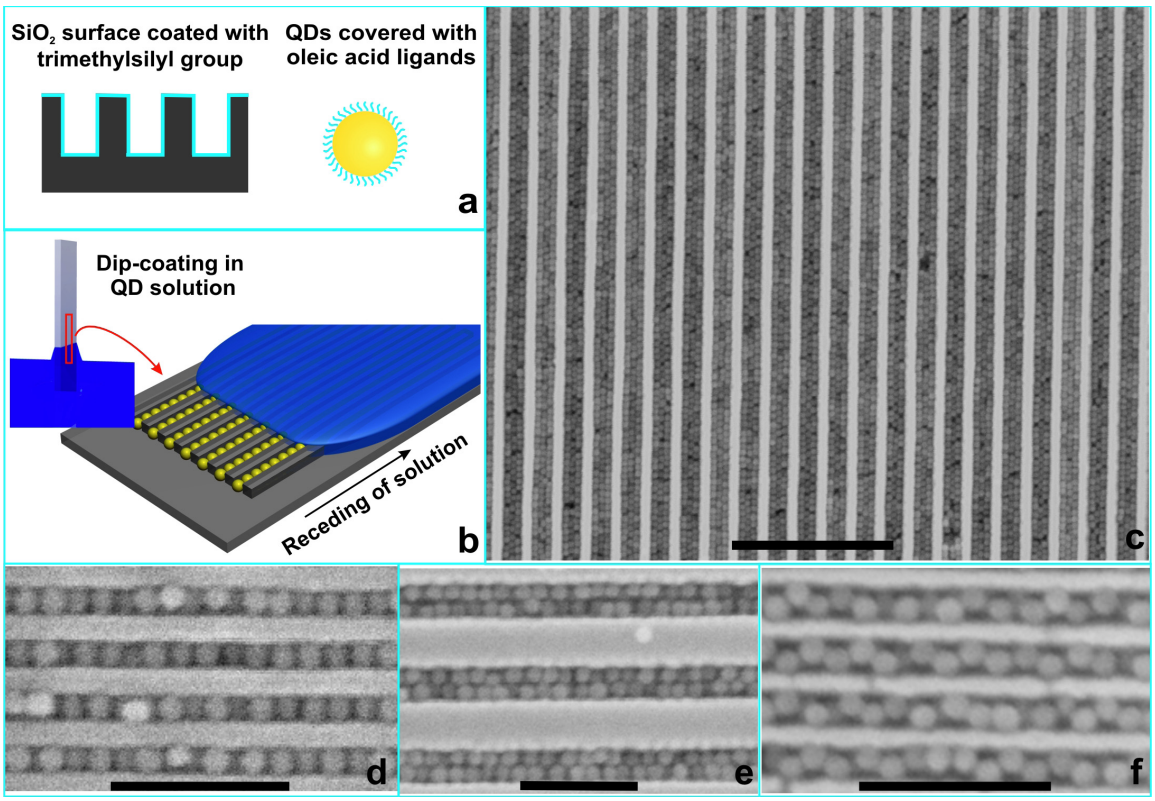

Figure 4-1. Assembling quantum dots (QDs) into 1D and quasi-1D arrays. (**a):** Surface functionalization of silica nanowire/nanotrench arrays and the schematic diagram of a QD and its surface ligands. (**b):** The dip-coating method to fabricate QD arrays: 1D QD arrays are formed as the QD solution recedes along the nanotrench substrate. (**c)-(f):** Scanning electron microscope images of **(c)** 3-line, **(d)** 1-line, **(e)** 2-line, and **(f)** 1.5-line (zigzag) QD arrays of 15 nm magnetite QDs. Scale bars: **(c)**, 400 nm, **(d)**-**(f)**, 100 nm.

Closest-packed QDs fill the nanotrenches (Fig. 4-1,c-f). Fig. 4-1c shows the fidelity of this technique: well ordered, 3-QD wide, closest packed structures are observed in each of the nanotrenches, with lengths of up to 1 mm. The QD solution coats the entire wafer during dip-coating, but only leaves a single layer of QDs deposited within the trenches under optimized experimental conditions – a result that likely arises

from the increased QD/surface interactions within the trenches. The packing pattern can be fine-tuned by either adjusting the trench width (Fig. 4-1c-f), or the QD size or shape (Fig. 4-2).

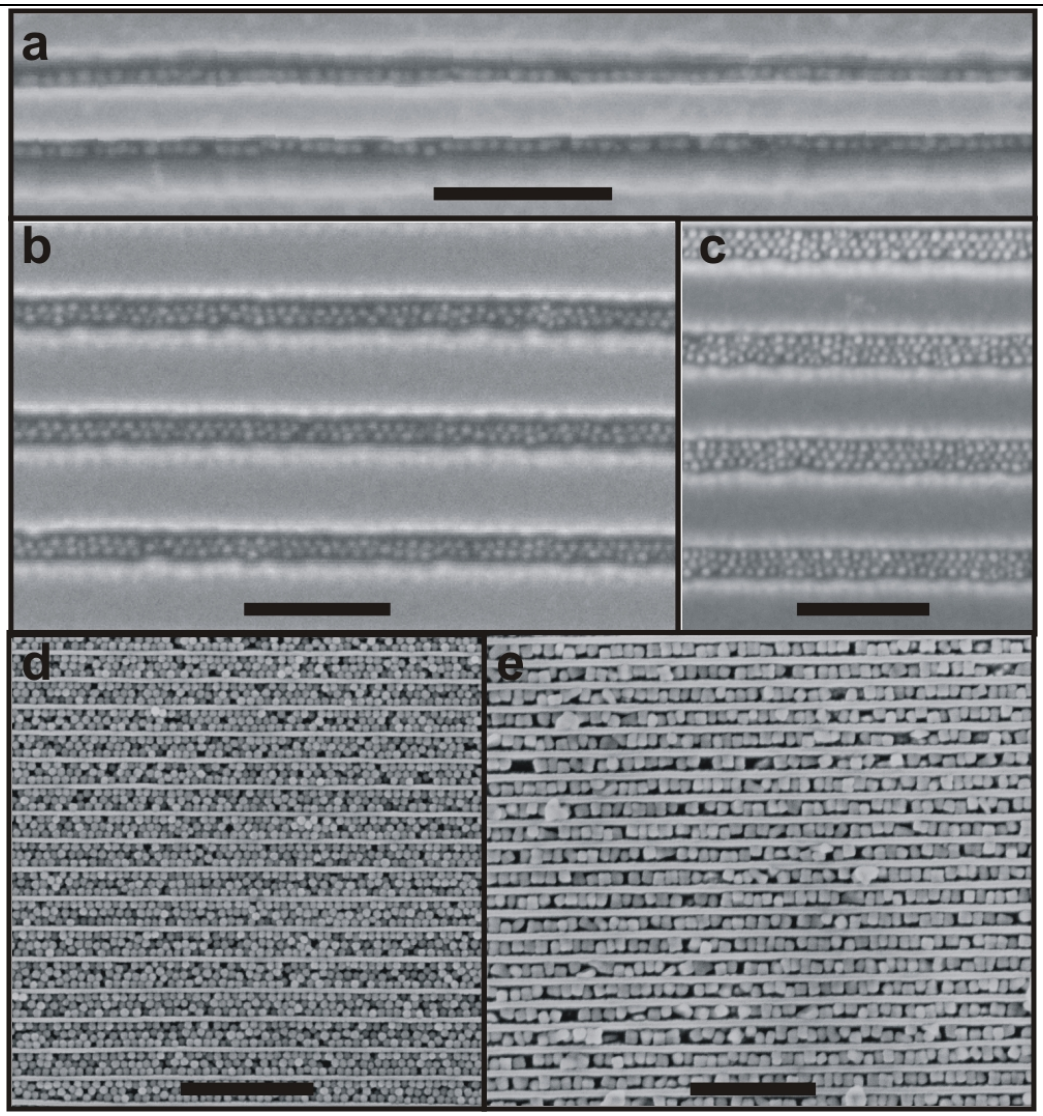

Figure 4-2. Scanning electron microscope (SEM) images of assembled quantum dot (QD) arrays, using QDs of varied sizes and shapes. SEM images of **(a)** 1-line, **(b)** 2-line, **(c)** 3-line arrays of 5 nm Au QDs. **(d)** 3-line arrays of 25 nm magnetite QDs. **(e):** 1-line arrays of 40 nm cuboid magnetite QDs. Scale bars: **(a), (b), (c),** 100 nm; **(d), (e),** 400 nm.

As shown in Fig. 4-2, our assembly method is independent of the specific material or shape of the QDs, and works well for trench widths of 5 nm and larger. However, we note that the assemblies presented in Fig. 4-2 are not intended for electrical measurements, and so went through significantly less optimization of experimental conditions than did the ones used for the electrical measurements as discussed in this chapter.

The detailed fabrication processes are described below.

A. SiO_2 SNAP nanotrench array preparation. An array of Pt SNAP nanowires was obtained by e-beam evaporation onto the raised edges of a differentially etched edge of a epitaxially grown GaAs/$Al_xGa_{(1-x)}As$ superlattice wafer (IQE, Cardiff, UK).[23] The array of Pt SNAP nanowires was transferred as an ink onto a 300 nm thick, thermally grown SiO_2 layer on top of a silicon substrate. A thin (~10 nm) layer of heat-curable epoxy (EpoxyBond 110, Allied High Tech, Rancho Dominguez, CA) was used to securely bond the Pt nanowire array to the surface. The superlattice/nanowire array/epoxy/SiO_2 substrate assembly was baked on a hot plate at 150 °C for 15 min, and the superlattice was then released by a wet etch in a $H_3PO_4/H_2O_2/H_2O$ (5:1:50 v/v, 4.5 h) solution, leaving a highly aligned array of Pt nanowires on the surface of the SiO_2 substrate. The Pt nanowire array served as the protective mask for a reactive-ion-etch (RIE) process to produce a highly ordered SiO_2 nanowire/nanotrench array. A highly directional, 40 MHz Unaxis SLR parallel-plate RIE system was implemented to produce 50 nm deep trenches in SiO_2 using CF_4/He (20/30 sccm, 5 mTorr, 40 W). The Pt nanowires were then dissolved in aqua regia (3:1 HCl:HNO_3) at boiling temperature for 30 minutes. The wafer was then rinsed with water and dried with nitrogen blow, and

heated in PRX-127 (Rohm & Haas LLC.) to remove residual epoxy and other possible organic contaminants. Eventually, a highly ordered, ultrahigh-density array of SiO_2 nanowires/nanotrenches is obtained with clean surface. The width of each nanowire is controlled by the thickness of the $Al_xGa_{(1-x)}As$ epilayers in the starting superlattice wafer, while the width of each nanotrench is controlled by the thickness of the GaAs epilayers. The number of nanowires/nanotrenches in the array is controlled by the number of epilayers in the superlattice wafer.

B. SNAP nanotrench array surface functionalization. The as-prepared nanotrench array wafer was heated in a piranha solution (3:1 H_2SO_4:H_2O_2) at 120 °C for about 10 minutes, rinsed with water, and dried on a hot plate at 160 °C. The wafer was then surface-functionalized by exposure to a hexamethyldisilazane (Sigma-Aldrich) vapor within a sealed chamber. The resulting hydrophobic substrates formed a wetting meniscus contact with a toluene solution of QDs.

C. QD solution preparation. QDs covered with oleic acid ligands are used in this study. All the magnetite QD solutions were purchased from Ocean Nanotech Inc. (Fayetteville, AR). For the 15 nm QDs, the as-purchased chloroform solution (48 mg/ml) was diluted 40 times with toluene toward a final concentration of 1.2 mg/ml. The diluted QD solution appeared dark gray and QDs were completely dispersed without any precipitates. The 25 nm and 40 nm magnetite QD solutions were prepared with the same protocol to a concentration of 1.5 mg/ml and 2.0 mg/ml, respectively. 5 nm Au QDs, which were a generous gift from Xingchen Ye in Christopher Murray lab in University of Pennsylvania, were dissolved in toluene at a final concentration of 5.0 mg/ml.

D. Assembling QDs into nanotrench arrays. The QD assembly step was performed by dip-coating a surface-functionalized SiO_2 nanotrench array wafer in a toluene solution of QDs. The wafer, clamped by a pair of tweezers and fixed onto a syringe pump (NE-1000 programmable syringe pump, New Era Pump Systems, Inc.), was slowly withdrawn from the QD solution at a finely controlled speed (~0.5 mm/min) set to the gears of the pump. The speed was optimized for the formation of a close-packed monolayer inside each nanotrench, as discussed below.

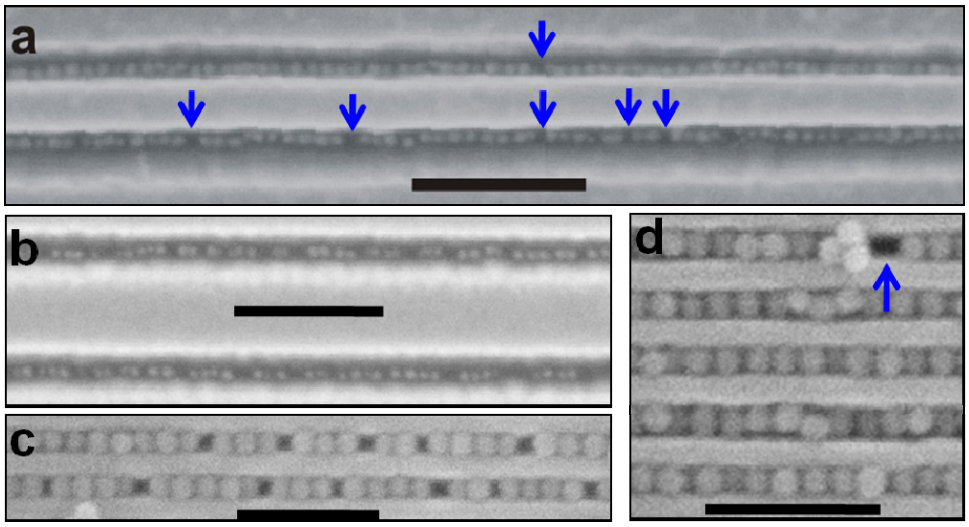

Figure 4-3. Additional scanning electron microscope images for **(a):** *d* ~5 nm Au QDs assembled in ~50 nm deep trenches at a dip-coating speed that is slightly higher than the optimal speed. Blue arrows point to missing particles. **(b):** *d* ~5 nm Au QDs assembled at a still higher dip-coating speed. **(c):** 15 nm magnetite QDs assembled at a dip-coating speed that is slightly higher than the optimal speed. **(d):** 15 nm magnetite QDs assembled at the optimized speed. Blue arrow points to a defect (missing particle).

E. Dip-coating speed optimization. The number of layers inside each nanotrench can be controlled by adjusting the concentration of the QD solution and the dip-coating

speed. For example, for the 1D assembly of *d*~5 nm Au QDs, when the number of layers inside each nanotrench was controlled to be slightly below 1, defects were observed as missing particles in the arrays (blue arrows in Fig. 4-3a). When a higher dip-coating speed was used, the QD coverage was further reduced, and the submonolayer coverage resulted in discontinued QD 1D lines inside the nanotrenches (Fig. 4-3b). For all the QD arrays fabricated for electrical measurements, the QD concentration and dip-coating speed were carefully optimized to keep the number of layers inside each nanotrench to be as close to 1 as possible. We typically begin with higher dip-coating speeds, at which clear submonolayers of QDs form in the nanotrenches (Fig. 4-3c). We then gradually reduce and optimize the dip-coating speed to achieve close-packed monolayers inside each nanotrench. Once optimized, the speed is stable and can be applied to multiple SNAP nanotrench arrays. For QD arrays assembled at the optimized speed, sparse defects (missing particles) indicate that there are no additional QDs beneath the QD arrays (Fig. 4-3d). These sparse defects, however, are not expected to affect our measurements, due to the large number of parallel channels.

F. Annealing of magnetite QD arrays. All assembled magnetite QD arrays were annealed to form a conductive phase.[25-27] The wafer with QD arrays was heated up to 400 °C and annealed at the temperature for 60 minutes under the protection of ultra-high purity argon in a tube furnace (Linderberg, Model 54233), and then cooled down to room temperature overnight. The annealed QD arrays kept their original shape and arrangement as confirmed by scanning electron microscopy.

G. Fabricating electrodes to contact the QD arrays. Metallic contact electrodes were patterned across the annealed QD arrays using electron-beam lithography. Two

parallel electrodes (30 nm thick Ti and 150 nm thick Au), separated by a designed distance (from 50 nm to 500 nm), were precisely positioned across QD arrays according to alignment markers that were patterned on the wafer in an earlier step. The two electrodes were then connected to two large (150 μm × 150 μm) Au pads from opposite directions (Fig. 4-6a), so the measured current is transmitted through a well-defined number of QD arrays. The pads were then wire-bonded to a chip carrier.

H. Temperature and magnetic field dependent electrical measurements. All electrical measurements were carried out in a Magnetic Property Measurement System (MPMS-XL, Quantum Design Inc.) with standard DC techniques using a Keithley 6430 sub-femtoamp remote sourcemeter.

4.3 Electrical properties in the low-voltage, variable-range-hopping regime

The assembly method typically generates >100 identically packed parallel QD arrays. This enabled us to carry statistical numbers of temperature-dependent electrical and magneto-transport measurements. The insulating SiO_2 trench walls prevent electrical crosstalk between adjacent QD arrays. Magnetite QDs, used as our model system, are half-metallic, and strong magnetoresistance effects have been reported in magnetite QD films .[25]

To characterize how the 2D→1D cross-over influences the electrical properties of granular electronic systems, we investigated a single QD size (15 nm), and varied the trench widths to control the number of QDs across the width of each array. Quasi-1D arrays with 3 (Fig. 4-1c), 2 (Fig. 4-1e), and 1.5 (zigzag structure, Fig. 4-1f) QDs across

the width, as well as 1D linear arrays (Fig. 4-1d) were studied and compared with a close-packed QD monolayer film. Elteto *et al.* found that quasi-1D QD arrays as narrow as four-QD wide are electronically similar to full 2D arrays[16].

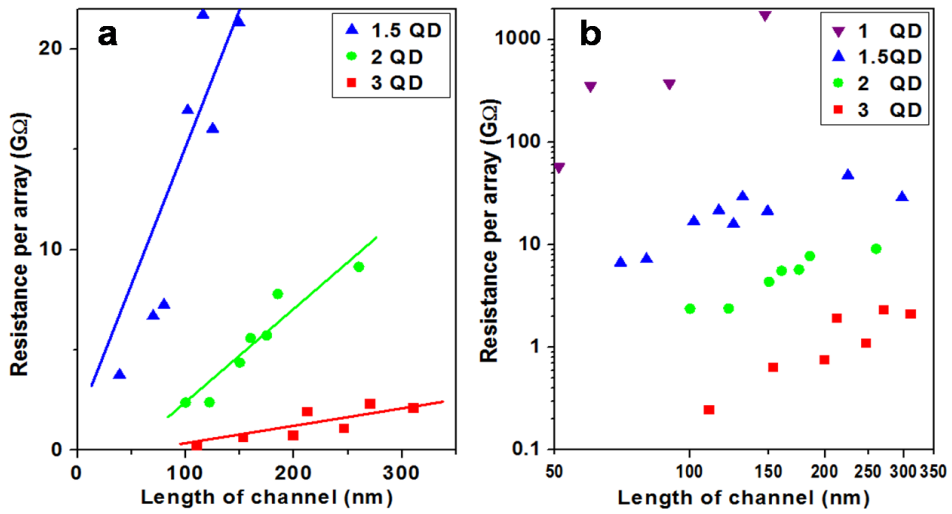

Figure 4-4. Measured resistance per array at room temperature as a function of array length for quasi-1D and 1D QD arrays with different widths. (a): Plotted on linear scales. (**b)**: Plotted on logarithmic scales. The number of QDs across the width of each array is label in the graph. 1D zigzag arrays are labeled as 1.5 QD.

We fabricated a number of devices, each contacting 50 to 400 parallel, identically packed 1D or quasi-1D arrays (Fig. 4-6a), and plotted the measured resistance per array as a function of array length (Fig. 4-4). A linear dependence is observed, indicating that the device transport properties are dominated by the QD arrays with negligible contribution from contacts. In addition, consistent trends are found for different arrangement of QD arrays: data from arrays with the same designed number of QDs across the width of each array follow the same linear trend, whereas much larger resistance per array is found as the number of QDs across is reduced. Due to the large

number of parallel channels, defects, such as missing particles, are not expected to affect the measurements at the array lengths reported here.

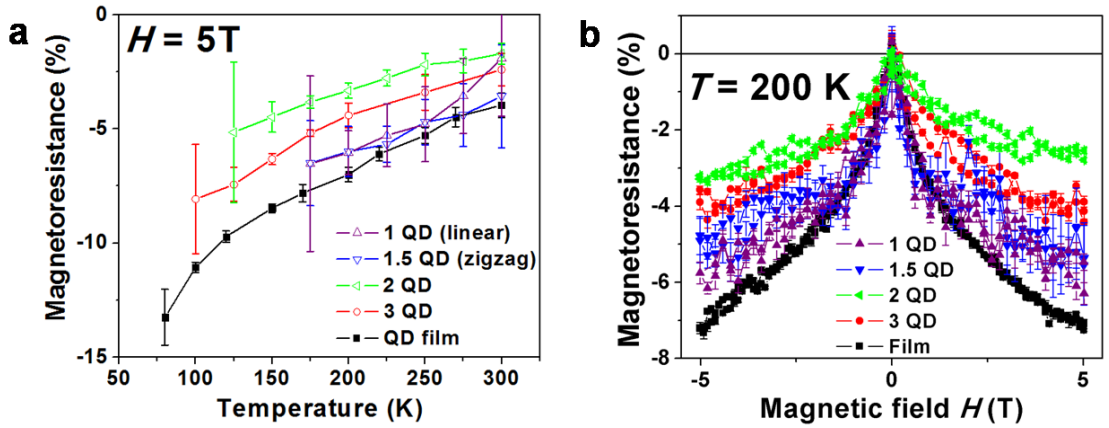

Figure 4-5. Magnetoresistance response of the QD arrays. (a): Magnetoresistance at an applied magnetic field of 5 T, as a function of temperature. (**b**): Magnetoresistance at 200 K, as a function of applied magnetic field. Magnetoresistance is defined by the percentage change of resistance when an external magnetic field is applied. The number of QDs across the width of each array is label in the graph. 1D zigzag arrays are labeled as 1.5 QD.

We have also measured the magnetoresistance (MR) response of all magnetite QD arrays investigated in this study. MR is defined by the percentage change of resistance when an external magnetic field is applied. Large negative MR is found for all devices (Fig. 4-5), and similar temperature trends are found for all devices. This verifies that the electrical properties measured in our experiments arise from the magnetite QD arrays, since positive and much smaller MR is expected for conductance through non-magnetic materials. Reduced MR is found for quasi-1D and 1D arrays comparing to the QD film, possibly due to surface effects.[26,28]

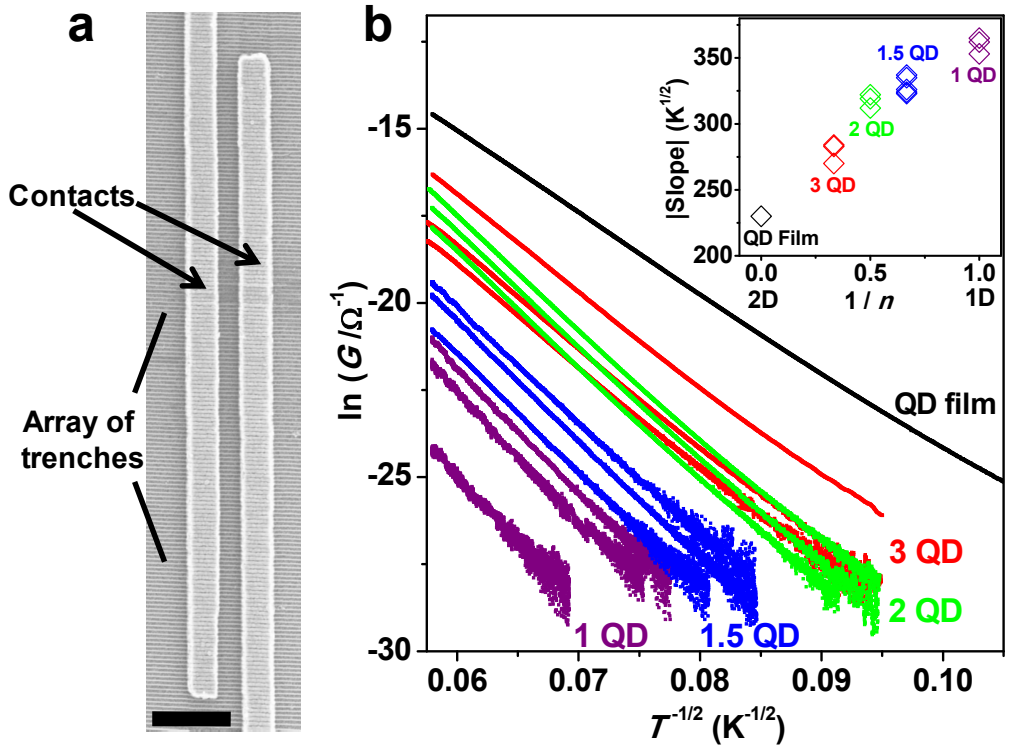

Figure 4-6. Low-bias conductance measurement of the QD arrays. (a): Scanning electron microscope image of a typical device used in the electrical measurements, which contacts 160 parallel 1D QD arrays. Scale bar: 1 μm. **(b):** Temperature-dependent conductance at low voltage bias. The number of QDs across the width of each array is labeled in the graph. 1D zigzag arrays are labeled as 1.5 QD. Inset: ln(G)-$T^{-1/2}$ slopes of the QD arrays, plotted as a function of the dimensionality of the system. n is the number of QDs across the width of each array.

The conductance (G) of the QD arrays was studied at low (<100 mV) applied voltage bias as a function of temperature (T) (Fig. 4-6b). A linear dependence was found for all arrays when G is plotted on a logarithmic scale against $T^{-1/2}$, in agreement with previous studies on 2D and 3D QD assemblies.[25,29-32] Such behavior is commonly ascribed[29-32] to the Efros-Shklovskii variable range hopping (ES-VRH),[33] or super-

exchange,[34] transport mechanisms, although recent studies have also suggested alternative mechanisms,[8,32] e.g., elastic and inelastic cotunneling.[8,35,36] We employ the ES-VRH model to explain our data because that model has been the most widely used and permits the broadest comparison of our results against the literature.

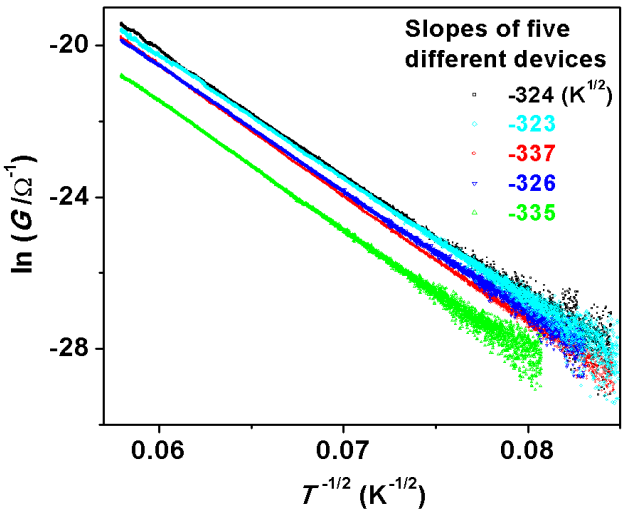

Figure 4-7. The temperature-dependent conductance data obtained on five different 1D zigzag (1.5 QD) array devices. The slopes of each set of data are labeled in the graph.

Precisely controlled assembly helps to reveal trends in our *G*-*T* data: similar ln(*G*)-$T^{-1/2}$ slopes were found for devices with the same designed numbers of QDs across the width of each array. For example, for 1D zigzag (1.5 QD) arrays, we have performed temperature-dependent conductance measurement on five different devices, and the full dataset is re-plotted with different colors in Fig. 4-7. Consistent results [in particular, the ln(*G*)-$T^{-1/2}$ slopes, as labeled in the graph] are observed for different devices. We have presented the ln(*G*)-$T^{-1/2}$ slopes obtained from the five sets of data in the inset of Fig. 4-6b, but only plotted three sets of the conductance data in Fig. 4-6b due to the overlapping

between data obtained from different devices. On the other hand, notably (up to ~60%) steeper slopes were observed as the QD assemblies cross over from 2D to 1D (Fig. 4-6b inset).

The steeper $\ln(G)$-$T^{-1/2}$ slopes indicate an increasing energy barrier for charge transport accompanies the 2D-1D crossover. According to VRH,[33,37] the charge transport efficiency is determined by the optimal hopping network, which in turn is determined by competition between the hopping distance and the number of available energy levels at a given distance. ES-VRH predicts a linear $\ln(G)$-$T^{-1/2}$ relationship:[33]

$$G(T) \sim \exp[-(T_0/T)^{1/2}], \quad T_0 = \beta_D e^2/\kappa a, \qquad (1)$$

where e is the electron charge and κ is the dielectric constant. a is the localization length, which characterizes the decay length of electronic wave functions, and in QD arrays is approximately the size of each QD.[30,31] The coefficient β_D depends on the system dimensionality, D, and should increase as D is reduced; establishing a (percolating) hopping network becomes increasingly difficult with reducing dimensions, and so the energy barrier for conductance is higher. For 3D and 2D cases, theory and simulations indicate[38,39] β_3 ~2.8, and β_2 ~6.5. No theoretical investigation of β_1 has been reported. Our data allow for an experimental determination of β_1. The consistent trend of the $\ln(G)$-$T^{-1/2}$ slopes suggests that β_D increases progressively as the array evolves from 2D to 1D. For the 1D linear arrays, the absolute value of the $\ln(G)$-$T^{-1/2}$ slope is increased to 360 $K^{1/2}$ from 230 $K^{1/2}$ in 2D. Consequently, assuming similar localization lengths for 1D and 2D arrays, this suggests β_1/β_2 ~$(360/230)^2$=2.45 and β_1~16. This result is plausible, considering a 2.3-fold (6.5/2.8) increase in β_D is found for 2D systems compared to 3D systems.

4.4 Electrical properties in the high-voltage, sequential-tunneling regime

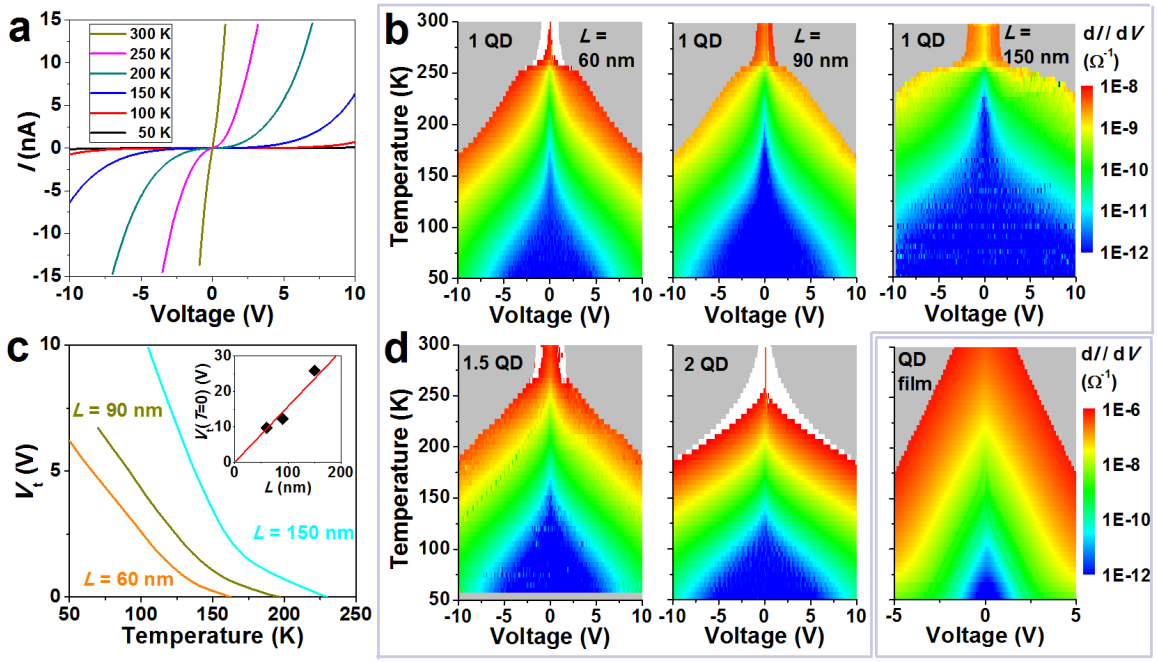

Figure 4-8. Electrical properties of the QD arrays at high voltage. (a): *I-V* curves of a QD 1D linear array device measured at various temperatures. **(b):** Differential conductance (d*I*/d*V*) as a function of voltage and temperature for 1D linear arrays with varied lengths. White areas indicate regions in which the differential conductance is higher than the upper limit of the color scale. Gray areas indicate unmeasured regions in which the current level would be higher than the upper compliance of current (~20 nA) set to protect the devices. **(c):** Threshold voltage as a function of temperature for the three devices in **(a)**. Inset: extrapolated threshold voltage at 0 K as a function of length. **(d):** Differential conductance as a function of voltage and temperature for a 1D zigzag QD array device, a quasi-1D device with 2 QDs across the width of each array, and a 2D QD monolayer film. The color scale shown in (b) applies to the 1D zigzag and quasi-1D devices, whereas the expanded scale in (d) applies for the QD film device. Gray areas indicate unmeasured regions.

At low temperature, conductance due to the thermally activated hopping processes falls below the detection limit at low bias voltages. On the other hand, high bias voltages can overcome the Coulomb blockade and result in measurable conductance through sequential tunneling between nearest-neighbor particles. This different mechanism of conductivity should yield different dimensional/geometric effects.

Fig. 4-8a presents the *I*-*V* curves measured on a 1D linear QD array device at different temperatures. As the temperature is lowered from room temperature, a gap of low current opens up at low voltages,[15,32,40,41] and a finite threshold voltage V_t is required for the onset of appreciable ($>5\times10^{-12}$ Ω^{-1}) conductance. To further characterize how the electrical properties evolve for all temperatures, we present in Fig. 4-8b the differential conductance d*I*/d*V* measured on three 1D linear array devices as a function of both *V* and *T*, from which the V_t–*T* relationship can be readily identified (Fig. 4-8c).

V_t is found to be directly proportional to the length of the assembly, *L*, both for 1D linear arrays (Fig. 4-8c) and zigzag arrays (Fig. 4-9). This result was predicted:[42,43] V_t, the overall energy barrier for charge transport, is proportional to the number of tunneling barriers in the conduction path, which is in turn proportional to *L*. This contrasts with the low-voltage VRH conductance, in which the relevant energy barrier for charge transport (T_0) only depends on the localization length and the dimensionality of the system (Eq. 1). As a result, similar $\ln(G)$-$T^{-1/2}$ slopes are found for different devices with the same numbers of QDs across the width of each array, regardless of *L* (Fig. 4-6b).

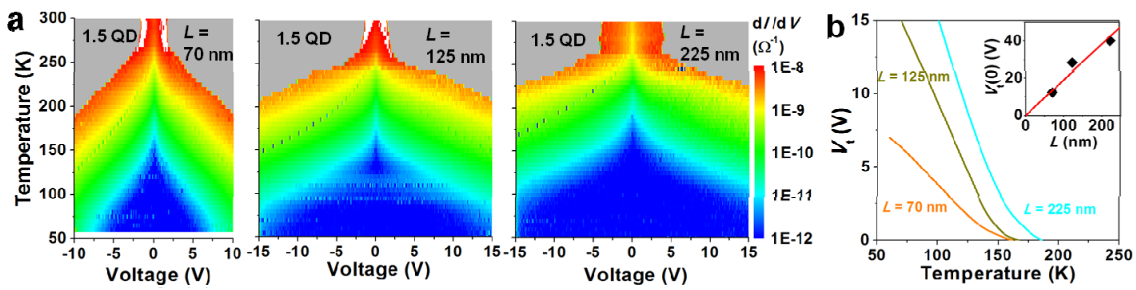

Figure 4-9. Additional data on the electrical properties of the 1D zigzag QD arrays at high voltage. (a): Differential conductance (d*I*/d*V*) as a function of voltage and temperature for 1D zigzag arrays with varied lengths. Gray areas indicate unmeasured regions in which the current level would be higher than the upper compliance of current (~20 nA) set for the protection of the devices. **(b):** Threshold voltage as a function of temperature for the three devices in **(a)**. Inset: extrapolated threshold voltage at 0 K, as a function of length.

For the 1D arrays, a linear V_t-T relationship is observed at low T, but at high T and low V, a pronounced sublinear V_t-T relationship is found (Fig. 4-8b,c). This indicates that more thermal energy is required to overcome the remaining energy barriers for charge transport. Linear V_t-T relationships have been previously observed, up to the temperature that V_t drops to 0, in 2D QD assemblies[40,41] and quasi-1D chains of irregular nanoparticles,[15] and explained by theory.[43,44] The sublinear V_t-T relationship we find has not been previously predicted or observed. Our results (Fig. 4-8, Fig. 4-9, and Fig. 4-10) indicate that this phenomenon is peculiar to 1D QD arrays: the sublinearity is pronounced in both the 1D linear and zigzag arrays, barely seen in 2-QD-wide quasi-1D arrays, and not observed at all in wider quasi-1D QD arrays or 2D QD films.

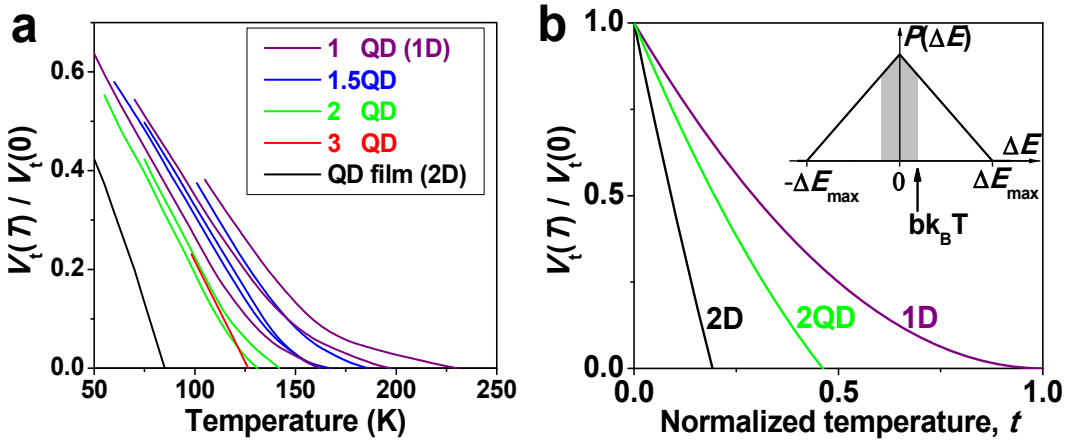

Figure 4-10. Temperature dependence of the threshold voltage. (a): Experimental threshold voltage-temperature dependence measured on different QD array devices. The threshold voltages are normalized to the extrapolated values at 0 K. The number of QDs across the width of each array is labeled in the graph. 1D zigzag arrays are labeled as 1.5 QD. **(b):** Theoretical threshold voltage-temperature dependence. Black and purple lines are for 2D and 1D cases, respectively. The green line is for an intermediate case with p_c = 0.71, corresponding to 2-QD-wide quasi-1D arrays (Supplementary Information). t is the normalized temperature: $t = bk_BT/\Delta E_{max}$. Inset: probability distribution for ΔE in tunneling events.

This novel sublinear V_t-T relationship can be explained by extrapolating the theory discussions of Jaeger *et al*.[41,43] Consider the case when the coupling capacitance between QDs is negligible compared to C_0, the capacitance of an individual QD. When an electron tunnels from a QD to its nearest neighbor, the energy change for the system, ΔE, falls into the range of $[-\Delta E_{max}, \Delta E_{max}]$, where $\Delta E_{max} = e^2/C_0$, and a triangle-shaped distribution of the probability density, $P(\Delta E)$, is expected (Fig. 4-10b inset).[41] A finite temperature broadens the energy levels of the QDs, and conduction barriers are removed

for neighboring QDs satisfying $|\Delta E| < bk_BT$, where b ~2.4 characterizes the extent of thermal broadening of the Fermi-Dirac distributions in QDs.[43] When the fraction of conduction barriers being removed, $p(T)$, reaches the bond percolation threshold of the lattice, p_c, a continuous path with all barriers removed emerges, and $V_t(T)$ drops to 0. The V_t-T relationship is thus modeled as $V_t(T)/V_t(0) = 1-p(T)/p_c$.[43]

Previous studies[41,43] have considered the 2D case, where p_c~0.347 is small due to the existence of multiple possible pathways. Only 34% of all the conduction barriers need to be overcome for $V_t(T)$ to drop to 0 (the shaded area in the Fig. 4-10b inset). In this region, $P(\Delta E)$ is effectively constant, so the same increment of temperature results in the removal of the same number of conductance barriers. As a result, a linear V_t-T relationship is observed.

By contrast, 1D lattices have only a single pathway available for tunneling conductance (p_c=1), and so every tunnel barrier must be overcome for current to flow. Because $P(\Delta E)$ is considerably smaller for larger $|\Delta E|$, smaller numbers of barriers are removed for an equal temperature increase at higher T. In particular, since $P(\Delta E)$ drops towards zero when $|\Delta E|$ approaches ΔE_{max}, the last small fraction of barriers that keep V_t from dropping to 0 are especially difficult to overcome. This explains the sublinear dependence of V_t on T we find at high temperature and low bias.

By integrating $P(\Delta E)$ from $-bk_BT$ to bk_BT, we have plotted the theoretical V_t-T relationship (Fig. 4-10b). The results satisfactorily capture our experimental data (Fig. 4-10a) for the 2D and 1D cases, and support our observation that the sublinearity is peculiar

to truly 1D QD arrays: p_c drops rapidly below 1 for quasi-1D arrays; for 2-QD-wide arrays, p_c~0.71, and the sublinearity becomes much less noticeable (Fig. 4-10b).

Here the calculation of the bond percolation threshold, p_c, for 2-QD-wide quasi-1D arrays was carried out using computer simulations. The model system was a 2-QD-wide quasi-1D array 15 QDs in length, arranged in a close-packed triangle lattice (Fig. 4-11 inset), similar to those investigated in our experiment. A Monte-Carlo method was used to randomly add in connecting bonds between neighboring sites, until a fully connected pathway was formed from the left end of the array to the right end. p_c was then calculated as the number of connecting bonds used divided by the number of all possible bonds.[45] ~500,000 rounds of simulation were carried out, and the resultant distribution of p_c is plotted in Fig. 4-11, yielding $p_c = 0.71 \pm 0.19$ (95% confidence).

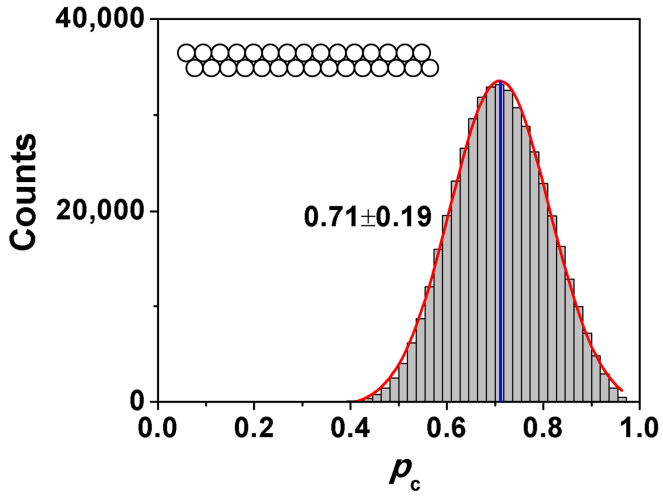

Figure 4-11. Computer simulation results of the bond percolation threshold for 2-QD-wide quasi-1D arrays. Inset: the model system used for the simulation.

Similar V_t-T behaviors were observed for 1D linear and zigzag arrays, because they are topologically equivalent for percolation in the tunneling regime, i.e., each QD has two nearest neighbors for charge tunneling. In contrast, in the VRH regime, the zigzag arrangement allows for an increase in the density of hopping pathways, and therefore appreciably smaller β_D and $\ln(G)$-$T^{-1/2}$ slopes are found relative to the linear arrangement (Fig. 4-6b inset).

4.5 Conclusion

The described[1] approach for assembling arrays of monodisperse quantum dots permits the electron transport properties of granular systems to be characterized across the 2D-1D dimensional cross-over. The electrical properties of 1D granular systems are significantly different from 2D systems, due to the single available transport pathway in one dimension. The energy barriers to transport increase in the 1D limit, in both the variable-range-hopping (low-voltage) and sequential-tunneling (high-voltage) regimes. In the variable-range-hopping regime, we experimentally determine the relevant dimensional factor that describes the 2D→1D transition. In the sequential-tunneling regime, we find an unexpected relationship between the temperature, and the voltage at which the conductance becomes appreciable - a relationship that appears peculiar to 1D systems. These results are explained by extrapolating existing granular conductor theories to 1D.

Harnessing related approaches to characterize other, equally rich transport phenomena, such as thermal conductance, represents an exciting future challenge. In

Chapter 6, we will further discuss how similar assembly methods can be tailored to produce ordered 2D arrays of quantum dots.

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Chapter 5

The Emergence of a Coupled Quantum Dot Array in a Silicon Nanowire Gated by Ultrahigh Density Top Gate Electrodes

The contents presented in this chapter are based on the experimental part of K. Xu, J. E. Green, J. R. Heath, F. Remacle, and R. D. Levine, "The emergence of a coupled quantum dot array in a doped silicon nanowire gated by ultrahigh density top gate electrodes," *Journal of Physical Chemistry C,* 111, 17852-17860 (2007). (Ref. [1])

5.1 Introduction

Sufficiently small (<100 nm) particles exhibit charge quantization like natural atoms. Such "artificial atom"[2,3] finite fermion systems are often called ‘‘quantum dots’’ (QDs), referring to the quantum confinement in all three spatial dimensions. The charge transport properties of QD systems are characterized by single-electron charging and resonant tunneling through the quantized energy levels of the QDs.[2-5] As single-electron devices, QDs represent an ultimate limit.[6,7] They can also serve as building blocks to form complex superstructures with intriguing properties (cf. discussions in Chapter 4). Coupled QD systems,[8-11] in particular double QDs,[12,13] have also been investigated, often as platforms for the realization of solid state quantum bits.[14] For these

experiments, gate electrodes are utilized to both spatially confine and to control the coupling between the QDs.

Lithographically patterned (field-confined) QDs[2-5] are relatively large (>~100 nm) structures. While this implies weak quantization effects and therefore the need for ultra-low temperature measurements, such QDs are readily integrated into device platforms, and electrical contacts to the QDs are intrinsically established. By contrast, chemically synthesized (spatially confined) QDs,[15,16] while challenging to incorporate into device platforms, are significantly smaller, and so are characterized by much larger energy level spacings and can be interrogated at higher temperatures. In Chapter 4, we have demonstrated a method to align chemically synthesized QDs into one-dimensional and quasi-one-dimensional arrays that can be relatively easily incorporated into device platforms.[17]

A compromise between these two classes of devices are QDs defined within single-wall carbon nanotubes[18] and semiconductor nanowires (NWs).[19,20] Here, the size of the QD is defined by tunnel barriers at the source and drain contacts to a nanowire-based field-effect transistor. Smaller QDs have been achieved by utilizing intrinsic[21,22] or induced[23] defects in nanotubes, or barrier heterostructures intentionally introduced during the axial growth of the NWs.[24,25] Recently, coupled double QD systems defined by local gates have been reported in InAs NWs[26] and carbon nanotubes.[27] However, these systems have involved relatively large gate electrodes and electrode spacings (>100 nm).[26-28] Narrower and more closely spaced gates, in combination with true size-confined NWs, would help enhance quantization effects of the system, as well as the coupling strength between QDs.

Silicon [in particular, silicon on insulator (SOI)] is, in principle, an attractive material for QD experiments due to its highly developed fabrication technology and the potential integration of QD devices with conventional electronics circuits.[7,29] Previous approaches towards building QD systems on SOI substrates have mainly focused on obtaining NWs from lithography followed by etching procedures to reduce the NW width.[30-35] Single-electron effects have been observed in devices fabricated using this method, but the results disagree with the designed device geometry. The etching processes introduce defects and surface roughness that lead to the random formation of QDs within the nanostructure and irreproducible transport characteristics. For example, Coulomb blockade diamonds in conductance maps, which are considered a signature of single-electron charging, are typically not obtainable because the change of signal in consecutive scans can be much larger than the gate influence.[35] Electrostatically defined systems have resulted in highly controllable and reproducible coupled double QDs along NWs,[28] but the lithography step employed to pattern the gate electrodes limits the spacing between the gates (and hence the length of each QD) to be relatively large (~100 nm). This leads to very small charging energy scales (on the order of 1 meV) and correspondingly low coupling strengths for the QDs.[28]

We report[1] here on the investigations of Si NW-based coupled QD systems. We utilized the superlattice nanowire pattern transfer (SNAP) method[36,37] to produce high-quality Si NWs as a template for investigating coupled QDs. We also utilized SNAP to pattern an array of high density metal nanowire top gate electrodes (nanowire gate array; NWGA). This novel combination of geometric confinement from the width of the underlying Si NW and the electric field confinement from the ultrahigh-density NWGA

has for the first time allowed for the controlled formation of a concatenated 1D array of small (17 nm) quantum dots coupled in series along the length of the underlying Si NW. As a result, reproducible Coulomb blockade is observed with much larger energy scales (on the order of 10 meV), and full characterization of devices are achieved at readily attainable liquid helium temperatures (~4 K). The regularity of the Coulomb blockade diamonds in differential conductance maps is shown to be closely related to the regularity of the NWGA. The gate capacitance of each QD, as calculated from the Coulomb blockade diamonds, is in agreement with those calculated from the geometry of each QD as defined by top gate electrodes. The QD size effect is examined by varying the width of the underlying Si NWs. In addition, grouping of Coulomb blockade diamonds resulting from the coupling of QDs was observed in a device with three evenly spaced top gate electrodes. These results demonstrate that coupled QDs in series can be defined along the underlying Si NW by an array of ultrahigh-density SNAP top gate electrodes.

5.2 Fabrication of Si nanowire-based coupled quantum dot devices

The fabrication process flow is shown in Fig. 5-1. The starting structures were single-crystal Si NWs defined by patterning a 30 nm thick silicon-on-insulator (SOI) substrate with a 250 nm thick buried oxide (<100> orientation; Simgui, Shanghai, China). The SOI substrate was doped with boron by thermal diffusion of a spin-on dopant (Boron A, Filmtronics, Butler, PA) to a level of $\sim 5\times10^{18}$ cm^{-3},[38] as determined by four-point resistivity measurements. This process generates a gradient of dopant atoms through the thickness of the SOI wafer, effectively limiting the conducting part of the Si layer to the top 10 nm of its 30 nm thickness.[39]

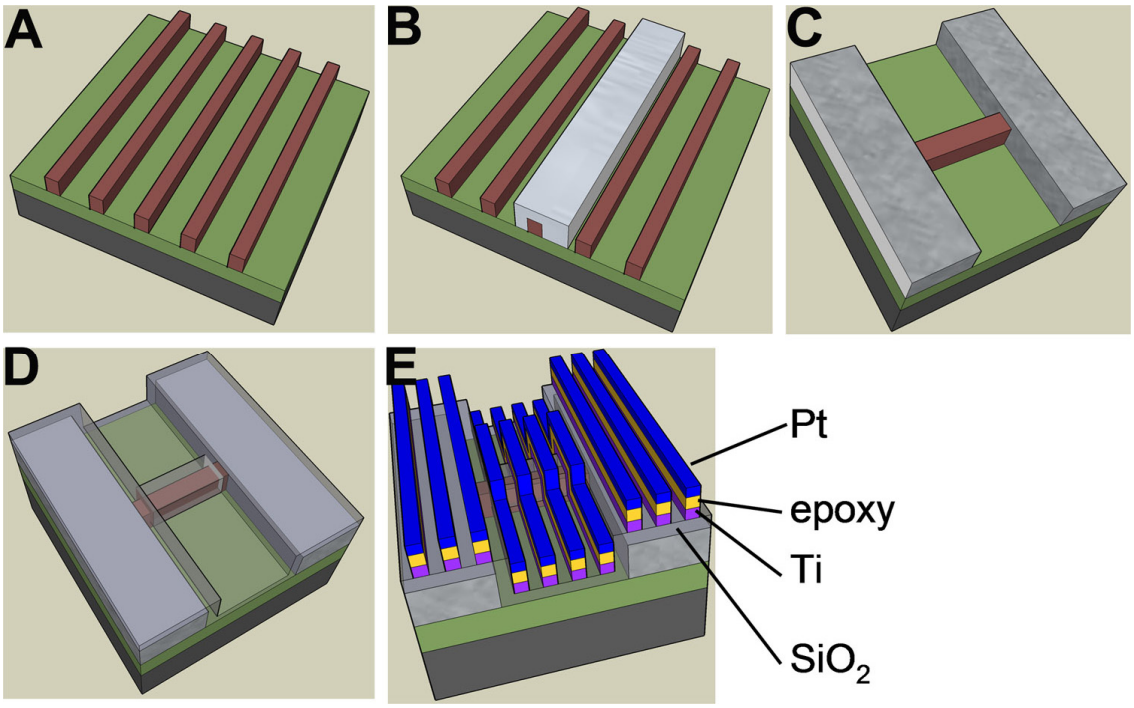

Figure 5-1. Process flow for the fabrication of a Si nanowire-based coupled quantum dot device. (A): An array of ~17 nm wide Si nanowires (NWs) with 50 nm spacing is prepared using SNAP. (B): An electron-beam-defined, ~50 nm wide aluminum mask is put down to protect one single Si NW. (C): The single Si NW is sectioned out and contacted with source/drain leads. (D): A SiO_2 layer is deposited on top as the dielectric layer. (E): An array of ultrahigh-density titanium NWs is fabricated on top of the dielectric layer in perpendicular to the single Si NW, serving as the nanowire gate array.

The wider Si NWs (40 nm wide, 30 nm thick) investigated in this study were patterned using electron-beam lithography (EBL), while the narrower nanowires (17 nm wide, 30 nm thick) were obtained by sectioning out a single NW from an array of SNAP Si NWs: an array of ~17 nm wide Si NWs with 50 nm spacing were patterned from the SOI using SNAP (Fig. 5-1A),[36,37] and an EBL-defined, ~50nm wide aluminum mask was put down to protect one single Si NW in the array (Fig. 5-1B). All other NWs were etched away with reactive ion etching (RIE).

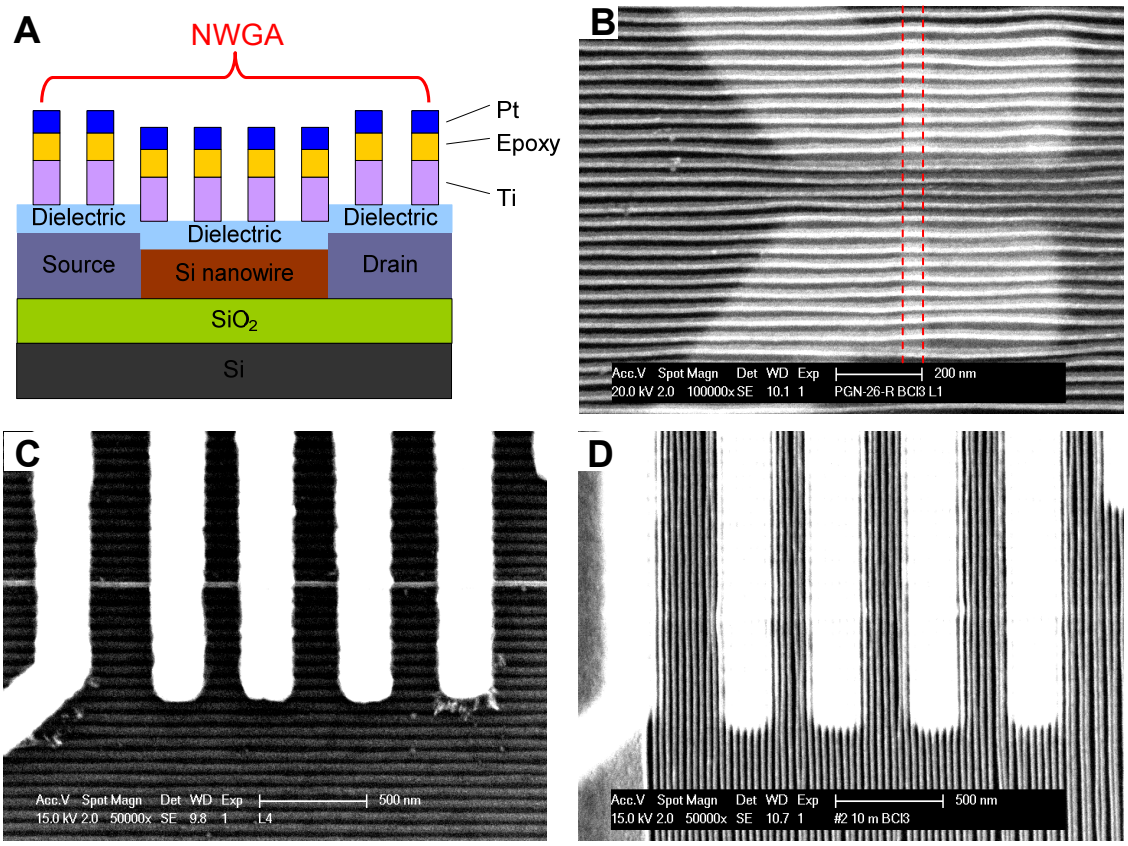

Figure 5-2. Si nanowire-based coupled quantum dot devices. (A): Schematic drawing of the side view of the device. The nanowire (NW) is contacted by source and drain electrodes, and gated by the nanowire gate array (NWGA) on the top. (B): Scanning electron micrograph of a device with an e-beam defined 40 nm-wide underlying Si NW and three top gate NWs. The contour of the underlying Si NW is highlighted with red dashed lines. Scale bar: 200 nm. (C): Five Ti/Pt contacts made to one single Si NW sectioned out from an array of ~17 nm wide Si NWs, corresponding to the structure drawn in Fig. 5-1C. Scale bar: 500 nm. (D): The same structure after dielectric layer and NWGA are fabricated on top, resulting in four full devices each corresponding to the structure drawn in (A) and Fig. 5-1E, with different source/drain distances and hence different numbers of top gate NWs.

Metallic contacts (Ti/Pt, 20nm/30nm) were established to the Si NWs by EBL (Fig. 5-1C) to generate source-drain channels that varied in length from 100 to 300 nm. The device was annealed in forming gas (5% H_2 in N_2) at 475 °C for 5 min to promote low-barrier source/drain contacts.[38] A dielectric layer (silicon oxide, 15 nm) was then deposited on top of the device (Fig. 5-1D), followed by a 35 nm titanium layer. An array of ultrahigh-density platinum SNAP NWs[36] with ~17 nm width and 33 nm pitch was glued down on top of the titanium layer, perpendicular to the underlying single Si NW. RIE was used to transfer the platinum pattern into the titanium layer, which serves as the NWGA to define QDs along the underlying Si NW (Fig. 5-1D and Fig. 5-2A). Note that the titanium NWs over the source and drain leads are not expected to affect the transport properties of the device: metallic contacts do not respond to a gate voltage.

The number of SNAP top gate electrodes across the underlying Si NW (and hence the number of QDs in series) is varied from device to device (3 to ~10) and controlled by the source-drain length, as SNAP wires of the same pitch (33 nm) are always used to define the top gate electrodes. All gate electrodes were shorted together: independent control of the different gate electrodes, which would constitute a non-trivial fabrication procedure,[39] is not attempted for the study reported here. Representative micrographs of the devices are given in Fig. 5-2.

5.3 Electrical measurement results

Electrical measurements were first carried out on devices with e-beam defined ~40 nm wide underlying Si NWs. Fig 5-3a shows such a device with about four top gate electrodes across the underlying Si NW, with modest disorder of the NWGA in the Si

NW region. Even for devices in which the NWGA exhibited significant disorder, reproducible Coulomb blockade diamond diagrams were readily measured. Such reproducibility is demonstrated in the $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plots of Fig 5-3b and c, which were obtained by scanning the gate voltage from low to high and from high to low, respectively. The comparable sizes of the diamonds suggest the formation of QDs of comparable sizes along the NW, while irregularities of the diamonds are attributed to the inevitable small variation of the sizes of the QDs due to the irregularity of the NWGA.

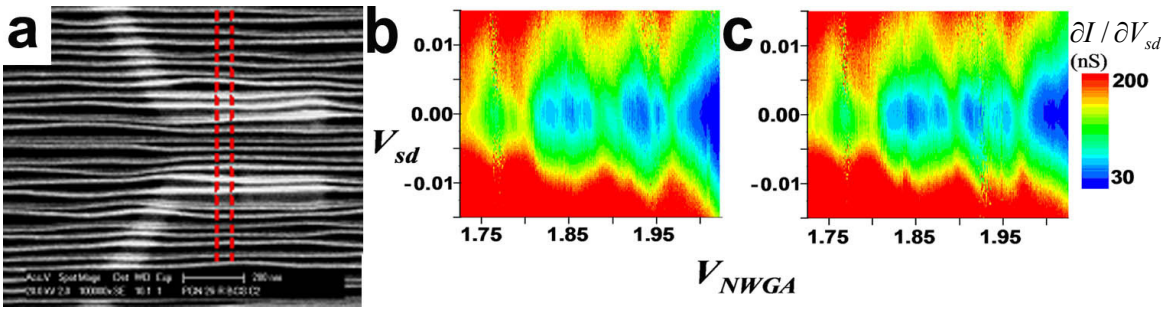

Figure 5-3. Electrical measurement results on a device with an e-beam defined ~40 nm wide underlying Si nanowire. (a): Scanning electron micrograph of the device. The contour of the underlying Si nanowire is highlighted with red dashed lines. Scale bar: 200 nm. (b): Coulomb blockade map ($\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot) of the device recorded at 4.3 K, obtained when scanning the gate voltage from low to high. (c) The same plot obtained when scanning the gate voltage from high to low.

Another 40nm-wide device with relatively ordered NWGA is reported in Fig. 5-4AB. Diamonds of similar energy scales were again observed. For comparison, we also performed measurements on a 40nm-wide device with a significantly disordered NWGA, as shown in Fig. 5-4CD. Reproducible Coulomb blockade was still observed, with diamond-like features in the $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot. In contrast to the results of Fig.

5-3 and Fig 5-4B, however, the sizes of the diamonds in this disordered device varied significantly, and diamond structures exhibited significant overlap with one another. These results were suggestive that QDs of varying sizes had been defined in series along the silicon NW, in agreement with the observed structure of that specific device.

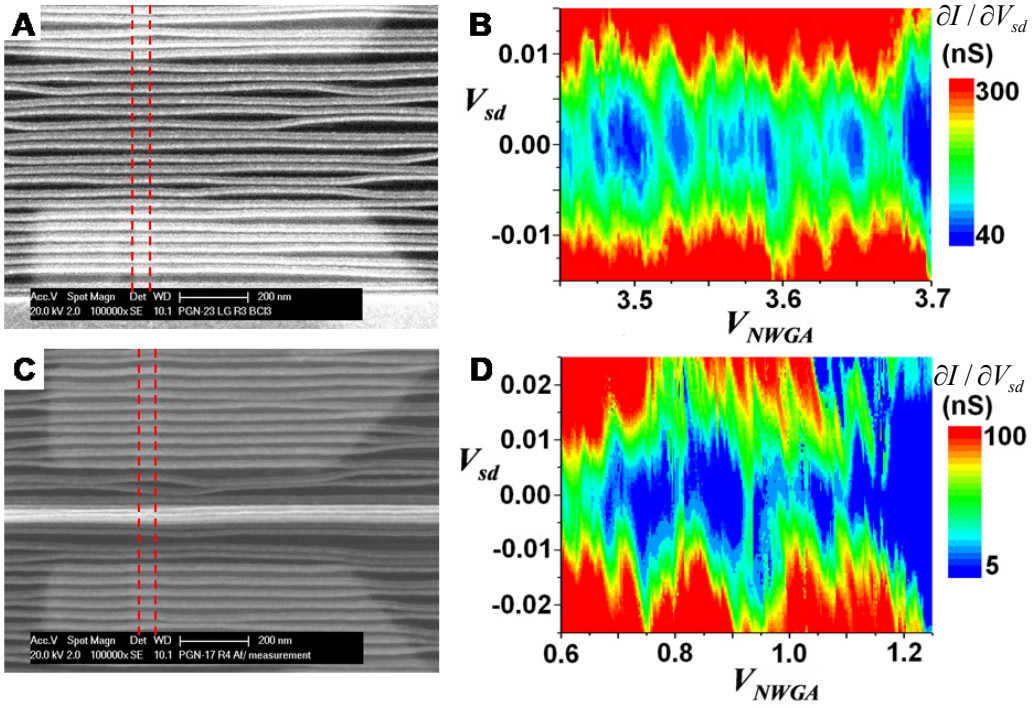

Figure 5-4. Comparison of data obtained on devices with different degrees of irregularity of top gate electrodes. (A): Scanning electron micrograph of a device with an e-beam defined ~40 nm wide underlying Si nanowire (NW) and very little irregularity of top gate electrodes, especially for the underlying Si NW region. The contour of the underlying Si NW is highlighted with red dashed lines. Scale bar: 200 nm. (B): $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot of the device recorded at 4.5 K. (C): Scanning electron micrograph of a device with an e-beam defined ~40 nm wide underlying Si NW and highly irregular top gate electrodes. The contour of the underlying Si NW is highlighted with red dashed lines. Scale bar: 200 nm. (D): $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot of the device recorded at 4.5 K.

The properties of the QDs in these 40nm-wide devices can be obtained from the Coulomb blockade diamond diagrams as shown in Fig. 5-3, Fig. 5-4, and Fig. 5-6.[4,5,20] The addition energy E_{add} can be directly measured from the maximum in V_{sd} for the conductance gap of the diamonds, ΔV_{sd} ~10 mV. This 10 meV addition energy is reflected in the gate voltage domain by the distance between consecutive diamonds, or the width of each diamond in V_g, which is estimated to be ΔV_g ~30 mV. The gate coupling factor can therefore be calculated as: $\alpha = \Delta V_{sd}/\Delta V_g = C_g/C = 0.33$, where C_g and C are the gate capacitance and total capacitance of each QD, respectively. This α value is close to those reported for systems with similar dimensions.[20]

The gate capacitance C_g of each dot can be calculated from ΔV_g assuming charging energy $U = e^2/C$ is the dominant component of E_{add} compared to the other component ΔE, the single-particle energy difference between consecutive quantized energy levels of the QD. This assumption should be valid for the dimension discussed here, and leads to:[20] $C_g = \alpha C = \alpha \frac{e^2}{U} \sim \alpha \frac{e^2}{E_{add}} = \alpha \frac{e}{\Delta V_{sd}} = \frac{e}{\Delta V_g} = 5.3$ aF. This value is in good agreement with the gate capacitance calculated from the geometry of each QD as defined by top gate electrodes, C_g' = 4.7 aF, indicating that the QDs in this system are really defined by the NWGA.

QD size effects were examined by comparing the above data with the results obtained from devices with narrower underlying Si NWs. Fig. 5-5A shows the Coulomb blockade diagram of one of the devices shown in Fig. 5-2D, with a ~17 nm wide underlying Si NW, and Fig. 5-5B shows the data on another device with a ~20 nm wide underlying Si NW. Diamonds of similar sizes were obtained with a certain amount of

overlapping structure for both devices, in agreement with the observed modest disorder of the NWGA (Fig. 5-2D). Note the change of the (V_{sd}) energy scale for these plots as compared with those of Fig. 5-3 and Fig. 5-4. The addition energy E_{add} directly measured from the maximum in V_{sd} for the conductance gap of the diamonds (Fig. 5-5A) is 30~40 mV for the device with ~17 nm wide underlying Si NW, more than double the value obtained on devices with ~40 nm wide underlying Si NWs (10~15mV). This is consistent with the formation of smaller QDs along the SNAP Si NWs. The addition energy for the device with a ~20 nm wide underlying Si NW is estimated from Fig. 5-5B to be 25~30 mV, a little smaller than the ~17 nm device, and about twice that of the ~40 nm devices, again in agreement with the size of each individual QD defined by the device geometry.

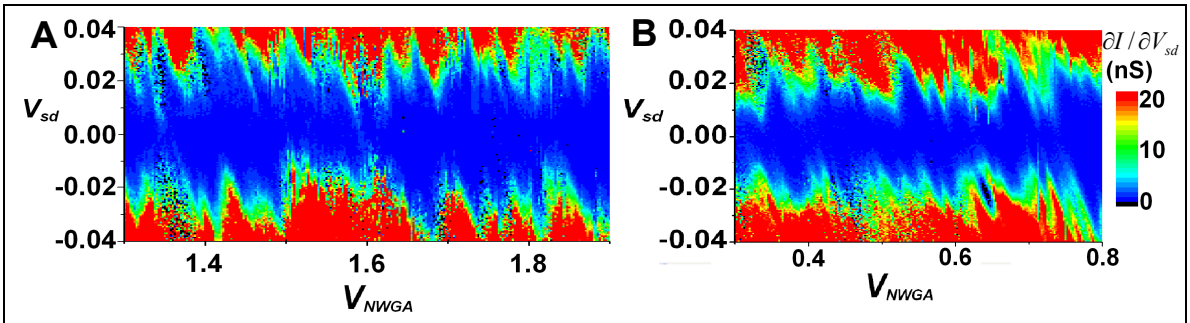

Figure 5-5. Coulomb blockade maps ($\partial I/\partial V_{sd}$ - V_{NWGA} - V_{sd} plots) of two devices with SNAP-defined underlying Si NWs, measured at 4.5 K. (A): Measured from a device with a ~17 nm wide underlying Si NW (Fig. 5-2D); (B): Measured from a device with a ~20 nm wide underlying Si NW.

Grouping of Coulomb blockade diamonds resulting from the coupling of QDs was observed in a device with three evenly spaced top gate electrodes (Fig. 5-6). A micrograph of the device is presented in Fig. 5-2B. Very little disorder of the NWGA is observed in the Si NW region of this device, and this allows for the formation of three

QDs of nearly identical sizes that electronically couple with each other. In the $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot, Coulomb blockade diamonds of similar sizes appear to be arranged into groups of three, as marked out by dotted frames in Fig. 5-6. The observed structures are reminiscent of previous studies on lithographically patterned coupled QD systems, in which three coupled QDs gave rise to conductance peaks that were arranged into groups of three.[9] However, we were able to observe such effects in Si at much higher temperatures (4.3 K vs. 15 mK).

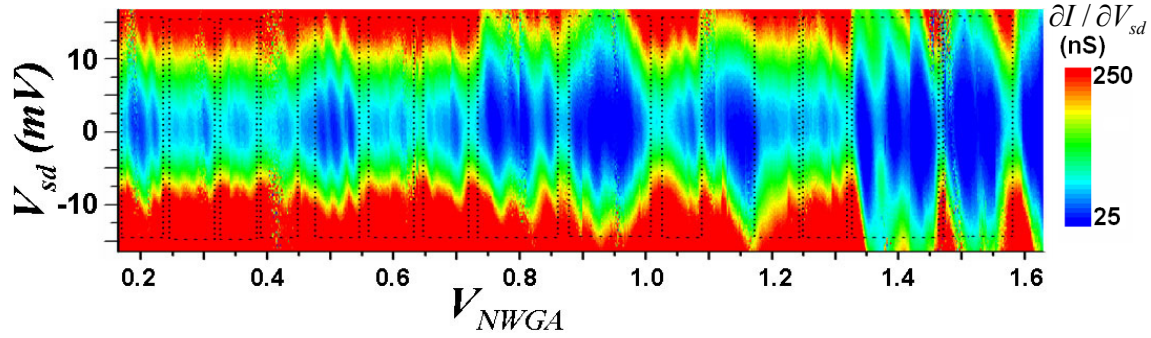

Figure 5-6. Coulomb blockade map ($\partial I/\partial V_{sd}$ - V_{NWGA} - V_{sd} plot) of a device with 40 nm wide underlying Si NW and three highly-ordered top gate NWs (Fig. 5-2B), recorded at 4.3 K. Coulomb blockade diamonds of similar sizes appear to arrange into groups of three, as marked out by dotted frames.

5.4 Conclusions

In this chapter, we have reported[1] the electrical characteristics of Si nanowires gated by arrays of very closely spaced nanowire gate electrodes. This novel combination of geometric confinement from the width of the underlying Si nanowire and the electric field confinement from the ultrahigh-density top gates has allowed for the controlled

formation of a concatenated 1D array of small quantum dots coupled in series along the length of the Si nanowire. Experiments were reported for two widths of Si nanowires: 40 nm and 17 nm, and for a varying number of gate electrodes, all spaced at a pitch of 33 nm. Reproducible confinement and inter-dot coupling effects are observed with large energy scales (~10 meV), and clear Coulomb blockade diamond features were obtained at liquid helium temperatures when the conductance is plotted in the plane of the source-drain and gate voltages. The regularity of the Coulomb blockade diamonds in differential conductance maps is shown to be closely related to the regularity of the top gate electrodes. The gate capacitance of each QD, as calculated from the diamond diagrams, is in agreement with those calculated from the geometry of each QD defined by top gate electrodes. In addition, grouping of Coulomb blockade diamonds resulting from the coupling of QDs was observed in a device with three evenly spaced top gate electrodes. These results demonstrate that coupled QDs in series can be defined along the underlying Si nanowire by an array of ultrahigh-density top gate electrodes.

5.5 References

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