MILLIMETER-WAVE PHASED ARRAYS IN SILICON

Thesis by

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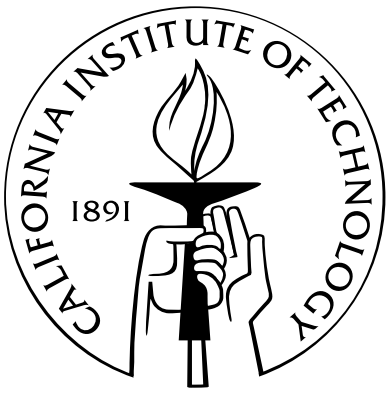

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To Amma, Appa, and Karen

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Abstract

Integration of mm-wave multiple-antenna systems on silicon-based processes enables complex, low-cost systems for high-frequency communication and sensing applications. While individual silicon devices struggle to achieve the same performance as III-V semiconductor-based transistors at mm-wave frequencies, the benefits of integration, such as good component matching and near-zero incremental device cost, can be leveraged to achieve good system performance. This dissertation presents different techniques and architectures for integrating mm-wave phased arrays on commercial silicon process technologies by demonstrating phased-array transmitters and receivers at 24GHz, 60GHz, and 77GHz, in CMOS and SiGe BiCMOS processes.

Initially, the tradeoffs of high-frequency systems are discussed in the context of Shannon capacity and the benefits of integrating phased arrays at such high frequencies are discussed in detail. An analysis of the output noise in a phased-array receiver in the presence of antenna coupling and input noise correlation is carried out and measurements on a discrete two-element array demonstrate the dependence of output noise on the phase-shift setting.

The design of the first fully-integrated 24GHz phased-array transmitter using mainly 0.18μm CMOS transistors is described. The four-element array adopts a centralized LO-path phase-shifting approach using a multi-phase VCO. The on-chip 19.2GHz VCO generates 16 equally spaced LO phases leading to 7° beam resolution for radiation normal to the array. The transmitter includes four on-chip CMOS power amplifiers, with outputs matched to 50Ω, that are each capable of generating up to 14.5dBm of output power at 24GHz. The array achieves a peak-to-null ratio of 23dB

with four elements active and can support data rates of 500Mb/s on each channel (with BPSK modulation) while occupying 6.8mm x 2.1mm of die area.

A high-resolution *local* LO-path phase-shifting architecture is presented as part of the first fully-integrated 77GHz phased-array transceiver in a SiGe BiCMOS process. The SiGe transceiver includes four transmit and four receive elements (including 77GHz LNA and PA), along with the LO frequency generation and distribution circuitry. The local LO-path phase-shifting scheme enables a robust distribution network that scales well with increasing frequency and/or number of elements, while providing high-resolution phase shifts. Each transmit element of the heterodyne transmitter generates +12.5dBm of output power at 77GHz, with a bandwidth of 2.5GHz leading to a four-element EIRP of 24.5dBm. Each on-chip PA has a maximum saturated power of +17.5dBm at 77GHz while the on-chip VCO achieves a phase noise of -95dBc/Hz@1MHz offset at 54GHz. The phased-array performance is measured using an internal test option and achieves 12dB peak-to-null ratio with two transmit and receive elements active.

While the 24GHz and 77GHz array are multiple-input single-output systems, higher-order phase-shifting and combining techniques can be used to achieve arrays with multiple outputs, with beams focused on different directions concurrently. Toward this end, a 60GHz bidirectional RF-combined phased array front-end is implemented in SiGe BiCMOS, using a hybrid parallel/series phase-shift approach that reduces the requirements of the on-chip phase shifters, enabling RF signal combining. The four-element array enables simultaneous illumination of two angles of incidence and includes amplitude control, as well as continuous phase adjustment. The front-end has a noise figure lower than 6.9dB at 60GHz and the array achieves full spatial coverage with peak-to-null ratio higher than 25dB. The four-element front-end consumes 265mW and occupies $4.6mm^2$ of die area.

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Chapter 1

Introduction

"The adventures first," said the Gryphon in an impatient tone, "explanations take such a dreadful time."

Alice's Adventures in Wonderland, Lewis Carroll

The last decade has seen strong growth in the wireless communication market as mobile data and voice services become ubiquitous. This expansion has been fueled by the integration of wireless ICs on silicon processes that achieve very low costs for large volumes. Wireless communication ICs accounted for $40 billion in revenue in 2006 and are expected to grow faster than other IC segments over the next few years. Silicon device scaling has provided sufficient high-frequency performance to enable integration of RF ICs on silicon with RFCMOS and Silicon BJT devices now achieving near total market share for mobile wireless transceivers operating below 6GHz, with other technologies being used only for the power amplifiers [1]. This dominance is expected to continue in the future as wireless LAN and GSM chips combining the RF front-end with the digital baseband establish their presence in the marketplace.

However, the demand for ever-increasing data rates for data-intensive applications like video transmission and wireless backhaul links has led to interest in higher frequencies that offer larger available bandwidths. As can been seen in Figure 1.1, the available bandwidth increases steadily with frequency, with the 57-64GHz ISM

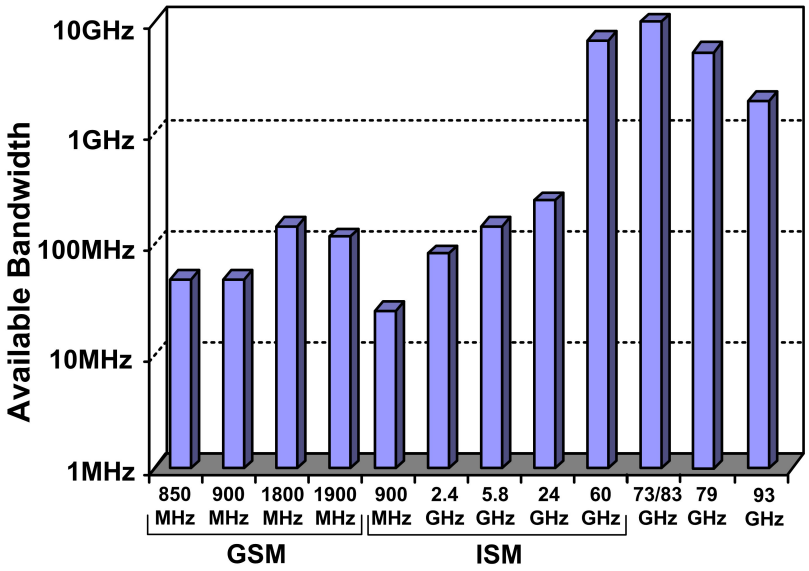


Figure 1.1: Large bandwidths available at mm-wave frequencies for high data rate communication and high-resolution sensing applications.

band and 71-76GHz/81-86GHz point-to-point communication bands offering multi-gigahertz available spectrum [2, 3]. The large available bandwidths also enable high-resolution sensing applications like automotive collision-avoidance radar at 77GHz [3].

The attractiveness of high frequencies from an application perspective is tempered by the high costs associated with the III-V semiconductor device technologies that are currently used in mm-wave systems (Figure 1.2 - from [4]). Integration of mm-wave systems on silicon would enable these applications to replicate the success of the voice and data communication systems, such as cellular telephony, Bluetooth and wireless LAN (WiFi), that operate in the 900MHz - 6GHz range.

While individual silicon devices struggle to achieve the same output power, linearity and low-noise performance as GaAs or InP transistors at mm-wave frequencies, silicon integration provides unique advantages on the system level, notably in terms of near-zero incremental device cost, high yield, good device matching and easy integration of digital calibration and control circuitry. Therefore, an attempt to achieve mm-wave silicon systems must leverage the powers of

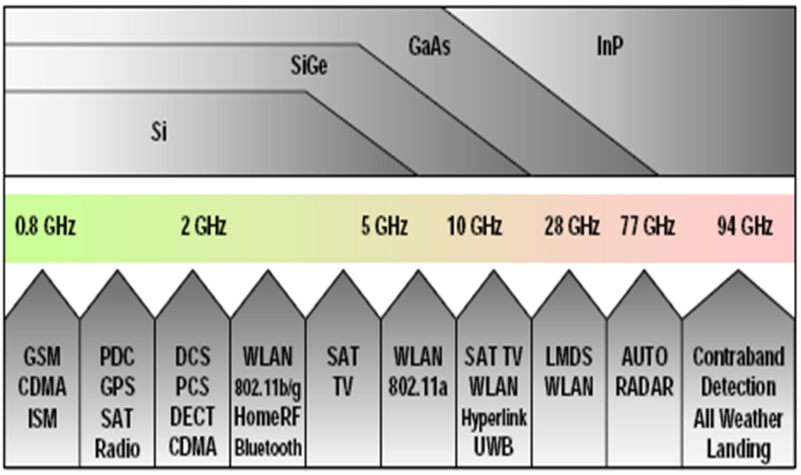


Figure 1.2: Process technologies for high frequency applications

integration, using system and circuit innovations to achieve desired performance.

Phased arrays, a class of multiple antenna systems, represent one potential means of using parallel signal conditioning elements to achieve improved system performance. The smaller wavelengths at high frequencies result in a reduction in the physical size of multiple antenna systems due to the smaller antenna size and spacing. The beamforming and beam steering properties of phased arrays, coupled with the improvements in signal-to-noise ratio (SNR) provided by such systems, make them ideal for mm-wave sensors and reconfigurable point-to-point communication links.

This dissertation explores methods to integrate mm-wave phased-arrays on commercial silicon-based process technologies. Architectural and circuit level innovations are presented in the context of transmit and receive array implementations at 24GHz, 77GHz and 60GHz.

1.1 Organization

A brief overview of the operating principles and advantages of phased-arrays is provided in Chapter 2. This is followed by a detailed discussion of the expected output noise in a phased-array receiver (Section 2.5). Various sources of correlation of noise in different elements are explored, leading to expressions for output noise in the array as a function of phase-shift setting. The dependence of the output noise power on the element phase shift indicates that the improvement in SNR in an array is angle-dependent.

Chapter 3 discusses the motivation behind implementing high-frequency integrated systems on silicon. Section 3.1 provides a Shannon capacity based analysis to demonstrate the advantages of high-frequency communication systems. The benefits of silicon integration are then discussed in Section 3.2, followed by a study of the various integrated phase-shifting architectures and their relative merits and demerits (Section 3.3). Phase-shift based array architectures are inherently narrowband in nature and the error introduced due to this approximation is quantized in Section 3.4. A simple OFDM-based equalization scheme that overcomes the deleterious effects of the narrowband phase-shift approximation is also presented.

The next three chapters are dedicated to phased-array implementations that demonstrate the feasibility of fully-integrated mm-wave transceiver arrays on silicon. As the first step towards integrating such systems on low-cost CMOS process technologies, Chapter 4 describes a four-element phased-array transmitter implemented using mainly 0.18μm CMOS transistors. Section 4.2 discusses the multiphase VCO based LO-path phase-shifting architecture adopted in the transmitter, while the design of key circuit blocks and measurement results are detailed in Sections 4.3 and 4.4.

Continuing toward higher levels of integration and higher frequencies of operation, Chapter 5 presents a fully-integrated four-element 77GHz phased-array transceiver that has been implemented in a commercial SiGe BiCMOS process. The high-resolution local LO-path phase-shifting architecture adopted in the system is presented in Section 5.2, followed by the detailed description of the circuits in the transmit and LO paths (Section 5.3). Chip measurements, discussed in Section 5.4, indicated 12.5dBm output power in each transmit element at 77GHz and good array performance.

While the phased arrays in Chapter 4 and Chapter 5 are multiple-input single-output systems, it is possible to implement more complex phase-shifting and combining schemes in order to achieve multiple-input multiple-output systems that receive signals from more than one direction. In Chapter 6, a bidirectional RF-combined phased-array architecture is presented that can receive signals from two different directions concurrently. Following a detailed analysis of the hybrid series-parallel architecture in Section 6.1, the design of a bidirectional 60GHz phased-array front-end is described in Section 6.2. The front-end was implemented in a commercial SiGe BiCMOS process and the measurement results are discussed in Section 6.3. Extensions of the hybrid array architecture to a higher number of outputs and true-time delay-based arrays are discussed in Section 6.4.

Chapter 2

Phased-Array Systems

Phased arrays are a class of multiple antenna systems that provide beamforming and beam steering capabilities. In this chapter, the operating principles and applications of phased arrays are presented. An introduction to phased arrays is provided in Section 2.1 along with a mathematical description of their operation. The advantages offered by phased-array transmitters and receivers are presented in Section 2.3 and Section 2.4. In Section 2.5, a detailed analysis of the expected increase in noise power in a receive array is presented, leading to conclusions on expected SNR improvement in phased arrays in the presence of coupling between different elements.

2.1 Introduction to Phased Arrays

In the late 1930s, engineers were faced with the problem of generating narrow beams for communication and for emerging radar applications. The prevalent solution of increasing antenna size had run into mechanical limitations as the antenna beam width is inversely proportional to antenna diameter [5]. Furthermore, radar applications require the direction of the narrow beam to be changed quickly, which was challenging with physically large antennas that had to be mechanically rotated. Phased arrays presented a solution to this problem by creating a *virtual* high gain antenna in which phase-shifted signals from multiple low-gain antennas combined to create a narrow beam. Additionally, the direction of the beam could be

scanned by varying the phase shifts in each antenna element. One of the first implementations of such an active array for shortwave reception was presented in 1937 by Friis and Feldman [6] using mechanical phase shifters. In response to military needs during World War II, Luis Alvarez designed the first electronically steered array, *Eagle*, at the MIT Radiation Lab [7]. This system evolved into the AN/APQ-7 bomb-targeting radar used aboard the B-29 *Superfortresses* towards the end of the war. The potential of electronic beamforming and beam steering for military applications was soon recognized, leading to the development of phased arrays for mainly radar applications. After the war, phased-array technology was developed on both sides of the Iron Curtain with investigations into the most critical component of electronically steerable arrays – electronic phase shifters, resulting in significant improvements in array size and performance [8–13].

As expected, arrays have proved to be more advantageous than fixed antenna systems and have found various sensing and communication applications. Even as phased arrays are being used extensively in military radar [14–16], the relatively lower cost and smaller size of mmic-based phased arrays have led to their use in satellite links such as the Globalstar network, for satellite-based data and voice services. In this network, the antenna array aboard each satellite forms 16 independent transmit and receive beams that cover the region of the earth visible from the satellite [17]. Some other examples of phased-array based links include mobile TV reception systems for aircraft and automobiles [18, 19], airborne communication systems [20] and communication systems aboard the MESSENGER spacecraft on a mission to Mercury [21].

Arrays have also been widely used in radio astronomy, where the signals from several small antennas are combined to emulate an antenna with a large aperture. An example is the Very Large Array (VLA)(currently operational in New Mexico) that consists of 27 antennas, and has a a resolution of 0.04 arcseconds (at 43GHz) [22]. Building on the VLA, a Square Kilometer Array (SKA) has been

proposed and is an active area of research [23]. The proposed array includes as many as a few hundred elements working together to create a telescope with a $10^6 m^2$ aperture area, enabling sensitive astronomical measurements.

The miniaturization of phased arrays has also led to a number of potential sensing applications such as automotive collision-avoidance radar to improve road safety [24, 25] and for civil aircraft navigation. Recently, the use of microwave phased arrays has been proposed for medical purposes such as tumor detection, where the difference between the dielectric properties of cancerous and healthy tissue at microwave frequency is used to detect the presence of a tumor [26, 27]. Ultrasound imaging systems are also phased arrays, albeit those that operate on sound waves rather than EM waves.

The instances described in the preceding paragraph merely scratch the surface of existing and potential applications of phased arrays. However, the hitherto high cost of these systems, arising from the expensive semiconductor technologies and complex module-based assembly, has confined them to military, research and niche commercial applications [28]. Furthermore, the architecture of these systems is limited by the reliability of the modules, since increasing the number of active devices results in a decrease in yield. As discussed in the Introduction and in Chapter 3, integration of phased arrays on silicon-based processes enables the realization of complex architectures that are tailored for particular applications. The integration of the entire array on silicon coupled with the low cost of silicon processes promises a future in which multiple antenna systems find widespread use in mass commercial applications.

2.2 Phased Array: Principles of Operation

In the following, the governing equations of a phased-array receiver are derived. The defining equation for a transmit array can be developed using a similar

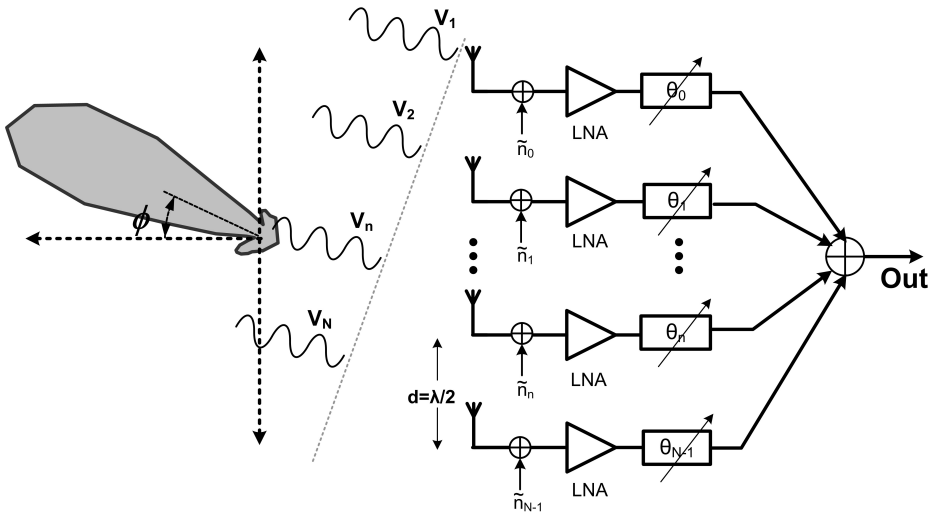


Figure 2.1: Principle of operation of phased-array receiver

procedure.

The operating principle of a phased array is illustrated in Figure 2.1. In a receiver array with N elements spaced a distance d apart, a signal with incidence angle, ϕ, arrives at the n^{th} element, after experiencing an excess delay, τ_n,

$$\tau_n = \frac{nd\sin\phi}{c} = n\tau \tag{2.1}$$

where $\tau = \frac{d\sin\phi}{c}$. The phase shifter in the n^{th} element adds a phase shift, $\theta_n = (N-n)\theta$, as a result of which the output signal of the n^{th} element before combining is,

$$V_n(t) = V(t-\tau_n)\, cos(\omega_{RF}(t-\tau_n) - \theta_n) \tag{2.2}$$

The output of the array after combining is,

$$\begin{aligned} V_{out}(t) &= \sum_{n=0}^{N-1} V(t-\tau_n)\cos(\omega_{RF}(t-\tau_n) - \theta_n) \\ &= \sum_{n=0}^{N-1} V(t-n\tau)\cos(\omega_{RF}t - n\psi - (N-n)\theta) \end{aligned} \tag{2.3}$$

where $\psi = \omega_{RF}\tau$ is the phase difference between the input signal at adjacent

elements at frequency, ω_{RF}. Assuming that the excess delay is much smaller than the time period of the highest modulation frequency or that the modulation is narrowband,

$$V(t) \approx V(t-\tau) \approx V(t-n\tau) = V_0(t) \tag{2.4}$$

Applying the approximation in (2.4) in (2.3),

$$\begin{aligned} V_{out}(t) &= V_0(t) \sum_{n=0}^{N-1} \cos\left(\omega_{RF} t - n\psi - (N-n)\theta\right) \\ &= Re\left(V_0(t)\, e^{j(\omega_{RF} t - N\theta)} \sum_{n=0}^{N-1} e^{-jn(\psi-\theta)} \right) \end{aligned} \tag{2.5}$$

From (2.5), it can be seen that,

$$|V_{out}(t)| = \left| \frac{\sin\frac{N(\psi-\theta)}{2}}{\sin\frac{(\psi-\theta)}{2}} V_0(t) \right| \tag{2.6}$$

Hence, signals from a particular direction add constructively in the array, while signals from other directions add destructively, leading to beam formation. For an incidence angle, ϕ, the maximum amplitude of $V_{out}(t)$ is achieved when,

$$\theta = \psi = \omega_{RF} \frac{d \sin\phi}{c} \tag{2.7}$$

A larger spacing between antennas ensures less coupling between different antenna elements and also makes physical realization of antennas easier. Figure 2.2 plots the array pattern for a two-element array for different choices of antenna separation, d. As can be seen from the figure, $d > \frac{\lambda}{2}$ leads to grating lobes in the pattern. Therefore, $d = \frac{\lambda}{2}$ is a good choice for antenna separation leading to,

$$\theta = \pi \sin\Phi \tag{2.8}$$

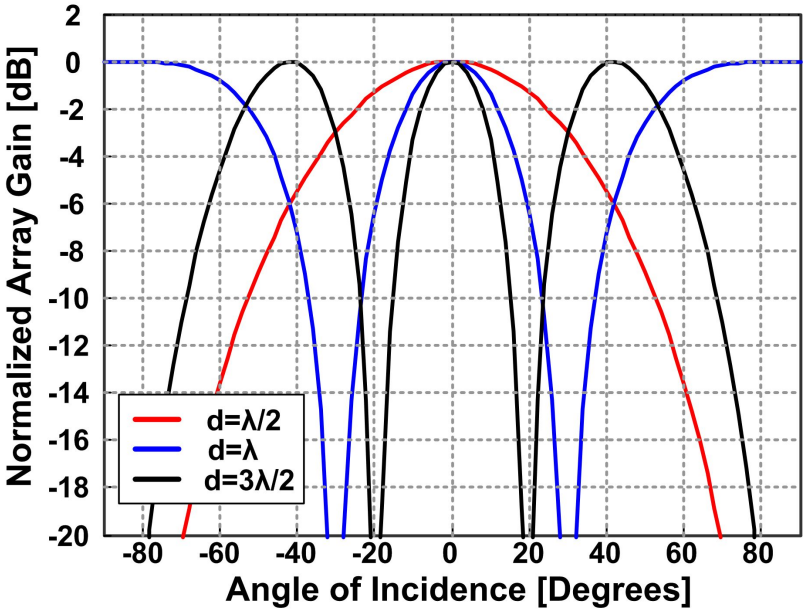


Figure 2.2: Two-element array pattern for different antenna spacing demonstrating grating lobes for $d > \frac{\lambda}{2}$.

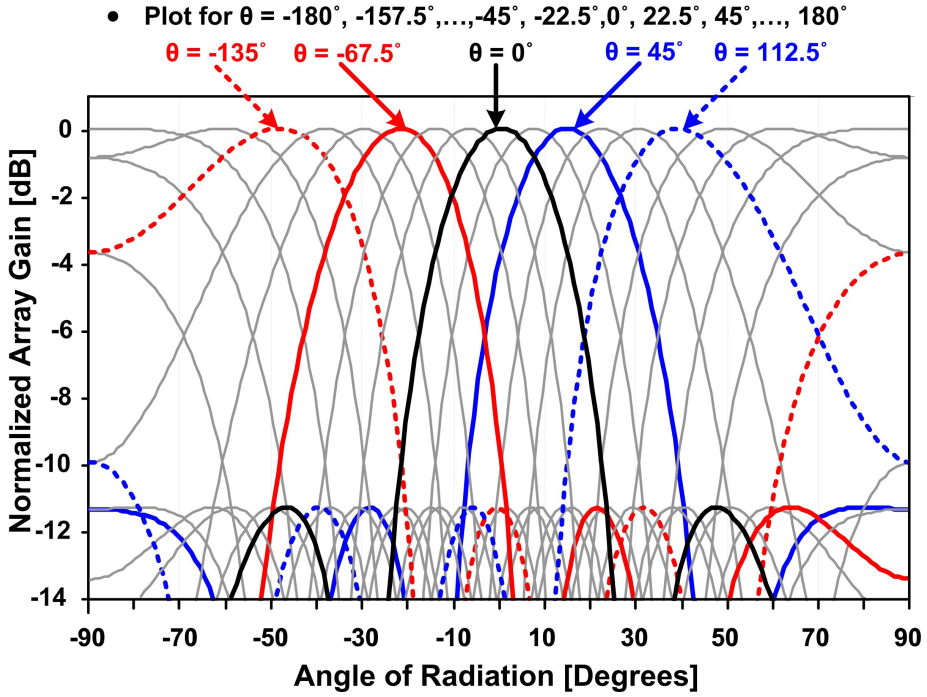


Figure 2.3: Four-element array pattern with uniformly spaced values of θ (Step size = 22.5°).

Figure 2.3 plots $|V_{out}(t)|$ as a function of the angle of incidence for a four-element array ($N = 4$) for uniformly-spaced values of θ (step size = 45°) and $d = \frac{\lambda}{2}$. From (2.6), it can be shown that the 3dB beamwidth in the ϕ plane (incidence plane) is a function of N and the desired angle of incidence, ϕ_0. For non-end fire angles of incidence, it can be approximated by,

$$\phi_{3dB} = \frac{0.866\lambda}{Nd\cos\phi_0} \tag{2.9}$$

Electronic beam steering can be accomplished by electronically varying the phase shift, θ_n in each element. It must be noted that in order to achieve complete scanning in the incidence plane (i.e $-\frac{\pi}{2} \leq \phi \leq \frac{\pi}{2}$), the phase shift in each element has to vary from 0 to 2π.

Thus, a phased array is equivalent to, and is often referred to as, an active antenna, which provides gain in a direction that can be electronically varied. In the following sections, the advantages of phased arrays with respect to transmitters and receivers are discussed in greater detail. The effects of the narrowband approximation in (2.4) are detailed in Chapter 3.

2.3 Phased-Array Transmitters

The beamforming properties of phased-array transmitters provide two significant advantages over isotropic transmitters. Firstly, for the same total transmit power, the power at the receiver is increased and secondly, the interference at receivers that are not targeted is reduced. A simple analogy can be made between a phased array and a flashlight. Isotropic transmitters, like incandescent bulbs, illuminate all directions equally, while phased arrays, like flashlights, focus their energy in particular directions leading to brighter illumination only in the selected direction.

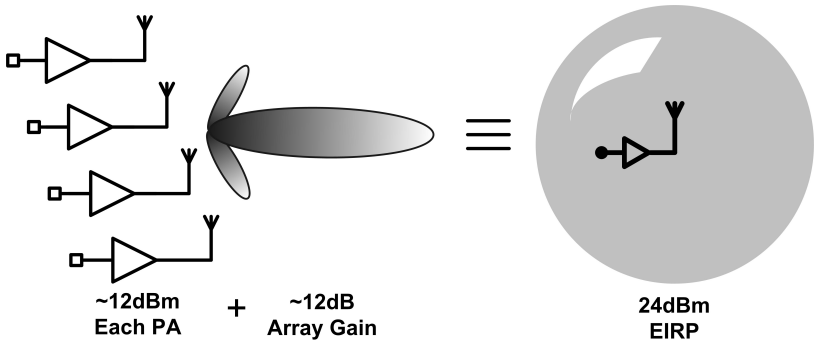


Figure 2.4: Improvement in the EIRP in a phased-array transmitter

2.3.1 Improvement in Effective Isotropic Radiated Power

For a transmitter, the effective isotropic radiated power (EIRP) is a metric of the fraction of the power generated by the transmitter that is available at the receiver. The EIRP of a transmitter in a particular direction is defined as the power an isotropic transmitter would have to radiate to generate the same electric field in that direction. For e.g, if a transmitter generates P Watts, and has an effective antenna gain, $G(\phi)$, the EIRP is given by,

$$EIRP = PG(\phi) \tag{2.10}$$

In an N-element transmitter, if each element radiates P Watts and has isotropic antennas ($G = 1$), from (2.6) the power radiated in the desired direction is N^2P Watts. Thus, an N-element array improves the EIRP in the desired direction by $20 \log N$ dB as compared to a single element thereby increasing signal power at the targeted receiver, as illustrated in Figure 2.4. The beamforming properties of the array also ensures that the transmitter power is attenuated in other directions. For example, in a four-element array, the peak sidelobe level is 11dB below the main beam, thereby ensuring low interference power at receivers that are not targeted.

2.4 Phased-Array Receivers

A phased-array receiver provides beam steering and beamforming properties similar to a phased-array transmitter leading to improved immunity to interferers and higher signal-to-noise ratio (SNR). In a receiver array, the noise sources in different receive elements are independent. Therefore, noise signals at the receiver output due to different elements are uncorrelated and add in power. However, as shown in (2.5), the desired signals combine at the output coherently in voltage. Assuming that there is no coupling between different elements and that the input noise at any element is uncorrelated with the input noise at other elements, the SNR at the output of an N-element array is given by,

$$SNR_{out} = \frac{N^2 V_0^2}{\sum_{i=1}^{N} \tilde{n}_i} = N \frac{V_0^2}{\tilde{n}_0} \tag{2.11}$$

where V_0 is the amplitude of the signal, and $\tilde{n}_i = \tilde{n}_0$ is the noise power at the output of i^{th} element. Hence, the output SNR of a phased-array receiver can be up to $10 \log N$ dB better than the output SNR of a single receive element.

Thus, a phased-array transmit and receive system improves SNR by increasing the transmit power available at the receiver, and also by improving receiver output SNR. In the following section, the noise figure improvement in a receiver array is studied in the presence of coupling and conclusions are presented on expected SNR improvement.

2.5 Output Noise in Phased-Array Receiver

The noise factor of a receiver, F, is a measure of the noise that is added by the receiver during the process of signal conditioning and is calculated as the ratio of the SNR at the input, SNR_{input} to the SNR at the output, SNR_{output} [29].

$$F = \frac{\text{SNR}_{input}}{\text{SNR}_{output}} \tag{2.12}$$

Defining the noise from the input termination to be $\tilde{n}_s$, the total output noise to be $\tilde{n}_{out}$ and the receiver available power gain to be G_a, F can also be calculated as,

$$F = \frac{\frac{S_{in}}{Noise_{in}}}{\frac{S_{out}}{Noise_{out}}} = \frac{\tilde{n}_{out}}{G_a \tilde{n}_s} = 1 + \frac{\tilde{n}_{rec,out}}{G_a \tilde{n}_s} \tag{2.13}$$

where $\tilde{n}_{rec,out}$ is the noise due to the receiver at the output. Since F is defined for a particular $\tilde{n}_s$, the definition is standardized by defining $\tilde{n}_s$ to be the noise available from the input termination at temperature 290K.

From (2.13), the noise factor directly measures the signal-to-noise degradation due to a receiver. The noise figure, NF, is the noise factor, F, expressed in dB, i.e,

$$NF = 10log_{10}F \tag{2.14}$$

The ratio between the noise at the output due to the receiver and the noise from the input source can also be expressed in terms of noise temperatures. The equivalent input noise temperature of a receiver, T_{rec}, is defined as the temperature at which an input termination connected to an equivalent noiseless receiver produces the same noise power at the output as the actual receiver when connected to a noiseless input termination. From the definition in (2.13), it follows that,

$$F = 1 + \frac{T_{rec}}{T_0} \tag{2.15}$$

where T_0 is the noise temperature of the input source. Again, the definition is standardized by defining $T_0 = 290K$.

Thus, using the definition of noise factor provided in (2.13) and from the *SNR* ratio calculated in (2.5), it can be seen that the NF of an N-element phased-array receiver can be up to $10 \log N$ dB lower than that of a single receive element. However, such an improvement is predicated on two assumptions:

1. there is no coupling between different elements before signal combining

2. the noise from the surroundings at the input of any element is uncorrelated with the input noise at other elements in the array

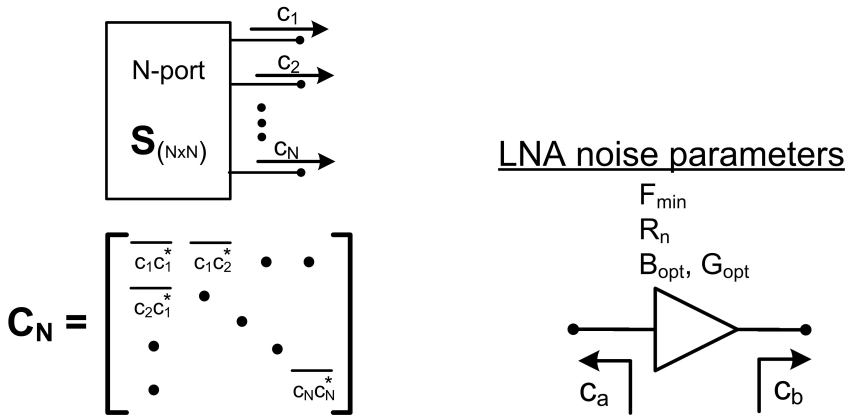
When there is correlation between the noise at the output of each element, the noise from different elements do not add in power leading to an improvement in the signal-to-noise ratio that is different from the expected $10logN$ dB. In this section, expressions are derived to estimate the output noise in a phased-array receiver in the presence of coupling and input noise correlation.

2.5.1 Low-Noise Amplifier(LNA) Noise Parameters

In a typical receiver, the LNA is the first element following the antenna and is designed such that the noise parameters of the LNA dominate the noise behavior of the receiver. For a two-port system such as the LNA, the noise parameters are often characterized using four parameters - the minimum achievable noise figure, F_{min}, the optimum source admittance, G_{opt} and susceptance, B_{opt}, that result in F_{min}, and the noise resistance of the two-port, R_n. Given these parameters, the noise figure for an arbitrary source termination, Γ_s, is given by [30],

$$F = F_{min} + \frac{4R_n}{Z_0} \frac{|\Gamma_s - \Gamma_{opt}|^2}{\left(1 - |\Gamma_s|^2\right) |1 + \Gamma_{opt}|^2} \tag{2.16}$$

The noise parameters of an N-port can also be expressed in terms of outgoing noise waves at each port that deliver noise power from the N-port to the terminations [31, 32]. In this case, the noise generated in the N-port is modeled by the correlation between the noise waves at each port. Thus, the N-port is characterized in the frequency domain by the s-parameter matrix and the noise correlation matrix [Figure 2.5(a)]. In the case of the LNA shown in Figure 2.5(b), the noise due to the amplifier is represented by two correlated noise waves at the input and the output, c_a and c_b. The amplitude and the correlation between these waves can be determined from the s-parameters, actual noise temperature, T, and



(a) Noise wave representation of n-port

(b) Input and output noise waves in LNA

Figure 2.5: Noise modeling of n-ports using noise waves

minimum noise temperature of the LNA, T_{min}, as derived in [32, 33].

$$k_t = \frac{4kTR_n}{Z_0} \tag{2.17}$$

$$|c_a|^2 = kT_{min}\left(|s_{11}|^2 - 1\right) + \frac{k_t|1 - s_{11}\Gamma_{opt}|^2}{|1 + \Gamma_{opt}|^2} \tag{2.18}$$

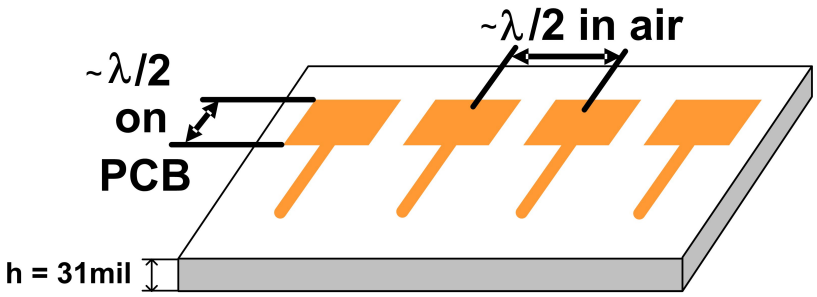
$$|c_b|^2 = |s_{21}|^2\left(kT_{min} + \frac{k_t|\Gamma_{opt}|^2}{|1 + \Gamma_{opt}|^2}\right) \tag{2.19}$$

$$\overline{c_a c_b^*} = \frac{-s_{21}^*\Gamma_{opt}^* k_t}{|1 + \Gamma_{opt}|^2} + s_{11}s_{21}^*\left(kT_{min} + \frac{k_t|\Gamma_{opt}|^2}{|1 + \Gamma_{opt}|^2}\right) \tag{2.20}$$

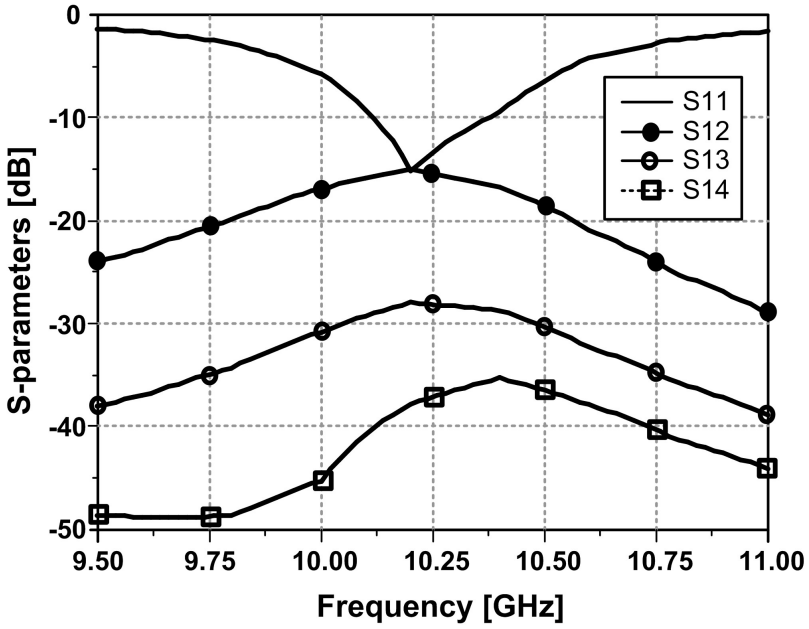
The noise waves c_a are directed towards the antenna and coupled into the other receive elements through the coupling between the antennas. Thus, the noise at the array output consists of the c_b component as well as the c_a components that couple into other receivers [34].

2.5.2 Antenna Coupling

In a multiple antenna system, the separation between antennas is of the same order as the wavelength. The close spacing between antennas results in coupling between them and hence noise from one receive element couples into another



(a) Four-element patch antenna array at 10.24GHz ($d = \frac{\lambda}{2}$)



(b) Simulated s-parameters

Figure 2.6: Antenna coupling in array

element. For e.g., Figure 2.6(a) shows a four-element patch antenna array at 10GHz with spacing $d = \frac{\lambda}{2}$ on a substrate with dielectric constant, $\epsilon_r = 2.2$. The simulated s-parameters, shown in Figure 2.6(b), demonstrate the coupling between different antenna elements [35]. This coupling depends upon both the topology of the antennas and the spacing between them. In an array receiver, this coupling along with a non-ideal match at the input of the receiver results in correlation between the noise in different receivers [34].

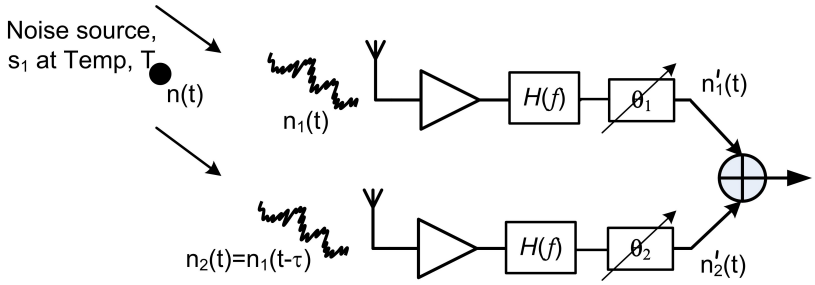


Figure 2.7: Correlation of noise from a point source at different element inputs

2.5.3 Input Noise Correlation

Another source of noise correlation in an array is the correlation between the noise at the input of different antennas. For example, if the noise source is a point source, the signal arrives at different antennas with different delays (Figure 2.7). Using the notation in Figure 2.7, the correlation between the output noise of element 1, $\acute{n}_1(t)$, and that of element 2, $\acute{n}_2(t)$, can be expressed in terms of the cross-correlation spectral density, $S_{\acute{n}_1\acute{n}_2}(f)$ which is given by,

$$S_{\acute{n}_1\acute{n}_2}(f) = S_{nn}(f)\,|H(f)|^2\, e^{-j2\pi f\tau_0} e^{-j(\theta_2-\theta_1)} \tag{2.21}$$

where path loss has been ignored and all circuit elements are assumed to be noiseless.

The cross correlation between the output noise at different elements thus depends upon system bandwidth, spacing between the antennas and noise spectrum of the source. Correlation radiometers exploit this input noise correlation in order to detect the temperature of objects in their field [36–38].

In the case of extended noise sources such as the sky or a wall, the noise radiated from different parts is assumed to be incoherent and the noise properties are specified through the brightness, B, of the source which is defined to be the power

radiated per steradian per unit area. Given a blackbody[1] at a temperature, T, the brightness per Hertz at a given frequency is given by Planck's equation [39],

$$B_f = \frac{2hf^3}{c^2}\left(\frac{1}{e^{\frac{hf}{k_BT}}-1}\right) \tag{2.22}$$

where h is the Planck's constant, c is the speed of light, and k_B is Boltzmann's constant. The Rayleigh-Jeans equation for blackbody radiation approximates Planck's equation(2.22) at low frequencies [39],

$$B_f = \frac{2f^2k_BT}{c^2} = \frac{2k_BT}{\lambda^2} \tag{2.23}$$

Thus, the noise radiated from the blackbody is characterized in terms of its noise temperature, T. Since most objects are not perfect black bodies, a noise temperature, T_B, can be defined for such objects in terms of their brightness.

When a single lossless antenna with a normalized radiation pattern, $F(\theta,\phi)$ is placed in a region with unpolarized noise sources at temperature, $T_B(\theta,\phi)$, the effective noise temperature at the antenna terminal is given by [39],

$$T_{eff} = \frac{1}{\Omega_a}\iint_{\Omega} T_B(\theta,\phi)F(\theta,\phi)d\Omega \tag{2.24}$$

where Ω_a is the beam solid angle of the antenna and is given by,

$$\Omega_a = \iint_{\Omega} \left|F\left(\theta,\phi\right)\right|^2 d\Omega \tag{2.25}$$

When multiple lossless antennas are located in a region where the temperature map is given by $T_B\left(f,\theta,\phi\right)$, the correlation between noise at the input to each element can be calculated by integrating the correlation due to all noise sources across all space,

[1] A perfect blackbody is one that absorbs all of the radiation incident on it and radiates energy at all wavelengths with perfect efficiency.

$$\overline{bs_i bs_j^*}(f) = \frac{1}{\sqrt{\Omega_{a1}\Omega_{a2}}} \iint_{\Omega} kT_B(f,\theta,\phi) \exp^{j2\pi f\tau(\theta,\phi)} F_i(f,\theta,\phi) F_j^*(f,\theta,\phi)\, d\Omega \quad (2.26)$$

As shown in [40], in the case of an antenna in thermal equilibrium with the surroundings that are at temperature, T_0, Bosma's theorem [41] can be applied to determine the noise correlation without performing the laborious integration. According to Bosma's theorem, for a passive multiport, in this case the multiple antenna system, characterized by the s-parameter matrix, $\mathbf{S}$, the noise correlation matrix is given by,

$$\mathbf{C_s} = kT_0\left(\mathbf{I} - SS^{\dagger}\right) \quad (2.27)$$

When the multiple antenna array is surrounded by absorbers, the system is in thermal equilibrium and hence (2.27) can be applied. However, when the antenna array is in a region with non-uniform temperature $T(\theta,\phi)$, it is not in thermal equilibrium but rather is in steady state. As a result, the noise correlation should be determined using (2.26).

2.5.4 Total Output Noise

The system in Figure 2.8 depicts a simplified phased-array receiver with an amplifier and phase shifter in each element. In the following analysis, the frequency dependence of all parameters is not shown explicitly for notational simplicity. The noise vector, $\tilde{\mathbf{N}}_{\mathbf{out}}$, represents the noise at the output of each array element due to the input noise vector, $\mathbf{B}$, and the amplifier noise wave vectors, $\mathbf{C_a}$ and $\mathbf{C_b}$.

$$\mathbf{B} = \begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_N \end{pmatrix} \mathbf{C_a} = \begin{pmatrix} c_{a,1} \\ c_{a,2} \\ \vdots \\ c_{a,N} \end{pmatrix} \mathbf{C_b} = \begin{pmatrix} c_{b,1} \\ c_{b,2} \\ \vdots \\ c_{b,N} \end{pmatrix} \quad (2.28)$$

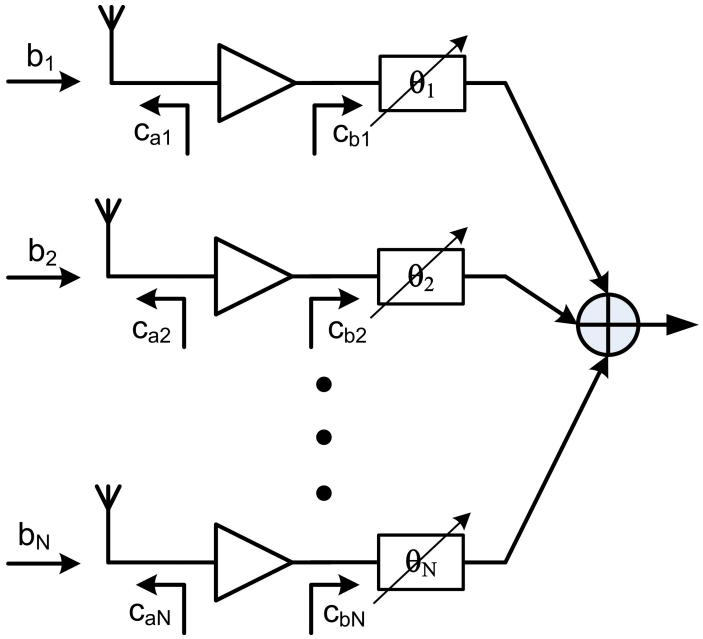


Figure 2.8: Simplified phased-array receiver with noise sources

The matrices $\mathbf{\Gamma_R}$, and $\mathbf{G_{21}}$ are defined to be,

$$\mathbf{\Gamma_R} = \begin{pmatrix} s_{11,1}^{amp} & 0 & 0 & 0 \\ 0 & s_{11,2}^{amp} & \ddots & 0 \\ 0 & \ddots & \ddots & 0 \\ 0 & 0 & 0 & s_{11,N}^{amp} \end{pmatrix} \mathbf{G_{21}} = \begin{pmatrix} s_{21,1}^{amp} & 0 & 0 & 0 \\ 0 & s_{21,2}^{amp} & \ddots & 0 \\ 0 & \ddots & \ddots & 0 \\ 0 & 0 & 0 & s_{21,N}^{amp} \end{pmatrix} \tag{2.29}$$

In order to derive the output noise in the array, the analysis in [42] for correlation radiometers is initially followed, which does not include the variable phase shift in each element. While considering the contribution of the input noise to the noise in the array, it must be noted that lossy antennas reduce the correlation between the input noise in each element. Assuming that the antenna in the n^{th} element has an

efficiency, η_n the antenna efficiency matrix $\boldsymbol{\Upsilon}$, is defined to be,

$$\boldsymbol{\Upsilon} = \begin{pmatrix} \eta_1 & 0 & 0 & 0 \\ 0 & \eta_2 & \ddots & 0 \\ 0 & \ddots & \ddots & 0 \\ 0 & 0 & 0 & \eta_N \end{pmatrix} \tag{2.30}$$

Considering only the input noise vector, $\mathbf{B}$, and defining, $\boldsymbol{\Lambda} = (\mathbf{I} - \mathbf{S_{ant}}\boldsymbol{\Gamma_R})^{-1}$, the output noise vector is,

$$\tilde{\mathbf{N}}_{\mathbf{out,B}} = \mathbf{G_{21}}\left(\boldsymbol{\Lambda}\boldsymbol{\Upsilon}^{\frac{1}{2}}\mathbf{B} + k_B T_{ant}\mathbf{S_{ant}}\boldsymbol{\Lambda}\left(\boldsymbol{\Upsilon}^{-1} - \mathbf{I}\right) + k_B T_{ant}\left(\mathbf{I} - \boldsymbol{\Upsilon}\right)\right) \tag{2.31}$$

where $\mathbf{S_{ant}}$ are the s-parameters of the antenna array and T_{ant} is the temperature of the antenna array. Similarly, the noise vector at the output when only the amplifier noise wave vector, $\mathbf{C_a}$ is considered, is given by,

$$\tilde{\mathbf{N}}_{\mathbf{out,C_a}} = \mathbf{G_{21}}\mathbf{S_{ant}}\boldsymbol{\Lambda}\mathbf{C_a} \tag{2.32}$$

From (2.31) and (2.32), and including the contribution to output noise from $\mathbf{C_b}$ the total output noise vector is,

$$\tilde{\mathbf{N}}_{\mathbf{out}} = \tilde{\mathbf{N}}_{\mathbf{out,B}} + \tilde{\mathbf{N}}_{\mathbf{out,C_a}} + \mathbf{C_b} \tag{2.33}$$

The phase shift provided by the phase shifters in each element can now be included, through the phase-shift matrix, $\mathbf{E}$, where,

$$\mathbf{E} = \begin{pmatrix} e^{j\beta_1} & 0 & 0 & 0 \\ 0 & e^{j\beta_2} & \ddots & 0 \\ 0 & \ddots & \ddots & 0 \\ 0 & 0 & 0 & e^{j\beta_N} \end{pmatrix} \tag{2.34}$$

Incorporating the effect of phase shift in (2.33), the total noise correlation matrix,

$\tilde{\mathbf{N}}_{\mathbf{c}}$ is given by,

$$\tilde{\mathbf{N}}_{\mathbf{c}} = \mathbf{E}\tilde{\mathbf{N}}_{\mathbf{out}}\tilde{\mathbf{N}}_{\mathbf{out}}^{\dagger}\mathbf{E}^{\dagger} \tag{2.35}$$

In order to determine the noise power at the output, the frequency dependence of all the parameters in (2.35) has to be considered. The effect of the system bandwidth on noise correlation is accounted for through the frequency dependence of the antenna and the amplifier s-parameters.
From the Wiener-Khinchin theorem [43], the expected noise power at the output due to all elements is,

$$\overline{|\tilde{n}_{sum}(t)|^2} = R_{\tilde{n}_{sum},\tilde{n}_{sum}}(0) = \int_{-\infty}^{\infty} \sum_{l=1}^{l=N} \sum_{m=1}^{m=N} \tilde{\mathbf{N}}_{c_{(l,m)}}\, df \tag{2.36}$$

The output noise power in the case of a single element can be calculated from (2.36) for $N = 1$. It must be noted that when a single element is considered, it's pattern is affected by the presence of the other antennas even if they are terminated ideally. However, in order to estimate the increase in noise power, the noise when $N = 1$ is used as the baseline.

From (2.35) and (2.36), the output noise power and hence the SNR improvement in an array can depend upon the phase shift setting. This effect of this angle-dependent variation depends upon the relative magnitudes of the noise parameters.

2.5.5 Experimental Evidence

The theoretical analysis in the previous section was verified using a two-element discrete array consisting of InP LNAs and discrete phase shifters (as shown in Figure 2.9). The array operates at 10.24GHz with a filter bandwidth of 200MHz. The s-parameters of the receive element are shown in Figure 2.10. The noise parameters for the receive element were calculated by measuring the output noise power for different source impedances using a sliding short and 3dB attenuator.

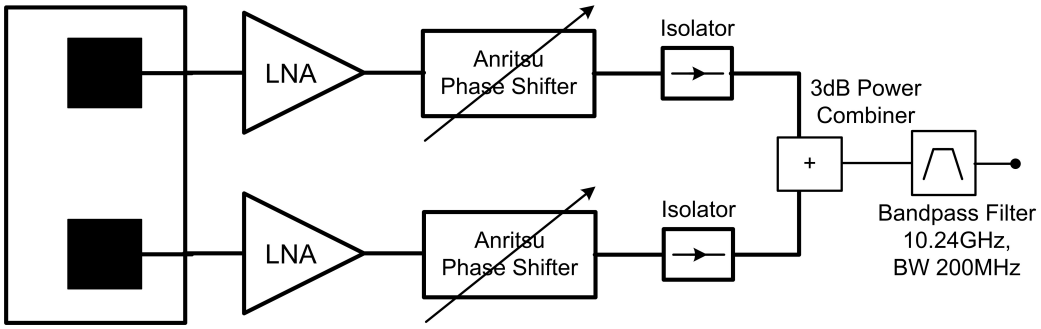


Figure 2.9: Experimental setup for measuring effect of input noise correlation on array noise

Figure 2.11 plots the fitted noise-parameters in the bandwidth of interest.

A two-element patch array was fabricated using Rogers 3002 with $\epsilon_r = 2.2$ and $h = 31mils$. The simulated and measured s-parameters of the patch are shown in Figure 2.12(a) along with the simulated and measured patch pattern shown in Figure 2.12(b).

In order to examine the case when the system is in thermal equilibrium, the array was places in an enclosure filled with absorbers. Figure 2.13 plots the measured increase in noise power along with the increase expected from (2.36). The measurements clearly demonstrate that the improvement is dependent on phase shift angle. Figure 2.14 plots similar curves for the same amplifier with a hypothetically higher noise figure[2]. For higher noise figures, the amplifier noise waves dominate the noise in the system and hence the variation in noise power with phase shift setting is mainly due to the coupling of the C_a noise waves in each element.
It is also interesting to look at systems with larger number of elements. Figure 2.15 plots the simulated output noise for an four-element array consisting consisting of the measured receivers connected to a 4-element patch antenna array (simulated shown in Figure 2.6(b)). The larger variation in output noise power indicates that such a phenomenon becomes more important with increasing number of elements in

[2]The higher noise figure is achieved by increasing the magnitude of all elements of the amplifier's noise correlation matrix

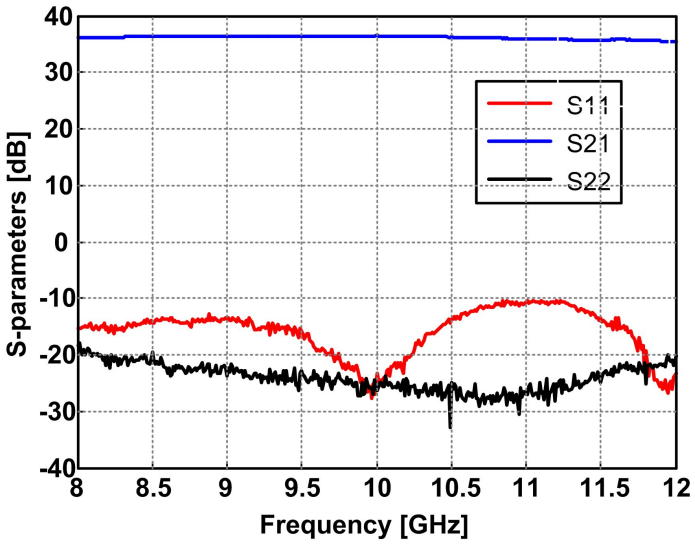


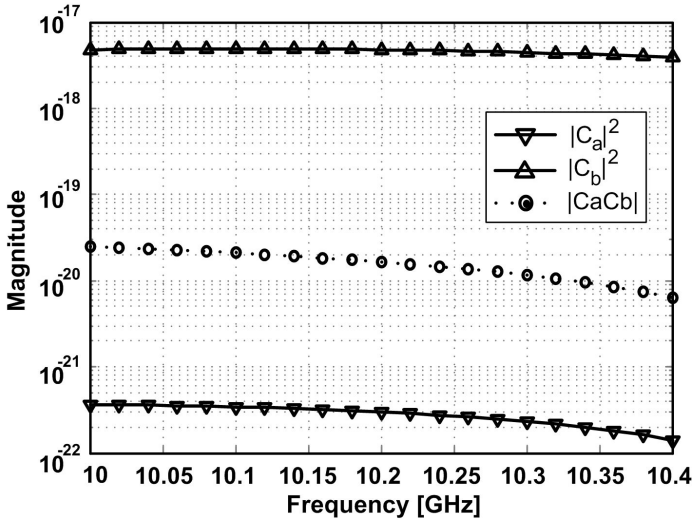
Figure 2.10: Measured s-parameters of each element of the array (excluding power combiner and filter)

the array.

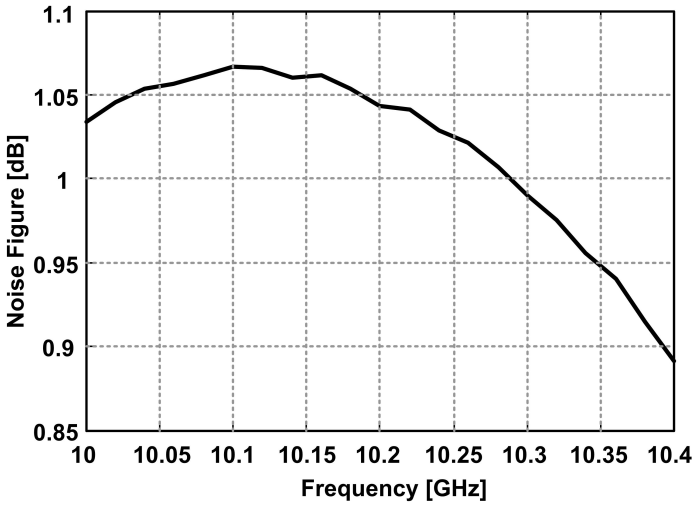
Also of interest is the expected noise output in typical indoor environments. The noise temperature of three different environments were measured using a 15dB gain horn antenna followed by a LNA. The noise figure of the measurement setup is determined using a cold sky and absorber noise measurement and was found to be 86.5K. The three environments for which measurements were made were an office, a corridor and a roof (as shown in Figure 2.16)[3]. Photographs of the measurement environments can be seen in Appendix A.

For the indoor environments considered, the noise temperature variations can be traced to the presence of fluorescent lights and windows. The windows present a noise temperature that is around 40K lower than ambient while fluorescent lights present a noise temperature 30K above ambient. Array noise measurements in such anisotropic noise environments are shown in Figure 2.17. As opposed to the SNR improvement curves in Figure 2.14, the curves in Figure 2.17 displays an a larger

[3]The effects of polarization have not been considered in this measurement

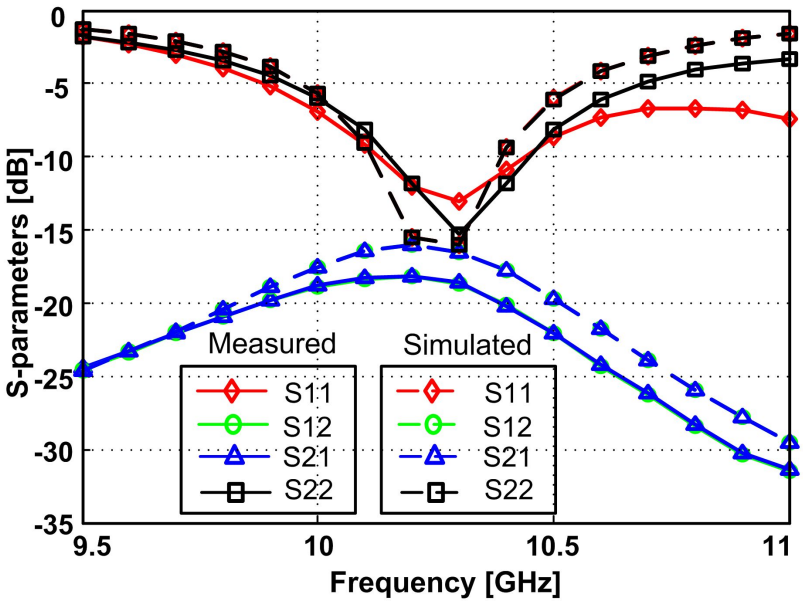


(a) Noise wave magnitudes for an array element

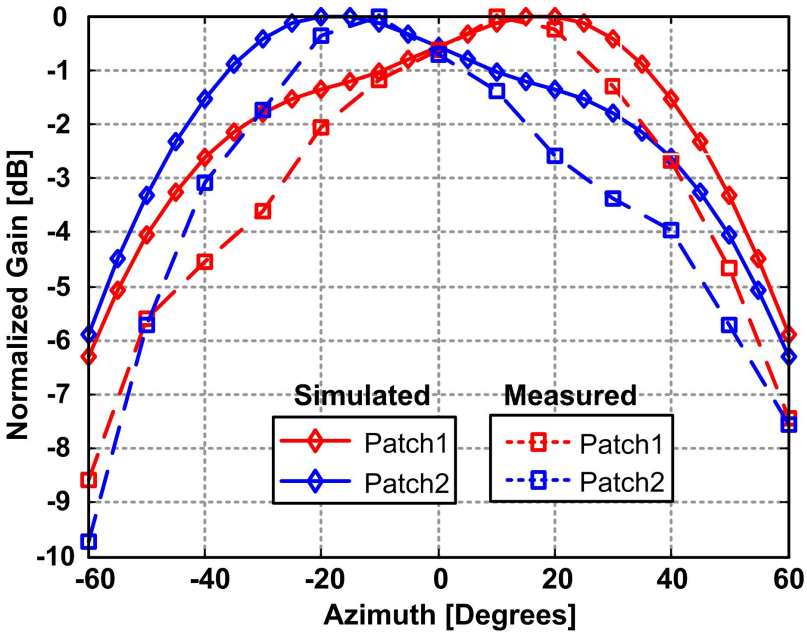


(b) Noise figure of array element ($\Gamma_s = 0$)

Figure 2.11: Measured noise parameters of array element



(a) Simulated and measured s-parameters of 2-element patch array



(b) Simulated and measured patch pattern

Figure 2.12: Simulated and measured patch antenna performance

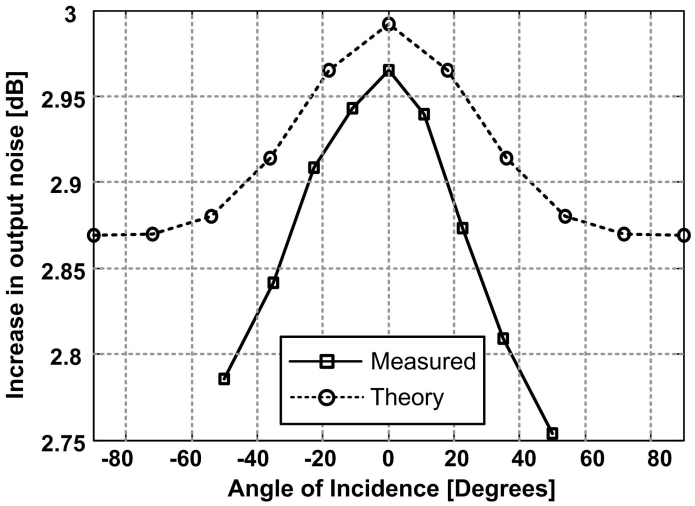


Figure 2.13: Output noise variation with phase shift setting when array is surrounded by absorbers

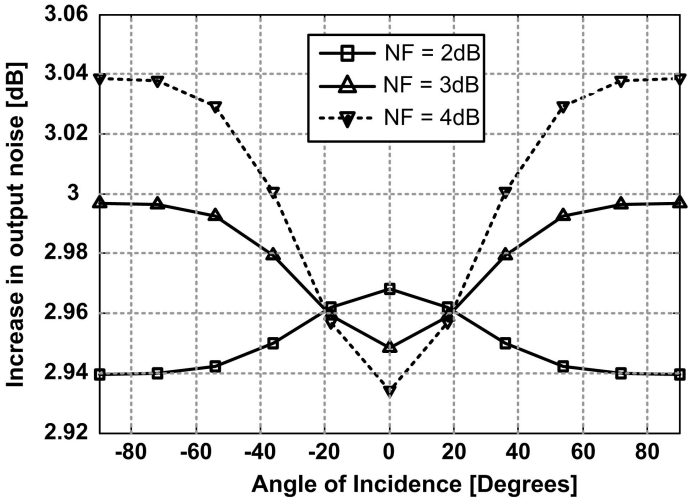


Figure 2.14: Simulated output noise variation with phase shift setting for higher LNA noise figures

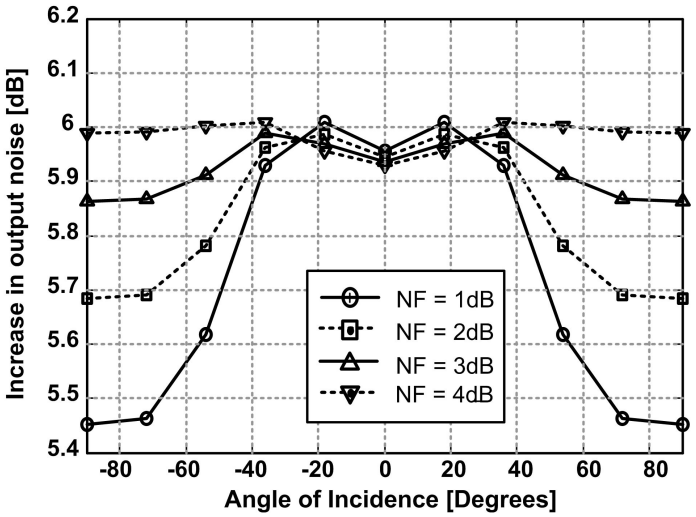
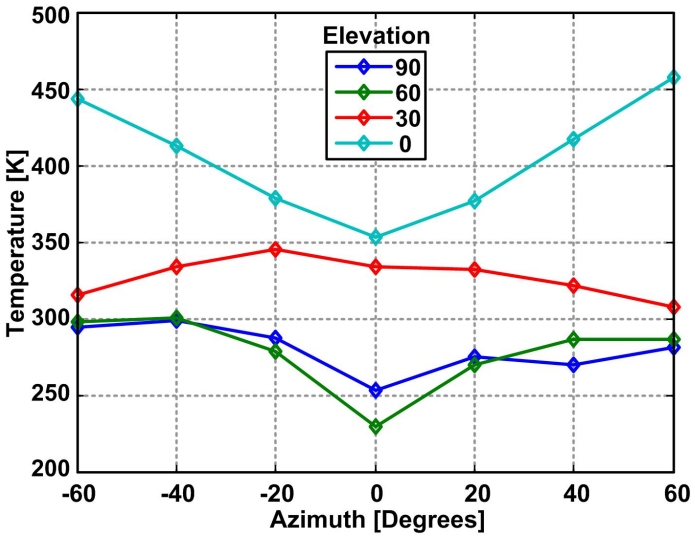


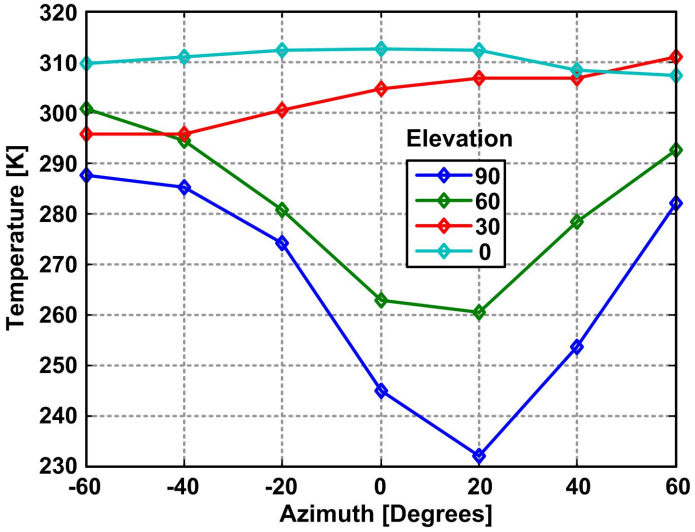
Figure 2.15: Simulated output noise variation with phase shift setting for four-element array

variation in input noise temperature with phase-shift setting due to the effect of input noise correlation. The array noise curve is convex in Figure 2.17(a) due to the higher noise temperature for higher angles of elevation on the roof [Figure 2.16(c) and Appendix A]. While such variations of output noise would be expected when a high gain antenna is physically pointed towards different directions with varying noise temperatures (from (2.24)), such variation would not occur in the measured array unless the input noise at different elements is correlated.

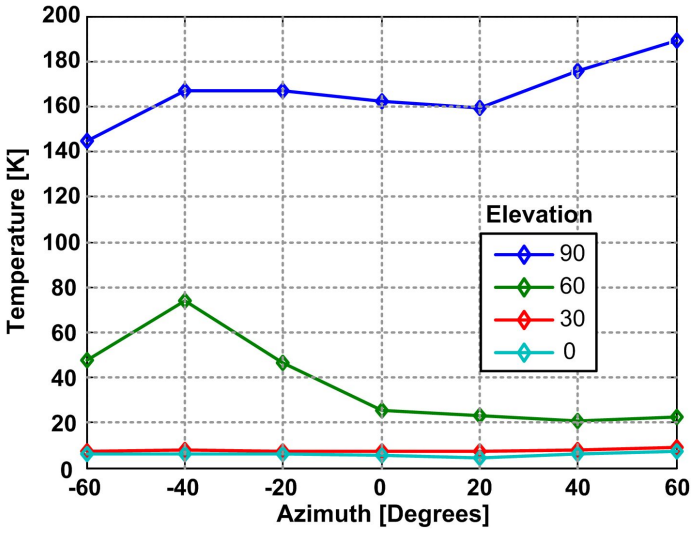
Thus, while the noise power increase in the array measured under different conditions is close to the 3dB expected from 2.11, it displays a dependence on phase shift setting as predicted by (2.35). This variation can be particularly important for arrays that have low element noise figures, that have large number of elements or those that operate in an environment where there is a large variation in noise temperature with direction.



(a) Noise temperature in office environment

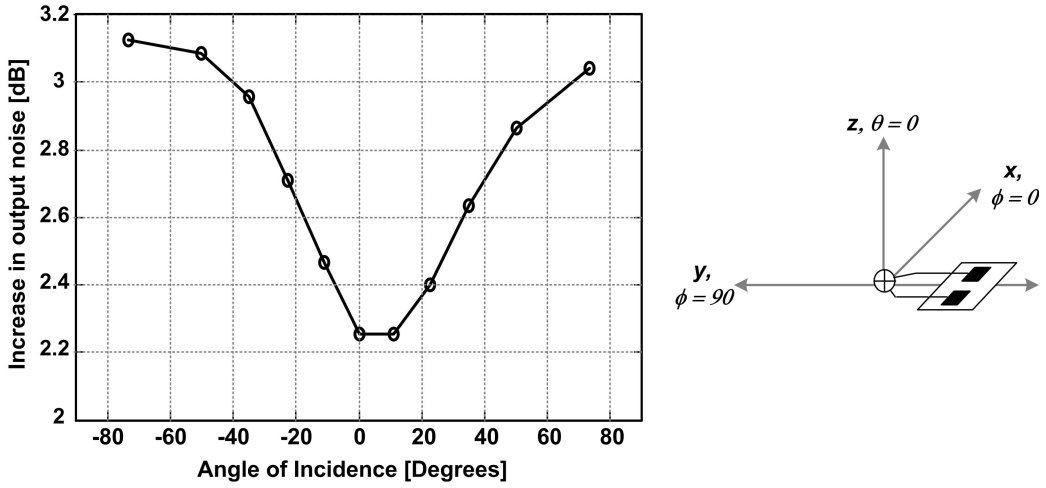


(b) Noise temperature in corridor environment

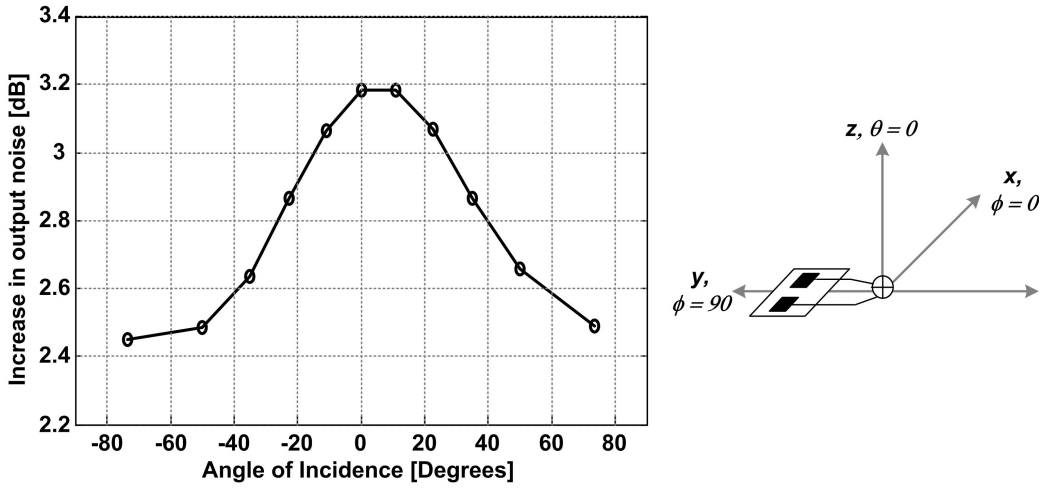


(c) Noise temperature on roof

Figure 2.16: Noise temperature as a function of direction in different environments



(a) Array output noise when measured on the roof



(b) Array output noise when measured in the office

Figure 2.17: Increase in output noise for different phase shift settings in indoor and outdoor environments

2.6 Chapter Summary

A brief introduction to the principles of operation of a phased array was provided in this chapter. The beamforming properties of the array lead to improvement in the SNR in the receiver and EIRP in the transmitter. An examination of the expected output noise in a phased array receiver in the presence of coupling and input noise correlation shows that that the output noise power depends upon the angle of incidence. Measurements on a discrete two-element array confirm the theoretically predicted output noise power variation with phase shift setting.

Chapter 3

Phased Arrays at High Frequencies

Space is the next frontier as wireless systems evolve to provide increasing functionality such as radar and high data rate communication. While improvements in spectral efficiency are getting increasingly difficult to achieve using time-and-frequency domain methods, spatial processing using multiple antenna elements provides several methods of extracting the most from scarce and expensive spectrum [44–46]. Phased arrays are one such class of multiple antenna systems that have beamforming and beams steering properties. In such multiple-antenna systems, the physical size of the system decreases with an increase in frequency as the antenna size and spacing are inversely proportional to frequency. Furthermore, larger bandwidths are available at high frequencies such as 24GHz and 60GHz. Thus, the large available bandwidths and smaller physical system size render high frequencies attractive for integrated multiple-antenna systems.

In this chapter, the advantages and challenges of high-frequency phased arrays are discussed in depth. Section 3.1 discusses the tradeoffs of communication systems operating at high frequencies using a Shannon capacity based approach. The motivation and challenges of implementing high-frequency phased arrays in silicon are considered in Section 3.2. Different architectural choices for integrated phased arrays and the tradeoffs associated with each architectural choice are discussed in Section 3.3. Section 3.4 evaluates the effect of the narrowband approximation that is implicit in the operation of a phased array and discusses an equalization scheme

that reduces the error due to the approximation.

3.1 High-Frequency Wireless Communication

High frequencies appear very attractive for wireless communication due to the large available bandwidth. However, the advantage of large bandwidths at high frequencies is offset to some extent by the lower received power and the higher receiver noise figure at high frequencies. The tradeoffs of moving to high frequencies can be captured through the capacity of the network, given by Shannon's theorem [47], according to which the capacity, C, of a communication channel, with bandwidth, B, is,

$$C = B \log_2 (1 + SNR) \tag{3.1}$$

where SNR is the signal-to-noise ratio. The signal power at the receiver, P_{RX} is given by Friis equation [48],

$$P_{RX} = P_{TX} \frac{G_{TX} G_{RX} \lambda^2}{(4\pi)^2 d^l} \tag{3.2}$$

where, P_{TX} is the transmit power, G_{RX} and G_{TX} are receiver and transmitter antenna gain, λ is the wavelength, d is the distance between the transmitter and receiver, and l is the exponent that accounts for excess path loss. Thus the received power decreases as the square of the frequency. While it is possible to increase the received power by increasing the antenna aperture area, A_e, the antenna theorem [5] states that the aperture area, A_e and the gain, G of the antenna are related by,

$$A_e = G \frac{\lambda^2}{4\pi} \tag{3.3}$$

Therefore, for a given frequency of operation, an increase in the aperture area is accompanied by an increase in gain which is undesirable since high antenna gain in a fixed antenna limits system operation to the directions in which the antenna has

gain. Thus, increasing aperture area is often not a useful method of increasing received power.

The noise of a receiver is typically dominated by the noise figure of the low-noise amplifier (LNA) immediately following the antenna. Using an optimally designed CMOS common-source LNA as a template, the noise factor, F, is assumed to increase linearly with frequency,

$$F = 1 + k\frac{f}{f_t} \tag{3.4}$$

where f_t is the unity current-gain frequency of the process technology [49]. The noise power at the receiver input for a bandwidth B and antenna noise temperature T is,

$$P_{noise} = k_B T B \tag{3.5}$$

where k_B is the Boltzmann constant (1.38e-23 W/K/Hz). Hence, the SNR at the output of the receiver is,

$$\text{SNR}_{out} = \frac{P_{RX}}{F k_B T B} \tag{3.6}$$

Applying (3.2), (3.4) and (3.6) in (3.1), the capacity can be expressed as,

$$C = B \log_2 \left(1 + \frac{\alpha P_{TX} G_{TX} G_{RX} \lambda^2}{(4\pi d)^2 k_B T B \left(1 + \frac{f}{f_t}\right)} \right) \tag{3.7}$$

where α accounts for the frequency-dependent loss in air due to water-vapour and oxygen absorption (Figure 3.1).

Figure 3.2 plots the channel capacity against carrier frequencies for numerical values of the variables in (3.7). A noise figure of 3dB is assumed at 6GHz, resulting in a noise figure of 7dB at 24GHz which is close to performance achieved in literature [50, 51]. The transmit and receive antennas are assumed to be isotropic ($G = 1$) and fading due to multipath propagation is not considered (i.e., $l = 2$).

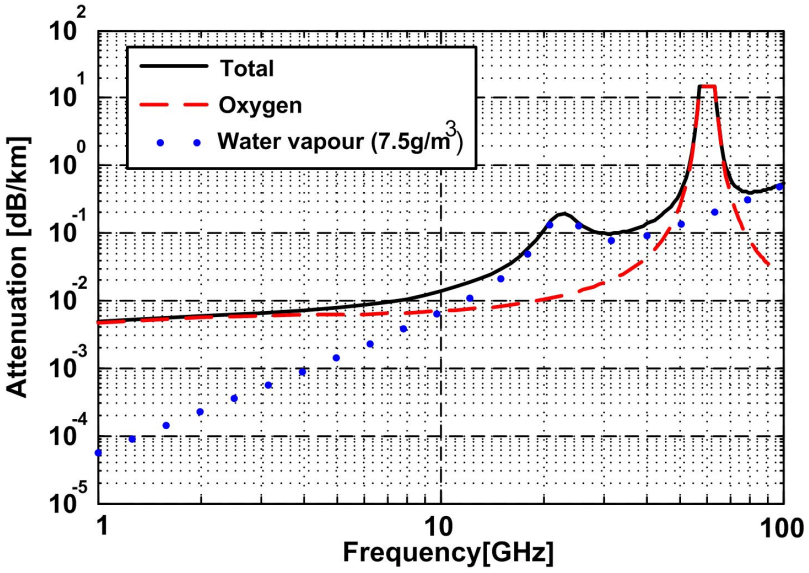
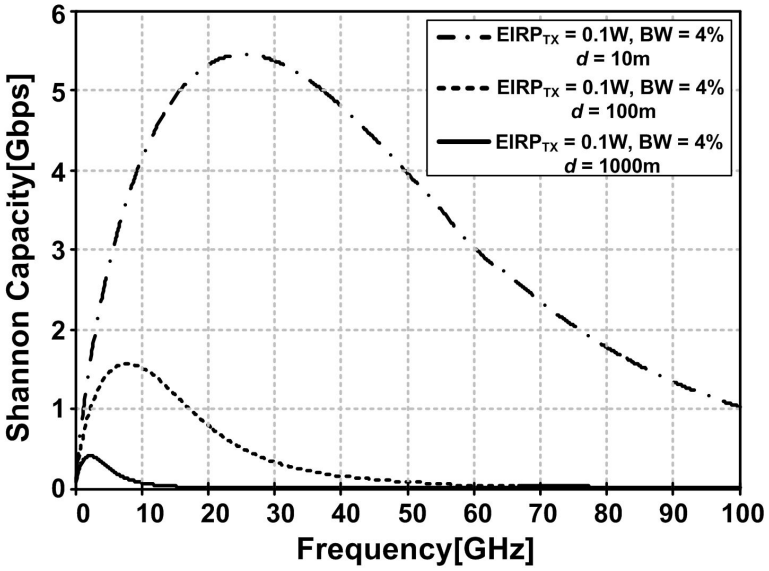


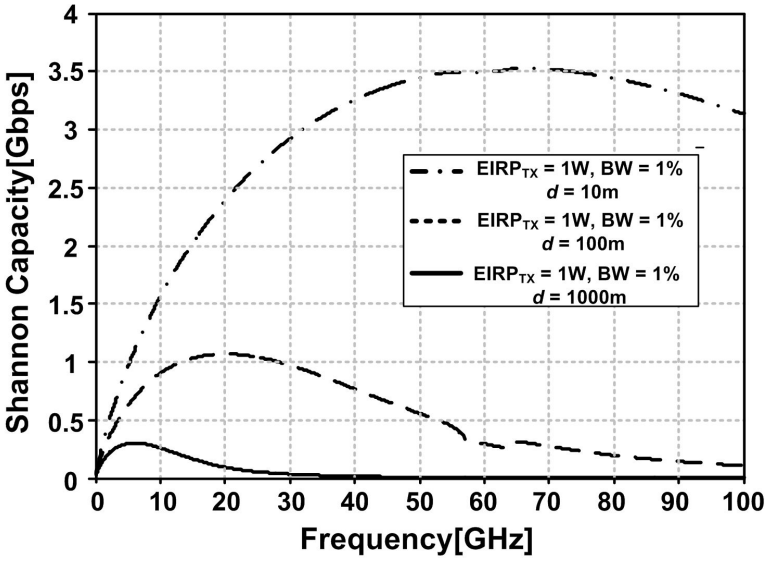
Figure 3.1: Attenuation in the atmosphere due to water vapour ($7.5\text{g}/m^3$) and oxygen.

Since the quality-factor of resonant circuits remains fairly constant across frequency, the fractional bandwidths are assumed constant which implies that the absolute bandwidths increase with frequency.

The fact that the curves are not monotonic and exhibit a peak, demonstrates the tradeoff between larger bandwidths, lower collected power, and higher noise figure at high frequencies. The peak in the channel capacity curve moves to lower frequencies for larger distances and occurs at higher frequencies for larger fractional bandwidths. Also, the peak moves to higher frequencies with higher transmit EIRP or lower noise figure, both of which can be improved by implementing multiple-antenna systems such as phased arrays. Figure 3.3 plots the channel capacity, C, for different transmitter-receiver separations, assuming a bandwidth of 200MHz, EIRP of 30dBm and receiver noise figure of 7dB at 24GHz. If such a 24GHz communication system were to employ a four-element phased-array receiver, the signal-to-noise ratio at the output may be improved nominally by 6dB (2.11). When this improvement in SNR is included in (3.7), it can be seen that high-speed (greater than 1Gbps) phased-array data links are possible up to distance of 200m at



(a) Channel capacity for EIRP = 0.1W, BW = 4%



(b) Channel capacity for EIRP = 1W, BW = 1%

Figure 3.2: Comparison of channel capacities for different system parameters demonstrate the tradeoffs of moving to high frequencies.

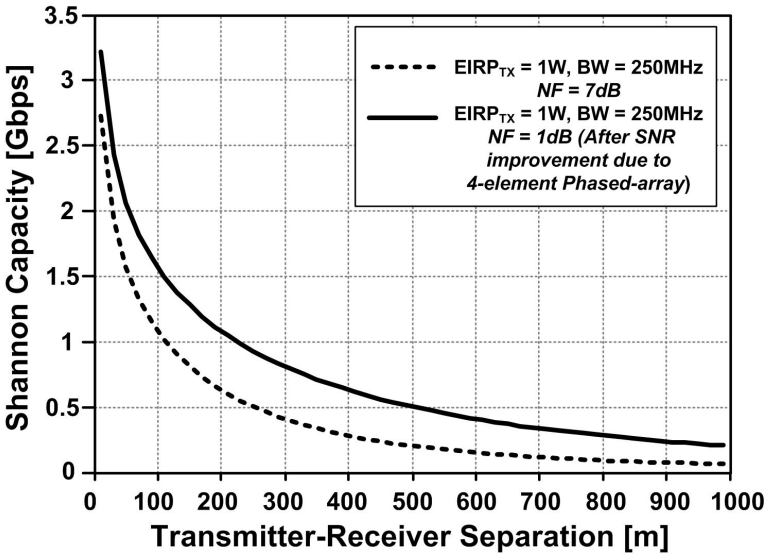


Figure 3.3: Channel capacity for different transmitter-receiver separations at 24GHz.

24GHz, demonstrating the potential of mm-wave wireless communication.

3.2 Phased-Array Integration in Silicon

The success of silicon integration over the last 30 years has bred more success, with vast investments in research and infrastructure, leading to rapid improvements in device speed and reliability. The aggressive Moore's law type scaling of transistors while maintaining high yield, has resulted in faster device performance and drastically lowered costs for mass-produced high transistor-count products [52, 53]. While other III-V semiconductor technologies like GaAs and InP provide better single device performance, they do not provide the same large-scale integration capabilities and consequently the same cost structure. Therefore, from a commercial standpoint, it is silicon-based technologies like CMOS and SiGe that are preferred for cost-sensitive consumer applications, with III-V semiconductors being used only when warranted by performance requirements.

From the perspective of RF systems, silicon process technologies have advanced exponentially over the years, with the f_t in excess of 60GHz and 200GHz for CMOS

and SiGe transistors respectively. Unfortunately, the same scaling that improves transistor speed also leads to lower breakdown voltages [53]. Integration of passives, such as inductors and capacitors, also presents a problem in silicon due to the interconnect loss and the lossy silicon substrate. While semiconductors such as GaAs and InP are insulating (10^7 - 10^9 Ω-cm), the silicon bulk used in standard processes has a conductivity from 5mΩ-cm to 10Ω-cm (part of this doping is to prevent latch-up). In the case of inductors, the eddy currents generated in the substrate contribute significantly to loss leading to typical on-chip inductor Q of 15-35. While the inductor can be shielded from the substrate by patterned ground shields [54], the shielding increases the parasitic capacitance of the inductors leading to lower self-resonance frequency.

In spite of these shortcomings, silicon integration is a very promising solution for millimeter-wave systems because of the great advantages it affords. Since multiple well-matched devices can be manufactured with high yield, performance requirements can be achieved by harnessing the capabilities of multiple devices operating in sync. Furthermore, digital tuning and calibration incorporated in integrated systems can be used to improve the performance of critical analog/RF parts compensating for inferior performance of silicon transistors [55, 56]. Importantly, the very low incremental cost of signal processing elements, i.e., transistors, and the benefits of integration such as short and robust interconnects and good component matching, enable the realization of novel system architectures that are designed specifically for existing and emerging applications. Thus, the simultaneous integration of the digital baseband circuitry and the analog RF circuits enables mm-wave system-on-a-chip solutions that would improve performance while lowering cost.

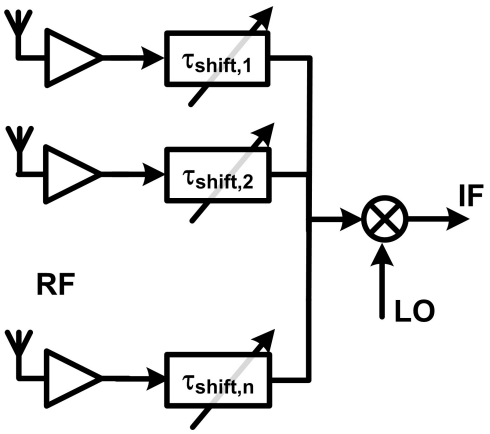
As mentioned before, the low breakdown voltages and low-Q passives present significant obstacles towards generating high power on silicon. If the output matching network of power amplifiers is integrated using such lossy passives, the

loss in the output matching network along with low active gain of CMOS transistors leads to single-digit power-added efficiencies. On the receiver side, the lower active gain and the higher noise of silicon devices lead to lower receiver sensitivity. Phased arrays provide a solution to both these problems as they increase transmit EIRP and improve system SNR, making them attractive candidates for silicon integration. However, an attempt to integrate phased arrays by replicating architectures used in III-V process technologies would be difficult due to the unique challenges posed by silicon. Hence, new architectures have to be adopted that leverage the advantages of silicon and improve performance. In the next section, various phased-array architectures are discussed in the context of their suitability for silicon integration.

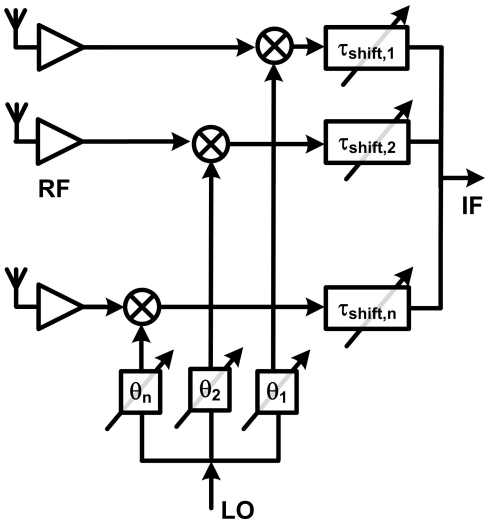
3.3 Phase-Shift Architectures for Integrated Phased Arrays

Traditionally, the phase shift necessary in each element of the phased-array is implemented using discrete modules like ferrite phase-shifters or switch-based phase shifters [13]. In case of ferrite phase shifters, the phase shift is controlled by varying the magnitude of the magnetic field. While such a phase shifter achieves low loss and high linearity, it is not very suitable for silicon integration. GaAs FET switches with insertion loss of 2.5dB and isolation better than 22dB have been reported up to 110GHz [57]. While CMOS switches have achieved 1.8dB insertion loss and 20dB isolation at 15GHz [58], higher frequency switches with similar performance are yet to be demonstrated.

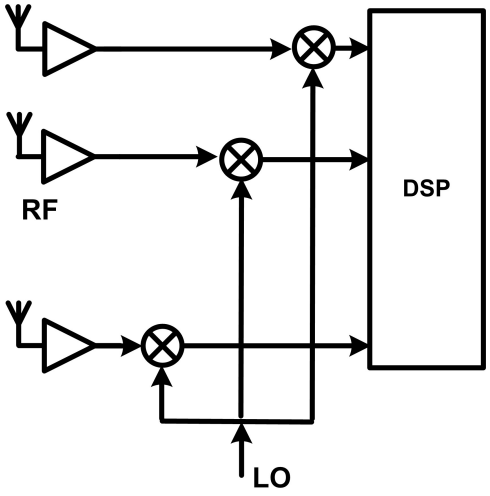
In order to investigate phased-array architectures suitable for integration, the governing equation of the array is once again analyzed. Figure 3.4(a) shows an N-element broadband array architecture with true-time delay in each element that compensates for the different signal arrival times in each element. In this case the output of each element before combining is



(a) Delay at RF

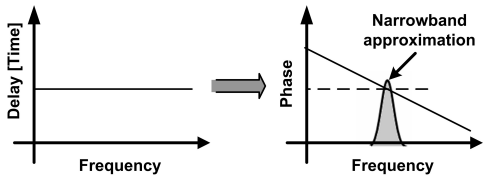


(b) Delay at IF

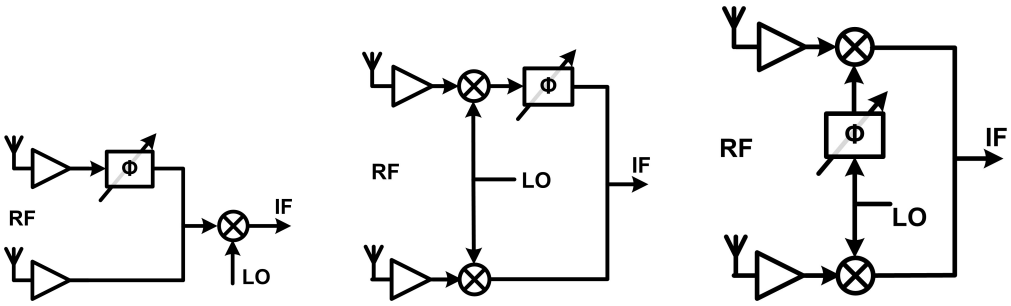


(c) Delay in DSP backend

Figure 3.4: Broadband array architectures



(a) Narrowband phase shift approximation for delay



(b) RF Phase shift (c) IF Phase shift (d) LO Phase shift

Figure 3.5: Narrowband phased array architectures

$$V_n(t) = V(t - \tau_n - \tau_{shift,n})\, cos(\omega_{RF}(t - \tau_{shift,n})) \tag{3.8}$$

In case of a heterodyne architecture where the signals from all elements are downconverted to an IF frequency before combining, this true-time delay at RF is mathematically equivalent to a delay at IF accompanied by a delay in the LO path [Figure 3.4(b)]. Since the signal in the LO path is a single tone, a phase shift at the LO frequency is exactly equivalent to a delay. Therefore, the architecture in Figure 3.4(b) is a true broadband array architecture. While the signal from each element can also be delayed in the digital back-end [Figure 3.4(c)], the delay resolution required is of the scale of the RF time period and hence difficult to achieve.

A true-time delay is equivalent to a linear phase shift in the frequency domain. In case of narrowband signals, the linear phase shift can be approximated by a constant phase shift as shown in Figure 3.5(a). The architecture in Figure 3.5(b) is thus an approximation of the one in Figure 3.4(a) while the LO and IF phase-shifting architectures approximate the true-time delay architecture in Figure 3.4(b). The IF

phase shift can also be implemented in the digital domain as shown in Figure 3.4(c). Phase shifting and signal combining in the RF path would potentially simplify array design as it eliminates the need for additional mixers and downconversion paths. Furthermore, since undesired signals are attenuated before the mixer, the mixer linearity requirement is reduced. However, in case of RF-combining, since the phase shifters are in the signal path, the linearity, the noise figure of the phase shifters and the gain bandwidth of the phase shifters are extremely important. Additionally, the gain/loss of the phase shifter must be equalized across different phase shifts as the peak-to-null ratio and the sidelobe levels in the array pattern are determined by the amplitude matching between different elements. Implementing such wideband, low-noise, high-frequency phase shifters with constant gain across phase settings in silicon is a challenging task. In Chapter 6, a bidirectional array architecture is introduced that uses hybrid parallel-series phase shifting to reduce phase-shifter requirements.

Phase shifters at IF suffer from the same problems as phase shifters at RF while needing additional mixers as well as amplifiers. Moreover, since the phase shifters operate at lower frequencies, the physical size of the passives increases leading to larger area consumption. These disadvantages can be overcome by implementing the phase shift digitally at baseband. While such an implementation provides the most flexibility, it places a high requirement on the DSP which has to process signals at the twice the bitrate from each of the elements. Additionally, the DSP speed requirements increase linearly with number of elements and the bitrate.

Phase shifters in the LO path circumvent problems of non-linearity and amplitude matching as the circuits in the LO path such as the voltage-controlled oscillator(VCO) and the LO-path amplifiers operate in saturation by design since the performance of the typical integrated frequency conversion mixers is improved with larger LO voltage swings. Furthermore, with large LO signal swings at the LO ports of the mixers, the sensitivity of mixer gain to the LO signal amplitude is low.

As a result, with phase shifters in the LO path, the variation in signal amplitude for different values of phase shift is minimal.

The phase shift necessary in the LO path can be implemented in many ways [59–61]. In Chapter 4, a centralized LO phase-shifting scheme that utilizes a multi-phase VCO is adopted in an 24GHz Tx. For the 77GHz array presented in chapter 5, a localized LO phase-shifting scheme is introduced that scales well with an increase in number of elements and/or operating frequency and provides higher resolution phase-shifts.

In the following sections, various sources of errors in phased arrays are discussed along with their effects. One of the most important limitations of arrays, stemming from the narrowband approximation, is discussed in Section 3.4.

3.4 Phase-Shift Approximation in Phased Arrays

Phased array is perhaps a misnomer for these systems given that true-time delay, and not phase shift, is required in each path for coherent addition of signals, as shown in (2.3). Fortunately, in many practical applications, particularly in wireless communications, the bandwidth of interest is a small fraction of the center frequency; hence, a uniform delay (linear phase shift) is only required over this narrow bandwidth and can be approximated with a constant phase shift. This aligns the carrier phase of different paths. However, the modulating signal is not delayed appropriately, leading to some dispersion in the demodulated signal. A higher modulation-bandwidth-to-carrier-frequency ratio results in larger signal dispersion, manifested by the spreading of the constellation points. This distortion results in an increased bit error rate (BER) in wireless communication systems and in a reduced radial resolution in radar applications.

The input signal to the first element in an N-element phased-array receiver can be represented as,

$$s(t) = v(t)\cos\left(\omega_{rf}t + \phi(t)\right) \tag{3.9}$$

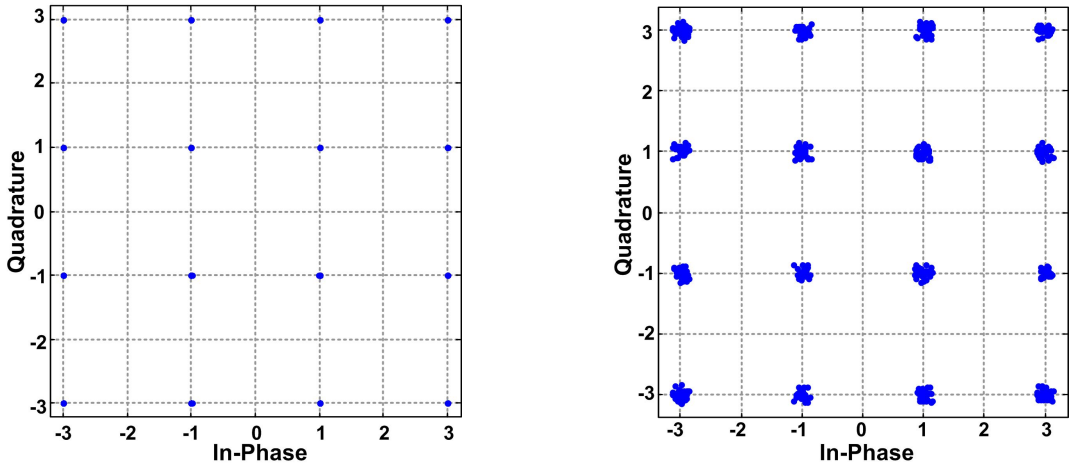
where $s(t)$ and $\phi(t)$, represent the baseband signal modulating the carrier. When phase shifts are implemented in each element to achieve a radiation angle of Φ, for which the propagation delay between successive elements differs by τ, the combined signal power is,

$$S(t) = \sum_{n=0}^{N-1} v(t - n\tau)\cos\left(\omega_{rf}t + \phi(t - k\tau)\right) \tag{3.10}$$

Thus, the phase-shifting architectures do not ensure that the baseband modulating signals add up coherently as the group delay in each element is zero. This causes signal distortion which can seen by the shift of points from their ideal location in the data constellation. A measure of constellation distortion is the error vector magnitude (EVM), which is defined as the average euclidean distance between the distorted point and the ideal constellation point. The EVM, when represented as a fraction of signal power is,

$$EVM = \sqrt{\frac{P_{error}}{P_{signal}}} * 100 \tag{3.11}$$

In case of the narrowband approximation in phased arrays, the EVM increases with an increase in the number of elements and the bandwidth of the baseband signal, and can be a source of error on both the transmitter and receiver side leading to higher bit error rates [62]. Figure 3.6 plots the constellation points for a 5Gbps data stream with 16-QAM modulation at a carrier frequency of 60GHz. Raised-cosine filtering is assumed with a rolloff factor, $\alpha = 0.5$, leading to a bandwidth of 1.875GHz . The constellation is shown for angle of incidence, $\phi = 0°$ (Figure 3.6(a)) and for $\phi = 49°$ (Figure 3.6(b)). (In this case, only the distortion in the receiver is considered. In the case of a system based on a phased-array transceiver, the distortion occurs at both transmitter and receiver.)



(a) Signal constellation: $\phi = 0°$ (b) Signal constellation: $\phi = 49°$

Figure 3.6: Phased array signal constellation (Carrier_freq = 60GHz; Nelements = 8; Datarate = 5Gbps; 16QAM; Symbol Rate = 1.25Gbps; Rolloff = 0.5)

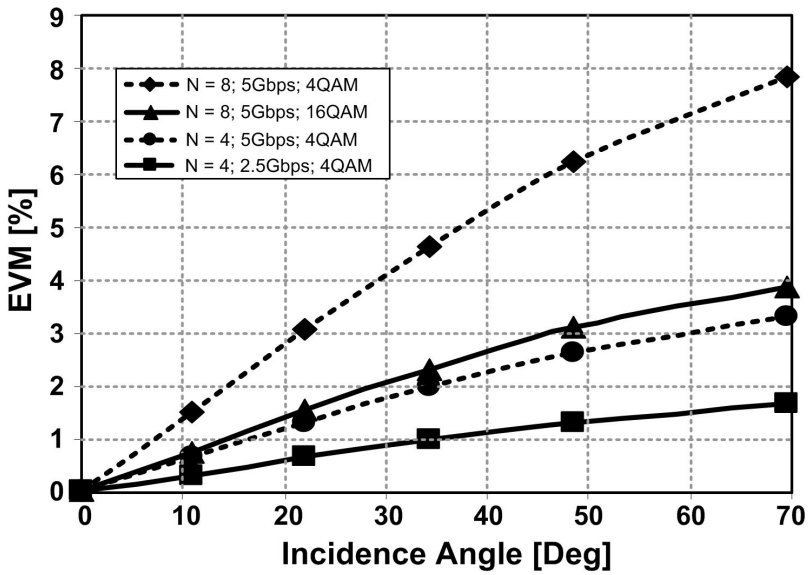


Figure 3.7: EVM vs angle of incidence for various system parameters (Carrier_Freq = 60GHz; Rolloff = 0.5)

As can be seen from (3.10) and Figure 3.6, the signal distortion increases with increasing angle of incidence. In Figure 3.7, the EVM is plotted as a function of the angle of incidence for different modulation depths, data rates and bandwidths, demonstrating the systemic increase in the EVM due to the narrowband approximation inherent in phased-array architectures. As will be shown in the next section, a method to mitigate the deterministic errors caused by the phase-shift approximation is to use orthogonal frequency division multiplication (OFDM), with normalization, to modulate the carrier signal.

3.4.1 OFDM-based Equalization Scheme

For a QAM signal at data rate R bps, modulated using a quadrature amplitude modulation (QAM) scheme with 2^M symbols, the time period of each symbol, T_s,

$$T_s = \frac{1}{MR} \tag{3.12}$$

Therefore, the complex digital baseband signal,s_d is,

$$s_d(nT_s) = b_n \tag{3.13}$$

where b_n is complex. In OFDM, the total bandwidth of the system is divided into N_c channels, with the N_c sub-carriers orthogonal. The baseband digital data is divided into N_c parallel streams, each of which is used to modulate a sub-carrier [63]. Thus, each OFDM symbol consists of N_c QAM symbols, and for each frame (of duration N_cT_s),

$$s_d(nT_s) = \sum_{k=0}^{N_c-1} b_k e^{j2\pi \frac{kn}{N_c}} \tag{3.14}$$

Since each of the channels in the OFDM scheme is narrowband, the distortion seen by the signal in any particular channel is constant and depends only upon the

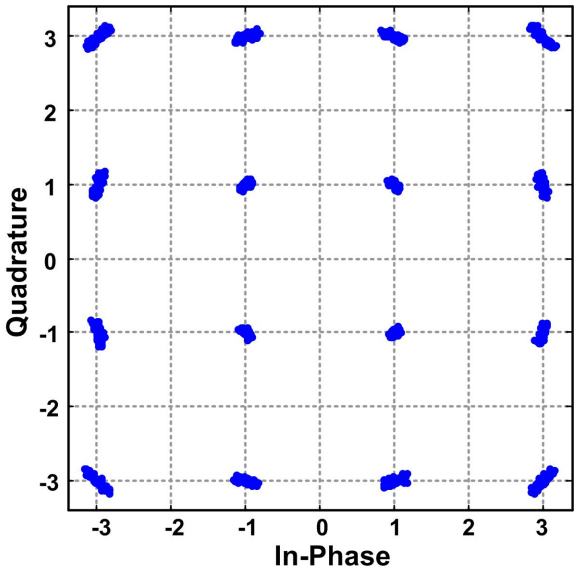


Figure 3.8: Phased array signal constellation for OFDM modulation; $\phi = 49°$ (Carrier_freq = 60GHz; Nelements = 8; Ncarriers = 64; Datarate = 5Gbps; 16QAM; Symbol Rate = 1.25Gbps; Rolloff = 0.5)

angle of incidence or radiation. This can be seen by the systematic nature of the distortion in the constellation shown in Figure 3.8. Hence, the error due to the time delay being replaced by a constant phase shift can be largely corrected by multiplying the input at each channel by a complex normalizing factor, a_k, such that,

$$s_d(nT_s) = \sum_{k=0}^{N_c-1} a_k b_k e^{j2\pi \frac{kn}{N_c}} \tag{3.15}$$

The memory-less pre-distortion coefficients, a_k, depend upon the direction of radiation which is known a priori in the transmitter or receiver. Figure 3.9 compares the EVM for a raw QAM modulation scheme and for a 64 carrier OFDM modulation scheme with complex normalization. The signal has a data rate of 5Gbps and a bandwidth of 3.75GHz. As can be seen in Figure 3.9, the EVM corresponding to a radiation angle of 45°, improves from 5.9% to 1.1%, demonstrating the efficacy of the normalized OFDM scheme. A larger number of subcarriers can be used to further decrease the EVM and compensate for higher bandwidth. Thus, careful

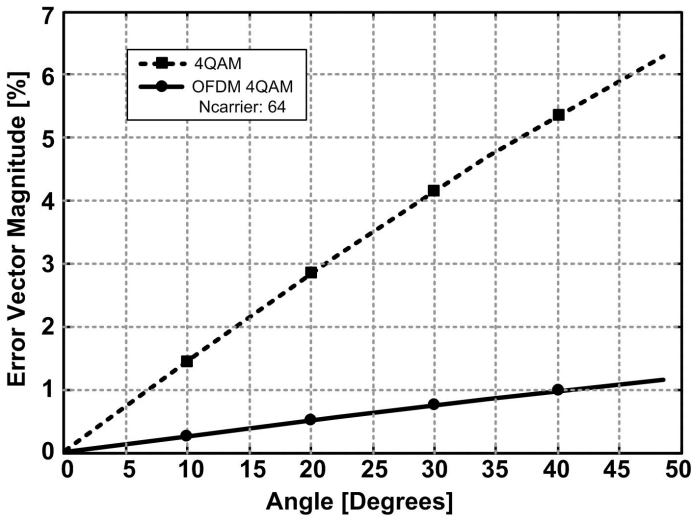


Figure 3.9: EVM improvement with OFDM-based equalization scheme (Carrier_freq = 60GHz; Nelements = 8; Ncarriers = 64; Datarate = 5Gbps; 4QAM; Symbol Rate = 2.5Gbps; Rolloff = 0.5)

choice of modulation schemes and simple equalization methods can render the implementation of actual analog or digital delay in each element unnecessary.

3.5 Chapter Summary

The large available bandwidths and reduced physical size at high frequencies makes mm-wave multiple antenna systems attractive. While a higher operating frequency implies higher noise and lower received signal power, a close examination of the tradeoffs indicates that for indoor and short distance communications, the large bandwidths make high bandwidths advantageous.

The tradeoffs of implementing such systems on silicon are discussed. Different phase-shift architectures are presented along with their suitability for integration in silicon. The effects of the narrowband approximation in phased arrays has been discussed in terms of the distortion in the signal introduced by it. The narrowband phase-shift approximation leads to an increased EVM at higher angles of radiation. This distortion, can however, be easily corrected with a careful choice of modulation

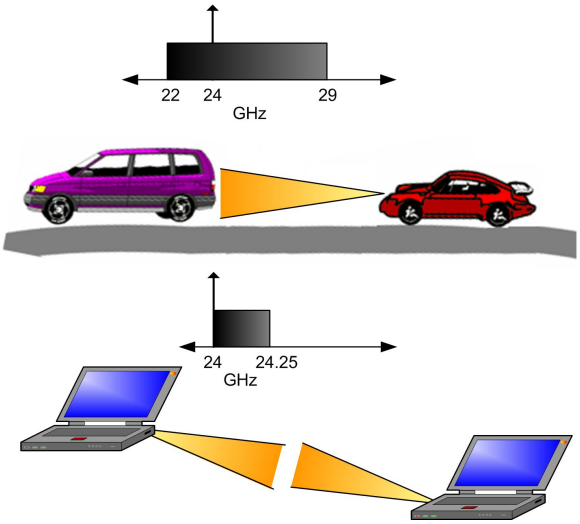
schemes and equalization methods as shown by the reduction in EVM achieved through an OFDM-based scheme.

Chapter 4

A 24GHz Phased-Array Transmitter in CMOS

The suitability of integrated phased arrays for sensing and high data rate communication applications motivates efforts to demonstrate such systems in commercial silicon technologies. CMOS process technologies are the most attractive among silicon-based technologies for integrated systems due to the benefits of scaling and the possibility of integrating the digital backbone with the RF front-end. However, the low active gain of MOS transistors and the lossy passives at high frequencies have prevented any significant movement toward integrating entire high-frequency phased arrays systems on CMOS technologies. The fully integrated four-element 24GHz phased-array transmitter, with on-chip power amplifiers, described in this chapter is not only the first fully-integrated phased-array transmitter but also the first system to demonstrate such levels of integration at 24GHz using largely 0.18μm CMOS transistors. This transmitter and the companion eight-element phased-array SiGe receiver [59] demonstrate the feasibility of 24GHz phased-array systems in silicon-based processes.

In the following sections, the system level and circuit level aspects in the design of the transmitter will be discussed in depth. Section 4.1 describes briefly the allocated spectrum at 24GHz. The architecture of the transmitter is presented in Section 4.2 while the design of key circuit building blocks are described in Section 4.3. The measurement results are presented in Section 4.4.



Vehicular Radar System
Bandwidth: 7GHz,
EIRP: -41.3dBm/Mhz → -3dBm [7GHz BW]
Radiation 30° above horizontal
attenuated by > 25dB

ISM Band: Wireless Communication
Bandwidth: 250MHz,
Field Strengh < 2.5V/m @3m distance
→EIRPavg = 26dBm
Antenna Gain > 33dB or Beamwidth < 3.5°

Figure 4.1: Spectrum allocation at 24GHz

4.1 Spectrum at 24GHz

The spectrum around 24GHz is appealing for both sensing and communication applications (Figure 4.1) as an Industrial, Scientific and Medical (ISM) band has been allocated from 24GHz to 24.25GHz for wireless point-to-point links and 7GHz of spectrum from 22GHz to 29GHz has been earmarked for vehicular radar systems [3]. Collision avoidance systems operating at these frequencies are expected to play a pivotal role in collision avoidance, assisted parking and automatic cruise control systems in automobiles [64, 65].However, there are users in the field of astronomy around 24GHz that are very sensitive to interference signals [66]. Therefore, the FCC, in addition to a spectral mask, has also specified spatial requirements such as antenna gain and placed limits on the power that can be radiated at angles higher than 30° above the horizontal plane [3].

Thus, in addition to the normally specified output power limitations, spatial directionality is also mandated for these applications (detailed in Figure 4.1). As has been shown in Chapter 2 and Chapter 3, phased-array transmitters provide an effective and flexible means to achieve both high output power and directionality requirements.

4.2 24GHz Phased-Array Transmitter Architecture

In this section, the architecture of the transmitter is discussed in depth. While the tradeoffs of various architectural choices for electronic phase shifting have been discussed in Chapter 3, this section focuses on the particular 24GHz phased-array transmitter implementation.

The four-element fully-integrated transmitter has on-chip power amplifiers as well as an integrated frequency synthesizer. Due to concerns related to frequency pulling, direct upconversion was considered to be unsuitable. A two-step upconversion architecture was chosen for the transmitter with LO frequencies of 4.8GHz and 19.2GHz (Figure 4.2). The two LO frequencies are generated by a single synthesizer loop using a divide-by-four.

Quadrature upconversion was implemented in both stages [67]. While the image attenuation of the first upconversion step depends upon the matching and quadrature accuracy, the image signal of the second upconversion step falls at 14.4GHz and is therefore attenuated not only by the quadrature architecture but also by the tuned stages at RF.

Figure 4.3 shows the architecture and floorplan of the four-element transmitter. In the signal path, the baseband I and Q signals are upconverted to 4.8GHz by a pair of quadrature upconversion mixers. The 4.8GHz I and Q signals are buffered and provided to the 4.8GHz-to-24GHz upconversion mixers in each element. The output of the mixers is amplified and differential to single-ended conversion is performed to drive the on-chip single-ended CMOS power amplifiers which are matched at the output to 50Ω.

In the LO path, the output of the 16-phase 19.2GHz VCO is provided to the phase selectors in each element. These phase selectors select the right phase of the

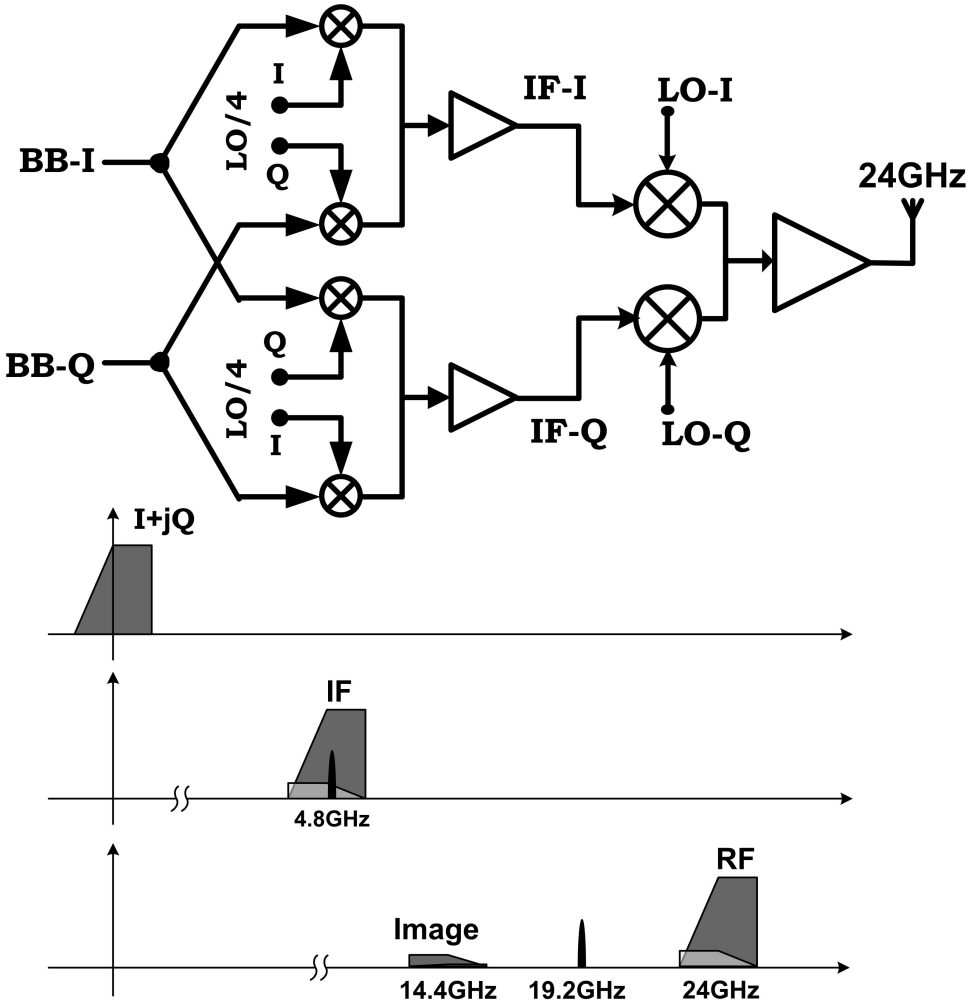


Figure 4.2: Equivalent architecture of a single transmitter element and frequency plan

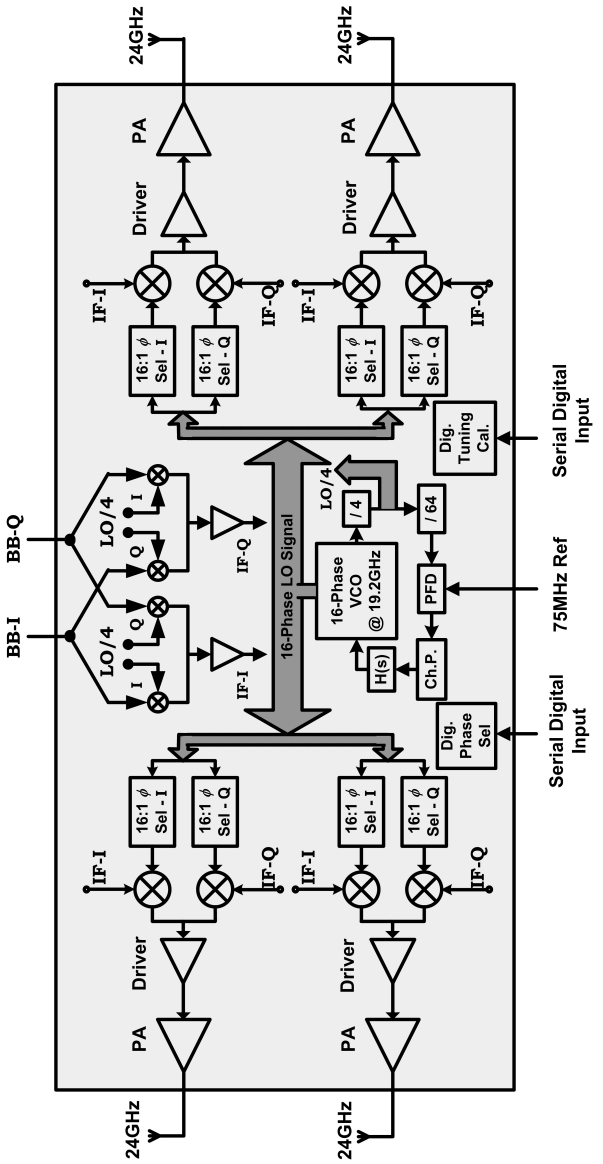


Figure 4.3: Architecture and floorplan of 24-GHz four-element phased-array transmitter

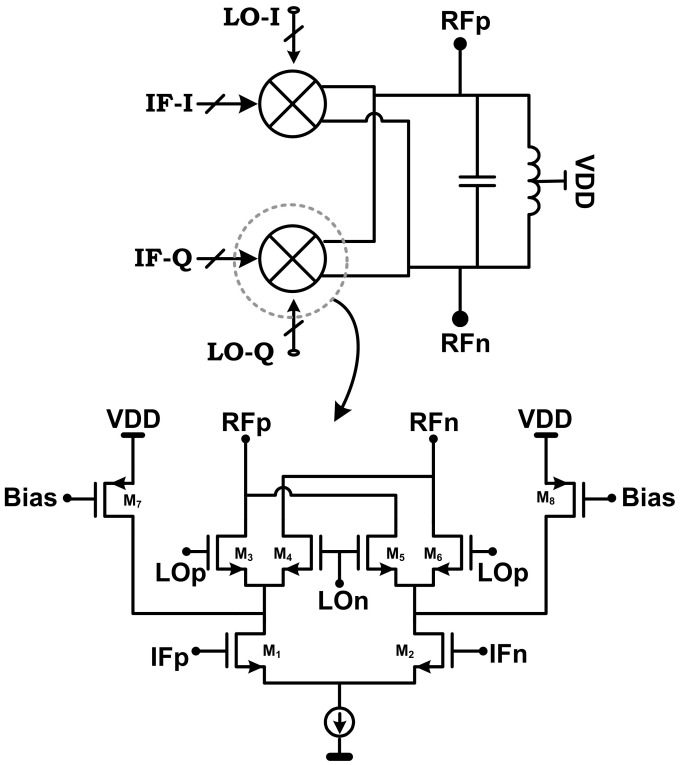
LO in each element for the desired beam direction. The phase-selection circuitry is controlled by shift registers that can be programmed using a digital serial interface, enabling electronic beam-steering. The VCO is part of an on-chip frequency synthesizer which generates the 19.2GHz LO signals from a 75MHz reference. A divide-by-four in the synthesizer loop generates the 4.8GHz LO I and Q signals for the first upconversion step.

4.3 Circuits in Signal Path and LO Path

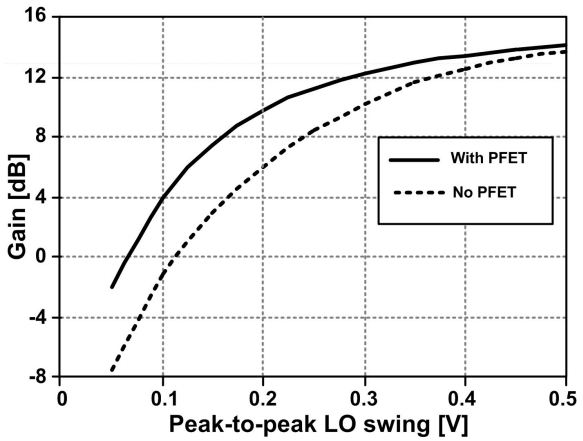
4.3.1 Circuits in Signal Path

4.3.1.1 IF and RF Upconversion Mixers

The Baseband-to-4.8GHz quadrature mixers common to all elements are Gilbert-type upconversion mixers. The first upconversion mixer consumes 3.8mA of dc current while the buffers following the mixer consume 4.3mA. The output of these buffers is distributed to the quadrature upconversion mixers in each element using a symmetric H-tree structure to ensure good array performance. Figure 4.4(a) shows the schematic of 4.8GHz-to-24GHz upconversion mixers in each element. These mixers are essentially Gilbert-type upconversion mixers with some of the dc current provided by the PFETs [68, 69]. The current in the IF transconductance part of the mixer (M1 and M2) needs to be high to improve mixer linearity and gain. However, the V_{GS} drop in the switching devices (M3, M4, M5, and M6) increases significantly with higher dc current and hence the amplitude of the LO needed to switch these transistors increases. Therefore, to increase the conversion gain at a given LO swing and to reduce the sensitivity of the conversion gain to the LO amplitude, part of the dc current (55%) is provided by the PFETs (M7 and M8), which reduces the dc current and, consequently, the V_{GS} drop across the switching devices. Figure 4.4(b) plots the simulated conversion gain of the quadrature mixers against LO amplitude for the same dc current in the IF transconductance part, with the PFETs and without the PFETs. It can be seen that the simulated quadrature

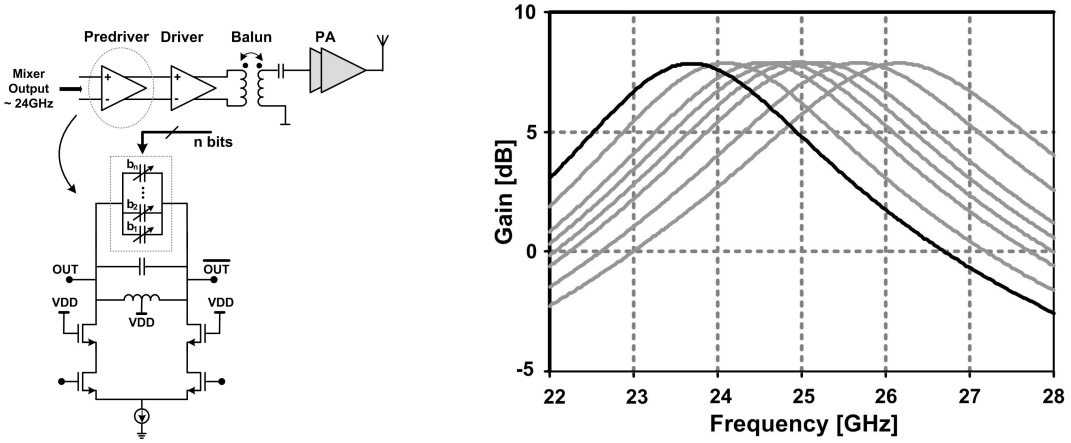


(a) Gilbert-type mixer with PFETs for current boosting



(b) Variation of gain with LO amplitude with and without current boosting

Figure 4.4: RF up-conversion mixers (4.8 to 24 GHz).



(a) Predriver stage with switchable capacitors in load

(b) Simulated change in center frequency with digital tuning control

Figure 4.5: Digital tuning calibration in high-frequency stages

conversion gain increases from 6dB to 9.7dB for 200mV peak-to-peak LO swing and is less sensitive to LO amplitude with the PFETs.

4.3.1.2 Tunable Passive Loads at 24GHz

The cascade of tuned stages in the RF path in each element exacerbates any off-tuning in the passive loads. To avoid the problem of gain loss due to off-tuning, switchable capacitors, controlled by programmable shift registers, were implemented at the output of some of the high frequency stages [Figure 4.5(a)]. In the pre-driver stage, for example, these capacitors allow the center frequency to be tuned from 23.5GHz to 27GHz which is sufficient to account for process variations and errors in simulation of passives [Figure 4.5(b)].

4.3.1.3 Balun

All the circuits up to and including the 24GHz PA driver are differential while the PA was designed to be single-ended. To avoid power and efficiency loss at the output of the PA, a balanced-unbalanced converter (balun) was placed before the PA. This eliminates the need for an off-chip balun or a differential antenna. As shown in Figure 4.6, the balun was realized with a single-turn transformer to

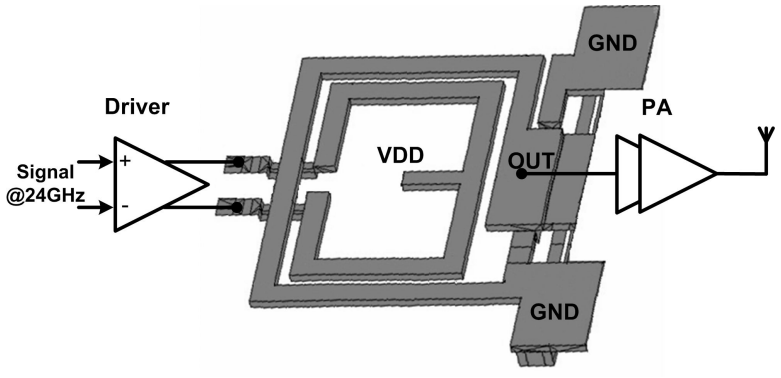
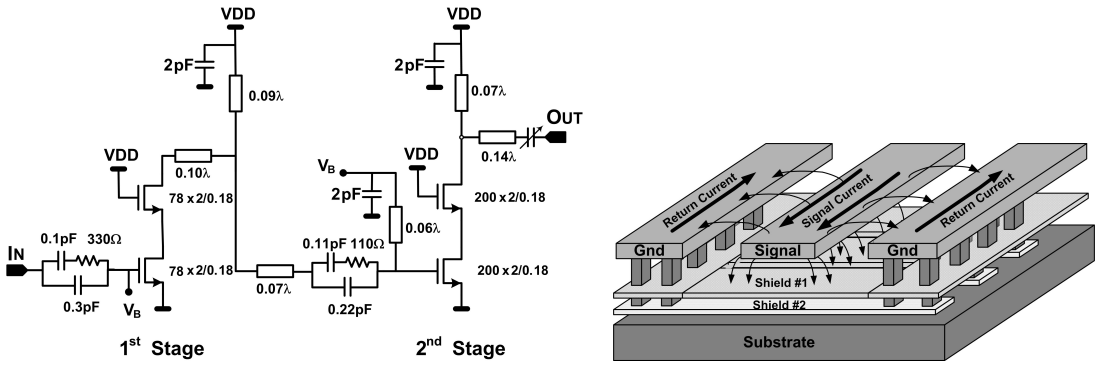


Figure 4.6: Balun for differential to single-ended conversion at PA input.

minimize substrate loss through capacitive coupling. Electromagnetic simulations show an insertion loss of 1.5dB for the balun when input and output parasitic inductances are tuned out with parallel capacitors [35].

4.3.1.4 Power Amplifier (PA)

The transmitter contains four on-chip power amplifiers matched at the output to 50Ω [70, 71]. The parasitic inductance of the balun is used to tune out the input capacitance in the first stage of the amplifier integrated in the transmitter. The PA has two gain stages with each consisting of a cascode transistor pair to ensure stability and increase breakdown voltage [Figure 4.7(a)]. The output and interstage matching networks in the PA are realized with the substrate-shielded coplanar waveguide structure shown in Figure 4.7(b) to reduce power losses and area [72]. In this structure, the presence of the ground shield beneath the coplanar signal line increases the capacitance per unit length, C_u. However, as the return current cannot flow through the patterned ground shield, the inductance per unit length, L_u, remains the same. The simultaneously high C_u and L_u result in lower wave velocity, leading to more than a factor of two reduction in wavelength at 24GHz when compared to a standard coplanar waveguide structure in silicon dioxide. Additionally, as the structure is well shielded, the isolation between the power amplifier and other circuits in the transmitter is improved. The low loss per unit length (1dB/mm), improved isolation, and short wavelengths make this structure



(a) Two-stage on-chip power amplifier.

(b) Substrate-shielded coplanar waveguide structure

Figure 4.7: On-chip power amplifier

particularly suitable for integrating multiple power amplifiers on the same die.

4.3.2 LO-Path Circuits

4.3.2.1 Multiple-Phase Voltage-Controlled Oscillator

The multiple-phase VCO, shown in Figure 4.8, is at the heart of the LO phase-shifting architecture adopted in this work. The 19.2GHz CMOS VCO consists of 8 differential amplifiers connected together in a ring structure and is similar to the design in [59]. As the ring is closed by flipping the inputs of the last amplifier, the VCO is capable of generating 16 equally spaced phases of the LO with a step size of 22.5^o [73].

The outputs of the VCO have to be provided to the phase selectors in each element in a symmetric fashion as any asymmetry in this distribution leads to an error in the phase shift causing degradation of the array pattern. Therefore, a symmetric H-tree structure, using the top two thick metal layers, is used to distribute the multiple VCO outputs.

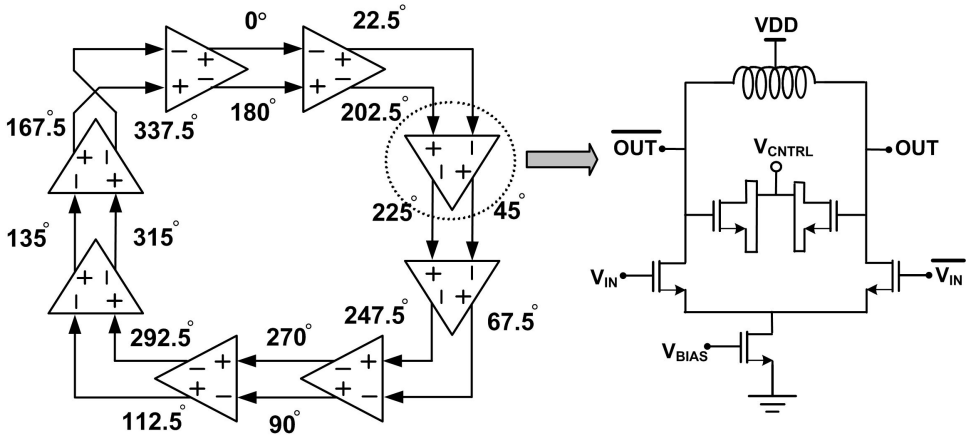


Figure 4.8: 19.2-GHz 16-phase CMOS VCO

4.3.2.2 Phase Selectors

The phase selectors in each element work in two stages. In the first stage, the 8 differential outputs of the VCO are provided to 3 sets of 8 differential pairs (Figure 4.9). The tail current of each differential pair is controlled by a shift register. The first two sets of differential pairs determine the I and Q LO signal while the third set is a dummy to ensure that the VCO buffers see a constant load. By turning on the right differential pair, the VCO differential pair outputs corresponding to desired LO phases for the I and Q can be selected independent of each other. While this provides flexibility to account for phase-distribution and device mismatches, in practice the LO distribution matching was sufficient to render independent selection superfluous. The tail current sources of the dummy set of differential pairs is controlled by bits complementary to the LO I and Q phase selection bits to ensure constant loading of the VCO buffers. The eight differential pairs (six dummy, one I and one Q) that are turned on for any given phase shift, draw a total of 16mA from a 2.5V supply.

The next stage of the phase selectors consists of a set of two differential pairs with tail current sources that are also controlled by the shift registers (Figure 4.9). The inputs to the differential pairs are anti-phase with respect to each other. Thus the output can either be in-phase or anti-phase with respect to the input. The

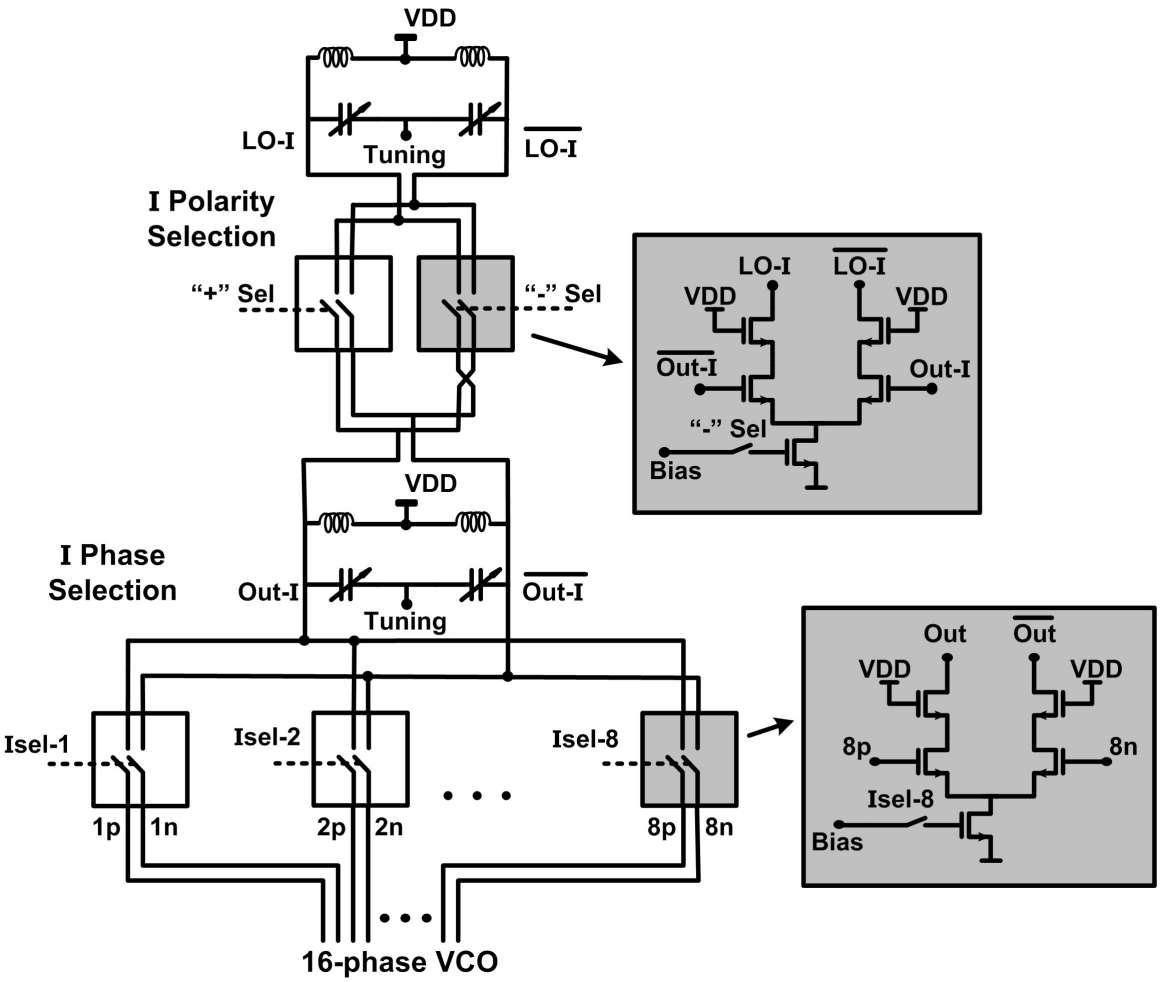


Figure 4.9: Two-stage phase selector

differential pairs in the second stage of phase selection draw 3.1mA each.

Interpolation of the raw 16 phases of the VCO is possible by selecting more than one differential pair in the first stage of the phase selector. (The two-stage phase selection procedure, limits the phase shifts that can be generated by using this interpolation method). For example, by selecting the 0^o phase and the 22.5^o phase output, the output has a phase of 11.25^o. Selecting more than two differential pairs provides even finer resolution.

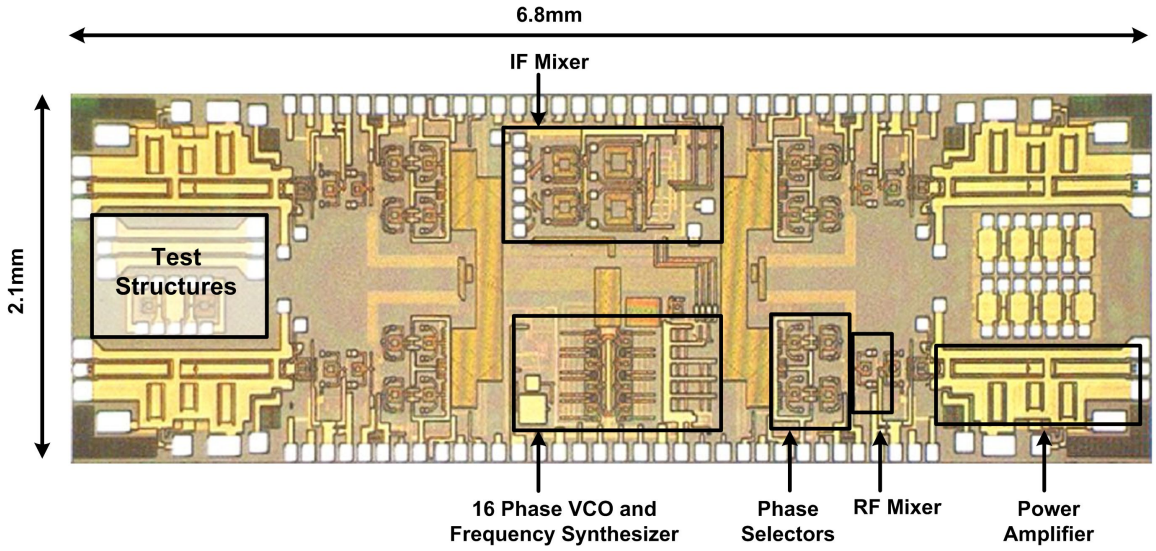
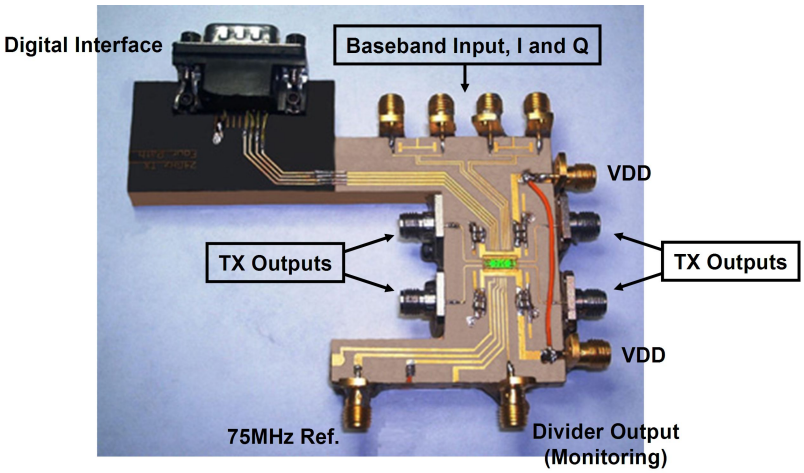


Figure 4.10: Die micrograph of 24-GHz four-element phased-array transmitter

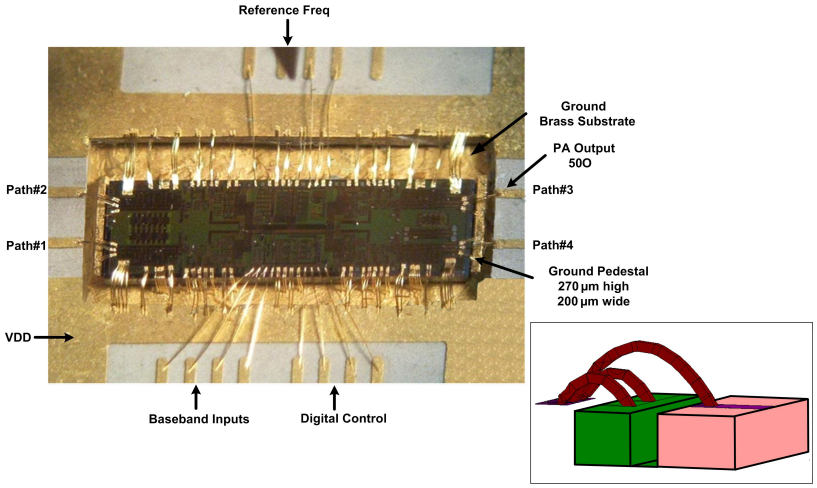
4.4 Measurement Results

The phased-array transmitter has four elements and is implemented using mainly 0.18μm CMOS transistors in a BiCMOS process [74]. The f_t of the NMOS transistors in the process is 65GHz. The process offers 5 metal layers with the thickness of the top two metal layers being 4μm and 1.25μm. Figure 4.10 shows a die photograph of the transmitter which occupies 6.8mm x 2.1mm of die area.

A high-frequency printed circuit board (PCB) measurement setup has been designed to characterize complete system performance. Some of the packaging parasitics, such as wirebond inductance, have been taken into account during circuit design. Figure 4.11(a) shows the measurement setup for the transmitter chip. The PCB is a high-frequency laminate that is compatible with planar antenna design and is supported by a brass substrate that acts as the ground. Two ground pedestals are milled on the brass substrate and the chip is mounted on the substrate, between the pedestals, using silver epoxy as shown in Figure 4.11(b). By wirebonding the PA ground pads onto the pedestals, the length and therefore the inductance of these wirebonds is reduced. The height of the PCB (10mil dielectric thickness) is chosen to be close to the height of the chip ($\approx 350\mu m$) to reduce the length of the



(a) 24GHz 4-path test PCB



(b) Close-up of area around chip

Figure 4.11: Measurement setup to characterize transmitter performance

wirebonds to traces on the PCB. Figure 4.12 shows the output matching of each element of the transmitter when measured by probing and by wirebonding the output to the PCB. Though the match with wirebond is more narrowband, there is better than 10dB match from 23.4GHz to 24.1GHz. A broader frequency range for matching can be achieved by using flip-chip packaging techniques.

Figure 4.13 summarizes the performance of the on-chip power amplifiers, which are capable of generating up to 14.5dBm output power at 24GHz with an output-referred 1dB compression point of 11dBm. The coupling between multiple

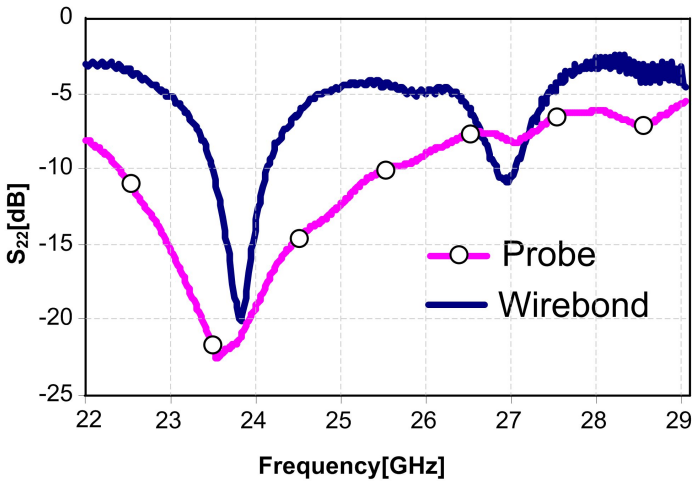


Figure 4.12: Output matching with probe-based testing and with wirebonds to PCB

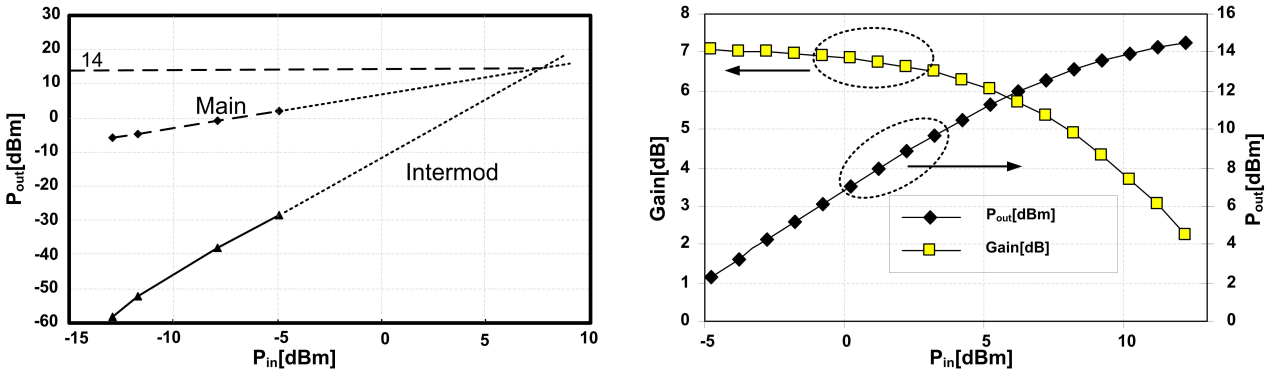


Figure 4.13: Performance of on-chip 24-GHz CMOS power amplifier

power amplifiers on the same die is a concern in an integrated phased array. The physical distance (∼1mm) between the power amplifiers and the use of shielded transmission line in the matching networks improve the isolation in this work. In order to measure the isolation between elements, three of the elements were switched off by switching off all the LO phases in the phase selectors in those elements. The isolation was determined by comparing the power at the output of the active element with the output power of the three inactive elements. The worst-case isolation (i.e., between two adjacent elements) is measured to be 28dB. The isolation between the other elements is better than 30dB.

The image rejection of the first upconversion stage, which depends upon the quadrature matching of the mixers and the first LO, is 24dB. The image signal of the second upconversion step, which falls at 14.4GHz, is found to be attenuated by 43dB due to the additional attenuation provided by the tuned stages at RF.

To measure the performance of the transmitter alone, without antenna non-idealities such as coupling, the different propagation delays for each element for each direction of radiation have to be replicated. This is done by connecting the output of each element to variable phase shifters (Figure 4.14). By varying the relative phase shift in the external phase shifters, the propagation delays for each beam direction can be emulated. The output of the phase shifters is combined and measured using a spectrum analyzer or a power meter. Figure 4.15 shows the measured array pattern of the transmitter with two elements active for different phase-shift settings. Figure 4.16 compares the measured performance of the transmitter with two elements active and with all four elements active to theoretically expected results. When compared to theory, these results demonstrate the proper functioning of the phased-array transmitter. The worst-case peak-to-null ratio with all four elements active is 23dB.

While the PA has a bandwidth of 3.1GHz, the bandwidth of the entire transmitter is constrained by the bandwidth of the IF stages and also by the cascade of tuned stages at IF and RF. Figure 4.17, which shows the measured spectrum of the transmitter when a 100Mbps and 500Mbps QPSK signal is provided at baseband, indicates that the transmitter is capable of supporting high data rates. To measure the performance of the transmitter for high data rate input, an external direct downconversion receiver was assembled, consisting of a passive mixer followed by an amplifier (Figure 4.18). For this measurement, the LO signal that is used for downconversion needs to be locked to the carrier signal of transmitter. Therefore, the 24GHz LO signal to the external mixer is divided by 320 to generate the 75MHz reference for the on-chip frequency synthesizer. The baseband input was provided to

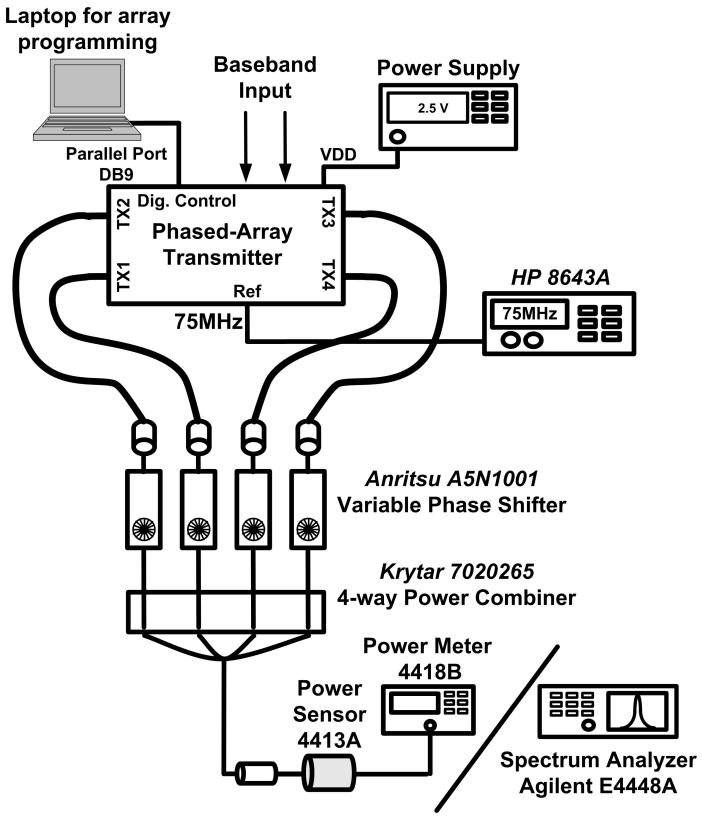


Figure 4.14: Array measurement setup

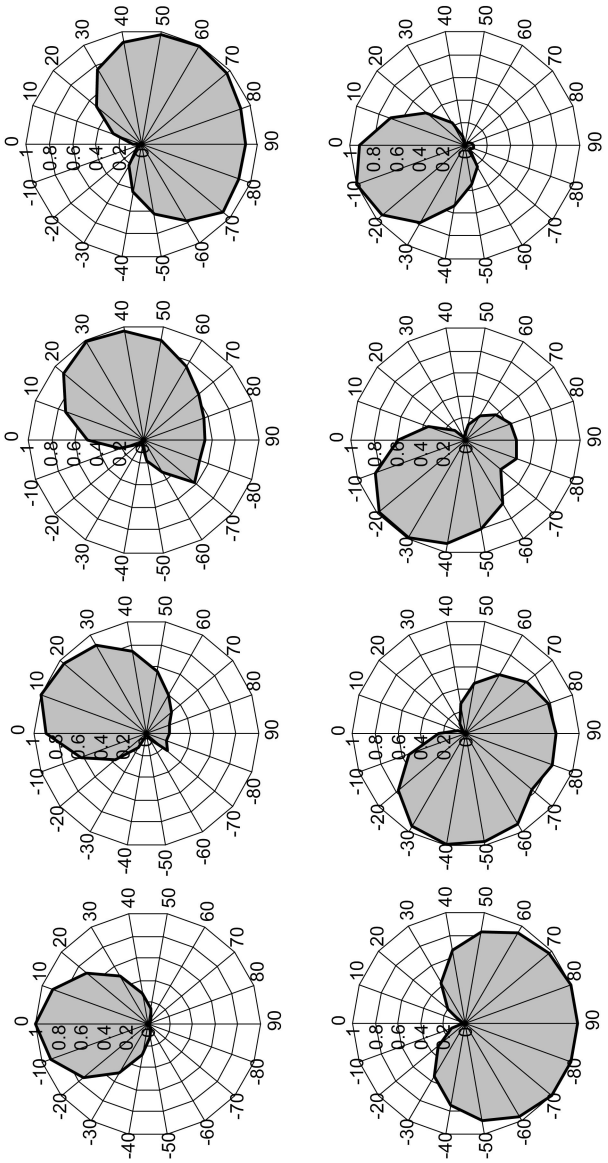


Figure 4.15: Measured array patterns with two elements active

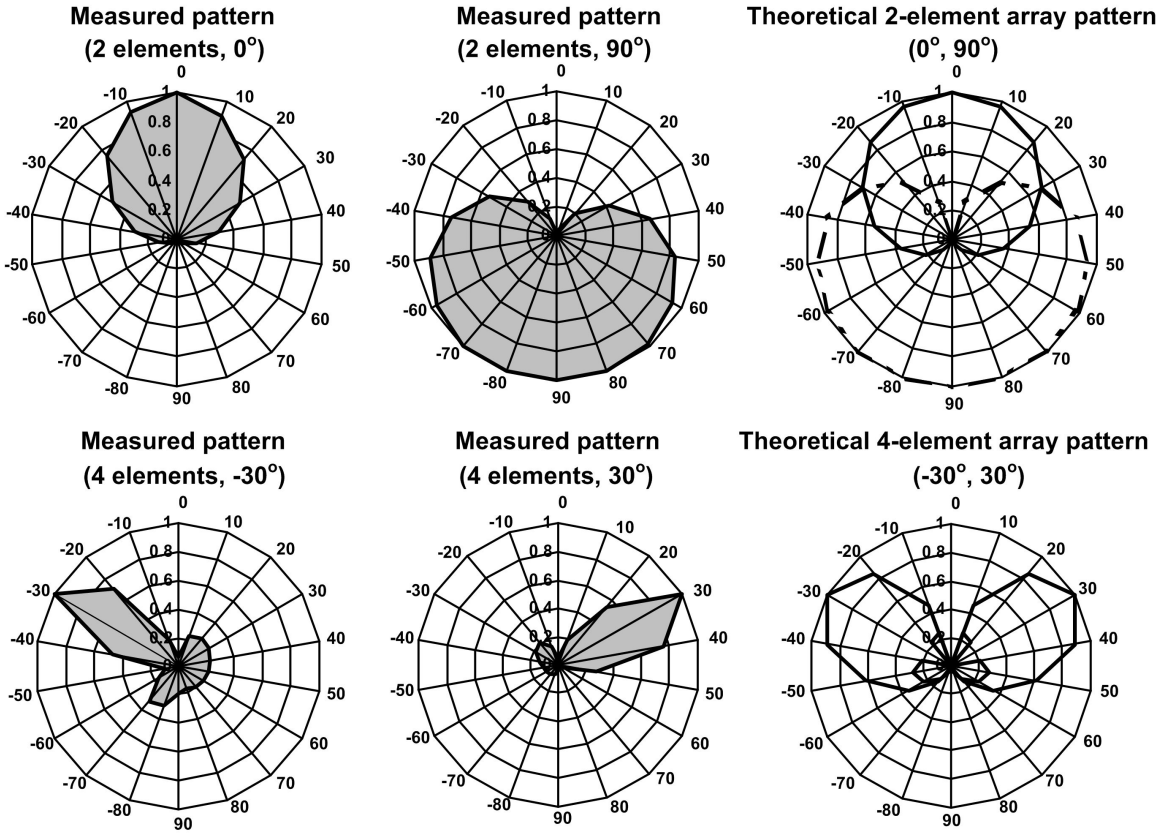
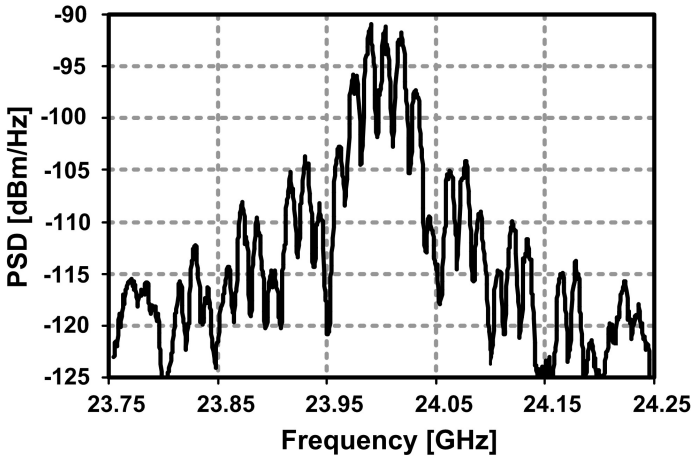
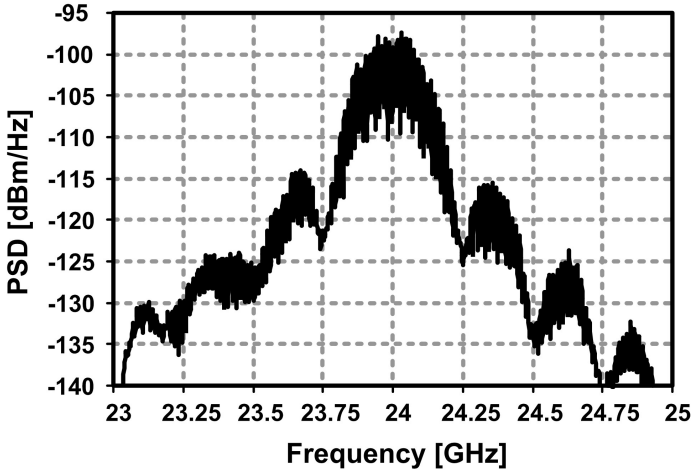


Figure 4.16: Comparison of theoretical and measured array pattern with two elements and with four elements active



(a) Output spectrum for 100-Mb/s QPSK input



(b) Output spectrum for 500-Mb/s QPSK input

Figure 4.17: Output spectrum of transmitter for 100- and 500-Mb/s QPSK input

one channel using a pseudo-random bit-pattern generator and no pulse-shaping was done at the input to minimize ISI. Figure 4.19 plots the eye diagram for the downconverted baseband output for 250Mbps and 500Mbps BPSK signal. The measured EVM did not increase significantly with an increase in data rate, indicating that it is dominated by the noise in the external downconversion setup.

The entire system with four on-chip power amplifiers draws 788mA from a 2.5V supply. The measured performance of the chip is summarized in Figure 4.20.

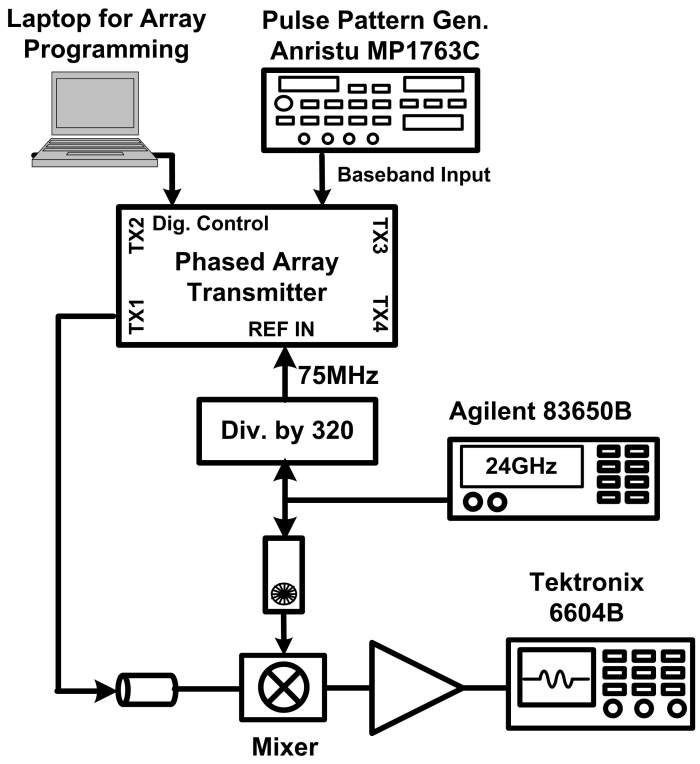
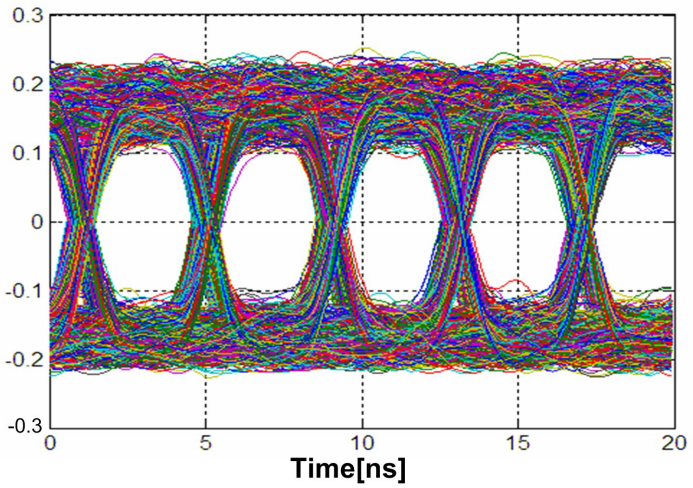


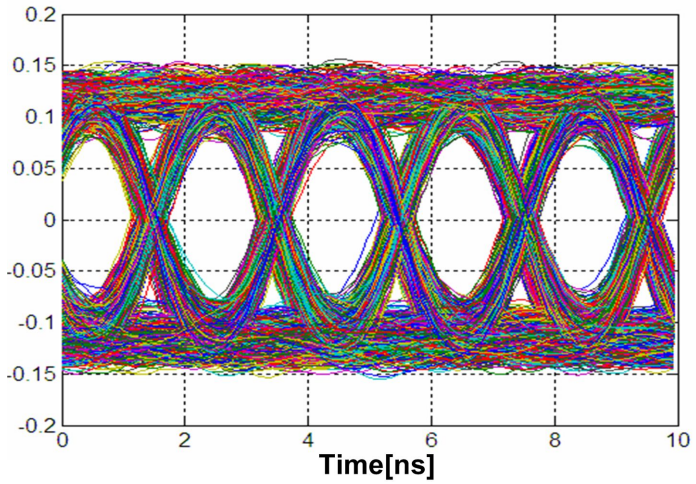
Figure 4.18: Setup for direct down-conversion of 24-GHz transmitter output

4.5 Chapter Summary

In this chapter, the first fully-integrated phased-array transmitter has been demonstrated using mainly 0.18μm CMOS transistors, proving the feasibility of high-frequency integrated phased arrays on silicon-based processes. The 4-bit LO-path phase-shifting approach adopted in the transmitter has better than 10° beam-steering resolution for radiation normal to the array. Each on-chip PA is capable of generating up to 14.5dBm output power, translating to an EIRP of 26.5dBm. The transmitter is capable of supporting data rates in excess of 500Mbps, and is well-suited for 24GHz wireless links. While the multiphase VCO based LO-path phase shifting scheme intrinsically provides uniformly spaced LO phases, it was found to be susceptible to errors due to coupling in the distribution network and it does not allow for calibration and correction abilities. Furthermore, scaling for larger number of elements and higher operation frequency is challenging. Hence, a more robust architecture based on a local LO-path phase shifting scheme was



(a) Single-channel 250 Mb/s (only to I channel):EVM = 9.7%



(b) Single-channel 500 Mb/s (only to I channel):EVM = 9.8%

Figure 4.19: Eye diagram of the down-converted transmitter output for 250- and 500-Mb/s BPSK input

On-Chip CMOS Power Amplifier Performance	
Maximum Saturated Output Power	+14dBm
Current Consumption @ 2.5V	68mA
Output Match @ 24GHz	-20dB
Equivalent 4-element EIRP	+26dBm
Output Referred 1dB compression point	11dBm
Peak PAE	6.5%
Output 3rd-order Intercept Point (OIP3)	14dBm
Phased Array Performance	
Peak-to-Null Ratio for 4-element Array	> 23dB
Beam Steering Resolution (for normal radiation)	< 10^{o}
3dB Array Beam-Width @ 30° Radiation Angle	17^{o}
Isolation between Paths (including wire bonds)	> 28dB
Image Signal Attenuation	
First upconversion	> 24dB
Second upconversion (image @ 14.4GHz)	> 43dB
Transmit 3dB Bandwidth	> 400MHz
Current Consumption @ 2.5V	
Signal Path (per element)	26mA
Phase Selector (per element)	34mA
16-Phase Frequency Synthesizer	180mA
Total (including IF stage and VCO buffers)	788mA
Device Technology	0.18µm CMOS
Die Area	6.8mm x 2.1mm

Figure 4.20: 24GHz Phased-array transmitter performance summary

adopted for the integrated 77GHz phased-array transceiver presented in the next chapter.

Chapter 5

An Integrated 77GHz Phased-Array Transceiver

The potential of mm-wave frequencies for sensing and commercial applications has long been recognized [24, 75, 76]. For example, studies have concluded that even a small increase of 2 seconds in the time the driver has to react, leads to a drastically lowered probability of collision in common driving situations (Figure 5.1 from [77, 78]) [79]. The possibility of reducing accident casualties, when allied with the scenario of collision-warning sensors being present in every automobile, makes mm-wave based automotive radar systems compelling from both humanitarian and commercial perspectives.

While radar-based systems are finding their way into high-end automobiles [65], the high cost of module-based systems has prevented widespread commercial introduction. These modules have been implemented using III-V semiconductor based HEMT transistors [80–83]. Silicon integration bypasses many of the yield and packaging challenges faced in GaAs modules [78, 84, 85], enabling low-cost mm-wave sensors. Building blocks such as VCOs [86], PAs [87] and LNAs [88], and mixers [89] have been demonstrated in silicon at mm-wave frequencies. As mentioned in Chapter 3, while the performance metrics of individual silicon components such as output power and noise figure can be poorer due to scaling and due to the material properties of silicon, they can be overcome by adopting more complex systems that are amenable to integration.

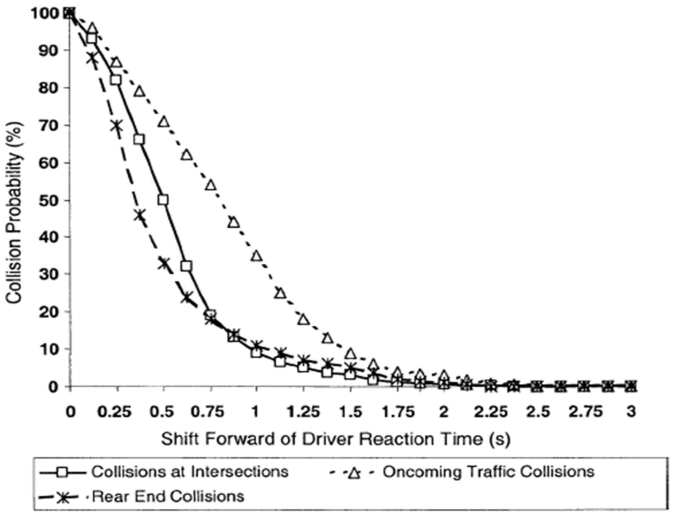


Figure 5.1: Reduction in collision probability with an increase in driver reaction time for different crash situations)

In this chapter, the first fully-integrated SiGe 77GHz four-element phased-array transceiver is described [60, 90]. The transceiver includes four on-chip transmit and receive elements (including 77GHz PAs and 77GHz LNAs) and adopts a local LO-path phase-shifting architecture that scales well with an increase in number of elements and/or frequency while providing high-resolution phase shifts. Section 5.1 presents a brief summary of some of the specifications in the 77GHz band. The architecture of the transceiver is discussed in Section 5.2 with an emphasis on the local LO-path phase-shifting scheme. While the transmit and LO-path circuits in the 77GHz transceiver are described in Section 5.3, a description of the receiver circuits and on-chip dipole antennas can be found in [90–92]. The measurement results of the transceiver are presented in Section 5.4. It must be noted that though the system demonstrated in this chapter functions at 77GHz, similar architectures and techniques can be applied at other mm-wave frequencies of interest such as the communication bands at 60GHz and 75-85GHz and the imaging band at 94GHz.

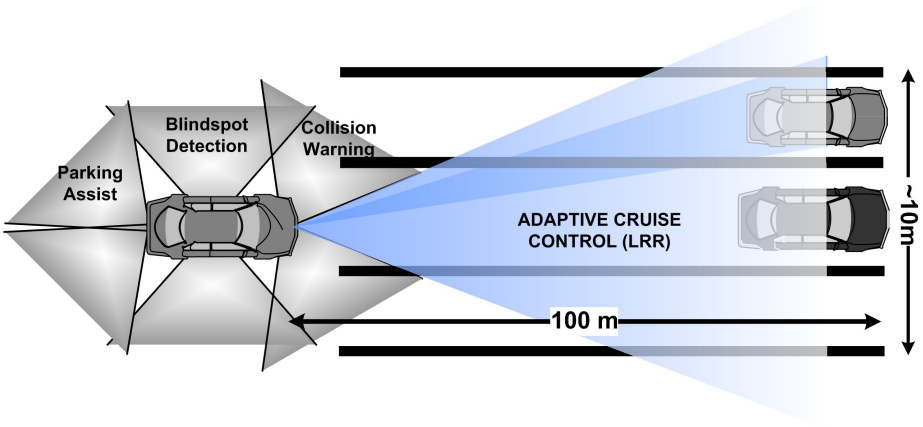


Figure 5.2: Collision-avoidance radar in automobiles

5.1 The Spectrum at 77GHz

The high carrier frequency and larger bandwidth available in mm-wave systems leads to a decrease in physical size and increase in resolution for radar-based sensors. Such sensor systems mounted aboard vehicles are expected to play a major role in reducing accidents and improving automotive safety through collision warning, brake assist, blindspot detection, adaptive cruise control(ACC) and parking assist [65, 93, 94] (Figure 5.2 from [65]).

In the case of automotive radar, the radar systems are divided into long-range radar (LRR) and short-range radar (SRR) based on the range of the objects that they are attempting to detect. LRR systems operate between 76-77GHz and are targeted primarily at ACC applications where the radar system detects the distance to the car ahead and maintains a safe separation. SRR systems are intended to provide more active safety features by detecting objects and other vehicles within a range of 30m [65]. A survey of historical the development of automotive radar has been published [95].

Though SRR systems are permitted to operate at 24GHz, in the near future these systems will have to transition to 76-81GHz due to concern over frequency bands

near 24GHz that are used for sensitive measurements in astronomy [3, 66, 96]. While ACC systems require beams to have 1° beamwidths and a scanning range of ±10° in the azimuth, larger scanning ranges of ±80° would be necessary for collision-avoidance applications [65]. The gain pattern of a phased array is the product of the individual antenna patterns and the array pattern for the particular phase setting. Since it is challenging to implement antennas with beamwidth as high as 160°, such a system would probably have to employ atleast two subarrays, each scanning a part of the incidence plane. In order to get accurate bearing of the objects, the beamwidth has to be of the order of 5°. A conservative beamwidth of 3° in the azimuth and elevation planes calls for 36dBi system directivity. Splitting this directivity evenly between the transmitter and receiver leads to a 18dBi directivity requirement in the transmitter. A single transmitter with a highly directive antenna limits the scanning range whereas in a phased array the required directivity can be partitioned between the array gain and the directivity of the antennas, thereby permitting beam scanning. For a phased-array with n elements, the directivity is $10\log(n)$ dBi, which translates to 12dBi directivity for a 16-element array. Such a phased array coupled with planar antennas with directivity 6dB, leads to sufficient system directivity.

One of the major challenges with integration at mm-wave frequencies is the generation of sufficient output power. As shown in Chapter 3, the lower breakdown voltages of the SiGe transistors constrain the output power of PA to be lower than their III-V transistor-based PAs. PAs with output powers greater than 26dBm have been demonstrated in GaAs and InP at 62GHz and 95GHz [97, 98]. Achieving similar EIRP with silicon technologies requires power combining schemes, such as the spatial power combining that occurs in phased arrays. If each element in the array can generate up to 17dBm [99], the EIRP for a four-element array is 29dBm. The EIRP can be further increased by increasing the antenna gain in the elevation plane, as the gain in the elevation plane does not affect the scanning in the azimuthal plane.

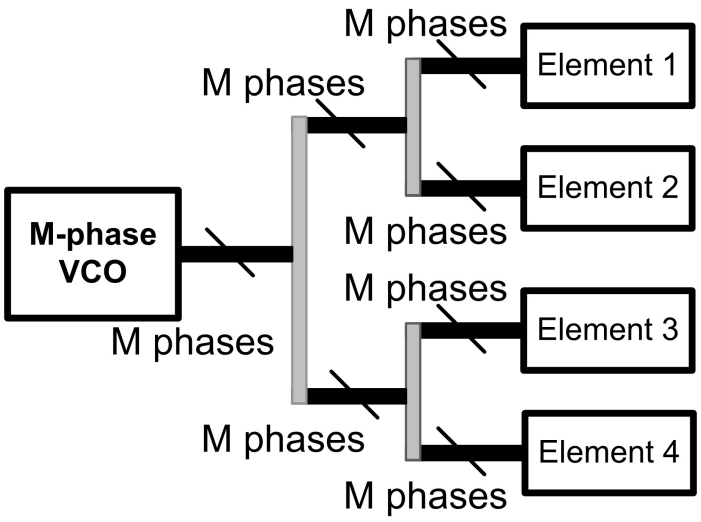


Figure 5.3: Centralized LO-path phase shifting

5.2 System Architecture

5.2.1 Local LO-Path Phase Shifting

In the integrated phased-array receiver and transmitter designs introduced in [59] and Chapter 4, a centralized LO-path phase-shifting scheme was adopted in which an m-phase VCO generates multiple phases of the LO, as shown in Figure 5.3. These multiple phases are then distributed to the phase selector in each element which selects the appropriate phase of the LO for the desired beam direction. One limitation with this approach stems from the fact that the phase resolution is limited by the number of phases generated by the VCO. Another limitation, more important at mm-wave frequencies, arises from the necessity to distribute all the LO phases to each element since the distribution of a large number of LO phases precludes a power-matched, buffered LO-phase distribution network with transmission-line (t-line) interconnects and matched LO buffers. As a result, the centralized scheme is unsuitable for an array operating at high frequencies and/or having a large number of elements, since such arrays would require a larger distribution network with intermediate buffering.

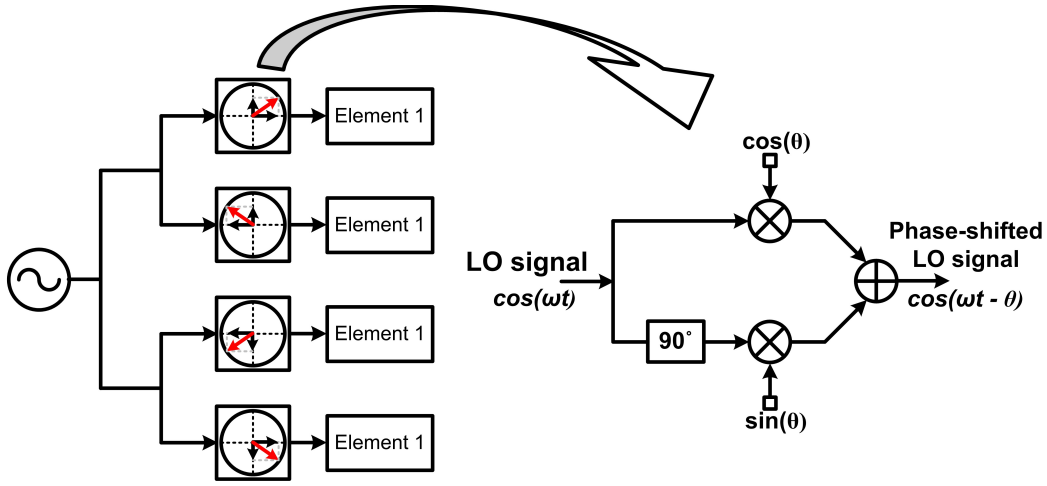


Figure 5.4: Local LO-path phase shifting

The above-mentioned limitations of the centralized phase-shifting scheme dictated the move to the *local* LO-path phase-shifting architecture adopted in this system. In this architecture (shown in Figure 5.4), the output of a single-phase VCO is distributed to the phase rotator in each element through a buffered binary-tree distribution network. The use of power-matched buffers ensures an LO signal with sufficient amplitude at the phase rotator input. The phase rotator in each element generates the LO quadrature phase locally and then interpolates between the in-phase (I) and quadrature-phase (Q) LO signals to generate the desired phase shift in each element. From the detailed description of the phase rotator circuitry, presented in [60], it can be seen the phase shift resolution in this approach depends primarily upon the resolution of interpolator weights which can be generated with high-resolution by DACs. This increased resolution can also be used to improve phase matching between different elements through calibration procedures.

5.2.1.1 Beam Jitter due to Phase Noise

In addition to the resolution of the weights, the resolution of a LO-path phase-shifting architecture is also limited by the phase noise of the LO signal as the phase setting in each element is affected by LO phase noise which translates to jitter in the beam direction. An estimate of this degradation can be obtained from a

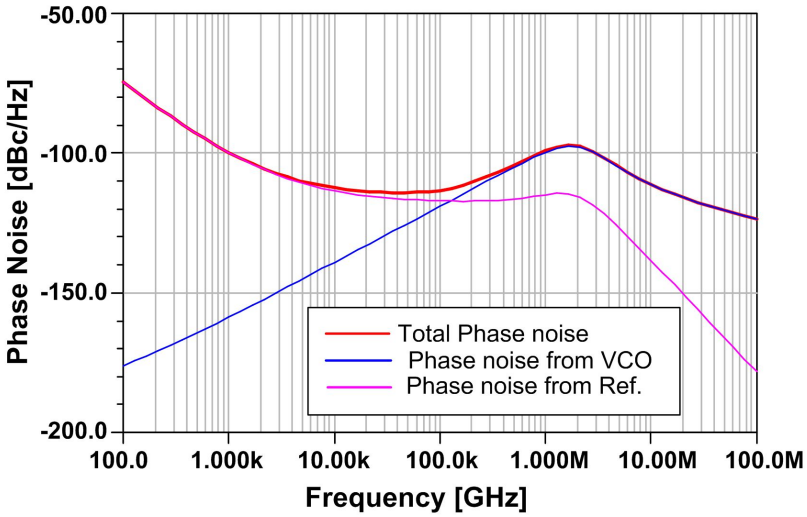


Figure 5.5: Typical phase noise of 52GHz synthesizer (based on implemented 52GHz VCO)

sample 50GHz synthesizer phase noise plot shown in Figure 5.5. The output of the phase rotator is a weighted combination of the LO signal and a delayed version of it. Ignoring the effect on phase noise of the correlation induced by this weighted combination, the rms jitter in the phase setting is given in radians by,

$$\langle \theta^2(t) \rangle = 2 \int_{fmin}^{\infty} 10^{L(f)} \tag{5.1}$$

where $L(f)$ is the phase noise of the closed loop synthesizer in dBc/Hz. For the sample synthesizer plot in Figure 5.5, with $fmin = 100$Hz the rms jitter in the phase setting in each element is 2.9°.

5.2.2 Transceiver Architecture

The 77GHz phased-array transceiver has four transmit-receive elements and includes on-chip LO generation and phase-shifting circuitry that are shared between the receiver(RX) and the transmitter(TX). It is important to note that each transmit and receive element includes an independent phase rotator that applies the desired phase of the LO to the upconversion or downconversion mixer in that element.

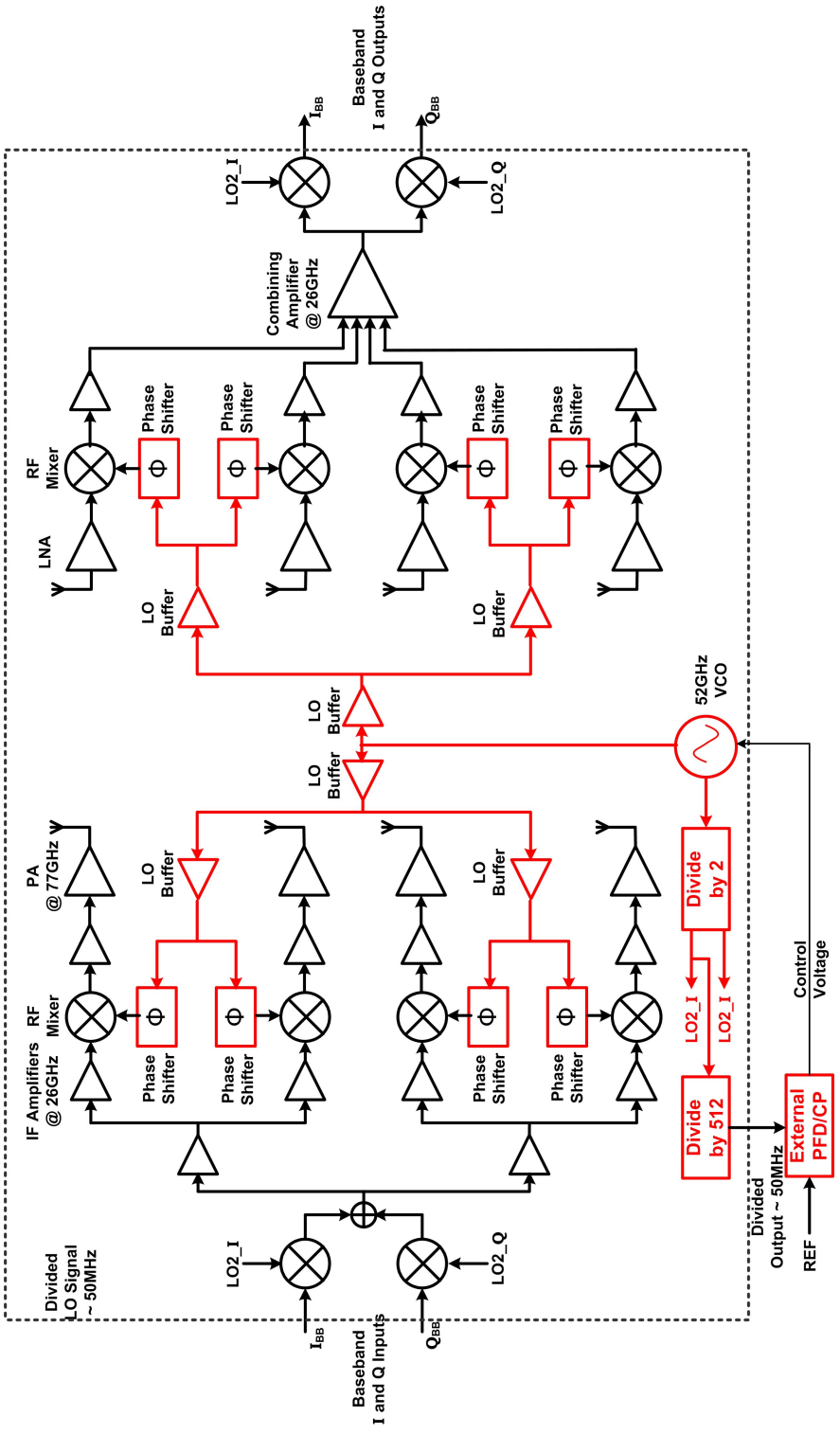


Figure 5.6: Architecture of 77GHz phased-array transceiver

The architecture of the transceiver is shown in Figure 5.6. The transmitter and receiver utilize a two-step upconversion/downconversion scheme with an IF frequency of 26GHz. The on-chip VCO generates the 52GHz LO signal necessary for the second upconversion in the TX (and for the first downconversion in RX) while the quadrature 26GHz signal required for the first upconversion (and second downconversion in RX) is provided by a quadrature injection-locked divide-by-two following the VCO.

In the LO path, the output of the differential, crosscoupled 52GHz VCO is distributed to the phase rotators in each element through a symmetric network of distribution buffers that ensures that the phase of the LO signal is the same at the input of the phase rotator in all transmit elements and in all receive elements. A cascade of divide-by-two frequency divider blocks following the VCO generate the 50MHz signal that is used by an off-chip PFD to lock the VCO.

5.2.2.1 77GHz Phased-Array Transmitter

In the transmit signal path, the baseband signals are upconverted to 26GHz by a pair of quadrature upconversion mixers. The signal distribution to all the elements is done at IF through a network of distribution amplifiers. The RF mixer in each element upconverts the 26GHz input signal to 77GHz, providing the input for a driver that feeds on-chip 77GHz power amplifiers. The adopted frequency plan leads to the undesired product of the second upconversion falling at 26GHz while the RF is at 77GHz. The tuned mixer, driver and power amplifier (PA) stages provide sufficient attenuation at 26GHz, therefore the second upconversion does not employ quadrature upconversion.

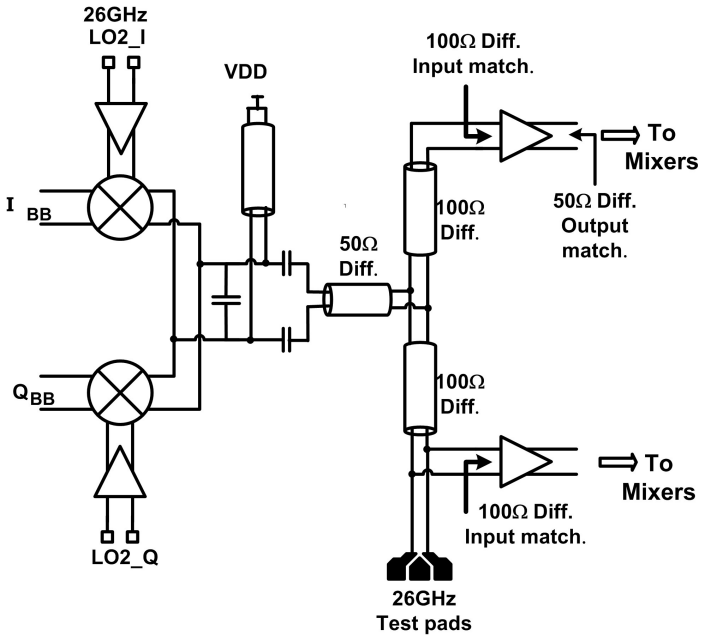


Figure 5.7: 26GHz upconversion stage

5.3 Circuits in Transmit and LO Paths

5.3.1 IF Stage

The baseband to IF upconversion is achieved using Gilbert-type quadrature upconversion mixers with a shorted t-line as load (Figure 5.7). As the mixers drive a pair of IF distribution buffers that are input-matched to 100Ω differential, the output impedance of the mixers is designed to be 50Ω differential to provide maximum power into the distribution network. The mixers and the buffers draw 46mA from a 2.5V supply.

The multiple elements present on the same die in an integrated phased array result in on-chip interconnects that are up to 1.5mm in length. At the LO frequency of 52GHz, this represents 0.53λ. Therefore interconnect modeling is critical and adoption of t-line based interconnects, that are easily and reliably modeled, dramatically simplifies the design effort. The t-line structure adopted in this system is shown in Figure 5.8. The presence of the ground shield improves the isolation

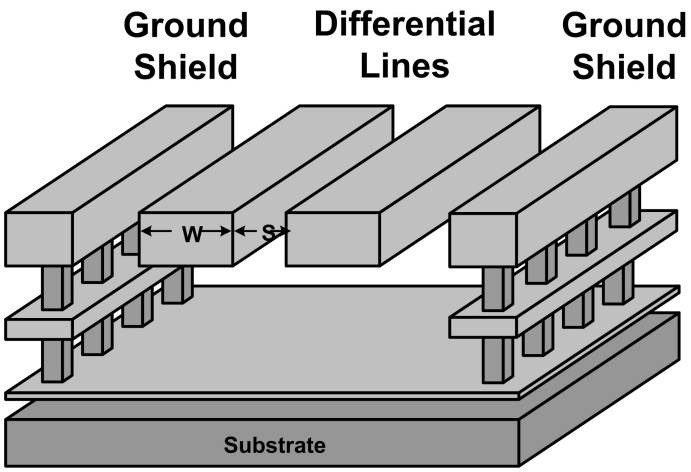


Figure 5.8: Shielded microstrip t-line structure

between adjacent t-lines by 20dB, which is important given the number of signal t-lines in the integrated transceiver.

While t-lines simplify modeling, the design is still heavily floorplan dependent as the load impedances are a strong function of interconnect length. This dependency can be eliminated by conjugate-matching each circuit block at the input and output to the t-line interconnects, thereby ensuring that the load impedances are independent of the floorplanning. However, it must be noted that this separation of design and floorplanning is achieved at the cost of bandwidth. For a simple shunt-series t-line matching network, the bandwidth depends upon the transformation ratio which can be high, as the range of impedances achievable with on-chip t-lines for reasonable layout parameters and acceptable loss is limited to 65Ω. While this reduction in bandwidth can be desirable for some applications, it can pose problems for broadband applications. This challenge can be overcome by reducing the quality-factor (Q) of the tuned loads or by using higher-order matching networks [30]. In the transmitter, the Q of the tuned loads was chosen such that the system had a bandwidth of 2.5GHz. Furthermore, the characteristic impedance of t-line interconnects was generally chosen to be 50Ω to allow for probe-based measurements at internal test points.

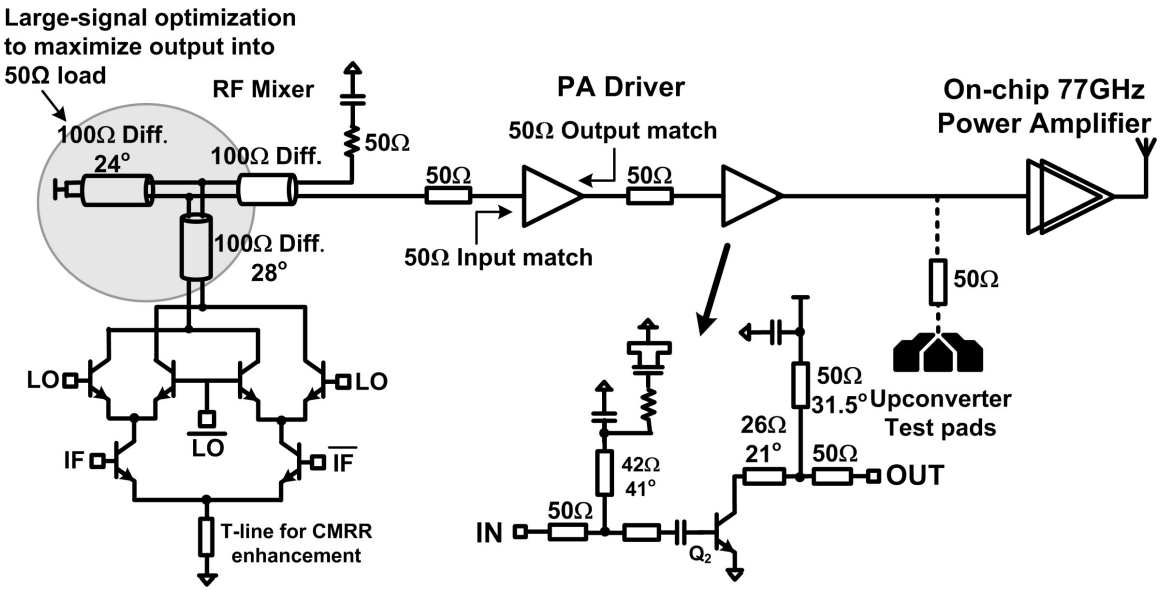


Figure 5.9: 77GHz upconversion stage

5.3.2 RF Stage

The 26GHz IF signal is upconverted to 77GHz by a Gilbert-type upconversion mixer in each element (Figure 5.9). All the circuits in the transmitter up to and including the mixer are differential whereas the PA driver and the PA are single-ended in order to facilitate measurements. While an on-chip mm-wave balun can be implemented, similar to [100], area limitations did not permit that option. Therefore, one of the differential outputs of the mixer is terminated to 50Ω through a capacitor. The other output of the mixer is fed to the PA driver that is input matched to 50Ω. A large LO amplitude is desirable at the LO port to improve conversion gain and provide high output power. Since the mixer sees large signals at both its LO and output ports, the mixer output should not be power-matched under small-signal conditions. Therefore the lengths of the stub and series t-lines used in the mixer output-matching network are optimized, using a methodology similar to the load-pull methodology used in PA design, to maximize the output power into a 50Ω load under large signal conditions. Figure 5.10 plots the simulated[1] small-signal

[1]For the small-signal simulations, the LO transistors in the mixer are assumed to be completely switched.

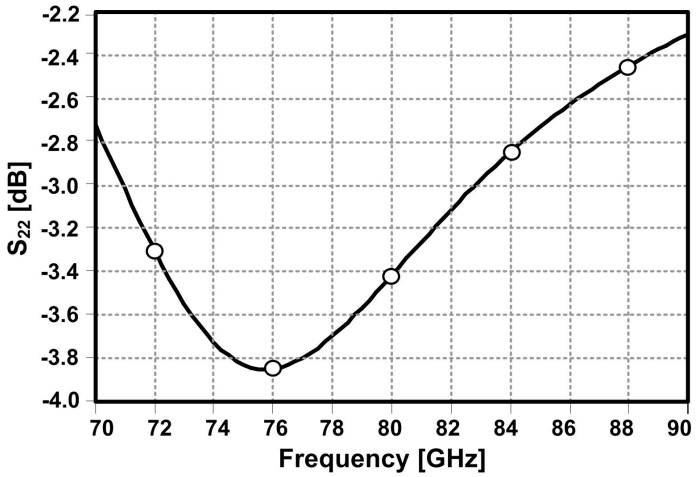


Figure 5.10: Simulated power match at RF mixer output under small-signal conditions

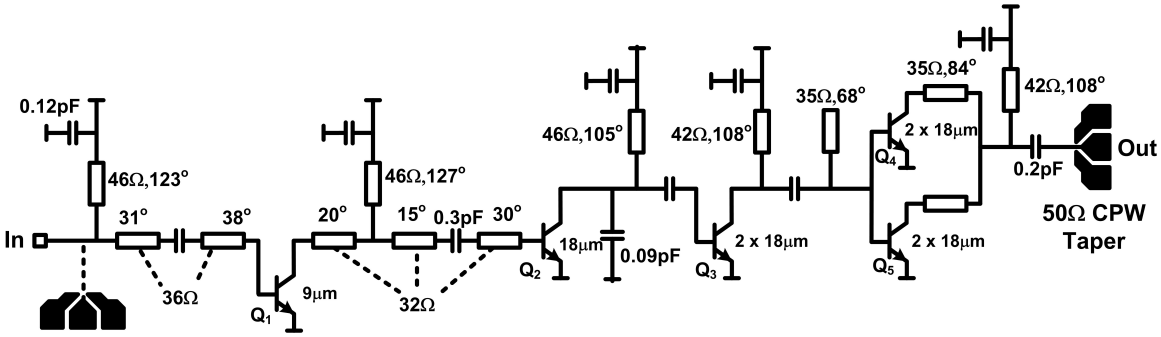


Figure 5.11: 77GHz power amplifier

output-match for the optimized network. The poor power-match at 77GHz at the mixer output with the optimized load shows that small-signal matching is not a good metric to maximize output power.

5.3.3 Power Amplifier

The four transmitter outputs are generated by on-chip PAs in each element [99][2]. As shown in Figure 5.11, the PA is a four-stage design with the transistor size doubled in each stage to ensure that the output-stage saturates first provided each stage has at least 3dB gain. While the first three stages of each PA are designed for

[2]The power amplifier was designed by A. Komijani

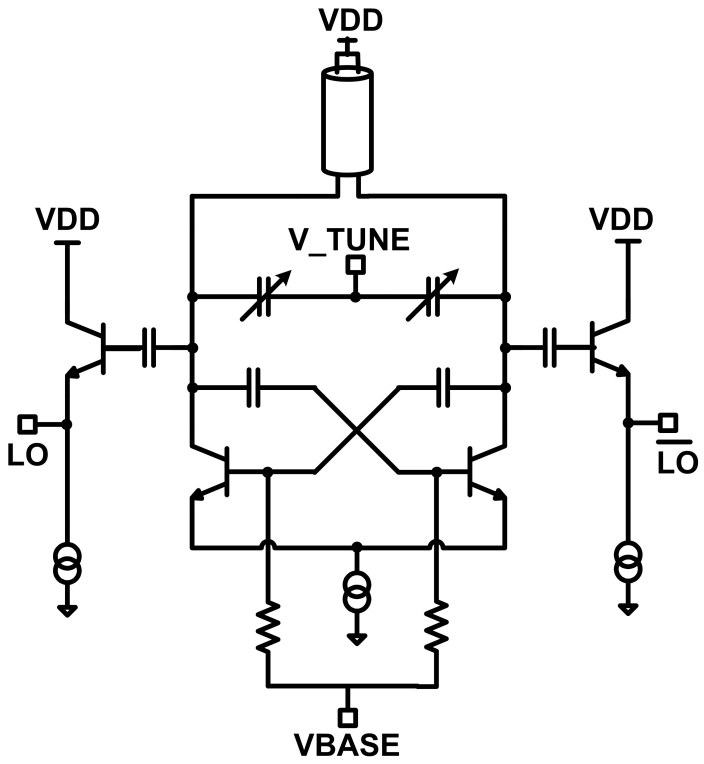


Figure 5.12: 52GHz Voltage-controlled Oscillator

maximum gain, the output stage is designed for maximum efficiency. The outputs from two transistors are combined at the output stage, and the combined output is matched to 50Ω with a t-line network. Each of the PAs is connected to an on-chip dipole antenna that can be trimmed out using a laser for direct electrical measurements via pads. The design and measurement of the PA has been discussed in depth in [101].

5.3.4 52GHz Voltage-Controlled Oscillator

The 52GHz VCO, schematic of which is shown in Figure 5.12, employs a differential cross-coupled design. A shorted differential t-line that provides approximately 95pH@52GHz is used as the inductor in the tank. The proximity of the return-path in the chosen t-line reduces the inductance-per-unit-length and increases current-crowding which leads to an inductor Q of 24@53GHz that is lower

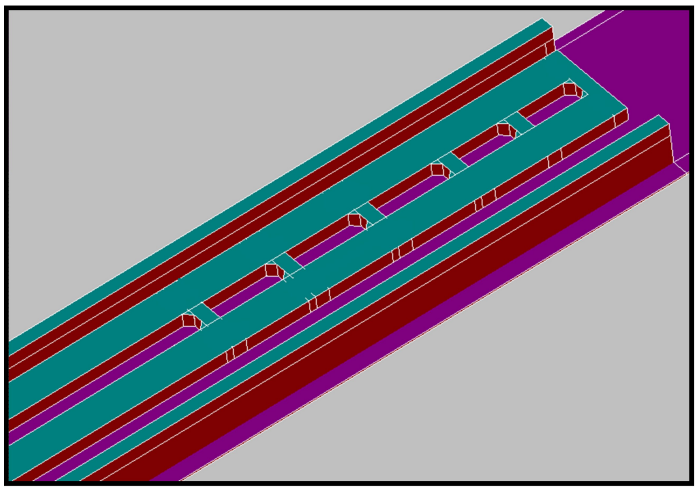


Figure 5.13: Shorting bars across t-line load for one-time coarse tuning

than an optimum Q of around 30. In the first implementation, shorting bars were added to the t-line in order to have a one-time coarse tuning option through laser trimming (Figure 5.13). The continuous VCO tuning range of 10% is achieved through varactors that have a Q of 40 at 52.5GHz. The VCO tuning ranges under different trimming scenarios is shown in Figure 5.14. However, the well-defined path for return current in the t-line (which enables accurate modeling) and careful extraction of interconnect parasitics ensured that VCO operates at the desired frequency of 52.5GHz for the nominal t-line length of 120μm. Hence, the shorting bars were discarded in later implementations. The output of the VCO can be measured by probing test pads that are placed after the first stage of the two-stage VCO buffer that follows the VCO.

The VCO output buffers drive both an 52GHz injection-locked frequency divider[3] and the 52GHz phase rotators. The design details of the injection-locked divider can be found in [91].

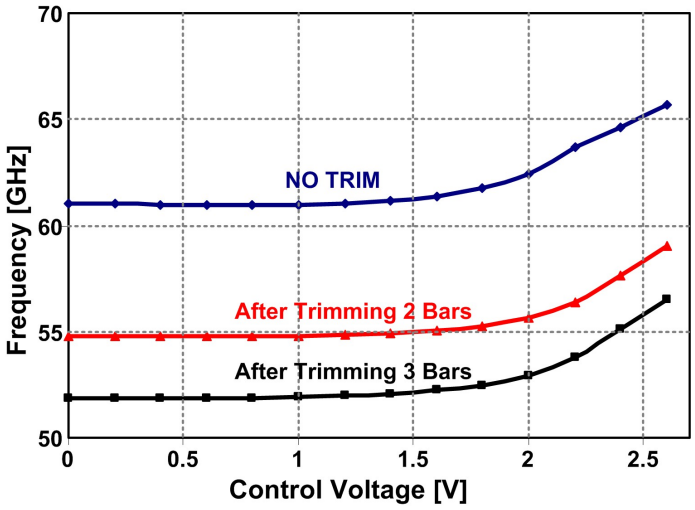


Figure 5.14: VCO tuning ranges with different trim options

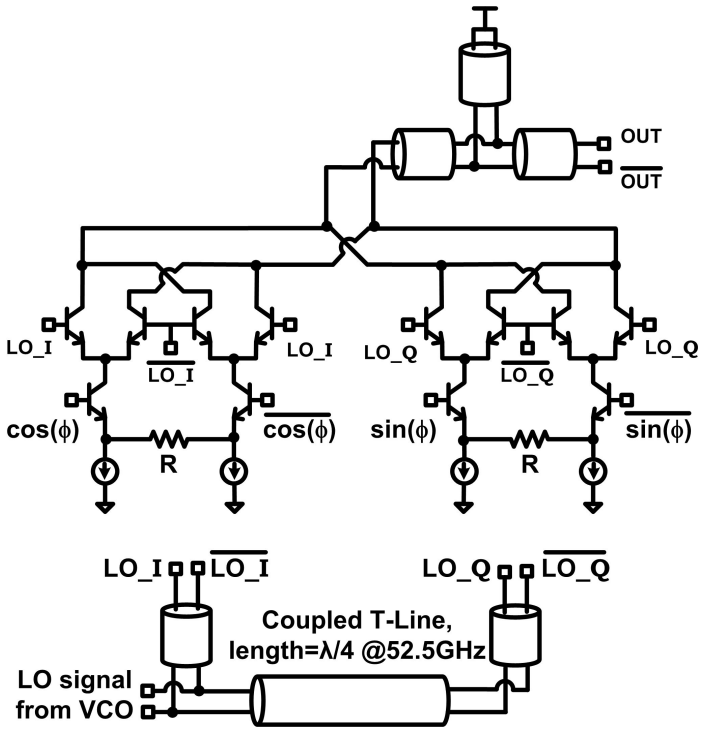


Figure 5.15: 52GHz Phase Rotator

5.3.5 52GHz Phase Rotator

The input from the LO distribution network to the phase rotator is divided into two paths as shown in Figure 5.15[4]. An extra $\lambda/4$ t-line in one of the paths generates the quadrature LO signal locally. The I and Q LO signals are provided to an analog phase rotator. The emitter-degenerated differential pairs at the bottom in each half of the phase rotator control the relative weights of the I and Q signals that are combined at the output of the phase rotator. The emitter degeneration increases the voltage range of the weights in the rotator. As described in the previous section, this local phase-generation scheme minimizes the number of t-lines carrying the 52GHz signal over long distances and enables the use of well-defined t-lines and power matched LO-path buffers without excessive area and power penalties. Unlike the multi-phase distribution approach in [59, 102], the local phase-shifting scheme presented here does not suffer from additional coupling-induced phase errors and signal loss in the distribution path.
The complete design details of the phase rotator can be found in [101].

5.4 Measurement Results

The four-element transceiver was implemented in a SiGe BiCMOS process that had SiGe Bipolar transistors with an f_t of 200GHz [103]. The process offered seven metal layers. The top two thick metal layers are 4μm and 1.25μm and are used for signal distribution to minimize losses. Figure 5.16 shows a die micrograph of the entire transceiver which occupies 6.8mm x 3.8mm of die area. The transmitter and the LO circuits occupy 17mm^2. As the transmitter measurements have to be performed at mm-wave frequencies, a waveguide based measurement setup is utilized for characterizing the transmitter (Figure 5.17). In the case of single-element measurements, the output of the transmitter is probed using WR-12 probes. The output is then connected to an external downconverter which mixes the

[3]The frequency divider was designed by X. Guan.
[4]The phase rotator was designed by A. Komijani.

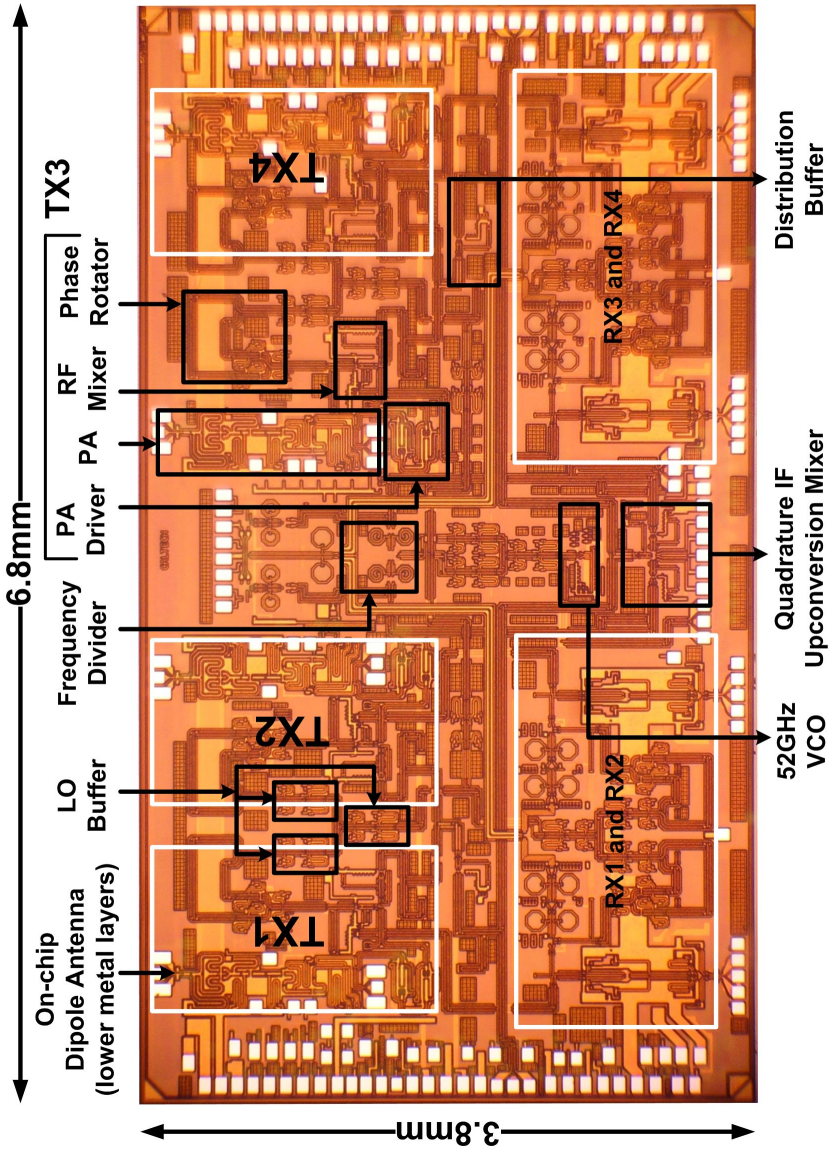


Figure 5.16: 77GHz Die photograph

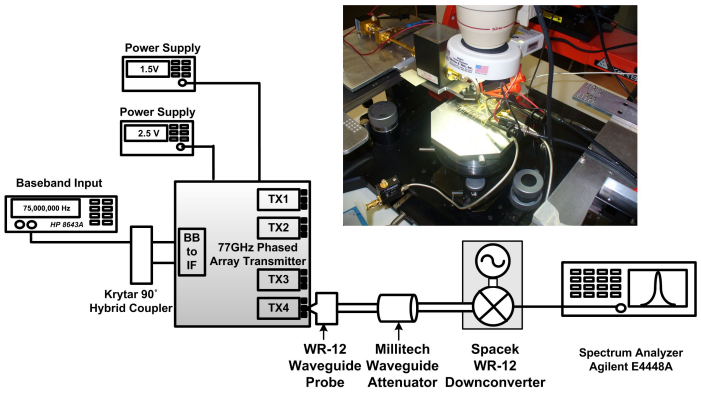


Figure 5.17: Measurement setup for 77GHz transmitter

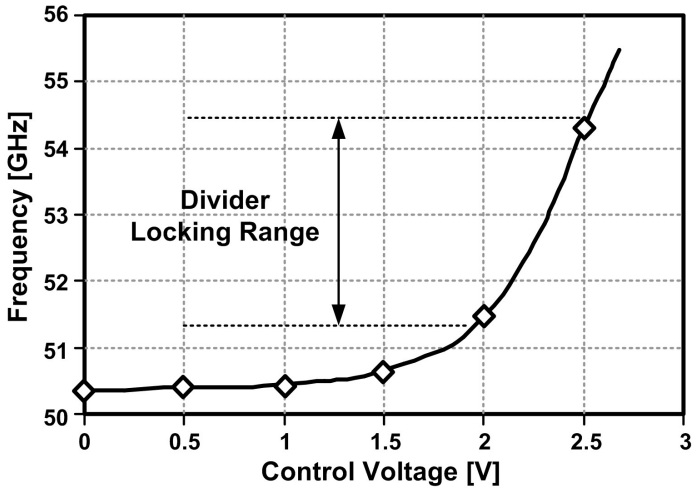


Figure 5.18: Tuning range of 52GHz VCO and locking range of injection-locked divider

77GHz output down to 18GHz, making it possible to view the output on a spectrum analyzer. As mentioned, the chip requires a 1.5V supply for the PA and the PA driver and a 2.5V supply for the rest of the circuitry.

The 52GHz VCO and frequency divider were measured using internal test points. Figure 5.18 shows that the VCO can be tuned from 50.35GHz to 55.49GHz which is a tuning range of 9.7%. Figure 5.18 also shows that the injection-locked divider locks to the VCO input from 51.4GHz to 54.5GHz. The VCO phase-noise was measured using a waveguide and external mixer that downconverted the 52GHz LO to 8GHz

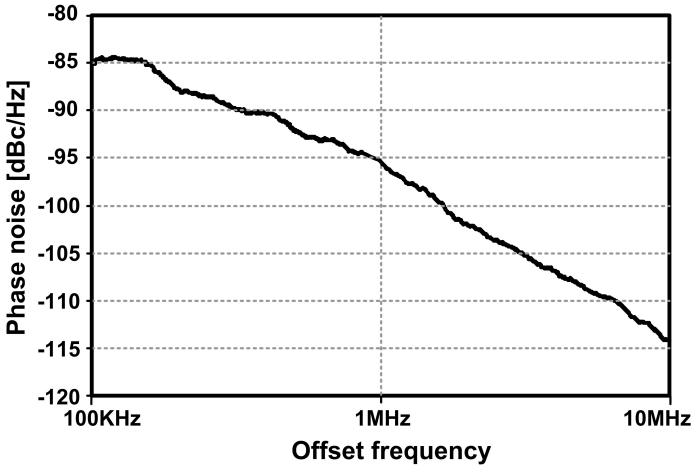


Figure 5.19: Phase noise of 52GHz voltage-controlled oscillator

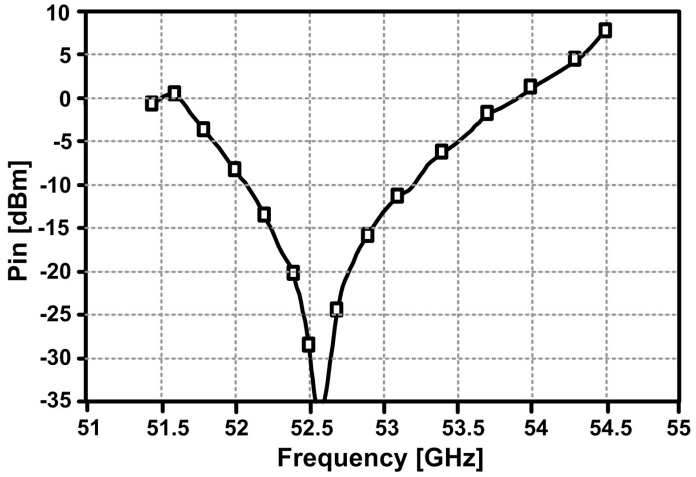


Figure 5.20: Injection-locked divider sensitivity

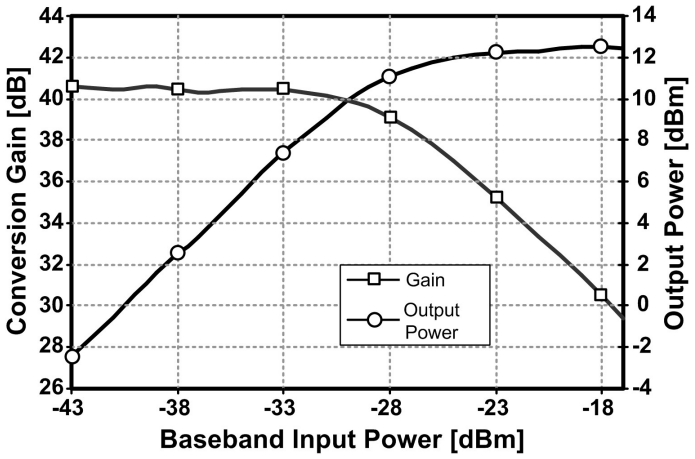


Figure 5.21: 77GHz transmitter output power

using an external 60GHz signal. The VCO measurements show a phase noise of -95dBc/Hz at 1MHz offset at 54GHz (Figure 5.19). The dividers input sensitivity, which is the input power necessary for the divider to achieve locking, is plotted in Figure 5.20. As can be seen from Figure 5.18 and Figure 5.20, the VCO tuning range and the divider locking range are sufficient for the applications of interest.

Figure 5.21 plots the output power of the transmitter at 77GHz. Each element in the transmitter generates up to 12.5dBm with an output-referred 1dB compression point of 10.2dBm. The transmitter has a bandwidth of 2.5GHz. Stand-alone measurements on the PA indicate a maximum power of 17.5dBm with a power-added efficiency (PAE) of 12.8%.

The phased-array transmitter is a part of the 77GHz phased-array transceiver [60, 90], which allows for testing via an internal 77GHz loopback option that utilizes laser trimming. To implement the loopback option, the output of the RF upconversion mixer in the transmit element is connected to the input of the RF downconversion mixer in the receive element. During stand-alone receiver and transmitter characterization, the internal loopback connections between the transmit and receive elements are laser trimmed. However, for testing in the loopback mode, the PA in the transmitter element and the LNA in the receiver

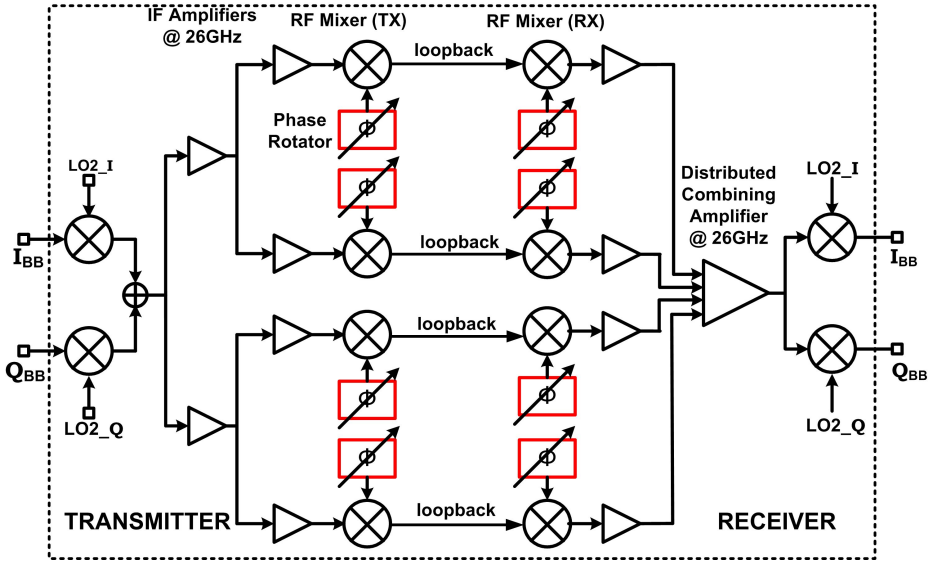


Figure 5.22: Loopback configuration of 77GHz transceiver

element are bypassed using laser trimming and the loopback connection between the output of the 77GHz upconversion mixer in a transmit element and the input of the 77GHz downconversion mixer in a receive element is preserved as shown in Figure 5.22. In order to characterize an array pattern, without using antennas, the outputs of different transmit elements have to be combined with different phase shifts to emulate signal combining in different directions. As mentioned in Section 5.2, the LO phase in each element of the transceiver can be set independently. Therefore, in the loopback mode, it is possible to measure the transmitter pattern for a particular phase-shift setting by varying the phase-shift settings in the receive elements to emulate signal-combining with different phase shifts in different directions. Thus, the loopback option allows for transmitter and receiver array patterns to be measured using baseband input-output, with no off-chip mm-wave connection. Figure 5.23 shows the measured patterns with two transmit-receive pairs active in the loopback mode. The good match between expected and measured beam direction demonstrates the beamforming capabilities of the transmitter.

Table 1 summarizes the measured performance of the transmitter.

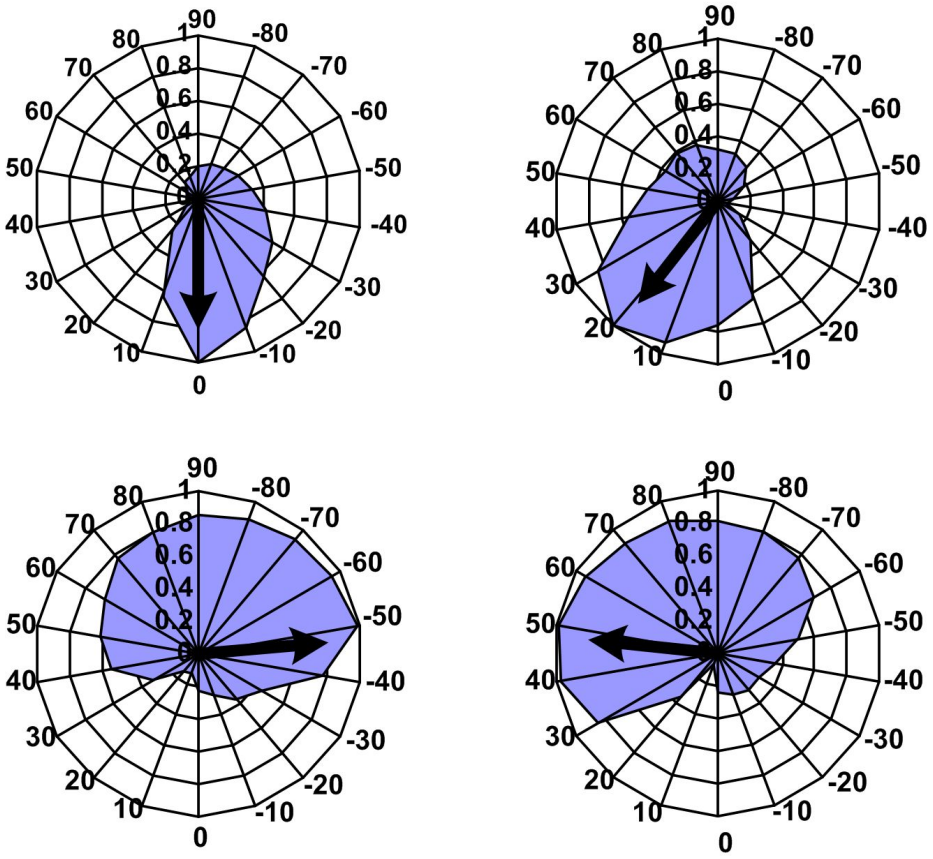


Figure 5.23: Two-element pattern measured using *loopback* method

Transmitter performance	
Maximum output power	+12.5dBm
4-element EIRP	+24.5dBm
Transmit 3dB-bandwidth	2.5GHz
Gain	40.6dB (single element)
Output referred 1dB compression point	+10.2dBm
Image signal attenuation	> 20dBc (for first upconversion step) > 30dBc (for second upconversion step)
LO leakage power	<-19dBc
Transmitter power consumption	
Signal path @ 77GHz	
PA and PA Driver (@1.5V)	200mA (per element)
RF mixer and buffer (@2.5V)	18mA (per element)
Distribution buffers and baseband mixers (@2.5V)	46mA
Phased array performance	
Peak-to-null ratio (2-element *loopback*)	> 12dB
Beam-steering resolution	Continuous (limited by DAC resolution)
VCO tuning range	50.35GHz to 55.49GHz (9.6%)
Divider locking range	51.4GHz to 54.5GHz (5.9%)
LO-path power consumption	
VCO and buffers (@2.5V)	10mA
Analog divider core (@2.5V)	3.1mA
Divider buffers	28mA
LO path distribution buffers (@2.5V)	12mA (each distribution buffer)
Phase rotators (@2.5V)	14mA (each phase rotator)
Die size	$17mm^2$ (Tx + LO circuits) $25.8mm^2$ (Transceiver)
Device Technology	0.12μm SiGe BiCMOS

Figure 5.24: 77GHz transmitter performance summary

5.5 Chapter Summary

This chapter presented a scalable *local* LO-path phase shifting architecture that overcame some of the challenges with the centralized LO-path phase-shifting scheme and enabled integration of a four-element phased-array transceiver at 77GHz in SiGe. The architecture scales well with an increase in number of elements and/or frequency and provides high-resolution phase shifting limited by the resolution of DACs. The detailed design of the circuits in the LO-path and in the transmitter were also described in this chapter. Each transmit element provides up to 12.5dBm output power at 77GHz leading to an EIRP of 26.5dBm. The 52GHz VCO has a tuning range of 9.7% from 50.35GHz to 55.49GHz while the injection-locked divider locks to the VCO input from 51.4GHz to 54.5GHz. Measurements show a VCO phase noise of -95dBc/Hz at 1MHz offset at 54GHz. A built-in *loopback* testing methodology was used to measure the array pattern which indicate good array performance. The implementation of a *local* LO-path phase-shifted array in SiGe at mm-wave frequencies demonstrates how silicon integration opens up many new architectural possibilities that can achieve desired system performance in non-traditional ways. Continuing in the same vein, a hybrid parallel-series phase-shift architecture is presented in the next chapter that extends the concept of a phased-array as a multiple-input single-output system to a multiple-input multiple-output system.

Chapter 6

A Bidirectional RF-Combined 60GHz Phased-Array Front-End

In general, a phased array is configured as a multiple-input single-output system which enables beamforming. As was discussed in Chapter 3, different phase-shifting architectures can be used to combine the signals from a particular direction coherently while rejecting signals from other directions. However, it is noteworthy that signals from all directions are available at the input of the phase shifters and it is only the beamforming network that selects a particular direction from which to receive signals. Therefore, it is conceivable that by implementing a more complex phase-shifting-and-combining network, it is possible to receive signals from multiple directions simultaneously (Figure 6.1) [104–106].

From an application perspective, such multibeam approaches can provide several advantages (Figure 6.2). In the case of communication systems, concurrent reception from different angles provides higher capacity since each beam is akin to a separate communication channel [107]. In the case of networks in which multipath is dominant, the signals from each beam can be combined in an optimal ratio to improve SNR. In sensing applications, multibeam arrays enable simultaneous multiobject tracking and can also reduce scanning times as each beam covers a smaller sector [85, 108].

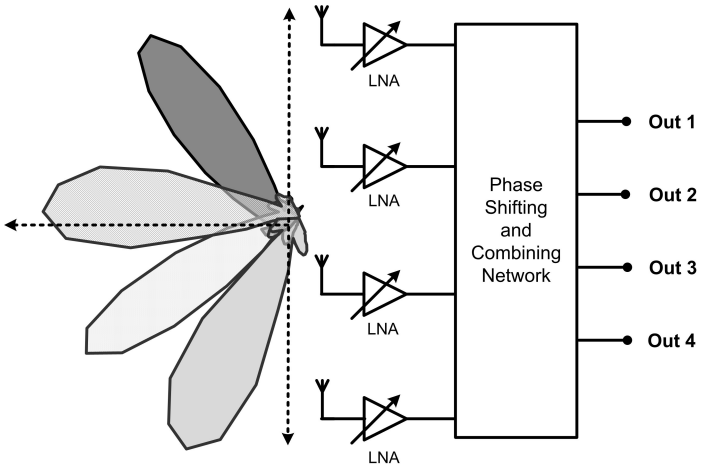
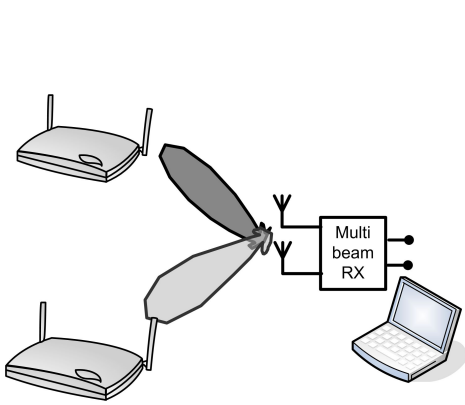
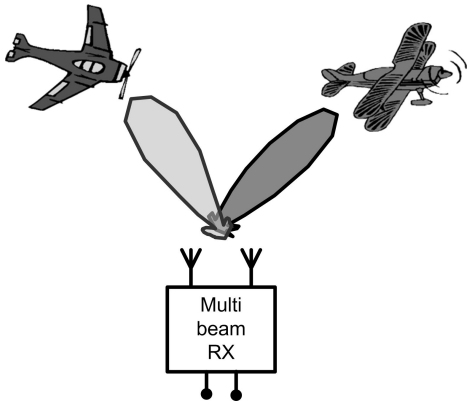


Figure 6.1: An array with multiple outputs



(a) Larger capacity in communication networks



(b) Multiple object tracking in sensing applications

Figure 6.2: Applications of multiple-beam arrays

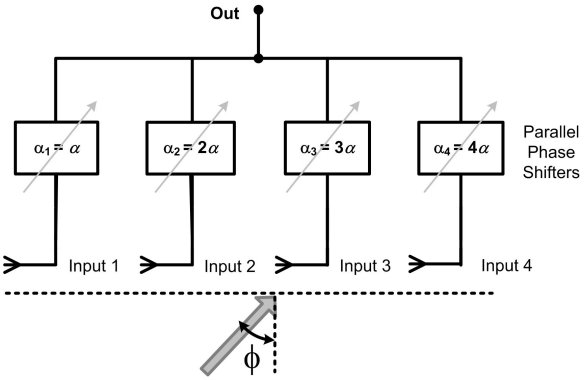
From an implementation perspective, multibeam receivers make efficient use of front-end blocks like the LNAs and antennas as a larger number of outputs are generated with the same front-end [109]. Seemingly, the complexity of the phase-shifting-and-combining network is increased in the realization of a multibeam receiver. However, it has been recognized that employing a divide-and-rule approach by using each individual beam to scan a small sector of space leads to a reduction in the phase shift or delay variation requirements in the array [104].

In this chapter, a novel RF-combining phased-array receiver architecture is presented that enables simultaneous reception from two different angles. The architecture uses a hybrid series and parallel phase shift approach to reduce the phase-shifter variation requirements enabling RF combining in silicon. As will be shown in Section 6.1, the division of the incident angle plane into multiple sectors results in a reduction in phase-shift, or delay, variation requirements enabling silicon integration.

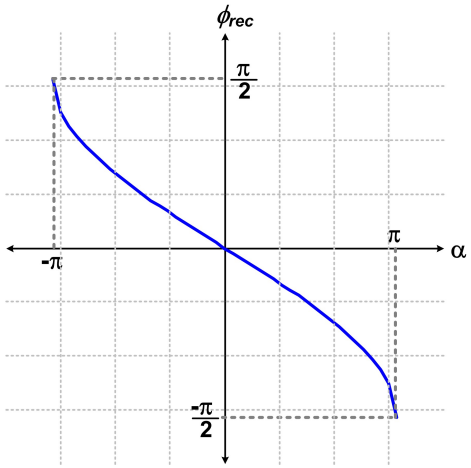
In the following sections, the theory of the bidirectional combining scheme and the implementation of a 60GHz receive array front-end will be discussed in detail. Section 6.1 provides the theoretical framework for the receive array while Section 6.2 describes the circuits in the 60GHz receive front-end. Section 6.3 presents the measured results and Section 6.4 describes theoretical extensions of the phase-shifting and combining scheme for true-time delay based arrays.

6.1 Hybrid Multibeam Array Architecture

In a classic linear array (a parallel-fed array), the signals in each element are combined at the output after undergoing appropriate amounts of phase shift. For the array shown in Figure 6.3(a) with antenna spacing, d, the signal arriving at the n^{th} element in the array with an angle of incidence, ϕ, will experience an excess



(a) Parallel-fed array



(b) Required phase variation in parallel-fed array

Figure 6.3: Parallel-fed array architecture

phase shift, ψ_n,

$$\psi_n = (n-1)\, 2\pi \frac{d}{\lambda} \sin(\phi) \tag{6.1}$$

where λ is the signal wavelength. Assuming antenna spacing to be $d = \frac{\lambda}{2}$,

$$\psi_n = (n-1)\, \pi \sin(\phi) = (n-1)\, \psi \tag{6.2}$$

where $\psi = \pi \sin(\phi)$ is the phase difference between the input to adjacent elements. The directionality of the the input signal can thus be expressed either in terms of the angle of incidence, ϕ, or the phase difference between the inputs to adjacent elements, ψ.

If each parallel phase shifter in Figure 6.3(a) introduces a phase shift, $\alpha_n = n\alpha$, the output signal

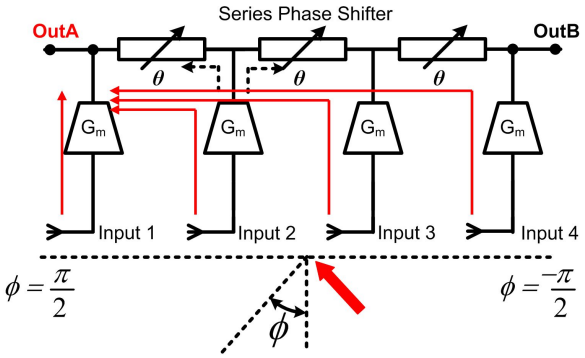
$$I_{out} = I_o \left(\sum_{n=1}^{N} e^{-j([n-1]\psi + n\alpha)} \right) \tag{6.3}$$

From 6.3, the incidence angle of maximum sensitivity is given by,

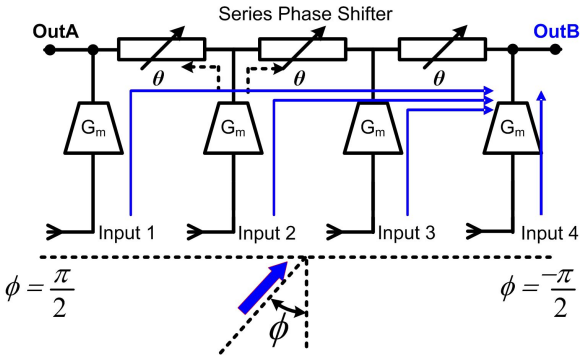
$$\phi_{rec} = \arcsin\left(\frac{-\alpha}{\pi}\right) \tag{6.4}$$

In such an array, α needs to have a 2π variation in phase shift from $-\pi$ to $+\pi$ in order to receive all angles of incidence from $\frac{-\pi}{2}$ to $\frac{\pi}{2}$ [Figure 6.3(b)]. Such a large variation in the phase shifter is often difficult to achieve since the phase shifter bandwidth and loss can degrade with larger phase variations.

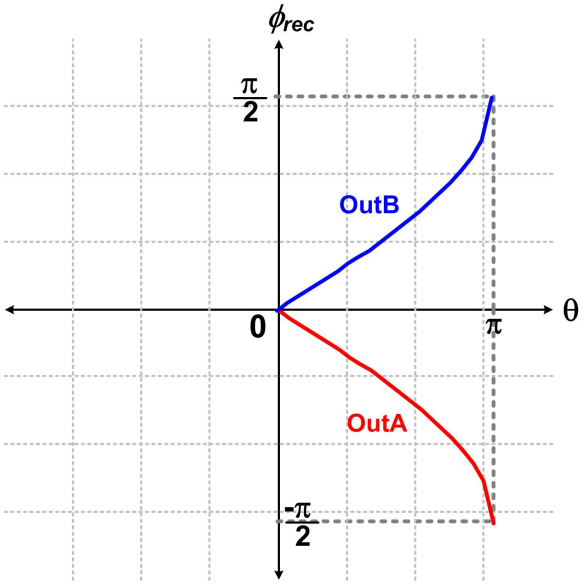
However it is possible to take advantage of the linear relationship between the phase shifts required in different elements and move to a a series-fed array. In a series-fed array, the bilateral phase shifters are coupled between adjacent elements and are reused. As shown in the series-fed architecture in Figure 6.4, the array now has two outputs, `OutA` and `OutB`. For $0 \leq \theta \leq \pi$, signals coming in from directions such that $\frac{-\pi}{2} \leq \phi \leq 0$ combine at `OutA` [Figure 6.4(a)] whereas signals coming in from $0 \leq \phi \leq \frac{\pi}{2}$ combine at `OutB` [Figure 6.4(b)]. Similar to (6.3), the outputs at



(a) Series-fed array-`OutA`



(b) Series-fed array-`OutB`



(c) Required phase variation in series-fed array

Figure 6.4: Series-fed array architecture

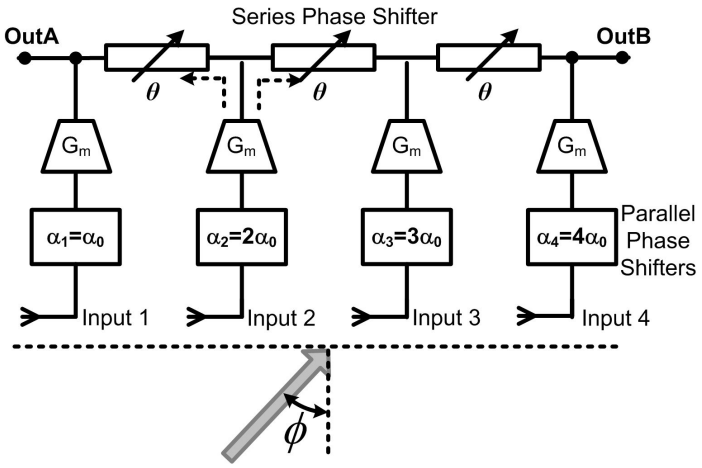


Figure 6.5: Hybrid array architecture

`OutA` and `OutB` are,

$$I_{\texttt{OutA}} = I_o \sum_{n=1}^{N} e^{-j([n-1]\psi+[n-1]\theta)} \tag{6.5}$$

$$I_{\texttt{OutB}} = I_o \sum_{n=1}^{N} e^{-j([n-1]\psi+[N-n]\theta)} \tag{6.6}$$

The angles of maximum sensitivity at `OutA` and `OutB` are given by,

$$\phi_{rec,A} = \arcsin\left(\frac{-\theta}{\pi}\right) \tag{6.7}$$

$$\phi_{rec,B} = \arcsin\left(\frac{\theta}{\pi}\right) \tag{6.8}$$

Hence between `OutA` and `OutB`, all angles of incidence can be received by 0 to π variation in θ [Figure 6.4(c)]. Thus, the phase shifter variation requirement has been reduced by a factor of two as compared to the parallel-fed array. It is important to note that since there is only one degree of freedom, θ, the outputs at `OutA` and `OutB` are not independent of each other.

This concept can be extended further to an hybrid series-parallel approach with both parallel and series phase shifters in the array. As shown in Figure 6.5, the signal in the n^{th} element undergoes a phase shift, α_n, in the parallel path while each series phase shifter provides a phase shift of θ. Signals on the series phase shifter travel in both directions, yielding the following signal summations at `OutA` and `OutB`,

$$I_{\texttt{OutA}} = I_0 \sum_{n=1}^{N} e^{-j(n\alpha+[n-1]\theta+[n-1]\psi)} \tag{6.9}$$

$$I_{\texttt{OutB}} = I_0 \sum_{n=1}^{N} e^{-j(n\alpha+[N-n]\theta+[n-1]\psi)} \tag{6.10}$$

From (6.9), it can be shown that the incident angles of maximum sensitivity at `OutA` and `OutB` are,

$$\phi_{rec,A} = \arcsin\left(\frac{-(\alpha+\theta)}{\pi}\right) \tag{6.11}$$

$$\phi_{rec,B} = \arcsin\left(\frac{-(\alpha-\theta)}{\pi}\right) \tag{6.12}$$

Thus, for given values of α and θ, `OutA` and `OutB` receive signals from different directions simultaneously[1]. By enabling variation in α, the required variation in θ can now be further reduced as compared to the series phase shifter case. If the array has m modes of operation, with the value of α in the i_{th} mode,

$$\alpha^i = i\frac{2\pi}{m} \tag{6.13}$$

then the series phase shifter variation requirement is reduced to $\frac{\pi}{m}$. In the 60GHz frontend described in Section 6.2, the array has four modes of operation, and hence the series phase-shifter variation requirement is reduced to $\frac{\pi}{4}$ or 45°.

[1]It can also be seen that for the cases when $\theta = 0$ and $\alpha = 0$, (6.9) reduces to the parallel-fed array and series-fed array respectively

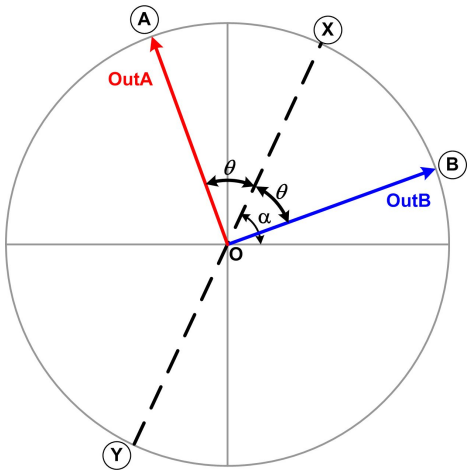


Figure 6.6: Incidence angles received at `OutA` and `OutB` represented in the ψ-plane

Limiting the variation in α to discrete steps does inhibit the ability to specify the two angles of reception independently. There are now two degrees of freedom, α and θ in (6.11), that can theoretically be used to set the receive angles at `OutA` and `OutB` independent of each other. The incidence angles of maximum sensitivity can be expressed graphically in the ψ plane in which the angles received at `OutA` and `OutB` are symmetrically located about a diameter, XY that is defined by α (Figure 6.6). The angle formed by the received angles, OA and OB, with respect to XY are given by θ. Hence, in order to receive any two angles of incidence, it is sufficient if α and θ can both vary from 0 to π. In this case, however the reduction in required phase variation is sacrificed in order to specify reception angles independently.

6.2 60GHz Phased-Array Receiver Front-End

6.2.1 60GHz Array Architecture

Figure 6.7 shows the block diagram of the implemented array receiver. The front-end has four elements with a 60GHz variable-gain LNA at the input of each element. The variable gain is included in the LNA in order to compensate for gain variation downstream. The output of the LNA drives the discrete phase selector

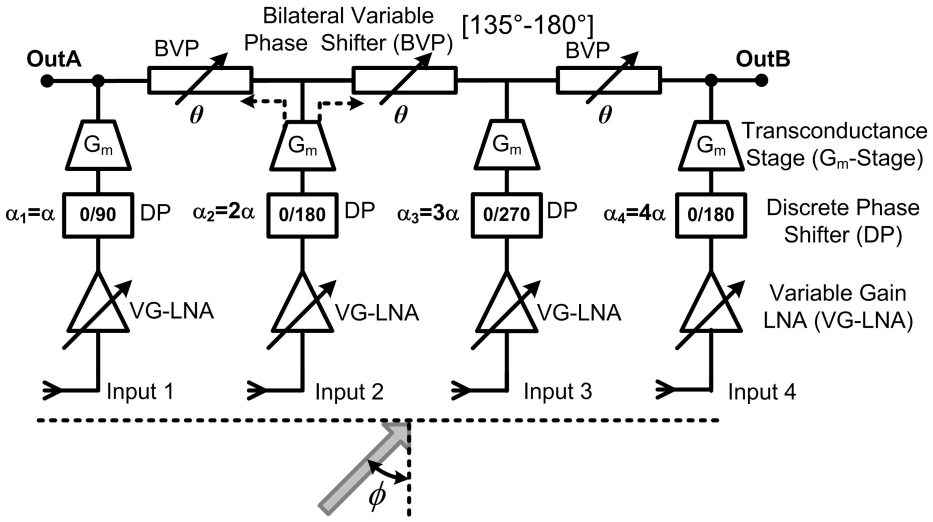
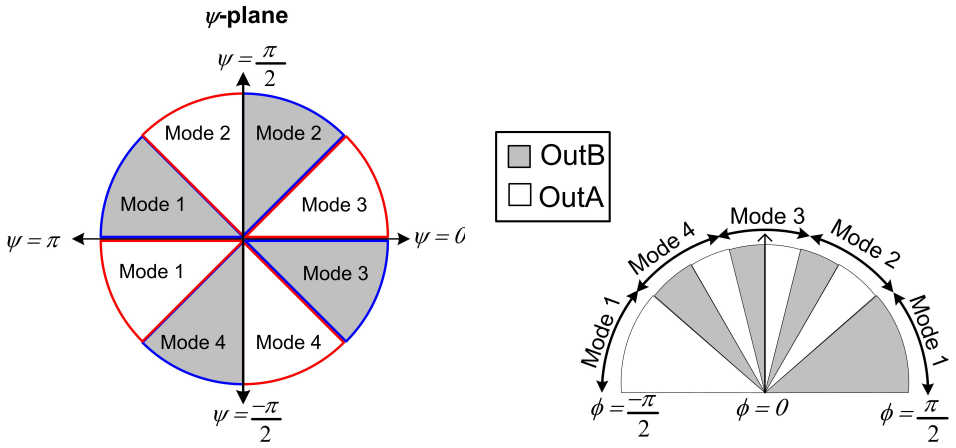


Figure 6.7: 60GHz phased-array receiver front-end

Mode \ Element	1	2	3	4
1	0°	0°	0°	0°
2	90°	180°	270°	0° (360°)
3	0°	180°	0° (360°)	180° (540°)
4	90°	0° (360°)	270°	180°

Mode	α
1	0°
2	90°
3	180°
4	-90°

Figure 6.8: Modes of operation of array



(a) Angles received at `OutA` and `OutB` in ψ-plane

(b) Angles received at `OutA` and `OutB` in ϕ-plane

Figure 6.9: Angles received at `OutA` and `OutB` in ψ-plane and ϕ-plane

that can select between two phase shifts. The possible phase shift choices are 0° and 90° in element 1, 0° and 180° in element 2, 0° and 270° in element 3, and 0° and 180° in element 4. The output of the discrete phase shifter is provided to the transconductance stage (Gm_stage), which converts the signal to current and drives the bilateral series phase shifters. Both `OutA` and `OutB` are matched to 50Ω using $\frac{\lambda}{4}$ transmission lines.

The array can be configured in four modes of operation, each corresponding to a particular value of α. The discrete phase shifter setting in each mode and the value of α are listed in Figure 6.8. The angles received at `OutA` and `OutB` can be calculated in each mode using 6.11 and is shown in the ψ-plane and ϕ-plane in Figure 6.9. Thus, between `OutA` and `OutB` and across the four modes of operation, all angles of incidence, $i.e., \frac{-\pi}{2} \leq \phi \leq \frac{\pi}{2}$ can be received.

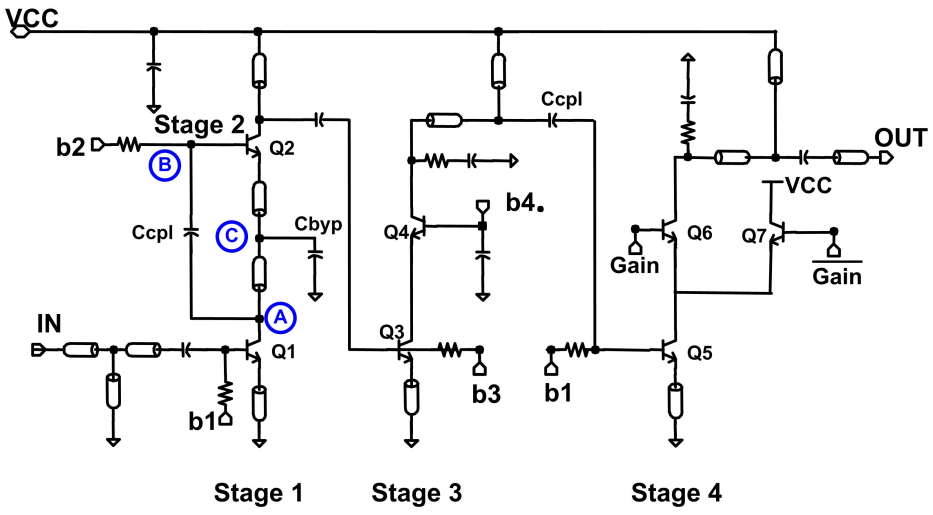


Figure 6.10: 60GHz variable-gain LNA

6.2.2 Circuits

6.2.2.1 60GHz Variable-Gain LNA

The 60GHz LNA is a four-stage design with variable gain implemented in the fourth stage (Figure 6.10). The first two stages of the LNA, which similar to the design in [110], are common-emitter stages with current reuse [111]. While transistors $Q1$ and $Q2$ share the same DC current, node C is bypassed to ground at RF while node A is coupled to node B. The third stage of the LNA, comprising $Q3$ and itś tuned load is another common-emitter design with a tuned load. Variable gain is achieved in the LNA using current steering in the fourth stage. The RF output current of transistor $Q5$ gets divided by $Q6$ and $Q7$, with the relative current in each path being controlled by the V_{gcntrl} voltage. By varying this signal, the current through $Q6$ and hence, the gain of the stage can be controlled. The gain, G_{LNA}, can be expressed as,

$$G_{LNA} = \frac{g_{m,Q5} Z_L}{2} \left(1 + \tanh\left(\frac{V_{gcntrl}}{2V_T}\right)\right) \tag{6.14}$$

where Z_L is the load impedance seen by $Q6$ and $g_{m,Q5}$ is the transconductance of $Q5$. In order to linearize the gain variation with control voltage, the V_{gcntrl} voltage is

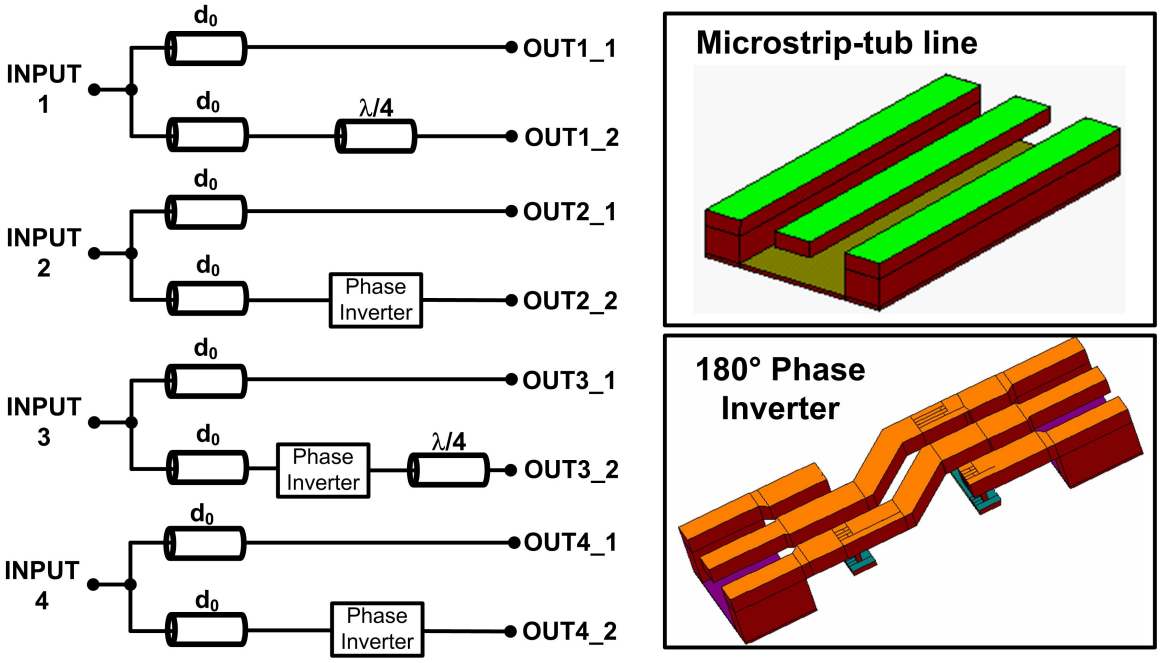
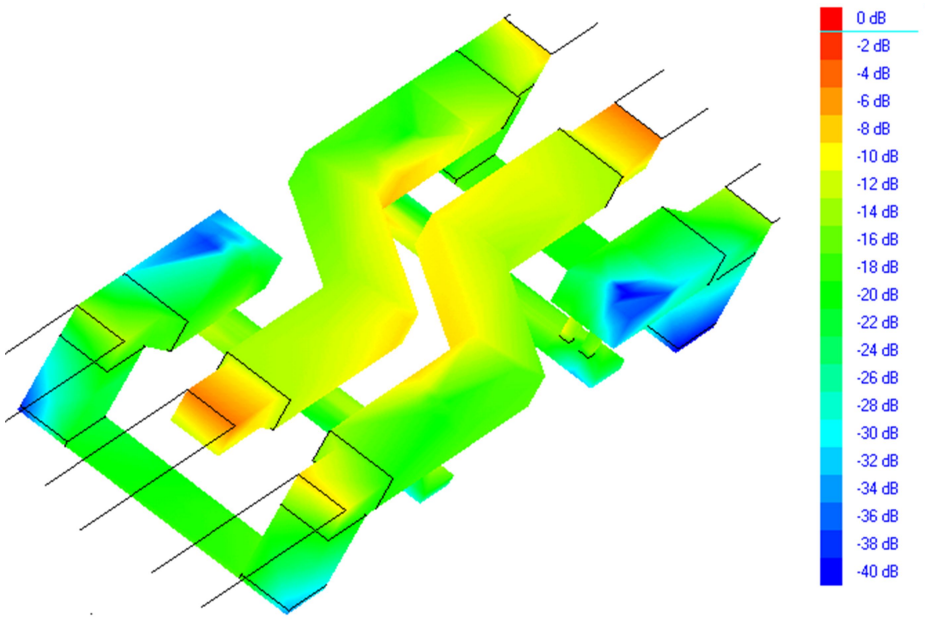


Figure 6.11: Discrete phase selector passives

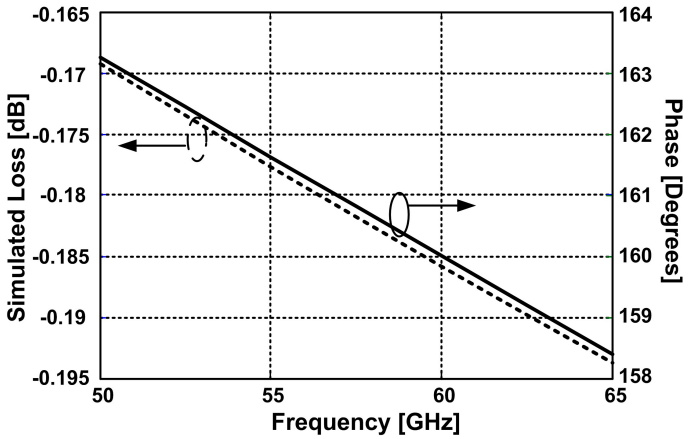
generated using a *arctanh* cell. The output of the LNA is matched to 25Ω using shunt-stub tuning. The LNA consumes 12.5mA from a 2.7V supply.

6.2.2.2 Discrete Phase Selector

The output from the LNA is divided into two paths in the discrete phase selector. Since each of the paths presents a 50Ω impedance, the output of the LNA is matched to 25Ω. One of the paths is the nominal 0° path while the other is the non-zero phase shift. The discrete phase shifts are achieved using a combination of passive phase inverter and transmission lines (Figure 6.11). While the 90° phase shift is achieved using a $\frac{\lambda}{4}$ transmission line, the 180° phase shift is implemented using a passive phase inverter which is shown in Figure 6.11 [112]. In this structure, the signal and ground lines in a coplanar waveguide are interchanged. DC blocking capacitors at input and output ensure that the bias points of all stages connected to it are not affected. Figure 6.12(a) shows the current distribution of the passive phase inverter simulated using IE3D [35]. As can be seen from the figure, interchanging



(a) Simulated current distribution at 60GHz in passive phase inverter



(b) Simulated phase shift and insertion loss of phase inverter

Figure 6.12: EM simulations of passive phase inverter

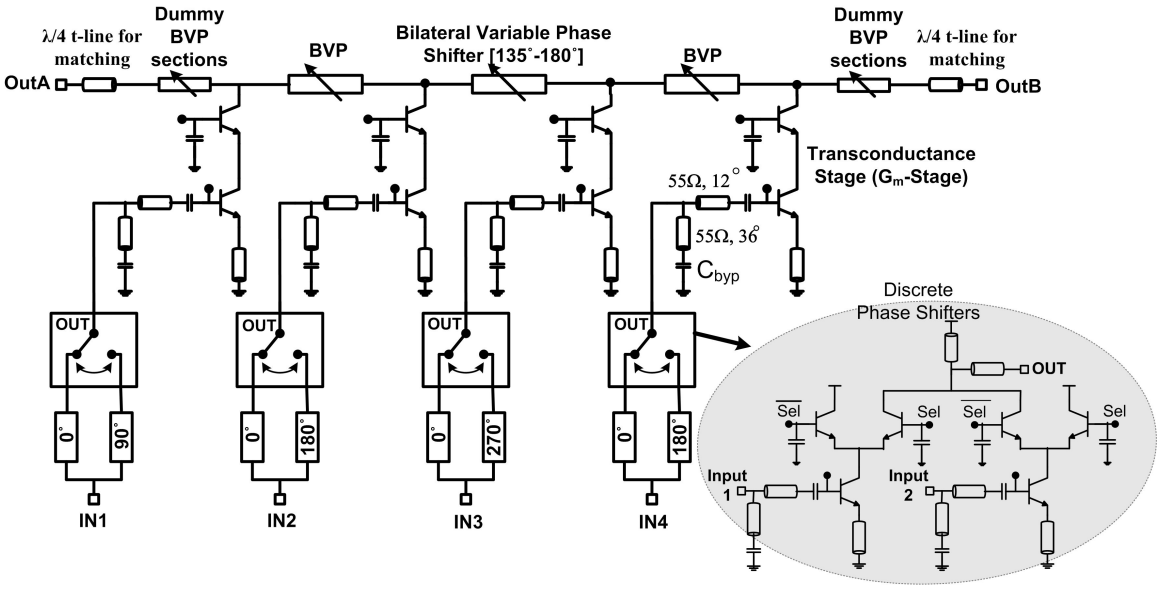
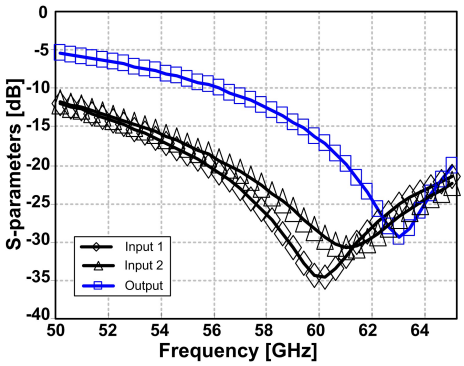


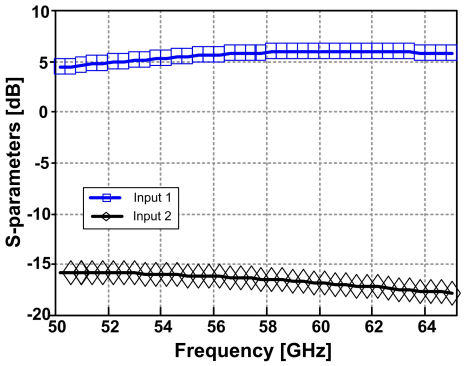
Figure 6.13: Schematic of discrete phase selectors and transconductance stage(Gm_stage)

ground and signal traces ensures a 180° phase inversion. The simulated phase shift and the insertion loss of the phase inverter are plotted in Figure 6.12(b). The phase shift through the structure shown in Figure 6.12(a) is approximately -200°. The excess phase shift is equalized by a longer t-line in the nominal 0° path.

Figure 6.13 shows the schematic of the discrete phase selector. The selector essentially acts as a multiplexer, with the *Sel* signal determining which of the two inputs goes through to the output. When the *Sel* is low ($1.2V$), Input 1 is selected whereas when *Sel* is high ($2.3V$), Input 2 is selected as the output. Figure 6.14(a) shows the simulated input and output matching of the discrete phase selector. The output and each of the inputs is 50Ω. Figure 6.14(b) plots the simulated input-to-output s-parameters when Input 1 is selected, demonstrating the operation of the discrete phase selector.



(a) Simulated matching at Input1, Input2 and Output of Discrete phase selector



(b) Simulated input-to-output s-parameters when Input1 is selected

Figure 6.14: Simulated s-parameters of discrete phase shifter stage

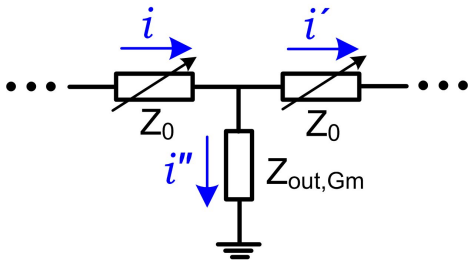


Figure 6.15: Error introduced by finite output impedance of transconductance stage

6.2.2.3 Transconductance Stage

The transconductance stage (*Gm_stage*) converts the output of the discrete phase selector to current and drives the series phase shifters (Figure 6.13). The finite output impedance of the *Gm_stage* introduces an error in the phase shift as some of the current in the series phase shifters sees a parasitic load impedance (Figure 6.15). In order to increase the output impedance, a cascode structure is chosen for the *Gm_Stage*. The output impedance of the *Gm_Stage* is dominated by the output capacitance. Given the 25Ω impedance of the series phase shifters, the phase shift error introduced by each stage is,

$$Err = \angle \frac{Z_{out,Gm}}{Z_0 + Z_{out,Gm}} \tag{6.15}$$

The error per stage at 60GHz is 5.3° for an output impedance of 1kΩ in parallel with 10fF and is 7.9° for an output impedance of 1kΩ in parallel with 15fF. In case of a 24GHz implementation the errors in the two cases are -2.1° and 3.2° respectively.

6.2.2.4 Bilateral Series Phase Shifters

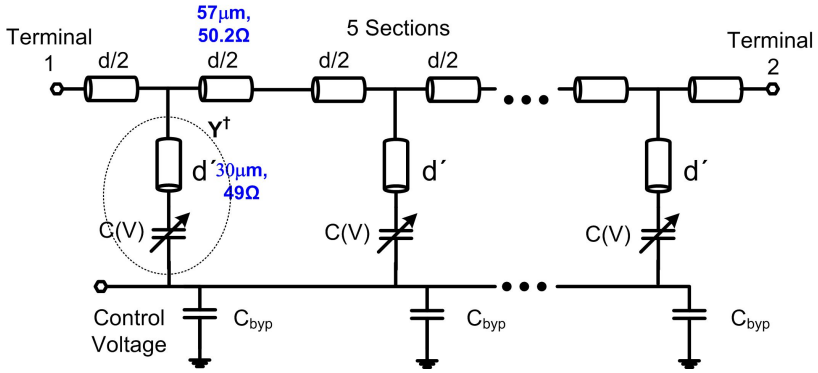
The bilateral variable phase shifter is implemented using a loaded transmission line structure as shown in Figure 6.16(a). By varying the capacitance, the phase shift through the structure can be changed from $\frac{3\pi}{4}$ to π. In order to provide design insight, a simplified lumped approximation of the phase shifter, as shown in Figure 6.16(b), is analyzed. The phase shift, θ through n sections of a lumped LC line is given by,

$$\theta \approx n\omega\sqrt{LC\left(V\right)} \tag{6.16}$$

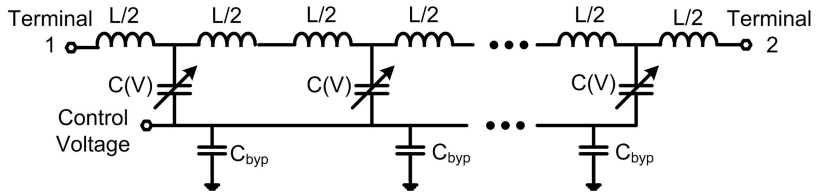
and the impedance is given by,

$$Z = \sqrt{\frac{L}{C\left(V\right)}\left(1 - \frac{\omega^2 LC\left(V\right)}{4}\right)} \tag{6.17}$$

As shown by (6.16) and (6.17), the impedance is proportional to $\frac{1}{\sqrt{C}}$ while the phase



(a) Series phase shifter



(b) Simplified lumped approximation

Figure 6.16: Series phase shifter

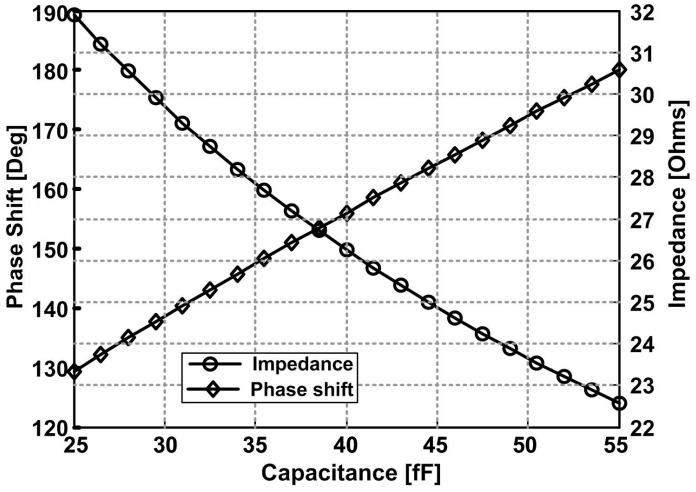


Figure 6.17: Phase shift and impedance variation with capacitance

shift is proportional to $\sqrt{C}$, and hence a large variation in phase shift leads to a large variation in impedance. This implies that the series phase shifter cannot be matched to a constant load for a large variation in phase shift. However, in the hybrid array architecture, the phase-shifter variation requirements have been reduced to $\frac{\pi}{4}$. For the given phase variation,

$$\text{If}\theta : \frac{3\pi}{4} \rightarrow \pi \Rightarrow Z : Z_{max} \rightarrow \frac{3Z_{max}}{4} \tag{6.18}$$

Assuming a matching impedance,

$$Z_0 = \frac{Z_{max} + Z_{min}}{2} = \frac{7Z_{max}}{8} \tag{6.19}$$

the matching is better than 20dB across all phase shift values.

In the case of the n-section t-line based periodic structure in Figure 6.16(a), the phase shift, θ and the impedance, Z_0, are given by [33],

$$\theta = n\cos^{-1}\left(\cos(kd) - \frac{b}{2}\sin(kd)\right) \tag{6.20}$$

$$Z_0 = \frac{BZ_t}{\sqrt{A^2 - 1}} \tag{6.21}$$

where

$$b = Y^{\dagger}Z_t \tag{6.22}$$

$$A = \cos(kd) - \frac{b}{2}\sin(kd) \tag{6.23}$$

$$B = j\left(\sin(kd) + \frac{b}{2}\cos(kd) - \frac{b}{2}\right) \tag{6.24}$$

Applying the parameters in Figure 6.16(a) in (6.22), a capacitance variation from 18fF to 45fF results in the phase and impedance variation plots shown in Figure 6.17. Thus, the phase shifter provides the desired phase variation from 135° to 180°

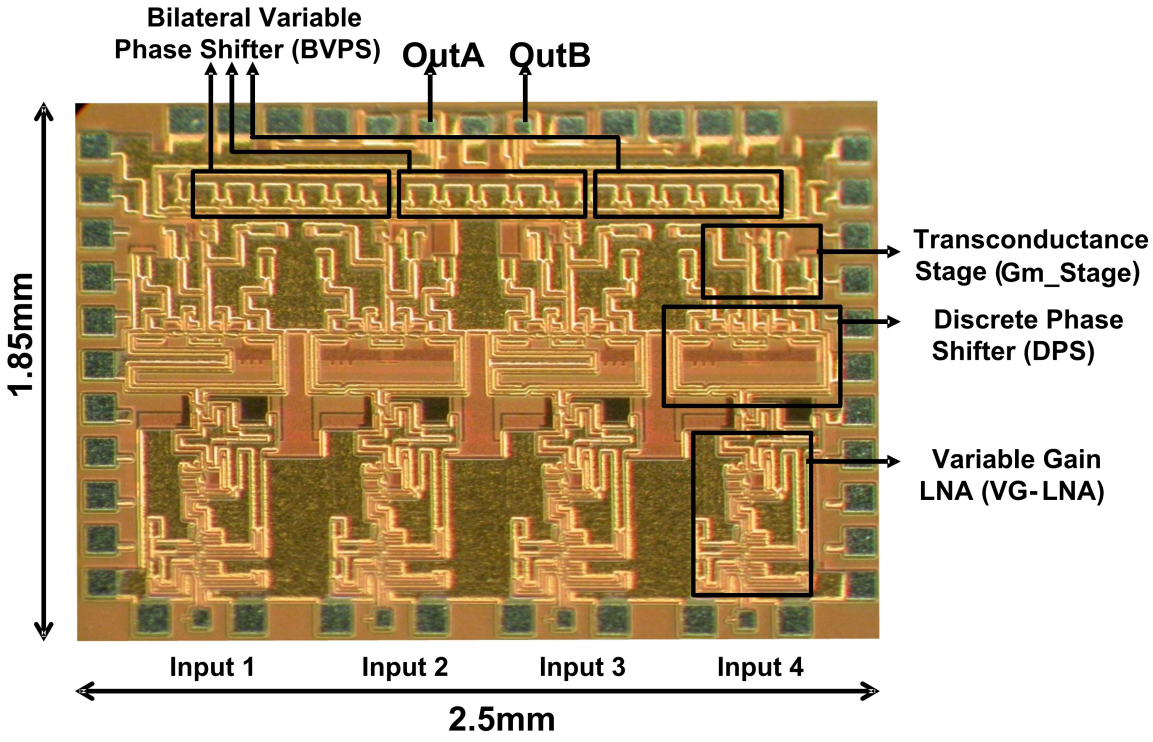


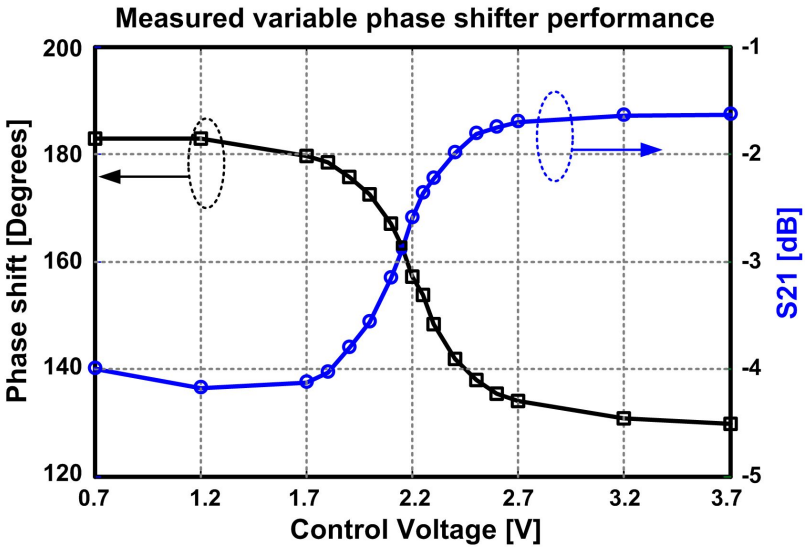
Figure 6.18: Die micrograph of 4-element 60GHz phased-array receive front-end

while ensuring good matching to a constant load impedance.

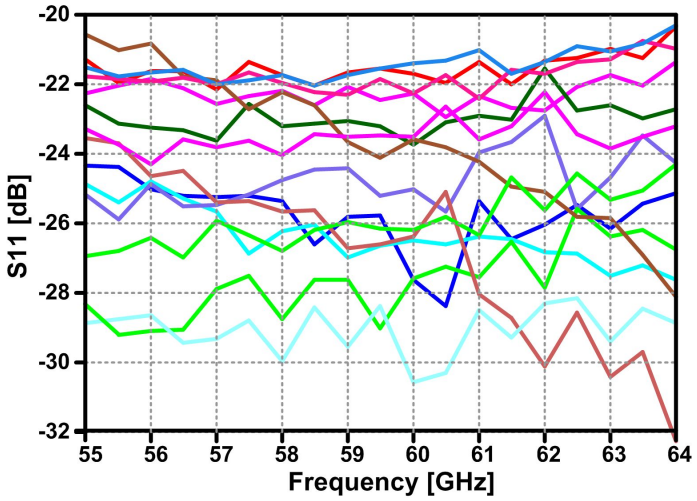
6.3 Measurement Results

Figure 6.3 shows the die micrograph of the implemented 60GHz receive front-end which occupies 2.5mm x 1.85mm of die area in a 0.12um SiGe BiCMOS process with HBT f_t greater than 200GHz [103]. The chip consumes 88mA from a 2.7V supply and 12mA from a 2.2V supply leading to a total power consumption of 265mW across all four elements.

A test chip was also fabricated to determine the performance of the phase shifters stand-alone. Figure 6.19(a) shows the measured phase shift and loss of a stand-alone series phase shifter. The measurements show that the phase shift can be varied from $\frac{3\pi}{4}$ to π as the control voltage is varied. The loss of the phase shifter varies from 1.5dB to 4dB. The measured impedance match of the series phase



(a) Measured phase shift and loss at 60GHz



(b) Measured impedance match to 25Ω

Figure 6.19: Measured phase shifter performance

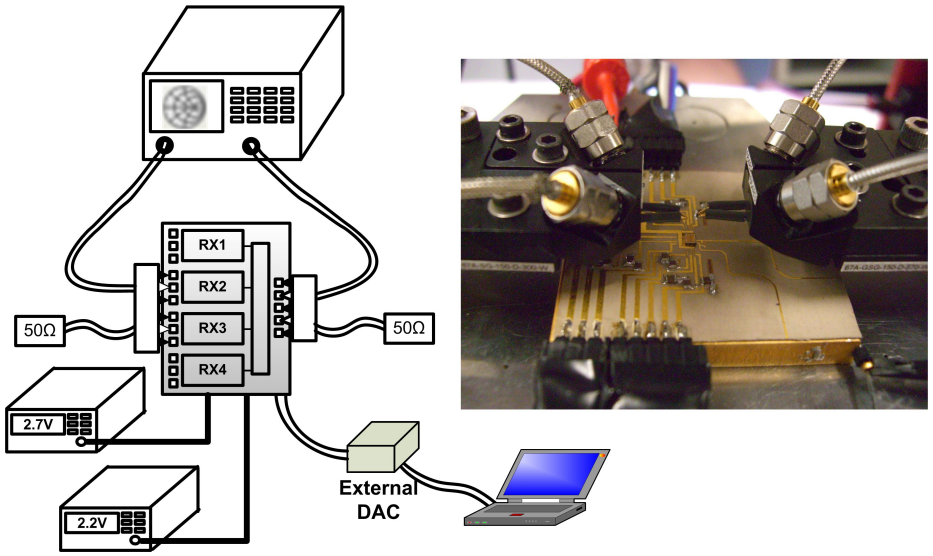


Figure 6.20: S-parameters measurement setup for receive array

shifter to a 25Ω termination impedance is shown in Figure 6.19(b) which indicates better than 20dB match across all phase-shift settings.

The complete chip was measuring using an s-parameter based measurement setup (Figure 6.20). In order to characterize the array, the s-parameters were measured between each input-output pair. (There are four inputs and two outputs leading to eight input-output pairs).

Figure 6.21 plots the measured s-parameters from Input 1 to `OutA` as a function of frequency which show good input and output match from 55GHz to 65GHz. The magnitude of S_{21} from each input to `OutB` is plotted in Figure 6.22. The variation in gain is due to the varying loss in the phase shifters. The signal in Input 1 goes through three phase shifters and hence undergoes the most loss (∼12dB in the 180° phase shift mode). Improving the performance of the bilateral phase shifters by using alternate topologies such as switch-based phase shifters is a future area of research.

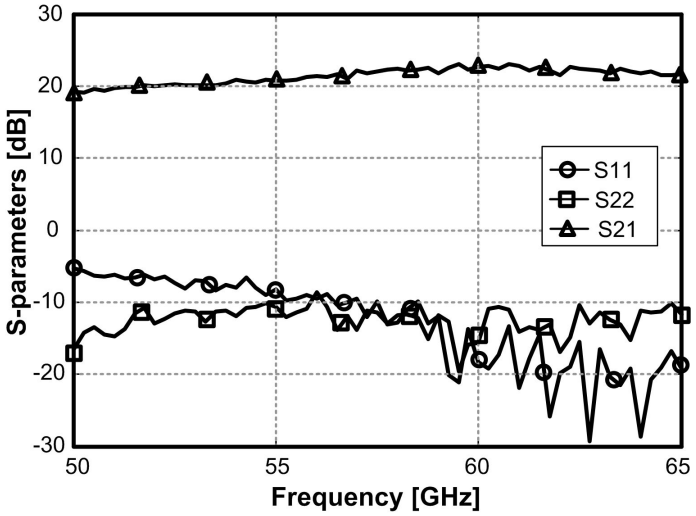


Figure 6.21: Measured s-parameters from Input 1 to `OutA`

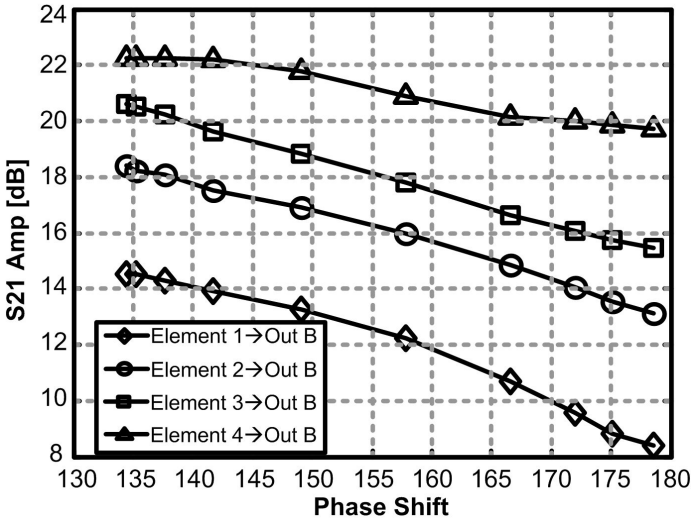


Figure 6.22: Gain from each input to `OutB`

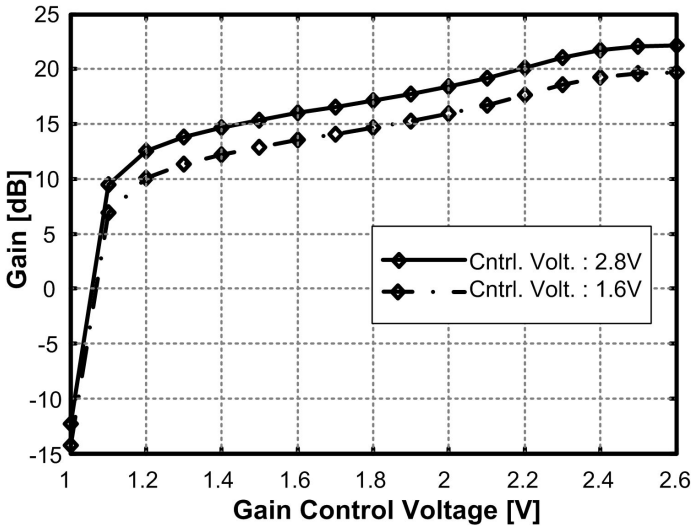


Figure 6.23: Gain variation provided by the variable-gain LNA (Input 1 to `OutA`)

The variation in gain with phase-shift setting has to be compensated by the variable gain functionality in the LNA upfront. Figure 6.23 plots the system gain from Input 1 to `OutA` for two different phase shift settings. The linear gain variation is due to the *tanh* cell used to generate the gain control voltage.

Figure 6.24 plots the gain of the receiver as a function of the input power. The measured input-referred 1dB compression point is -33.5dBm, which corresponds to an output-referred 1dB compression point of -13dBm.

The phase shift from Input 1 to `OutB` is shown in Figure 6.25(a). The blue curves plot the phase variation with control voltage for the nominal 0° phase-shift mode in the discrete phase selector for different gain settings while the red curves represent the phase variation for the 90° discrete phase shift mode. Similar curves are plotted for Input 2 to `OutB` in Figure 6.25(b).

Figure 6.26(a) and Figure 6.26(b) plot the noise figure of each element (with `OutB` as the output) for the minimum and maximum series phase-shift setting. The 180° phase-shift setting corresponds to the lossiest setting in the phase shifter (Figure 6.19(a)) which accounts for the higher noise figure of Element 1 and the variation in

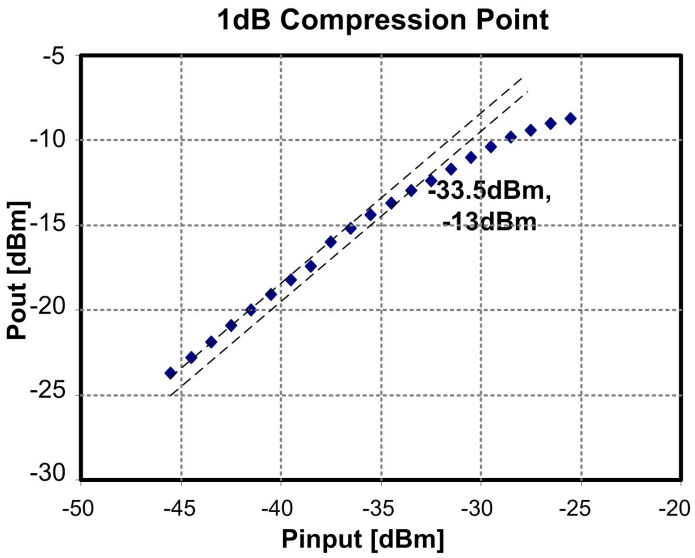


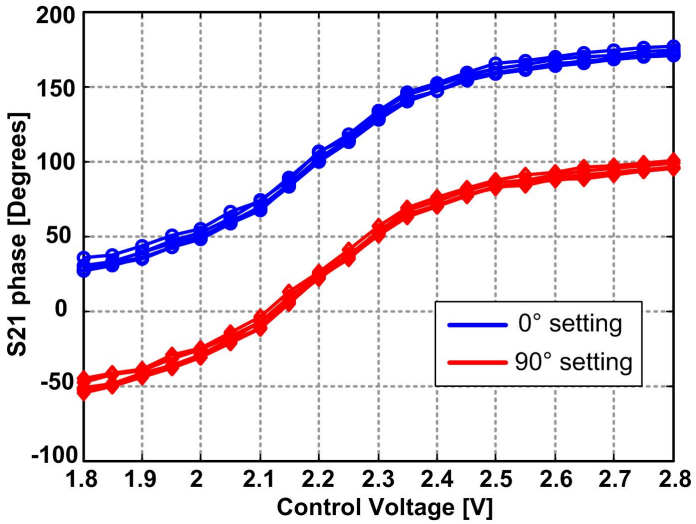
Figure 6.24: Gain compression in 60GHz receiver front-end

element noise figures in the 180° phase-shift setting. The element noise figure varies from 4.8dB to 6.2dB at 60.5GHz in this setting while the noise figure is below 5.2dB in the 135° phase-shift setting.

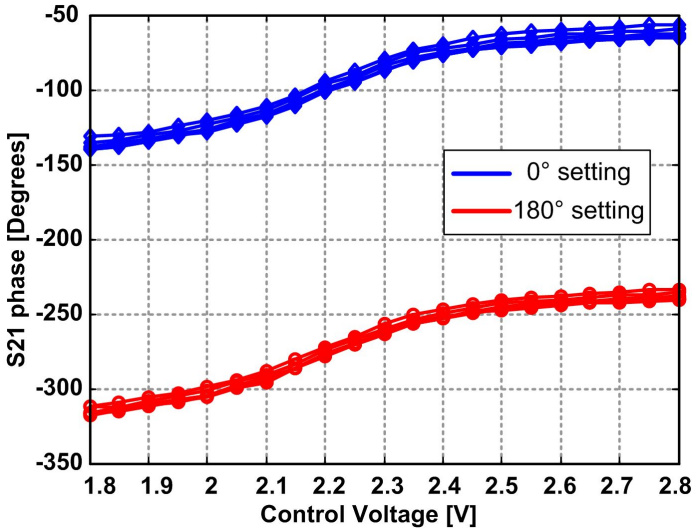
The array performance of the receiver chip can be extrapolated from the element s-parameters. Figure 6.27 shows the normalized array pattern at both `OutA` and `OutB`, across different modes of operation.

6.4 Extensions of Hybrid Series-Parallel Array Architectures

The hybrid series-parallel multibeam array architectures demonstrated in sections 6.1 and 6.2 can potentially be extended to arrays having a larger number of outputs and true-time delay based arrays. In this section, a theoretical analysis of some architectures is carried out to demonstrate the reduction in delay variation requirements in multibeam delay-based arrays.

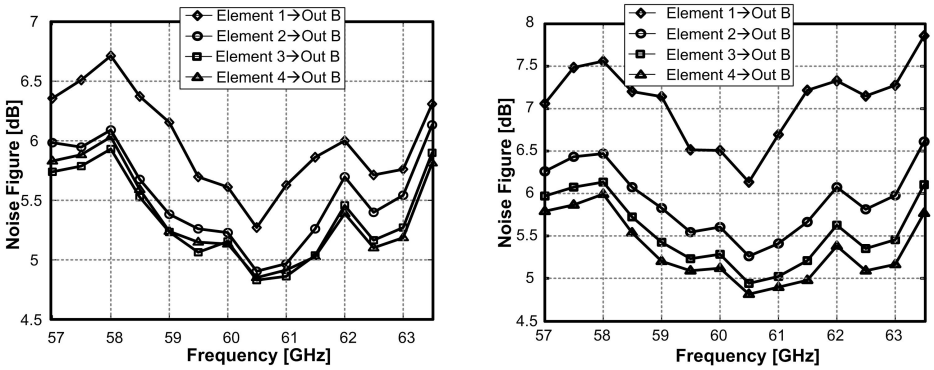


(a) Phase shift variation from Input 1 to `OutB`



(b) Phase shift variation from Input 1 to `OutB`

Figure 6.25: Measured phase shift variation from different inputs to `OutB`



(a) Noise figure (Phase shift: 135°) (b) Noise figure (Phase shift: 180°)

Figure 6.26: Element noise figure

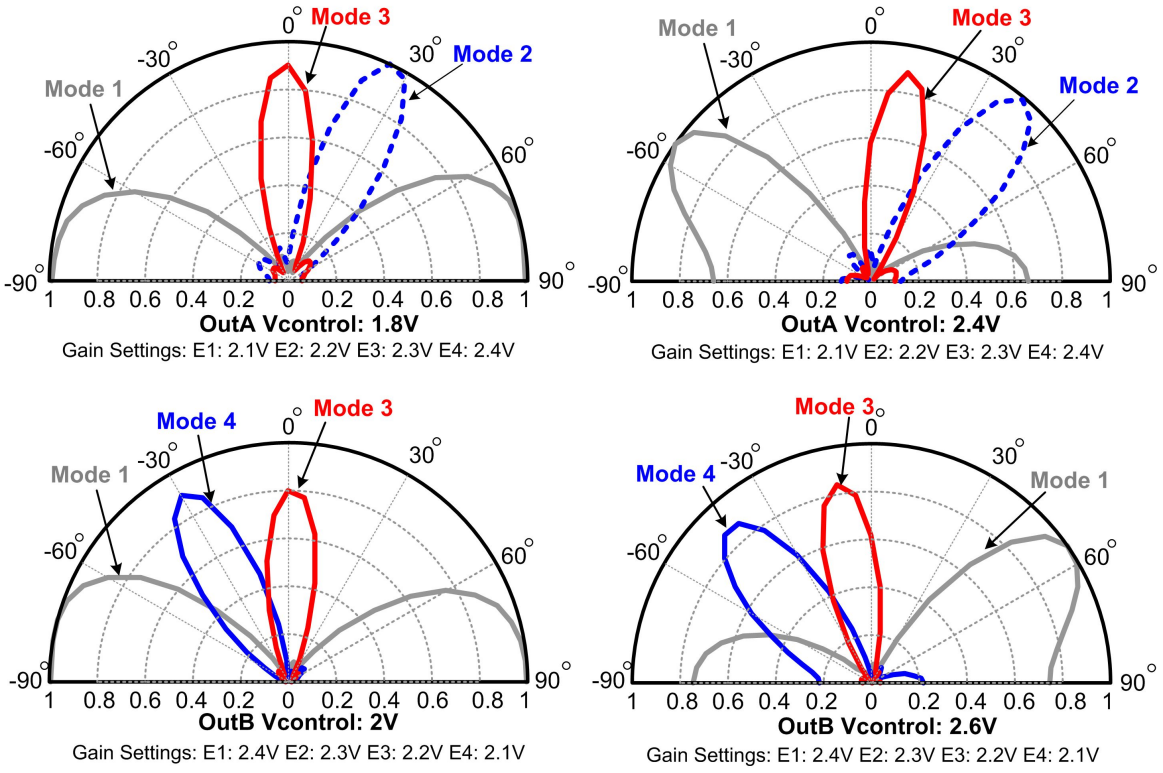


Figure 6.27: Normalized array pattern extrapolated from measured s-parameters

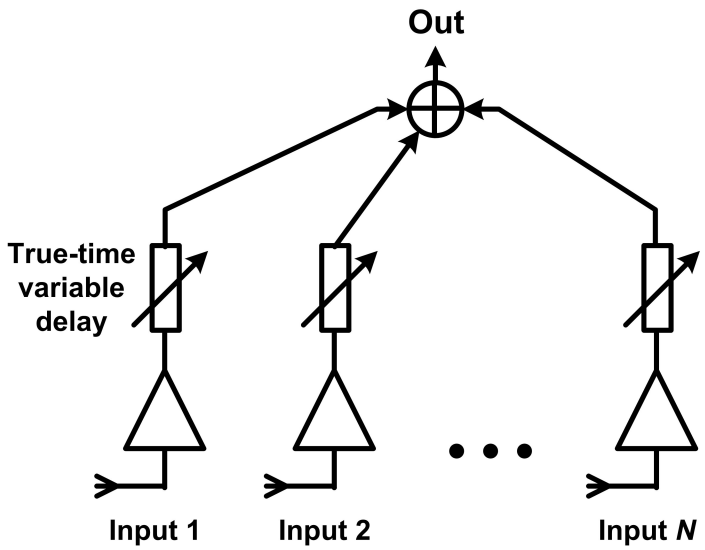


Figure 6.28: Parallel-fed time-delay based array

An array with true-time variable delay in each element, as shown in Figure 6.28, avoids the errors due to the narrowband approximation detailed in Section 3.4. However, in addition to the low-loss and large bandwidth requirements, time-delay based arrays present a challenge due to the large delay variation requirements that increase linearly with the size of the array. For e.g, in the parallel-fed array with N elements in 6.28, assuming antenna spacing $d = \frac{\lambda}{2}$ the required delay in Element 1 and Element N varies from 0 to $N\frac{T_0}{2}$, where T and λ are the time period and wavelength of the input signal[2]. Since the bandwidth of the variable delay cells degrades with an increase in the delay required (similar to the phase shifters in section 6.2.2.4), the large delay variation requirement makes it difficult to integrate wideband delay-based arrays.

As in the narrowband case detailed in section 6.1, the series-parallel hybrid delay architectures can be used in order to receive signals concurrently from different directions while reducing delay variation requirements. An example of such an architecture with three outputs is shown in Figure 6.29. Delay cells are required in

[2]This linear increase in required variation with an increase in number of elements does not occur in phase-shift based arrays due to the modulo-2π property of the phase shift

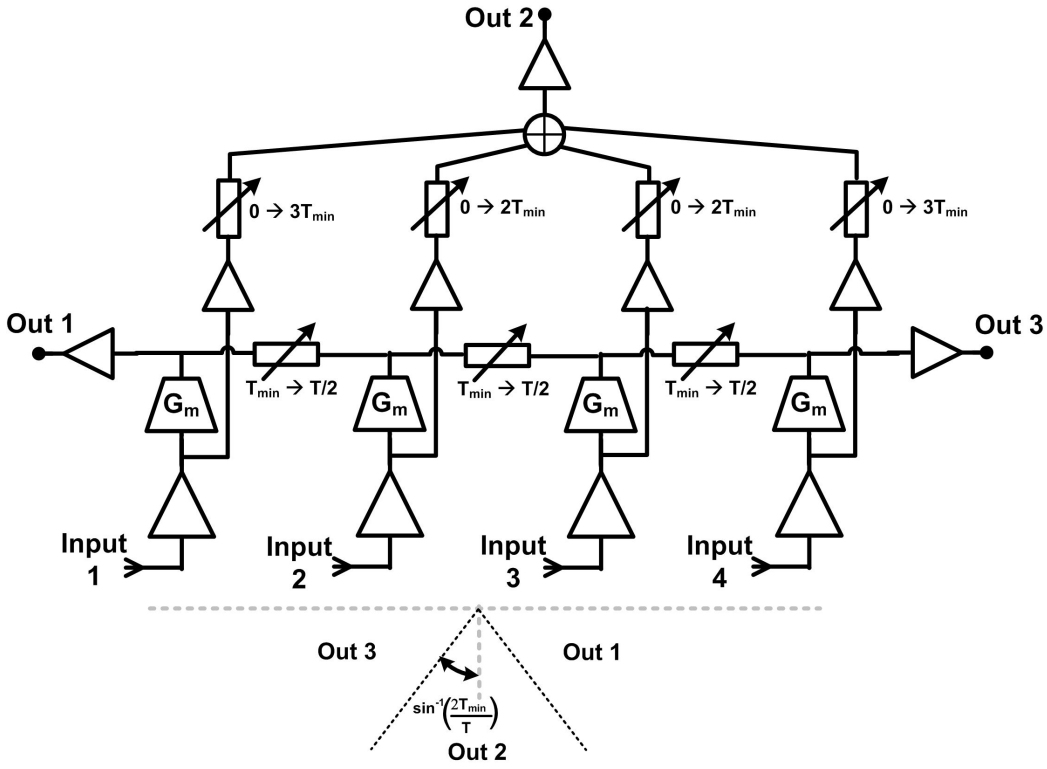


Figure 6.29: Hybrid time-delay based array

the parallel path since the series delay cells have non-zero minimum delay. If T_{min} in Figure 6.29 is set to be $\frac{T}{4}$, the series delay elements require a factor of two delay variation while the required variation in the parallel elements is reduced.

6.5 Chapter Summary

Multibeam architectures enable concurrent reception from different angles of incidence, while reducing the required phase variation in the variable phase shifters. In this chapter, a hybrid array architecture has been described that receives signals from two different directions simultaneously while reducing the phase-shifter variation requirement by a factor of 8 as compared to the parallel-fed array. The architecture was adopted in a 60GHz four-element phased-array receive front-end that was implemented in a commercial SiGe process. This represents the first efforts towards an integrated RF-combined phased-array at mm-wave frequencies. The complete four-element front-end consumes 88mA from a 2.7V supply and 12mA from a 2.2V supply leading to a total power consumption of 265mW. The front-end achieves a noise figure varying from 4.8dB to 6.2dB at 60GHz and measurements yield array performance that matches theoretical predictions. Extensions of the hybrid architecture that are suitable for true-time delay based arrays were also described in this chapter.

Chapter 7

Conclusion

The large available bandwidths and the smaller frequency size of multiple antenna systems make high frequencies very attractive for high data rate communication and sensing applications. Integration of such systems on silicon opens up several architectural possibilities that enable good system performance in non-traditional ways.

In this dissertation, different architectures for integrated phased arrays at mm-wave frequencies have been presented. A centralized LO-path phase shifting scheme was adopted in the first fully-integrated 24GHz phased-array transmitter that uses mainly 0.18μm CMOS transistors. Each element of the transmitter includes on-chip 24GHz PAs that generate up to 14.5dBm output power at 24GHz translating to an EIRP of 26.5dBm. The 4-bit LO-path phase-shifting approach adopted in the transmitter has better than 10° beam-steering resolution for radiation normal to the array. The transmitter is capable of supporting data rates in excess of 500Mbps, and is well-suited for 24GHz wireless links.

A local LO-path phase-shifting architecture was presented that enabled the first fully-integrated 77GHz phased-array transceiver. The architecture scales well with an increase in number of elements and/or frequency and provides high resolution phase shifting limited by the resolution of DACs. Each transmit element provides up to 12.5dBm output power at 77GHz leading to an EIRP of 26.5dBm. The

52GHz VCO has a tuning range of 9.7% from 50.35GHz to 55.49GHz while the injection-locked divider locks to the VCO input from 51.4GHz to 54.5GHz. Measurements show a VCO phase noise of -95dBc/Hz at 1MHz offset at 54GHz. A built-in *loopback* testing methodology was used to measure the array pattern which indicates good array performance.

While the 24GHz and 77GHz arrays are multiple-input single-output systems, higher-order phase-shifting and combining techniques can be used to achieve arrays with multiple outputs, with beams focused on different directions concurrently. A hybrid array architecture was described that receives signals from two different directions simultaneously while reducing the phase-shifter variation requirement by a factor of 8 as compared to the parallel-fed array. The architecture was adopted in a 60GHz four-element phased-array receive front-end that was implemented in a commercial SiGe process. This represents the first efforts towards an integrated RF-combined phased-array at mm-wave frequencies. The complete four-element front-end consumes 88mA from a 2.7V supply and 12mA from a 2.2V supply leading to a total power consumption of 265mW. The front-end achieves a noise figure varying from 4.8dB to 6.2dB at 60GHz and measurements yield array performance that matches theoretical predictions. Extensions of the hybrid architecture that are suitable for true-time delay based arrays were also described.

7.1 Recommendations For Future Investigations

The mm-wave phased arrays discussed in this dissertation demonstrate the feasibility of multiple-antenna systems in silicon. The last major element that is yet to be integrated with an acceptable degree of success is the antenna. The integration of on-chip dipole antennas in the 77GHz phased array transceiver in Chapter 5 brought into focus several challenges with achieving high-efficiency antennas on lossy silicon substrates. While certain techniques presented in [90] are promising for efficiency improvement, many issues related to antenna efficiency and

coupling to other parts of the system still need to be resolved before the antenna can be integrated along with the RF and baseband circuitry. Such integration is particularly advantageous for arrays with a large number of elements as it eases packaging requirements enormously.

In the context of large arrays, on-the-fly calibration and control circuits are also important for integrated systems. The scaling in CMOS technologies has led to larger process variations and temperature sensitivity which will result in inter-element variations in an array that will have to be calibrated out. Therefore, performance estimation algorithms, circuits for calibration and control, and architectures that lend themselves to easy calibration such as the local LO-path phase-shifting scheme are of great interest.

Multiple-beam architectures are also very attractive for large elements arrays for efficient utilization of the front-end circuits. Architectures, such as the hybrid array in Chapter 6, can be extended to larger number of outputs and to true-time delay based architectures that are suitable for sensing applications requiring large instantaneous bandwidth.

Given the high data rates that are possible at mm-wave frequencies, the power consumption of the A/D and digital circuitry is of concern. For certain applications operating at less than 5GHz, the challenges due to process variations and low dynamic range have been combated by pushing the digitization of the signal closer and closer to RF [56]. Exploring similar techniques for mm-wave systems by partitioning the analog and digital part of the system optimally for robust and low-power operation is an interesting challenge.

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Appendix A

Noise Environments

As detailed in Figure 2.16 in Section 2.5, the noise temperatures of the surroundings were measured in three different scenarios. Figure A.1, Figure A.2, and Figure A.3 show photographs of the measured environments, namely, an office, a corridor and a roof.

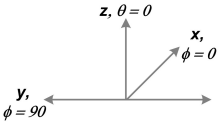

Figure A.1: Office

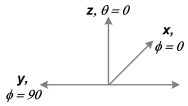

Figure A.2: Corridor

Figure A.3: Roof