ULTRA-DENSE NANO- AND MOLECULAR-ELECTRONIC CIRCUITS

Thesis by

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for Jennie

soulmate, best friend, accomplice

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Abstract of the thesis

This thesis describes research towards the realization of large-scale, ultra-dense nanowire-based circuits. The primary means for the construction of such circuits is the superlattice nanowire pattern transfer (SNAP) technique. This technique was optimized for the fabrication of large nanowire arrays containing over 1000 nanowires at narrow pitch and aligned over millimeter length scales. Silicon nanowire arrays were fabricated with wire widths down to ten nanometers, and with precisely-controlled electronic properties and bulk-like resistivity values through the use of diffusion doping and the selection of high-quality silicon-on-insulator substrates.

A binary tree demultiplexer circuit allows the unique addressing of N nanowires from within an ultra-dense array using of order $2\times\log_2(N)$ control wires. An implementation of this circuit was experimentally demonstrated to bridge from the submicrometer dimensions of lithographic patterning to the nanometer-scale dimensions of SNAP patterning. This circuit utilized field-effect gating by relatively large control wires to address individual nanowires from within a 150-nanowire array patterned at a wire width and pitch of 13 and 34 nanometers, respectively.

Silicon- and metal-nanowire arrays were integrated with [2]rotaxane molecular materials for the fabrication of an ultra-dense, 160,000-bit crosspoint molecular electronic memory circuit. This circuit is patterned at a record density of 1×10^{11} bits per square centimeter (device-pitch of 33 nanometers), and contains bistable, electrochemically addressable [2]rotaxane switching molecules as the data storage elements within the

individual crosspoint junctions. Defective junctions could be readily identified through electronic testing and isolated through software coding. The working bits could then be configured to form a functional memory circuit. The molecular-mechanical nature of the switching mechanism was confirmed through volatility measurements.

An optimized two-step chlorination/methylation protocol was used to methyl passivate thin (~20-nanometer) silicon(111)-on-insulator microelectronic device surfaces, that were then demonstrated to be stable in air for arbitrarily long periods, and to resist oxidation due to common microelectronic fabrication procedures and wet-chemical treatments. Additionally, temperature-dependent mobility data showed that methylated silicon-on-insulator surfaces can be prepared with bulk-like mobility characteristics through careful optimization of the methylation reaction protocol.

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Chapter 1

Thesis overview

1.1 Nanotechnology and nanoelectronics

The rapidly expanding fields of nanoscience and nanotechnology are within the midst of an extraordinary period of scientific and technological productivity, due in no small part to the unprecedented collaboration of researchers from across the physical, chemical, biological, and life sciences. The promise of functional systems at the nanometer (nm) length scale (1–100 nm) has spurred researchers in diverse disciplines to engage in fruitful collaborations across traditional academic boundaries and between academia, industry, and government[1]. The result has been a modern-day scientific renaissance as the talents of chemists, physicists, biologists and engineers are simultaneously leveraged to understand and exploit novel phenomena and functionality particular to the nanometer size regime. Emerging applications of nanotechnology range from ultra-dense information storage[2] to sustainable water purification[3], to *in-vivo* biological sensors and intelligent drug delivery systems[4], to 'smart materials' capable of sensing changes to their external environment and responding accordingly[5].

An exciting sub-field of nanotechnology is nanoelectronics and, in particular, molecular electronics[6]. Interest in this field has been fueled by the realization that the

technologies and materials systems currently in use by the semiconductor microelectronics industry cannot sustain the forty-year-old trend of device miniaturization into the coming decades. Indeed, the microelectronics industry had to overcome significant technical barriers to achieve the sub-100-nanometer dimensions of today's transistors, and such barriers are becoming increasingly numerous and more difficult to overcome as device dimensions continue to shrink. This is highlighted by a recent assessment[7] of the technology requirements for future generations of integrated circuits, which forewarns the emergence of insurmountable technical barriers (either physical or economical) by as early as the year 2010.

This has led to a growing consensus that continued improvements in computational technology will likely occur through the development of alternative materials, patterning methods, and architectures[7, 8]. To that end, the Heath group began a research program with the intent to develop the required materials, methods, and circuit architecture to construct an ultra-dense molecular electronic computer. The Heath group 'vision' for such an integrated circuit is shown in Figure 1-1. The dominant theme of this circuit is the crossbar architecture[6], which consists of two perpendicularly overlaid arrays of high-density nanowires. These nanowires tile together the various computational elements of the circuit (logic, memory, etc.), which are themselves derived from unique electrically active thin-film materials sandwiched between the nanowires at the locations shown in the figure.

My research has focused on a number of the components shown in Figure 1-1 for realizing this multifunctional computational architecture. These have included the development of techniques for patterning ultra-high-density arrays of silicon nanowires

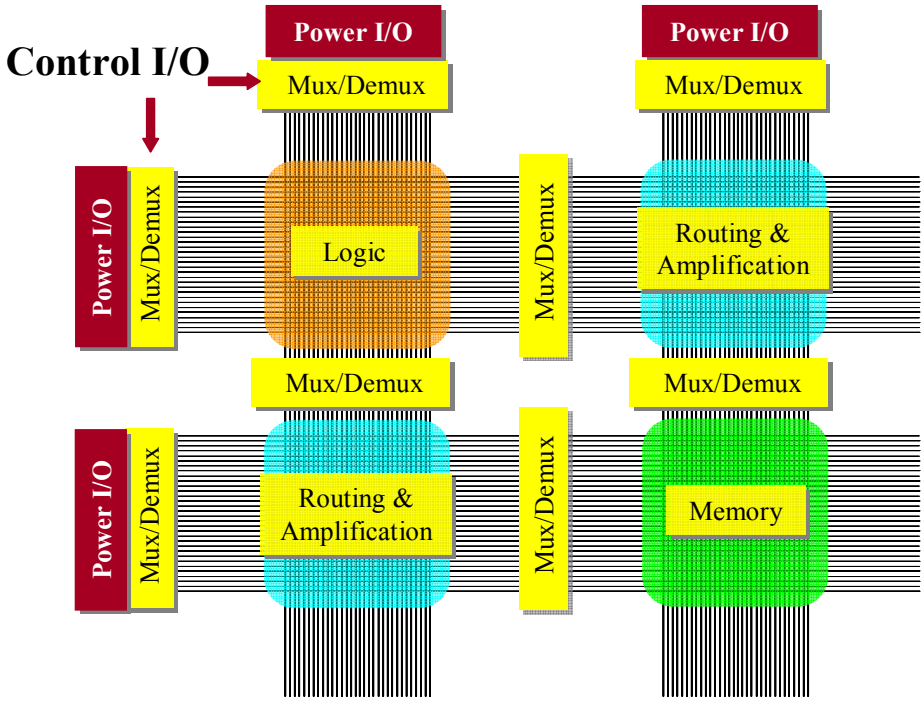

Figure 1-1. Schematic diagram of a nanoelectronic crossbar architecture. The various computational elements such as memory, logic, and routing are shown tiled together through nanowire arrays. Multiplexers (Mux) and/or demultiplexers (Demux) control signals within the circuit and to outside electronics (power I/O).

with precisely controlled electronic properties (Chapter 2), the demonstration of a field-effect transistor (FET)-based demultiplexer capable of bridging from the sub-micrometer length scales of conventional silicon microelectronic technology to the nanometer length scales of molecular electronics (Chapter 3), the integration of sub-lithographic patterning techniques and molecular materials for the fabrication of ultra-dense molecular electronic memory circuits (Chapter 4), and molecular-level control over nanoelectronic device surfaces (Chapter 5).

1.2 Organization of the thesis

To accommodate the largely independent, but closely related, projects which have comprised my graduate research in the Heath group at Caltech, I have chosen to organize this thesis into chapters—with each chapter completely self-contained and with its own background and references. The following sections will provide a brief overview the chapters in this thesis, summarizing the main results of the research described in each chapter and (hopefully) providing some overall unity to the topics discussed individually in the chapters.

1.2.1 Fabrication of ultra-dense nanowire arrays

In Chapter 2, I describe research directed towards the development of high-quality arrays of silicon and metallic nanowires. One-dimensional nanostructures such as nanowires are useful in a wide variety of applications in nanotechnology[9], and have emerged as the fundamental building blocks of novel nanoelectronic circuits. Such structures can be fabricated using highly parallel techniques and assembled into ultra-dense crossed-nanowire (crossbar) circuits such as shown in Figure 1-1. Nanowires not only propagate electrical signals throughout the circuit, but can also serve as the active components within the circuit. This dual functionality results in significant savings in wiring overhead, and enables crossed-nanowire circuits to be fabricated at the incredible densities I describe in Chapter 4.

There are a number of methods for the fabrication of silicon nanowires, with most based on the catalytic growth of nanowires from molecular precursors[9]. However, this technique has a number of significant drawbacks for application to large-scale nanoelectronic circuitry. For one, crossbar circuits fabricated from catalytically-grown nanowires are usually limited in size to around 10 micrometers, and to date have contained at most 100 junctions[10]. Additionally, the techniques required to align catalytically-grown nanowires are rather complicated and generally imperfect. This makes their integration with lithographically-defined structures such as binary tree decoder circuits (discussed in Chapter 3) awkward and difficult. Dr. Nick Melosh, a former post-doc in the Heath group, developed a method in which high-density arrays of silicon or metal nanowires could be patterned without such a limitation. This method is called the superlattice nanowire pattern transfer, or SNAP, technique and allows the fabrication of dense arrays of nanowires aligned over millimeter length scales.

Chapter 2 describes my efforts to systematically remove much of the phenomenology that had previously plagued the SNAP technique and the extension of SNAP to higher-density and larger-element arrays of nanowires. In addition, Chapter 2 will describe my efforts in developing reliable doping protocols and eliminating fabrication-induced nanowire defects to achieve bulk-like conductivity characteristics from narrow-width silicon nanowires.

1.2.2 Demultiplexing ultra-dense nanowire arrays

The SNAP technique is capable of producing arrays of metal and silicon nanowires with dimensions (width and pitch) beyond the capabilities of conventional lithographic techniques. However, such dense circuitry provides a new challenge for the field of nanoelectronics, namely, how to electrically address circuits that have characteristic wire dimensions and pitches that are smaller than the resolution achievable through lithographic patterning. The selective addressing of, and interaction with, individual nanostructures at high densities is one of the central challenges of both nanoscience and nanotechnology—in the absence of a resolution to this problem, many of the potential benefits of these emerging fields will remain unrealized. For instance, the nanowire-based molecular electronic memory circuit described Chapter 4 is nearly two orders of magnitude denser than conventional circuitry. However, the lack of a robust technology to selectively address individual nanowires from within an ultra-dense array reduces the effective density of such a circuit to that of conventional (lithographically-defined) circuitry.

Chapter 3 describes research by my co-workers (Dr. Robert Beckman, Dr. Ezekiel Johnston-Halperin and Dr. Yi Luo) and me to demonstrate a FET-based nanowire demultiplexing architecture that can be patterned with significantly larger dimensions than the nanowires it addresses, and with wide alignment tolerances. Its shown that this architecture successfully interfaces with high-density SNAP-fabricated nanowires to bridge the dimensional gap between nanometer-scale circuitry and conventional patterning technology[11].

1.2.3 Ultra-dense crossbar molecular electronic circuits

In 2002, the Heath group reported on the use of bistable [2]rotaxane molecules as the active elements within a 64-bit molecular electronic random access memory (RAM) circuit that utilized micrometer-scale wiring[12]. Although this work successfully demonstrated that molecules could be used store information within a solid-state crossbar circuit, it did not take advantage of the unique scalability offered by molecular components.

Chapter 4 is devoted to what has comprised the majority of my research efforts in the Heath group, namely, the integration of SNAP-fabricated arrays of silicon and metal nanowires with molecular materials for the fabrication of an ultra-dense, 160,000-bit molecular electronic crossbar memory circuit patterned at a record density of 100 gigabits per square centimeter (1×10^{11} bits cm^{-2})[13]. The construction of this memory circuit was a true *tour de force* in nanofabrication that would not have been possible without the efforts my colleague, Jang Wook Choi. In addition, numerous other members of the Heath and Stoddard group (at UCLA) made important contributions to this effort[13].

Beginning with a description of the rich science underlying the switching mechanism of bistable [2]rotaxane molecules and their integration into high-density crossbar architectures, Chapter 4 covers, in depth, the fabrication and operation of the memory circuit. The work described in this chapter shows that molecules *can* be used as scale-invariant components in solid state circuitry and, moreover, that functional circuitry *can* be assembled at macromolecular dimensions. A false-colored image of a typical molecular memory circuit is shown in Figure 1-2.

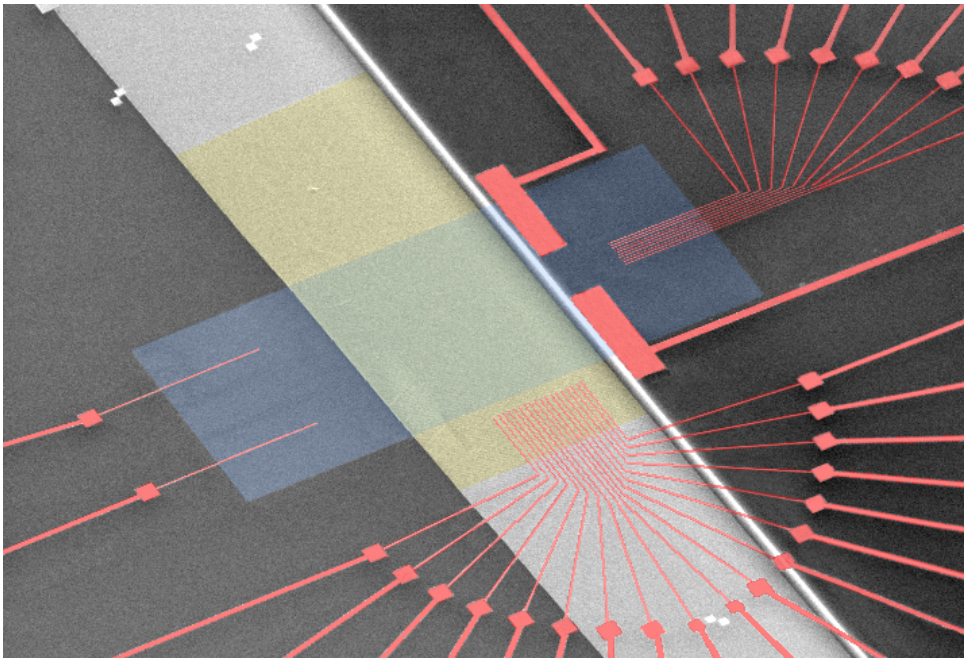

Figure 1-2. A false-colored scanning electron micrograph of a molecular electronic memory circuit fabricated from [2]rotaxane molecular materials and SNAP-fabricated silicon and titanium nanowires. The memory region is defined by the intersection of 400 silicon nanowires (light blue) and 400 titanium nanowires (light yellow), and contains 160,000 bits in an area of 13×13 square micrometers (or 1×10^{11} bits per square centimeter).

1.2.4 Covalent modification and electrical characterization of silicon-on-insulator devices

As the feature sizes of silicon devices continue to be scaled towards nanometer dimensions, the physical and chemical properties of the surface play an increasingly prominent role in determining the overall device behavior. This has presented significant challenges, and opportunities, to the nanotechnology community, where surface effects manifest over a range of applications from nanoelectromechanical systems (NEMs)[14] to electrical transport in thin silicon-on-insulator (SOI) films[15].

Covalent alkyl passivation of silicon surfaces is attractive for a variety of nanoelectronic applications, such as FET-based demultiplexing and molecular electronics. However, the majority of work with alkyl-passivated, (111)-oriented silicon surfaces has utilized bulk wafers. While such wafers are convenient for surface characterization studies, they are less useful for the nanoelectronic applications of interest to us, where SOI structures are generally required. This last chapter of my thesis describes ongoing work to obtain high-quality methyl passivation of ultra-thin (111)-oriented SOI devices and their subsequent electrical characterization using variable-temperature conductivity and mobility measurements. Using an optimized (for SOI devices) version of the surface methylation protocols developed by the Lewis group at Caltech[16], robust methyl passivation of silicon surfaces was achieved with devices as thin as 20 nanometers thick. Chapter 5 presents data showing that this passivation is resistant to oxidation for extended periods of time in ambient air, and after exposure to an assortment of common nanofabrication procedures and chemical treatments. Additionally, temperature-dependent mobility data shows that methylated ultra-thin surfaces can be prepared with bulk-like mobility characteristics.

1.3 References

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Chapter 2

Fabrication of ultra-dense nanowire arrays

2.1 Introduction

The development of arrays of semiconducting and metallic nanowires (NWs) will undoubtedly be important for the realization of any future nanoelectronic circuit architecture. NWs serve to not only propagate electrical signals into and out of a circuit, but can also function as the active components within the circuit. For example, NWs have been used to fabricate nanoscale field-effect transistors (FETs)[1-6], p-n diodes[7, 8], bipolar junction transistors[7], nanoscale electro-mechanical oscillators[9, 10], lasers[11], LEDs[12], complex logic gates[13], and complementary inverters with signal gain[14]. This economy of functionality makes NWs an ideal building block for assembling larger and more-complicated nanoelectronic circuits since the fabrication of such circuits can be accomplished with little additional complexity[15]. For instance, aligned arrays of NWs can be used to fabricate a crossbar structure (an expanded ticktacktoe board) by repeating the NW fabrication procedure twice with the second set of NWs fabricated on top of, and perpendicular to, the underlying first set of NWs. By implementing a computational function at the intersection of two NWs, such as logic or memory, a crossed-nanowire

circuit containing $N \times M$ electronic devices can be fabricated from two constituent N- and M-nanowire arrays. The device-to-device pitch is limited by the pitch of the NWs, so the ultimate density of a NW crossbar circuit is limited by the dimension and pitch of the technique used to form the NW arrays. This has driven researchers in the field to develop methods for assembling NW arrays at very narrow pitch. The scalability and manufacturability of crossbar circuits has lead to an emerging consensus that future nanoelectronic applications (not necessarily limited to conventional computational functions, such as memory and logic) will most likely be based on the crossbar architecture[16-19].

In addition to NWs, single-walled carbon nanotubes (SWNTs) have gained considerable attention from the nanotechnology community. Carbon nanotubes are cylindrical, rolled-up sheets of graphene that are about a nanometer in diameter and possess remarkable electronic, thermal, and mechanical properties (excellent reviews are available from Hongjie Dai[20] and Paul McEuen[21]). Current synthesis techniques produce a mix of semiconducting and metallic nanotubes (with about two-thirds being semiconducting), and while great progress has been made to separate the two[22], nanotube electronics continues to be hindered in the absence of a high-throughput separation technique. This is in contrast to semiconductor NWs, where the electrical properties can be precisely controlled through doping. In addition, NW length, width, and morphology can be tailored during fabrication. Considerations such as these have made semiconducting NWs the dominant structure for building nanoelectronic circuits containing more than just a handful of devices.

For electronics applications, the semiconducting material of choice is silicon. The physical and mechanical properties of silicon have been well characterized and there are highly developed protocols for patterning and electrically contacting silicon devices. An additional benefit is the possibility of integration onto a conventional CMOS technology platform, thus opening the door for relatively near-term commercial applications.

The versatility of Si NW-based electronics has fueled intense research and development of semiconductor NW fabrication protocols to enable the parallel fabrication of large numbers of NWs of specific geometry and with precisely controlled electrical properties.

The most widely used Si NW fabrication technique is the vapor-liquid-solid (VLS) growth mechanism[23, 24]. A typical procedure is to heat a gold nanocluster in the presence of vapor-phase silicon (usually SiH_4 in an H_2 carrier gas) to the Au-Si eutectic temperature (363° C), resulting in the formation of a liquid droplet of Au-Si alloy. As vapor-phase silicon is continuously fed into the reaction chamber, the droplet becomes supersaturated and solid silicon precipitates out of the melt. As long as there is silicon precursor in the reaction vessel to keep the droplet supersaturated, a Si NW grows from the solid-liquid interface with the supersaturated droplet riding on top. This process can be fine tuned to produce Si NWs with reasonably well controlled lengths and diameters[25] (which is primarily determined by the diameter of the Au catalyst). However, the VLS NW fabrication technique faces some significant challenges. VLS-grown NWs tend to be limited in length to around 10 micrometers (μm)[26], which in turn limits their practical applicability to anything other than small-scale nanoelectronic circuits. The precise electrical properties of VLS-grown NWs are generally unknown before they are wired up

since the NWs are doped *in-situ* by adding dopant precursor to the reaction vessel. Additionally, while the VLS technique can be used fabricate large numbers of NWs in parallel, subsequent procedures are required to align the NWs into arrays and crossbar circuits[24]. The most successful procedure to date employs a Langmuir-Blodgett (LB) trough[27] to align the NWs parallel to one another. However, this technique suffers from fluctuations in the average alignment direction and poor end-to-end registry of individual NWs. This makes interconnecting and integrating such arrays into larger (especially CMOS-compatible) circuitry difficult. In addition, the LB technique would be difficult to scale-up for the commercial manufacture of NW circuits.

2.2 The SNAP nanowire fabrication technique

2.2.1 Introduction to SNAP

The ability to assemble nanoscale building blocks such as Si NWs into integrated nanoelectronic structures at narrow pitch (and therefore high density) is a general challenge in nanotechnology. The majority of work in the field has focused on few-device demonstrations of scaling feature size, and has largely neglected such considerations as feature pitch, device-to-device reproducibility, and manufacturability—all of which are required for any robust application. The superlattice nanowire pattern transfer (SNAP) technique was developed within the Heath group[10] to simultaneously address these issues. The SNAP technique is a 'top-down,' non-photolithographic technique that enables the fabrication of ultra-dense arrays of high aspect ratio (length-to-

width ratio routinely > 10^6) Si and/or metal NWs that are aligned over millimeter length scales, and without the need for a secondary alignment step after NW fabrication. NW width and wire-to-wire pitch are highly reproducible and the technique is compatible with conventional CMOS technology and adaptable for large-scale manufacturability. Furthermore, the SNAP technique permits precise control of the electrical characteristics of Si NWs through quantitative doping control. These traits make the SNAP technique ideally suited for realizing large-scale NW circuits.

My initial research efforts in the Heath group were devoted to optimizing the SNAP procedure so that fabrication of Si NW arrays with precisely controlled electrical properties would be routine and reproducible. Previous efforts were successful in using SNAP to generate arrays of 128 Si NWs of widths down to 20 nm, but only a fraction of those NWs conducted, and none exhibited bulk-like conductivity characteristics[10]. We found that Si NWs of widths of less than 30 nm are critically sensitive to the defects introduced by standard processing methods such as ion-implantation doping. Nanowires significantly smaller than 50 nm in width (~25-nm thick) and longer than 10 μm will often contain at least one such defect, and the result is a poorly conducting wire. However, by moving to diffusion doping we were able to improve the conductivity of our Si NWs by a factor of 10^3, and to demonstrate that Si NWs with diameters of 10 nm and lengths in excess of 1 mm can be fabricated with controllable, bulk-like conductivity characteristics and useful field-effect transistor properties[28]. In what follows I will describe the efforts of my coworkers and I to optimize SNAP NW fabrication procedures for extending the SNAP technique to arrays of 400 NWs for use in ultra-dense crossbar

memory circuits, in addition to achieving bulk-like conductivity from SNAP-fabricated Si NWs. I will begin with a general description of the SNAP NW fabrication protocol.

2.2.2 Detailed description of SNAP nanowire fabrication

SNAP uses molecular-beam epitaxy (MBE) to create a physical template for NW patterning. This template is a custom-grown gallium arsenide/aluminum gallium arsenide ($GaAs/Al_xGa_{(1-x)}As$) superlattice structure consisting of alternating layers of GaAs and $Al_xGa_{(1-x)}As$ grown on top of a (100) GaAs substrate. The mole fraction x ranges from 0.5 to 0.8; for clarity, the subscripts will be omitted in what follows. For typical applications, the AlGaAs layer thickness determines the NW width and the GaAs layer thickness determines the separation between NWs. Because MBE is capable of growing layers with atomic resolution, the NW width and separation can in principle be reduced to just a couple of atomic layers. In practice, however, NWs have been limited to about 7–8 nm in width and 15 nm in pitch[29], although, as of this writing, we haven't pushed very hard on this limit.

The number of alternating layers of GaAs and AlGaAs determines the number of NWs in the array. To date, we have successfully used the SNAP technique to fabricate arrays containing up to 1400 NWs[29]; however, there is no reason (in principle) why we couldn't increase this number considerably.

The SNAP fabrication protocol begins by carefully dicing a portion of the superlattice wafer into small rectangular pieces approximately 2 mm wide and 5 mm long (Figure 2-1.A). These pieces will henceforth be referred to as masters for reasons that will become obvious. The masters are cleaved from the parent GaAs/superlattice wafer

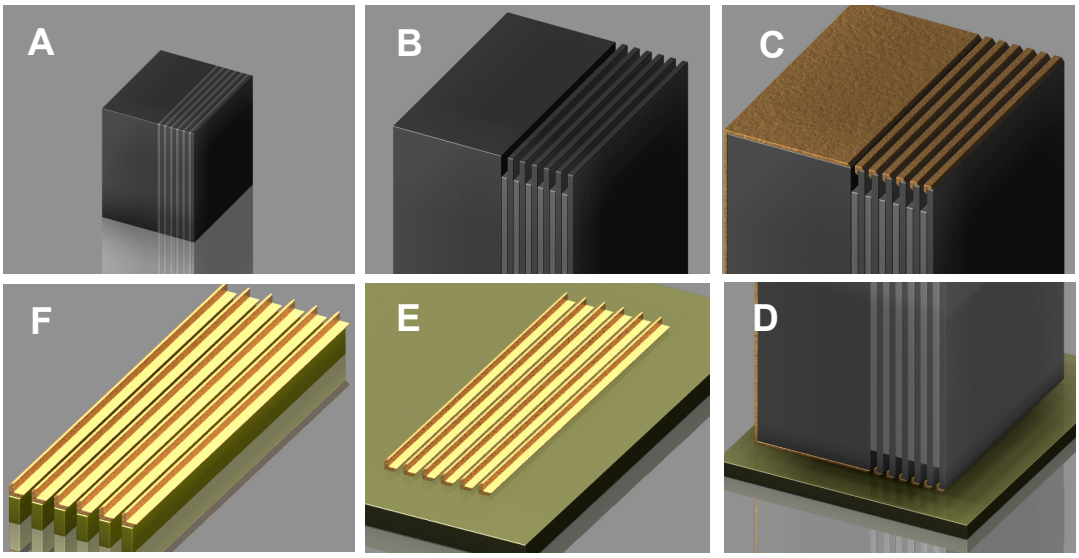

Figure 2-1. The major steps in SNAP nanowire fabrication (clockwise direction) A. A small piece of the GaAs/AlGaAs superlattice is selectively etched, **B**, forming a comb-like structure. **C.** Pt is then deposited along the ridges of the comb. **D.** The superlattice template is adhered to an epoxy-coated thin-film substrate. **E.** The superlattice is released from the Pt nanowires and, **F**, the Pt nanowire pattern is transferred into the underlying thin film.

such that one of the 2-mm-wide edges of the master is precisely along a lattice direction. This leaves an atomically flat {110} or {001} plane exposed on that edge (depending on the direction of cleave). The masters are then loaded into a custom-made Teflon holder with the atomically flat edge facing up. They are sonicated in methanol (~10 seconds at a time) and the atomically flat edge is gently swabbed until all particulates visible under a 160× magnification optical microscope are removed. The superlattice region of the master is scrupulously cleaned before proceeding since a single micrometer-sized piece of debris can (and frequently does) result in unsuccessful NW fabrication. I have found that small particulates relatively far away from the superlattice region are not usually a problem and can be ignored. Also, particulates that cannot be removed from sonication and swabbing may come off in the subsequent etch step.

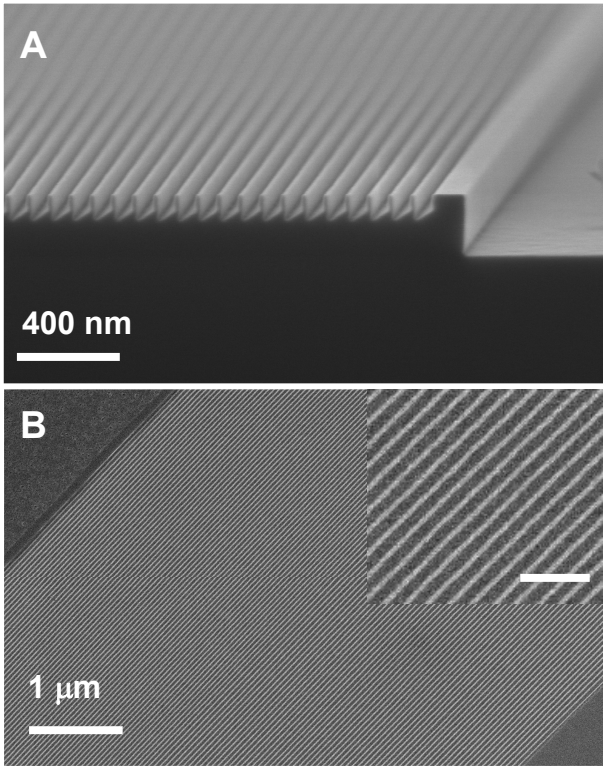

Figure 2-2. Scanning electron microscope (SEM) images of SNAP nanowire fabrication. A. Partially etched GaAs/$Al_{0.5}Ga_{0.5}As$ superlattice showing the $Al_{0.5}Ga_{0.5}As$ ridges forming the Pt nanowire template. **B** 128 12-nm-wide Si nanowires generated by using the transferred Pt nanowires as an etch mask. The inset is a higher-resolution image revealing the incredible fidelity obtained with the SNAP process. The scale bar is 150 nm.

The GaAs (or AlGaAs) layers are selectively etched in an NH_4OH-H_2O_2 etch solution to form a comb-like structure (Figures 2-1.B and 2-2.A) and 10 nm of Pt is then deposited with the superlattice surface oriented at 45° with respect to the evaporative flux of an electron-beam-evaporated Pt source (Figure 2-1.C). The orientation of the superlattice determines how much metal is deposited along the ridges of the AlGaAs (or GaAs) comb, which defines the Pt NW template. The metal-coated superlattice is then applied to a thin (~10 nm) layer of heat-curable epoxy spun onto a substrate with a thin-film epilayer (Figure 2-1.D). To ensure that the epoxy spins down uniformly, the surface is rigorously cleaned beforehand. The epoxy is then baked in two steps for 10 minutes and 30 minutes at approximately 100° C and 135° C, respectively. After curing, excess epoxy is removed by a high-power, 100-Watt (W) oxygen reactive-ion etch (RIE) at 5 milliTorr (mTorr). The superlattice template is released from the Pt NWs by etching the GaAs/AlGaAs superlattice in either commercially available gold-

etch solution (4 g KI + 1 g I_2 into 100 ml H_2O) or 1:5:50 solution of 30% H_2O_2 to conc. H_3PO_4 to H_2O; both for 3–5 hours*. The epoxy between the Pt wires is subsequently removed in another oxygen RIE step (40W, 5 mTorr).

At this stage the SNAP procedure has produced an array of Pt NWs adhered to a thin-film substrate (Figure 2-1.E). The Pt NWs can then be used as an etch mask in an anisotropic RIE to transfer the NW pattern into the thin-film substrate (Fig 2-1F). The highly versatile SNAP technique can be used to fabricate NWs out of any thin-film material that can be anisotropically dry-etched. To fabricate Si NWs, the Pt NW pattern is adhered to a doped silicon-on-insulator substrate. High-fidelity pattern transfer with vertical side walls is accomplished using a high-frequency RIE tool (40 MHz Unaxis SLR parallel-plate RIE) and fluorine-based reactive-ion etching at low substrate bias (10–20 volts DC). An etch recipe of CF_4, He, and H_2 (20:30:2.5) at 40 W and 5 mTorr was found to give vertical Si sidewalls with no observable undercut. (The added hydrogen promotes the deposition of a fluoropolymer on the Si NW sidewalls to prevent undercutting.) However, I found that this etch would occasionally reduce the conductivity of boron-doped NWs. One possible explanation is that hydrogen in the etch was diffusing into the NWs and forming a boron-hydrogen complex[30]. This complex results in passivation of the dopant so it can no longer produce free charge carriers. For thin Si epilayers, I have found this problem can be avoided without altering the etch fidelity by simply removing H_2 from the recipe. The Si etch end-point is determined by interferometry, although the etch efficiency may be lower between the narrow-pitched Pt NWs than where the actual laser spot is positioned (due to residual epoxy and Pt NW

* A lower bound for the etch time is given by (thickness of superlattice region)/etch rate. The phosphoric acid etch rate is ~0.1 μm/min at room temperature. The KI/I_2 etch rate was not measured but is estimated to be ~0.2 μm/min.

charging effects). To ensure complete transfer of the Pt NW pattern into the underlying Si film, the etch time is usually extended by 25–50 percent. Over-etching is not a problem for most applications since this only results in transferring the NW pattern into the underlying oxide by a small fraction (CF_4 etches Si and SiO_2 equally[31] in pure CF_4). After transferring the Pt NW pattern to the underlying Si epilayer, the final step is to remove the Pt NWs in hot aqua regia (1:4 conc. HCl to conc. HNO_3 at 120° C, ~10 min). The result is an array of Si NWs on an insulating oxide that are aligned and continuous over hundreds of microns (Figure 2-1.E & Figure 2-2.B).

The selective GaAs etch, Pt evaporation angle, and epoxy formulation are all key for obtaining high-quality NW arrays. Accordingly, I will discuss each in more detail below.

2.2.3 Selective etching of GaAs on AlGaAs

The SNAP technique relies on a physical template for NW fabrication. The construction of this template requires not only the fidelity of MBE to define alternating layers of GaAs and AlGaAs, but the ability to etch GaAs with high selectivity. One of my goals was to optimize this etch for various GaAs/AlGaAs superlattice structures. Although I will only consider the selective etching of GaAs over AlGaAs, as an alternative AlGaAs can be selectively etched over GaAs[10] using a buffered-oxide etch solution (BOE) (6:1 NH_4F to HF). Selective etching of AlGaAs is generally avoided because BOE is hazardous to work with. However, the ability to alternatively etch AlGaAs instead of GaAs can be useful for reversing the NW width and spacing for a given superlattice.

The GaAs etch must be highly selective to GaAs over AlGaAs so that the AlGaAs ridges of the comb are not rounded. It also needs to be controllable so that the etch parameters can be calibrated to produce a consistent etch depth. The optimal etch depth is dependent on the GaAs layer thickness and the Pt evaporation angle. This can be seen from the cross-sectional schematic of a GaAs/AlGaAs comb shown in Figure 2-3.A. Each AlGaAs ridge acts as a self-aligned shadow mask for the ridge behind it. Since the evaporation angle must always be less than 90° to avoid depositing metal into the GaAs recess, the Pt lines actually have an 'L' structure, where the dimensions of the 'L' depend on the angle of evaporation (Figure 2-3.B). The metal extends along one side of each

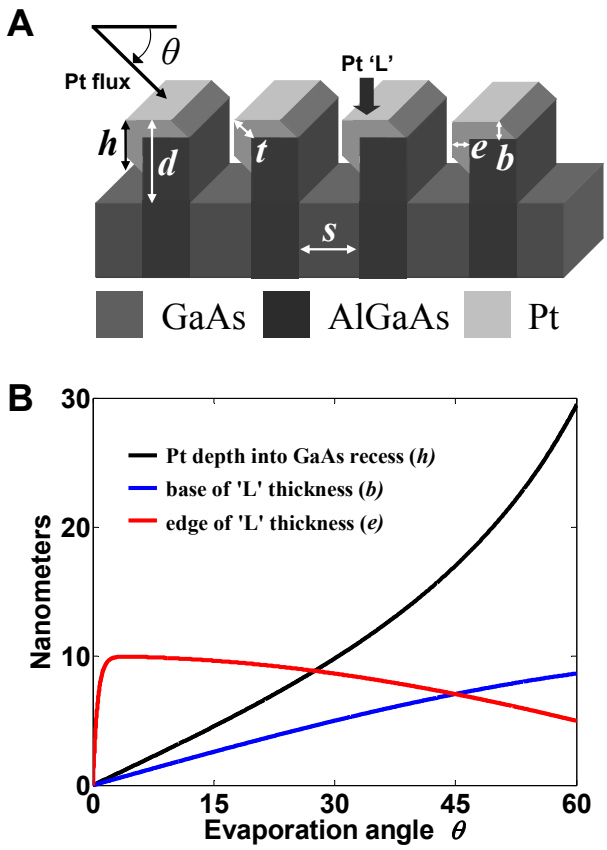

Figure 2-3. Pt deposition onto an etched GaAs/AlGaAs template. A. Cross-sectional diagram of a portion of the etched GaAs/AlGaAs template. Pt is evaporated onto the AlGaAs ridges at an angle θ forming an upside-down 'L' structure (right-side up after depositing the Pt NW array) with base and edge thicknesses b and e, respectively. Pt coats one side of each AlGaAs sidewall to a depth, h, that depends on θ and the AlGaAs spacing, s. **B.** Calculated dimensions of the Pt 'L' as a function of θ for a superlattice with AlGaAs spacing s = 17 nm and evaporated Pt thickness t = 10 nm. The evaporation angle is chosen to give the best Pt nanowire morphology within the constraint that h is less than the GaAs etch depth, d. For the superlattice considered here, this is 45° (see text).

AlGaAs ridge into the GaAs recess (*h* in Figure 2-3.A) for all relevant evaporation angles (*i.e.*, $0° < \theta < 90°$) and increases with both the evaporation angle (Figure 2-3.B, black line) and the spacing of the AlGaAs layers. For maximum applicability to different superlattices and varying evaporation angles, it is desirable for the GaAs etch to produce a GaAs recess as deep as possible.

I explored two etch chemistries* and a range of etch concentrations on superlattices containing 128, 150, and 400 alternating layers of GaAs/AlGaAs with layer thicknesses of 10 nm/20 nm, 10 nm/25 nm, and 15 nm/20 nm, respectively. The 128- and 150-wire superlattices were grown by University of California Santa Barbara with mole fraction of Al $x = 0.5$. The 400-wire superlattices were grown from either University of California Santa Barbara or IQE Inc. (Bethlehem PA) with mole fraction of Al $x = 0.8$. The two etch solutions were 1:20 conc. NH_4OH to 30% H_2O_2[32] and 5:1 50% aqueous citric acid ($C_6H_8O_7$) to 30% H_2O_2[33, 34]. Aqueous citric acid was prepared by dissolving 1 gram of anhydrous $C_6H_8O_7$ per milliliter of H_2O. These stock solutions were diluted by varying margins in H_2O before use. Extra wide masters (about 4–5 mm) were cleaved from a given superlattice along a lattice direction and subsequently etched for times ranging from 5 seconds to 20 seconds, then rinsed with de-ionized (DI) (18 MΩ) water, and dried under N_2. After etching, each master was cleaved lengthwise into halves and loaded onto a scanning electron microscope (SEM) puck with one piece laid on its side with the fresh cleave facing up. This way a top-down view showing the registry of the AlGaAs ridges as well as a cross-sectional view to measure the etch depth could be obtained from the same master. Figure 2-2.A was generated in this fashion.

* An acetic acid-based etch was also tried but was found to be inferior to the NH_4OH and $C_6H_8O_7$ etches.

Both of the etch solutions were found to have excellent selectivity for GaAs over AlGaAs. While the citric-acid etch in dilutions ranging from undiluted to 1:5 (stock solution to H_2O) and etch times from 6 to 30 seconds, respectively, produced good results for the 128-wire superlattice, we found the NH_4OH-H_2O_2 etch solution diluted by a factor of 15 in H_2O to be easier to prepare and more consistent from one run to another and for different superlattices. Using this etch solution, the maximum (reliable) GaAs etch depth was found to be 30–40 nm, corresponding to 10–12 seconds of etch time. Longer etch times occasionally resulted in collapsed or broken-off AlGaAs ridges.

After etching the IQE-grown 400-wire superlattice in NH_4OH-H_2O_2 solution, I frequently observed small aggregates (< 50 nm) of what appeared to be solid Ga on the superlattice surface (Figure 2-4). This excess Ga may originate from a Ga-rich reconstruction[35] of the exposed {001} crystal plane after cleaving along the ⟨110⟩

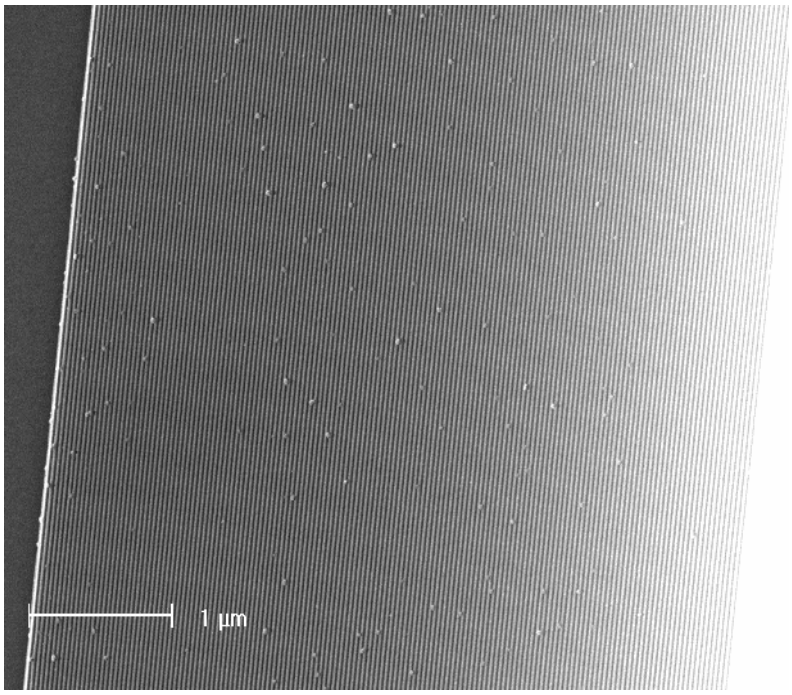

Figure 2-4. Scanning electron micrograph (SEM) of a freshly-etched 400-nanowire GaAs/AlGaAs superlattice. This master was not treated with an additional H_2O_2 dip, and aggregates of solid Ga can clearly be seen dispersed over the GaAs/AlGaAs layer surface.

direction (the direction along the IQE wafer flat). I found these aggregates could be oxidized and removed from the superlattice surface by a 5-second dip in undiluted 30% H_2O_2 immediately following the NH_4OH-H_2O_2 etch. Although Ga aggregates on the superlattice surface were found to be present only after cleaving along the ⟨110⟩ or ⟨010⟩ directions, the extra H_2O_2 treatment was adopted as a standard step in the NH_4OH-H_2O_2 etch procedure. (In the very least, this step helped to remove particulates from the superlattice surface.)

2.2.4 Optimum platinum evaporation angle

In addition to the GaAs etch, I systematically investigated how different Pt evaporation angles affected the Pt NW morphology. Smooth Pt NWs are important because they must serve as a high-fidelity stencil to define arrays of Si or other thin-film material NWs. Ideally, Pt should only deposit along the AlGaAs ridges so that the transferred Pt NWs are as symmetrical as possible. This requires a small evaporation angle to reduce the depth of evaporated Pt along the side of individual AlGaAs ridges (Figure 2-3.B, black line). However, this was found to also increase the roughness of transferred Pt NWs along their corresponding side. This roughness is likely due to the accumulation of Pt along one side of the AlGaAs ridge as a result of the small evaporation angle (Figure 2-3.B, red line). Larger evaporation angles gave smoother Pt NWs, but to also increased the depth of evaporated Pt along AlGaAs ridges (Figure 2-3.B, black line). After some trial and error, I found that a 45° evaporation angle worked the best. A 45° angle consistently

produces smooth Pt NWs while being shallow enough that evaporated Pt does not reach the bottom of the GaAs recess (Figure 2-3.B).

2.2.5 Epoxy formulation

Optimizing the epoxy formulation for high-yield SNAP-NW fabrication has proven to be quite difficult, and numerous members of the Heath group have worked to establish a reliable formulation. In fact, one of my initial efforts in the Heath group was to investigate the use of amine-terminated self-assembled monolayers (SAMs) on silicon to replace the epoxy altogether as a Pt NW adhesive. We found that SAMs could produce small arrays of aligned Pt NWs over distances of up to 50 μm, but reliable alignment over longer distances and larger NW arrays was very difficult. To date, two epoxy formulations are used in the Heath group; both are modifications of Epoxy Bond 110 (Allied High Tech, Rancho Dominguez California). Both formulations include a polymeric additive that functions as a plasticizer to make the epoxy easier to etch in the oxygen plasma steps described above. The first version uses a PMMA additive (0.37 g of 6 % PMMA, 20 drops of Epoxy Bond part A, 2 drops of Epoxy Bond part B, 15 ml of chlorobenzene). This epoxy recipe etches easily in O_2 but does not adhere to the substrate as well as the following recipe using dibutyl phthalate as a plasticizer: 5 drops part A, 1 drop part B, 2 drops of dibutyl phthalate, 10 ml of anhydrous tetrahydrofuran (THF). The latter recipe was used exclusively for the fabrication of crossbar circuits, described in Chapter 4. The epoxy is spun onto a clean substrate at 5000 RPM to achieve a film

thickness of about 10 nm. (Note that film thickness is critical to ensure good pattern transfer.)

2.3 Achieving bulk-like conductivity of silicon nanowires

To maximize the conductivity of our Si NWs, we undertook a systematic investigation[28] of the relative importance of the defects native to our SOI substrates as compared to defects introduced through processing techniques such as doping and reactive-ion etching (RIE). A *p*-doped Si (100) epilayer grown via MBE represented our 'gold standard' for fabricating high-quality Si NWs; this substrate was used to assess how the RIE transfer of the NW pattern from Pt to Si affected Si-NW conductivity. NWs fabricated from the MBE substrate then served as a metric for comparison to commercially available 4-inch SOI wafers (defect density = 0.23 cm^{-2}) and industry-standard 8-inch SOI wafers (defect density < 0.1 cm^{-2}). In addition, NWs fabricated from 4-inch SOI wafers were used to compare ion-implantation doping to diffusion doping from a spin-on dopant source. As expected, NWs fabricated from the higher quality 8-inch SOI wafers resulted in better-conducting Si NWs. The use of spin-on doping resulted in a more dramatic improvement in NW conductivity, and has proved to be essential for reliably obtaining conductive Si NWs below 50 nm in width.

The Si-NW resistivity was used as the figure of merit for NW quality. To facilitate resistivity measurements, Si-NW arrays were sectioned into multiple regions of length 5–25 μm with each section contacted by two sets of Ti/Al/Pt (10 nm/150 nm/20 nm) electrodes via electron-beam lithography and thin-film metal deposition and lift-off.

Individual NWs were 10–15 nm wide and each electrode addressed 2–4 NWs (Figure 2-5.A inset). The contacts were subsequently annealed at 450° C for 5 minutes in argon to promote ohmic contact formation. Four contacts allow the measurement of two sets of wires per region and cross-conductance measurements between sets to measure leakage current.

Figure 2-5.A (filled circle) shows a current-voltage (*I-V*) trace for a 7-μm-long section of Si NWs fabricated from the MBE substrate (30 nm of Boron:Si on intrinsic Si, $p = 1\times10^{19}$ cm^{-3}); the linearity of the trace confirms the ohmic nature of the contacts. The histogram in Figure 2-5.B represents many such resistance measurements normalized by the bulk-scaled resistance, R_o, and reveals the bulk-like conductivity of these NWs despite their narrow width of ~10 nm. The good morphological properties of these NWs apparently correspond to good electronic properties, confirming that the RIE recipe described above does not damage the NWs.

In contrast, when Si NWs were fabricated from the same substrate used in previous studies[10] (ion-implantation doped 4-inch SOI wafer; 25 nm of boron-doped Si on 150 nm of SiO_2; $p = 3\times10^{19}$ cm^{-3}), the R/R_o histogram was centered at 10^4 (not shown), indicating that the electrical properties of those NWs were severely degraded. The most probable cause is lattice defects from ion-implantation methods. Ion-implantation doping uses a high-energy beam of ionized dopant atoms to implant dopants into the Si substrate. These high-energy dopants collide with Si atoms in the lattice and produce point defects that degrade the conductivity of the substrate. Post-implantation thermal annealing can alleviate most of these defects[36], but for NWs of narrow width (~10 nm here) even a small number of doping-induced defects can dramatically affect

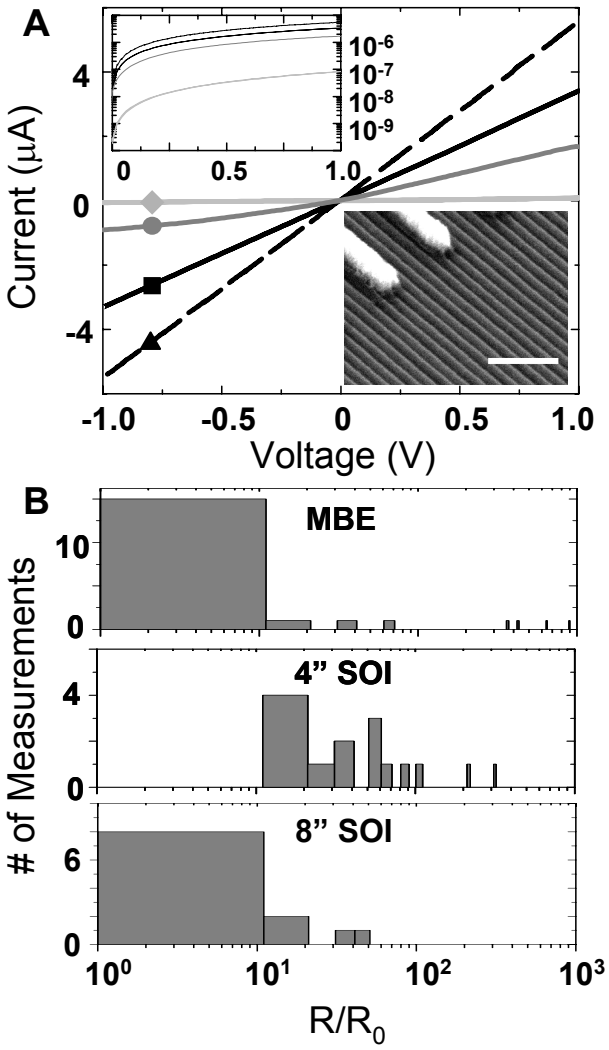

Figure 2-5. **Si nanowire electrical properties. A**. IV measurements of 4 nanowire samples (all samples doped via spin-on diffusion doping): ■ 8" SOI, p=5e19cm^{-3}, 10nm×31nm×3μm ▲ 8" SOI, n=1e20cm^{-3}, 10nm×31nm×3μm ● MBE, p=1e19cm^{-3}, 10nm×30nm×7μm ♦ 4" SOI, p=5e18cm^{-3}, 10nm×25nm×2.5μm. Upper-left inset shows data plotted on a semi-log scale. Lower-right inset shows an SEM image of the nanowire contacts; scale bar is 200 nm. **B**. Statistical distribution of normalized nanowire resistance (R/R_o) for various substrates. R/R_o values for ion-implantation doped Si NWs are greater than 10^3 and are not shown. The bin size is 10.

NW conductivity. This is confirmed by the observation that we could reliably fabricate conductive NWs from ion-implanted substrates down to 50 nm in width, but NWs of 10–15 nm in width were frequently poor conductors. Consequently, we moved to spin-on doping as an alternative to ion-implantation doping. This method forgoes the use of ion-implantation and instead uses high-temperature annealing to gently diffuse dopant atoms into the Si lattice from a spin-on dopant source.

To test the efficacy of spin-on doping to improve NW conductivity, we used SNAP to fabricate Si NWs from a 4-inch SOI substrate doped with the spin-on doping technique (25 nm of Si on 150 nm of SiO_2, p = 5×10^{18} cm^{-3}). Figure 2-5.A (filled diamond) shows

an *I-V* scan[*] for a 3-μm-long section of these NWs, and Figure 2-5.B shows a histogram of the normalized resistance constructed from several such *I-V* scans. Although the normalized resistance is still a factor of ten higher than the bulk-scaled resistance, NWs fabricated from spin-on doped substrates are a thousand-times-better conductors than their ion-implantation doped counterparts. This dramatic increase in NW conductivity is the result of eliminating lattice defects from ion-implantation doping, and highlights the importance of spin-on doping for the fabrication of conductive NWs with narrow widths.

Improving NW conductivity by another factor of ten, and thus achieving bulk-scaled NW resistance, was accomplished simply by using a lower-defect-density SOI wafer as the starting material (8-inch industry-standard SOI[†] instead of 4-inch SOI). Figure 2-5.A (filled square) shows a typical *I-V* scan for NWs fabricated from a spin-on doped 8-inch SOI wafer (30.8 nm of Si on 145 nm of SiO_2, 3-μm long, $p = 5\times10^{19}$ cm^{-3}); and Figure 2-5.B, the normalized resistance, which is comparable to the resistance histogram of NWs fabricated from the MBE substrate. Phosphorous-doped NWs fabricated from 8-inch spin-on doped SOI (30.8 nm of Si on 150 nm of SiO_2, 3-μm long, $n = 1\times10^{20}$ cm^{-3}) also show bulk-scaled resistance (statistical data not shown) and a typical *I-V* scan is showed in Figure 2-5.A (filled triangle, dashed line).

The SNAP technique was additionally used to fabricate high-quality Si NWs with a (111) surface orientation from bonded silicon(111)-on-insulator wafers (Isonics Semiconductor, Vancouver, WA.; 40 nm of Si on 2 μm of SiO_2). In accord with the

[*] A slight non-linearity in the IV scan at voltages below 250 mV is observed, but length-dependent resistance measurements revealed linear (ohmic) scaling implying that the observed resistance is dominated by the native NW conductivity and not by the contacts.

[†] Further confirmation of the superior quality of 8-inch industry standard SOI over 4-inch SOI comes from the observation that 4-inch SOI shows substantial leakage current through the insulating oxide while the 8-inch SOI does not.

versatility of the SNAP technique, no modification was required to the procedures that were described above in the context of (100) SOI wafers. The (111) SOI epilayer was 80-nm thick as received, but was thinned to 40 nm through sacrificial dry thermal oxidation and BOE wet etching. The wafer was then diffusion doped with phosphorus using the spin-on doping method ($n = 1\times10^{20}$ cm^{-3}), and the SNAP technique was used to fabricate 150-element arrays of Si(111) NWs on top of an insulating oxide (Figure 2-6.B, inset). The Si NWs were sectioned into regions 1 μm in length, then contacted and tested as described above. Figure 2-6.A shows representative *I-V* scans from these NWs and Figure 2-6.B shows a histogram of the normalized resistance constructed from several such *I-V* scans.

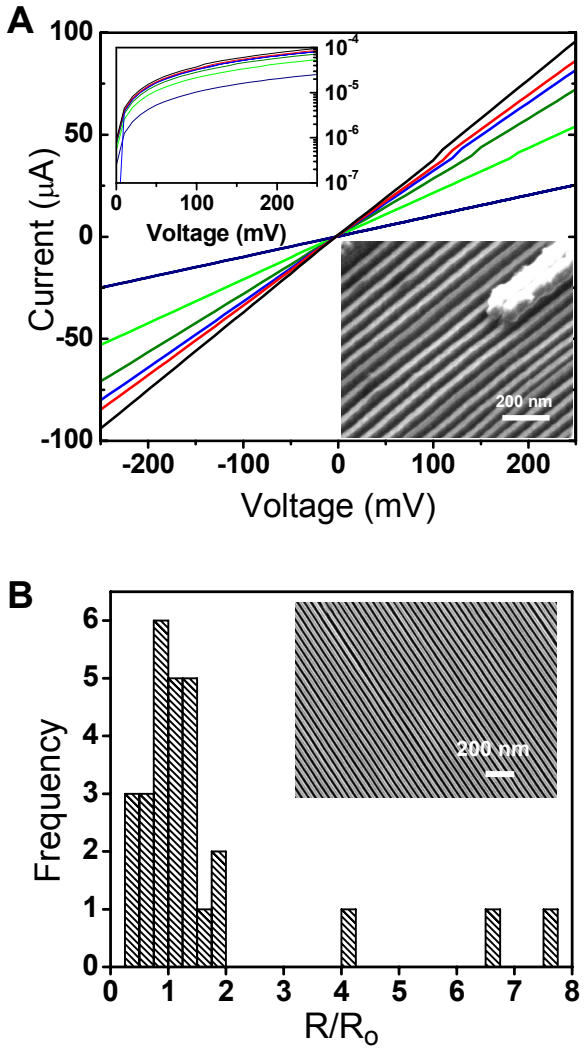

Figure 2-6. Electrical properties of Si(111) nanowires. A. Representative current-voltage scans from 6 sets of Si(111) nanowires showing linear response and high conductivity. The top-left inset shows the same data plotted on a semi-log scale and the bottom-right inset shows a nanowire contact. **B.** Statistical distribution of normalized nanowire resistances (R/R_o). The bin size is 0.25. The inset shows a zoomed-in SEM image of 15-nm wide nanowires within a 150-element Si NW array. The scale bar is 200 nm.

By comparing the normalized NW resistance histograms of Figures 2-5.B and 2-6.B, it is seen that Si NWs

fabricated from the (111)-oriented SOI substrates are better conductors than those fabricated from (100)-oriented SOI substrates. (The R/R_o distribution for the Si(111) NWs is more sharply peaked at unity.) This provides further evidence of the detrimental effects that ion-implantation processes have on Si NW conductivity. The buried oxide layer of the (100) SOI wafers used in the study above were created (commercially) using the *separation by implanted oxygen* (SIMOX) technique. This process is similar to ion-implantation doping in that it bombards the silicon surface with an energetic beam of ions. Oxygen ions are implanted into the Si substrate to form a buried SiO_2 layer separating the Si epilayer from the substrate. Like ion-implantation doping, a post-implantation anneal does not repair all of the implantation-related defects in the Si epilayer. In contrast, the (111) SOI wafers were fabricated (commercially) using a bonding technique whereby two oxidized Si wafers are bonded together at their SiO_2 surfaces, thus forming a SOI structure without the need for oxygen ion implantation.

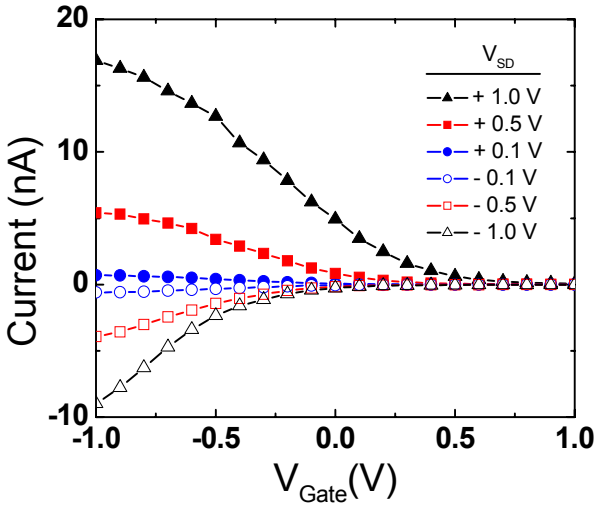

Figure 2-7. P-type nanowire gating response for various values of the source-drain voltage. The asymmetry in source-drain bias is attributed to asymmetrical Schottky barriers.

Using NWs fabricated from a 4-inch spin-on doped SOI substrate (7.5-μm long, $p = 5\times10^{18}$ cm^{-3}), a crossbar-FET was constructed by depositing 7 nm of Al_2O_3 over the NW array, followed by a 250-nm-wide metallic wire as a gate. Figure 2-7 shows the gating response for

various values of the source-drain voltage. An impressive modulation in conductivity was obtained through a gate bias of just ±1V. (Although difficult to see in the figure, we could tune the NW conductivity by a factor of 10^3.) These results show that by minimizing defects at all stages of NW fabrication we can fabricate Si NWs with bulk-scaled conductance that are highly responsive to field-effect gating.

2.4 Silicon nanowire doping

The observation that diffusion-doped Si NWs are thousand-fold-better conductors than their ion-implantation-doped counterparts makes diffusion doping an important part of the SNAP NW fabrication protocol. In what follows, I will discuss the technical aspects of diffusion doping using spin-on dopants for use in SNAP NW fabrication.

Most spin-on dopants consist of the desired dopant species (such as phosphorus or boron) incorporated into a SiO_2 polymer-matrix and dissolved in an organic solvent. This dopant solution is spin-coated onto a clean Si chip and baked at an intermediate temperature to drive off solvent. This results in the formation of a thin, dopant-rich SiO_2 film on the Si surface that provides a virtually infinite source of dopant atoms. The chip is then annealed at high temperature in an inert environment to facilitate diffusion of dopant atoms from the dopant-rich SiO_2 film into the Si lattice. This method provides a simple and gentle route for doping SOI epilayers that is compatible with batch-processing for manufacturability.

The spin-on doping procedure consists of four steps: cleaning the wafer, applying the dopant, annealing and removing the dopant. Because spin-on doping requires high

temperatures, the wafer must be rigorously cleaned to ensure all organic material is removed. To remove organic contamination I frequently used 'piranha clean' (2:1 H_2SO_4 to H_2O_2, 120° C, 10 min) followed by an RCA clean (5:1:1 H_2O to H_2O_2 to NH_4OH, 80° C, 10 min; followed by 1:10 BOE to H_2O, 25° C, 10 sec; followed by 5:1:1 H_2O to H_2O_2 to HCl, 80° C, 10 min). The piranha step was usually omitted if the wafer had not come into contact with photoresist. The RCA clean usually removes small particulates in addition to organic contaminates, but this should be checked under a microscope. If any particulates are found, sonication and swabbing of the wafer surface in methanol is required.

After ensuring that the wafer is clean, the dopant solution is generously applied to the wafer surface using a syringe and a 0.2-μm PTFE filter. The wafer is then spun at 4000 RPM and subsequently baked on a hotplate set at 200° C for 10 min. I obtained the best results for n-type doping using Emulsitone (Whippany, NJ) phosphorosilicafilm (phosphorus concentration = 5×10^{20} cm^{-3}) and for p-type doping using Emulsitone Borosilicafilm (boron concentration = 5×10^{20} cm^{-3}). The n-type dopant was frequently diluted by a factor of ten in methanol for easier removal after annealing, but can be used as is without difficulty. However, I regularly had difficulty removing the p-type film after annealing unless it was ten-fold diluted in methanol before use.

The dopant-film-coated wafer is then annealed under nitrogen in a rapid thermal annealer (RTA) for the appropriate time and temperature to achieve a given doping concentration. After annealing, the n-type dopant is removed with brief sonication in acetone followed by swirling in BOE until the surface is hydrophobic (usually less than 10 seconds). The p-type dopant frequently required acetone sonication and swabbing

before using BOE to remove the dopant film. If the surface is not hydrophobic after 15 seconds in BOE, I found a brief piranha clean followed by soaking in water and another 10 seconds in BOE to be effective.

To determine the correct anneal time and temperature to achieve a given doping, small test pieces of the substrate to be doped are annealed under various conditions to construct a look-up table of measured dopant density for particular anneal parameters. To determine the doping, I used a home-built four-point probe to measure wafer resistivity and calculated the dopant density from an empirical equation relating dopant density to Si resistivity. Although this technique is widely used to measure dopant density, it should be emphasized that sheet resistivity measurements only give an integrated average of the dopant density through the thickness of the measured substrate.

To obtain an estimate of the proper anneal time and temperature for a given doping, I started by modeling the diffusion of dopant atoms into Si. Taking the thickness of the Si epilayer to be infinite and the dopant concentration at the surface to be constant, a 1-D diffusion model $\left(\frac{\partial C}{\partial t} = D(T)\frac{\partial^2 C}{\partial d^2};\ C(d=0) = C_{surface},\ C(d \to \infty) = 0 \right)$ gives

$$C(d,t,T) = C_{surface}\ erfc\left(\frac{d}{2\sqrt{D(T)t}} \right), \qquad (1)$$

where *erfc* is the complementary error function, C is the dopant concentration, $C_{surface}$ is the concentration of dopant atoms in the spin-on dopant film, d is the depth into the Si epilayer, t is the anneal time, and $D(T)$ is the temperature (T)-dependent diffusivity. For Si, $D(T)$ is given by the empirical relation

$$D(T) = A\exp\left(-\frac{E}{8.6\times10^{-5} T/K} \right) \qquad (2)$$

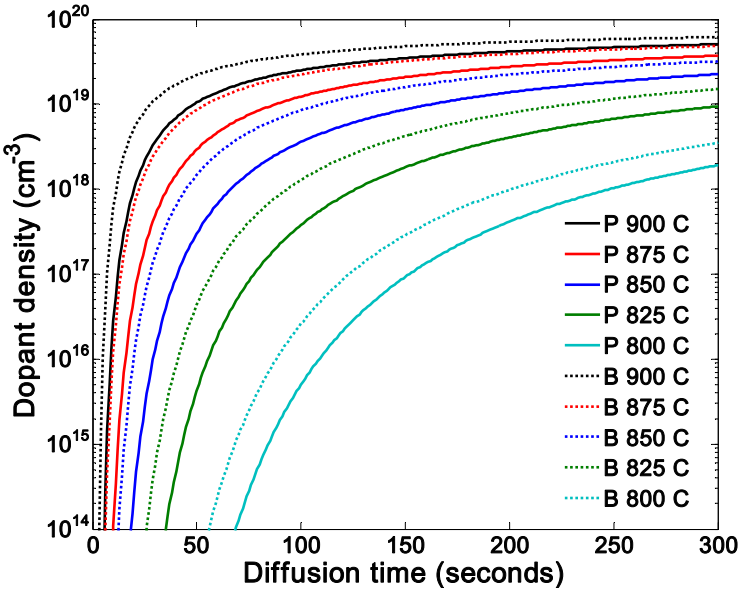

Figure 2-8. Calculated dopant concentrations as a function of diffusion time for various anneal temperatures. Calculations are for P and B diffusion in Si from a spin-on dopant (SOD) of concentration 1×10^{20} cm^{-3}. For other SOD concentrations, multiply by the appropriate scale factor (*e.g.*, multiply by 5 for a SOD concentration of 5×10^{20} cm^{-3}) Depth was taken to be the doping-weighted integrated average (~6 nm for a 5 minute anneal at 900 C). B and P diffusivity parameters were taken from ref. 37.

with A and E constants that depend on the diffusing dopant atom. For phosphorus (boron) diffusion, A = 8x10^{-4} cm^2/s (0.06 cm^2/s) and E = 2.74 eV (3.12 eV)[37]. Figure 2-8 shows the calculated density of P (n-type doping) and B (p-type doping) in Si as a function of anneal time for various anneal temperatures. Using equation (1) as a guide, several SOI substrates with Si epilayer thicknesses from 25–50 nm were annealed under various conditions to study diffusion doping in our SOI substrates. Figure 2-9.A shows the measured (filled circles) and calculated (dashed line) n-type dopant density for 50-nm SOI after various anneal times at 900° C. Both experiment and calculation reveal a latent period before any appreciable doping occurs, after which the dopant density rises sharply before asymptotically approaching C_{surf}. Analogous behavior is observed with 31-nm (Figure 2-9.B) and 25-nm (Figure 2-9.C) SOI epilayers. The (intuitive) trend from this dataset is that higher-temperature anneals produce a sharply rising dopant density that

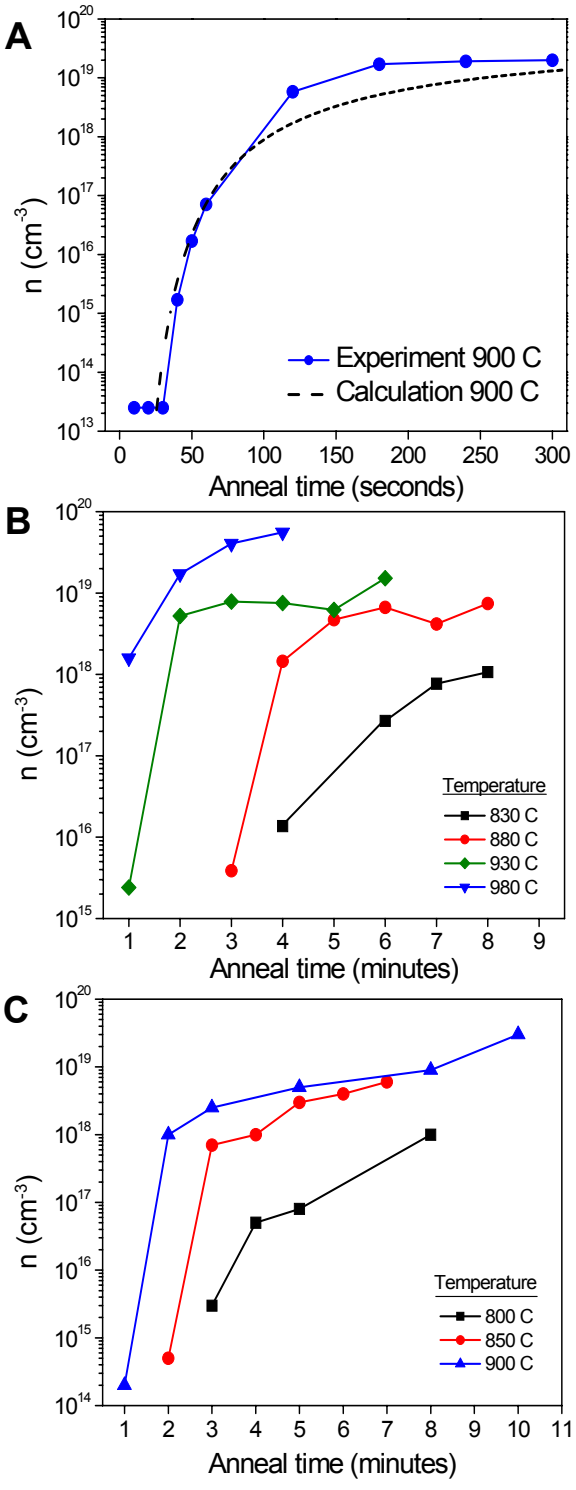

Figure 2-9. Time and temperature dependence of phosphorus doping in SOI substrates A. 50-nm SOI; note the good agreement between the calculated and measured dopant densities. **B.** 31-nm SOI. **C.** 25-nm SOI.

subsequently flattens out at high doping, while lower-temperature anneals produce a slow, monotonically increasing dopant density requiring long anneals to achieve dopant densities greater than 1×10^{18} cm^{-3}.

For the higher anneal temperatures, dopant density rises by many orders of magnitude over a small time interval making it difficult to reliably obtain a given dopant density by varying the anneal time (especially for densities lower than $\approx 1\times10^{19}$ cm^{-3}). A better approach is to adjust the anneal temperature while fixing the anneal time to achieve a rough dopant density, and to adjust the anneal time for fine tuning.

The doping profile as a function of depth into the Si epilayer was determined

experimentally (Figure 2-10 blue triangles and red squares) by thinning a 50-nm Si epilayer (via CF_4-based RIE) in 10-nm increments and measuring the doping (via 4-point resistivity) after each increment. As expected, diffusion doping produces a dopant density gradient that falls rapidly with depth into the Si epilayer. Note that the infinitely-thick Si epilayer model (Figure 2-10, dashed line) agrees well with experiment over most of the epilayer thickness (Figure 2-10, blue triangles).

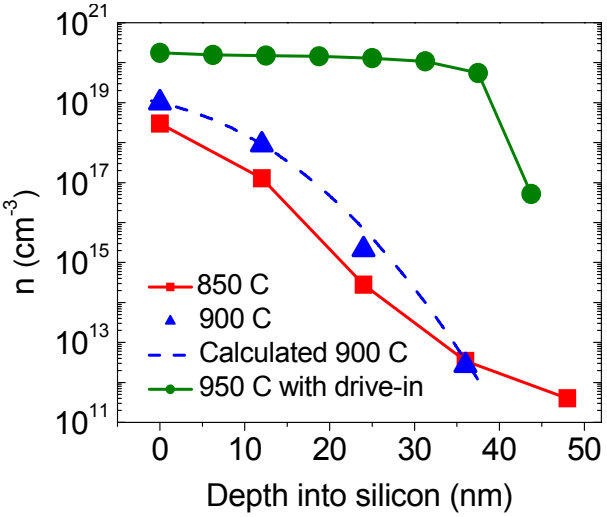

Figure 2-10. Dopant density vs. depth for 50 nm SOI substrates with and without dopant drive-in. Si epilayers that were diffusion doped as normal (triangles and squares) show a rapid decrease in dopant density with depth as expected from calculation (dashed line). SOI subjected to an additional dopant drive-in step as described in the text show a more homogeneous dopant density with depth (circles).

This dopant density gradient will be transferred to SNAP-fabricated Si NWs from diffusion-doped SOI epilayers, and can be very useful for nanoelectronic applications. For instance, the dopant density and hence the conductivity along the length of SNAP-fabricated Si NWs can be tuned very simply by etching the NW surface in regions where the conductivity is to be decreased. The appropriate etch depth to achieve a given doping density can be determined from a dopant density vs. depth plot corresponding to the anneal time and temperature of the starting SOI epilayer.

The ability to spatially control the conductivity of SNAP-fabricated Si NWs has important applications in NW crossbar circuit architectures. Si NWs can be made highly-

doped in regions where electrical signals must propagate and moderate- to lowly-doped in regions that need to be responsive to field-effect gating. This becomes especially important when tiling together multiple nanoelectronic functional blocks fabricated from a single array of NWs. In Chapter 3, I describe the application of this technique to a FET-based demultiplexer.

There are applications where a homogeneous dopant density is desired. For instance, in Chapter 4, I describe the fabrication of an ultra-dense memory circuit made from crossed NW arrays in which Si NWs are unavoidably etched but must nonetheless maintain robust conductivity. In cases such as this, the dopant density can be homogenized with a secondary high-temperature anneal. After diffusion-doping as usual, approximately 250 nm of SiO_2 is deposited over the SOI surface. I frequently used plasma-enhanced chemical deposition (PECVD) for this step. This oxide layer prevents out-gassing of dopant atoms during a second anneal at 1000° C for 10–15 minutes. Due to the long anneal time and high temperature of this step, I used a tube-furnace and an argon ambient. If perfect homogeneity is not required, a shorter anneal at 1000° C will suffice. (Most RTAs are capable of staying at 1000° C for 2 minutes.) Figure 2-10 (dark green circles) reveals that the dopant density vs. depth profile after drive-in is nearly constant throughout the 50-nm Si player (the abrupt drop in dopant density at 45-nm depth may be due to increased surface resistance from RIE damage and/or uneven etching of the surface).

2.5 Concluding remarks

As described in this chapter, the SNAP technique is a highly versatile NW fabrication protocol capable of producing dense arrays of aligned NWs over millimeter length scales. Furthermore, because SNAP is a 'top-down' technique, NWs can be fabricated from any thin-film material that can be anisotropically dry-etched. The physical properties of the NWs are thus derived from those of the starting thin-film material. In this chapter, the SNAP technique was used to fabricate high-quality Si NW arrays with specific surface orientation through the use of (100)- or (111)-oriented Si epilayers. In addition, through the use of diffusion doping and surface resistivity measurements, which are only possible with a bulk surface, the electrical properties of the NWs could be precisely determined and controlled. This is in contrast to catalytically grown NWs where, in general, the doping is unknown before NW fabrication and can be difficult to determine afterwards. In the next chapter, I describe how the highly ordered nature of SNAP-fabricated NWs enables the development of binary tree demultiplexing architectures capable of electrically addressing a single NW from within a dense array. In chapter 4, I describe how the unique capability of SNAP to pattern NWs from thin-film materials can be used to construct an ultra-dense molecular electronic memory circuit.

In addition to the work described in this thesis, the SNAP technique could be used to pattern more exotic thin-film materials. For instance, SNAP could be used to define nanoscale ribbons from two-dimensional graphene, a recently discovered form of graphite only a single atomic layer thick with exciting electrical characteristics[38].

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Appendix 2.1: Experimentally determined doping data for 25, 31 and 50 nm SOI

n-type 25 nm SIMOX			*p-type 25 nm SIMOX*		
doping (cm^{-3})	***temp (^oC)***	***time (min)***	***doping (cm^{-3})***	***temp (^oC)***	***time (min)***
mid 10^{15}	800	3	mid 10^{15}	700*	4*
mid 10^{16}	800	4	mid 10^{16}	750	3
high 10^{16}	800	5	high 10^{16}	750	4
low 10^{17}	800	6	low 10^{17}	750*	6*
mid 10^{17}	800	7	mid 10^{17}	750*	7*
high 10^{17}	850	4	high 10^{17}	800*	3*
low 10^{18}	850	5	low 10^{18}	800	4
mid 10^{18}	900	5	mid 10^{18}	800*	5*
high 10^{18}	900	8	high 10^{18}	850	3
low 10^{19}	900	9	low 10^{19}	900*	2
mid 10^{19}	950	6	mid 10^{19}	900	6
high 10^{19}	1000	7	high 10^{19}	1000	5

n-type 31 nm SIMOX			*p-type 31 nm SIMOX*		
doping (cm^{-3})	***temp (^oC)***	***time (min)***	***doping (cm^{-3})***	***temp (^oC)***	***time (min)***
mid 10^{15}	880	3	mid 10^{15}	830*	3*
mid 10^{16}	830	4	mid 10^{16}	780*	4*
high 10^{16}	830	5	high 10^{16}	780*	5*
low 10^{17}	830	6	low 10^{17}	780*	6*
mid 10^{17}	830	7	mid 10^{17}	780*	7*
high 10^{17}	830	8	high 10^{17}	780*	8*
low 10^{18}	880	4	low 10^{18}	830*	4*
mid 10^{18}	880	5	mid 10^{18}	830*	5*
high 10^{18}	880	6	high 10^{18}	830*	6*
low 10^{19}	930	6	low 10^{19}	880*	6*
mid 10^{19}	980	4	mid 10^{19}	930	4
high 10^{19}	1000	7	high 10^{19}	950	7*

n-type 50 nm SIMOX			*p-type 50 nm SIMOX*		
doping (cm^{-3})	***temp (^oC)***	***time (min)***	***doping (cm^{-3})***	***temp(^oC)***	***time (min)***
mid 10^{15}	850	1	mid 10^{15}	700*	2*
mid 10^{16}	800	2	mid 10^{16}	750*	2*
high 10^{16}	800	3	high 10^{16}	750	3
low 10^{17}	850	2	low 10^{17}	800	2
mid 10^{17}	850	3	mid 10^{17}	800	3
high 10^{17}	850	3.5	high 10^{17}	800*	3.5*
low 10^{18}	900	1.5	low 10^{18}	850*	1.5*
mid 10^{18}	900	2.5	mid 10^{18}	850*	2.5*
high 10^{18}	875	4	high 10^{18}	825	4
low 10^{19}	900	4	low 10^{19}	850	4
mid 10^{19}	950	4	mid 10^{19}	850	6
high 10^{19}	1000	7	high 10^{19}	1000	6

* Extrapolated or best estimate

Chapter 3

Demultiplexing ultra-dense nanowire arrays

3.1 Introduction

One of the central challenges of both nanoscience and nanotechnology is the selective addressing of and interaction with individual nanostructures at high densities (*i.e.*, densities limited only by the intrinsic size and packing of the nanostructures); in the absence of a resolution to this problem, many of the potential benefits of these emerging fields will remain unrealized. Specifically, this challenge manifests over a range of problems varying from coupling conventional electronics to novel nano-scale memory and logic architectures[1], to addressing of single nanoparticles for applications in quantum computing[2], to construction of high-density biomolecular sensor circuits[3, 4], to name a few. Within the field of nano-electronics, this challenge can be framed as the ability to fabricate and address circuits that have characteristic wire dimensions and pitches that are smaller than the resolution achievable through lithographic patterning. For instance, I describe in Chapter 4 a novel molecular electronic memory circuit fabricated from crossed arrays of nanowires (NWs) that is nearly two orders of magnitude denser than conventional circuitry. However, the lack of a robust technology to selectively address

individual NWs from within such an ultra-dense array reduces the effective density of the memory circuit to that of conventional (lithographically-defined) circuitry.

The first aspect of this challenge, which consists of patterning and assembling NWs at ultra-high densities, has been achieved by several groups. Methods have included the assembly of catalytically-grown[5] NWs with the use of Langmuir-Blodgett techniques[4, 6, 7], harnessing competing interactions (*i.e.*, long-range Coulombic repulsions and short-range van der Waals attractions) to control NW length and pitch[8, 9], and, as described in detail in Chapter 2, using molecular beam epitaxy (MBE)-grown $GaAs/Al_xGa_{(1-x)}As$ superlattices as templates for depositing and subsequently transferring NWs onto thin-film substrates[10, 11].

Architectural concepts for meeting the second aspect of this challenge, which consists of electrically addressing (demultiplexing) individual NWs that are patterned at sub-lithographic densities, have also been proposed, but not yet implemented. The key objectives are three-fold. First, the demultiplexer architecture must bridge from the micrometer or submicrometer dimensions achievable through lithography to the few-nanometer dimensions achievable through alternative patterning methods. Second, the architecture should allow for the addressing of large numbers of NWs with small numbers of micrometer or submicrometer wires. Third, the manufacture of the multiplexer should be tolerant of fabrication defects.

Proposed demultiplexer architectures[12] have been based on combining crossbars[1] (NWs crossed by lithographically patterned demultiplexing wires)[13] with multi-input binary tree decoders[14]. Binary tree decoders, by their very nature, exhibit order $2\times\log_2(N)$ scaling, where N is the number of output NWs and $2\times\log_2(N)$ is the number of input

demultiplexing wires needed to address the NWs. Because each wire among a pair of input wires addresses one-half of the output NWs (Figure 1.A), 2^n NWs can be addressed by n input-wire pairs. This allows a small number of input wires to uniquely address an exponentially large number of NWs. In practice, demultiplexers for addressing very dense arrays of NWs require additional input wires above the theoretical minimum of $2\times\log_2(N)$, due to fabrication constraints. However, the number of additional input wires increases only linearly as fabrication tolerances are increased for the optimized structure described in this work. As will be discussed in the next section, this makes the binary tree demultiplexer very tolerant to alignment and manufacturing defects.

3.2 Demultiplexer architectures and alignment tolerance

Kuekes and Williams[15] were the first to describe a scheme for bridging microscale and nanoscale wires with a diode- or resistor-based decoder that utilized randomly deposited gold nanoparticles sandwiched within a crossbar of microscale address wires crossing the NW array. Although they demonstrated that $5\times\log_2(N)$ 'large' wires should be sufficient to address a dense array of N NWs, their technique required non-standard fabrication procedures and extensive testing to identify unique NW addresses. DeHon, Lincoln, and Savage[12] described a more complex architecture for addressing N NWs using no more than $2.2\times\log_2(N) + 11$ address wires. Their scheme utilizes field-effect gating of NWs by a microwire demultiplexer that allows tighter address encoding, and is compatible with conventional microelectronic fabrication procedures. However, their scheme requires control over the doping profile along the axial dimension of the NWs. Such NWs have

been recently realized experimentally[16-18], and Lieber's group has used them to demonstrate a demultiplexer that bridges fabrication methods (*i.e.*, self-assembly versus lithographic patterning), but not length scales[19, 20]. Both of these demultiplexing schemes are based upon placing a number of control regions (gates) on the surface of the NWs. An individual NW, which is initially in the non-conducting state, will conduct only when all of the control regions are field- or voltage-addressed; that is, it is the logical equivalent of a multi-input AND gate. (Conversely, demultiplexed NWs described herein conduct only when they are not addressed; *i.e.*, the control regions amount to a multi-input NOR gate.) While both architectures are tolerant of a certain amount of randomness in their fabrication process and both exhibit logarithmic scaling to allow a few inputs to address many NWs, they are required to be more complex than the architecture described below due to the stochastic dimensions of the NWs they function to address. How precisely the dimensions of the NW array (*i.e.*, NW diameter, length, pitch, etc.) can be controlled determines how much additional complexity is required from the NWs' electrical properties or from the demultiplexer architecture to facilitate unique addressing of each NW within an array.

Most NW fabrication procedures (including those described above) only approximately control NW diameter, pitch, and length. Proposed demultiplexing concepts then require a combination of sophisticated NWs (*i.e.*, NWs in which the doping is controlled along the axial dimension as described above) and demultiplexers with several additional (redundant) address lines. Conversely, the superlattice NW pattern transfer (SNAP) technique, described in detail in Chapter 2, permits the fabrication of NWs with precisely controlled NW width and pitch, and this substantially eases the requirements of

the NWs' electrical properties and on the demultiplexer architecture. Rather than requiring the demultiplexer to bridge fabrication approaches and dimensions, it only has to bridge dimensions. The highly ordered nature of SNAP-fabricated NW arrays enables the development of a straightforward field effect transistor (FET)-based demultiplexing architecture that uses traditional microelectronic (lithographic) processing.

The FET-based binary decoder architecture used in this work (in conjunction with SNAP-fabricated NWs) is a defect-tolerant design that can allow for large margins of error in its implementation and still remain fully functional. This architecture provides at least partial solutions to two issues: 1) alignment of the submicrometer demultiplexer features with the nanoscale features of a NW array, and 2) the use of large demultiplexer feature sizes and feature pitches to address a NW array that is characterized by a substantially smaller (but tightly defined) NW width and pitch. As described in the paragraphs below, redundancy can be built into the binary tree decoder architecture to significantly ease constraints in lithographic patterning and alignment of the decoder with respect to the NW array. Although there are more subtle constraints in the placement of the smallest gate structures with respect to individual NWs in the array, the highly ordered nature of SNAP-fabricated NWs allows the translation of this constraint into an equivalent constraint on the relative placement of gate structures with respect to each other within the decoder pattern. Such relative alignment within the decoder pattern can be readily achieved. Details of a scheme to affect this translation are briefly considered in Section 3.4. I will now turn to a discussion of the alignment tolerance afforded by the synergistic combination of SNAP-fabricated NWs and binary tree decoders, using Figure 3-1 as a guide.

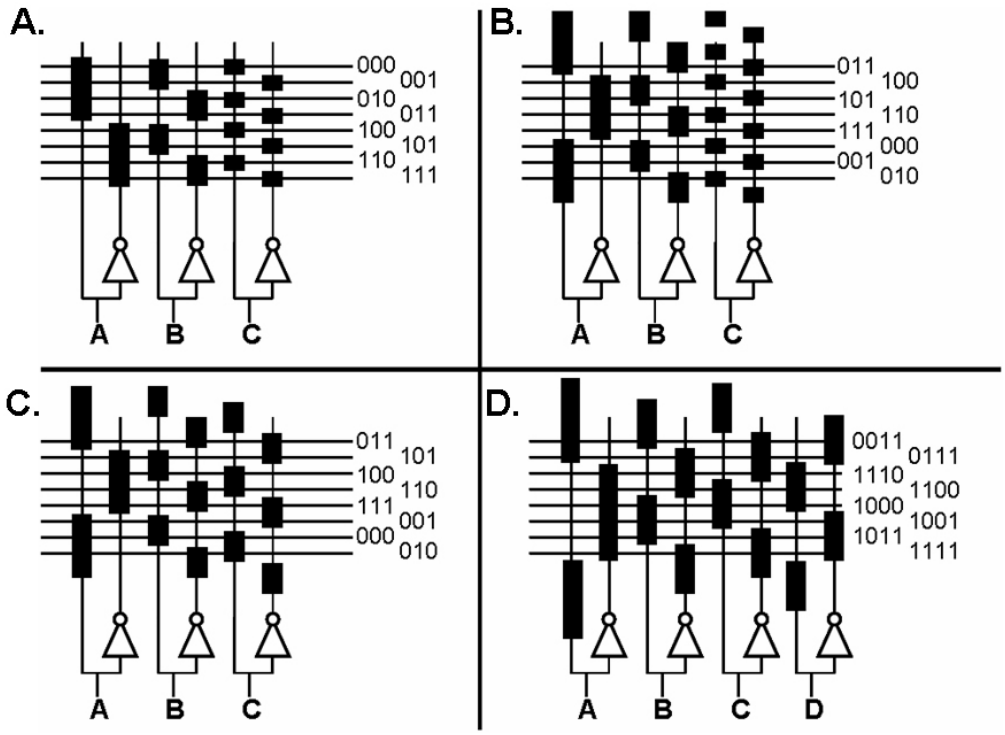

Figure 3-1. The operation of a NOR logic binary tree demultiplexer with varying fabrication constraints. A-D. The NWs are represented by eight horizontal wires, and the demultiplexer by three vertical complementary wire pairs. The operation of a complementary wire pair may be understood by considering an input address of '1' to wire pair A. The left wire is sent high by this address, and the right wire is sent low. For an input address of '0', the reverse is true. Regions where the gates interact strongly with the underlying NWs are shown as bars. When a NW passes under a bar that is connected to a wire in the high state, that NW is deselected (gated). The input address that selects each NW is indicated next to the NW. **A**. A standard binary tree demultiplexer; note that every MW pair turns off half of the NWs it contacts. **B**. A binary tree demultiplexer in which the binary tree pattern is not registered with specific NWs, and extends beyond the limits of the NW pattern. Note that the addresses are no longer sequential. **C**. The binary tree pattern of gate electrodes is shown at twice the pitch and twice the feature size of the NW array. Note that $2\times\log_2(N)$ address wires are still need to address N nanowires. **D**. The binary tree pattern of gate electrodes is shown at three times the pitch and three times the feature size of the NW array. Note that an additional pair of address wires is needed and so half of all address values are inactive.

3.2.1 Alignment tolerance through architecture

Alignment along the length (*x*-axis) of SNAP-fabricated NWs is relatively straightforward since such NWs can be extremely long (typically millimeters). Precise alignment along the perpendicular (*y*-axis) direction, however, is more difficult. A partial solution to this problem is to fabricate the binary tree of the demultiplexer with a repeating pattern, the period of which is equal to the width of the NW array. In this fashion, the decoder pattern will extend beyond the boundaries of the array (Figure 3-1.B). If, for example, the decoder pattern misses its intended position on the NW array by 500 nm, causing the top 500 nm of addresses to miss their mark, the addresses are simply repeated at the bottom of the array. The decoder pattern can be fabricated to an arbitrary length, giving any amount of *y*-axis tolerance desired. The cost of giving up absolute demultiplexer alignment is knowledge of which NW corresponds to which demultiplexer address. However, it is still possible to know that every NW has a unique address.

The constraints on rotational alignment are tighter than for translational alignment since small deviations of the decoder pattern from 90° (with respect to the *x*-axis) can result in a NW shifting from its intended decoder address to that of its neighbor. Fortunately, angular alignment of the decoder pattern relative to the NW array can be accomplished with high precision. This is primarily because the SNAP technique is capable of producing very straight arrays of NWs over millimeter length scales, which can readily be aligned to using lithographic techniques. Nonetheless, if rotational alignment is imperfect, extra input wire pairs at the smallest gate-pitch and slightly offset from each other can be used to distinguish NWs without unique addresses.

3.2.2 Feature size tolerance through architecture

The second challenge towards bridging the dimensions from the nanometer features of a NW array to the sub-micrometer features of the demultiplexer revolves around the limits of the lithography used to define the demultiplexer binary tree features. For the binary decoder depicted in Figure 3-1.C, the narrowest-pitch gate patterns on the address wires are at twice the pitch of the output wires, and there is no need for redundant address lines (*i.e.*, the scaling is exactly $2\times\log_2 N$ address wires for N NWs). In reality, addressing an array of narrow-pitch NWs (the SNAP-fabricated NWs described in this work are at ~30-nm pitch) with large repetitions of gates at twice the NW pitch would be exceedingly difficult and certainly not practical. However, the gate electrodes may be fabricated at a pitch that is m times the NW pitch, where m is an integer. This is shown in Figure 3-1.D for $m = 3$. This requires an additional input wire pair with the same gate periodicity but offset by a single NW pitch. Note that using any three out of the four input wire pairs does not produce a set of unique addresses for the eight NWs shown – all four are needed. This type of alignment, in which the gates are aligned to one another with high precision but not aligned with the underlying NW pattern, is practical to achieve. However, there are penalties associated with adding additional wire pairs (besides the need to fabricate more input wires). Each additional address pair of demultiplexing wires reduces the number of good addresses by half. This is illustrated in Figure 3-1.D in which an additional pair of address lines is needed to uniquely address each NW in the array, but only half of the input addresses actually identify a wire; *e.g.*, there are $2^4 = 16$ addresses but only eight wires. Thus, the circuit must be tested to discover the good addresses and once they are found they must be stored in memory. Since the number of

good addresses is nominally the number of NWs to be addressed, only a relatively small amount of memory is required. For instance, a NW crossbar memory circuit (such as described in Chapter 4) fabricated from two NW arrays of N NWs each would yield $N \times N$ bits of storage requiring about $N \times \log_2 N$ bits to store the good NW addresses. A one-megabit memory circuit ($N = 10^3$) requires about 1 percent of its bits to store the good NW addresses, while a 10-gigabit memory ($N = 10^5$) requires about 0.01 percent of its bits to store the good NW addresses. On the other hand, finding the good addresses in the first place requires testing the circuit, with the amount of testing increasing significantly as additional address wire pairs are needed.

3.3 FET-based demultiplexing of SNAP-fabricated NW arrays

In what follows, I will describe the research of my co-workers and me to demonstrate a field-effect-based demultiplexing scheme that is tolerant of manufacturing defects, has no serious restrictions in terms of the wire size and pitch of the demultiplexer structure, and utilizes $2 \times \log_2(N) + R$ microwires to address N NWs, where R (for redundant address lines) is zero or a small integer. This scheme does not require control over the axial doping profile of the underlying NWs, but can take advantage of the readily achieved vertical doping profiles described in Chapter 2. It is optimized (*i.e.*, R is small) for NW arrays in which the NW pitch and width are precisely controlled, such as the case for NWs fabricated using the SNAP method described above. The scheme is based on NOR logic; that is, the only NW that is not field-addressed is the one selected (Figure 3-1).

The demultiplexer concept is shown in Figure 3-2, in which 32 (= 2^5) NWs are addressed with five pairs of (drawn) submicrometer wires. Note that the binary tree pattern extends above and below the NW array to ease the lateral alignment requirements. As long as the

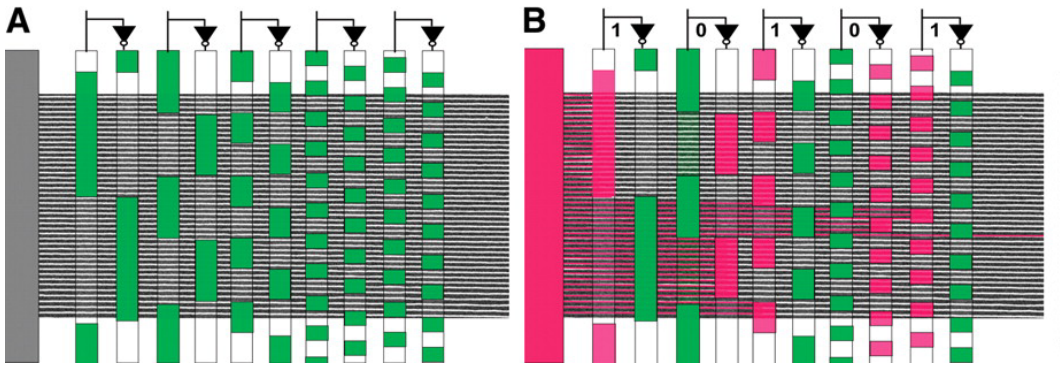

Figure 3-2. **The nanowire demultiplexer, drawn over an electron micrograph of 2^5 (= 32) silicon nanowires. A**. All NWs are ohmically contacted to the left electrode. A binary tree pattern consisting of five complementary pairs of large wires is shown. The green regions correspond to areas in which a voltage applied to the top (metal) wires can reduce the conductivity of the NWs through field-effect gating. All multiplexer features are larger than the NW features. **B.** A voltage applied to the left electrode raises all NWs to that voltage level. A single NW is selected by applying the input address '1 0 1 0 1'. Application of a voltage onto a given wire pair sends one wire high and the other low. The resistance of NWs that pass under a voltage-gated (red) region is increased. Only a single NW (colored red across the entire structure) remains in the high-conducting state.

multiplexer pattern is oriented perpendicular to the NW array, and the NW pitch and width dimensions are well defined, the circuit will be functional. As described above, the cost associated with giving up lateral alignment precision is the knowledge of exactly which NW is selected by a given input address. For example, the binary address '1 0 1 0 1' utilized in Figure 3-2 corresponds to the decimal address 21, but it is the 28th wire from the top that is selected. In practice, one usually doesn't need to know the physical location of the actual NW, just the address of that NW, and so this 'cost' is not significant for most applications. Also notice that the smallest-patterned binary tree feature sizes and

pitches are significantly larger than the smallest corresponding dimensions within the NW array (although $R = 0$ for the example of Figure 3-2). This aspect of the architecture makes it particularly amenable to manufacturing processes. For example, the dimensions of the multiplexed control wires are well suited to micro-imprint molding, a relatively high-throughput lithographic technique[21].

Development of the demultiplexer architecture described here proceeded in two stages: first by selectively addressing lithographically patterned NWs, and second by selectively addressing small groups of NWs patterned at sublithographic dimensions. For both cases, the key elements of the structure of the multiplexer are illustrated in Figure 3-3. The goal of this structure is to achieve voltage gating on one NW (NW_G) and to minimize voltage gating on an adjacent NW (NW_I), and this requires careful selection of both low-κ and high-κ dielectric materials. For the high-κ dielectric, HfO_2 was chosen because it has a high dielectric constant ($\kappa = 25$), it forms an insulating film on Si that is stable to high temperatures[22], interdiffusion between Si and Hf is not observed[23] (as it can be for other high-κ dielectrics[23]), and methods for growing very thin films of HfO_2 exist. Finally, HfO_2 has been shown to be an effective gate dielectric for nanotube[24, 25] and NW[26] field-effect transistors. For the low-κ dielectric, we chose SiO_2 ($\kappa = 3.9$) because of the ease of fabricating such films.

Figure 3-4 shows data from a demonstration circuit in which ten relatively large Si wires (doping, $n = 5\times10^{18}$ cm^{-3}) are uniquely addressed. For this circuit (in the context of Figure 3-3), W = 200 nm and P = 1000 nm. The thickness of the SiO_2 low-κ dielectric

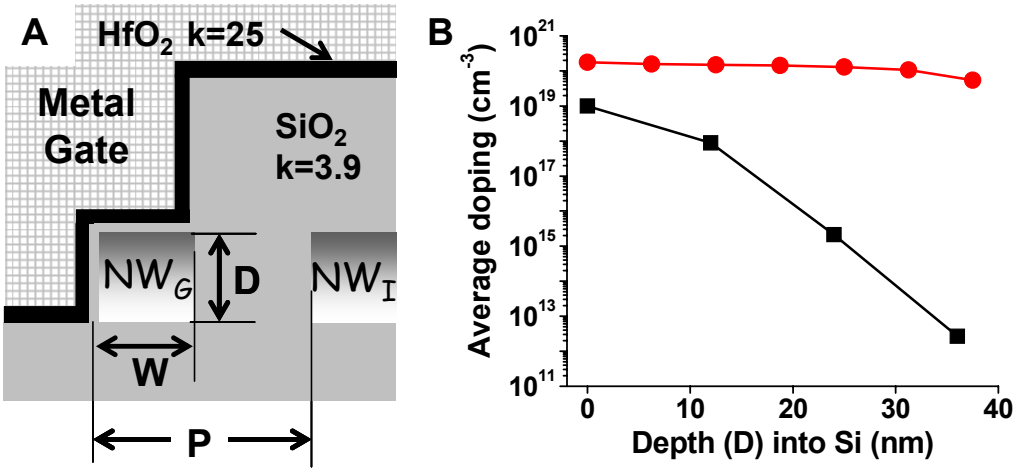

Figure 3-3. A. Side view schematic of the demultiplexer. Two NWs are shown in an end-on view, and D, W, and P refer to the depth, width, and pitch of the NWs. NW_G and NW_I refer to voltage gated and isolated NWs. The HfO_2 high-κ dielectric film is typically 3–6 nm thick, while the SiO_2 dielectric is 50–100 nm thick. Note that for small P values, P determines the distance of the NW_I from the gate electrode, and hence the gating selectivity. The shading of the NWs represents the doping profile. **B.** Measured doping profile through the silicon-on-insulator wafers from which the NWs are formed. Two modes of doping are illustrated: drive-in doping (red circles), which produces a uniform doping level through the depth of the NWs, and gradient doping (black squares), which produces a rapidly decreasing dopant density, and is utilized for demultiplexing high-conductivity NWs.

(t = 100 nm) largely determines the selectivity (*i.e.*, the selected NW/deselected NW current ratio). This is seen by considering the capacitances (per unit area) between a given NW and the gate. The total capacitance of NW_G is given by the series combination of the wire native oxide (thickness t = 1–2 nm) and the HfO_2 dielectric ($t \approx$ 5 nm), which is

$$C_G \approx \varepsilon_o \left(\frac{t_{HfO_2}}{\kappa_{HfO_2}} + \frac{t_{native}}{\kappa_{SiO_2}} \right)^{-1} \approx \varepsilon_o \left(\frac{5}{25} + \frac{1.5}{3.9} \right)^{-1} = 1.7 \varepsilon_o \, \mathrm{nm}^{-1}, \qquad (1)$$

while the total capacitance of NW_I has two contributions in parallel. NW_I is coupled to the gate horizontally through the P–W thick (800 nm) SiO_2 dielectric (ignoring the relatively small series contributions by the HfO_2 layer and the NW_I native oxide) and

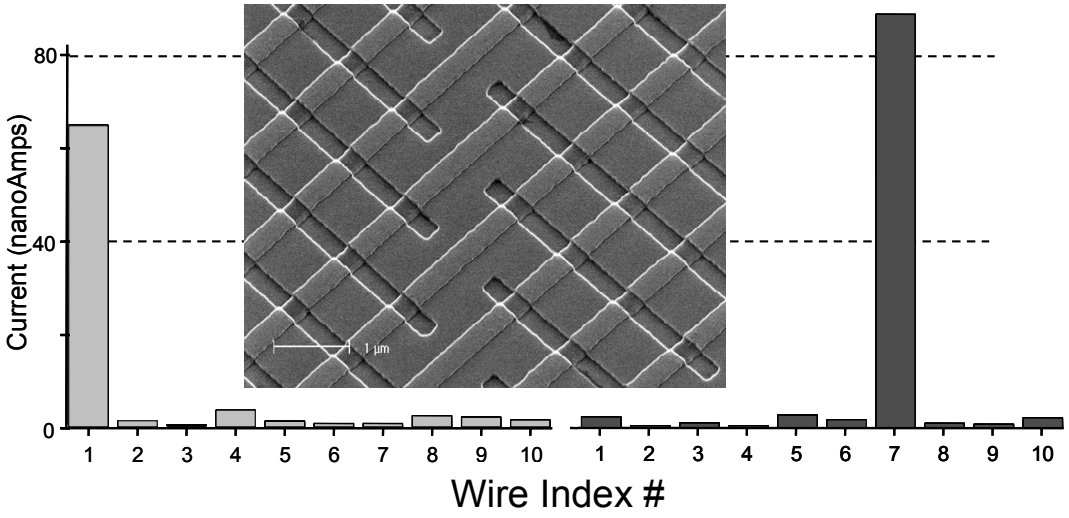

Figure 3-4. A demultiplexer constructed on a test circuit of 10 Si wires, each 200 nm wide, patterned at 1-µm pitch. The inset shows the gating electrode structure (before deposition of the gate electrodes) that was patterned on top of the underlying wire array. Results illustrating the operation of this circuit are shown in the two bar graphs, in which individual wires were maintained in the high-conductivity state while all other wires were deselected through appropriate input addressing.

vertically through the SiO_2 dielectric thickness (again ignoring smaller series combinations). Thus, the total capacitance of NW_I is given by

$$C_I \approx \kappa_{SiO_2}\varepsilon_o\left(\frac{1}{t_{SiO_2}}+\frac{1}{\mathrm{P}-\mathrm{W}}\right). \tag{2}$$

For the NW array of Figure 3-4, C_I is dominated by the first term of equation (2) which gives $C_I \approx 0.04\ \varepsilon_o\,\mathrm{nm}^{-1}$. The selectivity is then given by $C_G / C_I \approx 40$.

While the data of Figure 3-4 illustrates the validity of our FET-based demultiplexer architecture for the selection of individual wires, it does not demonstrate the capability to bridge length scales. Referring again to Figure 3-3, we next considered a NW circuit with width W = 13 nm and pitch P = 34 nm. Again, the metal gate electrode is separated from NW_G by about 5 nm of HfO_2 and 1–2 nm of SiO_2 (the native oxide on the NW surface). However, NW_I is now separated from the gate by 5 nm of HfO_2 and

only about 20 nm (= P – W) of SiO_2. Thus, in contrast to the demonstration of Figure 3-4, it is the dimensions of the NW array (pitch and width) rather than the thickness of the low-κ dielectric that determines the gating selectivity of adjacent and very closely spaced NWs, *i.e.*, C_I is dominated by the second term in equation (2) and is approximately 0.02 $\varepsilon_o\,\mathrm{nm}^{-1}$. The result is that for a perfectly fabricated circuit, when a gating voltage is applied, the field felt by NW_G is about ten times greater than that felt by NW_I. For realistic fabrication tolerances, the field ratio is likely to be reduced.

Figure 3-5 shows images of the demultiplexer fabrication process for a circuit designed to address an ultra-high density NW circuit. Using the SNAP method, 150 n-doped Si NWs were fabricated. As described in Chapter 2, this technique can produce aligned arrays of high-aspect ratio (> 10^6) metal and semiconductor NWs at dimensions that are not achievable through alternative methods. Silicon NW arrays containing between 10^2–10^3 NWs, with bulk-like and controllable conductivity characteristics, may be fabricated at dimensions down to W = 8 nm and P = 16 nm.

The demultiplexer itself was patterned using electron-beam lithography and thin-film materials deposition. A brief description of the fabrication procedure is given in Section 3.5. For this demonstration, highly conducting p^+ (10^{19} cm^{-3}) Si NWs were utilized to ensure ohmic contacts and good signal. However, highly doped NWs do not exhibit a strong gating response. Thus, the NWs were thinned (etched) by about 10 nm in the regions where the gate electrodes were deposited, so that in those regions, the doping was ~10^{18} cm^{-3} (Figure 3-3.B). This is a unique feature of diffusion-doped, SNAP-fabricated Si NWs and allows the gating response to be tuned in automatic registry with the gating regions, while also maintaining highly conductive NWs (Figure 3-5.B).

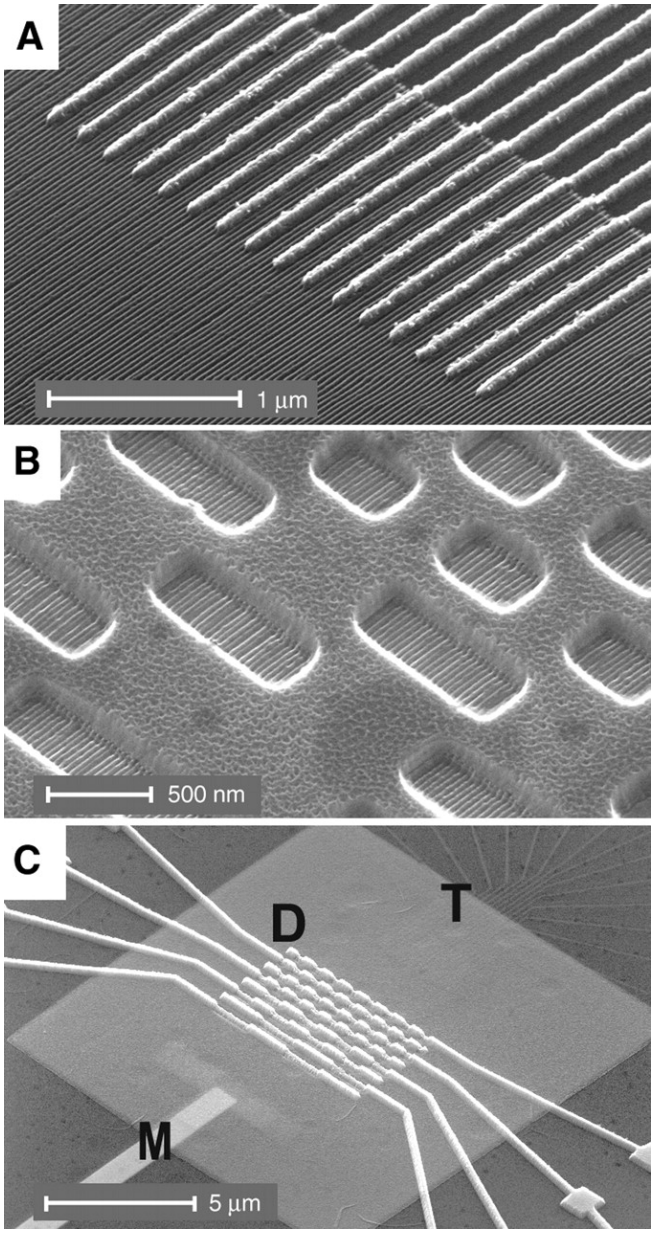

Figure 3-5. Scanning electron micrographs of the nanowire demultiplexer assembly process. A. Sixteen electrical contacts are established, each to two or three NWs from an array of Si NWs. **B**. The binary gate demultiplexer pattern after deposition of the low-κ SiO_2 dielectric and patterning of lithographically-defined windows. Note that once the tops of the underlying Si NWs were exposed, the CF_4-based reactive ion etch process (used to etch the windows in the SiO_2 layer) was briefly extended to intentionally remove approximately 10 nm from the NW surface. This lowers the dopant concentration in the gate region. The high-κ HfO_2 dielectric is deposited following this etch step. **C.** Assembled demultiplexer circuit. M refers to the multiplexer electrode used to apply a voltage to all of the NWs. D is the demultiplexer structure, shown with metal electrodes deposited on the HfO_2 gate insulator. T refers to test electrodes. Individual NWs are measured by applying a voltage to M and grounding the test connections through an ammeter.

There is a chicken-and-egg challenge associated with testing this demultiplexer on narrow-pitch NW arrays; that is, how does one test whether the demultiplexer can address individual NWs when the individual NWs themselves are too closely spaced to separately wire up for the test? Our approach was twofold: First, we established 2^4 (= 16) electrical contacts, each bridging two or three NWs, at a 150-nm pitch for testing (Figure 3-5.A). Second, a binary gating tree of four pairs of microwires was fabricated to allow for the separate addressing of these 16 individual groups (Figure 3-5.B). The most closely spaced wire pairs were patterned at a 600-nm pitch, and these pairs were repeated twice, with the second wire pair phase-shifted by the pitch of the electrical contacts (= 150 nm). The gate width (= 300 nm) was twice the inter-gate spacing. The result was that relatively large binary-tree features could select out the two or three NWs addressed by a given test electrode.

Figure 3-6 shows results from the NW demultiplexer, in which, for two different address combinations, two different sets of NWs were selected, at a signal-to-background level of about four for the worst-case comparison. It is important to note that due to slight variations in the process conditions, different sections of the NW array show both small differences in conductivity as well as different coupling strengths to the gate electrodes. As a result, the data shown is normalized by the values obtained by setting the entire gate array high (+10 V, suppressing conductivity for these p-type NWs), yielding a map of nanoFET response for this specific device. Additionally, we have fabricated a second device based on n-type NWs and found similar values for both the contrast and the selectivity.

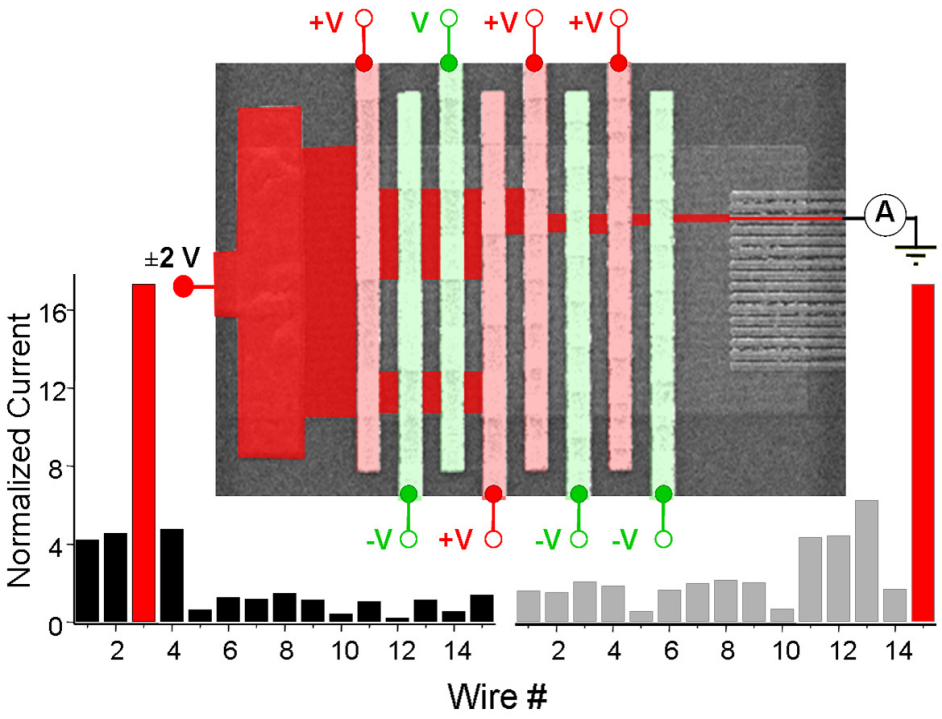

Figure 3-6. Characteristic operation of the nanowire demultiplexer for two different input addresses. The central picture illustrates the address that was used to select out wire 3 in the bottom left bar graph. Gate voltages of +10 V and –10 V were applied to the red and green wires, respectively. The normalized current is the ratio of wire current measured under an addressing gate configuration to the current of the wire when +10 V is applied to all gates

This result validates our demultiplexing architecture, and provides a viable pathway toward bridging length scales between micro- and nano-electronic circuits. As mentioned above, the full demonstration of single-wire selectivity is currently hindered by the lack of an appropriate validation technique, but there is no reason to believe that this architecture can not be extended to even smaller dimensions, given a modest scaling of the controlling gate array. Additionally, we believe molecular-level control of the Si NW-dielectric interface could significantly increase the NW selectivity presented here.

Returning again to Figure 3-3, the 1–2 nm native oxide on the Si NW surface significantly limits the selectivity by greatly reducing the effective dielectric constant of the gate insulator. Although the Si NW native oxide can be removed by hydrofluoric acid

etching, the surface will quickly re-oxidize in an ambient environment. However, through chemical modification of the Si surface, the native oxide can be replaced by a monolayer of covalently bonded methyl groups (*i.e.*, a CH_3-terminated surface). As will be discussed in more detail in Chapter 5, this passivation prevents oxidation of the Si surface and is resistant to typical nanofabrication processing techniques. Replacing t_{native} in equation (1) with the methyl monolayer thickness (about 0.2 nm) and replacing κ_{SiO_2} by the methyl monolayer dielectric constant (believed to be about 2[27, 28]), the capacitive coupling of NW_G to the gate, and hence the NW selectivity, doubles. The selectivity can be further improved by decreasing the HfO_2 dielectric thickness using atomic layer deposition methods (down to about 2 nm). Lastly, further generations of this structure can be improved through the incorporation of ultralow-κ (< 2.0) materials, such as nanoporous silica films (κ = 1.3–2.5), porous polymers, and polytetrafluoroethylene (PTFE) (κ = 1.9)[29]. A challenge will be to incorporate these changes while maintaining a low-leakage current through the gate electrodes (currently 6 pA into a signal channel, or 300 μA cm^{-2}). For nanowires much smaller than those used here, statistical fluctuations in dopant density may ultimately prove limiting to this and other field-effect approaches.

3.4 Demultiplexer patterning requirements

A source of alignment error that cannot be compensated for with increasing redundancy of the input wires is schematically illustrated in Figure 3-7. Note that in Figure 3-7.A it is clear that NW_G represents a deselected (gated) NW, and NW_I represents a selected (isolated) NW. For Figure 3-7.B, it is not clear whether the NW labeled with a question

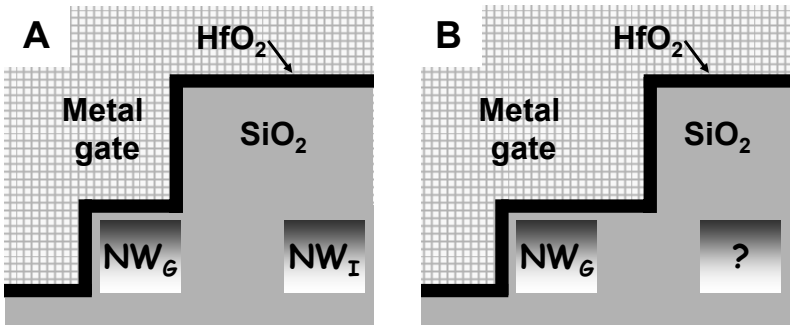

Figure 3-7. An illustration of the importance of alignment precision between the demultiplexer gate structure and the underlying nanowire array. **A.** A perfectly fabricated demultiplexer gate structure, with a deselected (NW_G) and an adjacent selected (NW_I) NW. **B**. An imperfectly fabricated demultiplexer. NW_G is clearly deselected, but the status of the other NW is unclear.

mark (?) is deselected or selected. The implication is that it is necessary to control the placement of the gate electrodes to at least one-half of the pitch of the NWs. This is true, but, as described below, that accuracy is only required for the relative placement of the gates with respect to each other, rather than with respect to the underlying NW array.

Absolute alignment of the demultiplexer pattern with an underlying NW array to an accuracy of the half-pitch of the NWs is difficult, but highly precise relative alignment of the demultiplexer features (gates) with each other is relatively straightforward. To solve the problem of ambiguously addressed NWs depicted in Figure 3-7, extra input wire pairs at the highest gate frequency (smallest gate size) can be added to the demultiplexer with the gate pattern of the extra lines slightly offset from one another (ideally by the NW half-pitch). Note that the extra wires are probably only required for wire pairs with the smallest gate size. This is because wires with larger gating regions will have a smaller fraction of ambiguously gated NWs.

Unlike the case of using extra wiring to address NWs with relatively large gates (discussed in Section 3.2), these redundant address lines do not lead to redundant

addresses. Instead, extra wire pairs are separately tested and then one of them is selected according to which address wire pair yields the best performance. The idea is to take advantage of the precise relative alignment that can be achieved with EBL without requiring absolute alignment to the NW array. Note that this scheme requires the NW array to have a well-defined NW width and pitch; such is the case with SNAP-fabricated NWs.

Finally, fluctuations in the decoder features due to resolution limitations of EBL techniques may result in NWs having non-unique addresses similar to the problem of poor rotational alignment. This problem can be alleviated by using the same strategy for overcoming rotational alignment errors, that is, by adding redundant input wire pairs; however, for NWs at very narrow pitch such lithographic limitations may preclude single NW addressability.

3.5 Demultiplexer fabrication

The following section briefly describes the major steps in fabricating the demultiplexer described herein. More detail can be found in the thesis of Dr. Robert R. Beckman[30]. The NWs were fabricated using the SNAP technique and (100)-oriented silicon-on-insulator (SOI) wafers (30 nm of Si on 150 nm of SiO_2) doped using diffusion-based doping methods (as described in Chapter 2). The fall in dopant density with depth into the Si epilayer, which is characteristic of diffusion-based doping, was critical for increasing the response of NWs to field-effect addressing.

The SNAP-fabricated NWs were then sectioned (via lithographic patterning and an SF_6 dry etch) to at least 10 μm in length, and ohmic contacts were patterned using standard electron-beam lithography (EBL), thin-film metal evaporation, and lift-off. The contacts were annealed in N_2 (5 min, 450° C), and Si NW conductivity was verified before proceeding to the dielectric material deposition steps.

A thick (> 50 nm) SiO_2 layer was used as the low-κ (low-gate-capacitance) dielectric material, and was deposited by either spin-on glass (SOG; Honeywell, see Chapter 4, Section 4.6 for details) or plasma-enhanced chemical vapor deposition (PECVD). The SOG is likely to have a slightly lower κ value than a PECVD oxide, due to the lower quality of the film, which is useful for increasing the high- and low-gate contrast. EBL was used to patterning windows in either poly-methyl methacrylate (PMMA) or ZEP-520A (Zeon Corp. Tokyo, Japan), and reactive-ion etching (20:30:2.5 CF_4 to He to H_2, 40 W, 5 mTorr) was used to etch the SiO_2 over the binary-tree-gated regions. The etch time was extended beyond the interferometrically-determined end-point to slightly thin (by about 10 nm) the Si NWs. As described above, this decreases the dopant density in the regions where a strong gating response is desired.

Following the critical SiO_2 etch, a thin film (<5 nm) of HfO_2 is deposited (via electron-beam evaporation of Hf metal in an O_2 atmosphere of 6.7×10^{-5} Torr) over the entire decoder pattern as the high-κ dielectric. Lastly, Ti/Al/Pt (10 nm/100 nm/ 20 nm) top-gate electrodes are deposited using EBL, thin-film metal evaporation, and lift-off. Note that the evaporated HfO_2/Ti/Al/Pt stack fills the etched recesses in SiO_2 where the gate electrodes couple strongly to the underlying Si NWs to be gated (Figure 3-5.B and Figure 3-5.C).

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Chapter 4

Ultra-dense crossbar molecular memory circuits

4.1 Introduction

The past four decades have witnessed extraordinary advances in computation that have revolutionized the way people communicate and process information. Sustained progress in this field has largely been driven by the consistent reduction of silicon-based microelectronic-device dimensions with accompanying increases in device density. This guiding principle of advancing computational technology through regular increases in device integration is widely referred to as 'scaled CMOS' after the ubiquitous complementary metal-oxide-semiconductor integrated circuit, and has driven the now famous exponential increase in computational performance as measured by any number of metrics (*e.g.*, speed, size, cost, power consumption, etc.). However, there are strong indications that continued scaling of conventional CMOS technology may falter in the near future due to physical and (perhaps more importantly) financial considerations[1]. This has led to a growing consensus within the semiconductor industry that continued improvements in information processing technology will likely occur through the development of alternative materials, patterning methods, and architectures[2, 3] that can be

integrated into the well-established silicon CMOS infrastructure in the near term[1, 4] while being scalable in the long term. Ideally, any new technology should be compatible with conventional CMOS to bridge computational requirements during its assimilation period while having the intrinsic potential to continue the exponential pace of computational performance once traditionally-scaled CMOS comes to an end.

These considerations have brought a great deal of attention to the possibility of engineering molecules for use as the active electronic components in otherwise solid-state computational systems[5]. While the idea of using molecules to mimic traditional computational functions is not new[6], it is only within the past decade that molecules have been integrated into hybrid solid-state/molecular devices to perform the traditional computational functions of rectification[7], storage[8], and logic[9]. Although a complete picture of electronic transport through molecular junctions continues to elude theorists[10, 11], molecules have nonetheless empirically demonstrated their potential for computation. Additionally, a number of methods have been reported for assembling small numbers of nanowire[12, 13] or carbon-nanotube[14, 15] devices. However, while these studies demonstrate individual device scalability, they seldom address issues such as device pitch or density, which are equally important from a technology standpoint.

To that end, the Heath group began a research program focused on the concept of developing an ultra-dense molecular electronic computer architecture where the various computational elements would be tiled together through high-density arrays of nanowires (NWs) (Figure 4-1)[5]. Along with my co-workers, my research in the Heath group has focused on a number of the components shown in Figure 4-1 for realizing this multifunctional computational architecture. These included the development of

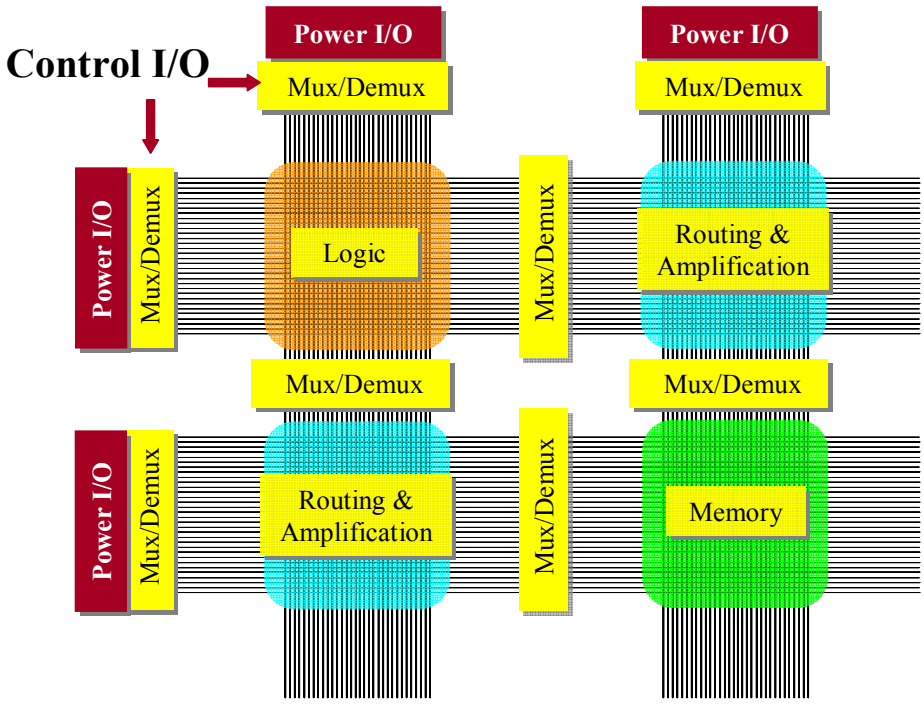

Figure 4-1. Schematic diagram of a nanoelectronic crossbar circuit architecture. The various computational building-blocks are shown tiled together through ultra-dense nanowire arrays. Multiplexers (Mux) and/or demultiplexers (Demux) control signals within the circuit and to outside electronics (power I/O). This structure is both defect-tolerant and amendable to non-lithographic fabrication techniques.

techniques for patterning ultra-high-density arrays of silicon NWs with precisely controlled electronic properties (Chapter 2), and the demonstration of a field-effect transistor (FET)-based demultiplexer capable of bridging from the sub-micrometer length scales of conventional CMOS technology to the nanometer length scales of molecular electronics (Chapter 3). In this chapter, I will discuss the integration of sub-lithographic patterning techniques and [2]rotaxane-based molecular materials for the fabrication of an ultra-dense, error-tolerant, 160,000-bit molecular electronic crossbar memory patterned at a density of 100 gigabits per square centimeter (1×10^{11} bits cm^{-2}). Before describing in detail the fabrication and testing of this memory, I will give a brief introduction to the

rich science underlying the switching mechanism of bistable [2]rotaxane molecules and their integration into high-density crossbar architectures.

4.2 The [2]rotaxane switching cycle

Figure 4-2.A shows the molecular structure of a bistable [2]rotaxane $HRT5^{4+}$ used in the crossbar molecular memory circuits discussed herein. This molecule was synthesized by Dr. Hsian-Rong Tseng of the J. Fraser Stoddart group at UCLA using the techniques of supramolecular[16] template-directed[17, 18] chemical synthesis. [2]Rotaxanes consist of two mechanically-interlocked components: an amphiphilic dumbbell-shaped component and a π-electron-accepting cyclobis(paraquat-*p*-phenylene) ($CBPQT^{4+}$) ring (blue). The dumbbell component features two bulky stoppers (light blue and grey) on either end to prevent the ring from slipping off the [2]rotaxane shaft and to facilitate orientational incorporation into solid-state devices via Langmuir-Blodgett techniques. The $CBPQT^{4+}$ ring can translate along the shaft of the dumbbell-shaped component to sit at one of two π-electron-donating recognition sites: the tetrathiafulvalene (TTF) unit (green) or the 1,5-dioxynapthalene unit (DNP) (red). [2]Rotaxanes have been extensively studied experimentally[19-29] and theoretically[30-33] in a variety of environments to elucidate the physical mechanism underlying their switching behavior, and to quantify the switching kinetics and equilibrium thermodynamics. Under ambient conditions, the $CBPQT^{4+}$ ring preferentially encircles the TTF unit over the DNP unit. For the [2]rotaxane $RTTF^{4+}$ (which is very similar to $HRT5^{4+}$) in acetonitrile solution, this equilibrium is greater than

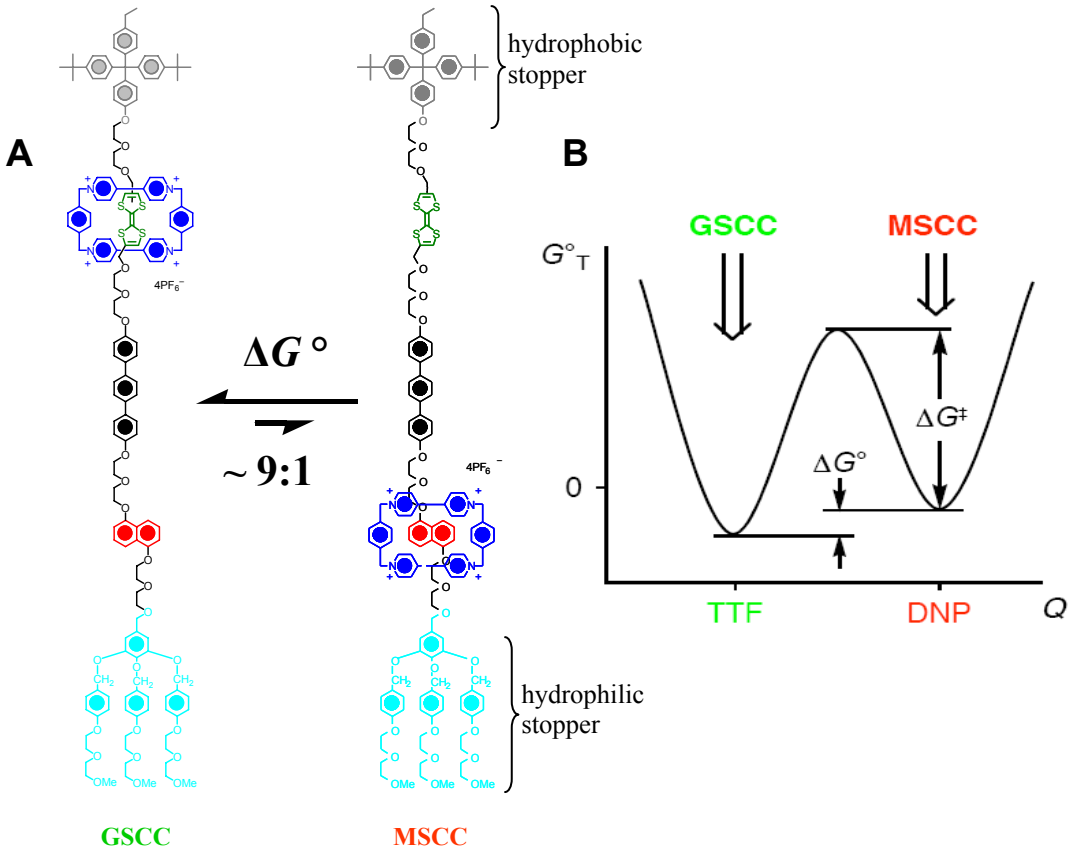

Figure 4-2. Molecular structure and energy diagram of the bistable [2]rotaxane HRT5^{4+}. A. At equilibrium, the ground-state co-conformation (GSCC) is energetically favored over the metastable-state co-conformation (MSCC) by a free energy of $\Delta G°$. This corresponds to a GSCC-to-MSCC distribution of about 9:1. Within a Si/mol/Ti MSTJ (see text), the molecule is oriented with the (light blue) hydrophilic stopper in contact with the Si electrode and the grey hydrophobic stopper in contact with the Ti electrode. **B.** The potential energy landscape revealing the basis of bistability in [2]rotaxane molecular switches is plotted against the reaction coordinate, *Q,* representing translation of the ring from the TTF unit to the DNP unit. The rate of relaxation from the MSCC ('1') state to the GSCC ('0') state depends on the energy barrier, $\Delta G^{‡}$, which increases with the viscosity of the physical environment (*e.g.*, $\Delta G^{‡}_{\text{solid-state}} > \Delta G^{‡}_{\text{solution}}$).

90 percent, and is described by a free energy change of $\Delta G° = +1.6$ kcal/mol (Figure 4-2.B) when the CBPQT^{4+} ring moves from the TTF to the DNP unit[20]. Thus, the co-conformation with the CBPQT^{4+} ring encircling the TTF unit is referred to as the ground-state co-conformation of the molecule. Recent experiments[20] have shown that the ground state equilibrium distribution of these molecules is dominated by molecular structure,

with the physical environment (*e.g.*, solution or solid-state) of the molecular-switch playing only a minor role. Within a silicon/molecule(s)/titanium (Si/mol/Ti) solid-state molecular-switch tunnel junction (MSTJ), the ground-state co-conformation corresponds to the low conductivity or binary '0' state of the molecule.

The universal[19] molecular-mechanical switching mechanism of bistable [2]rotaxanes is shown in Figure 4-3. Starting at the ground-state co-conformation ($CBPQT^{4+}$ ring encircling the TTF unit), the first two oxidation states of the molecule result from sequential oxidations of the TTF unit corresponding to the reaction $TTF^0 \xrightarrow{-e^-} TTF^{\bullet+} \xrightarrow{-e^-} TTF^{2+}$. Upon forming the $TTF^{\bullet+}$ radical cation, coulombic repulsion between the $CBPQT^{4+}$ ring and the $TTF^{\bullet+}$ unit results in translation of the ring from the TTF unit to the DNP unit. This process occurs on a millisecond time scale[27-29], and is believed to convert all of the molecules from their ground-state co-conformation to

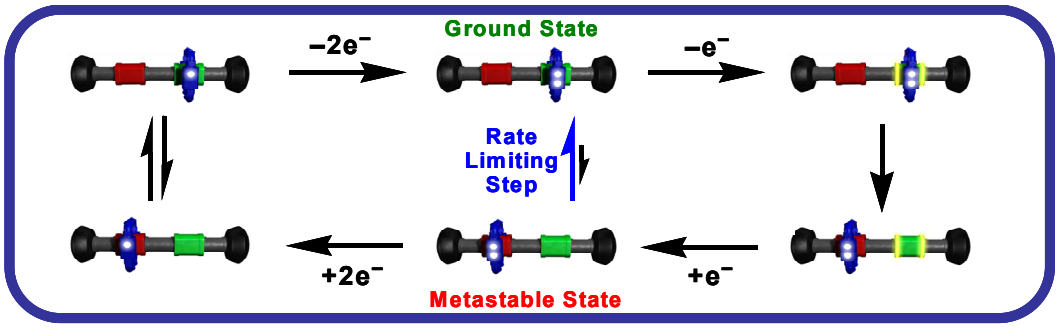

Figure 4-3. Bistable [2]rotaxane switching cycle. Starting from the ground state with the $CBPQT^{4+}$ ring (blue, each white dot corresponding to a +2 charge) encircling the TTF (green) unit and moving clockwise: The TTF unit is oxidized (highlighted now) resulting in translation of the ring from the TTF to DNP (red) unit and formation of the metastable state after the TTF unit regains neutrality. The molecule can relax back to the ground state through the rate-limiting kinetic step, or through the clockwise loop on the left in which the ring is reduced resulting in recovery of the ground state at least one thousand times faster.

a translational isomer with the ring encircling the DNP unit, referred to as the metastable-state co-conformation of the molecule. Within a Si/mol/Ti MSTJ, this co-conformation corresponds to the high conductivity or binary '1' state of the molecule, and is obtained by applying a positive voltage of about 1.5 V across the molecule (with respect to the hydrophilic stopper, or equivalently, silicon electrode; see Figure 4-2.A).

Neutrality is quickly restored to the TTF unit in the absence of an oxidizing potential; however, the $CBPQT^{4+}$ ring continues to encircle the DNP unit for a period of time due the energy barrier of $\Delta G^{\ddagger}$ = 22.5 kcal/mol ($HRT5^{4+}$) shown in Figure 4-2.B. Recovery of the ground- to metastable-state equilibrium distribution (~9:1) is a thermally activated process, and temperature-dependent relaxation-time measurements have been used to understand the kinetics of this relaxation[20, 34]. From a device perspective, relaxation from the metastable-state co-conformation ('1' state) to the ground-state co-conformation ('0' state) corresponds to the volatility or bit-retention time of a Si/mol/Ti MSTJ. For the [2]rotaxane $RTTF^{4+}$ in a 50-μm^2 MSTJ, this relaxation time was measured to be about 58 minutes at room temperature[20].

The ground-state equilibrium distribution with the $CBPQT^{4+}$ ring encircling the TTF unit (> 90%) can be recovered at least 1000 times more quickly (this is a lower limit; the actual value was not obtained experimentally)[25, 35, 36] by electrochemically reducing the two bipyridinium units in the $CBPQT^{4+}$ ring to their radical cations corresponding to the reaction $CBPQT^{4+} \xrightarrow{+2e^-} CBPQT^{\bullet\bullet 2+}$. According to previous investigations[37, 38], the doubly-reduced $CBPQT^{\bullet\bullet 2+}$ ring then loses its affinity for the π-electron-donating DNP recognition site, and the molecule relaxes back to its ground-state co-conformation with the ring encircling the TTF unit before neutrality is restored. In

terms of the solid-state switching mechanism, this corresponds to switching the molecule from its high conductivity '1' state to its low conductivity '0' state, and is accomplished by applying a negative voltage of about 1.5 V to the molecule at the hydrophilic stopper, or equivalently, to the silicon electrode of a Si/mol/Ti MSTJ.

4.3 The crossbar architecture

The crossbar (Figure 4-1) is an attractive architecture for nanoelectronic circuitry for a number of reasons[5, 9, 39]. First, nanoelectronic circuits based on the crossbar structure are tolerant of manufacturing defects[40, 41]. Each device in the crossbar structure can be uniquely addressed by two crossed wires that define the junction. If initial testing reveals that a device is defective; its address can be stored and routed around during future computations. This characteristic becomes increasingly important as electronic devices approach macromolecular dimensions and non-traditional (and imperfect) fabrication methods (*e.g.*, self-assembly) are employed. A proof-of-concept demonstration that robust computation can be obtained from a configurable circuit with defective components was given by Hewlett Packard's defect-tolerant, custom-configurable computing machine, Teramac[42]. The Teramac computer had nearly a quarter million hardware defects, but through the use of testing and configuration algorithms, it could be transformed into a robust computing machine.

Second, the crossbar architecture can be fabricated without using lithographic techniques. This is important because it is doubtful that conventional lithographic

techniques will ever be able to achieve the resolution necessary to cost-effectively fabricate a truly nanoelectronic architecture[1, 43]. Self-assembly and other non-traditional patterning methods typically generate highly regular structures, so they aren't practical for fabricating the arbitrarily complex architectures characteristic of traditional CMOS microelectronics. A crossbar structure, however, consists of only two sets of straight, aligned wires and can be readily fabricated using a variety of non-lithographic techniques. Indeed, several groups have demonstrated methods for assembling nanowires (NWs) into crossbar structures using fluidic alignment[12, 44], Langmuir-Blodgett alignment[45], and imprinting[46-48], and various architectural concepts have been introduced that can take advantage of such circuits[49-52]. However, only the superlattice nanowire pattern transfer (SNAP) method (described in Chapter 2) has been successful in producing NW arrays aligned over the length scales required for large-scale circuitry.

Third, the highly ordered nature of NW arrays has enabled the development of demultiplexing architectures capable of addressing 2^n NWs using order (n) number of control wire pairs (see Chapter 3)[53-55]. These architectures allow the selection of an individual NW from within an array that has been patterned at sub-lithographic density using relatively large wires patterned using traditional lithographic processing. This demonstrates that crossbar architectures can exhibit excellent scaling from the microscale to the nanoscale, in addition to being compatible with standard CMOS microelectronic technology.

Finally, the crossbar architecture is the highest-density two-dimensional circuit for which every device can be independently addressed[56]. Wiring overhead in a crossbar circuit is minimized because the NWs defining a junction are used to both configure and

read the device. This is in contrast to conventional CMOS-based configurable devices that require one set of wires (address lines) to configure the device and another set of wires (data lines) to read it. The ability to independently address every component in the circuit is useful for memory applications, but also enables the circuit to be fully tested for manufacturing defects so these can be routed around during configuration. However, taking advantage of the inherent density afforded by the crossbar architecture requires the development of electrically active thin-film materials that function within the two-terminal junctions of the circuit.

4.4 [2]Rotaxane molecular electronic crossbar circuits

Two-terminal molecular switches, such as [2]rotaxanes, have a number of important advantages (and some disadvantages) over more-developed two-terminal electronic materials such as ferroelectrics[57]. As discussed above, comprehensive experimental and theoretical investigations have verified the distinctly molecular basis of [2]rotaxane electrical switching. Thus, devices based on these switches should scale to macromolecular dimensions without a significant change in the switching characteristics. Solid-state-based switching materials are unlikely to exhibit similar scaling since they arise from inherently bulk properties. Two-terminal devices based on these materials are switched by applying a field across the junction to polarize crystallographic domains. The hysteresis of this polarization disappears, and the device no longer switches, once the

junctions are made smaller than the domain size of the material. For ferromagnetic materials, this is referred to as the superparamagnetic limit[58].

Another advantage of [2]rotaxane-based devices is that the voltage at which the molecular switches are opened or closed is very stable. This is because the switching mechanism is based on an electrochemical process in which current has to flow in or out of molecular orbitals before the molecule isomerizes to its high- or low-resistance co-conformations. In contrast, domain polarization is driven by nucleation events, and so is intrinsically statistical. A consequence of this nucleation-driven switching mechanism is that the field required to switch solid-state-based devices can fluctuate randomly from one device to the next within a crossbar circuit, or even from one switching cycle to the next within a single device.

In a crossbar structure, a given junction is switched by applying a voltage, V, across the wires defining the junction. To avoid switching every junction sharing one of the two address lines, V is split into $-\frac{1}{2}V$ and $+\frac{1}{2}V$ components and applied symmetrically across the two wires of the junction. Thus, junctions in the given row and column only receive half of the required switching voltage and should not switch. Nevertheless, because the required field for domain polarization is subject to statistical fluctuation, $\pm\frac{1}{2}V$ occasionally generates a sufficient field to inadvertently switch junctions that received only half the switching voltage. This is generally referred to as the 'half-select' problem and is a generic problem for crossbar circuits utilizing domain-switched electronic materials. To the contrary, the half-select problem has not been observed in the [2]rotaxane-based crossbar circuits discuss herein (discussed in Section 4.6).

Despite the significant advantages of [2]rotaxane switches in terms of scalability and operability in crossbar structures, these switches do have some drawbacks. For one, the relaxation of the switch from its low-resistance binary '1' state to its high-resistance binary '0' state is thermally activated. Thus, [2]rotaxane-based devices will show temperature-dependent variations in their operation. Another drawback is that [2]rotaxane molecular-switch tunnel junctions (MSTJs) are observed to stop functioning after a relatively low number of write cycles. In large MSTJs (~50 μm^2), this number ranges from 100 to 1000 cycles[9, 39], and is significantly less in nanometer-scale junctions. A possible explanation is that molecules along the perimeter of a junction are more susceptible to environmental damage. Reducing the area of the junction increases the fraction of molecules found along the perimeter, thus resulting in a lower average number of write cycles. Finally, because the switching mechanism is due to large-amplitude molecular mechanical motion, it is relatively slow. The solid-state kinetic processes responsible for molecular mechanical switching have been quantified for a variety of bistable [2]rotaxanes, revealing that switching occurs on a millisecond time scale[27, 29]. While quite slow compared to conventional CMOS-based switches, this is not a significant limitation since in highly parallel architectures, such as the crossbar, computational speed may be generated by switching many devices at once rather than quickly switching one device at a time.

4.5 A 160,000 bit memory circuit patterned at 1×10^{11} bits/cm^2

In 2002, the Heath and Stoddart groups reported on the use of bistable [2]rotaxane molecules as the active elements within a 64-bit molecular electronic random access memory (RAM) circuit that utilized micrometer-scale wiring[9]. While this work successfully demonstrated that [2]rotaxane molecules could be used as the active elements within in a solid-state crossbar memory circuit to store, read out, and erase small data strings, it did not take advantage of the unique scalability offered by molecular components. This would have required methods for patterning circuits with macromolecular feature sizes and pitches. The Superlattice Nanowire Pattern Transfer (SNAP) method, which can pattern ultra-dense arrays of NWs aligned over millimeter length scales, provides this capability.

A major focus of my research in the Heath group was to integrate SNAP-fabricated NW arrays with [2]rotaxane molecular materials to demonstrate an ultra-dense crossbar molecular electronic memory circuit patterned at macromolecular dimensions. In addition to demonstrating device density, we wanted to demonstrate large-scale device integration. To that end, the SNAP method was extended from previous reports[59, 60] to generate arrays of 400 NWs that were used to construct and test a 400-by-400 crossbar memory circuit at extreme dimensions. As Figure 4-4 shows, the entire 160,000-bit crossbar circuit is approximately the size of a white blood cell (~13×13 μm^2).

The fabrication of this molecular memory circuit proved to be a significant challenge on many fronts. First and foremost was the inherent difficulty in making

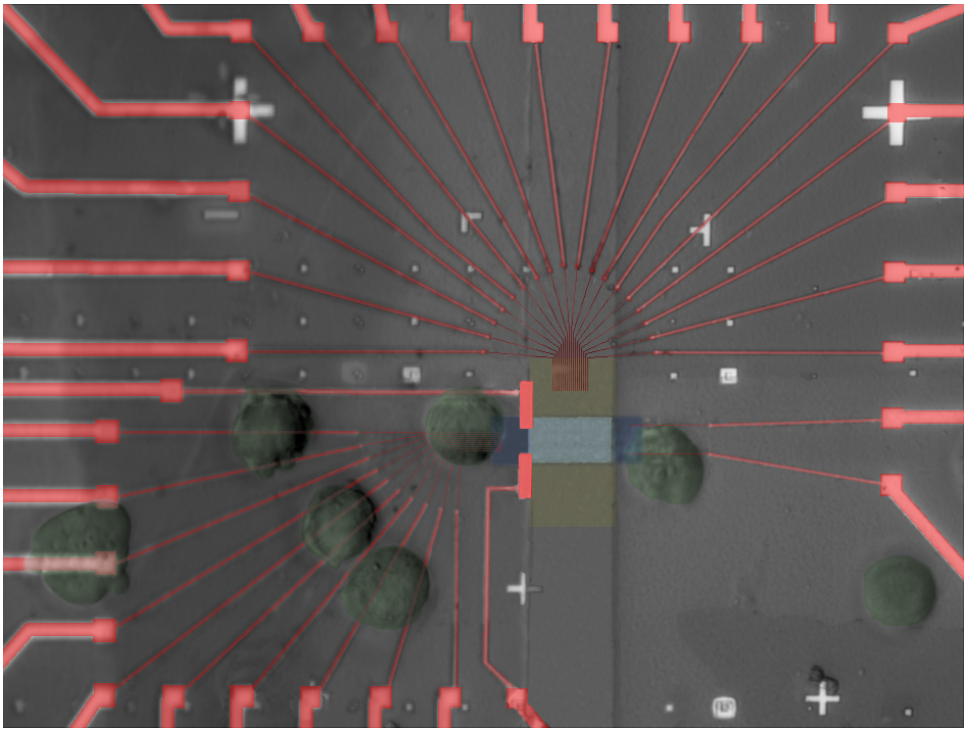

Figure 4-4. A false-colored optical micrograph of a memory circuit with white blood cells for scale. White blood cells (shown in green) approximately 15 micrometers in diameter were sprinkled over this functional memory circuit to provide a biological metric for the level of device integration accomplished in this work. All 160,000 bits are contained within the intersection of the yellow and blue rectangles.

devices at the density described herein, and of integrating those devices into large-scale functional circuits. This is emphasized by contrasting the level of device integration in our molecular memory with its analog in conventional microelectronic technology, the dynamic random access memory (DRAM) circuit. The 2005 International Technology Roadmap for Semiconductors (ITRS) consortium reports[1] that current DRAM circuits are patterned with a memory cell size of 0.04 μm^2 and a density of 1.5×10^9 bits/cm^2. For comparison, the molecular memory described here is about two orders of magnitude more dense with a memory cell size of 0.001 μm^2 and device density of 1×10^{11} bits/cm^2. In fact, this level of integration is on par with 'ultimately scaled' CMOS-based

microelectronic technology, which ITRS projects may reach a cell area of 0.001 μm^2 and density of 5×10^{10} bits/cm^2 by the year 2020.

An additional fabrication challenge was developing a process flow compatible with the delicate [2]rotaxane molecular monolayers. This was accomplished by adopting a fabrication scheme in which the memory was built up sequentially, with the molecular monolayer incorporated as close to the final step as possible, and then protecting that monolayer during subsequent processing steps. It also required establishing electronic-measurement protocols that could be employed to follow the conductivity status of the NWs during the entire nanofabrication procedure. Details of this process flow, along with the various electronic testing protocols, are discussed in Section 4.6. However, a list of the major steps in memory fabrication is as follows:

1. Use SNAP to fabricate the bottom array of Si NW electrodes.
2. Pattern all necessary electrical contacts using electron beam lithography.
3. Planarize the chip using a spin-on glass.
4. Deposit the [2]rotaxane monolayer and evaporate a thin Ti layer on top.
5. Deposit a Pt NW array over the molecule/Ti layer perpendicular to the Si NWs.
6. Using dry etching, transfer the Pt NW pattern to the underlying Ti layer.

Note that, in the last step, the Pt NW pattern only serves as a mask to define an array of Ti NWs from a continuous Ti film. This fabrication protocol not only minimizes the number of processing steps after deposition of the molecular monolayer, but also uses the Ti layer to both protect the molecules and serve as the top electrode in the molecular-

switch tunnel junctions. This technique has been shown, via infrared spectroscopy in conjunction with electronic transport measurements, to protect the functional sites of the [2]rotaxane molecules by reacting with the hydrophobic end groups while leaving the functional regions of the molecule unscathed (Figure 4-2.A)[22].

The structure of our crossbar molecular memory circuit is shown in Figure 4-5.A, and consists of a bottom electrode set of 400 Si NWs (16-nm wide, 33-nm pitch; highly phosphorous doped, as discussed in Chapter 2, $n = 5\times10^{19}$ cm^{-3}) crossed by a top electrode set of 400 Ti NWs (16-nm wide, 33-nm pitch) sandwiching a monolayer of bistable [2]rotaxanes. Each bit corresponds to an individual molecular-switch tunnel junction defined by a Si bottom NW and Ti top NW, and contains approximately 350 [2]rotaxane molecules. The solid-state switching signature of the bistable [2]rotaxanes that were used in this study has been shown to originate from electrochemically addressable, molecular mechanical switching for C/mol/metal or Si/mol/metal junctions[61], but not for metal/mol/metal wire junctions[62]. The desire to utilize molecular mechanical bistable switches as the storage elements is what dictated the choice of the Si NW/mol/Ti NW (Si/mol/Ti) crossbar structure.

Electrical contacts were established to several bottom and top NWs to allow for testing of up to 180 ‘effective’ bits (ebits) from the central region of the crossbar, but only 128 were actually tested due to measurement constraints. The ‘effective’ prefix is used because SNAP-fabricated NWs are patterned beyond the resolution of lithographic methods[63], so each contact bridges 2–4 NWs (Figure 4-5.B). As a result, most of the tested ebits contained an average of 4–9 junctions. We recently reported on a demultiplexer[54] (see Chapter 3) that would allow for this memory circuit to be fully

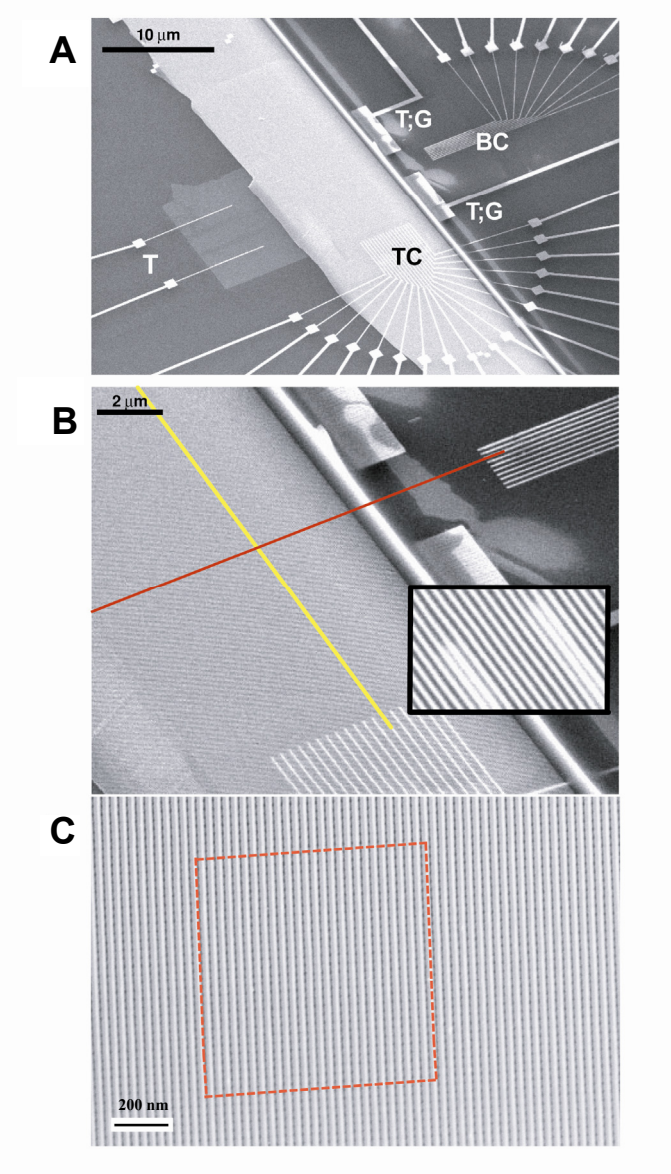

Figure 4-5. Scanning electron micrographs (SEMs) of the NW crossbar memory. A. Image of the entire circuit. The array of 400 bottom Si NWs is seen as the light grey rectangular patch extending diagonally up from bottom left. The top array of 400 Ti NWs is covered by the SNAP template of 400 Pt NWs, and extends diagonally down from top left. Testing contacts (T) are for monitoring the electrical properties of the Si NWs during the fabrication steps. Two of those contacts are also grounding contacts (G), and are used for grounding most of the Si NWs during the memory evaluation, writing, and reading steps. Electron-beam-lithography patterned 18 top (TC) and 10 bottom (BC) contacts are also visible. The scale bar is 10 micrometers. **B.** An SEM image showing the cross-point of top and bottom NW electrodes. Each cross-point corresponds to an 'effective bit' in memory testing because (inset) the electron-beam-lithography defined contacts bridged 2–4 nanowires. The scale bar is 2 micrometers. **C.** High-resolution SEM of approximately 2500 junctions out of a 160,000-junction nanowire crossbar circuit. The red square highlights an area of the memory that is equivalent to the number of bits that were tested. The scale bar is 200 nanometers.

tested, including the ability to address each junction independently. However, implementation of that demultiplexer would have added significant complexity to an already demanding nanofabrication procedure, and wasn't necessary to demonstrate the viability of this circuit. (This limitation simply adds some level of uncertainty to our estimates of device yield.) Assuming 4–9 junctions per ebit, the 128 ebits tested represents between 0.5–0.7 percent of the full 160,000-bit crossbar circuit distributed across 6 percent of the device area (Figure 4-5.C). We believe that this relatively small portion of the crossbar is representative of the overall circuit. This belief is based upon the fact that we have fabricated approximately 50 full 160,000-junction crossbar memory circuits, four of which have been fully tested as memories. Each of those tested memory circuits yielded similar results.

By scanning-electron-microscopy inspection, the 160,000-junction crossbar appeared to be structurally defect-free, with no evidence of broken, wandering, or electrically shorted NWs (Figure 4-5.B). Nevertheless, there were a large number of electrical defects. Comprehensive electrical characterization was used to determine the address locations of both working and defective ebits, as well as to provide insight into the nature of the defective ebits. This was done by first applying +1.5 V relative to the Si NW electrodes to set all ebits to '1', or alternatively to switch the [2]rotaxane molecules to their metastable-state co-conformation. Each ebit was then read sequentially using a non-perturbing +0.2 V bias. Application of –1.5 V to the Si electrode was then used to set all ebits to '0'; this effectively returned the active molecular monolayer to its ground-state co-conformation. The status of each of the 128 ebits was then read again. The 1/0 current ratios are presented in Figure 4-6.A. Approximately 50 percent of the tested ebits

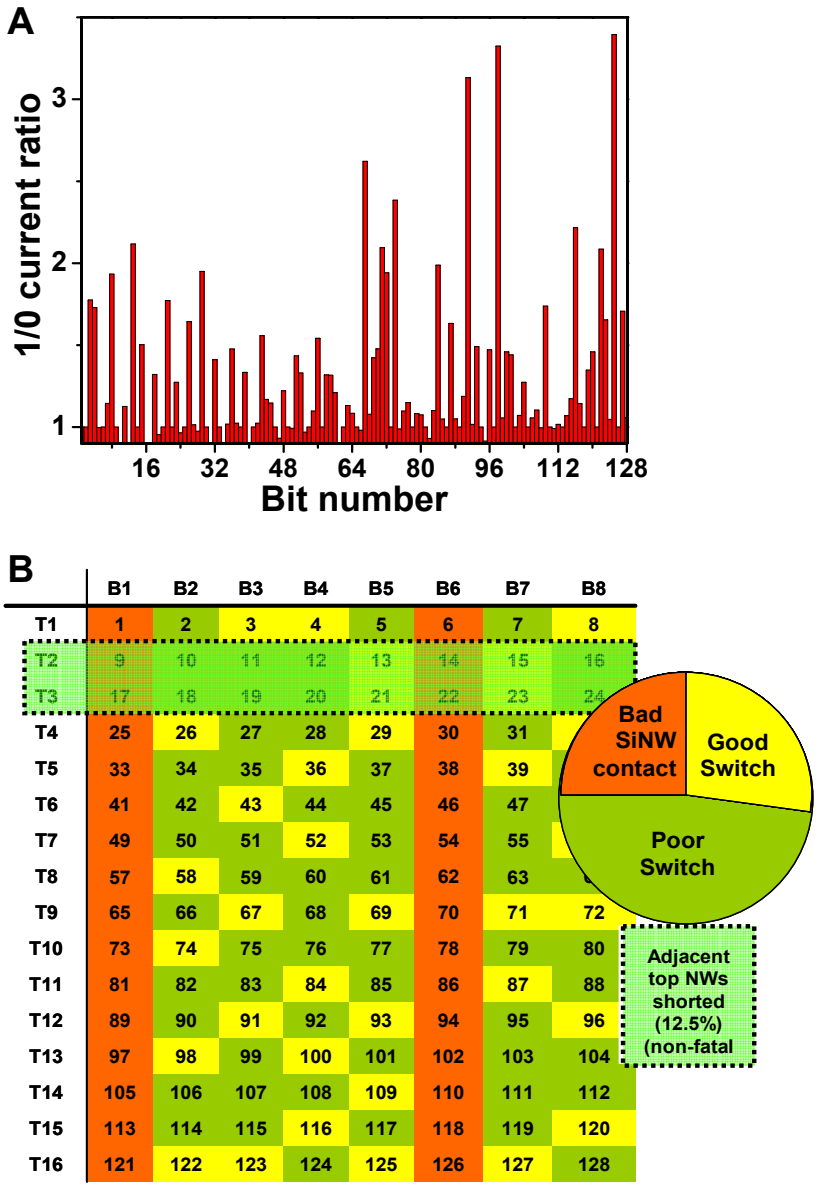

Figure 4-6. Data from evaluating the performance of 128 ebits within the crossbar memory circuit. **A.** The current ratio of the '1' state divided by the '0' state of the tested ebits. Note that many of the ebits exhibit little to no switching response. Those ebits are defective. **B.** A map of the defective and usable ebits, along with a pie-chart giving the testing statistics. Note that, except for the bad Si NW contacts on bottom electrodes B1 and B6, and the shorted top electrodes, T2 and T3, the defective and good bits are randomly distributed. Poor switches can be divided into two types: Type I defects (26% of the 128 tested) are ebits that exhibited an open-circuit conductance and a low- or zero-amplitude switching response when tested. Type II defects (22%) are non-switchable ebits that exhibited a conductance similar to that of a closed switch. In both cases, the 1/0 ratio is near unity.

yielded some sort of switching response; however, some of those ebits may have been exhibiting behavior originating from assorted parasitic current pathways through the crossbar array.

Multiple current pathways between an input and output electrode are an inherent drawback of crossbar architectures wherein each junction is electrically connected to every other junction. Thus, when many devices are switched from the '0' to the '1' state, the current through the non-switching devices can also change due to a modification of the effective resistance of these parasitic loops. A standard remedy is to incorporate diodes at each crosspoint[64] that will suppress parasitic loops by acting as one-way current valves. Although the molecule/Ti interface yields some built-in rectification, we have additionally fabricated micrometer-scale molecular electronic memory circuits with a vertical p-n doping gradient through each junction[19]. This resulted in improved memory performance that should, in principle, extend to the nanometer-scale memory described here. For this prototype circuit, however, we found it sufficient to simply ground all NW electrodes not being used during a read cycle in conjunction with the establishment of a threshold for a 'good' ebit based upon a minimum 1/0 current ratio of ~1.5. About 25 percent of the ebits passed this threshold. While this yield may be low for a mature technology, we are very encouraged by this result in an unpackaged first-generation circuit.

Defective bits impacted memory performance with varying levels of severity (Figure 4-6.B). Bits with a 1/0 ratio of unity were classified as 'poor switches' and resulted from switches stuck in either the '1' or '0' state. Poorly switching bits only lead to a proportional loss in memory performance. Bad contacts to the NWs, however,

removed an entire row of bits from memory operation. In a similar vein, two Ti electrodes that are shorted together effectively turn two rows of bits into one row of usable bits—also removing a row of bits from operation and doubling the number of junctions in the ebits for that row. We believe the majority of these defects resulted from sub-nanometer variations in the reactive-ion etching process that was employed to define the top Ti NWs. As will be explained more fully in the next section, these Ti NWs originate as a uniform thin film (~20 nm) that is deposited on top of the [2]rotaxane Langmuir monolayer. The SNAP process is used to deposit 400 Pt NWs on top of this film, and those Pt NWs serve as an etch mask for defining the 400 top Ti electrodes. The capability of etching tools to define nanostructures at the narrow pitches required here is largely unexplored and, in fact, this etching step was one of the most challenging nanofabrication steps for constructing the memory.

Isolated devices, or crossbar memories patterned at substantially lower densities and with larger wires, can typically be prepared with a nearly 100 percent yield. The capability of etching tools to define nanostructures at the narrow pitches required here is largely unexplored and, in fact, was one of the most challenging nanofabrication steps in constructing the memory.

An important result from the defect map shown in Figure 4-6.B is that the good and bad ebits are randomly dispersed throughout the matrix, implying that the good junctions are not correlated to one another. However, the ultimate test of any memory circuit is whether it can store information. Based upon the defect map shown in Figure 4-6.B, and taking advantage of the inherent defect tolerance of the crossbar architecture[42], we were able to identify the addresses of good ebits, and from those addresses configure

an operational memory. This is demonstrated by the data of Figure 4-7 in which we have utilized 24 out of 30 operational ebits to write a string of '1's and '0's that represent the ASCII characters for 'CIT,' short for 'California Institute of Technology.'

Our principle motivation for utilizing bistable [2]rotaxane molecules as the active elements within this memory is that even though we are measuring of order 100 molecules in each junction, the change in conductivity correlated with the two conformational states is a single-molecule property[20, 27, 34]. The implication is that the switching signature should be effectively size-invariant (neglecting statistical effects), meaning that it should scale down to the macromolecular dimensions that characterize these crossbar junctions. In fact, the success of these molecules at this scale implies that next-generation devices using only tens of molecules may be possible. While it may be unlikely that these digital circuits will scale to a density that is only limited by the size of the molecular switches, it should be possible to significantly increase the bit density over what is described here (Section 4.6).

Previous work (see Section 4.2) has quantified the thermodynamic and kinetic parameters that describe both the bistability and the switching mechanism of the [2]rotaxane (Figure 4-2.A) and related molecules in a variety of environments. Those measurements required robust switching devices that could be cycled many times and at various temperatures. The junctions measured here were much more delicate: While all good ebits could be cycled multiple times (as evidenced by the testing and writing steps), most ebits failed after a half-dozen cycles or so. While the exact failure mode is still under investigation, it is worth noting that these junctions have a very large perimeter-to-area ratio, and that molecules along the perimeter of a junction are likely to be more

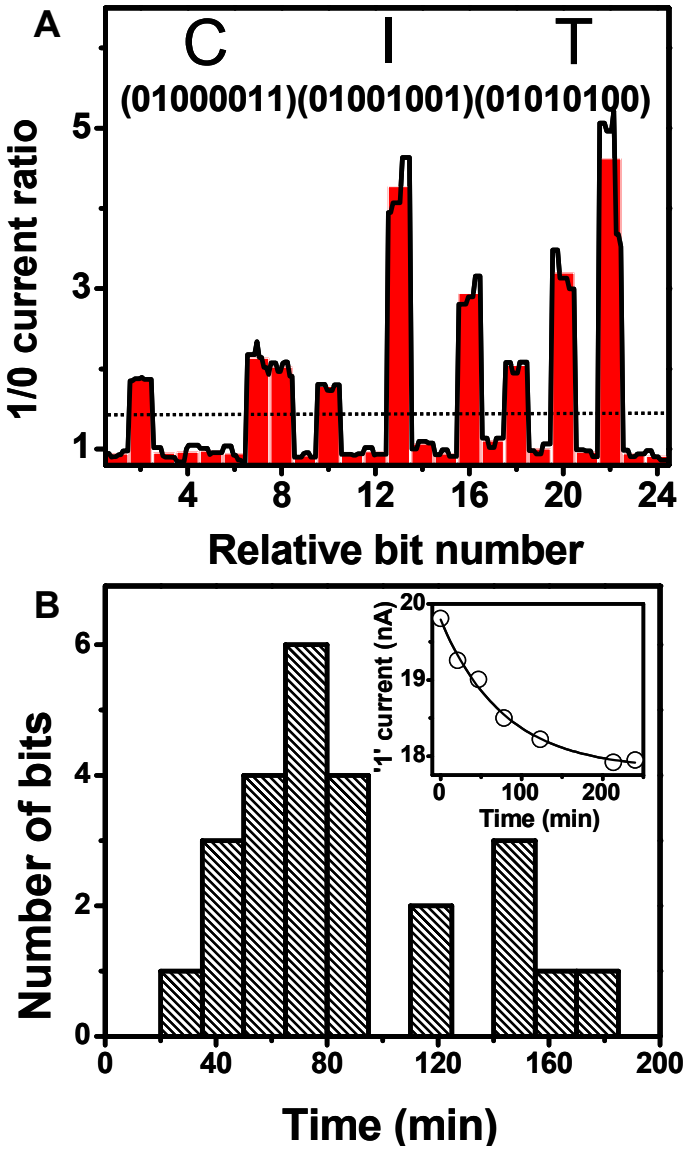

Figure 4-7. Demonstration of memory storage and retention characteristics from the molecular electronic crossbar memory. A. A demonstration of point-addressability within the crossbar. Good ebits were selected from the defect mapping of the tested portion of the crossbar. A string of '0's and '1's corresponding to ASCII characters for 'CIT' (abbreviation for California Institute of Technology) were stored and read out sequentially. The dotted line indicates the separation between a '0' and '1' state of the individual ebits. The black trace is raw data showing ten sequential readings of each bit while the red bars represent the average of those ten readings. Note that deviations of individual readings from their average are well separated from the threshold 1/0 line. **B.** A histogram representing the 1/*e* decay time of the '1' state to the '0' state. The 25 ebits represented in the data each were 'large' ebits, comprised of approximately 100 junctions, to increase the measurement signal to noise. Raw data from a single large ebit is shown in the inset. The line is a single exponential fit used to extract the decay time.

susceptible to processing damage or contamination since the circuit is measured under ambient conditions (*i.e.*, the circuit is unpackaged). Despite this difficulty, we were able to measure the rate of relaxation from the 1→0 state for many of the ebits (Figure 4-7.B). From a device perspective, this time represents the volatility, or memory retention time, of the ebits. With respect to the bistable [2]rotaxane switching cycle, this time represents a room-temperature measurement of the rate-limiting kinetic step within the switching cycle wherein the metastable co-conformation relaxes to the ground state. Our measured rate (90 ± 40 minutes; median decay = 75 minutes) was statistically equivalent to the rate reported for much larger devices (50 μm^2 junction area) containing the same [2]rotaxane switches (58 ± 5 minutes) and measured using a more comprehensive thermodynamic analysis[20]. Thus, our results are consistent with previous reports of a molecular mechanism for the memory operation[9].

4.6 Crossbar molecular memory circuit fabrication and testing

In this section, I will discuss the details of memory fabrication and testing. In an effort to keep this section more or less self-contained, some of the material mentioned above is repeated (albeit with greater detail). A bottom-up approach was critical to the successful fabrication of this memory. This approach both minimized the number of processing steps following deposition of the delicate molecular monolayer, as well as protected the molecules from remaining processing steps. The following in-depth description of how

this memory was fabricated will proceed with an analogous structure, that is, from the bottom up.

The 160,000-junction crossbar memory described above consists of 400 Si nanowire (NW) bottom electrodes of 16-nm width and 33-nm pitch, crossed with 400 Ti NW top electrodes of the same dimensions, and with a monolayer of bistable [2]rotaxane molecules sandwiched in between. We have previously reported on using the superlattice nanowire pattern transfer (SNAP) technique to fabricate highly ordered arrays of metal and Si NWs of up to 128 NWs. For this work, the SNAP technique was extended to create 400-element NW arrays of both the bottom and top electrode materials, and so was the primary patterning method for achieving the 1×10^{11}-cm^{-2} bit density of the crossbar. The SNAP NW fabrication procedure is described in detail in Chapter 2. Briefly, SNAP is a 'top-down,' non-photolithographic technique that uses molecular-beam epitaxy (MBE) to create a physical template for NW patterning. This template is used to deposit an array of Pt NWs onto an epoxy-coated thin-film material. The Pt array then serves as an etch mask to transfer the NW pattern into the underlying thin-film. This technique enables the fabrication of ultra-dense arrays of high-aspect-ratio (length to width routinely > 10^6) Si and metal NWs that are aligned over millimeter length scales, without the need for a secondary alignment step after NW fabrication.

4.6.1 Fabrication and contact to bottom Si nanowire electrodes

An overview of the process flow used to fabricate the memory is shown in Figure 4-8. The Si NW array was fabricated as described in Chapter 2. The starting wafer for the Si

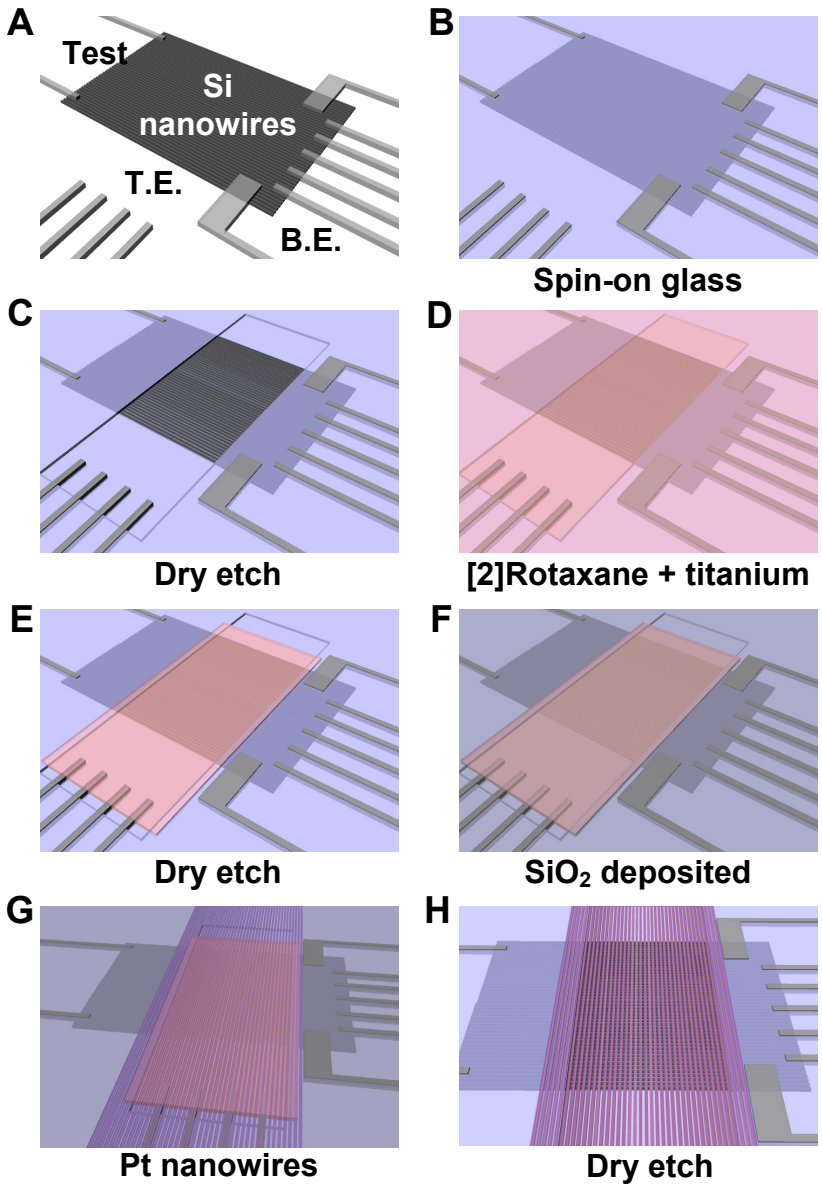

Figure 4-8. Process flow for fabricating the 160,000 bit molecular electronic memory circuit at 10^{11} bits/cm^2. A. A section of SNAP-patterned SiNW bottom electrodes are electrically contacted to electron-beam lithography patterned metal electrodes. **B.** The entire circuit is coated with SiO_2 using an optimized spin-on-glass procedure. **C.** The active memory region is exposed using lithographic patterning followed by CF_4 dry etching. **D.** The bistable [2]rotaxane Langmuir monolayer is deposited on top of the Si NWs and then protected by the deposition of a Ti layer. **E.** The molecule/Ti layer is etched everywhere except for the active memory region. **F.** An evaporated SiO_2 insulating layer is deposited over the entire chip. **G.** An array of Pt NWs is deposited on top of the Ti/SiO_2 layer at a right angle to the bottom Si NWs using the SNAP method. **H.** The Pt NW pattern is transferred, using BCl_3 dry etching, to the underlying Ti layer to form an array of top Ti NW electrodes, and the crossbar structure is complete.

NWs was a 33-nm-thick silicon-on-insulator (SOI) substrate with a 250-nm-thick buried oxide (Simgui, Shanghai, China). This wafer was highly diffusion doped (phosphorous; $n=5\times10^{19}$ cm^{-3}) to ensure that NWs fabricated from it would maintain robust conductivity throughout the various nanofabrication procedures, in addition to forming ohmic contacts with Ti-Pt leads. This proved to be important in later stages where the Si NW surface is unavoidably etched. To fabricate the Si NW array, an array of Pt NWs was deposited onto the doped SOI substrate using the SNAP method, and high-frequency (40 MHz) fluorine-based (CF_4 to He 20:30, 5 mTorr, 40 W) reactive-ion etching was used to transfer the Pt NW pattern into the underlying Si epilayer to form an approximately 2-millimeter-long array of Si NWs. The Pt NW array was then dissolved in hot aqua regia (1:4 conc. HCl to conc. HNO_3, 120° C, 10 min) and the Si NW array was sectioned into a 30-μm-long region using a lithographically-patterned Al mask and three sequential reactive-ion etch (RIE) steps. The first was a high-power O_2 RIE (20 mTorr, 100 W, 2 min) to remove any residual epoxy (from the SNAP procedure), then a brief SF_6 RIE (5 mTorr, 30 W, 30 sec) to remove any unmasked Si, and finally a low-power O_2 RIE (20 mTorr, 10 W, 2 min) to oxidize any pinholes through the insulating oxide that may have been bored out from the first two RIE steps. We had occasionally observed leakage current through the insulating oxide when this last step was omitted.

Ten electrical contacts to these bottom Si NWs, as well as 18 contacts that are intended for the top Ti NWs, were defined at this point using standard electron-beam lithography (EBL) patterning and electron-beam evaporation to produce wires consisting of a 15-nm Ti adhesion layer followed by 50 nm of Pt (Appendix 4.1). Immediately prior to metal evaporation, the Si NWs were cleaned using a gentle O_2 plasma (20 mTorr, 10

W, 30 seconds) followed by a 5-second dip in buffered oxide etch (BOE) (6:1; NH_4F to HF) solution to remove the Si NW native oxide. After metal lift-off, the chip was annealed at 450 °C in N_2 for 5 minutes. In addition to promoting the formation of ohmic contacts, this anneal helped to prevent peeling of the smallest lithographically-defined wires during the spin-on glass step described below.

Figure 4-9.A shows an SEM image of the memory circuit at the stage in which the Si NWs and all of the external electrical contacts have been created. Note that there are four sets of EBL-defined contacts. The 18 narrow contacts at the bottom left of the image (nominal width of 70 nm at 300-nm pitch) will eventually connect to the top Ti NW electrodes and are used for testing of the final memory circuit. The ten narrow contacts to the Si NWs at the bottom right (nominal width of 60 nm at 300-nm pitch) of the image are also used for testing of the memory circuit. Finally there are two narrow test electrodes at the top left and two wide electrodes at the bottom right. The wide electrodes contact about two-thirds of all the Si NWs and serve a dual function. First, they ground unused Si NWs during memory testing to minimize parasitic current loops through the crossbar. (This procedure approximates how a fully multiplexed crossbar circuit would be utilized.) Second, when used in conjunction with the two narrow test-electrodes on the opposite side of Si-NW array, they enable testing of the Si-NW conductivity at various stages throughout the memory-fabrication processes. This testing procedure provided invaluable feedback for finely tuning and tracking many of the fabrication processes, most notably the etching procedures described below. Once these various contacts were established, robust Si-NW conductivity was confirmed via current-voltage (*I-V*) measurements. If the Si NWs were measured to be poor conductors (a very infrequent

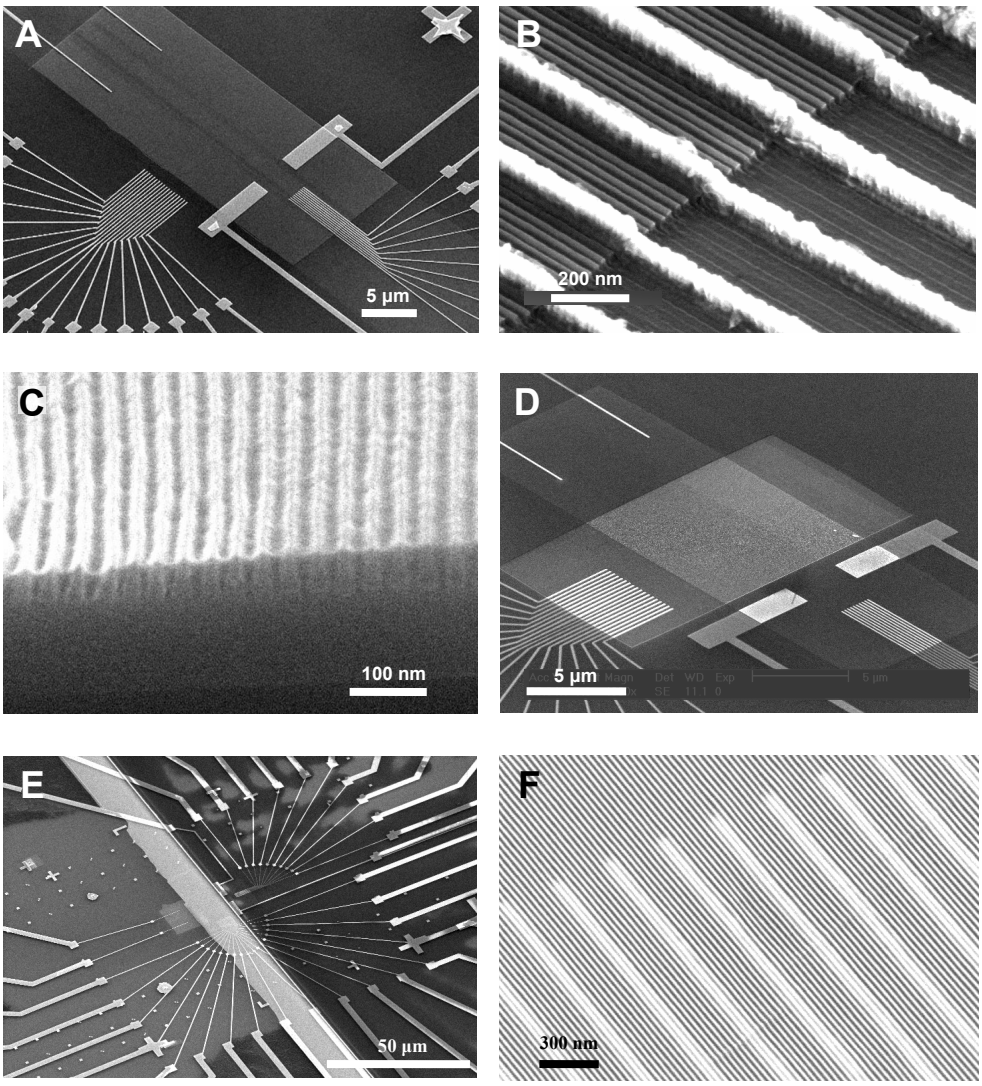

Figure 4-9. Representative scanning electron micrographs illustrating the crossbar memory fabrication process. A. A 30-micrometer-long section of 400 Si NWs with electron-beam lithography (EBL) defined contacts to the Si NWs (bottom right) and pre-patterned contacts to the Ti-NW array (not deposited at this stage) (bottom left). **B.** Representative contacts to Si NWs showing each EBL-defined metal lead is about 70-nm wide and contacts 2–4 NWs. **C.** Micrograph verifying that the spin-on-glass layer fills the narrow trenches between the Si NWs. The chip was cleaved after the planarization process to allow for the view shown here. **D.** Lithographically patterned window in the SOG film defining the memory active region. **E.** Deposition of 400 Pt NWs over the memory active region. Note the Pt NWs extend for about a millimeter in either direction. **F.** Micrograph of the Ti NWs contacting pre-patterned EBL-defined leads after transferring the Pt NW pattern to the underlying [2]rotaxane/Ti layer.

occurrence) or if there was any measurable leakage current through the insulating oxide, the chip was discarded. Additionally, the chip was discarded if *I-V* measurements showed rectification at the contacts (unless ohmic behavior could be established through further efforts).

The device was then planarized using an optimized spin-on-glass (SOG) procedure (Accuglass 214, Honeywell Electronic Materials, Sunnyvale CA) (Figure 4-8.B). This planarization process is critical because the SOG not only protects Si NWs and EBL defined wiring outside of the active memory region from damage that can arise during subsequent processing steps, but it also prevents evaporated Ti from entering the gaps between Si NWs where it would be extremely difficult to remove. For the SOG to fill the narrow gaps between adjacent Si NWs (Figure 4-9.C), it had to be applied to the surface of the chip while under vacuum (< 1 mTorr). This was accomplished by placing the chip into a clean Erlenmeyer flask* sealed with an air-tight rubber septum and piercing the septum with a syringe needle attached via tubing to a diffusion pump. After a couple of minutes to ensure evacuation of the flask, a scrupulously-clean glass syringe and a 5-inch metal needle were used to generously apply the SOG liquid to the chip surface (while maintaining vacuum with the other needle). The chip was then immediately taken out of the flask and spun at 5000 RPM to ensure a uniform film.

At this point, the chip was inspected using a light microscope to look for any particulates on the surface. If any were found (which almost inevitably there were), the SOG film was stripped from the chip with extremely delicate swabbing while immersed in methanol, followed by repeatedly rinsing in methanol and isopropyl alcohol and drying

* The flask was modified with a cylindrical glass pedestal for mounting the chip off the flask bottom.

under a stream of N_2. The repeated solvent rinses followed by blowing with N_2 seemed to be particularly effective at removing particles from the surface. Sonication was avoided because it would occasionally damage the finest EBL-defined wires. The SOG was then re-applied to the chip under ambient conditions, spun at 5000 RPM, and re-checked for particulates. Note that vacuum application was found to be unnecessary for subsequent SOG applications, probably because the SOG applied under vacuum continued to wet the NW gaps through subsequent methanol cleanings. This entire procedure was repeated until no particulates were seen on the chip surface. It was very important to ensure that the chip was rigorously clean before proceeding, since particles on the surface would frequently result in an unsuccessful transfer of the Pt NW array (which is required in a later step to define the top Ti NW electrodes for the memory).

After globally thinning the SOG layer to 50 nm using a CF_4 plasma (10 mTorr, 40 W), an opening in polymethyl-methacrylate (PMMA) was lithographically defined over the Si NWs, and the tips of the 18 EBL-defined contacts (Figure 4-8.C). The SOG was then further etched until the tops of the underlying Si NWs were exposed (Figure 4-9.C). This step was monitored by periodically measuring the Si NW conductivity using the test electrodes. The majority of dopant atoms in the Si NWs reside within 10 nm of the surface (Chapter 2), so the NW conductivity is very sensitive to any etching of the surface. This unique feature of SNAP-fabricated Si NWs makes it very straightforward to etch back the SOG until just the tops of the Si NWs are exposed, since the etch end-point can be precisely determined by a small drop in the Si NW conductivity. At this stage, the entire memory circuit is under SOG (and thus electrically isolated from any further top

processing) except for the lithographically-defined opening over the Si NWs and the 18 EBL-defined contacts. This opening defines the active memory region (Figure 4-9.D).

4.6.2 Deposition of molecules and top electrode materials

A monolayer of bistable [2]rotaxane switches was prepared by Langmuir-Blodgett techniques and transferred onto the device, as reported previously[9, 22]. A thin film of Ti (20 nm) was then evaporated over the entire chip (Figure 4-8.D). This Ti layer serves to protect the molecules from further top processing and will later be patterned into the crossbar top electrodes. As briefly mentioned above, this Ti layer additionally adds (favorable) current rectification to each Si/mol/Ti MSTJ to reduce the impact of parasitic current pathways within the crossbar circuit. The amount of rectification is dependent upon the amount of Ti oxidation that occurs at the molecule/Ti interface, which, in turn, depends upon the vacuum level of the metal deposition system[65-67]. For this work, the Ti was deposited at a pressure of approximately 5×10^{-7} Torr. For micrometer-scale Si/mol/Ti MSTJs, this typically produced a rectification of about 10:1 at 1 V.

Using photolithographic techniques and BCl_3 RIE (5 mTorr, 30 W), the molecule/Ti layer was then removed from everywhere except for the memory active region where electrical contact to the underlying Si NWs is made (Figure 4-8.E). Patterning the Ti film is important for two reasons: First, it prevents the deposited Ti film from bridging (shorting) EBL-defined wiring that protrudes from the SOG film (explained below). Second, it removes the requirement of precise NW registry over the entire length (> 1 millimeter) of the Pt NW array deposited in a later step (Figure 4-9.E).

This is important because the dry etch used to define the Ti NW pattern from the Pt NW stencil can cause adjacent Pt NWs to wander into each other (thus shorting the corresponding Ti NWs beneath) in regions with non-uniform epoxy (used to adhere the Pt NW array to the surface; explained further below). Over the length of a typical SNAP-fabricated NW array, the likelihood of this occurrence is expected to be almost certain.

Next, a thin (~15 nm) SiO_2 layer was deposited over the entire substrate to isolate the EBL-defined wires from the Pt NWs to be deposited in the next step. (Recall that the EBL-defined wires are 65-nm tall and the SOG was globally thinned to 50 nm; Figure 4-8.F.) It may seem that the SiO_2 deposition can be avoided by etching the SOG film to a thickness greater than the EBL-defined wire height. However, this results in a larger recess in the SOG opening that defines the memory active region. Spin-coated epoxy used for Pt NW deposition in the next step fills this opening, which, as explained below, can be problematic during subsequent etching.

A thin layer of epoxy (~10 nm) is then spin-coated onto the chip and the SNAP technique is used to deposit an array of 400 Pt NWs over the Ti/SiO_2/epoxy layer at a right angle to the underlying Si NWs (Figure 4-8.G and Figure 4-9.E). Finally, careful BCl_3 RIE (5 mTorr, 30 W) was used to transfer the Pt NW pattern to the underlying Ti/SiO_2/epoxy film, thus forming Ti NW top electrodes (Figure 4-8.H). Although the Pt NW array is in excess of 1 mm long (Figure 4-9.F), the top Ti electrodes of the crossbar circuit only extend from the tips of the 18 EBL-defined leads to a couple of micrometers past the underlying Si NW array. The etch endpoint was determined by monitoring the

cross-conductance of the top Ti NWs* (Figure 4-10.A). Complete transfer of the Pt NW pattern to the underlying Ti film is indicated by a fall in the cross-conductance to about ten nanoSiemens (nS). Note that the cross-conductance does not go to zero since the Ti electrodes, while physically separated, are still electrically coupled through the crossbar

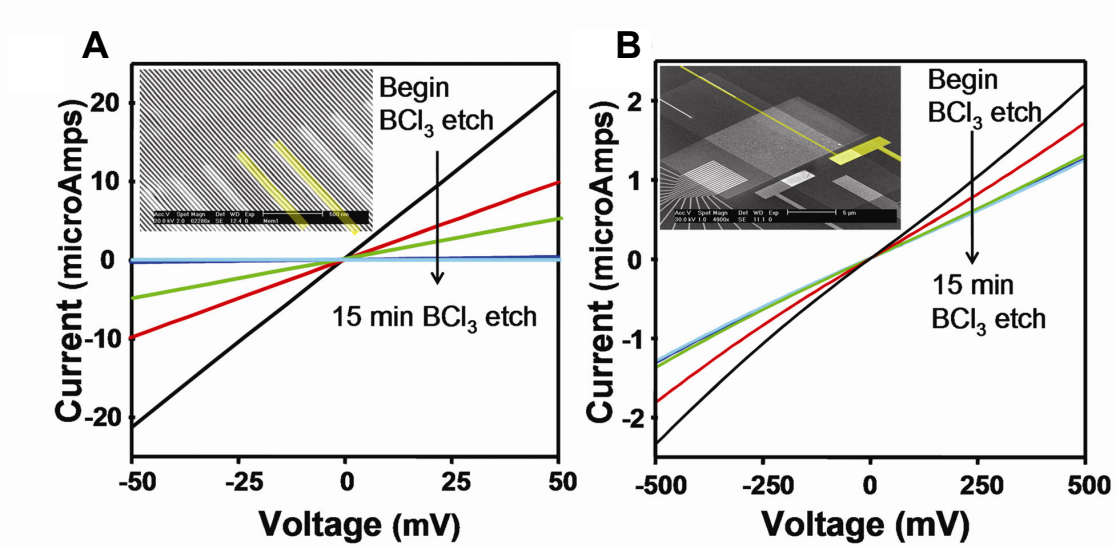

Figure 4-10. Conductance monitoring during the Ti layer etching. A. Cross-conductance measurements between electrical contacts to the top nanowire array were performed to monitor the Ti layer etching. When the current drops to sub-10 nanoAmps, the top Ti electrodes are separated. The inset scanning electron microscope (SEM) image shows two representative contacts to the top Ti electrodes as highlighted in yellow. It is the cross-conductance between such contacts that was used for this measurement. **B.** The Si NW conductance was measured throughout the Ti layer etching to ensure that Si NWs were not damaged. The SEM image (inset) shows the current pathway that was measured.

junctions and the underlying Si NWs. The health of the underlying Si NWs throughout the Ti-etching process was also monitored, as shown in Figure 4-10.B.

The use of Ti as the top electrode material here was necessary since its high reactivity prevents metal from spiking across the [2]rotaxane monolayer during evaporation[22]. However, Ti is a difficult metal to etch because it forms a tough TiO_2 layer

* Interferometric end-point detection cannot be used here since the etch rate for Ti within a 16-nm trench is likely to be quite different from that of a regular Ti surface.

at its surface[68]. Highly-directional BCl_3 reactive ion etching was used because it provides the needed momentum to erode the TiO_2 layer while additionally providing reactive Cl ions to chemically remove Ti. Figure 4-11 shows a fully functional memory circuit in which the final Pt NW deposition (using SNAP) was substituted by EBL-patterned Pt microwires (about 210 nm in width) of variable spacing down to 90 nm (less than 3 times the SNAP Pt NW pitch). The [2]rotaxane/Ti film was etched using an iterative procedure so the Ti electrode cross-conductance could be periodically checked. Also, SEM analysis was used to gauge how effectively the BCl_3 etch removed Ti from between the Pt microwires after each etch iteration. Note that SEM analysis cannot be used to track the etch progress using SNAP fabricated Pt NWs because 1) the SNAP NW spacing is too narrow, and 2) the electron beam heats up the underlying epoxy causing the Pt NWs to collapse into each other. SEM analysis confirmed complete separation of the underlying Ti electrodes after the Ti electrode cross-conductance fell to below 50 nS (Figure 4-11.A). Taking into account that the (210-nm-wide) EBL-defined Ti microwires are about five times wider than the combined average number Ti NWs defining a row of ebits (3×16 nm = 48 nm), we reasoned that Ti NWs patterned from SNAP-fabricated Pt NWs would be separated when their cross-conductance fell to below 10 nS. We have found this metric to be accurate with many memory chips. Note that while the Ti electrode cross-conductance at separation scales linearly with the Pt wire width, the total etch time does not scale predictably with the Pt wire spacing. In fact, the total etch time to achieve Ti NW separation can vary considerably from one memory chip to the next with nominally identical SNAP Pt NW arrays.

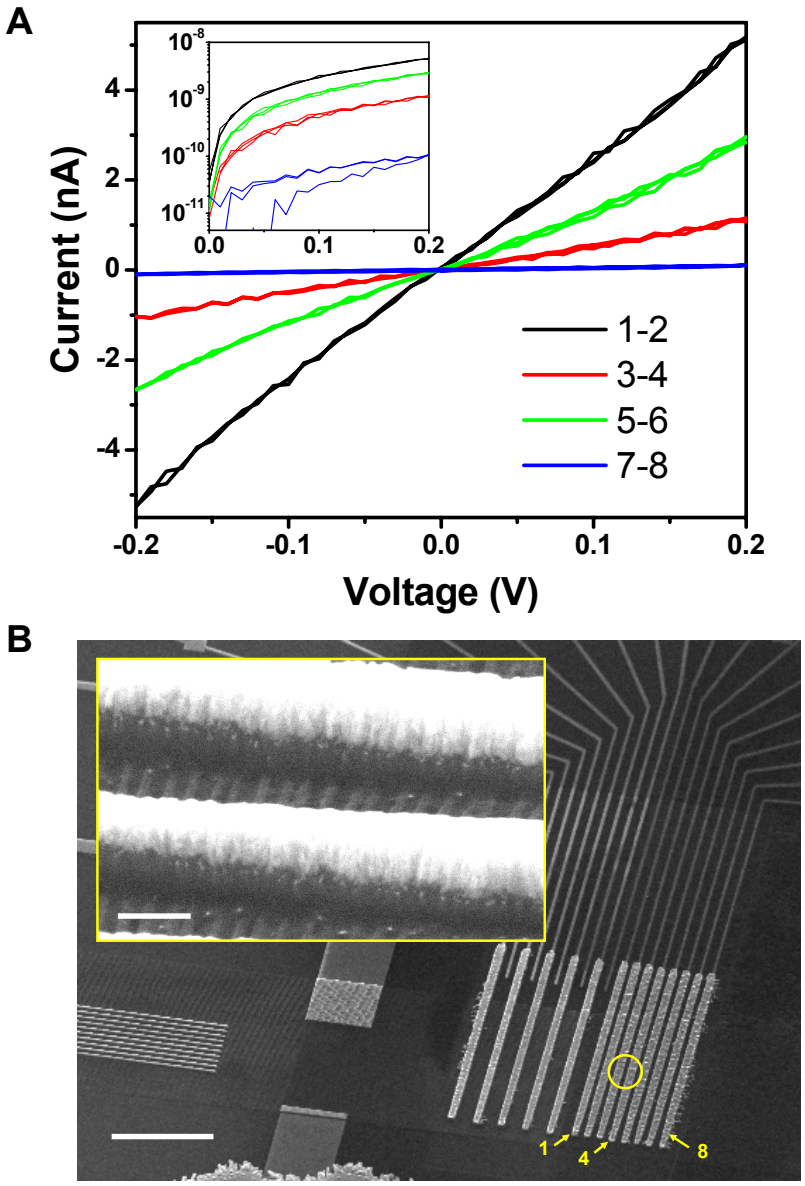

Figure 4-11. Diagnostic Ti etching between electron-beam lithography (EBL)-defined Pt microwires. A. Ti electrode cross-conductance after separation. The numbers in the legend correspond to cross-conductance measurements between the 90-nm-spaced EBL-defined microwires numbered (sequentially from 1 to 8) in panel B. The cross-conductance values after separation are 0.5 nS (blue trace, corresponding to microwires 7–8), 5 nS (red trace, microwires 3–4), 15 nS (green trace, microwires 5–6), and 25 nS (black trace, microwires 1–2). **B.** SEM images of the diagnostic memory circuit. The background shows the EBL-defined Pt microwires patterned over the memory active region to form a Si NW/Ti microwire crossbar. Scale bar is 2.5 μm. The inset is a high-resolution SEM image of the region between two Pt microwires indicated by the yellow circle. Note the Ti has been cleanly removed, revealing the underlying Si NWs. The scale bar is 100 nm.

To form Ti NWs as the top electrodes from SNAP deposited Pt NWs, the chip was etched (via BCl_3) in intervals of time ranging from five minutes (at the beginning) to 30 seconds (near the end) so that periodic conductance measurements could be made to monitor the etch progress. This significantly increased the total BCl_3 etch time because the chip had to be periodically removed from the vacuum environment of our reactive ion etcher resulting in re-growth of surface TiO_2. The total BCl_3 etch time ranged from 15 to 20 minutes, although a large fraction of that time was undoubtedly spent etching re-grown TiO_2 at the beginning of each BCl_3 etch iteration. As will be discussed below, this unavoidably* long etch time can lead to fidelity problems in transferring the Pt NW pattern to the underlying Ti film.

The Ti etching step described above proved to be one of the most challenging aspects of memory fabrication and required the simultaneous optimization of a number of correlated factors. This included the BCl_3 etch recipe described above, the depth of the SOG recess defining the memory active region, and the epoxy used to bond the Pt NW array to the Ti/SiO_2 film. This epoxy fills in the SOG recess, thus separating the Ti/SiO_2 film from the Pt NWs by a relatively thick organic spacer. If the epoxy is too thick significant undercutting can occur. This leads to blurring of the Ti NW pattern and wandering of individual Pt NWs on top of a sea of shifting epoxy. Frequently the Pt NWs would wander so much they would short into each other (Figure 4-12), resulting in Ti NW top electrodes that could not be physically separated (more on this below). This problem was exacerbated with the relatively long BCl_3 etch times required to define the Ti NWs.

* In principle, the etch time could be reduced considerably by monitoring the conductance in-situ with the BCl_3 etch so the time-consuming TiO_2-removal step would only need to be done once. Obviously, our RIE system did not have this feature.

The epoxy thickness over the Ti film was reduced by decreasing the recess of the SOG window defining the memory active region. This was accomplished by globally thinning the SOG film beforehand. Trial and error in conjunction with atomic force microscopy (AFM) measurements of the SOG recess and surrounding region after curing the spin-coated epoxy (without the deposited Pt NWs) determined the optimal SOG

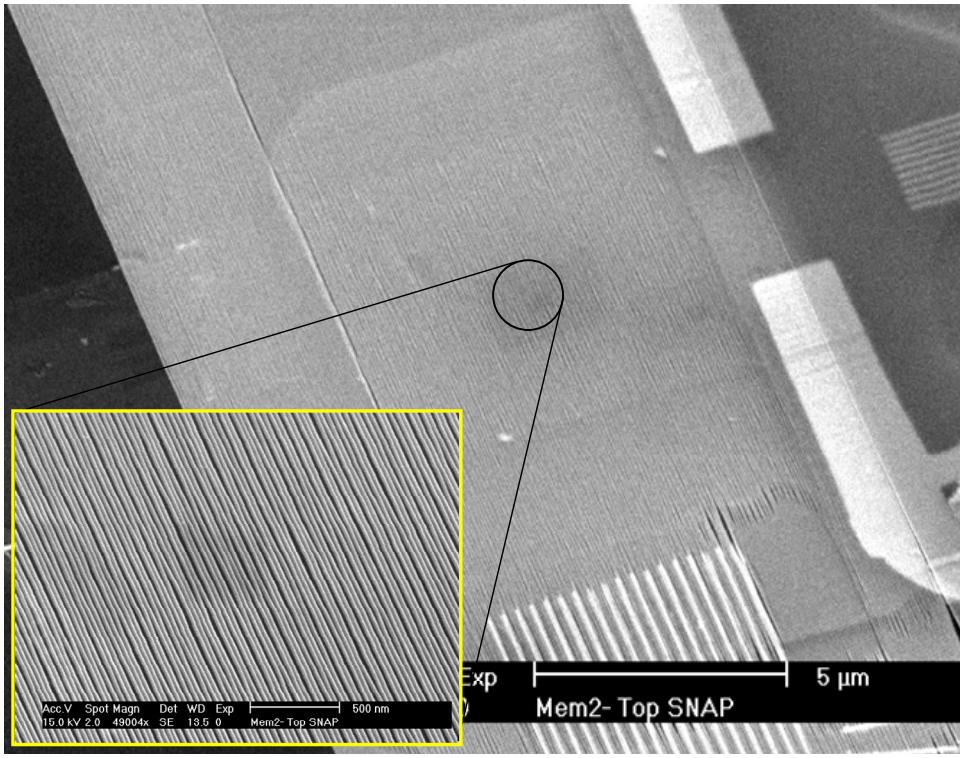

Figure 4-12. SEM image of a crossbar memory circuit before optimization of the Ti NW fabrication parameters. This image shows wandering of individual Pt NWs due to shifting epoxy from the BCl_3 etch used to define the Ti NW array. The inset shows a zoomed-in view from the center of the memory crossbar region. The scale bar in the inset is 500 nm.

thickness to be about 50 nm. Thinning the SOG further required reducing the thickness (65 nm) of the EBL-defined wires so they did not protrude from the SOG + SiO_2 film (keeping the thickness of SiO_2 deposited over the Ti film to be constant at 15 nm[*]). However, this led to problems in making reliable contact to the Si NWs, since the

[*] Increasing the SiO_2 thickness beyond 15 nm adversely affected the etch fidelity.

deposited metal would be more prone to becoming discontinuous at the ends of the Si NWs where there is a step of 33 nm (the starting SOI thickness) (Figure 4-9.B). It should be noted, however, that more advanced metal deposition systems capable of depositing metal conformally would eliminate this constraint.

While reducing the epoxy thickness over the Ti film was necessary to achieve high-fidelity pattern transfer of the Pt NW mask, it was not sufficient. This required improving the epoxy recipe to make it more resistant to undercutting without making it overly difficult to etch using O_2 or BCl_3. (A O_2 etch of 5 mTorr at 40 W always preceded the initial BCl_3 etch to remove epoxy from between the SNAP-fabricated Pt NWs.) After some trial and error, the optimal epoxy recipe was determined to be a modified version of Allied High Tech (Rancho Dominguez, CA) Epoxy Bond 110. (5 drops part A, 1 drop part B, 2 drops of dibutyl phthalate, and diluted with 10 ml of anhydrous tetrahydrofuran. The dibutyl phthalate is a plasticizer that makes the epoxy easier to etch from between Pt NWs.)

4.6.3 Memory testing

The memory circuit was tested using a Probe 2000 (San Jose, CA) custom-built probe card (Appendix 4.2) and a Keithley 707A switching matrix in conjunction with a Keithley 7174A low-current matrix card for off-chip demultiplexing. Individual ebits (containing 4–16 crossbar junctions, but most often containing nine crossbar junctions) were electrically addressed within the 2-D cross-point array by the intersection of 2–4 sequential Si NW bottom electrodes and 2–4 sequential Ti NW top electrodes. Individual

molecular junctions were set to their low resistance, or ‘1’ state, through the application of a positive 1.5–2.3 V pulse (voltages are referenced to the bottom Si NW electrode) of 0.2-second duration. A junction was set to its ‘0’ or high resistance state through application of a −1.5 V pulse, also of 0.2-second duration. To avoid switching an entire column or row of bits, the switching voltage was split between the two electrodes defining the ebit. Thus, to write a ‘1’ with +2 V, a single Si NW electrode is charged to +1 V, while a single Ti NW electrode is set to −1 V, and only where they cross does the junction receive the full +2 V switching voltage. Half-selected bits, that is, bits receiving only half the switching voltage, were never observed to switch. Individual ebits were read by applying a small, non-perturbing +0.2 V bias to the bottom Si NW electrode and grounding the top Ti NW electrode through a Stanford Research Systems SR-570 current pre-amplifier. Bits not being read were held at ground to reduce parasitic current pathways through the crossbar array. Note that all the electrical writing and reading operations described in this work were done sequentially.

Configuring the memory circuit for information storage proceeded as follows. Initially, all ebits were read with +0.2 V to document their baseline current. The value of this baseline current varied from being greater than the current through the junction when set to its low-resistance or ‘1’ state to being less than the current through the junction when set to its high-resistance or ‘0’ state. However, after a (good) bit had been switched though the application of ± 1.5 V, it performed reliably (*i.e.*, on current > off current) until it no longer exhibited switching behavior. After the baseline current was read, all ebits were switched to their ‘1’ state, read out, then set to their ‘0’ state and again read out (Figure 4-13 shows raw data). Good ebits were identified as those with 1/0 current

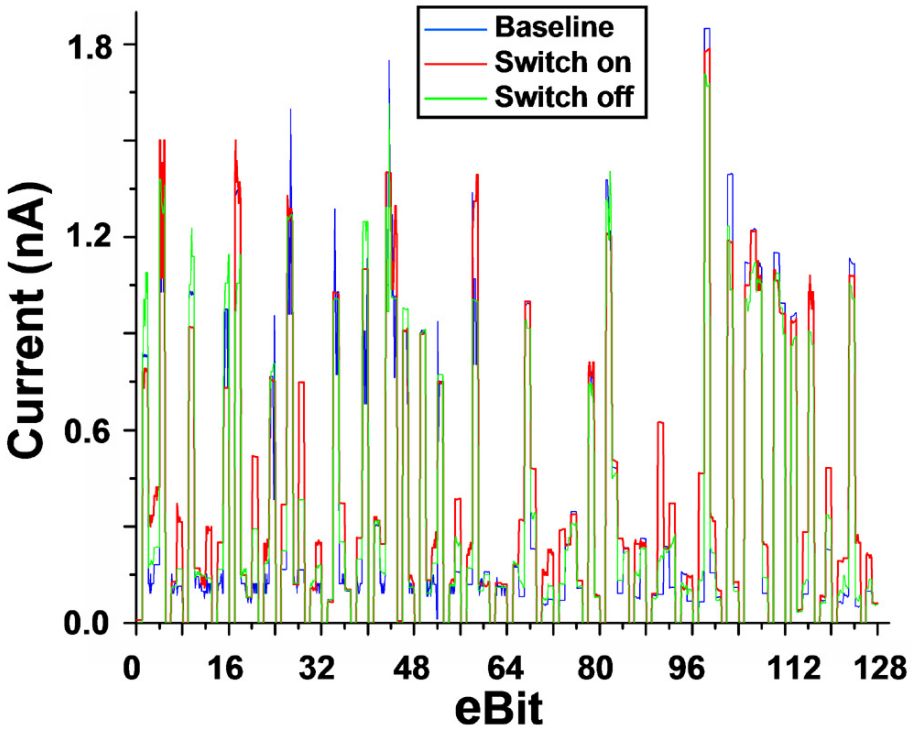

Figure 4-13. Raw switching data from a molecular electronic crossbar memory circuit. The raw data in this figure was used to generate the 1/0 plot and defect matrix shown in Figure 4-6.

ratios roughly greater than or equal to 1.5. Bad ebits fell into a few classes, with the two most common groups being ebits that were either poor switches with little or no switching response or open circuits. In both cases, the 1/0 ratio was unity. Adjacent Ti top electrodes that were shorted together were identified when the ebits addressed by those electrodes were not independently addressable. This is evidenced by an 8-bit periodicity in the response of bits sharing a single Si NW bottom electrode and the shorted Ti top electrodes. This can be seen from the bit matrix in Figure 4-6.B where the shorting of top electrodes T2 and T3 results in nearly equivalent responses from bits 13 & 21 and bits 15 & 23. A more-severe case of top Ti NW shorting is shown in Figure 4-14, which corresponds to the memory circuit shown in Figure 4-12. Even though this type of defect is not completely fatal (*i.e.*, two rows of ebits could still be utilized as a single row

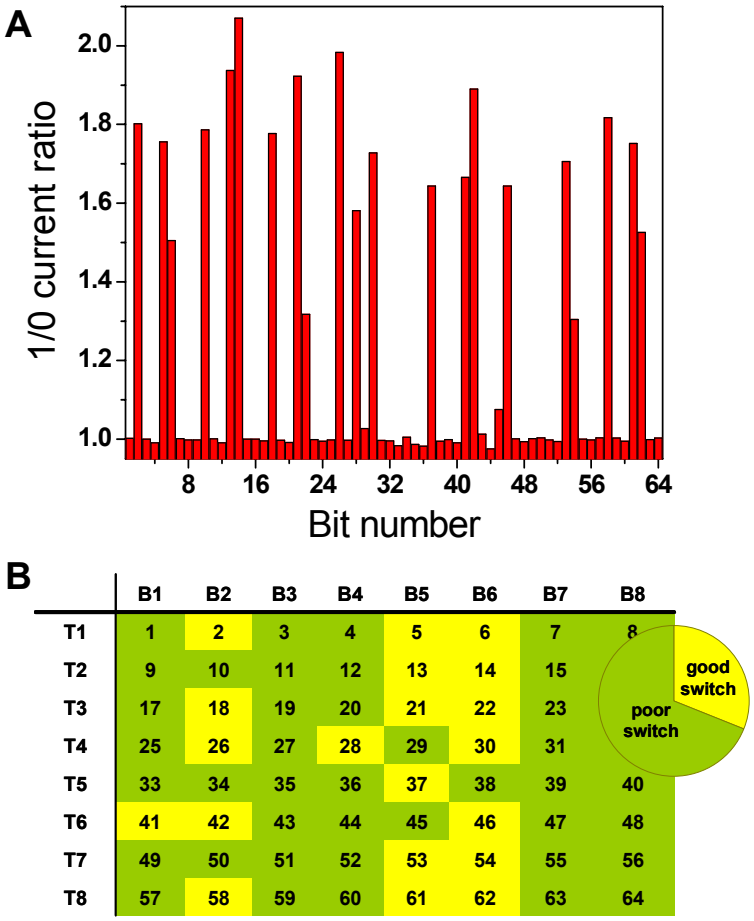

Figure 4-14. Data from a memory circuit with extensive Ti NW top electrode shorting. **A.** 1/0 current ratio measurements from 64 bits of the memory circuit shown in Figure 4-12. **B.** Defect map of the good and defective ebits with a pie chart showing the testing statistics. Good ebits were defined as ebits with 1/0 ratios greater than 1.2 (31% of the tested bits). Note that most of the good ebits (yellow) are clustered together within columns (Si NW bottom electrodes), indicating severe Ti NW (rows) shorting.

of twice-as-large ebits), we did not use ebits associated with shorted top electrode defects.

Once the good ebits were identified, they were used to store and read out small strings of information written in standard ASCII code. The maximum number of ebits that could be tested was 180, but our electronics were configured to test 128 ebits (less than 1 percent of the actual crossbar). Based on results from similarly fabricated memory

circuits, we believe this small subset of measured bits is representative and sufficient to demonstrate the key concepts of this memory.

To increase the measured current, volatility measurements were carried out with approximately 100 (~30 ebits) junctions in parallel. The junctions were switched to their '1' or low resistance state, as described above, and the current was periodically measured through the parallel combination of all 100 junctions at discrete time points. Note that defective switches stuck in a low conductivity state contribute little signal to the parallel combination while defective switches stuck in a high conductivity state only add a constant offset to the decaying current. There could be an unknown number of defective switches (and hence junctions) stuck in their '1' state; however, the current through a parallel combination of functional and defective junctions will decay with the same time constant as that of the functional junctions as long as the number of defective junctions is not too large. We occasionally observed parallel combinations with a large fraction of defective junctions. These were identified by an approximately constant measured current as a function of time. Data from these parallel combinations were not used.

If a defective junction is shorted (*i.e.*, the Ti top electrode is shorted to the bottom Si electrode through direct metal contact), the current through the junction would be orders of magnitude higher than expected and readily identified. We did not observe such junctions in the memory circuits described above.

4.7 Limitations of the SNAP process for crossbar circuits

The nanofabrication methods described above for creating the 160,000-bit crossbar memory circuit can be significantly extended in terms of both memory size and bit density. For [2]rotaxane-based molecular electronic memory circuits, proper choice of electrode materials within the crossbar has proven to be very important for successful memory operation[61]; that is, having Si bottom electrodes and metallic top electrodes with a thin Ti layer to protect the underlying [2]rotaxane monolayer was key. Arrays of SNAP-fabricated Pt NWs only serve as stencils for forming the crossbar electrodes. To be used in a crossbar memory, the SNAP NW pattern must be transferred to Si or Ti NWs for the bottom and top electrodes, respectively. Thus, it is not just the SNAP process, but the ability to translate the initially deposited SNAP NWs to form other NWs that ultimately limits the size and density of the circuitry that can be fabricated.

Figure 4-15 (left micrograph) shows an array of 7-nm-wide, 15-nm-tall single crystal Si NWs patterned at 13-nm pitch. This array could be used to produce to a crossbar molecular memory circuit at about six times the density of this work (~ 6×10^{11} bits cm^{-2}). While this array may not represent the density limit of what could be achieved, densities in excess of 1×10^{12} cm^{-2} may difficult to obtain using these patterning methods and conventional nanofabrication tools. Similarly, the 160,000-bit crossbar described herein can be extended in terms of the total number of bits by using larger-element SNAP NW arrays. Figure 4-15 (right two micrographs) shows SEM images of an array of 1400 Si NWs formed using the SNAP method. An array this size makes possible

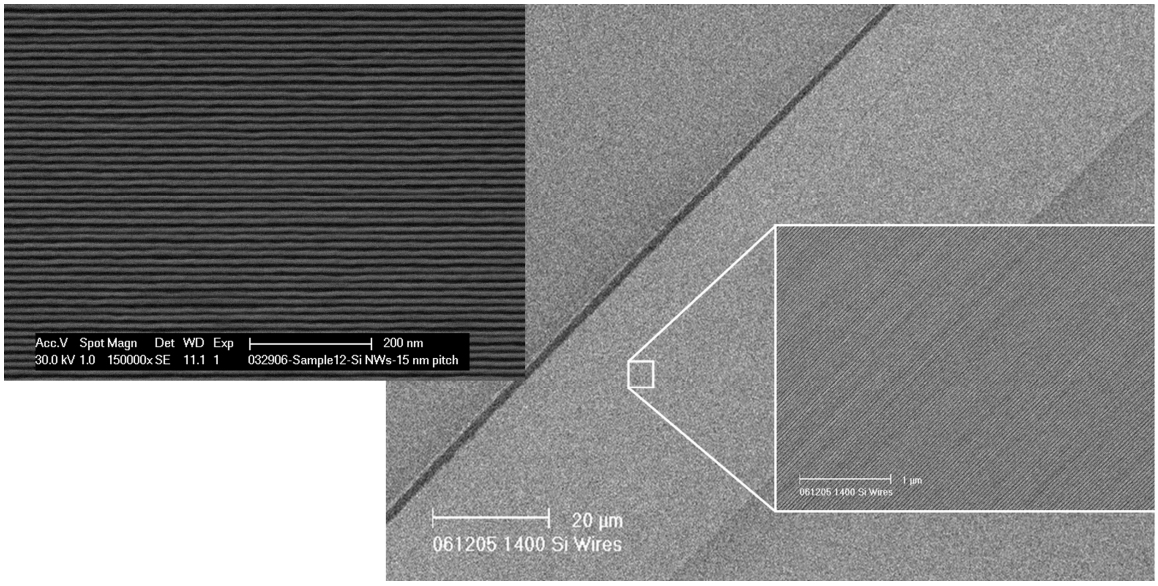

Figure 4-15. Next-generation crossbar molecular memory circuits using SNAP patterning. (left) An array of 7-nm-wide Si NWs patterned at 13-nm pitch could produce a crossbar molecular memory circuit with six times the bit density of this work. **(right)** An array of 1400 Si NWs patterned at 33-nm pitch could provide enough nanowires to produce an approximately two-million-bit crossbar molecular memory circuit. The inset shows an expanded view of the array, which is virtually free of defective nanowires.

the construction of an approximately two-million-bit crossbar molecular memory circuit and it is certainly possible to further expand this concept to substantially larger structures.

From a manufacturing perspective, a significant limitation of the SNAP process is that each NW array must be fabricated serially using a labor-intensive process (despite SNAP being a parallel patterning method in that all NWs within an array are created simultaneously). For instance, in a single day a worker can usually fabricate not more than 10–20 arrays of Si NWs. However, a recent collaboration with Stan Williams' group at Hewlett Packard labs (Palo Alto, CA) has demonstrated that nanoimprinting can be used to replicate SNAP NWs and to form crossbar structures[47]. This indicates that high-

throughput parallel fabrication methods can be developed, even at the near molecular-densities described in this work.

4.8 Concluding remarks

Many challenges remain to be addressed before the type of crossbar molecular memory described here can be practically implemented. For example, areas of future interest include finding faster and more-robust molecular switches, addressing nanofabrication challenges associated with improving the fidelity of these tools and procedures, and meeting engineering challenges such as those involved with combining demultiplexing architectures, such as those described in Chapter 3, with crossbar circuits[69]. Nevertheless, this circuit stands as a new benchmark for nanoelectronic device integration and provides evidence that at least some of the most challenging scientific issues associated with integrating nanowires, molecular materials, and defect-tolerant circuit architectures at extreme dimensions are solvable. The circuits described in this work represent significant advances in sub-lithographic patterning, large-scale assembly of nanoscale electronic devices, and the integration of molecular and solid state materials. Furthermore, recently published nanoimprinting results imply that methods for the high-throughput manufacturing of these types of circuits are possible[46-48].

4.9 References

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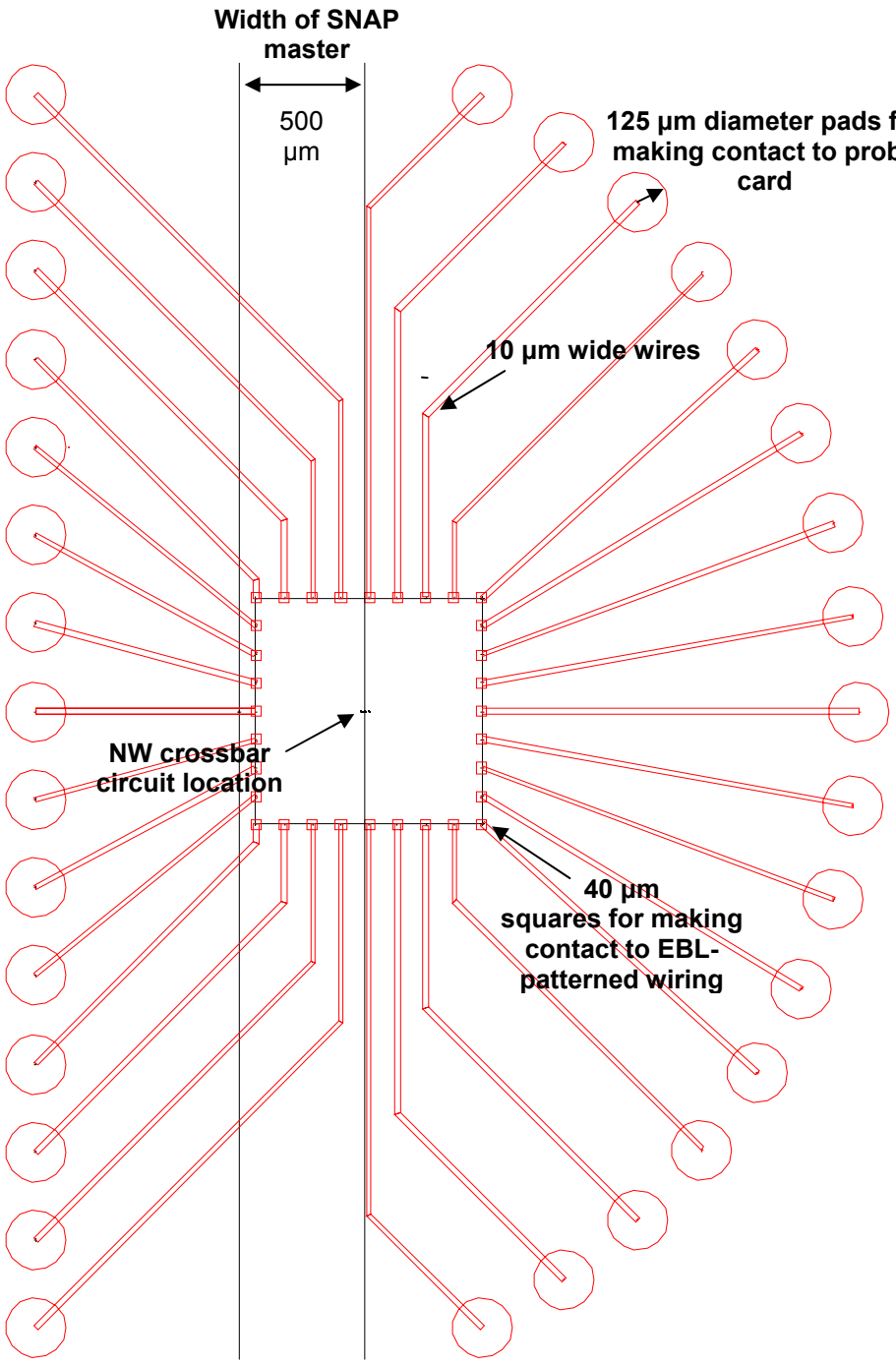
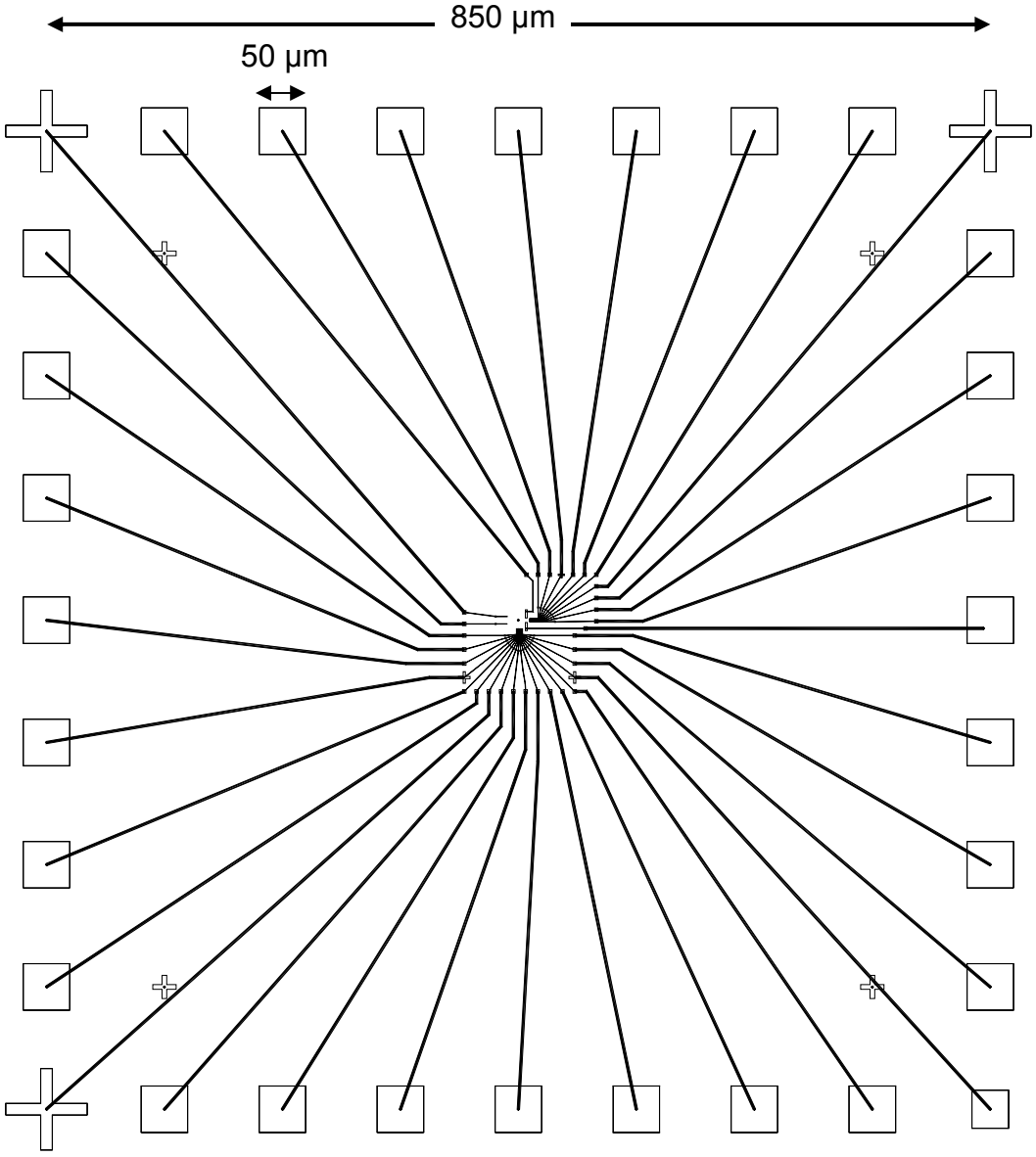
Appendix 4.1 Details of lithographically-patterned structures



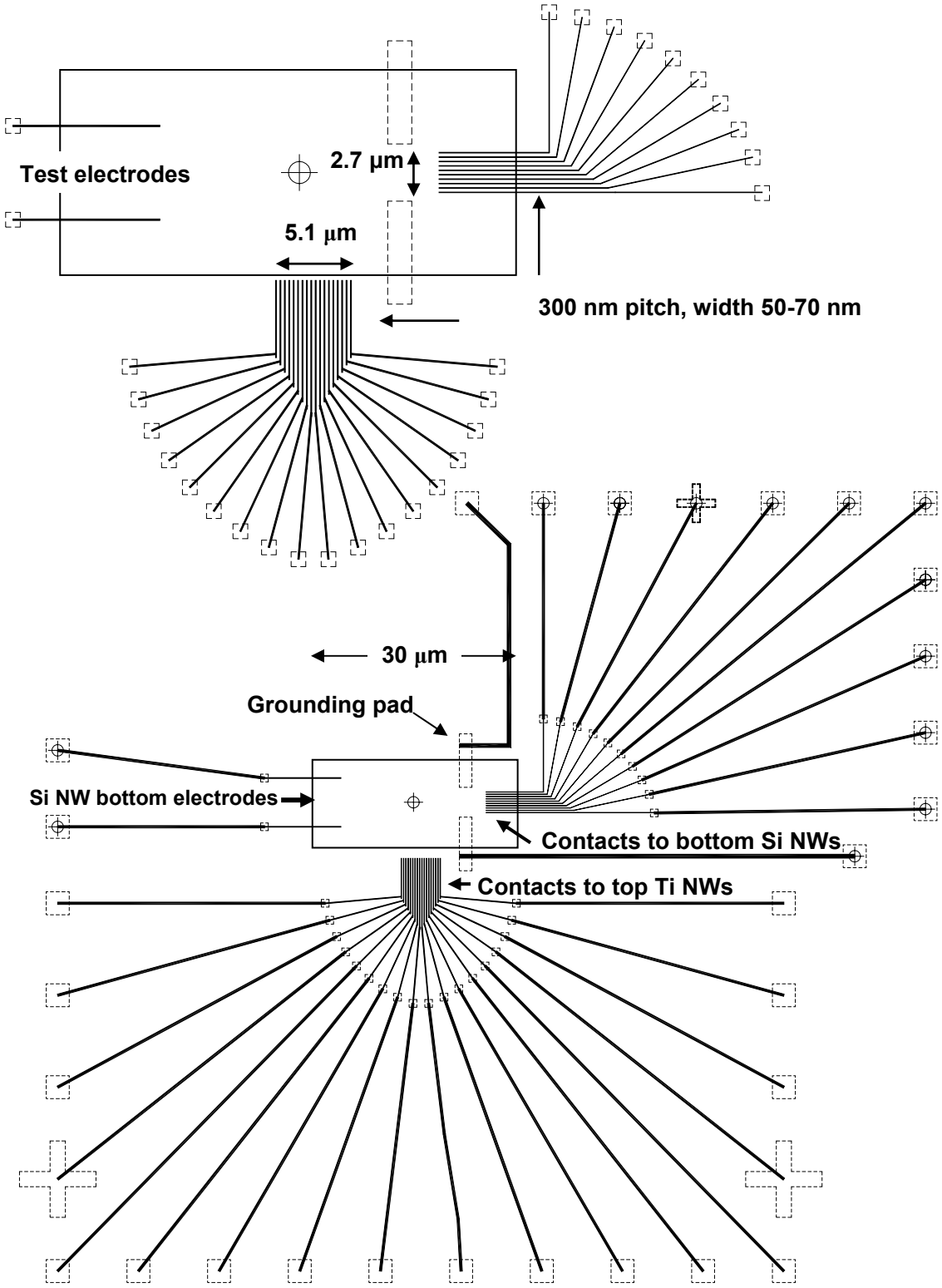
Optical lithography patterned structure. The coordinates for the pads are on the next page. A printed photomask (Output City, Eoway CA) was used to expose the pattern in AZ 5214 (Clariant). AZ 400K was used for development and metal lift-off was in acetone.

Coordinates for the optical mask pattern on previous page (1 unit = 1 micrometer) with the origin at the lower left pad.

PAD #	*X COORDINATE*	*Y COORDINATE*
1	0.0000	0.0000
2	0.0000	350.0000
3	0.0000	700.0000
4	0.0000	1050.0000
5	0.0000	1400.0000
6	0.0000	1750.0000
7	0.0000	2100.0000
8	0.0000	2450.0000
9	0.0000	2800.0000
10	0.0000	3150.0000
11	0.0000	3500.0000
12	0.0000	3850.0000
13	0.0000	4200.0000
14	0.0000	4550.0000
15	0.0000	4900.0000
16	1778.0000	4900.0000
17	2101.6561	4705.6744
18	2395.6589	4468.8663
19	2654.4711	4194.0355
20	2873.2185	3886.3582
21	3047.7811	3551.6291
22	3174.8715	3196.1523
23	3252.0959	2826.6227
24	3278.0000	2450.0000
25	3252.0959	2073.3773
26	3174.8715	1703.8477
27	3047.7811	1348.3709
28	2873.2185	1013.6418
29	2654.4711	705.9645
30	2395.6589	431.1337
31	2101.6561	194.3256
32	1778.0000	0.0000

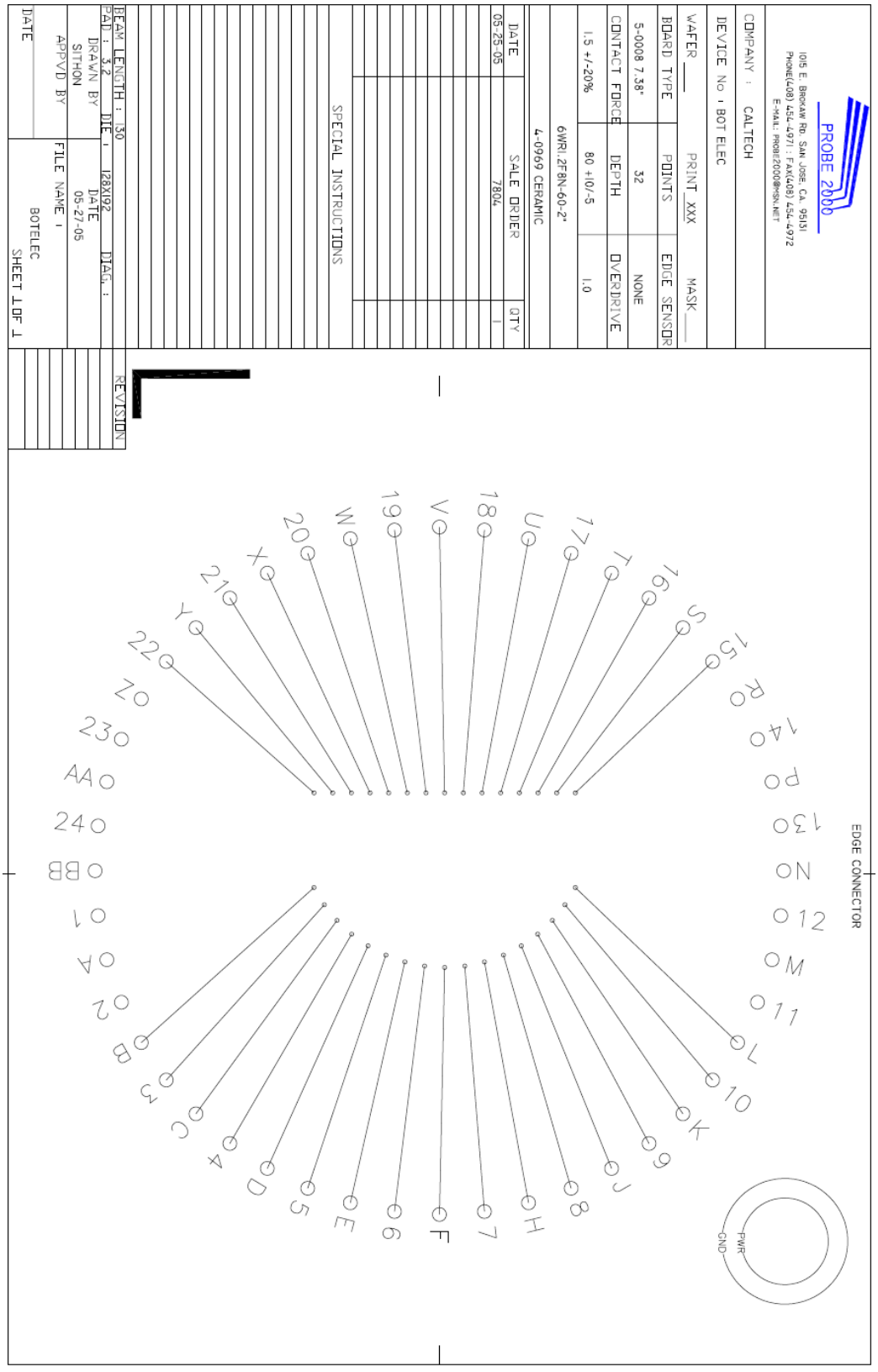


Outermost electron-beam lithography written structures. The large 50-μm pads and crosses at the periphery make contact to optical-lithography-defined pads that in turn fan-out to large circular pads (125 μm diameter) for making contact to a custom-built probe card. All electron-beam lithography was done using an FEI XL-30 SEM with the Nanometer Pattern Generation System (NPGS) version 6.0 (J.C. Nabity Systems) to expose regions of 3% polymethyl-methacrylate (PMMA) over 2.25% MMA. Pattern development was done with 1:3 methyl isobutyl ketone to isopropyl alcohol. Metal depositions were done using an electron-beam evaporator (Semicore Corp, CHA-Mark 40; Freemont, CA), and lift-off was in acetone.



Intermediate-to-smallest EBL-patterned structures.

Appendix 4.2 Memory probe card specifications



Appendix 4.3 NI LabWindows /CVI code used for memory reading/writing operations

---

Note that much of the code below has been commented out (/*…*/). I nonetheless left those portions intact in its original location within the code. This code was written primarily by Dr. Yi Luo for use with a Keithley 707A switching matrix, National Instruments (NI) DAQ PC card (v. 4.8), and a Stanford Research Systems SR-570 current pre-amplifier.

```
#include <gpib.h>
//#include <windows.h>
#include <utility.h>
//#include "decl-32.h"
#include <stdio.h>
#include <string.h>
#include <userint.h>
#include <dataacq.h>
#include <ansi_c.h>
#include "MUX_AC.h"

static int daq, daq1;
FILE *fp_out;
int Device1;
int cross_point[9][9],set_bit[9][9];
int num_read, all_switch,all_control=-1, ramp, ramp_num=20;
double time_write, time_read, volt_write_on,volt_write_off, volt_read, volt_hold, threshold_high,threshold_low;
double adch0,adch1, volt_ramp0, volt_ramp1, ramp_rate;
const char tmp_file[10]="tmp.dat";

void main(){
        int i;
        Device1=ibdev(0,18,0,10,1,0);                                   /* initiate 707A  */
        ibwrt(Device1,"REMOTE",6);                                              /* enable remote mode   */
        ibwrt(Device1,"E0X",3);                                                 /* Point to present relays  */

        daq = LoadPanel (0, "MUX_AC.uir", MUX);
        DisplayPanel (daq);
        i=AI_Clear (1);
        RunUserInterface ();
}
int select_ind (int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2)
        {
        daq1 = LoadPanel (1, "MUX_AC.uir", MUX1);
        DisplayPanel (daq1);
        return 1;
        }
int close_selection(int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2)
        {
        int i,m;
        i=HidePanel(daq1);
        return 0;
        }
int switch_control(int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2)
        {
                        int m;
                        if(all_control==-1){
                                m=SetCtrlAttribute(daq,MUX_ALL_SWITCHES, ATTR_DIMMED, 0);
                        }
                        else{
                                m=SetCtrlAttribute(daq,MUX_ALL_SWITCHES, ATTR_DIMMED, 1);
                        }
                        all_control=all_control*(-1);
                        return 1;
        }
int configure_ind (int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2)
        {
        int i,j,k,m,i_ramp;
        char c[5],d[6];
        if (all_control!=1){
        m = GetCtrlVal (daq, MUX_Switch1_1, &cross_point[1][1]);
        m = GetCtrlVal (daq, MUX_Switch1_2, &cross_point[1][2]);
        m = GetCtrlVal (daq, MUX_Switch1_3, &cross_point[1][3]);
```

```
m = GetCtrlVal (daq, MUX_Switch1_4, &cross_point[1][4]);
m = GetCtrlVal (daq, MUX_Switch1_5, &cross_point[1][5]);
m = GetCtrlVal (daq, MUX_Switch1_6, &cross_point[1][6]);
m = GetCtrlVal (daq, MUX_Switch1_7, &cross_point[1][7]);
m = GetCtrlVal (daq, MUX_Switch1_8, &cross_point[1][8]);
m = GetCtrlVal (daq, MUX_Switch2_1, &cross_point[2][1]);
m = GetCtrlVal (daq, MUX_Switch2_2, &cross_point[2][2]);
m = GetCtrlVal (daq, MUX_Switch2_3, &cross_point[2][3]);
m = GetCtrlVal (daq, MUX_Switch2_4, &cross_point[2][4]);
m = GetCtrlVal (daq, MUX_Switch2_5, &cross_point[2][5]);
m = GetCtrlVal (daq, MUX_Switch2_6, &cross_point[2][6]);
m = GetCtrlVal (daq, MUX_Switch2_7, &cross_point[2][7]);
m = GetCtrlVal (daq, MUX_Switch2_8, &cross_point[2][8]);
m = GetCtrlVal (daq, MUX_Switch3_1, &cross_point[3][1]);
m = GetCtrlVal (daq, MUX_Switch3_2, &cross_point[3][2]);
m = GetCtrlVal (daq, MUX_Switch3_3, &cross_point[3][3]);
m = GetCtrlVal (daq, MUX_Switch3_4, &cross_point[3][4]);
m = GetCtrlVal (daq, MUX_Switch3_5, &cross_point[3][5]);
m = GetCtrlVal (daq, MUX_Switch3_6, &cross_point[3][6]);
m = GetCtrlVal (daq, MUX_Switch3_7, &cross_point[3][7]);
m = GetCtrlVal (daq, MUX_Switch3_8, &cross_point[3][8]);
m = GetCtrlVal (daq, MUX_Switch4_1, &cross_point[4][1]);
m = GetCtrlVal (daq, MUX_Switch4_2, &cross_point[4][2]);
m = GetCtrlVal (daq, MUX_Switch4_3, &cross_point[4][3]);
m = GetCtrlVal (daq, MUX_Switch4_4, &cross_point[4][4]);
m = GetCtrlVal (daq, MUX_Switch4_5, &cross_point[4][5]);
m = GetCtrlVal (daq, MUX_Switch4_6, &cross_point[4][6]);
m = GetCtrlVal (daq, MUX_Switch4_7, &cross_point[4][7]);
m = GetCtrlVal (daq, MUX_Switch4_8, &cross_point[4][8]);
m = GetCtrlVal (daq, MUX_Switch5_1, &cross_point[5][1]);
m = GetCtrlVal (daq, MUX_Switch5_2, &cross_point[5][2]);
m = GetCtrlVal (daq, MUX_Switch5_3, &cross_point[5][3]);
m = GetCtrlVal (daq, MUX_Switch5_4, &cross_point[5][4]);
m = GetCtrlVal (daq, MUX_Switch5_5, &cross_point[5][5]);
m = GetCtrlVal (daq, MUX_Switch5_6, &cross_point[5][6]);
m = GetCtrlVal (daq, MUX_Switch5_7, &cross_point[5][7]);
m = GetCtrlVal (daq, MUX_Switch5_8, &cross_point[5][8]);
m = GetCtrlVal (daq, MUX_Switch6_1, &cross_point[6][1]);
m = GetCtrlVal (daq, MUX_Switch6_2, &cross_point[6][2]);
m = GetCtrlVal (daq, MUX_Switch6_3, &cross_point[6][3]);
m = GetCtrlVal (daq, MUX_Switch6_4, &cross_point[6][4]);
m = GetCtrlVal (daq, MUX_Switch6_5, &cross_point[6][5]);
m = GetCtrlVal (daq, MUX_Switch6_6, &cross_point[6][6]);
m = GetCtrlVal (daq, MUX_Switch6_7, &cross_point[6][7]);
m = GetCtrlVal (daq, MUX_Switch6_8, &cross_point[6][8]);
m = GetCtrlVal (daq, MUX_Switch7_1, &cross_point[7][1]);
m = GetCtrlVal (daq, MUX_Switch7_2, &cross_point[7][2]);
m = GetCtrlVal (daq, MUX_Switch7_3, &cross_point[7][3]);
m = GetCtrlVal (daq, MUX_Switch7_4, &cross_point[7][4]);
m = GetCtrlVal (daq, MUX_Switch7_5, &cross_point[7][5]);
m = GetCtrlVal (daq, MUX_Switch7_6, &cross_point[7][6]);
m = GetCtrlVal (daq, MUX_Switch7_7, &cross_point[7][7]);
m = GetCtrlVal (daq, MUX_Switch7_8, &cross_point[7][8]);
m = GetCtrlVal (daq, MUX_Switch8_1, &cross_point[8][1]);
m = GetCtrlVal (daq, MUX_Switch8_2, &cross_point[8][2]);
m = GetCtrlVal (daq, MUX_Switch8_3, &cross_point[8][3]);
m = GetCtrlVal (daq, MUX_Switch8_4, &cross_point[8][4]);
m = GetCtrlVal (daq, MUX_Switch8_5, &cross_point[8][5]);
m = GetCtrlVal (daq, MUX_Switch8_6, &cross_point[8][6]);
m = GetCtrlVal (daq, MUX_Switch8_7, &cross_point[8][7]);
m = GetCtrlVal (daq, MUX_Switch8_8, &cross_point[8][8]);
}
else{
        m = GetCtrlVal (daq, MUX_ALL_SWITCHES, &all_switch);
        for(i=1;i<=8;i++){
                for(j=1;j<=8;j++){
                cross_point[i][j]=all_switch;
                }
        }
}
m = GetCtrlVal (daq1, MUX1_Switch1_1, &set_bit[1][1]);
m = GetCtrlVal (daq1, MUX1_Switch1_2, &set_bit[1][2]);
m = GetCtrlVal (daq1, MUX1_Switch1_3, &set_bit[1][3]);
m = GetCtrlVal (daq1, MUX1_Switch1_4, &set_bit[1][4]);
m = GetCtrlVal (daq1, MUX1_Switch1_5, &set_bit[1][5]);
m = GetCtrlVal (daq1, MUX1_Switch1_6, &set_bit[1][6]);
m = GetCtrlVal (daq1, MUX1_Switch1_7, &set_bit[1][7]);
m = GetCtrlVal (daq1, MUX1_Switch1_8, &set_bit[1][8]);
m = GetCtrlVal (daq1, MUX1_Switch2_1, &set_bit[2][1]);
m = GetCtrlVal (daq1, MUX1_Switch2_2, &set_bit[2][2]);
m = GetCtrlVal (daq1, MUX1_Switch2_3, &set_bit[2][3]);
m = GetCtrlVal (daq1, MUX1_Switch2_4, &set_bit[2][4]);
m = GetCtrlVal (daq1, MUX1_Switch2_5, &set_bit[2][5]);
m = GetCtrlVal (daq1, MUX1_Switch2_6, &set_bit[2][6]);
m = GetCtrlVal (daq1, MUX1_Switch2_7, &set_bit[2][7]);
m = GetCtrlVal (daq1, MUX1_Switch2_8, &set_bit[2][8]);
m = GetCtrlVal (daq1, MUX1_Switch3_1, &set_bit[3][1]);
m = GetCtrlVal (daq1, MUX1_Switch3_2, &set_bit[3][2]);
m = GetCtrlVal (daq1, MUX1_Switch3_3, &set_bit[3][3]);
m = GetCtrlVal (daq1, MUX1_Switch3_4, &set_bit[3][4]);
m = GetCtrlVal (daq1, MUX1_Switch3_5, &set_bit[3][5]);
m = GetCtrlVal (daq1, MUX1_Switch3_6, &set_bit[3][6]);
m = GetCtrlVal (daq1, MUX1_Switch3_7, &set_bit[3][7]);
```

```
m = GetCtrlVal (daq1, MUX1_Switch3_8, &set_bit[3][8]);
m = GetCtrlVal (daq1, MUX1_Switch4_1, &set_bit[4][1]);
m = GetCtrlVal (daq1, MUX1_Switch4_2, &set_bit[4][2]);
m = GetCtrlVal (daq1, MUX1_Switch4_3, &set_bit[4][3]);
m = GetCtrlVal (daq1, MUX1_Switch4_4, &set_bit[4][4]);
m = GetCtrlVal (daq1, MUX1_Switch4_5, &set_bit[4][5]);
m = GetCtrlVal (daq1, MUX1_Switch4_6, &set_bit[4][6]);
m = GetCtrlVal (daq1, MUX1_Switch4_7, &set_bit[4][7]);
m = GetCtrlVal (daq1, MUX1_Switch4_8, &set_bit[4][8]);
m = GetCtrlVal (daq1, MUX1_Switch5_1, &set_bit[5][1]);
m = GetCtrlVal (daq1, MUX1_Switch5_2, &set_bit[5][2]);
m = GetCtrlVal (daq1, MUX1_Switch5_3, &set_bit[5][3]);
m = GetCtrlVal (daq1, MUX1_Switch5_4, &set_bit[5][4]);
m = GetCtrlVal (daq1, MUX1_Switch5_5, &set_bit[5][5]);
m = GetCtrlVal (daq1, MUX1_Switch5_6, &set_bit[5][6]);
m = GetCtrlVal (daq1, MUX1_Switch5_7, &set_bit[5][7]);
m = GetCtrlVal (daq1, MUX1_Switch5_8, &set_bit[5][8]);
m = GetCtrlVal (daq1, MUX1_Switch6_1, &set_bit[6][1]);
m = GetCtrlVal (daq1, MUX1_Switch6_2, &set_bit[6][2]);
m = GetCtrlVal (daq1, MUX1_Switch6_3, &set_bit[6][3]);
m = GetCtrlVal (daq1, MUX1_Switch6_4, &set_bit[6][4]);
m = GetCtrlVal (daq1, MUX1_Switch6_5, &set_bit[6][5]);
m = GetCtrlVal (daq1, MUX1_Switch6_6, &set_bit[6][6]);
m = GetCtrlVal (daq1, MUX1_Switch6_7, &set_bit[6][7]);
m = GetCtrlVal (daq1, MUX1_Switch6_8, &set_bit[6][8]);
m = GetCtrlVal (daq1, MUX1_Switch7_1, &set_bit[7][1]);
m = GetCtrlVal (daq1, MUX1_Switch7_2, &set_bit[7][2]);
m = GetCtrlVal (daq1, MUX1_Switch7_3, &set_bit[7][3]);
m = GetCtrlVal (daq1, MUX1_Switch7_4, &set_bit[7][4]);
m = GetCtrlVal (daq1, MUX1_Switch7_5, &set_bit[7][5]);
m = GetCtrlVal (daq1, MUX1_Switch7_6, &set_bit[7][6]);
m = GetCtrlVal (daq1, MUX1_Switch7_7, &set_bit[7][7]);
m = GetCtrlVal (daq1, MUX1_Switch7_8, &set_bit[7][8]);
m = GetCtrlVal (daq1, MUX1_Switch8_1, &set_bit[8][1]);
m = GetCtrlVal (daq1, MUX1_Switch8_2, &set_bit[8][2]);
m = GetCtrlVal (daq1, MUX1_Switch8_3, &set_bit[8][3]);
m = GetCtrlVal (daq1, MUX1_Switch8_4, &set_bit[8][4]);
m = GetCtrlVal (daq1, MUX1_Switch8_5, &set_bit[8][5]);
m = GetCtrlVal (daq1, MUX1_Switch8_6, &set_bit[8][6]);
m = GetCtrlVal (daq1, MUX1_Switch8_7, &set_bit[8][7]);
m = GetCtrlVal (daq1, MUX1_Switch8_8, &set_bit[8][8]);
m = GetCtrlVal (daq, MUX_TIME_WRITE, &time_write);
m = GetCtrlVal (daq, MUX_VOLT_WRITE_ON, &volt_write_on);
m = GetCtrlVal (daq, MUX_VOLT_WRITE_OFF, &volt_write_off);
m = GetCtrlVal (daq, MUX_VOLT_HOLD, &volt_hold);
m = GetCtrlVal (daq, MUX_Ramp, &ramp);
m = GetCtrlVal (daq, MUX_Ramp_Rate, &ramp_rate);

/********   starting the loop of configuring   *******/

    /********  test ********/
m=SetCtrlVal(daq,MUX_STOP_SCAN,1);
m=SetCtrlVal(daq,MUX_Config_complete,0);
m=SetCtrlVal(daq,MUX_Memory_Check_Done,0);
ibwrt(Device1,"CA72X",5);                                   /* dummy line */
ibwrt(Device1,"NA72X",5);
for(i=1;i<=8;i++){
        for(j=1;j<=8;j++){
        if (set_bit[i][j]==1){                              /* check if the bit is selected   */
                c[0]='C';
                c[1]='B';
                c[2]=(char)(48+i);
                c[3]='X';
                c[4]='\0';
                ibwrt(Device1,c,4);
                c[0]='N';
                c[1]='A';
                c[2]=(char)(48+i);
                c[3]='X';
                c[4]='\0';
                ibwrt(Device1,c,4);
                if (j<2){
                c[0]='C';
                c[1]='C';
                c[2]=(char)(48+j+8);
                c[3]='X';
                c[4]='\0';
                ibwrt(Device1,c,4);
                c[0]='N';
                c[1]='H';
                c[2]=(char)(48+j+8);
                c[3]='X';
                c[4]='\0';
                ibwrt(Device1,c,4);
                }
                else{
                d[0]='C';
                d[1]='C';
                d[2]='1';                                   /* two-digit  */
                d[3]=(char)(48+j-2);
                d[4]='X';
                d[5]='\0';
                ibwrt(Device1,d,5);
```

```
                                        d[0]='N';
                                        d[1]='H';
                                        d[2]='1';                                                       /* two-digit  */
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        }
                                for(k=1;k<=16;k++){
                                        if((k!=i)&&(k!=j+8)){
                                                if (k<10){
                                                        if (k<=8){
                                                        c[0]='C';
                                                        c[1]='A';           /* apply -1.0 volt to rows from Keithley 5-25-01  */
                                                        c[2]=(char)(48+k);
                                                        c[3]='X';
                                                        c[4]='\0';
                                                        ibwrt(Device1,c,4);
                                                        }
                                                        else{
                                                        c[0]='C';
                                                        c[1]='H';
/*  Ground the columns */
                                                        c[2]=(char)(48+k);
                                                        c[3]='X';
                                                        c[4]='\0';
                                                        ibwrt(Device1,c,4);
                                                        }
                                                }
                                                else{
                                                d[0]='C';
                                                d[1]='H';
                                                d[2]='1';
                                                d[3]=(char)(48+k-10);
                                                d[4]='X';
                                                d[5]='\0';
                                                ibwrt(Device1,d,5);
                                                }
                                        }
                                }
                                /*  set write voltage */
                                Delay(0.1);
                                printf("\a");
                                if(ramp==1){
                                        if(cross_point[i][j]==1){
                                                volt_ramp0=volt_hold;
                                                volt_ramp1=0.0;
                                                for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
/* ramp-up */
                                                        volt_ramp0=volt_ramp0 + (volt_write_on/2-volt_hold)/ramp_num;
                                                        volt_ramp1=volt_ramp1 + (volt_write_on/2)/ramp_num;
                                                        m = AO_VWrite (1, 0, volt_ramp0);
                                                        m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                        Delay(volt_write_on/ramp_num/ramp_rate);
                                                }
                                                Delay(time_write);                                                                      /* hold */
                                                for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
/* ramp-down */
                                                        volt_ramp0=volt_ramp0 - (volt_write_on/2-volt_hold)/ramp_num;
                                                        volt_ramp1=volt_ramp1 - (volt_write_on/2)/ramp_num;
                                                        m = AO_VWrite (1, 0, volt_ramp0);
                                                        m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                        Delay(volt_write_on/ramp_num/ramp_rate);
                                                }
                                                                                                                        }
                                        else{
                                                volt_ramp0=volt_hold;
                                                volt_ramp1=0.0;
                                                for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
/* ramp-up */
                                                        volt_ramp0=volt_ramp0 + (volt_write_off/2-volt_hold)/ramp_num;
                                                        volt_ramp1=volt_ramp1 + (volt_write_off/2)/ramp_num;
                                                        m = AO_VWrite (1, 0, volt_ramp0);
                                                        m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                        Delay(volt_write_off/ramp_num/ramp_rate);
                                                }
                                                Delay(time_write);                                                                      /* hold */
                                                for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
/* ramp-down */
                                                        volt_ramp0=volt_ramp0 - (volt_write_off/2-volt_hold)/ramp_num;
                                                        volt_ramp1=volt_ramp1 - (volt_write_off/2)/ramp_num;
                                                        m = AO_VWrite (1, 0, volt_ramp0);
                                                        m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                        Delay(volt_write_off/ramp_num/ramp_rate);
                                                }
                                        }
                                }   /* with ramp */
                                else{
                                        if(cross_point[i][j]==1){
                                                m = AO_VWrite (1, 0, (volt_write_on/2));
                                                m = AO_VWrite (1, 1, (-volt_write_on/2-0.06225)/0.9938);
                                        }
                                        else{
```

```
                                                m = AO_VWrite (1, 0, (volt_write_off/2));
                                                m = AO_VWrite (1, 1, (-volt_write_off/2-0.06225)/0.9938);
                                        }
                                        Delay(time_write);
                                        m = AO_VWrite (1, 0, volt_hold);
                                        m = AO_VWrite (1, 1, -0.06225/0.9938);
                                }                               /* no ramp */
                        /*****  set holding voltage to the row, and Ground to the column  *****/
                                        c[0]='C';
                                        c[1]='A';
                                        c[2]=(char)(48+i);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        c[0]='N';
                                        c[1]='B';
                                        c[2]=(char)(48+i);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        if (j<2){
                                        c[0]='C';
                                        c[1]='H';
                                        c[2]=(char)(48+j+8);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        c[0]='N';
                                        c[1]='C';
                                        c[2]=(char)(48+j+8);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        }
                                        else{
                                        d[0]='C';
                                        d[1]='H';
                                        d[2]='1';                                                       /* two-digit  */
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        d[0]='N';
                                        d[1]='C';
                                        d[2]='1';                                                       /* two-digit  */
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        }
                                /*ibwrt(Device1,"P0X",3);                       open all relays  5-21-01 */
                        }   /*   finish setting one selected bit  */
                        }   /* j */
                        }
                /* close i loop  */
                m=SetCtrlVal(daq,MUX_Config_complete,1);
                return 1;
                }
int configure (int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2)
                {
                int i,j,k,m,i_ramp;
                char c[5],d[6];
                if (all_control !=1){

                m = GetCtrlVal (daq, MUX_Switch1_1, &cross_point[1][1]);
                m = GetCtrlVal (daq, MUX_Switch1_2, &cross_point[1][2]);
                m = GetCtrlVal (daq, MUX_Switch1_3, &cross_point[1][3]);
                m = GetCtrlVal (daq, MUX_Switch1_4, &cross_point[1][4]);
                m = GetCtrlVal (daq, MUX_Switch1_5, &cross_point[1][5]);
                m = GetCtrlVal (daq, MUX_Switch1_6, &cross_point[1][6]);
                m = GetCtrlVal (daq, MUX_Switch1_7, &cross_point[1][7]);
                m = GetCtrlVal (daq, MUX_Switch1_8, &cross_point[1][8]);
                m = GetCtrlVal (daq, MUX_Switch2_1, &cross_point[2][1]);
                m = GetCtrlVal (daq, MUX_Switch2_2, &cross_point[2][2]);
                m = GetCtrlVal (daq, MUX_Switch2_3, &cross_point[2][3]);
                m = GetCtrlVal (daq, MUX_Switch2_4, &cross_point[2][4]);
                m = GetCtrlVal (daq, MUX_Switch2_5, &cross_point[2][5]);
                m = GetCtrlVal (daq, MUX_Switch2_6, &cross_point[2][6]);
                m = GetCtrlVal (daq, MUX_Switch2_7, &cross_point[2][7]);
                m = GetCtrlVal (daq, MUX_Switch2_8, &cross_point[2][8]);
                m = GetCtrlVal (daq, MUX_Switch3_1, &cross_point[3][1]);
                m = GetCtrlVal (daq, MUX_Switch3_2, &cross_point[3][2]);
                m = GetCtrlVal (daq, MUX_Switch3_3, &cross_point[3][3]);
                m = GetCtrlVal (daq, MUX_Switch3_4, &cross_point[3][4]);
                m = GetCtrlVal (daq, MUX_Switch3_5, &cross_point[3][5]);
                m = GetCtrlVal (daq, MUX_Switch3_6, &cross_point[3][6]);
                m = GetCtrlVal (daq, MUX_Switch3_7, &cross_point[3][7]);
                m = GetCtrlVal (daq, MUX_Switch3_8, &cross_point[3][8]);
                m = GetCtrlVal (daq, MUX_Switch4_1, &cross_point[4][1]);
                m = GetCtrlVal (daq, MUX_Switch4_2, &cross_point[4][2]);
                m = GetCtrlVal (daq, MUX_Switch4_3, &cross_point[4][3]);
                m = GetCtrlVal (daq, MUX_Switch4_4, &cross_point[4][4]);
```

```
		m = GetCtrlVal (daq, MUX_Switch4_5, &cross_point[4][5]);
		m = GetCtrlVal (daq, MUX_Switch4_6, &cross_point[4][6]);
		m = GetCtrlVal (daq, MUX_Switch4_7, &cross_point[4][7]);
		m = GetCtrlVal (daq, MUX_Switch4_8, &cross_point[4][8]);
		m = GetCtrlVal (daq, MUX_Switch5_1, &cross_point[5][1]);
		m = GetCtrlVal (daq, MUX_Switch5_2, &cross_point[5][2]);
		m = GetCtrlVal (daq, MUX_Switch5_3, &cross_point[5][3]);
		m = GetCtrlVal (daq, MUX_Switch5_4, &cross_point[5][4]);
		m = GetCtrlVal (daq, MUX_Switch5_5, &cross_point[5][5]);
		m = GetCtrlVal (daq, MUX_Switch5_6, &cross_point[5][6]);
		m = GetCtrlVal (daq, MUX_Switch5_7, &cross_point[5][7]);
		m = GetCtrlVal (daq, MUX_Switch5_8, &cross_point[5][8]);
		m = GetCtrlVal (daq, MUX_Switch6_1, &cross_point[6][1]);
		m = GetCtrlVal (daq, MUX_Switch6_2, &cross_point[6][2]);
		m = GetCtrlVal (daq, MUX_Switch6_3, &cross_point[6][3]);
		m = GetCtrlVal (daq, MUX_Switch6_4, &cross_point[6][4]);
		m = GetCtrlVal (daq, MUX_Switch6_5, &cross_point[6][5]);
		m = GetCtrlVal (daq, MUX_Switch6_6, &cross_point[6][6]);
		m = GetCtrlVal (daq, MUX_Switch6_7, &cross_point[6][7]);
		m = GetCtrlVal (daq, MUX_Switch6_8, &cross_point[6][8]);
		m = GetCtrlVal (daq, MUX_Switch7_1, &cross_point[7][1]);
		m = GetCtrlVal (daq, MUX_Switch7_2, &cross_point[7][2]);
		m = GetCtrlVal (daq, MUX_Switch7_3, &cross_point[7][3]);
		m = GetCtrlVal (daq, MUX_Switch7_4, &cross_point[7][4]);
		m = GetCtrlVal (daq, MUX_Switch7_5, &cross_point[7][5]);
		m = GetCtrlVal (daq, MUX_Switch7_6, &cross_point[7][6]);
		m = GetCtrlVal (daq, MUX_Switch7_7, &cross_point[7][7]);
		m = GetCtrlVal (daq, MUX_Switch7_8, &cross_point[7][8]);
		m = GetCtrlVal (daq, MUX_Switch8_1, &cross_point[8][1]);
		m = GetCtrlVal (daq, MUX_Switch8_2, &cross_point[8][2]);
		m = GetCtrlVal (daq, MUX_Switch8_3, &cross_point[8][3]);
		m = GetCtrlVal (daq, MUX_Switch8_4, &cross_point[8][4]);
		m = GetCtrlVal (daq, MUX_Switch8_5, &cross_point[8][5]);
		m = GetCtrlVal (daq, MUX_Switch8_6, &cross_point[8][6]);
		m = GetCtrlVal (daq, MUX_Switch8_7, &cross_point[8][7]);
		m = GetCtrlVal (daq, MUX_Switch8_8, &cross_point[8][8]);
		}
		else{
			m = GetCtrlVal (daq, MUX_ALL_SWITCHES, &all_switch);
			for(i=1;i<=8;i++){
				for(j=1;j<=8;j++){
				cross_point[i][j]=all_switch;
				}
			}
		}
		m = GetCtrlVal (daq, MUX_TIME_WRITE, &time_write);
		m = GetCtrlVal (daq, MUX_VOLT_WRITE_ON, &volt_write_on);
		m = GetCtrlVal (daq, MUX_VOLT_WRITE_OFF, &volt_write_off);
		m = GetCtrlVal (daq, MUX_VOLT_HOLD, &volt_hold);
		m = GetCtrlVal (daq, MUX_Ramp, &ramp);
		m = GetCtrlVal (daq, MUX_Ramp_Rate, &ramp_rate);

/********   starting the loop of configuring   *******/

	/********  test ********/
		m=SetCtrlVal(daq,MUX_STOP_SCAN,1);
		m=SetCtrlVal(daq,MUX_Config_complete,0);
		m=SetCtrlVal(daq,MUX_Memory_Check_Done,0);
		ibwrt(Device1,"CA25X",5);                                        /* dummy line */
		ibwrt(Device1,"NA25X",5);
		for(i=1;i<=8;i++){
			for(j=1;j<=8;j++){
			/*		if(cross_point[i][j]==1){                                  2-17-01      */
					c[0]='C';
					c[1]='B';
					c[2]=(char)(48+i);
					c[3]='X';
					c[4]='\0';
					ibwrt(Device1,c,4);
					c[0]='N';
					c[1]='A';
					c[2]=(char)(48+i);
					c[3]='X';
					c[4]='\0';
					ibwrt(Device1,c,4);
					if (j<2){
					c[0]='C';
					c[1]='C';
					c[2]=(char)(48+j+8);
					c[3]='X';
					c[4]='\0';
					ibwrt(Device1,c,4);
					c[0]='N';
					c[1]='H';
					c[2]=(char)(48+j+8);
					c[3]='X';
					c[4]='\0';
					ibwrt(Device1,c,4);
					}
					else{
					d[0]='C';
					d[1]='C';
					d[2]='1';                                                  /* two-digit  */
```

```
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        d[0]='N';
                                        d[1]='H';
                                        d[2]='1';                                                       /* two-digit  */
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        }
                /*              }
                                else{
                                        c[0]='C';
                                        c[1]='B';
                                        c[2]=(char)(48+i);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        if (j<4){
                                        c[0]='C';
                                        c[1]='A';
                                        c[2]=(char)(48+j+6);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        }
                                        else{
                                        d[0]='C';
                                        d[1]='A';
                                        d[2]='1';
                                        d[3]=(char)(48+j-4);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        }
                                }
                  2-17-01       */
                                for(k=1;k<=16;k++){
                                        if((k!=i)&&(k!=j+8)){
                                                if (k<10){
                                                        if (k<=8){
                                                        c[0]='C';
                                                        c[1]='A';           /* apply -1.0 volt to rows from Keithley 5-25-01  */
                                                        c[2]=(char)(48+k);
                                                        c[3]='X';
                                                        c[4]='\0';
                                                        ibwrt(Device1,c,4);
                                                        }
                                                        else{
                                                        c[0]='C';
                                                        c[1]='H';
/*  Ground the columns */
                                                        c[2]=(char)(48+k);
                                                        c[3]='X';
                                                        c[4]='\0';
                                                        ibwrt(Device1,c,4);
                                                        }
                                                }
                                                else{
                                                d[0]='C';
                                                d[1]='H';
                                                d[2]='1';
                                                d[3]=(char)(48+k-10);
                                                d[4]='X';
                                                d[5]='\0';
                                                ibwrt(Device1,d,5);
                                                }
                                        }
                                }
                                /*  set write voltage */
                                Delay(0.1);
                                printf("\a");
                                if(ramp==1){
                                        if(cross_point[i][j]==1){
                                                volt_ramp0=volt_hold;
                                                volt_ramp1=0.0;
                                                for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
/* ramp-up */
                                                        volt_ramp0=volt_ramp0 + (volt_write_on/2-volt_hold)/ramp_num;
                                                        volt_ramp1=volt_ramp1 + (volt_write_on/2)/ramp_num;
                                                        m = AO_VWrite (1, 0, volt_ramp0);
                                                        m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                        Delay(volt_write_on/ramp_num/ramp_rate);
                                                        Delay(-volt_write_on/ramp_num/ramp_rate);
                                                }

                                                Delay(time_write);                                                                      /* hold */
                                                for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
/* ramp-down */
                                                        volt_ramp0=volt_ramp0 - (volt_write_on/2-volt_hold)/ramp_num;
                                                        volt_ramp1=volt_ramp1 - (volt_write_on/2)/ramp_num;
```

```
                                                m = AO_VWrite (1, 0, volt_ramp0);
                                                m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                Delay(volt_write_on/ramp_num/ramp_rate);
                                                Delay(-volt_write_on/ramp_num/ramp_rate);
                                        }
                                }
                                else{
                                        volt_ramp0=volt_hold;
                                        volt_ramp1=0.0;
                                        for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
                        /* ramp-up */
                                                volt_ramp0=volt_ramp0 + (volt_write_off/2-volt_hold)/ramp_num;
                                                volt_ramp1=volt_ramp1 + (volt_write_off/2)/ramp_num;
                                                m = AO_VWrite (1, 0, volt_ramp0);
                                                m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                Delay(volt_write_off/ramp_num/ramp_rate);
                                                Delay(-volt_write_off/ramp_num/ramp_rate);
                                        }
                                        Delay(time_write);                                                              /* hold */
                                        for(i_ramp=1; i_ramp<=ramp_num; i_ramp++){
                        /* ramp-down */
                                                volt_ramp0=volt_ramp0 - (volt_write_off/2-volt_hold)/ramp_num;
                                                volt_ramp1=volt_ramp1 - (volt_write_off/2)/ramp_num;
                                                m = AO_VWrite (1, 0, volt_ramp0);
                                                m = AO_VWrite (1, 1, (-volt_ramp1-0.06225)/0.9938);
                                                Delay(volt_write_off/ramp_num/ramp_rate);
                                                Delay(-volt_write_off/ramp_num/ramp_rate);
                                        }
                                }
                        }               /* with ramp */
                        else{
                                if(cross_point[i][j]==1){
                                        m = AO_VWrite (1, 0, (volt_write_on/2));
                                        m = AO_VWrite (1, 1, (-volt_write_on/2-0.06225)/0.9938);
                                }
                                else{
                                        m = AO_VWrite (1, 0, (volt_write_off/2));
                                        m = AO_VWrite (1, 1, (-volt_write_off/2-0.06225)/0.9938);
                                }
                                Delay(time_write);
                                m = AO_VWrite (1, 0, volt_hold);
                                m = AO_VWrite (1, 1, -0.06225/0.9938);
                        }                       /* no ramp */
                /*****  set holding voltage to the row, and Ground to the column  *****/
                                c[0]='C';
                                c[1]='A';
                                c[2]=(char)(48+i);
                                c[3]='X';
                                c[4]='\0';
                                ibwrt(Device1,c,4);
                                c[0]='N';
                                c[1]='B';
                                c[2]=(char)(48+i);
                                c[3]='X';
                                c[4]='\0';
                                ibwrt(Device1,c,4);
                                if (j<2){
                                c[0]='C';
                                c[1]='H';
                                c[2]=(char)(48+j+8);
                                c[3]='X';
                                c[4]='\0';
                                ibwrt(Device1,c,4);
                                c[0]='N';
                                c[1]='C';
                                c[2]=(char)(48+j+8);
                                c[3]='X';
                                c[4]='\0';
                                ibwrt(Device1,c,4);
                                }
                                else{
                                d[0]='C';
                                d[1]='H';
                                d[2]='1';                                                               /* two-digit  */
                                d[3]=(char)(48+j-2);
                                d[4]='X';
                                d[5]='\0';
                                ibwrt(Device1,d,5);
                                d[0]='N';
                                d[1]='C';
                                d[2]='1';                                                               /* two-digit  */
                                d[3]=(char)(48+j-2);
                                d[4]='X';
                                d[5]='\0';
                                ibwrt(Device1,d,5);
                                }
                        /*   ibwrt(Device1,"P0X",3);                    /*  open all relays (skipped  5-25-01) */
                }
        }
/* close the loop  */
m=SetCtrlVal(daq,MUX_Config_complete,1);
return 1;
}
```

```
int logic_check(int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2){
        /*SetCtrlVal(daq,MUX_STOP_SCAN,1);      */
        return 1;
}
int memory_check(int panel, int control, int event,
                        void *callbackData, int eventData1, int eventData2){
        /*SetCtrlVal(daq,MUX_STOP_SCAN,1);      */
int i,j,k,ii,m;
double r_dummy;
int fail[9][9];
double AD0[9][9][100],AD1[9][9][100];
char c[5],d[6];
        DeleteGraphPlot (daq, MUX_GRAPH, -1, VAL_IMMEDIATE_DRAW);
        m=SetCtrlVal(daq,MUX_Memory_Check_Done,0);
        m=SetCtrlVal(daq,MUX_Set_phase,0);
/*
        m=SetCtrlAttribute(daq,MUX_switch1_1r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch1_2r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch1_3r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch1_4r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch1_5r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch1_6r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch2_1r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch2_2r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch2_3r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch2_4r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch2_5r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch2_6r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch3_1r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch3_2r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch3_3r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch3_4r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch3_5r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch3_6r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch4_1r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch4_2r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch4_3r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch4_4r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch4_5r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch4_6r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch5_1r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch5_2r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch5_3r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch5_4r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch5_5r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch5_6r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch6_1r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch6_2r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch6_3r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch6_4r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch6_5r, ATTR_DIMMED, TRUE);
        m=SetCtrlAttribute(daq,MUX_switch6_6r, ATTR_DIMMED, TRUE);
12-12-01  LED's removed and kept in an untitled panel    */
        for(i=1;i<=8;i++){
                for(j=1;j<=8;j++){
                PlotLine(daq, MUX_GRAPH, (i-1)*8+(j-1), cross_point[i][j], (i-1)*8+j, cross_point[i][j],VAL_BLUE);
                }
        }
        m = GetCtrlVal (daq, MUX_TIME_READ, &time_read);
        m = GetCtrlVal (daq, MUX_VOLT_READ, &volt_read);
        m = GetCtrlVal (daq, MUX_Threshold_High, &threshold_high);
        m = GetCtrlVal (daq, MUX_Threshold_Low, &threshold_low);
        m = GetCtrlVal (daq, MUX_NUM_READ, &num_read);
        m = GetCtrlVal (daq, MUX_VOLT_HOLD, &volt_hold);
        fp_out=fopen(tmp_file,"w");
/*      Device1=ibdev(0,18,0,10,1,0);                   /* initiate 707A  */
/*      ibwrt(Device1,"E0X",3);                                         /* Point to present relays  */
        for(i=1;i<=8;i++){
                for(j=1;j<=8;j++){
                        c[0]='C';
                        c[1]='D';                       /* use relay row D to read (Vread+AC from function generater)  */
                    2]=(char)(48+i);
                        c[3]='X';
                        c[4]='\0';
                        ibwrt(Device1,c,4);
                        c[0]='N';
                        c[1]='A';
                        c[2]=(char)(48+i);
                        c[3]='X';
                        c[4]='\0';
                        ibwrt(Device1,c,4);
                        if (j<2){
                        c[0]='C';
                        c[1]='G';                                               /* amp-meter  */
                        c[2]=(char)(48+j+8);
                        c[3]='X';
                        c[4]='\0';
                        ibwrt(Device1,c,4);
                        c[0]='N';
                        c[1]='H';                                               /*  GND  */
                        c[2]=(char)(48+j+8);
                        c[3]='X';
```

```
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        }
                                        else{
                                        d[0]='C';
                                        d[1]='G';                                       /* amp-meter  */
                                        d[2]='1';
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        d[0]='N';
                                        d[1]='H';                                       /*  GND  */
                                        d[2]='1';
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        }
                                for(k=1;k<=16;k++){
                                        if((k!=i)&&(k!=j+8)){
                                                if (k<10){
                                                        if (k<=8){
                                                        c[0]='C';
                                                        c[1]='A';           /* apply -1.0 volt to rows from Keithley 5-25-01  */
                                                        c[2]=(char)(48+k);
                                                        c[3]='X';
                                                        c[4]='\0';
                                                        ibwrt(Device1,c,4);
                                                        }
                                                        else{
                                                        c[0]='C';
                                                        c[1]='H';
        /*  Ground the columns */
                                                        c[2]=(char)(48+k);
                                                        c[3]='X';
                                                        c[4]='\0';
                                                        ibwrt(Device1,c,4);
                                                        }
                                                }
                                                else{
                                                d[0]='C';
                                                d[1]='H';
                                                d[2]='1';
                                                d[3]=(char)(48+k-10);
                                                d[4]='X';
                                                d[5]='\0';
                                                ibwrt(Device1,d,5);
                                                }
                                        }
                                }

                                /*  set read voltage and measure the current  */
                                /* Delay (0.1);                                 5-25-01  */
                                printf("\a");
                                m = AO_VWrite (1, 0, volt_read);            /* channel 0's output goes to relay row B directly
                                                                                and goes to row D through function generater  */
                                Delay (0.1);                                /* delay after setting the read voltage */
                                /*manually set phase on the lock-in  5_28_01  */
                                /*
                                m=SetCtrlVal(daq,MUX_Set_phase,1);
                                scanf("%f",r_dummy);
                                m=SetCtrlVal(daq,MUX_Set_phase,0);          taken out for non-volatile devices   6-5-01*/

                                for (ii=0;ii<num_read;ii++){
                                m = AI_VRead (1, 0, 1, &adch0);                     /* output from current amplifier  */
                                m = AI_VRead (1, 1, 1, &adch1);                     /* output from lock-in amplifier   */

                                AD0[i][j][ii]=-adch0;                               /****  Current Amplifier revise the polarity!!  *****/
                                AD1[i][j][ii]=adch1;

                                if(ii>0) m=PlotLine (daq, MUX_GRAPH, 8.0*(i-1)+j-1+(double)(ii-1)/(double)(num_read-1), AD0[i][j][ii-1], 8.0*(i-1)+j-
1+(double)(ii)/(double)(num_read-1), AD0[i][j][ii], VAL_RED);
                                if(ii>0) m=PlotLine (daq, MUX_GRAPH, 8.0*(i-1)+j-1+(double)(ii-1)/(double)(num_read-1), AD1[i][j][ii-1], 8.0*(i-1)+j-
1+(double)(ii)/(double)(num_read-1), AD1[i][j][ii], VAL_GREEN);

                                Delay (time_read/num_read);
                                }
        /*****  set holding voltage to the row, and Ground to the column  *****/
                                        c[0]='C';
                                        c[1]='A';
                                        c[2]=(char)(48+i);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        c[0]='N';
                                        c[1]='D';
                                        c[2]=(char)(48+i);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        if (j<2){
                                        c[0]='C';
```

```
                                        c[1]='H';
                                        c[2]=(char)(48+j+8);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        c[0]='N';
                                        c[1]='G';
                                        c[2]=(char)(48+j+8);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        }
                                        else{
                                        d[0]='C';
                                        d[1]='H';
                                        d[2]='1';                                                       /* two-digit  */
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        d[0]='N';
                                        d[1]='G';
                                        d[2]='1';                                                       /* two-digit  */
                                        d[3]=(char)(48+j-2);
                                        d[4]='X';
                                        d[5]='\0';
                                        ibwrt(Device1,d,5);
                                        }
                                fail[i][j]=0;
                                if(cross_point[i][j]==0){
                                        for (ii=0;ii<num_read;ii++){
                                                if(AD0[i][j][ii]>threshold_low) {
                                                        fail[i][j]=1;
                                                        break;
                                                }
                                        }
                                }
                                if(cross_point[i][j]==1){
                                        for (ii=0;ii<num_read;ii++){
                                                if(AD0[i][j][ii]<threshold_high) {
                                                        fail[i][j]=1;
                                                        break;
                                                }
                                        }
                                }
                                /*  m = AO_VWrite (1, 0, 0.0);
                                ibwrt(Device1,"P0X",3);                                                 5-25-01  */
                        }
                }
/* close the loop  */

/*****  set holding voltage to the rows, and Ground to the columns  *****/
                for(k=1;k<=16;k++){
                        if (k<10){
                                if (k<=8){
                                        c[0]='C';
                                        c[1]='A';                       /* apply -1.0 volt to rows from Keithley 5-25-01  */
                                        c[2]=(char)(48+k);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        }
                                        else{
                                        c[0]='C';
                                        c[1]='H';                                       /*  Ground the columns */
                                        c[2]=(char)(48+k);
                                        c[3]='X';
                                        c[4]='\0';
                                        ibwrt(Device1,c,4);
                                        }
                                }
                                else{
                                d[0]='C';
                                d[1]='H';
                                d[2]='1';
                                d[3]=(char)(48+k-10);
                                d[4]='X';
                                d[5]='\0';
                                ibwrt(Device1,d,5);
                                }
                        }
/*
if(fail[1][1]==0) {
                m=SetCtrlAttribute(daq,MUX_switch1_1r, ATTR_DIMMED, FALSE);
                m=SetCtrlVal(daq,MUX_switch1_1r,cross_point[1][1]);}
if(fail[1][2]==0) {
                m=SetCtrlAttribute(daq,MUX_switch1_2r, ATTR_DIMMED, FALSE);
                m=SetCtrlVal(daq,MUX_switch1_2r,cross_point[1][2]);}
if(fail[1][3]==0) {
                m=SetCtrlAttribute(daq,MUX_switch1_3r, ATTR_DIMMED, FALSE);
                m=SetCtrlVal(daq,MUX_switch1_3r,cross_point[1][3]);}
if(fail[1][4]==0) {
                m=SetCtrlAttribute(daq,MUX_switch1_4r, ATTR_DIMMED, FALSE);
```

```
		m=SetCtrlVal(daq,MUX_switch1_4r,cross_point[1][4]);}
if(fail[1][5]==0) {
		m=SetCtrlAttribute(daq,MUX_switch1_5r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch1_5r,cross_point[1][5]);}
if(fail[1][6]==0) {
		m=SetCtrlAttribute(daq,MUX_switch1_6r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch1_6r,cross_point[1][6]);}
if(fail[2][1]==0) {
		m=SetCtrlAttribute(daq,MUX_switch2_1r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch2_1r,cross_point[2][1]);}
if(fail[2][2]==0) {
		m=SetCtrlAttribute(daq,MUX_switch2_2r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch2_2r,cross_point[2][2]);}
if(fail[2][3]==0) {
		m=SetCtrlAttribute(daq,MUX_switch2_3r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch2_3r,cross_point[2][3]);}
if(fail[2][4]==0) {
		m=SetCtrlAttribute(daq,MUX_switch2_4r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch2_4r,cross_point[2][4]);}
if(fail[2][5]==0) {
		m=SetCtrlAttribute(daq,MUX_switch2_5r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch2_5r,cross_point[2][5]);}
if(fail[2][6]==0) {
		m=SetCtrlAttribute(daq,MUX_switch2_6r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch2_6r,cross_point[2][6]);}
if(fail[3][1]==0) {
		m=SetCtrlAttribute(daq,MUX_switch3_1r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch3_1r,cross_point[3][1]);}
if(fail[3][2]==0) {
		m=SetCtrlAttribute(daq,MUX_switch3_2r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch3_2r,cross_point[3][2]);}
if(fail[3][3]==0) {
		m=SetCtrlAttribute(daq,MUX_switch3_3r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch3_3r,cross_point[3][3]);}
if(fail[3][4]==0) {
		m=SetCtrlAttribute(daq,MUX_switch3_4r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch3_4r,cross_point[3][4]);}
if(fail[3][5]==0) {
		m=SetCtrlAttribute(daq,MUX_switch3_5r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch3_5r,cross_point[3][5]);}
if(fail[3][6]==0) {
		m=SetCtrlAttribute(daq,MUX_switch3_6r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch3_6r,cross_point[3][6]);}
if(fail[4][1]==0) {
		m=SetCtrlAttribute(daq,MUX_switch4_1r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch4_1r,cross_point[4][1]);}
if(fail[4][2]==0) {
		m=SetCtrlAttribute(daq,MUX_switch4_2r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch4_2r,cross_point[4][2]);}
if(fail[4][3]==0) {
		m=SetCtrlAttribute(daq,MUX_switch4_3r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch4_3r,cross_point[4][3]);}
if(fail[4][4]==0) {
		m=SetCtrlAttribute(daq,MUX_switch4_4r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch4_4r,cross_point[4][4]);}
if(fail[4][5]==0) {
		m=SetCtrlAttribute(daq,MUX_switch4_5r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch4_5r,cross_point[4][5]);}
if(fail[4][6]==0) {
		m=SetCtrlAttribute(daq,MUX_switch4_6r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch4_6r,cross_point[4][6]);}

if(fail[5][1]==0) {
		m=SetCtrlAttribute(daq,MUX_switch5_1r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch5_1r,cross_point[5][1]);}
if(fail[5][2]==0) {
		m=SetCtrlAttribute(daq,MUX_switch5_2r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch5_2r,cross_point[5][2]);}
if(fail[5][3]==0) {
		m=SetCtrlAttribute(daq,MUX_switch5_3r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch5_3r,cross_point[5][3]);}
if(fail[5][4]==0) {
		m=SetCtrlAttribute(daq,MUX_switch5_4r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch5_4r,cross_point[5][4]);}
if(fail[5][5]==0) {
		m=SetCtrlAttribute(daq,MUX_switch5_5r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch5_5r,cross_point[5][5]);}
if(fail[5][6]==0) {
		m=SetCtrlAttribute(daq,MUX_switch5_6r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch5_6r,cross_point[5][6]);}
if(fail[6][1]==0) {
		m=SetCtrlAttribute(daq,MUX_switch6_1r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch6_1r,cross_point[6][1]);}
if(fail[6][2]==0) {
		m=SetCtrlAttribute(daq,MUX_switch6_2r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch6_2r,cross_point[6][2]);}
if(fail[6][3]==0) {
		m=SetCtrlAttribute(daq,MUX_switch6_3r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch6_3r,cross_point[6][3]);}
if(fail[6][4]==0) {
		m=SetCtrlAttribute(daq,MUX_switch6_4r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch6_4r,cross_point[6][4]);}
if(fail[6][5]==0) {
```

```
		m=SetCtrlAttribute(daq,MUX_switch6_5r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch6_5r,cross_point[6][5]);}
if(fail[6][6]==0) {
		m=SetCtrlAttribute(daq,MUX_switch6_6r, ATTR_DIMMED, FALSE);
		m=SetCtrlVal(daq,MUX_switch6_6r,cross_point[6][6]);}

  12-12-01	taken out, because the LED's are removed*/

m=SetCtrlVal(daq,MUX_Memory_Check_Done,1);
		for(i=1;i<=8;i++){
			for(j=1;j<=8;j++){
				for (k=0;k<num_read;k++){
					fprintf(fp_out, "%d %d %d %f %f\n", i, j, cross_point[i][j], AD0[i][j][k], AD1[i][j][k]);
					}
				}
			}
		fclose(fp_out);
		return 1;
}
int stop(int panel, int control, int event,
			void *callbackData, int eventData1, int eventData2){
		return 1;
}
int save_file(int panel, int control, int event,
			void *callbackData, int eventData1, int eventData2){
		int i;
		int tmp1[6400],tmp2[6400],tmp3[6400];
		float tmp4[6400], tmp5[6400];
		char line[100];
		char name[30];
		fp_out=fopen (tmp_file,"r");
		for (i = 0; i < num_read*64; ++i)
			{
			fgets(line,sizeof(line),fp_out);
			sscanf(line,"%d %d %d %f %f", &tmp1[i], &tmp2[i], &tmp3[i], &tmp4[i], &tmp5[i]);
			}
		 fclose(fp_out);
		PromptPopup ("SAVE FILE", "Enter the file name (*.txt).", name, 20);
		fp_out=fopen(name,"w");
		for (i =0; i < num_read*64; ++i)
			fprintf(fp_out,"%d %f %f\n",tmp3[i], tmp4[i], tmp5[i]);
		fclose(fp_out);
		return 1;
}
int quit(int panel, int control, int event,
			void *callbackData, int eventData1, int eventData2)
{
		int i;
		switch (event) {
			case EVENT_COMMIT:
				i = AO_VWrite (1, 0, 0.0);
				i = AO_VWrite (1, 1, 0.0);
				ibwrt(Device1,"P0X",3);
				QuitUserInterface (0);
				break;
			case EVENT_RIGHT_CLICK:
				break;
		}
		return 0;
}
/*
int load_individual_panel (int panel, int control, int event, void *callbackData, int eventData1, int eventData2)
{
		daq1 = LoadPanel (0, "MUX.uir",SET_INDIVI);
		DisplayPanel (daq1);
		return 0;
}
*/
int clear (int panel, int control, int event,
			void *callbackData, int eventData1, int eventData2)
{
		int i;
		switch (event) {
			case EVENT_COMMIT:
				DeleteGraphPlot (daq, MUX_GRAPH, -1, VAL_IMMEDIATE_DRAW);
/*				DeleteGraphPlot (daq, DAQ_GRAPH_2, -1, VAL_IMMEDIATE_DRAW);		*/
				break;
		}
		return 0;
}
```

Chapter 5

Covalent modification and electrical characterization of silicon (111)-on-insulator devices

5.1 Introduction

5.1.1 Electrical properties of silicon surfaces

As the dimensions of silicon (Si) devices are scaled to the nanometer regime, the properties of the surface play an increasingly prominent role in determining the overall device characteristics. This has presented significant challenges, and opportunities, to the nanoelectronic community, where surface effects manifest over a range of applications. Recent examples include substantial increases in the quality factor of electromechanical resonators through covalent modification of the surface[1], and the demonstration that electrical transport in ultra-thin (< 20 nm) silicon-on-insulator epilayers can be completely dominated by the electronic properties of the surface[3]. Silicon-on-insulator, or SOI, consists of a thin layer of single-crystal Si on a SiO_2 support, and is rapidly becoming the preferred platform for high-speed microelectronics, nanoelectronics, and sensor applications. However, surface effects such as interface roughness[6, 7], surface

optical[8-13] (SO) phonons, film stress[14], and coulombic interactions with electrically active surface states[15] (also called interface or trap states) scatter charge carriers in thin-film SOI devices, resulting in degradation of charge-carrier mobility. Additionally, surface states introduce localized energy levels continuously distributed in energy throughout the silicon bandgap that function as recombination-generation (R-G) centers catalyzing the annihilation and/or creation of charge carriers (Figure 5-1.A). Such states facilitate indirect recombination of electron-hole pairs by capturing an electron (or hole) within a bound-state orbit about the R-G center site until recombination occurs. This significantly increases the probability of electron-hole recombination, since an electron and hole no longer have to interact simultaneously in space and time[16, 17]. The technological implication of charge-carrier annihilation and creation due to electrically active surface states is the introduction of a significant amount of randomness into the operational behavior of the device. This is because the character, density, and energy distribution of surface states are exquisitely sensitive to very small fabrication details, and thus vary considerably from device to device[18].

The most egregious effect of surface states is their introduction of significant non-idealities into the behavior of metal-oxide-silicon (MOS) field-effect devices, the workhorse of modern information-processing technology, and the operational basis for the demultiplexer architecture described in Chapter 3. Figure 5-1.B shows how surface states influence the electrical characteristics of field-effect devices. To a good approximation, all surface states below the Fermi energy, E_F, are full and those above it are empty. These states continuously fill and empty as the Fermi energy moves upward in the bandgap with positive gate voltages and downward with negative gate voltages,

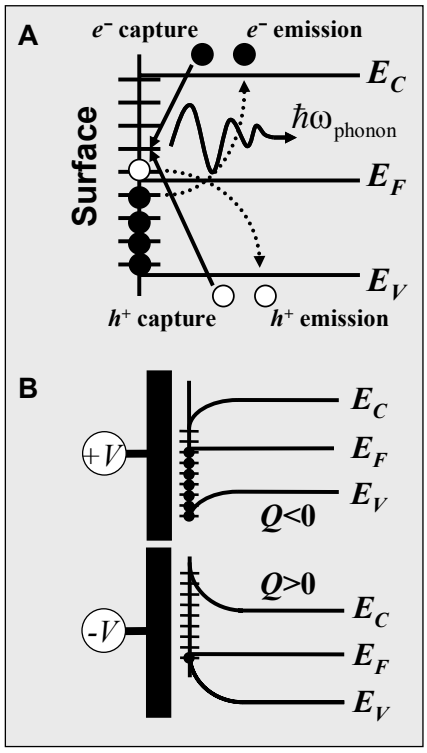


Figure 5-1. Surface states at a silicon interface. A. Surface states are distributed throughout the bandgap and can capture (solid arrows) or emit (dotted arrows) charge carriers. Carrier capture can result in electron-hole recombination with emission of lattice phonons. **B.** Surface states charge and discharge as a function of gate bias producing a net charge Q at the surface (see text).

respectively. Surface states roughly above the middle of the bandgap are believed to be acceptor-like (that is, neutral when empty and negative when filled with an electron), while those below midgap are believed to be donor-like (that is, positively charged when empty and neutral when filled with an electron)[19]. Thus, the application of a gate voltage produces a net charge per unit area, Q, at the Si/oxide interface of a MOS device. Since the surface states always remain fixed in energy relative to the conduction and valence band edges, a voltage more positive than the flat-band voltage, V_{FB}, (the voltage in which there is no band bending at the surface) draws electrons into the upper, acceptor-like surface states, making $Q < 0$, while negative voltages less than V_{FB} empties those states, making $Q > 0$. The point is that surface states can charge and discharge as a function of gate voltage, resulting in understandable, but generally unpredictable, behavior from field-effect devices.

To see this more quantitatively, consider a simple metal-oxide-silicon (MOS) capacitor (where the oxide is unspecified). Taking the direction from the metal/oxide interface into the Si layer as the positive x-direction (with $x = 0$ at the metal/oxide

interface), the potential applied to the metal gate, V_G, is dropped partly across the oxide, $\Delta\phi_{ox}$, and partly across the Si bulk, $\Delta\phi_{Si}$, or

$$V_G = \Delta\phi_{ox} + \Delta\phi_{Si} = \Delta\phi_{ox} + \phi_S \,, \tag{1}$$

where ϕ_S is the potential at the Si/oxide interface (since the potential goes to zero within the Si bulk). Poisson's equation can be used to relate the voltage dropped across the oxide to the potential at the Si surface as

$$\nabla^2\phi = -\frac{\rho_{ox}(x)}{\kappa_{ox}\varepsilon_0} = -\frac{dE_{ox}}{dx}, \tag{2}$$

where $\rho_{ox}(x)$ is the charge density distribution across the oxide layer, E_{ox} is the electric field across the oxide layer, and κ_{ox} is the oxide dielectric constant. Two integrations of equation (2) across the oxide layer of thickness t_{ox} then gives

$$\Delta\phi_{ox} = t_{ox}E_{ox}(t_{ox}) - \frac{1}{\kappa_{ox}\varepsilon_0}\int_0^{t_{ox}}\int_x^{t_{ox}} \rho_{ox}(x')dx'\,dx \,. \tag{3}$$

Invoking the electrostatic boundary condition relating the normal components of the electric displacement fields on either side of the Si/oxide interface, and assuming there is no charge at the interface other than that possibly included in ρ_{ox} gives

$$E_{ox}(t_{ox}) = \frac{\kappa_{Si}}{\kappa_{ox}}E_S(\phi_S) \,, \tag{4}$$

where κ_{Si} is the Si dielectric constant, and E_S is the electric field at the Si/oxide interface (which, of course, is a function of ϕ_S). The oxide charge density due to charged surface states resides right at the Si/oxide interface, and thus can be modeled as a delta function. Substituting $\rho_{ox}(x) = \pm Q(\phi_S)\,\delta(x - t_{ox})$ and equation (4) into equation (3) then gives

$$\Delta\phi_{ox} = \frac{\kappa_{Si}}{\kappa_{ox}}t_{ox}E_S - \frac{t_{ox}Q}{\kappa_{ox}\varepsilon_0} = \frac{\kappa_{Si}}{\kappa_{ox}}t_{ox}E_S(\phi_S) \pm \frac{Q(\phi_S)}{C_{ox}} \,, \tag{5}$$

where C_{ox} is the oxide capacitance per unit area. Substituting equation (5) into equation (1) gives

$$V_G = \phi_S + \frac{\kappa_{Si}}{\kappa_{ox}} t_{ox} E_S(\phi_S) \pm \frac{Q(\phi_S)}{C_{ox}}. \quad (6)$$

Equation (6) relates the voltage applied to the gate of a field-effect device, V_G, to the voltage 'seen' by the Si surface, ϕ_S. The effect of charged surface states is accounted for by the last term, which shows that the required gate voltage to obtain a given surface potential (the operational voltage of the device) will vary from device to device due to the presence of Q in equation (6).

Intensive experimental investigation of the Si surface and the Si/oxide interface (especially the Si/SiO_2 interface) has identified unsatisfied or 'dangling' Si bonds at the Si surface as the primary physical origin of surface states. When the Si lattice is cleaved along a particular plane to form a surface, one of the four Si–Si bonds is broken, thus leaving a dangling bond pointing in the direction perpendicular to the surface plane. The density of these dangling bonds per unit area of surface depends on the surface orientation and whatever reconstruction the surface might undergo[18]. Growth of a SiO_2 layer at the Si surface satisfies many of these dangling bonds (with the number critically dependent on the quality of the SiO_2 and thus the growth conditions), but not all, and the remaining dangling bonds are believed to result in electrically active surface states[20].

While the density of surface states and their energy distribution can vary considerably from one device to the next, the vast amount of experimental research on the electrical properties of Si surfaces has revealed some general trends[19]. For one, the density of surface states (states per unit area per unit energy) is about an order of magnitude greater on (111) surfaces than on (100) surfaces. This observation is correlated

with the number of dangling bonds per unit area at the Si surface. A (111) surface has roughly 15 percent more dangling bonds, which results in a faster oxidation rate of the (111) surface than the (100) surface during SiO_2 growth, a higher percentage of Si sub-oxides (SiO_x with $x \leq 2$), and thus a larger density of surface states[21]. It is primarily for this reason that the Si(100) surface has been used almost exclusively in the microelectronics industry.

5.1.2 Covalent modification of silicon (111) surfaces

Despite the less-than-ideal Si(111)/SiO_2 interface, the Si(111) surface has a number of attractive qualities for scientific and technological applications. The majority of these applications stem from the fact that a (111) surface can be made atomically smooth with nearly perfect hydrogen termination through simple bench-top aqueous NH_4F etching[22, 23]. In addition, dangling bonds on a (111) surface point in a direction normal to the surface plane, resulting in a structurally and chemically simple surface ideal for ultra-high vacuum (UHV) surface studies, such as scanning tunneling microscopy (STM)[24, 25] and small molecule adsorption[26], in addition to providing a convenient handle for covalent functionalization of the surface using a variety of techniques[27].

The hydrogen-terminated Si(111) surface obtained after aqueous fluorine-based etching has been well documented to have a low number of structural defect sites and electrically active surface states. This was first demonstrated by Yablonovich *et al.* through surface recombination measurements of hydrogen-terminated Si(111) surfaces[28] and has since been corroborated by a number of researchers[2, 27, 29]. The number of electrically active states on Si(111) surfaces has been reduced to very low levels (less

than one electrically active state per 10^8 surface atoms) through complete hydrogen passivation[28]. This is about two orders of magnitude less than the number of surface states measured from optimally-processed Si(100)/SiO_2 interfaces.

However, the electronic quality of hydrogen-terminated Si(111) surfaces rapidly degrades in air due to surface oxidation[29-31]. Consequently, several methods have been developed to achieve robust oxide-free alkyl passivation of crystalline Si surfaces[27]. These methods feature direct carbon-silicon bonding (as opposed to more labile Si–O–C linkages) and offer the advantage of a well ordered monolayer via kinetically inert covalent bonds that are stable up to 650° C in UHV[32].

Directly bonded alkyl monolayers have been demonstrated to be of much higher quality on Si(111) surfaces than on Si(100) surfaces[33]. This is because the top-most atoms of a Si(111) surface are characterized by a single dangling bond pointing perpendicular to the surface plane, while each Si(100) surface atom has two dangling bonds that point towards neighboring Si(100) surface atoms in adjacent rows. Steric interference thus prevents full alkyl passivation of Si(100) surfaces, even with the smallest hydrocarbon species, *e.g.*, methyl groups.

This is in contrast to Si(111) surfaces in which molecular modeling and cryogenic STM experiments by Yu *et al.*[24] have confirmed that complete methyl termination of every (top-most) surface Si atom on an unreconstructed (1×1) surface is possible. It is believed that surface functionalization with longer-chain alkyl groups (C_nH_{2n+1} with $n \geq 2$) results in incomplete coverage of the Si(111) surface due to steric interactions, with non-alkyl passivated surface sites being terminated primarily by hydrogen[4, 34].

The surface functionalization chemistry employed in studies by Yu *et al*. to obtain high-quality methyl-terminated Si(111) surfaces was developed within the Lewis group at Caltech[35], and consists of a simple two-step chlorination/methylation procedure. This method has been demonstrated from numerous studies to produce high-quality methyl passivated Si(111) surfaces[2, 5] that are robust to oxidation[36], and are characterized by low numbers of electrically active surface states[29]. Beyond STM studies, molecular-level control over the interfacial chemistry of Si surfaces is expected to find applications in molecular electronics[37] and nanoelectronics[38, 39]. A specific example of the latter is described below.

5.1.3 Application to FET-based nanowire demultiplexers

Methyl passivation of Si surfaces could have important applications in nanoelectronics where control of the surface is paramount. For instance, the nanowire (NW) demultiplexer described in Chapter 3 was hindered in its ability to selectively address a given NW from within an ultra-dense array by the presence of a thin native oxide coating the NWs. Figure 5-2 shows a schematic cross section of a portion of the demultiplexer structure with four NWs coming out of the plane of the page. The ability of the demultiplexer to reduce the conductivity of NW_G relative to that of NW_I is determined by the how much of the

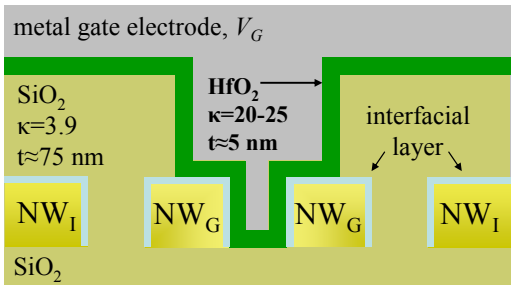


Figure 5-2. Schematic cross-section of a nanowire (NW) demultiplexer. The demultiplexer architecture selects a given NW by field-effect gating all the rest of the NWs in the array. Gated and isolated nanowires, NW_G and NW_I, respectively, are shown coming out of the page.

applied gate voltage, V_G, is seen at NW_G. This is given by the voltage dropped across the HfO_2/interfacial layer shown in the figure, and which equation (5) gives as (ignoring the surface-state term and modifying the second term to account for the added layers of dielectric material)

$$\Delta\phi_{ox} = V_G - \phi_S = \kappa_{Si}\left(\frac{t_i}{\kappa_i} + \frac{t_{HfO_2}}{\kappa_{HfO_2}}\right)E_S(\phi_S), \tag{7}$$

where t_i and κ_i are the thickness and dielectric constant of the interfacial layer (SiO_2 or CH_3). Equation (7) clearly shows that the selective gating of NW_G can be enhanced by replacing the NW native SiO_2 at the interface ($t_i \approx 1.5$ nm, $\kappa_i = 3.9$) by a covalently bonded methyl monolayer ($t_i \approx 0.2$ nm, $\kappa_i \approx 2$). Plugging these numbers into equation (7) predicts a 100 percent increase in the gating of NW_G, and, thus, a 100 percent increase in the demultiplexer selectivity (isolated NW current/gated NW current).

Additionally, CH_3-passivated NWs eliminate the electrically active native SiO_2/Si interface that has been present in previous-generation demultiplexer devices. Due to their chaotic mode of formation, native oxides are highly defective and do not successfully passivate surface states[21, 40]. Conversely, a well-ordered CH_3-Si(111) interface reduces the number of surface states by many orders of magnitude and should translate into more-efficient and -reliable FET-based devices. This could be particularly important for use with high-κ dielectrics, which generally form a significantly more-defective interface than does Si/SiO_2.

The majority of work with alkyl-passivated Si(111) surfaces has utilized bulk wafers. While such wafers are convenient for obtaining high-quality, atomically flat surfaces, and are compatible with a variety of surface characterization techniques, they

are less useful for nanoelectronic applications, where silicon-on-insulator (SOI) structures are generally required. This was the motivation for the work described below. The next two sections of this chapter will first describe the passivation and surface characterization of ultra-thin SOI, followed by electrical measurements employing variable temperature Hall effect measurements.

5.2 Fabrication and methyl passivation of SOI devices

This section describes the fabrication of Si(111)-on-insulator Hall bar devices and their functionalization using a modified two-step chlorination/methylation procedure.

5.2.1 Si(111)-on-insulator wafer fabrication

An unexpected challenge proved to be obtaining the appropriate SOI starting material. This is because the overwhelmingly dominant SOI material is Si(100), which can be purchased commercially. Additionally, (100)-oriented SOI wafers are available with Si epilayer thicknesses in the low tens of nanometers by fabrication techniques such as *separation by implanted oxygen* or SIMOX. This is in contrast to (111)-oriented SOI wafers, which are usually custom fabricated using a bonding process. This involves the oxidation of two bulk Si(111) wafers that are bonded together on their oxidized side through a high-temperature process. While this produces a Si(111)-on-insulator structure, the Si epilayer is very thick and must be subsequently thinned.

This led us to a collaboration with Isonics Corp. to develop a (111)-oriented, bonded SOI wafer (buried oxide thickness of 0.9–2 μm) with an epilayer thickness of less than 100 nm. A feedback loop was set up between our lab and Isonics to determine the processing parameters that consistently gave the highest quality Si(111) epilayer surface. Isonics' processing consisted of bonding the SOI wafer, grinding and lapping to thin it down, and applying a final (proprietary) touch polish to further reduce the Si epilayer thickness and smoothen out thickness inhomogeneities introduced during the grinding and lapping procedure. This set of procedures reduced the bonded SOI epilayer thickness to 100–200 nm. Our post-processing then consisted of thinning the wafers by growing a high-quality sacrificial oxide under dry conditions (*e.g.*, $Si + O_2 \rightarrow SiO_2$) at temperatures ranging from 1050° to 1100°. The exact growth time and temperature was obtained from calculations employing the Deal-Grove model[18] of thermal oxidation on a Si(111) surface, taking into account that 44 percent of the total thermal oxide thickness was due to consumed Si. The sacrificial oxide was then removed by wet etching in buffered oxide etch (BOE) (6:1 40% NH_4F to 49% HF; Gallade) and the thickness was measured using optical reflectance or ellipsometry. After a couple of SOI generations, the optimal starting thickness to begin thermal oxidation thinning was determined to be about 180 nm. Wafers that were polished to be thinner before the thermal oxidation step were found to produce poorer surfaces. Although these wafers were found to be locally homogeneous by atomic force microscopy (AFM) measurements, they were quite inhomogeneous over centimeter length scales. The data below shows pooled standard deviations of Si epilayer thicknesses for representative wafers. (Each row represents averages from three wafers.)

Average Si(111) epilayer thickness (nm)	Pooled standard deviation from 35 measurements on each of three samples (± nm)
20	6
34	3
45	9
50	6

5.2.2 Hall bar fabrication

Si(111)-on-insulator wafers were cleaved into approximately 1-cm squares, and doped using the spin-on doping protocol described in Chapter 2. Briefly, the wafers were sonicated in methanol and swabbed using a Texwipe CleanTip swab to remove particulates. After ensuring the wafer was clean, a 1:10 diluted (dopant to methanol) spin-on dopant solution was spin-coated (at 4000 RPM) onto the wafer surface and subsequently baked at 200° C for 10 min to drive off excess solvent. Emulsitone (Whippany, NJ) Phosphorosilicafilm and Borosilicafilm were used for n-type and p-type doping, respectively. The dopant-film-coated wafer was then annealed under nitrogen in a rapid thermal annealer for the appropriate time and temperature to achieve a given doping concentration. After annealing, the dopant film was removed by swirling in BOE until the surface was hydrophobic (usually less than 10 seconds). At this point, four-point-probe surface-resistivity measurements were used to measure the doping level, which ranged from $1\times10^{18} - 1\times10^{20}$ P or B atoms/cm^3. The measured dopant distribution

as a function of depth into n- and p-doped (111)-oriented SOI epilayers is shown in Figure 5-3.

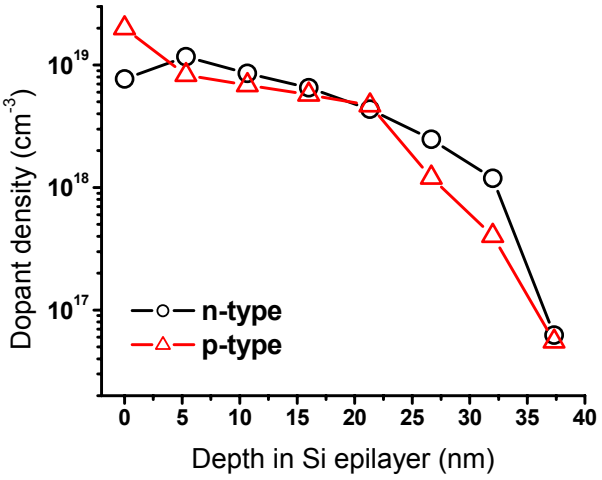


Figure 5-3. Dopant density vs. depth for 40-nm-thick diffusion-doped Si(111) epilayers. The n-type wafer was annealed for 5 min at 950° C; the p-type wafer was annealed for 5 min at 1050 ° C.

Photolithography was used to define rectangular Hall bars (described in more detail below) to facilitate resistivity and Hall mobility measurements. Specifically, AZ-5214 (Clariant) was spin-coated onto the wafer at 4000 RPM, baked at 105° C for 5 minutes, and exposed (λ = 405 nm, area dose ≈ 20 mW/cm^2) using a Karl Suss MA-6 mask aligner through a Cr mask. The exposed pattern was then developed in AZ-400k developer (pH ≈ 13, Clariant). The Cr mask exposed four Hall bar patterns into the photoresist (spaced by 1 mm along the perimeter of a square). Additionally, the mask exposed a large 2-mm square to facilitate x-ray photoelectron spectroscopy (XPS) measurements from the same chip from which the devices were fabricated. Electron-beam evaporation followed by lift-off was used to deposit 100 nm of Al onto the wafer surface to act as an etch mask. The Al Hall bar patterns were transferred into the underlying Si(111) epilayer using fluorine-based (CF_4 to He 20:30, 5 mTorr, 40 W) reactive-ion etching. The endpoint was determined via interferometric detection. The Al was then removed by 5 minutes in a ~ 50° C solution of 80% H_3PO_4 + 5% HNO_3 + 5% glacial acetic acid + 10% H_2O (18 MΩ Millipore),

revealing four Si Hall bars and a 2-mm square sitting on top of an oxide surface. Note that devices were fabricated, as much as possible, before surface passivation. This strategy avoided exposing CH_3-SOI surfaces to the harsh procedures described above (particularly AZ-400k, which is strongly basic, and the H_3PO_4/HNO_3 step).

5.2.3 Methyl passivation of SOI devices

With bulk Si(111) wafers, the various wet-chemical procedures can be allowed to continue for arbitrarily long periods without regard to over-etching the Si surface. In contrast, all of the wet chemical steps described here had to be optimized to obtain high-quality methyl passivation without over-etching the SOI surface or significantly etching the supporting SiO_2 in contact with solution. For small devices and nanowires, this caused significant undercutting which occasionally resulted in lifting-off of the SOI device (or nanowires).

Figure 5-4 shows the chlorination/methylation reaction protocol adapted from the Lewis group at Caltech[2]. Before functionalization, the wafers were rigorously cleaned to remove photoresist and fluoropolymeric by-products that may have been deposited on the surface from the previous photolithographic and etching steps. (For consistency, these steps were also followed for wafers that were not patterned into Hall bars, *i.e.*, surfaces intended for XPS analysis only.) This was accomplished with an aggressive piranha-clean

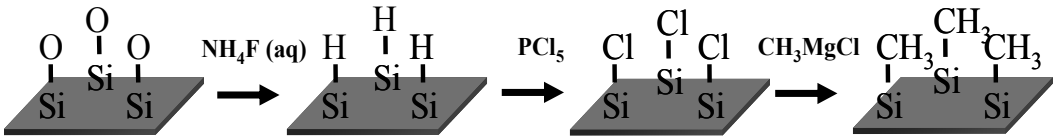


Figure 5-4. SOI chlorination/methylation reaction protocol.

step (1:2 concentrated H_2SO_4 to 30% H_2O_2 at 120º C for 5 minutes followed by a ~10 minute soak in H_2O). The wafer was etched for 5 seconds in diluted BOE (1:10 BOE to H_2O) to strip the native oxide, and rinsed in H_2O. The wafer was immediately immersed in a 1:1:5 NH_4OH:H_2O_2:H_2O solution for 15 minutes at 80º C, followed by an H_2O rinse and another 5 second dip in diluted BOE, and dried under a stream of N_2.

To obtain a flat Si(111) surface, the wafer was then etched for 5 minutes at room temperature in de-oxygenated 40% NH_4F (pH ≈ 7.8; Transene Inc.). The NH_4F was de-oxygenated by bubbling Ar into the solution with occasionally stirring for at least 40 minutes. The wafer was rinsed in water, dried under N_2, and immediately loaded into a N_2-purged glovebox for the chlorination and methylation steps. The surfaces were chlorinated using a saturated solution of PCl_5 in chlorobenzene with a few grains of benzoyl peroxide for radical initiation. The reaction time ranged from 10 to 45 minutes at 80–90º C, with the optimal reaction time discussed in Section 5.3. (It is worth noting that the chlorination reaction can also be carried out using Cl_2 gas in a Schlenk line[2] which has been demonstrated to result in less pitting of the Si surface[41].) The PCl_5 method was used here primarily because of convenience; however, it is worth noting that the PCl_5 method is compatible with batch-manufacturing protocols making this reaction protocol more relevant for technical applications.

The wafers were removed from the PCl_5 solution, rinsed with tetrahydrofuran (THF) followed by CH_3OH, and dried under N_2. The chlorine-terminated surfaces were methylated by refluxing in 3.0 M CH_3MgCl in THF (Aldrich) for 2.5–3 hours at 70–80º C. After the reaction, the wafers were rinsed in THF followed by CH_3OH, dried under N_2, and removed from the glovebox. The samples were additionally sonicated for 5 minutes in CH_3OH, followed by CH_3CN to remove any Mg from the methyl-Grignard reagent.

5.2.4 Making electrical contact to methyl-passivated devices

Electrical contacts to Hall bar structures had to be deposited following the methylation reaction since typical contact metals react with the various wet-chemical procedures (NH_4F, PCl_5, and CH_3MgCl). This constraint can be alleviated by masking the metal contacts with Si_2N_3 (which is not etched in NH_4F) before the functionalization reaction; however, as I will show in the next section this is not required since the methyl monolayer is robust to the microelectronic fabrication protocols used here.

Positive-tone photoresists such as AZ-5214 result in significant carbon contamination[18] of the CH_3–Si(111) surface, is difficult to remove without using harsh treatments (such as acidic piranha), that, as will be shown below, oxidize the CH_3–passivated surface. Thus, the surface was protected by spin-coating it with a layer of either 3% poly-methyl methacrylate (PMMA) or 5.5% methyl methacrylate (MMA) before spin-coating the photoresist on top. An optical mask was used to expose the contact electrode pattern followed by development in AZ-400k. To obtain good electrical contacts, the methyl-passivation and the PMMA or MMA layer protecting the methyl

surface (which is not removed during the basic AZ-400k development) had to be removed before depositing contacting metals. This was accomplished by an aggressive O_2 plasma etch (4 min, 20 mTorr, 100 W) followed by a five-second dip in undiluted BOE. Contact angle measurements on similarly processed methyl-passivated wafers were performed before and after this treatment to confirm removal of the organic layer as shown in the table below. Note that the surface was allowed to sit in air for a couple of hours to oxidize after the BOE step. Rapid re-growth of surface oxide confirmed removal of the methyl monolayer.

Treatment on CH_3-Si(111) surface	Water contact angle
Before O_2 + BOE	70 ± 3°
After O_2 + BOE + sitting in air	32 ± 3°

Following the O_2 + BOE step, the wafer was immediately loaded into an electron-beam metal evaporator and a tri-layer stack of Ti/Pt/Au (10 nm/10 nm/150 nm) was deposited at rates of 0.25 Å s^{-1}, 0.25 Å s^{-1}, and 1 Å s^{-1}, respectively. The temperature was monitored during the metal deposition on a separate Si(111) surface using a thermocouple lead in contact with the wafer surface. The highest recorded temperature was ~30° C and occurred during the Pt deposition. The capping Au layer was deposited to facilitate (Au) wire bonding in a subsequent step. The Pt layer was required to prevent Au from diffusing into the Si during a subsequent contact anneal, which was observed to result in a significant reduction of the device conductivity (note that Au impurities in Si introduce efficient mid-bandgap R-G centers[19]).

Lift-off was accomplished in acetone with brief sonication. After lift-off, the wafer was immersed in fresh acetone, sonicated for 5 minutes, and allowed to soak for ~20 minutes at 50° C. To gently remove excess organic residue, the wafer was soaked for over an hour in anisole heated to 150° C. The wafer was then annealed for 5 minutes at 425° C under a N_2 ambient to promote ohmic contact formation. Before proceeding, room temperature current-voltage (*I–V*) scans were performed to confirm the quality of the device contacts. Last, the chip was protected with a thick spin-coated layer of PMMA and cleaved to separate the four wired-up Hall bar patterns and the large 2-mm square. The PMMA was removed from the five (now individual) pieces by sonication in acetone followed by soaking in 150° C anisole. Note that the diagnostic 2-mm square underwent the exact same treatment as the Hall bar devices (*i.e.*, lithography → methylation → more lithography → cleaning and separation).

At this point, the 2-mm square surface was characterized via x-ray photoelectron spectroscopy to (1) confirm complete surface passivation and (2) check for gross carbon contamination following the device fabrication work-up. If the surface was contaminated (from photoresist or CF_4 plasma etch residue), more aggressive cleaning procedures were used, such as Aleg-310 positive photoresist/residue stripper (n-methyl-2-pyrrolidone, amine, and catechol in solvent; 55° C, 10–20 min) (Mallinckrodt Baker, Phillipsburg, NJ) or 1:1:5 $NH_4OH:H_2O_2:H_2O$ (75° C, 10 min). Note that adventitious carbon was always present due to solvent, wafer handling, etc.

5.3 Spectroscopic characterization of methyl-passivated SOI devices

5.3.1 Measurement description

X-ray photoelectron spectroscopy (XPS) data were collected at room temperature in a UHV (10^{-9}–10^{-10} Torr) chamber described in detail elsewhere[2, 42]. X-rays from an Al Kα line at energy $h\nu$ = 1486.6 eV were incident to the wafer surface at 35° from the surface plane. Ejected photoelectrons were collected with a hemispherical electron energy analyzer at a take-off angle of 35° from the sample surface. Data was collected using M-probe ESCA Software version S-Probe 1.36.00. Survey scans were always taken in the energy range 0–1000 BeV (binding electron volts, or, $h\nu$ minus the photoelectron energy) to confirm the presence of only Si, C, and O (except possibly Mg from the methyl-Grignard reaction). High-resolution XP spectra of the Si 2p region from approximately 97–106 BeV were used to identify any surface oxidation as indicated by the formation of a broad SiO_x peak at ~103.4 BeV. Additionally, high-resolution scans of the C 1s region from approximately 282–289 BeV were used to identify direct C–Si bonding, if possible (dependent on the amount of adventitious carbon adsorbed to the surface). All peak fitting was done using the M-probe software. Si 2p fitting employed a 95% Gaussian and 5% Lorentzian line shape, with a 15% asymmetry. The $2p_{1/2}$ and $2p_{3/2}$ peak separation was fixed at 0.6 eV with a $2p_{1/2}$:$2p_{3/2}$ area ratio of 0.51[2, 42]. C 1s peaks were roughly fit by manually specifying the approximate peak positions and allowing the software to freely adjust all remaining parameters.

For chips used to fabricate Hall bar structures, XP spectra were collected from the photolithographically-defined 2-mm square described above. Before each scan, the x-ray spot was centered in the 2-mm square. This was made possible through the use of a fluorescent screen to identify the location of the x-ray spot relative to the square. Once the spot was located, the sample stage was translated accordingly.

5.3.2 Surface characterization data

Figure 5-5 shows a representative AFM image of a ~40-nm bonded Si(111) SOI epilayer ($n = 1\times10^{19}$ cm^{-3}) that was etched for 15 minutes in de-oxygenated NH_4F at room temperature, and Figure 5-5 shows XPS data from this surface immediately after functionalization, and after 108 hours of air exposure. The AFM image of Figure 5-5 shows triangular etch pits pointing in the $[11\bar{2}]$ direction[43] can be resolved and used to assign lattice directions as shown. The terrace width was measured to be ≈ 20 nm. For very thin (≤ 30 nm) Si devices on top of a 1–2 μm supporting SiO_2 layer, 15 minutes of NH_4F etching frequently resulted in severe thinning of the device, despite NH_4F being a very slow Si(111)

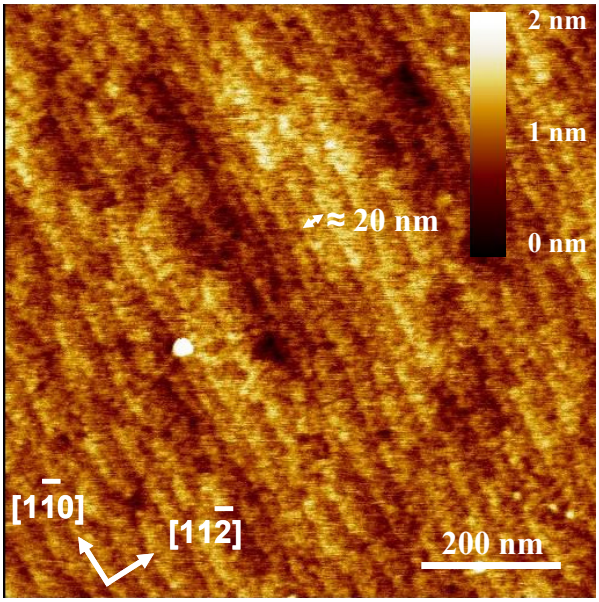


Figure 5-5. Atomic force microscopy (AFM) image of a 40-nm Si(111) epilayer etched in NH_4F.

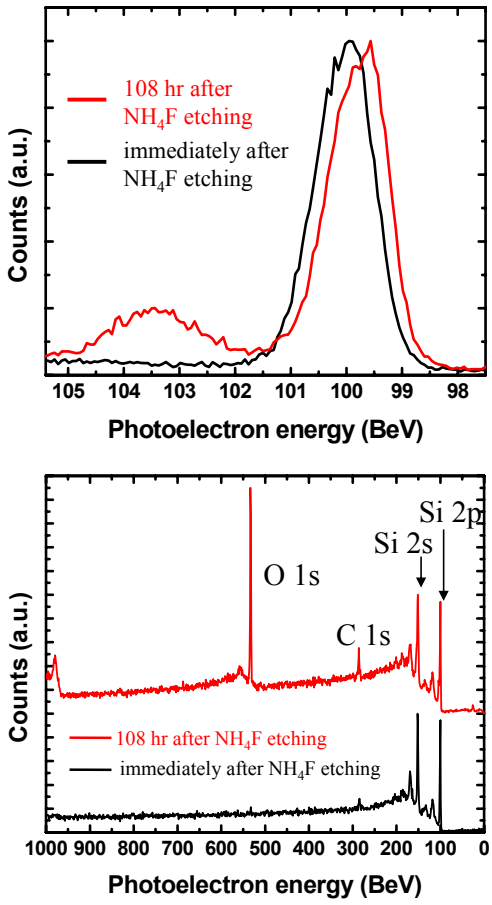


Figure 5-6 XP spectra of an H-terminated silicon epilayer. (Top) Si 2p region immediately after (black) and 108 hr after (red) NH_4F etching. Note the dramatic re-growth of surface oxide. (Bottom) Survey scans showing the presence of only O, C, and Si. The satellite peaks at lower binding energy to the Si 2s and 2p peaks are due to surface plasmon excitation. The peak at 970 BeV is characteristic of oxygen $K_1L_{23}L_{23}$ Auger emission.

etchant (etch rate ≈ 2 Å/min)[44]. A possible explanation for the enhanced etch rate may be excess dissolved oxygen in the NH_4F solution originating from the SOI SiO_2 layer. Transport of O_2 to the reactive, bare Si surface would result in rapid oxidation, followed by subsequent etching by F^- in the solution[45, 46]. Additionally, the presence of dissolved O_2 in the NH_4F solution may cause roughening of Si(111) surfaces[45], the extent of which requires further study using STM measurements. Nevertheless, a five-second 1:10 BOE:H_2O dip to remove the native oxide followed by a 4–5 minute NH_4F etch resulted in complete hydrogen termination, and robust methyl passivation of SOI surfaces was obtained with the chlorination/methylation steps described above.

To ascertain the quality of this passivation, high-resolution XP spectra of the Si 2p region were taken as a function of exposure time to air, and oxidation-resistance was taken as the figure of merit. The results of this study are presented in Figures 5-7.A and 5-7.B. Methyl-passivated SOI surfaces showed little re-growth of surface oxide, even after 108 hours (4.5 days) of exposure to ambient

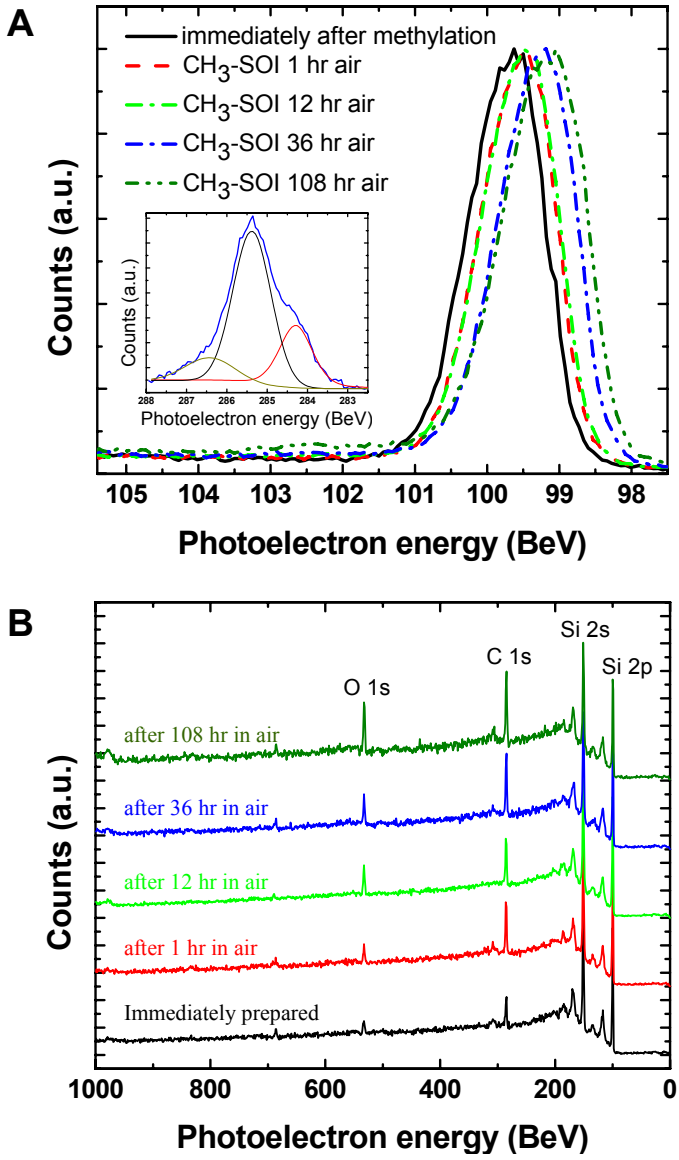


Figure 5-7. XP spectra of a 30 nm methyl-terminated SOI surface as a function of time in air. A. High-resolution scans of the Si 2p region showing very little oxidation after 108 hours in air. The noticeable shifting of the Si 2p peak to lower binding energy as a function of time may or may not be physical. This shift is seen in reported XPS data from the same instrument[2], but not for a different instrument[4]. If physical, the mechanism may be due to surface band bending and surface dipole effects[5] caused by the slow oxidation of unpassivated regions[4]. Inset. High-resolution scan of the C 1s region. Direct C–Si bonding is evidenced by the presence a side-peak shifted from the C 1s peak by 1.1 BeV to lower binding energy. **B.** Survey scans from 0–1000 BeV confirm only C, O, and Si. The growth of the O 1s peak is primarily due to adsorbed H_2O or adventitious C. This is verified by the Si 2p scan in **A**, which shows no significant surface oxidation.

air. Furthermore, follow-up XP scans on these surfaces after many months showed no significant further oxidation (not shown). This is in contrast to the H-terminated SOI surface shown in Figure 5-6, where surface oxidation is clearly evident by the presence of a broad peak at 103.4 BeV (due to formation of Si^{+}, Si^{2+}, Si^{2+} and Si^{4+} [4] species). The data of Figure 5-7.A does reveal some surface oxidation after 108 hours of air exposure, which is also observed with methylated bulk wafers. Recent work by Webb *et al*. has found this to result from the slow oxidation of isolated, inhomogeneous patches on the Si(111) surface[4]. Significantly, this study also found that slight oxidation of alkylated surfaces after prolonged air exposure resulted in no noticeable degradation of the surface's remarkable electronic properties.

The inset of Figure 5-7.A shows a high-resolution scan of the C 1s region. Although partially obscured by a ubiquitous aliphatic C 1s peak at 285.4 BeV, a shifted C 1s peak can be seen at 284.3 BeV. This shift to lower binding energy is due to direct C–Si bonding, and results from the carbon atom being negatively charged in its bond polarity, as expected from the electronegativities of C and Si (2.55 and 1.90, respectively)[5, 34].

For application to nanoelectronics, methyl-passivated SOI devices must be resistant to common microelectronic fabrication protocols and chemicals. To that end, 2-mm-square CH_3–Si(111) surfaces on SiO_2 were subjected to a host of fabrication chemicals, lithography procedures, and metal-deposition steps. XP spectra were collected before and after such treatments with re-growth of surface oxide once again taken as the figure of merit. As expected, immersion in a wide variety of solvents[47] heated to their boiling point (for 20–30 min) did not affect the passivation by any discernable amount.

Additionally, photolithography and metal deposition procedures* employing common positive-tone photoresists such as AZ-5214 (Clariant) and S-1813 (Shipley), and electron-beam lithography using PMMA did not result in appreciable oxidation of CH_3-SOI surfaces. An XP spectrum of the Si 2p region following photolithography and metal deposition (and lift-off in acetone) is shown in Figure 5-8.A for both a methyl-passivated (black trace) and untreated surface (red trace).

As expected, Figure 5-8.B (black trace) shows that one minute of diluted piranha-clean (2:1:10 H_2SO_4:H_2O_2:H_2O, ~ 100° C) resulted in oxidation of the methylated SOI surface, albeit to a significantly lesser extent than for an untreated Si surface (red trace). Aqua Regia (2:1 HCl:HNO_3, 1 min, ~100° C) treatment also resulted in significant oxidation (Figure 5-8.C). On the other hand, Figure 5-8.D shows that the popular RCA-I cleaning step (1:1:5 NH_4OH:H_2O_2:H_2O, 75° C, 10 min) did not result in appreciable oxidation of the CH_3-SOI surface. Methylated SOI was also resistant to oxidation from Aleg-310, a common photoresist stripper (n-methyl-2-pyrrolidone, amine, and catechol in solvent; 55° C, 10 min) (Figure 5-8.E).

Lithographic procedures frequently resulted in significant contamination of CH_3-SOI surfaces after metal lift-off in acetone. The signature of carbon contamination from photoresist was the presence of a shifted C 1s peak to ~ 290 BeV from the aliphatic carbon peak at 284.5 BeV, attributed to the presence of ester-bonded C atoms in photoresists and PMMA. This is clearly seen in the C 1s XP spectrum shown in Figure 5-8.F (top panel). Prolonged immersion (~1 hour) in anisole at 150° C significantly improved the surface in most cases (Figure 5-8.F, middle panel), but occasionally more-

* Note that, as described above, methyl-terminated surfaces do not come into contact with developers except where photo- or e-beam-resists are exposed.

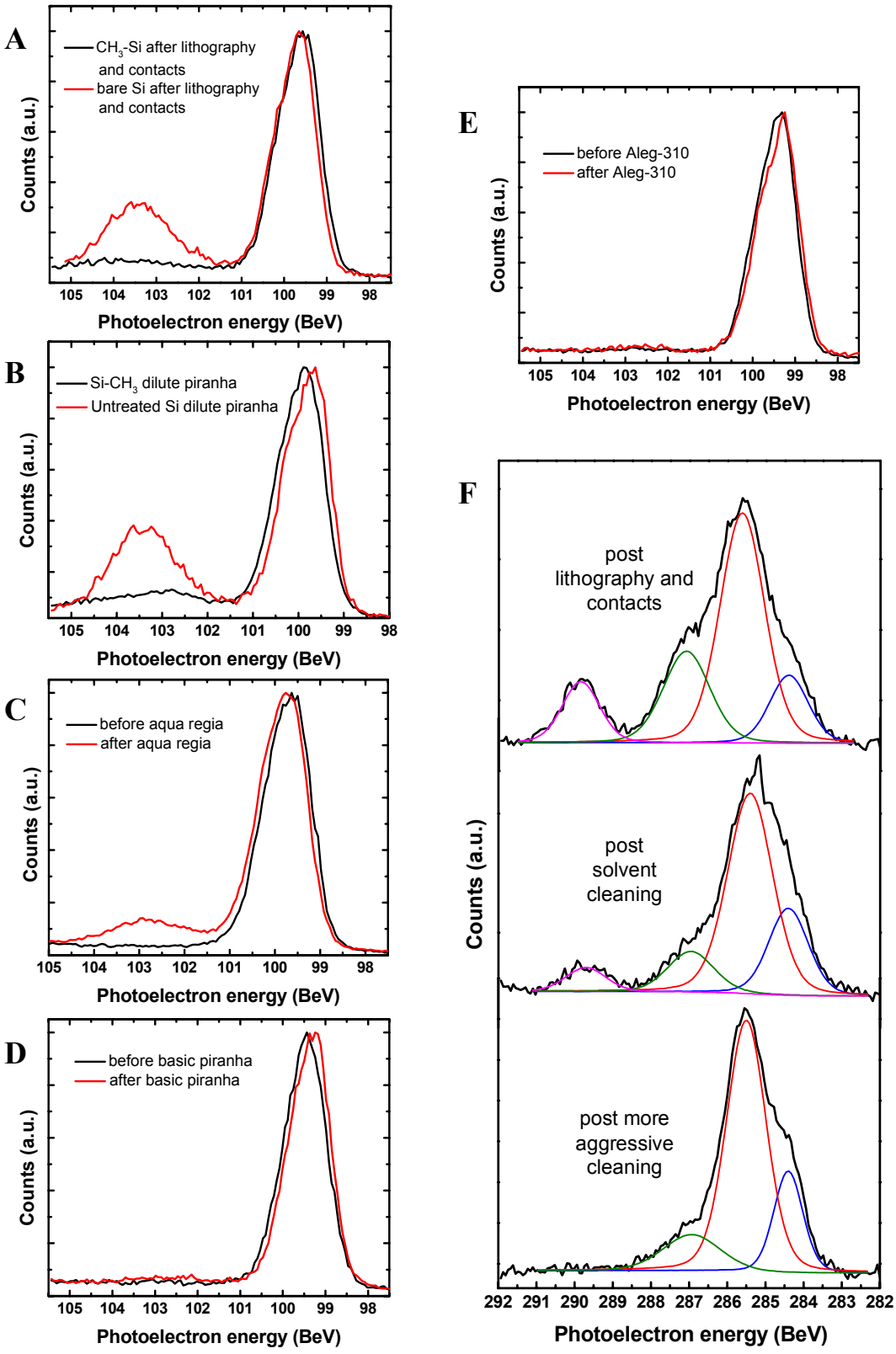


Figure 5-8. High-resolution XP spectra of Si 2p (A-E) and C 1s (F) regions from ~20-30 –nm-thick CH_3-SOI surfaces after various chemical treatments described in the text.

aggressive cleaning techniques were needed such as treatment with either RCA-I (basic piranha) or Aleg-310 (Figure 5-8.F, bottom panel).

The data in Figures 5-8.A–F show that CH_3-terminated SOI surfaces are resistant to oxidation from common micro/nanofabrication chemicals and lithographic protocols, and that devices fabricated from such surfaces should retain the excellent electrical properties of a CH_3-terminated surface.

5.4 Electrical characterization of methyl-passivated SOI devices

The previous section showed that methyl-passivated ultra-thin SOI devices remained passivated with little surface oxidation after complete microelectronic device fabrication. The studies described in this section aimed to directly measure the electronic transport parameters in such devices using variable-temperature magneto-transport measurements. By measuring electrical transport parameters, such as mobility at various temperatures, insight can be gained into the constituent scattering mechanisms.

5.4.1 Introduction to low-field Hall measurements

Measurements of the magnetoresistivity tensor in a weak magnetic field is a basic material characterization technique that enables the measurement of the Hall mobility, μ, and carrier concentration, n, separately, as opposed to zero-field resistivity measurements that only determine the product of the two. To see this, consider an n-doped rectangular

thin-film with a magnetic field, B, perpendicular to the surface. At steady state, the average rate in which an electron loses momentum due to the scattering forces within a crystal lattice is equal to rate at which it is accelerated by the external field, or, in equation form:

$$\left\langle \frac{d\mathbf{p}}{dt} \right\rangle_{lattice} = \left\langle \frac{d\mathbf{p}}{dt} \right\rangle_{field} . \tag{i}$$

In the low-field, single-carrier Drude model[48], a velocity-independent average momentum relaxation time, τ_m (the mean time between scattering events), is defined such that equation (i) can be simplified to

$$\frac{m^* \mathbf{v}}{\tau_m} = e\mathbf{E} + \mathbf{v} \times \mathbf{B} , \tag{ii}$$

where $\mathbf{v}$ is the drift velocity and m^* the effective mass. Taking the electric field, $\mathbf{E}$, to be in the plane of the thin-film (the x-y plane), equation (ii) can be simplified to

$$\begin{pmatrix} m^*/e\tau_m & -B \\ B & m^*/e\tau_m \end{pmatrix} \begin{pmatrix} J_x/en \\ J_y/en \end{pmatrix} = \begin{pmatrix} E_x \\ E_y \end{pmatrix} , \tag{iii}$$

where $\mathbf{J} = e\,\mathbf{v}\,n$ is the in-plane current density per unit cross-sectional area (= film thickness, t, × Hall bar width, w). The conductivity is given by $\sigma = en\mu$ and the Hall mobility by $\mu = e\tau_m / m^*$; thus, equation (iii) can put into the form of the magnetoresistivity tensor, $\mathbf{E} = \vec{\rho} \cdot \mathbf{J}$, with

$$\vec{\rho} = \begin{pmatrix} \rho_{xx} & \rho_{xy} \\ \rho_{yx} & \rho_{yy} \end{pmatrix} = \begin{pmatrix} 1/\sigma & -\mu B/\sigma \\ \mu B/\sigma & 1/\sigma \end{pmatrix} \tag{iv}$$

or

$$\rho_{xx} = \rho_{yy} = 1/en\mu \qquad \text{and} \qquad \rho_{xy} = -\rho_{yx} = B/en\,. \tag{v}$$

Equations (v) show that the Drude model predicts a field-independent longitudinal resistivity and a transverse resistivity that increases linearly with the applied magnetic field.

An eight-contact Hall bar geometry, shown in Figure 5-9 (on page 166), was utilized for this study because it enabled two independent four-point longitudinal voltage measurements, V_x, and a transverse (Hall) voltage measurement, V_H, at the center of the Hall bar structure. The remaining two measurement arms were not used, but were nonetheless patterned to keep the Hall bar as symmetrical as possible. From these measurements and the known dimensions of the device, the magnetoresistivity tensor components of the thin film can be calculated. This in turn enables the calculation of the Hall mobility, μ (cm^2/V s), resistivity, ρ (Ω cm), and carrier concentration, n (cm^{-3}), from equations (v).

Experimentally, a low-frequency AC or DC current was driven through the Hall bar structure and the longitudinal voltage, V_x, and Hall voltage, V_H, were synchronously measured. This enabled the calculation of ρ_{xx} and ρ_{yx} from

$$\rho_{xx} = \frac{E_x}{J_x} = \frac{V_x}{I}\frac{w}{l}t \qquad \text{and} \qquad \rho_{yx} = \frac{E_y}{J_x} = \frac{V_H}{I}t\,, \tag{vi}$$

where l is the distance between the same-side voltage measurement arms in Figure 5-9 (page 166), and I is the current. From equations (v) and (vi), the Hall mobility and carrier density were calculated from

$$\mu = \frac{|R_H|}{\rho_{xx}} \qquad \text{and} \qquad n, p = \frac{1}{e|R_H|}; \quad R_H = \frac{t}{I}\frac{V_H}{B}\,, \tag{vii}$$

where R_H is the Hall factor (= E_y / IJ_x); which was calculated by suitably averaging V_H measurements at different field and current polarities (described in the next section). The mobility (and carrier concentration) measured using this technique is qualified with the word 'Hall' because it differs from the true mobility by a scattering factor, r. The absence of this factor in the derivation above is due to the assumption of a velocity-independent mean time between collisions, τ_m. In reality, τ_m depends on the scattering mechanism (ionized impurity, phonon, etc.), and must be averaged over energy in addition to time. Further considerations give $r = \langle \tau_m^2 \rangle / \langle \tau_m \rangle^2$ where $\langle \ldots \rangle$ denotes an average over energy[49]. Fortunately, the scattering factor is close to unity ($\approx$ 0.95–1.2)[49] for the doping levels considered herein and was ignored.

5.4.2 Measurement description

Following fabrication, the Hall bar structures described in Section 5.2 were wired-bonded to a Au/plastic chip carrier and loaded into a Quantum Design Magnetic Property Measurements System (MPMS) cryostat with temperature control from 1.5 K to 400 K, and field capability of –50,000 to +50,000 Oersted. Independent longitudinal voltage measurements at two different locations of the Hall bar shown in Figure 7-8 allowed the homogeneity of the sample to be checked by comparing the two calculated resistivity values. I generally found the two resistivity measurements to agree to within ±10 percent unless there were poor Si-metal contacts, in which case I discarded the sample. It is desirable to measure the Hall voltage in the center of the Hall bar structure, as shown in Figure 5-9, because the measurement is then as far as possible from the end contacts of

the Hall bar. The proximity of the Hall bar end contacts can cause shorting of the transverse voltage, which can lead to an underestimate of the Hall coefficient. Theoretical analysis shows that if the contacts are in the middle of the Hall bar sample, and the aspect ratio of Hall bar length to width is $l/w > 3$, then the error from the contacts will be less than one percent [50]. For all the Hall bar structures tested $l/w > 7$, thus edge contacting errors should be negligible. Perturbations to the current flow and electric field pattern caused by voltage contacts were also reduced by using monolithic contact arms and making metal-Si contact at the ends of the arms[51].

Two sets of three equally-spaced contacts lie on opposite sides of the Hall bar. The distance between contacting arms is 150 μm and the distance from an end contact to a Hall voltage probe is nominally 220 μm. The Hall bar is 800 μm long and 100 μm wide, although after making electrical contacts the Hall bar length is effectively reduced to 750 μm.

5.4.2.1 DC measurements

For most of the measurements described herein, the Hall voltage signal, V_H, was three orders of magnitude smaller than the longitudinal voltage signal, V_x. Furthermore, the Hall voltage was usually offset by 'misalignment' voltage[49]. The misalignment voltage is caused by a voltage gradient parallel to the excitation current flow and is usually present even in the absence of a field, and for perfectly aligned Hall voltage probes. However, this voltage is (to a good approximation) independent of field, and was cancelled by measuring the Hall voltage at opposite field polarities and subtracting the two measurements. Likewise, thermoelectric and smaller magnetothermal-electric voltages

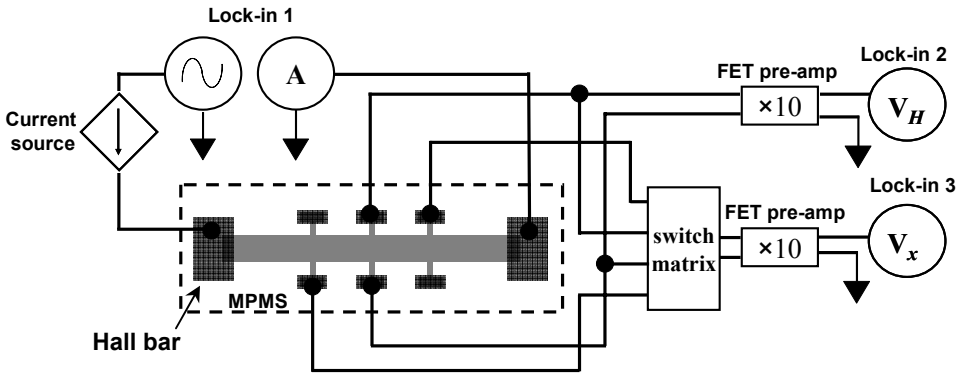


Figure 5-9. Hall measurement circuit. **For AC measurements**, an AC voltage output from Lock-in 1 (Stanford Research Systems SR-830 DSP) was used to control a current source consisting of either an operational amplifier operated in feedback or a precision resistor. For the resistor current source, the excitation current was monitored using the same lock-in. For an Op Amp current source, the excitation current was measured indirectly by using lock-in 1 to measure the voltage across a small precision resistor in series with the current (not shown). FET pre-amplifiers (100 MΩ) with a voltage gain of 10 amplified the voltage signals before they were measured by lock-in's 2 and 3. A switching matrix (Keithley 707A) was used to measure two longitudinal voltages with one pre-amplifier and lock-in. Note that the signal from V_H was much smaller than V_x, so an additional lock-in was dedicated for measuring V_H to avoid noise from the additional wiring of the switching matrix. **For DC measurements** lock-in 1 was replaced by a Keithley 2400 SourceMeasure unit and lock-in 3 was replaced by a Keithley 2182A Nanovoltmeter.

(Ettingshausen and Righi-Leduc effects)[52] were eliminated by reversing the current polarity and subtracting the measured Hall voltages. The resistivity was measured at zero-field on opposite sides on the bar and averaged. The equations for calculating transport parameters using the DC method are as follows:

Resistivity $$\rho_{1,2} = \frac{V_x(+I) - V_x(-I)}{2I}\frac{w \times t}{l} \quad , \qquad \rho_{avg} = \frac{\rho_1 + \rho_2}{2}$$

Hall factor $$R_H = \frac{\left(V_H(+B;+I) - V_H(+B;-I)\right) - \left(V_H(-B;+I) - V_H(-B;-I)\right)}{4I}\frac{t}{B}$$

Mobility $$\mu = \frac{|R_H|}{\rho_{avg}}$$

Carrier concentration $$n, p = \frac{1}{e|R_H|}$$

A constant current of 100 nA to 1 μA was used for DC measurements, and was adjusted with temperature to avoid sample heating and nonlinearities in the current-voltage response. (This was tested by doubling and/or halving the current and ensuring the voltage followed accordingly.) The applied magnetic field magnitude ranged from 3–5 T, depending on the Hall voltage signal level and the sourced current. (See Figure 5-9.)

5.4.2.2 AC measurements

DC measurements from samples doped below ~4×10^{18} cm^{-3} often became unreliable at lower temperatures due to decreased signal-to-noise from the need to use low current levels (which were required to avoid joule-heating of resistive samples[*]). Thus, many of the Hall measurements were made using low-frequency (≤ 13 Hz) and low current (1–10 nA) AC measurements with the measurement circuit shown in Figure 5-9. (The figure caption describes the electrical measurement in more detail.) The advantages of the AC technique for Hall measurements are: (1) Increased signal-to-noise via synchronous detection, and (2) elimination of thermal and magnetothermal voltage offsets. However, AC measurements create their own spurious effects, which are much more difficult to diagnose than are DC measurements, due to the involvement of phase. Accordingly, AC measurements were checked where possible with DC measurements. From 100 K to 400 K, AC measurements were found to differ from DC measurements in most cases by less than approximately five percent.

[*] Near this doping the Si:P alloy system undergoes a semiconductor-to-metal transition[49]

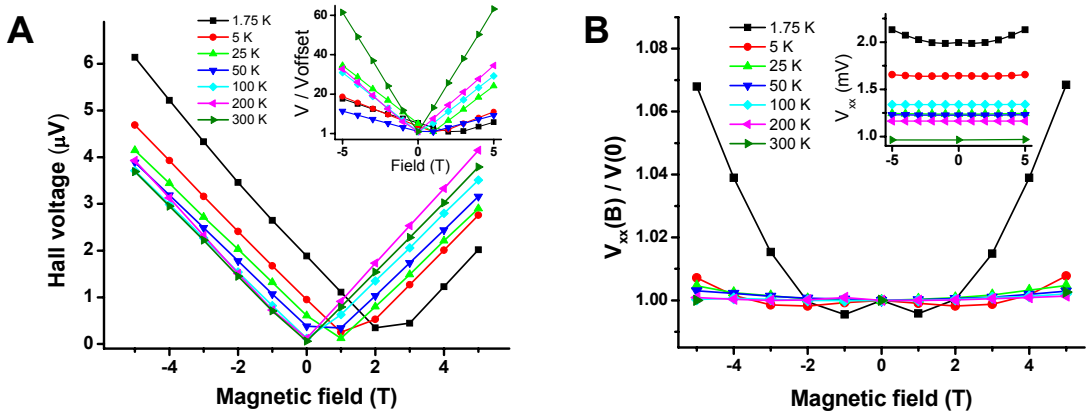


Figure 5-10. Hall and longitudinal voltages versus magnetic field from a 30-nm Hall bar. A. Hall voltage magnitude vs. field at various temperatures down to 1.75 K. The misalignment voltage is the residual voltage of the lowest point on the V_H vs. B plots and becomes smaller as the temperature increases and the device becomes less resistive. The inset shows the Hall voltage normalized by the offset voltage. **B**. Longitudinal voltage normalized by the zero-field value. The voltage is nearly independent of field down to ~5 K where characteristic B^2 behavior emerges due to departures from the single-carrier Drude model of magnetoresistance. Inset shows absolute voltage levels.

To eliminate the misalignment voltage, which is synchronous with the source current, V_H was calculated from the slope of V_H vs. B using two field points at each temperature. This eliminated the misalignment voltage as long as V_H was linear in B and the misalignment voltage was not field dependent. (This is also an implicit requirement for the validity of the single-carrier Drude model described above.) To that end, V_H and V_x vs. B scans were initially taken at a relatively small number of temperature points to establish the temperatures and field strengths where this is true. Figure 5-10 shows typical data down to 1.75 K.

Although a rather large field of 5 T was frequently used to increase the Hall voltage signal with respect to background (which was important for DC measurements), such fields were still within the low-field regime for the devices measured herein since

the measured mobilities were generally less than 300 cm^2/V-s, giving the low-field criterion* as $B < 1/\mu \approx 1/(300\ cm^2/V\text{-}s) \approx 30$ T.

5.4.3 Electrical characterization data

In this section, I will present preliminary data from methyl-passivated ultra-thin SOI devices. The majority of these devices are characterized by Si epilayers of approximately 10–25 nm thick. Figure 5-11 shows data from very highly doped ~20-nm thick CH_3-passivated SOI devices that were measured using DC techniques. This was possible because the samples were very highly-doped, resulting in metallic behavior down to 1.75 K. The observed metallic behavior is caused by the formation of phosphorus impurity banding, resulting in a vanishing dopant ionization energy[53, 54]. This behavior is clearly evident from the resistivity-vs.-temperature plot of Figure 5-11.A. (Although not shown, the measured carrier concentration displayed little temperature dependence, as expected.) The temperature dependence of the mobility shown in Figure 5-11.B is indicative of weak phonon scattering with a power-law temperature dependence, $\mu \sim T^s$, with temperature exponent $s = 0.34 \pm 0.03$ for the n-type CH_3 SOI device from 100–300 K, and $s = 0.24 \pm 0.04$ for the p-type CH_3 SOI device from 77–300.

For moderately-doped devices (approximately l–4×10^{18} cm^{-3}), the amount of time the device remained in the PCl_5 solution during the chlorination reaction was found to be an important parameter determining device mobility. This is most likely the result of

* The low-field criterion amounts to the requirement of non-closing cyclotron orbits. The frequency of a cyclotron orbit is $\omega_c = eB/m^*$, and an electron will be scattered before completing an orbit provided $\omega_c \langle \tau_m \rangle < 1$ radian, or $B < 1/\mu$.

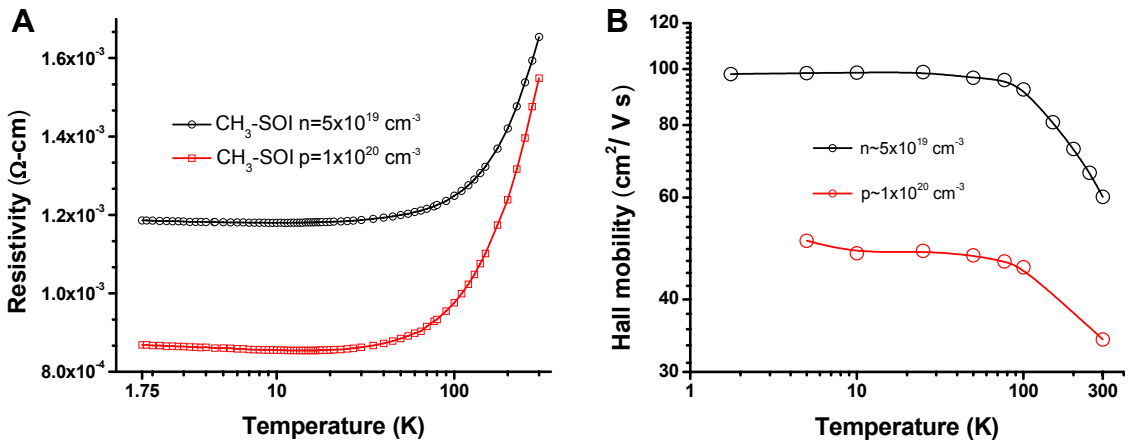


Figure 5-11 Resistivity and Hall mobility of highly-doped CH_3–SOI devices. **A**. Resistivity vs. temperature data showing clear metallic-like behavior due to high doping and impurity band formation. **B**. The mobility characteristics of n- and p-type CH_3 SOI devices indicating phonon scattering of charge carriers in impurity bands as the dominant scattering mechanism. As expected, the p-type doped sample mobility is roughly half the n-type sample mobility. Both devices were chlorinated via 30 minutes in PCl_5.

significant device thinning[1, 55] and etch-pit formation from the PCl_5 chlorination reaction, which is expected to have an enhanced effect on very thin epilayers, such as those studied here. This is in accord with recent work by Cao *et al.*[56], where STM measurements determined that wet-chemical chlorination of bulk Si(111) surfaces with PCl_5 resulted in significant etch-pit formation.

Supporting this hypothesis is the data of Figure 5-12, which displays the measured mobility of ~20-nm-thick CH_3-SOI devices as a function of PCl_5 chlorination time with the reaction temperature at ~90° C. Because the devices had different doping levels (from roughly $1–4\times10^{18}$ cm^{-3}), the measured mobility was normalized by the bulk mobility. The data suggests that short PCl_5 chlorination times are required to achieve good electrical properties from CH_3-terminated SOI devices using PCl_5 as the chlorination reagent. (Lower reaction temperatures and longer reaction times are expected to yield similar results). To verify that the surfaces used to obtain the data

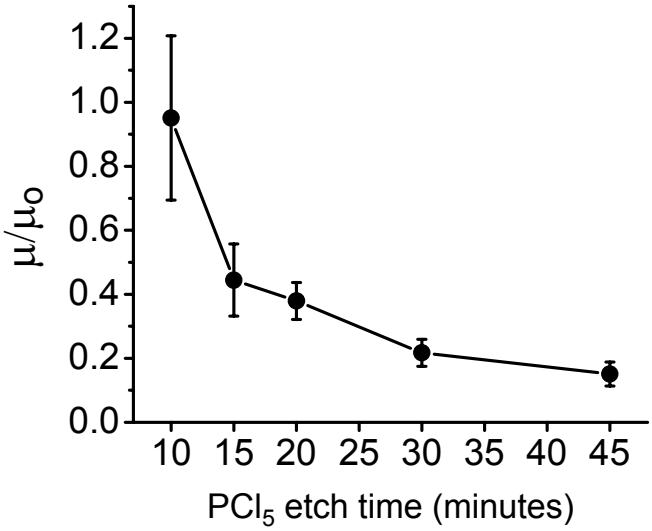


Figure 5-12. Normalized mobility as a function of PCl_5 chlorination time. The normalization constant, μ_o, is the bulk mobility for the device doping, which ranged from n=1–6×10^{18}. The uncertainty in these measurements is primarily due to uncertainty in the device thickness after functionalization, which in turn leads to uncertainty in the normalization factor. The PCl_5 reaction temperature was ~90° C.

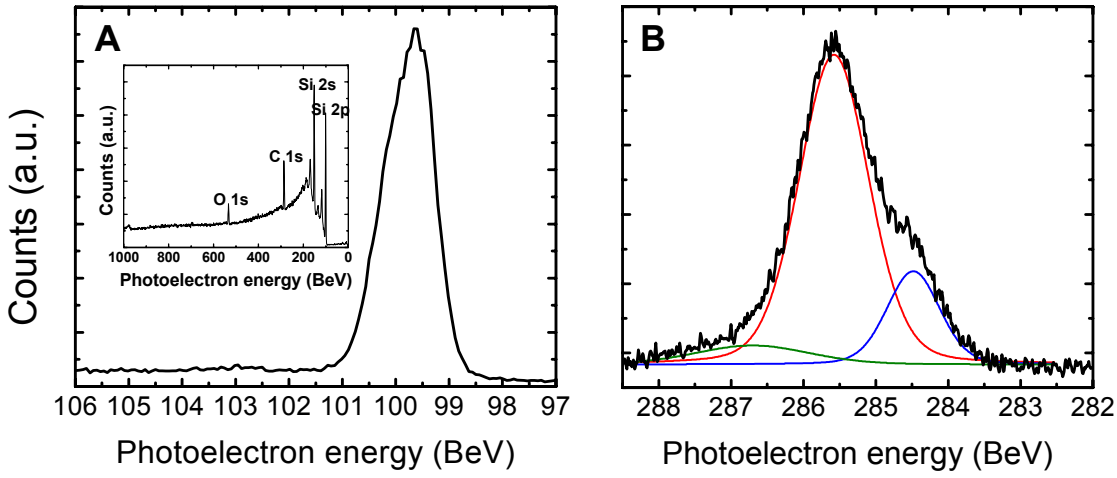


Figure 5-13. XP spectra of an approximately 20-nm-thick CH_3-SOI device chlorinated by a 10-minute immersion PCl_5. A. High-resolution scan of the Si 2p region showing little oxidation after ~24 hours of air exposure. Inset, survey scan showing only C, O, and Si. **B**. High-resolution scan of the C 1s region showing direct C–Si bonding evidenced by a chemical shift of the C 1s peak to lower binding energy (blue trace). The PCl_5 reaction temperature was ~90° C.

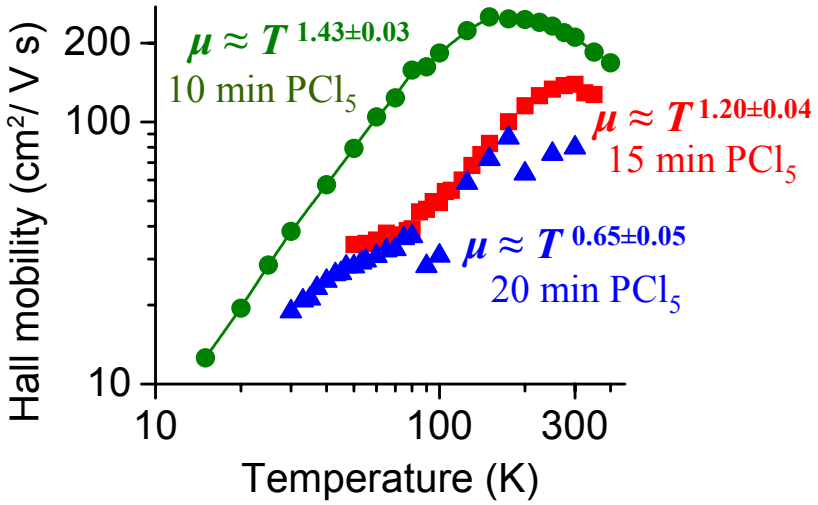


Figure 5-14. Hall mobility vs. temperature. Black circles: ~20 nm CH_3–SOI, n=2×10^{18} cm^{-3}, 10 min PCl_5. Red squares: ~20 nm CH_3–SOI, n=1×10^{18} cm^{-3}, 15 min PCl_5. Blue triangles: ~20 nm CH_3–SOI, n=2×10^{18} cm^{-3}, 20 min PCl_5.

shown in Figure 5-12 were methyl passivated, XP spectra were collected from the same chips on which the devices were fabricated. Figure 5-13 shows XP spectra from a device chlorinated from 10 minutes in PCl_5 at ~ 90° C.

Figure 5-14 shows the measured mobility vs. temperature characteristics from three moderately-doped devices (n = 1–2×10^{18} cm^{-3}) after 10, 15, and 20 minutes in PCl_5 solution at ~90° C. The data shows the mobility is dominated by lattice interactions, such as ionized impurity scattering at low temperature, and phonon scattering at high temperature, as expected for non-degenerately doped Si[19]. The device chlorinated with a ten-minute immersion in PCl_5 (black circles) displayed the highest mobility value (~210 cm^2/Vs at 300 K), which is slightly better than the bulk value for comparable doping. The low-temperature mobility of this device displays a temperature exponent of s = 1.43 ± 0.03 indicating that ionized impurity scattering (which theoretical considerations predict depends on temperature as $\mu \sim T^{3/2}$) is the dominant mobility reduction mechanism in

this device[57]. Thus, the mobility of this device displays bulk-like behavior, where ionized impurity scattering is the dominant contribution to the temperature dependence of the mobility * (at low temperature). The other two devices show lower temperature exponents: $s = 1.20 \pm 0.04$ (red squares, 15 min PCl_5) and $s = 0.65 \pm 0.05$ (blue triangles, 20 min PCl_5). This may be due to increased contributions from other scattering mechanisms, perhaps related to the surface, such as surface roughness scattering[14] due to increased etch pit density, and/or neutral impurity scattering. The latter has been observed to be important at low temperatures with a temperature exponent of $s = 0.5$ in bulk samples[57].

5.5 Concluding remarks

This chapter presented research directed towards chemically controlling the surface of Si(111)-on-insulator epilayers using a modified chlorination/methylation protocol. The surface characterization data is fairly complete, and shows that electronic devices with oxide-free surfaces can be prepared from ultra-thin SOI epilayers using standard microelectronic fabrication protocols. The electronic measurements suggest the various wet-chemical processing steps employed to alkylate the surface of thin-film devices

* The total mobility, μ_T, due to an assortment of independent scattering mechanisms, can be written as $1/\mu_T = \sum_s 1/\mu_s$, where $\mu_s \sim T^s$. Thus, the presence of surface scattering mechanisms (and/or other possible scattering mechanisms), each with a different temperature exponent, s, alters the measured temperature-dependence of the mobility from $\mu \sim T^{1.5}$ (the expected temperature-dependence for moderately-doped bulk devices).

should be used with caution to avoid degrading the overall electronic properties of the device.

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