Chapter 3

Demultiplexing ultra-dense nanowire arrays

3.1 Introduction

One of the central challenges of both nanoscience and nanotechnology is the selective addressing of and interaction with individual nanostructures at high densities (*i.e.*, densities limited only by the intrinsic size and packing of the nanostructures); in the absence of a resolution to this problem, many of the potential benefits of these emerging fields will remain unrealized. Specifically, this challenge manifests over a range of problems varying from coupling conventional electronics to novel nano-scale memory and logic architectures[1], to addressing of single nanoparticles for applications in quantum computing[2], to construction of high-density biomolecular sensor circuits[3, 4], to name a few. Within the field of nano-electronics, this challenge can be framed as the ability to fabricate and address circuits that have characteristic wire dimensions and pitches that are smaller than the resolution achievable through lithographic patterning. For instance, I describe in Chapter 4 a novel molecular electronic memory circuit fabricated from crossed arrays of nanowires (NWs) that is nearly two orders of magnitude denser than conventional circuitry. However, the lack of a robust technology to selectively address

individual NWs from within such an ultra-dense array reduces the effective density of the memory circuit to that of conventional (lithographically-defined) circuitry.

The first aspect of this challenge, which consists of patterning and assembling NWs at ultra-high densities, has been achieved by several groups. Methods have included the assembly of catalytically-grown[5] NWs with the use of Langmuir-Blodgett techniques[4, 6, 7], harnessing competing interactions (*i.e.*, long-range Coulombic repulsions and short-range van der Waals attractions) to control NW length and pitch[8, 9], and, as described in detail in Chapter 2, using molecular beam epitaxy (MBE)-grown $GaAs/Al_xGa_{(1-x)}As$ superlattices as templates for depositing and subsequently transferring NWs onto thin-film substrates[10, 11].

Architectural concepts for meeting the second aspect of this challenge, which consists of electrically addressing (demultiplexing) individual NWs that are patterned at sub-lithographic densities, have also been proposed, but not yet implemented. The key objectives are three-fold. First, the demultiplexer architecture must bridge from the micrometer or submicrometer dimensions achievable through lithography to the few-nanometer dimensions achievable through alternative patterning methods. Second, the architecture should allow for the addressing of large numbers of NWs with small numbers of micrometer or submicrometer wires. Third, the manufacture of the multiplexer should be tolerant of fabrication defects.

Proposed demultiplexer architectures[12] have been based on combining crossbars[1] (NWs crossed by lithographically patterned demultiplexing wires)[13] with multi-input binary tree decoders[14]. Binary tree decoders, by their very nature, exhibit order $2\times\log_2(N)$ scaling, where N is the number of output NWs and $2\times\log_2(N)$ is the number of input

demultiplexing wires needed to address the NWs. Because each wire among a pair of input wires addresses one-half of the output NWs (Figure 1.A), 2^n NWs can be addressed by n input-wire pairs. This allows a small number of input wires to uniquely address an exponentially large number of NWs. In practice, demultiplexers for addressing very dense arrays of NWs require additional input wires above the theoretical minimum of $2\times\log_2(N)$, due to fabrication constraints. However, the number of additional input wires increases only linearly as fabrication tolerances are increased for the optimized structure described in this work. As will be discussed in the next section, this makes the binary tree demultiplexer very tolerant to alignment and manufacturing defects.

3.2 Demultiplexer architectures and alignment tolerance

Kuekes and Williams[15] were the first to describe a scheme for bridging microscale and nanoscale wires with a diode- or resistor-based decoder that utilized randomly deposited gold nanoparticles sandwiched within a crossbar of microscale address wires crossing the NW array. Although they demonstrated that $5\times\log_2(N)$ 'large' wires should be sufficient to address a dense array of N NWs, their technique required non-standard fabrication procedures and extensive testing to identify unique NW addresses. DeHon, Lincoln, and Savage[12] described a more complex architecture for addressing N NWs using no more than $2.2\times\log_2(N) + 11$ address wires. Their scheme utilizes field-effect gating of NWs by a microwire demultiplexer that allows tighter address encoding, and is compatible with conventional microelectronic fabrication procedures. However, their scheme requires control over the doping profile along the axial dimension of the NWs. Such NWs have

been recently realized experimentally[16-18], and Lieber's group has used them to demonstrate a demultiplexer that bridges fabrication methods (*i.e.*, self-assembly versus lithographic patterning), but not length scales[19, 20]. Both of these demultiplexing schemes are based upon placing a number of control regions (gates) on the surface of the NWs. An individual NW, which is initially in the non-conducting state, will conduct only when all of the control regions are field- or voltage-addressed; that is, it is the logical equivalent of a multi-input AND gate. (Conversely, demultiplexed NWs described herein conduct only when they are not addressed; *i.e.*, the control regions amount to a multi-input NOR gate.) While both architectures are tolerant of a certain amount of randomness in their fabrication process and both exhibit logarithmic scaling to allow a few inputs to address many NWs, they are required to be more complex than the architecture described below due to the stochastic dimensions of the NWs they function to address. How precisely the dimensions of the NW array (*i.e.*, NW diameter, length, pitch, etc.) can be controlled determines how much additional complexity is required from the NWs' electrical properties or from the demultiplexer architecture to facilitate unique addressing of each NW within an array.

Most NW fabrication procedures (including those described above) only approximately control NW diameter, pitch, and length. Proposed demultiplexing concepts then require a combination of sophisticated NWs (*i.e.*, NWs in which the doping is controlled along the axial dimension as described above) and demultiplexers with several additional (redundant) address lines. Conversely, the superlattice NW pattern transfer (SNAP) technique, described in detail in Chapter 2, permits the fabrication of NWs with precisely controlled NW width and pitch, and this substantially eases the requirements of

the NWs' electrical properties and on the demultiplexer architecture. Rather than requiring the demultiplexer to bridge fabrication approaches and dimensions, it only has to bridge dimensions. The highly ordered nature of SNAP-fabricated NW arrays enables the development of a straightforward field effect transistor (FET)-based demultiplexing architecture that uses traditional microelectronic (lithographic) processing.

The FET-based binary decoder architecture used in this work (in conjunction with SNAP-fabricated NWs) is a defect-tolerant design that can allow for large margins of error in its implementation and still remain fully functional. This architecture provides at least partial solutions to two issues: 1) alignment of the submicrometer demultiplexer features with the nanoscale features of a NW array, and 2) the use of large demultiplexer feature sizes and feature pitches to address a NW array that is characterized by a substantially smaller (but tightly defined) NW width and pitch. As described in the paragraphs below, redundancy can be built into the binary tree decoder architecture to significantly ease constraints in lithographic patterning and alignment of the decoder with respect to the NW array. Although there are more subtle constraints in the placement of the smallest gate structures with respect to individual NWs in the array, the highly ordered nature of SNAP-fabricated NWs allows the translation of this constraint into an equivalent constraint on the relative placement of gate structures with respect to each other within the decoder pattern. Such relative alignment within the decoder pattern can be readily achieved. Details of a scheme to affect this translation are briefly considered in Section 3.4. I will now turn to a discussion of the alignment tolerance afforded by the synergistic combination of SNAP-fabricated NWs and binary tree decoders, using Figure 3-1 as a guide.

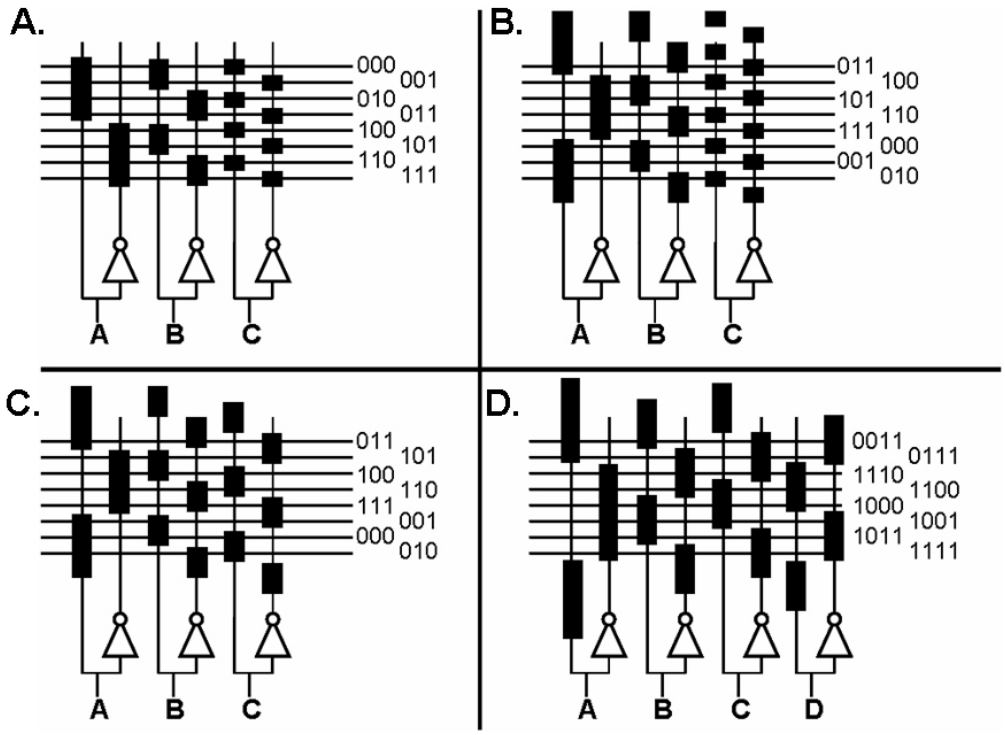

Figure 3-1. The operation of a NOR logic binary tree demultiplexer with varying fabrication constraints. A-D. The NWs are represented by eight horizontal wires, and the demultiplexer by three vertical complementary wire pairs. The operation of a complementary wire pair may be understood by considering an input address of '1' to wire pair A. The left wire is sent high by this address, and the right wire is sent low. For an input address of '0', the reverse is true. Regions where the gates interact strongly with the underlying NWs are shown as bars. When a NW passes under a bar that is connected to a wire in the high state, that NW is deselected (gated). The input address that selects each NW is indicated next to the NW. **A**. A standard binary tree demultiplexer; note that every MW pair turns off half of the NWs it contacts. **B**. A binary tree demultiplexer in which the binary tree pattern is not registered with specific NWs, and extends beyond the limits of the NW pattern. Note that the addresses are no longer sequential. **C**. The binary tree pattern of gate electrodes is shown at twice the pitch and twice the feature size of the NW array. Note that $2\times\log_2(N)$ address wires are still need to address N nanowires. **D**. The binary tree pattern of gate electrodes is shown at three times the pitch and three times the feature size of the NW array. Note that an additional pair of address wires is needed and so half of all address values are inactive.

3.2.1 Alignment tolerance through architecture

Alignment along the length (*x*-axis) of SNAP-fabricated NWs is relatively straightforward since such NWs can be extremely long (typically millimeters). Precise alignment along the perpendicular (*y*-axis) direction, however, is more difficult. A partial solution to this problem is to fabricate the binary tree of the demultiplexer with a repeating pattern, the period of which is equal to the width of the NW array. In this fashion, the decoder pattern will extend beyond the boundaries of the array (Figure 3-1.B). If, for example, the decoder pattern misses its intended position on the NW array by 500 nm, causing the top 500 nm of addresses to miss their mark, the addresses are simply repeated at the bottom of the array. The decoder pattern can be fabricated to an arbitrary length, giving any amount of *y*-axis tolerance desired. The cost of giving up absolute demultiplexer alignment is knowledge of which NW corresponds to which demultiplexer address. However, it is still possible to know that every NW has a unique address.

The constraints on rotational alignment are tighter than for translational alignment since small deviations of the decoder pattern from 90° (with respect to the *x*-axis) can result in a NW shifting from its intended decoder address to that of its neighbor. Fortunately, angular alignment of the decoder pattern relative to the NW array can be accomplished with high precision. This is primarily because the SNAP technique is capable of producing very straight arrays of NWs over millimeter length scales, which can readily be aligned to using lithographic techniques. Nonetheless, if rotational alignment is imperfect, extra input wire pairs at the smallest gate-pitch and slightly offset from each other can be used to distinguish NWs without unique addresses.

3.2.2 Feature size tolerance through architecture

The second challenge towards bridging the dimensions from the nanometer features of a NW array to the sub-micrometer features of the demultiplexer revolves around the limits of the lithography used to define the demultiplexer binary tree features. For the binary decoder depicted in Figure 3-1.C, the narrowest-pitch gate patterns on the address wires are at twice the pitch of the output wires, and there is no need for redundant address lines (*i.e.*, the scaling is exactly $2\times\log_2 N$ address wires for N NWs). In reality, addressing an array of narrow-pitch NWs (the SNAP-fabricated NWs described in this work are at ~30-nm pitch) with large repetitions of gates at twice the NW pitch would be exceedingly difficult and certainly not practical. However, the gate electrodes may be fabricated at a pitch that is m times the NW pitch, where m is an integer. This is shown in Figure 3-1.D for $m = 3$. This requires an additional input wire pair with the same gate periodicity but offset by a single NW pitch. Note that using any three out of the four input wire pairs does not produce a set of unique addresses for the eight NWs shown – all four are needed. This type of alignment, in which the gates are aligned to one another with high precision but not aligned with the underlying NW pattern, is practical to achieve. However, there are penalties associated with adding additional wire pairs (besides the need to fabricate more input wires). Each additional address pair of demultiplexing wires reduces the number of good addresses by half. This is illustrated in Figure 3-1.D in which an additional pair of address lines is needed to uniquely address each NW in the array, but only half of the input addresses actually identify a wire; *e.g.*, there are $2^4 = 16$ addresses but only eight wires. Thus, the circuit must be tested to discover the good addresses and once they are found they must be stored in memory. Since the number of

good addresses is nominally the number of NWs to be addressed, only a relatively small amount of memory is required. For instance, a NW crossbar memory circuit (such as described in Chapter 4) fabricated from two NW arrays of N NWs each would yield $N \times N$ bits of storage requiring about $N \times \log_2 N$ bits to store the good NW addresses. A one-megabit memory circuit ($N = 10^3$) requires about 1 percent of its bits to store the good NW addresses, while a 10-gigabit memory ($N = 10^5$) requires about 0.01 percent of its bits to store the good NW addresses. On the other hand, finding the good addresses in the first place requires testing the circuit, with the amount of testing increasing significantly as additional address wire pairs are needed.

3.3 FET-based demultiplexing of SNAP-fabricated NW arrays

In what follows, I will describe the research of my co-workers and me to demonstrate a field-effect-based demultiplexing scheme that is tolerant of manufacturing defects, has no serious restrictions in terms of the wire size and pitch of the demultiplexer structure, and utilizes $2 \times \log_2(N) + R$ microwires to address N NWs, where R (for redundant address lines) is zero or a small integer. This scheme does not require control over the axial doping profile of the underlying NWs, but can take advantage of the readily achieved vertical doping profiles described in Chapter 2. It is optimized (*i.e.*, R is small) for NW arrays in which the NW pitch and width are precisely controlled, such as the case for NWs fabricated using the SNAP method described above. The scheme is based on NOR logic; that is, the only NW that is not field-addressed is the one selected (Figure 3-1).

The demultiplexer concept is shown in Figure 3-2, in which 32 (= 2^5) NWs are addressed with five pairs of (drawn) submicrometer wires. Note that the binary tree pattern extends above and below the NW array to ease the lateral alignment requirements. As long as the

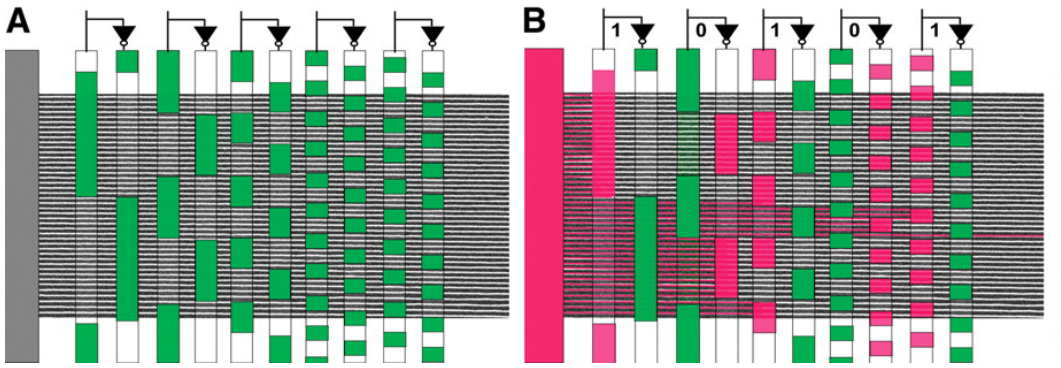

Figure 3-2. **The nanowire demultiplexer, drawn over an electron micrograph of 2^5 (= 32) silicon nanowires. A**. All NWs are ohmically contacted to the left electrode. A binary tree pattern consisting of five complementary pairs of large wires is shown. The green regions correspond to areas in which a voltage applied to the top (metal) wires can reduce the conductivity of the NWs through field-effect gating. All multiplexer features are larger than the NW features. **B.** A voltage applied to the left electrode raises all NWs to that voltage level. A single NW is selected by applying the input address '1 0 1 0 1'. Application of a voltage onto a given wire pair sends one wire high and the other low. The resistance of NWs that pass under a voltage-gated (red) region is increased. Only a single NW (colored red across the entire structure) remains in the high-conducting state.

multiplexer pattern is oriented perpendicular to the NW array, and the NW pitch and width dimensions are well defined, the circuit will be functional. As described above, the cost associated with giving up lateral alignment precision is the knowledge of exactly which NW is selected by a given input address. For example, the binary address '1 0 1 0 1' utilized in Figure 3-2 corresponds to the decimal address 21, but it is the 28th wire from the top that is selected. In practice, one usually doesn't need to know the physical location of the actual NW, just the address of that NW, and so this 'cost' is not significant for most applications. Also notice that the smallest-patterned binary tree feature sizes and

pitches are significantly larger than the smallest corresponding dimensions within the NW array (although $R = 0$ for the example of Figure 3-2). This aspect of the architecture makes it particularly amenable to manufacturing processes. For example, the dimensions of the multiplexed control wires are well suited to micro-imprint molding, a relatively high-throughput lithographic technique[21].

Development of the demultiplexer architecture described here proceeded in two stages: first by selectively addressing lithographically patterned NWs, and second by selectively addressing small groups of NWs patterned at sublithographic dimensions. For both cases, the key elements of the structure of the multiplexer are illustrated in Figure 3-3. The goal of this structure is to achieve voltage gating on one NW (NW_G) and to minimize voltage gating on an adjacent NW (NW_I), and this requires careful selection of both low-κ and high-κ dielectric materials. For the high-κ dielectric, HfO_2 was chosen because it has a high dielectric constant ($\kappa = 25$), it forms an insulating film on Si that is stable to high temperatures[22], interdiffusion between Si and Hf is not observed[23] (as it can be for other high-κ dielectrics[23]), and methods for growing very thin films of HfO_2 exist. Finally, HfO_2 has been shown to be an effective gate dielectric for nanotube[24, 25] and NW[26] field-effect transistors. For the low-κ dielectric, we chose SiO_2 ($\kappa = 3.9$) because of the ease of fabricating such films.

Figure 3-4 shows data from a demonstration circuit in which ten relatively large Si wires (doping, $n = 5\times10^{18}$ cm^{-3}) are uniquely addressed. For this circuit (in the context of Figure 3-3), W = 200 nm and P = 1000 nm. The thickness of the SiO_2 low-κ dielectric

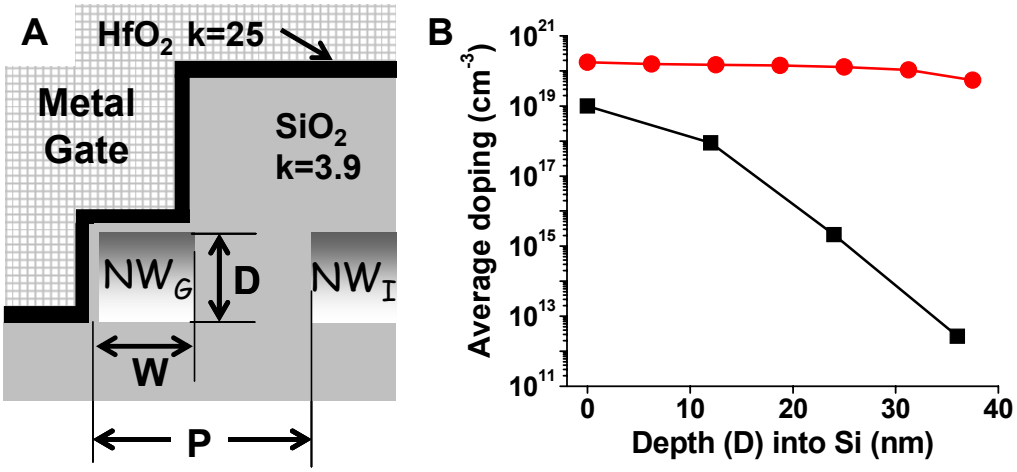

Figure 3-3. A. Side view schematic of the demultiplexer. Two NWs are shown in an end-on view, and D, W, and P refer to the depth, width, and pitch of the NWs. NW_G and NW_I refer to voltage gated and isolated NWs. The HfO_2 high-κ dielectric film is typically 3–6 nm thick, while the SiO_2 dielectric is 50–100 nm thick. Note that for small P values, P determines the distance of the NW_I from the gate electrode, and hence the gating selectivity. The shading of the NWs represents the doping profile. **B.** Measured doping profile through the silicon-on-insulator wafers from which the NWs are formed. Two modes of doping are illustrated: drive-in doping (red circles), which produces a uniform doping level through the depth of the NWs, and gradient doping (black squares), which produces a rapidly decreasing dopant density, and is utilized for demultiplexing high-conductivity NWs.

(t = 100 nm) largely determines the selectivity (*i.e.*, the selected NW/deselected NW current ratio). This is seen by considering the capacitances (per unit area) between a given NW and the gate. The total capacitance of NW_G is given by the series combination of the wire native oxide (thickness t = 1–2 nm) and the HfO_2 dielectric ($t \approx$ 5 nm), which is

$$C_G \approx \varepsilon_o \left(\frac{t_{HfO_2}}{\kappa_{HfO_2}} + \frac{t_{native}}{\kappa_{SiO_2}} \right)^{-1} \approx \varepsilon_o \left(\frac{5}{25} + \frac{1.5}{3.9} \right)^{-1} = 1.7 \varepsilon_o \, \mathrm{nm}^{-1}, \qquad (1)$$

while the total capacitance of NW_I has two contributions in parallel. NW_I is coupled to the gate horizontally through the P–W thick (800 nm) SiO_2 dielectric (ignoring the relatively small series contributions by the HfO_2 layer and the NW_I native oxide) and

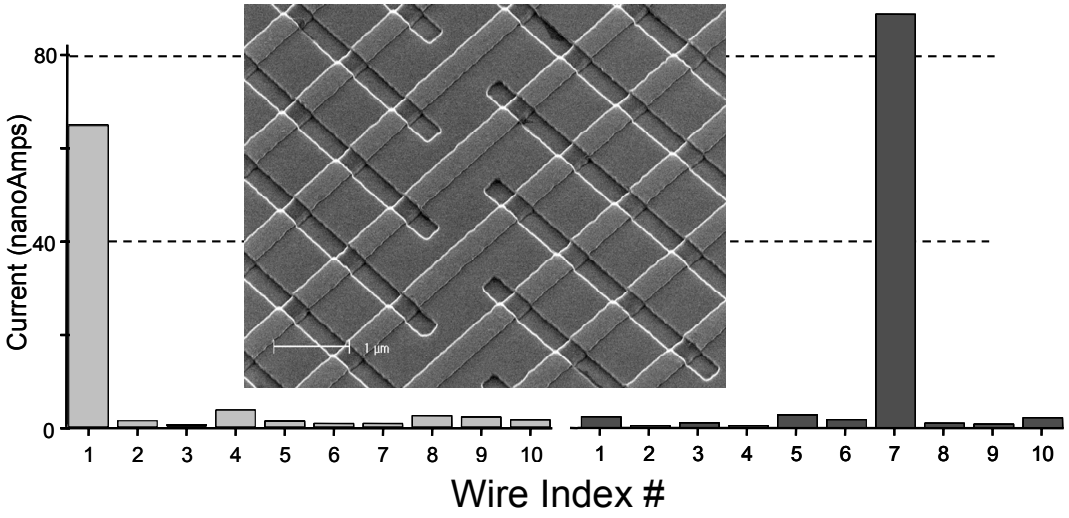

Figure 3-4. A demultiplexer constructed on a test circuit of 10 Si wires, each 200 nm wide, patterned at 1-µm pitch. The inset shows the gating electrode structure (before deposition of the gate electrodes) that was patterned on top of the underlying wire array. Results illustrating the operation of this circuit are shown in the two bar graphs, in which individual wires were maintained in the high-conductivity state while all other wires were deselected through appropriate input addressing.

vertically through the SiO_2 dielectric thickness (again ignoring smaller series combinations). Thus, the total capacitance of NW_I is given by

$$C_I \approx \kappa_{SiO_2}\varepsilon_o\left(\frac{1}{t_{SiO_2}}+\frac{1}{\mathrm{P}-\mathrm{W}}\right). \tag{2}$$

For the NW array of Figure 3-4, C_I is dominated by the first term of equation (2) which gives $C_I \approx 0.04\ \varepsilon_o\,\mathrm{nm}^{-1}$. The selectivity is then given by $C_G / C_I \approx 40$.

While the data of Figure 3-4 illustrates the validity of our FET-based demultiplexer architecture for the selection of individual wires, it does not demonstrate the capability to bridge length scales. Referring again to Figure 3-3, we next considered a NW circuit with width W = 13 nm and pitch P = 34 nm. Again, the metal gate electrode is separated from NW_G by about 5 nm of HfO_2 and 1–2 nm of SiO_2 (the native oxide on the NW surface). However, NW_I is now separated from the gate by 5 nm of HfO_2 and

only about 20 nm (= P – W) of SiO_2. Thus, in contrast to the demonstration of Figure 3-4, it is the dimensions of the NW array (pitch and width) rather than the thickness of the low-κ dielectric that determines the gating selectivity of adjacent and very closely spaced NWs, *i.e.*, C_I is dominated by the second term in equation (2) and is approximately 0.02 $\varepsilon_o\,\mathrm{nm}^{-1}$. The result is that for a perfectly fabricated circuit, when a gating voltage is applied, the field felt by NW_G is about ten times greater than that felt by NW_I. For realistic fabrication tolerances, the field ratio is likely to be reduced.

Figure 3-5 shows images of the demultiplexer fabrication process for a circuit designed to address an ultra-high density NW circuit. Using the SNAP method, 150 n-doped Si NWs were fabricated. As described in Chapter 2, this technique can produce aligned arrays of high-aspect ratio (> 10^6) metal and semiconductor NWs at dimensions that are not achievable through alternative methods. Silicon NW arrays containing between 10^2–10^3 NWs, with bulk-like and controllable conductivity characteristics, may be fabricated at dimensions down to W = 8 nm and P = 16 nm.

The demultiplexer itself was patterned using electron-beam lithography and thin-film materials deposition. A brief description of the fabrication procedure is given in Section 3.5. For this demonstration, highly conducting p^+ (10^{19} cm^{-3}) Si NWs were utilized to ensure ohmic contacts and good signal. However, highly doped NWs do not exhibit a strong gating response. Thus, the NWs were thinned (etched) by about 10 nm in the regions where the gate electrodes were deposited, so that in those regions, the doping was ~10^{18} cm^{-3} (Figure 3-3.B). This is a unique feature of diffusion-doped, SNAP-fabricated Si NWs and allows the gating response to be tuned in automatic registry with the gating regions, while also maintaining highly conductive NWs (Figure 3-5.B).

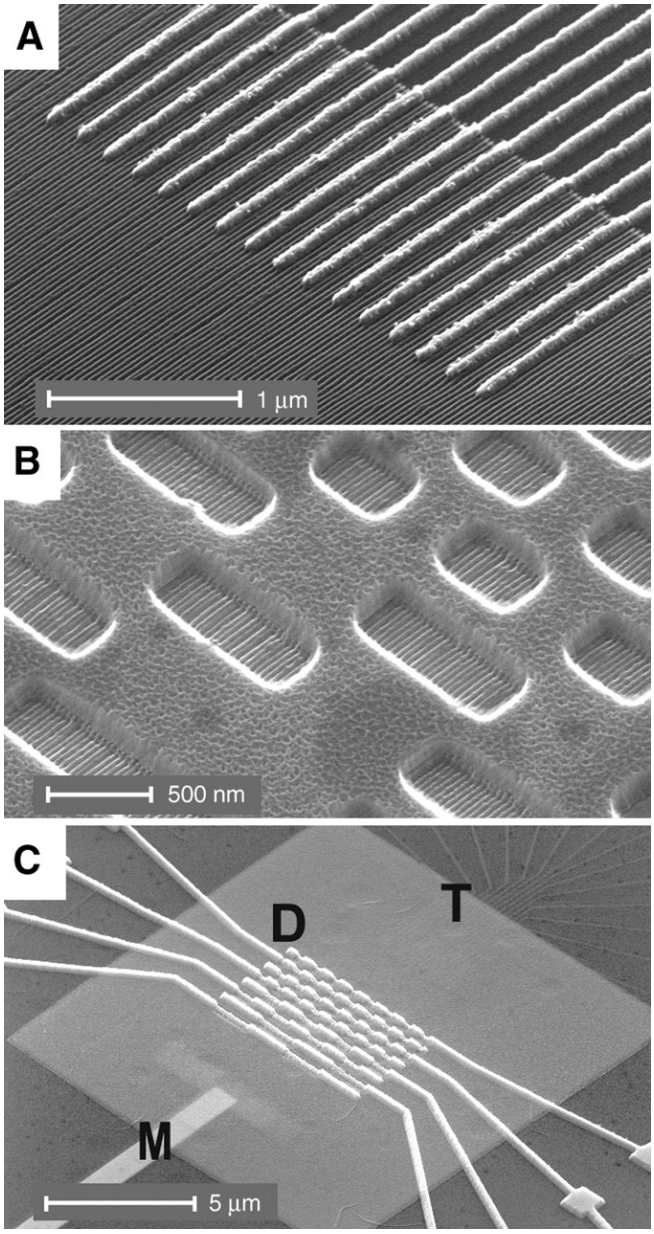

Figure 3-5. Scanning electron micrographs of the nanowire demultiplexer assembly process. A. Sixteen electrical contacts are established, each to two or three NWs from an array of Si NWs. **B**. The binary gate demultiplexer pattern after deposition of the low-κ SiO_2 dielectric and patterning of lithographically-defined windows. Note that once the tops of the underlying Si NWs were exposed, the CF_4-based reactive ion etch process (used to etch the windows in the SiO_2 layer) was briefly extended to intentionally remove approximately 10 nm from the NW surface. This lowers the dopant concentration in the gate region. The high-κ HfO_2 dielectric is deposited following this etch step. **C.** Assembled demultiplexer circuit. M refers to the multiplexer electrode used to apply a voltage to all of the NWs. D is the demultiplexer structure, shown with metal electrodes deposited on the HfO_2 gate insulator. T refers to test electrodes. Individual NWs are measured by applying a voltage to M and grounding the test connections through an ammeter.

There is a chicken-and-egg challenge associated with testing this demultiplexer on narrow-pitch NW arrays; that is, how does one test whether the demultiplexer can address individual NWs when the individual NWs themselves are too closely spaced to separately wire up for the test? Our approach was twofold: First, we established 2^4 (= 16) electrical contacts, each bridging two or three NWs, at a 150-nm pitch for testing (Figure 3-5.A). Second, a binary gating tree of four pairs of microwires was fabricated to allow for the separate addressing of these 16 individual groups (Figure 3-5.B). The most closely spaced wire pairs were patterned at a 600-nm pitch, and these pairs were repeated twice, with the second wire pair phase-shifted by the pitch of the electrical contacts (= 150 nm). The gate width (= 300 nm) was twice the inter-gate spacing. The result was that relatively large binary-tree features could select out the two or three NWs addressed by a given test electrode.

Figure 3-6 shows results from the NW demultiplexer, in which, for two different address combinations, two different sets of NWs were selected, at a signal-to-background level of about four for the worst-case comparison. It is important to note that due to slight variations in the process conditions, different sections of the NW array show both small differences in conductivity as well as different coupling strengths to the gate electrodes. As a result, the data shown is normalized by the values obtained by setting the entire gate array high (+10 V, suppressing conductivity for these p-type NWs), yielding a map of nanoFET response for this specific device. Additionally, we have fabricated a second device based on n-type NWs and found similar values for both the contrast and the selectivity.

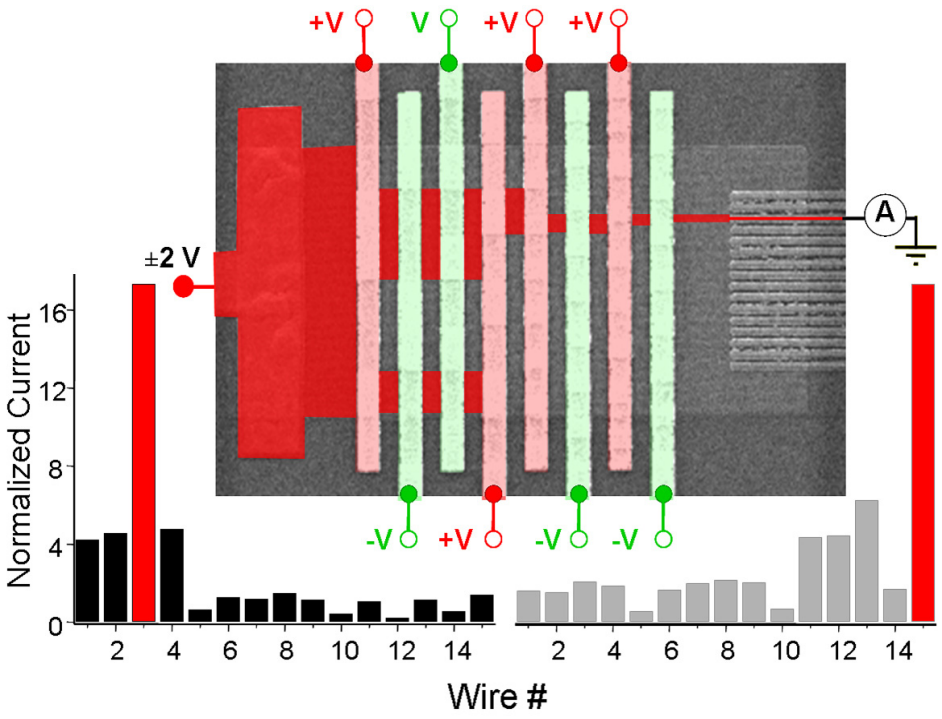

Figure 3-6. Characteristic operation of the nanowire demultiplexer for two different input addresses. The central picture illustrates the address that was used to select out wire 3 in the bottom left bar graph. Gate voltages of +10 V and –10 V were applied to the red and green wires, respectively. The normalized current is the ratio of wire current measured under an addressing gate configuration to the current of the wire when +10 V is applied to all gates

This result validates our demultiplexing architecture, and provides a viable pathway toward bridging length scales between micro- and nano-electronic circuits. As mentioned above, the full demonstration of single-wire selectivity is currently hindered by the lack of an appropriate validation technique, but there is no reason to believe that this architecture can not be extended to even smaller dimensions, given a modest scaling of the controlling gate array. Additionally, we believe molecular-level control of the Si NW-dielectric interface could significantly increase the NW selectivity presented here.

Returning again to Figure 3-3, the 1–2 nm native oxide on the Si NW surface significantly limits the selectivity by greatly reducing the effective dielectric constant of the gate insulator. Although the Si NW native oxide can be removed by hydrofluoric acid

etching, the surface will quickly re-oxidize in an ambient environment. However, through chemical modification of the Si surface, the native oxide can be replaced by a monolayer of covalently bonded methyl groups (*i.e.*, a CH_3-terminated surface). As will be discussed in more detail in Chapter 5, this passivation prevents oxidation of the Si surface and is resistant to typical nanofabrication processing techniques. Replacing t_{native} in equation (1) with the methyl monolayer thickness (about 0.2 nm) and replacing κ_{SiO_2} by the methyl monolayer dielectric constant (believed to be about 2[27, 28]), the capacitive coupling of NW_G to the gate, and hence the NW selectivity, doubles. The selectivity can be further improved by decreasing the HfO_2 dielectric thickness using atomic layer deposition methods (down to about 2 nm). Lastly, further generations of this structure can be improved through the incorporation of ultralow-κ (< 2.0) materials, such as nanoporous silica films (κ = 1.3–2.5), porous polymers, and polytetrafluoroethylene (PTFE) (κ = 1.9)[29]. A challenge will be to incorporate these changes while maintaining a low-leakage current through the gate electrodes (currently 6 pA into a signal channel, or 300 μA cm^{-2}). For nanowires much smaller than those used here, statistical fluctuations in dopant density may ultimately prove limiting to this and other field-effect approaches.

3.4 Demultiplexer patterning requirements

A source of alignment error that cannot be compensated for with increasing redundancy of the input wires is schematically illustrated in Figure 3-7. Note that in Figure 3-7.A it is clear that NW_G represents a deselected (gated) NW, and NW_I represents a selected (isolated) NW. For Figure 3-7.B, it is not clear whether the NW labeled with a question

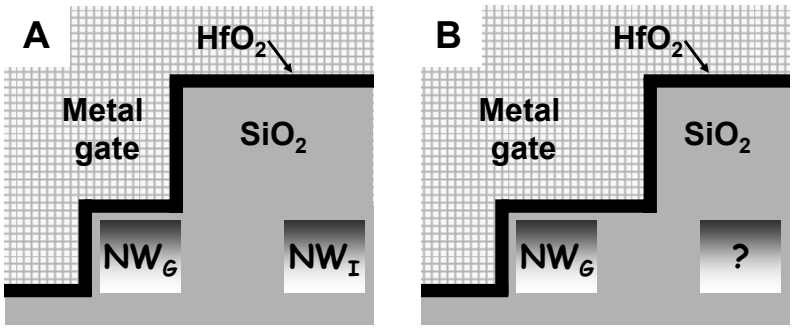

Figure 3-7. An illustration of the importance of alignment precision between the demultiplexer gate structure and the underlying nanowire array. **A.** A perfectly fabricated demultiplexer gate structure, with a deselected (NW_G) and an adjacent selected (NW_I) NW. **B**. An imperfectly fabricated demultiplexer. NW_G is clearly deselected, but the status of the other NW is unclear.

mark (?) is deselected or selected. The implication is that it is necessary to control the placement of the gate electrodes to at least one-half of the pitch of the NWs. This is true, but, as described below, that accuracy is only required for the relative placement of the gates with respect to each other, rather than with respect to the underlying NW array.

Absolute alignment of the demultiplexer pattern with an underlying NW array to an accuracy of the half-pitch of the NWs is difficult, but highly precise relative alignment of the demultiplexer features (gates) with each other is relatively straightforward. To solve the problem of ambiguously addressed NWs depicted in Figure 3-7, extra input wire pairs at the highest gate frequency (smallest gate size) can be added to the demultiplexer with the gate pattern of the extra lines slightly offset from one another (ideally by the NW half-pitch). Note that the extra wires are probably only required for wire pairs with the smallest gate size. This is because wires with larger gating regions will have a smaller fraction of ambiguously gated NWs.

Unlike the case of using extra wiring to address NWs with relatively large gates (discussed in Section 3.2), these redundant address lines do not lead to redundant

addresses. Instead, extra wire pairs are separately tested and then one of them is selected according to which address wire pair yields the best performance. The idea is to take advantage of the precise relative alignment that can be achieved with EBL without requiring absolute alignment to the NW array. Note that this scheme requires the NW array to have a well-defined NW width and pitch; such is the case with SNAP-fabricated NWs.

Finally, fluctuations in the decoder features due to resolution limitations of EBL techniques may result in NWs having non-unique addresses similar to the problem of poor rotational alignment. This problem can be alleviated by using the same strategy for overcoming rotational alignment errors, that is, by adding redundant input wire pairs; however, for NWs at very narrow pitch such lithographic limitations may preclude single NW addressability.

3.5 Demultiplexer fabrication

The following section briefly describes the major steps in fabricating the demultiplexer described herein. More detail can be found in the thesis of Dr. Robert R. Beckman[30]. The NWs were fabricated using the SNAP technique and (100)-oriented silicon-on-insulator (SOI) wafers (30 nm of Si on 150 nm of SiO_2) doped using diffusion-based doping methods (as described in Chapter 2). The fall in dopant density with depth into the Si epilayer, which is characteristic of diffusion-based doping, was critical for increasing the response of NWs to field-effect addressing.

The SNAP-fabricated NWs were then sectioned (via lithographic patterning and an SF_6 dry etch) to at least 10 μm in length, and ohmic contacts were patterned using standard electron-beam lithography (EBL), thin-film metal evaporation, and lift-off. The contacts were annealed in N_2 (5 min, 450° C), and Si NW conductivity was verified before proceeding to the dielectric material deposition steps.

A thick (> 50 nm) SiO_2 layer was used as the low-κ (low-gate-capacitance) dielectric material, and was deposited by either spin-on glass (SOG; Honeywell, see Chapter 4, Section 4.6 for details) or plasma-enhanced chemical vapor deposition (PECVD). The SOG is likely to have a slightly lower κ value than a PECVD oxide, due to the lower quality of the film, which is useful for increasing the high- and low-gate contrast. EBL was used to patterning windows in either poly-methyl methacrylate (PMMA) or ZEP-520A (Zeon Corp. Tokyo, Japan), and reactive-ion etching (20:30:2.5 CF_4 to He to H_2, 40 W, 5 mTorr) was used to etch the SiO_2 over the binary-tree-gated regions. The etch time was extended beyond the interferometrically-determined end-point to slightly thin (by about 10 nm) the Si NWs. As described above, this decreases the dopant density in the regions where a strong gating response is desired.

Following the critical SiO_2 etch, a thin film (<5 nm) of HfO_2 is deposited (via electron-beam evaporation of Hf metal in an O_2 atmosphere of 6.7×10^{-5} Torr) over the entire decoder pattern as the high-κ dielectric. Lastly, Ti/Al/Pt (10 nm/100 nm/ 20 nm) top-gate electrodes are deposited using EBL, thin-film metal evaporation, and lift-off. Note that the evaporated HfO_2/Ti/Al/Pt stack fills the etched recesses in SiO_2 where the gate electrodes couple strongly to the underlying Si NWs to be gated (Figure 3-5.B and Figure 3-5.C).

3.6 References

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