# Chapter 2

# Fabrication of ultra-dense nanowire arrays

## 2.1 Introduction

The development of arrays of semiconducting and metallic nanowires (NWs) will undoubtedly be important for the realization of any future nanoelectronic circuit architecture. NWs serve to not only propagate electrical signals into and out of a circuit, but can also function as the active components within the circuit. For example, NWs have been used to fabricate nanoscale field-effect transistors (FETs)[1-6], p-n diodes[7, 8], bipolar junction transistors[7], nanoscale electro-mechanical oscillators[9, 10], lasers[11], LEDs[12], complex logic gates[13], and complementary inverters with signal gain[14]. This economy of functionality makes NWs an ideal building block for assembling larger and more-complicated nanoelectronic circuits since the fabrication of such circuits can be accomplished with little additional complexity[15]. For instance, aligned arrays of NWs can be used to fabricate a crossbar structure (an expanded ticktacktoe board) by repeating the NW fabrication procedure twice with the second set of NWs fabricated on top of, and perpendicular to, the underlying first set of NWs. By implementing a computational function at the intersection of two NWs, such as logic or memory, a crossed-nanowire

circuit containing $N \times M$ electronic devices can be fabricated from two constituent $N$- and $M$-nanowire arrays. The device-to-device pitch is limited by the pitch of the NWs, so the ultimate density of a NW crossbar circuit is limited by the dimension and pitch of the technique used to form the NW arrays. This has driven researchers in the field to develop methods for assembling NW arrays at very narrow pitch. The scalability and manufacturability of crossbar circuits has lead to an emerging consensus that future nanoelectronic applications (not necessarily limited to conventional computational functions, such as memory and logic) will most likely be based on the crossbar architecture[16-19].

In addition to NWs, single-walled carbon nanotubes (SWNTs) have gained considerable attention from the nanotechnology community. Carbon nanotubes are cylindrical, rolled-up sheets of graphene that are about a nanometer in diameter and possess remarkable electronic, thermal, and mechanical properties (excellent reviews are available from Hongjie Dai[20] and Paul McEuen[21]). Current synthesis techniques produce a mix of semiconducting and metallic nanotubes (with about two-thirds being semiconducting), and while great progress has been made to separate the two[22], nanotube electronics continues to be hindered in the absence of a high-throughput separation technique. This is in contrast to semiconductor NWs, where the electrical properties can be precisely controlled through doping. In addition, NW length, width, and morphology can be tailored during fabrication. Considerations such as these have made semiconducting NWs the dominant structure for building nanoelectronic circuits containing more than just a handful of devices.

For electronics applications, the semiconducting material of choice is silicon. The physical and mechanical properties of silicon have been well characterized and there are highly developed protocols for patterning and electrically contacting silicon devices. An additional benefit is the possibility of integration onto a conventional CMOS technology platform, thus opening the door for relatively near-term commercial applications.

The versatility of Si NW-based electronics has fueled intense research and development of semiconductor NW fabrication protocols to enable the parallel fabrication of large numbers of NWs of specific geometry and with precisely controlled electrical properties.

The most widely used Si NW fabrication technique is the vapor-liquid-solid (VLS) growth mechanism[23, 24]. A typical procedure is to heat a gold nanocluster in the presence of vapor-phase silicon (usually $SiH_4$ in an $H_2$ carrier gas) to the Au-Si eutectic temperature (363° C), resulting in the formation of a liquid droplet of Au-Si alloy. As vapor-phase silicon is continuously fed into the reaction chamber, the droplet becomes supersaturated and solid silicon precipitates out of the melt. As long as there is silicon precursor in the reaction vessel to keep the droplet supersaturated, a Si NW grows from the solid-liquid interface with the supersaturated droplet riding on top. This process can be fine tuned to produce Si NWs with reasonably well controlled lengths and diameters[25] (which is primarily determined by the diameter of the Au catalyst). However, the VLS NW fabrication technique faces some significant challenges. VLS-grown NWs tend to be limited in length to around 10 micrometers (μm)[26], which in turn limits their practical applicability to anything other than small-scale nanoelectronic circuits. The precise electrical properties of VLS-grown NWs are generally unknown before they are wired up

since the NWs are doped *in-situ* by adding dopant precursor to the reaction vessel. Additionally, while the VLS technique can be used fabricate large numbers of NWs in parallel, subsequent procedures are required to align the NWs into arrays and crossbar circuits[24]. The most successful procedure to date employs a Langmuir-Blodgett (LB) trough[27] to align the NWs parallel to one another. However, this technique suffers from fluctuations in the average alignment direction and poor end-to-end registry of individual NWs. This makes interconnecting and integrating such arrays into larger (especially CMOS-compatible) circuitry difficult. In addition, the LB technique would be difficult to scale-up for the commercial manufacture of NW circuits.

## 2.2 The SNAP nanowire fabrication technique

### 2.2.1 Introduction to SNAP

The ability to assemble nanoscale building blocks such as Si NWs into integrated nanoelectronic structures at narrow pitch (and therefore high density) is a general challenge in nanotechnology. The majority of work in the field has focused on few-device demonstrations of scaling feature size, and has largely neglected such considerations as feature pitch, device-to-device reproducibility, and manufacturability—all of which are required for any robust application. The superlattice nanowire pattern transfer (SNAP) technique was developed within the Heath group[10] to simultaneously address these issues. The SNAP technique is a 'top-down,' non-photolithographic technique that enables the fabrication of ultra-dense arrays of high aspect ratio (length-to-

width ratio routinely > $10^6$) Si and/or metal NWs that are aligned over millimeter length scales, and without the need for a secondary alignment step after NW fabrication. NW width and wire-to-wire pitch are highly reproducible and the technique is compatible with conventional CMOS technology and adaptable for large-scale manufacturability. Furthermore, the SNAP technique permits precise control of the electrical characteristics of Si NWs through quantitative doping control. These traits make the SNAP technique ideally suited for realizing large-scale NW circuits.

My initial research efforts in the Heath group were devoted to optimizing the SNAP procedure so that fabrication of Si NW arrays with precisely controlled electrical properties would be routine and reproducible. Previous efforts were successful in using SNAP to generate arrays of 128 Si NWs of widths down to 20 nm, but only a fraction of those NWs conducted, and none exhibited bulk-like conductivity characteristics[10]. We found that Si NWs of widths of less than 30 nm are critically sensitive to the defects introduced by standard processing methods such as ion-implantation doping. Nanowires significantly smaller than 50 nm in width (~25-nm thick) and longer than 10 μm will often contain at least one such defect, and the result is a poorly conducting wire. However, by moving to diffusion doping we were able to improve the conductivity of our Si NWs by a factor of $10^3$, and to demonstrate that Si NWs with diameters of 10 nm and lengths in excess of 1 mm can be fabricated with controllable, bulk-like conductivity characteristics and useful field-effect transistor properties[28]. In what follows I will describe the efforts of my coworkers and I to optimize SNAP NW fabrication procedures for extending the SNAP technique to arrays of 400 NWs for use in ultra-dense crossbar

memory circuits, in addition to achieving bulk-like conductivity from SNAP-fabricated Si NWs. I will begin with a general description of the SNAP NW fabrication protocol.

### 2.2.2 Detailed description of SNAP nanowire fabrication

SNAP uses molecular-beam epitaxy (MBE) to create a physical template for NW patterning. This template is a custom-grown gallium arsenide/aluminum gallium arsenide ($GaAs/Al_xGa_{(1-x)}As$) superlattice structure consisting of alternating layers of GaAs and $Al_xGa_{(1-x)}As$ grown on top of a (100) GaAs substrate. The mole fraction $x$ ranges from 0.5 to 0.8; for clarity, the subscripts will be omitted in what follows. For typical applications, the AlGaAs layer thickness determines the NW width and the GaAs layer thickness determines the separation between NWs. Because MBE is capable of growing layers with atomic resolution, the NW width and separation can in principle be reduced to just a couple of atomic layers. In practice, however, NWs have been limited to about 7–8 nm in width and 15 nm in pitch[29], although, as of this writing, we haven't pushed very hard on this limit.

The number of alternating layers of GaAs and AlGaAs determines the number of NWs in the array. To date, we have successfully used the SNAP technique to fabricate arrays containing up to 1400 NWs[29]; however, there is no reason (in principle) why we couldn't increase this number considerably.

The SNAP fabrication protocol begins by carefully dicing a portion of the superlattice wafer into small rectangular pieces approximately 2 mm wide and 5 mm long (Figure 2-1.A). These pieces will henceforth be referred to as masters for reasons that will become obvious. The masters are cleaved from the parent GaAs/superlattice wafer

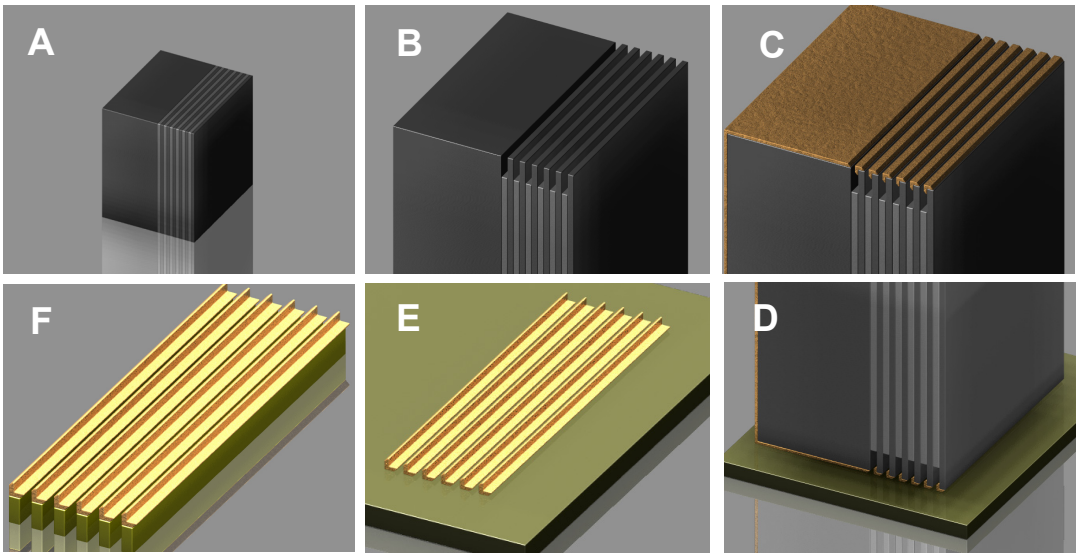


**Figure 2-1. The major steps in SNAP nanowire fabrication (clockwise direction) A.** A small piece of the GaAs/AlGaAs superlattice is selectively etched, **B**, forming a comb-like structure. **C.** Pt is then deposited along the ridges of the comb. **D.** The superlattice template is adhered to an epoxy-coated thin-film substrate. **E.** The superlattice is released from the Pt nanowires and, **F**, the Pt nanowire pattern is transferred into the underlying thin film.

such that one of the 2-mm-wide edges of the master is precisely along a lattice direction. This leaves an atomically flat {110} or {001} plane exposed on that edge (depending on the direction of cleave). The masters are then loaded into a custom-made Teflon holder with the atomically flat edge facing up. They are sonicated in methanol (~10 seconds at a time) and the atomically flat edge is gently swabbed until all particulates visible under a 160× magnification optical microscope are removed. The superlattice region of the master is scrupulously cleaned before proceeding since a single micrometer-sized piece of debris can (and frequently does) result in unsuccessful NW fabrication. I have found that small particulates relatively far away from the superlattice region are not usually a problem and can be ignored. Also, particulates that cannot be removed from sonication and swabbing may come off in the subsequent etch step.

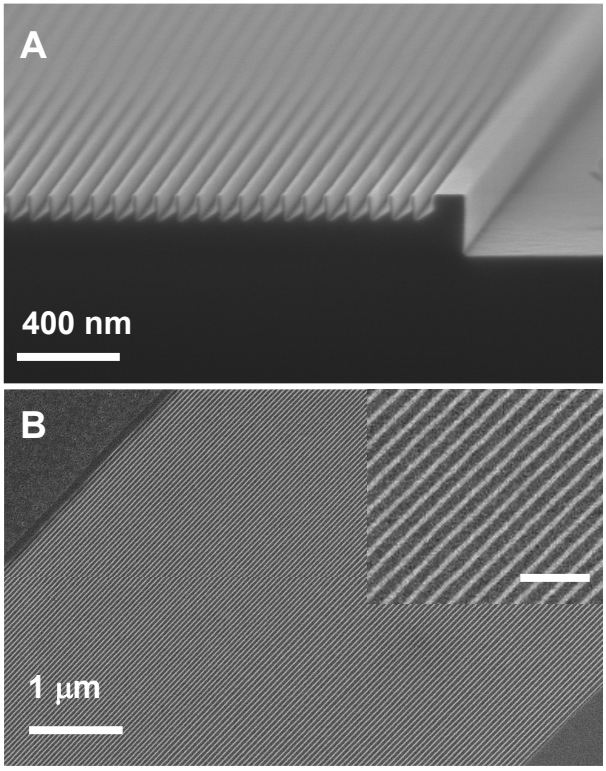


**Figure 2-2. Scanning electron microscope (SEM) images of SNAP nanowire fabrication. A**. Partially etched GaAs/$Al_{0.5}Ga_{0.5}As$ superlattice showing the $Al_{0.5}Ga_{0.5}As$ ridges forming the Pt nanowire template. **B** 128 12-nm-wide Si nanowires generated by using the transferred Pt nanowires as an etch mask. The inset is a higher-resolution image revealing the incredible fidelity obtained with the SNAP process. The scale bar is 150 nm.

The GaAs (or AlGaAs) layers are selectively etched in an $NH_4OH$-$H_2O_2$ etch solution to form a comb-like structure (Figures 2-1.B and 2-2.A) and 10 nm of Pt is then deposited with the superlattice surface oriented at 45° with respect to the evaporative flux of an electron-beam-evaporated Pt source (Figure 2-1.C). The orientation of the superlattice determines how much metal is deposited along the ridges of the AlGaAs (or GaAs) comb, which defines the Pt NW template. The metal-coated superlattice is then applied to a thin (~10 nm) layer of heat-curable epoxy spun onto a substrate with a thin-film epilayer (Figure 2-1.D). To ensure that the epoxy spins down uniformly, the surface is rigorously cleaned beforehand. The epoxy is then baked in two steps for 10 minutes and 30 minutes at approximately 100° C and 135° C, respectively. After curing, excess epoxy is removed by a high-power, 100-Watt (W) oxygen reactive-ion etch (RIE) at 5 milliTorr (mTorr). The superlattice template is released from the Pt NWs by etching the GaAs/AlGaAs superlattice in either commercially available gold-

etch solution (4 g KI + 1 g $I_2$ into 100 ml $H_2O$) or 1:5:50 solution of 30% $H_2O_2$ to conc. $H_3PO_4$ to $H_2O$; both for 3–5 hours*. The epoxy between the Pt wires is subsequently removed in another oxygen RIE step (40W, 5 mTorr).

At this stage the SNAP procedure has produced an array of Pt NWs adhered to a thin-film substrate (Figure 2-1.E). The Pt NWs can then be used as an etch mask in an anisotropic RIE to transfer the NW pattern into the thin-film substrate (Fig 2-1F). The highly versatile SNAP technique can be used to fabricate NWs out of any thin-film material that can be anisotropically dry-etched. To fabricate Si NWs, the Pt NW pattern is adhered to a doped silicon-on-insulator substrate. High-fidelity pattern transfer with vertical side walls is accomplished using a high-frequency RIE tool (40 MHz Unaxis SLR parallel-plate RIE) and fluorine-based reactive-ion etching at low substrate bias (10–20 volts DC). An etch recipe of $CF_4$, He, and $H_2$ (20:30:2.5) at 40 W and 5 mTorr was found to give vertical Si sidewalls with no observable undercut. (The added hydrogen promotes the deposition of a fluoropolymer on the Si NW sidewalls to prevent undercutting.) However, I found that this etch would occasionally reduce the conductivity of boron-doped NWs. One possible explanation is that hydrogen in the etch was diffusing into the NWs and forming a boron-hydrogen complex[30]. This complex results in passivation of the dopant so it can no longer produce free charge carriers. For thin Si epilayers, I have found this problem can be avoided without altering the etch fidelity by simply removing $H_2$ from the recipe. The Si etch end-point is determined by interferometry, although the etch efficiency may be lower between the narrow-pitched Pt NWs than where the actual laser spot is positioned (due to residual epoxy and Pt NW

* A lower bound for the etch time is given by (thickness of superlattice region)/etch rate. The phosphoric acid etch rate is ~0.1 μm/min at room temperature. The $KI/I_2$ etch rate was not measured but is estimated to be ~0.2 μm/min.

charging effects). To ensure complete transfer of the Pt NW pattern into the underlying Si film, the etch time is usually extended by 25–50 percent. Over-etching is not a problem for most applications since this only results in transferring the NW pattern into the underlying oxide by a small fraction ($CF_4$ etches Si and $SiO_2$ equally[31] in pure $CF_4$). After transferring the Pt NW pattern to the underlying Si epilayer, the final step is to remove the Pt NWs in hot aqua regia (1:4 conc. HCl to conc. $HNO_3$ at 120° C, ~10 min). The result is an array of Si NWs on an insulating oxide that are aligned and continuous over hundreds of microns (Figure 2-1.E & Figure 2-2.B).

The selective GaAs etch, Pt evaporation angle, and epoxy formulation are all key for obtaining high-quality NW arrays. Accordingly, I will discuss each in more detail below.

### 2.2.3 Selective etching of GaAs on AlGaAs

The SNAP technique relies on a physical template for NW fabrication. The construction of this template requires not only the fidelity of MBE to define alternating layers of GaAs and AlGaAs, but the ability to etch GaAs with high selectivity. One of my goals was to optimize this etch for various GaAs/AlGaAs superlattice structures. Although I will only consider the selective etching of GaAs over AlGaAs, as an alternative AlGaAs can be selectively etched over GaAs[10] using a buffered-oxide etch solution (BOE) (6:1 $NH_4F$ to HF). Selective etching of AlGaAs is generally avoided because BOE is hazardous to work with. However, the ability to alternatively etch AlGaAs instead of GaAs can be useful for reversing the NW width and spacing for a given superlattice.

The GaAs etch must be highly selective to GaAs over AlGaAs so that the AlGaAs ridges of the comb are not rounded. It also needs to be controllable so that the etch parameters can be calibrated to produce a consistent etch depth. The optimal etch depth is dependent on the GaAs layer thickness and the Pt evaporation angle. This can be seen from the cross-sectional schematic of a GaAs/AlGaAs comb shown in Figure 2-3.A. Each AlGaAs ridge acts as a self-aligned shadow mask for the ridge behind it. Since the evaporation angle must always be less than 90° to avoid depositing metal into the GaAs recess, the Pt lines actually have an 'L' structure, where the dimensions of the 'L' depend on the angle of evaporation (Figure 2-3.B). The metal extends along one side of each

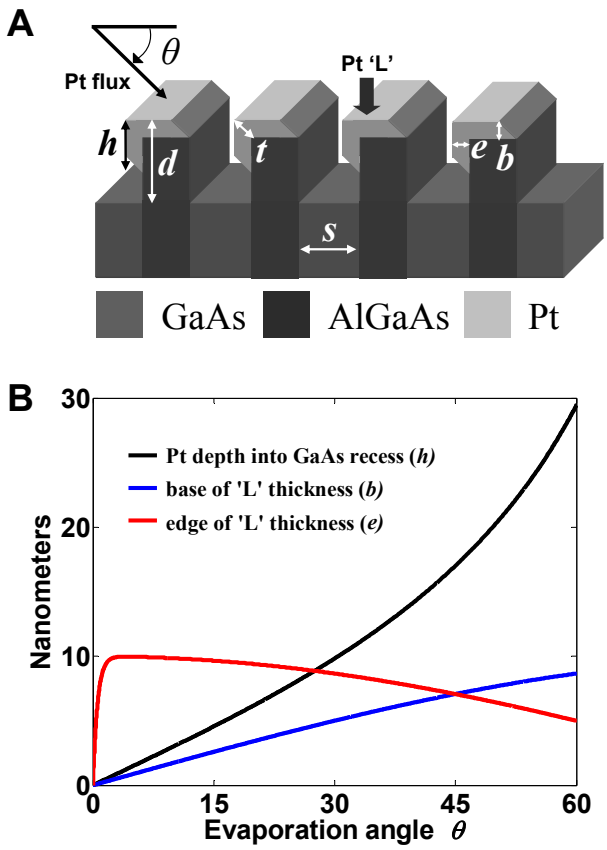


**Figure 2-3. Pt deposition onto an etched GaAs/AlGaAs template. A.** Cross-sectional diagram of a portion of the etched GaAs/AlGaAs template. Pt is evaporated onto the AlGaAs ridges at an angle $\theta$ forming an upside-down 'L' structure (right-side up after depositing the Pt NW array) with base and edge thicknesses $b$ and $e$, respectively. Pt coats one side of each AlGaAs sidewall to a depth, $h$, that depends on $\theta$ and the AlGaAs spacing, $s$. **B.** Calculated dimensions of the Pt 'L' as a function of $\theta$ for a superlattice with AlGaAs spacing $s$ = 17 nm and evaporated Pt thickness $t$ = 10 nm. The evaporation angle is chosen to give the best Pt nanowire morphology within the constraint that $h$ is less than the GaAs etch depth, $d$. For the superlattice considered here, this is 45° (see text).

AlGaAs ridge into the GaAs recess (*h* in Figure 2-3.A) for all relevant evaporation angles (*i.e.*, $0° < \theta < 90°$) and increases with both the evaporation angle (Figure 2-3.B, black line) and the spacing of the AlGaAs layers. For maximum applicability to different superlattices and varying evaporation angles, it is desirable for the GaAs etch to produce a GaAs recess as deep as possible.

I explored two etch chemistries* and a range of etch concentrations on superlattices containing 128, 150, and 400 alternating layers of GaAs/AlGaAs with layer thicknesses of 10 nm/20 nm, 10 nm/25 nm, and 15 nm/20 nm, respectively. The 128- and 150-wire superlattices were grown by University of California Santa Barbara with mole fraction of Al $x = 0.5$. The 400-wire superlattices were grown from either University of California Santa Barbara or IQE Inc. (Bethlehem PA) with mole fraction of Al $x = 0.8$. The two etch solutions were 1:20 conc. $NH_4OH$ to 30% $H_2O_2$[32] and 5:1 50% aqueous citric acid ($C_6H_8O_7$) to 30% $H_2O_2$[33, 34]. Aqueous citric acid was prepared by dissolving 1 gram of anhydrous $C_6H_8O_7$ per milliliter of $H_2O$. These stock solutions were diluted by varying margins in $H_2O$ before use. Extra wide masters (about 4–5 mm) were cleaved from a given superlattice along a lattice direction and subsequently etched for times ranging from 5 seconds to 20 seconds, then rinsed with de-ionized (DI) (18 MΩ) water, and dried under $N_2$. After etching, each master was cleaved lengthwise into halves and loaded onto a scanning electron microscope (SEM) puck with one piece laid on its side with the fresh cleave facing up. This way a top-down view showing the registry of the AlGaAs ridges as well as a cross-sectional view to measure the etch depth could be obtained from the same master. Figure 2-2.A was generated in this fashion.

* An acetic acid-based etch was also tried but was found to be inferior to the $NH_4OH$ and $C_6H_8O_7$ etches.

Both of the etch solutions were found to have excellent selectivity for GaAs over AlGaAs. While the citric-acid etch in dilutions ranging from undiluted to 1:5 (stock solution to $H_2O$) and etch times from 6 to 30 seconds, respectively, produced good results for the 128-wire superlattice, we found the $NH_4OH$-$H_2O_2$ etch solution diluted by a factor of 15 in $H_2O$ to be easier to prepare and more consistent from one run to another and for different superlattices. Using this etch solution, the maximum (reliable) GaAs etch depth was found to be 30–40 nm, corresponding to 10–12 seconds of etch time. Longer etch times occasionally resulted in collapsed or broken-off AlGaAs ridges.

After etching the IQE-grown 400-wire superlattice in $NH_4OH$-$H_2O_2$ solution, I frequently observed small aggregates (< 50 nm) of what appeared to be solid Ga on the superlattice surface (Figure 2-4). This excess Ga may originate from a Ga-rich reconstruction[35] of the exposed {001} crystal plane after cleaving along the ⟨110⟩

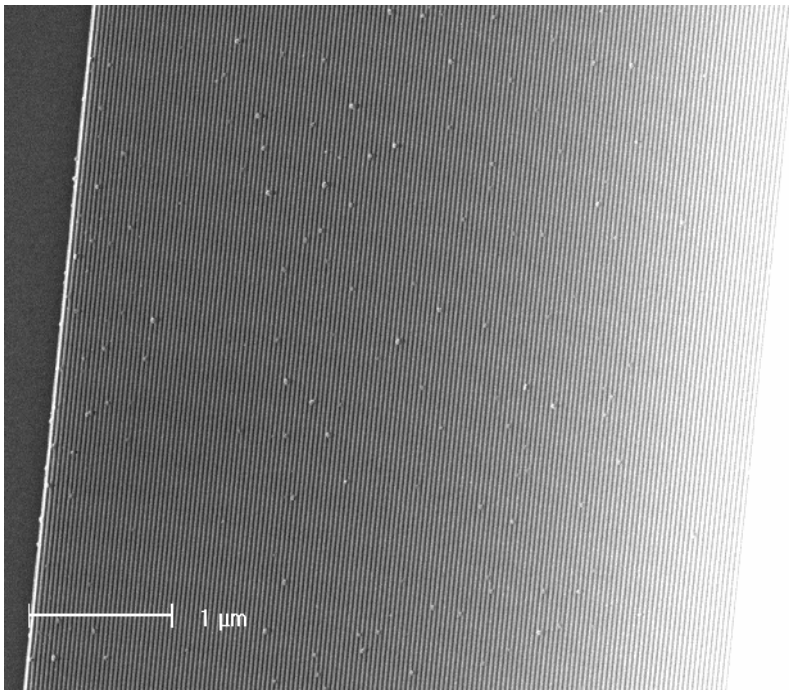


**Figure 2-4. Scanning electron micrograph (SEM) of a freshly-etched 400-nanowire GaAs/AlGaAs superlattice.** This master was not treated with an additional $H_2O_2$ dip, and aggregates of solid Ga can clearly be seen dispersed over the GaAs/AlGaAs layer surface.

direction (the direction along the IQE wafer flat). I found these aggregates could be oxidized and removed from the superlattice surface by a 5-second dip in undiluted 30% $H_2O_2$ immediately following the $NH_4OH$-$H_2O_2$ etch. Although Ga aggregates on the superlattice surface were found to be present only after cleaving along the ⟨110⟩ or ⟨010⟩ directions, the extra $H_2O_2$ treatment was adopted as a standard step in the $NH_4OH$-$H_2O_2$ etch procedure. (In the very least, this step helped to remove particulates from the superlattice surface.)

### 2.2.4 Optimum platinum evaporation angle

In addition to the GaAs etch, I systematically investigated how different Pt evaporation angles affected the Pt NW morphology. Smooth Pt NWs are important because they must serve as a high-fidelity stencil to define arrays of Si or other thin-film material NWs. Ideally, Pt should only deposit along the AlGaAs ridges so that the transferred Pt NWs are as symmetrical as possible. This requires a small evaporation angle to reduce the depth of evaporated Pt along the side of individual AlGaAs ridges (Figure 2-3.B, black line). However, this was found to also increase the roughness of transferred Pt NWs along their corresponding side. This roughness is likely due to the accumulation of Pt along one side of the AlGaAs ridge as a result of the small evaporation angle (Figure 2-3.B, red line). Larger evaporation angles gave smoother Pt NWs, but to also increased the depth of evaporated Pt along AlGaAs ridges (Figure 2-3.B, black line). After some trial and error, I found that a 45° evaporation angle worked the best. A 45° angle consistently

produces smooth Pt NWs while being shallow enough that evaporated Pt does not reach the bottom of the GaAs recess (Figure 2-3.B).

### 2.2.5 Epoxy formulation

Optimizing the epoxy formulation for high-yield SNAP-NW fabrication has proven to be quite difficult, and numerous members of the Heath group have worked to establish a reliable formulation. In fact, one of my initial efforts in the Heath group was to investigate the use of amine-terminated self-assembled monolayers (SAMs) on silicon to replace the epoxy altogether as a Pt NW adhesive. We found that SAMs could produce small arrays of aligned Pt NWs over distances of up to 50 μm, but reliable alignment over longer distances and larger NW arrays was very difficult. To date, two epoxy formulations are used in the Heath group; both are modifications of Epoxy Bond 110 (Allied High Tech, Rancho Dominguez California). Both formulations include a polymeric additive that functions as a plasticizer to make the epoxy easier to etch in the oxygen plasma steps described above. The first version uses a PMMA additive (0.37 g of 6 % PMMA, 20 drops of Epoxy Bond part A, 2 drops of Epoxy Bond part B, 15 ml of chlorobenzene). This epoxy recipe etches easily in $O_2$ but does not adhere to the substrate as well as the following recipe using dibutyl phthalate as a plasticizer: 5 drops part A, 1 drop part B, 2 drops of dibutyl phthalate, 10 ml of anhydrous tetrahydrofuran (THF). The latter recipe was used exclusively for the fabrication of crossbar circuits, described in Chapter 4. The epoxy is spun onto a clean substrate at 5000 RPM to achieve a film

thickness of about 10 nm. (Note that film thickness is critical to ensure good pattern transfer.)

## 2.3 Achieving bulk-like conductivity of silicon nanowires

To maximize the conductivity of our Si NWs, we undertook a systematic investigation[28] of the relative importance of the defects native to our SOI substrates as compared to defects introduced through processing techniques such as doping and reactive-ion etching (RIE). A *p*-doped Si (100) epilayer grown via MBE represented our 'gold standard' for fabricating high-quality Si NWs; this substrate was used to assess how the RIE transfer of the NW pattern from Pt to Si affected Si-NW conductivity. NWs fabricated from the MBE substrate then served as a metric for comparison to commercially available 4-inch SOI wafers (defect density = 0.23 $cm^{-2}$) and industry-standard 8-inch SOI wafers (defect density < 0.1 $cm^{-2}$). In addition, NWs fabricated from 4-inch SOI wafers were used to compare ion-implantation doping to diffusion doping from a spin-on dopant source. As expected, NWs fabricated from the higher quality 8-inch SOI wafers resulted in better-conducting Si NWs. The use of spin-on doping resulted in a more dramatic improvement in NW conductivity, and has proved to be essential for reliably obtaining conductive Si NWs below 50 nm in width.

The Si-NW resistivity was used as the figure of merit for NW quality. To facilitate resistivity measurements, Si-NW arrays were sectioned into multiple regions of length 5–25 μm with each section contacted by two sets of Ti/Al/Pt (10 nm/150 nm/20 nm) electrodes via electron-beam lithography and thin-film metal deposition and lift-off.

Individual NWs were 10–15 nm wide and each electrode addressed 2–4 NWs (Figure 2-5.A inset). The contacts were subsequently annealed at 450° C for 5 minutes in argon to promote ohmic contact formation. Four contacts allow the measurement of two sets of wires per region and cross-conductance measurements between sets to measure leakage current.

Figure 2-5.A (filled circle) shows a current-voltage (*I-V*) trace for a 7-μm-long section of Si NWs fabricated from the MBE substrate (30 nm of Boron:Si on intrinsic Si, $p = 1\times10^{19}$ $cm^{-3}$); the linearity of the trace confirms the ohmic nature of the contacts. The histogram in Figure 2-5.B represents many such resistance measurements normalized by the bulk-scaled resistance, $R_o$, and reveals the bulk-like conductivity of these NWs despite their narrow width of ~10 nm. The good morphological properties of these NWs apparently correspond to good electronic properties, confirming that the RIE recipe described above does not damage the NWs.

In contrast, when Si NWs were fabricated from the same substrate used in previous studies[10] (ion-implantation doped 4-inch SOI wafer; 25 nm of boron-doped Si on 150 nm of $SiO_2$; $p = 3\times10^{19}$ $cm^{-3}$), the $R/R_o$ histogram was centered at $10^4$ (not shown), indicating that the electrical properties of those NWs were severely degraded. The most probable cause is lattice defects from ion-implantation methods. Ion-implantation doping uses a high-energy beam of ionized dopant atoms to implant dopants into the Si substrate. These high-energy dopants collide with Si atoms in the lattice and produce point defects that degrade the conductivity of the substrate. Post-implantation thermal annealing can alleviate most of these defects[36], but for NWs of narrow width (~10 nm here) even a small number of doping-induced defects can dramatically affect

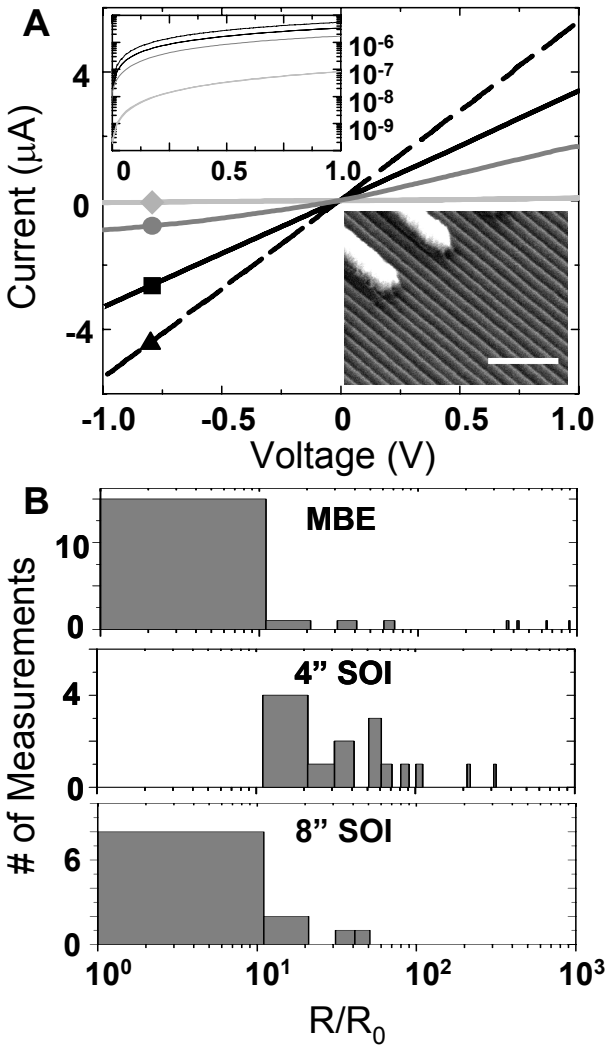


**Figure 2-5**. **Si nanowire electrical properties. A**. IV measurements of 4 nanowire samples (all samples doped via spin-on diffusion doping): ■ 8" SOI, p=5e19cm$^{-3}$, 10nm×31nm×3μm ▲ 8" SOI, n=1e20cm$^{-3}$, 10nm×31nm×3μm ● MBE, p=1e19cm$^{-3}$, 10nm×30nm×7μm ♦ 4" SOI, p=5e18cm$^{-3}$, 10nm×25nm×2.5μm. Upper-left inset shows data plotted on a semi-log scale. Lower-right inset shows an SEM image of the nanowire contacts; scale bar is 200 nm. **B**. Statistical distribution of normalized nanowire resistance ($R/R_o$) for various substrates. $R/R_o$ values for ion-implantation doped Si NWs are greater than $10^3$ and are not shown. The bin size is 10.

NW conductivity. This is confirmed by the observation that we could reliably fabricate conductive NWs from ion-implanted substrates down to 50 nm in width, but NWs of 10–15 nm in width were frequently poor conductors. Consequently, we moved to spin-on doping as an alternative to ion-implantation doping. This method forgoes the use of ion-implantation and instead uses high-temperature annealing to gently diffuse dopant atoms into the Si lattice from a spin-on dopant source.

To test the efficacy of spin-on doping to improve NW conductivity, we used SNAP to fabricate Si NWs from a 4-inch SOI substrate doped with the spin-on doping technique (25 nm of Si on 150 nm of $SiO_2$, p = $5\times10^{18}$ cm$^{-3}$). Figure 2-5.A (filled diamond) shows

an *I-V* scan[*] for a 3-μm-long section of these NWs, and Figure 2-5.B shows a histogram of the normalized resistance constructed from several such *I-V* scans. Although the normalized resistance is still a factor of ten higher than the bulk-scaled resistance, NWs fabricated from spin-on doped substrates are a thousand-times-better conductors than their ion-implantation doped counterparts. This dramatic increase in NW conductivity is the result of eliminating lattice defects from ion-implantation doping, and highlights the importance of spin-on doping for the fabrication of conductive NWs with narrow widths.

Improving NW conductivity by another factor of ten, and thus achieving bulk-scaled NW resistance, was accomplished simply by using a lower-defect-density SOI wafer as the starting material (8-inch industry-standard SOI[†] instead of 4-inch SOI). Figure 2-5.A (filled square) shows a typical *I-V* scan for NWs fabricated from a spin-on doped 8-inch SOI wafer (30.8 nm of Si on 145 nm of $SiO_2$, 3-μm long, $p = 5\times10^{19}$ $cm^{-3}$); and Figure 2-5.B, the normalized resistance, which is comparable to the resistance histogram of NWs fabricated from the MBE substrate. Phosphorous-doped NWs fabricated from 8-inch spin-on doped SOI (30.8 nm of Si on 150 nm of $SiO_2$, 3-μm long, $n = 1\times10^{20}$ $cm^{-3}$) also show bulk-scaled resistance (statistical data not shown) and a typical *I-V* scan is showed in Figure 2-5.A (filled triangle, dashed line).

The SNAP technique was additionally used to fabricate high-quality Si NWs with a (111) surface orientation from bonded silicon(111)-on-insulator wafers (Isonics Semiconductor, Vancouver, WA.; 40 nm of Si on 2 μm of $SiO_2$). In accord with the

[*] A slight non-linearity in the IV scan at voltages below 250 mV is observed, but length-dependent resistance measurements revealed linear (ohmic) scaling implying that the observed resistance is dominated by the native NW conductivity and not by the contacts.

[†] Further confirmation of the superior quality of 8-inch industry standard SOI over 4-inch SOI comes from the observation that 4-inch SOI shows substantial leakage current through the insulating oxide while the 8-inch SOI does not.

versatility of the SNAP technique, no modification was required to the procedures that were described above in the context of (100) SOI wafers. The (111) SOI epilayer was 80-nm thick as received, but was thinned to 40 nm through sacrificial dry thermal oxidation and BOE wet etching. The wafer was then diffusion doped with phosphorus using the spin-on doping method ($n = 1\times10^{20}$ $cm^{-3}$), and the SNAP technique was used to fabricate 150-element arrays of Si(111) NWs on top of an insulating oxide (Figure 2-6.B, inset). The Si NWs were sectioned into regions 1 μm in length, then contacted and tested as described above. Figure 2-6.A shows representative *I-V* scans from these NWs and Figure 2-6.B shows a histogram of the normalized resistance constructed from several such *I-V* scans.

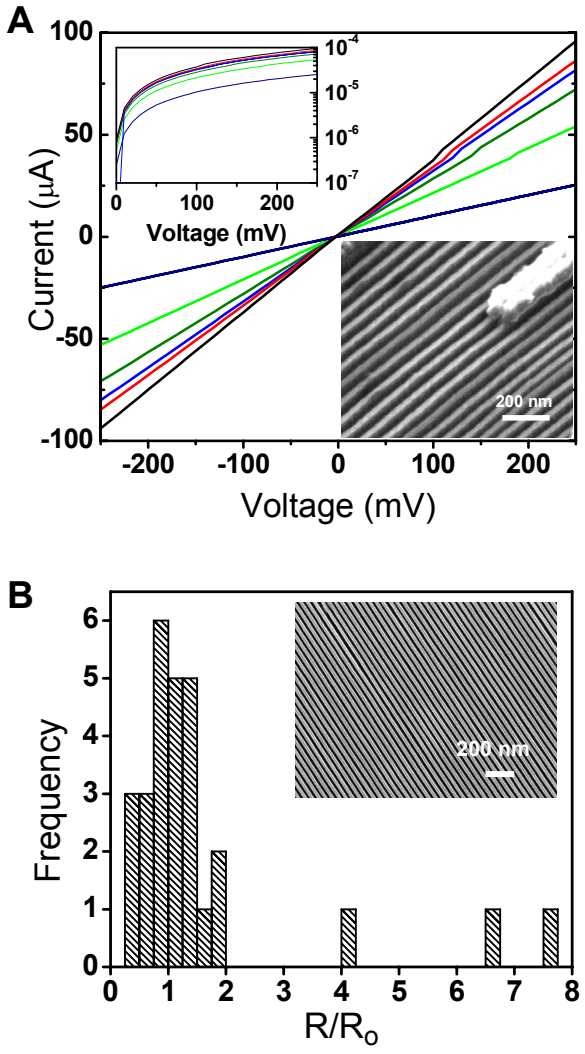


**Figure 2-6. Electrical properties of Si(111) nanowires. A.** Representative current-voltage scans from 6 sets of Si(111) nanowires showing linear response and high conductivity. The top-left inset shows the same data plotted on a semi-log scale and the bottom-right inset shows a nanowire contact. **B.** Statistical distribution of normalized nanowire resistances ($R/R_o$). The bin size is 0.25. The inset shows a zoomed-in SEM image of 15-nm wide nanowires within a 150-element Si NW array. The scale bar is 200 nm.

By comparing the normalized NW resistance histograms of Figures 2-5.B and 2-6.B, it is seen that Si NWs

fabricated from the (111)-oriented SOI substrates are better conductors than those fabricated from (100)-oriented SOI substrates. (The $R/R_o$ distribution for the Si(111) NWs is more sharply peaked at unity.) This provides further evidence of the detrimental effects that ion-implantation processes have on Si NW conductivity. The buried oxide layer of the (100) SOI wafers used in the study above were created (commercially) using the *separation by implanted oxygen* (SIMOX) technique. This process is similar to ion-implantation doping in that it bombards the silicon surface with an energetic beam of ions. Oxygen ions are implanted into the Si substrate to form a buried $SiO_2$ layer separating the Si epilayer from the substrate. Like ion-implantation doping, a post-implantation anneal does not repair all of the implantation-related defects in the Si epilayer. In contrast, the (111) SOI wafers were fabricated (commercially) using a bonding technique whereby two oxidized Si wafers are bonded together at their $SiO_2$ surfaces, thus forming a SOI structure without the need for oxygen ion implantation.

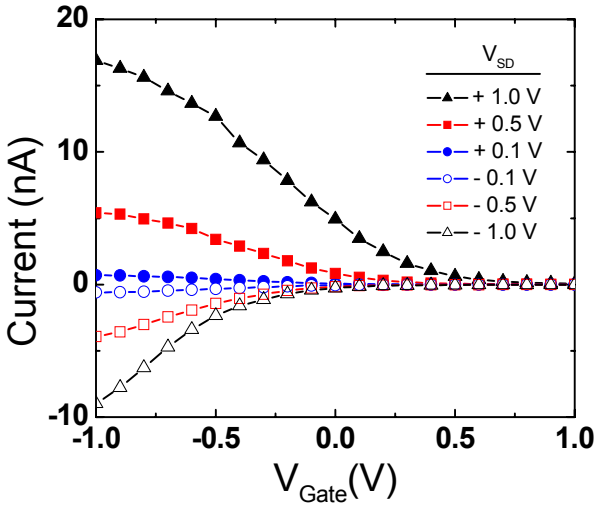


**Figure 2-7. P-type nanowire gating response** for various values of the source-drain voltage. The asymmetry in source-drain bias is attributed to asymmetrical Schottky barriers.

Using NWs fabricated from a 4-inch spin-on doped SOI substrate (7.5-μm long, $p = 5\times10^{18}$ $cm^{-3}$), a crossbar-FET was constructed by depositing 7 nm of $Al_2O_3$ over the NW array, followed by a 250-nm-wide metallic wire as a gate. Figure 2-7 shows the gating response for

various values of the source-drain voltage. An impressive modulation in conductivity was obtained through a gate bias of just ±1V. (Although difficult to see in the figure, we could tune the NW conductivity by a factor of $10^3$.) These results show that by minimizing defects at all stages of NW fabrication we can fabricate Si NWs with bulk-scaled conductance that are highly responsive to field-effect gating.

## 2.4 Silicon nanowire doping

The observation that diffusion-doped Si NWs are thousand-fold-better conductors than their ion-implantation-doped counterparts makes diffusion doping an important part of the SNAP NW fabrication protocol. In what follows, I will discuss the technical aspects of diffusion doping using spin-on dopants for use in SNAP NW fabrication.

Most spin-on dopants consist of the desired dopant species (such as phosphorus or boron) incorporated into a $SiO_2$ polymer-matrix and dissolved in an organic solvent. This dopant solution is spin-coated onto a clean Si chip and baked at an intermediate temperature to drive off solvent. This results in the formation of a thin, dopant-rich $SiO_2$ film on the Si surface that provides a virtually infinite source of dopant atoms. The chip is then annealed at high temperature in an inert environment to facilitate diffusion of dopant atoms from the dopant-rich $SiO_2$ film into the Si lattice. This method provides a simple and gentle route for doping SOI epilayers that is compatible with batch-processing for manufacturability.

The spin-on doping procedure consists of four steps: cleaning the wafer, applying the dopant, annealing and removing the dopant. Because spin-on doping requires high

temperatures, the wafer must be rigorously cleaned to ensure all organic material is removed. To remove organic contamination I frequently used 'piranha clean' (2:1 $H_2SO_4$ to $H_2O_2$, 120° C, 10 min) followed by an RCA clean (5:1:1 $H_2O$ to $H_2O_2$ to $NH_4OH$, 80° C, 10 min; followed by 1:10 BOE to $H_2O$, 25° C, 10 sec; followed by 5:1:1 $H_2O$ to $H_2O_2$ to HCl, 80° C, 10 min). The piranha step was usually omitted if the wafer had not come into contact with photoresist. The RCA clean usually removes small particulates in addition to organic contaminates, but this should be checked under a microscope. If any particulates are found, sonication and swabbing of the wafer surface in methanol is required.

After ensuring that the wafer is clean, the dopant solution is generously applied to the wafer surface using a syringe and a 0.2-μm PTFE filter. The wafer is then spun at 4000 RPM and subsequently baked on a hotplate set at 200° C for 10 min. I obtained the best results for n-type doping using Emulsitone (Whippany, NJ) phosphorosilicafilm (phosphorus concentration = $5\times10^{20}$ $cm^{-3}$) and for p-type doping using Emulsitone Borosilicafilm (boron concentration = $5\times10^{20}$ $cm^{-3}$). The n-type dopant was frequently diluted by a factor of ten in methanol for easier removal after annealing, but can be used as is without difficulty. However, I regularly had difficulty removing the p-type film after annealing unless it was ten-fold diluted in methanol before use.

The dopant-film-coated wafer is then annealed under nitrogen in a rapid thermal annealer (RTA) for the appropriate time and temperature to achieve a given doping concentration. After annealing, the n-type dopant is removed with brief sonication in acetone followed by swirling in BOE until the surface is hydrophobic (usually less than 10 seconds). The p-type dopant frequently required acetone sonication and swabbing

before using BOE to remove the dopant film. If the surface is not hydrophobic after 15 seconds in BOE, I found a brief piranha clean followed by soaking in water and another 10 seconds in BOE to be effective.

To determine the correct anneal time and temperature to achieve a given doping, small test pieces of the substrate to be doped are annealed under various conditions to construct a look-up table of measured dopant density for particular anneal parameters. To determine the doping, I used a home-built four-point probe to measure wafer resistivity and calculated the dopant density from an empirical equation relating dopant density to Si resistivity. Although this technique is widely used to measure dopant density, it should be emphasized that sheet resistivity measurements only give an integrated average of the dopant density through the thickness of the measured substrate.

To obtain an estimate of the proper anneal time and temperature for a given doping, I started by modeling the diffusion of dopant atoms into Si. Taking the thickness of the Si epilayer to be infinite and the dopant concentration at the surface to be constant, a 1-D diffusion model $\left( \frac{\partial C}{\partial t} = D(T)\frac{\partial^2 C}{\partial d^2};\ C(d=0) = C_{surface},\ C(d \to \infty) = 0 \right)$ gives

$$C(d,t,T) = C_{surface}\ erfc\left( \frac{d}{2\sqrt{D(T)t}} \right), \qquad (1)$$

where *erfc* is the complementary error function, $C$ is the dopant concentration, $C_{surface}$ is the concentration of dopant atoms in the spin-on dopant film, $d$ is the depth into the Si epilayer, $t$ is the anneal time, and $D(T)$ is the temperature ($T$)-dependent diffusivity. For Si, $D(T)$ is given by the empirical relation

$$D(T) = A\exp\left( -\frac{E}{8.6\times10^{-5} T/K} \right) \qquad (2)$$

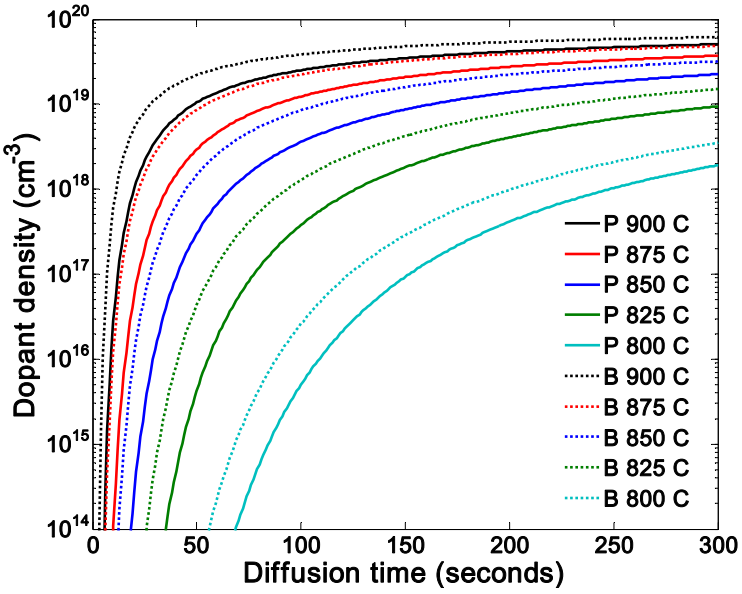


**Figure 2-8. Calculated dopant concentrations as a function of diffusion time for various anneal temperatures.** Calculations are for P and B diffusion in Si from a spin-on dopant (SOD) of concentration $1\times10^{20}$ cm$^{-3}$. For other SOD concentrations, multiply by the appropriate scale factor (*e.g.*, multiply by 5 for a SOD concentration of $5\times10^{20}$ cm$^{-3}$) Depth was taken to be the doping-weighted integrated average (~6 nm for a 5 minute anneal at 900 C). B and P diffusivity parameters were taken from ref. 37.

with $A$ and $E$ constants that depend on the diffusing dopant atom. For phosphorus (boron) diffusion, $A$ = 8x10$^{-4}$ cm$^2$/s (0.06 cm$^2$/s) and $E$ = 2.74 eV (3.12 eV)[37]. Figure 2-8 shows the calculated density of P (n-type doping) and B (p-type doping) in Si as a function of anneal time for various anneal temperatures. Using equation (1) as a guide, several SOI substrates with Si epilayer thicknesses from 25–50 nm were annealed under various conditions to study diffusion doping in our SOI substrates. Figure 2-9.A shows the measured (filled circles) and calculated (dashed line) n-type dopant density for 50-nm SOI after various anneal times at 900° C. Both experiment and calculation reveal a latent period before any appreciable doping occurs, after which the dopant density rises sharply before asymptotically approaching $C_{surf}$. Analogous behavior is observed with 31-nm (Figure 2-9.B) and 25-nm (Figure 2-9.C) SOI epilayers. The (intuitive) trend from this dataset is that higher-temperature anneals produce a sharply rising dopant density that

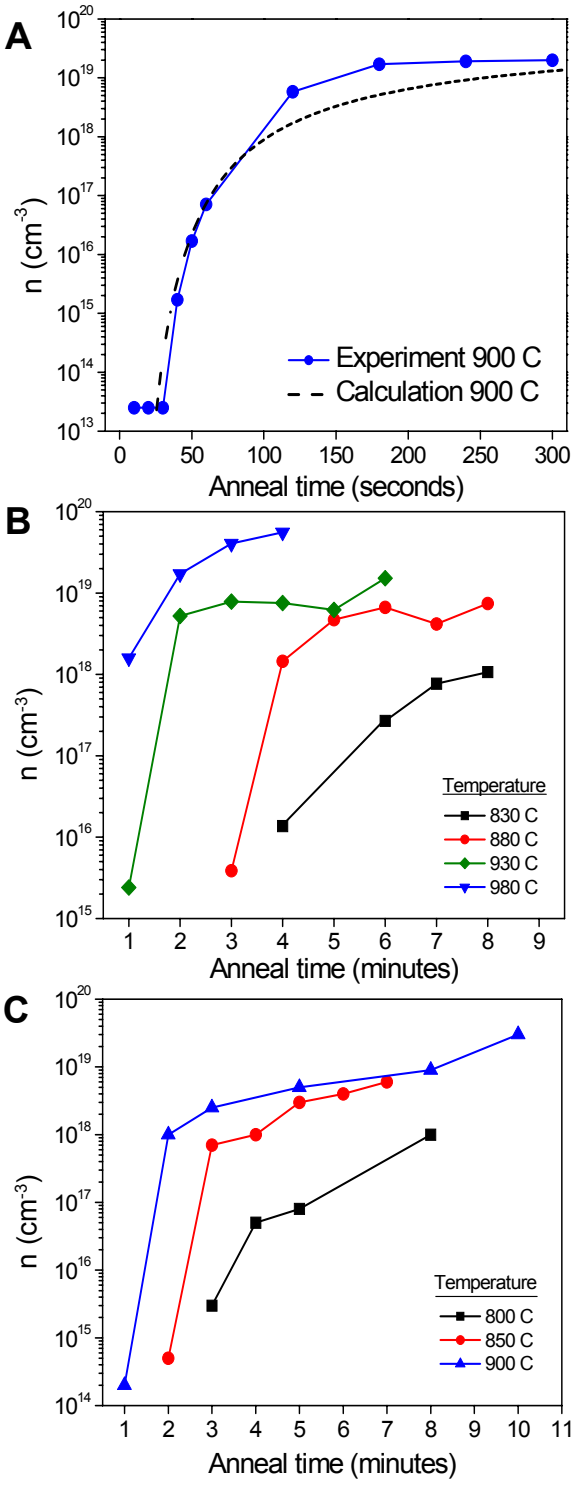


**Figure 2-9. Time and temperature dependence of phosphorus doping in SOI substrates A.** 50-nm SOI; note the good agreement between the calculated and measured dopant densities. **B.** 31-nm SOI. **C.** 25-nm SOI.

subsequently flattens out at high doping, while lower-temperature anneals produce a slow, monotonically increasing dopant density requiring long anneals to achieve dopant densities greater than $1\times10^{18}$ cm$^{-3}$.

For the higher anneal temperatures, dopant density rises by many orders of magnitude over a small time interval making it difficult to reliably obtain a given dopant density by varying the anneal time (especially for densities lower than $\approx 1\times10^{19}$ cm$^{-3}$). A better approach is to adjust the anneal temperature while fixing the anneal time to achieve a rough dopant density, and to adjust the anneal time for fine tuning.

The doping profile as a function of depth into the Si epilayer was determined

experimentally (Figure 2-10 blue triangles and red squares) by thinning a 50-nm Si epilayer (via $CF_4$-based RIE) in 10-nm increments and measuring the doping (via 4-point resistivity) after each increment. As expected, diffusion doping produces a dopant density gradient that falls rapidly with depth into the Si epilayer. Note that the infinitely-thick Si epilayer model (Figure 2-10, dashed line) agrees well with experiment over most of the epilayer thickness (Figure 2-10, blue triangles).

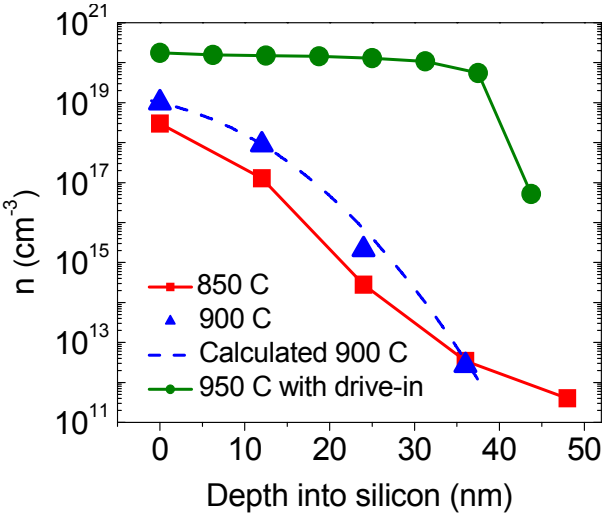


**Figure 2-10. Dopant density vs. depth for 50 nm SOI substrates with and without dopant drive-in**. Si epilayers that were diffusion doped as normal (triangles and squares) show a rapid decrease in dopant density with depth as expected from calculation (dashed line). SOI subjected to an additional dopant drive-in step as described in the text show a more homogeneous dopant density with depth (circles).

This dopant density gradient will be transferred to SNAP-fabricated Si NWs from diffusion-doped SOI epilayers, and can be very useful for nanoelectronic applications. For instance, the dopant density and hence the conductivity along the length of SNAP-fabricated Si NWs can be tuned very simply by etching the NW surface in regions where the conductivity is to be decreased. The appropriate etch depth to achieve a given doping density can be determined from a dopant density vs. depth plot corresponding to the anneal time and temperature of the starting SOI epilayer.

The ability to spatially control the conductivity of SNAP-fabricated Si NWs has important applications in NW crossbar circuit architectures. Si NWs can be made highly-

doped in regions where electrical signals must propagate and moderate- to lowly-doped in regions that need to be responsive to field-effect gating. This becomes especially important when tiling together multiple nanoelectronic functional blocks fabricated from a single array of NWs. In Chapter 3, I describe the application of this technique to a FET-based demultiplexer.

There are applications where a homogeneous dopant density is desired. For instance, in Chapter 4, I describe the fabrication of an ultra-dense memory circuit made from crossed NW arrays in which Si NWs are unavoidably etched but must nonetheless maintain robust conductivity. In cases such as this, the dopant density can be homogenized with a secondary high-temperature anneal. After diffusion-doping as usual, approximately 250 nm of $SiO_2$ is deposited over the SOI surface. I frequently used plasma-enhanced chemical deposition (PECVD) for this step. This oxide layer prevents out-gassing of dopant atoms during a second anneal at 1000° C for 10–15 minutes. Due to the long anneal time and high temperature of this step, I used a tube-furnace and an argon ambient. If perfect homogeneity is not required, a shorter anneal at 1000° C will suffice. (Most RTAs are capable of staying at 1000° C for 2 minutes.) Figure 2-10 (dark green circles) reveals that the dopant density vs. depth profile after drive-in is nearly constant throughout the 50-nm Si player (the abrupt drop in dopant density at 45-nm depth may be due to increased surface resistance from RIE damage and/or uneven etching of the surface).

## 2.5 Concluding remarks

As described in this chapter, the SNAP technique is a highly versatile NW fabrication protocol capable of producing dense arrays of aligned NWs over millimeter length scales. Furthermore, because SNAP is a 'top-down' technique, NWs can be fabricated from any thin-film material that can be anisotropically dry-etched. The physical properties of the NWs are thus derived from those of the starting thin-film material. In this chapter, the SNAP technique was used to fabricate high-quality Si NW arrays with specific surface orientation through the use of (100)- or (111)-oriented Si epilayers. In addition, through the use of diffusion doping and surface resistivity measurements, which are only possible with a bulk surface, the electrical properties of the NWs could be precisely determined and controlled. This is in contrast to catalytically grown NWs where, in general, the doping is unknown before NW fabrication and can be difficult to determine afterwards. In the next chapter, I describe how the highly ordered nature of SNAP-fabricated NWs enables the development of binary tree demultiplexing architectures capable of electrically addressing a single NW from within a dense array. In chapter 4, I describe how the unique capability of SNAP to pattern NWs from thin-film materials can be used to construct an ultra-dense molecular electronic memory circuit.

In addition to the work described in this thesis, the SNAP technique could be used to pattern more exotic thin-film materials. For instance, SNAP could be used to define nanoscale ribbons from two-dimensional graphene, a recently discovered form of graphite only a single atomic layer thick with exciting electrical characteristics[38].

## 2.6 References


1. Wang, D., Sheriff, B. A. & Heath, J. R. Silicon p-FETs from Ultrahigh Density Nanowire Arrays. Nano Lett. (2006).
2. Cui, Y., Zhong, Z. H., Wang, D. L., Wang, W. U. & Lieber, C. M. High performance silicon nanowire field effect transistors. Nano Letters 3, 149–152 (2003).
3. Duan, X. F., Huang, Y., Cui, Y., Wang, J. F. & Lieber, C. M. Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices. Nature 409, 66–69 (2001).
4. Singh, N. et al. High-performance fully depleted silicon-nanowire (diameter <= 5 nm) gate-all-around CMOS devices. Ieee Electron Device Letters 27, 383–386 (2006).
5. Zheng, G. F., Lu, W., Jin, S. & Lieber, C. M. Synthesis and fabrication of high-performance n-type silicon nanowire transistors. Advanced Materials 16, 1890 (2004).
6. Ng, H. T. et al. Single crystal nanowire vertical surround-gate field-effect transistor. Nano Letters 4, 1247–1252 (2004).
7. Cui, Y. & Lieber, C. M. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. Science 291, 851–853 (2001).
8. Huang, Y., Duan, X. F., Cui, Y. & Lieber, C. M. Gallium nitride nanowire nanodevices. Nano Letters 2, 101–104 (2002).
9. Husain, A. et al. Nanowire-based very-high-frequency electromechanical resonator. Applied Physics Letters 83, 1240–1242 (2003).
10. Melosh, N. A. et al. Ultrahigh-density nanowire lattices and circuits. Science 300, 112–115 (2003).
11. Pauzauskie, P. J., Sirbuly, D. J. & Yang, P. D. Semiconductor nanowire ring resonator laser. Physical Review Letters 96, (2006).
12. Mcalpine, M. C., Friedman, R. S. & Lieber, C. M. High-performance nanowire electronics and photonics and nanoscale patterning on flexible plastic substrates. Proceedings of the Ieee 93, 1357–1363 (2005).
13. Huang, Y. et al. Logic gates and computation from assembled nanowire building blocks. Science 294, 1313–1317 (2001).
14. Wang, D. W., Sheriff, B. A. & Heath, J. R. Complementary symmetry silicon nanowire logic: Power-efficient inverters with gain. Small 2, 1153–1158 (2006).
15. DeHon, A. Array-based architecture for FET-based, nanoscale electronics. Ieee Transactions on Nanotechnology 2, 23–32 (2003).
16. DeHon, A. Deterministic addressing of nanoscale devices assembled at sublithographic pitches. Ieee Transactions on Nanotechnology 4, 681–687 (2005).
17. Stan, M. R., Franzon, P. D., Goldstein, S. C., Lach, J. C. & Ziegler, M. M. Molecular electronics: From devices and interconnect to circuits and architecture. Proceedings of the Ieee 91, 1940–1957 (2003).
18. Lee, M. H., Kim, Y. K. & Choi, Y. H. A defect-tolerant memory architecture for molecular electronics. Ieee Transactions on Nanotechnology 3, 152–157 (2004).

19. Ziegler, M. M. et al. in Molecular Electronics Iii 312–330 (New York Acad Sciences, New York, 2003).
20. Dai, H. J. Carbon nanotubes: opportunities and challenges. Surface Science 500, 218–241 (2002).
21. McEuen, P. L., Fuhrer, M. S. & Park, H. K. Single-walled carbon nanotube electronics. Ieee Transactions on Nanotechnology 1, 78–85 (2002).
22. Arnold, M. S., Green, A. A., Hulvat, J. F., Stupp, S. I. & Hersam, M. C. Sorting carbon nanotubes by electronic structure using density differentiation. Nat Nano 1, 60–65 (2006).
23. Morales, A. M. & Lieber, C. M. A laser ablation method for the synthesis of crystalline semiconductor nanowires. Science 279, 208–211 (1998).
24. Lu, W. & Lieber, C. M. Semiconductor nanowires. Journal of Physics D-Applied Physics 39, R387–R406 (2006).
25. Wu, Y. et al. Controlled growth and structures of molecular-scale silicon nanowires. Nano Letters 4, 433–436 (2004).
26. Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J. F. & Lieber, C. M. Diameter-controlled synthesis of single-crystal silicon nanowires. Applied Physics Letters 78, 2214–2216 (2001).
27. Whang, D., Jin, S., Wu, Y. & Lieber, C. M. Large-scale hierarchical organization of nanowire arrays for integrated nanosystems. Nano Letters 3, 1255–1259 (2003).
28. Beckman, R. A. et al. Fabrication of conducting Si nanowire arrays. Journal of Applied Physics 96, 5921–5923 (2004).
29. Green, J. E. et al. A 160-kilobit molecular electronic memory patterned at 10(11) bits per square centimetre. Nature 445, 414–417 (2007).
30. Fukata, N. et al. Formation of hydrogen-boron complexes in boron-doped silicon treated with a high concentration of hydrogen atoms. Physical Review B 72 (2005).
31. Handbook of Semiconductor Manufacturing Technology (eds. Nishi, Y. & Doering, R.) (Marcel Dekker, Inc., New York, 2000).
32. Bryce, C. & Berk, D. Kinetics of GaAs dissolution in H2O2-NH4OH-H2O solutions. Industrial & Engineering Chemistry Research 35, 4464–4470 (1996).
33. Moon, E.-A., Lee, J.-L. & Yoo, H. M. Selective wet etching of GaAs on $Al_xGa_{1-x}As$ for AlGaAs/InGaAs/AlGaAs pseudomorphic high electron mobility transistor. Journal of Applied Physics 84, 3933–3938 (1998).
34. Juang, C., Kuhn, K. J. & Darling, R. B. Selective etching of GaAs and Al[sub 0.30]Ga[sub 0.70]As with citric acid/hydrogen peroxide solutions. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 8, 1122–1124 (1990).
35. Pristovsek, M. et al. Gallium-rich reconstructions on GaAs(001). physica status solidi (b) 240, 91–98 (2003).
36. Sze, S. M. Physics of Semiconductor Devices (John Wiley & Sons, 1999).
37. Christensen, J. S. in Materials and Semiconductor Physics (Royal Institute of Technology, Stockholm, 2004).
38. Berger, C. et al. Electronic Confinement and Coherence in Patterned Epitaxial Graphene. Science 312, 1191–1196 (2006).

# Appendix 2.1: Experimentally determined doping data for 25, 31 and 50 nm SOI

| *n-type 25 nm SIMOX* | | | *p-type 25 nm SIMOX* | | |
|---|---|---|---|---|---|
| ***doping ($cm^{-3}$)*** | ***temp ($^oC$)*** | ***time (min)*** | ***doping ($cm^{-3}$)*** | ***temp ($^oC$)*** | ***time (min)*** |
| mid $10^{15}$ | 800 | 3 | mid $10^{15}$ | 700* | 4* |
| mid $10^{16}$ | 800 | 4 | mid $10^{16}$ | 750 | 3 |
| high $10^{16}$ | 800 | 5 | high $10^{16}$ | 750 | 4 |
| low $10^{17}$ | 800 | 6 | low $10^{17}$ | 750* | 6* |
| mid $10^{17}$ | 800 | 7 | mid $10^{17}$ | 750* | 7* |
| high $10^{17}$ | 850 | 4 | high $10^{17}$ | 800* | 3* |
| low $10^{18}$ | 850 | 5 | low $10^{18}$ | 800 | 4 |
| mid $10^{18}$ | 900 | 5 | mid $10^{18}$ | 800* | 5* |
| high $10^{18}$ | 900 | 8 | high $10^{18}$ | 850 | 3 |
| low $10^{19}$ | 900 | 9 | low $10^{19}$ | 900* | 2 |
| mid $10^{19}$ | 950 | 6 | mid $10^{19}$ | 900 | 6 |
| high $10^{19}$ | 1000 | 7 | high $10^{19}$ | 1000 | 5 |

| *n-type 31 nm SIMOX* | | | *p-type 31 nm SIMOX* | | |
|---|---|---|---|---|---|
| ***doping ($cm^{-3}$)*** | ***temp ($^oC$)*** | ***time (min)*** | ***doping ($cm^{-3}$)*** | ***temp ($^oC$)*** | ***time (min)*** |
| mid $10^{15}$ | 880 | 3 | mid $10^{15}$ | 830* | 3* |
| mid $10^{16}$ | 830 | 4 | mid $10^{16}$ | 780* | 4* |
| high $10^{16}$ | 830 | 5 | high $10^{16}$ | 780* | 5* |
| low $10^{17}$ | 830 | 6 | low $10^{17}$ | 780* | 6* |
| mid $10^{17}$ | 830 | 7 | mid $10^{17}$ | 780* | 7* |
| high $10^{17}$ | 830 | 8 | high $10^{17}$ | 780* | 8* |
| low $10^{18}$ | 880 | 4 | low $10^{18}$ | 830* | 4* |
| mid $10^{18}$ | 880 | 5 | mid $10^{18}$ | 830* | 5* |
| high $10^{18}$ | 880 | 6 | high $10^{18}$ | 830* | 6* |
| low $10^{19}$ | 930 | 6 | low $10^{19}$ | 880* | 6* |
| mid $10^{19}$ | 980 | 4 | mid $10^{19}$ | 930 | 4 |
| high $10^{19}$ | 1000 | 7 | high $10^{19}$ | 950 | 7* |

| *n-type 50 nm SIMOX* | | | *p-type 50 nm SIMOX* | | |
|---|---|---|---|---|---|
| ***doping ($cm^{-3}$)*** | ***temp ($^oC$)*** | ***time (min)*** | ***doping ($cm^{-3}$)*** | ***temp($^oC$)*** | ***time (min)*** |
| mid $10^{15}$ | 850 | 1 | mid $10^{15}$ | 700* | 2* |
| mid $10^{16}$ | 800 | 2 | mid $10^{16}$ | 750* | 2* |
| high $10^{16}$ | 800 | 3 | high $10^{16}$ | 750 | 3 |
| low $10^{17}$ | 850 | 2 | low $10^{17}$ | 800 | 2 |
| mid $10^{17}$ | 850 | 3 | mid $10^{17}$ | 800 | 3 |
| high $10^{17}$ | 850 | 3.5 | high $10^{17}$ | 800* | 3.5* |
| low $10^{18}$ | 900 | 1.5 | low $10^{18}$ | 850* | 1.5* |
| mid $10^{18}$ | 900 | 2.5 | mid $10^{18}$ | 850* | 2.5* |
| high $10^{18}$ | 875 | 4 | high $10^{18}$ | 825 | 4 |
| low $10^{19}$ | 900 | 4 | low $10^{19}$ | 850 | 4 |
| mid $10^{19}$ | 950 | 4 | mid $10^{19}$ | 850 | 6 |
| high $10^{19}$ | 1000 | 7 | high $10^{19}$ | 1000 | 6 |

* Extrapolated or best estimate