SIGNAL GENERATION AND PROCESSING IN HIGH-FREQUENCY / HIGH-SPEED SILICON-BASED INTEGRATED CIRCUITS

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Hui Wu

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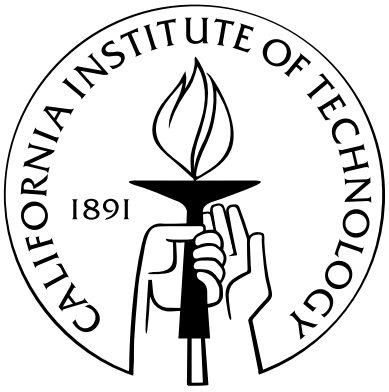

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Abstract

High-frequency/high-speed integrated circuits become increasingly important because of the strong demand for higher data rate and lower power consumption, and they rely more on silicon-based technologies, which has the advantages of low cost, fast technological development and system-on-a-chip (SoC) capabilities. However, silicon technologies also present great challenges in high-frequency/high-speed integrated circuits. This work demonstrated that distributed circuit and injection locking are two enabling circuit techniques that can help overcome silicon limitations.

Distributed voltage-controlled oscillators (DVCO's) demonstrated the high-frequency capabilities of distributed circuits. The operation of distributed oscillators is analyzed and the general oscillation condition is derived, resulting in analytical expressions for the oscillation frequency and amplitude. Two tuning techniques are developed, namely, the inherent-varactor tuning and delay-balanced current-steering tuning. A complete analysis of the tuning techniques is also presented. CMOS and bipolar DVCO prototypes have been designed and fabricated in a commercial $0.35\mu m$ BiCMOS process. A 10-GHz CMOS DVCO achieves a tuning range of 12% and a phase noise of -103 dBc/Hz at 600 kHz frequency offset. A 12-GHz bipolar DVCO achieves a tuning range of 26% and a phase noise of -99 dBc/Hz at 600 kHz frequency offset. New DVCO architectures are also proposed to improve the performance.

The distributed circuit technique is also used for equalization in high-speed fiber-optic systems, in which inter-symbol interference (ISI) caused by fibre dispersion imposes a major limitation. Compared to optical-domain methods and other electrical-domain methods, equalization with distributed transversal filters (DTF's) presents the most cost-effective and SoC-compatible solution. Prototype DTF's have been implemented in a commercial $0.18\mu m$ SiGe BiCMOS process for 10 Gpbs fiber-optic systems. A 7-tap DTF reduces the ISI of a 10 Gbps signal after 800m $50\mu m$ multi-mode fiber from 5 dB to 1.38 dB, and

improves the BER from 10^{-5} to 10^{-12}.

The injection locking technique is applied in high-speed, low-power frequency dividers, namely, injection-locked frequency dividers (ILFD's). Based on the detailed analysis, shunt-peaking and oscillation-suppression techniques are developed to enhance the locking range. Prototypes are implemented in a commercial $0.35\mu m$ BiCMOS process using only CMOS transistors. A 19 GHz ILFD achieves a locking range of 1350 MHz with the power consumption of 1 mW. A 9 GHz ILFD achieves a locking range of 1490 MHz with the power consumption of 1.3 mW. Self-dividing oscillators are proposed to generate accurate low-phase-noise quadrature signals.

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Chapter 1

Introduction

In the next decade, wireless communications promises to become the locomotive driving the electronics industries, like what personal computers and Internet did in the 80's and 90's [1]. The progress in both personal mobile communications and wireless broadband Internet access will lead to a new ubiquitous wireless communications [2]. The backbone of this wireless infrastructure will be the next-generation fiber-optic communications. With such promising prospects, high-frequency/high-speed integrated circuits have become among the most active research areas with strong industry demands and fast technological advances.

1.1 High Frequency and Wideband

All these applications require higher data rate, which follows the trend through the history of communications (Fig. 1.1). According to Shannon's information capacity theorem ($C = BW \cdot log_2(1 + SNR)$), the capacity of a point-to-point communication channel is largely limited by its bandwidth[1]. Therefore, increasing the bandwidth is a convenient way to achieve the high data rate, e.g., for the fast-growing broadband data services in wireless communications. In practice, the required bandwidth needs to be in frequencies that have favorable propagation properties, which are mostly in the low-GHz range. Unfortunately, most bands within this spectrum range have already been allocated [4].

To circumvent the regulation barrier, unlicensed Industrial-Scientific-Medical (ISM) bands are widely used. For example, 802.11b wireless LAN and Bluetooth share the 2.4GHz ISM band with cordless phones and microwave ovens [4]. However, squeezing more applica-

[1]Recently there is some argument on the issue of *spectrum shortage* [3]. Nevertheless, bandwidth is still one of the most important communications resources in the near future.

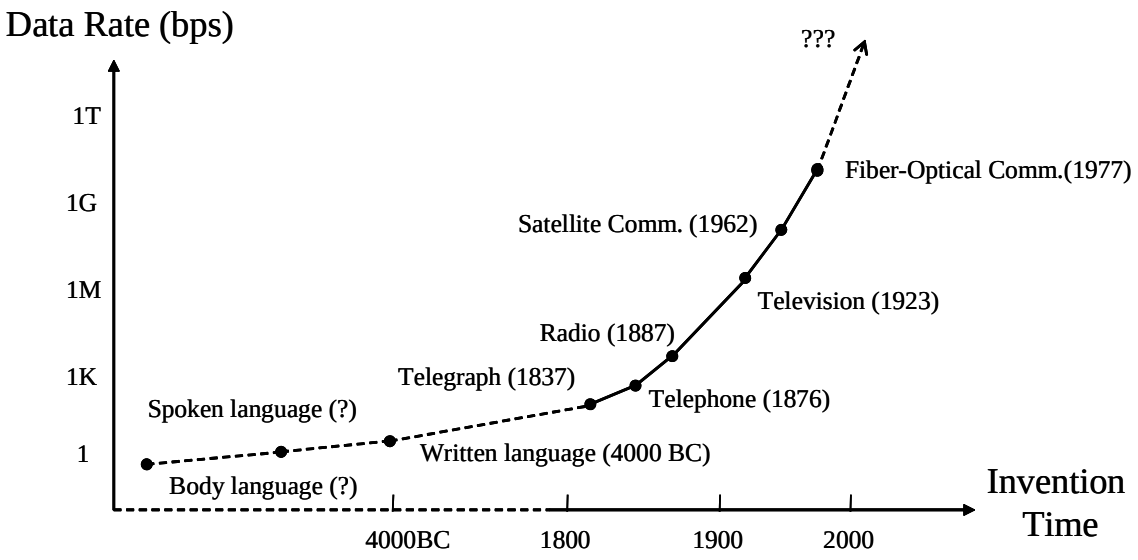


Figure 1.1: Evolution of Communication

tions into these crowded ISM bands seems increasingly problematic because of interference concerns. Another approach is to improve *spectral efficiency* (bit/s/Hz) by using more advanced coding, modulation and multiple-access techniques (e.g., spread spectrum [5], OFDM [6], space-time coding [7]). In practice, the approach has trade-offs between spectral efficiency and system complexity. The third option is the more radical Ultra Wideband (UWB) [8], which can potentially achieve very high data rate (500Mbps). However, its range is limited due to the power level and interference constraints, and thus can be used only in short-range applications.

Therefore, an arguably more fundamental solution is to move to higher frequencies, where more bandwidth is readily available. For example, the unlicensed band at 60GHz can provide 5GHz bandwidth (59-64GHz), which is significant compared to the ISM bands at 2.4GHz (80MHz) or 5.8GHz (150MHz) [4]. However, it presents a new challenge, i.e., how to achieve both high frequency operation and wide bandwidth at the same time.

1.2 High Frequency and High Speed

Historically, *high frequency*[2] is associated with RF/microwave systems, while *high speed* is linked with digital systems, particularly computers. They are considered totally different

[2]Throughout this text,*high frequency* is used in its literal meaning, instead of as the technical term, *HF*.

fields. High-frequency RF systems used to have narrow bandwidth relative to their carrier frequencies. Digital systems operate in the baseband, and are described using data-rate instead of bandwidth, which is theoretically from half data-rate down to dc according to Nyquist's Sampling Theorem and in practice with some overhead. Correspondingly, different design techniques and methodologies have been developed in these two areas. RF design tends to use frequency-domain methods and S-parameters, while digital circuits rely on time-domain models and SPICE-type simulations.

The technology progress, however, is changing these assumptions and blurring the boundary between these two fields. On one hand, cell phones and other wireless products have dominated RF market. Driven mostly by the unsatiable demand for capacity from service providers and data contents from users, the bandwidth used by these RF systems increases constantly, and broadband systems are on the rise. On the other hand, high-speed digital circuits also reach a point that circuits cannot be treated simply as binary logic gates – the interconnects have become the performance bottleneck, which is essentially an analog/RF problem.

Therefore, the overlap between these two fields become more and more evident. It is in this context that we want to address the challenges of high-frequency/high-speed silicon-based IC design to showcase that the same analog circuit techniques and methodologies can be used successfully in both fields.

1.3 System-on-a-Chip

In the history of telecommunications, the technology advances in microelectronics, digital computers, and lightwave systems are all responsible for the spectacular improvements on system performance, such as sensitivity, selectivity, capacity, power consumption, reliability, and cost. In the meantime, there is also a constant increase in system complexity (Fig.1.2), which is considered the price paid for performance improvements. For example, modern digital communications relies heavily on sophisticated coding, modulation, and multiple-access techniques to achieve the best performance. The resulted implementations require powerful digital-signal-processing (DSP) subsystems in addition to complex RF frond-end circuitry. The latter usually needs additional analog or digital control circuits, such as automatic gain control (AGC), digital calibration, and power control circuits, to meet stringent

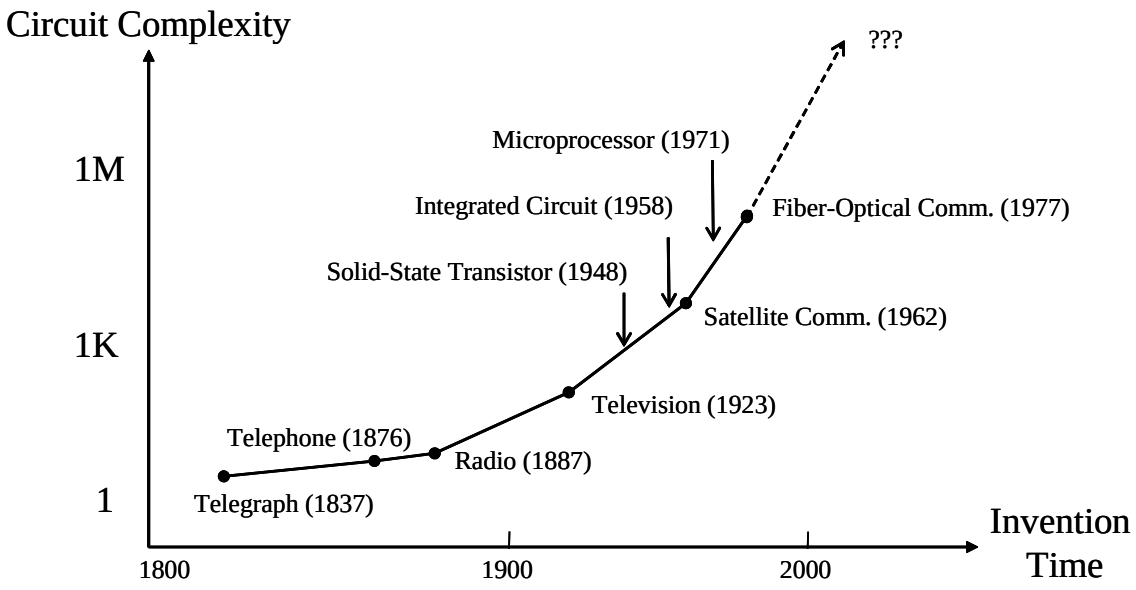


Figure 1.2: Evolution of Telecommunications

specifications.

It is always a challenge to cost-effectively implement such complex communications systems. Conventionally, the baseband DSP modules are implemented as separate integrated circuits from analog/RF modules. The latter might be partitioned further into more IC's or even discrete components. Then all these modules are assembled into systems on circuit boards. This approach definitely has its own advantages:

- Different process technologies can be used for different modules.
- Each module can be designed and optimized separately for its target process technology to achieve its best performance.
- Interference between modules can be minimized.

In recent years, however, *system-on-a-chip* (SoC) has emerged as a strong contender in communications systems because of the rapid progress in process technologies, and the bottom-line economics. SoC can greatly reduce the system size in terms of board area and component count, simplify the system design by reusing modules from previous designs or IP cores from outside sources, and thus shorten the time-to-market, lower the cost, and enhance the product portability. In addition, SoC has the following distinctive advantages in communication systems:

- No bottleneck from inter-chip interfaces. In the conventional approach, packages, bondwires or flip-chip bumps on the path of high-frequency/high-speed signals introduce extra parasitic capacitance and inductance, and thus seriously compromise the system performance and largely limit the design space.

- 50-ohm standard in RF systems also complicates matters because additional circuitry needs to be added to match the internal impedance, which is usually higher than 50-ohm, with 50-ohm interface. For example, in a system-on-a-board radio, extra buffers are added between the off-chip VCO and on-chip mixer to compensate for the parasitics and match the 50-ohm interface, even though both circuits might have high internal impedances.

- Power consumption can be greatly reduced. First, the power used by the interface I/O circuitry is largely saved. Secondly, there is no need to convert to 50-ohm in RF subsystems, and correspondingly smaller signal power is required and less buffers are needed. Lastly, all the power-saving techniques (*e.g.*, current sharing) can be fully employed.

- New circuits are possible with the blessing of extra design freedom. For example, self-dividing oscillators (see section 5.4) in this work.

Therefore, it seems that SoC is the inevitable future of communication systems. It is crucial to study the design of high-frequency/high-speed communication circuits in the context of SoC.

1.4 High Power Efficiency

As both the data rate and system complexity of communications increase, power consumption becomes increasingly critical,[3] particularly in wireless communications because of the mobility requirement. Advances in both process technologies and circuit techniques are needed to address this problem. While technologies set the fundamental limit on the power consumption, only smart circuit design can ever approaching this limit. In other words, bet-

[3]Here the discussion is limited to the power consumption for circuit operation, and does not include that due to leakage current, which itself has become one of the major obstacles for CMOS to continue scaling down.

ter circuit techniques can enable the use of low-cost technologies to achieve power consumption comparable to those using more advanced technologies but inferior circuits. Therefore, instead of simply optimizing conventional circuit topologies, new circuit techniques must be explored to achieve *high power efficiency*.[4]

1.5 Why Silicon?

It is amazing that most of the new process technologies under development are silicon-based, e.g., deep-sub-micron CMOS, silicon germanium(SiGe) BiCMOS, silicon-on-insulator(SOI), silicon carbide (SiC), to name the most important ones. In the competition with traditional III-V compound semiconductors, including gallium arsenide (GaAs), indium phosphide (InP), and most recently gallium nitride (GaN) [9], it seems that silicon technologies are catching up (Table 1.1) [10][11][12].

Despite lower carrier mobility, vast investments in research and infrastructure of silicon process have enabled fast advances in transistor speed, which has followed Moore's Law in the past 30 years and most likely into the next decades. SiGe HBT's have achieved speed performances comparable to GaAs HBT's, and SOI transistors are even approaching InP in term of transistor cut-off frequencies. To be fair, GaAs and InP technologies are also breaking their own records and making new progress. Nevertheless, silicon processes have achieved the capability to implement most commercial RF circuits in terms of speed.

Silicon's real strength lies in its SoC capability. In fact, BiCMOS, SiGe, and possibly CMOS are the only feasible SoC solutions for communication systems. GaAs and InP lag far behind silicon technologies in device density and yield. VLSI on III-V semiconductors is still far from reality. This situation is unlikely to improve in the near future.

Lastly, silicon technologies have a large cost advantage. Lower substrate cost, higher yield, and much heavier infrastructure investments are all responsible for the lower cost per chip area on silicon. More importantly, silicon's SoC capability can dramatically reduce the total system cost, including design and fabrication by eliminating external components and reduce the board area.

[4]This is a more accurate and generic term than simply low power. For example, a highly-efficient power amplifier may not qualify for low power. Accordingly, a good quantitative metric would be *power added efficiency* (PAE), the ratio between the output power and the sum of dc power consumption and input power.

	Silicon			III-V		
Characteristic	CMOS 0.13 μm	SiGe BiCMOS 0.18 μm	SOI CMOS 0.13 μm	GaAs HBT (power device)	InP HBT 1 μm	InP HEMT 0.15 μm
f_T (GHz)	105	120	145	25	160	130
f_{max} (GHz)	NA	100	160	50	200	185
$NF_{min}(dB)$	0.7@2GHz	0.4@2GHz	<1@5GHz	NA	NA	1.4@26GHz
Breakdown Voltage (V)	<2.5	1.8	2.5	14	NA	4
Substrate resistance (ohm-cm)	10	10	10-2000	1M	1M	1M
Cost	Low	Medium	NA	Medium	High	High
SoC	Good	Good	Good	Difficult		

Table 1.1: State-of-Art Semiconductor Technologies

It is noteworthy that III-V semiconductors will still play important roles in applications that require extremely high frequency, extremely low noise, or high power. In the mainstream communication system market, however, silicon technologies seem to have more advantages.

1.6 Challenges

There are many challenges in high-frequency/high-speed circuit design because of fundamental physical limitations. SoC design on silicon makes it a more difficult task. Firstly, the cutting-edge specifications required by modern communication systems still go beyond the capabilities of current silicon technologies using conventional design techniques. For example, SONET OC-768 [13], the next-generation fiber-optic communication technology, have a bit-rate of 40 Gb/s and a bandwidth about 30 GHz, which presents a big challenge for transistor speed because conventional circuits can hardly achieve such large gain-bandwidth product. Even if the latest silicon technology can reach the required speed, the associated high cost and large power consumption render it far from attractive. Therefore, it is necessary to develop new circuit techniques that can achieve high-frequency/high-speed operation using the most cost-effective silicon technology and consuming less power.

Another important issue is on-chip passive components (including spiral inductors, capacitors, varactors, and resistors) and interconnect (transmission lines). Compared to their discrete counterparts, on-chip passive components suffer from larger energy loss (low Q), inferior absolute accuracy, and higher vulnerability to process and temperature variations. Semiconducting silicon substrate further deteriorates the situation by increasing the loss of spiral inductors and transmission lines and lowering their self-resonance frequency. There-

fore, it is necessary to develop new circuit techniques that can overcome these inherent difficulties in silicon technologies and achieve the goal of SoC.

Last but not the least, accurate models for transistors and on-chip passive devices operating at high frequency or high speed are still lacking, simply because the technology progress is so fast that theoretic understanding and CAD modeling for these devices are still under development. For example, accurate modeling of on-chip transmission lines on silicon substrate is still an open question both in theory and practice. Therefore, it is necessary to develop new design methodologies that can take these constraints into account and achieve successful and robust designs despite the inaccuracies.

This work is trying to address the challenges mentioned above. We developed several new circuit techniques along with design methodologies, namely, distributed voltage-controlled oscillators with current-steering delay-balanced tuning (10 GHz and above), injection-locked frequency dividers with shunt-peaking enhancement (19 GHz), self-dividing oscillators (21 GHz), and distributed transversal equalizer (10 Gbps). Circuit prototypes have been successfully implemented using CMOS and SiGe BiCMOS technologies and demonstrated the new circuit techniques and design methodologies.

1.7 Organization

In Chapter 2, we introduce the two important circuit techniques in this work: distributed circuit and injection locking, as well as basic oscillator theory.

Chapter 3 presents distributed voltage controlled oscillators as a good candidate for high-frequency low-noise signal generation. Basic distributed oscillators are analyzed, leading to general expressions for the amplitude and frequency conditions. Tuning techniques (inherent-varactor tuning and current-steering delay-balanced tuning) will be demonstrated. The design and layout issues of DVCO's will also be discussed, followed by experimental results of several prototypes, including a 10 GHz CMOS DVCO and a 12 GHz bipolar DVCO. Finally, several novel DVCO architectures will be discussed.

In Chapter 5, injection-locked frequency dividers are presented as the alternative solution for high-speed dividers, which have lower power consumption and better noise performance than conventional digital dividers. Based on locking-range analysis, two prototype divide-by-2 ILFD's with shunt-peaking locking-range enhancement are demonstrated. Quadrature

signal generation is discussed. Lastly, self-dividing oscillators will be presented as a new type of low-phase-noise quadrature oscillators.

Chapter 4 presents integrated transversal equalizers based on distributed circuit techniques for high-speed fiber-optical communications. The dispersion problem and compensation techniques are discussed, with the emphasis on adaptive equalization and its implementations. The design of integrated transversal equalizers is further discussed with detailed analysis on transmission lines and gain stages, followed by measurement results for a 4-tap and 7-tap 10 Gb/s prototypes.

Chapter 2

Basic Theory and Techniques

In this chapter, we introduce two important circuit techniques, namely, *distributed circuit* and *injection locking*, which form the two main themes in this work: the distributed circuit technique is applied in voltage controlled oscillators (Chapter 3) and transversal equalizers (Chapter 4); the injection locking technique is applied to frequency dividers and a new type of oscillators (Chapter 5). Since our application of distributed circuits is distributed oscillators, and injection locking is a nonlinear behavior of oscillators, we also discuss the basic theory of oscillators (especially phase noise) in this chapter.

2.1 Distributed Amplifiers

Distributed amplification (also known as traveling-wave amplifiers) was first conceived by Percival [14] in 1936 and clearly presented by Ginzton [15] in 1948. In the next 30 years, extensive research and development efforts [16][17] have been made with great success in amplification, pulse instrumentation, oscillography, radar systems, particle detection, broadband communication systems and various applications that require wideband amplification with good phase linearity [18]. In early 80's, distributed amplifiers were successfully implemented as monolithic microwave integrated circuits (MMIC's) [19], which inspired a new wave of exploration, including study of theory and design guidelines [20][21][22][23], noise analysis [24], application of new devices [25], new circuit techniques [26][27][28][29][30], and new records [31][32]. Recently, distributed amplifiers have also been implemented in state-of-art silicon technologies [33][34][35] – it has become a tradition that whenever a new technology becomes available, it would be used for distributed amplifier applications, which vividly demonstrates the timeless significance of distributed amplification.

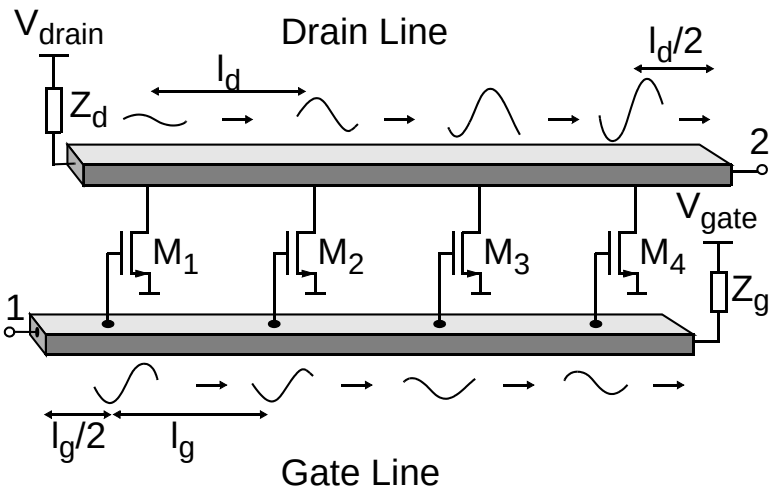


Figure 2.1: Basic distributed amplifier.

The strength of a distributed amplifier resides in its ability to deliver, from a given device technology, a gain-bandwidth product not easily achievable by other circuit configurations. For a single-stage lumped amplifier, the gain-bandwidth product is limited by $g_m/\pi\ C$ [36][18], where g_m is the transconductance of the device, and $C = lim_{\omega\to\infty}\,(1/j\omega\ Z)$ (Z is the load impedance), which is determined by the parasitic capacitance. Thus this maximum achievable gain-bandwidth product (*Bode-Fano Limit* [37]) is mainly determined by the intrinsic parameters of the devices. Cascading several stages of the *same* amplifier does not increase the gain-bandwidth product since the gain is close to unity at frequencies close to the bandwidth. If amplifiers with different load impedance characteristics are cascaded, a larger bandwidth might be achieved [38]. However, this usually comes with the price of lower gain within the bandwidth, and thus it is unlikely that Bode-Fano Limit is violated. On the contrary, a distributed amplifier achieves a potentially larger gain-bandwidth product by "absorbing" the parasitic capacitances of transistors into transmission line structures, which form a high-order LC ladder filter, while combining the gain from all devices. In other words, the gain of a distributed amplifier increases with the number of active devices (limited by the loss from the transmission line structures), while the bandwidth stay almost constant. The price for this gain-bandwidth-product enhancement is the larger time delay (latency) for the amplifier. These characteristics will become clear after the analysis.

2.1.1 Architecture

A basic distributed amplifier consists of two transmission lines, the gate line and drain line, and gain transistors[1] coupled between them, as shown in Fig. 2.1. The input signal travels forward (to the right in Fig. 2.1) along the gate line, and is amplified by each transistor. The amplified signals travels on the drain line in both directions. The forward traveling-waves on the drain line is in synchronization with the traveling-wave on the gate line and each other. In other words, each transistor adds power *in phase* to the output signal at each tap point on the drain line. The forward traveling-wave on the gate line and the backward (to the left Fig. 2.1) traveling-wave on the drain line are absorbed by terminations, which are usually matched to the characteristic impedance of the *loaded* gate line and drain line, respectively.

2.1.2 Basic Analysis

Refer to Fig. 2.1. Assuming that the number of transistors on the line is large and their spacing is much smaller than the wavelength, their input and output capacitances may be considered distributed. The characteristic impedance of the gate line Z_g is given by

$$Z_g \approx \sqrt{\frac{j\omega L_g + R_g}{j\omega(C_g + \frac{c_{in}}{l_g}) + G_g}} \tag{2.1}$$

where L_g, R_g, C_g, G_g are the series inductance and resistance, and parallel capacitance and conductance of the gate transmission line per unit length, respectively, and c_{in} is the small signal input capacitance of the amplifying stage, which is a MOS transistor in this case. A similar expression can be obtained for the characteristic impedance of the drain line Z_d, i.e.,

$$Z_d \approx \sqrt{\frac{j\omega L_d + R_d}{j\omega(C_d + \frac{c_{out}}{l_d}) + G_d}} \tag{2.2}$$

where L_d, R_d, C_d, G_d are the series inductance and resistance, and parallel capacitance and conductance of the drain transmission line per unit length, respectively, and c_{out} is the output capacitance of the amplifying stage.

The complex propagation constants of the transmission lines are also changed due to

[1] Although the discussion is carried out in MOS terminology, it is equally valid for implementations using other technologies.

the transistor loading, i.e.,

$$\gamma_g \approx \sqrt{(j\omega L_g + R_g) \cdot \left[j\omega (C_g + \frac{C_{in}}{l_g}) + G_g \right]} \tag{2.3}$$

$$\gamma_d \approx \sqrt{(j\omega L_d + R_d) \cdot \left[j\omega (C_d + \frac{c_{out}}{l_d}) + G_d \right]} \tag{2.4}$$

It can be seen from (2.1)-(2.4) that device parasitic capacitances are absorbed into the capacitive component of the transmission lines and therefore contribute mainly to the real part of Z_0 and imaginary part of γ, which do not induce loss.

The gain of the distributed amplifier can be calculated in the following way. Note that the voltage at the kth tap of the gate line (v_{gk}) is related to the gate lines segment length, l_g, and complex propagation constant of the loaded gate line, γ_g, through [39]

$$v_{gk} = v_1 e^{(k-\frac{1}{2})\gamma_g l_g} \tag{2.5}$$

where v_1 is the voltage at the input node 1 in Fig. 2.1. This is assuming that the gate line is terminated to Z_g on the right end. Also assuming that the drain line is terminated to Z_d on the left end, the wave going out of the drain of each transistor sees an impedance of $Z_d/2$, which is the parallel combination of the two Z_d's seen on the left and right. The generated wave at the kth drain tap traveling to the right is therefore given by:

$$E_{dk} = -g_m \frac{Z_d}{2} v_{gk} = -g_m \frac{Z_d}{2} v_1 e^{-(k-\frac{1}{2})\gamma_g l_g} \tag{2.6}$$

where g_m is the small signal transconductance of each transistor. Note that a simple g_m can be used to the first order since the transistor parasitic capacitances are primarily absorbed into the real part of Z_0 and imaginary part of γ. These generated waves travel through different lengths of drain line to reach the output node 2. Therefore, the total wave traveling

to the right at the output is given by superposition, i.e., [2]

$$\begin{aligned} E_{i2} &= \sum_{k=1}^{n} E_{dk} e^{-(n-k+\frac{1}{2})\gamma_d l_d} \\ &= -g_m \frac{Z_d}{2} v_1 \cdot \sum_{k=1}^{n} e^{-(k-\frac{1}{2})\gamma_g l_g} \cdot e^{-(n-k+\frac{1}{2})\gamma_d l_d} \\ &= -g_m \frac{Z_d}{2} v_1 \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \end{aligned} \tag{2.7}$$

where n is the number of transistors.

Part of this incident wave will be reflected due to the impedance mismatch at node 2, since in general the load impedance Z_L is different from Z_d. The reflected wave, E_{r2}, is related to the incident wave, E_{i2}, through the reflection coefficient, i.e.,

$$\Gamma_2 \equiv \frac{E_{r2}}{E_{i2}} = \frac{Z_L - Z_d}{Z_L + Z_d} \tag{2.8}$$

The voltage at node 2 is thus related to the incident wave by

$$v_2 = E_{i2} + E_{r2} = E_{i2} \cdot \frac{2Z_L}{Z_L + Z_d} \tag{2.9}$$

Combining (2.7) and (2.9), the following general expression for the voltage gain of the amplifier can be obtained:

$$A_v = \frac{v_2}{v_1} = -g_m (Z_L \| Z_d) \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \tag{2.10}$$

To gain more insight into (2.10), let us consider the special case where $\gamma l \equiv \gamma_d l_d = \gamma_g l_g$. This can be achieved by having different lengths and widths for the drain and gate lines in the design to guarantee that the product is the same on both lines. Then the voltage gain of (2.10) can be written as

$$\begin{aligned} A_v &= -n g_m (Z_L \| Z_d) \cdot e^{-\gamma n l} \\ &= -n g_m (Z_L \| Z_d) \cdot e^{-\alpha n l} \cdot e^{-j\beta n l} \end{aligned} \tag{2.11}$$

where , in which α and β are the attenuation and phase constant of the transmission lines,

[2] Using the identity $a^n - b^n = (a-b)(a^{n-1} + a^{n-2}b + ... + b^{n-1})$

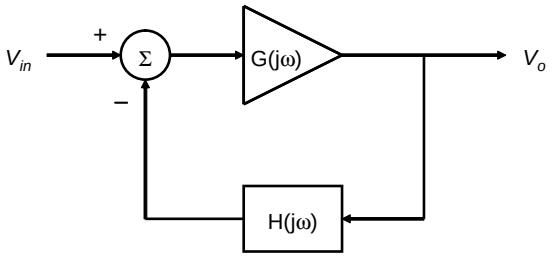


Figure 2.2: Basic feedback amplifier model of oscillators

respectively.

From (2.11) we can clearly see the basic characteristics of distributed amplifiers: (1) the gain increases with n; (2) the gain from each device is determined by g_m and load impedance ($Z_L \| Z_d$) like in a lumped amplifier; (3) the gain is also limited by the loss $e^{-\alpha nl}$ from the loaded transmission lines; (3) there is an extra time delay $e^{-j\beta nl}$, which increases with n.

2.2 Oscillators

Oscillators are intriguing electronic devices. Their beauty lies in the contrast between the simplicity in their circuit topology and the mystery in their theory as well as design. They are also used as one of the major benchmark circuits for evaluation of any new process technology.

2.2.1 Basic Theory of Oscillators

An electrical oscillator is a device that outputs periodic signals without any external excitation, i.e., it converts dc power into ac power at some harmonically-related frequencies.

The classic oscillator theory is based on a generalized *feedback amplifier model* (Fig. 2.2) [40], whose transfer function is given by:

$$\frac{V_o}{V_{in}} = \frac{G(j\omega)}{1 + G(j\omega)H(j\omega)} = \frac{G(j\omega)}{1 + T(j\omega)} \tag{2.12}$$

where $T(j\omega) = G(j\omega)H(j\omega)$ is the loop gain.

If the loop gain at some frequency makes the denominator in (2.12) equal to 0, the amplifier will violate Nyquist criterion of stability (or equivalently, Barkhausen criterion) and

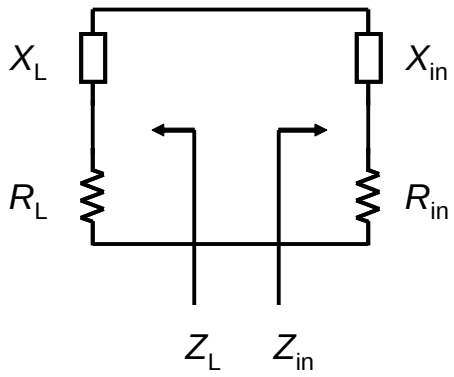


Figure 2.3: One-port negative resistance model of oscillators

become unstable. Thus any disturbance (initial condition or noise) will start the oscillation. At steady state, the oscillation condition satisfies:

$$T(j\omega) = -1 \tag{2.13}$$

or, expressed in amplitude and phase:

$$|T(j\omega)| = 1 \tag{2.14}$$

$$arg[T(j\omega)] = 180^\circ \tag{2.15}$$

For RF and microwave oscillators, the *one-port negative-resistance model* (Fig. 2.3) is more frequently used [41]. The oscillator is partitioned between the active device and its passive load, with the impedance of $Z_{in} = R_{in} + jX_{in}$ and $Z_L = R_L + jX_L$, where R_L and R_{in} are the load and input resistance, and X_L and X_{in} are the load and input reactance, respectively. Simply by applying Kirchhoff's voltage law, the oscillation condition can be expressed as:

$$Z_L + Z_{in} = 0 \tag{2.16}$$

which can be re-written as

$$R_L + R_{in} = 0 \tag{2.17}$$

$$X_L + X_{in} = 0 \tag{2.18}$$

Equation (2.17) states that the active device must compensate for the loss of the load,

and the oscillation amplitude is determined by the signal level at which $R_{in} = -R_L$, while (2.18) dictates that there must be zero (or multiple 360°) phase shift around the loop[3] and the oscillation frequency is determined when this phase condition is satisfied.

Both models can also be used to explain the oscillation startup and amplitude stability: oscillation starts by initial condition or noise when $|T(j\omega)| > 1$ and $\angle\, T(j\omega) = 0$, or equivalently, $R_L(j\omega) + R_{in}(j\omega) < 0$, and $X_L(j\omega) + X_{in}(j\omega) = 0$. Oscillation reaches the steady state when (2.13) or equivalently (2.16) is satisfied, i.e., the circuit is saturated by the signal amplitude and thus the loop gain drops to unity, or equivalently, the gain from the active device drops to the level that equals the total loss. Notice that neither model guarantees that there is only one oscillation frequency possible or any particular frequency is stable. This is because both models are basically linear models while oscillators are nonlinear circuits. Therefore, a more thorough study of oscillators has to resort to nonlinear differential equations [42][43]. This is particularly true when noise property of oscillators is involved.

Both models are valid for the same physical phenomenon. However, the one-port negative resistance model is more useful in the analysis of RF and microwave oscillators, because it is directly related to the circuit, and s-parameters can be applied. It also reveals more physical insight, especially when nonlinearity of active devices and startup conditions are concerned. Therefore, it is widely used in the practical design of high-frequency oscillators. There is also a *two-port approach* in microwave oscillator design, which is just an application of one-port negative-resistance model in circuits that use two-port active devices, e.g., transistors – both ports satisfies (2.16) simultaneously. Nevertheless, both feedback and negative-resistance models are useful in later chapters when we analyze distributed oscillators and conventional LC oscillators.

2.2.2 Phase Noise

The most important characteristic of oscillators is *frequency stability*. There are two types of frequency stability: long term and short term. Long-term frequency stability is caused by temperature variation and component aging, which is not our concern in this work. Short-term frequency stability is mainly affected by noise, including circuit intrinsic noise and interference from outside sources such as power supply fluctuation or substrate-coupled

[3]Notice that in Fig. 2.2 the loop is a negative feedback, and hence the minus sign.

noise. Short-term frequency stability is usually referred to as *phase noise* [44]. Phase noise performance of oscillators is critical in modern communication systems: in transmitters, it results in adjacent-channel interference and modulation errors; in receivers, it can result in demodulation errors and degraded sensitivity and dynamic range [45][46].

Phase noise is usually quantified using the power spectral density function (PSD) of the output signal around the oscillation frequency. It would be instructive to see how phase fluctuations is transferred into PSD. Equation (2.19) represents the output signal of a sinusoidal oscillator, in which the amplitude fluctuation is negligible compared to phase fluctuation, as in most practical oscillators.[4]

$$V_{osc}(t) = V_o \cos\left[\omega_0 t + \phi(t)\right] \tag{2.19}$$

Assuming the phase fluctuation is a single-tone sine wave $\phi(t) = \phi_p \sin \omega_m t$, and the phase fluctuation is small ($\phi_p \ll 1$), (2.19) can be expanded as

$$V_{osc}(t) = V_o\{\cos\omega_0 t - \frac{\phi_p}{2}[\cos\left(\omega_0 + \omega_m\right)t - \cos\left(\omega_0 - \omega_m\right)t]\} \tag{2.20}$$

Now, two frequency sidebands appear in the spectrum around the oscillation frequency. In fact, this is exactly the spectrum of a narrow-band frequency modulation (FM) signal. From (2.20), we can see that the phase fluctuation at low frequency ω_m is up-converted to $\omega_0 \pm \omega_m$, or equivalently, the oscillation signal is modulated by the phase fluctuation.

Convert it to noise-to-signal power ratio, we get the double-sideband (DSB) "phase noise" for this *deterministic* phase fluctuation. In the case of real noise, which is a random process, the auto-correlation function of oscillation signal can be used and then followed by a Fourier transform to find the phase noise.

$$\mathcal{L}(\omega_m) = (\frac{V_n}{V_o})^2 = \frac{\phi_p^2}{4} = \frac{\phi_{rms}^2}{2} \tag{2.21}$$

where ϕ_{rms} is the RMS value of $\phi(t)$.

Expression (2.21) is quite straight-forward – the real question is how noise (thermal

[4]This is because oscillators have inherent amplitude limiting mechanism due to the circuit nonlinearity, while no such limiting mechanism for phase fluctuation. Mathematically it comes from the fact that oscillators are autonomous systems, and thus any time-shifted solution still satisfies the nonlinear differential equations. It can be best visualized with a limit cycle in an amplitude-phase state-space.

noise, flicker noise, shot noise, etc.) is converted into phase fluctuation $\phi(t)$. Different models have been developed to address this problem. The earliest and probably most well-known model is Leeson's Formula [47] and its derivatives, which use a *linear-time-invariant* (LTI) approach,

$$\mathcal{L}(\Delta\omega) = \frac{2Fk_BT}{P_s} \cdot \left(\frac{\omega_0}{2Q_{loaded}\Delta\omega}\right)^2 \tag{2.22}$$

where P_s is the power dissipation in the loaded resonator, Q_{loaded} is the loaded quality factor of the resonator, and F is an empirical parameter usually derived from measurement data.

Hajimiri's model [44][48][49] further takes into account the time-variant nature of noise-phase-conversion, i.e.,

$$\phi(t) \propto \int_{-\infty}^{t} \Gamma(\omega_0\tau) i(\tau) d\tau \tag{2.23}$$

where $\Gamma(\omega_0\tau)$ is the *impulse sensitivity function*, i.e., the impulse response of phase fluctuation due to noise. Since it still assumes that the noise-phase-conversion is linear, it is called *linear-time-variant* (LTV) model of phase noise. Further, it can take into account the cyclostationary noise sources[5] and time-varying circuit parameters (such as parasitic capacitors of the active device) using an effective ISF [44]. For thermal noise, it gives

$$\mathcal{L}(\Delta\omega) = \frac{1}{2}\frac{\Gamma_{eff,rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{(\Delta\omega)^2} \tag{2.24}$$

where q_{max} is the maximum charge swing, $\overline{i_n^2}/\Delta f$ is a current noise source, and Γ_{eff} is the effective ISF.

Recently, Ham's phase noise model treated phase noise as *phase diffusion* [51], which leads to a more physical interpretation of phase noise, namely, *virtual damping* [52]. The same assumption of linear noise-phase-conversion is assumed, and results similar to more rigorous development by directly solving stochastic differential equations [53][54][55] is obtained.

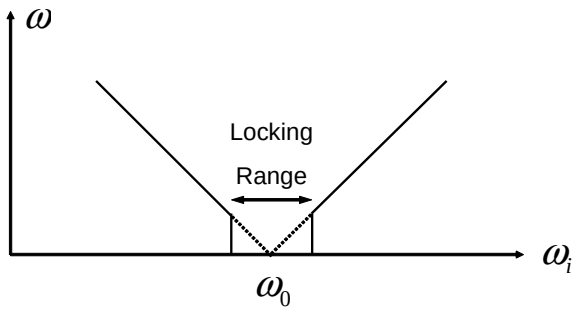


Figure 2.4: Injection Locking.

2.3 Injection Locking

Injection locking is a special type of forced oscillation in nonlinear oscillators (also known as *synchronization* or *frequency entrainment*). Suppose a signal of frequency ω_i is injected into an oscillator, which has a self-oscillation (free-running) frequency ω_0. When ω_i is quite different from ω_0, "beats" of the two frequencies are observed. As ω_i approaches ω_0, the beat frequency ($|\omega_i - \omega_0|$) decreases. When ω_i enters some frequency range very close to ω_0, the beats suddenly disappear, and the oscillator starts to oscillate at ω_i instead of ω_0. Fig. 2.4 shows this nonlinear behavior. The frequency range in which injection locking happens is called the *locking range*. Injection locking also happens when ω_i is close to the harmonic or subharmonic of ω_0, i.e., $n\omega_0$ or $\frac{1}{n}\omega_0$. They are called harmonic (or superharmonic) and subharmonic injection locking, respectively.

2.3.1 Basic Mathematical Analysis

Injection locking was first observed by Hyugens in 17th century in a mechanic phenomenon: clocks that are close enough can synchronize each other. In early 20th century, physicists rediscovered this phenomenon in electrical circuits. Since then injection locking has become a subject in standard textbooks on nonlinear theories [42]. Among various mathematical treatments of injection locking, the method developed by van der Pol [56] and its topological extension by Andronov and Witt [43] are very popular. The basic idea is the following ([57], chapter 7).

[5] *Cyclostationary* means that the statistics of a random process is time-varying[50].

A *forced* van der Pol oscillator can be expressed using a nonlinear differential equation:

$$\ddot{x} + \epsilon(x^2 - 1) + x = \Gamma \cos \omega t \tag{2.25}$$

The solution is assumed to be in the form[6] :

$$x(t) = a(t) \cos \omega t + b(t) \sin \omega t \tag{2.26}$$

where $a(t)$, $b(t)$ are slow-varying functions. Plug (2.26) into (2.25), neglect $\ddot{x}$, $\ddot{b}$ and higher harmonic terms, then the following equations can be obtained by using harmonic balance for $\sin(\omega t)$ and $\cos(\omega t)$,

$$\begin{aligned} (2\omega - \frac{1}{2}\epsilon ab)\dot{a} + \epsilon(1 - \frac{1}{4}a^2 - \frac{3}{4}b^2)\dot{b} &= \epsilon\omega a(1 - \frac{1}{4}r^2) - (\omega^2 - 1)b \\ -\epsilon(1 - \frac{3}{4}a^2 - \frac{1}{4}b^2)\dot{a} + (2\omega + \frac{1}{2}\epsilon ab)\dot{b} &= (\omega^2 - 1)a + \epsilon\omega b(1 - \frac{1}{4}r^2) + \Gamma \end{aligned} \tag{2.27}$$

where $r = \sqrt{(a^2 + b^2)}$. To facilitate the topological representation, replace the variables by $\nu = (\omega^2 - 1)/\epsilon\omega$, $\gamma = \Gamma/\epsilon\omega$, where ν is the measure of de-tuning, and γ represents the locking signal "energy". The equations for equilibrium points ($\dot{a} = \dot{b} = 0$) become

$$\begin{aligned} a(1 - \frac{1}{4}r^2) - \nu b &= 0 \\ \nu a + b(1 - \frac{1}{4}r^2) &= -\gamma \end{aligned} \tag{2.28}$$

which can be further degenerated into an autonomous equation

$$r^2\{\nu^2 + (1 - \frac{1}{4}r^2)^2\} = \gamma^2 \tag{2.29}$$

Equation 2.29 can be presented in a r^2-ν phase plane (Fig. 2.5), from which we can analyze the stability of the equilibrium points – injection locking can only happen at the stable equilibrium points.

- When $\gamma < 1.18$, and ν small enough, the system has three equilibrium points: a stable node, a saddle point, and a unstable spiral. Thus injection locking happens –

[6]Note that the van der Pol equation without the forcing term has a nearly-sinusoidal periodic solution with frequency of 1 when ϵ is small.

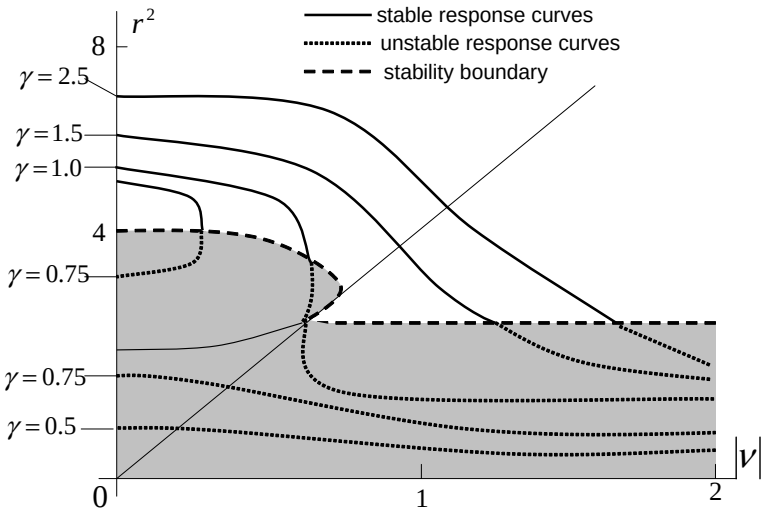
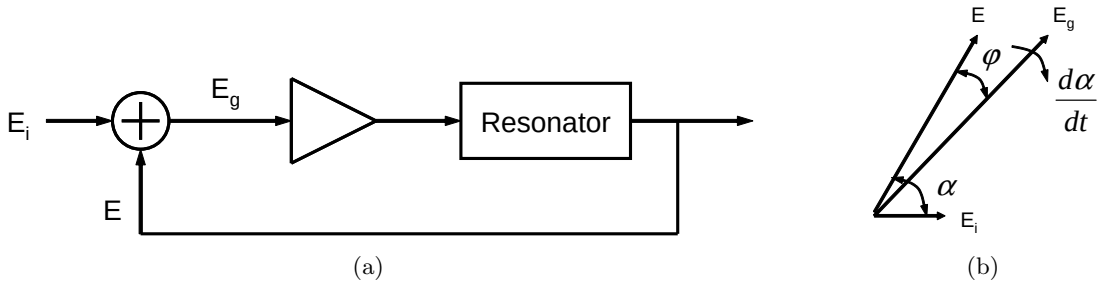


Figure 2.5: Topological representation of forced van der Pol oscillator.



(a) (b)

Figure 2.6: Adler's analysis of an injection-locked oscillator. (a) oscillator model; (b) phasor diagram of signals.

the system starting in the two unstable equilibrium points will evolve into the stable node.

- When $\gamma > 1.18$, and ν small enough, the system has only a stable equilibrium point, and thus injection locking can be established.

- When $\gamma > 1.18$, and ν large enough, there is only an unstable spiral. The system will enter a limit cycle in the $a(t)$-$b(t)$ phase plane, which corresponds to the beat phenomenon.

2.3.2 Locking range

Van der Pol's method is difficult to be effectively applied in practical circuits because it requires the exact nonlinear differential equation for the oscillator, which may not be easily

obtained. Instead, Adler developed a first-order nonlinear differential equation to describe the phase relationship between the injected signal and the injection-locked oscillator [58], which can be used to find the locking range as well as the transient process. It goes like the following.

The oscillator is modeled as a feedback amplifier with a resonator (Fig. 2.6a). The injection signal E_i is added to the feedback signal E, and the total signal is E_g, which are represented in phasor forms (Fig. 2.6b)[7]. Assuming $E_i \ll E$,

$$\phi = \frac{E_i \sin\alpha}{E} = \frac{E_i}{E}\sin\alpha \tag{2.30}$$

The instantaneous frequency of the oscillator can be found from the phase-frequency relation of the resonator. Assuming small frequency deviation $\frac{\omega-\omega_0}{\omega_0} \ll 1$,

$$\phi = \arctan\left(-2Q\frac{\omega-\omega_0}{\omega_0}\right) \approx -2Q\frac{\omega-\omega_0}{\omega_0} \tag{2.31}$$

The instantaneous beat frequency is

$$\frac{d\alpha}{dt} = \omega - \omega_i = (\omega-\omega_0) + (\omega_0-\omega_i) = (\omega-\omega_0) + \Delta\omega_0 \tag{2.32}$$

Then from (2.30), (2.31), it follows

$$\frac{d\alpha}{dt} = -\frac{E_i}{E}\frac{\omega_0}{2Q}\sin\alpha + \Delta\omega_0 \tag{2.33}$$

At steady state ($\frac{d\alpha}{dt} = 0$), the phase difference is

$$\sin a = 2Q\frac{E_i}{E}\frac{\Delta\omega_0}{\omega_0} \tag{2.34}$$

which immediately leads to the expression of locking range

$$\left|\frac{\Delta\omega_0}{\omega_0}\right| < \frac{1}{2Q}\cdot\frac{E_i}{E} \tag{2.35}$$

Thus the locking range is proportional to the injection signal amplitude, E_i, and inversely proportional to the quality factor Q and oscillation amplitude E. The assumptions ($E_i \ll E$

[7] In [58], the phase deviation is defined as $-\alpha$.

and $(\omega - omega_0)/\omega_0 \ll 1)$ were later removed in Paciorek's extended treatment [59].

2.4 Summary

In this chapter, distributed circuits and injection locking have been introduced. The advantages of distributed amplification has been discussed, and a basic distributed amplifier has been analyzed. The phenomenon of injection locking has been mathematically analyzed using van der Pol's method, and the locking range of injection locked oscillators has also been analyzed using Adler's equation. Finally the basic oscillator analysis and phase noise theory were discussed. These discussions will facilitate our study in later chapters.

Chapter 3

Distributed Voltage-Controlled Oscillators

This chapter is dedicated to distributed voltage-controlled oscillators. The motivation behind distributed oscillators is introduced Section 3.1, followed by the basic architecture and analysis in Section 3.2.3. The latter leads to general expressions for the oscillation amplitude and frequency. Two novel tuning techniques, namely, *inherent varactor tuning* and *current-steering delay-balanced tuning*, will be demonstrated in Section 3.3, which enable *distributed voltage-controlled oscillators* (DVCO's) to be realized. The design and layout issues of DVCO's will be discussed in Section 3.4, followed by experimental results of several prototypes, including a 10 GHz CMOS DVCO and a 12 GHz bipolar DVCO, in Section 3.5. Finally, several novel DVCO architectures will be discussed in Section 3.6.

3.1 Voltage-Controlled Oscillators

A *voltage controlled oscillator* (VCO) is an oscillator whose frequency can be varied by a control signal (usually a voltage). VCO's are essential building blocks in modern communication systems. For example, they are widely used in clock generation and distribution,

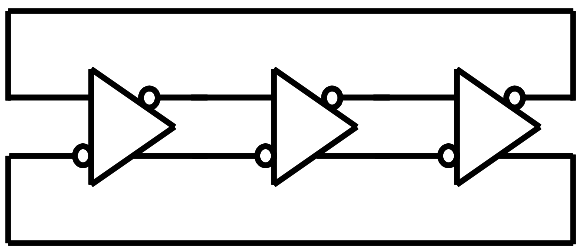


Figure 3.1: Block Diagram of a Ring Oscillator

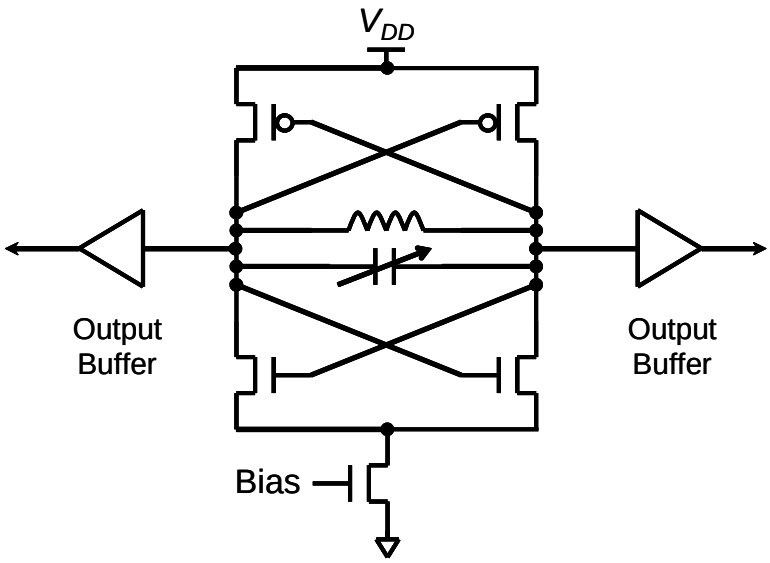


Figure 3.2: Schematic of a LC Oscillator

frequency synthesizers, as well as clock-and-data recovery circuits. Almost all electronic oscillators in communications are VCO's (except those that are used as the frequency reference, e.g., crystal oscillators), because frequency tuning is an essential feature of oscillators – most oscillators in these systems are used in some phase-locked loops to control their frequency accuracy and stability. In fact, even crystal oscillators are usually voltage-controlled (VCCO's) to compensate temperature variations. More importantly, the specified tuning range of an oscillator is usually considerably larger than the required operation range to accommodate process and temperature variations as well as inaccurate modeling.

VCO's can be specified into two categories: resonator-less oscillators and resonator-based oscillators. A ring oscillator (Fig. 3.1) is an example of resonator-less oscillators, which consist of a cascade of inverting gain stages. Ring oscillators can generate quadrature signals very easily, but suffer from inferior noise performance because their effective Q is close to unity, and there are noise active and passive devices in the signal path [49]. Thus resonator-less oscillators are seldom used in RF applications.

On the contrary, resonator-based oscillators offer better phase noise performance for a given power dissipation. The resonators can be made of surface-acoustic-wave (SAW) filters, transmission lines, or LC tanks. LC oscillators (Fig. 3.2) are quite popular in RF applications because of their simple structure and reasonably-good phase noise performance.

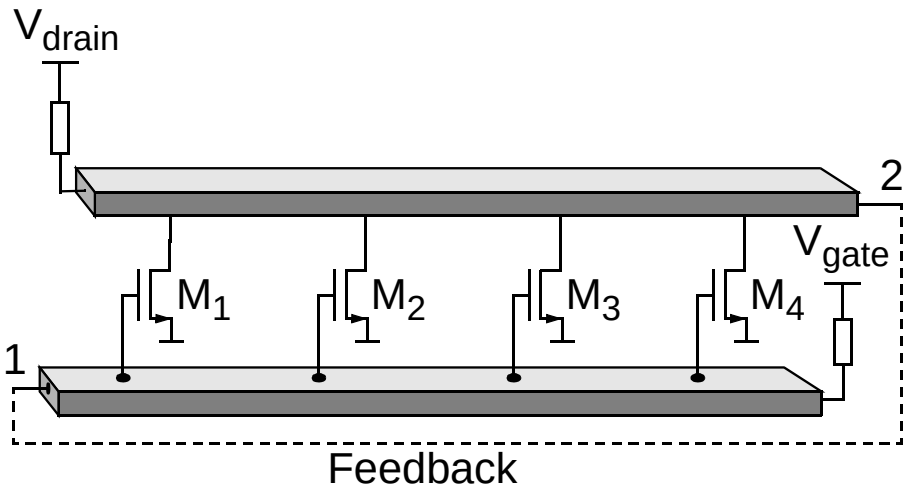


Figure 3.3: Basic distributed oscillator.

3.1.1 Challenges in High-Frequency VCO's

However, it becomes more difficult to achieve all the desired VCO specifications simultaneously as the frequency of operation approaches the self-resonance frequency of the on-chip inductors and the maximum oscillation frequency of transistors, f_{max}. More specifically, to operate at higher frequencies, the tanks LC product should decrease. However, the inductor loss, parasitic capacitances of transistors and loading from the next stage (e.g., output buffers) do not scale at the same rate. This results in the choice of even smaller L, which corresponds to larger power dissipation for a given oscillation amplitude, and more stringent constraints on the tuning capability of such an LC VCO [60]. These limitations make it necessary to pursue alternative approaches, such as distributed oscillators.

3.2 Distributed oscillators

A distributed oscillator can be formed by feeding the output (node 2) of a distributed amplifier back to its input (node 1) as shown in Fig. 3.3. Alternatively, it can also be considered as several oscillators with synchronized power combination, and each of them uses part of the power-combining transmission lines as its resonator.

3.2.1 Why distributed oscillators ?

From Section 3.1.1, we have seen the formidable challenges in high-frequency VCO design on silicon, namely, transistor speed limit (f_{max}), low-Q passive devices (on-chip inductors

and varactors), and wideband tuning capability. There is a strong demand for alternative solutions other than conventional LC oscillators.

Since a distributed amplifier can have a bandwidth close to f_{max}, a properly-designed distributed oscillator correspondingly can operate at frequencies close to f_{max}. This is a substantial improvement compared to current LC oscillators, which usually operates up to a smaller fraction of f_{max}[1]. Therefore, distributed oscillators are very attractive in extremely-high-frequency applications, e.g., the proposed broadband wireless communications at 60 GHz [61].

In addition, distributed oscillators can also be used in applications at lower frequencies that requires substantial amount of digital signal processing, e.g., fiber-optic communication systems at 2.5Gb/s (OC-48). In such a small-RF-with-big-digital scenario, a mainstream silicon process (i.e., CMOS) instead of a state-of-art one, is the sound choice technically and economically because of its good SoC capability and low cost. The limited transistor speed, however, makes it difficult to achieve the required oscillator performance using conventional designs. The situation is further complicated by the fact that these mainstream CMOS processes are developed specifically for digital circuits, and thus (1) are optimized for higher f_T instead of f_{max}; (2) usually have a low-resistivity substrate to prevent latch-up, which means even lower Q for on-chip inductors. A distributed oscillator can be used in these technologies to achieve the required oscillator performance.

Also, from Fig. 3.3, it is immediate clear that through a proper choice of the number of stages, a distributed oscillator can generate multiple-phase signals. This is a very desirable characteristic. For example, quadrature LO signals are required in most modern digital communication systems, while conventional VCO's usually generate differential signals. Thus there is usually a *quadrature generation circuit* in current radios, which consists of a pair of divide-by-2 digital dividers or poly-phase filters [45]. In the former case, the VCO has to operate at $2f_0$ instead of f_0, where f_0 is the required LO frequency – a large amount of power is wasted for the $2f_0$ oscillation frequency and power-hungry high-speed digital dividers (See Section 5.1). In the latter case, poly-phase filters introduces additional loss and noise. On the contrary, a distributed oscillator can generate the quadrature signals

[1]The maximum oscillation frequency f_{max} is the frequency at which the unilateral power-gain becomes unity [41]. Since transistors are not conjugated matched in LC oscillators as required in the definition of unilateral power gain, the power gain in this case is lower than the unilateral power gain, and hence the achievable oscillation frequency is lower than f_{max}.

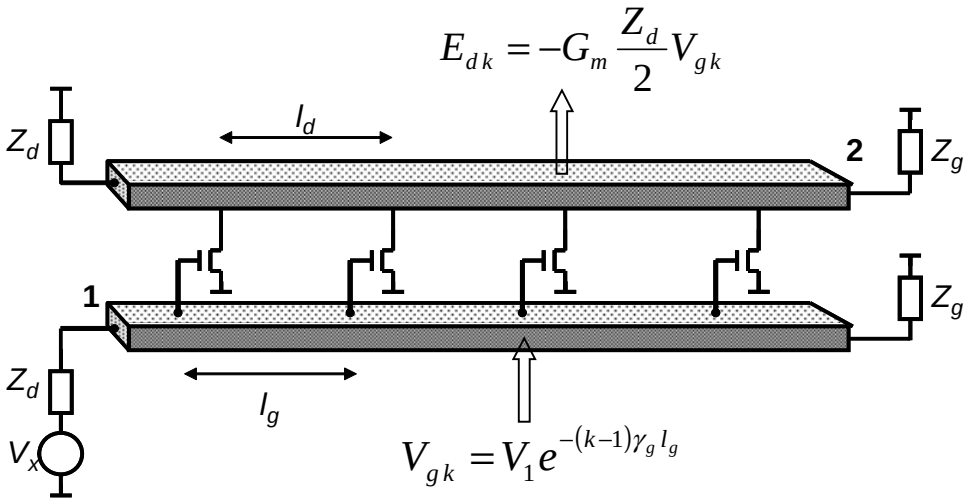


Figure 3.4: Equivalent circuit of an open-loop distributed oscillator

without any additional effort.

3.2.2 History

It is surprising that the development of distributed oscillators was a very recent event, considering that applying distributed circuit techniques in oscillators seems to be so appealing. In 1992, Skvor, et al [62] proposed to build a VCO by operating a distributed amplifier in the *reverse gain mode*, feeding the signal from the drain dummy load back to the gate line. A discrete 4 GHz distributed oscillator was demonstrated using four discrete GaAs pHEMT's[2] and microstrip lines on a printed circuit board [63]. Recently, using the forward gain mode, Kleveland, et al [64] showed a 0.18 μm CMOS distributed oscillator at 17 GHz with off-chip terminations and without any tuning capability.

Despite these advances, it is not clear how integrated distributed oscillators using low-speed silicon transistors can be tuned without significantly lowering the loop gain and hence increasing the power dissipation for reliable operation. Therefore, it is necessary to devise new tuning techniques for such distributed voltage controlled oscillators (DVCO's). Also, a systematic and analytical approach to the design of DVCO's is needed to be able to make accurate a *priori* predictions of frequency and amplitude.

3.2.3 Analysis

Breaking the feedback loop at nodes 1 and 2, the distributed oscillator of Fig. 3.3 reduces to the distributed amplifier of Fig. 2.1 with a load impedance $Z_L = Z_g$ and a source impedance of $Z_s = Z_d$ (Fig. 3.4). The voltage gain is given by (2.10), which is repeated here:

$$A_v = \frac{v_2}{v_1} = -g_m(Z_L \| Z_d) \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \tag{3.1}$$

Assuming that the feedback path is ac short circuit[3], the ac voltages at nodes 1 and 2 should be equal at steady-state. Therefore, the large signal gain from 1 to 2 should be unity ($A_v = 1$), which can be approximately calculated from (3.1) by replacing the small signal g_m with the large signal transconductance of each transistor, G_m, using the *describing function* method as defined in [40]. Then, the following general oscillation condition is obtained:

$$G_m \cdot (Z_L \| Z_d) \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} = -1 \tag{3.2}$$

This complex equality determines both the amplitude and the frequency of the oscillation. In the special case of equal propagation properties for both lines, i.e., $\gamma_d l_d = \gamma_g l_g \equiv \gamma l$, (3.2) reduces to

$$G_m \cdot (Z_L \| Z_d) \cdot n \cdot e^{-\alpha n l} \cdot e^{-j\beta n l} = -1 \tag{3.3}$$

where $\gamma = \alpha + j\beta$.

3.2.3.1 Frequency Condition

Assuming that the characteristic impedances for the gate and drain lines are real, the phase condition from (3.6) becomes

$$e^{-j\beta n l} = -1 \tag{3.4}$$

or

$$n l \beta = \pi \tag{3.5}$$

[2]Pseudomorphic high electron mobility transistor.

[3]This is a valid assumption since the feedback path should only introduce negligible loss and then there is only a phase shift term missing in the expression, which can also be very small, e.g., if the feedback path is implemented using a large ac coupling capacitor.

Noting that $\beta = 2\pi f/v_{phase}$, the oscillation frequency is:

$$f_0 \approx \frac{v_{phase}}{2nl} \approx \frac{1}{2nl\sqrt{LC}} \tag{3.6}$$

where $v_{phase} \approx 1/\sqrt{LC}$ is the phase velocity in the line, L and C are the inductance and the capacitance per unit length of the *loaded* transmission lines, respectively.

Several observations can be made on (3.6):

- Intuitively, the oscillation frequency is determined by the round-trip time delay, i.e., the time it takes the wave to travel through the transmission lines and then get amplified by one of the transistors. Thus (3.6) makes intuitive sense as $2nl$ is the total length of the transmission lines in the oscillator and the v_{phase} is the propagation velocity of the wave on the lines. However, the signal only travels through an effective length of nl around the feedback loop. The factor of 2 is caused by the extra phase shift due to the inverting gain of transistors. Therefore, if $\gamma_d l_d \neq \gamma_g l_g$, the oscillation frequency can be estimated by calculating the average gate and drain line propagation delays, i.e.,

$$\begin{aligned} f_0 &\approx \left(\frac{nl_g}{v_g} + \frac{nl_d}{v_d}\right)^{-1} \\ &\approx 1/[nl_g\sqrt{L_g\left(C_g + \frac{c_{in}}{l_g}\right)} + nl_d\sqrt{L_g\left(C_d + \frac{c_{out}}{l_d}\right)}] \end{aligned} \tag{3.7}$$

  where

$$\begin{aligned} v_d &\approx 1/\sqrt{L_d\left(C_d + \frac{c_{out}}{L_d}\right)} \\ v_g &\approx 1/\sqrt{L_g\left(C_g + \frac{c_{in}}{L_g}\right)} \end{aligned} \tag{3.8}$$

  are the phase velocities on the loaded gate line and drain line, respectively. The accuracy of (3.7) is verified in Section 3.5.

- Equation (3.6) can be written as $f_0 \approx 1/2\sqrt{L_{tot}C_{tot}}$, where $L_{tot} = nlL$ and $C_{tot} = nlC$ are respectively the inductance and capacitance of the loaded transmission lines in the feedback path. If we compare (3.6) to an LC oscillator , whose frequency is

$f_0 = 1/2\pi\sqrt{LC}$, a distributed oscillator can (1) achieve an oscillation frequency π times higher with the same LC product, or (2) use a π^2 times larger "LC tank" to achieve the same frequency. The latter greatly relieves the design constraint we discussed in Section 3.1.1.

- $f_0 = \pi f_c/2n$, or $f_0/f_c = \pi/2n$, where $f_c = 1/(l\sqrt{LC})$ is the cutoff frequency of the *periodically-loaded* transmission line and represents the pessimistic estimate for the maximum achievable frequency for a distributed oscillator. The smaller f_0/f_c, the more accurate the distributed assumption is. This implies that for a given frequency, a larger number of smaller transistors (larger n), and hence a smaller section length, l, would result in a smaller f_0/f_c ratio and hence a frequency and amplitude closer to those predicted by (3.6)-(3.7).

3.2.3.2 Amplitude Condition

The magnitude part of (3.3) can be solved for G_m to determines the amplitude. Noting that for amplitude, V_{amp}, much larger than quiescent gate overdrive, $V_{GS} - V_T$, the large signal transconductance is $G_m \approx 2I_D/V_{amp}$ [65]. Assuming that Z_g and Z_d is real, the oscillation amplitude is given by

$$V_{amp} \approx \frac{2I_D}{G_m} \approx 2nI_D(Z_g \| Z_d)e^{-\alpha nl} \tag{3.9}$$

where $e^{-\alpha nl}$ represents the loss on the transmission lines. This expression is valid for both MOS and bipolar implementations of the oscillator as long as the amplitude is large. It is noteworthy that (3.9) reduces to the expression for the amplitude of a lumped oscillator [65] for $n = 1$.

The above analysis is based on the assumption that the transistor loading can be treated as distributed over the total length of the transmission lines. Although this is strictly valid only for a large number of transistors, the derived oscillation conditions result in valuable design insights.

3.3 Tuning techniques

According to (3.6), the oscillation frequency is proportional to the phase velocity of the loaded transmission lines, v_{phase}, and inversely proportional to the total length of trans-

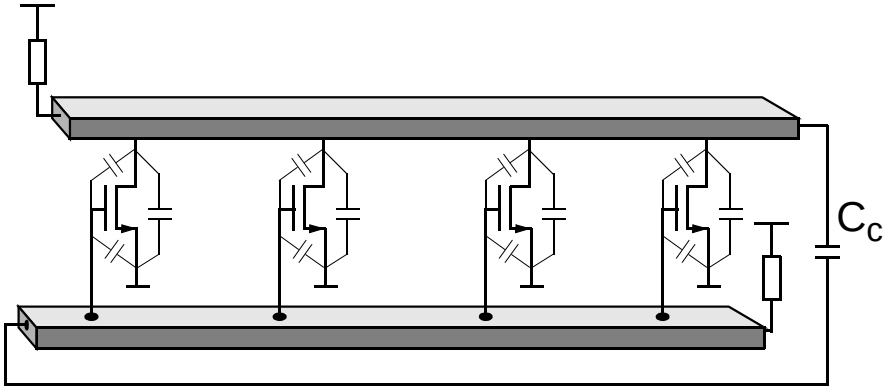


Figure 3.5: Inherent varactor tuning.

mission lines, $2nl$. This leads to two approaches for frequency tuning: changing the phase velocity, and/or changing the effective length of the transmission lines.

3.3.1 Inherent Varactor tuning

The most straightforward way of changing the phase velocity is by introduction of explicit varactors on the transmission lines and hence changing the phase velocity, $v_{phase} \approx 1/\sqrt{LC}$. Unfortunately, this approach suffers from a severe reduction in the oscillation frequency due to the extra zero-bias capacitance added to the lines which does not contribute to the tuning. This will cancel the advantages obtained by using a distributed structure, namely, higher operation frequency. Also the quality factor, Q, of the varactors significantly degrades at higher frequencies which makes them even more undesirable.

Fortunately, the parasitic capacitances of transistors can be used as inherent varactors. Therefore, by varying the dc voltage on the transistors, we can change these parasitic capacitances to tune the oscillation frequency. However, if applied blindly, the changes in the control voltage will change the dc operating point of the transistors, and thus vary their transconductance and output resistance. This will in turn change the oscillation amplitude, which is an undesirable effect. Therefore any tuning technique should guarantee stable operation point with changes in the control voltage. This goal can be achieved by biasing the transistors using current sources.

Tuning can be achieved by adjusting the dc level of the gate-line or drain-line in Fig. 3.5, while maintaining a constant quiescent current using current source biasing as will be shown in the next subsection. It is essential to introduce an ac coupling capacitor, C_c, between the drain and gate lines to be able to control the dc voltages on the two lines independently.

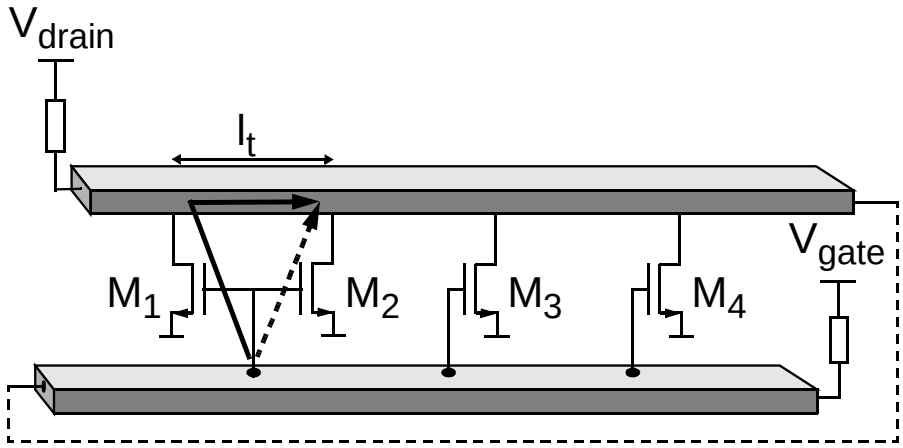


Figure 3.6: Path length adjustment tuning.

With this modification, it is possible to change the nonlinear capacitances of transistors (such as C_{gs} and C_{gd}) as well as their transconductance, g_m, by changing the dc voltages. Changes in C_{gd} have the largest effect on the tuning range as the voltage across C_{gs} does not change significantly due to the constant current biasing scheme. Circuit simulations confirm this observation.

3.3.2 Current-steering, delay-balanced tuning

An alternative way of changing the round-trip time delay is to change the length of the transmission lines. Although the physical length cannot be changed, the effective length can be varied, i.e., we can control and change the path for the waves to travel. The basic concept is shown in Fig. 3.6, where the gates of M_1 and M_2 are connected to the same point on the gate line while separated on the drain line by l_t. To understand the operation in this tuning mode, let us consider two limiting cases. In the first case, when M_1 is on and M_2 is off, the signal travels along the solid path. In the second extreme case when M_2 is on and M_1 is off, the signal travels along the dashed path. The latter is shorter than the former by l_t. Therefore, the round-trip time delay can be varied by selecting either the solid or dashed path, and thus the oscillation frequency can be tuned accordingly.

The path length adjustment can be implemented by current steering [66]. Fig. 3.7 shows a section of a DVCO using such tuning technique, which we call a drain-line-tuning (DLT) section. The gain transistors, M_a and M_b share the same tap point on the gate line, while their drains are connected to the drain line at two different points. The transistors are

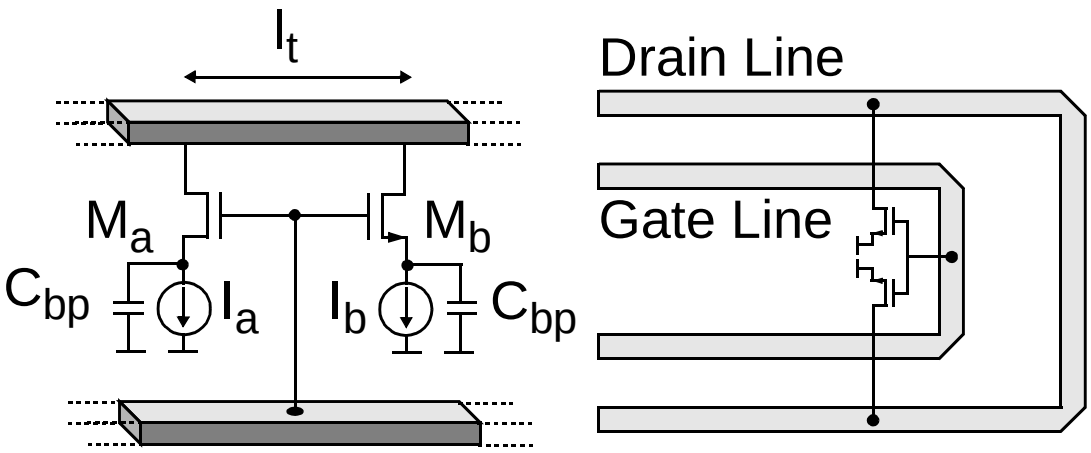


Figure 3.7: Drain line tuning (DLT) section.

biased using current sources I_a and I_b, and their sources are ac grounded using two bypass capacitors to maintain the high-frequency gain while suppressing the low-frequency parasitic oscillations. The bias current of each transistor is then controlled independently of the dc voltage on the gate and drain lines. The effective length of the drain line can be changed by varying the ratio of I_a and I_b to tune the oscillation frequency continuously. The difference between the minimum and maximum effective lengths of the drain line is controlled by l_t. Thus, the tuning range is determined by the ratio of l_t to the total length of transmission lines, as will be shown analytically. A U-turn structure can be used in the layout of a DLT to minimize the length of interconnection wires to the transmission lines and avoid extra unbalanced delay from these wires, as shown in Fig. 3.7.

A DVCO tuned by DLTs experiences the problem of delay mismatch as the transistor loading on the gate line is more concentrated than on the drain line. The delay mismatch is deteriorated by the fact that the gate capacitance is usually larger than the drain output capacitance. Also, the total length of the drain line is longer than the gate line if the U-turn structure is used which results in more delay mismatch. Therefore, the traveling wave on the drain line will lag the gate wave in phase. This phase mismatch between the gate and drain line affects the oscillators phase condition and makes it difficult for the oscillator to maintain phase shift around the loop. In other words, it degrades the synchronization of the waves on the gate and drain lines. If not resolved, this phase mismatch will degrade the phase noise and tuning range.

To remedy this problem, the delay mismatch between the gate and drain lines must be

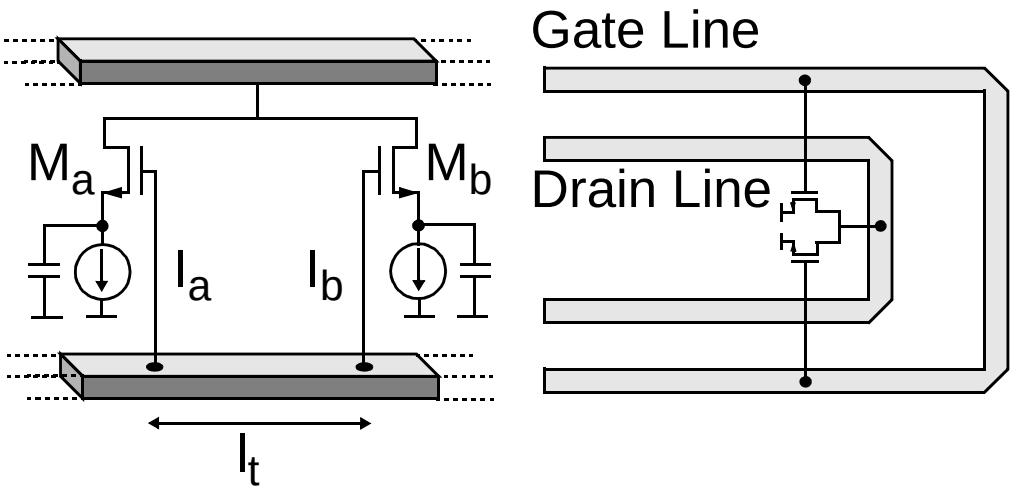


Figure 3.8: Gate line tuning (GLT) section.

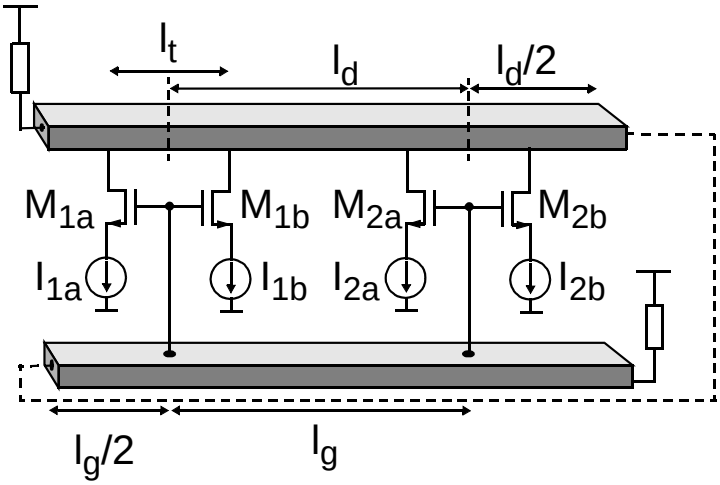


Figure 3.9: DVCO using DLTs.

minimized. This can be done using the structure of Fig. 3.8, which is complementary to that of Fig. 3.7 in that the gain transistors share the same drain tap point but are separated on the gate line by the same distance as the separation on the drain line of Fig. 3.7. We will refer to this structure as gate-line-tuning (GLT) section. A pair of these complementary sections can be used to cancel the delay mismatch. We will refer to this tuning technique as delay-balanced current-steering tuning.

Now we can extend the previous analysis of distributed oscillators to a DVCO using the current-steering tuning technique. For simplicity, we consider a DVCO with only DLTs (Fig. 3.9), assuming that there is no phase mismatch. The analysis of a delay-balanced DVCO with both DLTs and GLTs can also be performed using the same approach. The

bias currents of M_a in Fig. 3.7 and all the similar transistors in other DLTs are the same. We will refer to these transistors as group A and transistor M_b and its counterparts in the other DLTs as group B. The large signal transconductance of each transistor in group A and group B will be shown with G_{ma} and G_{mb}, respectively. An analysis similar to that of the original distributed oscillator of Fig. 3.3 will be applied to both groups to find the new oscillation condition in the presence of tuning. The resultant voltage at node 2 due to the transistors of group A is

$$v_{2a} = -G_{ma}V_1(Z_g\|Z_d)\cdot e^{-\gamma_d l_t/2}\cdot e^{-(\gamma_d l_d+\gamma_g l_g)/2}\cdot\frac{e^{-\gamma_d n l_d}-e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}-e^{-\gamma_g l_g}} \tag{3.10}$$

Similarly, for group B,

$$v_{2b} = -G_{mb}V_1(Z_g\|Z_d)\cdot e^{-\gamma_d l_t/2}\cdot e^{-(\gamma_d l_d+\gamma_g l_g)/2}\cdot\frac{e^{-\gamma_d n l_d}-e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}-e^{-\gamma_g l_g}} \tag{3.11}$$

Superimposing these two voltages, the following steady-state oscillation condition is obtained:

$$(G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{-\gamma_d l_t/2})\cdot(Z_g\|Z_d)\cdot e^{-(\gamma_d l_d+\gamma_g l_g)/2}\cdot\frac{e^{-\gamma_d n l_d}-e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}-e^{-\gamma_g l_g}} = -1 \tag{3.12}$$

In the special case of $\gamma l \equiv \gamma_d l_d = \gamma_g l_g$, (20) simplifies to

$$2n(Z_g\|Z_d)e^{-\gamma n l}(G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2}) = -1 \tag{3.13}$$

Assuming that $|\gamma l_t| \ll 1$, (3.13) can be re-written as

$$2n(Z_g\|Z_d)\cdot e^{-\alpha n l}\cdot e^{-j\beta n l}(G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2}) = -1 \tag{3.14}$$

Define

$$\begin{aligned} Ae^{j\theta} &= G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2} \qquad (3.15)\\ &= \cos\left(\frac{\beta l_t}{2}\right)(G_{ma}e^{-\alpha l_t/2}+G_{mb}e^{\alpha l_t/2})+j\sin\left(\frac{\beta l_t}{2}\right)(-G_{ma}e^{-\alpha l_t/2}+G_{mb}e^{\alpha l_t/2}) \end{aligned}$$

where

$$\theta \approx \tan\theta = \tan\left(\frac{\beta l_t}{2}\right)\cdot\frac{G_{mb}e^{\alpha l_t/2}-G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2}+G_{ma}e^{-\alpha l_t/2}} \tag{3.16}$$

Assume that $\beta l_t \ll 1$, the frequency condition becomes

$$-\beta nl + \frac{\beta l_t}{2} \cdot \frac{G_{mb}e^{\alpha l_t/2} - G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2} + G_{ma}e^{-\alpha l_t/2}} = -\pi \tag{3.17}$$

The frequency is given by

$$\begin{aligned} f &\approx \frac{v_{phase}}{2}\left(nl - \frac{l_t}{2} \cdot \frac{G_{mb}e^{\alpha l_t/2} - G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2} + G_{ma}e^{-\alpha l_t/2}}\right)^{-1} \\ &\approx \frac{v_{phase}}{2nl}\left(1 + \frac{l_t}{2nl} \cdot \frac{G_{mb}e^{\alpha l_t/2} - G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2} + G_{ma}e^{-\alpha l_t/2}}\right) \end{aligned} \tag{3.18}$$

If we further assume $\alpha\ l_t|||1$, (3.18) can be simplified as

$$f \approx \frac{v_{phase}}{2nl}\left(1 + \frac{G_{mb} - G_{ma}}{G_{mb} + G_{ma}} \cdot \frac{l_t}{2nl}\right) \tag{3.19}$$

As can be seen from (3.19), as long as l_t is small compared to the total length of the transmission line, the tuning range is directly proportional to the tuning length l_t. However, if l_t increases excessively, the phase difference between contributions from transistor groups A and B as well as the loss on l_t increase as can be seen from (3.13). Both effects decrease the total loop gain, and hence set a practical upper-bound for l_t.

3.4 Design of DVCO's

3.4.1 Transmission-line design

As we discussed in Section 1.6, one of the challenges in silicon-based VCO design is the lossy silicon substrate, which renders on-chip passive devices such as spiral inductors very lossy as well. This is also true for on-chip transmission lines. However, compared to spiral inductors, transmission lines [4] have lower loss and less parasitic capacitance for the same inductance value[67]. The latter translates into higher cut-off frequency (f_c). Nevertheless, transmission-line design and modeling is still critical in the design of DVCO's.

[4] On-chip transmission lines which are used as inductive elements sometimes are referred to as *slab inductors* [67].

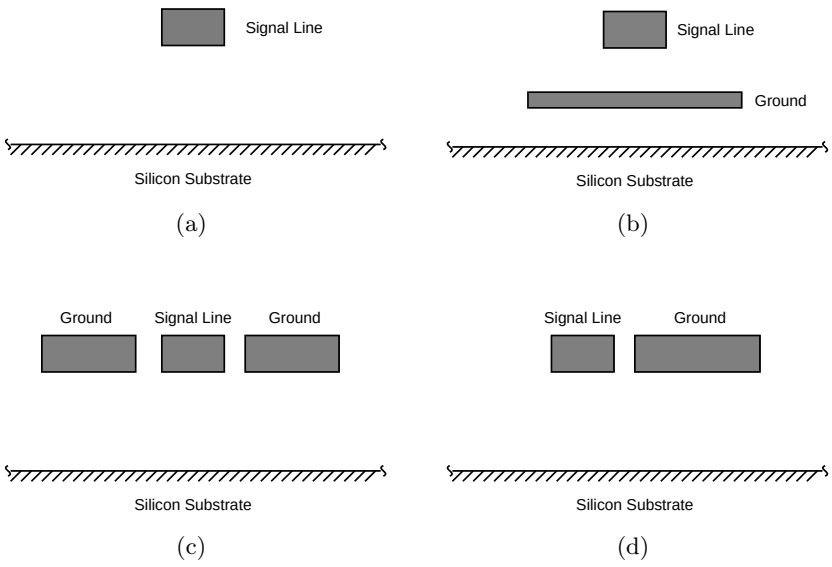


Figure 3.10: Transmission Lines on Silicon. (a) Microstrip on silicon substrate; (b) Microstrip on metal groundplane; (c) Coplanar waveguide; (d) Coplanar strip.

Type	Loss	Impedance
Microstrip with substrate ground-plane	High	Low
Microstrip with metal ground-plane	Very low	Very low
Coplanar waveguide	Low	Medium to High
Coplanar strip	Low	High

Table 3.1: On-Chip Transmission Line Comparison

3.4.1.1 On-chip transmission-line comparison

For DVCO's, it is desirable to find a particular type of on-chip transmission lines that have low loss and high impedance[5]. Low loss can reduce the power consumption and improve phase noise performance. It requires that the electromagnetic field is confined within the transmission line structures, and stay away from lossy silicon substrate. High impedance can increase the oscillation amplitude and thus improve the phase noise. It means that the capacitance per unit length (C) should be reduced while maintain the inductance per unit length (L)[6], which usually corresponds to larger spacing between conductors that form the transmission line structure. The latter is usually in conflict with low loss, since it results in spread EM field and probably larger substrate loss.

On-chip transmission lines commonly available in a silicon process (Fig. 3.10) are com-

[5]Cut-off frequency (f_c) is not a major concern since it is determined mainly by the periodically-loaded capacitance from transistors.

[6]Quasi-TEM transmission lines are assumed here, as in the usual case of MMIC.

Simulator	Dimension	Method	Computing Load	Targeting Problems
HFSS	3D	FEM	Large	Antenna, board
Sonnet	2.5D	Moment	Medium	IC, board
IE3D	2.5D	Moment	Low-Medium	IC, board
Momentum	2D	Moment	Medium	IC, board
Asitic	2D	Green's Functions	Low	On-chip inductors

Table 3.2: EM Simulators

pared in Table 3.1. Based on the comparison, coplanar strip was selected as the best compromise in the prototype design. Note that the decision depends on a particular process. For example, if the process has good-quality top metal layer which is far away from substrate, microstrip lines with substrate or lower metal layer as ground plane might be a good choice.

3.4.1.2 Electromagnetic simulation

Once the right type of on-chip transmission lines are determined, the next important question is how to properly model them [68]. In the initial design phase, some analytic approximations [69][39][70] can be used for estimation of oscillation frequency and amplitude, assuming there is only metal loss in the transmission lines. After that, electromagnetic (EM) simulations are needed to generate the data for circuit simulation.

There are several EM simulators available (Table 3.2) with emphasis on different problems, using different methods. 3D simulators such as HFSS [71] use *finite-element method* (FEM) and thus can simulate very complex 3D structures with very good accuracy. But the simulation time is quite long and requires large amount of memory. 2D or 2.5D[7] simulator such as Sonnet and IE3D use *moment* method and are very suitable for IC design because of the planar structure. Asitic [72] is a special program to simulate on-chip inductors using Green's Functions and tailored for silicon substrate. In our design practices, all these tools have been used in different design and measurement phases.

For the prototype DVCO's, full-wave 3D EM simulations with HFSS (Fig. 3.11) were used to simulate these coplanar strips (CPS). Then the simulation data (Z_0 and γ) was processed using Matlab codes to extract frequency-dependent circuit parameters ($L(f)$, $C(f)$, $R(f)$, and $G(f)$), which were then curve-fitted with W Element model of transmission lines in HSpice. The process is shown in Fig. 3.12, and some extracted circuit parameters for

[7] 2.5D usually means 2D with capability to take into account thickness of dielectric and/or metal.

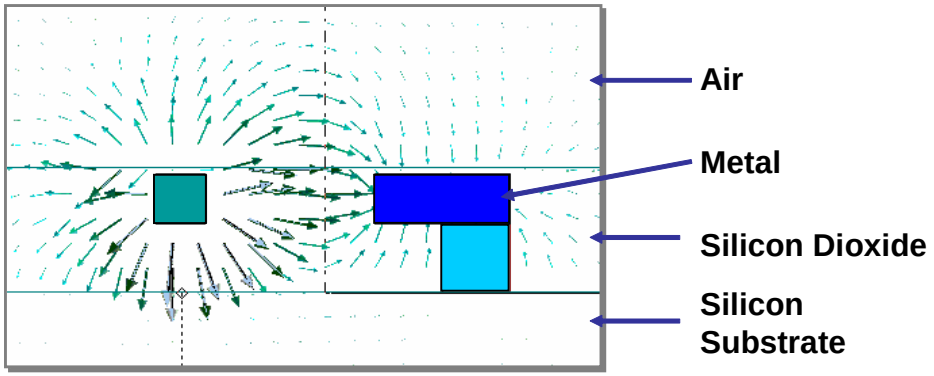


Figure 3.11: Electromagnetic Simulation of On-Chip Transmission Lines

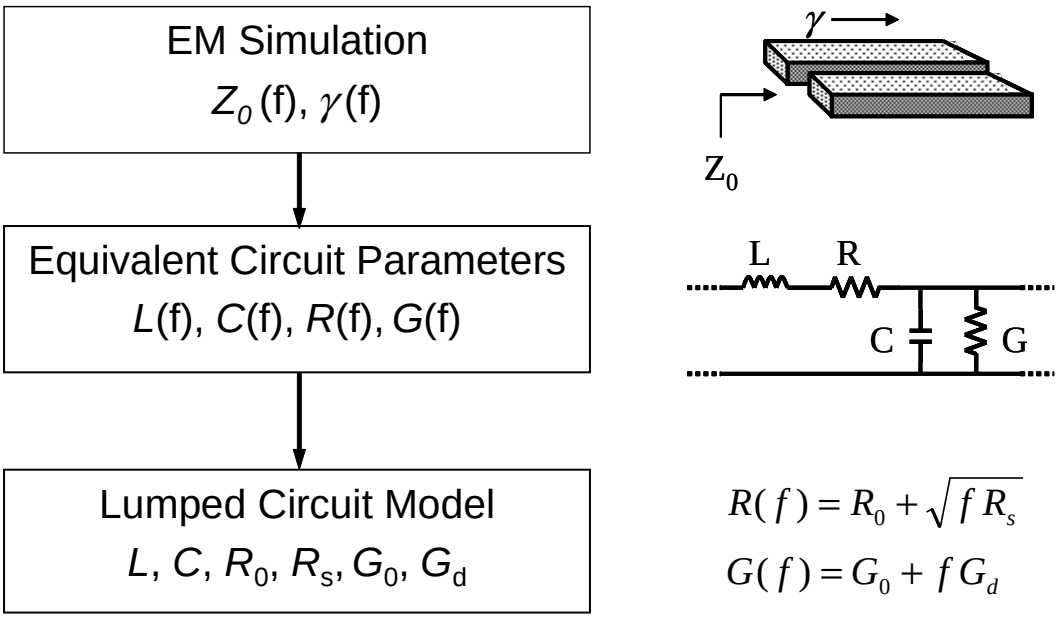
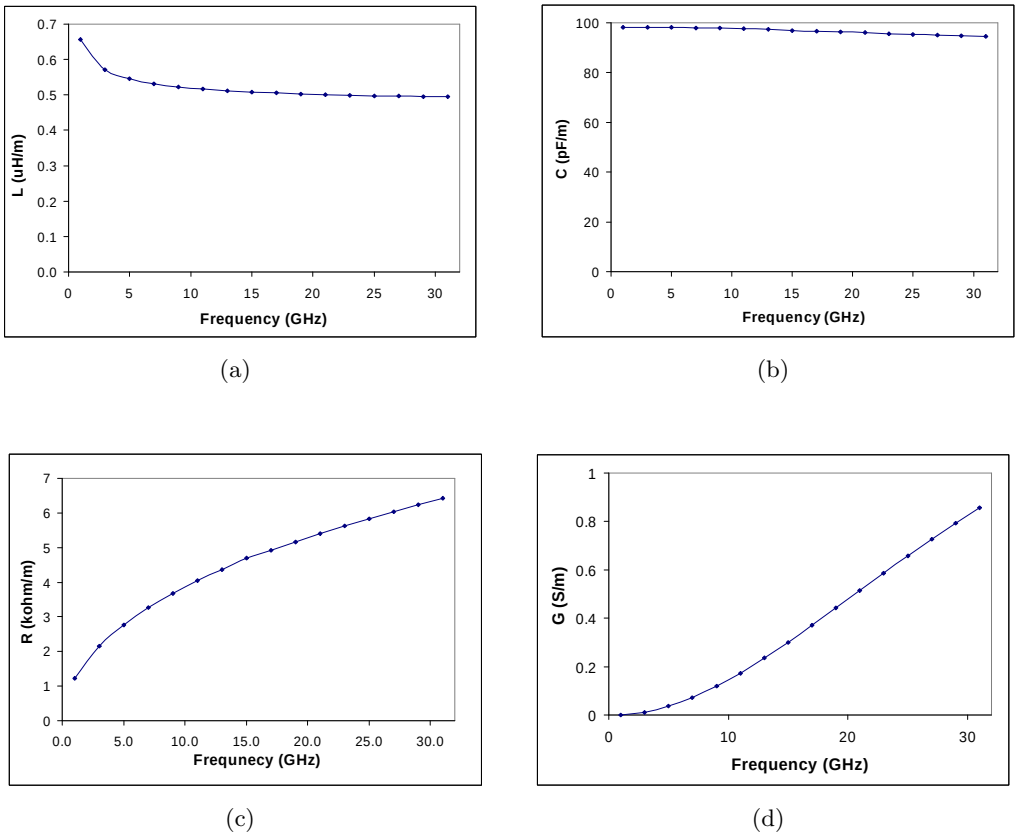


Figure 3.12: Electromagnetic Simulation of On-Chip Transmission Lines

a coplanar waveguide (CPW) in the same process (3μm-wide signal line, 8μm-wide ground, and 10μm spacing) using this procedure is shown in Fig. 3.13.[8] Note that the inductance and capacitance per unit length are almost constant while the resistance and conductance per unit length change almost linearly with frequency.

In the prototype design, coplanar strips are used for their high Z_0 and low loss. The coplanar strips have a metal thickness of 3 μm, a vertical spacing to the substrate of 4.2 μm, a signal-line width of 3 μm, a ground-line width of 8 μm and a lateral spacing between them

[8]The CPS lines were also designed in this procedure. But due to negligence, substrate contacts were not properly modeled, which presents a big problem for convergence of HFSS simulation. Thus the modified structure which reflects the real layout was only simulated around the oscillation frequency.



(a) (b)

(c) (d)

Figure 3.13: Circuit Parameters of CPW Line. (a) L; (b) C; (c) R; (d) G.

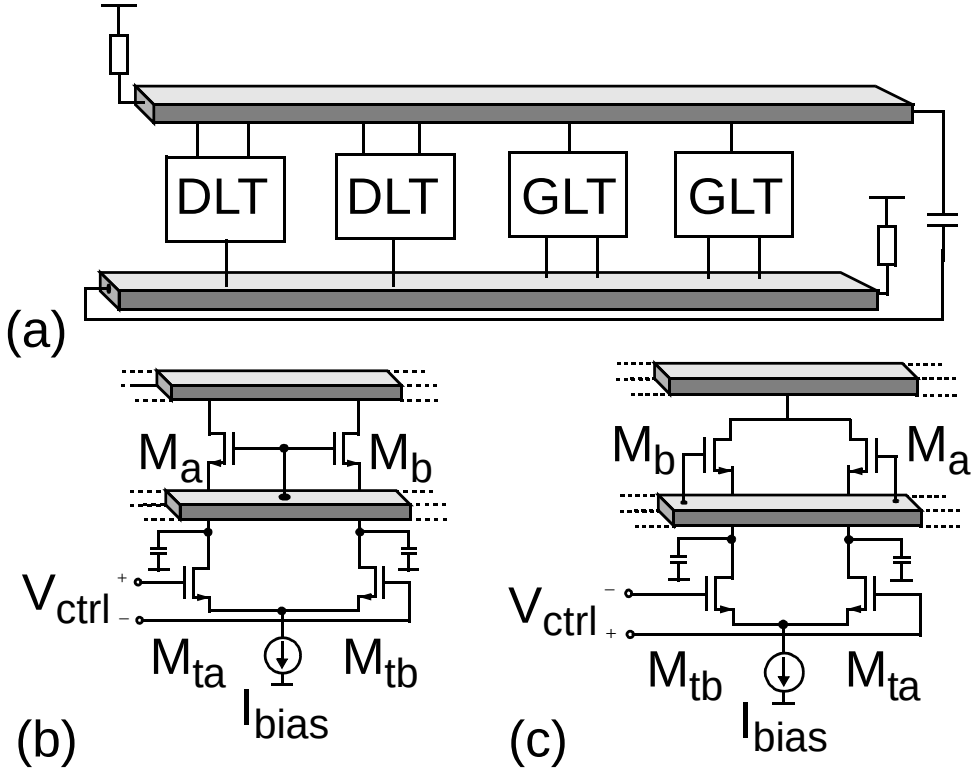


Figure 3.14: Delay-balanced current-steering tuning.

of 10 μm.They are $L = 0.72\ nH/\mu m$ and $C = 81\ aF/\mu m$ around frequencies of interest.

3.4.2 Circuit Design

The designed DVCO's comprise two GLT's (Fig. 3.14b) and two DLT's (Fig. 3.14c) as shown in Fig. 3.14a. In each section, I_a and I_b are implemented using a current source I_{bias} and two current steering transistors M_{ta} and M_{tb}. The differential control voltage steers the tail current between M_a and M_b. The channel lengths of transistors M_{ta} and M_{tb} should be chosen longer than the minimum channel lengths to allow for a larger and more uniform range of the differential control voltage, $V_{control}$. Longer channel length also reduces the excess channel noise of these devices which improves the phase noise of the oscillator [73][74]. The ac coupling capacitor between the end of the drain line and beginning of the gate line is used to allow the inherent varactor tuning. This dual differential and single-ended tuning capability allows a simultaneous coarse and fine tuning in a frequency synthesizer, which is useful for improving the capture range in a phase-locked loop.

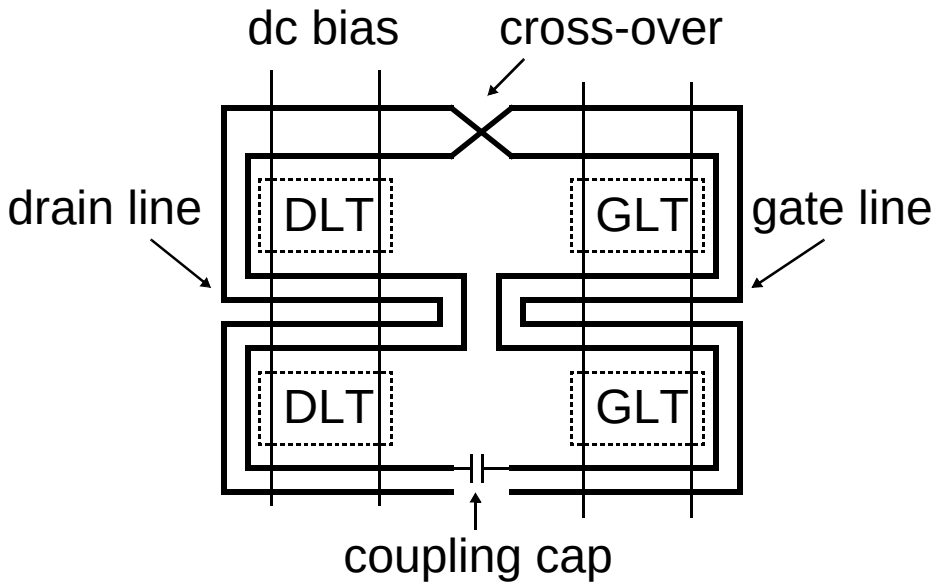


Figure 3.15: Floor plan of a DVCO.

3.4.3 Layout

Since the circuit operates at microwave frequencies and any conductive line can act as a transmission line, special attention should be paid to the layout. Fig. 3.15 shows the floor plan of a DVCO. A few important considerations are highlighted here. The gate and drain lines should be parallel to maintain synchronization of waves and their spacing should be large enough to lower interference. Due to the feedback path in the oscillator, a crossing where one transmission line goes underneath the other is inevitable. This crossing is implemented using both *metal1* and *metal2* lines to minimize the loss and compensate for the thickness difference between the top layer and the lower metal layers and thus impedance difference between the drain line and gate line. Enough vias are introduced at the crossing point to minimize the resistance. There are reverse-biased PN junctions (also known as laminations) underneath the entire transmission line structure to suppress Eddy currents in the substrate and thus lower the loss. In each section, the two gain transistors have identical distances from the tap points on the transmission lines in order not to introduce unbalanced excess delay as shown in Fig. 3.7 and Fig. 3.8. The dc bias lines pass underneath and are perpendicular to the transmission lines to minimize the capacitive loading on the lines.

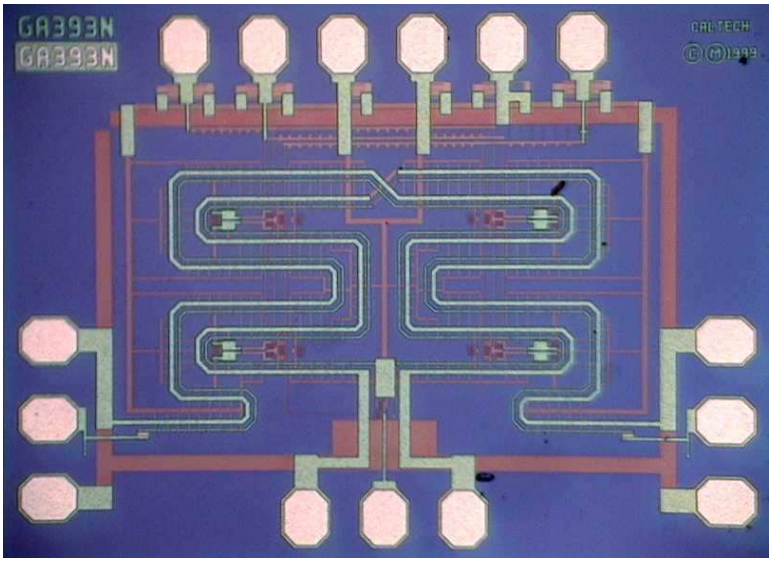


Figure 3.16: Die photo of the CMOS DVCO.

3.5 Measurement and Experimental Results

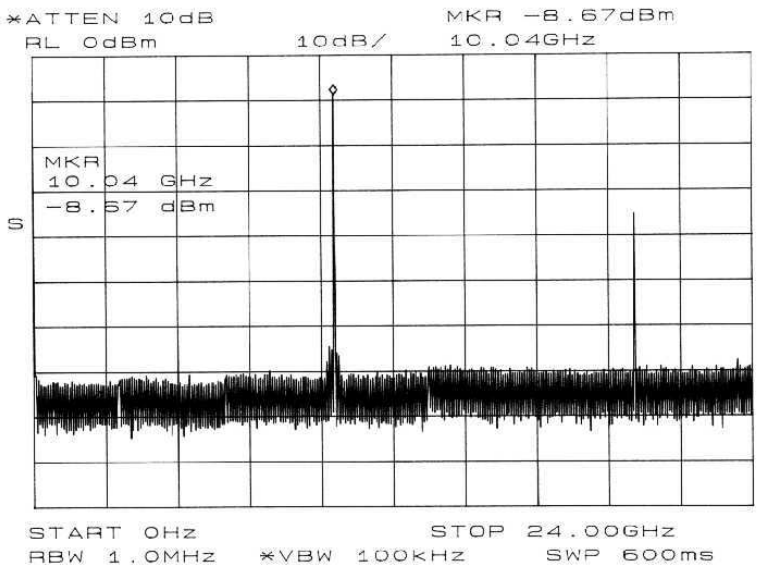
3.5.1 High-frequency on-wafer probing measurement

In our test setup, the chip is attached to a circuit board with conductive adhesive. The dc pads are wire-bonded to the PCB. A microwave probe station equipped with microwave coplanar probes is used to probe the RF pads on the sides. The probes are connected to the measurement instruments and bias circuitry through coaxial cables. An HP 8563E spectrum analyzer is used to measure the oscillation frequency and the output power. The measured insertion loss from the probes to the spectrum analyzer is 4.3 dB at 10 GHz and 6.3 dB at 12 GHz, respectively. Therefore, any measured power on the spectrum analyzer should be adjusted for the extra loss.

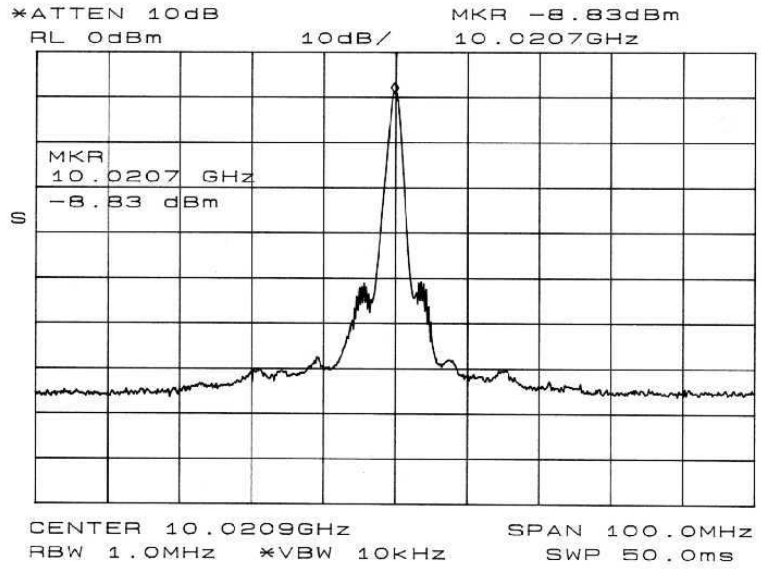
3.5.2 CMOS DVCO

A 10 GHz CMOS DVCO is fabricated in a 0.35 μm BiCMOS technology using only CMOS transistors. Fig. 3.16 shows its chip micrograph. It occupies an area of $1.4\mu m \times 1\ \mu m$, including the pads. The total length of transmission lines is about 7 μm. It is noteworthy that CMOS transistors in a BiCMOS process are known to have inferior f_T compared to transistors of comparable size in pure CMOS technologies.

The measured power spectrum is shown in Fig. 3.17, which should be adjusted for the



(a)



(b)

Figure 3.17: Spectrum of 10 GHz CMOS DVCO. (a) Harmonics. (b) Detailed.

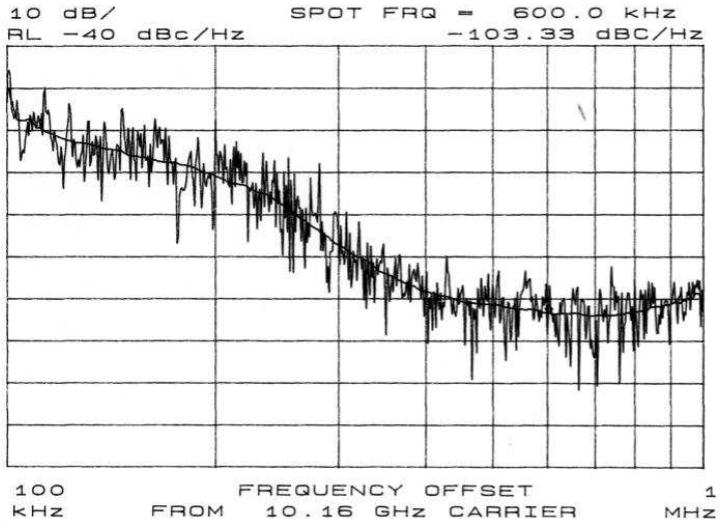


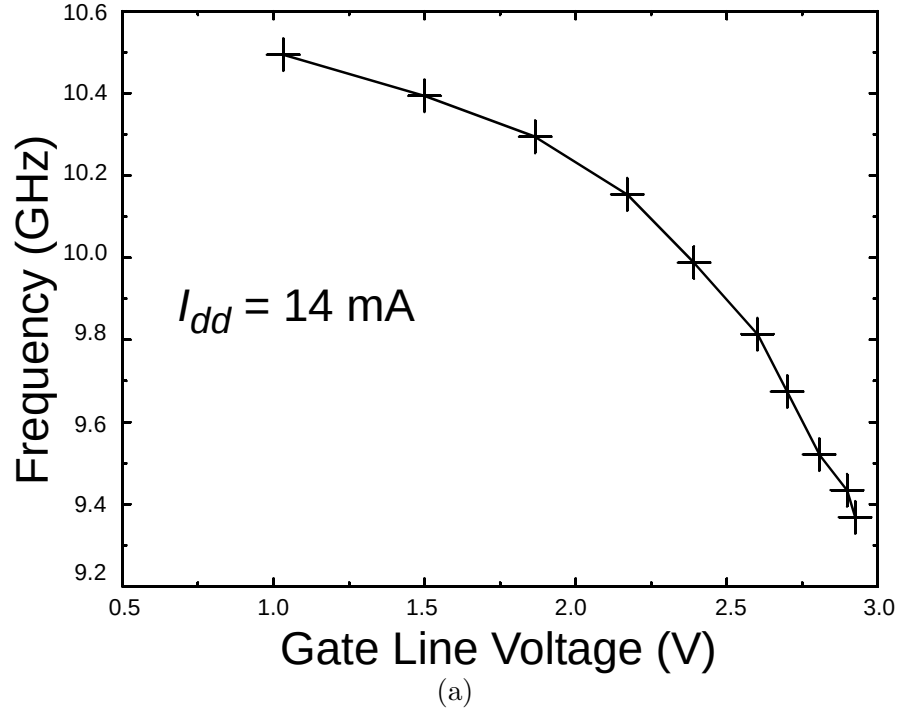
Figure 3.18: Phase Noise of 10 GHz CMOS DVCO.

4.3 dB loss in the setup. The center frequency of the oscillator is 10.0 GHz and the output power is -4.5 dBm. Fig. 3.18 shows the single-side-band (SSB) phase noise. The phase noise is -103 dBc/Hz at 600 kHz offset from a 10.2 GHz carrier with a total drain current of 14 mA. Deterministic modulation sidebands induced by external interference can be observed in Fig. 3.17b. These sidebands degrade the measured phase noise at higher offset frequency from the carrier.

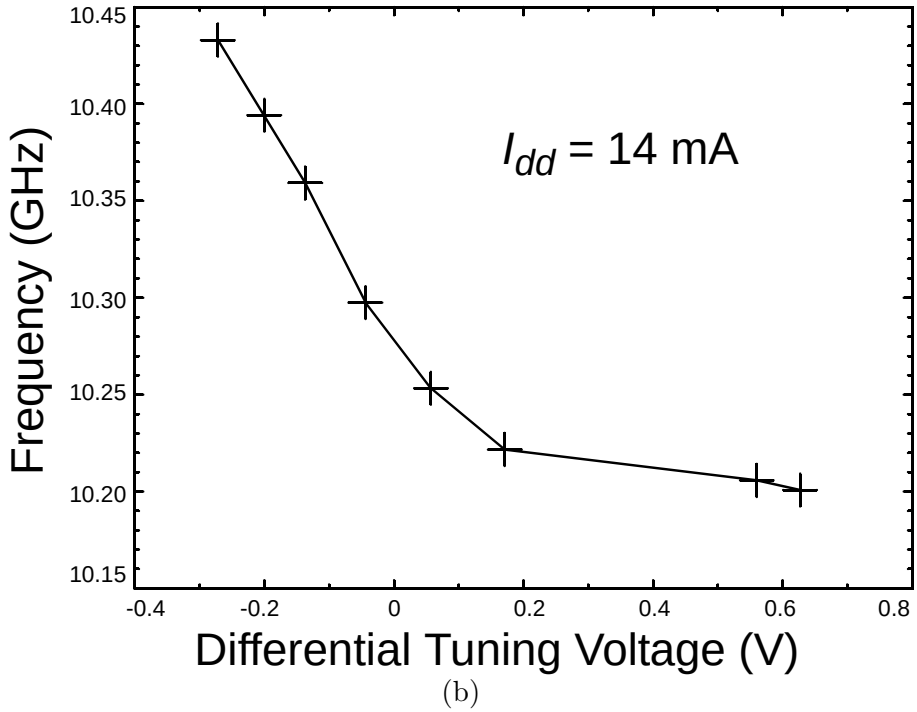
A tuning range of 9%(9.5 − 10.4 GHz) can be obtained using the inherent-varactor tuning with a total drain current of 14mA. The output power variation is 2.7dB over this tuning range. If maintaining a constant output power is not required, the tuning range can be extended to 12%, as shown in Fig. 3.19a. The measured tuning range of the delay-balanced current-steering tuning technique is 2.5% around the center frequency set by the inherent-varactor tuning, as shown in Fig. 3.19b for a center frequency of 10.3 GHz.

Using transmission line parameters obtained from EM simulations with HFSS (L = 0.72 $nH/\mu m$ and $C = 81$ $aF/\mu m$) and the circuit parameters ($l_g = l_d = 0.9\mu$m, $l_t = 0.3\mu$m, $n = 4$, C_{in} = 188fF/stage, C_{out} = 152fF/stage), (3.7) predicts a center frequency of f_0 = 9.97GHz.

The measured output power from the gate and drain terminations vs. total drain current are compared in Fig. 3.20. These measurements are good indicators of the oscillators internal voltage levels.



(a)



(b)

Figure 3.19: Tuning Characteristics of 10 GHz CMOS DVCO. (a) Inherent-varactor tuning. (b) Current-steering delay-balanced tuning.

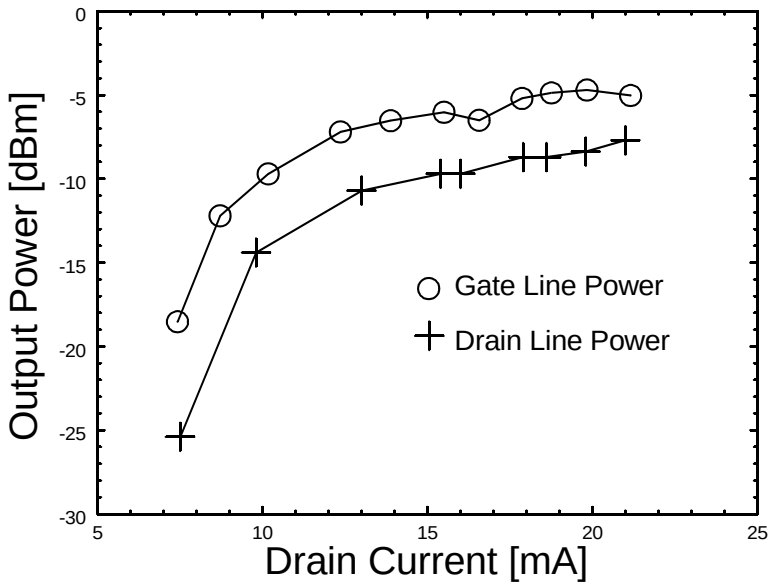


Figure 3.20: Power consumption vs. output power of 10 GHz CMOS DVCO.

3.5.3 Bipolar DVCO's

The 12 GHz bipolar DVCO is fabricated in the same BiCMOS process. Fig. 3.21 shows its chip micrograph. It occupies an area of $1.2\mu\text{m} \times 1\mu\text{m}$. The total length of transmission lines is about 5 μm, which primarily controls the center frequency. The measured power spectrum and phase noise spectrum of the 12 GHz DVCO are shown in Fig. 3.23 and Fig. 3.24. A phase noise of -99 dBc/Hz at 600 kHz offset from a 11.7 GHz carrier is achieved on 6 mA bias current from a 2.5 V dc supply. This power dissipation is comparable to low power lumped VCO's operating at lower frequencies. A better phase noise can be achieved by increasing the bias current.

The inherent varactor tuning on the collector line achieves a tuning range of 12% (10.6 - 12GHz) with 2 dB output power variation. This tuning range can be extended to 26% by tolerating larger output variation, as shown in Fig. 3.25a. The delay-balanced current-steering tuning achieves a tuning range of 7.4% around the center frequency set by the inherent-varactor tuning, as shown in Fig. 3.25b for a center frequency of 12.1 GHz.

Using transmission line parameters obtained from EM simulations with HFSS (L = 0.72mH/m, $C = 81$pF/m) and the circuit parameters ($l_g = l_d = 0.6\mu$m, $l_t = 0.2\mu$m, $n = 4$, $C_{in} = 386$fF/stage, $C_{out} = 116$fF/stage), (3.6) predicts a center frequency of $f_0 = 11.3$GHz.

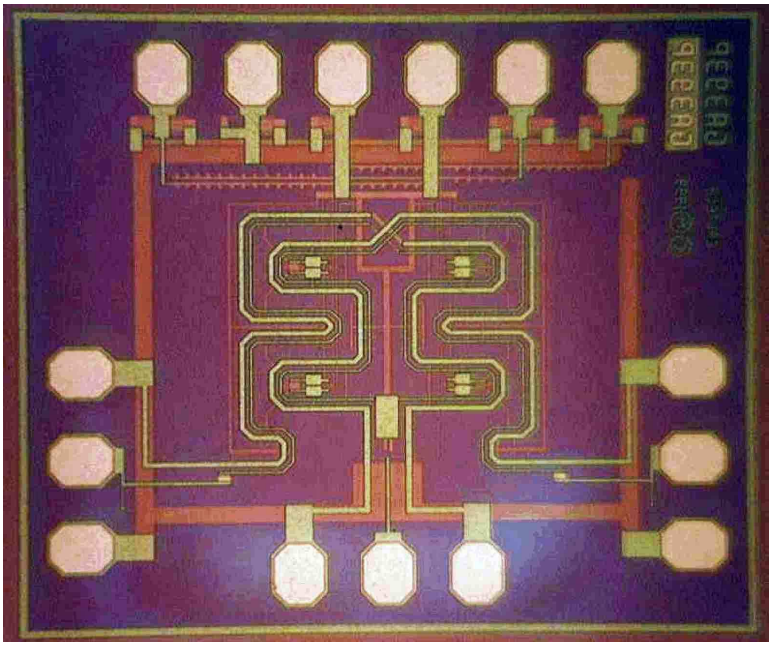


Figure 3.21: Die photo of the 12 GHz bipolar DVCO.

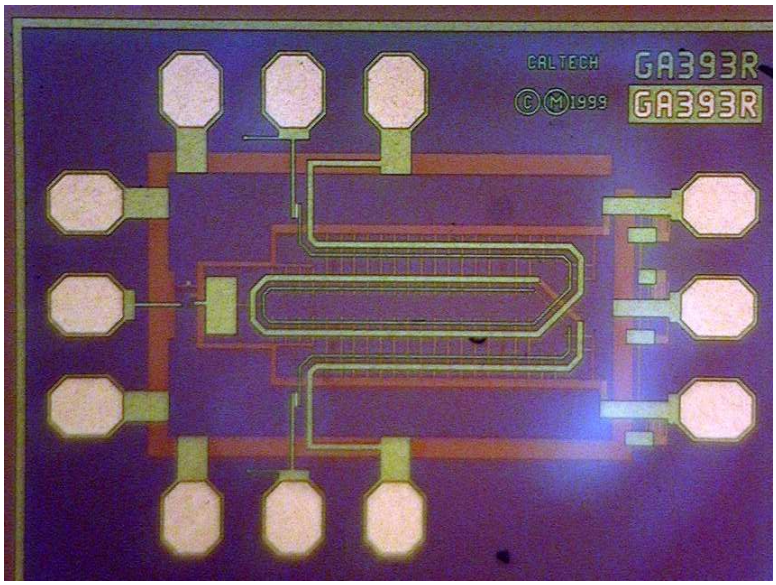
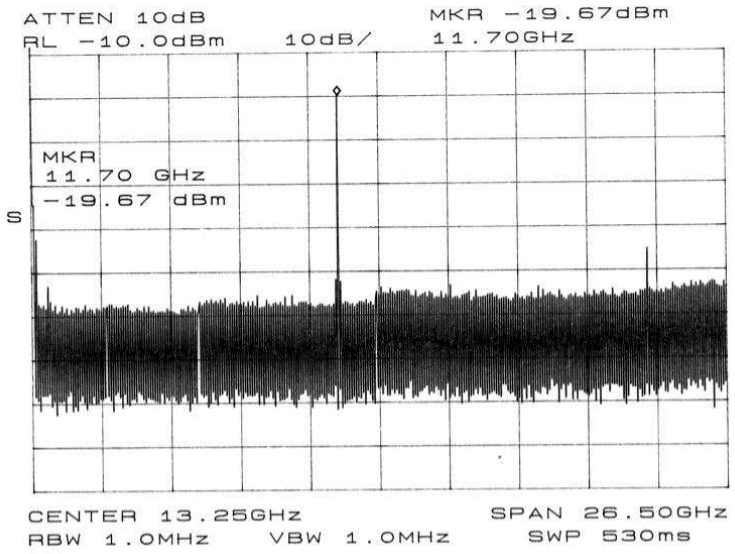
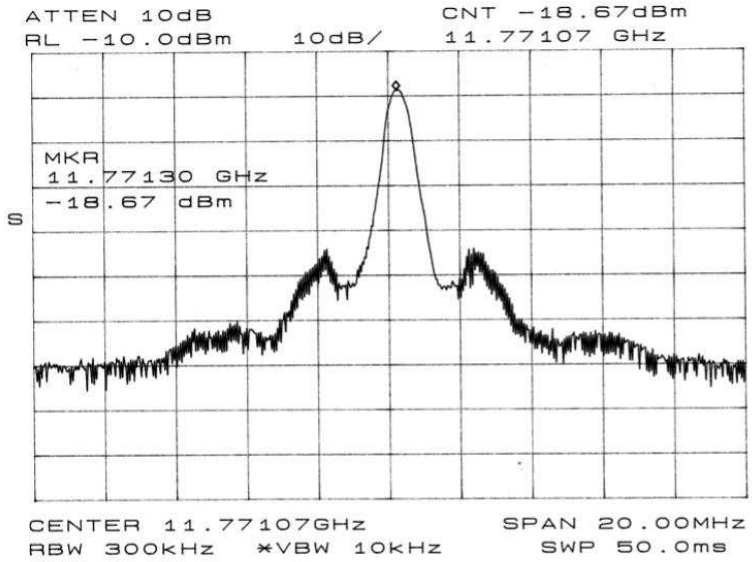


Figure 3.22: Die photo of the 17 GHz bipolar DVCO.



(a)



(b)

Figure 3.23: Spectrum of 12 GHz Bipolar DVCO. (a) Harmonics. (b) Detailed.

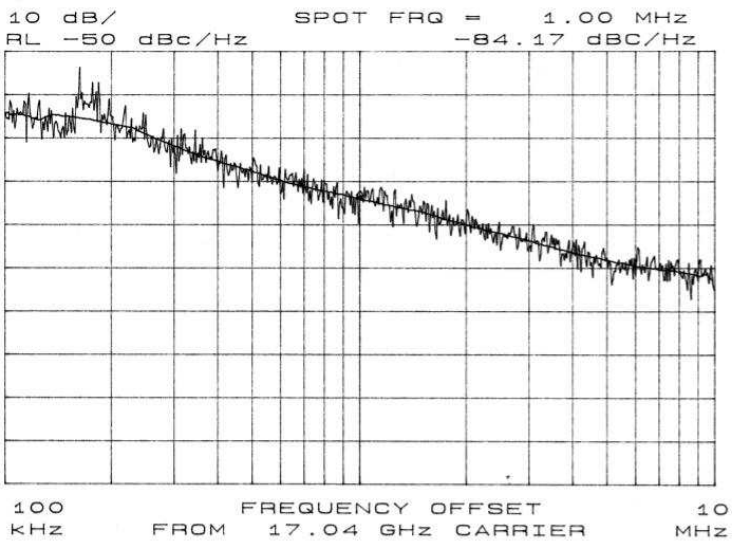


Figure 3.24: Phase Noise of 12 GHz Bipolar DVCO.

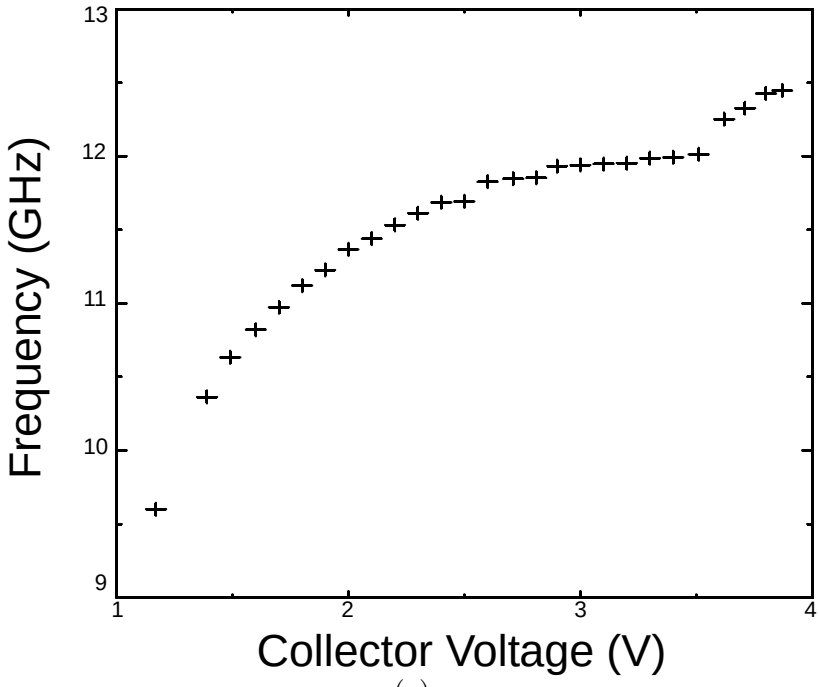
3.6 Alternative Architectures of Distributed Oscillators

3.6.1 Problems in "Conventional" Architecture

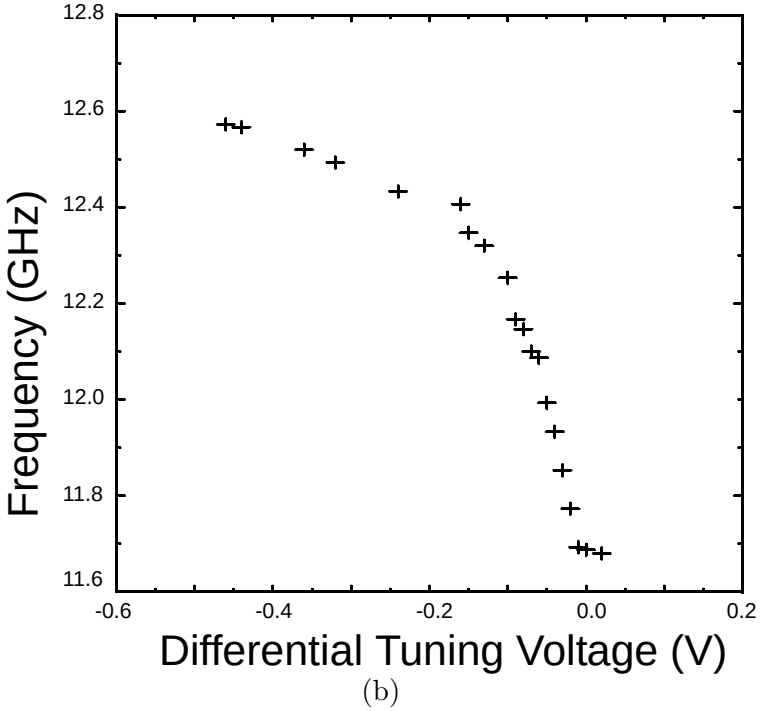
Despite the earlier advances, the full potential of distributed oscillators has yet to be fully exploited, and there are still some problems to be solved.

3.6.1.1 Dummy loads

Recall from Section 3.2, the forward wave on the gate line is absorbed at the dummy output by a matched load, and so does the backward wave on the drain line. Obviously RF energy is wasted on these dummy loads, which lowers the power efficiency and degrades the phase noise performance because loss is always linked with noise. Dummy loads also result in implementations difficulty – since on-chip passive components (resistors, capacitors, and inductors) have limited range and poor tolerance in absolute values, the required circuitry for loads matched to some particularly impedance value (e.g., 50 ohm) can be either impossible to implement on-chip, or highly likely to be mismatched. The latter leads to excessive reflections from dummy loads back into the oscillator, and thus degrades its performance.



(a)



(b)

Figure 3.25: Tuning Characteristics of 12 GHz Bipolar DVCO. (a) Inherent-varactor tuning. (b) Current-steering delay-balanced tuning.

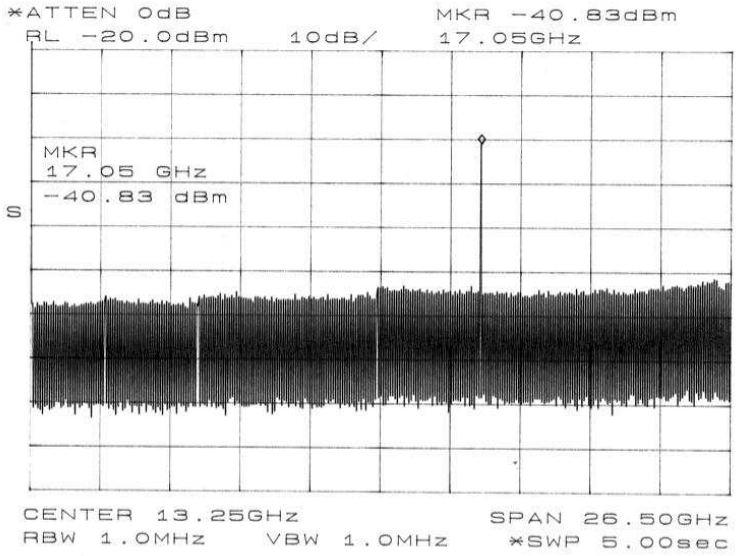


Figure 3.26: Spectrum of 17 GHz Bipolar DVCO.

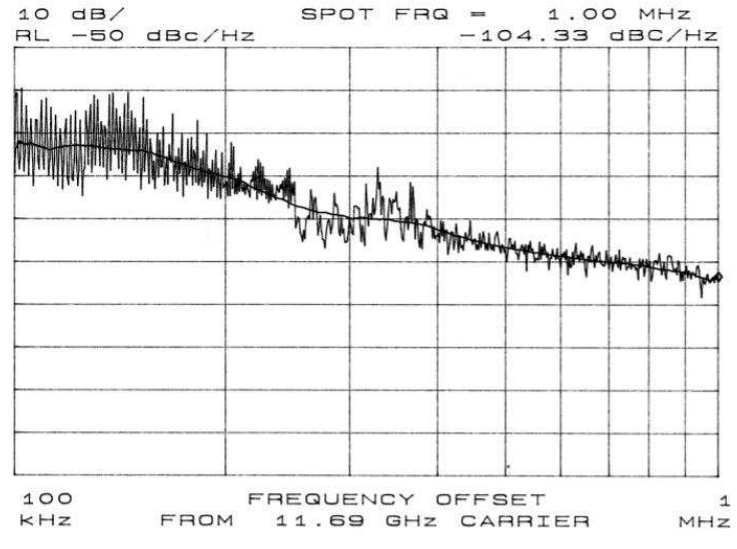


Figure 3.27: Phase Noise of 17 GHz Bipolar DVCO.

3.6.1.2 Inherent imbalance

As discussed in Section 2.1, a major challenge in the design of a conventional distributed amplifier or distributed oscillator is to synchronize the signals on the gate and drain lines. In the ideal case, the phase velocity is equal on both loaded transmission lines, which is highly unlikely to be satisfied in real implementations, since the input admittance of transistors is usually quite different from the output admittance. For example, the input capacitance of a NMOS transistor in a common-source configuration, C_{gs}, is usually much larger than the output capacitance, $C_{gd} + C_{db}$. In conventional designs, therefore, either gate and drain lines are made with different physical length, which results in different electrical length for the loaded lines, or balancing capacitors are added to one line (usually the drain line) or both to obtain equal phase velocity.

These solutions, however, are not effective for integrated implementations because (1) the poor tolerance of on-chip capacitors make the *compensation loading* quite inaccurate; (2) there is always layout constraints such as chip size and topology. The latter is particularly troublesome for DVCO's because it is more difficult to implement the feedback loop with unequal physical length of transmission lines; (3) The input and output admittances of transistors are nonlinear with regard to voltage, which is important since most oscillators operate in the large signal mode. Since it is very difficult to accurately predict the oscillation amplitude, especially at RF frequencies due to inadequate and inaccurate modeling, it is extremely difficult to achieve perfect balance between the two loaded lines only by design – some kind of trimming is usually needed; (4) Even if the two loaded transmission lines are meticulously designed and trimmed to be balanced, process and temperature variations make the design far from robust, repeatable or reliable.

Consequently, the inherent imbalance impairs the signal synchronization on the two transmission lines. This has several effects: (1) the phase shift around the total loop is no longer 360 degrees at the designed oscillation frequency, and thus there must be a shift in oscillation frequency to maintain the 360-degree phase shift; (2) even worse, this frequency shift is neither well controlled nor easily predictable, and can drift with time or temperature, which directly translates into phase noise; (3) RF power of signals in all feedback loops do not add in phase, and thus part of RF power is wasted, which lowers the oscillation amplitude and deteriorates the phase noise performance.

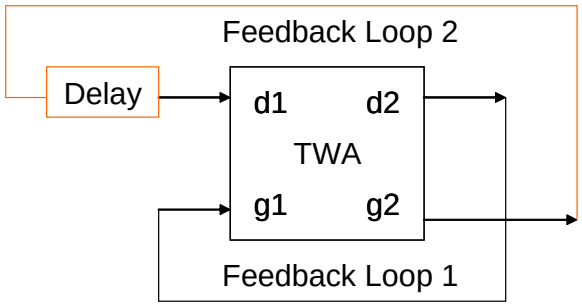


Figure 3.28: Double Feedback Distributed Oscillator.

3.6.1.3 AC grounding

There is a technical challenge need to be addressed in the physical design of distributed oscillators, namely, the ground path for ac signals. This is a general problem in RF circuit design, but it is particularly difficult in the case of a distributed oscillator because of the relatively long distance between ground nodes of transistors. Accurate modeling of the ground path can partially mitigate the problem, but a systematic solution is more desirable.

3.6.2 Double Feedback Distributed Oscillator

Fig. 3.28 shows a *double-feedback distributed oscillator*, in which the traveling-wave amplifier is represented as a TWA block. In addition to the feedback path from output $d2$ to input $g1$ as in the conventional distributed oscillator architecture, a second feedback path from $g2$ to $d1$ is added with an extra delay element. Now, the forward wave on the gate line is not absorbed by a dummy load; instead, it goes on along the second feedback path and combines with on the drain line, and thus contributes to the total synchronized signal at output $d2$.

The delay element is added to account for the extra delay introduced by transistors, otherwise the feedback signal from $g2$ to $d1$ would be ahead of signals amplified by each transistors in phase. In this manner, the synchronization of signals on the drain line is conserved. Further, this delay makes the circuit *asymmetric* for signals traveling in two directions: the signals on both lines are synchronized in the forward direction (i.e., towards the right in Fig. 3.28), but not so in the backward direction (i.e., towards the left in Fig. 3.28). Therefore, the oscillation only happens in the forward direction at the steady state of the oscillator, and there exist pre-determined phase relations along both transmission lines. The

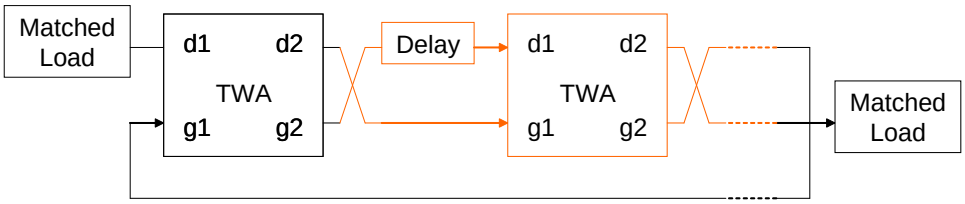


Figure 3.29: Balanced Distributed Oscillator.

delay can be implemented using an additional section of transmission lines.

A double-feedback distributed oscillator avoids the need for dummy matched terminations at all, and thus operates with higher power efficiency and improved phase noise performance. It is also helpful in cases where on-chip matched loads are unavailable or their values have poor tolerance.

3.6.3 Balanced Distributed Oscillator

Fig. 3.29 is a diagram of a *balanced distributed oscillator*. It consists of multiple TWA sections[9], while even number of sections is preferred. Between adjacent TWA sections, gate line and drain line cross each other and exchange their roles. Thus there is no longer distinctive *gate* or *drain* lines as in the conventional distributed oscillator architecture. For even number of TWA stages, the two lines have almost identical device loading and thus similar phase velocity in the first order. In this manner, signal synchronization on these two lines can be well maintained, even if there is inherent imbalance within each TWA section. Therefore, oscillation frequency accuracy and stability can be greatly improved, which corresponds to better phase noise performance and less stringent design requirements. Since it is a systematic approach, it is also immune to process or temperature variations. It is noteworthy that this technique can also be useful in other distributed applications.

3.6.4 Double Balanced Distributed Oscillator

We can further combine the previous two techniques, and achieve a balanced double-feedback distributed oscillator (Fig. 3.30, or simply *double-balanced distributed oscillator*. In addition to all the benefits of both double-feedback and balanced distributed oscillators, a double-balanced distributed oscillator also have perfect symmetry between the two

[9]When there is only one section, it degenerates into a conventional distributed oscillator.

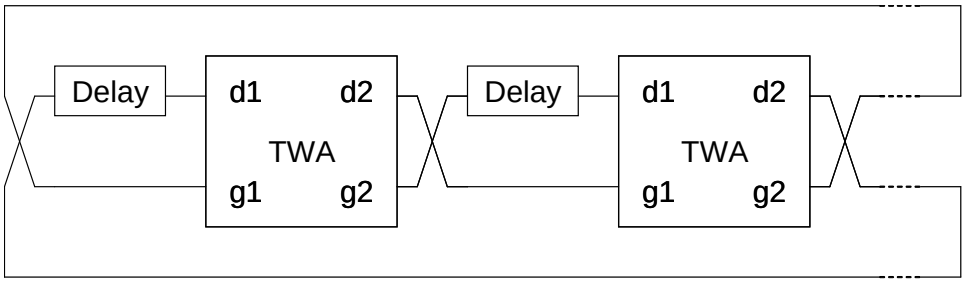


Figure 3.30: Double Balanced Distributed Oscillator.

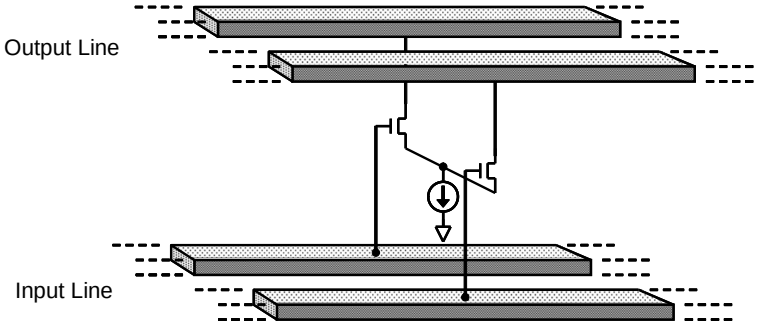


Figure 3.31: Differential Distributed Oscillator.

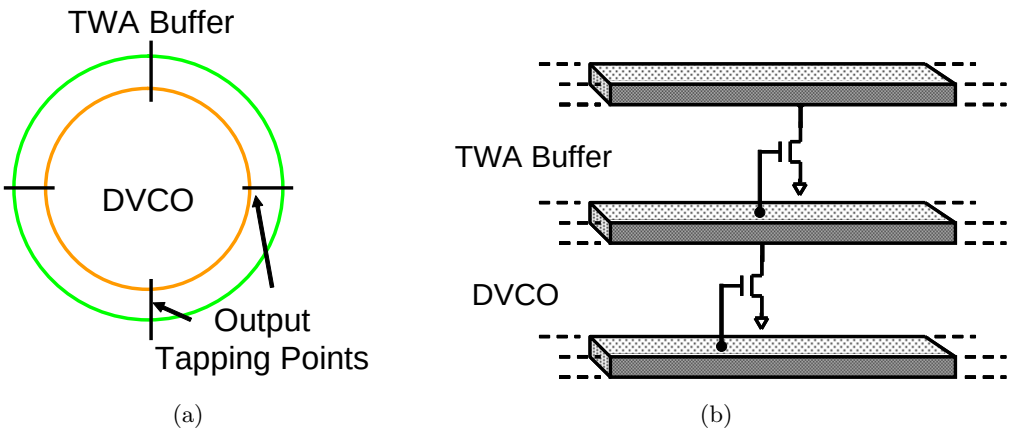
transmission lines, which makes the design more robust to inaccurate modeling and layout easier.

3.6.5 Differential Distributed Oscillator

Fig. 3.31 is one section of a *differential distributed oscillator*, which uses differential amplifiers and differential transmission lines. It is always desirable to have differential topology in RF circuits because it improves the circuit performance and reduces the effect of common-mode noise, such as power supply noise, substrate coupling or electromagnetic interference (EMI). In addition, a differential distributed oscillator largely alleviates the return path problem for ac currents, because the differential currents cancel each other in the first order within each stage. Therefore, the quality of RF grounding becomes less critical and thus modeling and layout becomes easier.

3.6.6 TWA-Buffered Distributed Oscillator

Buffering is required at the oscillator output to isolate its core from load pulling, which degrades the phase noise performance. If a lumped buffer is used, the loading on a DVCO



(a) (b)

Figure 3.32: TWA-Buffered Distributed Oscillator. (a) topology; (b) circuit detail.

core becomes asymmetrical and unbalanced. So it is desirable to conserve the distributed nature of the circuitry. A TWA is a natural choice.

Fig. 3.32 shows the topology and schematic of a *TWA-buffered distributed oscillator*. It has a distributed oscillator in the center, and a TWA at outside. Output tapping points are evenly distributed on the output transmission lines of the distributed oscillator, which also become the input transmission lines of the TWA buffer, as shown in the right schematic.

It is noteworthy that this new architecture is different from using a TWA as a buffer, in which there is a single point-to-point connection between the output of distributed oscillator and the input of the TWA. A TWA-buffered distributed oscillator, however, have multiple taps as the interface between the core of the distributed oscillator and the buffered outputs. Therefore, the distributed circuit topology is well preserved.

Further, TWA-buffered distributed oscillators can provide multiple-phase outputs by using a number of short TWA buffering sections with pre-defined interval.

3.6.7 Injection-Locked Distributed Oscillator

Fig. 3.33 shows an *injection-locked distributed oscillator*. It consists of a conventional distributed oscillator DVCO1 and a differential distributed oscillator DVCO2. DVCO2 operates at frequency f_0 and DVCO1 at $2f_0$. DVCO1 and DVCO2 are injection locked to each through the tail current of each differential amplifier (M_1 and M_2) in DVCO2. Capacitor C_1 and C_2 provide the return path for the injection locking signal, and also serve as loading compensation capacitors for DVCO2. DVCO1 and DVCO2 can be independently

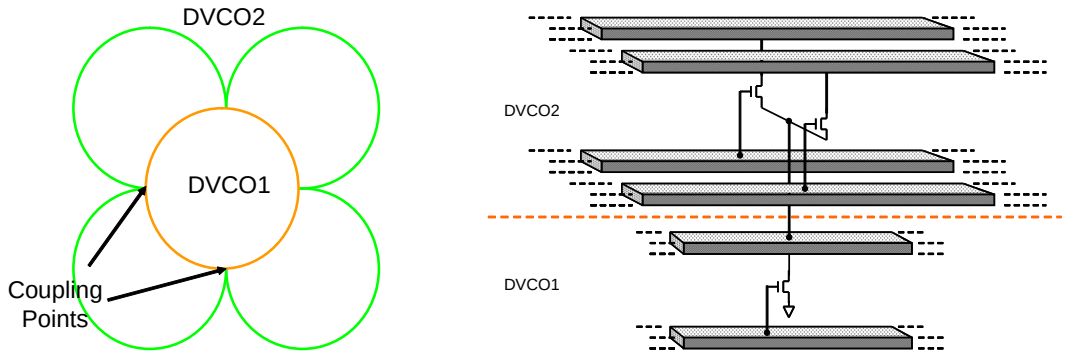


Figure 3.33: Injection-Locked Distributed Oscillator. (a) topology; (b) circuit detail.

tuned (tuning circuitry not shown in Fig. 3.33). Fig. 3.33b shows the physical topology for such an injection-locked distributed oscillator. DVCO1 is in the center and has shorter transmission lines since it oscillates at higher frequency.

Such an injection-locked distributed oscillator can be used for frequency synthesis, serving as both quadrature VCO and high-speed prescalar. In addition, injection locking further improves the phase noise performance of *each* DVCO in this subsystem within the locking range. Therefore, it potentially can be used as an extremely low-phase-noise oscillator.

3.6.8 Multi-Mode Distributed Oscillators ?

The "conventional DVCO only generates a single frequency. Because of the wideband nature of distributed circuits, it is also possible to generate several frequencies that are harmonically related, i.e., the DVCO has multiple modes. If these modes are built up in a synchronized fashion, it becomes very narrow pulses in time domain. It can visualized as an electronic pulse laser. Such a multi-mode DVCO has great potential in various applications, such as "soliton-like" narrow pulse generators, fiber-optic laser modulator, and ultra-wide-band (UWB) communications.

3.7 Summary

In this chapter, distributed voltage-controlled oscillators have been introduced and analyzed. General oscillation conditions for the amplitude and frequency have been derived. Two novel tuning techniques (inherent varactor tuning and current-steering delay-balanced tuning)

have been developed and analyzed. The design and layout issues of DVCO's were also discussed. Experimental results of several prototypes, including a 10 GHz CMOS DVCO and a 12 GHz bipolar DVCO, were presented. Finally, several novel DVCO architectures were discussed.

Chapter 4

Integrated Transversal Equalizer

This chapter discusses applying the distributed circuit technique in equalization for high-speed fiber-optical communications. Section 4.1 introduces the ISI problem and its main cause in fiber-optic systems, dispersion. Dispersion compensation techniques in optical and electrical domains are discussed in Section 4.2, and integrated transversal equalizers are presented as a promising solution to the challenges in high-speed equalization in Section 4.3. Section 4.4 describes the design of the prototype 10Gb/s transversal equalizers, including detailed analysis on the delay elements (transmission lines) and gain stages. Measurement results of the prototypes are presented in Section 4.5. Section 4.6 discusses the possible improvements in the future.

4.1 Inter-symbol interference and dispersion

Inter-symbol interference (ISI) (Fig. 4.1) is a fundamental problem in digital communications [75]. Together with noise, it sets the limits for the data-rate and transmission distance without repeaters in a communication system, given a certain bit-error rate (BER).

The current long-haul fiber-optic link (2.5 Gb/s and 10 Gb/s) [13] consists of series of regenerator spans (Fig. 4.2). In each regenerator span, there is a distributed-feedback laser

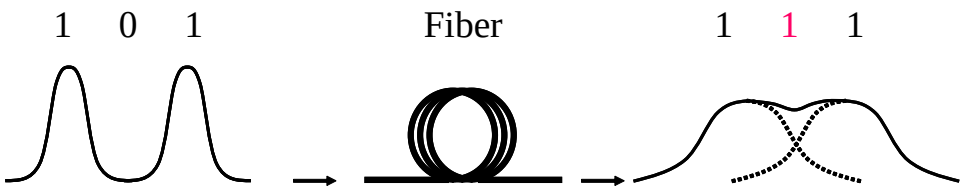


Figure 4.1: ISI in fiber-optic systems.

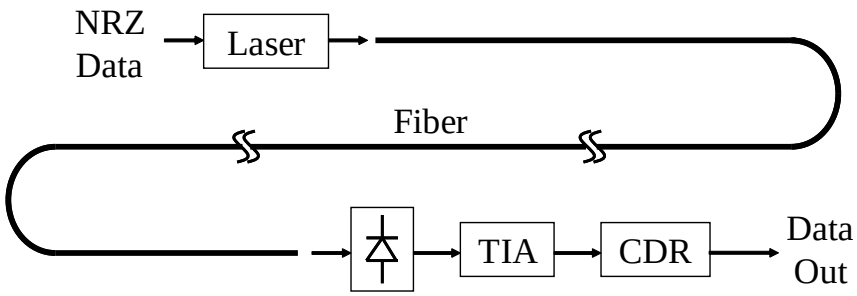


Figure 4.2: Long-haul fiber-optic communication system.

operating at 1.3μm or 1.56μm wavelength on the transmitter side. The laser is on/off-modulated by the input or regenerated non-return-to-zero (NRZ) data stream. On the receiver side, the optical signal is detected by a PIN or avalanche photodiode (direct-detection), and the electrical signal is then amplified by a transimpedance amplifier (TIA), followed by a clock-and-data-recovery (CDR) circuit, by which the recovered signal is re-timed and re-shaped before being transmitted to the next span. Between the transmitter and receiver, there is a single-mode fiber (SMF) of 40-100 km. Due to the invention of erbium-doped fiber amplifiers [76], which are optical amplifiers and thus can be inserted into the fiber link without optical-electrical conversion, fiber attenuation is not longer the dominant limiting factor for regenerator span distance. Instead, ISI becomes the bottleneck in high-speed, long-haul fiber-optic systems because of the fast advances in data rate and broad deployment of wavelength division multiplex (WDM).

A short-haul fiber-optic link has the same basic architecture as in a long-haul system (Fig. 4.2) with a shorter fiber length. Gigabit ethernet [77] and storage area networks (SAN)(e.g., Fibre Channel [78]) are two important examples. In these systems, multi-mode fibers (MMF) are more cost effective than SMF, but more problematic in ISI.

ISI in a fiber-optic system has many sources, such as laser and fiber nonlinearity, non-ideal receiver frequency response, echoes, optical amplifier distortion, and most importantly, fiber dispersion [79][80][81]. There are three types of dispersion in a fiber-optic system: modal dispersion, chromatic dispersion, and polarization mode dispersion. For a given data rate, dispersion-induced ISI sets the limit on the link distance without repeaters, which is referred to as *dispersion limit* [82].

Modal dispersion occurs in multi-mode fibers, in which different modal components of a signal pulse travel at different velocities. It is more serious in older step-index MMF

Fiber @ 850nm Wavelength	Modal Dispersion Limit (MHz·km)	Link Distance at 10Gb/s (m)
62.5 μm MMF	160	26
50 μm MMF	500	82
50 μm NGMMF	2000	300

Table 4.1: Dispersion limit of common multi-mode fibers.

than later graded-index MMF's. For example, Table 4.1 shows the dispersion limit and achievable link distance of common MMFs in short-haul systems at 10 Gb/s. It is evident that neither the common FDDI-grade 62.5 μm MMF nor newer 50 μm MMF is effective at such high speed. Even though the latest, special-tailored 50 μm next-generation MMF (NGMMF) can achieve the same distance as in the previous generation networks (300m), it would be more attractive to utilize the huge installed base of old fibers.

Chromatic dispersion (CD) [83][84] is due to the variation of group velocity with optical frequency in fibers, and can be further categorized as material dispersion and waveguide dispersion. Material dispersion is caused by variation in refractive index of the glass in the fiber as a function of the optical frequency. Waveguide dispersion is due to changes in distribution of light between the core and the cladding of single-mode fibers. CD is usually measured by the the amount of broadening that would occur in a pulse with a bandwidth of 1nm while propagating through 1km of fiber, and is given by (for a conventional step-index single-mode fiber):

$$D = \frac{d}{d\lambda}\frac{1}{v_g} = \frac{d^2\beta}{d\lambda d\omega} \tag{4.1}$$

where λ, v_g, β and ω are the wavelength, group velocity, propagation constant and angular frequency, respectively. D is about 17ps/km/nm in the 1.56μm wavelength window in a standard fiber.

The dispersion limit due to chromatic dispersion is given by (for a multi-mode laser)

$$L_D = \frac{\epsilon}{R_b D \Delta\lambda} \tag{4.2}$$

where R_b is the signal bit-rate, $\Delta\lambda$ is the laser linewidth (optical bandwidth), and ϵ is a constant that depends on the power penalty[1]. For example, in an OC-48 system, R_b = 2.5Gb/s, D = 17ps/nm/km, $\Delta\lambda$ = 0.5nm, assuming $\epsilon = 1$ (a pulse has broadened by one bit), the estimated dispersion limit due to CD is 47 km. If an external modulator is used,

[1]Power penalty refers to the additional loss budget required to account for degradations due to reflections, and the combined effects of dispersion, mode-partition noise, and laser chirp.

which results in much lower chirp[2] than a direct modulated laser, the laser line-width can be reduced to approximately 1.2 times of the bit-rate R_b. Then the dispersion limit becomes

$$L_D = \frac{\epsilon}{1.2 R_b^2 D} \tag{4.3}$$

This results in a 1000 km dispersion limit in the previous OC-48 case. However, it is evident that the dispersion limit decrease with R_b^2 from (4.3), which means it shrinks to 1/16 for every generation of fiber-optic systems, whose bit-rate increases by 4 times every generation. For example, the same fiber network has a dispersion limit of less than 70 km for OC-192 (10 Gb/s), and about 4 km for OC-768 (40 Gb/s). Therefore, CD has a major impact on long-haul fiber-optic systems. Since the introduction of erbium-doped fiber amplifiers, fiber-optic systems began shifting to 1.56 μm transmission window, in which erbium-doped amplifiers are more effective than in the 1.3 μm transmission window. This makes CD more problematic since most conventional fibers were designed to have minimum CD in the latter.

Polarization mode dispersion (PMD) [85][84] occurs because of the velocity difference between the two polarization modes in single-mode fibers, which can be caused by fiber asymmetry, fiber bending, temperature variation, etc. PMD is a random process and can only be describe using a statistical model [86]. PMD is proportional to the square of the bit-rate and square root of the distance, and is usually given in ps/$\sqrt{\text{km}}$, typically 0.1$\sim$0.5 ps/$\sqrt{\text{km}}$. For fiber-optic networks operating below 10 Gb/s, PMD effect is usually smaller than that of CD. However, it becomes more problematic as the data rate further increases.

4.2 Dispersion Reduction

In order to reduce the dispersion effects on fiber-optic system performance, different methods have been proposed and implemented in all three parts of a regenerator span (transmitter, fiber, and receiver) and in both optical and electrical domains. Each method has its own distinctive advantages and disadvantages. The main criteria for a good dispersion reduction method are small power penalty (low loss), good integration with current network, low cost, and tunability/adaptability. The latter is important because: 1) dispersion is usually time-variant due to environmental changes such as temperature variation; 2) dispersion is also

[2]Chirp refers to the shift of the lasers center wavelength during single pulse durations.

related to fiber length, and thus a tunable solution would be faster, easier, and cheaper to implement and maintain.

Traditionally, spools of *dispersion compensating fibers*, which have negative dispersion compared to common fibers, are placed at intervals along the network in long-haul systems (typically stacked atop telecommunication racks, and approximately 15km for every 80km) to compensate chromatic dispersion. But they also cause extra loss and nonlinearity.

Later, *dispersion shifted fibers* are introduced in long-haul systems, which have a more complex refractive index profile and less dispersion. They are engineered to have both minimum attenuation and dispersion at the transmission window around 1550 nm wavelength. However, due to the high installation cost, dispersion shifted fibers only comprise a small portion of the global fiber-optic networks.

Recently, interferometers are used to implement optical equalization, i.e., providing wavelength-dependent paths of different lengths for different spectral components. For example, chirped fiber Bragg gratings are formed in optic dispersion compensation modules (ODCM) [87] by changing the fiber refractive index periodically. Since light is reflected if its wavelength is half of the grating period, different spectral component will be reflected at different lengths if the grating period changes continuously along the signal path. These devices offer very low loss, and multiple gratings in series can handle WDM signals. However, they require an optical circulator to separate the input signal from the reflected signal.

All these optical solutions tend to have narrow bandwidth, and thus can only compensate dispersion at the center wavelength, which is less effective in WDM systems. More importantly, they are expensive to deploy and maintain, and thus are only viable in long-haul telecommunications. For local area networks such as 10G Ethernet [77], there is a strong demand for an electrical solution, which is highly desirable in long-haul systems as well.

In the electrical domain, fiber dispersion can be compensated at the transmitter by pre-emphasis [88] or coding [89]. However, both approaches lack adaptability, and coding also lowers channel capacity. Instead, equalization at the receiver is preferred, which is expected to be integrated with the receiver circuit (Fig. 4.3).

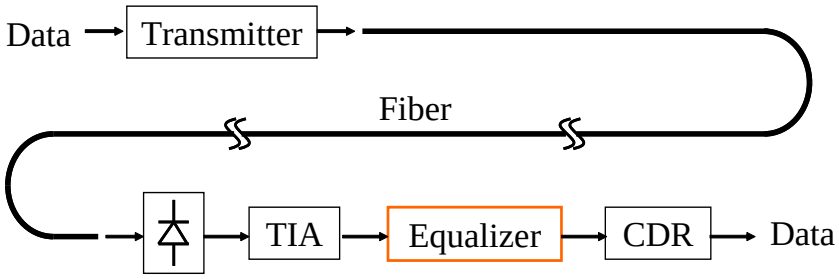
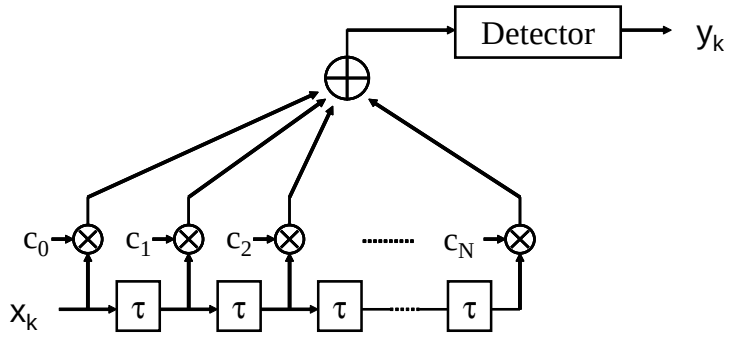
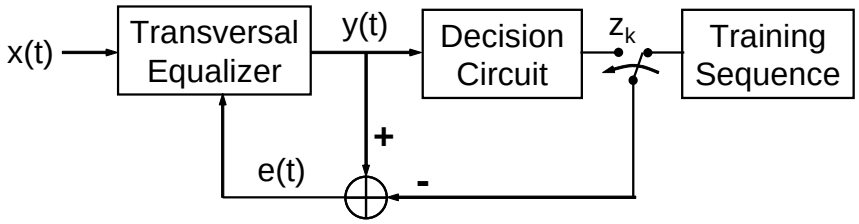


Figure 4.3: Dispersion compensation by equalization.



(a)



(b)

Figure 4.4: Transversal equalizer. (a) basic structure; (b) adaptive transversal equalizer.

4.3 Distributed Transversal Equalizer

In a communication system, equalization is the process of correcting channel induced distortion such as dispersion in fiber-optic systems [75]. An equalizer is essentially an FIR filter that can be electrically adjusted to compensate the distortion. Its frequency response multiplied by actual channel response yields the assumed channel response that was used in system design. Equalizers have been widely used in telephone networks and disk drives [90].

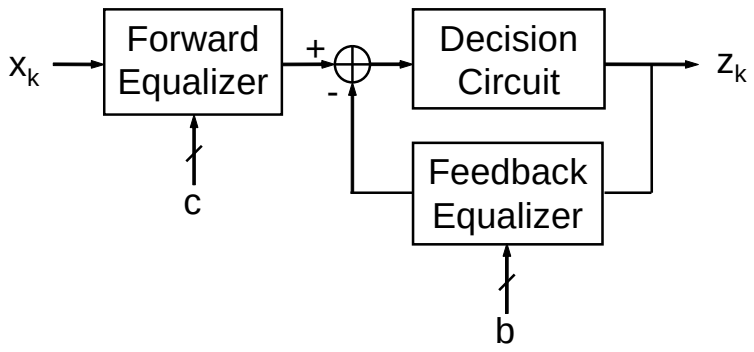


Figure 4.5: Decision-Feedback Equalizer.

4.3.1 Transversal Equalizer

In a transversal equalizer (Fig. 4.4a), the input signal $x(t)$ propagates along a delay line. The signal $x(t)$ and its delayed versions of $x(t - k\tau)$ (where $\tau = T$, the signal period, and $k = 1, ..., n$) are *tapped* along the delay line with equal space, multiplied by equalization coefficients (weights), and then summed to generate the equalized output $y(t)$. Thus this architecture is sometimes referred to as a *tapped-delay-line* structure. A fractionally-spaced equalizer has delay of $\tau < T$ (typically τ is selected to satisfy the Nyquist sampling theorem for the input signal, i.e., the "sampling" rate of the equalizer $1/\tau$ is higher than twice the input signal bandwidth). Thus an fractionally-spaced equalizer can overcome the aliasing problem in a T-spaced transversal equalizer and improve the equalizer performance [91]: 1) it can equalize both slopes of the input signal spectrum separately, and thus can effectively compensate more severe delay distortion; 2) it is less sensitive to sampling-time error (jitter); 3) it has less noise enhancement.

An adaptive transversal equalizer is shown in Fig. 4.4b. In the initial training period, a known training sequence is transmitted and compared with its local copy in the receiver to find the channel characteristics and calculate the initial values for the equalization coefficients. Then the coefficients can be adjusted based on the decision results using adaptive algorithm such as least-mean-square (LMS) [92] and zero-forcing algorithm [93].

A decision-feedback equalizer [94][95] is a nonlinear equalizer, and usually consists of a forward equalizer and a feedback one, both of which can be a transversal equalizer (Fig. 4.5). Decisions made on the equalized signal are fed back, and the ISI caused by these symbols can be canceled (with appropriate weights) from the equalizer output. Compared to a linear equalizer, a decision-feedback equalizer has the following advantages: 1) it is less sensitive

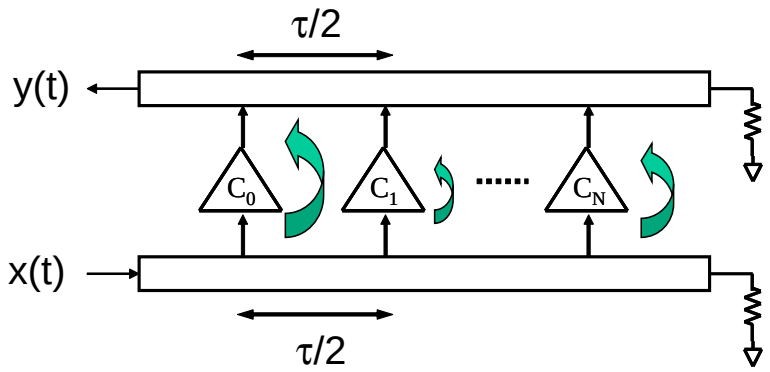


Figure 4.6: Transversal equalizer with on-chip transmission lines as delay elements.

to sampler phase; 2) it can achieve better performance with the same circuit complexity; 3) it is particularly useful for channels with severe amplitude distortion.

From the above discussions, we can see transversal equalizers are of particular importance. They have relatively simple structures, and can compensate any type of linear distortion and can be made adaptive easily. They can also be used as building blocks for more advanced equalizer architectures, such as decision-feedback equalizers and maximum likelihood detection [96].

4.3.2 Distributed Architecture

At low speed, transversal equalizers can be implemented as digital FIR filters: the input signal is first sampled and digitized, and the delay line can be constructed using a shift register [97] or memory [98]. Consequently, the maximum data-rate is limited, usually below 1 Gb/s, while the circuit complexity and power consumption would be unacceptable at high speed. In addition, clock generation poses another problem if fractionally-spaced equalization is required. Therefore, continuous-time transversal equalizers have been explored for high-speed applications, using charge coupled devices (CCD) [99], surface acoustic wave (SAW) filters [100] as well as switch capacitors [101] and G_m-C ladder filters [102][103]. Beside speed, such analog equalization has an additional advantage: since sampling is done after equalization, signal delay in the equalizer does not affect the performance and stability of the clock-and-data-recovery (CDR) [104]. However, as signal speed further increases beyond 1 Gb/s, even these analog equalizers become inadequate to achieve the high-speed operation. Instead, RF and microwave approaches are needed.

Distributed circuits are a good candidate for high-speed integrated circuits because of their unique wideband characteristic, which was originated from traveling-wave amplifiers (see Section 2.1). Fig. 4.6 shows an integrated transversal filter using a distributed architecture. The similarity with a traveling-wave amplifier is immediately evident. In fact, it can be viewed as a traveling-wave amplifier operating in the reverse-gain mode. The input signal travels along the input transmission lines, and tapped by each gain stage in sequence (from left to right in Fig. 4.6). Thus the loaded transmission lines act as delay elements. The tapped signal is amplified by each gain stage by a gain that corresponds to the corresponding equalization coefficient (weight), and the output signals from all stages are added on the output transmission lines. It should be noted that the delay between adjacent stages consists of that from both the input and output transmission lines.

Compared to conventional digital and analog transversal equalizer architectures, this architecture has the following advantages:

- It is an RF implementation, which can operate at very high data-rates compatible with all current fiber-optic systems.
- It is an integrated circuit solution, which reduces the system complexity and cost significantly compared to conventional optical methods.
- The equalization coefficients can be realized by the gain from each stage, and thus it is inherently adaptive.
- It is more power efficient since there is no power-hungry DSP as in digital implementations.
- Fractionally-spaced equalization can be easily implemented without over-sampling.

This architecture was first contemplated by Rauscher [105]. In 1989, Schindler developed an MMIC bandpass transversal filter at 9.8-11.1 GHz using microstrip lines and on-chip capacitors [106]. Kasper and Mizuhara first suggested to use such an integrated transversal filter for fiber-optic equalization [79], followed by others with simulation results [107][108]. In 1997, Jamani et al [109] and Borjak et al [108] reported the first implementations using reverse-gain mode and forward-gain mode (in traveling-wave amplifier terminology), respectively. The latter group later switched to the reverse-gain mode architecture [110]. In 2000,

Lee and Freundorfer introduced Gilbert cell to generate both positive and negative weights [111]. These implementations verified that it is feasible to use distributed amplification techniques to achieve integrated transversal equalizer for high-speed fiber-optic systems.

However, there are important questions to be answered and serious problems to be solved:

- Analog weight adjustment. There is no such mechanism reported in [108] and [110], and only binary weight control (on/off) in [109] (because of the cascode gain stage) and [111]. Without analog weight adjustment, adaptivity cannot be achieved.
- Unlike a traveling-wave amplifier, the gain stages have to be controlled independently with varying weights to achieve the adaptive transfer function. This makes it very difficult to maintain the same loading on the transmission lines from all stages at all time, i.e., the transfer function itself tends to disrupt the distributed circuit characteristics.
- Systematic analysis and equalization test data are still lacking.

4.4 Design

It is the goal of this work to answer the questions above in the context of a practical fiber-optic system [112]. A generic 10 Gb/s multi-mode fiber optic system was chosen, which is fully compatible with the newly adopted 10 Gigabit Ethernet standard (IEEE 802.3ae) [77]. Based on system simulations using data from different lasers, fibers, and launch conditions, link distance improvement was evaluated versus complexity, number of stages and delay per stage. It was concluded that a 7 tap transversal equalizer with a 50 ps delay per stage would be adequate [113], which resulted in the following specifications:

- Input bit-rate: 10Gb/s
- Bandwidth: 7 GHz
- Architecture: fractionally-spaced transversal equalizer.
- Time delay: 50 ps/stage
- Voltage gain/stage: 0 dB max

4.4.1 Technology Choice: SiGe BiCMOS

The use of SiGe BiCMOS technology [114] is critical to the successful implementation of the proposed circuit for the following reasons:

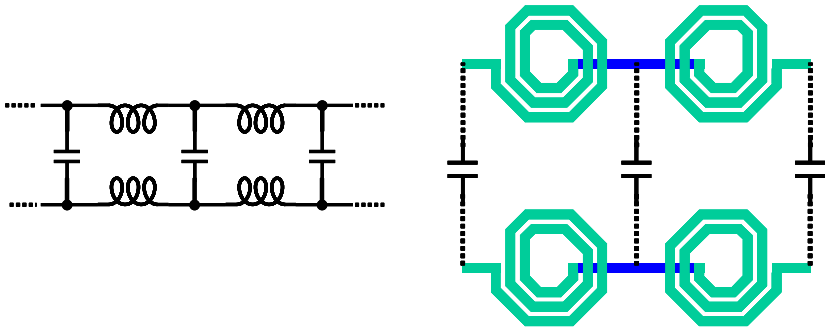
- A complete adaptive equalizer requires both high-frequency RF/analog (transversal filter) and high-speed digital circuits (equalization coefficient update circuitry). The system-on-a-chip (SoC) requirement basically limits our choice to silicon-based technologies, because III-V semiconductor technologies are simply not ready for such high-integration applications, and multi-chip module (MCM) solutions have problem with high-speed digital interface.

- The equalizer requires transistors that can handle the wideband signal from dc to 7-GHz (for 10-Gbps applications) with very good linearity and reasonable power consumption. This makes SiGe BiCMOS the best choice in silicon technologies.

- SiGe BiCMOS also provides high-Q on-chip passive components (spiral inductors, MIM capacitors, and varactors), which are needed for the construction of transmission lines in the equalizer.

4.4.2 Delay Lines

As we discussed in Chapter 3, the design of transmission lines is of critical importance. In the case of distributed transversal equalizers, we have a new constraint: large time delay per stage. For the prototypes, the delay per stage is specified as 50 ps, i.e., half of the symbol period. To achieve this amount of delay, microstrip lines or coplanar waveguides would be too long to be effectively implemented on-chip. For example, for microstrip lines with metal groundplane, the phase velocity of a TEM wave can be estimated as $v = c/\sqrt{\epsilon_{SiO_2}} = 0.5c$, and then the microstrip line length per stage would be $l \approx vt_d = 0.5c \times 50\text{ps} = 7.5\text{mm}$. Even if the loading effect is taken into account, the required length is still impractical. Note that using smaller fraction of signal period for each stage does not solve this problem – larger number of stages are needed since the equalizer still needs the information from its previous symbols to correctly cancel the ISI. Instead, we used artificial transmission lines constructed with LC ladders of spiral inductors and MIM capacitors, which can generate larger delay for a given chip area.



(a) (b)

Figure 4.7: Section of LC delay lines. (a) schematic; (b) layout.

Another important question is ac grounding. Since the physical size of the equalizer is comparable to the wavelength, the return path for the ac current must be taken into account, which introduces considerable loss. It is also a difficult problem for modeling since the equalizer is a wideband system. In order to overcome the problem, differential architecture is adopted for the equalizer, i.e., differential transmission line structures and differential gain stages. In this manner, there is a local virtual ground within each gain stage and each section of transmission line structures, since the fundamental frequency components of the differential ac currents cancel each other.

Fig. 4.7 shows a section of the delay line structures between each gain stages for both the input and output transmission lines. Unlike distributed amplifiers, there is no strict synchronization requirement for transversal equalizers. Since the spiral inductors are densely packed, the electromagnetic coupling between them has to be properly modeled. A 6-port electromagnetic simulation [115] is used to simulate the whole transmission line section, and generate frequency-swept S-parameters for circuit simulation.

4.4.3 Gain Stage

The function of the gain stage in a transversal filter is to implement the equalization coefficient (weight). Thus it should have a flat and linearly-controllable amplitude response. It should also be able to change the phase of its gain by 180°, i.e., to generate negative coefficients. A flat group-delay response across the equalizer bandwidth is required to prevent phase distortion in the equalization process, which is more critical because it cannot be easily compensated by equalization itself. Therefore, the gain stage can be considered an

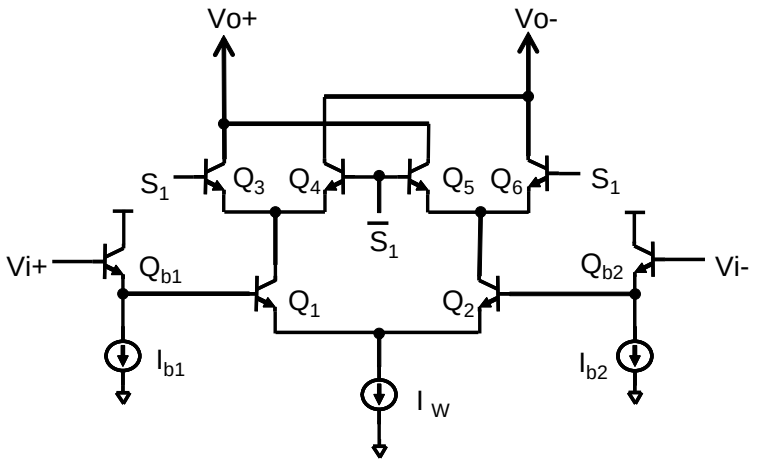


Figure 4.8: Gain Stage.

analog multiplier with a high-speed data input and a low-speed control signal. In addition, the gain stage should present a constant load to both the input and output transmission lines when changing the weights to maintain a constant delay between adjacent stages.

Fig. 4.8 shows the simplified schematic of the gain stage. The core of the circuit is a differential amplifier (Q_1 and Q_2). Additional circuits are added to accomplish the analog multiplication. The weight is implemented using the tail current source I_w. In this manner, the weight linearity, i.e., from I_w to the output voltage, is better than a cascode structure like in [109]. I_w is implemented using a current mirror, and thus the weights can be controlled linearly. In our prototypes, they are controlled manually.

The sign of the weight is implemented using two differential pairs (Q_3, Q_4, Q_5 and Q_6) to steer the differential current from Q_1 and Q_2 to the output transmission lines. The control signals of these transistors (S_1 and $\bar{S_2}$) are analog voltages (V_{on} and V_{off}) selected by a single digital bit (S), which represents the sign of the corresponding equalization coefficient. Because the output nodes are always connected to the collector of a "ON" transistor and that of a "OFF" transistor, there is no loading variation on the output transmission lines.

The differential input signals are buffered using emitter followers (Q_{b1}, Q_{b2}, I_1 and I_2). Buffering reduces the loading and thus improve the phase response linearity on the input transmission lines. Further, the buffers are biased with constant currents, and thus the parasitic capacitances of Q_{b1} and Q_{b2} do not change with the weight (I_w). So there is no loading variation on the input transmission lines.

Overall the gain stage satisfies the *strong impedance mismatching* condition between

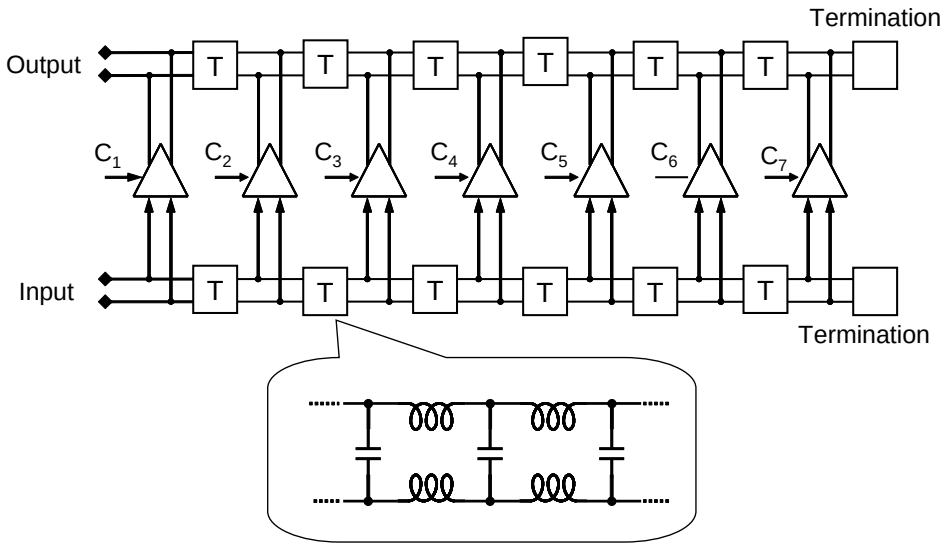


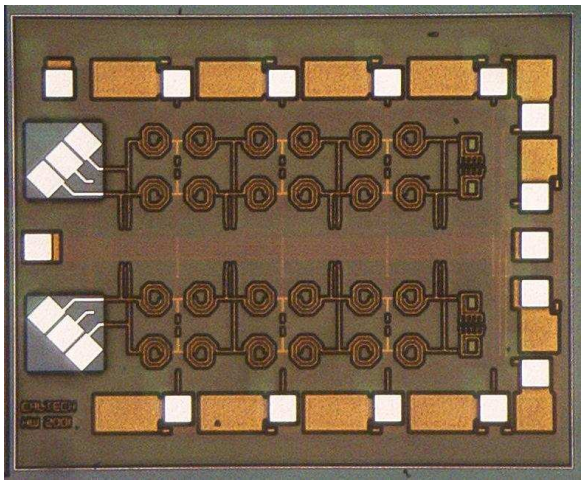
Figure 4.9: Schematic of prototype equalizers.

succeeding stages [116]: the input transmission lines have a low impedance (50Ω); the emitter-follower buffers have a high input impedance and low output impedance ($1/g_m$); the core differential amplifier has high input impedance and very high output impedance; the switching pairs (common base) have a low input impedance ($1/g_m$) and high output impedance; and the output transmission lines have a low impedance (50Ω). In this manner, the gain stage can achieve the stringent requirements for bandwidth and group-delay.

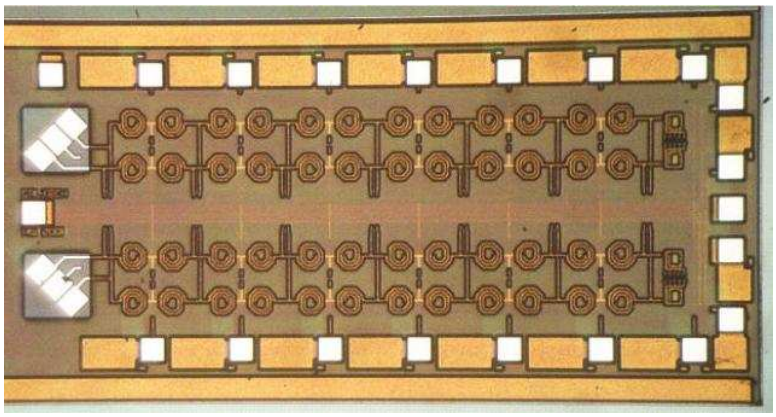
4.4.4 Prototype Design

Two prototypes of distributed transversal equalizers were designed and fabricated [112] using IBM's 0.18μm SiGe BiCMOS 7HP process with f_T of 120 GHz [10]. Fig. 4.9 shows the top-level schematic of the 7-tap prototype. The other one has 4-taps. They were simulated using ADS [117] with frequency-swept S-parameters of the transmission lines from IE3D [115].

Figure 4.10 shows the chip micrographs of the prototype transversal equalizers. The 4-tap equalizer occupies an area of 2.5 mm x 1.5 mm, and the 7-tap equalizer is 3 mm x 1.5 mm, both including pads. The pads on the top are inputs of sign bits of weights, and the bottom ones are inputs of absolute values of weights (reference voltage for the current mirror). The pads on the right-hand side are for "ON"/"OFF" voltages and dc bias. The left-hand side pads are differential input and output, which are titled 45° for RF probing. Note that the



(a)



(b)

Figure 4.10: Prototype transversal equalizers. (a) 4 taps; (b) 7 taps.

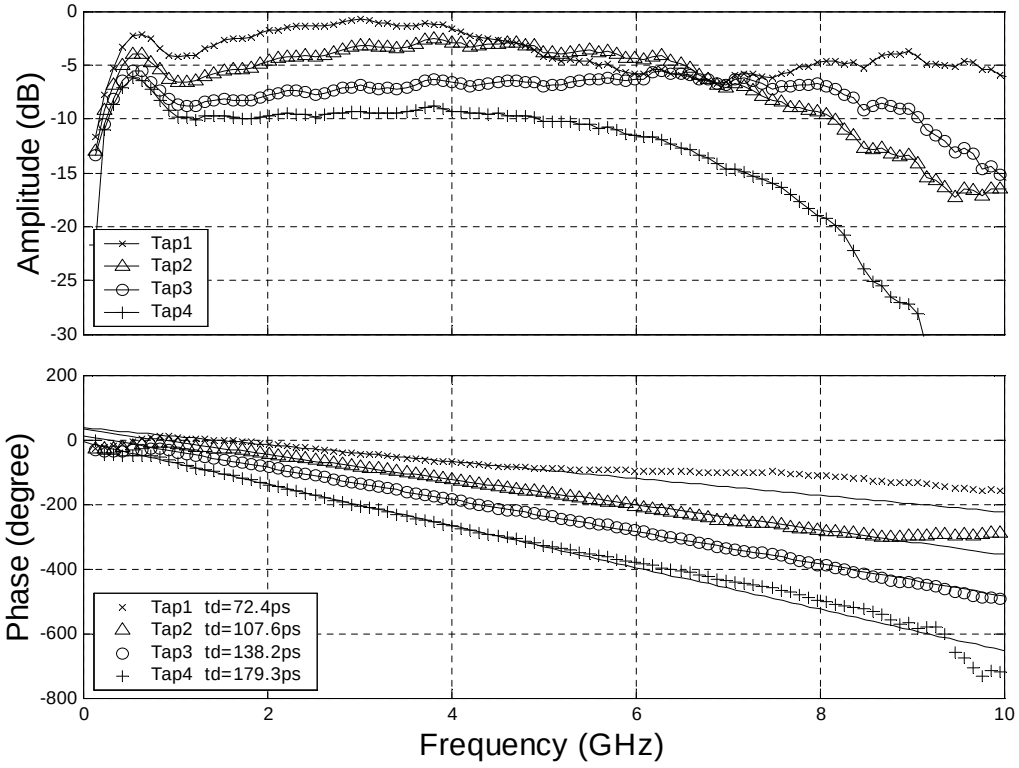


Figure 4.11: Frequency response of the 4-tap equalizer.

terminations have multiple resistors in parallel, which can be laser-trimmed to find-tune the matching properties of the transmission lines.

4.5 Measurement Results

Figure 4.11 shows the frequency response of the 4-tap equalizer with each tap weighted independently. It demonstrates the basic characteristic of a distributed circuit, i.e., each tap has similar shape response within the bandwidth with attenuated amplitude along the length. The low-frequency drop-off is due to the ac-coupling capacitors in the input bias tees. The amplitude fluctuation is larger than the simulation, possibly due to the following reasons: 1) due to equipment limitations, it was a single-ended network analysis instead of differential measurement, i.e., only one input and one output are used; 2) termination is not find-tuned to achieve the best matching for both transmission lines; 3) the wideband modeling of transistors and spiral inductors are not accurate.

Fig. 4.12 shows the pulse response of the 7-tap equalizer to a 2.5 GHz square wave

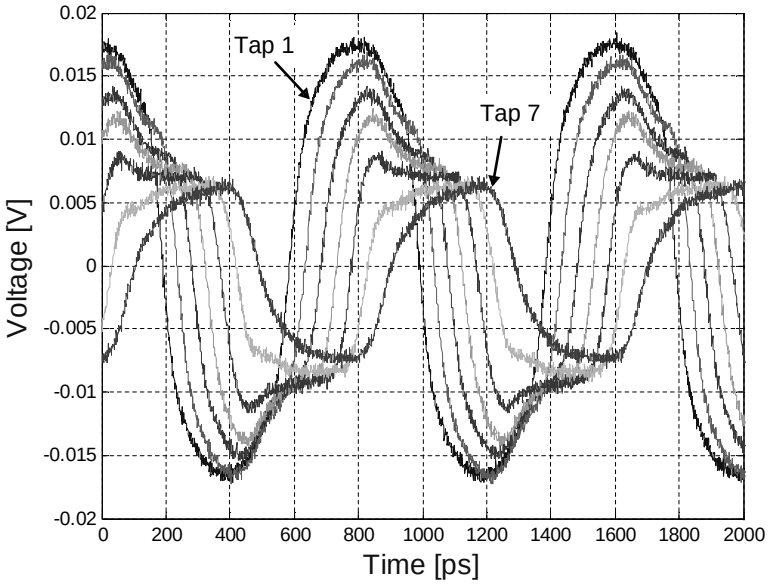


Figure 4.12: Pulse response of the 7-tap equalizer. (Courtesy of J. Tierno et al, IBM Research.)

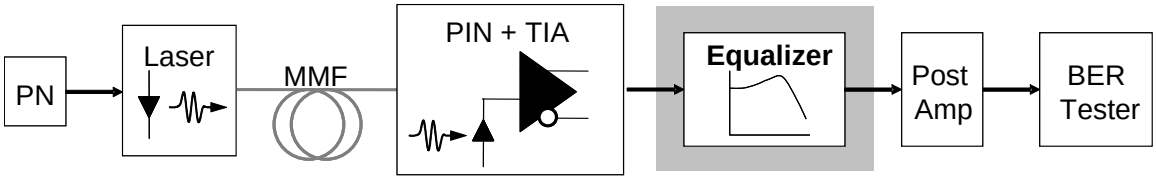


Figure 4.13: Equalization test.

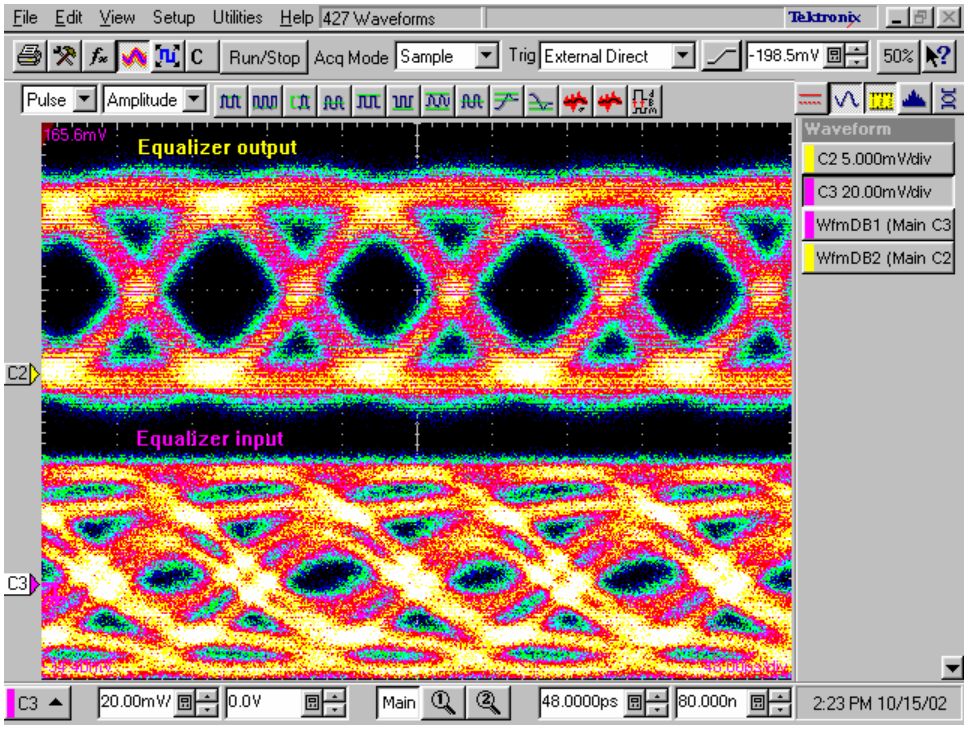


Figure 4.14: Eye diagrams for 800 m 50μm of multi-mode fiber before and after equalization.

input with each tap weighted independently. The delay per stage is approximately 50 ps. The pulse response from the earlier taps also has more high-frequency peaking and less attenuation than that from later stages.

The actual equalization ability of the equalizer was tested using the setup in Fig. 4.13, which is similar to its application environment. A pattern generator was used to drive a 850nm vertical cavity surface emitting laser (VCSEL) using direct modulation, and 800m of 50μm non-compliant NGMMF fiber was used to generate distortion on the signal. The pattern was set to be $2^{31} - 1$ PRBS, K28.5 8b/10b pattern and the data rate was 10Gb/s. This generated a signal with 5dB of ISI at the input of the equalizer, while the equalized signal has residual ISI of only 1.38dB. Also notice that the equalization operation did not degrade the jitter performance – the deterministic jitter in fact was reduced from 62ps to 38ps. The overall BER was improved from about 10^{-5} to less than 10^{-12}. Figure 4.14 shows the eye diagrams, before and after equalization using the 7-tap equalizer.

While the equalization chip was designed to operate on 10 Gb/s signals, it was tested at higher speeds of 12.5Gb/s and 14Gb/s (limited by equipment). The signal from the pattern generator passed through the same setup as before resulting in even larger eye closure and

ISI penalty. Similarly to the previous case at 10Gb/s, the signals were recorded at the input of the equalizer, the output of the equalizer with only one coefficient active and with two coefficients active to reduce the ISI penalty. In the last case the ISI penalty was reduced to negligible values.

The total power dissipation, including all biasing circuits, is 30mW, plus 2mW per active coefficient (typical max dissipation is 40mW).

4.6 Future Improvements

We have demonstrated that integrated transversal equalizer can be used in high-speed fiber-optic communication networks to fight the problem of dispersion. The next question is how to generate the coefficients so as to close the feedback loop and complete the adaptive equalizer. Again the conventional digital solution, which updates the coefficients in every symbol period, is not an option at such high speed. Some analog technique has to be used, which can be controlled by some digital circuits at lower speed generated by DSP after detection. It is also important to study the systematic behavior of such an equalizer, and use it as guidelines for the design.

4.7 Summary

Inter-symbol interference caused by fiber dispersion imposes a major limitation on data rate and transmission distance in high-speed fiber-optic systems. Compared to optical-domain and other electrical-domain dispersion compensation methods, equalization with transversal filters based on distributed circuit techniques presents a cost-effective and low-power solution in these systems. The design of integrated transversal equalizers has been further discussed with detailed analysis on transmission lines and gain stages, followed by measurement results for a 4-tap and 7-tap distributed transversal equalizer prototypes implemented in a commercial $0.18\mu m$ SiGe BiCMOS process for 10 Gp/s multi-mode fiber optic systems. The future work will answer the other part of the challenge: how to generate the equalization coefficients at such high speed and make the equalizer fully adaptive.

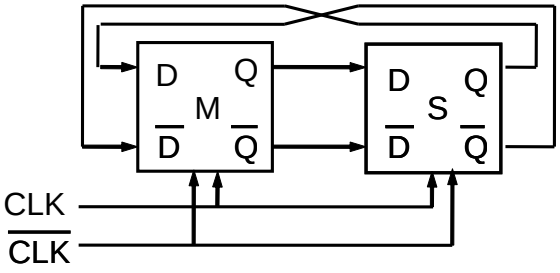
Chapter 5

Injection-Locked Frequency Dividers

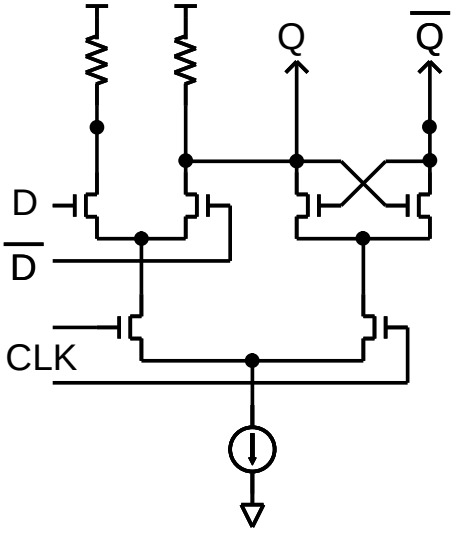
This chapter discusses applying injection locking techniques in frequency dividers, i.e., *injection-locked frequency dividers* (ILFD's). After introducing the problem in high-speed frequency divider design and different categories of frequency dividers in Section 5.1, ILFD's are presented as a promising solution, followed by analysis in Section 5.1.3. Two prototype divide-by-2 ILFD's with *shunt-peaking locking-range enhancement* are demonstrated in Section 5.2. Quadrature signal generation is discussed in Section 5.3. Lastly, a new type of low-phase-noise quadrature oscillators, *self-dividing oscillators*, will be presented in Section 5.4.

5.1 Challenges in High-Speed Frequency Dividers

Frequency dividers are essential building blocks in modern communication systems [45][46][118]. They are widely used in frequency synthesis, quadrature signal generation, MUX/DEMUX, and radar systems. They are also frequently used as a benchmark for new process technologies, particularly in digital circuits. As the operation frequencies of communications increase, the trade-off between the speed and power dissipation of dividers becomes more critical, especially in wireless applications such as mobile phones. For example, they have become one of the major sources of power dissipation in widely-used frequency synthesizers [119][120]. Associated with large power dissipation, high-speed frequency dividers can also introduce considerable noise degradation in the system. For example, a digital frequency divider with large power consumption can increase the noise floor the frequency synthesizer



(a)



(b)

Figure 5.1: TFF static digital divider. (a) Block diagram; (b) Flip-flop.

if the divided signal is directly output from the divider core without buffering [121][122], which is particularly problematic for broadband systems since it affects the phase noise at large offset of the synthesizer.

Existing frequency-division techniques can be categorized into two groups: digital and analog dividers. The more suitable names for them might be *wideband* and *narrow-band* because signals in high-speed "digital" dividers can look quite different from 0's and 1's in digital circuits: (1) they have small amplitude; (2) their waveform is closer to sinusoidal instead of square pulses; (3) they are very sensitive to the input threshold voltage and amplitude (i.e., input signal power). Therefore, they should be considered as analog circuits, and designed using analog techniques and methodologies.

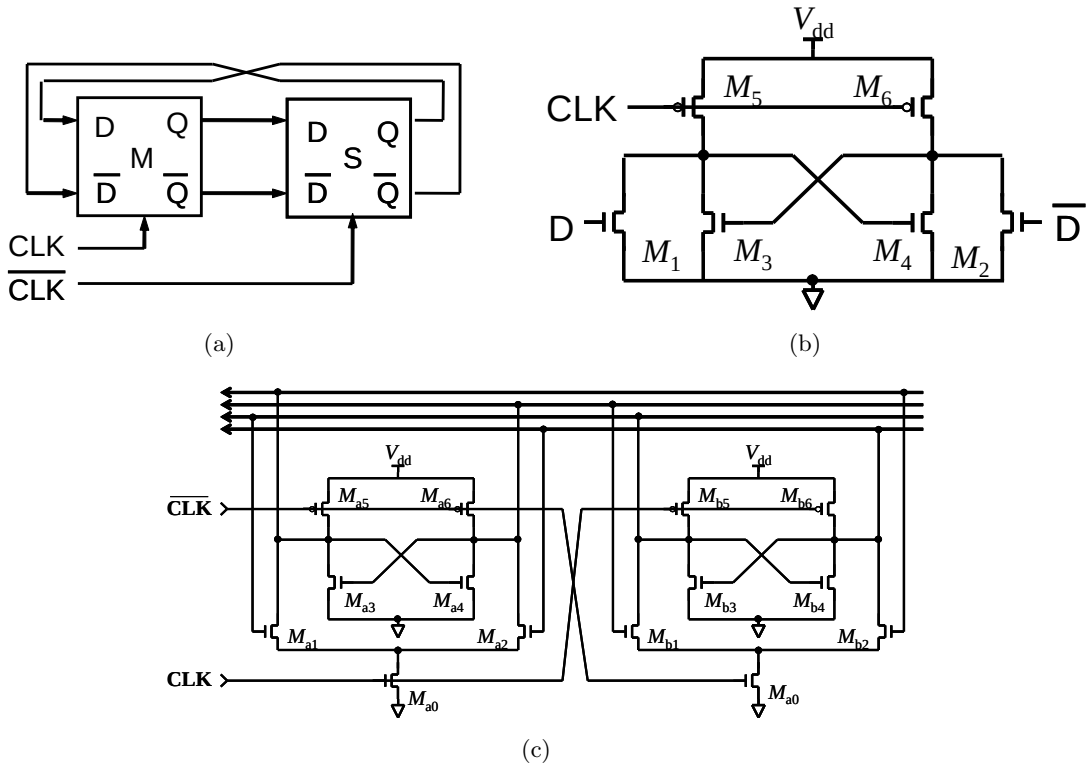


Figure 5.2: Advanced static digital divider. (a) Razavi's divider; (b) D-latch; (c) Wang's divider.

5.1.1 Digital Frequency Divider

Currently most high-speed frequency dividers in communication systems are digital dividers because it is believed that they have simpler architecture and larger bandwidth than analog dividers, offering further robustness over process variations. Therefore, they are considered indispensable in wideband applications such as MUX and DEMUX in fiber-optic systems and more reliable in other applications such as frequency synthesis in wireless communications.

Digital dividers can be further categorized into *static* and *dynamic* digital dividers. Static digital dividers can operate down to very low frequencies, while dynamic dividers cannot.

Fig. 5.1 shows a static digital divider with the commonly-used *master-slave toggle-flip-flop* (TFF) architecture. It consists of two identical and cross-coupled flip-flops (Fig. 5.1b), which are implemented in a current-steering topology with a differential pair for sensing, and a cross-coupled pair for regeneration.

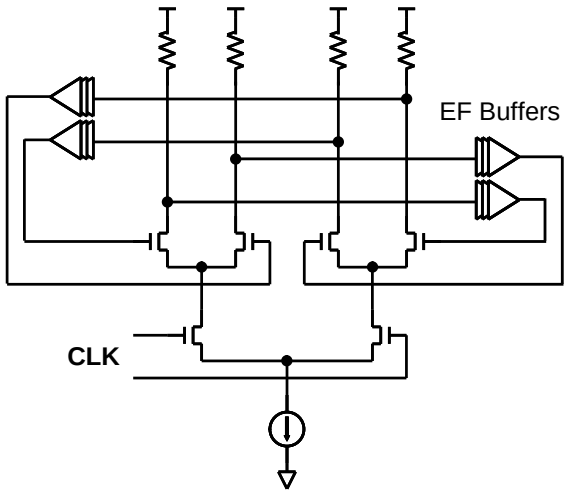


Figure 5.3: Dynamic digital divider.

A modified architecture of SFD's [123][124] uses D-latches instead of full-blown flip-flops as shown in Fig. 5.2a and b. PMOS transistors are used as dynamic loads. Notice that the D-latch does not disable its input in its regeneration phase, which is problematic in general digital circuits [123]. This confirms that digital dividers are not really digital. Fig. 5.2c shows an improved version [125] which combines the toggle operation of flip-flops (only for the sensing pair) with dynamic loads.

Dynamic digital dividers can be implemented by removing the regeneration pair from static dividers in Fig 5.3. Now the internal parasitic capacitances serves as storage elements, which leads to faster toggle rate, i.e., higher maximum input frequency. The drawback is that they cannot function properly below some minimum input frequency, i.e., they have smaller bandwidth. Some other implementations use *regenerative division* method like in regenerative analog dividers, and will be discussed in Section 5.1.2.

As shown in Table 5.1, high-speed digital dividers have the capability to operate over a wide frequency range. In order to achieve such large bandwidth, however, they require high supply voltages and large power dissipation. The latter is due to the complete charging and discharging of capacitances during each cycle, which results in unnecessary energy loss in Fig. 5.4. Although dynamic loading [125] can be used to alleviate this problem to some extent, the fundamental problem with energy loss still remains because of the wideband nature of digital dividers. Also, as in most digital circuits, digital dividers generate large amount of white and $1/f$ noise, which degrades the noise performance of the whole system,

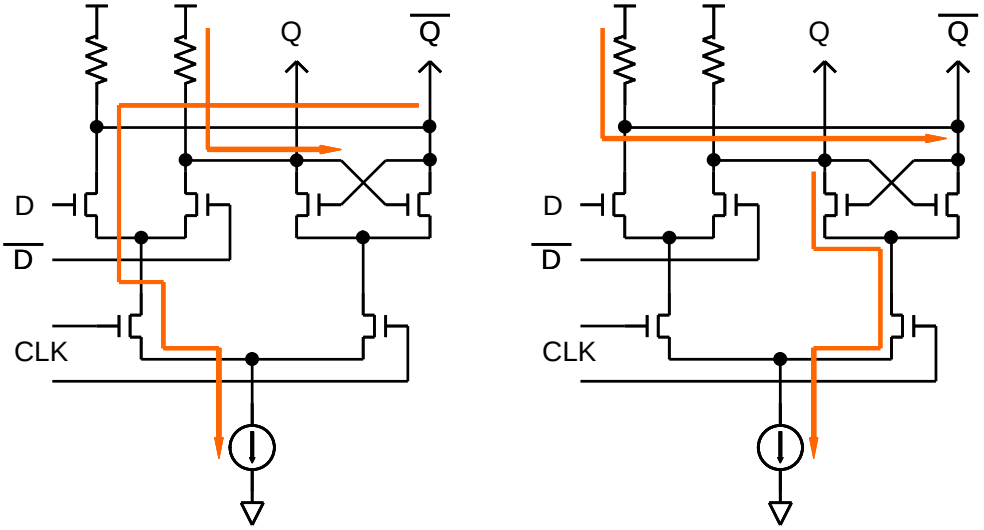
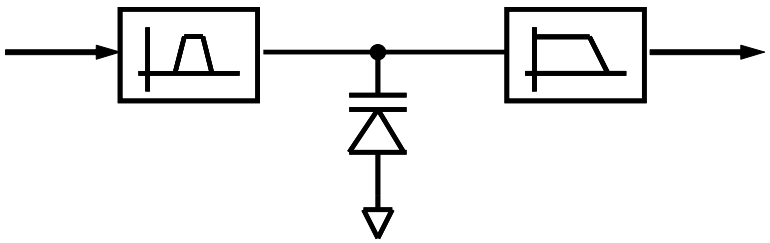


Figure 5.4: Power dissipation of a flip-flop in a digital divider. (a) Flipping phase; (b) latched phase.

Ref	Type	Frequency (GHz)		P_d (mW)	V_{dd} (V)	Sensitivity @F_{max} (dBm)	Technology
		max	min				
[123]	s	13.6	N/A	28	2.6	N/A	0.1μm CMOS
[126]	s	42	<3	300*	-6.5	0.4	68GHz SiGe HBT
[125]	s	18	<1	3.6	1.8	4	0.25μm CMOS
[127]	s	53	<2	303*	6.3	2	80GHz SiGe HBT
[128]	d	82.4	32	40	-5.2	-15	122GHz SiGe HBT
[129]	d	79.2	26.6	1075	7.5	4	80GHz SiGe HBT
[130]	s	25.4	<1	61	1.5	10	0.12μm CMOS

* Excluding power dissipation of buffers.

Table 5.1: Silicon-based digital divider performance



(a)

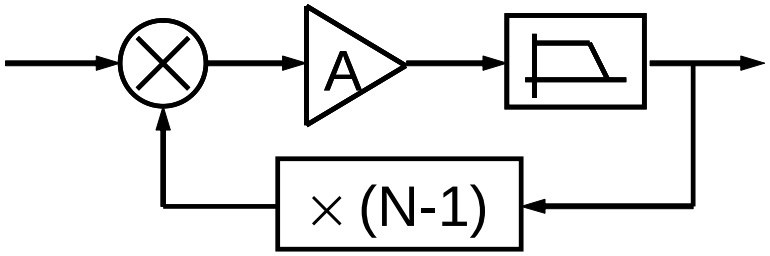
Figure 5.5: Parametric frequency dividers. (a) Parametric divider; (b) Carrier-storage divider.

For example, digital dividers in frequency synthesizers increase the noise floor and thus degrade the phase noise at large offset. Therefore, there is a strong demand for alternative approaches that can use lower supply voltage and reduce the power dissipation.

5.1.2 Analog Frequency Dividers

5.1.2.1 Parametric and Carrier-Storage Dividers

A parametric divider [41][131][132] consists of a band-pass filter, a nonlinear varactor, and a low-pass filter (Fig. 5.5a). The varactor generates sub-harmonics of the input signal due to its nonlinearity; the input band-pass filter isolate the signal source from the generated sub-harmonic signal; and the output filter isolates the output from the input signal frequency components. In this manner, RF energy is to transfer form the input frequency to its sub-harmonic by *parametric pumping*. Parametric dividers are widely used in microwave and millimeter-wave applications. However, it suffers from several drawbacks: (1) it is a "passive divider, and thus it has conversion loss instead of gain. So its input sensitivity is lower and output amplitude is smaller compared to dividers using active mixers. (2) In order to operate with normal-amplitude input signal and generate the output amplitude required by next stage, a pre-amplifier and post-amplifier are usually needed, which further complicates the circuit; (3) it is difficult to implement the required high-quality filters on-chip. Therefore, parametric dividers are not good candidates for high-speed silicon-based applications.



(a)

Figure 5.6: Regenerative frequency divider. (a) Operation; (b) Detailed block diagram; (c) Digital regenerative divider.

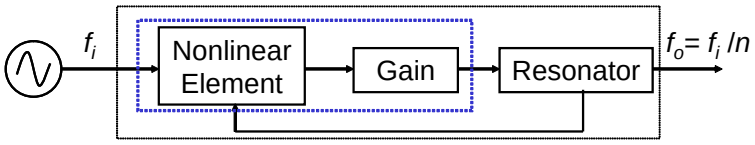


Figure 5.7: Injection-Locked Frequency Divider

5.1.2.2 Regenerative Dividers

A regenerative divider [133][134] is a *frequency feedback loop* which consists of a mixer, a low-pass filter, and possibly a multiplier (Fig. 5.6a). The input frequency f_i is mixed with the feedback frequency $f_f = (N-1)f_0$, and the lower mixing sideband $f_i - f_f$ is filtered out by the low-pass filter. Therefore, the output frequency is $f_0 = f_i - f_f = f_i/N$. Particularly, if the output is directly feeded back into the mixer without multiplication, the division ratio be $N = 2$, which is known as a *Miller divider*. Fig. 5.6b shows the block diagram of a typical MMIC implementation. As shown in Fig. 5.6c, some digital dividers also use regenerative mechanism with the intrinsic RC delay as low-pass filtering [128][129].

Compared to other analog dividers, regenerative dividers suffer from their complex circuit implementation, which also results in large power dissipation. It is also undesirable that a regenerative divider might need an initial signal to start [131], which further complicates the circuit.

5.1.3 Injection-Locked Frequency Dividers

A harmonic-injection-locked oscillator (see Section 2.3) can be used as an analog frequency divider (Fig. 5.7), i.e., an *injection-locked frequency divider* (ILFD). We can view ILFD's as a special type of regenerative dividers in which the nonlinear active device acts as a mixer,

and the resonator as the filter, with the feedback inherent in the oscillator [1].

Compared to other analog dividers, ILFD's have several advantages:

- ILFD's have simpler structure.
- ILFD's have lower power consumption.
- ILFD's do not require special devices or many filters, and thus are more suitable for silicon-based IC implementations.

An ILFD also has several advantages compared to a digital divider, which may or may not be the common characteristics of all analog dividers:

- It is fundamentally an oscillator that oscillates at the subharmonic frequency of the input signal, which effectively lowers the speed requirement for the technology by n-fold. So for a given technology, it can operate at higher frequency than a digital divider, whose speed is limited to a small fraction of the device cutoff frequency f_T.
- As a resonant circuit, only a fraction of the stored energy is dissipated in every cycle, which is determined by the quality factor Q of the resonator. This means that an ILFD can have lower power consumption than a digital divider.
- An injection-locked oscillator can be considered as an ultra-wide-band phase-locked-loop (PLL) in which the VCO and phase detector are combined and the loop filter is missing. Therefore, the "in-band" phase noise is suppressed by locking, i.e., the intrinsic phase noise of an ILFD does not affect the overall phase noise of the divided signal within the "loop bandwidth", which is its locking range. Further, its noise floor is also improved since it has higher power efficiency than digital dividers.

The advantage of better phase noise performance is worth a further look. Fig. 5.8 is a divide-by-2 ILFD and its waveforms in the time domain. The output signal is synchronized to the input n times in every cycle. As can be seen, if any phase error happens in the oscillation, it will be adjusted quickly back to the correct phase. Therefore, the phase noise of the output signal follows that of the input with a $20 \log N$ reduction, as in an ideal frequency divider [121]. This will be confirmed with the measurement data in Section 5.2.4.

[1] The other direction of this analogy may not be valid since the feedback loop in a regenerative divider preferably does not oscillate without the input signal.

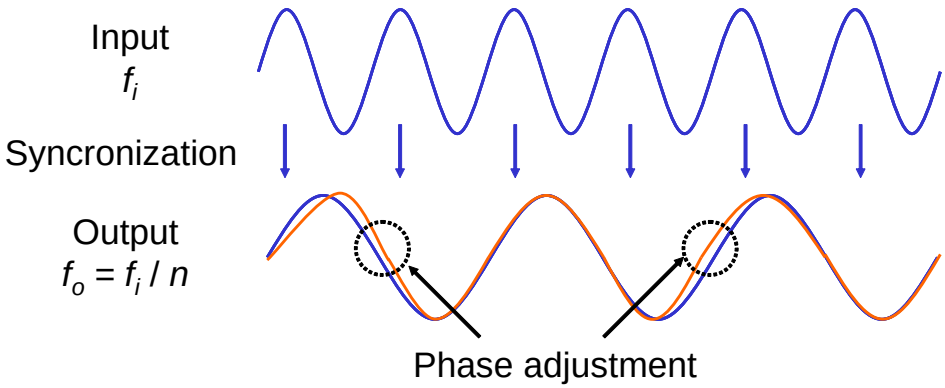


Figure 5.8: Phase Noise of ILFD's

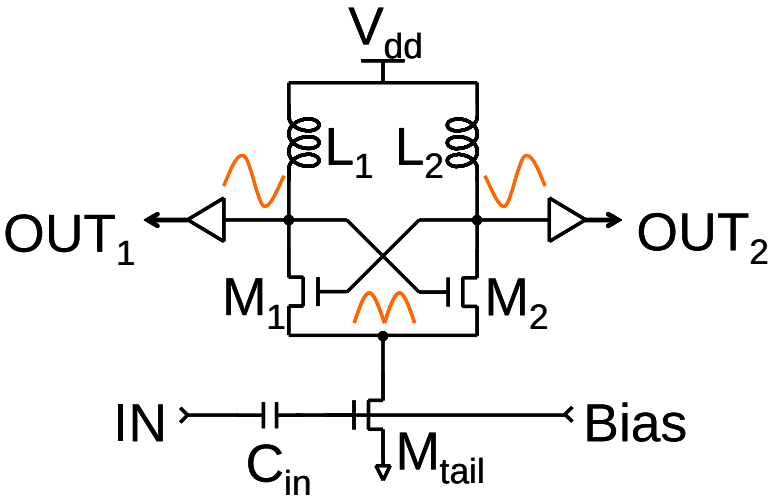


Figure 5.9: Divide-by-2 ILFD

5.2 Divide-by-2 injection-locked frequency dividers

The differential LC oscillator of Fig. 5.9 is a good candidate for divide-by-2 ILFD's because the tail node (the drain of the tail transistor, M_{tail}) offers natural frequency doubling, i.e., it oscillates at the second harmonic of the oscillation frequency when the oscillator is free-running. As we discussed in Section 5.1.3, it can also be viewed as a regenerative divider with a single-balanced mixer, LC band-pass filter and cross-coupled feedback.

The same way as other analog dividers, ILFD's have limited frequency range of operation, i.e., *locking range* (see Section 2.3), due to their narrow-band nature. Recalling Adler's formula (2.35), an injection-locked oscillator has a locking range that is proportional to the injected signal amplitude and inversely proportional to the resonator Q and oscillation amplitude. This still holds for harmonic injection locking in ILFD's, which will be verified

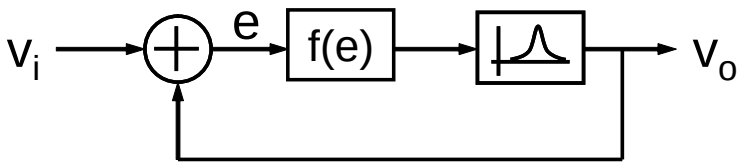


Figure 5.10: ILFD model.

with measurement results.

In [135], an ILFD is modelled as a regenerative divider(Fig. 5.10), in which the mixer is represented as a nonlinear function of the sum of V_i and V_o, and bandpass filtering is accomplished by the resonator with a high-Q approximation. Power series method [136][137] have been applied in the analysis of locking range. It is found to be

$$\Delta\omega = \Delta\omega_A \left[\frac{H_0}{2V_i} \sum_{m=1}^{\infty} K_{m,Nm\pm1} \sin(m\phi) \right] \tag{5.1}$$

with $\Delta\omega_A = \frac{\omega_r}{2Q}\frac{V_i}{V_o}$, the Adler's locking range (2.35). Here, H_0 and Q are the maximum value of the bandpass transfer function and quality factor of the resonator, V_i and V_o are the amplitude of the input and output signals, ω_r is the self-oscillation frequency of the injection-locked oscillator, $K_{m,Nm\pm1}$ is the power series coefficient, ϕ is the phase difference between the input and output signals. For a special case of $N = 1$ and $f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$, the locking range is found to be

$$\left| \frac{\Delta\omega}{\omega_r} \right| < \left| \frac{H_0 a_2 V_i}{2Q} \right| \tag{5.2}$$

Equation (5.2) can help us understand injection locking in ILFD's, and it also satisfies our intuition very well: locking range increases with the input signal amplitude V_i, open-loop gain H_0, and second-order nonlinearity a_2; it decreases with the resonator Q.

However, the injected signal is not always mixed with the feedback signal in voltage domain. Also nonlinearity may not be applied to both the input and feedback signal, nor is this necessary. In fact, this particular ILFD can be modeled as a regenerative divider using a single-balanced mixer, which is known to be nonlinear for the LO input (in our case $-V_o$ because of the cross-coupled feedback) and *linear* for the RF input (in our case V_i). Therefore, it is not clear how this model can be directly applied to many high-frequency circuit implementations of ILFD's. Therefore, instead of relying on this ideal model, it would be more meaningful to carry out the analysis for our particular implementation.

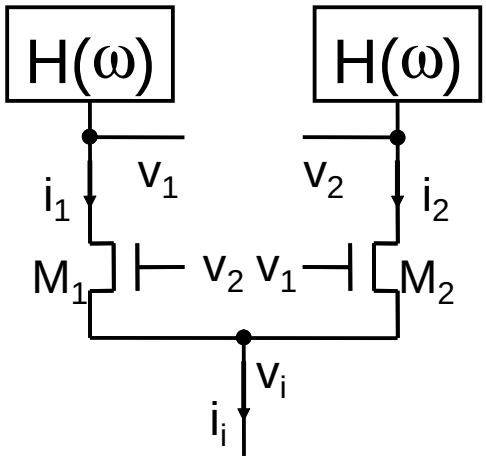


Figure 5.11: Locking Range Analysis.

5.2.1 Analysis

Fig. 5.11 shows the model for the locking range analysis, will be carried out using harmonic balance method [137]. Assuming that the fundamental frequency component, ω, dominates in the oscillation voltages v_1, v_2, we have

$$v_1 = V_{12} + V_o \sin(\omega t) \tag{5.3}$$

$$v_2 = V_{12} + V_o \sin(\omega t + \pi) \tag{5.4}$$

where V_{12} is the dc voltage ,and V_o is the oscillation amplitude, both at the drain nodes of M_1 and M_2.

Similarly, the second harmonic frequency, 2ω, dominates in the injected voltage v_i and current i_i at the tail node, i.e.,

$$v_i = V_I + V_i \sin(2\omega t + \phi_i) \tag{5.5}$$

$$i_i = I_I + I_i \sin(2\omega t + \phi_i + \phi_{vi}) \tag{5.6}$$

where V_I, V_i, I_I and I_i are the dc and ac amplitude of v_i and i_i, respectively. ϕ_{vi} is the phase difference between the injected voltage v_i and current i_i.

Further assuming that the transistors have second-order nonlinearity[2],

$$i_1 = a_0 + a_1 v_{gs_1} + a_1 v_{gs_1}^2 = a_0 + a_1(v_2 - v_i) + a_1(v_2 - v_i)^2 \quad (5.7)$$

$$i_2 = a_0 + a_1 v_{gs_2} + a_1 v_{gs_1}^2 = a_0 + a_1(v_1 - v_i) + a_1(v_1 - v_i)^2 \quad (5.8)$$

For dc components,

$$i_{1,0} = i_{2,0} = a_0 + a_1 V_{GS} + a_2[V_{GS}^2 + \frac{1}{2}V_o^2 + \frac{1}{2}V_i^2] \quad (5.9)$$

where $V_{GS} = V_{12} - V_I$ is the dc bias voltage of transistors. Note that $a_2(\frac{1}{2}V_o^2 + \frac{1}{2}V_i^2)$ represents the dc current increment due to oscillation.

The fundamental frequency components in the current of M_1 and M_2 are

$$i_{1,1} = a_1 v_o \angle\pi + a_2[2V_{GS}V_o\angle\pi + V_o V_i \angle(\phi_i - \frac{\pi}{2})] \quad (5.10)$$

$$i_{2,1} = a_1 v_o + a_2[2V_{GS}V_o + V_o V_i \angle(\phi_i + \frac{\pi}{2})] \quad (5.11)$$

which can be related to the voltages using the transfer function of the resonator,

$$\begin{aligned} v_{1,1} &= i_{1,1} \cdot A_H(\omega)\angle\phi_H(\omega) \quad (5.12)\\ &= A_H V_o[a_1\angle(\phi_H + \pi) + 2a_2 V_{GS}\angle(\phi_H + \pi) + a_2 V_i \angle(\phi_H + \phi_i - \frac{\pi}{2})] \\ v_{2,1} &= i_{2,1} \cdot A_H(\omega)\angle\phi_H(\omega) \quad (5.13)\\ &= A_H V_o[a_1\angle\phi_H + 2a_2 V_{GS}\angle\phi_H + a_2 V_i \angle(\phi_H + \phi_i + \frac{\pi}{2})] \end{aligned}$$

where A_H and $\angle\phi_H$ are the amplitude and phase of the resonator transfer function at ω.

Compare $v_{1,1}$ to (5.3), we have

$$A_H V_o[a_1\cos(\phi_H + \pi) + 2a_2 V_{GS}\cos(\phi_H + \pi) + a_2 V_i \cos(\phi_H + \phi_i - \frac{\pi}{2})] = V_o \quad (5.14)$$

$$A_H V_o[a_1\sin(\phi_H + \pi) + 2a_2 V_{GS}\sin(\phi_H + \pi) + a_2 V_i \sin(\phi_H + \phi_i - \frac{\pi}{2})] = 0 \quad (5.15)$$

[2]It is not necessary to assume 3rd-order nonlinearity because: (1) the 3rd-order term does not generate 2nd harmonic components from (5.3)-(5.5); (2) due to the differential topology, the odd harmonic components cancel out at the tail node.

which can be simplified as

$$-(a_1 + 2a_2\Delta\ VGS)\cos\phi_H - a_2 V_i \sin(\phi_H + \phi_i) = \frac{1}{A_H} \quad (5.16)$$

$$-(a_1 + 2a_2\Delta\ VGS)\sin\phi_H + a_2 V_i \cos(\phi_H + \phi_i) = 0 \quad (5.17)$$

which can be used to find ϕ_H, ϕ_i for a given V_i.

The 2nd harmonic components of transistor currents are

$$i_{1,2} = -a_1 V_i \angle\phi_i + a_2[\frac{1}{2}V_o^2 \angle\frac{3}{2}\pi - 2V_{GS}V_i\angle\phi_i] \quad (5.18)$$

$$i_{2,2} = -a_1 V_i \angle\phi_i + a_2[\frac{1}{2}V_o^2 \angle\frac{1}{2}\pi - 2V_{GS}V_i\angle\phi_i] \quad (5.19)$$

and thus

$$i_{i,2} = i_{1,2} + i_{2,2} = -2V_i\angle\phi_i(a_1 + 2a_2V_{GS}) \quad (5.20)$$

Compare to (5.5),

$$I_i = 2V_i\angle\phi_i(a_1 + 2a_2V_{GS}) \quad (5.21)$$

$$\angle\phi_{vi} = \pi \quad (5.22)$$

Thus the injected voltage and current are 180° out of phase, which means that i_i actually flows up into the oscillator core. This verifies that the injected signal does pump energy into the oscillator core as we expect.

Now let us find the locking range. From (5.16),

$$cos(\phi_H + \phi_i) = \frac{a_1 + 2a_2V_{GS}}{a_2V_i}\sin\phi_H \quad (5.23)$$

Assuming that the frequency deviation from the self-oscillation frequency, ω_0, is small, and so is ϕ_H (recall Adler's method),

$$\sin\phi_H \approx \phi_H \approx -2Q\frac{\Delta\omega}{\omega_0} \quad (5.24)$$

and thus

$$\left|\frac{\Delta\omega}{\omega_0}\right| \leq \frac{1}{2Q}\frac{a_2V_i}{a_1 + 2a_2V_{GS}} \quad (5.25)$$

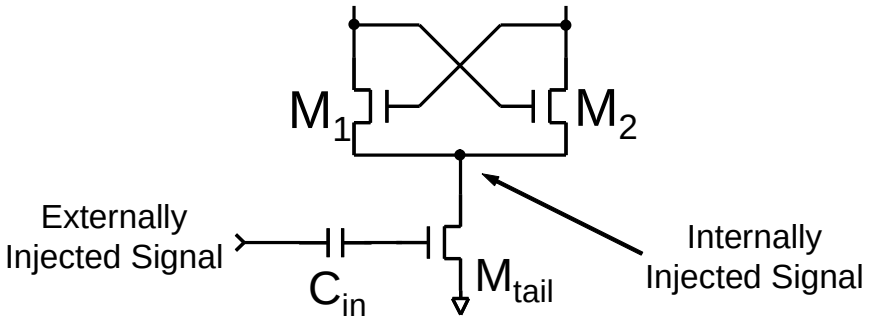


Figure 5.12: External vs. Internal Injected Signal.

or

$$\left|\frac{\Delta\omega}{\omega_0}\right| \leq \frac{1}{4Q}\frac{a_2 I_i}{(a_1 + 2a_2 V_{GS})^2} \tag{5.26}$$

Therefore, the locking range is still proportional to the input signal amplitude (V_i or I_i), and inversely proportional to the self-oscillation amplitude, which is related to V_{GS}.

Further, it is evident that we have to distinguish between the internal and external injection signals. In this implementation, the input signal is injected into the gate of M_{tail}, while the internal injection point is at the tail node. The internal injection power, i.e., the power injected into the oscillator core, determines the locking range of the ILFD. Therefore, the locking range can be enhanced by maximizing the internal injection power using the same external injection power, i.e., maximizing the power gain from the external injection point to the internal injection point. In this context, we still refer to the external injection power as injection power for simplicity since this is power provided by the previous stage and what can be measured more easily.

5.2.2 Locking-range enhancement by shunt peaking

In order to achieve a larger locking range, an ILFD can be tuned with varactors like in a VCO. Particularly, an ILFD prescalar in a frequency synthesizer can be tuned in this manner to track the oscillation frequency of the previous-stage VCO [135]. However, the tuning control signal is not always available in most applications. Even in a frequency synthesizer, it is difficult to use the same control voltage for both VCO and ILFD prescalar because they might require different dc voltage range. Therefore, it is important to increase the locking range of ILFD's without tuning or sacrificing its input sensitivity.

In this particular implementation, we notice that there is a large parasitic capacitance,

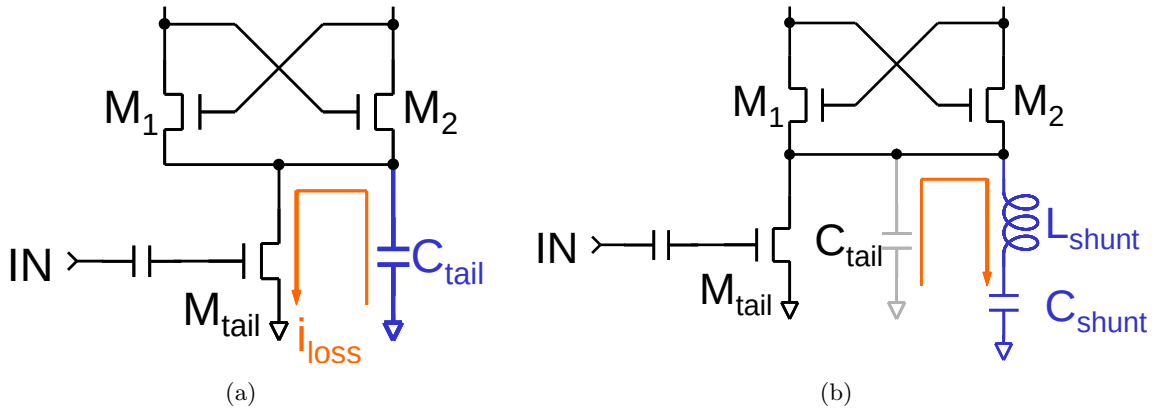


Figure 5.13: Shunt-Peaking Locking-Range Enhancement. (a) Injection energy loss on C_{tail}. (b) Shunt peaking.

C_{tail}, consisting of C_{gd} and C_{db} of M_{tail} as well as C_{sb} of M_1 and M_2, which wastes a large amount of internal injection current and thus significantly lowers the effective injection power (Fig. 5.13a).

In order to remedy the power loss on C_{tail}, a shunt inductor, L_{shunt}, is introduced to resonate with C_{tail} at the injection frequency, f_i, with a serial dc-blocking capacitor, C_{shunt} (Fig. 5.13b). Thus, the impedance at the tail node increases at f_i and so does the internal injection power. Another way to look at this effect is that M_{tail}, C_{tail}, and L_{shunt} form a tuned amplifier with output power peaking at f_i. Therefore, we refer to this technique as *shunt-peaking locking-range enhancement*.

5.2.3 Locking-range enhancement by oscillation amplitude suppression

Intuitively, the weaker the self-oscillation of an ILFD, the "easier" it is injection-locked to the input signal and thus the larger its locking range. This is evident in Adler's formula (2.35), which says that locking range is inversely proportional to the oscillation amplitude E_{osc}, which is very close to the self-oscillation amplitude. Eq. 5.26 further verifies this statement since V_{GS} is directly related to the self-oscillation amplitude.

Therefore, it is possible to expand the locking range by suppressing the self-oscillation amplitude. This can be done in several ways: 1) decrease dc bias current; 2) reduce Q of the resonator, e.g., by using smaller metal strip width for spiral inductor L_1 and L_2 while keeping the inductance the same;[3] 3) resize the transistor properly. The only limiting factor

[3]In some regenerative divider implementations, a serial resistor is added with the resonator, which may not be good because it decreases the dc voltage headroom.

would be the output amplitude specification.

5.2.4 Experimental results

Two ILFD's with input frequencies of 9GHz and 19GHz using the shunt-peaking locking-range enhancement technique have been designed and fabricated using 0.35μm CMOS transistors (Fig. 5.14). Each of them occupies an area of 0.6μm $\times$ 0.5μm, including the pads. Inductors L_1 and L_2 in Fig. 5.9 have a value of 8.5nH and L_{shunt} is 2nH in the 9GHz ILFD. Inductor L_1 and L_2 are 3nH and L_{shunt} is 1nH in the 19GHz ILFD.

The measurement setup is shown in Fig. 5.15. In order to measure the injection power correctly, a directional coupler is inserted between the signal generator and injection port, with a power meter at the coupling port to measure the injection power. Two one-port s-parameter measurements are necessary to characterize the loss from the cables, adaptors and probes between the output of the directional coupler and the ILFD input as well as to measure the reflection coefficient at the input. The measured injection power can be adjusted accordingly to obtain the actual injection power using the following calibration formula:

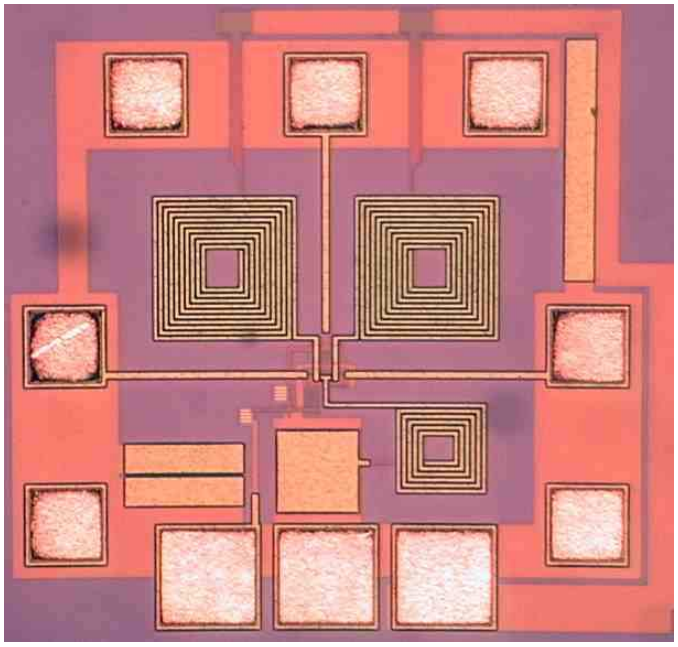
$$P_i = P_m \cdot \frac{|S_{d21}|^2}{|S_{d31}|^2} \cdot |S_{c21}|^2 \cdot (1 - |S_{i11}|^2) \tag{5.27}$$

where P_m is the power meter reading, S_{d21} and S_{d31} are S_{21} and S_{31} of directional coupler, S_{c21} is S_{21} of cables and connectors, and S_{i11} is S_{11} at the input.

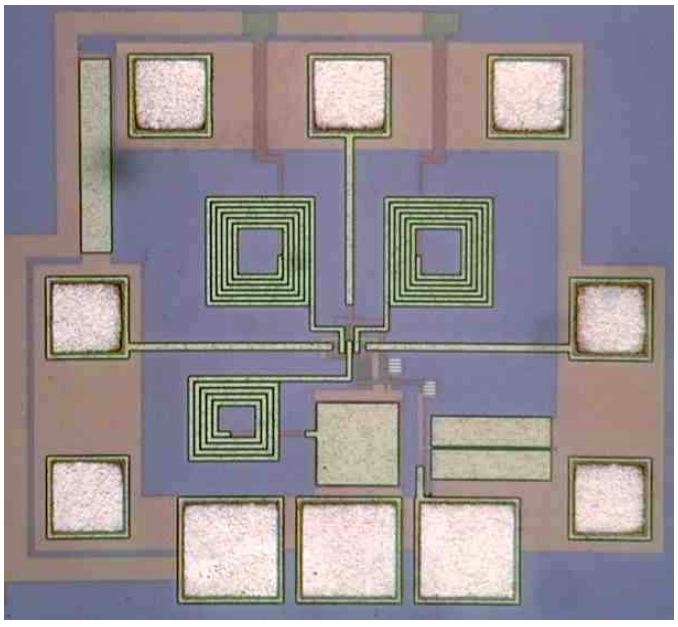
To verify the effectiveness of shunt-peaking locking-range enhancement, each ILFD is measured twice before and after disconnecting the shunt-peaking circuitry using a laser trim. The locking range and dc power consumption with and without shunt peaking are compared in Fig. 5.16 and Fig. 5.17 for the 9GHz and 19GHz ILFD's, respectively. Note that the dc level of the tail current, I_{tail}, increases with injection power due to the *clamped-biasing effect*[40].

The power supply voltage is 1.2V. The 9GHz ILFD achieves a locking range of 1490MHz (8.38-9.87GHz, 17%), with the injection power of +2dBm and tail current of 1.1mA, compared to 840MHz (8.37-9.21GHz, 9%), 2.4dBm and 1.5mA without shunt-peaking. This corresponds to 77% improvement in locking range.

The 19GHz ILFD achieves a locking range of 1350MHz (18.01-19.36GHz, 7%) with the injection power of +5dBm and tail current of 1mA. It can also operate at 0.37mA with



(a)



(b)

Figure 5.14: Chip Photos of Prototype CMOS ILFD's. (a) 9GHz; (b) 19GHz.

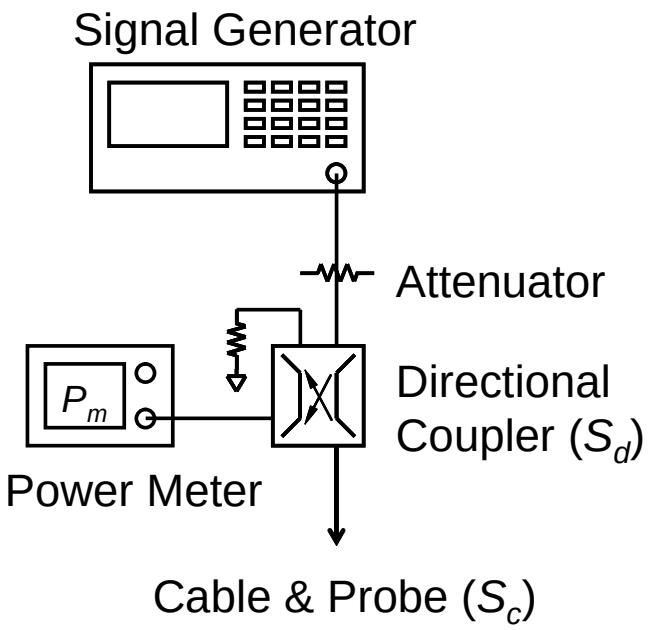
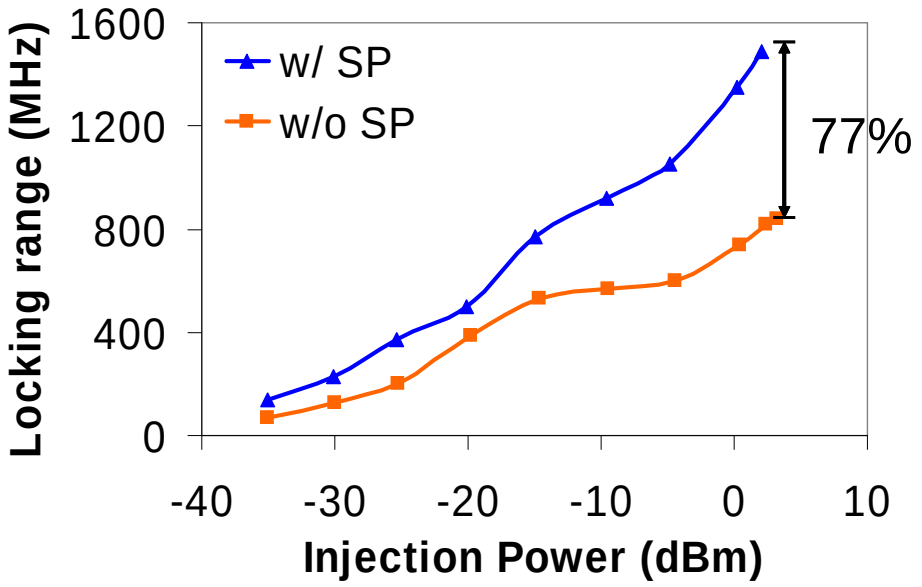


Figure 5.15: Measurement Setup.

an injection power of -10dBm to achieve a locking range of 760MHz (18.50-19.26GHz). The relative locking-range improvement is smaller than that of the 9GHz ILFD due to an inadvertent mismatch in the center frequency of the shunt-peaking network.

Fig. 5.18 demonstrates the effectiveness of the second locking-range enhancement technique, self-oscillation amplitude suppression. It shows the locking range and power consumption of the 19GHz ILFD under different dc bias conditions with a constant injection power of 0dBm. We see that when the external bias voltage decreases, which corresponds to the decrease in the dc bias current of the *free-running* oscillator, the locking range increases while the dc current decreases. It verifies that the locking range can be expanded at the price of oscillation amplitude.

Fig. 5.19 shows the phase noise performance of the free-running 19GHz ILFD, as well as the phase noise of the signal source and the locked output. It can be seen that the divided output is not affected by the poor phase noise of the free-running oscillator and follows the phase noise of the injected signal with a 6dB offset until it reaches the noise floor of the spectrum analyzer at frequency offset above 100KHz. This verifies that ILFD's can have superior noise performance than digital dividers, as we discussed in Section 5.1.3.



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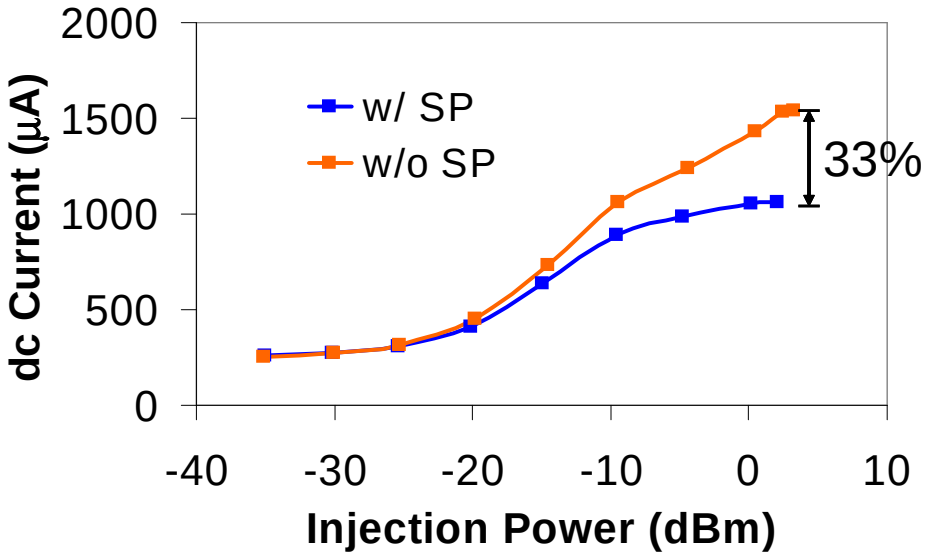

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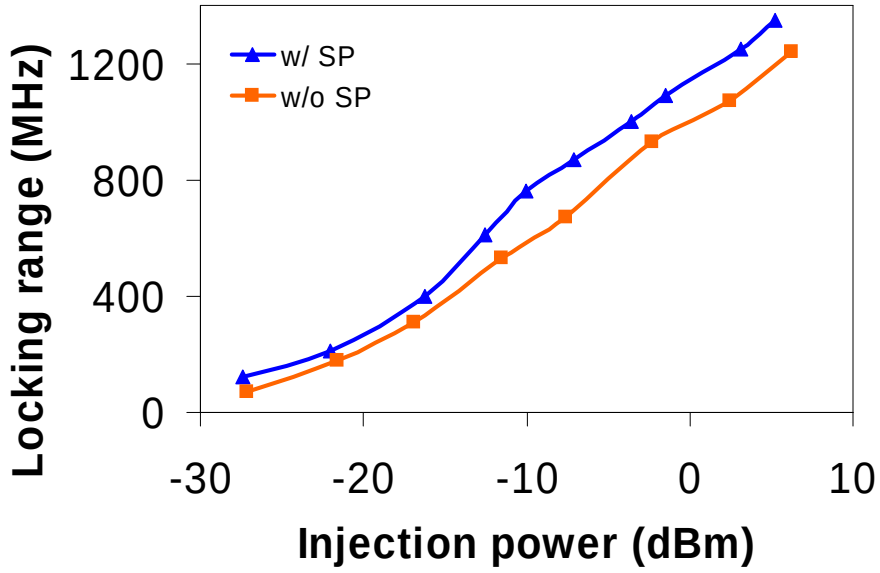
Figure 5.16: Performance of 9GHz ILFD. (a) Locking range; (b) Power consumption.



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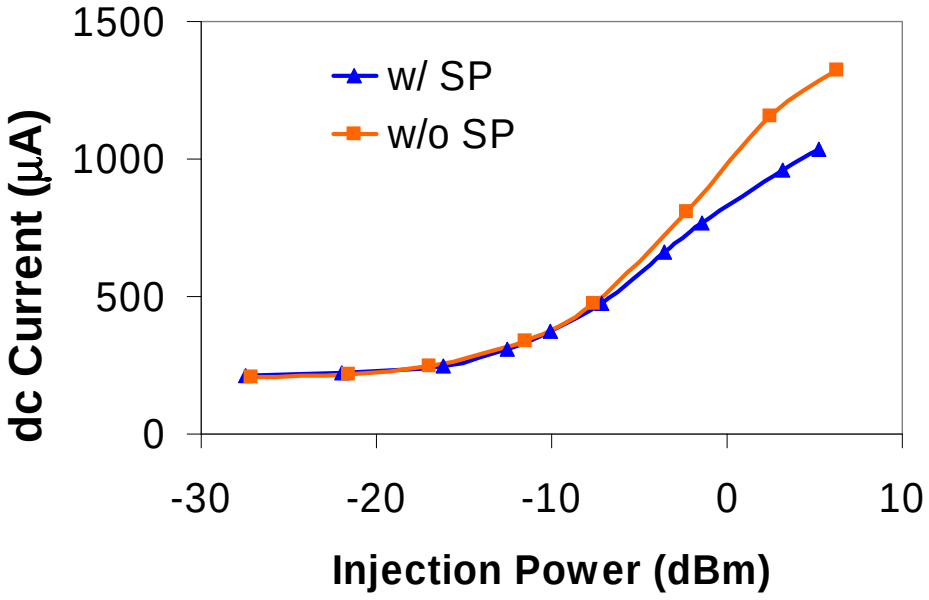


(b)

Figure 5.17: Performance of 19GHz ILFD. (a) Locking range; (b) Power consumption.

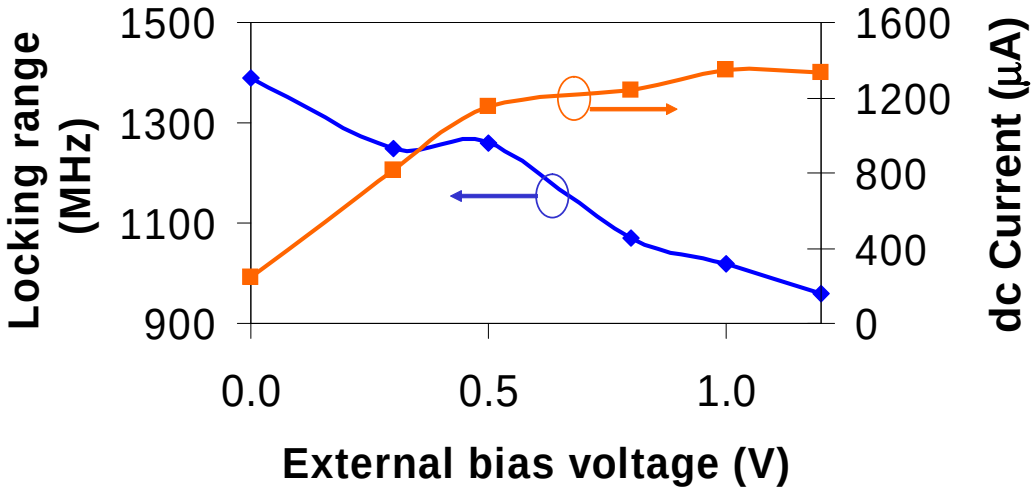


Figure 5.18: Self-oscillation amplitude suppression.

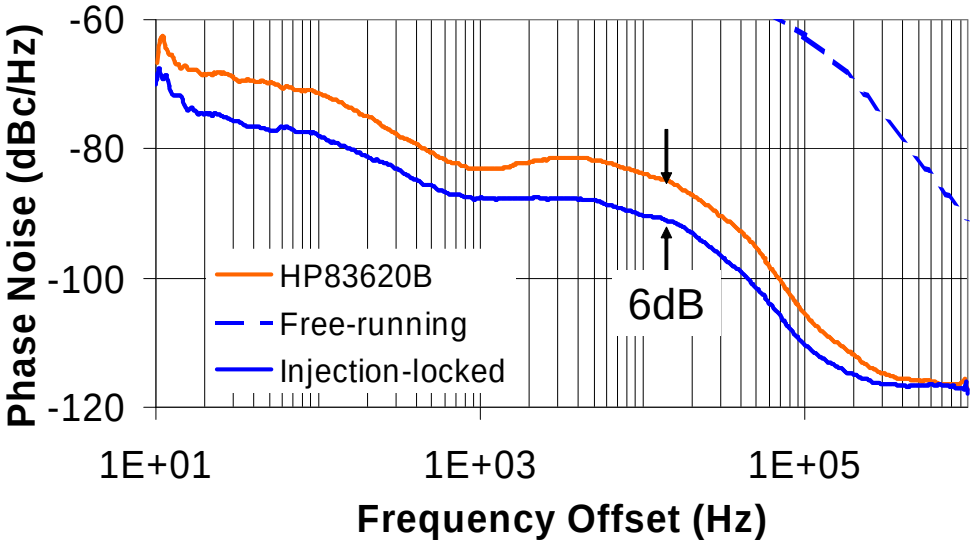


Figure 5.19: Phase noise of 19GHz ILFD.

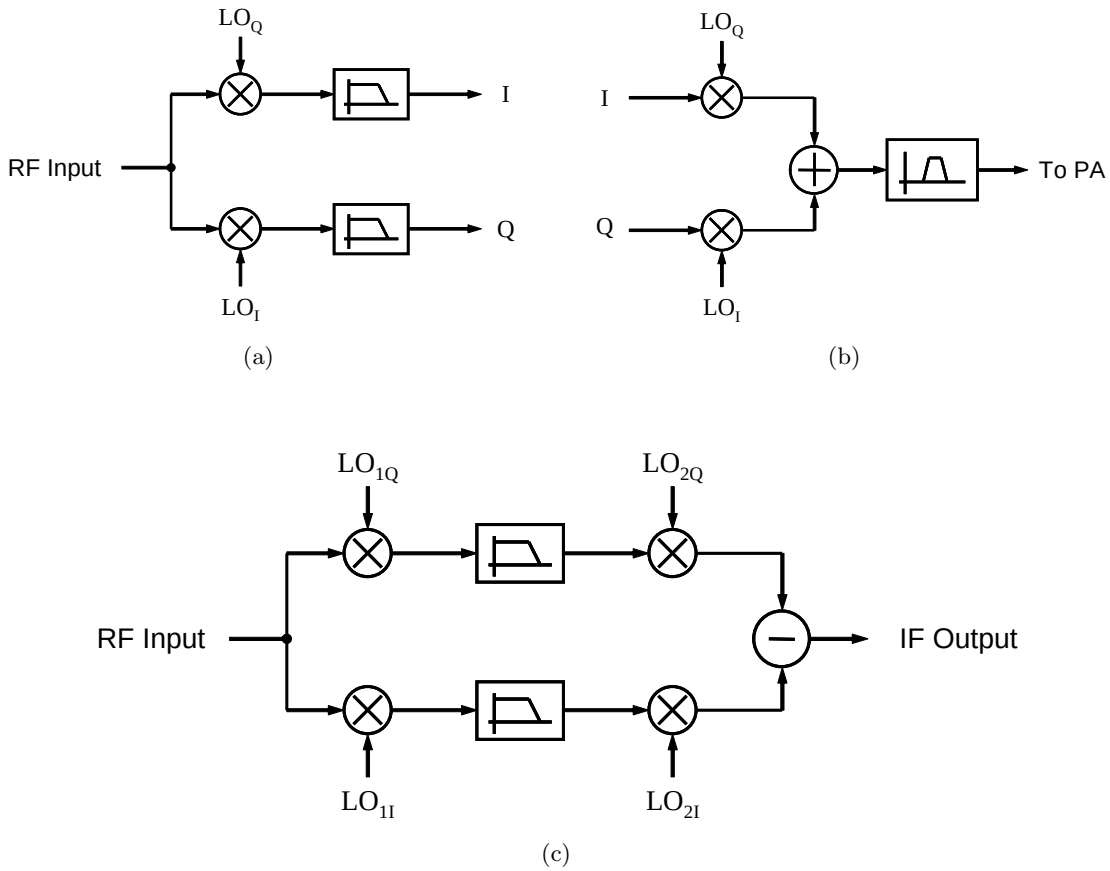


Figure 5.20: Quadrature signal applications. (a) I/Q component separation; (b) Direct-conversion transmitter; (c) Image rejection in Weaver architecture.

5.3 Quadrature Signal Generation with ILFD's

Beside phase noise, another important issue of high-frequency signal generation is how to generate signals with a phase difference of 90°, i.e., *quadrature signal generation*. Quadrature LO signals are required in many modern receivers and transmitters to accomplish several critical functions:

- Demodulate and separate in-phase and quadrature components of the signal in receivers using digital modulation schemes (Fig. 5.20a). If only a single LO signal is used, the information in the phase will be lost due to the overlap of both sidebands.

- In a commonly-used direct-conversion transmitter, the baseband I and Q data are modulated and up-converted by a quadrature LO, and then combined into the RF signal for transmission (Fig. 5.20b).

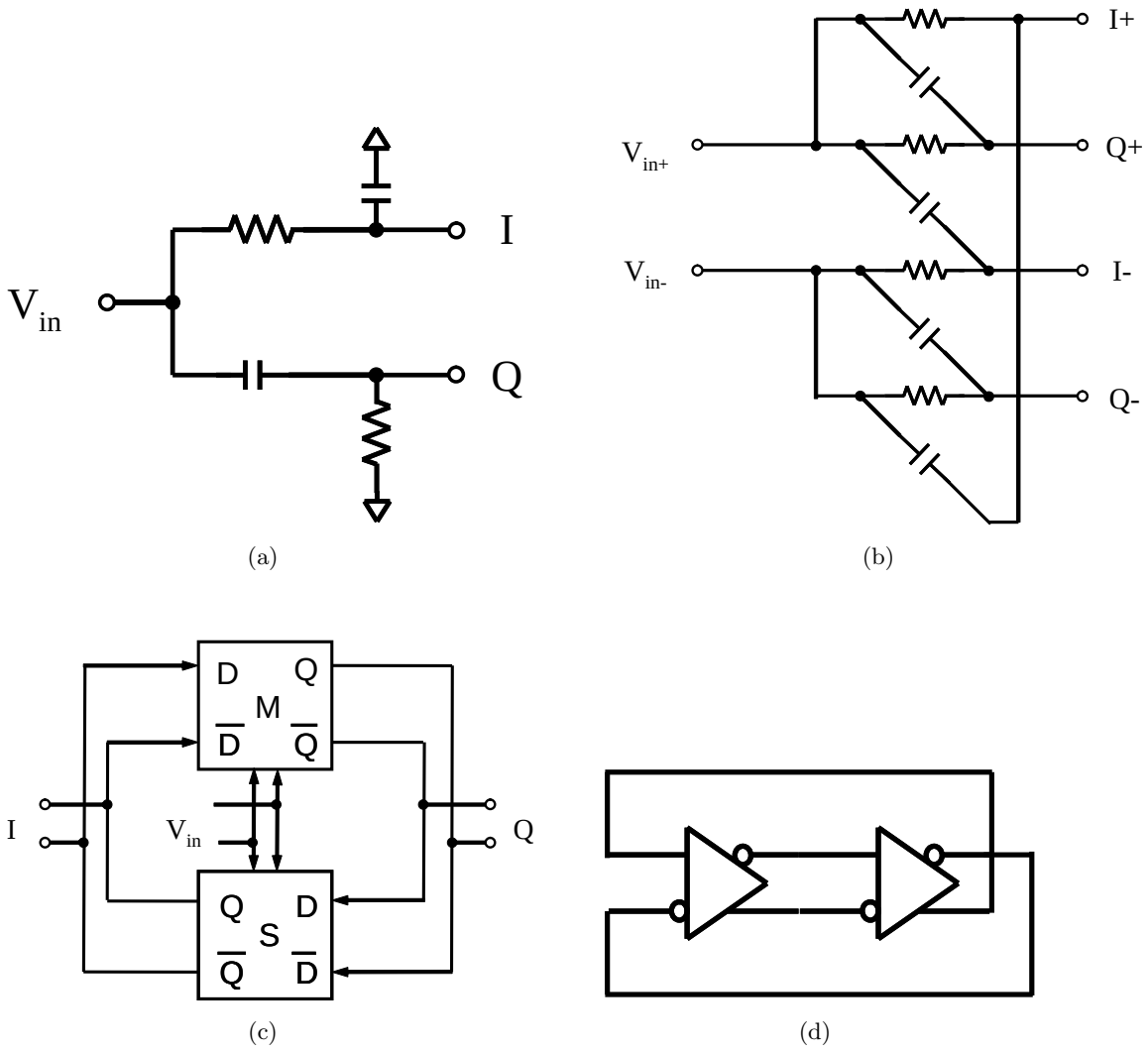


Figure 5.21: Conventional quadrature signal generation. (a) RC-CR network; (b) Polyphase filter; (c) Digital divider; (4) Ring oscillator.

- Quadrature signals are required in image-rejection receivers such as in Weaver architecture (Fig. 5.20c) to improve image rejection.

In RF and microwave frequencies, there are several conventional methods for quadrature signal generation:

- RC-CR networks (Fig. 5.21a). The phase of the input signal is shifted by $\pm 45^\circ$ using the upper and lower RC networks. There are several problems with this simple approach: (1) the output amplitudes from two paths are not equal except at $\omega = 1/(RC)$, and thus can only be used in narrow-band applications, unless limiting stages are added, which are difficult to implement at high frequencies and can introduce

extra phase and amplitude mismatch between the I and Q outputs; (2) it has 3dB signal attenuation at $\omega = 1/(RC)$, and is quite noisy; (3) it cannot handle harmonic components of input signal because the phase shift is 90° for all frequencies, and thus the fundamental and harmonic components are not synchronized [45].

- Poly-phase filters [138][139] are symmetric RC networks with inputs and outputs symmetrically disposed in relative phases (Fig. 5.21b). If any single-tone inputs with arbitrary phase and amplitude relations are decomposed into four balanced sequences [138], a poly-phase filter can only pass the counterclockwise sequence, which has four quadrature phases. In practical implementations, it is usually driven by a differential LO input. However, this sequence selection is only effective around the RC pole frequency ($\omega = 1/(RC)$), and the bandwidth is about 10% of the center frequency [65]. More polyphase stages have to be added for larger bandwidth. Consequently, polyphase filters are quite lossy and noisy, and thus unsuitable for demanding high-frequency applications.

- Frequency division with digital dividers naturally generates quadrature outputs. In a divide-by-2 architecture (Fig. 5.21c), it is sensitive to both rising and falling edges of the input signal and thus requires that the input signal has a 50% duty-cycle. In order to remedy this problem, a divide-by-4 configuration can be used. However, signal generation and division at $2f_0$ or even at $4f_0$ consume substantial power, or can simply be impossible for high-frequency applications.

- Ring oscillators with 2 or 4 stages (Fig. 3.1) can be used to generate accurate quadrature signals. However, they fundamentally have inferior phase noise performance than resonator-based oscillators, especially at high frequencies (see Section 3.1), and thus are unsuitable for most modern digital communication systems.

Therefore, new methods for quadrature signal generation are highly needed and enthusiastically pursued. Among the new techniques, coupled LC[4] oscillators recently receive much attention [142][143][144]. A coupled LC oscillator (Fig. 5.22d) consists of two identical LC oscillators, and coupling are introduced by transconductance of coupling transistors, which force the two oscillators to oscillates in quadrature phases. In each of these oscillators, the

[4]Coupled relaxation oscillators like [140] were also reported, but they are not suitable for high frequency use because of their speed limit and large phase noise [141].

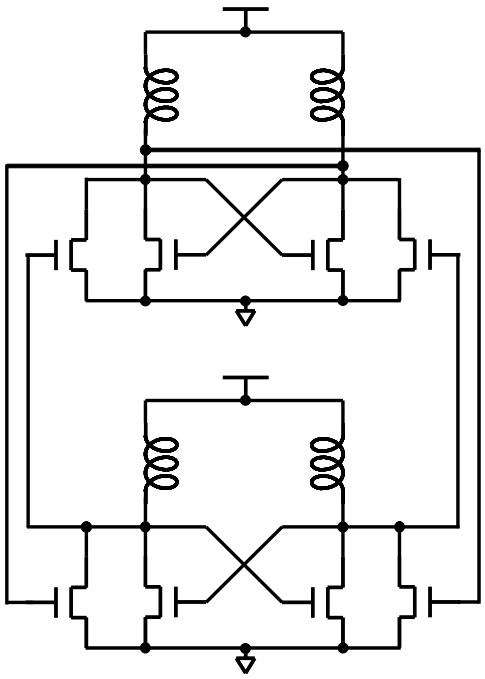


Figure 5.22: Coupled Oscillator

current from the cross-coupled transistors are in quadrature with that from the coupled transistor, and thus the total current through the resonator is not in phase with the voltage across the resonator. This phase shift must be compensated by some extra phase shift from the resonator itself. Since the resonator has the largest Q at zero phase shift, which is already small for LC tank using on-chip inductors, a coupled oscillator has inferior phase noise than its individual LC oscillator with twice the power consumption, resulting in a direct tradeoff between phase noise performance and quadrature signal generation [145].

Recently there are efforts to reducing this extra phase shift, e.g., by using more coupling stages to form a ring structure [146], which effectively decreases the phase shift in each stage, or by introducing extra phase-shift circuits between two oscillators [147]. However, they create their own problems: the coupled ring approach increases power consumption by several times, which renders it almost unacceptable in most applications; in the phase-shift circuit approach, it is very difficult to control the absolute value of phase shift, and thus the circuit can be an easy victim of any uncertainties such as process and temperature variations.

As we discussed in Chapter 3, DVCO's are a good candidate for high-frequency low-noise quadrature signal generation. Their quadrature accuracy is guaranteed by the distributed

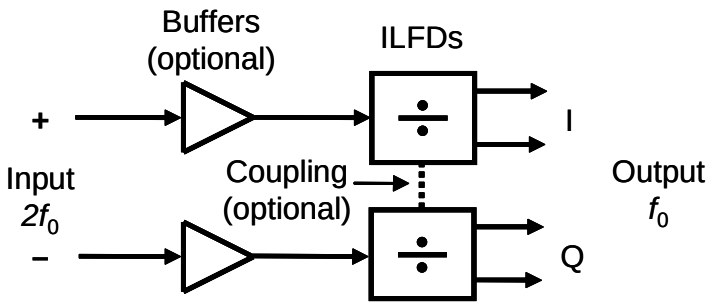


Figure 5.23: Quadrature generation using ILFD's.

structure itself, and their phase noise performance is comparable to LC oscillators. The only limitation might be the physical size and associated cost in some not-so-high-frequency applications.

The other promising alternative is quadrature generation using ILFD's. This can be easily done by driving two identical ILFD's with a pair of differential signals like using digital dividers, as shown in Fig. 5.23. Because there is a pre-determined phase relation between the input signal of an ILFD and its subharmonic out signals, such an *ILFD quadrature generator* can have very good quadrature accuracy. Further, the excellent phase noise performance of ILFD's does not suffer since the injection locking approach uses the same nonlinear effect that maintains the oscillation instead of the "brute force" coupling. Additionally, this approach has the benefits of ILFD's compared to the common digital divider configuration, i.e., higher speed and lower power dissipation.

5.4 Self-Dividing Oscillators

5.4.1 Observations

From the study of ILFD's, we have the following observations:

- The fundamental frequency and its harmonics usually co-exist in the oscillator. For example, in the LC oscillator of Fig. 5.9, the tail node oscillates at the second harmonic due to the differential topology. The relative amplitudes of these harmonics are determined by the circuit topology, Q of the resonator, and circuit nonlinearity.

- The fundamental and harmonic frequencies are injection-locked to each other, and therefore their phase noise should follow the $-20\log N$ relation, where N is the har-

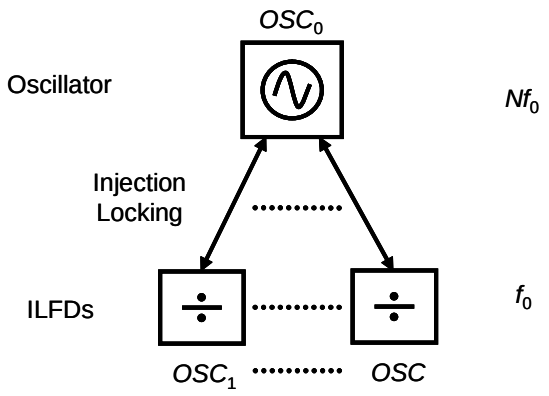


Figure 5.24: Self-Dividing Oscillator.

monic number of a particular frequency. If these inherent harmonic frequencies can be amplified without changing the loading on the oscillator too much while minimizing phase noise degradation from amplification, we can achieve comparable low-phase-noise signal generation at frequencies several times higher than the conventional LC oscillator.

- Since frequency division (by injection locking) can improve phase noise by $-20 \log N$dB, it might be advantageous to consider generating a $2f_0$ oscillation with reasonably good phase noise and then dividing it to generate the desired frequency with excellent phase noise and quadrature outputs. The challenge is how to achieve this without excessive power dissipation increase.

5.4.2 Basic Idea

Based on these observations, we developed a new type of circuit that can achieve both quadrature (in general multi-phase) signal generation and ultra-low phase noise simultaneously. It is such a circuit that combines an oscillator with a number of ILFD's ($M \geq 2$) by injection locking, as shown in Fig. 5.24. We will refer to such an oscillator and ILFD combination circuit as a *self-dividing oscillator* (SDO).

SDO's have the following characteristics, which will become clear after we discuss an exemplary implementation in the next section:

- In an SDO, the ILFD's operate at the fundamental frequency (f_0), while the oscillator has a center frequency at the harmonic frequency (Nf_0). There is a dominant fre-

quency component in each part of the circuit, and the desired frequency components can be output from the corresponding parts.

- An SDO can re-use its dc current between the oscillator and ILFD's, and thus is more power efficient than a conventional oscillator in the sense that larger percentage of dc energy is converted into ac signals. Therefore, it can potentially achieve better phase noise performance than a stand-alone oscillator.

- An SDO can generate multiple phases of the output (e.g., quadrature) at its fundamental frequency.

- When used in frequency synthesizer applications, an SDO has much less power consumption than a conventional "oscillator-buffer-divider" configuration, because both frequency components are readily available from the combo circuit.

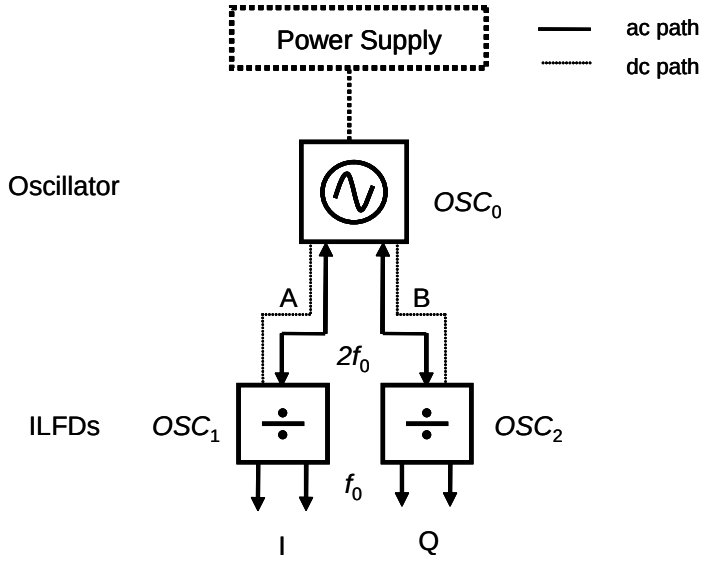
- Since an SDO takes advantage of the inherent harmonic coupling between the fundamental and harmonic frequencies, it has a larger locking range than a stand-alone ILFD.

5.4.3 Architecture

An integrated circuit implementation of SDO is shown in Fig. 5.25a and Fig. 5.25b with $M = N = 2$. In this particular configuration, the circuit consists of three oscillators, two of which (OSC_1 and OSC_2) form ILFD's. The center frequencies of free-running OSC_1 and OSC_2 are designed to be both at f_0, and $2f_0$ for OSC_0 accordingly. The oscillation frequency of OSC_0 can be tuned by V_{t1}, and so do OSC_1 and OSC_2 with V_{t2}. Also coherent tuning [135] can be used to further increase the locking range. We will refer to this topology as "∇"

OSC_1 and OSC_2 are injection-locked to OSC_0 at nodes A and B through current coupling. The bypass capacitor C_r provides the return path for the injected ac signal. The cascode topology enables dc current re-use, i.e., the dc current of OSC_0 is re-used for OSC_1 and OSC_2. For a given power supply voltage, this leads to lower dc power consumption.

OSC_0 has differential outputs at nodes A and B, and so do OSC_1 and OSC_2, which are in quadrature phases. All the outputs are buffered, which is not shown in Fig. 5.25. As we discussed before, the SDO can be used to generate low-phase-noise LO signals at



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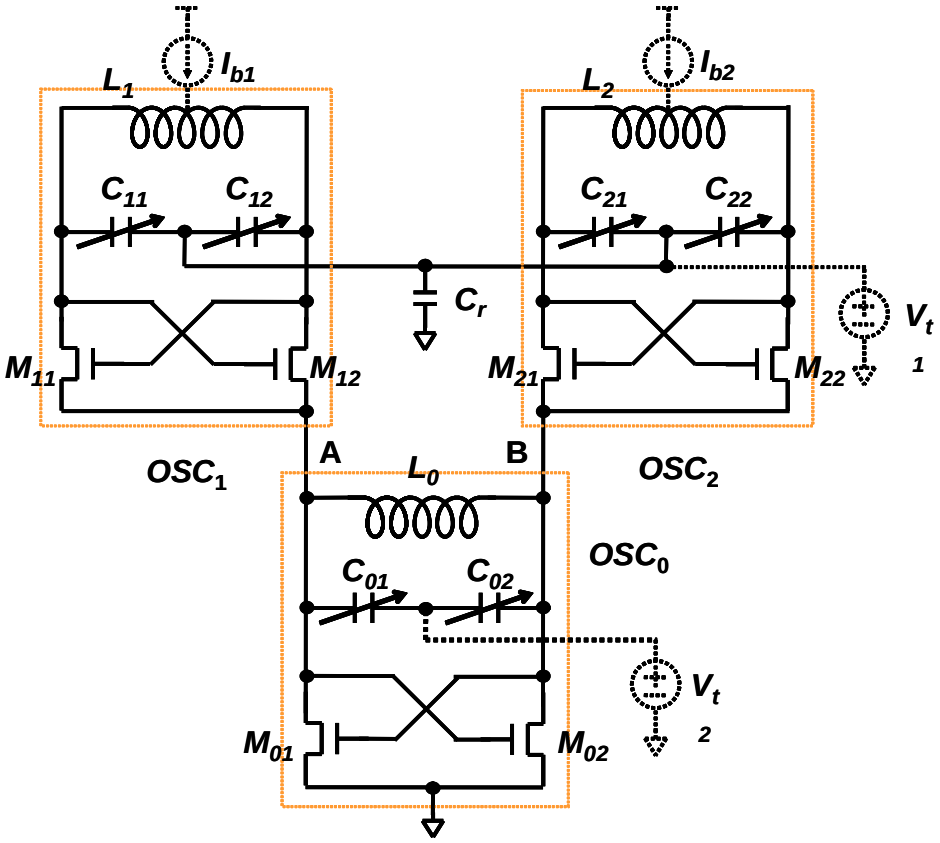

(b)

Figure 5.25: SDO implementation. (a) Block diagram; (b) Schematic.

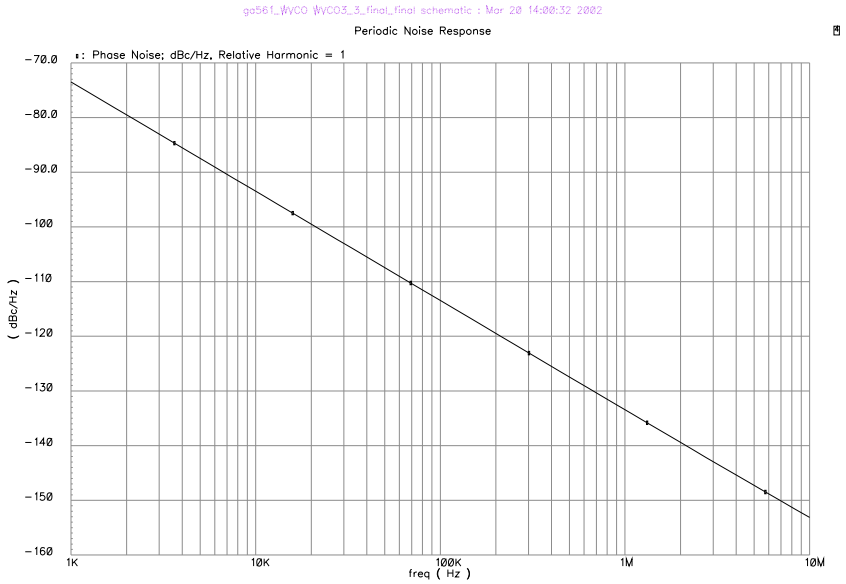

Figure 5.26: SDO Phase Noise (simulated).

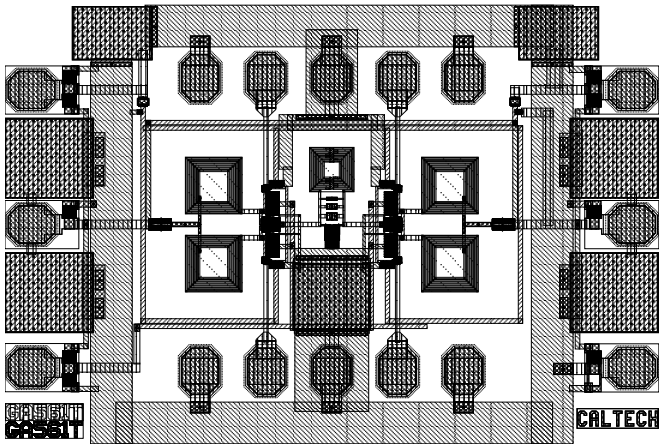

Figure 5.27: Self-Dividing Oscillator.

$2f_0$, or ultra-low-phase-noise quadrature signals at f_0, or both (which is particular useful in frequency synthesis).

Because of the nature of injection locking and higher power efficiency, SDO's can achieve substantial improvement in phase noise compared to conventional LC oscillators. This has been verified in simulation for several prototypes we designed using different process technologies. The phase noise at the differential nodes A and B ($2f_0$) is shown in Fig. 5.26 as an example. The circuit was implemented in a 0.35μm BiCMOS technology using only CMOS transistors. It was designed to generated quadrature LO signals at 2.4GHz ($f_0 = 2.4GHz$) with output buffering. Considering the 6dB improvement after the division, the

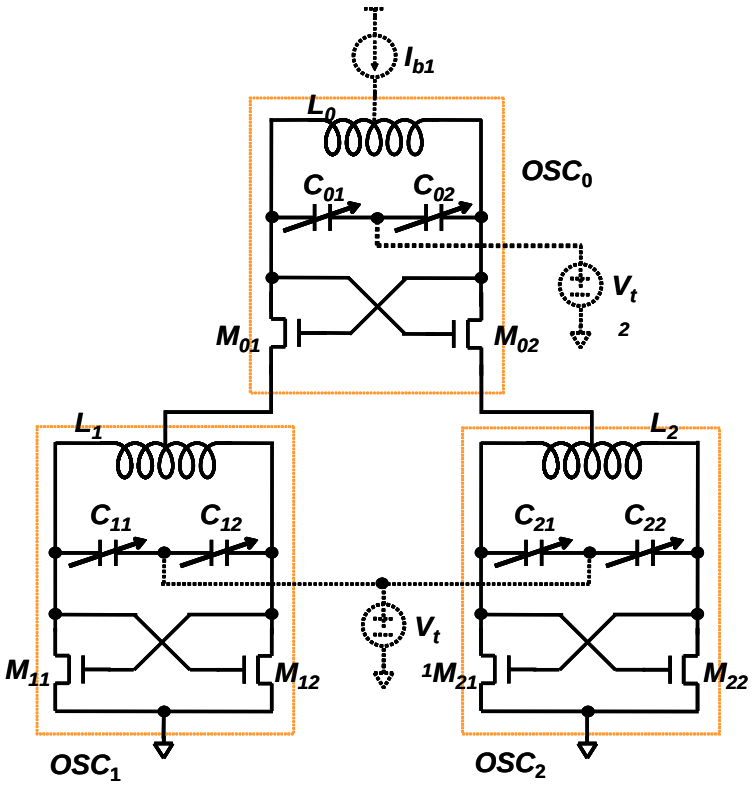

Figure 5.28: Δ topology.

phase noise at the quadrature outputs is -140dBc/Hz at 1MHz frequency offset (simulated). The chip layout is shown in Fig. 5.27.

5.4.4 Variations

There can also be many more variations for SDO's:

- Δ topology (Fig. 5.28). The signals are injected directly into the resonator of the ILFD's (OSC_1 and OSC_2) and indirectly into that of the oscillator (OSC_0), while the ∇ topology above does the opposite. In this manner, OSC_0, which oscillates at $2f_0$ and usually limits the overall phase noise performance of SDO, can achieve better *stand-alone* phase noise, because: 1) there is no direct loading of its resonator, and thus the resonator Q does not degrade; 2) it can have larger oscillation amplitude because of larger dc headroom. Therefore, this topology might leads to better overall phase noise for the SDO.

- Multi-tier cascode structure (Fig. 5.29). We can further expand the *injection-locked*

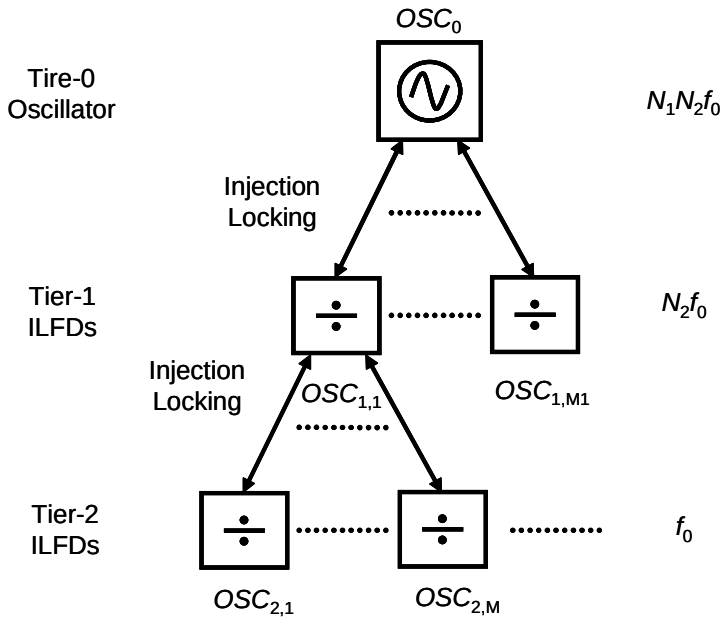

Figure 5.29: Multi-tier cascode SDO.

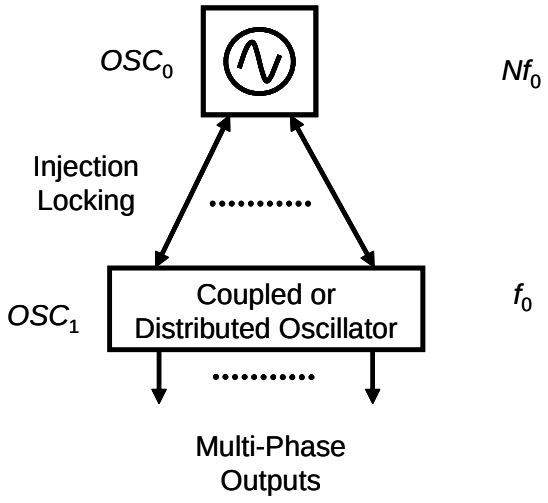

Figure 5.30: SDDO.

cascode structure into multiple layers. In this manner, multi-harmonic, multi-phase outputs can be generated, which might be useful in MUX/DEMUX or phase array systems. The only limiting factor is the power supply voltage.

- A distributed oscillator can be used as ILFD's in a SDO to generate multi-phase outputs, namely, *self-dividing distributed oscillator* (SDDO)(Fig. 5.30). The exact phase relation between outputs in a distributed oscillator can be maintained, while injection locking can further improve its phase noise performance.

Some of these options can be investigated in the future work.

5.5 Summary

In this chapter, injection-locked frequency dividers are presented as the alternative solution for high-speed dividers, which have lower power consumption and better noise performance than conventional digital dividers. Based on locking-range analysis, two prototype CMOS divide-by-2 ILFD's (9 GHz and 19 GHz) with shunt-peaking locking-range enhancement have been demonstrated with experimental results. Quadrature signal generation were discussed, and further developed into self-dividing oscillators with low-phase-noise and quadrature outputs.

Chapter 6

Conclusion

This dissertation presents our studies in high-frequency/high-speed silicon-based integrated circuits. We have demonstrated that silicon technologies, despite their limitations in fundamental physical properties and device characteristics, are capable of implementing high-frequency/high-speed integrated circuits, especially in SoC applications. In order to achieve such potential capabilities, we need to find new circuit techniques to overcome the physical limitations of silicon technologies, in other words, push silicon technologies to their limit.

Distributed circuit and injection locking are among these enabling circuit techniques which we have investigated. The distributed circuit technique is a versatile linear circuit technique. It can increase the bandwidth of high-frequency circuits for a given technology, and thus enables such circuits to operate at frequencies close to and possibly beyond f_{max}. It is also an effective power combining scheme at high frequencies, and thus can be used in high-frequency power amplifiers and oscillators. In addition, a distributed passive network can generate accurate, controllable time delays for high-frequency/high-speed signals.

In Chapter 3, the distributed circuit technique is applied in high-frequency oscillators, resulting in a new type of VCO's, namely, distributed VCO's (DVCO). Based on the analysis of distributed oscillators, which leads to general oscillation frequency and amplitude conditions, two novel tuning techniques (inherent varactor tuning and current-steering delay-balanced tuning) were developed. A 10-GHz CMOS and 12-GHz bipolar DVCO prototypes implemented in a commercial $0.35\mu m$ BiCMOS process successfully demonstrated the high-frequency capabilities of DVCO's and the effectiveness of the new tuning techniques. Further improvements in the phase noise and power consumption performance DVCO are also studied with the proposed new DVCO architectures.

In Chapter 4, the distributed circuit technique is applied in high-speed equalization,

which has become a bottleneck in fiber-optic systems. Unlike conventional optical and electrical dispersion compensation techniques, integrated transversal equalizers using distributed circuit techniques presents a more effective solution in terms of both cost and power consumption. Two 10-Gb/s distributed transversal equalizer prototypes implemented in a commercial $0.18\mu m$ SiGe BiCMOS process successfully demonstrated the potential of distributed circuit technique in high-speed fiber-optic systems and other applications.

The injection locking technique is based on the intriguing nonlinear phenomenon, and is useful in amplification, oscillation, frequency division/multiplication, and other applications. Thanks to its resonant circuit nature, it can achieve very high power efficiency, especially at high frequencies and high-speed.

In Chapter 5, the injection locking technique is applied in high-speed frequency dividers. Facing the dilemma between high speed and low power, injection-locked frequency dividers (ILFD's) present a better solution than conventional digital dividers, while introducing new challenge in their narrow locking range. Based on analysis, new locking-range enhancement techniques are then invented to solve the new problem, and demonstrated in two CMOS prototypes. It has also been showed that injection locking can also be used in low-power accurate quadrature signal generation, which is further expanded into a new type of oscillators (self-dividing oscillators).

Therefore, distributed circuit and injection locking techniques have become the main themes in this work, with applications in signal generation (oscillators and frequency dividers) and signal processing (equalizers). It should be emphasized that the real strength of these techniques lies in better understanding of the fundamental physical possibilities and limitations in technologies, circuits, and systems. Equipped with such knowledge, the door to future innovations would be wide-open in our never-ending quest for higher frequencies and speed.

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