

# **Distributed Active Transformer for Integrated Power Amplification**

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# Abstract

A novel on-chip impedance transformation and power-combining technique, the *distributed active transformer* (DAT) is introduced. It overcomes the fundamental difficulties presented by silicon technology in the design of integrated rf power amplifiers. This technique efficiently combines several low-voltage push-pull amplifiers and simultaneously performs an impedance transformation to produce a larger output power while maintaining a  $50\ \Omega$  match. It also uses virtual ac grounds and magnetic couplings extensively to eliminate the need for any off-chip component, such as tuned bonding wires or external inductors. Furthermore, it desensitizes the operation of the amplifier to the inductance of bonding wires making the design more repeatable.

In this work, the performance of the introduced DAT structure is compared to that of conventional on-chip impedance transformation methods. Their fundamental power-efficiency limitations in the design of high-power fully-integrated amplifiers in standard silicon process technologies are analyzed and the DAT is demonstrated to be more efficient. Furthermore, different classes of power amplification operations and their use in DAT power amplifiers are studied.

To demonstrate the feasibility of this concept several silicon integrated power amplifiers have been fabricated and measured including a 2.4-GHz, 2-W, 2-V truly fully-integrated power amplifier with  $50\ \Omega$  on-chip input and output matching using  $0.35\ \mu\text{m}$  CMOS transistors. It achieves a power added efficiency (PAE) of 41% at this power level, demonstrating for the first time a truly fully-integrated watt-level GHz range CMOS power amplifier. It can also produce 450mW using a 1 V supply. A two stage DAT prototype, also at 2.4GHz using the same technology, operates with higher gain and lower supply voltage achieving 1-W output power, 30% PAE, and 14-dB gain with 1.15-V supply.

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## Chapter 7: Conclusion

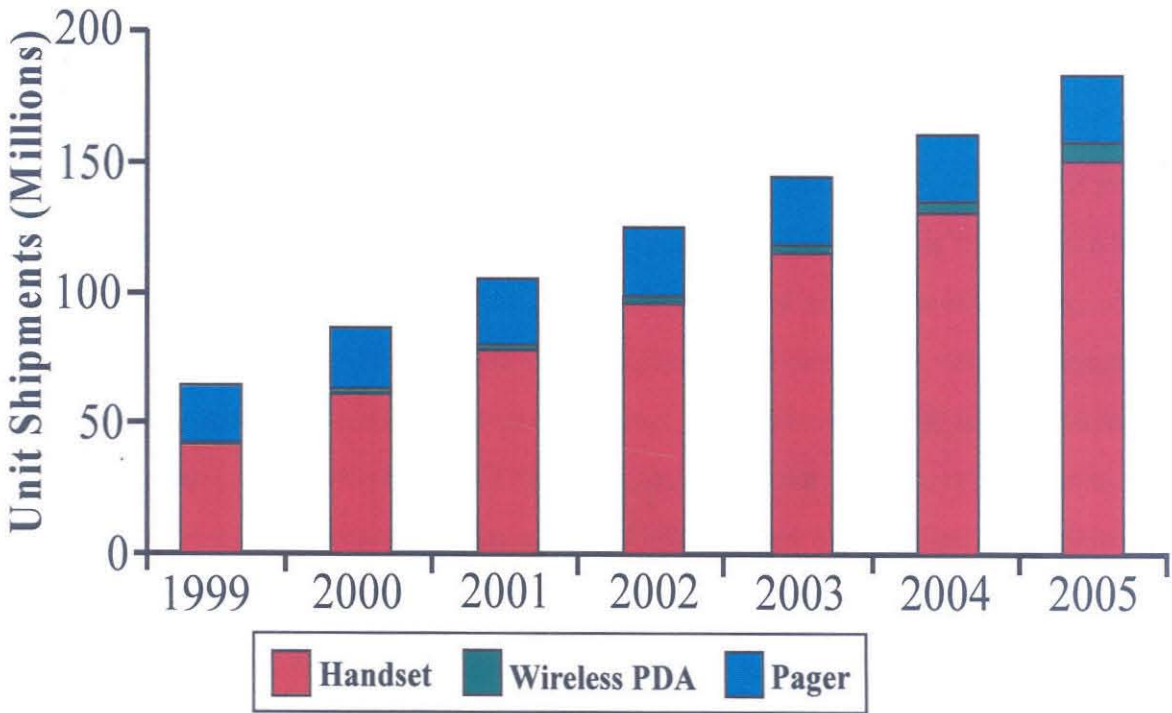
**Chapter*****1******Introduction***

As the demand and use of communication and data processing of our society increases in an exponential fashion similar to the well known Moore's law<sup>1</sup>, the communication market in general and the mobile wireless industry in particular has experienced a rapid growth since the introduction of the first analog cellular phone in 1970s.

From the simple first generation analog phones, which handled only voice, mobile phones rapidly evolved to the second generation (2G) with digitally transmitted voice introduced in 1990s, such as Code Division Multiple Access (CDMA), Global System for Mobile Communications (GSM), and Time Division Multiple Access (TDMA). This market is currently transitioning to the third generation (3G) broadband phones intended to transmit data at high bit-rate in addition to speech and includes standards such as Wideband-CDMA (W-CDMA), CDMA2000, etc. On the other hand, applications related mainly to wireless Local Area Network (LAN), such as wireless personal digital assistants (PDAs), wireless laptops, Bluetooth, IEEE 802.11, HomeRF, etc., have also been driving the growth of the mobile wireless market. It is predicted [1] that the past impressive rate of growth in this market should continue for the foreseeable future. The number of wireless access terminals are expected to exceed 180 million by the year 2005 in the United States (US) alone. Figure 1.1 shows the present data and future projections for the US mobile wireless communication market size per type of product [1].

---

1. Moore's law predicts that the processing capacity of microprocessors doubles each 18 months.



**Figure 1.1:** Unit shipment of U.S. mobile wireless communications terminals.

## 1.1 Motivation

The mobile wireless products inherently operate on batteries having limited charge and need to be compact and cost effective while providing a high performance. Most of the power dissipation in mobile wireless products is due to their transmitters, more specifically, the power amplifier. This naturally leads to the conclusion that increasing the power efficiency while reducing the size and the cost of the rf power amplifier in particular and the transceiver in general while keeping other specifications within the standard is a key factor to the evolution of overall performance of the wireless mobile products.

Perhaps the most effective way to simultaneously achieve compactness and reduce cost is a high level of integration. Eliminating hybrid technologies in a large scale production brings higher repeatability, reliability, and productivity leading to a cost reduction. Integration of multiple circuit blocks into a single chip would reduce the size of



the final product, the number of packages, packaging and testing cost, and printed circuit board footprint. The widespread quest for a *single-chip radio* shows the potential significance of integrating the entire transceiver into a single chip.

Although massive integration is clearly advantageous, hybrid solutions are still in use today in most mobile wireless transceivers. The primary reason for this trend is the high output power and power efficiency required for the power amplifier specifications, which are extremely difficult to be achieved using silicon-based circuits. In order to meet the strict performance requirement, power amplifiers are produced using III-V compound semiconductors, mostly GaAs HBTs (heterojunction bipolar transistors) in conjunction with external passive components. Due to the high cost and limited digital capability of the GaAs technology, designing a fully-integrated transceiver using this technology is not an economically and technically viable solution.

The design of a fully-integrated rf power amplifier in a silicon technology with a reasonable output power, efficiency and gain remains one of the major challenges in the pursuit of this single-chip transceiver. Although several advances have been made in this direction, a truly fully-integrated power amplifier using silicon technology at watt level output power has not been reported to this date.

Until now, the highest output powers achieved by fully-integrated CMOS power amplifiers are 85mW [2] delivered to a differential 50 $\Omega$  load with a power added efficiency (PAE) of 30% and 100mW with a drain efficiency of 16% [3]. Other works using CMOS [4],[5] or silicon Bipolar [6],[7] processes rely on the use of multiple external passive components such as bond wire inductors, off-chip transmission lines, off-chip capacitors, and/or external baluns to achieve watt level output power.

Several other works have been reported using alternative process technologies with higher transistor breakdown voltages and/or semi-insulating substrates to achieve watt-level output power, such as GaAs MMICs (monolithic microwave integrated circuits) [8],[9],[10] or SOI LDMOS with 20V breakdown voltage [11].

These results, [2]-[7], demonstrate that while silicon transistors are capable of producing watt-level output power in the GHz frequency range with reasonable efficiency, the on-chip passive devices are the major limiting factor in the performance of the amplifier and therefore deserve special attention. These passive devices, especially the on-chip inductors, are unavoidable due to the impedance transformation required to achieve high power with low-breakdown silicon transistors.

Two major problems associated with the design of on-chip power amplifiers using sub-micron CMOS processes are low transistor breakdown voltage [12] and high energy loss of on-chip impedance transformation [13]. The latter is caused by the highly conductive substrate, as well as thin metal and dielectric layers used in on-chip inductors. rf signals in an on-chip inductor induce currents inside the conductive substrate through capacitive and magnetic couplings resulting in power loss. Additionally, narrow metal lines used in on-chip inductors present a significant resistance, further dissipating rf power. These problems become more serious as the minimum feature sizes are scaled down in each new process generation [14] reducing the transistor breakdown voltage even further so that larger impedance transformation is required.

This work investigates the design of rf power amplifiers with emphasis on achieving higher integration using silicon technology while keeping high output power and power efficiency. The *Distributed Active-Transformer* (DAT) is presented as a new method to achieve simultaneous impedance transformation and power combining that can be used to overcome the abovementioned problems [17],[19],[20]. This new method relies on extensive use of symmetric push-pull amplifiers, ac virtual grounds, and magnetic coupling for series power combining. The DAT also provides means to allow the power amplifier to operate in a switching mode allowing an higher power efficiency. Using this new technique, power amplifiers using conventional CMOS technologies are designed achieving an order of magnitude higher power than previously reported results.

An experimental 2.4-GHz, 2-W power amplifier has been fabricated using the DAT technique for the first time and demonstrates the feasibility of this concept. Its input and output are matched to  $50\Omega$  and 0.35- $\mu\text{m}$  CMOS transistors are used. It achieves a power added efficiency (PAE) of 41 %. It can also produce 450mW using a 1 V supply. Harmonic suppression is 64dBc or better.

In order to explore the potential of the DAT, several other versions of the DAT power amplifiers at different frequencies, classes, topologies, and power levels have been fabricated and measured, including a two stage amplifier at 2.4GHz using the same technology. It operates with higher gain and lower supply voltage achieving 1 W output power, 30 % PAE, and 14dB gain with 1.15 V supply.

## 1.2 Organization

Chapter 2 describes challenges in the design of an integrated silicon power amplifier having a reasonable output power and power efficiency.

Chapter 3 presents an overview of the rf power amplifiers in general. They are divided into three fundamental building blocks, namely input network, active device, and output network. The purpose of each block and how they should be designed to achieve the desired class operation are described with a special emphasis on the newly developed family of switching amplifiers E/F [21]. This mode of operation is extensively used in the reported DAT amplifiers. A performance comparison between several classes of amplifier operation is given. Also, some common power combining methods are discussed. To illustrate some of these approaches, measured results of two fabricated designs are then presented.

Chapter 4 analyses the fundamental power efficiency limitations of the conventional networks commonly used in the power amplifier building blocks. The efficiency is a function of the quality factor,  $Q$ , of the inductors used. As the silicon on-chip planar inductors present extremely low  $Q$ s, the consequent low power efficiency of the passive

networks used to build the power amplifiers are the bottleneck in order to design of fully-integrated silicon power amplifiers achieving acceptable power and efficiency.

A fundamental performance analysis with description and purpose of each building block of the *Distributed Active Transformer* (DAT), a new harmonic control, power combining, and impedance transformation technique for power amplifiers is the subject of Chapter 5. Furthermore, the use of DAT for different classes of power amplifiers are discussed. Presentation of some techniques to further improve its performance finalizes this chapter.

Chapter 6 presents a detailed description of the first power amplifier using DAT. It is the first reported watt-level fully integrated power amplifier in silicon technology. Experimental results for this prototype fabricated in 0.35 $\mu\text{m}$  BiCMOS process are presented. Theoretical performances based on the results of Chapter 5, simulation results, and measurements are compared. Also, the simulation and measured results of several CMOS fully integrated power amplifiers using different processes and operating at different frequencies, power levels and efficiency are described.

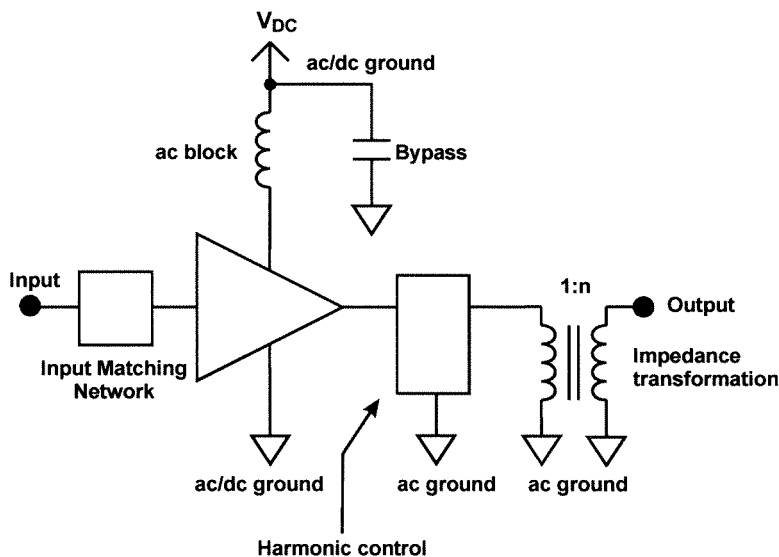
A summary of the results and suggestions for the future work are given in Chapter 7.

## Chapter

## 2

# Challenges in Integrated Power Amplifiers

Several problems arise when using sub-micron CMOS technology without any off-chip components or wire-bond inductors<sup>1</sup> for watt-level fully-integrated power amplifiers. Design issues of a power amplifier are described here to illustrate these problems. Figure 2.1 shows a simplified block diagram of a power amplifier with its key parts.



**Figure 2.1:** Block diagram of a power amplifier with critical points for integration.

In terms of frequency response, today's sub-micron CMOS and/or Si-bipolar technologies offer high-performance n-channel or npn transistors (e.g.,  $f_{max}$  and  $f_t$  of 0.15 $\mu$ m CMOS transistors reach up to 80GHz). If transistor's speed and gain were the only limitation, in principle it is possible to design switching or linear-mode amplifiers up to the 20GHz range. Unfortunately, low breakdown voltages and high knee voltages<sup>2</sup>,  $V_k$ ,

1. Wire-bond connection used as tuned inductors requires a length and height accuracy creating an extra cost and difficulty in the production process.

of the transistors limit the maximum voltage swing at their drains or collectors. This voltage swing limitation makes a large impedance transformation necessary in order to deliver any power beyond 100 mW to 50  $\Omega$  loads,  $R_L$ . This can be seen from the following calculations for a knee voltage of 0.5 V and supply voltage of 3 V:

$$P_{out} = \frac{(V_{dd} - V_k)^2}{2R_L} = \frac{(2.5\text{V})^2}{2 \cdot 50\Omega} = 63\text{mW} \quad (2.1)$$

For example, to achieve 1 W power with a 3 V supply and a  $V_k$  of 0.5 V, the maximum load resistance presented to the transistor may be calculated as follows:

$$R_{L,max} = \frac{(V_{dd} - V_k)^2}{2P_{out}} = \frac{(2.5\text{V})^2}{2 \cdot 1\text{W}} = 3.1\Omega \quad (2.2)$$

Another issue is the drain impedance control at the fundamental and harmonic frequencies taking into account the transistor parasitic capacitances. Impedance control is required to achieve the desired harmonic suppressions at the output and to improve the drain wave shaping for better power efficiency [15]. This harmonic control must incorporate an inductor in order to achieve a high-frequency selectivity and to resonate the transistor drain capacitance, as may be seen in the block diagram of the hypothetical power amplifier shown in Figure 2.1. Even in class-A operation, in order to satisfy the rigid wireless communications standards, it is necessary to have some harmonic suppression to offset the transistor non-linearity presented when the power amplifier is operating near its gain compression point.

Due to the series metal resistance and induced currents in substrate, the on-chip harmonic rejection inductor presents a very low quality factor,  $Q$ . Therefore, the loss of this component can have a significant effect on the power efficiency of a watt-level sub-micron CMOS power amplifier in multi-GHz range, typically losing 20% to 40% of

---

2. Knee voltage is defined to be the voltage below which the device ceases to operate as a transconductance. For the MOS device, it is the voltage below which the device operates in the triode region.

the power drained from the dc supply in this inductor alone. In order to minimize its loss, the impedance of this inductor should be comparable to the low impedance of the load presented to the transistor and the output impedance of the transistor.

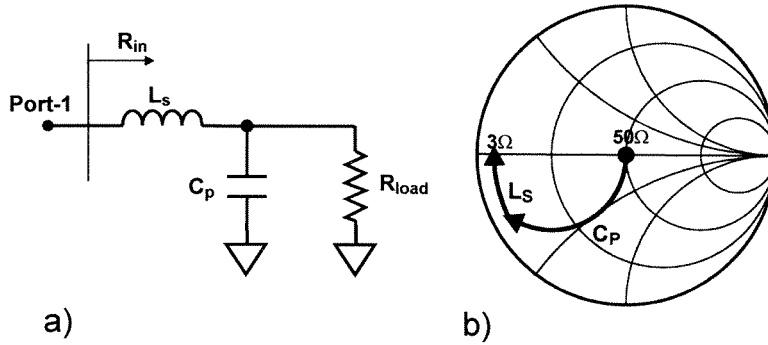
Another difficulty caused by this low-impedance inductor is its physical dimensions. For a single-ended amplifier topology, the transistor size must be large in order to have an acceptable maximum drain current and a low  $V_k$ . In this scenario, the physical size of this inductor becomes comparable to that of the transistor, making it difficult to establish a low parasitic connection between the two.

It is also necessary to provide the dc supply power to the amplifier. As shown in Figure 2.1, very low-impedance and low-loss connections are required for both ground and positive supply nodes and a high impedance inductor may be necessary to block the ac signal from the power supply. If implemented on-chip, this inductor will have a significant power loss mainly due to the metal ohmic loss. Wire-bonds may be used as a choke for the dc supply, if they do not need to be tuned. Providing a low-loss and low-impedance ac ground is also a challenge because unlike in GaAs technology, the silicon substrate is thick and does not have a backside ground plane with via access.

In order to obtain watt level output power despite the low breakdown voltage of the available devices, one can resort to impedance transformation, power combining, or a combination of both. It is necessary to present to the transistor drain or collector a low impedance, which must be matched to the  $50\ \Omega$  load. The impedance transformation could be achieved using an ideal  $1:n$  transformer. Unfortunately, an on-chip spiral  $1:n$  transformer on a standard CMOS substrate is very lossy and will degrade the performance of the amplifier significantly [13][16][17]. Another way to perform the impedance transformation is through a resonant match. A capacitor,  $C_p$ , is connected in parallel to the  $50\ \Omega$  load,  $R_{load}$ , and an inductor,  $L_s$ , in series as shown by Figure 2.2a.

This transformation can be seen graphically on the Smith Chart of Figure 2.2b. Although this method achieves lower loss than the transformer for low transformation

ratio, its loss is still significant and presents a layout problem similar to that described previously for the impedance control inductor [17].



**Figure 2.2:** a) Resonant impedance transformation network, b) Its impedance transformation shown graphically using a Smith chart.

In the input network of Figure 2.1, it is necessary to place an inductor in parallel with the gate to resonate the gate capacitance in order to match the low gate impedance to the  $50\Omega$  input. Besides the loss associated with this component and the difficulty in obtaining the necessary low-impedance low-loss ground, the input network also necessitates a low impedance dc block for gate biasing. Although easily implemented by an on-chip capacitor, the large size of this dc block is undesirable since it consumes a large die area.

This summarizes the fundamental difficulties, which have prevented the design of fully-integrated watt-level rf power amplifier before this work.



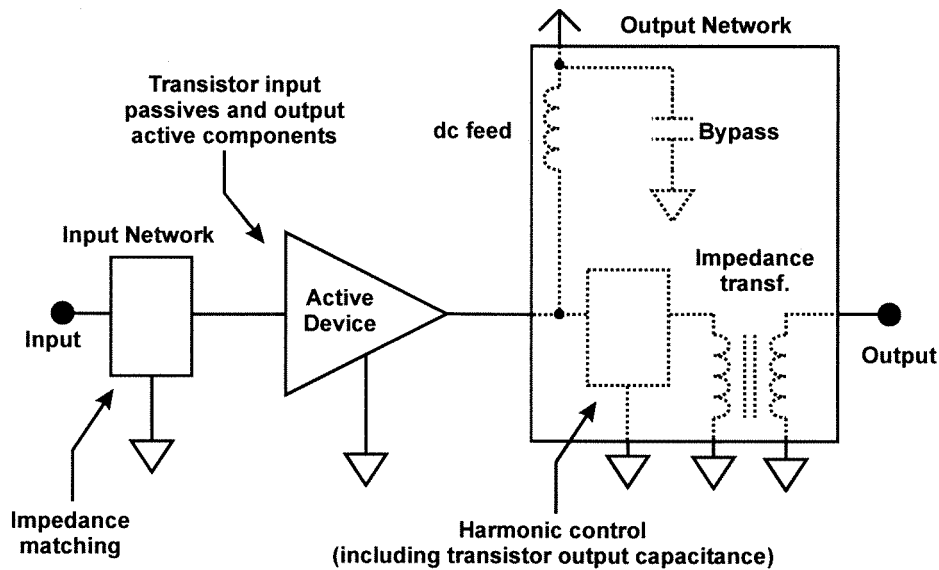
## Chapter

## 3

***Power Amplifier  
Building Blocks***

Although there are many publications regarding power amplifier designs, most of them give little or no attention to the losses caused by the passive components. They are normally focused either in active device efficiency and/or linearity and describe many different ways to operate the active device in order to achieve higher performances suitable for a desired application [12][15][22][23]. This approach is appropriate, as active devices do play a dominant role in the power losses and/or in their non-linear behavior of power amplifiers in most of the cases when these amplifiers are reactively matched. The second point which is not discussed in most of the literature is how transistor size and number can be increased to obtain a higher performance. In a discrete circuit, transistor size and quantity are dominant parameters in its cost and hence they should be minimized for a given output power to reduce the cost of the system. But in a design of power amplifiers using the very desirable integrated silicon technology as explained in the previous chapter, we have a completely different scenario. The losses caused by passive components, namely on-chip inductors or transmission lines, are as large as or even larger than the active device loss [13][16][17][24]. Also, unlike in a discrete circuit, the cost of an integrated circuit is proportional to the die area and the area is dominated by the passive components. Therefore, the effect of the size and quantity of the transistors on the cost is negligible. Hence, the IC designer can freely choose the transistor size and number within certain limits, increasing them without significant restriction in order to maximize the amplifier performance. To be able to better understand the problem under this new perspective, this chapter gives a general description of power-amplifier designs with greater emphasis on their passive networks.

In order to distinctly identify the passive network losses, we divide the power amplifier into three basic blocks, namely input network, active device, and output network



**Figure 3.1:** Fundamental building blocks of a power amplifier: input network, active device, and output network.

as can be seen in Figure 3.1. The input network includes every passive component used to match the transistor gate or base to the external input impedance. The active device comprises every internal functional blocks of the transistor except its output capacitance. Finally the output network is the set of all passive components including the transistor output capacitance, which perform harmonic control, dc feeding, and impedance matching to the output. Following the amplifier description, some power combining methods are briefly covered, as it is possible in some cases to significantly reduce the passive network losses by combining smaller amplifiers instead of using a large amplifier in order to achieve a necessary output power. Detailed discussion of impedance transformation, power combining and their associated power losses related to amplifiers using a very low  $Q$  inductors are presented in Chapter 4.

### 3.1 Input Network

The input network plays a major role in the power amplifier gain. In terms of the power efficiency, the most significant effect of the input network is indirect and through its con-

tribution to the amplifier gain, which affects the power added efficiency (PAE). The best amplifier performance, in gain and in power efficiency, is achieved when the maximum power transfer from the rf power source to the transistor gate or base is allowed by the input network, *i.e.*, when it performs a perfect power match between them by a lossless impedance transformation [23]. Any mismatch or power loss in the input network reduces the amplifier gain and consequently the power added efficiency.

### 3.1.1 Impedance Transformation

The impedance transformation to match the transistor gate or base to the available external power source is a relatively simple problem in a conventional narrow band power amplifier design, as we have to consider only the rf signal at the fundamental frequency. As we want to maximize the gain and the power efficiency, we will consider here only reactive matching circuits, avoiding lossy matching circuits which use resistors [23]. Impedance transformation networks like many other rf passive networks, can be classified into two categories, namely transmission line networks and lumped networks. The first one includes all circuits which present sizes comparable to the wavelength of the rf signal at the fundamental frequency [25][26]. If the circuit size is significantly (normally 10 to 20 times or more) smaller than the wavelength, the circuit is said to be composed of lumped elements.

Impedance matching in this case is to transform the unwanted gate or base capacitive impedance to the conjugate match of the external power source, normally  $50\ \Omega$ . It can also be matched to the impedance appropriate, normally inductive, to be connected to the drain or collector of the transistor of the previous stage. Although the non-linearity of the transistor gate or base capacitance and resistance generates harmonic signals, in many cases, these signals do not significantly affect the power gain and efficiency of the power amplifiers and, thus, are normally ignored. Hence, the power matching is accomplished only for the signal at the fundamental frequency. Some power amplifier designs take advantage of the harmonic signals generated in the gate or base to further improve the

amplifier efficiency [27][28], but these will not be covered here as they are beyond the scope of this work.

Perhaps, the simplest way to design the input network is through the use of a Smith chart [29][30]. An impedance transformation means transporting one point on the Smith chart representing the gate or base impedance located somewhere in the lower half of the chart to the center of it ( $50\Omega$  match) or to somewhere in the upper half of the chart corresponding to the desirable inductive load to be connected to the drain or collector of the previous stage.

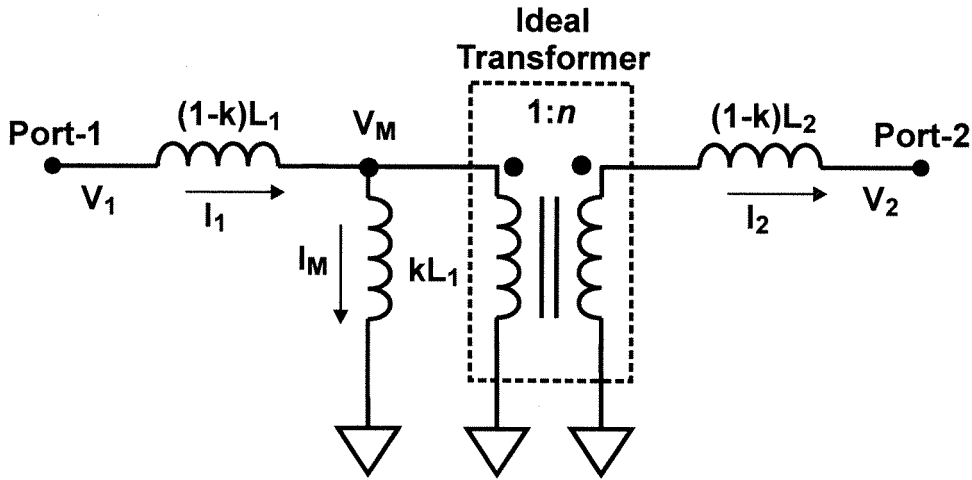
A set of simple properties of each reactive component can be used to estimate the type of components, type of connection, namely series or shunt, and what values should be used to achieve the desired impedance matching in the input network. Below we can see a list of the most common reactive passive components and their properties related to translations on the Smith chart:

Series connection:

- Transmission line: counterclockwise rotation around the  $Z_0$  of the line, every half-wave length corresponds to one complete rotation around  $Z_0$  on the Smith chart.
- Lumped capacitor: counterclockwise rotation on the line of constant resistance toward open circuit. The smaller the capacitance, the larger the translation.
- Lumped inductor: clockwise rotation on the line of constant resistance toward open circuit. The larger the inductance, the larger the translation.

Shunt connection:

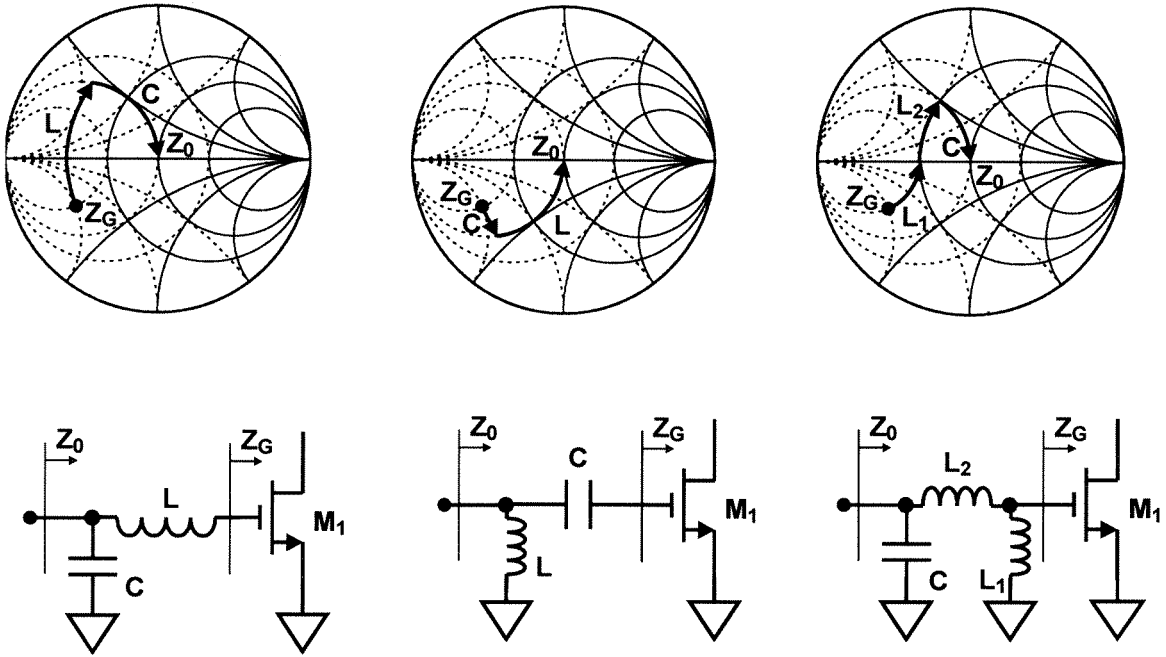
- Transmission line with short circuit end termination: counterclockwise rotation on the line of constant conductance toward short circuit, when the line is shorter than quarter-wave length. The shorter, the closer to the short. When the line is longer than quarter wave, clockwise on the line of constant conductance passing through short when the line is half-wave length.



**Figure 3.2:** Electrical equivalent model of a loss-less magnetically coupled transformer.

- Transmission line with open end termination: clockwise rotation on the line of constant conductance toward short circuit, passing through short circuit when the line is quarter-wave length.
- Lumped capacitor: clockwise rotation on the line of constant conductance toward short circuit.
- Lumped inductor: counterclockwise rotation on the line of constant conductance toward short circuit.
- Magnetically coupled inductors (transformers): As its behavior can be simulated by a combination of inductors and ideal transformers as shown by the equivalent electrical model of Figure 3.2, we can apply the Smith chart rules as described above to each one of internal equivalent component of the transformer to have its impedance transformation characteristics calculated using a Smith chart.

Other two-port components such as isolators are not considered here, as they are normally not able to be integrated. Figure 3.3 shows some examples of how the capacitive gate or base is matched to  $50\Omega$  using Smith chart and the electrical diagram of the corresponding input networks are shown below each chart. Further details about this method, such as how to read the component values from the chart can be found in many



**Figure 3.3:** Transistor gate matching examples using Smith chart. The gate with  $(12.5+12.5j)\Omega$  is transformed to  $50\Omega$ .

text books [30]. Analytical solutions for these networks can be found using the results of Chapter 4 as well as in many references [31]. This chapter also cover other related subjects such as their frequency response and multi-stage networks, which are beyond the scope of this work.

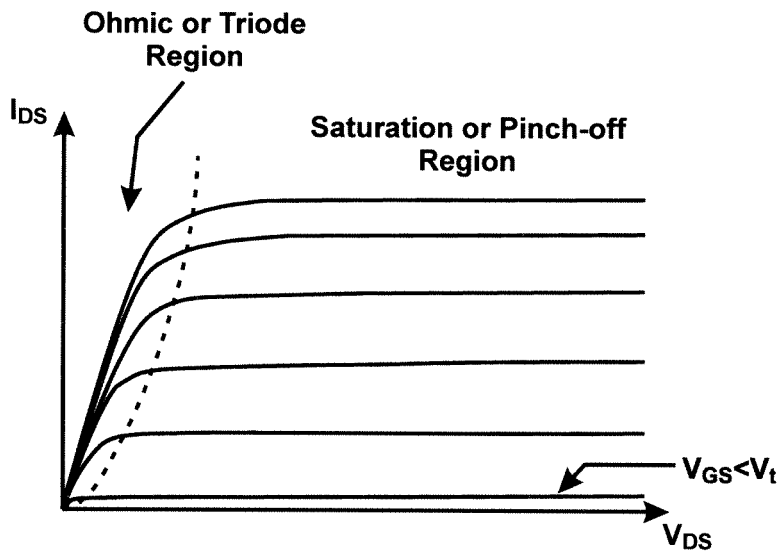
In a silicon integrated power amplifier design, where inductor  $Q$  is extremely low, the designer also needs to spend a significant effort to choose a network topology, which accomplishes the transformation with the smallest power loss. The treatment of power loss and its minimization is treated in Chapter 4.

## 3.2 Active Device

The active device plays a fundamental role in the performance of the power amplifiers, as it is one of the main sources of power loss and signal distortion, besides being the gain unit.

It is difficult to understand the operation of the active devices driving a power amplifier as, unlike in the most of other blocks of integrated circuits, the transistors in a power amplifier operate in a large signal mode and cannot always be approximated to the controlled linear current sources [32].

Under a large signal operation, transistor is operating in one or more of the three states, namely, open (below threshold), resistive (triode region), or current source (saturation region). In which of these three states the transistor will operate depend mostly on the drain and gate dc biases. An illustrative example of an IV curve is shown in Figure 3.4.



**Figure 3.4:** Typical NMOS Transistor IV curve.

Depending on which of these regions are used by the transistor, the amplifiers can be separated in two categories, namely transconductance amplifiers and switching amplifiers. In a transconductance amplifier a transistor operates all the time within saturation region and below threshold,  $V_{gs} < V_t$ , and in a switching amplifier it operates as much as possible within ohmic region and below threshold. As the scope of this work is high performance rf power amplifiers, we will consider amplifier topologies using only n-channel or npn transistors. These transistors present significantly higher frequency responses and gains

than their corresponding p-channel and pnp transistors using the same technology, due to their higher charge mobility.

As we cannot have dc currents conducting through the load in most applications, we need to use either a dc current supply, which is unavailable in most of the applications, or a high impedance component at rf frequencies connecting the transistor drain or collector to a dc voltage supply. To be able to have a high power efficiency, this component needs to have a low impedance at dc despite its high impedance at rf frequencies. This condition leads us to an inductor. Resistive or active components does not satisfy this condition and consume a significant power.

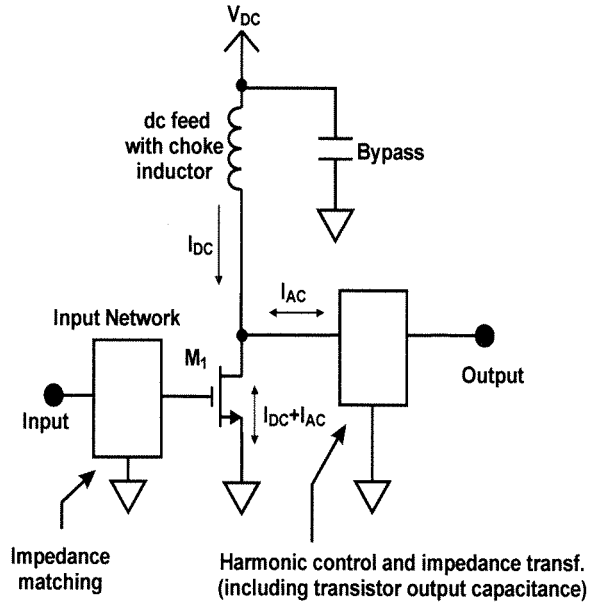
To simplify the analysis, this dc feed inductor is assumed to be a choke inductor with very high reactance connected in series to the transistor from a dc voltage supply, as can be seen in Figure 3.5. It is noteworthy that in many circuits the dc current supply may not necessarily be connected in this way. We will use the common source or emitter topology only, as other configurations present some shortfalls. The source or emitter follower presents no voltage gain, which severely limits the output impedance to a very low value in order to obtain a desired power. The common gate or base presents undesirable low input impedance, difficult to be matched to the  $50\Omega$  input.

Also in our analysis, the transistor output capacitance will be included in the output network as shown by Figure 3.1 and the transistor parasitic feedback capacitor will be neglected to make the discussion simpler. This last capacitance plays a very important role in the power amplifier stability, gain, and phase linearity, but these topics are beyond the scope of this work.

### 3.2.1 Transconductance Amplifiers

Transconductance amplifiers are those amplifiers, in which the transistors are operating always as current sources. The choke inductor conducts a dc current, the output network connected to the load conducts only ac currents, and the transistor therefore conducts the





**Figure 3.5:** Block diagram of a typical single ended power amplifier using a choke inductor as its dc current source.

sum of these dc and ac currents, as can be seen in Figure 3.5. The impedance of the output network including the load at each harmonic frequency and the ac current injected by the transistor to its input port will define the voltage waveform at the transistor drain or collector. As can be understood using IV curve, if this voltage waveform does not reach below the transistor knee voltage<sup>1</sup>,  $V_k$ , the transistor will be operating always as a current source. In this case, the transistor current is approximately proportional to the square of the difference between the gate voltage and its threshold in a NMOS transistor or to the base current in a npn bipolar transistor as can be seen in the following equations from [33]:

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_t)^2 \quad (3.1)$$

$$I_C = \beta \cdot I_B \quad (3.2)$$

1. The transistor knee voltage is the drain to source or collector to emitter voltage, which limits the ohmic region from the pinch-off region in a IV curve as shown by the dashed line in Figure 3.4.

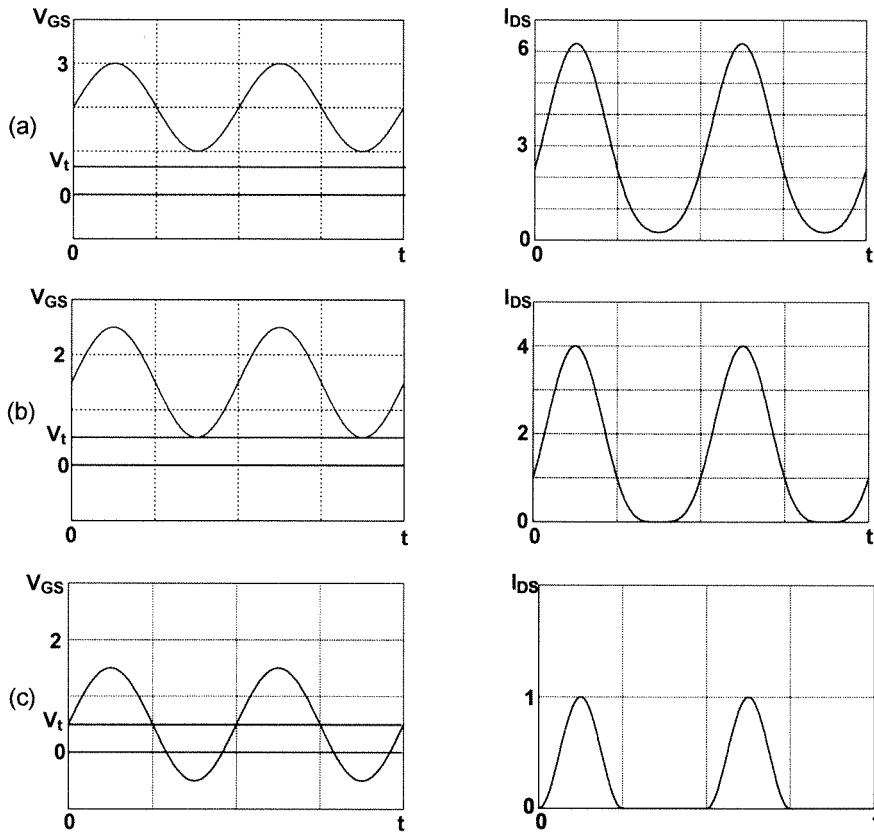
$$I_C = I_S \cdot \exp \frac{V_{BE}}{V_T} \quad (3.3)$$

where  $I_D$  is the drain current,  $I_C$  is the collector current,  $V_{GS}$  is the gate source voltage,  $V_t$  is the threshold voltage,  $I_B$  is the base voltage,  $\mu$  is the channel mobility,  $C_{ox}$  is the gate oxide capacitance per unit area,  $W$  is the gate width,  $L$  is the gate length,  $\beta$  is the bipolar current gain,  $I_S$  is the junction reverse saturation current,  $V_{BE}$  is the transistor base emitter voltage, and  $V_T$  is the transistor built in junction voltage.

As mentioned in Section 3.1, our study will be limited to only the cases with a fundamental frequency signal in the gate or base. Under this restriction, we can have either sinusoidal voltage or sinusoidal current. We cannot have both, the current and voltage, sinusoidal at the gate or base as they present strong non-linearities. A series or shunt resonant circuit connected to the gate or base is necessary to keep the voltage or current sinusoidal. Among four possible combinations, series or shunt with NMOS or bipolar transistors, in this work we will analyze the shunt matched NMOS with sinusoidal gate voltage and the series bipolar with sinusoidal base current, as they are the most simple ones. The bipolar transistors with a significantly sinusoidal voltage signal at the base is of extreme importance as this mode allows classes AB, B, and C, but unfortunately their collector waveforms in large signal cannot easily be solved analytically in terms of power efficiency and gain.

The current through the drain can be calculated using equation (3.1) and approximating the drain current to zero when the gate voltage is below  $V_t$ . Its waveform is significantly sinusoidal as illustrated by Figure 3.6.

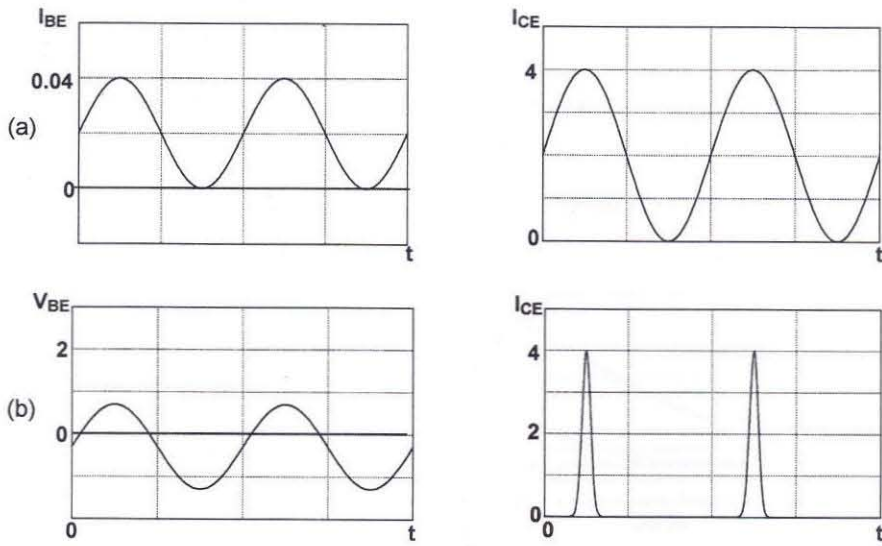
If a bipolar transistor is driven by a sinusoidal current, by (3.2) we have significantly sinusoidal current through the collector. On the other hand, by (3.3) we can see that a significantly sinusoidal voltage at the base causes a very narrow current pulses through the collector. Both cases are illustrated by Figure 3.7.



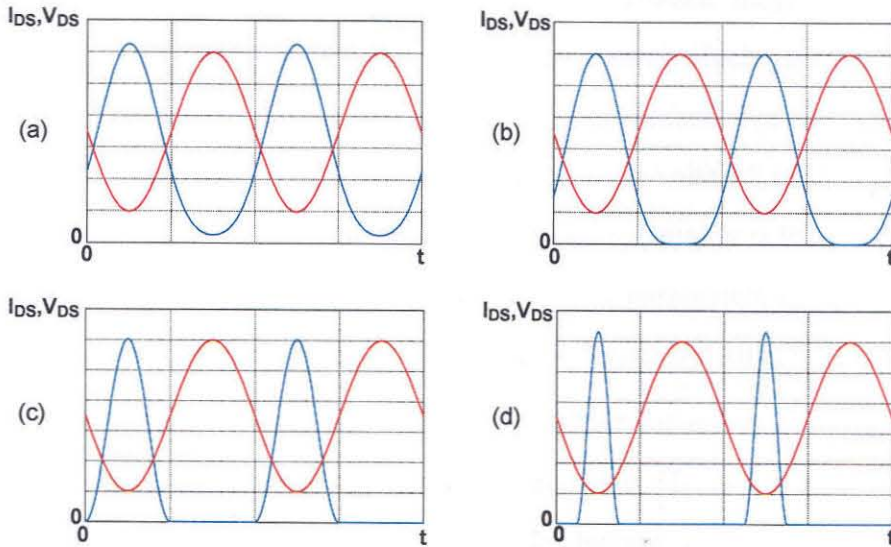
**Figure 3.6:** Gate voltages, at left, and corresponding drain currents, at right, of an ideal NMOS transistor. a)  $V_{gs} \gg V_t$ , b)  $V_{gs} \geq V_t$ , and c)  $V_{gs(\text{average})} = V_t$ .

Under the condition described above, if the output network presents a short circuit at all overtones, forcing the drain or collector waveform to be a sinewave at the fundamental frequency, we have amplifiers in classes A, AB, B, or C. If the transistor is conducting continuously, the amplifier class will be A. If it is conducting more than 50% of the cycle, it is denoted AB. If it is conducting around 50% of the time, it is class B, and finally, if it is conducting less than 50% of the cycle, it is class C.

The designer can choose one among these options, A, AB, B, or C, by changing the dc bias voltage and the driving power of the gate or base. We can see in Figure 3.8 the voltage and the current waveforms at drain or collector for each one of these classes.

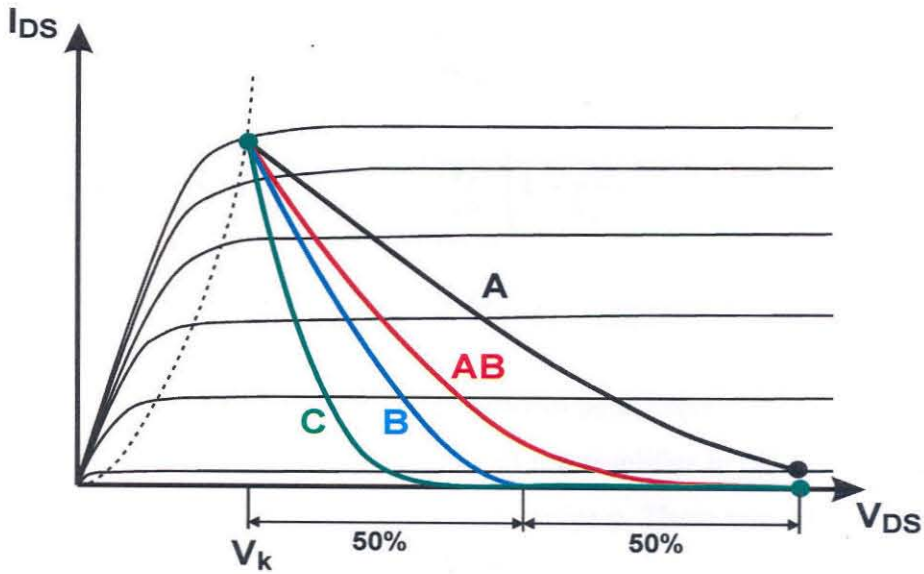


**Figure 3.7:** a) Bipolar base current and corresponding collector current. b) Bipolar base voltage and corresponding collector current.



**Figure 3.8:** a) Class-A voltage, red, and current, blue, waveforms of a power amplifier using an ideal NMOS, b) Class-AB waveforms, c) Class-B waveforms, and d) Class-C waveforms.

Figure 3.9 shows the transistor IV curve and transistor load line for each one of amplifiers in these classes.



**Figure 3.9:** Typical load lines of classes A, AB, B, and C power amplifiers using NMOS transistor.

In order to compare the performance difference between these classes and later between them and other classes, it is important to understand which parameters should be kept the same to each one of the classes to have a fair comparison. For instance, should we use the same supply voltage or same drain or collector peak voltage? Each class presents a different ratio between these two voltages. As the transistor quality is the limiting factor in many applications, we will adopt as our constants some parameters intimately related to them, namely the peak drain or collector voltage and current and knee voltage.

The following equations calculate the maximum “normalized output capability” [12],  $P_N$ , efficiency of the active device,  $\eta$ , and normalized gain,  $G_N$ , as a function of transistor knee voltage,  $V_k$ , supply dc voltage,  $V_{DC}$ , and conduction angle<sup>1</sup>,  $\phi$ , for amplifiers in classes, A, AB, B, and C, assuming the use of a fictitious device, in which the output current is proportional to the input voltage or current when they are above threshold and zero otherwise.

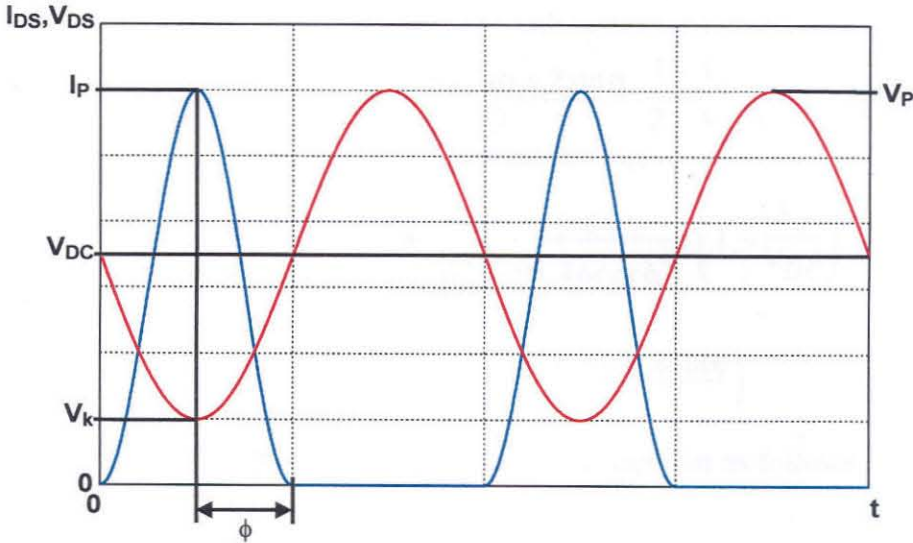
1. Conduction angle is the time interval relative to a period,  $2\pi$ , expressed in radians, during which there is a current flowing through the transistor.

$$P_N = \frac{2\phi - \sin(2\phi)}{4\pi(1 - \cos\phi)} \cdot \frac{1 - V_k/V_{DC}}{2 - V_k/V_{DC}} \quad (3.4)$$

$$\eta = \frac{1}{4} \cdot \frac{2\phi - \sin(2\phi)}{\sin\phi - \phi\cos\phi} \cdot \left(1 - \frac{V_k}{V_{DC}}\right) \quad (3.5)$$

$$G_N = 10\log\left[\frac{2\phi - \sin(2\phi)}{4\pi} \cdot (1 - \cos\phi)\right] \quad (3.6)$$

The  $P_N$  is the output power divided by the product of peak current,  $I_p$ , and peak voltage,  $V_p$ , of the drain or collector. The  $G_N$  is the gain of the amplifier in dB relative to the gain of a class-A amplifier using the same parameters except  $\phi$ . These variable definitions can be better visualized in Figure 3.10.

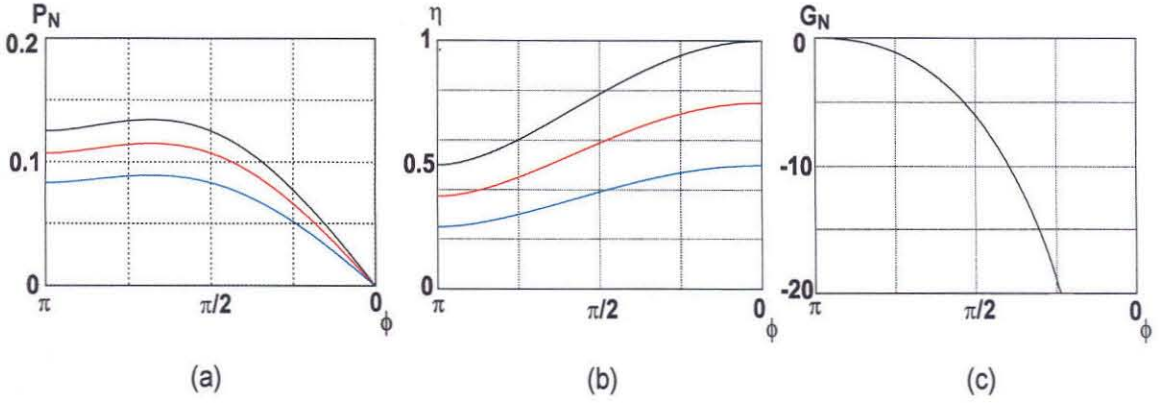


**Figure 3.10:** Voltage (red) and current (blue) waveforms of a power amplifier with the definitions of  $V_P$ ,  $V_k$ ,  $V_{DC}$ ,  $I_P$ , and  $\phi$ .

Figure 3.11 shows plots of  $P_N$ ,  $\eta$ , and  $G_N$  vs.  $\phi$  for amplifiers operating in one of the above classes for several different ratios of  $V_k/V_{DC}$ .

The previous assumption that the current is proportional to the sinusoidal driving signal is not true for most circuits. In NMOS devices, the drain current is approximately quadratic to the gate voltage, (3.1), but still it is possible to calculate the  $P_N$ ,  $\eta$ , and  $G_N$  of





**Figure 3.11:** Using an ideal linear device: a)  $P_N$  vs.  $\phi$  for  $V_k/V_{DC}=0$  (black)  $V_k/V_{DC}=0.25$  (red) and  $V_k/V_{DC}=0.5$  (blue). b)  $\eta$  vs.  $\phi$  c)  $G_N$ [dB] vs.  $\phi$ .

a power amplifier in classes A, AB, B, and C using this ideal square-law NMOS device as a function of  $\phi$ , as follows:

$$P_N = \frac{1}{3\pi} \cdot \frac{\cos^2 \phi \sin \phi - 3\phi \cos \phi + 2 \sin \phi}{(1 - \cos \phi)^2} \cdot \frac{1 - V_k/V_{DC}}{2 - V_k/V_{DC}} \quad (3.7)$$

$$\eta = \frac{4}{3} \cdot \frac{\cos^2 \phi \sin \phi + 2 \sin \phi - 3\phi \cos \phi}{2\phi + \sin(2\phi) - 8 \sin \phi \cos \phi + 4\phi \cos^2 \phi} \cdot \left(1 - \frac{V_k}{V_{DC}}\right) \quad (3.8)$$

$$G_N = 10 \log \left( \frac{\cos^2 \phi \sin \phi - 3\phi \cos \phi + 2 \sin \phi}{3\pi} \right) \quad (3.9)$$

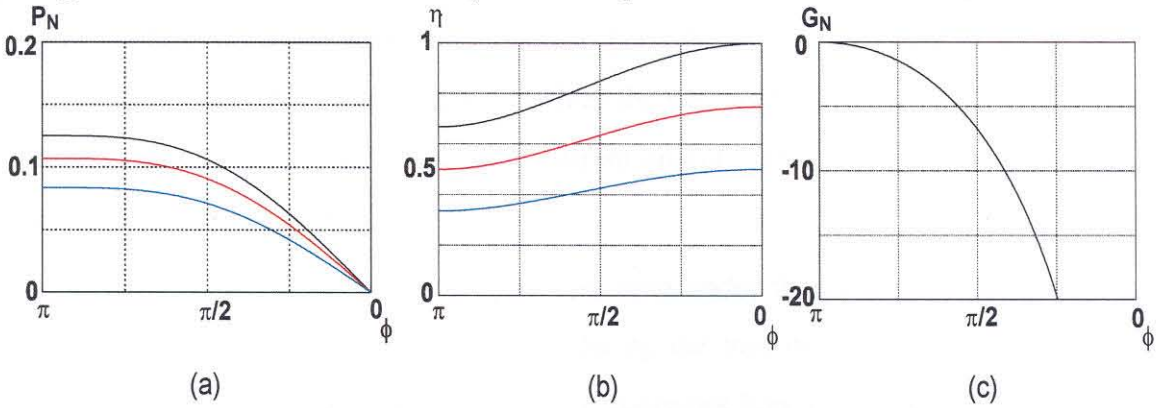
We can also calculate the approximate gain,  $G$ , of the amplifier as follows:

$$G = 10 \log \left( \frac{2}{3\pi} \cdot \frac{\mu C_{ox} W}{L} \cdot \frac{Q_{in}}{\omega C_{gs}} \cdot (\cos^2 \phi \sin \phi - 3\phi \cos \phi + 2 \sin \phi) \cdot (V_{DC} - V_k) \right) \quad (3.10)$$

where  $Q_{in}$  is the quality factor of the transistor gate matching circuit,  $\omega$  is the angular frequency, and  $C_{gs}$  is the gate to source capacitance.

Figure 3.12 shows plots of  $P_N$ ,  $\eta$ , and  $G_N$  vs.  $\phi$  for amplifiers using an ideal NMOS device and operating in one of the classes A, AB, B, or C under several different ratios  $V_k/V_{DC}$ . We can clearly see the effect of the current waveform providing an enhanced power efficiency to this amplifier using a quadratic NMOS when compared to an amplifier

using a linear device. The current pulse in a quadratic NMOS is narrower than that of



**Figure 3.12:** Using an ideal NMOS device: a)  $P_N$  vs.  $\phi$  for  $V_k/V_{DC}=0$  (black),  $V_k/V_{DC}=0.25$  (red), and  $V_k/V_{DC}=0.5$  (blue). b)  $\eta$  vs.  $\phi$  c)  $G_N$  [dB] vs.  $\phi$ .

linear device reducing the overlap between the device current and voltage waveforms, which generates the device power loss.

Based on these plots of Figure 3.11 and Figure 3.12 showing the performance of an ideal power amplifier, we can draw some conclusions. Although the efficiency is enhanced with lower conduction angles reaching 100% with zero conduction angle, the normalized power capability and the gain drops quickly as the angle is reduced, limiting the theoretical upper limit of the efficiency of a class C amplifier significantly below 100%. The normalized power capability of the class-AB power amplifier using an ideal linear device is higher than that of classes A or B. A high knee voltage significantly reduces the efficiency and the normalized output power capability of a power amplifier.

Similar power, efficiency, and gain analysis, as just presented for FETs, can be performed for amplifiers using bipolar transistors, but it is significantly more complex, as bipolar transistors normally do not operate with strictly sinusoidal voltage or sinusoidal current driving their bases. A large sinusoidal base voltage will allow only class-C operation due to the strong collector current peaking caused by the exponential nature of the relation between base voltage and collector current as can be seen in (3.3) and in



Figure 3.7. A sinusoidal base current will allow only class-A operation due to the almost linear relation between base and collector currents as can be seen in (3.2) and in Figure 3.7. To operate in other classes, such as the very useful classes AB or B, one needs to drive the base with quasi-sinusoidal current and/or voltage, which, unfortunately, is very complex to treat analytically.

So far, we have analyzed amplifiers operating under their maximum output power. Next, we will focus on how they behave during the transition from zero to maximum output power. The following set of equations describes how  $P_N$ ,  $\eta$ , and  $G_A$  changes as a function of  $\phi$  and  $k$ , where  $k$  is the square root of the normalized input power,  $P_{inN}$ . Its value is unity when the power amplifier is operating at its maximum output power.

$$P_N = \begin{cases} 0 & 0 < k < \cos\phi \\ \frac{(k(2\phi + \sin(2\phi)) - 4\sin\phi\cos\phi)^2}{4\pi(1 - \cos\phi)(2\phi - \sin(2\phi))} \cdot \frac{1 - V_k/V_{DC}}{2 - V_k/V_{DC}} & |\cos\phi| < k \\ \frac{\pi k^2}{(1 - \cos\phi)(2\phi - \sin(2\phi))} \cdot \frac{1 - V_k/V_{DC}}{2 - V_k/V_{DC}} & \cos\phi < k < 0 \end{cases} \quad (3.11)$$

$$\eta = \begin{cases} 0 & 0 < k < \cos\phi \\ \frac{(k(2\phi + \sin(2\phi)) - 4\sin\phi\cos\phi)^2}{4(k\sin\phi - \phi\cos\phi)(2\phi - \sin(2\phi))} \cdot \left(1 - \frac{V_k}{V_{DC}}\right) & |\cos\phi| < k \\ \frac{-\pi k^2}{\cos\phi(2\phi - \sin(2\phi))} \cdot \left(1 - \frac{V_k}{V_{DC}}\right) & \cos\phi < k < 0 \end{cases} \quad (3.12)$$

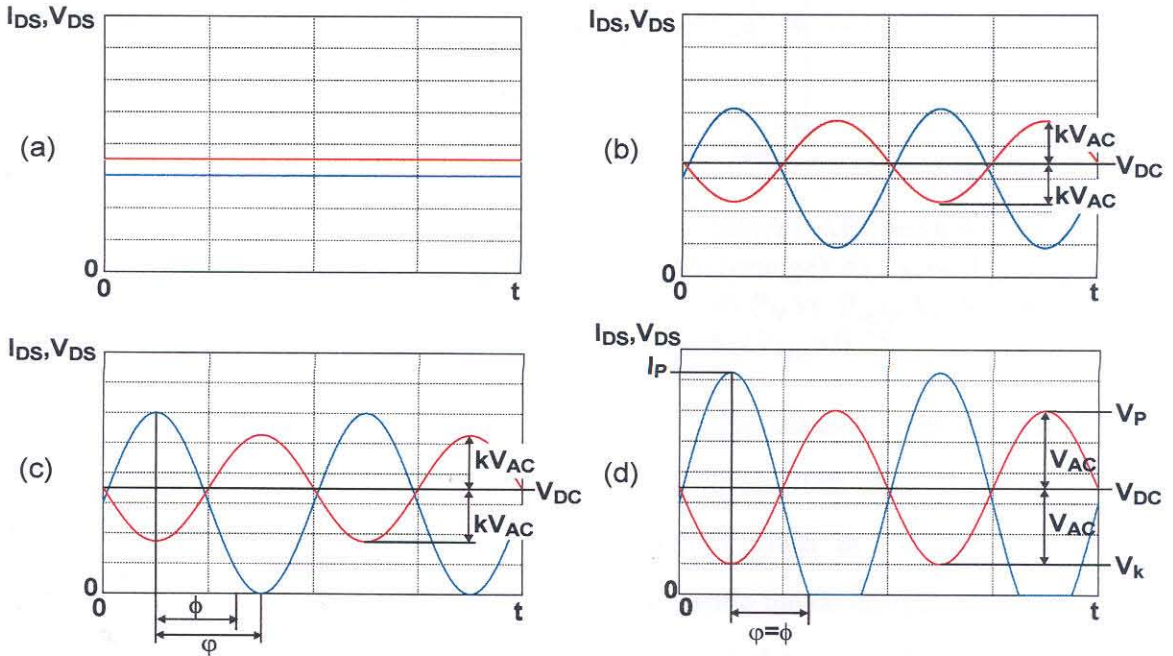
$$G_N = \begin{cases} 0 & 0 < k < \cos\phi \\ 10\log\left(\frac{(k(2\phi + \sin(2\phi)) - 4\sin\phi\cos\phi)^2(1 - \cos\phi)}{4\pi k^2(2\phi - \sin(2\phi))}\right) & |\cos\phi| < k \\ 10\log\left(\frac{\pi(1 - \cos\phi)}{2\phi - \sin(2\phi)}\right) & \cos\phi < k < 0 \end{cases} \quad (3.13)$$

where

$$\varphi = \arccos\left(\frac{\cos\phi}{k}\right) \quad (3.14)$$

$$k = \sqrt{P_{inN}} \quad (3.15)$$

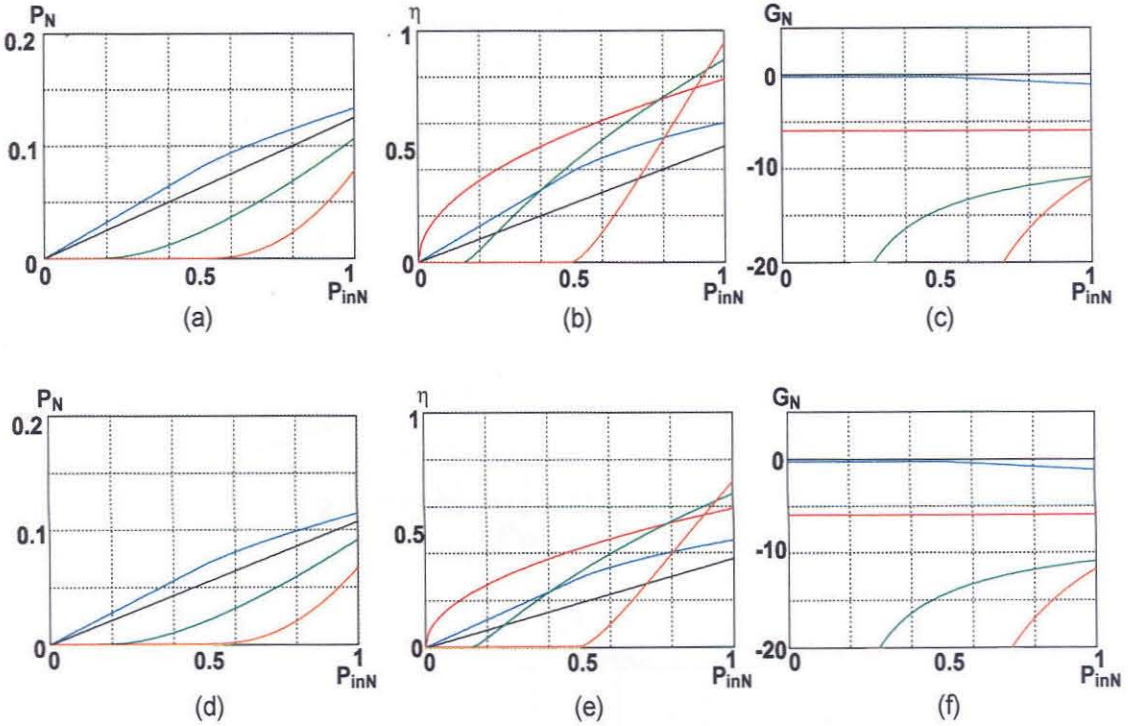
In each set of equations, the first equation is for class C amplifier with input signal below threshold all the time,  $\cos\phi > 0$ , the second equation is for classes C, B, and AB while their current sinusoids are truncated and the third equation is for classes AB and A while their current sinusoids are complete,  $\cos\phi < 0$ . These equations were calculated assuming that the sinusoidal current position is fixed, while  $k$  and  $\varphi$  are changing. Figure 3.13 clarifies how the  $k$  and  $\varphi$  are changing the current and voltage waveforms.



**Figure 3.13:** Voltage, red, and current, blue, waveforms of a Class-AB amplifier with  $\phi=0.75\pi$  at different power levels a)  $k=0$  with zero output power, b)  $k=0.5$ , c)  $k=\sqrt{2}$  and  $\varphi=\pi$ , d)  $k=1$  and  $\varphi=0.75\pi$ .

Figure 3.14 shows the  $P_N$ ,  $\eta$ , and  $G_N$  vs.  $P_{inN}$  for  $V_k/V_{DC}=0$  and  $V_k/V_{DC}=0.25$  for amplifiers in classes A, AB, B, and C using (3.11), (3.12), (3.13), (3.14), and (3.15).

These plots show that the only linear classes, even when the active device is linear, are classes A and B. We can also see that although the highest efficiency at maximum output

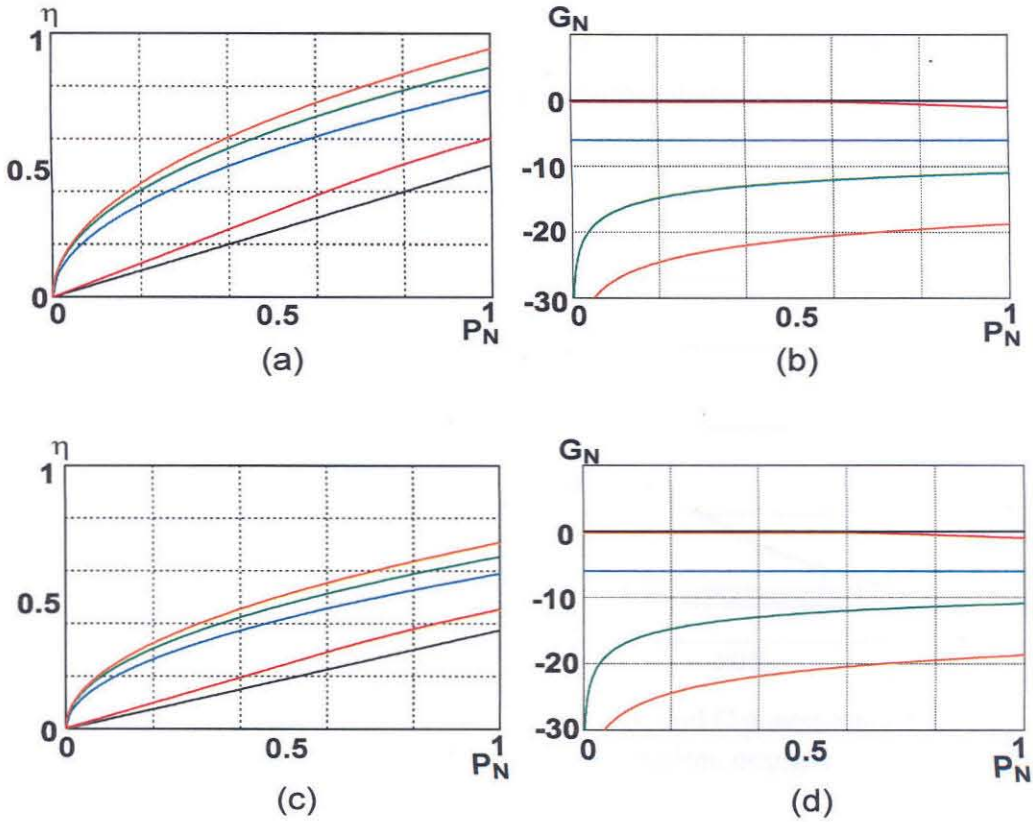


**Figure 3.14:** Performance of amplifiers in classes A (black), AB ( $\phi=3\pi/4$ ) (blue), B (red), C( $\phi=3\pi/8$ ) (green), and C( $\phi=\pi/4$ ) (orange). a)  $P_N$  vs.  $P_{inN}$ ,  $V_k=0$ , b)  $\eta$  vs.  $P_{inN}$ ,  $V_k=0$ , c)  $G_N$  vs.  $P_{inN}$ ,  $V_k=0$ , d)  $P_N$  vs.  $P_{inN}$ ,  $V_k/V_{DC}=0.25$ , e)  $\eta$  vs.  $P_{inN}$ ,  $V_k/V_{DC}=0.25$ , f)  $G_N$  vs.  $P_{inN}$ ,  $V_k/V_{DC}=0.25$ .

power is achieved with a class C at low conduction angle, class-B amplifiers present the highest efficiency at lower input and output power levels. The class B presents better efficiency than A at lower power levels. When output power in a class B amplifier is reduced, its dc current<sup>1</sup> and dc power also decrease, while the dc current and dc power of class-A amplifiers are independent of the output power and remains always constant. The class C power amplifiers also present a lower efficiency at lower output power levels, as their gain at low input power level is severely limited by the geometry of their current waveforms reducing both efficiency and output power.

1. The average current of class B amplifier decreases with its amplitude as its waveform is a half sinusoid and asymmetric, while the average current of a class A amplifiers does not change with its amplitude as its waveform is a complete sinusoid and symmetric.

Figure 3.15 shows the plots for  $\eta$  and  $G_N$  normalized for  $P_N$ . Under this condition we can see that class-C has the highest efficiency at every output power level. Under the normalized output power, the lower conduction angle, the higher efficiency at every output level.

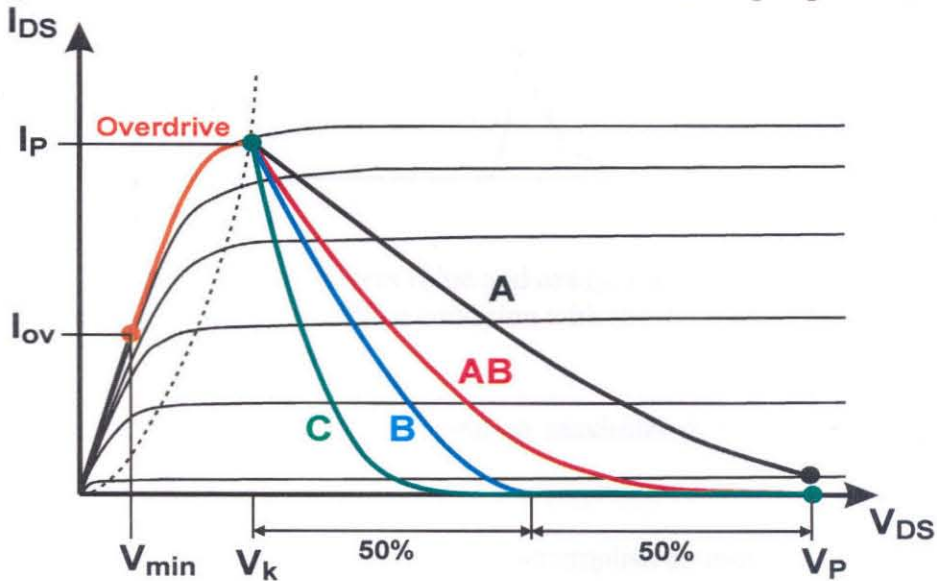


**Figure 3.15:** Performance of amplifiers in classes A (black), AB ( $\phi = 3\pi/4$ ) (blue), B (red), C ( $\phi = 3\pi/8$ ) (green), and C ( $\phi = \pi/4$ ) (orange). a)  $\eta$  vs.  $P_N$ ,  $V_k = 0$ , b)  $G_N$  vs.  $P_N$ ,  $V_k = 0$ , c)  $\eta$  vs.  $P_N$ ,  $V_k/V_{DC} = 0.25$ , d)  $G_N$  vs.  $P_N$ ,  $V_k/V_{DC} = 0.25$ .

At this point one might ask: What happens if an ideal power amplifier in class A, AB, B, or C is driven beyond the maximum point so far used, which is  $P_N = 1$  and the voltage amplitude is equal to  $V_{DC} - V_k$ ? The short straightforward answer is: The output power and efficiency will be severely affected as the current waveform will be strongly distorted. This condition is called over driven classes A, AB, B, or C.



In an ideal over driven class A to C, as all overtones are short circuited, the voltage waveform always remains sinusoidal. If the lower peak of this voltage waveform has to go below the  $V_k$  due to the overdrive, the load line must curve downward towards the origin of the IV curve as can be seen in Figure 3.16, reducing both  $V_{DS}$  and  $I_{DS}$  until reaching the minimum  $I_{ov}$  and  $V_{min}$ . The corresponding drain voltage and current waveforms can be seen in Figure 3.17. We can see in these waveforms that the output power is reduced

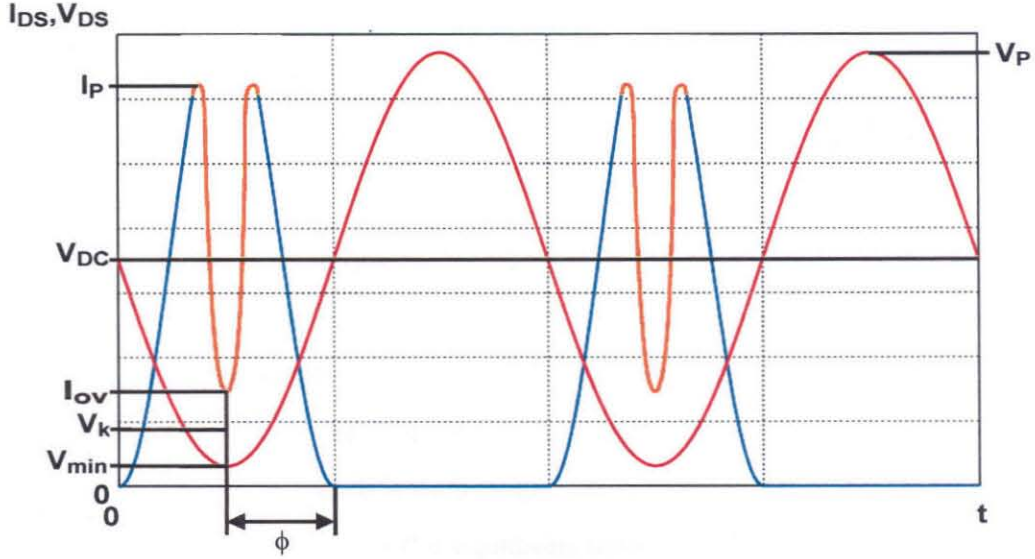


**Figure 3.16:** Typical load lines of classes A, AB, B, and C power amplifiers using NMOS transistor under overdrive condition, orange.

compared to the power when  $V_k=0$  due to the reduction of the fundamental frequency component of the drain current waveform and the efficiency is also reduced due to the drain current peaking,  $I_p$ , occurring twice per cycle, when the drain voltage is still high.

An analytical solution to calculate the output power, efficiency, and gain under overdrive is possible, but is beyond the scope of this work. These results also can easily be obtained from any circuit simulator without analytical analysis.

Once the designer has chosen the appropriate class among A, AB, B, or C based on the information discussed so far and decided the gate or base bias condition, the second but very important parameter to be determined in a power amplifier design is the transistor



**Figure 3.17:** Voltage (red) and current (blue and orange) waveforms of a class-B power amplifier under overdrive condition with the definitions of  $V_P$ ,  $V_k$ ,  $V_{min}$ ,  $V_{DC}$ ,  $I_P$ ,  $I_{ov}$ , and  $\phi$ .

type and size. They allow a further optimization maximizing the output power, power gain, and the power efficiency,

Assuming that we have an acceptable way to accomplish an impedance transformation from the transistor output to the load, we can conclude that under a fixed transistor size and type, and fixed drain or collector current, the higher the drain or collector load resistance,  $R_D$ , the higher will be the maximum output power,  $P_{out}$ , the power added efficiency,  $PAE$ , and the power gain,  $G$ . The equations below show these points for a NMOS transistor, by calculating these values as a function of the load resistance, input power,  $P_{in}$ , gate peak voltage,  $P_{gP}$ , drain efficiency,  $\eta$ , conduction angle,  $\phi$ , threshold voltage,  $V_t$ , and transistor parameters.

$$\begin{aligned}
 P_{out} &= \frac{I_o^2 \cdot R_D}{2} \\
 &= \left( \frac{\mu C_{ox} W}{3\pi L} \right)^2 \cdot \frac{(\cos^2 \phi \sin \phi - 3\phi \cos \phi + 2 \cos \phi)^2}{(1 - \cos \phi)^4} \cdot (V_{gP} - V_t)^4 \cdot R_D
 \end{aligned} \tag{3.16}$$

$$G = \frac{I_o^2 \cdot R_D}{2P_{in}} \quad (3.17)$$

$$PAE = \eta \cdot \left(1 - \frac{1}{G}\right) \quad (3.18)$$

where  $I_o$  is the fundamental frequency component of the drain current. In this equation,  $\eta$ ,  $P_{in}$ ,  $\phi$ , and  $P_{gP}$  are independent of  $R_D$ . Hence  $P_{out}$ ,  $G$ , and consequently  $PAE$  increase with larger  $R_D$ . In the equations above, it seems that we should have an infinite load resistance for the highest PA performance. This is not true, as any active device can support only a certain maximum voltage, which is their output breakdown voltage. Including this physical limitation and knee voltage in the equations above, we have the more realistic ones shown below:

$$\begin{aligned} P_{out} &= \frac{I_o \cdot (V_P - V_k)}{4} \\ &= \left( \frac{\mu C_{ox} W}{2L} \right) \cdot \frac{(\cos \phi^2 \sin \phi - 3\phi \cos \phi + 2\cos \phi)}{6\pi(1 - \cos \phi)^2} \cdot (V_{gP} - V_t)^2 \cdot (V_P - V_k) \end{aligned} \quad (3.19)$$

where  $V_P$  is the drain peak voltage, which must be lower than the drain breakdown voltage.

The above equations, (3.16), (3.17), (3.18), and (3.19), show that in order to obtain the highest power gain and PAE, the drain peak voltage should be as close as possible to the transistor breakdown voltage. Any amplifier using a current source device, including the bipolar transistor, shows this characteristic. Using this limitation, we can calculate the transistor drain or collector resistance once a desirable maximum output power is given, as follows:

$$R_D = \frac{(V_P - V_k)^2}{8P_{out}} \quad (3.20)$$

In an amplifier using an NMOS transistor, the power gain is constant with the transistor size as both  $P_{out}$  and  $P_{in}$  are approximately proportional to  $W$  and the square of the gate ac

voltage. The  $V_k$  scales approximately inversely proportional to the transistor size, when  $R_D$  is fixed. Therefore, the larger the transistor the higher will be the power efficiency of the amplifier.

But, again, there is a limit on the transistor size, as the loaded  $Q$  of the transistor output capacitor resonating circuit increases with the transistor size. And as the loaded  $Q$  approaches the value of the unloaded  $Q$  of this resonant circuit, the power efficiency of the output passive network decreases significantly.

Another limitation to the transistor size is the bandwidth requirement for the amplifier. The higher the loaded  $Q$  the narrower will be the amplifier bandwidth and, even if an infinite  $Q$  resonating network is available, the transistor size will be restricted by this factor. This point will be covered in more detail in Section 3.3.

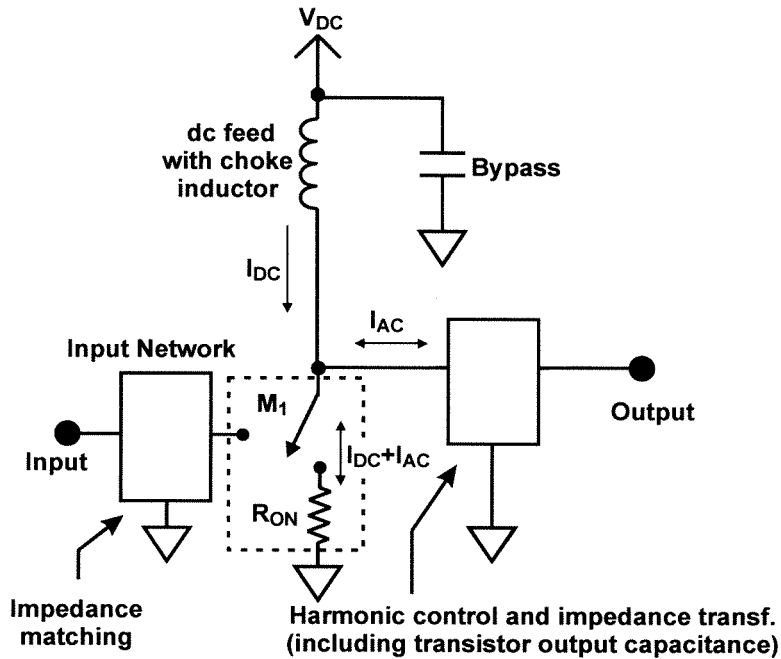
In an amplifier using bipolar transistors, the output power is approximately proportional to the base current and independent of the transistor size, as the collector current is proportional to the base current and collector voltage swing is limited by the supply voltage and collector breakdown voltage. The input power, when base current is kept constant, is inversely proportional to the transistor size, as the base impedance reduces with transistor size. Also the input power is proportional to the square of the base current. Therefore, the power gain increases approximately proportional to the transistor size. Hence, the transistor should be as large as possible, while the  $Q$  of output network permits.

### 3.2.2 Switching Amplifiers

Switching amplifiers are those amplifiers in which the transistor operates as a switch, *i.e.*, most of the time it is open (below threshold) or it is a low value resistor (triode region). The equivalent electrical diagram can be seen in Figure 3.18. In order to achieve this condition, the transistor gain should be relatively high, normally above 15 dB, and the amplifier should operate with input power significantly higher, normally at least 6 dB



higher than the power necessary to drive the same amplifier with peak class-A output power.



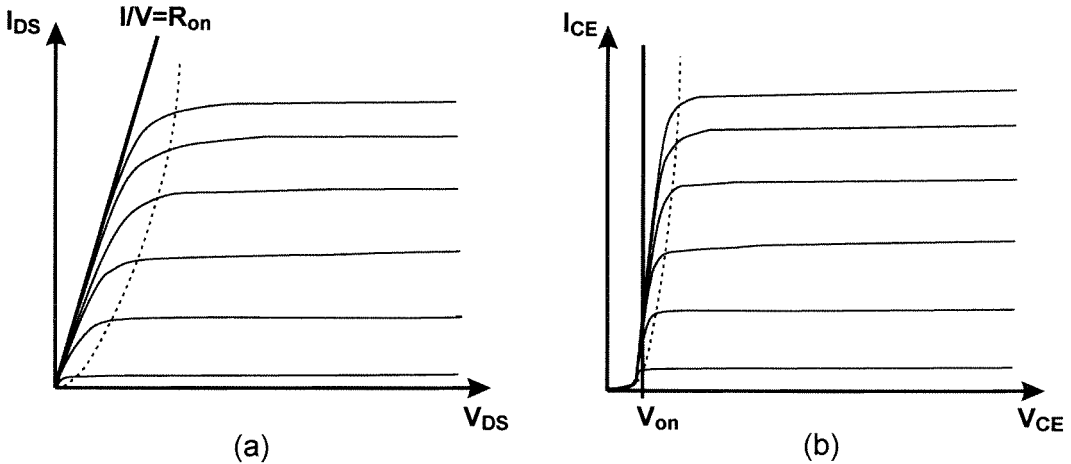
**Figure 3.18:** Fundamental building blocks of a switching power amplifier: input network, active device, and output network. The transistor is represented by its equivalent switch and on resistance.

The power loss at the transistor is kept minimal by always keeping one of either the voltage or the current through it zero or near zero. Using a real transistor, when there is a voltage across it, it is possible to keep its current, not including the current through parasitic capacitances, virtually zero. But when there is current through the transistor, it is not possible to keep the voltage zero, as FET transistors present  $R_{on}$  and bipolar transistors presents  $V_{on}$  as can be seen in the IV curve of Figure 3.19. The second loss comes during the transition from zero current to zero voltage and vice versa. As the transistor switching speed is not infinite, when the transistor is transitioning from conductance to non-conductance and vice versa actively, its current or voltage will decrease gradually and the counterparts voltage or current will start increasing before either of the first two reach zero. This transition loss can be reduced or virtually eliminated if the passive components,

through their resonance, bring the current and/or voltage to zero and the transistor switches after this zero condition is met. Switching amplifiers in which the passive network connected to the transistor drain or collector brings the current to zero before the transistor starts to open is said to be ZCS (zero current switching). Similarly, if the passive network brings the voltage to zero before the transistor starts to close, the amplifier is said to be ZVS (zero voltage switching). Unfortunately, we can prove in that it is theoretically not possible to have both ZVS and ZCS conditions simultaneously [34][35]. The theory in these references proves that the output power of any switching power amplifier is proportional to the integral of voltage or current slope multiplied by current or voltage amplitude during their overlaps.

$$P_{out} \propto \int_0^T \frac{dv}{dt} \cdot \frac{di}{dt} dt \Rightarrow P_{out} \propto \Delta v \cdot \frac{di}{dt} + \Delta i \cdot \frac{dv}{dt} \quad (3.21)$$

Although it is not possible to have ZCS and ZVS simultaneously, in order to reduce the transition loss, all the practical high-frequency<sup>1</sup> switching amplifiers are at least ZVS or ZCS amplifiers.



**Figure 3.19:** a)  $I \times V$  curve of a typical NMOS transistor with the current voltage slope in the ohmic region showing its  $R_{on}$ , b)  $I \times V$  curve of a typical npn bipolar transistor with its  $V_{on}$ .

1. Many low frequency class-D power amplifiers are neither ZVS nor ZCS.

As the output power of a switching power amplifier is constant when input power is above the level necessary to make it operate as a switching amplifier, its power gain can be any value from its maximum value to zero or below.

To be able to analyze their transistor efficiency, the best approximation we can make is the assumption that for part of the cycle the transistor is open, and the remainder a fixed value resistor,  $R_{on}$ . This approximation can be seen in Figure 3.19. Under this assumption, when the switch is open, the current is zero and when the switch is closed, the voltage is almost zero. The efficiency of this simplified model can be calculated as follows:

$$\begin{aligned}\eta &= \frac{P_{out}}{P_{DC}} = \frac{P_{DC} - P_{loss}}{P_{DC}} = \left(1 - \frac{P_{loss}}{P_{DC}}\right) \\ &= 1 - \frac{\int_0^{2\pi} i_D(\theta)^2 R_{on} d\theta}{\frac{1}{2\pi} \int_0^{2\pi} i_D(\theta) d\theta \cdot \int_0^{2\pi} v_D(\theta) d\theta}\end{aligned}\quad (3.22)$$

The output power can be calculated as follows:

$$P_{out} = P_{DC} - P_{loss} = \frac{1}{(2\pi)^2} \int_0^{2\pi} i_D(\theta) d\theta \cdot \int_0^{2\pi} v_D(\theta) d\theta - \frac{1}{2\pi} \int_0^{2\pi} i_D(\theta)^2 R_{on} d\theta \quad (3.23)$$

As can be seen in the (3.22), to maximize the amplifier's efficiency, the ratio between power loss,  $P_{loss}$ , and dc power,  $P_{DC}$ , should be minimized.  $P_{loss}$  is the power dissipated in the transistor on resistance and is proportional to the rms value of the transistor current.  $P_{DC}$  is the product of average current and voltage across the transistor. With drain voltage limited by the transistor breakdown voltage, the best waveform to maximize the  $P_{DC}$  is a square wave for drain voltage waveform<sup>1</sup>. Next, the best drain current waveform to minimize the ratio between average and rms current value seen in the (3.22) again is the square

---

1. A square wave has the lowest ratio between peak and average value among all possible waveforms.

waveform. Under this condition, the output power calculated by (3.23) is also maximized. Similar analysis can be made for bipolar transistor. Although square wave current with square wave voltage at the drain or collector are the best for a PA, unfortunately, this combination has proven difficult, because it requires generation of harmonic power [35].

Besides this best waveform, there are many others, which can be made using a simple or a complex output network controlling several overtones besides the fundamental frequency signal at the transistor collector or drain.

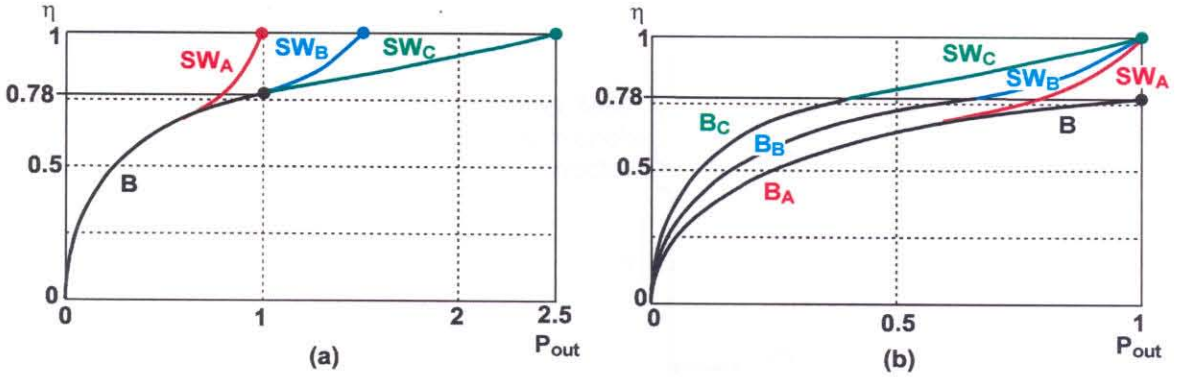
Next we will briefly present each one of the most useful rf switching amplifiers, comparing their performances.

Differently from the classes A to C, each switching amplifier class presents distinct voltage waveform. Consequently, even using the same peak voltage,  $V_p$ , and drain or collector load resistance,  $R_D$ , two amplifiers of different classes might present different output powers. This allows us to have a better metric to compare the output power capability of different amplifier classes than normalized output capability,  $P_N$ , used so far for transconductance power amplifiers. We can compare the available maximum output power of each amplifier class, when using the same peak voltage,  $V_p$ , and drain or collector load resistance,  $R_D$ , instead of peak current as in  $P_N$ . This comparison is better than a comparison under a constant  $I_p$ , as in fully integrated power amplifiers, the major efficiency limiting factor is the impedance transformation network using very lossy inductors. Therefore, we do not have the freedom to choose any  $R_D$ , assuming the use of lossless impedance transformation network and  $R_D$  becomes an important limiting factor. Furthermore, in switching amplifiers, in order to have a reduced  $R_{on}$ , the transistor size is very large relative to the operating current, hence output power is seldom limited by the  $I_p$ . Thus, we will define *load output capability*,  $P_{RD}$ , as the ratio between the maximum output power of a switching amplifier and the maximum output power of the amplifier operating under any of classes A to C with zero  $V_k$  and using the same  $R_D$  and  $V_p$ .

Many switching power amplifiers can be operated at lower input and output power levels as transconductance amplifiers. This dual mode of operation, first as a switching amplifier when operating at their maximum output power level and second as a variable power transconductance amplifier to provide operation at lower output power levels, is becoming very important in wireless communication applications. A dual mode power amplifier can provide a very high power efficiency at peak output power while simultaneously being able to operate at low power as is necessary when the distance between the transmitter and the receiver is short. We introduce here another metric very useful to evaluate the performance of these dual mode power amplifiers, the *load supply output capability*,  $P_{LS}$ .  $P_{LS}$  is  $P_{out}$  normalized by the  $P_{out}$  of a class-A amplifier using the same  $V_{DC}$  and  $R_D$ . A higher  $P_{LS}$  results in higher power efficiency at low level output power in dual mode power amplifiers as can be understood using Figure 3.20, which compares dual mode switching PAs,  $SW_A$ ,  $SW_B$ , and  $SW_C$  with  $P_{LS}=1$ , 1.5, and 2.5 respectively. They present ideal class B operation at lower power levels. Plot (a) shows  $\eta$  vs.  $P_{out}$  of these PAs using the same  $V_{DC}$  and  $R_D$ . Plot (b) shows the efficiency of the corresponding similar PAs with  $R_D$  and/or  $V_{DC}$  adjusted to have the same maximum  $P_{out}$ . We can clearly see the correspondence between  $P_{LS}$  and  $\eta$  at low power levels in the plot (b).

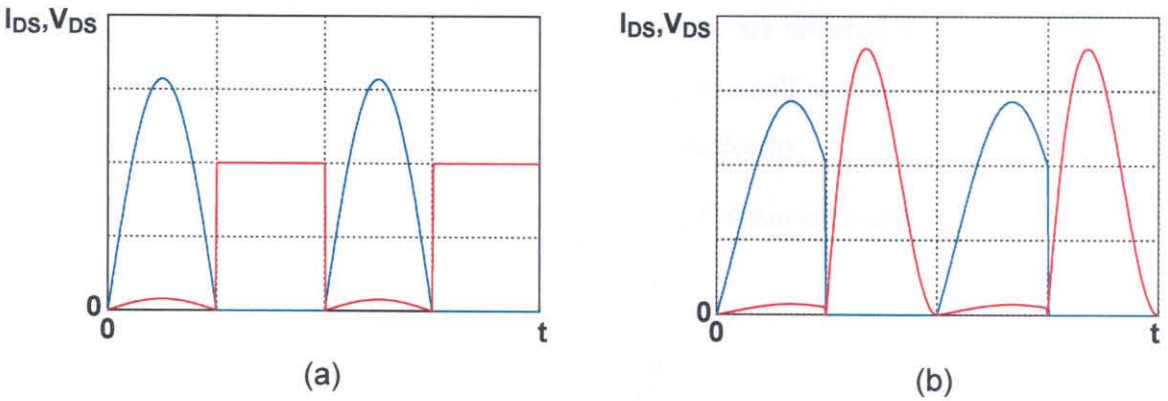
The  $P_N$ ,  $P_{RD}$ ,  $P_{LS}$ , and  $\eta$  will be presented, first limited by  $R_{on}$  normalized by load resistance,  $R_D$ , second limited by  $R_{on}$  normalized by  $P_{out}$  and drain or collector peak voltage,  $V_p$ , and third and last, limited by the product  $R_{on}$  and transistor parasitic output capacitor reactance,  $\omega C_S$ . This last metric is valid only for those switching amplifiers, which allow the transistor parasitic output capacitance as part of the circuit topology, such classes E [36] and E/F<sub>xx</sub> [21].

The most known switching amplifier classes for rf applications are classes E and D or F [36][37][38][39]<sup>1</sup>.



**Figure 3.20:** a)  $\eta$  vs.  $P_{out}$  of a class-B PA B, dual mode PAs  $SW_A$ ,  $SW_B$ , and  $SW_C$  operating in class-B mode at low power level and compressing into switching mode class with  $P_{LS} = 1, 1.5$ , and  $2.5$  respectively, b)  $\eta$  vs.  $P_{out}$  of the similar amplifiers B,  $SW_A$ ,  $SW_B$ , and  $SW_C$  with adjusted  $V_{DC}$  and/or  $R_D$  to have the same maximum  $P_{out}$ .

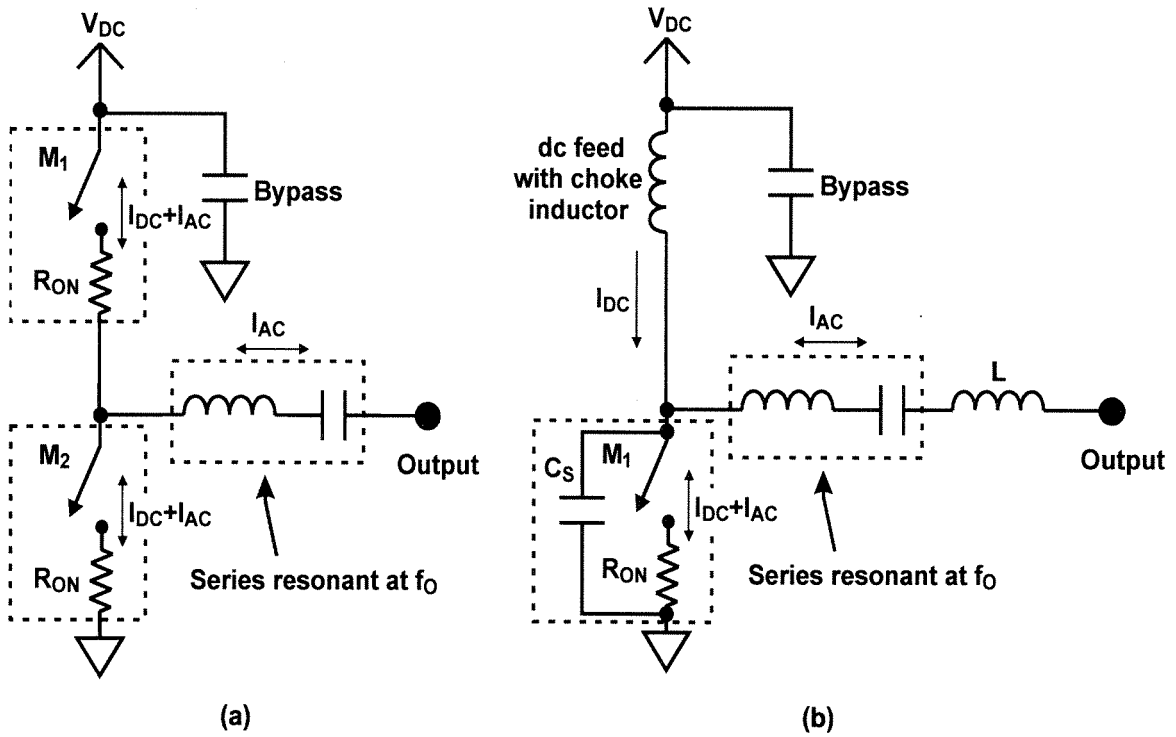
Figure 3.21 shows their waveforms, when the transistors are biased to have 50% duty cycle using an ideal device/transistor model consisting of a switch and on-resistance,  $R_{on}$ , as shown in Figure 3.18. Figure 3.22 shows the simplest topology of class D, F and class E



**Figure 3.21:** a) Drain voltage (red) and drain current (blue) of an ideal class D, F power amplifier with on resistance. b) Same for class-E power amplifier.

amplifiers.

1. Classes D and F are the same class. The denomination D is mostly used for low frequency applications using push-pull topology. The denomination F is a finite-harmonic approximation of D and is normally used for higher frequency application using single ended topology.



**Figure 3.22:** a) An example of class D, F power amplifier. b) Class-E power amplifier.

Further explanation about how these modes operate are covered in Section 3.3. Every equation in the following analysis assumes that  $R_{on}$  is small enough relative to  $R_D$  so as not to significantly distort the voltage and current waveforms.

Below we can see the equations for the class D, F drain efficiency  $\eta_{D,F}$  followed by  $\eta_E$ :

$$\eta_{D,F} = 1 - 2 \frac{R_{on}}{R_D} \quad (3.24)$$

where efficiency is calculated as a function of the ratio between  $R_{on}$  and  $R_D$  and we can call this efficiency,  $R_D$  efficiency,  $\eta_{RD}$ . The derivation of this equation is explained in Section 3.3.1.2. This equation shows that the higher the  $R_{on}$  normalized to the load resistance,  $R_D$ , the lower the efficiency, a quite obvious result. What is interesting to notice here is how the scaling coefficient, two in this case, changes with different classes of operation.

The next equation calculates the same efficiency as a function of  $P_{out}$ , drain or collector peak voltage  $V_p$ , and  $R_{on}$ :

$$\eta_{D, F} = 1 - \pi^2 \cdot \frac{P_{out}}{V_p^2} \cdot R_{on} = 1 - 9.87 \frac{P_{out}}{V_p^2 / R_{on}} \quad (3.25)$$

We can call this efficiency,  $P_{out}$  efficiency,  $\eta_{P_{out}}$ . This last equation shows that when using a transistor with certain  $R_{on}$ , the higher the necessary  $P_{out}$  and the lower the  $V_p$  used, the lower will be  $\eta$ .

We can see below the  $P_N$ ,  $P_{RD}$ ,  $P_{LS}$  of the class D or F amplifiers:

$$P_N = \frac{1}{2\pi} \eta = 0.159 - 0.318 \frac{R_{on}}{R_D} \quad (3.26)$$

$$P_{RD} = \frac{16}{\pi^2} \eta = 1.62 - 3.24 \frac{R_{on}}{R_D} \quad (3.27)$$

$$P_{LS} = \frac{16}{\pi^2} \eta = 1.62 - 3.24 \frac{R_{on}}{R_D} \quad (3.28)$$

The next equations show the corresponding results for class E:

$$\eta_E = 1 - \frac{\pi^2 + 28}{2(\pi^2 + 4)} \cdot \frac{R_{on}}{R_D} = 1 - 1.37 \frac{R_{on}}{R_D} \quad (3.29)$$

$$\eta_E = 1 - \frac{\pi^2 + 28}{4} \cdot \left( \tan\left(\frac{2}{\pi}\right) \cdot \pi \right)^2 \cdot \frac{P_{out}}{V_p^2} \cdot R_{on} = 1 - 30 \frac{P_{out}}{V_p^2 / R_{on}} \quad (3.30)$$

All above equations are derived in Section 3.3.1.2. It is interesting to note that when using the same  $R_D$ , transistor size, and  $R_{on}$ , the efficiency of a class-E PA is higher than that of class-D or F PA. But if we consider the higher  $P_{out}$  of the class-D or F PAs relative to that of the class-E PAs when they are using the same  $R_D$  and calculate the  $\eta$  normalized to the  $P_{out}$  under the same  $V_p$ , class D or F gives a higher  $\eta$ . This happens since under the same  $V_p$  and  $R_D$ , class D or F gives a higher  $P_{out}$  than class E, which is a result of the peaking voltage waveforms of the class E relative to the waveform of class D or F.



One very useful feature of the class-E PA is its topology, in which a capacitor shunt to the transistor output is part of the circuit. This allows the use of a relatively large transistor with a resulting large parasitic drain or collector capacitance without the need of a complex circuit to resonate it as required for the classes D or F PAs. In order to maximize  $\eta$ , the transistor size should be maximized until its shunt parasitic capacitance reaches the appropriate value<sup>1</sup> for the class E operation, so that output capacitance is making up all of the parallel capacitance, thus minimizing the  $R_{on}$ . Below is the  $\eta_E$  under this best transistor size condition calculated as a function of the product  $R_{on}\omega C_S$ <sup>2</sup> of the transistor, where  $C_S$  is the capacitance of the output parasitic capacitor of the transistor and  $\omega$  is the angular frequency.

$$\eta_E = 1 - \frac{\pi(\pi^2 + 28)}{16} \cdot R_{on}\omega C_S = 1 - 7.44 \cdot R_{on}\omega C_S \quad (3.31)$$

It is interesting to note that under the above condition, the efficiency is determined by the ratio  $R_{on}$  divided by the transistor parasitic capacitor reactance  $1/\omega C_S$ . We can call this third way of showing the efficiency,  $C_S$  efficiency,  $\eta_{C_S}$ . There is a situation when this best efficiency condition should not be achieved. It is when the transistor gain is low and making the transistor size large requires too large of an input power, reducing the power added efficiency, PAE. More details about this point will be given at the end of this subsection.

We can see below the  $P_N$ ,  $P_{RD}$ ,  $P_{LS}$  of the class-E amplifier:

$$P_N = \frac{1}{\pi \operatorname{atan}\left(\frac{\pi}{2}\right) \left(\sqrt{\pi^2 + 4} + 2\right)} \eta = 0.0981 - 0.134 \frac{R_{on}}{R_D} \quad (3.32)$$

1. In order to operate in class E mode, an exact proportion must be maintained between the reactance of  $C_S$  and the  $R_D$ .

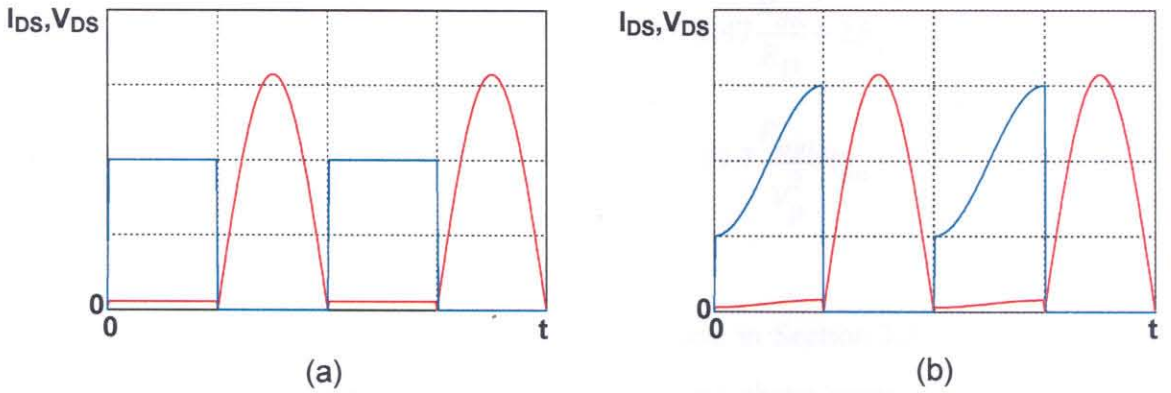
2. Although  $R_{on}$  and  $C_S$  changes with transistor size, the product  $R_{on}\omega C_S$  is constant as  $R_{on}$  decreases and  $C_S$  increases, both proportional to the transistor size.

$$P_{RD} = \frac{16}{\left(\pi \operatorname{atan}\left(\frac{\pi}{2}\right)\right)^2 (\pi^2 + 4)} \eta = 0.363 - 0.496 \frac{R_{on}}{R_D} \quad (3.33)$$

$$P_{LS} = \frac{16}{\pi^2 + 4} \eta = 1.15 - 1.58 \frac{R_{on}}{R_D} \quad (3.34)$$

Further details about these amplifiers such as their impedances of the output network to achieve these waveforms and how they can be derived analytically can be seen in Section 3.3.

More recently developed alternatives of rf switching amplifiers are classes inverse F [40] and several classes belonging to the family E/F<sub>x</sub> [21]. We can see the waveforms of class F<sup>-1</sup> and class E/F<sub>odd</sub>, in Figure 3.23 and their topology is shown in Figure 3.24.

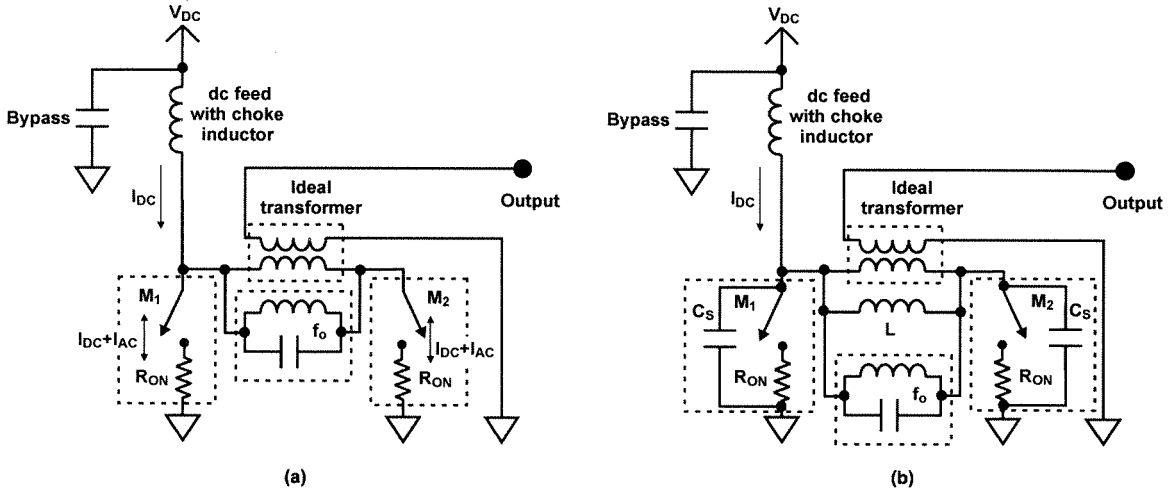


**Figure 3.23:** a) Drain voltage (red) and drain current (blue) of an ideal class-F<sup>-1</sup> power amplifier with on resistance. b) Same for class-E/F<sub>odd</sub> power amplifier.

Their efficiency calculations are shown below:

$$\eta_{F^{-1}} = 1 - \frac{\pi^2}{4} \cdot \frac{R_{on}}{R_D} = 1 - 2.47 \frac{R_{on}}{R_D} \quad (3.35)$$

$$\eta_{F^{-1}} = 1 - 2\pi^2 \cdot \frac{P_{out}}{V_p^2} R_{on} = 1 - 19.7 \frac{P_{out}}{V_p^2} R_{on} \quad (3.36)$$



**Figure 3.24:** a) An example of current mode class D or class-F<sup>-1</sup> power amplifier, b) class-E/F<sub>odd</sub> power amplifier.

$$\eta_{E/F_{odd}} = 1 - \frac{\pi^2}{4} \cdot \frac{R_{on}}{R_D} - 2R_D R_{on} \omega^2 C_S^2 = 1 - 2.47 \frac{R_{on}}{R_D} - 2R_D R_{on} \omega^2 C_S^2 \quad (3.37)$$

$$\eta_{E/F_{odd}} = 1 - 2\pi^2 \cdot \frac{P_{out}}{V_p^2} R_{on} - 2R_D R_{on} \omega^2 C_S^2 = 1 - 19.7 \frac{P_{out}}{V_p^2} R_{on} - 2R_D R_{on} \omega^2 C_S^2 \quad (3.38)$$

where  $\omega$  is the angular frequency.

Their derivations are shown in Section 3.3.1.3 and in Section 3.3.1.6. The new third term in each equation of  $\eta$  for class E/F<sub>odd</sub> amplifiers above comes from the extra loss caused by the peaking of the current waveform due to the current through the transistor parasitic drain or collector output capacitance,  $C_S$ .

Similar to class-E PAs, the class E/F<sub>odd</sub> topology allows a capacitor in parallel to each one of the switches. But unlike class E, the shunt capacitance of a class E/F<sub>odd</sub> amplifier can be any value from zero up to a maximum value. The current peaking of this amplifier increases with larger shunt capacitance, which occurs upward at the end edge of the current waveform and downward at the beginning edge of the same as can be seen in the plot (b) of Figure 3.23. As the current cannot be negative<sup>1</sup>, the maximum value of the capacitance is obtained when the downward peaking of the current reaches zero. This

capacitor reactance is 1.27 times  $R_D$  and the corresponding  $C_S$  size is 2.8 times larger than the  $C_S$  of the class E. It is interesting to notice that the larger the transistor, the smaller will be the  $R_{on}$  reducing the loss, as can be seen in the second term of the  $\eta$ . But the larger the transistor, the larger will be the shunt capacitance and the current peaking, which will increase the loss. This part is represented by the third term of the  $\eta$  equations. Hence, there is a best size for the transistor, which minimizes the loss. This size is achieved when the  $C_S$  reactance is 0.9 times the  $R_D$ . The capacitor in this case is larger than the maximum capacitor when current downward peak touches zero, hence cannot be achieved. So the best capacitor reactance under the positive-current assumption is 1.27 times the  $R_D$ .

The equations below calculate the  $\eta$  as a function of the ratio between reactance of  $C_S$  and  $R_D$  and as a function of transistor product  $R_{on}\omega C_S$ .

$$\eta_{E/F_{odd}} = 1 - \left( \frac{\pi^2}{4} \frac{1}{R_D \omega C_S} + 2R_D \omega C_S \right) R_{on} \omega C_S \quad (3.39)$$

Using the largest transistor size,  $R_D \omega C_S = 0.78$ , we have

$$\eta_{E/F_{odd}} = 1 - 4.72 R_{on} \omega C_S \quad (3.40)$$

The last equation and (3.35) shows that class E/ $F_{odd}$  is more forgiving to the  $C_S$  value and allows the use of a significantly larger transistor size, which provides lower  $R_{on}$  and higher  $\eta$  than what is possible with class E.

We can see below the  $P_N$ ,  $P_{RD}$ ,  $P_{LS}$  of the class-F<sup>-1</sup> amplifiers:

$$P_N = \frac{1}{2\pi} \eta = 0.159 - 0.393 \frac{R_{on}}{R_D} \quad (3.41)$$

---

1. Generally FET loss increases if a negative current is forced through it, as a conduction through slow substrate junction diode will occur. Bipolar transistor will have a direct conduction through the base collector junction, which also have a slow recovery and causes a significant gain and power losses.

$$P_{RD} = \eta = 1 - 2.47 \frac{R_{on}}{R_D} \quad (3.42)$$

$$P_{LS} = \frac{\pi^2}{4} \eta = 2.47 - 6.09 \frac{R_{on}}{R_D} \quad (3.43)$$

Below are the  $P_N$ ,  $P_{RD}$ ,  $P_{LS}$  of the class-E/ $F_{odd}$  amplifiers:

$$\begin{aligned} P_N &= \frac{1}{2\pi \left(1 + \frac{4}{\pi} \omega C_S R_D\right)} \eta \\ &= \frac{1}{\left(1 + \frac{4}{\pi} \omega C_S R_D\right)} \left(0.159 - 0.393 \frac{R_{on}}{R_D} - 0.318 R_D R_{on} \omega^2 C_S^2\right) \end{aligned} \quad (3.44)$$

$$P_{RD} = \eta = 1 - 2.47 \frac{R_{on}}{R_D} - 2 R_D R_{on} \omega^2 C_S^2 \quad (3.45)$$

$$P_{LS} = \frac{\pi^2}{4} \eta = 2.47 - 6.09 \frac{R_{on}}{R_D} - 4.94 R_D R_{on} \omega^2 C_S^2 \quad (3.46)$$

Table 3.1 summarizes the performance comparison of the power amplifiers performed so far in this Chapter.

Class	$\eta, \eta_{RD}$	$\eta_{Pout}$	$\eta_{C_S}$	$P_N$	$P_{RD}$	$P_{LS}$
A	$0.5 \left(1 - \frac{V_k}{V_{DC}}\right)$	–	–	$0.25\eta$	1	1
B	$0.78 \left(1 - \frac{V_k}{V_{DC}}\right)$	–	–	$0.16\eta$	1	1
C	$(0.78 \rightarrow 1) \left(1 - \frac{V_k}{V_{DC}}\right)$	–	–	$0.16\eta \rightarrow 0$	1	1
D,F	$1 - 2 \frac{R_{on}}{R_D}$	$1 - 9.9 \frac{P_{out}}{V_p^2} \cdot R_{on}$	No $C_S$ Allowed	$0.16\eta$	$1.6\eta$	$1.6\eta$

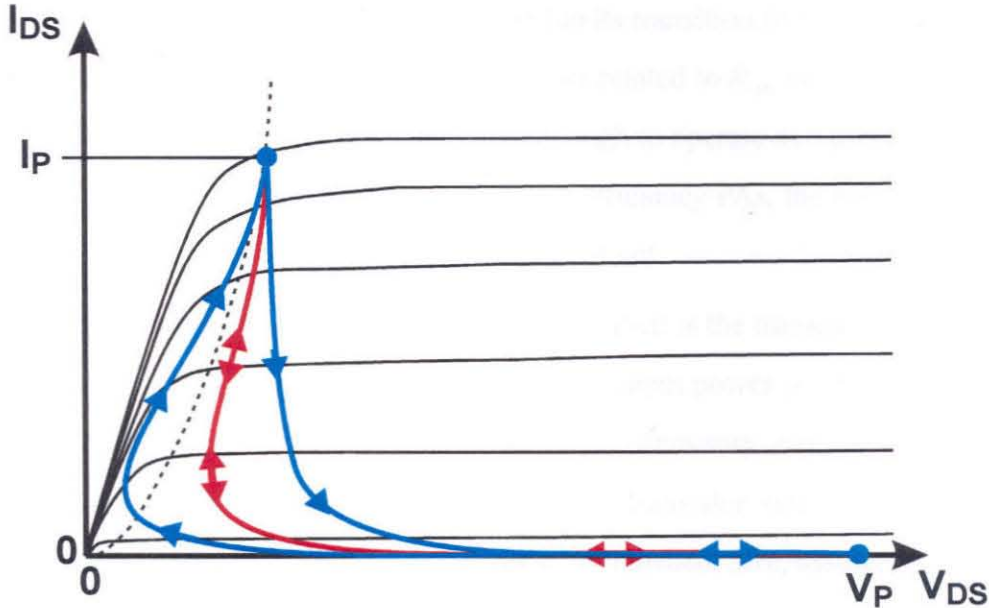
**Table 3.1:** Comparative table of the drain efficiency and several output power capabilities of the most known rf power amplifier classes. The  $\eta_{C_S}$  of E/ $F_{odd}$  is from (3.40), when the best transistor size is used.

E	$1 - 1.4 \frac{R_{on}}{R_D}$	$1 - 30 \frac{P_{out}}{V_p^2} \cdot R_{on}$	$1 - 7.4 R_{on} \omega C_S$	$0.098\eta$	$0.36\eta$	$1.2\eta$
$F^{-1}$	$1 - 2.5 \frac{R_{on}}{R_D}$	$1 - 20 \frac{P_{out}}{V_p^2} \cdot R_{on}$	No $C_S$ Allowed	$0.16\eta$	$\eta$	$2.5\eta$
$E/F_{odd}$	$1 - 2.5 \frac{R_{on}}{R_D}$	$1 - 20 \frac{P_{out}}{V_p^2} \cdot R_{on}$	$1 - 4.7 R_{on} \omega C_S$	$\frac{0.16}{\left(1 + \frac{4}{\pi} \omega C_S R_D\right)} \eta$	$\eta$	$2.5\eta$

**Table 3.1:** Comparative table of the drain efficiency and several output power capabilities of the most known rf power amplifier classes. The  $\eta_{C_S}$  of  $E/F_{odd}$  is from (3.40), when the best transistor size is used.

The derivation of the above equations are presented in Section 3.3.1.3 and in Section 3.3.1.6.

Some typical load lines of the presented switching amplifiers can be seen in the Figure 3.25.



**Figure 3.25:** Illustrative load line of switching amplifiers using NMOS. Red: classes D,  $F^{-1}$ , and  $E/F_{odd}$  with best tuning. Blue: Class E with “optimal” tuning.

In all switching amplifiers, the output power,  $P_{out}$ , is relatively independent of the input power,  $P_{in}$ . The output power is primarily a function of supply dc voltage,  $V_{DC}$ , and

the port-1 impedance of the output network,  $R_D$ , which is presented to the transistor drain or collector. Hence, the higher the input power, the lower the gain,  $G$ , of the switching power amplifier.

On the other hand, the drain efficiency,  $\eta$ , of a switching amplifier changes with input power, as the transistor  $R_{on}$  and the transition time from open to  $R_{on}$  and vice versa is strongly affected by the input power level. In FET power amplifiers, the clear relationship between the input power and  $R_{on}$  brings a hint about scaling factor of the amplifier power efficiency as a function of the input power, which is calculated based on the previously presented simplified  $R_{on}$ /open switch model. The input power increases quadratically with  $V_g - V_t$  and the transistor  $R_{on}$  decreases linearly with the same parameter.

In a very simplified and approximate model, the PAE, which can be calculated based on these relationships, will increase with input power up to its maximum value and then will decrease. The transistor power loss related to its transition from  $R_{on}$  state to open and vice versa is typically smaller than the power loss related to  $R_{on}$  itself while the transistor is conducting, if the transistor has a gain high enough to operate as a power amplifier even under compression. Hence, in the design of high efficiency PAs, the maximum  $P_{in}$  should be large enough to achieve this highest efficiency point.

Another important parameter to optimize in the PAE is the transistor size. As the input power is proportional to the transistor size and the output power is relatively constant, the gain of the power amplifier decreases with larger transitory size. Simultaneously, the transitory  $R_{on}$  varies inversely proportional to the transistor size. Therefore, while the amplifier gain is very high, its PAE increases with transistor size, assuming that its output capacitance is small enough to be tuned with the output network reactances. If we keep increasing the transistor size, the PAE will hit its maximum either due to the loss caused by the transistor output capacitance resonating network or due to the increasing input power. An amplifier limited in its PAE by the first factor is called a *capacitance limited*

*switching amplifier* and one limited by the second factor is called *gain limited switching amplifier*.

It is interesting to note that in a class E power amplifier, if the transistor size can be chosen freely (not constrained by package or by cost) and the amplifier is capacitance limited (like in many HF power amplifiers where gain is almost unlimited due to the high transistor speed relative to the low operating frequency), there is no reason to add any shunt capacitor to the transistor. Any design with shunt capacitor can obtain a higher PAE by eliminating this capacitor and increasing the size of the transistor up to the point, when only the transistor output capacitance will fulfill the necessary shunt capacitance value. (3.31) clearly shows that adding an external shunt capacitor will increase the parameter  $R_{on}\omega C_S$  and degrade the efficiency of a class-E amplifier. More details can be found in Section 3.3.1.4.

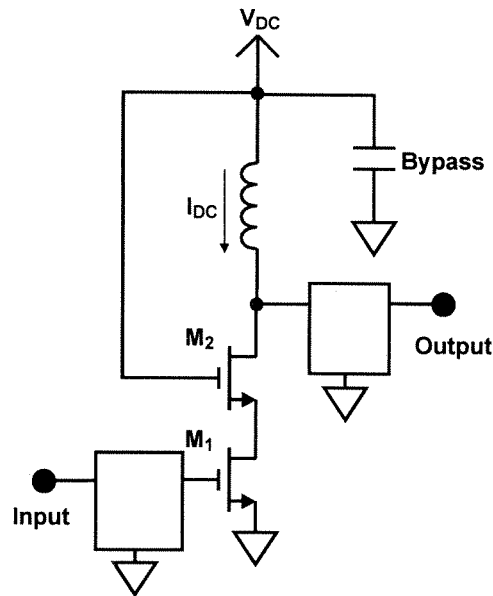
We have seen that the waveform, transistor size and the transistor performance, namely gain and the product  $R_{on}\omega C_S$ , play a strong role in the performance, output power and efficiency, of the designed power amplifier and how strong are their effects quantitatively through plots and normalized comparative equations. Based on this information, a designer can choose the best class and decide every other parameter, such as transistor size, maximum  $P_{in}$ ,  $V_{DC}$ ,  $V_p$ , etc., in order to maximize the power amplifier performance.

### 3.2.3 Cascode

Cascode is a topology which uses multiple transistors in series in which only the lowest transistor, the one with the source or collector connected to the ground, is driven by the input signal. All other transistors have their gate or base ac ground ac. An example with two NMOS transistors can be seen in Figure 3.26. Another way to understand this topology is to see the first transistor as a common source or emitter stage and the second and all other transistors as common gate or base stages. The dc bias of the upper transistor in this



case should be higher than the threshold voltage plus knee voltage of the lower transistor in order to allow the upper transistor to have gain.



**Figure 3.26:** Illustrative example of a cascode topology using two NMOS transistors. The boxes are input and output impedance matchings networks.

Cascode has an advantage over a single transistor topology as it supports higher voltages at the drain or collector before breakdown, as the applied voltage is split by several transistors [41]. Simultaneously, it can multiply the combined active device gain by the number of transistors, as the input power required is the same as in the case of a single device, but the output power is multiplied by the number of the transistors. For a given input power, the drain or collector current of a cascode structure is the same as that of a single transistor, but the drain or collector voltage swing is multiplied by the number of transistors stacked in series by increasing the load impedance by the same ratio. Hence, the output power and power gain are multiplied by the number of the stacked transistors.

Also, as a secondary effect, it provides even higher gain and frequency response, as the Miller capacitive negative feedback from source or collector to the gate or base through drain-gate or collector-base capacitor is significantly reduced. In cascode, there is

no direct path from the drain or collector of the output transistor to the gate or base of the input transistor.

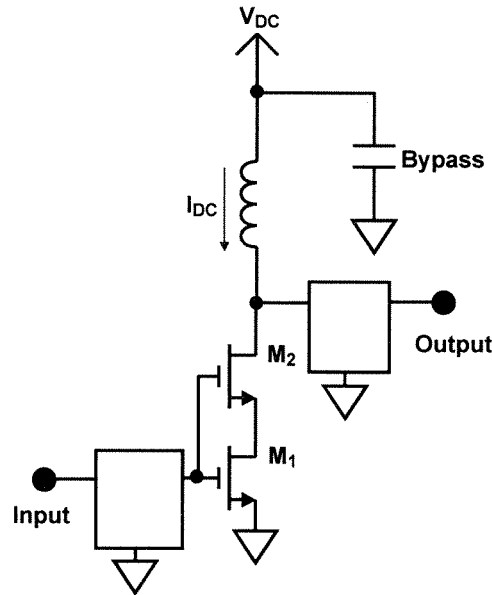
In some processes, when the drain or collector to bulk junction breakdown voltage is significantly higher than the drain-source or collector-base and gate-source or base-emitter breakdown voltages, cascode is useful to increase the maximum voltage swing at the transistor drain or collector enhancing the output power even under a given limited load impedance.

A negative effect of cascode or any topology that stacks several transistors in series is the increase of the total active device  $V_{knee}$ ,  $R_{on}$  and  $V_{on}$ . These effects will significantly increase the power loss of the amplifier, if the power amplifier is operated in a switching mode. Even the power amplifier operation is linear A, AB, or B, and their power efficiency and output power are jeopardized by the higher combined  $V_k$  of the active device will.

### 3.2.4 Series Combining

Another way to enhance the output power of a power amplifier under limited load impedance is to stack two or more transistors in series as shown by Figure 3.27 and drive all of them with the same ac input signal. This method, similar to cascode, also can be applied to enhance the  $P_{out}$  if the bulk junction breakdown voltage is significantly higher than the drain to source or drain to gate breakdown voltages.

Unlike cascode, in this configuration we have similar devices combining the power, hence the power gain remains the same as that of a single transistor. As the outputs are combined in series, the power is multiplied by the number of transistors, while keeping the same load impedance. The input can be associated in parallel, as in Figure 3.27, or in series with the use of a transformer.



**Figure 3.27:** Illustrative example of a series combining topology using two NMOS transistors. The boxes are input and output impedance matching networks.

### 3.3 Output Network

The output passive network, besides the active device, plays a dominant role in the performance of a rf power amplifier. It can perform one or more of the three tasks, namely, harmonic signal control, impedance transformation, and dc current feed. This can be seen in a simplified block diagram of the power amplifier Figure 3.1.

Its influence in the power efficiency is significant as the power, which is transmitted through it, is the high level output power. It also performs the transistor drain or collector waveform shaping, which determines the transistor power efficiency.

In a fully-integrated circuit, especially one using a silicon substrate, the power loss in this passive structure is prohibitively high, preventing truly fully-integrated watt-level power amplifiers from being reported before this work. Detailed analysis of this loss will be performed in Chapter 4. Concurrently, the quality of the output signal, *i.e.*, low harmonic content, depends in large part on the filtering characteristics of this network.

The simplest way to analyze a power amplifier in order to analytically calculate its output power and power efficiency is by calculating the output network impedance presented to the transistor drain or collector at the fundamental frequency and at each overtone, compute the drain or collector current and voltage waveforms based on these impedances, duty cycle, transistor  $R_{on}$ , and supply voltage, decompose the current and voltage waveforms into each harmonic, use these signals in the frequency domain as an input signal for the output network, and finally calculate the signal at the load independently for each harmonic. This last step can easily be accomplished as the output network is an LTI (linear time invariant) network [42].

It is important to mention that the transistor output parasitic capacitance should always be included in the output network in a power amplifier analysis in order to simplify the study.

Recently, general analytical solutions to find the current and voltage waveforms of a switching amplifier for any given values of the output network harmonic impedances presented to the transistor drain or collector have been discovered [42]. But in this work we will utilize the traditional methodology [39] as just described, which is easier to be understood intuitively without resorting to too much math. Efficiency can be calculated once switch voltage and current waveforms are found with or without analytical solutions.

### 3.3.1 Harmonic Control

The harmonic control function of the output network of a rf power amplifier has two main objectives, namely waveshaping of the drain or collector signal and filtering of the harmonics of the output signals. The first reduces the transistor power loss, as extensively covered in Section 3.2, and is used mainly in switching power amplifiers and the second is necessary to reduce the harmonic content of the output signal generated by the transistor non-linearity, in order to fulfill today's restrict wireless communication specifications.

Traditional transconductance power amplifiers are classified based on the conduction angle, as defined in Section 3.2. On the other hand, the fundamental way to classify switching amplifiers relies solely on how the harmonic impedances seen by the switch are terminated and it is independent of what topology is being used to provide these harmonic impedances. These impedance terminations, duty cycle, and scaling factor for dc bias level define completely the voltage and current waveforms at the switch. From these waveforms, the expected output power and drain efficiency may be easily calculated [43].

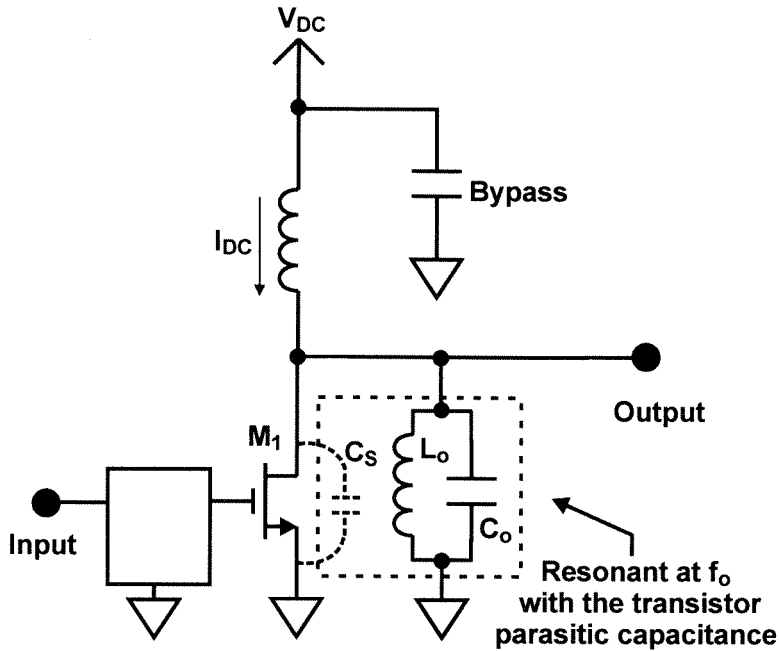
The best known ways of performing these harmonic related impedance terminations are described in the following sub-sections.

### **3.3.1.1 Classes A, B, AB, and C Transconductance Amplifiers**

The classes A, AB, B, and C are the simplest and easiest to be analyzed. As described in Section 3.2.1, in these classes of power amplifiers, the transistors are current sources with different current waveforms depending on the amplifier class. In these amplifiers, the drain or collector voltage waveform is always forced to be a sinusoid regardless of the current waveform, as a result of terminating these nodes without making a short circuit at all overtones. The current waveform will be defined by the conduction angle and the transistor transfer function as described in Section 3.2.1. Typical waveforms can be seen in Figure 3.8.

The filtering function can easily be accomplished by a parallel LC resonant circuit at the fundamental frequency and connected in shunt to the transistor and the load as can be seen in Figure 3.28.

Keeping the drain or collector voltage as high as possible up to the breakdown limit of the transistor, and using the highest possible drain or collector load resistance gives the highest gain and PAE in a power amplifier. The output power in an amplifier is proportional to its drain or collector voltage and current at the fundamental frequency. Also, in a transconductance amplifier, only the drain or collector current is directly related to the input power. Therefore, the higher the drain or collector voltage, the higher will be



**Figure 3.28:** Illustrative example of a typical class A, AB, B, or C rf power amplifier.

the output power and PAE of the amplifier. This condition can be provided by designing the output network so as to present a load resistance adjusted to make drain or collector voltage always as close as possible to the breakdown limit. It is important to note that this procedure differs from the common method where the output network of the amplifier is designed to provide the conjugate match to the load. Although conjugate matching is valid and useful for small signal amplifiers, it jeopardizes the power efficiency of any power amplifier.

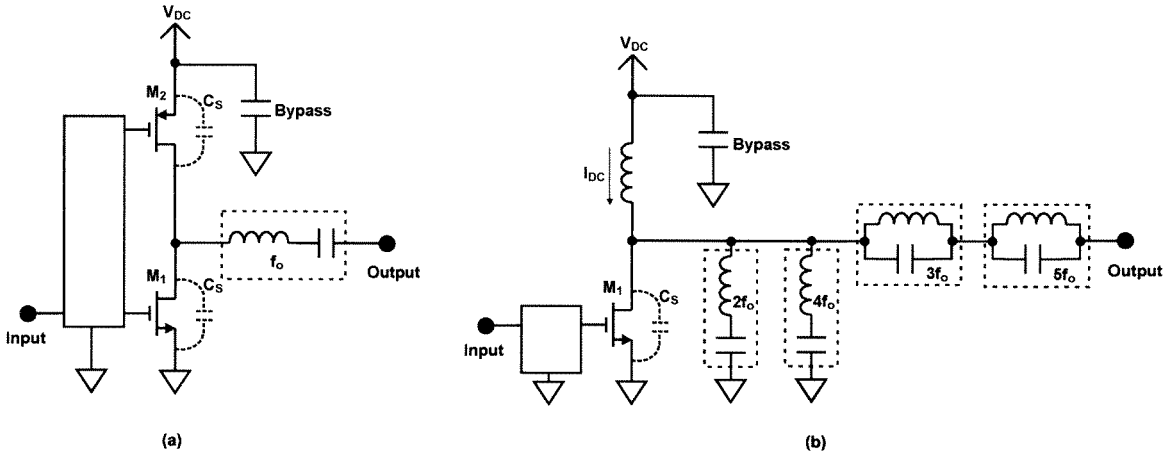
As extensively described in Section 3.2.1, the performance of amplifiers in these classes improves with larger transistor size and its limitation is the  $Q$  of the output network resonating the transistor parasitic capacitance and the bandwidth requirement for the amplifier.

In a silicon integrated circuit, due to the extremely low inductor quality factor,  $Q$ , a significant part of the output power is lost on this resonant inductor. Under this condition, the transistor size will be severely limited as a larger transistor with higher output capacitance will require a low impedance inductor resulting in higher power loss. The

peak PAE (PAE at maximum output power) of the classes A, AB, B, and C will increase with transistor size up to certain point as the power gain increases with it and the PAE will decrease beyond this point as the shunt inductor loss will be dominant.

### 3.3.1.2 Class-D (Class-F) ZCS Amplifier

Class-D and F amplifiers are ZCS amplifiers and these classes are similar as described in Section 3.2.2. The most common practical designs are shown in Figure 3.29. These examples assume that the transistor parasitic output capacitances,  $C_S$ , are small enough to be neglected.



**Figure 3.29:** a) Illustrative example of a typical push-pull class-D power amplifier, b) Typical Class-F power amplifier controlling up to 5<sup>th</sup> overtone.

In a class D or F amplifier, the harmonic impedances seen by the switch are real at fundamental frequency, zero at even overtones and infinite at odd overtones. This results in switch voltage and current waveforms as shown by Figure 3.21.

Although any output network which provides correct impedances at each harmonic frequency to the switch can be used to construct a class-D or F amplifier, we illustrate these networks below using the most common and simplest topology, as can be seen in Figure 3.29a), class D amplifier. This most common topology for a class-D power amplifier is a push-pull configuration, where two switches are connected in series between

the dc supply and the ground and their center point connected to the load through a series LC circuit resonating at the fundamental frequency as can be seen in Figure 3.22 a).

We can compose the current and voltage waveforms and find the harmonic impedances at the switches for the ideal class-D amplifiers as follows:

- As one of the switches are connected either to  $V_{DC}$  or  $GND$ , the voltage at switch node will be square, being either  $V_{DC}$  or  $GND$ .

- As we have a series resonant filter in series with the load, the current through it will be a sine wave at fundamental frequency and its amplitude can be calculated by dividing the harmonic component of the voltage waveform at fundamental frequency by the load resistance.

- The current through the switches will be zero when they are open and half sinewave while closed as they are connected in series with the load conducting sinewave current.

- The waveform of the current through the switch is a half sine wave, which contains only signals at fundamental frequency and at even overtones. The waveform of the voltage across the switch is square, which contains signals only at fundamental frequency and at odd overtones. Hence to allow the existence of these listed voltage and current overtones, the impedance seen by each one of the switch must be real at the fundamental frequency, zero at even overtones, and infinite at odd overtones.

Using the voltage and current waveforms as described above, we can compute the output power and power efficiency as follows:

$$v_D(\theta) = \begin{cases} 0 & 0 \leq \theta < \pi \\ V_D & \pi \leq \theta < 2\pi \end{cases} \quad (3.47)$$

$$i_D(\theta) = \begin{cases} I_p \sin(\theta) & 0 \leq \theta < \pi \\ 0 & \pi \leq \theta < 2\pi \end{cases} \quad (3.48)$$



$$\begin{aligned}
\eta &= 1 - \frac{P_{loss}}{P_{DC}} = 1 - \frac{\frac{1}{2\pi} \int_0^\pi i_D(\theta)^2 R_{on} d\theta}{I_{DC} \cdot V_{DC}} \\
&= 1 - \frac{\frac{I_p^2 R_{on}}{2\pi} \int_0^\pi \sin^2(\theta) d\theta}{\frac{I_p}{\pi} \cdot \frac{V_p}{2}} = 1 - 2 \frac{R_{on}}{R_D}
\end{aligned} \tag{3.49}$$

where

$$I_p = 2I_o = 2 \frac{V_o}{R_D} = 2 \frac{\frac{1}{2} \cdot \frac{4}{\pi} V_p}{R_D} = \frac{4}{\pi} \frac{V_p}{R_D} \tag{3.50}$$

and  $i_D(\theta)$  is drain current,  $P_{loss}$  is the power loss in the transistor due to  $R_{on}$ ,  $V_o$  is the amplitude of fundamental frequency component of the drain voltage, and  $I_o$  is the amplitude of the fundamental frequency component of the drain current.

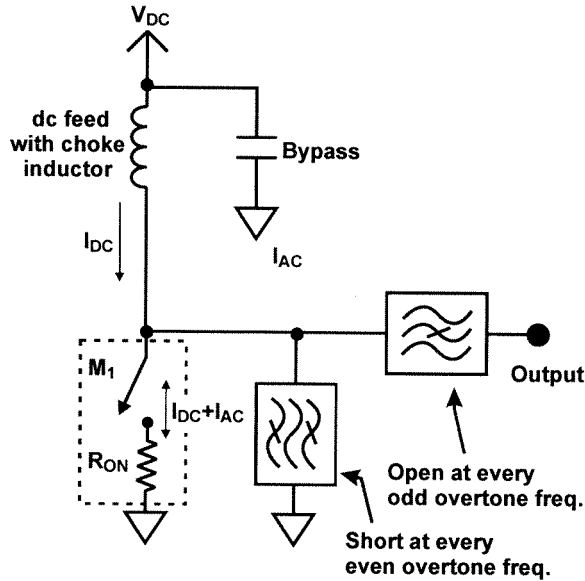
$$P_{out} = P_{DC} - P_{loss} = \frac{I_p}{\pi} \cdot \frac{V_p}{2} - \frac{I_p^2 R_{on}}{4} = \frac{I_p V_p}{2\pi} \cdot \eta \tag{3.51}$$

From (3.50), (3.51) and  $V_p = 2V_{DC}$ ,  $P_N$ ,  $P_{RD}$ , and  $P_{LS}$  can easily be calculated.

The above equations are valid only if the operating frequency is low enough relative to the transistor speed and transistor size small that the transistor output capacitance,  $C_S$ , is negligible. Further details about class-D power amplifiers may be found in several textbooks on power converters [22].

Class-F amplifiers are single ended versions of the class-D amplifiers and they are normally used in applications at higher frequencies. We can compose the waveforms and obtain necessary harmonic impedances for the class-F amplifiers based on the schematic of the ideal implementation shown in Figure 3.30. In this schematic we have a switch connected to the dc supply through a choke and an output network connected between the

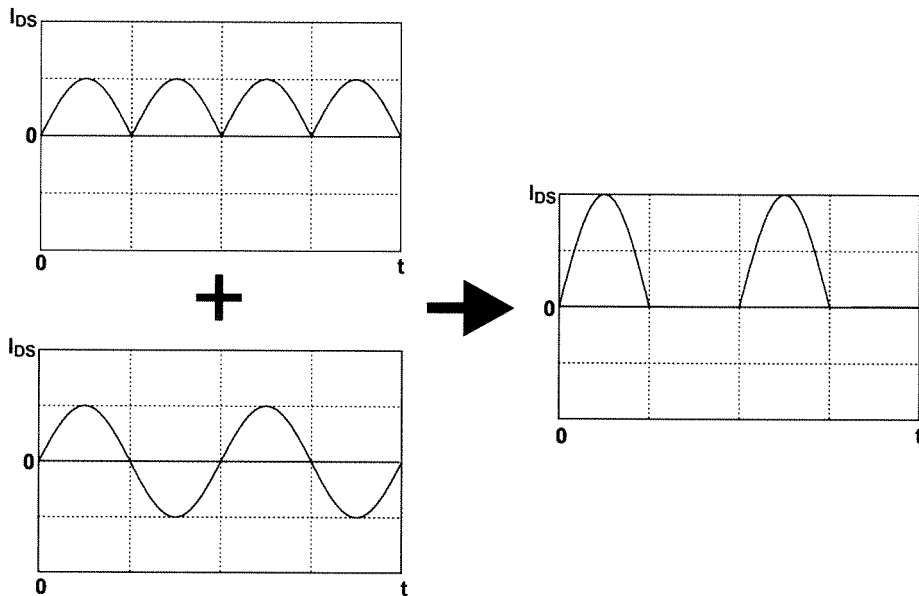
switch and the load. The output network provides the specific impedances to the switch at each harmonic as described below:



**Figure 3.30:** Block diagram of an ideal class-F switching power amplifier.

- While the switch is closed, the voltage across the output network is zero.
- The voltage waveform is forced to symmetry as all the even overtone components of the voltage waveform and impedances seen by the switch at the even overtones are zero. Hence, the voltage waveform is a square wave, as the lower half of the wave is a constant value forced by the closed switch and the voltage waveform must be symmetric relative to its average dc value and this symmetry makes the upper half of the wave to be a constant value also.
- The amplitude of the voltage square wave at the switch will be twice  $V_{DC}$ , as the area below  $V_{DC}$  and above  $V_{DC}$  of the voltage waveform at the switch must be the same to keep the current through the choke constant.
- The switch current waveform will be a half sinusoid as it is the sum of a fundamental frequency sinusoid and all even overtones. While the switch is open, the current is zero, which means that while the fundamental frequency signal is in its negative half cycle, the sum of all even overtones must compose a positive half sinusoid in order for the sum to be

zero. The sum of even overtones will repeat the positive half sinusoid in the other half cycle as they do not contain any odd overtone. This in addition to the positive half sinusoid of the fundamental frequency signal will compose a half sinusoid with twice the fundamental amplitude. This completes the half sinusoid current through the switch. Furthermore, the fundamental frequency current sinusoid is in phase with switching pattern, because the load is real valued at fundamental frequency. There are no odd overtone currents, as the switch sees infinite impedance at these frequencies. These waveforms can be seen in Figure 3.31.



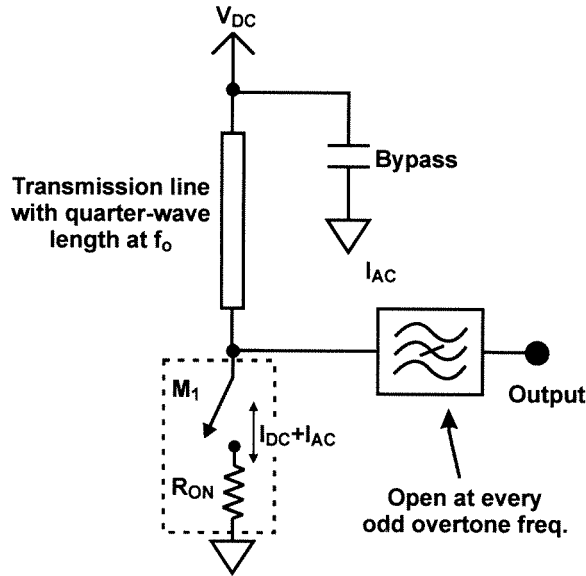
**Figure 3.31:** Current at the fundamental frequency with currents at the overtone frequencies results in half sinusoidal waveform.

The current amplitude through the switch at the fundamental frequency, under conditions described above, can be computed by dividing the fundamental frequency component of the voltage square wave by the load resistance. The total current through the switch will be a half sinusoid with twice the amplitude of the current at fundamental.

As can be seen above, the harmonic impedances involved, voltage and current waveforms, output power, and power loss is exactly the same as calculated for the class-D

amplifiers. Class-D amplifiers achieve same tuning as class-F amplifiers by their symmetry.

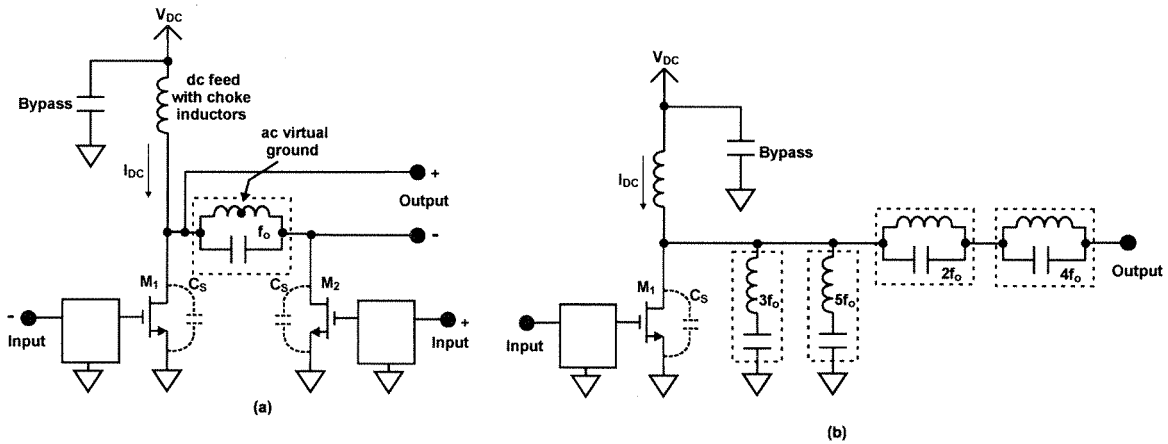
Another compact way to short circuit the even overtones in a class-F amplifier at high frequencies is by the use of a quarter-wavelength transmission line to connect the transistor to the dc voltage power supply. Although a series resonant circuit at fundamental frequency connected in series with the load completes the circuit providing open at every odd overtones, its implementation in a practical circuit is very difficult at microwave frequencies. This can be seen in Figure 3.32.



**Figure 3.32:** Current at the fundamental frequency with currents at the overtone frequencies result in half sinusoidal waveform.

### 3.3.1.3 Class- $D^{-1}$ (Class- $F^{-1}$ ) ZVS Amplifier

The class  $D^{-1}$  or  $F^{-1}$  (inverse F) are duals of previously presented class D or F. Their currents and voltages are complementary to the previous classes. Figure 3.33 shows typical implementation of these classes in single ended and in push-pull configuration [40]. In these implementations, the transistor output capacitance,  $C_S$ , is assumed to be negligible.



**Figure 3.33:** a) Illustrative example of a typical push-pull class-D<sup>-1</sup> power amplifier, b) Typical Class-F<sup>-1</sup> power amplifier controlling up to 5<sup>th</sup> overtone.

The push-pull configuration has two switches connected to the supply through a choke and a parallel LC circuit resonant at the fundamental frequency connected between the switches and parallel to the load, as shown by Figure 3.24:

We can compose the current and voltage waveforms and find the harmonic impedances at the switches for the ideal push-pull class D<sup>-1</sup> or F<sup>-1</sup> amplifiers as follows:

- While the switch is open, the current through it is zero. When it is closed the current through it will be constant and the same of total dc current drawn by the chokes as the closed switch is the only pass for the current to ground. Hence the currents through the switch and through the output network and load are square waves.

- As the parallel LC circuit is short for all overtones, the voltage waveform across the output network will be a sinusoid. Hence, when one switch is closed maintaining zero voltage at one node of the output network, the voltage at the other node where the other switch is connected will be a half sinusoid as can be seen in Figure 3.23.

- By symmetry of the topology, there will be a virtual ac ground in the center of the output network connected between the switches, as seen in Figure 3.33, for all odd harmonics including the signal at the fundamental frequency. Hence, the impedance seen

by the switch at the fundamental frequency will be the load resistance divided by two and at odd overtones, zero.

- By symmetry, there will be no current at even overtones through the output network or load. Hence the impedance seen by the switch at the odd overtones will be open.

- As the area of the voltage waveform at the switch below the supply voltage and above the supply voltage must be the same in order to maintain the constant current through the choke, the peak voltage of the half sinusoid at the switch must be  $\pi$  times  $V_{DC}$ .

- By dividing the voltage amplitude by load resistance, we have the amplitude of the current through the switch at the fundamental frequency. From this, we can compute the amplitude of the square wave current through the switch.

We can implement the single ended class-F<sup>-1</sup> circuit by providing the same impedances to the overtones using several resonant filters as can be seen in Figure 3.33 b).

Based on the waveforms studied above, we can compute the output power and efficiency of the single ended class D<sup>-1</sup> or F<sup>-1</sup> as follows:

$$i_D(\theta) = \begin{cases} I_p & 0 \leq \theta < \pi \\ 0 & \pi \leq \theta < 2\pi \end{cases} \quad (3.52)$$

$$\begin{aligned} \eta &= 1 - \frac{P_{loss}}{P_{DC}} = 1 - \frac{\frac{1}{2\pi} \int_0^\pi i_D(\theta)^2 R_{on} d\theta}{I_{DC} \cdot V_{DC}} \\ &= 1 - \frac{\frac{I_p^2 R_{on}}{2}}{\frac{I_p}{2} \cdot \frac{V_p}{\pi}} = 1 - \frac{\pi^2 R_{on}}{4 R_D} = 1 - 2.467 \frac{R_{on}}{R_D} \end{aligned} \quad (3.53)$$

where:

$$I_p = 2 \frac{\pi}{4} I_o = 2 \frac{\pi}{4} \frac{V_o}{R_D} = \frac{\pi V_p}{4 R_D} \quad (3.54)$$

and where  $i_D(\theta)$  is drain current,  $P_{loss}$  is the power loss in the transistor due to  $R_{on}$ ,  $V_o$  is the amplitude of fundamental frequency component of the drain voltage, and  $I_o$  is the amplitude of the fundamental frequency component of the drain current.

The output power can be calculated as the difference between the consumed dc power and the power loss at the switch as follows:

$$P_{out} = P_{DC} - P_{loss} = I_{DC} \cdot V_{DC} - P_{loss} = \frac{I_p}{2} \cdot \frac{V_p}{\pi} - \frac{I_p^2 R_{on}}{2} = \frac{I_p V_p}{2\pi} \cdot \eta \quad (3.55)$$

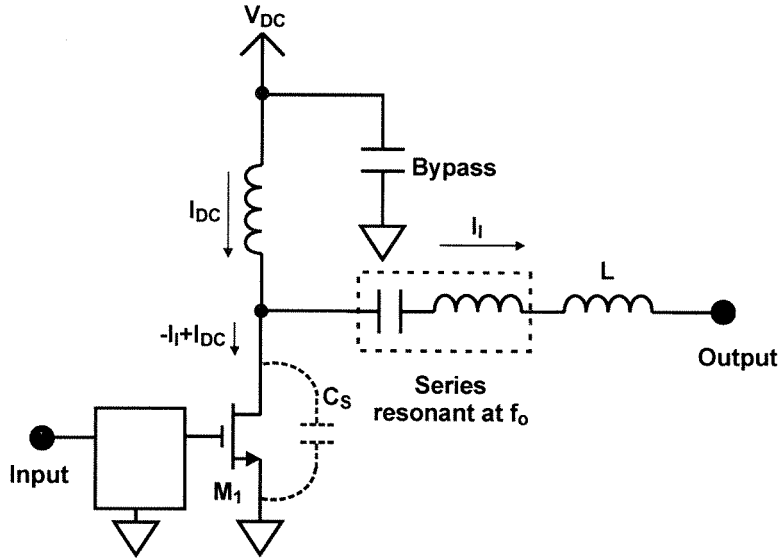
From (3.54), (3.55), and  $V_p = \pi V_{DC}$ ,  $P_N$ ,  $P_{RD}$ , and  $P_{LS}$  can easily be calculated.

The above equations are valid only if the operating frequency is low enough relative to the transistor speed allowing the use of a transistor with negligible output capacitance,  $C_S$  as seen in Figure 3.33.

#### 3.3.1.4 Class-E ZVS Amplifier

Class-E amplifier was first introduced by Ewing in 1969 [36]. It is a ZVS switching amplifier with significantly lower output power and power efficiency compared to the previously presented D,  $D^{-1}$ , F, or  $F^{-1}$  amplifiers, when using the same devices with the same size as can be seen in the comparative Table 3.1. If the transistor size is not limited, the best efficiency possible in class-E amplifiers is higher than that of other classes as, unlike in other topologies, the transistor output capacitance,  $C_S$ , can be used as a part of the circuit topology. The relative lower performance of class-E amplifiers is due to its very highly peaked voltage and current waveforms. The impedance seen by the switch at the fundamental frequency is inductive and resistive, while at all overtones it is capacitive.

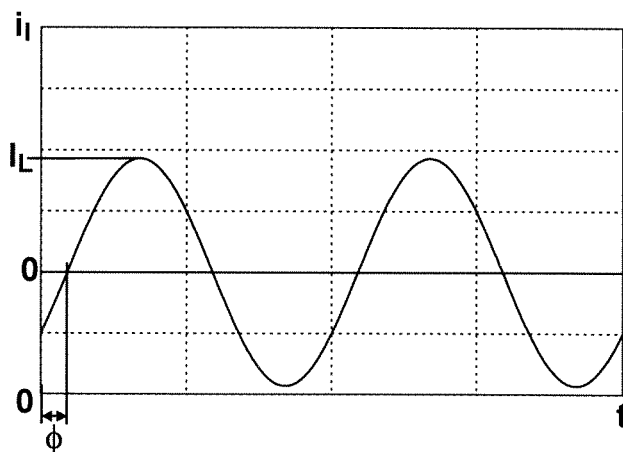
The basic topology of the class-E amplifier can be seen in Figure 3.34. and its voltage and current waveforms can be seen in Figure 3.21 b). Class-E amplifiers have a switch connected to the supply through a choke, an output network with a capacitor shunt to the switch, and a series LC circuit resonant at the fundamental frequency connected between the switch and another inductor connected in series with the load.



**Figure 3.34:** Illustrative example of a class-E power amplifier.

We can study the waveforms and performance of the class-E amplifier using basic circuit analysis:

- The current through the load,  $i_L$ , is a sinusoid at the fundamental frequency with unknown amplitude  $I_L$  and unknown phase  $\phi$ , as the LC circuit in series with the load is open for all overtones. The resulting  $i_L$  waveform is depicted in Figure 3.35.

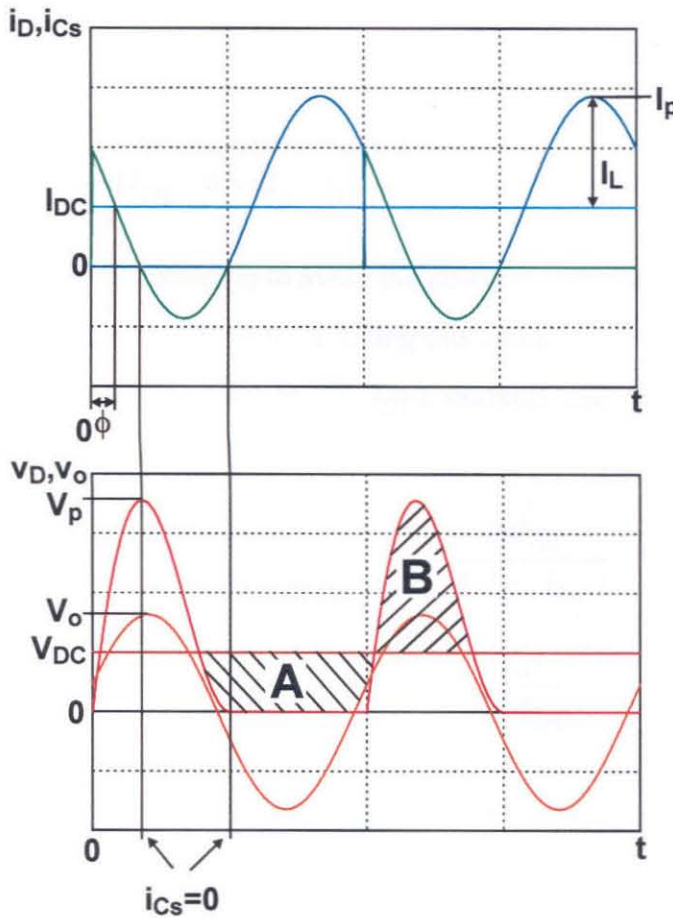


**Figure 3.35:** Illustrative  $i_L(\theta)$  vs.  $t$  of a class-E amplifier.

$$i_L(\theta) = I_L \sin(\theta - \phi) \quad (3.56)$$



- As we have a constant current through the choke,  $I_{DC}$ , by Kirchof law, the current through the switch,  $i_D$ , when it is closed,  $\pi \leq \theta < 2\pi$ , is negative sinusoid,  $-i_L$ , plus this dc current from the choke. The current through the shunt capacitor,  $C_S$ , during this period is zero as the voltage is hold zero by the switch, as can be seen in Figure 3.36.



**Figure 3.36:** Illustrative example several waveforms of a class-E power amplifier. Blue:  $i_D$ , Green:  $i_{CS}$ , Light Blue:  $I_{DC}$ , Red:  $V_D$ , Orange:  $V_o$ , Brown:  $V_{DC}$ .

From Figure 3.36, drain current can be computed as follows:

$$i_D(\theta) = \begin{cases} 0 & 0 \leq \theta < \pi \\ I_{DC} - (I_p - I_{DC}) \sin(\theta - \phi) & \pi \leq \theta < 2\pi \end{cases} \quad (3.57)$$

where

$$I_p = I_{DC} + I_l \quad (3.58)$$

- When the switch is open, the sinusoidal plus “dc” current should conduct entirely through the shunt capacitor. The voltage on the capacitor, which is the voltage on the open switch,  $v_D$ , can be obtained by integrating  $i_l + I_{DC}$  through the capacitor,  $C_S$ .

$$\begin{aligned} v_D(\theta) &= \frac{1}{\omega C_S} \int_0^\theta i_D(\theta) d\theta = \frac{1}{\omega C_S} \int_0^\theta (I_{DC} - (I_p - I_{DC}) \sin(\theta - \phi)) d\theta \\ &= \frac{1}{\omega C_S} [I_{DC} \cdot \theta + (I_p - I_{DC})(\cos(\theta - \phi) - \cos\phi)] \end{aligned} \quad (3.59)$$

- To fulfill the ZVS condition to avoid the power loss caused by charge and discharge of  $C_S$ ,  $v_D$  should return to zero at  $\theta = \pi$ . Using this condition, it is possible to calculate the ratio between these dc,  $I_{DC}$ , and ac,  $(I_p - I_{DC})$ , currents and the phase of the ac current relative to the switch cycle,  $\phi$ .

$$v_D(2\pi) = 0 \rightarrow \cos\phi = \frac{\pi I_{DC}}{2(I_p - I_{DC})} \quad (3.60)$$

$$i_D(0) = 0 \rightarrow \sin\phi = \frac{I_{DC}}{I_p - I_{DC}} \quad (3.61)$$

$$\phi = \text{atan}\left(\frac{2}{\pi}\right) = 0.5669 \quad (3.62)$$

$$I_p = \frac{2 + \sqrt{\pi^2 + 4}}{2} I_{DC} = 2.862 I_{DC} \quad (3.63)$$

-  $V_p$  can be calculated as a function of  $I_{DC}$  by finding the value of  $v_D$ , (3.59), at  $\theta = 2\phi$  when  $i_D$  (derivative of  $v_D$ ) is zero as indicated in Figure 3.36.

$$V_p = v_D(2\phi) = \frac{2\phi}{\omega C_S} I_{DC} \quad (3.64)$$

-  $V_{DC}$  can be calculated as a function of  $I_{DC}$  by averaging  $v_D$ , (3.59), over a period. The areas A and B indicated in Figure 3.36 should be the same in a steady-state condition.

$$V_{DC} = \frac{1}{2\pi} \int_0^{2\pi} v_D(\theta) d\theta = \frac{1}{\pi \omega C_S} I_{DC} \quad (3.65)$$

- From (3.64) and (3.65) we have

$$V_p = 2\pi \phi V_{DC} = 3.563 V_{DC} \quad (3.66)$$

- By calculating the fundamental frequency component of the voltage waveform,  $v_o$ , using Fourier transform on (3.59), and using the current through the load,  $i_l$ , we can calculate the required value of the load resistance,  $R_D$ , and series reactance,  $\omega L$ .

$$\begin{aligned} v_o(\theta) &= \left[ \frac{1}{\pi} \int_0^{2\pi} v_D(\theta) \cos \theta d\theta \right] \cos \theta + \left[ \frac{1}{\pi} \int_0^{2\pi} v_D(\theta) \sin \theta d\theta \right] \sin \theta \\ &= \left( \frac{2}{\pi} - \frac{\pi}{4} \right) \cos \theta - \frac{1}{2} \sin \theta \\ &= \left( \frac{4 - \pi^2}{4} \cos(\theta - \phi) - \frac{4}{\pi} \sin(\theta - \phi) \right) \frac{1}{\sqrt{\pi^2 + 4}} \frac{I_{DC}}{\omega C_S} \end{aligned} \quad (3.67)$$

$$i_l(\theta) = -(I_p - I_{DC}) \sin(\theta - \phi) = -\frac{\sqrt{\pi^2 + 4}}{2} I_{DC} \sin(\theta - \phi) \quad (3.68)$$

$$\frac{v_o(\theta)}{i_l(\theta)} = R_D + \omega L \cot(\theta - \phi) = \left( \frac{8}{\pi(\pi^2 + 4)} + \frac{\pi^2 - 4}{2(\pi^2 + 4)} \right) \frac{1}{\omega C_S} \quad (3.69)$$

$$R_D = \frac{8}{\pi(\pi^2 + 4)} \frac{1}{\omega C_S} = 0.1836 \frac{1}{\omega C_S} \quad (3.70)$$

$$\omega L = \frac{\pi^2 - 4}{2(\pi^2 + 4)} \frac{1}{\omega C_S} = \frac{\pi(\pi^2 - 4)}{16} R_D = 1.153 R_D \quad (3.71)$$

- From (3.65) and (3.70) we can calculate the ratio between  $V_{DC}$  and  $I_{DC}$  as a function of  $R_D$ :

$$\frac{V_{DC}}{I_{DC}} = \frac{\pi^2 + 4}{8} R_D = 1.734 R_D \quad (3.72)$$

Based on the waveforms determined as above, we can calculate the approximate power efficiency and the output power using (3.57), (3.63), and (3.72) as follows:

$$\begin{aligned}
 \eta &= 1 - \frac{P_{loss}}{P_{DC}} = 1 - \frac{\frac{1}{2\pi} \int_0^{2\pi} i_D(\theta)^2 R_{on} d\theta}{I_{DC} \cdot V_{DC}} \\
 &= 1 - \frac{\frac{I_{DC}^2 R_{on}}{4\pi} \int_0^{2\pi} \left(2 - \sqrt{\pi^2 + 4} \sin(\theta - \phi)\right)^2 d\theta}{\frac{\pi^2 + 4}{8} I_{DC}^2 R_D} \\
 &= 1 - \frac{\pi^2 + 28}{2(\pi^2 + 4)} \frac{R_{on}}{R_D} = 1 - 1.365 \frac{R_{on}}{R_D}
 \end{aligned} \tag{3.73}$$

where  $P_{loss}$  is the power loss in the transistor due to  $R_{on}$  and  $P_{DC}$  is the dc power consumed by the amplifier.

Using (3.70) we can rearrange (3.73) to have  $\eta$  exclusively as a function of the transistor parameter  $R_{on}\omega C_S$  when the transistor size is maximized to eliminate completely the use of an external capacitor connected in parallel to  $C_S$ . This transistor maximization is possible if it is not gain limited, as explained in Section 3.2.2.

$$\eta = 1 - \frac{\pi(\pi^2 + 28)}{16} \cdot R_{on}\omega C_S = 1 - 7.44 \cdot R_{on}\omega C_S \tag{3.74}$$

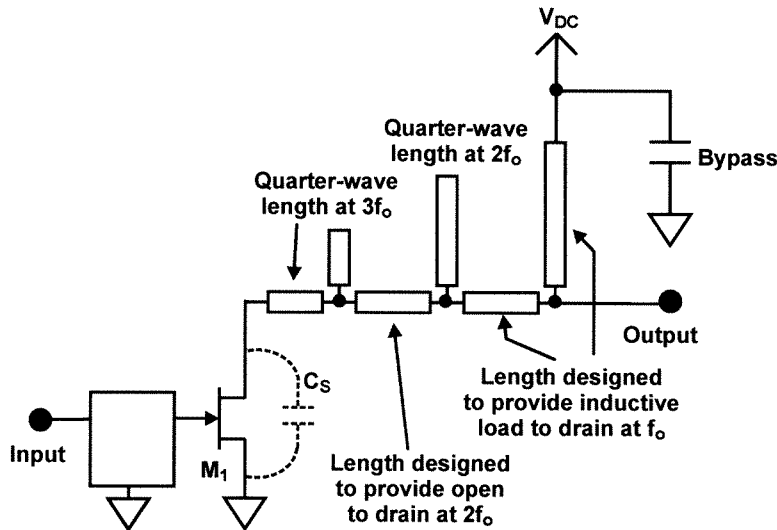
From (3.63), (3.66), and (3.73) we can calculate  $P_{out}$  as a function of  $I_p$ ,  $V_p$ , and  $\eta$ :

$$P_{out} = P_{DC} - P_{loss} = \frac{2I_p}{2 + \sqrt{\pi^2 + 4}} \cdot \frac{V_p}{2\pi\phi} \cdot \eta = 0.0981 I_p V_p \eta \tag{3.75}$$

From (3.63), (3.66), (3.72) and (3.75),  $P_N$ ,  $P_{RD}$ , and  $P_{LS}$  can easily be calculated.

At microwave frequencies, Class E amplifiers can be implemented using transmission lines [45]. But a compact implementation, such as transmission-line class F amplifier, where a single stub controls every even overtone matching, has not yet been found for the

class E. Unfortunately, a transmission-line implementation of this class requires individually tuned shunt open stubs for each harmonic, which makes this implementation unpractical. As can be seen in Figure 3.37, the shunt stub closest to the transistor provides the open for the highest overtone, 3<sup>rd</sup> in this example, the second from the transistor provides open for the second highest overtone and so on until the last stub closest to the load provides inductive impedance at the fundamental frequency. The capacitance parallel to transistor should be provided by choosing the largest transistor possible, which provides correct capacitive reactance at overtones for the class-E operation.



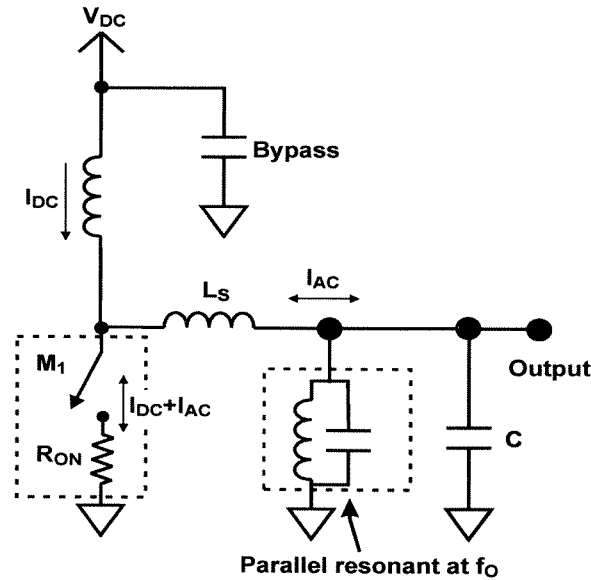
**Figure 3.37:** A transmission line class-E amplifier with three harmonics controlled.

### 3.3.1.5 Class- $E^{-1}$ ZCS Amplifier

Class  $E^{-1}$  is the dual of the class E amplifier wherein the current and voltage are interchanged. An illustrative example can be seen in Figure 3.38 [22]. But it is not practical, as it provides the same theoretical performance of the class E if the transistor output capacitance is ignored, but have a lower efficiency in practice with transistor output capacitance.

### 3.3.1.6 $E/F_{xx}$ ZVS Amplifier Family

A new set of classes of amplifiers has recently been developed at Caltech [21], many them presenting performance similar to class- $F^{-1}$  amplifiers with the simplicity of the class-E



**Figure 3.38:** Example of a class  $E^{-1}$  power amplifier.  $L_S$  is not a choke. It is part of the harmonic controlling network.

amplifiers, yet allows to have a  $C_S$  larger than what is permissible in a class E amplifier. These classes are denominated  $E/F_x$  and the set, family E/F.

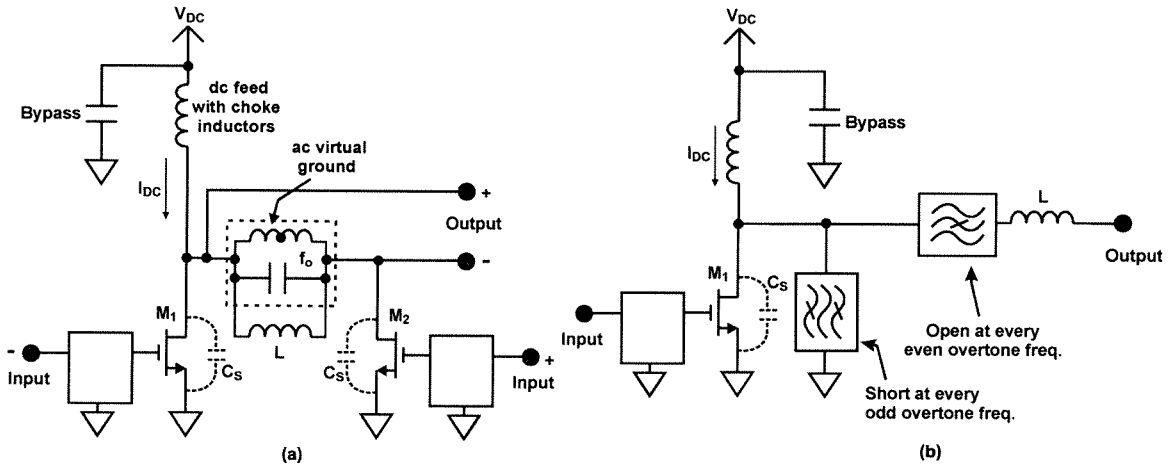
The switch in any amplifier belonging to this family will see inductive impedance at the fundamental frequency as in class E amplifiers and any combination of impedances of class E or Class  $F^{-1}$  for the overtones. Table 3.2 shows some examples of class  $E/F_x$  amplifier tunings. For example, as seen in the second line, if the third and fifth overtones are tuned as in class  $F^{-1}$  and all other harmonics are tuned as in the class E, the amplifier class is called  $E/F_{3,5}$ . On the other hand, if the switch sees at every odd overtone a short similar to class  $F^{-1}$  amplifiers and at all other overtones a capacitive load, and an inductive load at the fundamental as in class-E amplifiers, the new class is called  $E/F_{\text{odd}}$ .

Like other amplifiers, this family can be implemented in either a single ended or a push-pull configuration. In this case, the push-pull configuration deserves special attention as the complex harmonic tuning required for class  $E/F_{\text{odd}}$  may be automatically provided by the symmetry of the circuit, and the transistor output capacitance does not need to be resonated out as it is included as a part of the circuit topology. Consequently,

Class	$f_o$	$2f_o$	$3f_o$	$4f_o$	$5f_o$	$6f_o$	$7f_o$	$8f_o$
E	R,L	C	C	C	C	C	C	C
E/F <sub>3,5</sub>	R,L	C	short	C	short	C	C	C
E/F <sub>2</sub>	R,L	open	C	C	C	C	C	C
E/F <sub>2,3,7</sub>	R,L	open	short	C	C	C	short	C
E/F <sub>odd</sub>	R,L	C	short	C	short	C	short	C
F <sup>-1</sup>	R	open	short	open	short	open	short	open

**Table 3.2:** Some examples of the E/F amplifiers and their harmonic impedances presented to the switch. (Although the table shows only 8 harmonics, the ideal tuning is not restricted to 8 harmonics.)

with only one tuning element like class E amplifiers, it is possible to obtain a performance close to that of class F<sup>-1</sup>, which is significantly higher than the performance of class E amplifiers. Figure 3.39 shows implementations of both single ended and push-pull class



**Figure 3.39:** Examples of class E/F<sub>odd</sub> power amplifiers. a) Push-pull configuration, b) Single ended configuration.

E/F<sub>odd</sub> power amplifiers. Two switches, each with a shunt capacitor, are connected to the supply through a choke. The differential output network is a parallel LC circuit resonant at fundamental frequency in parallel with an inductor,  $L$ , which is connected in parallel to the load and between the two switches.

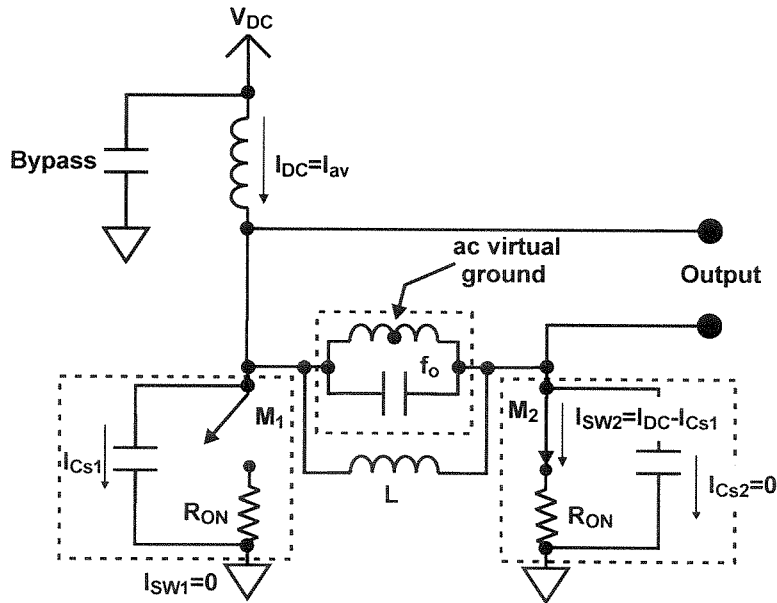
The analysis of this amplifier in push-pull version is similar to that of class D<sup>-1</sup>:

- As the parallel LC circuit is short for all overtones, the voltage waveform across the output network will be a sinusoid. Hence, when one switch is closed maintaining zero voltage at one terminal of the output network, the voltage at other switch will be a half sinusoid as can be seen in Figure 3.23b).

- As the area below the supply voltage and above the supply voltage at the switch must be the same to maintain the constant current through the choke, the peak voltage of the half sinusoid at the switch must be  $\pi$  times higher than the  $V_{DC}$ .

- The current through the capacitor,  $I_{CS}$ , shunt to the open switch will be the derivative of the half sinewave voltage, *i.e.*, half cosine wave.

- While the switch is open, the current through it is zero. When it is closed the current through it will be the dc current from the choke inductor,  $I_{DC}$ , minus the current through the capacitor,  $I_{CS}$ , shunt to the other open switch, as can be seen in Figure 3.40.



**Figure 3.40:** Push-pull class E/ $F_{\text{odd}}$  amplifier. Left switch is open and  $I_{DC}$  and  $I_{CS1}$  flows to ground through closed right switch.

- By symmetry of the topology, there will be a virtual ac ground in the center of the output network connected between the switches, as seen in Figure 3.40, for every odd



harmonic including the fundamental frequency. Hence, the impedance seen by the switch at the fundamental frequency will be nearly half the load resistance in series with a load inductance and, at odd overtones, nearly zero.

- By symmetry, there will be no current at even overtones through the output network or load. Hence the impedance seen by the switch at the even overtones will be the impedance of the shunt capacitor,  $C_S$ .

- By dividing the voltage amplitude by load resistance,  $R_D$ , we have the amplitude of the current through the switch at the fundamental frequency,  $I_o$ . From this amplitude we can compute the average amplitude of the current through the switch,  $V_p$ , while it is on,  $I_{av}$ .

Using the above analysis we can calculate the output power and the efficiency of this switching amplifier as follows:

$$i_D(\theta) = \begin{cases} I_{av} - \omega_o C_S V_p \cos \theta & 0 \leq \theta < \pi \\ 0 & \pi \leq \theta < 2\pi \end{cases} \quad (3.76)$$

$$\begin{aligned} \eta &= 1 - \frac{P_{loss}}{P_{DC}} = 1 - \frac{\frac{1}{2\pi} \int_0^\pi i_D(\theta)^2 R_{on} d\theta}{I_{DC} \cdot V_{DC}} \\ &= 1 - \frac{\left( \frac{I_{av}^2}{2} + \frac{(\omega C_S)^2 V_p^2}{4} \right) R_{on}}{\frac{I_{av}}{2} \cdot \frac{V_p}{\pi}} = 1 - \frac{\pi^2 R_{on}}{4 R_D} - 2(\omega C_S)^2 R_D R_{on} \\ &= 1 - 2.467 \frac{R_{on}}{R_D} - 2(\omega C_S)^2 R_D R_{on} \end{aligned} \quad (3.77)$$

where

$$I_{av} = 2 \frac{\pi}{4} I_o = 2 \frac{\pi V_o}{4 R_D} = \frac{\pi V_p}{4 R_D} \quad (3.78)$$

$$\eta_{E/F_{odd}} = 1 - \left( \frac{\pi^2}{4} \frac{1}{R_D \omega C_S} + 2R_D \omega C_S \right) R_{on} \omega C_S \quad (3.80)$$

As the current cannot be negative<sup>1</sup>, the maximum value of the capacitance is obtained when the downward peak of the current reaches zero.

$$I_{av} = \omega C_S \frac{dv_D(0)}{dt} = \omega C_S V_p = \frac{4}{\pi} \omega C_S R_D I_{av} \rightarrow \omega C_S R_D = \frac{\pi}{4} \quad (3.81)$$

Using the largest transistor size calculated above,  $R_D \omega C_S = 0.78$ , we have:

$$\eta_{E/F_{odd}} = 1 - 4.72 R_{on} \omega C_S \quad (3.82)$$

The last equation shows that class E/F<sub>odd</sub> is more forgiving to the  $C_S$  value and allows us the use of a significantly larger transistor size, which provides lower  $R_{on}$  and consequently a higher  $\eta$  than what is possible with class E.

From (3.77) we can calculate the output power of this amplifier:

$$P_{out} = P_{DC} \cdot \eta = \frac{I_{av}}{2} \cdot \frac{V_p}{\pi} \cdot \eta = \frac{I_p V_p}{2\pi \left( 1 + \frac{4}{\pi} \omega C_S R_D \right)} \cdot \eta \quad (3.83)$$

From (3.78), (3.83), (3.83), and  $V_p = \pi V_{DC}$ ,  $P_N$ ,  $P_{RD}$ , and  $P_{LS}$  can easily be calculated.

### 3.3.2 Impedance Transformation

Impedance transformation is one of the essential functions required in the output network of a power amplifier in most cases, as the load impedance is not always an appropriate value to obtain the desired output power. As commented in Chapter 2, this problem is exacerbated in silicon integrated circuits, as the breakdown voltage of the high speed transistors available in this technology is low and the available output power of amplifiers

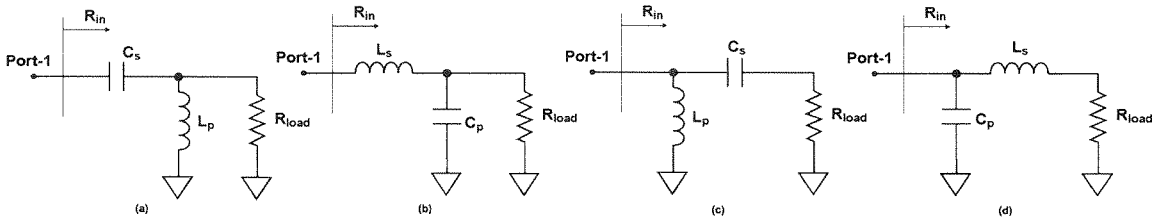
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1. FET loss increases significantly if a negative current with a reasonable amplitude is forced through it, as a conduction through slow substrate junction diode will occur. Bipolar transistor will have a direct conduction through the base collector junction, which also have a slow recovery and causes a significant power and gain losses.

designed without impedance transformation is too low for many applications. Next, we describe briefly some of the most familiar methods of impedance transformation.

### 3.3.2.1 LC Resonant Matching Network

This is the most straightforward way to do the impedance transformation. The series resonant network increases the voltage available to the load, and the parallel resonant network increases the current available to the load. Due to the power conservation, the corresponding current and voltage available respectively will be lower, so that the IV product is approximately constant. The four basic ways to implement an LC resonant impedance transformation are presented in Figure 3.42.



**Figure 3.42:** Four alternatives of a single stage LC resonant matching circuit. a) and b) reduces the load resistance to  $R_{in}$  and c) and d) increase it.

The intuitive way to understand the principle of operation of a series resonant impedance transformation, a) and b) in Figure 3.42, is by considering a series LC resonant circuit where the load resistance is very high and thus negligible compared to the inductor and capacitor reactances. In this case, as the L and C are in resonance, it is easy to accept that the voltage swing at the center node will be much larger than the input voltage applied to the external terminals of the inductor and capacitor. This higher voltage swing present in the center node is denoted the circulating voltage. By lowering the load resistance relative to the inductor and capacitor reactances, this voltage enhancement may be reduced and adjusted to the desired transformation ratio. A similar analysis can be used to understand the parallel LC resonant network, c) and d) in Figure 3.42. If we have a parallel LC resonant circuit with load resistance low enough to be negligible compared to the inductor and capacitor reactances, as they are in resonance, it's clear that the current

through the inductor and capacitor are significantly larger than the current supplied by the source applied to the input terminals. This larger current is called the circulating current. By increasing the load resistance relative to the inductor and capacitor reactances, again, the current enhancement can be adjusted to a desired value or transformation ratio.

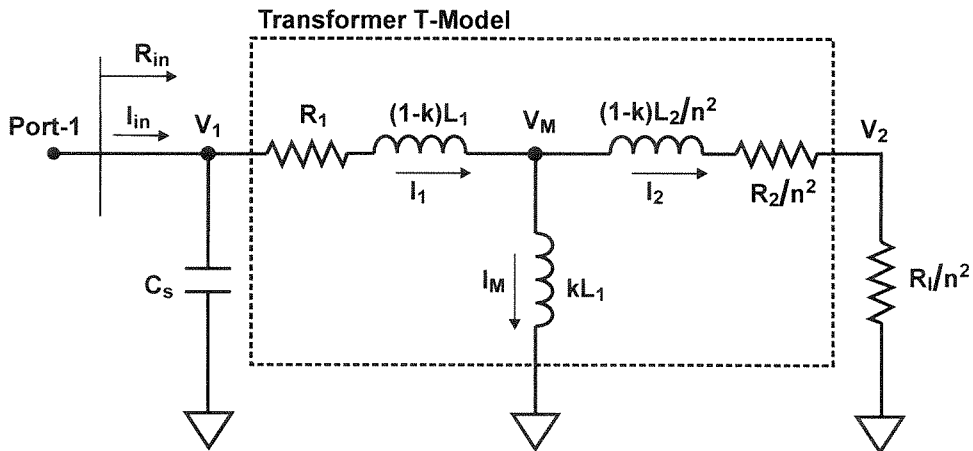
A mathematical treatment of these transformations will be covered in Section 4.1:

It is possible to cascade several stages of such a matching network, allowing lower power loss and higher bandwidth compared to a single stage.

More details about the power loss and multi-stage networks will also be covered in Section 4.1.

### 3.3.2.2 Magnetically Coupled Transformer

This is the most familiar way to do the impedance transformation. Using two or more inductors magnetically coupled, an impedance transformation may be achieved from two terminals of one of the inductors to two terminals of the other inductor. We can see its equivalent electrical model in Figure 3.43.



**Figure 3.43:** Transformer equivalent electrical model with matching capacitor  $C_s$ , turn ratio  $n$ , coupling factor  $k$ , inductance of the primary winding  $L_1$ , secondary winding  $L_2$ , primary loss  $R_1$ , and secondary loss  $R_2$ .

In cases when the magnetic coupling is almost perfect with  $k=1$ , the input impedance will be the transformed load resistance in parallel with the magnetizing inductance. This

later can be cancelled by a series or parallel capacitor in the input,  $C_S$ , obtaining a real transformed impedance at the input as can be seen in the Figure 3.43.

### 3.3.2.3 Transmission Line Matching Network

Impedance transformation using transmission lines may be similar to LC matching as described in Section 3.3.2.1. But it uses transmission lines to make the L and C. Additional to these components, in a transmission line matching, transmission lines of different impedances can also be used for this purpose. The effect of a transmission lines with appropriate impedance when used in a impedance transformation, can be understood as a succession of infinitesimal inductors and capacitors.

The easiest way to design an impedance transformation network using transmission lines is by the use of Smith charts as explained in Section 3.1.1. Open or short stubs may be designed to be used as shunt capacitors or inductors and transmission lines with different lengths and impedances may be used to translate the load impedance in circle on the Smith chart to a desired input impedance.

It is noteworthy that in silicon integrated circuits, it is very difficult, if not impossible, to design a useful impedance transformation network using transmission lines, as any transmission lines on silicon substrate is extremely lossy due to the silicon substrate high conductivity and thin oxide isolation layers. The conductivity of the substrate makes return current of the transmission line conduct inside the resistive substrate, instead of through the backside metal. The thin oxide layer makes the transmission line metal width very narrow to have any acceptable impedance, which in turn makes metal resistance of the line and the transmission line loss very high.

### 3.3.3 Dc Current Feeding

Most of the power amplifiers detailed in the previous examples require a constant dc current supply to operate. Unfortunately, as the available power supplies are dc voltage

sources in most applications, either a large value inductor or an active device is necessary to convert the dc voltage into a dc current.

A second way to feed the power amplifiers with a dc voltage supply directly is to use some symmetric topology to create a virtual ac ground where the dc voltage supply can be connected without interfering with the amplifier internal impedances needed for their operation.

It's noteworthy to say that in the design of a silicon integrated circuit, this is a major problem as large value inductors present low  $Q$  and high power consumption. More details about this problem will be covered in Chapter 4.

### 3.4 Power Combining

In many amplifier implementations, power combining is the best way to increase the output power when the transistor size is limited by the type of package, by the parasitic resistances and inductances of its connections, or by signal phase problems at very high frequencies. The second reason to utilize power combining is when the load impedance is too high and available supply voltage or transistor breakdown voltages are too low to obtain the desired output power and the impedance transformation is limited either by low power efficiency or by the available impedance transformation network having too narrow of a bandwidth.

Particularly in silicon integrated circuit power amplifiers, due to the low substrate resistivity and high metal ohmic loss [12,15], the power loss of any inductor is very high and therefore significantly degrades the output power and efficiency of the amplifier which uses them in their impedance transformation network.

Today's sub-micron transistors necessary for GHz operation in a silicon technology have breakdown voltages in the range of 4 to 6V [14]. This low breakdown voltage limits the drain (collector) ac voltage swing to around  $\pm 2V$ . Without any impedance

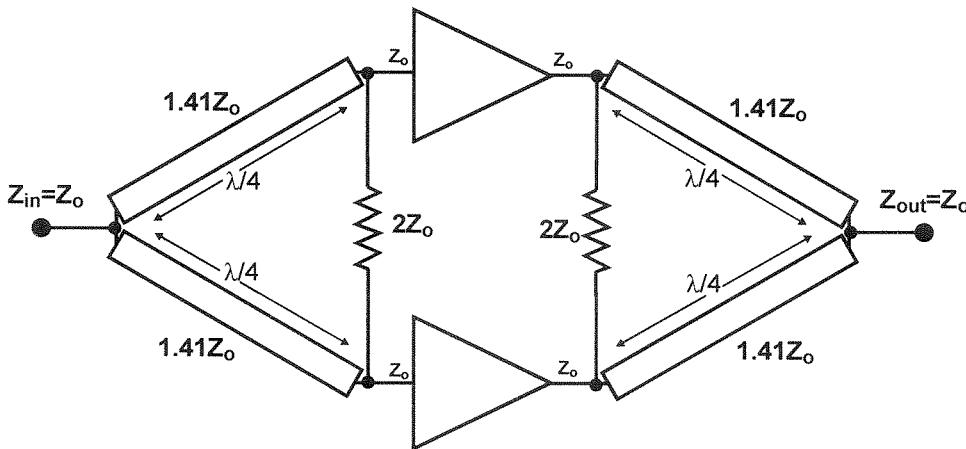
transformation or power combining, the power delivered to a  $50\text{-}\Omega$  load for a sinusoidal voltage waveform is only  $40\text{mW}$  as shown below:

$$P_{out} = \frac{V_D^2}{2R_D} = \frac{(2V)^2}{2 \cdot 50\Omega} = 40\text{mW} \quad (3.84)$$

### 3.4.1 Input Power Splitting

In order to provide power to each one of the transistors, unless some magnetic coupling devices are used, transistor gates or bases should be connected together in parallel. This connection lowers the input impedance of the amplifier, and some impedance transformation is usually necessary to increase the input impedance back to the desired one, normally  $50\Omega$ .

A second way of combining is through the use of transmission lines to connect several transistor gates or bases and simultaneously perform the desired impedance transformation. The most common one is the Wilkinson power divider [15]. If the input and two output impedances are  $Z_o$ , the divider will consist of two quarter-wave transmission lines with impedance  $\sqrt{2}Z_o$  connected together in one side and connected in the other side through a lumped resistor with value  $2Z_o$  as can be seen in Figure 3.44. The

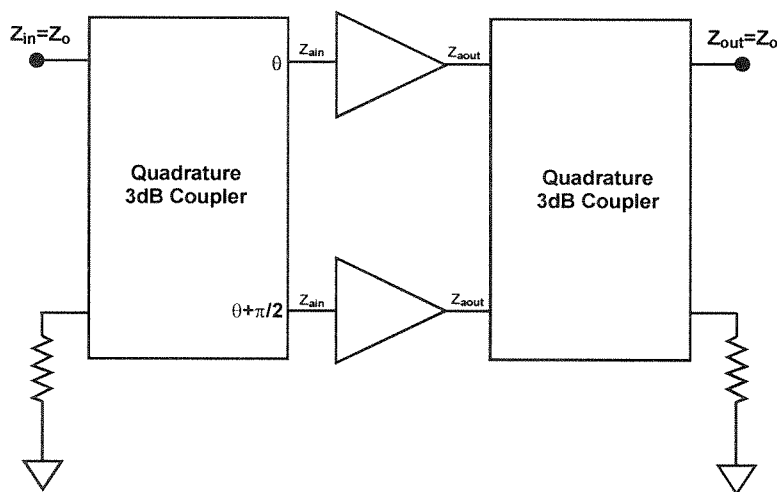


**Figure 3.44:** Wilkinson power divider in the input and combiner in the output of two combined power amplifiers.

transmission lines transform the output impedance to twice its value in order to be connected in parallel to the other branch resulting in  $Z_0$  for the input impedance. The lumped resistor matches the output impedances for any odd mode signal to  $Z_0$ .

In an application using a silicon substrate, due to the high power loss of any transmission lines and inductors, these networks reduce the gain of the power amplifier significantly. The PAE is affected indirectly as a consequence of this gain reduction.

A third way of splitting the power is through the use of balanced topologies. The input power is divided through a 3dB coupler into two signals with  $90^\circ$  out of phase. Several different couplers, such as a Lange coupler or a branch line coupler, might be used. Figure 3.45 shows a block diagram of a balanced amplifier. This topology brings an



**Figure 3.45:** Balanced amplifier diagram.

additional advantage of sending the signal reflected by the input or output mismatch of the amplifiers to the terminated coupler ports [44]. This effect prevents the amplifier operation from being perturbed by the reflected signal.

Still this approach presents a power loss problem as any transmission line used in couplers are highly lossy when fabricated on a silicon substrate.



### 3.4.2 Output Power Combining

Once each transistor receives a drive signal divided from the input power dividing network, the power generated by these transistor must be combined to a single output. This task is accomplished by the output power combining network, which can be designed in a similar fashion as the input power dividing network either using lumped components or transmission line components.

The power loss in this combining network directly affects the PAE of the power amplifier as this network is delivering the amplified output power into the load.

## 3.5 Implementations of Discrete Amplifiers

As an illustration of the power amplifier analysis so far described, a complete design, fabrication, and measurement of two class-E ZVS amplifiers are presented, one operating at an HF frequency and one at a microwave frequency.

### 3.5.1 8.5-GHz/50mW/67% Transmission Line Class-E Amplifier

The first version of a transmission line based class-E amplifier was reported in 1995 by Mader, *et al.* at 5GHz [45]. Shijie Lee in our research group, Caltech MMIC group, designed and tested two similar amplifiers at 10GHz [46].

This design, which uses the fundamental concepts so far studied in this chapter, was sponsored by NASA and was the first study toward the proposed construction of a 32GHz/20W/60% high efficiency solid state power amplifier for JPL deep space communication.

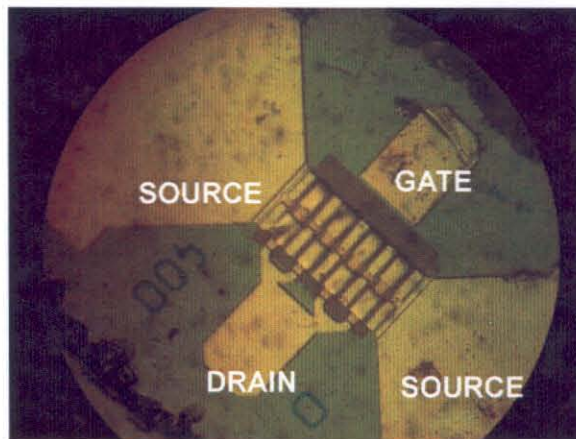
#### 3.5.1.1 Design

A transmission line class-E power amplifier, as described in Section 3.3.1.4, is a class-E power amplifier where the necessary capacitance parallel to the switch is given by the transistor output capacitance. The harmonic impedances necessary to complement this

capacitance, inductive at fundamental frequency and open at overtones, are given by shunt open stubs connected to calculated positions along the transmission line connecting the transistor to the load as can be seen in Figure 3.37.

As the open stubs are very narrow band and need accurate tuning, the design was simulated using transmission line parameters carefully measured from test structures. The transistor model was also measured and the foundry non-linear model adjusted giving higher accuracy through the load line of switching amplifier operation as can be seen in Figure 3.25. The foundry model was optimized to provide a higher accuracy for transistors operating in their forward-active region. Hence the foundry model was not accurate enough to design a switching power amplifier, as switching power amplifier load line remains mainly in ohmic and sub-threshold region.

Unfortunately, the size of the available transistor, a pHEMT (Pseudo-Amorphous High Electron Mobility Transistor) from Rockwell Science Center, was fixed at  $4 \times 80 \mu\text{m}$  gate width, hence the design was conducted to match this transistor size. It has a threshold voltage of  $-1.6\text{V}$ , drain to source breakdown voltage of  $10.5\text{V}$ , gate to source breakdown voltage of  $-5\text{V}$ , drain maximum current of  $160\text{mA}$ , and  $f_t = 60\text{GHz}$ . Figure 3.46 shows a microphotograph of the transistor.

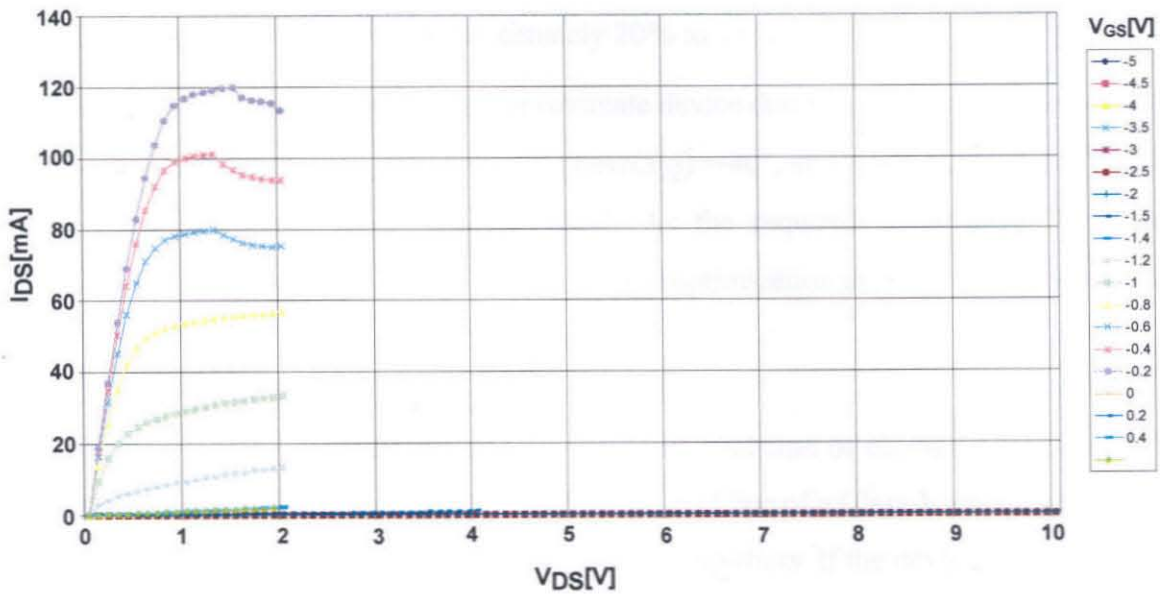


**Figure 3.46:** Microphotograph of a Rockwell LNA process pHEMT with  $W = 4 \times 80 \mu\text{m}$ ,  $L = 0.18 \mu\text{m}$ , and  $f_t = 60\text{GHz}$ .

In a transmission line amplifier, as we have stubs to tune each of the harmonics independently, we are not restricted by the transistor  $C_S$ . The  $C_S$  can be increased or reduced by the tuning stubs individually at each harmonic frequency. Therefore, we can choose any load resistance to be presented to the transistor drain.

Under this circumstance, we have a special situation where the transistor size and  $R_{on}$  are fixed variables and  $R_D$  and  $C_S$  can be of our choice. Hence, we can sacrifice the output power for higher efficiency or vice versa. Our design goal under this condition was to have 60 to 70% PAE with output power as high as possible.

From the transistor measured IV curve, Figure 3.47, a  $R_{on}$  of  $6.3\Omega$  is obtained.



**Figure 3.47:** Measured  $I_{DS}$  vs. ( $V_{DS}$  &  $V_{GS}$ ) of a Rockwell LNA process pHEMT with  $W=320\mu\text{m}$ ,  $L=0.18\mu\text{m}$ , and  $f_t=60\text{GHz}$ . When  $V_{GS}$  is below threshold, the  $I_{DS}$  is measured up to  $V_{DS}=10\text{V}$  to verify the drain breakdown, otherwise  $I_{DS}$  is measured up to  $V_{DS}=2\text{V}$  to avoid thermally damaging the transistor.

The transistor loss should be below around 20% to achieve the target PAE of above 60% as, by rule of thumb for the discrete rf power amplifiers, we expect to have around 10dB gain and 5 to 10% loss in the passive output circuit.

To have the device loss below 20% of total applied power, we have from (3.73):

$$\eta = 0.8 = 1 - 1.365 \frac{R_{on}}{R_D} \rightarrow R_D = 43\Omega \quad (3.85)$$

All the other component values are easily calculated using (3.70) and (3.71) and we obtain  $C_S=80\text{fF}$ ,  $L=930\text{pH}$ . From transistor breakdown voltage of 10.5 V, the dc supply voltage of 3 V is calculated using (3.66).

The predicted output power without including any passive losses is approximately 97mW with peak drain current of 115mA using (3.63) and (3.72). As the transistor drain maximum saturation current is 160mA, approximately up to 120mW may be achieved by increasing the  $I_p$ . For that,  $R_D$  should be  $31\Omega$ , using (3.63) and (3.72). But this would increase the transistor loss from approximately 20% to 28%, which is below our goal.

From measured transistor  $S_{22}$ , the approximate device drain to source capacitance may be calculated. From  $\text{mag}(S_{22})=0.586$  and  $\text{phase}(S_{22})=-40^\circ$ , at  $V_{GS}=0\text{V}$ ,  $V_{DS}=2.5\text{V}$  and 8.5GHz, the estimated capacitance is 126fF. As the required capacitance, 80fF, is relatively close, further adjustments were left to the optimization through the simulations.

### 3.5.1.2 Simulation

In Figure 3.9 and Figure 3.25 we can see a typical load line of classes A, B, C and E amplifiers. It is clear that the region covered by the load line of a Class-E amplifier is quite different from the region covered by classes A or B amplifiers. If the device was measured under the Class A load line and the simulation model equation coefficients optimized to fit the measurement under these condition, it is very unlikely that the model presents a good accuracy when used to design Class-E amplifiers.

Unfortunately, most foundry models are optimized for transistors operating under the class A, B, and C load lines. Hence, the resulting transistor model is inappropriate to design switching amplifiers, including class-E amplifiers, and leads to a large simulation error if used to design these amplifiers. One previous amplifier using the same transistor,

but designed with original foundry transistor simulation model, performed around 40% power added efficiency, while the simulation predicted a power added efficiency above 70%.

In device modeling, the measurement of dc  $I_{DS}$  vs. ( $V_{DS}$  &  $V_{GS}$ ) and  $I_{GS}$  vs.  $V_{GS}$ , provides data to adjust the models of transistor's gate Schottky diode and drain current source<sup>1</sup>.

By measuring S-parameters over a reasonable frequency range under one bias condition, we obtain hundreds of independent data points. Using this measured data, every model parameter under this bias condition may be determined. Finally, by measuring S-parameters under every bias condition, in which the device will be operating, the bias dependent capacitor coefficients may be found. All measurements should be restricted only to the bias conditions under which the amplifier will operate, linear and sub-threshold condition for switching amplifiers, otherwise, the model accuracy will be compromised.

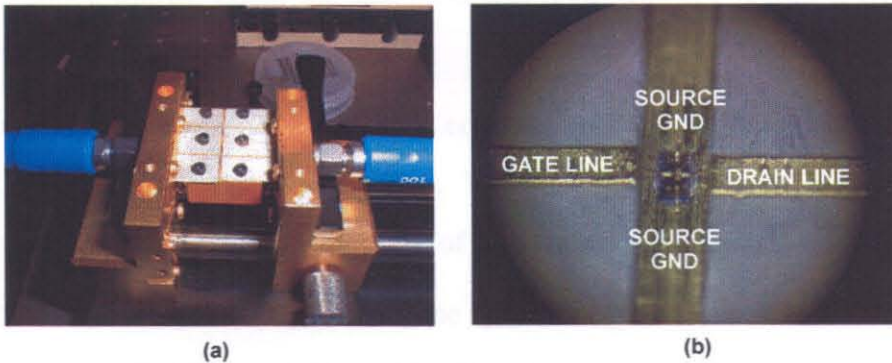
In our design, following the above guidelines, we have measured the dc IV curve, shown in Figure 3.47, and S-parameters of the device from 1 to 40GHz with an HP8722D Vector Network Analyzer using an rf probe station. The bias points measured were as follows: ( $V_{DS}=0.0V$ ,  $V_{GS}=-2.5V$ ,  $0.0V$ ,  $0.6V$ ), ( $V_{DS}=0.5V$ ,  $V_{GS}=-2.5V$ ,  $0.0V$ ,  $0.6V$ ), ( $V_{DS}=1.0V$ ,  $V_{GS}=-2.5V$ ,  $0.0V$ ,  $0.6V$ ), ( $V_{DS}=2.0$ ,  $V_{GS}= -2.5V$ ,  $0.0V$ ,  $0.6V$ ), ( $V_{DS}=5.0V$ ,  $V_{GS}=-2.5V$ ,  $-5.0V$ ), and ( $V_{DS}=10.0V$ ,  $V_{GS}=-2.5V$ ,  $-5.0V$ ).

In order to model the line to transistor transition consisting of bond-wires to a printed microstrip line, the transistor was also measured connected to a pair of  $50\Omega$  lines using bond-wires. The test is fabricated on the same substrate and ground plane assembly, which is used to build the final amplifier. Figure 3.48 shows the pictures of the measured lines with transistor.

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1. Except for transistors operating in the saturated region, for which a pulsed measurement is necessary in order to have an accurate measurement without the influence of the pHEMT thermal effect. Fortunately, Class-E load line does not reach this region.





**Figure 3.48:** Measurement set up for transistor wire bond transition model extraction. a) Test fixture with  $50\Omega$  line and transistor, b) Transistor gate and drain connected to  $50\Omega$  lines and source connected to metal ground.

The class-E amplifier circuit using the device model, wire bond connection model, and input and output load network consisting of by lossless lumped components was simulated using harmonic balance simulator in Agilent Advanced Design System (ADS). The circuit was initially simulated with an output load network using values calculated analytically and then was optimized by analyzing its drain voltage and current waveform. The harmonic impedances presented to the transistor drain was adjusted in order to achieve a ZVS operation. The input network was adjusted to provide conjugate matching to the gate in large signal simulation. It was optimized to minimize the reflected signal with the amplifier operating at its normal power level, which requires an input power of around 5 to 8 dBm. The gate dc voltage was adjusted to have a 50% duty cycle.

The resulted performance before optimization was  $\text{PAE}=71\%$ ,  $\eta=77\%$ ,  $\text{gain}=11\text{dB}$  and  $P_{\text{out}}=80\text{mW}$ . There was no significant improvement after optimization.

In order to test the circuit sensitivity to the condition of untuned harmonics, the amplifier was simulated short circuiting every harmonic signal above fourth harmonic from the drain to the load. The simulation was repeated opening or short circuiting to these same harmonics from drain to ground. The PAE obtained was around 0.5% lower than the PAE from a simulation with more than 15 harmonics, showing no necessity to control

harmonics above fourth. When the same test was done with harmonics above third, the PAE dropped around 3%.

The microstrip line model's dielectric constant and loss were adjusted to meet the measured values of a  $50\Omega$  through line. The substrate used was Roger RT/Duroid 6010LM 0.5oz with  $\epsilon_r=10.2$  and thickness of 0.381mm.

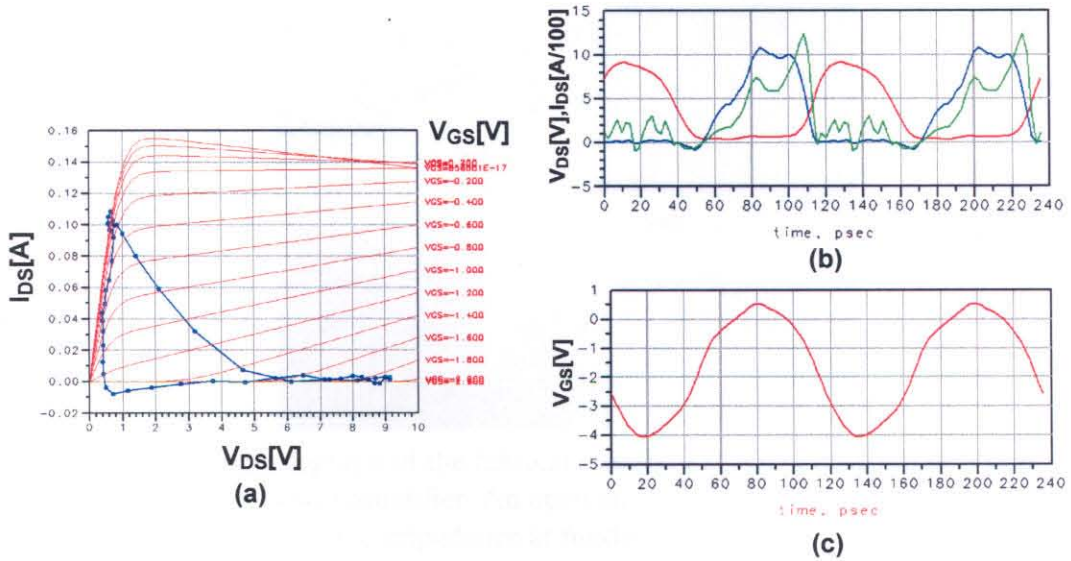
The input microstrip-line circuit with one open tuning stub was designed to present, to the gate, the same impedance presented by the simulated lumped component network at the fundamental frequency. The output microstrip line circuit with three open stubs was designed to present the same impedance at fundamental, second, and third harmonics to the drain.

A second version of the output network was designed with two open stubs presenting the same impedance of the optimized circuit to the drain, but only at fundamental and second harmonics. The previous amplifier, which controls up to the third harmonic, presents similar efficiency as this one controlling only two harmonics. The larger passive circuit loss of the amplifier controlling three harmonics offsets the efficiency improvement obtained with better drain waveshaping compared to the amplifier controlling two harmonics.

Final simulated performance:  $PAE=68\%$ ,  $\eta=75\%$ ,  $gain=10dB$  and  $P_{out}=64mW$  at  $P_{in}=8dBm$  and  $PAE=69\%$ ,  $\eta=70\%$ ,  $gain=18dB$  and  $P_{out}=60mW$  at  $P_{in}=0dBm$ . The simulated load line, drain current, and voltage waveforms can be seen in Figure 3.49.

### 3.5.1.3 Fabrication

The input and output circuit is constructed on two separate boards. They are mounted to a gold plated brass ground plane leaving a 0.5mm gap between the two boards. The pHEMT is placed directly on the ground plane using a silver epoxy and its gate, drain and source connected to input, output and ground respectively using 1mil diameter wire bonds.



**Figure 3.49:** a) Load line of the simulated class-E amplifier with Duroid transmission line networks, b) Drain voltage, red, current, blue, and instant power dissipated in the transistor, green, c) Gate voltage, red.

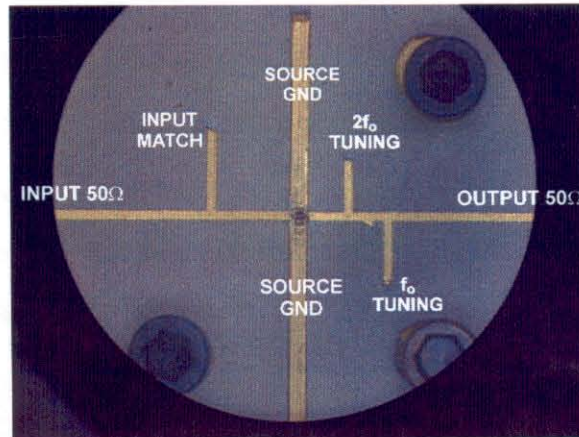
The input and output circuit S-parameters are measured independently to tune the circuits to be as close as possible to the simulated circuit S-parameters at the frequencies of interest. The measurement was made using an Anritsu Universal Test Fixture (UTF). The fixture to amplifier transitions are de-embedded to enhance accuracy. This tuning procedure eliminates the error caused by inaccuracy of the etched metal dimensions.

The amplifier has been simulated with measured input and output network S-parameters and the tuning has been performed until a simulated power efficiency using measured networks is comparable to the simulation using model networks.

Simulated performance with measured input and output network data when input power was 8dBm is PAE=70%,  $\eta$ =78%, gain=10dB, and  $P_{out}$ =67mW.

Figure 3.50 shows the fabricated amplifier.

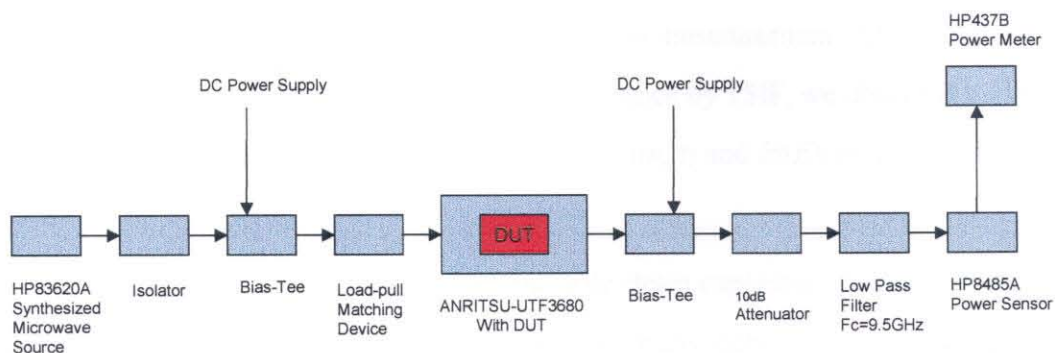




**Figure 3.50:** Microphotograph of the fabricated hybrid 8.5GHz transmission line class-E power amplifier. An open stub matches the input and two open stubs control the impedance at fundamental and second harmonic for the drain.

### 3.5.1.4 Experimental Results

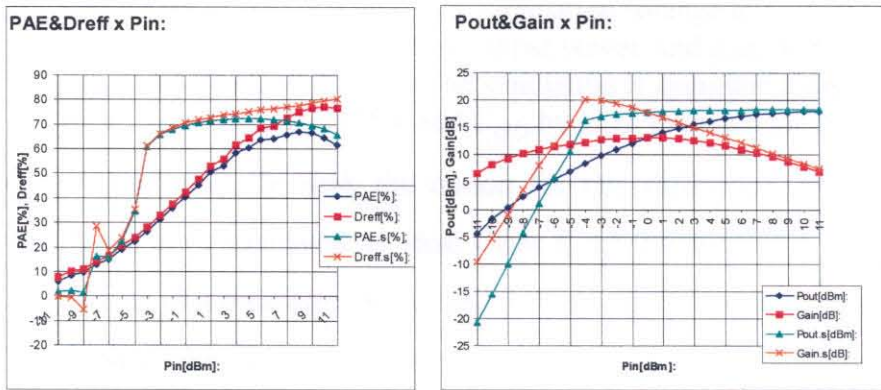
The assembled amplifier has been measured using an input isolator, output 10dB attenuator, and 9.5GHz low pass filter through a Anritsu UTF. The dc power is supplied through two bias-tees. The HP83620A Frequency Synthesizer supplies the input power. The Power Sensor HP8485A/HP437B measures the output power. Every measurement setup including the UTF has been previously measured and de-embedded from the amplifier measurements. The measurement setup can be seen in Figure 3.51.



**Figure 3.51:** Measurement set up for 8.5GHz transmission line class-E power amplifier.

The bias and input signal have been swept from -11dBm to 11dBm. The following peak performance has been measured when input power is 8dBm: PAE=67%,  $\eta$ =75%, gain=9.6dB and  $P_{out}$ =58mW. The maximum performance is obtained at exactly 8.5GHz.

At lower input powers, when transistor is not acting as a switch, the simulated and measured performance are significantly different as can be seen in Figure 3.52. At  $P_{in}$ =0dBm the measured performance is PAE=45%,  $\eta$ =48%, gain=13dB and  $P_{out}$ =21mW.

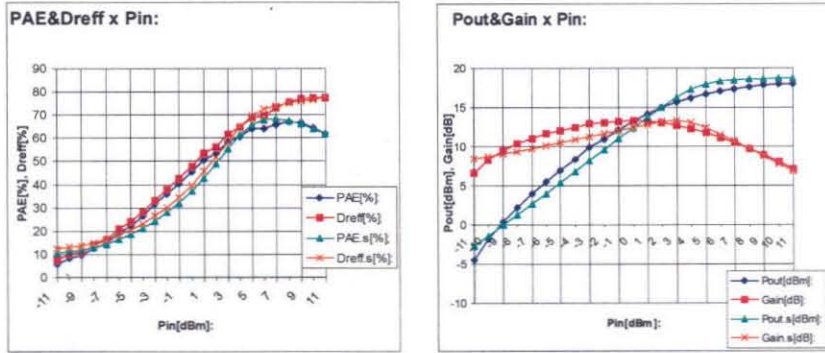


**Figure 3.52:** Measurement (red and blue) and simulation (orange and green) of the amplifier PAE, drain efficiency, output power, and gain with  $V_{DC}$ =3V,

As the transistor used in the measured amplifier was not the one which was measured for model parameter extraction, we changed slightly the transistor simulation model parameters to check if the  $P_{out}$  vs.  $P_{in}$  can agree to the measurement. After decreasing the threshold voltage by 0.25V and gate to drain capacitance by 15fF, we obtained a very good agreement between measured and simulated ( $P_{out}$ , gain,  $\eta$  and PAE) vs.  $P_{in}$  as may be seen in Figure 3.53.

These differences in threshold voltage and gate drain capacitance are small enough to be explained as the normal difference between two transistors of the same type and size due to process variation.

Comparing the theory, simulation, and measurement, we can see that the efficiency agrees well, but the simulated and theoretical output powers are 24% and 67% larger than



**Figure 3.53:** Measurement (red and blue) and simulation (orange and green) of the amplifier PAE, drain efficiency, output power, and gain with  $V_{DC}=3\text{ V}$ ,  $V_{GS}=-1.6\text{ V}$ , and at  $8.5\text{ GHz}$ . The simulation is using the transistor model with  $V_{th}$  adjusted by  $0.25\text{ V}$  and  $C_{GD}$  by  $15\text{ fF}$  to match the measurement.

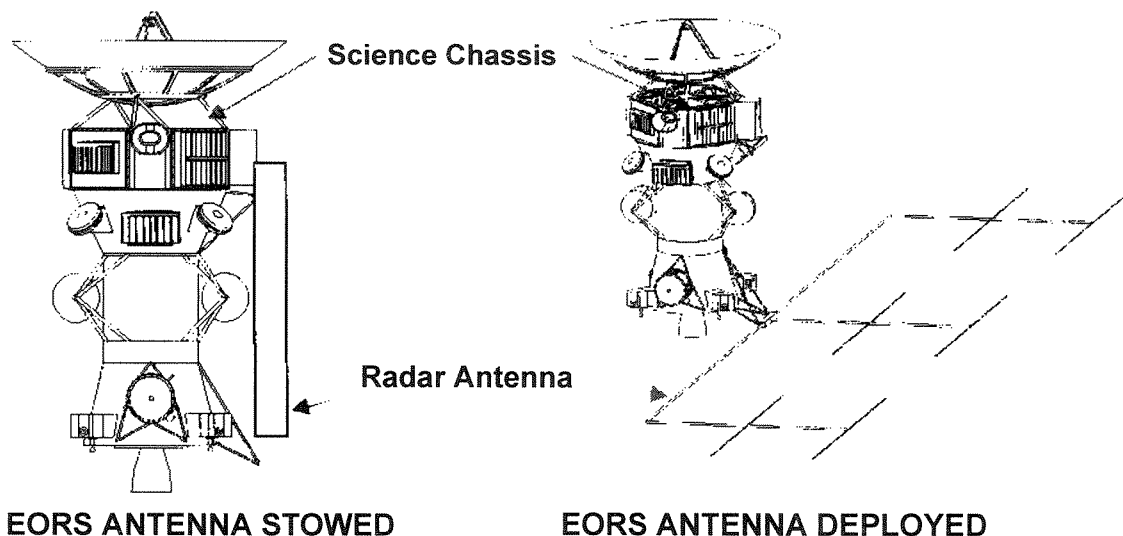
measured one, respectively. To seek the reason for this difference, especially of the analytical model, we have simulated an ideal Class E amplifier using a switch in series with  $6.3\Omega R_{on}$  instead of a transistor model, and its output power agrees with analytically calculated value. Next, the switch in the simulation is changed to a variable resistor, its conductivity varying sinusoidally from zero to  $1/6.3\text{ S}$  and back to zero throughout the switching period. In this case, we have much lower output power and efficiency close to what is seen in the simulation using the transistor model and in the measurement. Therefore, we can conclude that the inaccuracy of the analytical model is due to the low transistor switching speed caused by low gain at high frequencies. Unfortunately, this effect is very difficult to predict analytically and remains a subject for future investigations.

### 3.5.2 50-MHz/100-W/83% 3 Stage Injection Locked Class-E Amplifier

This second design is a HF 100W/50MHz class-E power amplifier. This amplifier has been sponsored by the NASA/JPL Advanced Radar Technology Program for use in the transmitter of the Radar System on board of the Europa Orbiter (EORS), shown in Figure 3.54, scheduled to be launched in 2003. The pulsed 50MHz signal will penetrate the ice layer on the surface of Europa, one of Jupiter's satellites, and the reflected radio



signal will bring back information to determine the presence of or absence of a subsurface ocean and characterize the three-dimensional distribution of any subsurface liquid water and its overlying ice layers. The low frequency has been chosen to allow the signal to penetrate the thick ice layer expected to be found on Europa [47].



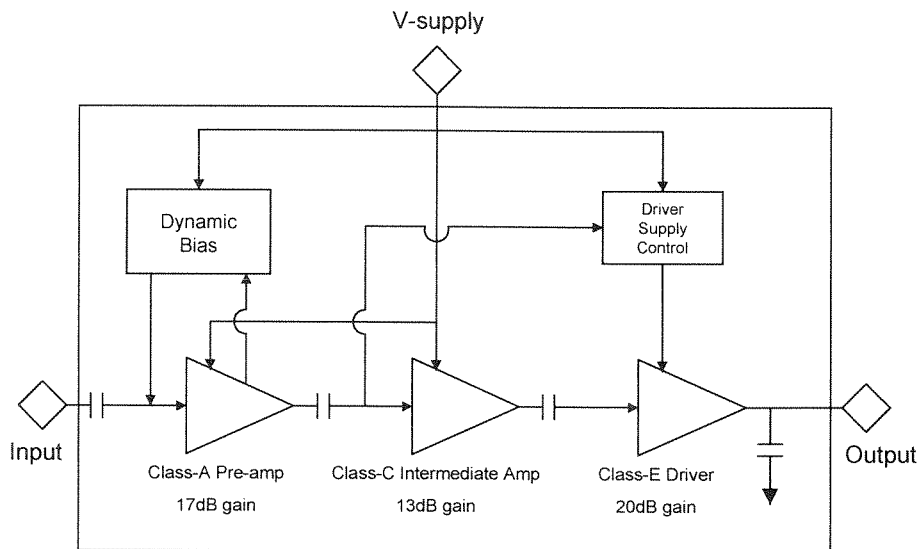
**Figure 3.54:** Europa Orbiter Spacecraft with Radar System (EORS) and its antenna.

### 3.5.2.1 Design and Simulation

The required specification for this design is 100W pulsed output with  $1\mu\text{s}$  pulse width repeated at 1KHz pulse rate, total PAE above 80%, 50dB gain,  $50\Omega$  output, and TTL level input. The entire circuit must fit in a space not larger than around 4cm x 7cm x 2cm and have a mass less than 54.3g.

To be able to have 50dB gain and simultaneously have 80% PAE, the amplifier has been designed with three stages, where the last stage is a 20dB gain injection locked class-E power amplifier (PA), the second stage, a 13dB gain class-C PA, and the first stage, a 17dB gain class-A PA as shown in Figure 3.55. Additional control circuitry to detect the input signal and turn on and off the class-E stage through supply current has also been implemented. In order to operate with very low duty cycle, 0.1%, and still

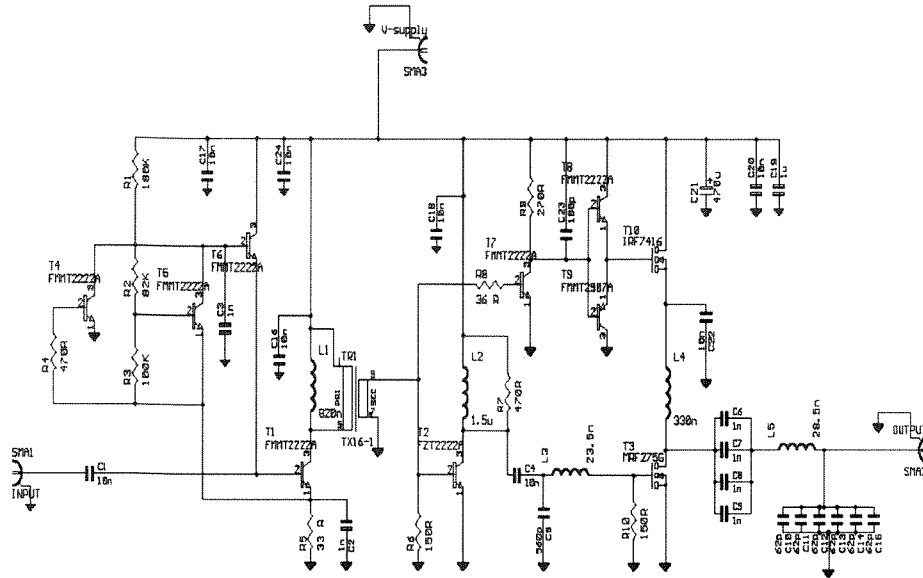
comply with the high PAE requirement, a dynamic bias circuit has been designed to control the first class-A stage. This class-A stage stays in a very low bias current standby state between the pulses and immediately goes to the full bias and operational state as soon as the input pulse is detected and during the duration of the pulse.



**Figure 3.55:** Block diagram of the three stage, 100W/50MHz EORS power amplifier.

A electrical diagram can be seen in Figure 3.56. The active device used is the Motorola MRF275G, transistor in the output stage, Zetex FZT2222A in the driver stage, and Zetex FZT2222A and FZT2907A in the input stage and control circuits. To control the supply current of the class-E stage, an International Rectifier IRF7416 is used to control the output stage supply.

This amplifier has been designed using the power amplifier theory described in this chapter and has been optimized through fabrication and modification of several prototypes. ADS simulations were used with the foundry MRF275G model for initial design of the output class-E stage only.



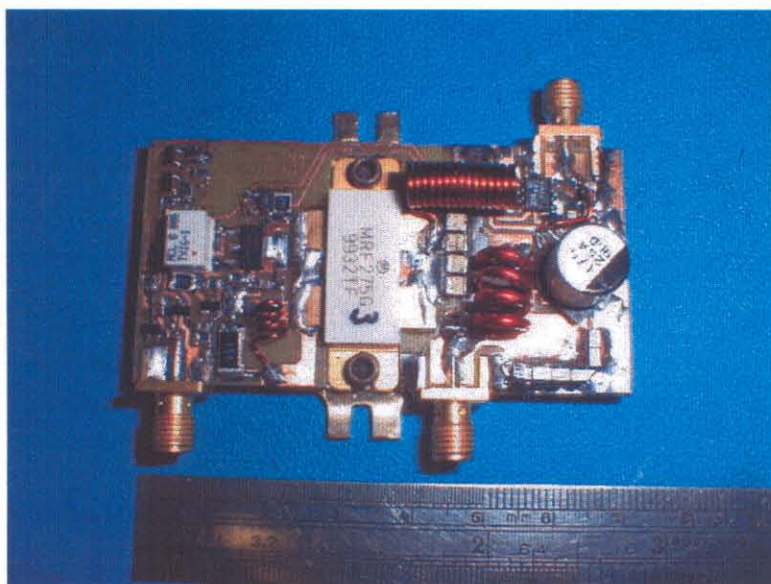
**Figure 3.56:** Electrical diagram of the three stage, 100W/50MHz EORS power amplifier.

### 3.5.2.2 Experimental Results

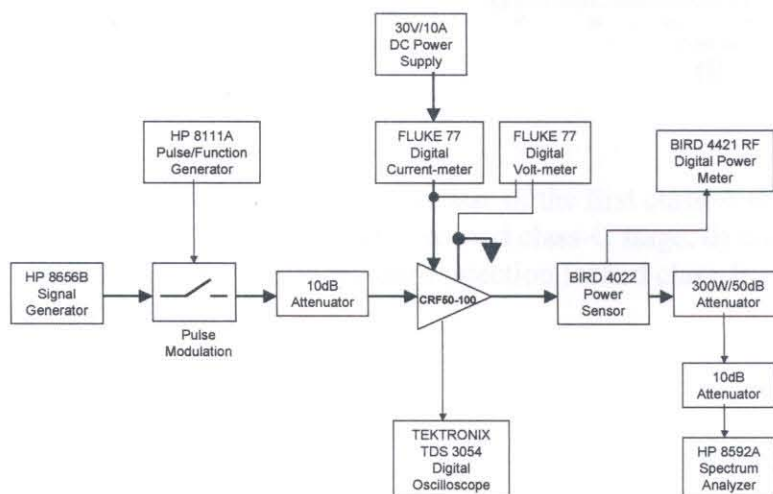
Figure 3.57 shows a photograph of a fabricated amplifier. Table 3.3 shows the measured performance obtained from a total of six amplifiers fabricated. Figure 3.58 shows the measured voltage input and output waveforms of each one of the three stages of a representative amplifier.

The measurement set up can be seen in Figure 3.59.

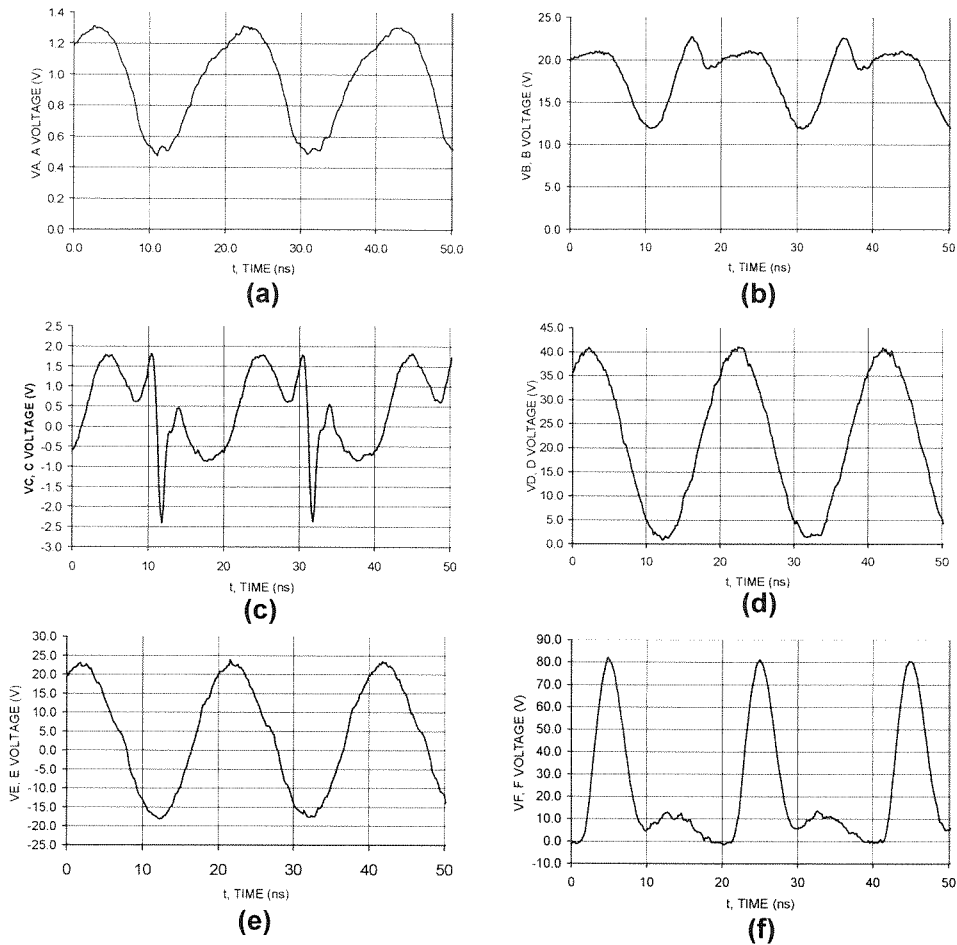
The final physical dimensions of the amplifier are 4cm x 7cm x 1.8cm and it weighs 75g.



**Figure 3.57:** Three stage, 100W/50MHz EORS power amplifier.



**Figure 3.59:** Block diagram of the measurement setup.



**Figure 3.58:** Measured voltage waveforms: a) base of the first class-A stage, b) collector of the first stage, c) base of the second class-C stage, d) collector of the second stage, e) gate of the third injection locked class-E stage, f) drain of the third stage.



Characteristic	Min.	Typ.	Max	Unit
Frequency Range	49	---	51	MHz
Output Power	50	50.2	---	dBm
Power Added Efficiency	80	83	---	%
Input VSWR	---	1.4	2.0	VSWR
2nd Harmonic Output	---	---	-27	dBc
3rd Harmonic Output	---	---	-43	dBc
Output Power at Low Supply (15V)	48.3	48.5	---	dBm
Output Power, Isolation (no supply)	---	-30	---	dB
Supply Current	---	7.0	7.3	A
Supply Current at Standby	---	0.5	0.8	mA
Supply Current at Standby (between pulses)	---	1.5	2.0	mA

**Table 3.3:** Performance measured from six EORS power amplifiers.

## Chapter

## 4

# *Fundamental Limitations of Conventional Networks*

This chapter presents a study of the most common passive impedance transformation networks for watt-level fully-integrated power amplifiers. We present simple models of common transformation networks, issues related to their design, and their corresponding lowest achievable power losses.

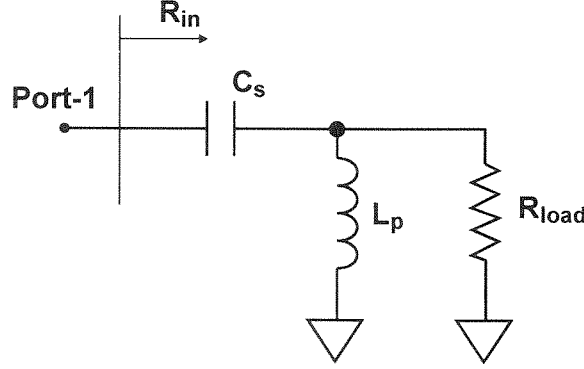
A low loss impedance transformation with a large ratio is essential to deliver a large ac power efficiently into a  $50\text{-}\Omega$  load using low-breakdown sub-micron high frequency integrated transistors. For instance, to deliver  $2\text{ W}$  to a  $50\text{-}\Omega$  load using a drain voltage swing of  $\pm 2\text{ V}$ , a minimum impedance transformation ratio of 1:50 is necessary.

We will present, here, an analytical study of the power efficiency of some common impedance transformation networks as a function of their inductor unloaded quality factor,  $Q_{ind}$ , and their transformation ratio. As the quality factors of the on-chip capacitors are significantly higher than that of the inductors, their losses are not considered here.

## 4.1 LC Resonant Impedance Transformation

Inductor-capacitor (LC) resonant matching [29][48][49] is one of the most straightforward means of impedance transformation. A single LC section, as shown in Figure 4.1, may be used to perform impedance matching. In some cases, it may be desirable to cascade several such sections to enhance the efficiency. We will analyze the single section and extend the analysis to the general, multi-section case.

Using the single section network in Figure 4.1, an impedance transformation ratio,  $r$ , is achieved with a parallel inductor and a series capacitor. The dual network with a parallel capacitor and a series inductor may also be used. However, a series capacitor has the



**Figure 4.1:** Ideal resonant LC impedance transformation network.

added advantage of blocking the dc current from flowing through the load, and a parallel inductor with a terminal connected to ground lowers the energy coupling into the substrate for integrated power amplifiers and hence lowers the associated loss of the inductor. The dual network, however, results in better harmonic suppression due to its low-pass nature.

The impedance transformation ratio,  $r$ , is defined as

$$r \equiv \frac{R_{load}}{R_{in}} = 1 + Q_l^2 \approx Q_l^2 \quad (4.1)$$

where  $R_{load}$  and  $R_{in}$  are the load resistance and its transformed impedance at port-1, and  $Q_l$  is the loaded quality factor of the network at the angular frequency,  $\omega$ , assuming lossless passive components, *i.e.*,

$$Q_l = \frac{R_{load}}{\omega L_p} \quad (4.2)$$

The voltage swing limitations of the active device in combination with desired output power determine  $R_{in}$ . A given  $R_{in}$  and  $R_{load}$  will set  $r$  and  $Q_l$  in (4.1). Then (4.2) can be used to calculate the value of the inductor,  $L_p$ . Knowing  $L_p$ , the capacitor value can be selected using the following resonant condition:

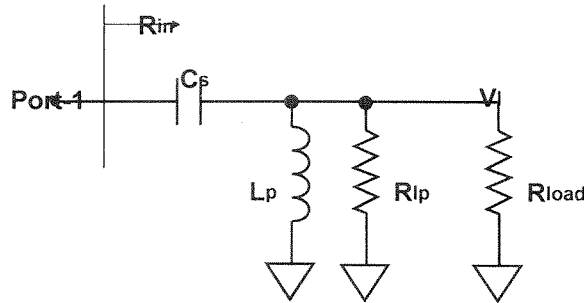
$$\frac{1}{\omega C_s} = \frac{\omega L_p}{1 + \frac{1}{\left(\frac{R_{load}}{\omega L_p}\right)^2}} = \frac{\omega L_p}{1 + \frac{1}{Q_l^2}} \approx \omega L_p \quad (4.3)$$

While complete models for on-chip inductors have been devised [50], the loss of a one-port inductor,  $L_p$ , at a single frequency can always be modeled using a single parallel resistor,  $R_{lp}$ , or by using its unloaded quality factor,  $Q_{ind}$ , defined as

$$Q_{ind} = \frac{R_{lp}}{\omega L_p} \quad (4.4)$$

at the frequency of interest. Figure 4.2 shows the resonant impedance transformation network with the simplified narrow-band inductor model. The passive power transfer efficiency,  $\eta$ , of this network, calculated as the ratio between the input rf power and the rf power delivered to the load, can be computed as a function of  $Q_{ind}$  and  $r$ , as follows:

$$\begin{aligned} \eta \equiv \frac{P_{out}}{P_{in}} &= \frac{|V_l|^2 / (2R_{load})}{|V_l|^2 / (2(R_{load} \parallel R_{lp}))} = \frac{1/R_{load}}{1/R_p + 1/R_{load}} \\ &= \frac{1}{1 + \frac{R_{load}}{\omega L_p Q_{ind}}} \end{aligned} \quad (4.5)$$



**Figure 4.2:** Resonant LC impedance transformation network with loss.

The efficiency is the ratio between the load conductance,  $1/R_{load}$ , and total conductance,  $1/R_{lp} + 1/R_{load}$ . The impedance transformation ratio,  $r$ , in the presence of loss

can be easily calculated using (4.1) as a function of  $R_{lp}$ ,  $R_{load}$ , unloaded inductor  $Q_{ind}$ , and total loaded quality factor,  $Q_{total}$ , namely,

$$r = \frac{R_{load}}{\left( \frac{R_{load} \parallel R_{lp}}{1 + Q_{total}^2} \right)} = \frac{\left( 1 + \frac{R_{load}}{R_p} \right)^2 + Q_{ind}^2 \left( \frac{R_{load}}{R_{lp}} \right)^2}{1 + \frac{R_{load}}{R_{lp}}} \quad (4.6)$$

where the total loaded quality factor,  $Q_{total}$ , is defined as

$$Q_{total} \equiv \frac{R_{load} \parallel R_{lp}}{\omega L_p} \quad (4.7)$$

Equations (4.4) and (4.6) can be solved for  $\omega L_p$  in terms of the desired transformation ratio,  $r$ , load resistance,  $R_{load}$ , and inductor quality factor,  $Q_{ind}$ , i.e.,

$$\omega L_p = \frac{R_{lp}}{Q_{ind}} = \frac{2(Q_{ind} + 1/Q_{ind})}{r - 2 + \sqrt{r^2 + 4Q_{ind}^2(r - 1)}} R_{load} \quad (4.8)$$

which can be used to calculate the value of  $L_p$  in the design process. In practice,  $Q_{ind}$  and  $r$  are both functions of  $L_p$  and therefore several iterations may be necessary to obtain the exact value of  $L_p$ .

The efficiency of the transformation network,  $\eta$ , can also be calculated as a function of  $Q_{ind}$  and  $r$  from (5) and (8):

$$\eta = \frac{Q_{ind}^2 + 1}{Q_{ind}^2 + \frac{r + \sqrt{r^2 + 4Q_{ind}^2(r - 1)}}{2}} \approx \frac{1}{1 + \frac{r}{Q_{ind}^2}} \quad (4.9)$$

For any matching network, we can define the *power enhancement ratio (PER)*,  $E$ , as the ratio of the rf power delivered to the load with a transformation network in place,  $P_{trans}$ , to the power delivered to the load for the same sinusoid input voltage source when it drives the load directly,  $P_{direct}$ , i.e.,

$$E \equiv \frac{P_{trans}}{P_{direct}} = \frac{P_{direct} r \eta}{P_{direct}} = r \eta \quad (4.10)$$

Unlike  $r$ , power enhancement ratio (PER) accounts for the loss in the passive impedance transformation ratio and is thus particularly important for lossy on-chip passive components in silicon technology.

Using the definition in (4.10) together with (4.4), (4.5), and (4.6), we can find a closed-form solution to calculate the passive network efficiency,  $\eta$ , for a necessary  $E$  and available inductor  $Q_{ind}$ , as follows:

$$\eta = 1 - \frac{\sqrt{E-1}}{Q_{ind}} \approx 1 - \frac{\sqrt{E}}{Q_{ind}} \quad (4.11)$$

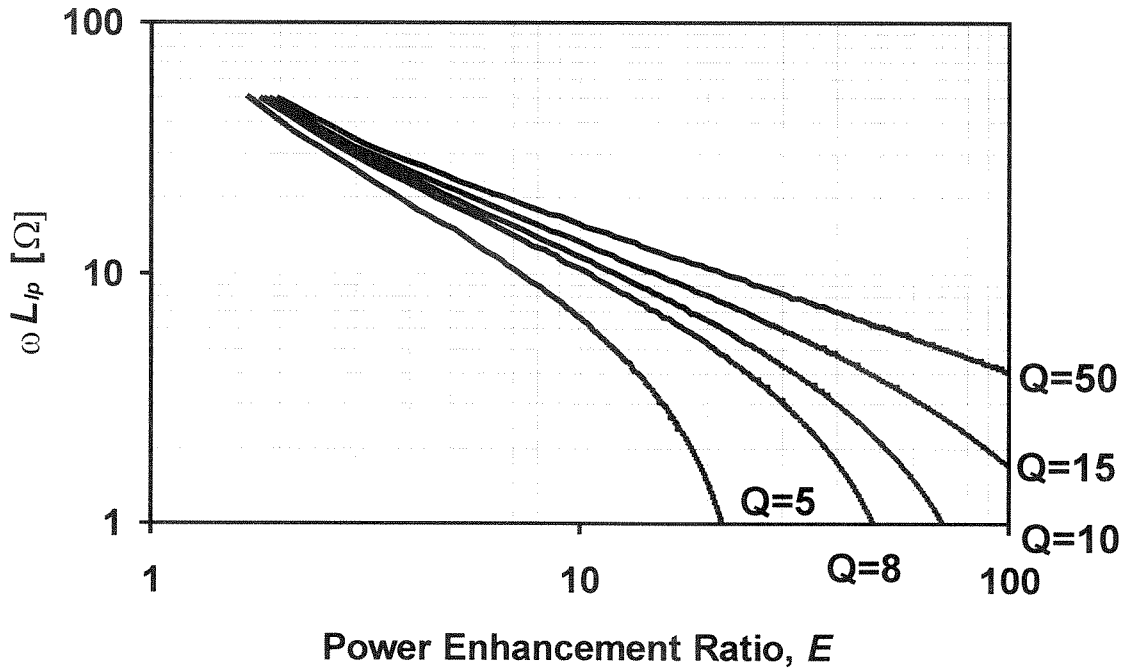
Furthermore,  $\omega L_p$  can be calculated from  $E$  and  $Q_{ind}$ :

$$\omega L_p = \frac{R_{lp}}{Q_{ind}} = \left( \frac{1}{\sqrt{E-1}} - \frac{1}{Q_{ind}} \right) R_{load} \quad (4.12)$$

Appendix A contains the derivations leading to (4.11) and (4.12).

Figure 4.3 shows plots of  $\omega L_p$  vs.  $E$  for several different values of  $Q_{ind}$  and a 50- $\Omega$  load resistor,  $R_{load}$ , for a single LC-section. As can be seen from these graphs, for a power enhancement ratio (PER) of 50, a reactance of 2j $\Omega$  is necessary if an inductor with  $Q_{ind}$  of 10 is to be used.

Figure 4.4 shows plots of  $\eta$  vs.  $E$  for several different  $Q_{ind}$  for a single section network. For instance, with a power enhancement ratio (PER) of 50 and an inductor  $Q_{ind}$  of 10, the matching network *alone* will have a maximum passive power efficiency of around 30%. This does not include any loss in the active device, the driving network, or the external connections. We can also see in the Figure 4.4 that for a given inductor quality factor,  $Q_{ind}$ , there is an upper bound on the maximum achievable power enhancement ratio (PER),  $E$ , where the efficiency,  $\eta$ , becomes zero. This maximum achievable PER,  $E_{MAX}$ , can be calculated from (4.11) to be

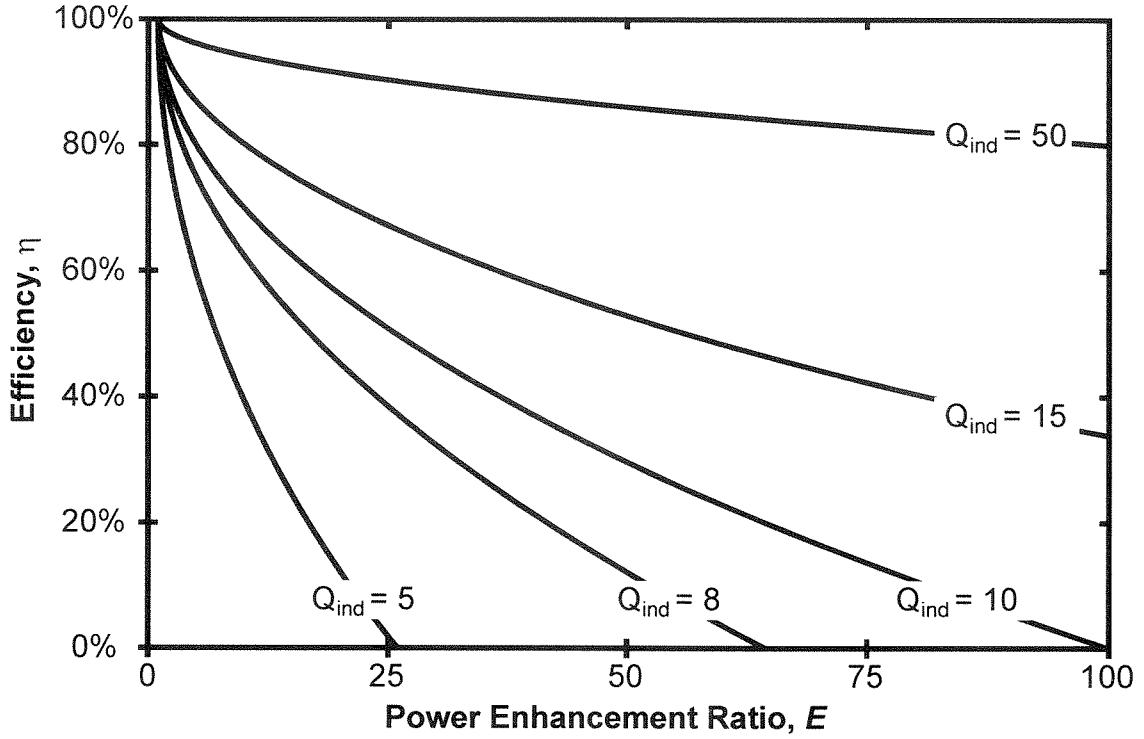


**Figure 4.3:** Required inductor reactance vs. power enhancement ratio and inductor  $Q$  for a resonant impedance transformation network.

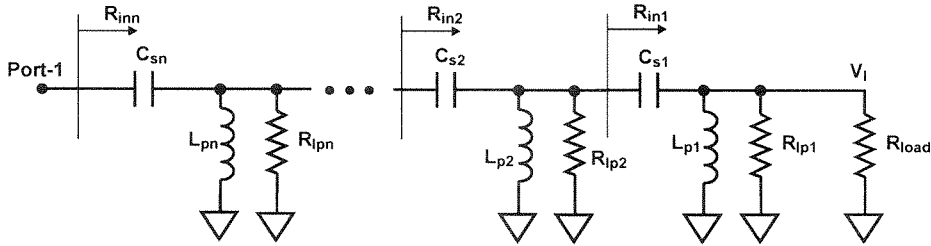
$$E_{MAX} = 1 + Q_{ind}^2 \quad (4.13)$$

Equation (4.13) provides an upper bound on the value of  $E$  in a single inductor-capacitor section. However, it should be noted that the efficiency would drop to zero as we approach this  $E_{MAX}$ , making this bound unachievable.

A similar analysis can be performed for the more general case of multi-section transformation with  $n$  segments, as shown in Figure 4.5. Assuming the same load enhancement ratio,  $E^{1/n}$ , for each individual section to have an overall power enhancement ratio (PER),  $E$ , the derivations in Appendix A lead to the following expression for passive efficiency:



**Figure 4.4:** Efficiency vs. power enhancement ratio and inductor  $Q$  for a single section resonant impedance transformation network.



**Figure 4.5:** Multi-section resonant LC impedance transformation network with loss.

$$\eta = \left( 1 - \frac{\sqrt{\frac{1}{E^n} - 1}}{Q_{ind}} \right)^2 \quad (4.14)$$

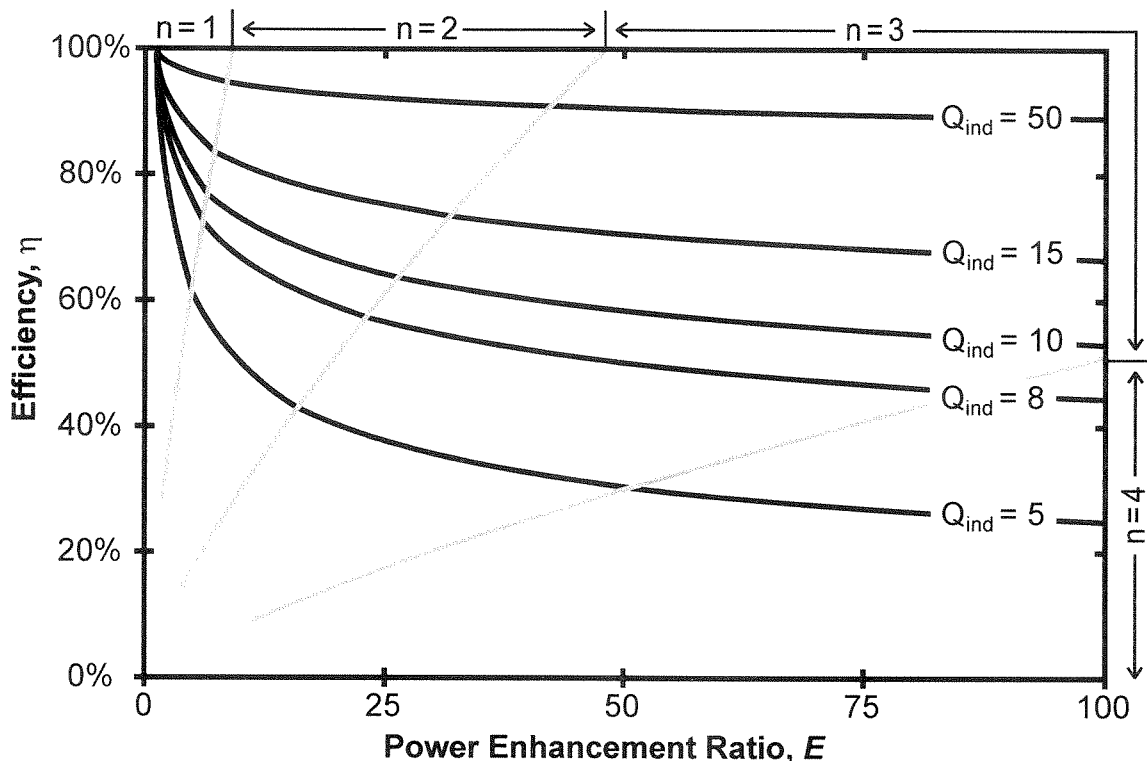
The inductance value for the  $k^{th}$  parallel inductor,  $L_{p,k}$ , in the chain can be calculated as follows:



$$\omega L_{p,k} = \left( \frac{1}{\sqrt{\frac{1}{E^n} - 1}} - \frac{1}{Q_{ind}} \right) \left( \frac{1 - \sqrt{\frac{1}{E^n} - 1}}{\frac{Q_{ind}}{E^n}} \right) R_{load} \quad (4.15)$$

In principle, the multi-section transformation network has a lower loss for high power enhancement ratio (PER) compared to a single section. However, it requires a more complex layout and some of its inductors will have very large or very small reactance compared to a single section. This results in a lower overall quality factor,  $Q$ , for the network. Figure 4.6 shows plots of  $\eta$  vs.  $E$  for several different values of  $Q_{ind}$  for a multi-section network. This figure only shows the efficiencies,  $\eta$ , for the number of sections leading to the minimum loss, so it can also be used to find the optimum number of sections. For example, we can see that with a power enhancement ratio (PER) of 50 and an inductor quality factor,  $Q_{ind}$ , of 10, the best matching network will have 3 LC-sections and will have a maximum passive efficiency of around 60%. Again, this figure does not include any loss in the active device, the dc feeds, or the external connections.

Equations (4.11) and (4.12) have important implications regarding the necessary reactance, transformation efficiency, and the power enhancement ratio (PER). In particular, (4.12) suggests that the inductor reactance necessary for this type of matching network with a single-section decreases rapidly as the desired power enhancement ratio (PER),  $E$ , is increased, as seen in Figure 4.3. More importantly, the transformation efficiency,  $\eta$ , also decreases quickly with higher power enhancement ratio (PER),  $E$ , as can be seen in Figure 4.4. In a multi-section approach, the loss is improved significantly compared to the single-section network, but still increases with higher power enhancement ratio,  $E$ , as can be seen from Figure 4.6. This analysis provides the theory for what PA designers have long understood by intuition and experience. The low  $Q$  passives currently available on chip fundamentally limit achievable power efficiencies at the

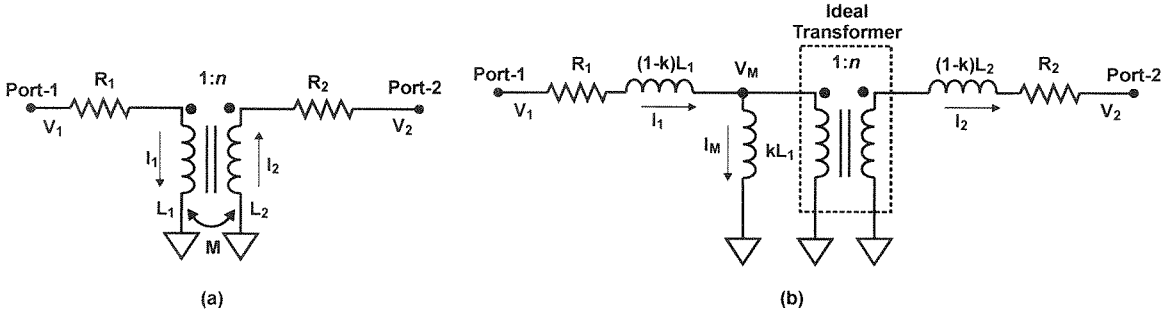


**Figure 4.6:** Efficiency vs. power enhancement ratio and inductor  $Q$  for a multi-section resonant network. Vertical gray lines separate regions using different number of sections. The best number of sections,  $n$  from 1 to 4, is chosen for the highest efficiency for different power enhancement ratios and inductor  $Q$ .

1-Watt level. No amount of complexity in an LC transformation network can overcome this limitation.

## 4.2 Magnetically Coupled Transformer

By magnetically coupling two inductors, we can create a coupled-inductor transformer. In a coupled-inductor transformer, the magnetic field created by the port-1 current,  $I_1$ , through the primary inductor,  $L_1$ , generates a voltage in the secondary inductor,  $L_2$ . At the same time, the current through the secondary,  $I_2$ , will magnetically induce a voltage in the primary circuit. The port voltages of the loosely-coupled lossy transformer,  $V_1$  and  $V_2$ , in Figure 4.7a are related to its port currents through:



**Figure 4.7:** a) Transformer model, b)Transformer equivalent T-model.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & -R_2 - j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (4.16)$$

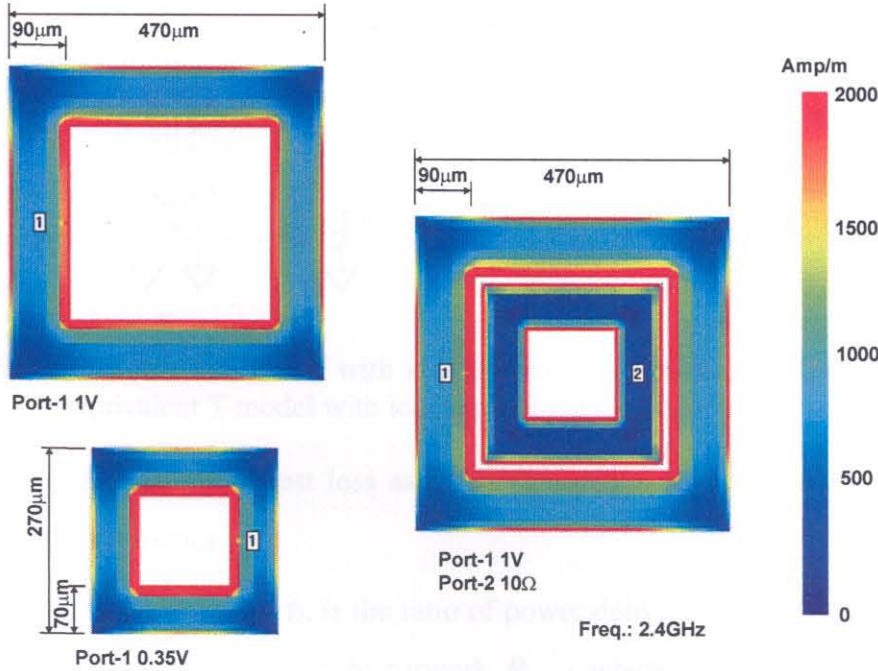
$$M = k\sqrt{L_1 L_2}$$

$$n = \sqrt{\frac{L_2}{L_1}} \approx \frac{I_1}{I_2} \approx \frac{V_2}{V_1}$$

where  $M$  is the mutual inductance,  $k$  is the coupling factor,  $r$  is the transformation ratio, and  $n$  is the turn ratio between primary and secondary coils. Figure 4.7b shows the equivalent model for the transformer of Figure 4.7a, where the lossy inductors of the transformer are modeled by the equivalent series resistors,  $R_1$  and  $R_2$ , and net inductances,  $L_1$  and  $L_2$  for a single frequency [51]. The quality factors,  $Q_1$  and  $Q_2$ , of the primary and the secondary inductors can be calculated in terms of  $R_1$  and  $R_2$  respectively, *i.e.*,

$$Q_1 = (\omega L_1)/R_1 \quad Q_2 = (\omega L_2)/R_2 \quad (4.17)$$

The quality factors of the coupled inductors are slightly different from those of the individual inductors due to the current redistribution that occurs on both inductors when they are coupled. This effect is shown in the current density graph of Figure 4.8, which shows the current densities in stand alone primary and secondary loops as well as the redistributed current densities due to their magnetic coupling. These graphs were obtained using the SONNET electromagnetic simulator [52].

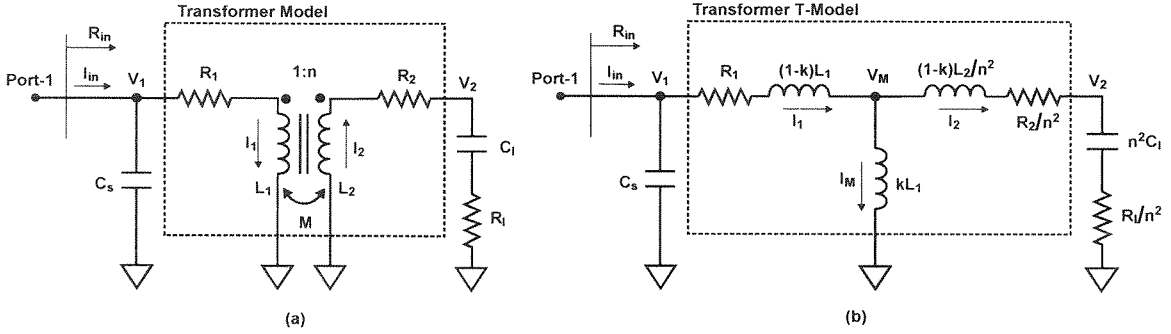


**Figure 4.8:** Current densities in planar one turn inductors and planar transformer.

The leakage inductances  $(1-k)L_1$  and  $(1-k)L_2$  can have a significant effect on the primary and secondary reactances if the coupling factor,  $k$ , is small. The factor  $k$  is low for on-chip spiral transformers because of the low permeability of the core material (e.g.,  $\text{SiO}_2$ ) and the planar geometry that results in large magnetic field leakage.

If a transformer is used to achieve output matching in a power amplifier, it will be necessary to resonate some of the transformer's inductance to minimize the loss. This effect is discussed in more detail in Appendix B. A capacitor is also necessary on the primary side of the transformer to adjust its input reactance to the desired value for the driving transistor. This can be done using a parallel capacitor on the primary and another capacitor in series with the secondary, as shown in Figure 4.9a, and its expanded form using the equivalent T-model in Figure 4.9b.

Now, we can use the equivalent model of Figure 4.9b to calculate the transformer efficiency,  $\eta$ , the best value of the series matching capacitor,  $C_b$ , and the best inductor



**Figure 4.9:** a) Transformer model with load and tuning capacitors, b) Transformer equivalent T-model with load and tuning capacitors.

values,  $L_1$  and  $L_2$ , for the lowest loss as a function of the load resistance  $R_l$  and other transformer characteristics.

The transformer efficiency,  $\eta$ , is the ratio of power delivered to the load,  $P_{load}$ , to the total power delivered into port-1 of the network,  $P_{total}$ , which is calculated in Appendix B to be

$$\eta \equiv \frac{P_{load}}{P_{total}} = \frac{R_l/n^2}{\left( \frac{\omega L_1/Q_2 + R_l/n^2}{\omega L_1} \right)^2 \cdot \frac{\omega L_1}{Q_1} + \frac{\omega L_1}{Q_2} + \frac{R_l}{n^2}} \quad (4.18)$$

This  $\eta$  is obtained assuming  $L_1 \cong L_2/n^2$  and using the optimum value of  $C_l$  given by

$$\frac{1}{\omega C_l} = \omega L_2 \quad (4.19)$$

Equation (4.18) can be differentiated to obtain the optimum value of  $L$  resulting in the highest possible  $\eta$ , which is

$$\omega L_1 = \frac{R_l}{n^2 \sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2} k^2}} = \frac{A \cdot R_l}{n^2} \quad (4.20)$$

where:

$$A \equiv \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2} k^2}} \quad (4.21)$$

Using this optimum  $L_I$ , the maximum efficiency will be given by

$$\eta = \frac{1}{1 + 2 \sqrt{\left(1 + \frac{1}{Q_1 Q_2 k^2}\right) \frac{1}{Q_1 Q_2 k^2} + \frac{2}{Q_1 Q_2 k^2}}} \quad (4.22)$$

The above equation shows that passive efficiency,  $\eta$ , can be maximized using a  $k$  as close as possible to unity. This is because the smaller the  $k$ , the larger fraction of the primary inductor current,  $I_I$ , will go through the magnetizing inductor,  $kL_I$ , and hence a lower power will be delivered to the load resistor. More importantly, unlike resonant matching, the transformer efficiency is not affected by the transformation ratio, as seen in (4.22)<sup>1</sup>. Figure 4.10 shows how the transformer efficiency is reduced when the reactance of the inductor is above or below the optimum value determined by (4.20). Several plots of  $\eta$  vs.  $\omega L_I$  are shown for a 50- $\Omega$  load and a peak power enhancement ratio (PER),  $E$ , of 50. For each plot, a fixed  $r$  is used in order to have  $PER=50$  for peak  $\eta$ . In these plots,  $Q_I$  and  $Q_2$  are assumed to be equal to facilitate visualization.

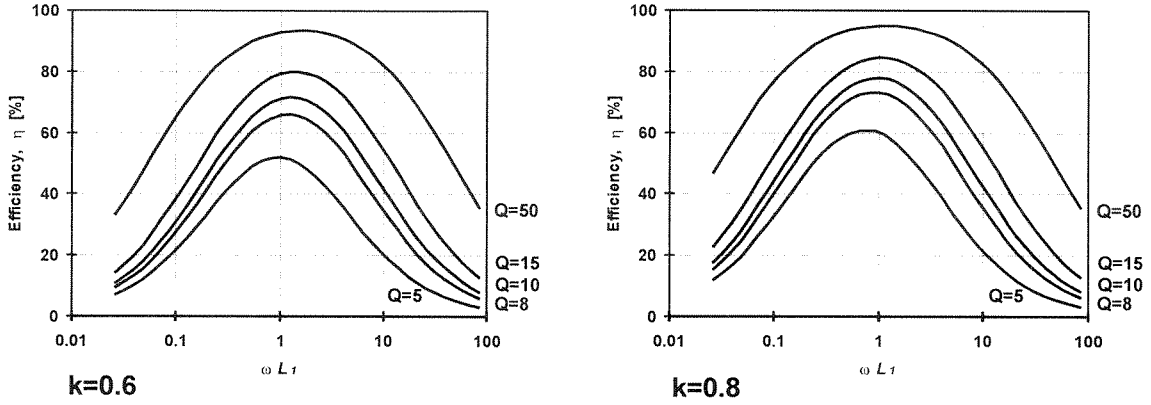
The equivalent input admittance of the transformer for the optimum values of  $C_I$  and  $L_I$  given by (4.19) and (4.20) can be calculated to be

$$Y_{in} \equiv \frac{1}{Z_{in}} = G_{in} + jB_{in} \approx \frac{Q_1}{\frac{Q_1}{k^2} + Q_2} \left( \frac{n^2}{R_I} + j \frac{1}{\omega L_I} \right) \quad (4.23)$$

We now calculate the transformer turn ratio,  $n$ , for a desired power enhancement ratio (PER),  $E$ , using (10) and (23), using the assumption  $k^2 Q_I Q_2 \gg 1$ :

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1. Except to the degree that  $L_I$ ,  $L_2$ ,  $k$ ,  $Q_I$ , and  $Q_2$  change with  $r$ .



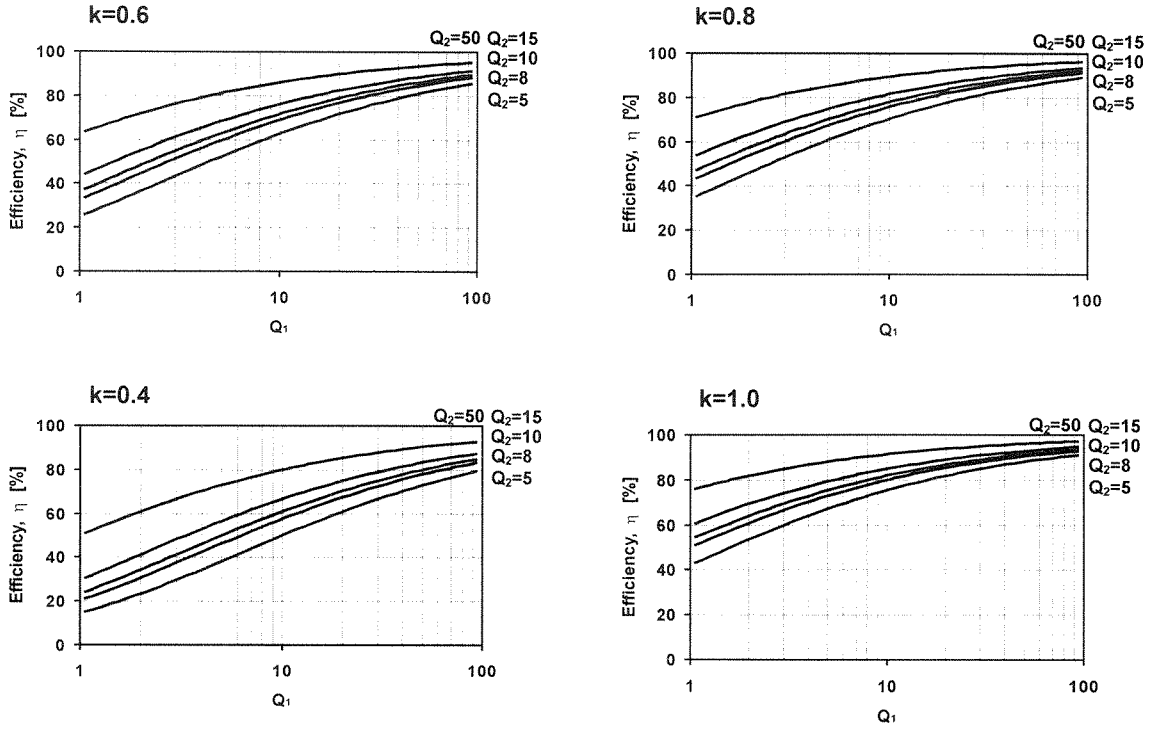
**Figure 4.10:** Efficiency vs. primary inductor reactance normalized to load resistance, inductor  $Q$ , and coupling factor  $k$ , for a transformer with loss.

$$E = \eta \frac{R_l}{(1/G_{in})} \approx \eta \frac{n^2 Q_1}{\frac{Q_1}{k^2} + Q_2} \quad (4.24)$$

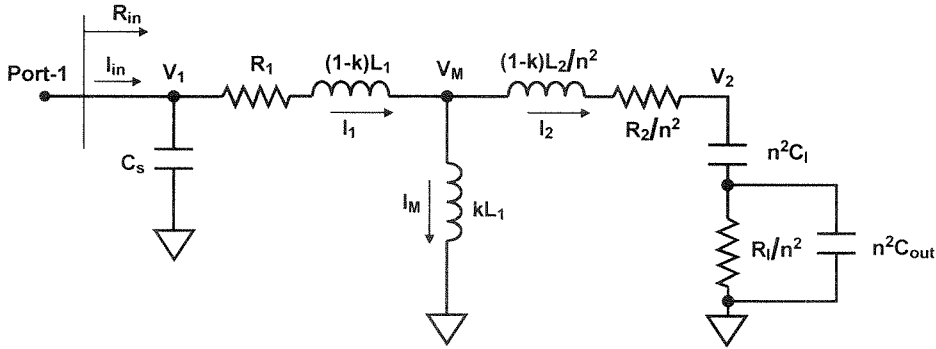
$$n \approx \sqrt{\frac{E(Q_1/k^2 + Q_2)}{\eta Q_1}} \quad (4.25)$$

Figure 4.11 shows plots of  $\eta$  vs.  $Q_1$  and  $Q_2$  for  $k=0.4, 0.6, 0.8$ , and 1 using (4.22). As an example, to obtain a transformation ratio of 50 with primary and secondary inductor quality factors of 10 and a  $k$  of 0.6, the transformer primary circuit should have an impedance of approximately  $1j\Omega$  at the frequency of operation to achieve the highest efficiency. In this case,  $n$  should be approximately 8 and the best achievable passive efficiency is 70%.

Although a single series capacitor with the load can provide the necessary negative reactance to resonate the inductive output of the transformer, an additional capacitor  $C_{out}$  parallel to the load (Figure 4.12) can be used to adjust the real part of the impedance seen by the secondary of the transformer to lower its loss. This extra degree of freedom can be used to obtain a lower turn ratio,  $n$ , and a lower primary inductance,  $L_2$ , for a given load resistance and power enhancement ratio (PER),  $E$ .



**Figure 4.11:** Efficiency vs. primary inductor  $Q_1$ , secondary inductor  $Q_2$ , and coupling factor,  $k$ , for a transformer with loss.



**Figure 4.12:** Transformer equivalent T-model for analysis with load, tuning capacitors, and extra tuning capacitor parallel to the load.

Equations (4.22), (4.24), and (4.25) determine the optimum value of  $\eta$ , and the resultant  $E$  and  $n$  for  $C_{out}=0$ . We can recalculate these parameters for the other limiting case, when  $C_l$  is large ( $C_l=\infty$ ), using (4.10), (4.16), (4.19), (4.20), and (4.24). The new PER,  $E$ , is



$$E \approx (1 + A^2) \eta \frac{n^2 Q_1}{\frac{Q_1}{k^2} + Q_2} \quad (4.26)$$

which is obtained for a  $C_{out}$  and an  $L_I$  given by

$$\begin{aligned} \frac{1}{\omega C_{out}} &= \frac{AR_I}{1 + A^2} \\ \omega L_I &= \frac{1}{1 + A^2} \frac{AR_I}{n^2} \end{aligned} \quad (4.27)$$

The new input admittance is

$$Y_{in} \approx \frac{1}{1 + A^2} \frac{Q_1}{\frac{Q_1}{k^2} + Q_2} \left( \frac{n^2}{R_I} + j \frac{1}{\omega L_I} \right) \quad (4.28)$$

The new turn ratio  $n$  in this case will be

$$n \approx \sqrt{\frac{1}{1 + A^2} \frac{E(Q_1/k^2 + Q_2)}{\eta Q_1}} \quad (4.29)$$

The efficiency,  $\eta$ , of this new setup is still given by (4.22). Note that plots of Figure 4.11 are still valid since they are calculated in terms of quality factors. The maximum PER is achieved when  $C_I$  is very large. This maximum PER given by (4.26) is  $(1 + A^2)$  times larger than (4.24)<sup>1</sup>.

In the design process, we start from a given transistor and a given power level that has to be delivered to the load. These two conditions determine the desired value of the PER,  $E$ . Once this  $E$  is achieved, there is no point in increasing it beyond the required value, and we should maximize the efficiency,  $\eta$ , instead. As can be seen from (4.29), the addition of the parallel capacitor,  $C_{out}$ , makes it possible to use smaller turn ratio,  $n$ , for a desired  $E$ .

---

1. In practice, there is no need for  $C_I$  as the transformer dc isolation between the input and output ports allows us to short circuit  $C_I$ .

Typically, a lower  $n$  results in a higher quality factor in magnetically coupled transformers, which translates to a higher efficiency, as can be seen from (4.22).

A capacitor  $C_s$  parallel to the transformer input completes this circuit. It tunes the reactive part of the transformer input impedance to the desired value appropriate to provide the required drain or collector impedance for the chosen class of the amplifier<sup>1</sup>.

Using the above analysis, we can compare the performance of a magnetically-coupled transformer with an LC-based resonant impedance transformation discussed in Section II. Unlike the resonant LC matching circuit, in a magnetically-coupled transformer the efficiency,  $\eta$ , does not depend on the PER,  $E$ , and hence does not drop for larger output power level, as can be seen from (4.11) and (4.22). The implicit assumption is that the quality factors do not change with larger  $n$ , which may not be correct as mentioned earlier. These equations shown graphically in figures 6 and 10 also show that for a PER above 15, the magnetically-coupled transformer provides a higher efficiency,  $\eta$ , than the resonant matching for a given  $Q$ .

This difference in behavior arises from a fundamental difference between the LC resonant and magnetically coupled transformer matching, which can be understood using a simple model. In both approaches, in order to achieve a high PER, the input ac current,  $I_{in}$ , has to be larger than the output ac current,  $I_{out}$ , and the output ac voltage,  $V_{out}$ , has to be larger than the input ac voltage,  $V_{in}$ , both by  $\sqrt{r}$ , approximately<sup>2</sup>. In a resonant matching network, the loss is proportional to the product of  $I_{in}$  and  $V_{out}$ , which are both large. On the other hand, while in a magnetically-coupled transformer, there are two loss components, namely,  $i_{in}v_{in}$  and  $i_{out}v_{out}$ , each one is smaller than the single loss component in the case of a resonant matching by  $\sqrt{r}$ . Therefore, loosely speaking, the loss of the resonant matching circuit is larger by a factor of  $\sqrt{r}/2$ .

---

1. Although the tuning capacitor could be placed in series, biasing issues usually favor the parallel setting. However, the series arrangement has the advantage of resulting in yet smaller  $n$ .

2. In a transformer,  $\sqrt{r} \approx n$ .

In a properly designed impedance transformation network using magnetically-coupled transformers, the reactance of the primary inductor,  $\omega L_1$ , is approximately the load resistance that should be seen by the active device, as seen in (4.20). Similarly, the reactance of output inductor,  $\omega L_2$ , will be approximately the load resistance. Additionally, a negative reactance in series with the load is necessary to achieve the highest possible efficiency. This negative reactance can be generated by a combination of a series and a parallel capacitor, as shown in Figure 4.12. These observations are particularly important for the *distributed active transformer* (DAT) structure introduced in the Chapter 5.

The disadvantage of a magnetically-coupled transformer is the low primary inductance necessary to achieve the highest efficiency. If spiral transformers on a silicon substrate were to be used, the small primary inductance results in extremely short metal lines. For instance, the necessary inductance to achieve an  $E$  of 50 into a  $50\text{-}\Omega$  load is approximately 80pH at 2GHz. Inter-winding these short primary metal lines with the multi-turn secondary forces them to be very narrow. Unfortunately, this reduces the  $Q$  of both primary and secondary circuits, significantly. Noting the limitations of these two conventional impedance transformation methods, we introduce an alternative solution, which does not suffer from these shortcomings.

### 4.3 Transmission Line Impedance Transformation

As described in Section 3.1.1, transmission lines may be used in several different ways to accomplish an impedance transformation. But any transmission line circuit requires several lines with lengths comparable to quarterwave-length [53], which, on a conductive silicon substrate, unfortunately, leads to a prohibitive high power attenuation.

We can see in Table 4.2, an illustrative example of how serious this power attenuation is. Several microstrip transmission line physical characteristics,  $\gamma$ ,  $Z_o$ , and power attenuation<sup>1</sup> of a quarterwave-length line at 2.4GHz [29] were obtained from a planar 3-D simulation using Sonnet [52]. The substrate characteristic were chosen to be typical of a

conventional analog CMOS process and a metal ground plane with the same conductivity as the metal line was assumed to exist below the substrate. Table 4.1 shows the process characteristics.

Line Width ( $\mu\text{m}$ )	$Z_o$ ( $\Omega$ )	$\gamma$ ( $\text{m}^{-1}$ )	$\epsilon_{eff}$	$\lambda/4$ @2.4 GHz (mm)	$\lambda/4$ atten. @2.4Gz (%)
10	90.7+2.05j	25+191j	14-4j	8	67
30	59.9+10.6j	51+222j	19-9j	7	49
50	49.9+11.0j	60+231j	20-11j	7	43
100	37.4+10.6j	75+247j	22-15j	7	35
300	23.8+8.3j	89+248j	21-17j	7.5	26
500	19.2+6.6j	83+237j	21-16j	7.5	28
1000	13.3+3.8j	70+241j	21-13j	7	37

**Table 4.1:** Electrical characteristics of microstrip lines on a typical bulk silicon substrate with metal ground below the substrate.

Description	Value
Metal Thickness	3 $\mu\text{m}$
Metal Conductivity	10m $\Omega$ /sq.
Metal Type	Al
Oxide Thickness	4.39 $\mu\text{m}$
Oxide $\epsilon_r$	4.0
Substrate Thickness	300 $\mu\text{m}$
Substrate $\epsilon_r$	11.9
Substrate Resistivity	8 $\Omega$ .cm

**Table 4.2:** Process characteristic of a typical bulk silicon process as used in the simulation for results of Table 4.1.

---

1. Power obtained at port-2 divided by power injected at port-1 of a matched transmission line.

The results shown in Table 4.1 clearly demonstrate that practice transmission line circuits cannot be used in a conventional way for power amplifiers using a conventional silicon substrate due to an unacceptable high loss.

## Chapter

## 5

*Distributed Active Transformer*

As described in the previous sections, there are many challenges in designing a watt-level power amplifier in CMOS. The *distributed active-transformer* (DAT) addresses these problems reducing their effects significantly, thus allowing the design of a truly fully-integrated power amplifier realizable using sub-micron CMOS technology.

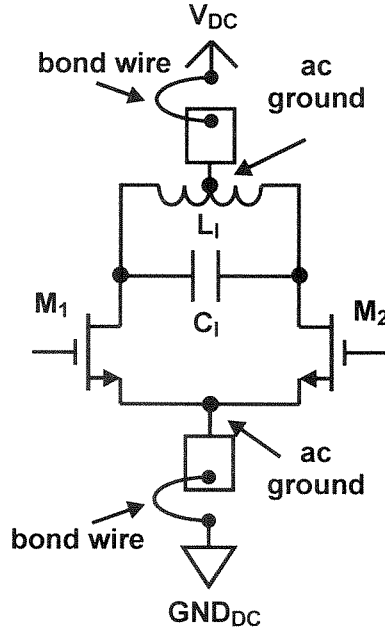
This DAT combines several low-voltage push-pull amplifiers efficiently in series to produce a larger output power while maintaining a  $50\Omega$  match. It also uses virtual ac grounds and magnetic couplings extensively to eliminate the need for any off-chip component such as inductors, capacitors, and tuned wire-bond inductors. Furthermore, it desensitizes the operation of the amplifier to the inductance of bonding wires and makes the design more reproducible.

This section describes the design evolution leading to the distributed active-transformer power amplifier. It is worthwhile to note that although the approach is described for MOSFETs here, this architecture may be implemented in a similar way using other technologies such as BJTs (bipolar junction transistor), MESFETs (metal-semiconductor field effect transistors), or HEMTs (high electron mobility transistors).

## 5.1 Double Differential Driver

The basic building block of the new topology is the push-pull amplifier shown in Figure 5.1. This topology creates a virtual ac ground at the power supply and ground. Because these virtual ac grounds are created by symmetry, they are inherently low loss and low impedance. They also avoid the need for a lossy on-chip choke inductor. The con-

nection from these ac virtual grounds to the positive supply and ground will carry only current at dc and even harmonics, thus eliminating the loss caused by the rf signal at the fundamental frequency and odd harmonics going through lossy supply lines. Furthermore, this effect desensitizes the operation of the amplifier to the inductances of bonding wires making the design more reproducible. It also eliminates the need for a large on-chip bypass capacitor on the supply.



**Figure 5.1:** Push-pull amplifier using two NMOS transistor with a common ground.

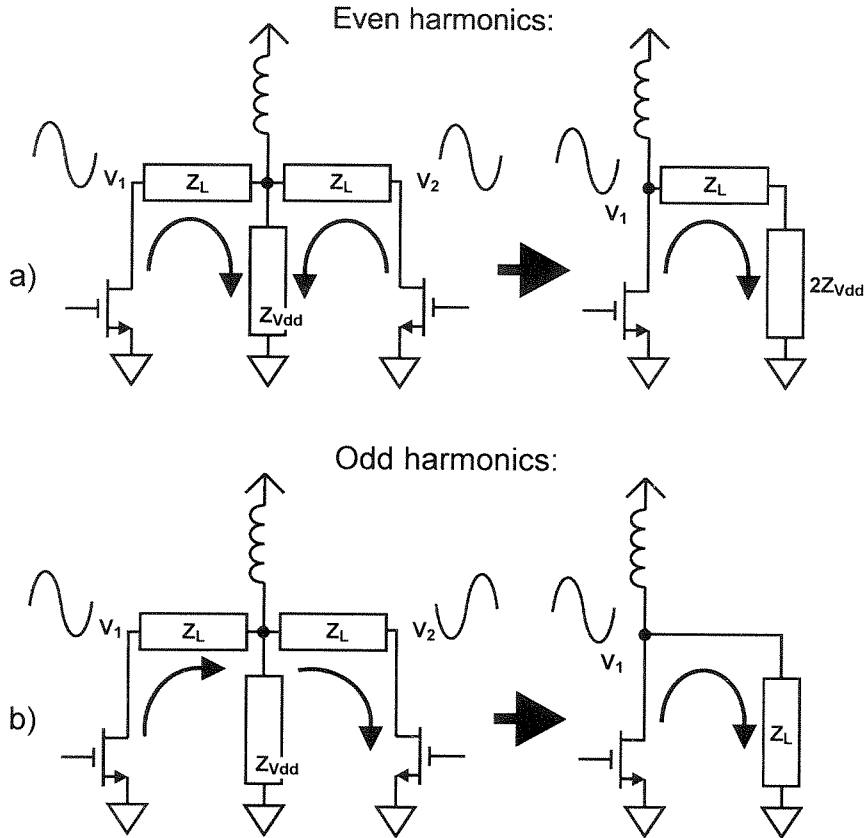
Figure 5.2a and Figure 5.2b show a push pull amplifier illustrating the impedances seen by even and odd harmonics, respectively. The differential output signal,  $V_1 - V_2$ , does not contain any even harmonic components due to symmetry, as demonstrated by the following equations:

$$V_1 = A_1 \cos(\omega t + \theta_1) + A_2 \cos(\omega t + \theta_2) + A_3 \cos(\omega t + \theta_3) + \dots \quad (5.1)$$

$$V_2 = A_1 \cos(\omega t + \theta_1 + \pi) - A_2 \cos(\omega t + \theta_2 + \pi) - A_3 \cos(\omega t + \theta_3 + \pi) + \dots \quad (5.2)$$

$$V_1 - V_2 = 2A_1 \cos(\omega t + \theta_1) + 2A_3 \cos(\omega t + \theta_3) + \dots \quad (5.3)$$

where  $A_n$  and  $\theta_n$  are the magnitude and phase of the  $n^{\text{th}}$  harmonic at the drain of transistor 1, and  $\omega$  is the fundamental angular frequency. The elimination of the even harmonics, specially the  $2^{\text{nd}}$ , by the circuit symmetry allows for the use of a lower loaded  $Q$  – and therefore lower loss – resonant circuit at the drain for harmonic suppression as it only needs to suppress odd harmonics.



**Figure 5.2:** Impedances of even and odd harmonic signals in a push-pull amplifier.

If switching modes of operation are desirable, the differential symmetry of this topology provides high impedances,  $\sim 2Z_{Vdd}$ , at each even harmonic to the transistor drains regardless of the impedances of the output resonant network,  $Z_L$ , at these frequencies, as shown by Figure 5.2a. The transistor drain impedances at odd harmonics will be  $Z_L$ , as can be seen in Figure 5.2b and the following equations



$$Z_{even} = \frac{V_1}{I_1} = \frac{I_1 Z_l + (I_1 + I_2) Z_{vdd}}{I_1} = \frac{I_1 Z_l + 2I_1 Z_{vdd}}{I_1} = Z_l + 2Z_{vdd} \approx 2Z_{vdd} \quad (5.4)$$

$$Z_{odd} = \frac{V_1}{I_1} = \frac{I_1 Z_l + (I_1 - I_2) Z_{vdd}}{I_1} = \frac{I_1 Z_l}{I_1} = Z_l \quad (5.5)$$

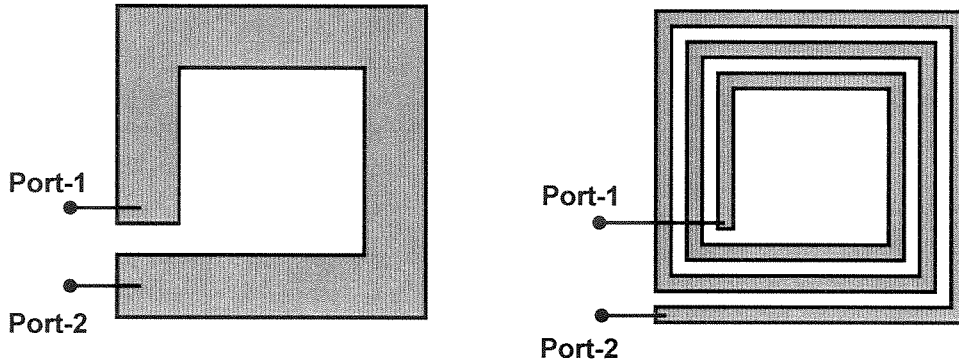
By providing a short circuit between the drains at odd harmonics using a simple parallel LC tank tuned to a frequency slightly above the fundamental frequency, the drain impedance will be inductive at the fundamental and will be small at odd harmonics and large at even harmonics. If transistors are driven into saturation, these impedances shape the drain waveforms to perform the high efficiency class E/F<sub>odd</sub> operation [21].

## 5.2 Design of a Low Impedance Inductor

As just seen in the previous section, inductors are essential blocks to design amplifiers from drain harmonic impedance control inductors to various forms of impedance transformation networks and their properties can significantly affect the performance of such networks, as discussed earlier in Chapter 4.

Spiral inductors [13][16][50] have been widely used in radio frequency integrated circuits. They can be single-turn or multi-turn, as shown in Figure 5.3. For a spiral inductor the negative magnetic coupling between the opposite sides of the polygon lowers its total equivalent inductance. However, this inductance reduction by negative mutual coupling does not occur when the distance between the opposite sides of the spiral is significantly larger than the mirror current penetration depth of the transmission line in the substrate.

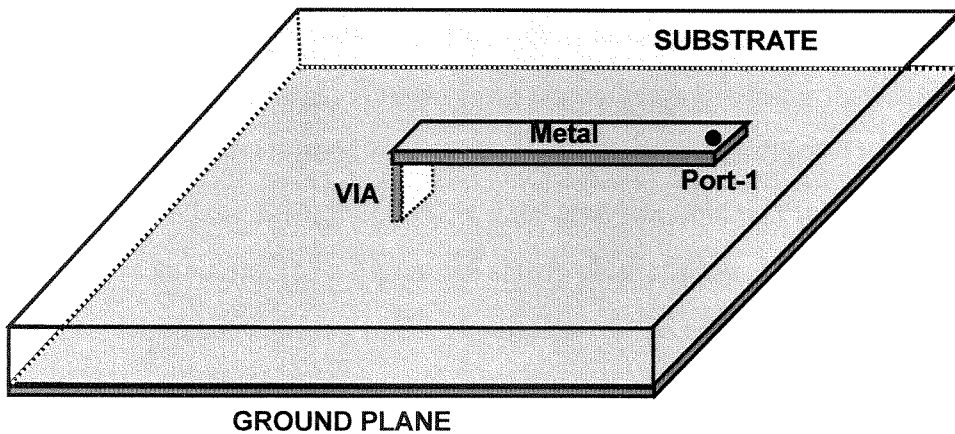
In a single turn inductor with larger spacing between its opposite sides, the substrate (back plane) mirror current limits the inductance per metal length. Therefore, it behaves similarly to a microstrip transmission line of the same length. Also, the proximity of the opposite terminals of the inductor provides an alternative current path through the shunt capacitors and the substrate that increases the loss.



**Figure 5.3:** Planar one-turn and multi-turn spiral inductors.

If we use more than one turn to form a spiral inductor, the positive magnetic couplings between the conductors in the same side of the polygon enhance the total equivalent inductance<sup>1</sup>.

We can also build an inductor using a short transmission line with one of its terminals short-circuited to the ground, as in Figure 5.4. Standard transmission line analysis can be used to calculate the inductance and the  $Q$  of this inductor [29]



**Figure 5.4:** Inductor made by a short microstrip transmission line terminated with a short to ground.

1. The multi-turn spiral inductor also suffers from a larger parasitic capacitance between adjacent turns that lowers its self-resonant frequency.

$$Z_{ind} = Z_o \tanh(\gamma l) \approx Z_o \left( \gamma l - \frac{1}{3}(\gamma l)^3 \right) \quad (5.6)$$

where  $Z_o$  and  $\gamma$  are transmission line's characteristic impedance and complex propagation constant given by

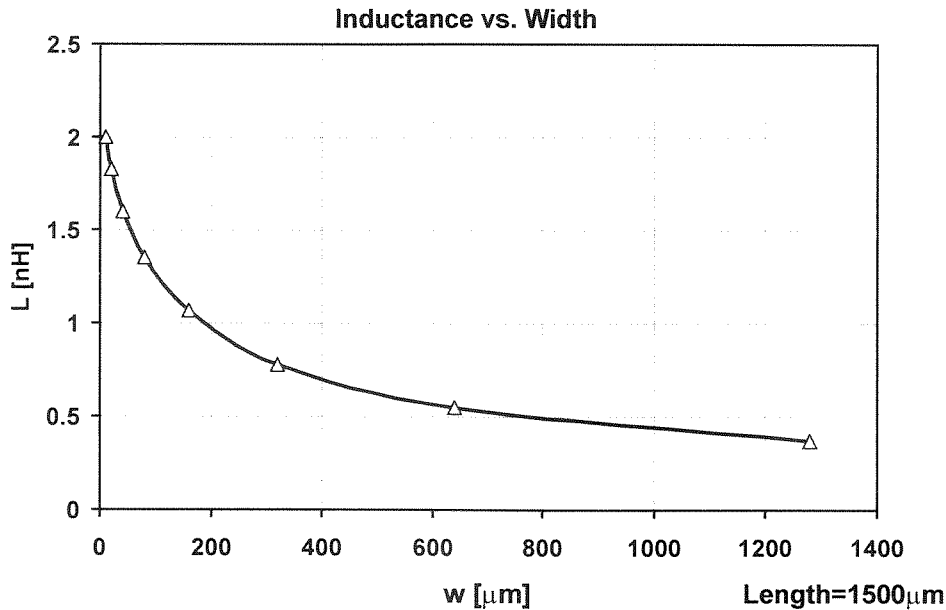
$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (5.7)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (5.8)$$

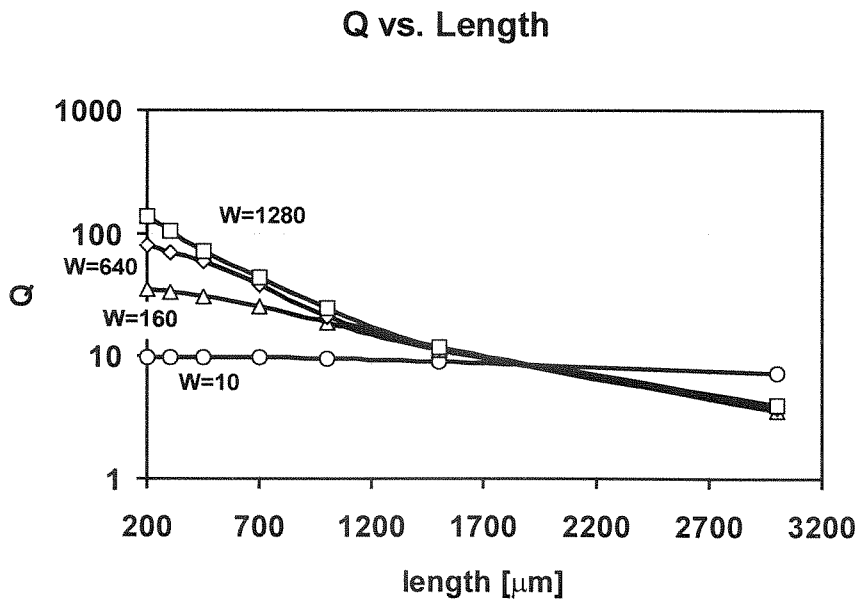
where  $R + j\omega L$  and  $G + j\omega C$ , are the series impedance and shunt admittance per unit length, respectively. Equation (5.6) shows that the inductance is proportional to the transmission line characteristic impedance and its length. If the substrate has a low resistivity (e.g., in silicon), the loss terms in (5.7) will be large which results in a relatively small inductor quality factor. In practice, it is very difficult to obtain analytical expressions for these loss components due to the non-uniformity of the conductor and substrate mirror current components, and one should resort to simulation methods such as the one discussed in [24].

For small lengths, the inductance of the microstrip transmission line inductor is proportional to its length,  $l$ , as shown in (5.6). Also, smaller line width,  $w$ , increases  $Z_o$ , and hence raise the inductance,  $L$ . However, the dependence is weaker than linear due to the mutual coupling between parallel current components on the line. This behavior is shown in Figure 5.5 where  $L$  is plotted vs.  $w$ . This plot was obtained for a silicon process using a planar E/M simulator [52]. Figure 5.6 shows plots of  $Q$  vs.  $l$  for different values of  $w$ . The process characteristics used in the simulation can be seen in Table 4.2. Figure 5.6 shows that series metal resistance,  $R$ , is the dominant loss factor for a narrow line (small  $w$ ) and hence  $Q$  is approximately constant as a function of  $l$ . This is because both the series resistance and the inductance are proportional to  $l$ , thus their ratio,  $Q$ , remains constant, *i.e.*,

$$Q = \frac{\text{Im}(Z_{ind})}{\text{Re}(Z_{ind})} \propto \frac{\omega L l}{R l} = \omega \frac{L}{R} \quad (5.9)$$



**Figure 5.5:** Simulated inductance vs. width of a short circuit microstrip line inductor with length=1.5 mm on a bulk silicon substrate.



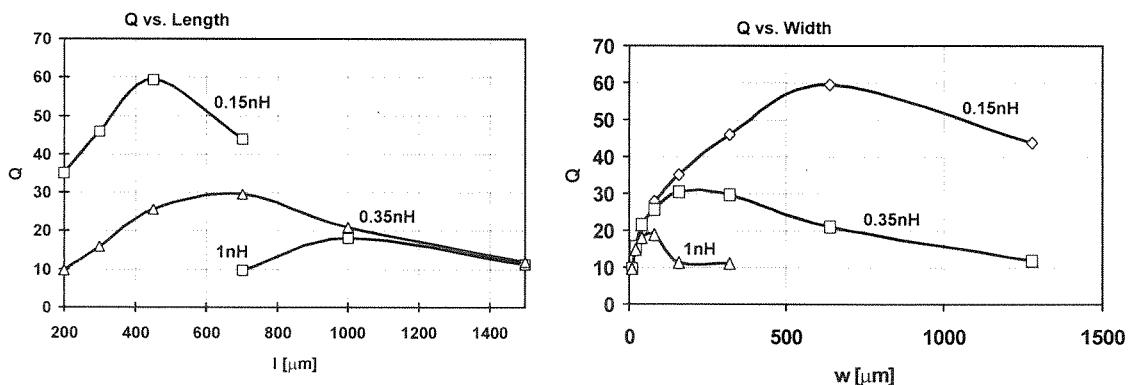
**Figure 5.6:** Simulated  $Q$  vs. length and width of short circuit microstrip line inductors on a bulk silicon substrate.

On the other hand, the shunt elements,  $G$  is the dominant loss factor for a wide line (large  $w$ ). In this case,  $Q$  decreases almost quadratically with increasing  $l$ , because both the series inductance and shunt-conductance scale with  $l$ , i.e.,

$$Q = \frac{\text{Im}(Y_{ind})}{\text{Re}(Y_{ind})} \propto \frac{1/(\omega Ll)}{Gl} = \frac{1}{\omega LGl^2} \quad (5.10)$$

Figure 5.6 shows this behavior, where  $Q$  for  $w=10\mu m$  is almost constant with  $l$ , while it drops with  $l$  rapidly for  $w=1280\mu m$ . Consequently, we can conclude that microstrip inductor  $Q$  increases with increasing  $w$  when it is short and  $Q$  degrades with increasing  $w$  when the line is long, as illustrated in Figure 5.6.

Based on this argument, we can find the  $w$  and  $l$  that maximize the  $Q$  for a desired inductance. This optimum  $Q$  is plotted as functions of  $l$  and  $w$  in Figure 5.7. The lower the inductance, the wider and shorter the optimum  $Q$  inductor. It should be noted that the optimum  $Q$  of a slab<sup>1</sup> inductor with small  $L$  is much larger than typical quality factors of large spiral inductors, as shown in Figure 5.7.



**Figure 5.7:** Simulated  $Q$  vs. length and inductance and  $Q$  vs. width and inductance of short circuit microstrip line inductors on a bulk silicon substrate. In the first plot, for each metal length, the width, which provides the selected inductance, is chosen. In the second plot, for each metal width, the length, which provides the selected inductance, is chosen.

1. Slab inductors are two port inductors formed by a straight piece of metal, opposite to curled metal used in one or two port spiral inductors.

Based on these results, we can compare the three different types of inductor, namely, slab, single-turn, and multi-turn inductors. The following guidelines can be used to obtain the best type of inductor in most practical applications.

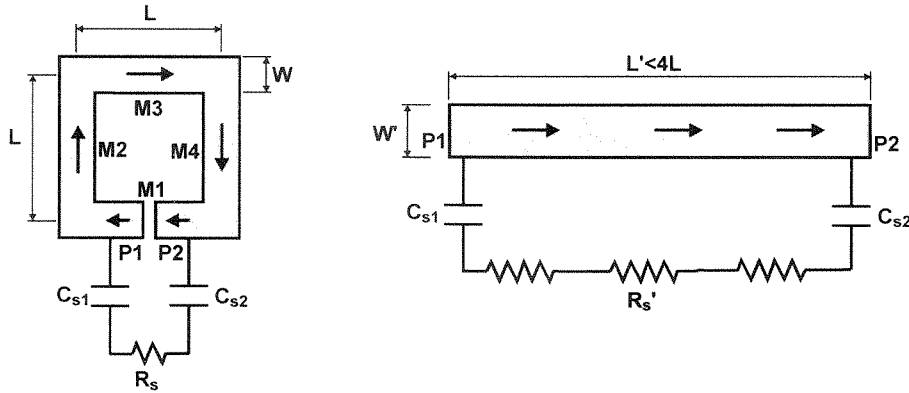
If for a given  $L$  the reactance of a slab inductor,  $\omega L$ , is much smaller than the transmission line characteristic impedance  $Z_0$ , it will have a higher  $Q$  compared to spiral inductors. On the other hand, if the desired reactance of the inductor is larger or comparable to  $Z_0$ , multi-turn spiral inductors should be used. One exception is when the transmission line is very low loss. In this case, a single ended high- $Q$  inductor can be obtained using a transmission line shorter than quarter wavelength with one of its terminals grounded. In this case, the slab inductor is still preferred.

Another issue is that the terminals of a slab inductor are not adjacent to each other and this may preclude their use in certain applications. It is interesting to note that the slab inductors always outperform single loop inductor in terms of  $Q$ , and therefore are always preferable unless two adjacent terminals are necessary.

DAT uses slab inductors as drain inductor of the push-pull blocks, as on-chip slab inductors present a significantly higher  $Q$  and consequently lower loss when compared to conventional low impedance single turn spiral inductors, as described in the previous section.

We can obtain further insights about the properties of slab inductors by their investigated loss properties. Several factors contribute to their higher  $Q$ . First, the negative mutual inductance between the current through metals on the opposite side of the spiral are reduced. Hence, the total metal length to obtain the same inductance is shorter than the circumference of the loop. Therefore, the resultant inductor demonstrates a lower total series metal resistance, as shown in Figure 5.8. Second, the shunt resistance through the substrate between the two terminals of the inductor,  $P_1$  and  $P_2$ , will be higher because of the larger distance between them as illustrated in Figure 5.8. Thus, the substrate current and power loss caused by it will be reduced. Third, the metal width of the inductor may be

increased beyond the maximum set by the spiral geometry. With wider metal, the series metal resistance is reduced although capacitive coupling to the substrate is increased. This allows a better optimization of the inductor and in many cases the total loss can be significantly reduced.



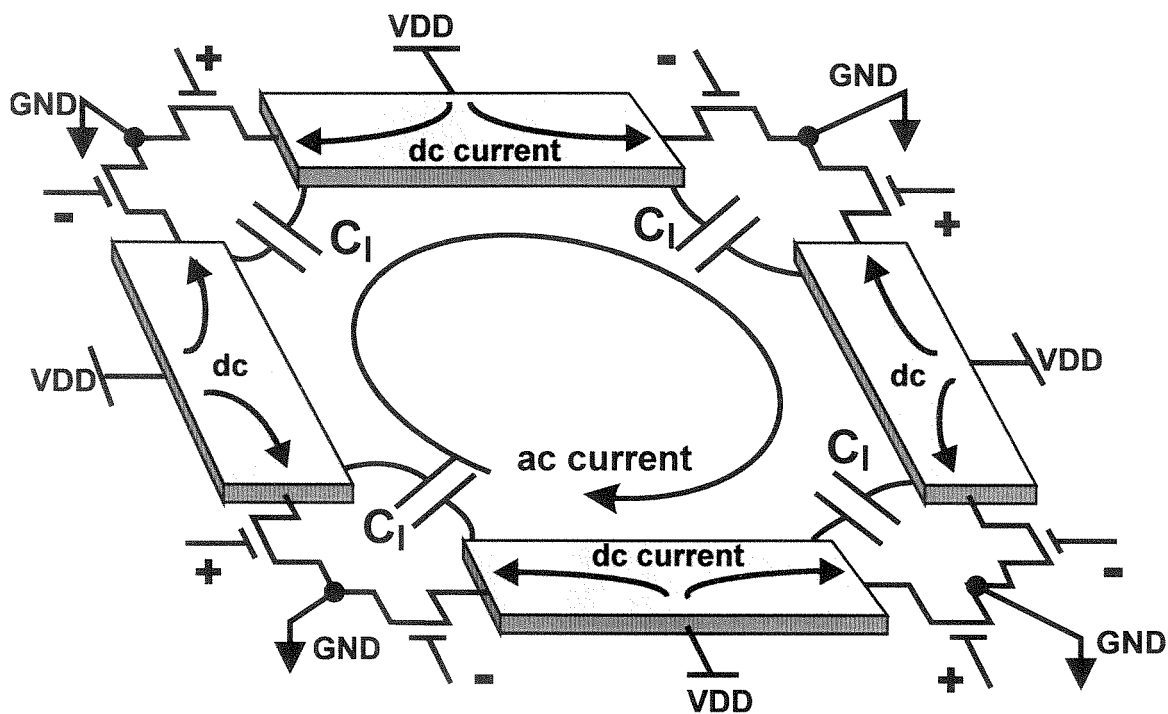
**Figure 5.8:** Comparing some of the loss mechanism of one-turn planar spiral inductor and slab inductor.

A slab inductor is used as drain inductor,  $L_I$ , of Figure 5.1. It also provides a path for the dc supply current.

### 5.3 Circular Geometry

Circular-geometry is a means to create low-loss, low-impedance virtual ac grounds while using several power amplifier blocks simultaneously. For instance, Figure 5.9 shows the primary circuits with four push-pull power amplifiers and eight transistors.

This architecture allows the creation of virtual ac grounds without having to connect together the sources of the pair of transistors of each push-pull amplifier, as shown in Figure 5.1. With slab inductors, this connection is physically impossible, without compromising the amplifier operation, as the slab inductors create a large distance between the sources. If a long metal line is used to connect the sources of this pair of transistors, the inductance of this metal will be comparable to that of the drain slab

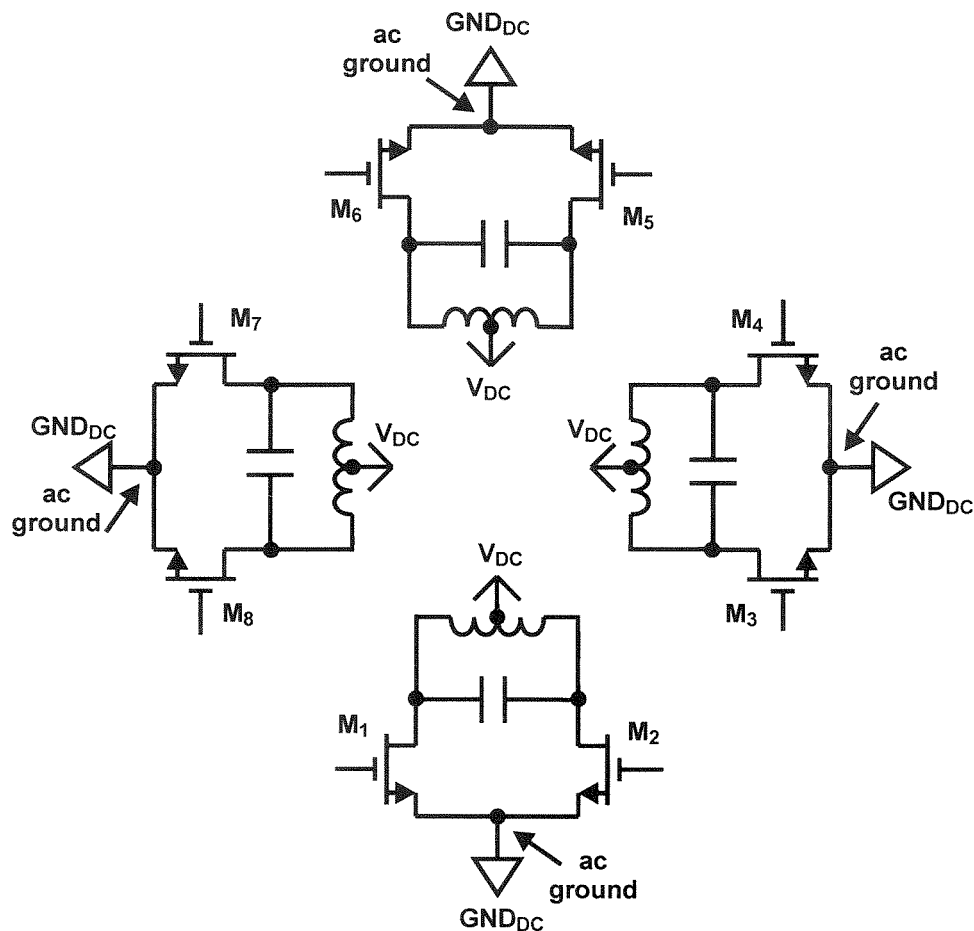


**Figure 5.9:** Primary circuit of a DAT with four push-pull power amplifiers and eight NMOS transistors.

inductor. The resulting source degeneration inductor will seriously degrade the amplifier performance and hence should be avoided.

Ac virtual grounds for the fundamental and all odd harmonics can be created in the corner points of the circular-geometry by connecting together the sources of the transistors of the adjacent push-pull amplifiers. By driving these transistors in opposite phase, as shown in Figure 5.2, their source currents, which belong to different push-pull amplifiers, have the same amplitude and the opposite phase and therefore cancel each other. The result is similar to connecting the sources of the pair of transistors belonging to the each push-pull amplifier with short low impedance connection. Two electrical diagrams show how four push-pull amplifiers of Figure 5.10 are rearranged to form the circular geometry of Figure 5.11.

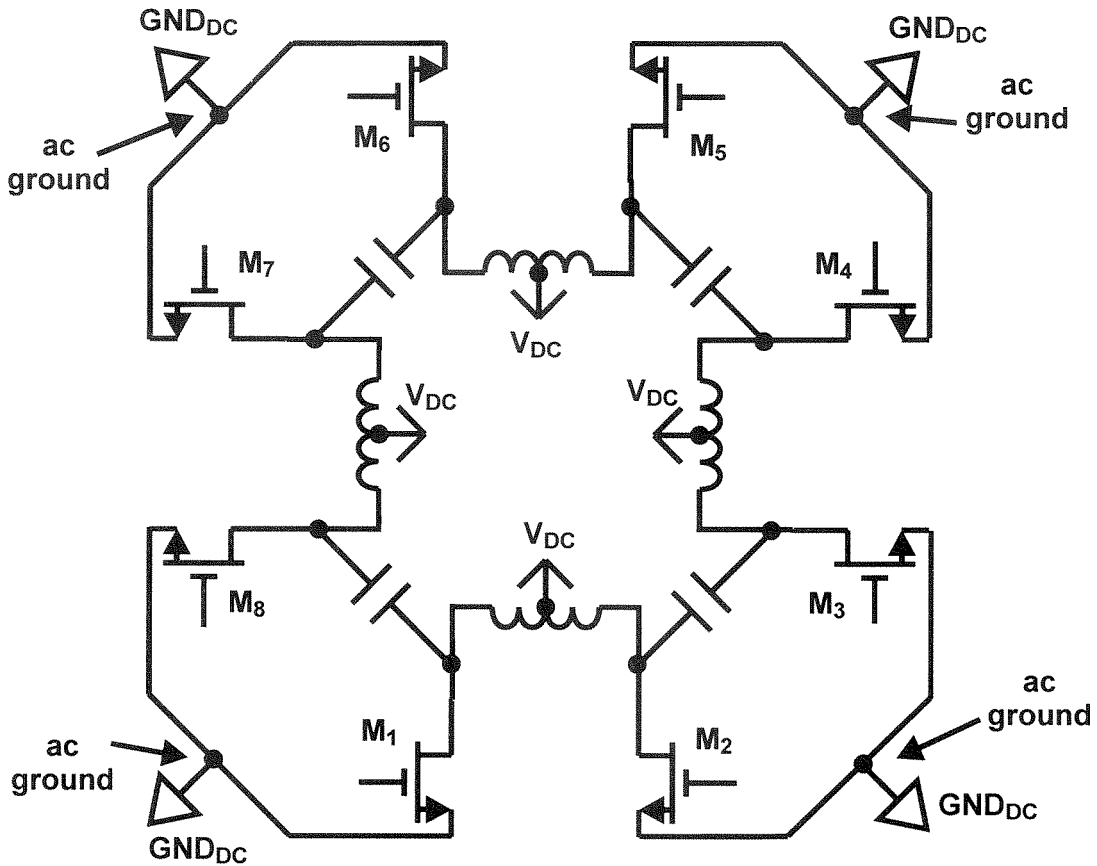




**Figure 5.10:** Four independent push-pull power amplifiers placed in a circular layout using eight NMOS transistors.

## 5.4 Cross Connected Drain Capacitors

The connection of the drain tank capacitor presents similar difficulties. These capacitors cannot be connected between the drains of transistors belonging to the same push-pull amplifier in a conventional way, as the inductance of the long metal lines used to connect them will be comparable to that of the drain slab inductor. In order to solve this layout problem, these capacitors are connected between the drains of adjacent transistors of the circular-geometry belonging to the adjacent push-pull amplifiers, as seen in Figure 5.9. The voltage between the drains of these adjacent transistors is exactly the same as the volt-



**Figure 5.11:** Four push-pull amplifiers each sharing the source ground connection and drain resonating capacitor connection with their adjacent amplifiers forming a circular geometry power amplifier.

ages between the drains of a single push-pull amplifier, so long as the transistors are driven in proper phase, as shown in Figure 5.9. Therefore, if we connect the capacitors between the drains of adjacent transistors, their currents remain exactly the same and the circuit operation does not change. This produces a harmonic suppression and wave shaping identical to connecting the capacitor across the drains of each differential pair.

## 5.5 Series Magnetic Power Combining

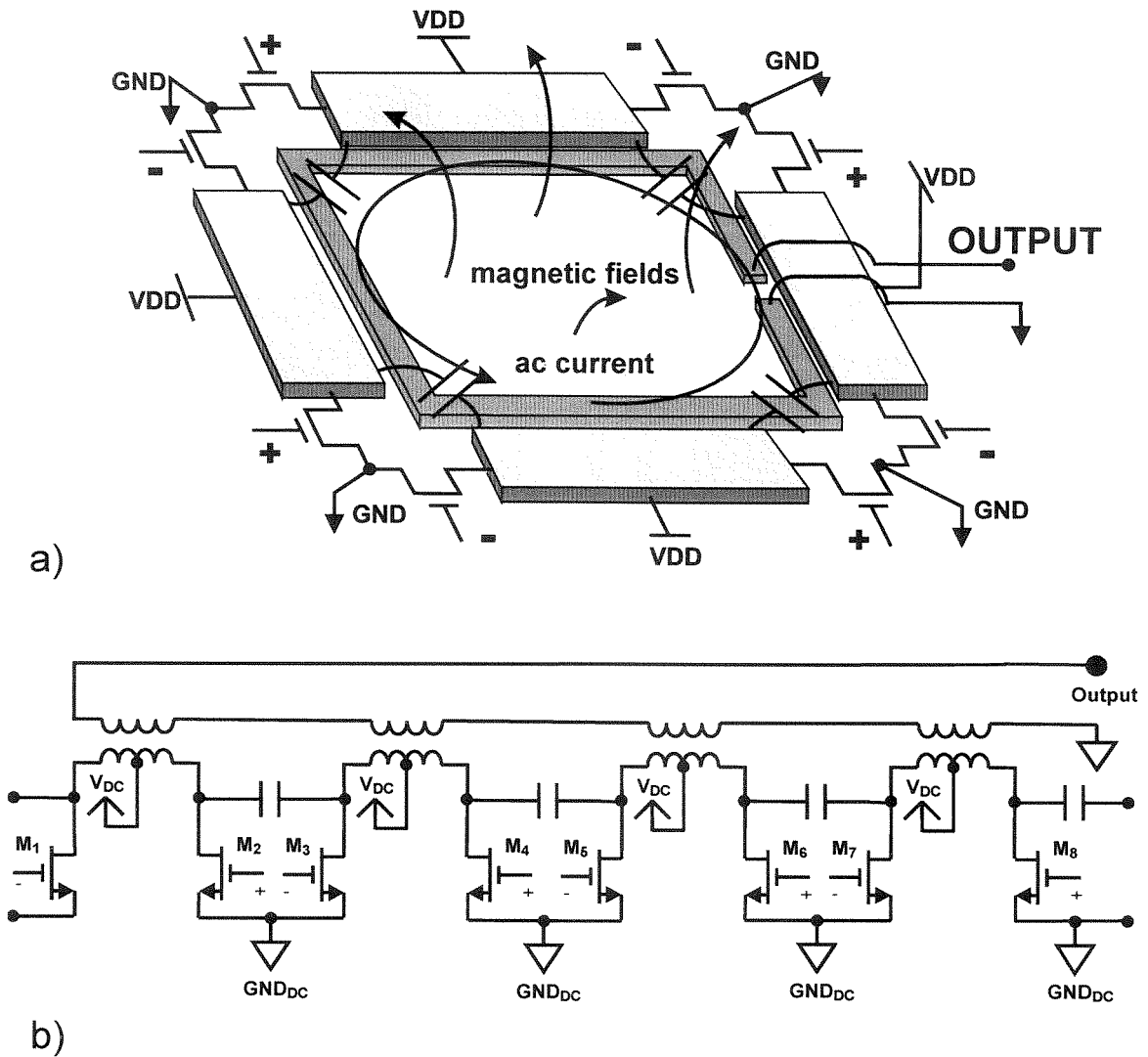
Although the circular-geometry introduced in Section 5.3 allows several push-pull amplifiers to be designed in a way so as to reduce the serious layout and thermal dissipation problems, their output powers must still be combined and delivered to the load.

This power combining is accomplished by introducing a one turn metal strip inside the circular geometry to act as a magnetic pick-up of the output power, as shown in Figure 5.12a. The  $n/2$  push-pull amplifiers (four in this example) conduct identical synchronized ac currents at the fundamental, inducing corresponding ac magnetic fields in this secondary loop. The internal metal loop harnesses the induced magnetic field to generate a voltage between its terminals equivalent to the sum of the differential voltages of the  $n/2$  push-pull amplifiers. Another way to interpret this is to view this topology as  $n/2$  push-pull amplifiers each with a 1:1 transformer, whose secondary circuits are connected in series. As the primary circuits of these transformers are independent, the result is a 1: $n$  impedance transformation as in Figure 5.12b. This *distributed active-transformer* (DAT) architecture results in a *simultaneous 1: $n$  impedance transformation and  $n$  transistor power combining*.

This DAT architecture is completed by proper tuning of the cross-connected drain capacitors and the introduction of a capacitor in parallel with the load. Both are necessary to partially compensate the leakage inductances created by the relatively low coupling coefficient (e.g.,  $k \approx 0.6$ ) of the transformer.

## 5.6 Cross Connected Gate Inductor

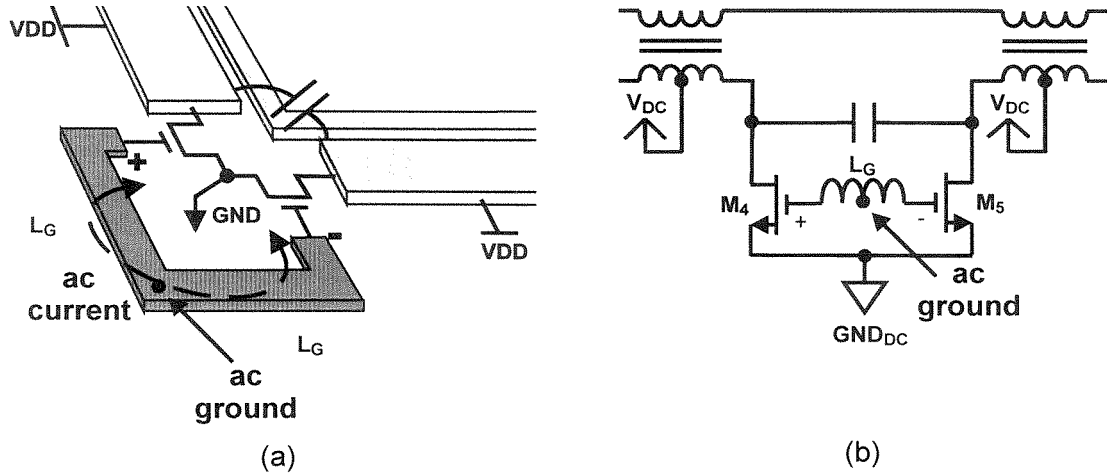
Inductors should be placed in parallel with the transistor gates to resonate the gate capacitance as the input impedance of any transistor large enough to obtain watt-level output power is much lower than that of the 50  $\Omega$  input.



**Figure 5.12:** a) An illustration of Distributed Active Transformer combined four push-pull amplifiers using eight NMOS transistors, b) Its corresponding electrical diagram.

This inductor can cause difficulty as there is no convenient ac ground to connect it to and its connection to circuit (dc) ground will necessitate an undesirable bypass capacitor. If the gate matching inductors of the adjacent transistors are connected to each other instead of circuit ground as shown in Fig. 10, an ac ground at the fundamental frequency is formed at this connection point and no connection to dc ground is formed, avoiding both

problems. Since this connection point can be located far from the transistors, slab inductors can be used to reduce the loss in this component.



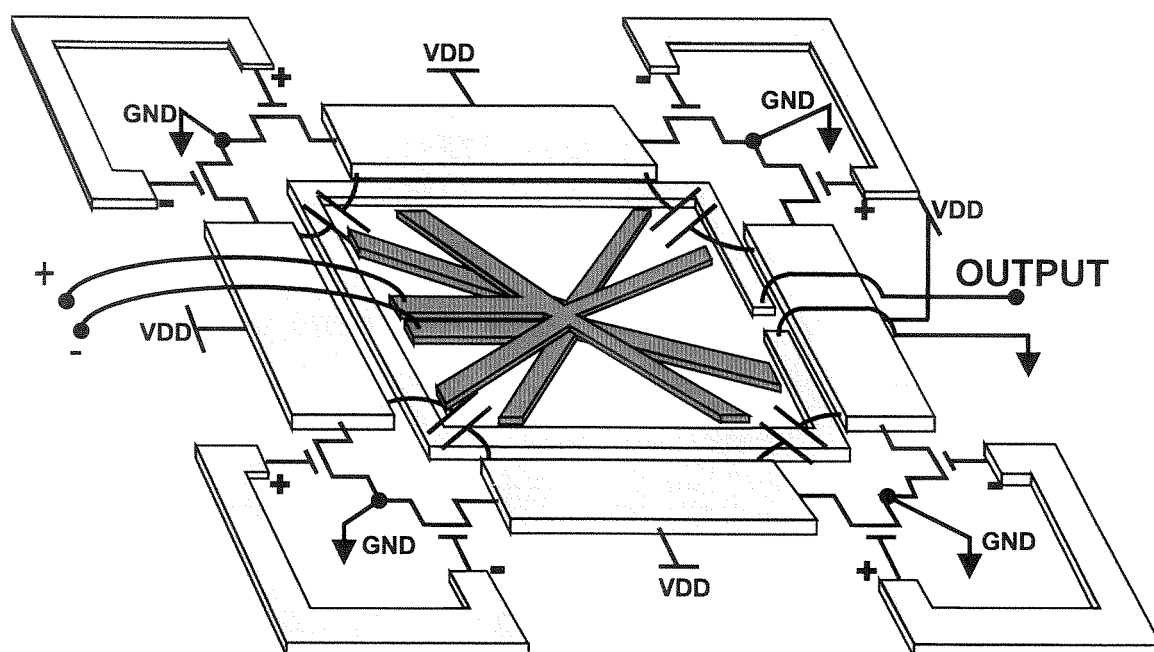
**Figure 5.13:** a) An illustration of cross connected gate matching inductor, b) Its corresponding electrical diagram.

## 5.7 Input Power Distributing and Driver Stage

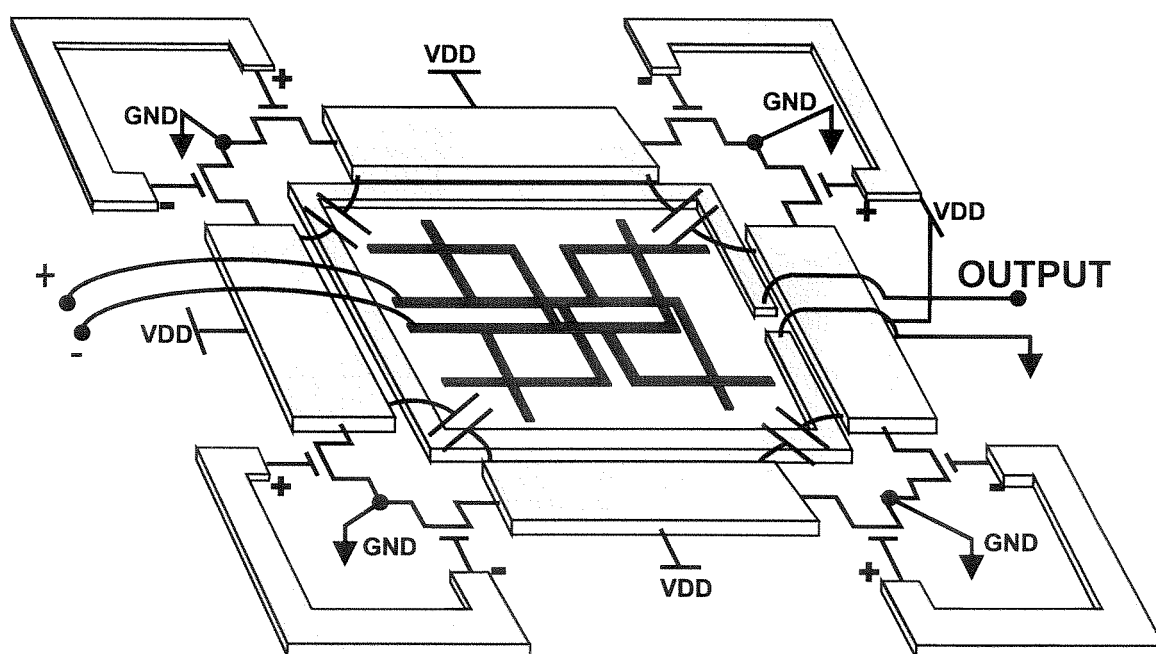
### 5.7.1 Internal Distributing

The power distribution network shown in Figure 5.14 and Figure 5.15 brings the synchronized differential power to the gates of the transistors. It consists of two parts, namely the connecting differential lines bringing the balanced signal to the center of the circular geometry, and a distribution network symmetrically connecting the center point to the gates of each transistor. The differential input can be generated by either an on-chip balun matched to the unbalanced  $50\Omega$  input or by an integrated differential pre-amp stage.

These input power-distributing lines may have a twisted layout, as in Figure 5.15, to introduce an adjustable amount of magnetic positive feedback to enhance the gain.



**Figure 5.14:** An illustration of DAT with star configuration input power distributing network.

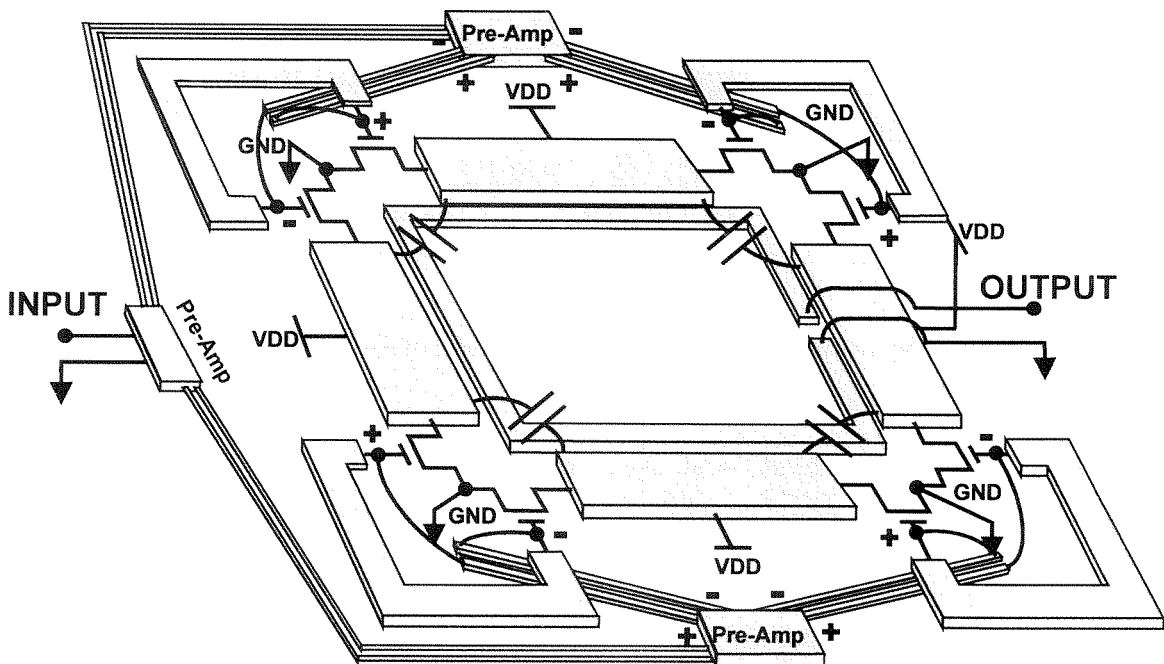


**Figure 5.15:** An illustration of DAT with twisted configuration input power distributing network.

### 5.7.2 External Drive Signal Distribution

Use of an internal power distribution network, as described in the previous section, will lead to an extra power loss, as the metal lines of this network will have Eddy currents induced by the strong magnetic field generated by the circular geometry push-pull amplifiers.

An alternative to reduce this power loss is to bring the input signal to each gate from outside of the circular geometry, where the magnetic field intensity is lower. An illustration of Figure 5.16 shows this external input network.



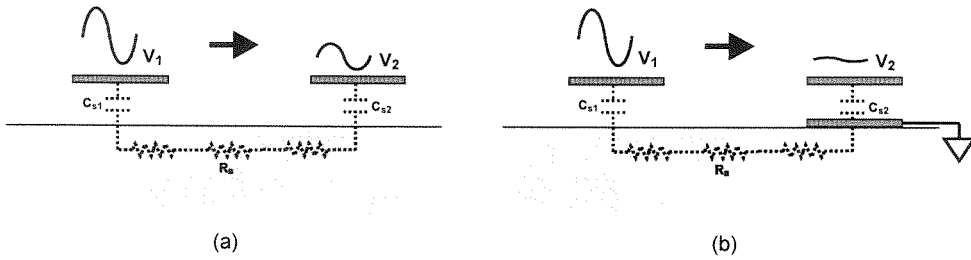
**Figure 5.16:** An illustration of DAT with external power distributing network with two stage pre-amps.

This external connection, though increasing the passive efficiency by around 5% in our simulations, will have longer connection to the input pad located at the edge of the chip. This will lead to an extra power and gain loss. Fortunately, the power loss in the input side can be reduced by increasing the gain of the power amplifier. This might be

accomplished introducing pre-amplification stages, as can be seen in the example of Figure 5.16.

### 5.7.3 Electric Shielding to Avoid Substrate Coupling

Another problem detected in the 3-D planar simulation of the DAT was a non-symmetric capacitive coupling from the drain and secondary metal lines to the input gate metal lines through conductive substrate, as shown in Figure 5.17.



**Figure 5.17:** Capacitive coupling of two metal lines through a conductive substrate (a) and its reduction in coupling using a lower grounded metal layer (b).

This coupling which is non-symmetric, will make each transistor receive a different signal level at their gates. As all of the transistors are connected in series for ac signal in a circular geometry, forcing one or some of them have a different current from other transistors in the loop, will lead to reduction in power and gain.

This problem can be minimized by electrically shielding the gate power splitting network using lower metal layers connected to the nearest ground, which was conformed in our simulations.

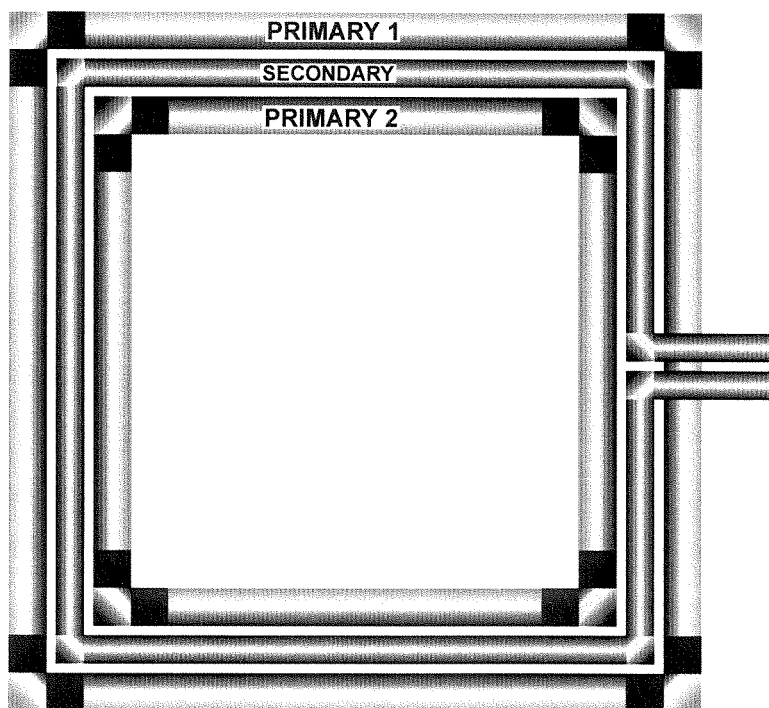
## 5.8 Interdigitation of the Primary and Secondary Circuit

Currents through conductors, when electrical field effects are minimal, distribute in a configuration in which the stored magnetic field energy is minimum. Using this condition we can easily understand that in a wide metal, the current tends to concentrate in its edges as



can be seen in Figure 4.8. On the other hand, if two currents flow in opposite directions, these currents tend to come closer to mutually cancel, as much as possible, their magnetic field and its stored energy. This makes the current concentrate to the inner edge of the loop in spiral inductors and at the edges of the primary inductor and secondary inductor facing each other in a planar transformer. This current crowding can be seen in Figure 4.8 showing two one turn spiral inductors and their current densities and a one turn spiral coupled-inductor transformer.

To further reduce the metal resistance loss of the slab inductors of the DAT, we can have more than one edge between primary and secondary circuit facing each other. In this way, the current will be distributed among several edges, thus reducing the effective metal resistance to the total current. Figure 5.18 shows a DAT with two primary circuits each with eight transistors and one secondary circuit, along with its current distribution among two edges between the primary and the secondary circuit.



**Figure 5.18:** An illustration of current density in a interdigitated DAT with two primary and one secondary circuits making two edges. This circuit uses 16 transistors represented by black boxes.

In this double primary topology, the inductance in the drain of the external primary will be higher than that of the internal primary. Thus the current in the external primary will be lower than that of the internal secondary and the transistor sizing of these 16 transistors and matching with eight cross-connected capacitors should be adjusted accordingly to these two levels of drain current. Dc connections between internal and external primary circuits for dc supply and ground, which are not drawn in Figure 5.18, completes this circuit. There is no necessity to have any ac connections between the internal and external loops.

In our planar 3-D simulations, this configuration with two edges increased the passive efficiency by around 5%. Creating more than two edges, with multiple secondary and primary circuits did not increase the passive efficiency significantly.

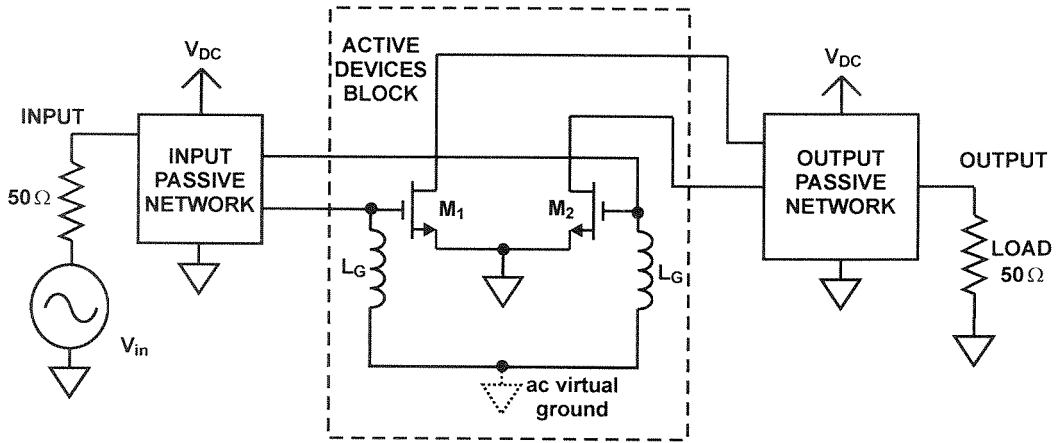
## 5.9 Classes of Amplifier Operation for DAT

The harmonic impedances available at drains in the distributed active-transformer described in Section 5.1 allow the DAT to operate in several different classes including A, AB, B, C, inverse F and E/F<sub>odd</sub> [15][40][21]. A DAT power amplifier can operate in one or more classes of operation depending on the gate bias level, drive level and drain tuning.

In this Section, we analyze the DAT power amplifier starting in either class-A or class-B and compressing into class-E/F<sub>odd</sub>. The general amplifier classes analysis covered in the Section 3.2.1 and Section 3.3.1.1 will be extended to some particularity of the DAT, specially for class B. The combinations, A to E/F<sub>odd</sub> or B to E/F<sub>odd</sub>, are the most useful ones when the transistor gain is limited, as class A and B biasing conditions extract the highest gain from the transistor. Starting in class-A results in a higher gain, while class-B operation results in a higher drain efficiency. If the operating frequency is low relative to transistor speed and very high transistor gain is available, other choices might be useful.

In the following subsection, we will investigate the DAT operation in classes A, B, and E/F<sub>odd</sub>. To simplify and clarify the analysis, the push-pull block is further divided into

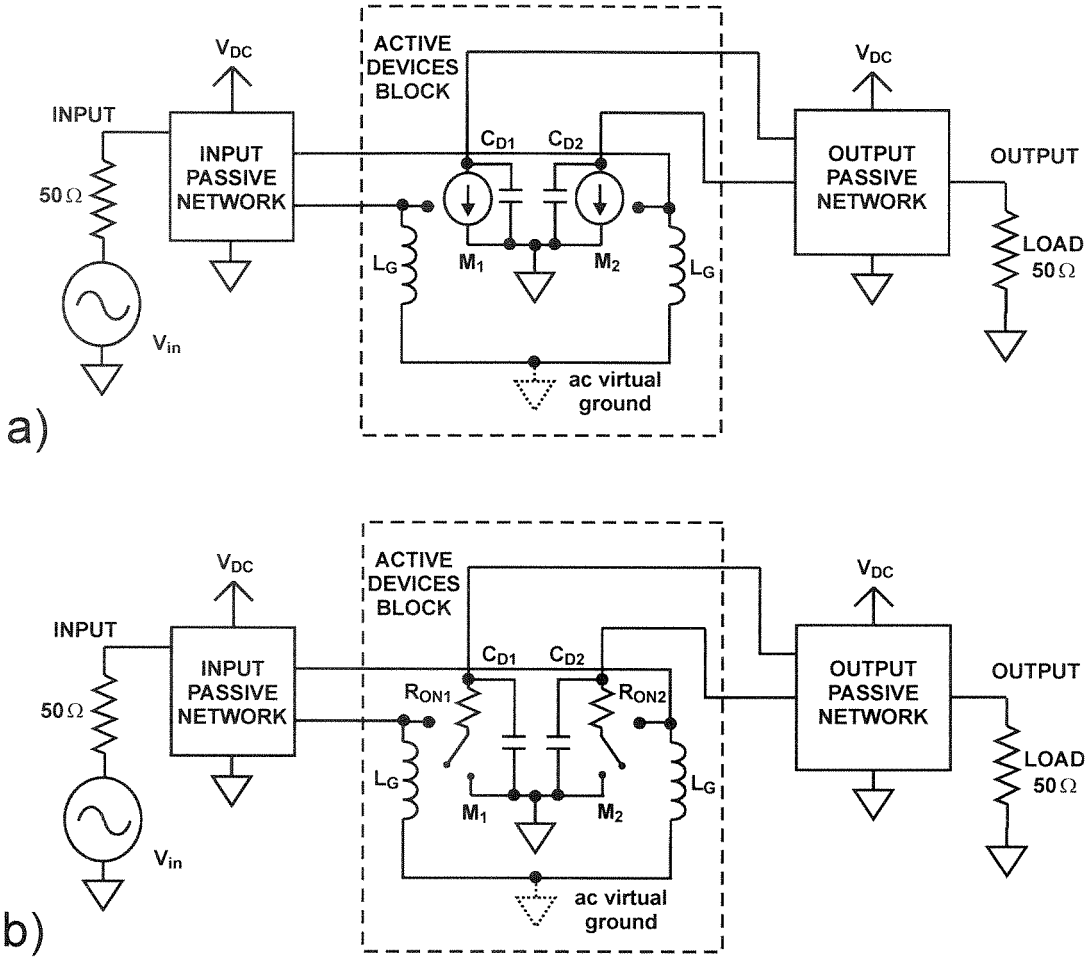
three sub-blocks, namely the input network, the active, devices, and the output network in a similar way to Chapter 3. The input network comprises every passive component from  $50\Omega$  input to transistor gates, the active devices block, and consists of transistors and gate matching inductors, and the output network formed by the passive components from the drain to the  $50\Omega$  load including the transformer and matching capacitors, as illustrated in Figure 5.19.



**Figure 5.19:** The three building blocks of the DAT push-pull amplifier: input, active device, and output.

### 5.9.1 Class A Operation

A straightforward analysis may be performed to calculate the gain, the maximum output power, and the power efficiency as a function of the active and passive parameters and the supply and bias voltages in a similar way of Section 3.3.1.1, but this time including the effect of input and output passive network loss, which is significant in silicon integrated power amplifiers, and the limited gain of transistor. We assume that the transistor is a linear current source with a transconductance,  $g_m$ . We assume perfect linearity in this case. An equivalent electrical diagram of a push-pull block operating in class-A mode can be seen in Figure 5.20a.



**Figure 5.20:** a) DAT operating in class A, AB, or B mode, b) DAT operating in class E/F<sub>odd</sub> mode.

The maximum output power,  $P_{out}$ , will be a function of the transistor knee voltage,  $V_k$ , [15], supply voltage,  $V_{dd}$ , number of combined push-pull blocks,  $n/2$ , output passive network power efficiency,  $\eta_{out}$ , and load resistance seen by each drain,  $R_l$ , i.e.,

$$P_{out} = n \frac{(V_{dd} - V_k)^2}{2R_l} \eta_{out} \quad (5.11)$$

where  $R_l$  is the real impedance seen by the drain of each transistor in the output network, which includes the effect of the output network losses and the load resistance. This value can be calculated using an electromagnetic simulator or approximated analytically [17].

The output capacitance of each transistor is resonated out by the tuning inductance of the output passive network, so that the load impedance including this capacitor is purely real.

The gain will be the product of the active device gain,  $G_A$ , input and output passive network power transfer efficiencies,  $\eta_{in}$  and  $\eta_{out}$ , i.e.,

$$G = \eta_{in} G_A \eta_{out} \quad (5.12)$$

The active device gain,  $G_A$ , may be calculated as a function of transistor transconductance,  $g_m$ , the gate voltage,  $V_g$ , the gate matching inductor and transistor equivalent parallel input resistance,  $R_g$ , and drain load differential resistance,  $R_l$

$$G_A = \frac{P_{Aout}}{P_{Ain}} = \frac{n(g_m V_g)^2 R_l / 2}{n V_g^2 / (2 R_g)} = g_m^2 R_l R_g \quad (5.13)$$

where  $P_{Aout}$  is the output power of the active block, as shown in Figure 5.19,  $P_{Ain}$  is the input power of the same active block, and  $n$  is the number of combined transistors.

The drain efficiency,  $\eta$ , and power added efficiency,  $PAE$ , can be calculated as functions of  $P_{DC}$ ,  $P_{out}$ ,  $V_k$ ,  $V_{dd}$ ,  $n$ , and  $R_l$ . The dc power dissipation is constant in class-A operation, as the output power changes. Therefore, the drain efficiency as a function of output power,  $P_{out}$ , is given by

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{n I_{dd} V_{dd}} = \frac{P_{out}}{n V_{dd} (V_{dd} - V_k) / R_l} \quad (5.14)$$

where  $I_{dd}$  is dc supply current to each transistor.

We can calculate the peak drain efficiency,  $\eta_{MAX}$ , from (5.11) and (5.14):

$$\eta_{MAX} = \frac{n \frac{(V_{dd} - V_k)^2}{2 R_l} \eta_{out}}{n V_{dd} (V_{dd} - V_k) / R_l} = \frac{1}{2} \left( 1 - \frac{V_k}{V_{dd}} \right) \eta_{out} \quad (5.15)$$

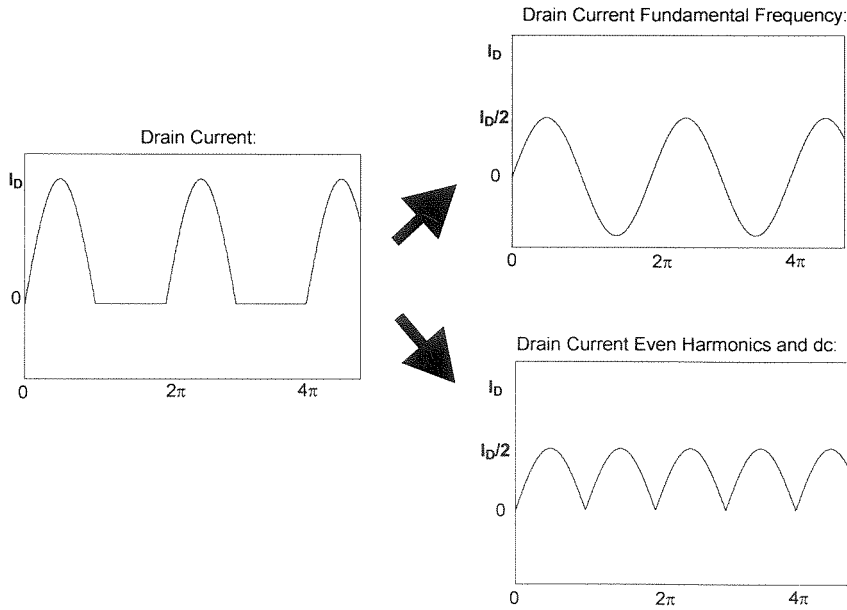
$$PAE = \eta \left( 1 - \frac{1}{G} \right) = \frac{P_{out}}{n V_{dd} (V_{dd} - V_k) / R_l} \left( 1 - \frac{1}{\eta_{in} g_m^2 R_l R_g \eta_{out}} \right) \quad (5.16)$$

### 5.9.2 Class B Operation

Push-pull amplifiers operating in class-B mode can be analyzed to obtain closed-form solutions for the drain current and voltage waveforms by treating even and odd current harmonics separately. This is shown in the time domain waveform of Figure 5.21. The drain current waveform of a transistor operating in ideal class-B mode is composed of fundamental frequency and even harmonics only. These currents can be calculated as follows:

$$\begin{aligned}
 I_{Deven}(t) &= \frac{I_D}{2} \sin(\omega t) - \frac{I_D}{\pi} & , 0 \leq t < T/2 \\
 I_{Deven}(t) &= -\frac{I_D}{2} \sin(\omega t) - \frac{I_D}{\pi} & , T/2 \leq t < T \\
 I_{Dodd}(t) &= \frac{I_D}{2} \sin(\omega t)
 \end{aligned} \tag{5.17}$$

where  $T$  is the period and  $I_D$  is the peak drain current. These waveforms can be seen in Figure 5.21.



**Figure 5.21:** Decomposition of the drain current waveforms into odd and even harmonics of a DAT amplifier operating in class B mode.

The even harmonic components of the voltage waveform can be easily computed noting the symmetry of the circuit. If the impedance of the transistor output capacitance is much less than  $Z_{Vdd}$ , the impedance seen by the even harmonic currents will be approximately that of the transistor output capacitance. Therefore, the even harmonic component of the drain voltage,  $V_{Deven}(t)$ , can be calculated by integrating  $I_{Deven}(t)$ , i.e.,

$$\begin{aligned}
 V_{Deven}(t) &= -\frac{1}{C_d} \int_0^t \frac{I_D}{2} \sin(\omega t) - \frac{I_D}{\pi} dt \\
 &= -\frac{I_D}{2\omega C_d} \left( (-\cos(\omega t) + 1) - \frac{2\omega}{\pi} t \right) \quad , 0 \leq t < T/2 \\
 V_{Deven}(t) &= -\frac{1}{C_d} \int_{T/2}^t -\frac{I_D}{2} \sin(\omega t) - \frac{I_D}{\pi} dt \\
 &= -\frac{I_D}{2\omega C_d} \left( (\cos(\omega t) + 1) - \frac{2\omega}{\pi} t \right) \quad , T/2 \leq t < T
 \end{aligned} \tag{5.18}$$

The fundamental component of the voltage can be computed by multiplying the fundamental component of the drain current by the resistance  $R_l$  presented by the output network. As in the class-A case presented in Section 5.9.1, we assume that the output network is adjusted so that this impedance is purely real.

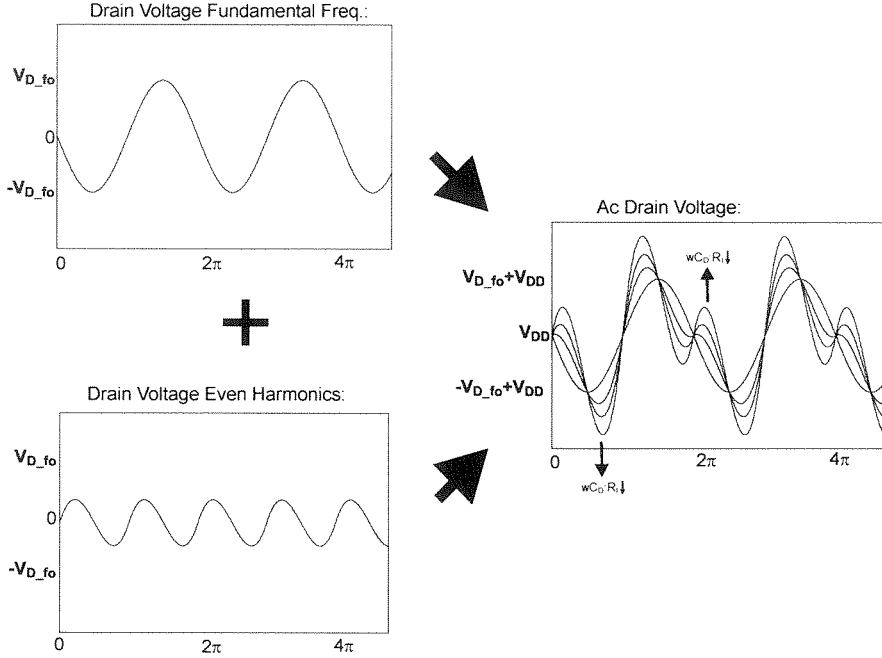
$$V_{Dodd}(t) = -\frac{I_D \sin(\omega t) R_l}{2} \tag{5.19}$$

The actual voltage waveform can be found by superimposing the odd and even harmonic components, as shown in Figure 5.22.

$$V_D(t) = V_{Deven}(t) + V_{Dodd}(t) + V_{DD} \tag{5.20}$$

It is noteworthy that the transistor output capacitance is essential to this mode of operation and cannot be ignored. Without this capacitance, the amplifier cannot operate in class-B mode since there would be no path for the even components of the drain current to flow through. Furthermore, if the transistors and these capacitors are small, the even component of the drain voltage becomes large and might damage the transistors, as depicted in

Figure 5.22. If the optimal transistor size has too small of an output capacitance, additional lumped capacitances can always be added.



**Figure 5.22:** Composition of the drain voltage waveform from odd and even harmonics of a DAT amplifier operating in class B mode.

In class-B operation, the maximum output power will be lower than that of class-A, as the even harmonics of the drain voltage will increase the maximum value of the drain voltage. This peak voltage can be calculated numerically from (5.19) and (5.20). The maximum allowable drain voltage component at the fundamental frequency is the difference between  $V_{dd}$  and  $V_k$ .

If the even voltage peaks are small enough to be neglected, the output power,  $P_{out}$ , is the same as for class-A under same conditions, i.e.,

$$P_{out} = n \frac{(V_{dd} - V_k)^2}{2R_l} \eta_{out} \quad (5.21)$$

An example of the drain waveform for  $\omega C_D / R_l = 0.5, 0.3$  and  $0.2$  can be seen in Figure 5.22.



The gain of the active block,  $G_A$ , for this mode of operation can be calculated as follows:

$$G_A = \frac{P_{Aout}}{P_{Ain}} = \frac{n\left(\frac{g_m V_g}{2}\right)^2 R_l / 2}{n V_g^2 / 2 R_g} = \frac{g_m^2 R_l R_g}{4} \quad (5.22)$$

The gain under conditions described by (5.22) will be 6dB lower than the gain of the class-A operation. The gain of actual amplifier will be even lower since the transistor transconductance in the class-B operation is lower than that under class-A. The total power gain can be computed using (5.12).

Combining (5.13) with (5.22), we notice that the drain efficiency,  $\eta$ , and power added efficiency,  $PAE$ , can be calculated as functions of  $P_{out}$ ,  $P_{DC}$ ,  $V_{dd}$ ,  $n$ , and  $R_l$ . The dc power dissipation,  $P_{DC}$  is proportional to  $I_D$  in class-B operation, therefore:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{n V_{dd} I_D / \pi} = \frac{P_{out}}{n V_{dd} \frac{2}{\pi} \sqrt{2 \frac{P_{out}}{n \eta_{out} R_l}}} = \pi \frac{\sqrt{P_{out} R_l \eta_{out}}}{2 \sqrt{2} n V_{dd}} \quad (5.23)$$

It is interesting to notice that in both class-A and class-B cases the drain efficiency can be kept higher when output power is low if we can change either  $R_l$  or  $V_{dd}$  or both dynamically as  $P_{out}$  changes. Equations (5.14) and (5.23) clearly show this fact.

We can calculate the peak efficiency,  $\eta_{MAX}$ , from (5.21) and following equation, if the peaking in the drain voltage caused by even harmonic components is negligible, i.e.,

$$\eta_{MAX} = \frac{\pi}{4} \left( 1 - \frac{V_k}{V_{dd}} \right) \eta_{out} \quad (5.24)$$

Finally,  $PAE$  can be determined using (5.16) and (5.24).

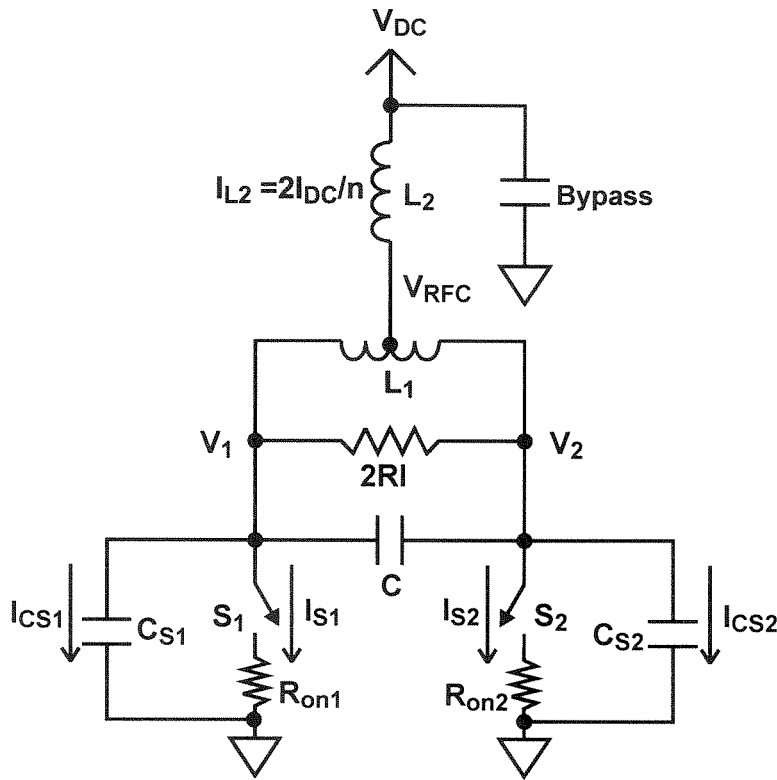
### 5.9.3 Classes $D^{-1}$ or $F^{-1}$ and $E/F_{\text{odd}}$ ZVS Amplifier

In this subsection, we will describe the push-pull class  $D^{-1}$  or  $F^{-1}$  and  $E/F_{\text{odd}}$  previously studied in Section 3.3.1.3 and Section 3.3.1.6 in further detail, as these classes are the most appropriate class of operation to extract high power efficiency from a DAT power amplifier.

Class  $D^{-1}$  or  $F^{-1}$  are switching amplifier class, in which the switch sees load resistance at fundamental frequency, open for every even overtones, and short to ground for every odd overtones [40]. On the other hand, Class  $E/F_{\text{odd}}$  belongs to the recently introduced  $E/F$  family of ZVS (zero voltage switching) power amplifiers and in this amplifier the impedances seen by the transistor drain is the same as that of the class  $F^{-1}$  at every odd harmonic frequency and the same as that of class  $E$  for the fundamental and the even harmonics [21]. As class  $D^{-1}$  or  $F^{-1}$  are the extreme case of class  $E/F_{\text{odd}}$ , when its switch shunt capacitor approaches zero, only the class  $E/F_{\text{odd}}$  needs to be analyzed.

To analyze class  $E/F_{\text{odd}}$ , the transistors should be approximated as switches with series resistance,  $R_{\text{on}}$ . This assumption is valid when the input power is high enough so that the transistor is either open or operates in the triode region during most of the cycle. The equivalent circuit may be seen in Figure 5.23. There is no known simple solution to analyze the circuit when the transistor is operating part of the cycle as a current source and part of the cycle as an open or short circuit. Also it is difficult to calculate the value of  $R_{\text{on}}$  analytically as a function of the input power and circuit parameters, since the transistor behavior during the transition from the open state to the short state and vice-versa is extremely non-linear. This can be an interesting subject for future work. For this work, we assume that  $R_{\text{on}}$  is constant for the input power above a certain value. This minimum input power and  $R_{\text{on}}$  may be extracted from numerical simulations of the amplifier.

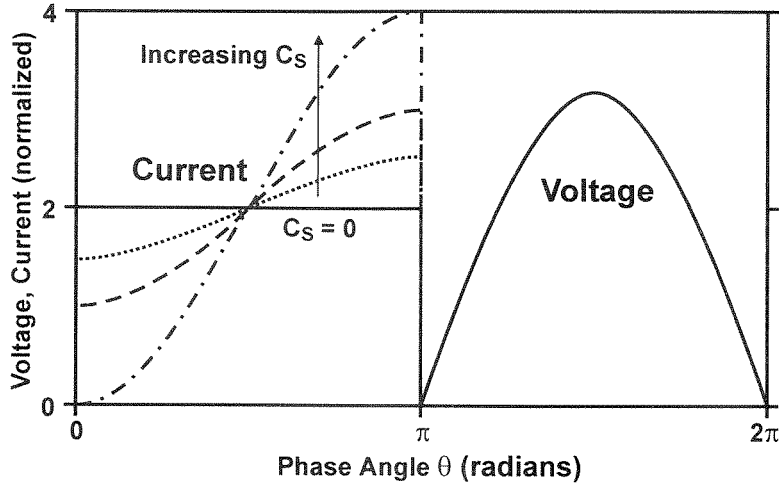
The simple push-pull circuit of Figure 5.23 can be used to provide virtual short-circuits at the odd harmonics to each switch while leaving the impedance seen by the switches at the even harmonics to be that of the switch output capacitance as described in



**Figure 5.23:** Equivalent circuit of a push-pull class E/ $F_{\text{odd}}$  power amplifier with transistors operating substantially as switches.

Section 5.1. Furthermore, due to the symmetry of the circuit, the even harmonics are suppressed at the load, easing the task of filtering the output.

Initially, we assume the loss is negligible and the loaded  $Q$  of the resonator composed of  $L_1$  and  $C$  is high. If this resonator is tuned near the fundamental frequency  $f_0$ , the voltage across it must be a sinusoid at that frequency. The resonator is then detuned to have the required inductance at the fundamental frequency to achieve ZVS conditions. The resonator should present between the transistor drains a reactance equal to that of each transistor's output capacitance, but with the opposite sign. Kirchhoff's voltage law requires that the voltage across the resonator be the same as the difference between the switch voltages,  $V_1$  and  $V_2$ . In addition,  $V_1$  and  $V_2$  are zero during the half-period when the corresponding switch is closed. Therefore, the voltage across each switch must be



**Figure 5.24:** Voltage and current waveforms of the switches of a class E/ $F_{\text{odd}}$  power amplifier. The change in the current waveform with increasing transistor output capacitance is depicted. The current on the plot does not include the current through this capacitance.

half-sinusoid, as in Figure 5.24. For the dc voltage of this waveform to equal the supply voltage,  $V_{DC}$ , the peak voltage,  $V_{pk}$ , must be  $\pi V_{DC}$ , i.e.,

$$V_1 = \begin{cases} 0 & 0 \leq t < T/2 \\ -\pi V_{DC} \sin(\omega t) & T/2 \leq t < T \end{cases} \quad (5.25)$$

$$V_2 = \begin{cases} \pi V_{DC} \sin(\omega t) & 0 \leq t < T/2 \\ 0 & T/2 \leq t < T \end{cases} \quad (5.26)$$

The currents,  $I_{CS1}$  and  $I_{CS2}$  through the output capacitors,  $C_{S1}$  and  $C_{S2}$ , may be found using the known switch voltages, i.e.,

$$I_{CS1} = \begin{cases} 0 & 0 \leq t < T/2 \\ -\pi \omega C_{S1} V_{DC} \cos(\omega t) & T/2 \leq t < T \end{cases} \quad (5.27)$$

$$I_{CS2} = \begin{cases} \pi \omega C_{S2} V_{DC} \cos(\omega t) & 0 \leq t < T/2 \\ 0 & T/2 \leq t < T \end{cases} \quad (5.28)$$

If  $L_2$  is large and conducts only dc current, for each half-cycle, one of the transistors is open circuited (and can be removed from the circuit), while the other is short circuited and

conducts the excess current. Therefore, we can calculate the currents through the switches,  $I_{s1}$  and  $I_{s2}$ , as a function of amplifier total dc current,  $I_{DC}$ , as follows:

$$I_{CS1} = \begin{cases} 2\frac{I_{DC}}{n} - I_{CS2} & 0 \leq t < T/2 \\ 0 & T/2 \leq t < T \end{cases} \quad (5.29)$$

$$I_{CS2} = \begin{cases} 0 & 0 \leq t < T/2 \\ 2\frac{I_{DC}}{n} - I_{CS1} & T/2 \leq t < T \end{cases} \quad (5.30)$$

The waveforms for the class E/F<sub>odd</sub> amplifier with linear output capacitance, calculated from (5.25)-(5.30), are plotted in Figure 5.24. A similar solution exists for non-linear capacitors [21].

To calculate the amplifier total dc current,  $I_{DC}$ , we can equate the fundamental frequency component of the square current through the switches to twice the current through the load. This will result in

$$I_{DC} = \frac{n}{2} \left( \frac{V_{DC}}{R_{on} - \frac{4R_l}{\pi^2}} \right) \quad (5.31)$$

The instantaneous power loss is the product of  $R_{on}$  and its rms current. The average power loss is then given by

$$\begin{aligned}
P_{loss} &= n \frac{1}{2\pi} \int_0^{2\pi} I_{S1}(\theta)^2 d\theta R_{on} \\
&= n \frac{1}{2\pi} \int_0^{\pi} \left( \frac{2I_{DC}}{n} - \frac{\pi}{X_{CS1}} \left( V_{DC} - \frac{2I_{DC}}{n} R_{on} \right) \cos\theta \right)^2 d\theta R_{on} \\
&= n \frac{R_{on}}{2} \left[ \left( \frac{2I_{DC}}{n} \right)^2 + \frac{\left( \frac{\pi}{X_{CS1}} \left( V_{DC} - \frac{2I_{DC}}{n} R_{on} \right) \right)^2}{2} \right]
\end{aligned} \tag{5.32}$$

To account for loss, the series resistance of the switch,  $R_{on}$ , and the voltage drop associated with it are included in (5.32).

Since the amplifier is saturated, the output power is no longer a function of the input power, but is instead a function of supply voltage,  $V_{DC}$ . We can calculate the approximate output power of the circular geometry amplifier as follows:

$$P_{out} = (P_{DC} - P_{loss})\eta_{out} = (V_{DC}I_{DC} - P_{loss})\eta_{out} \tag{5.33}$$

As  $P_{out}$  is not a function of  $P_{in}$ , the gain can be calculated using (5.32):

$$G = \frac{P_{out}}{P_{in}} = n \frac{\left( \pi \left( V_{DC} - \frac{2I_{DC}}{n} R_{on} \right) \right)^2}{8R_l P_{in}} \eta_{out} \tag{5.34}$$

The drain efficiency may be computed using (5.31) and (5.32) to be

$$\eta = \left( 1 - \frac{P_{loss}}{V_{DC}I_{DC}} \right) \eta_{out} \tag{5.35}$$

Finally, the PAE may be obtained from (5.16), (5.34) and (5.35).

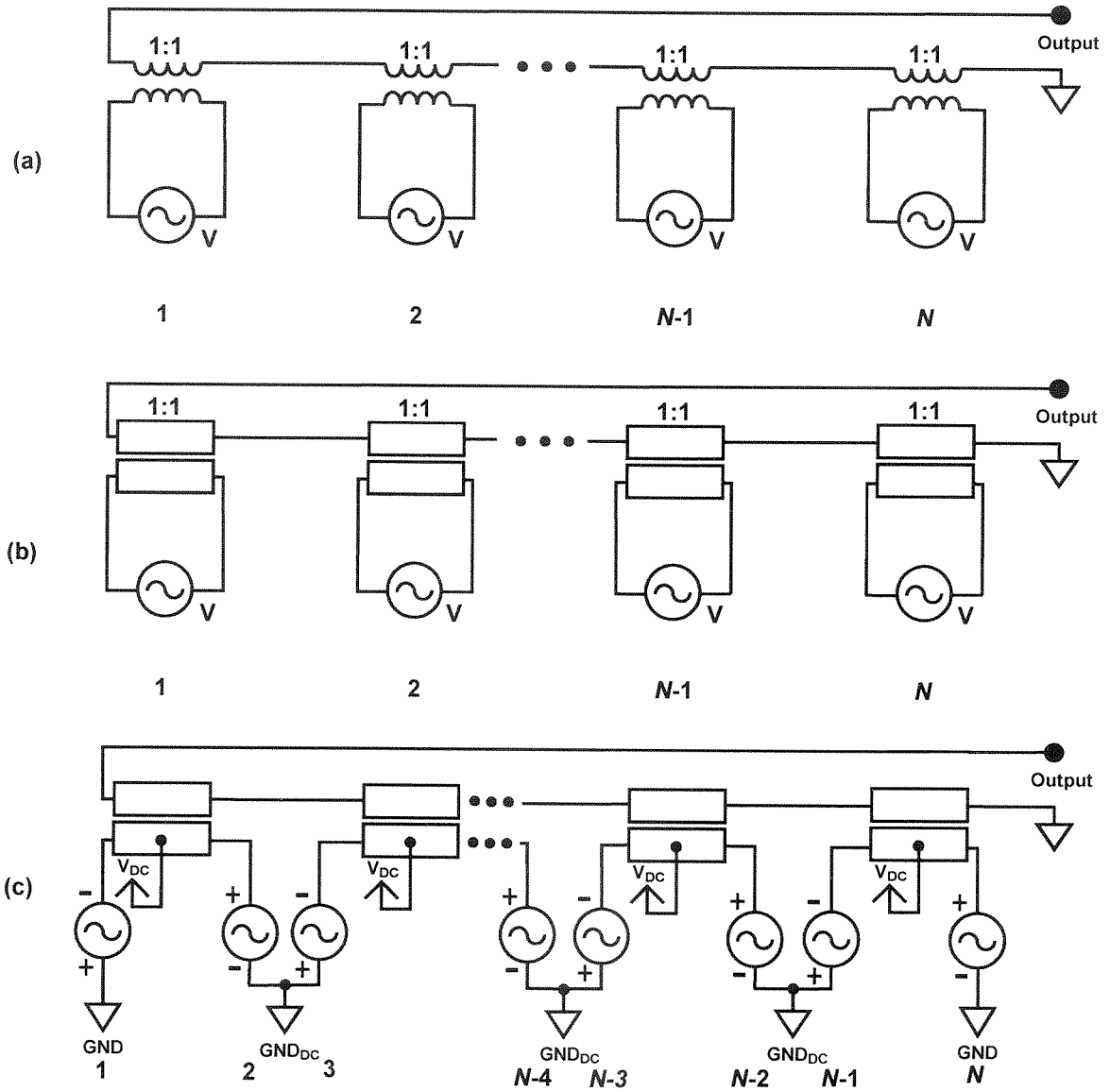
## 5.10 Power Efficiency of a DAT

In this subsection we will describe again the DAT in an electromagnetic perspective to enable us to understand how it achieves higher power efficiency when compared to a conventional impedance transformation or power combining networks.

The analysis performed in Chapter 4 show that if we could increase the transformer turn ratio,  $n$ , while maintaining a constant,  $Q$ , we could achieve a high efficiency for large PER, as suggested by (4.22) and (4.24). Unfortunately, the quality factor,  $Q$ , suffers if a large turn ratio is to be used for the reasons that were discussed in Section 5.2. Also (4.20) shows that the required impedance level at the input can become impractically small for large turn ratios because it is inversely proportional to  $n^2$ . These observations leave us no choice but to use lower turn ratios. In practice, the lowest loss can be achieved for a 1:1 ratio, which is also very appealing since high- $Q$  coupled slab inductors discussed in Section 5.2 can be used to realize it.

While 1:1 transformers are desirable for the above reasons, it is obvious that we need more than one 1:1 transformer to obtain any impedance transformation. A high PER, can be achieved using  $N$  independent 1:1 transformers by connecting the secondary circuits in series, as shown in Figure 5.25a & b. In this arrangement, the ac voltages on the secondaries add, while the primaries can be driven at a low voltage by separate active devices. It should be noted that this configuration still has an impedance transformation ratio,  $N$ . Additionally, as there are  $N$  devices being power combined, the PER of such a (loss less) structure is  $N^2$ .

Unlike loop or spiral inductors, the two terminals of a slab inductor are not in close proximity of each other. This inherent property adds extra constraints to how they can be used. For example, if one is to make a parallel LC tank using a slab inductor, the parallel capacitor cannot be connected using regular wires, as the inductance and resistance of this wire will be comparable to that of the slab inductor. The absence of low-loss ground planes in silicon technologies exacerbates the situation and degrades the quality factor of



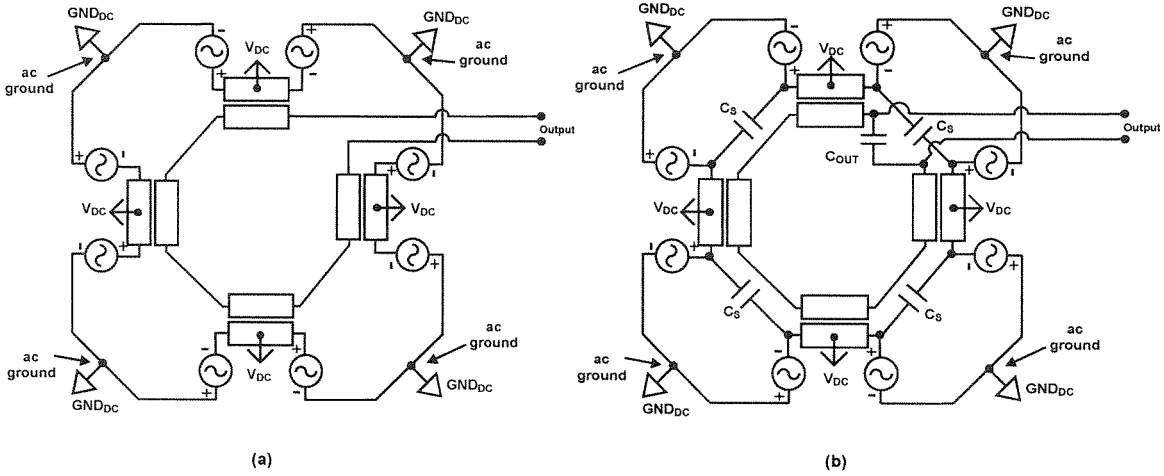
**Figure 5.25:** a) Fundamental building block of DAT.  $N$  independent power sources combined in series through  $N$  transformers with turn ratio 1:1, b) Same diagram using coupled slab inductors as the transformer, c) Same diagram using  $N/2$  transformers in double-differential configuration with grounds shared between adjacent power sources, except for the first and last sources in the chain.

slab inductors, if they are configured in such a way that the return current conducts through the substrate.



A *double differential* drive can solve this problem in a power amplifier. A virtual ac ground is created in the middle of the slab inductor if differential push-pull transistors drive it. This virtual ac ground can be used as a dc feed for the power supply, making the impedance of the dc biasing networking inconsequential as far as the differential signal is concerned. The differential drive solves only half of the problem as the ground connection for the driving transistors are not going to be in close proximity with each other. It is necessary to form an ac ground by connecting the two transistor grounds to stop the ac current from flowing through the lossy ground line and thus induce extra loss. Again, a wire cannot be used to form this ac ground, as its inductance will be comparable to that of the slab inductor itself. This problem can be solved by a double-differential drive shown in Figure 5.25c, where each driving transistor has an opposite phase to companion adjacent to it. In this case, the ac current flows through the adjacent transistors and hence an ac ground is created at their ground connections. Finally, to provide the same virtual ground for the two active devices at the ends of this combined structure, it can be wound to form a *distributed active transformer* (DAT), as depicted in Figure 5.26a for slabs. Although this winding will reduce the  $Q$  of the inductors, due to the negative magnetic coupling between opposite sides of the polygon, this effect is significantly lower than winding each transformer individually as the dimension of the total structure is much larger. The schematic of Figure 5.26a shows the central concept behind the *distributed active transformer* (DAT) structure. In this configuration, the impedance transformation and power combining functions are achieved concurrently. Also all the dc currents are provided to the amplifier through virtual ac grounds, which makes the amplifier insensitive to the means used to supply the dc voltages (e.g., length of bonding wires).

The DAT combines the relatively high primary inductance of the LC matching networks, the PER-independent efficiency of a magnetically-coupled transformer, and the high quality factor of slab inductors, while providing an effective means of power combining. In the DAT structure the loss is reduced because the voltages add on the secondary to combine power. Thus, the total ac current through the secondary inductor of



**Figure 5.26:** a)  $N$  independent power sources combined in series through  $N/2$  transformers in double-differential configuration with ground shared between every adjacent power sources using the circular geometry, b) Same diagram with cross-connected drain tuning capacitors and an output capacitor.

the DAT is smaller than the current through the LC matching inductor by a factor of  $\sqrt{r}$ . Since the impedance of the DAT secondary is larger than the LC matching inductor by the same factor, the loss of the DAT is smaller than that of the LC match by approximately a factor of  $\sqrt{r}$ . Additionally, while large currents do flow through the magnetizing inductors of the primary circuits in a DAT, the low-loss slab inductors minimize the associated loss due to their higher  $Q$ .

As discussed in Section 4.2 and shown in Figure 4.9a, the transformer's input shunt capacitor,  $C_s$ , is necessary for the transformer to present the proper impedance to the active device. As mentioned earlier,  $C_s$  cannot be placed in parallel with the slab inductors because of the physical distance between its terminals. However, placing capacitors between two adjacent ends of two slab inductors (Figure 5.26b) has exactly the same effect since the voltage across the capacitor will be identical to that of a capacitor in parallel with the slab. The output matching capacitor  $C_{out}$  can be simply placed in parallel to the load, as illustrated in Figure 5.26b. A representative drawing of this structure with 8 NMOS transistors and 4 slab transformers can be seen in Figure 5.12a.

A modified version of the transformer analysis described in Section 4.2 can be used to analyze the DAT. The new required primary inductance and the effective input admittance are given by

$$\omega L_1 = \frac{1}{(1 + A^2)} \frac{AR_l}{N} \quad (5.36)$$

$$Y_{in} \approx \frac{1}{1 + A^2 \frac{Q_1}{k^2} + Q_2} \left( \frac{N}{R_l} + j \frac{1}{\omega L_1} \right) \quad (5.37)$$

where  $N$  is the number of combined transistors. The new expressions for  $\omega L_1$  and  $Y_{in}$  in the presence of  $C_l$  and  $C_s$  can be derived using a similar derivation to that of Chapter 3.

The definition of PER can be generalized to the case of a matching/transformation network with multiple input ports. In this scenario, it is natural to define the power enhancement ratio (PER),  $E$ , as the ratio of the rf power delivered to the load with the network in place,  $P_{trans}$ , to the power delivered to load for one of the sinusoid input voltage sources driving the load directly,  $P_{one}$ . Based on this definition, the PER for the DAT can be calculated to be

$$E \approx (1 + A^2) \eta \frac{n^2 Q_1}{\frac{Q_1}{k^2} + Q_2} \quad (5.38)$$

Finally, the efficiency will be the same as the efficiency of a standard transformer matching circuit given by (4.22).

Several very important observations can be made about the DAT, when compared to conventional impedance transformation networks analyses in Chapter 4:

1. The power enhancement ratio (PER),  $E$ , of the DAT is proportional to the square of the number of transistors,  $N$ , as shown by (5.38). This is comparable to the PER of a standard transformer matching circuit with a turn ratio,  $n$ , given by (4.26).

2. Comparing (4.27) and (5.36), it can be seen that the primary inductance,  $L_I$ , will be  $N$  times larger in the DAT than the standard magnetically-coupled transformers. This will allow the DAT to use values that are more practical for  $L_I$  at the input ports.
3. In the DAT,  $N$  transistors generate the power and therefore each active device needs to deliver a smaller power to the passive structure. This difference manifests itself in (4.28) and (5.37), where the input conductance of each port in the DAT is  $N$  times smaller than the input of a standard magnetically-coupled transformer.
4. Unlike LC-resonant matching networks, the loss mechanism of the DAT structure is independent of the PER to the first order. It is noteworthy that standard magnetically-coupled transformers benefit from the same advantage.
5. The geometry of the DAT makes it possible to use 1:1 slab transformers. In the DAT, we can make the primary slab inductors wide to lower their series resistance. This reduction of loss in the primary is particularly important because large magnetizing currents flow in the primary circuits.
6. The two terminals of the slab inductors are not in close proximity of each other. The DAT uses a double-differential drive to be able to incorporate slab inductors into the design.
7. The distributed nature of the DAT can improve the thermal dissipation capability of the active devices up to a factor of  $N$  due to the more even distribution of the active device area across the chip.
8. The current in the secondary of the DAT is approximately  $N$  times smaller than in LC-resonant circuits, which allows narrower metal lines to be used on the secondary.

Table 5.1 summarizes the performances of each one of the discussed power combining, impedance transformation and harmonic tuning techniques.

	PER (E)	$\eta$	Power Combining	Drain Impedance	Lowest Inductor Reactance	Highest Inductor Reactance	Inductor Type	Harmonic Control
DAT	$\propto N^2$	Independent of E (4.22)	$N$	$\approx \frac{R_{load}}{\sqrt{E}}$	$\approx \frac{R_{load}}{\sqrt{E}}$	$R_{load}$	Slab and single turn spiral	Classes A, B, C, E/F <sub>x</sub> , and F <sup>-1</sup>
Transformer	$\propto n^2$	Independent of E (4.22)	1	$\approx \frac{R_{load}}{E}$	$\approx \frac{R_{load}}{E}$	$R_{load}$	Multi turn spiral	Classes A, B, and C
Single Resonant	$\propto \left(\frac{R_{load}}{\omega L_p}\right)^2$	$1 - \frac{\sqrt{E-1}}{Q_{ind}}$	1	$\approx \frac{R_{load}}{E}$	$\approx \frac{R_{load}}{\sqrt{E}}$	$\approx \frac{R_{load}}{\sqrt{E}}$	Single turn spiral	Classes A, B, and C
Multi Resonant	$\propto \left(\frac{R_{load}}{\omega L_{p,1}}\right)^{2n}$	$\left(1 - \frac{\sqrt{\frac{1}{E^n} - 1}}{Q_{ind}}\right)^n$	1	$\approx \frac{R_{load}}{E}$	$\approx \frac{R_{load}}{E^{1 - \frac{1}{2n}}}$	$\approx \frac{R_{load}}{E^{\frac{1}{2n}}}$	Single turn spiral	Classes A, B, and C

**Table 5.1:** Comparison of characteristics of several impedance matching and power combining techniques.  $N$  is number of active devices in a DAT,  $n$  is the turn ratio between primary and secondary circuits of a transformer, and  $E$  is PER.

## 5.11 Theoretical Design Examples

In this section, we will compare the performance of the three most promising methods of power enhancement techniques for silicon integrated power amplifiers discussed in Section 4.1, Section 4.2, and this chapter, namely LC resonant impedance transformation, magnetically coupled transformer, and DAT. A theoretical design process of a 2-W power amplifier will be demonstrated using these three techniques using 0.35- $\mu\text{m}$  CMOS transistors with a drain breakdown voltage around 6V. The passive parameters of this process are summarized in Table 5.2. Considering the knee voltage around 1V and the drain breakdown voltage of 6V, we will limit the drain ac voltage swing to 2V. To achieve 2W output power into a 50- $\Omega$  load with a 2-V drain ac voltage, we need a PER, higher than 50. For this design example, we have chosen a center frequency of 2.45GHz.

To obtain a PER of 50 using resonant impedance transformation (Section 4.1), we need to use a three-stage network, as determined by Figure 4.6. For this frequency and power level, the three inductors can be calculated using (4.15) to be 1.6nH, 0.35nH, and

Description	Value
Metal Thickness	3 $\mu\text{m}$
Metal Conductivity	10m $\Omega/\text{sq.}$
Metal Type	Al
Oxide Thickness	4.39 $\mu\text{m}$
Oxide $\epsilon_r$	4.0
Substrate Thickness	300 $\mu\text{m}$
Substrate $\epsilon_r$	11.9
Substrate Resistivity	8 $\Omega.\text{cm}$

**Table 5.2:** Process characteristic of a typical bulk silicon process used in the simulations for Section 5.11.

0.075nH. To obtain an estimate of the efficiency of the passive network, we can use ASITIC [50] to optimize these inductors, resulting in quality factors of 14, 10, and 3, respectively. The geometric mean of these quality factors can be used to approximate the efficiency of the passive network using Figure 4.6. With a mean  $Q$  of 7.5, the efficiency of the passive resonant matching network will be less than 50%. Even using a single LC section with an optimum<sup>1</sup> inductor  $Q$  of 15, Figure 4.2 indicates that passive efficiency cannot exceed 52%. Note that this is the efficiency of the passive network alone and does not include transistor or input power loss. It also assumes that ideal ac grounds can be provided and layout issues and parasitic components do not limit the performance. In practice, a resonator based passive network will have an even lower efficiency, for such high PER. Overall efficiency assuming 10dB gain and 70% transistor efficiency is limited to 32%.

The second alternative is a standard coupled-inductor transformer. If we assume a typical inductor  $Q$  of 8 and a coupling factor  $k$  of 0.6, we can obtain an passive efficiency of up to 68%, based on Figure 4.10. Although this is higher than that of resonant network,

---

1. This is the best value that could be obtained using SONNET [52] EM simulator for a spiral inductors in this process.

it is extremely difficult (if not impossible) to layout a moderate- $Q$  short and wide  $1j\text{-}\Omega$  (70pH at 2.4GHz) inductor<sup>1</sup> for the primary circuit and simultaneously inter-wind a secondary inductor with approximately  $50j\text{-}\Omega$  (3.3nH at 2.4GHz) and 7 turns without reducing the quality factors. Because of the physical layout constraints, these standard transformers will have a very narrow metal width and/or a reactance significantly higher than  $1j\text{-}\Omega$ . Due to these limitations, passive efficiency of these impedance transformation networks will be much lower than the theoretically predicted upper limit of 68%. Using more realistic  $Q$  of 5 with 52% passive efficiency, 10dB gain, and 70% transistor efficiency, the PAE is less than 32%.

Now, we can compare the LC-matching and coupled-inductor transformers with the distributed active transformer (DAT) structure. Since the primary of the DAT consists of a slab inductor, it achieves a  $Q$  of more than 30 in this process technology. The secondary loop of the DAT structure has a  $Q$  of 10 and coupling coefficient,  $k$ , of 0.6. The secondary parameters are comparable to a standard spiral transformer. Using (4.22), we predict a theoretical passive efficiency around 82%, for the DAT structure. As can be seen, The DAT achieves a higher passive efficiency than the resonant and standard transformer networks. Also, the double-differential drive of Figure 5.26b generating multiple virtual grounds makes it possible to implement a DAT on a lossy silicon substrate without a significant reduction in this theoretically predicted passive efficiency due to biasing and ground connections. The PAE limit assuming 10dB gain, 70% transistor efficiency is 52%.

## 5.12 DAT with Cascode Transistors

As described in Section 3.2.3, a cascode topology can be used in a DAT power amplifier for two purposes: to allow the higher voltage operation despite the drain and

---

1. The ASITIC optimized  $Q$  of this spiral inductor without the secondary is around 3.

gate low breakdown voltages and to increase the frequency response and gain of the transistor block. Although a DAT allows a very high power to be generated using a low supply voltage, in some cases the application demands the use of an undesirably high supply voltage, which, if directly applied to the transistor drain, will result in its breakdown. If the junction breakdown voltage supports the higher drain voltage, a two stage cascode block can support around twice the drain voltage and hence the amplifier can operate with a supply voltage twice that which a single transistor amplifier can afford. Whenever the junction breakdown voltage is not the limiting factor, multi-stage cascode may be implemented to obtain a gain block that supports even higher supply voltage.

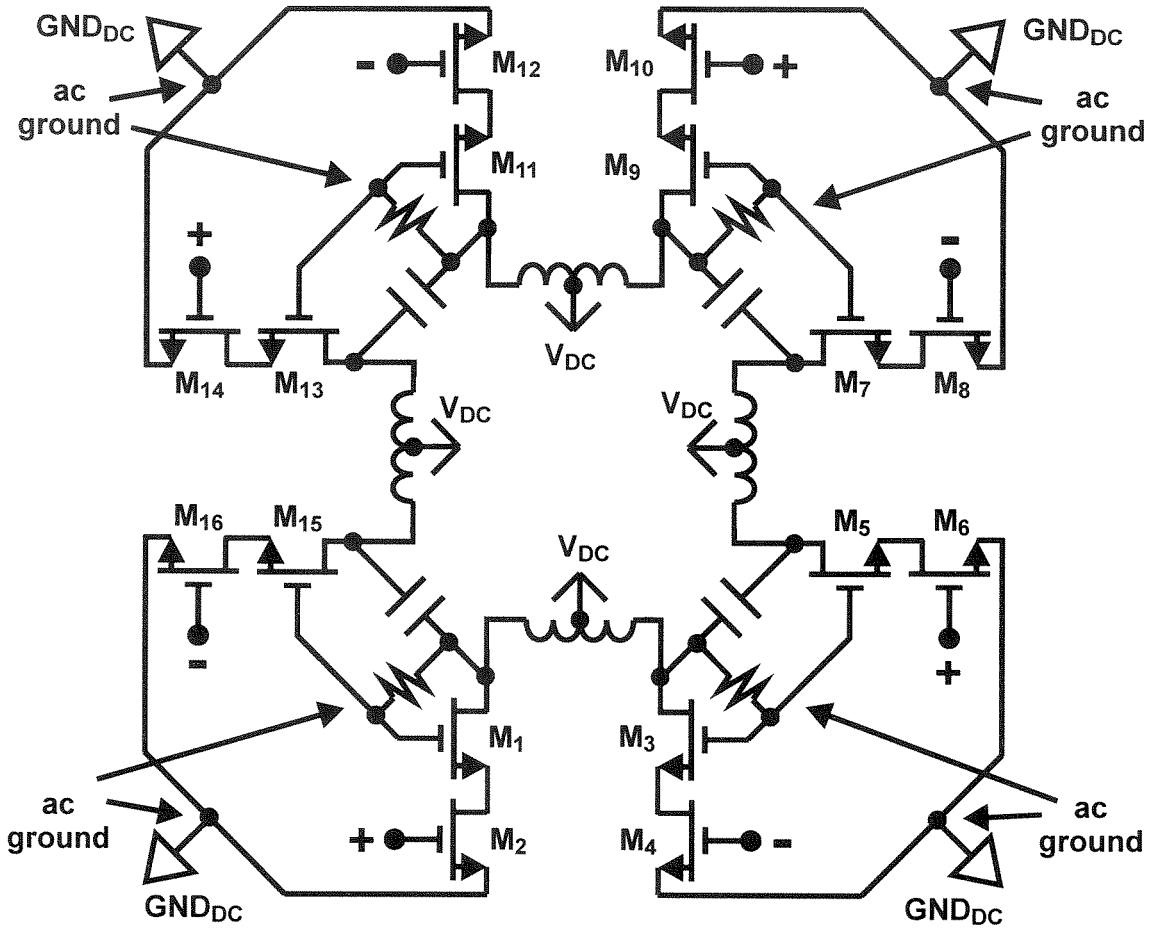
Moreover, in a DAT, we can take advantage of the circular geometry to avoid the use of large on chip capacitors to ac ground the gates of the upper stage transistors. As can be seen in Figure 3.26, in a basic cascode configuration using two transistors, the gate of the upper stage transistor must be ac grounded and must be provided a dc bias in order to operate as a common gate stage. If the gates of the two adjacent upper stage transistor are connected together and a dc voltage is supplied to this gate node through a high value resistor to isolate the ac signal, we have both a dc voltage and an ac virtual ground at each gate. Figure 5.27 shows an example of a cascode DAT using 16 NMOS transistors. The secondary loop is omitted in the drawing for ease of visualization.

This configuration can operate in any of the previously described classes of amplification, A, AB, B, C, or E/F<sub>odd</sub>, depending on the drain tuning, transistor size and gate bias voltage.

### 5.13 DAT with Embedded Two-Stage Gain Block

Another variation of the DAT is to have a two stage amplification block in each corner of the same. This will provide higher gain and higher PAE. As depicted in Figure 5.28, both stages are common source gain stages and the dc bias of the drain of the first stage is used as the bias of the gate of the second stage to avoid large dc on-chip decoupling capacitors.

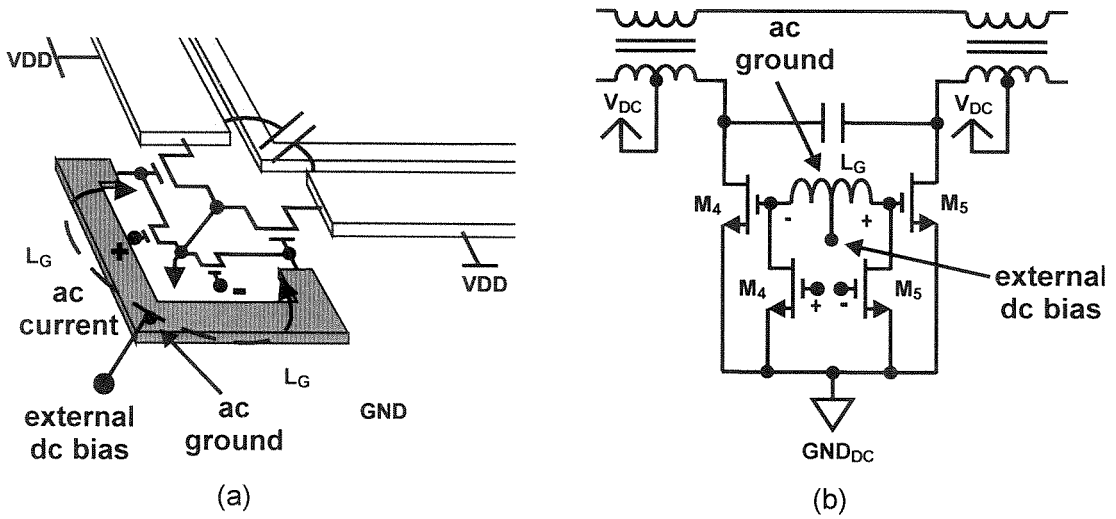




**Figure 5.27:** DAT power amplifier using eight cascode gain blocks with 16 NMOS transistors. The gates of the adjacent transistors of the upper stage are connected together to form an ac ground and are biased through a high value resistor connected to their drain. The output secondary loop is not depicted in this diagram.

The matching inductors are used to simultaneously resonate the drain capacitance of the first stage and the gate capacitance of the second stage.

Due to the simple parallel resonant matching in the interstage connection of this two stage amplifier, the first stage must operate as a transconductance amplifier. The second stage can operate either as a transconductance or switching power amplifier taking advantage of harmonic tuning provided by the double-differential push-pull topology. Figure 5.28a) and b) shows diagrams illustrating this topology.



**Figure 5.28:** Two stage common source DAT power amplifier. a) Illustration showing how the cross connected gate inductor is connected in this amplifier, b) Its corresponding electrical diagram.

Chapter  
**6**

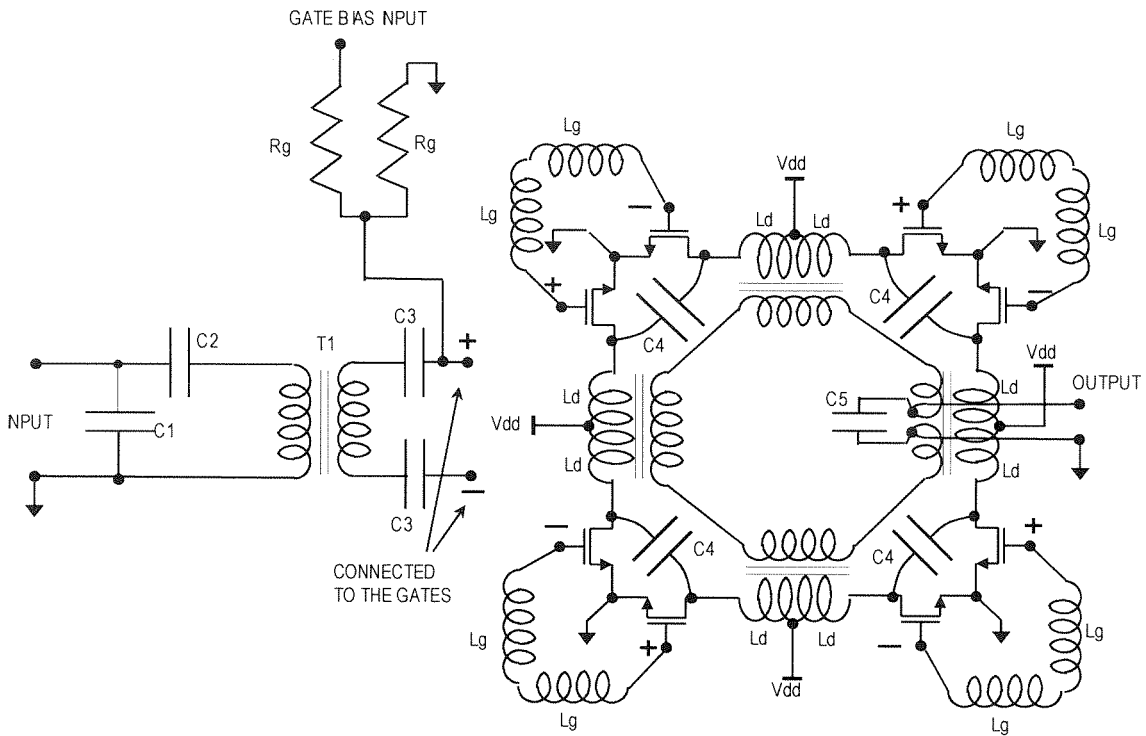
# *Implementation of the DAT Power Amplifiers*

## **6.1 Experimental Results of the First DAT Amplifier**

As a demonstration of the concept, a 2-W, 2.4-GHz single-stage fully-integrated DAT switching power amplifier operating in class E/ $F_3$  using  $0.35\mu\text{m}$  CMOS transistors in a BiCMOS process technology has been fabricated and tested. This process offers three metal layers, the top one being  $3\mu\text{m}$  thick with a distance of  $4.3\mu\text{m}$  from the substrate, which has a resistivity of  $8\Omega\cdot\text{cm}$ . The die area is  $1.3\text{mm} \times 2.0\text{mm}$  including pads. The complete electrical diagram of the designed circuit and microphotograph of the chip are shown in Figure 6.1 and Figure 6.2. Quasi-3D simulation using SONNET [52] and circuit simulation using Advanced Design System (ADS) [54] have been performed on the complete structure as a part of the design cycle to verify the performance of the amplifier.

Next, the steps followed in our design are presented. Once output power, the dc supply voltage and class of operation are chosen in accordance to the available technology and the application requirements, the designer should calculate how many transistors are required based on the theory detailed in Chapter 3 and Chapter 4. In a DAT the output power is determined approximately by these parameters and is very loosely related to the passive structure characteristics, such as inductance of the drain slab inductor. Several different design topologies, such as cascode, interdigitation, etc., suggested in Chapter 5 should be considered in the design process.

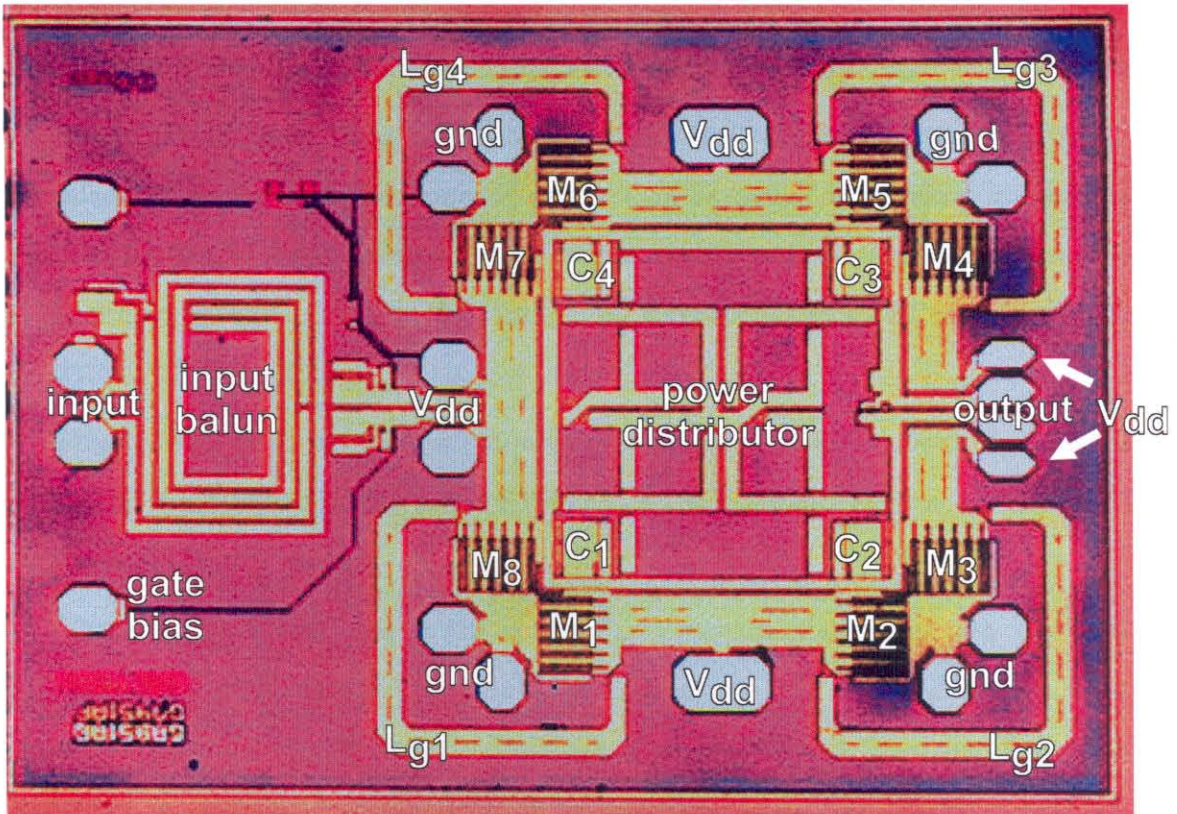
Next, a circuit simulation should be used with an appropriate transistor model, using ideal passive components to determine the best operating point of the push-pull power amplifier block with values of gate matching impedance, drain load impedance, and transistor size.



**Figure 6.1:** Electrical diagram of a complete DAT amplifier with four push-pull blocks.

The DAT passive structure should then be simulated using a planar 3D EM simulator and its parameters such as size, primary slab inductor width, secondary inductor width, spacing between the primary and secondary, number of primaries, number of secondaries, as described in Section 5.8, should be optimized to obtain the highest passive efficiency and an inductive drain impedance within a reasonable range of values<sup>1</sup>. As shown in Section 4.2 and Section 5.10, the power efficiency and drain impedances of the DAT are determined by these parameters. A very important factor in optimization is the use of a capacitor connected in series or in shunt to the output load. The value of this capacitor significantly affects the efficiency of the DAT as shown in Section 4.2. The

1. A reasonable value is an impedance, which in conjunction with the transistor output capacitance can be adjusted, using cross-connected capacitors, to a value suitable to the class of operation to be used at every harmonic frequencies.



**Figure 6.2:** Microphotograph of the first fabricated 2-W DAT power amplifier at 2.4GHz using 0.35 $\mu$ m CMOS technology.

cross-connected drain tuning capacitors do not affect the passive power efficiency of the DAT.

Once the highest passive efficiency and desirable drain conductances are obtained, cross-connected capacitors should be added to the EM simulation and adjusted to bring the drain conductance to a value suitable for the chosen class of operation as previously determined using the circuit simulation.

Next, the cross connected gate matching inductor model from EM simulation and the transistor model from circuit simulation should be included in the simulation and the size of the gate inductor should be optimized to resonate the gate capacitance obtaining a real value for the matched gate impedance.

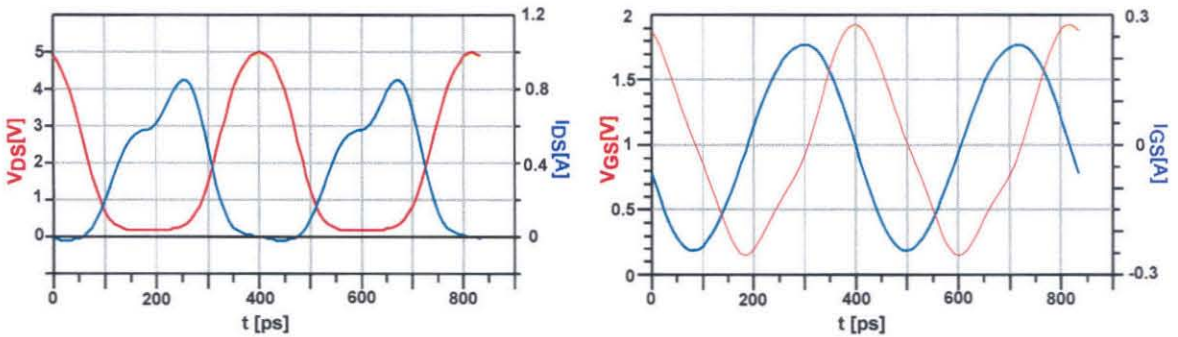


A full EM simulation should be done including the input power distribution network to obtain the impedance at the input of the power distribution network.

The balun should be designed and optimized to obtain the lowest power loss using the obtained distribution network input impedance as its output impedance. Capacitors in series or in parallel to this balun output should be used in optimization, their values chosen to minimize the power loss in the balun. The theoretical basis of this optimization is described in Section 4.2.

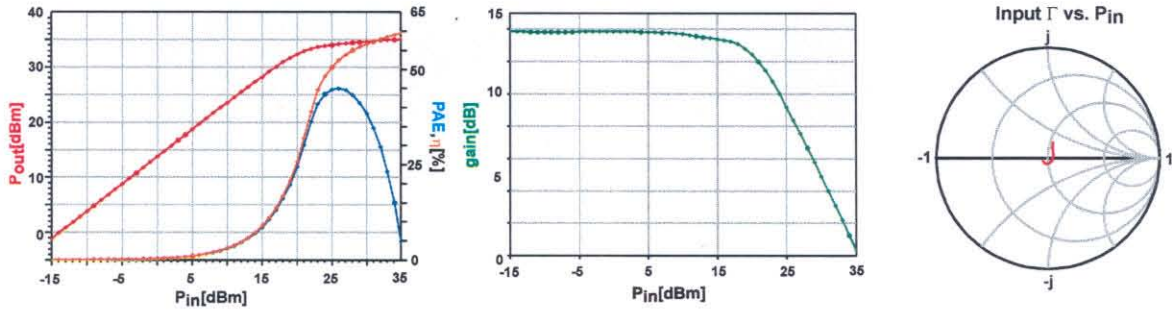
Finally, capacitors in series and in parallel to the input of balun should be adjusted to match the balun input to  $50\ \Omega$  and the DAT design is complete. Section 4.1 explains this final input matching process.

The simulated gate and drain voltage and current waveforms are depicted in Figure 6.3. A typical class E/ $F_{xx}$  waveforms as described in Section 3.3.1.6 can be seen, but with significant overlap between drain current and voltage waveforms as the operating frequency is relatively high compared to the transistor  $f_t$  (23GHz). Figure 6.4 shows the simulated  $P_{out}$ , PAE, input matching, and gain plots.



**Figure 6.3:** Simulated  $V_{DS}$  and  $I_{DS}$  vs. time and  $V_{GS}$  and  $I_{GS}$  vs. time of one of the 8 transistors of the DAT.

In our measurement, the chip is glued directly to a gold plated brass heat sink using conductive adhesive to allow for thermal dissipation. The chip ground pads are wire bonded to the heat sink. The input and output are wire bonded to  $50\ \Omega$  microstrip lines on

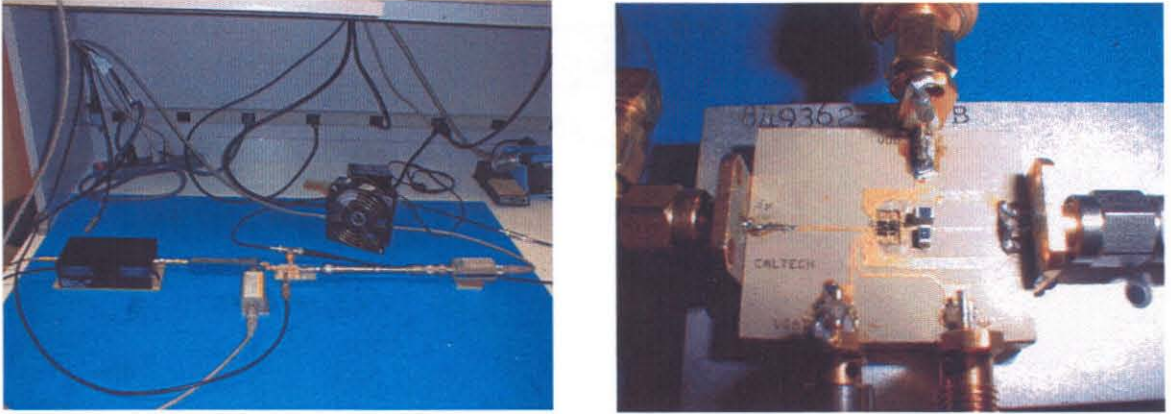


**Figure 6.4:** Simulated  $P_{out}$ , PAE, and  $\eta$  vs.  $P_{in}$ , gain vs.  $P_{in}$ , and input  $\Gamma$  vs.  $P_{in}$  of the 2.4GHz DAT prototype.

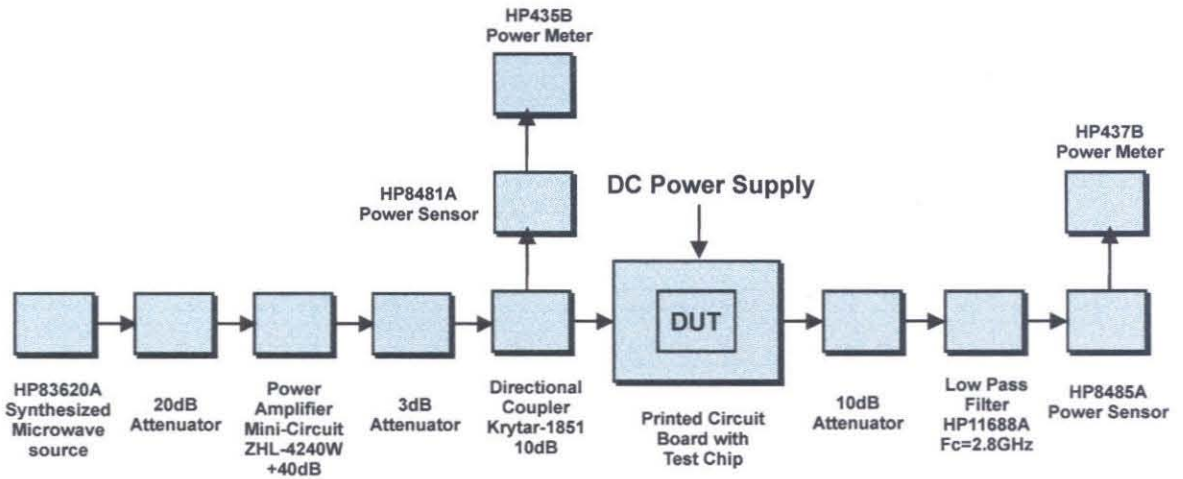
printed circuit board. Supply and gate bias pads are also wire bonded. The assembled test board for the measurement of the PA with balanced  $50\Omega$  load, provided by connecting a  $25\Omega$  chip resistor to one of the output terminals of the PA and another  $50\Omega$  chip resistor in parallel to a  $50\Omega$  transmission line connected to the second terminal, is shown in Figure 6.5. The input is driven using a commercial power amplifier connected to the circuit input through a directional coupler to measure the input return loss. The output is connected to a power meter through a 20dB attenuator and 2.9GHz low pass filter to avoid measuring harmonic signal powers. All measurement system power losses are calibrated out, including the connector and Duroid board losses. The bond wire power loss is included in the amplifier's measured performance. Block diagram of the measurement setup can be seen in Figure 6.6.

Driving a balanced load, an output power of 1.9W at 2.4GHz is obtained with 8.7dB gain using a 2V power supply. The corresponding power added efficiency (PAE) is 41% and drain efficiency,  $\eta$ , is 48%. The amplifier can also drive a  $50\Omega$  single-ended load, achieving a PAE of 31% with  $P_{out}$  of 2.2W (33.4dBm), gain of 8.5dB and drain efficiency of 36%. It can also produce 450mW into a single-ended  $50\Omega$  load using a 1V supply with a PAE of 27%. Figure 6.7, Figure 6.8 and Figure 6.9 show the gain and PAE vs. output power for 2V supply with differential output, 2V and 1V supplies with single-ended output respectively. Small signal gain biased for class-A operation is 14dB and input reflection coefficient is  $-9$ dB. The 3dB bandwidth is 510MHz centered at 2.44GHz. All





**Figure 6.5:** Measurement setup and DAT chip mounted on a printed circuit board and heat sink. (The two black components to the right of the PA chip on the PCB are chip resistors, which are a part of the balanced  $50\Omega$  load connected to the output of the amplifier.)

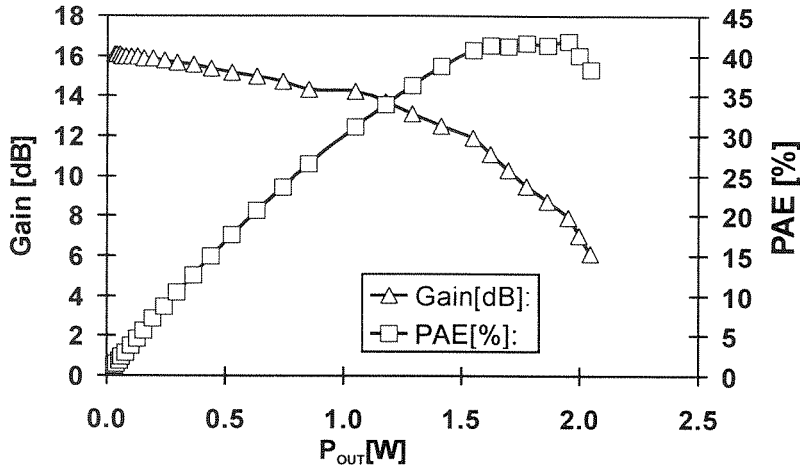


**Figure 6.6:** Block diagram of the measurement setup of DAT.

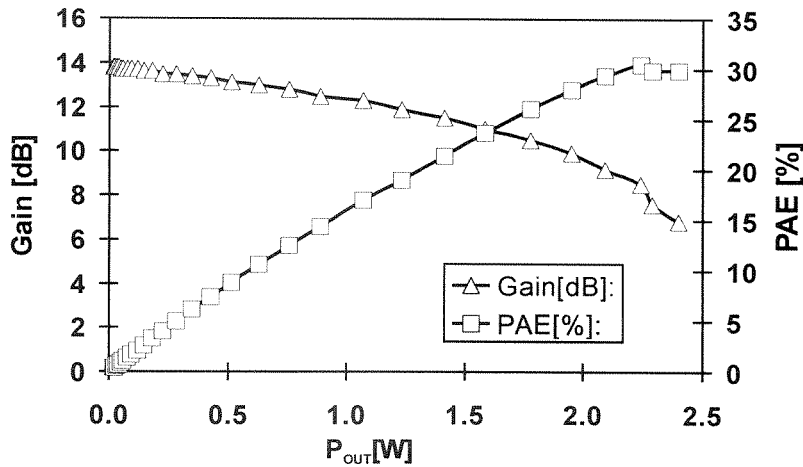
harmonics up to 20GHz were more than 64dB below the fundamental in the absence of the output filter.

Using the transistor parameters obtained from the Hspice transistor model ( $R_{on}=0.6\Omega$  and  $C_d=6.1\text{pF}$  for  $W=900\times 10\mu\text{m}$ ) and output network parameters obtained from Sonnet EM simulation ( $R_l=7\Omega$ ,  $\eta_{out}=0.7$ ), (5.33) predicts output power of  $P_{out}=33.9\text{dBm}$ , and





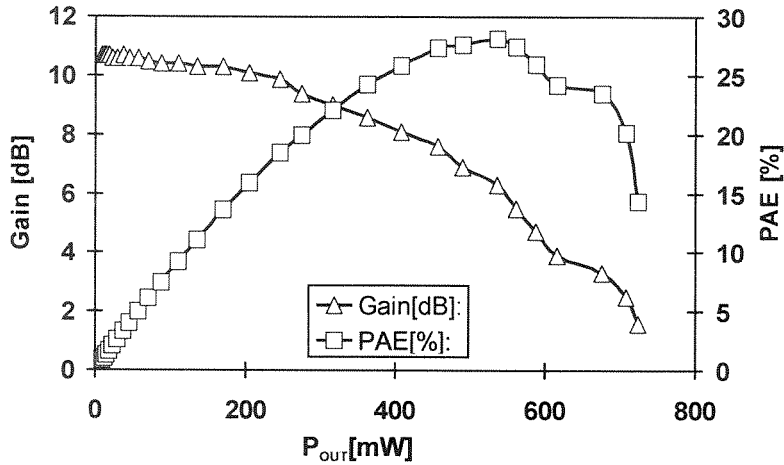
**Figure 6.7:** Measured PAE and gain vs. output power of the DAT power amplifier operating with 2V at 2.4GHz with 50 $\Omega$  balanced output.



**Figure 6.8:** Measured PAE and gain vs. output power of the DAT power amplifier operating with 2V at 2.4GHz with 50 $\Omega$  unbalanced output.

(5.35) predicts drain efficiency of 53%. The simulation predicts  $P_{out}=34.1$  dBm, and  $\eta=48\%$ .

Judging by the measured efficiency, we believe that all eight transistors are receiving approximately in-phase signals when the power amplifier is driving a symmetric differential load. On the other hand, the difference between the theoretical, simulated, and



**Figure 6.9:** Measured PAE and gain vs. output power of the DAT power amplifier operating with 1 V at 2.4 GHz with 50  $\Omega$  unbalanced output.

measured drain efficiencies with unbalanced load may be due to the transistor drive imbalance caused by the asymmetric feedback from the output signal. Also a difference in signal phase across the transistor area which is not accounted for in the simulation might also contribute to the simulation inaccuracy.

## 6.2 Comparison to the Best Published Results

In Table 6.1, we can see a comparison of this work to the other best reported partially or fully-integrated power amplifiers:

## 6.3 Discussion about Other Implementations of DAT Power Amplifiers

A total of four different DAT designs were fabricated using a 0.35  $\mu\text{m}$  CMOS process and measured for confirmation of the performance and to solve the difference between simulated and measured PAE with unbalanced load. Hence, all four designs are using shielded power distribution lines to minimize the asymmetric capacitive coupling of the signal from the output which, we believe, is the main cause of the difference.

Freq. (GHz)	P <sub>out</sub> (W)	Supply (V)	PAE (%)	Wirebond Inductor	External Comp.	Active Device	Reference
0.9	0.085	3	30 <sup>a</sup>	NO	NO	CMOS	[2]
1.9	0.1	3	16 <sup>b</sup>	NO	NO	CMOS	[3]
1.9	1.0	2	41	YES	YES	CMOS	[4]
0.9	1.0	1.9	41	YES	YES	CMOS	[5]
0.9	5.0	4.5	59	NO	YES	Si Bipolar	[6]
1.9	1.4	2.5	55	NO	YES	Si Bipolar	[7]
5-6	1.7	12	70	NO	NO	GaAsMESFET	[8]
1.9	0.63	3	52	NO	NO	GaAsMESFET	[9]
2.4	0.25	7	79	NO	NO	GaAsMESFET	[10]
0.9	0.2	5	49	NO	NO	SOI LDMOS	[11]
2.4	0.45	1	27	NO	NO	CMOS	DAT proto
2.4	1.9	2	41 <sup>c</sup>	NO	NO	CMOS	DAT proto
2.4	2.2	2	31	NO	NO	CMOS	DAT proto

**Table 6.1:** Comparative table of the performances of the most recent integrated power amplifiers.

a. Differential load.

b. Drain efficiency.

c. Differential load.

All three power amplifiers produced an output power over 1W in the 2GHz frequency range with 1 to 2V  $V_{dd}$ , showing the consistency of the DAT concept regarding its PER capability.

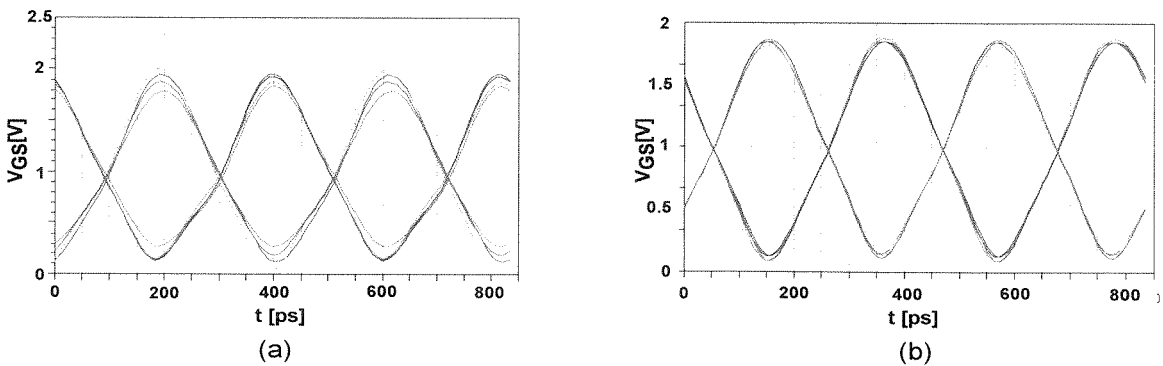
But, unfortunately, the measurement of all four designs presented a power gain around 7dB lower than the simulated value, per stage. This lower gain significantly reduced the PAE of these amplifiers. We believe that this may be the result of some process problem occurring in the transistors, as the difference of gain, simulation vs. measurement, per stage are similar in all four designs, even though they have a different number of stages and operates at different frequencies. As we have not included transistor rf test structures in this run, unfortunately, we are not able to confirm our thesis by checking the gain of a stand-alone transistor.

In addition to the above, a fifth DAT power amplifier using a  $0.15\mu\text{m}$  CMOS process was fabricated to test the DAT amplifier at very high frequency, 24GHz.

The simulated and measured results of the four most interesting ones among these five fabricated amplifiers are presented next.

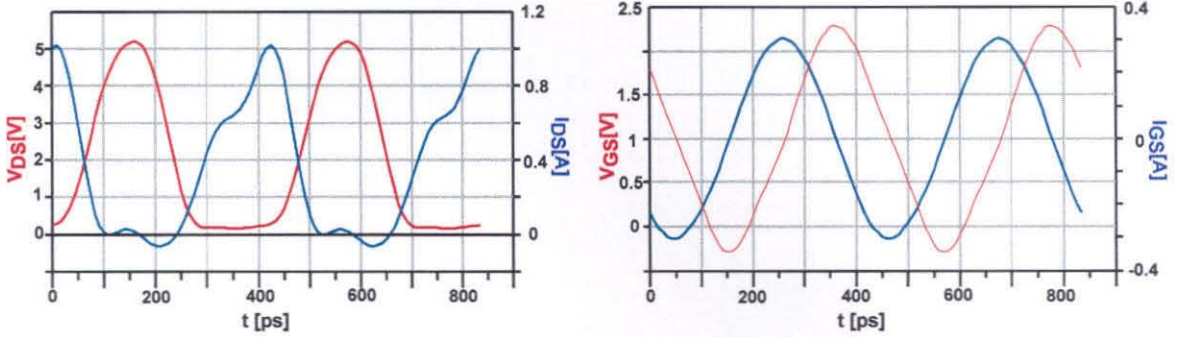
### 6.3.1 2-W/2.4-GHz/0.35- $\mu\text{m}$ Amplifier with Shielded Internal Power Distribution

The first 2.4GHz design has been elaborated to test if the shielded input power distribution, as described in Section 5.7.3, solves the problem of reduction in performance when PA is operating with unbalanced load. Figure 6.10 shows the simulated gate voltage waveforms of the eight transistors of the first DAT without shielding and of the same DAT using shielding. We can clearly see that the 8 gate signals of the second plot with shielding are better synchronized to each other than the signal of the first plot without the shielding. Except for the input distribution network, this PA is the same as the first built DAT. Simulated drain waveforms and performances of this DAT PA can be seen in Figure 6.11 and Figure 6.12.

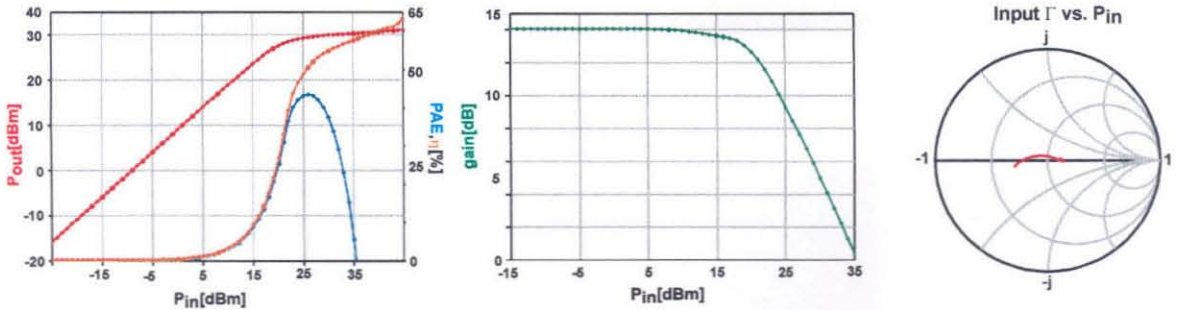


**Figure 6.10:** Simulated  $V_{GS}$  vs. time, each color representing one of eight transistor gates. a) the first DAT with twisted power distribution network. b) new DAT with shielded star distribution network.

Under the same measurement setup as in Section 6.1, in a small signal operation, the PA presents a measured gain of 6.1 dB and  $P_{out}=6.1$  dBm with  $V_{dd}=2$  V,  $I_{dd}=2.71$  A, and



**Figure 6.11:** Simulated  $V_{DS}$  and  $I_{DS}$  vs. time and  $V_{GS}$  and  $I_{GS}$  vs. time of one of the 8 transistors of the DAT.



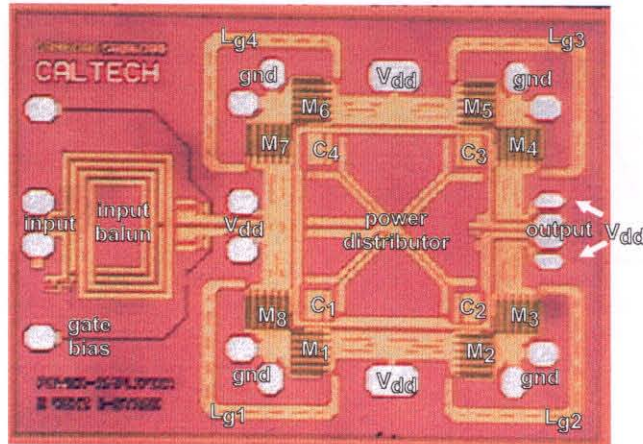
**Figure 6.12:** Simulated  $P_{out}$ , PAE, and  $\eta$  vs.  $P_{in}$ , gain vs.  $P_{in}$ , and input  $\Gamma$  vs.  $P_{in}$  of DAT.

$V_{gs}=0.7V$ . Under compression,  $P_{out}=32.6dBm$ , gain=4.6dB,  $\eta=29\%$ , PAE=19%, with  $V_{dd}=1.94V$ ,  $I_{dd}=3.19A$ , and  $V_{gs}=1.0V$  is obtained.

The microphotograph of the PA can be seen in Figure 6.13. The chip area is  $2.0 \times 1.3mm^2$  including pads.

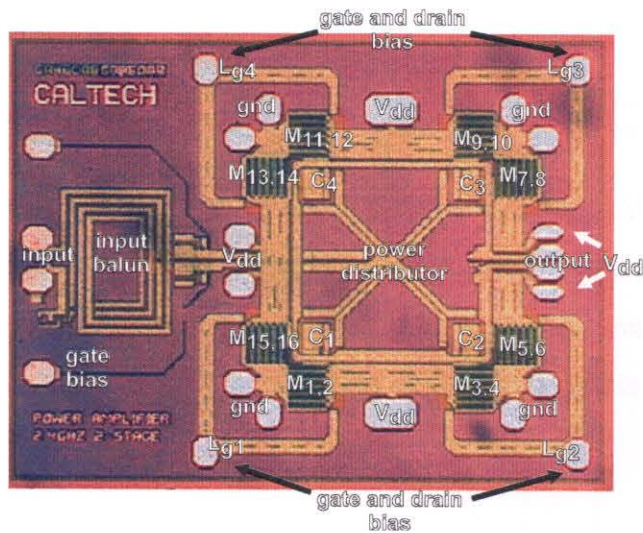
### 6.3.2 1-W/2.4-GHz/0.35- $\mu m$ Amplifier with Two Embedded Gain Stages

This design incorporates a two common source gain stages under double-differential topology as explained in Section 5.13, achieving a 45% PAE with 22dB small signal gain and 15 dB compressed gain in simulation. The drain of the first stage and the gate of the second stage are biased with one dc bias voltage and there are no dc decoupling capacitors between them, thus allowing a very compact two stage transistor block layout. The dc feed to this node is made through a pad located at the virtual ground of the cross-connected



**Figure 6.13:** Microphotograph of the DAT power amplifier at 2.4GHz using 0.35 $\mu$ m CMOS technology with shielded star power distribution network.

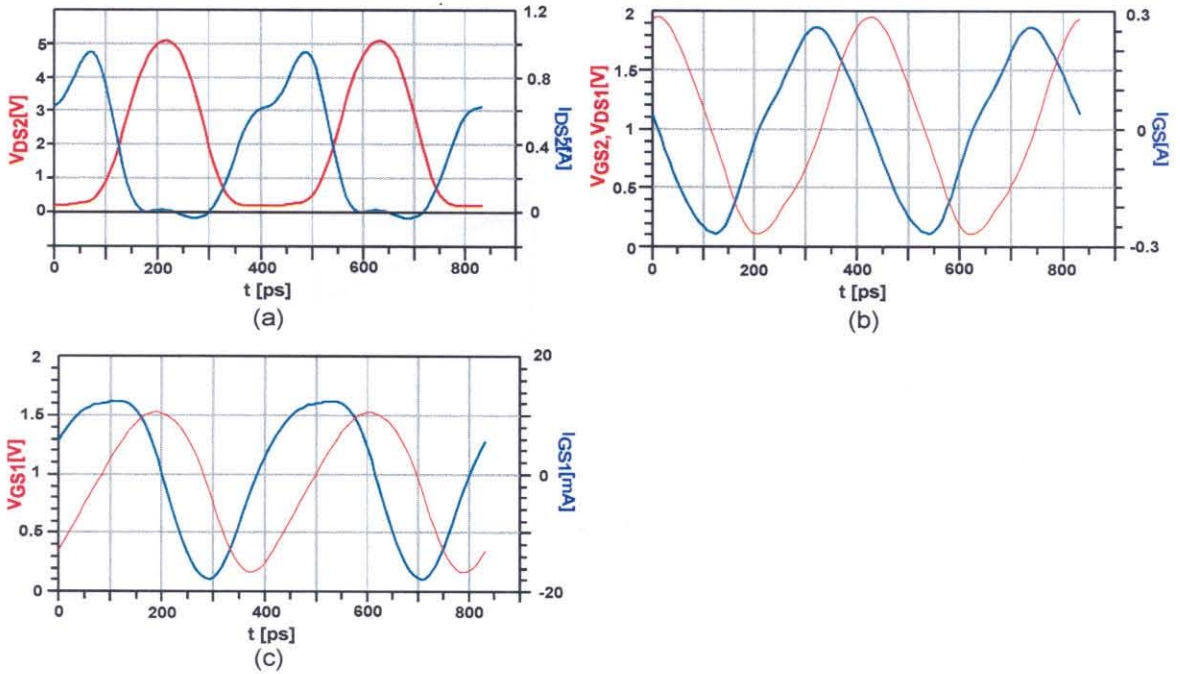
gate matching inductor as can be seen in the microphotograph of Figure 6.14. The gate



**Figure 6.14:** Microphotograph of the DAT power amplifier at 2.4GHz using 0.35 $\mu$ m CMOS technology with shielded star power distribution network.

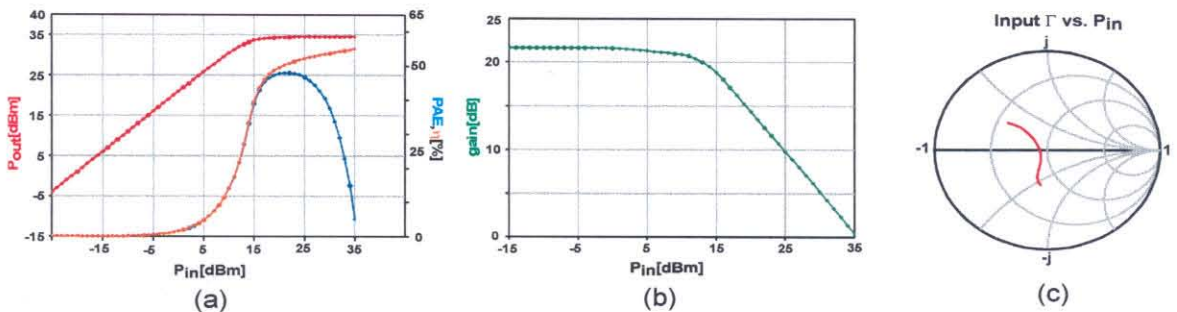
width of each second stage NMOS transistors are 10x912 $\mu$ m and of the first stage 10x90 $\mu$ m. Simulated drain waveforms and performances of this DAT PA can be seen in Figure 6.15 and Figure 6.16.





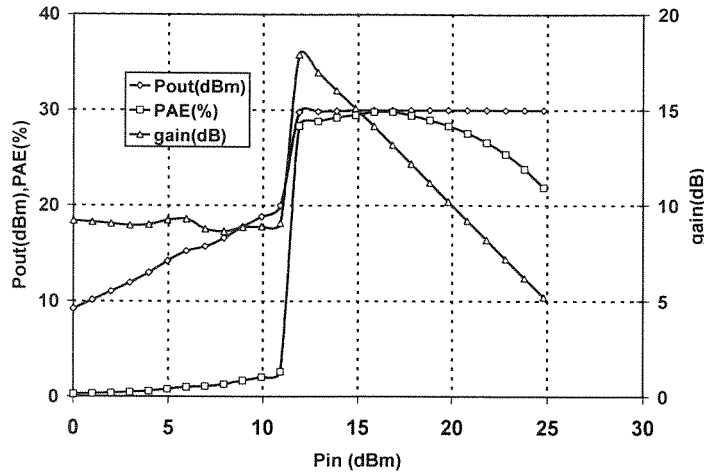
**Figure 6.15:** Simulated  $V_{DS2}$  and  $I_{DS2}$  vs. time,  $V_{DS1}$ ,  $V_{GS2}$  and  $I_{DS1}$  vs. time, and  $V_{GS1}$  and  $I_{GS1}$  vs. time of two of the 16 transistors of the two stage DAT.

Under the same measurement setup of Section 6.1,  $P_{out}=30$  dBm, gain=14dB,  $\eta=31\%$ , PAE=30%, with  $V_{dd}=1.15$  V,  $I_{dd}=2.6$  A are obtained for output stage,  $V_{dd}=0.75$  V,  $I_{dd}=0.33$  A for first stage, and  $V_{gs}=0.87$  V. Its measures PAE,  $P_{out}$ , and gain vs.  $P_{in}$  can be seen in Figure 6.17. The measured small signal gain is 7dB. The die area is



**Figure 6.16:** Simulated  $P_{out}$ , PAE, and  $\eta$  vs.  $P_{in}$ , gain vs.  $P_{in}$ , and input  $\Gamma$  vs.  $P_{in}$  of embedded dual stage DAT with  $V_{dd2}=2$  V,  $V_{dd1}=1$  V, and  $V_{GS1}=0.9$  V.

2.0x1.4mm<sup>2</sup>.



**Figure 6.17:** Measured  $P_{out}$ ,  $PAE$ , and gain vs.  $P_{in}$ , of an embedded dual stage DAT with  $V_{dd2}=1.15$  V,  $V_{dd1}=0.75$  V, and  $V_{GSI}=0.87$  V.

In the plot  $P_{out}$  vs.  $P_{in}$ , a sudden increase in the gain at  $P_{in}=11$  dBm can be seen which, we believe, is caused by a strong positive feedback inside the second stage transistors. Due to the non-linear transistor parasitic elements, the phase of the feedback might become positive when PA output power is above a certain level and an abrupt enhancement of the amplifier gain might have occurred at this power level and remain high above this point. This feedback mechanism, which might be useful to design injection locked amplifiers, is another subject for future investigations.

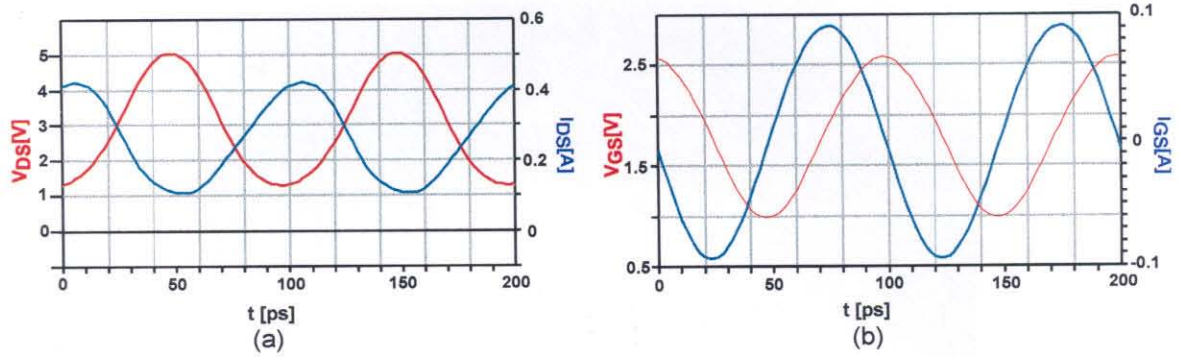
### 6.3.3 1-W/10GHz/0.35- $\mu$ m Amplifier

The 10GHz design has been assembled to test the highest frequency achievable in a design of integrated PA using a CMOS 0.35 $\mu$ m process.

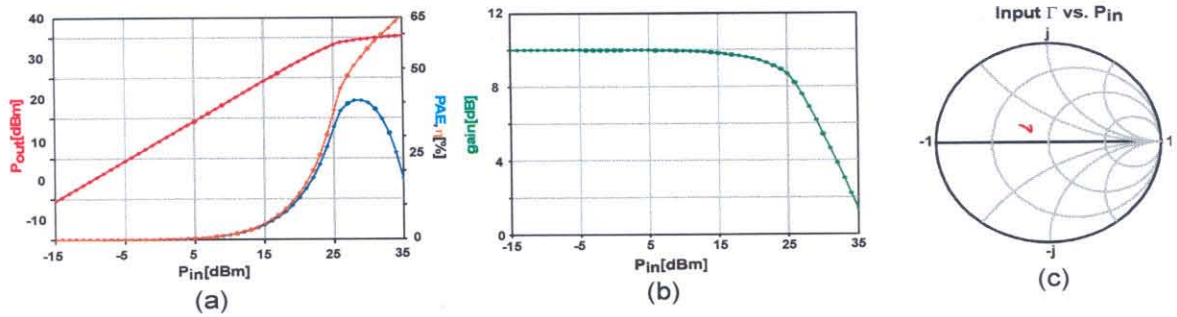
The amplifier has been designed to operate in class-A mode to extract the highest gain from the transistor in order to achieve the highest frequency. Transistor sizing and the drain tuning has been performed in accordance to meet the class-A requirements, as explained in Section 3.3.1.1. The width of each NMOS transistor is 10x100 $\mu$ m. Its simulated  $P_{out}$  is 1.1W,  $PAE=16\%$ , gain=9.5dB with  $V_{dd}=3$  V and  $V_{GS}=1.8$  V. Its



simulated drain waveforms and performances are shown in Figure 6.18 and Figure 6.19, in which we can see class-A drain waveforms. Due to thermal dissipation limitations imposed by the small thermal dissipation caused by small die area,  $0.9 \times 0.5 \text{ mm}^2$ , we believe that the amplifier cannot operate in CW above around 0.2 W.



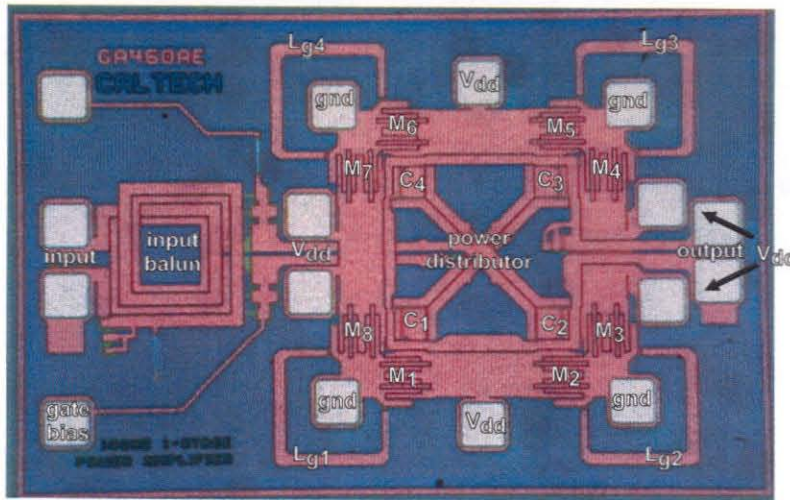
**Figure 6.18:** a) Simulated  $V_{DS}$  and  $I_{DS}$  vs. time. b)  $V_{GS}$  and  $I_{GS}$  vs. time of one of the eight transistors of the DAT.



**Figure 6.19:** a) Simulated  $P_{out}$ , PAE, and  $\eta$  vs.  $P_{in}$ , gain vs.  $P_{in}$ . b) Input  $\Gamma$  vs.  $P_{in}$  of DAT.

This PA is measured in small signal, with -10 dBm input, from 50 MHz to 40 GHz using a HP8722D VNA with GGB rf probes connected to input and output of the PA. Some of the measurements are done connecting the supply voltage and the gate bias using a PCB connected with wire bonds. Later measurements are done using dc probes instead of the PCB with no perceivable difference in the measured values. All the rf power losses of the setup including the loss of rf probes are de-embedded using the VNA's calibration routine and rf probe calibration standards on alumina board. The highest  $S_{21}$  was centered

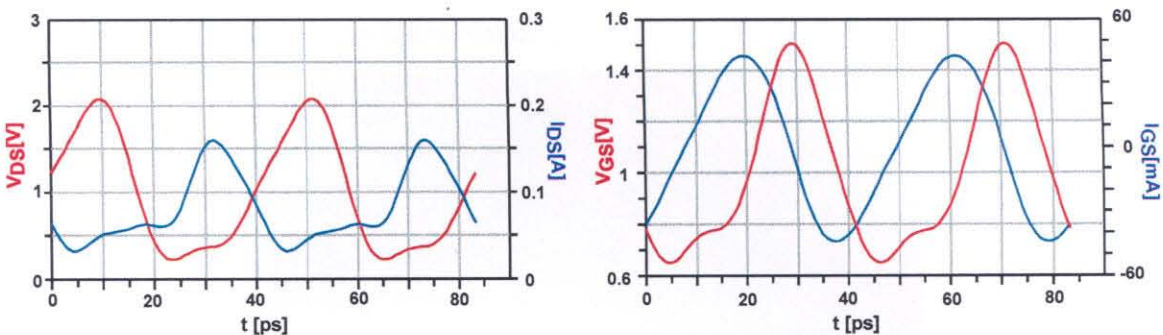
around 10GHz, but unfortunately measurements of 10 different PAs presented  $S_{21}$  around 0dB. Several different supply voltage from 0.5 to 3 V and gate bias voltage from 0.5 to 2 V are applied during the gain measurement seeking a higher gain. The die area is  $0.6 \times 0.5 \text{ mm}^2$ . Figure 6.20 shows the micrograph of the PA die.



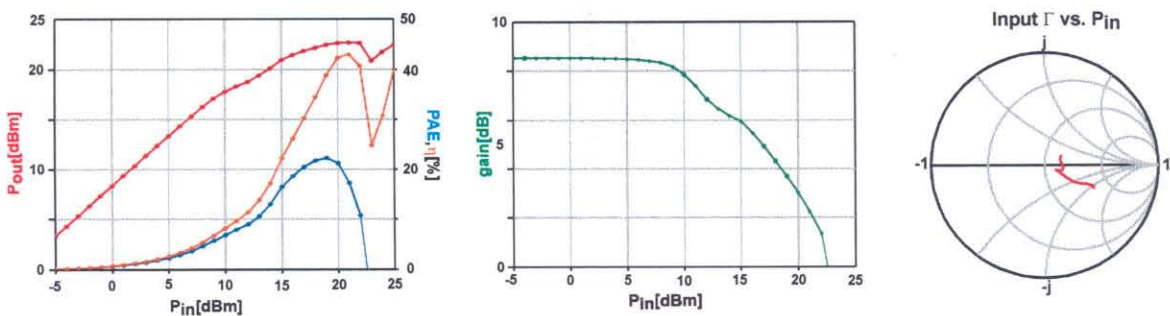
**Figure 6.20:** Micrograph of the 1-W DAT power amplifier at 10 GHz using  $0.35 \mu\text{m}$  CMOS technology with shielded star power distribution network.

### 6.3.4 150-mW/24GHz/0.15- $\mu\text{m}$ Amplifier

Using a  $0.15 \mu\text{m}$  gate length CMOS process with  $f_t$  around 80GHz, it is possible, in principle, to design a 24 GHz/150 mW DAT power amplifier using eight transistors. To verify this, a design was fabricated in  $0.15 \mu\text{m}$  CMOS process, with process characteristics shown in Table 6.2. The width of each NMOS transistors are  $10 \times 25 \mu\text{m}$  in this design. Simulated drain waveforms and performances of this DAT PA can be seen in Figure 6.21 and Figure 6.22. Since an on-chip balun would present a high power loss the design utilizes a  $100 \Omega$  differential input. The output of the amplifier can be connected directly to a balanced or unbalanced  $50 \Omega$  load. In this design, the cross-connected capacitor is located below the ground metal at the corners of the DAT as indicated in the die micrograph of Figure 6.23. As this process did not offer a MIM capacitor, the vertical bars



**Figure 6.21:** Simulated  $V_{DS}$  and  $I_{DS}$  vs. time and  $V_{GS}$  and  $I_{GS}$  vs. time of one of the 8 transistors of the 24GHz DAT amplifier.



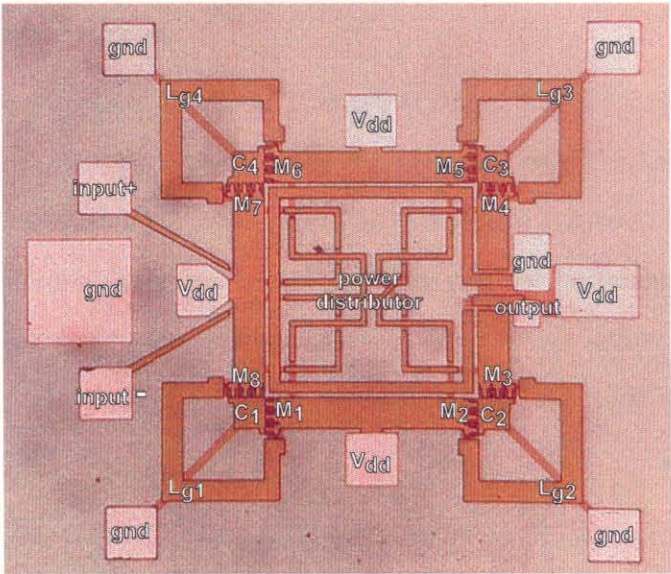
**Figure 6.22:** Simulated  $P_{out}$ , PAE, and  $\eta$  vs.  $P_{in}$ , gain vs.  $P_{in}$ , and input  $\Gamma$  vs.  $P_{in}$  of DAT.

Description	Value
Thickness of Top Metal	1 $\mu\text{m}$
Thickness of m2 to m6	0.53 $\mu\text{m}$
Thickness of m1	0.41 $\mu\text{m}$
Metal Type	Al
Thickness of SiO <sub>2</sub> from Top Metal to Substrate	8.3 $\mu\text{m}$
$\epsilon_r$ of SiO <sub>2</sub>	3.7
Thickness of SiO <sub>2</sub> between each Metal Layer	1.2 $\mu\text{m}$
Substrate Resistivity	8 $\Omega\text{cm}$
Substrate Thickness	725 $\mu\text{m}$

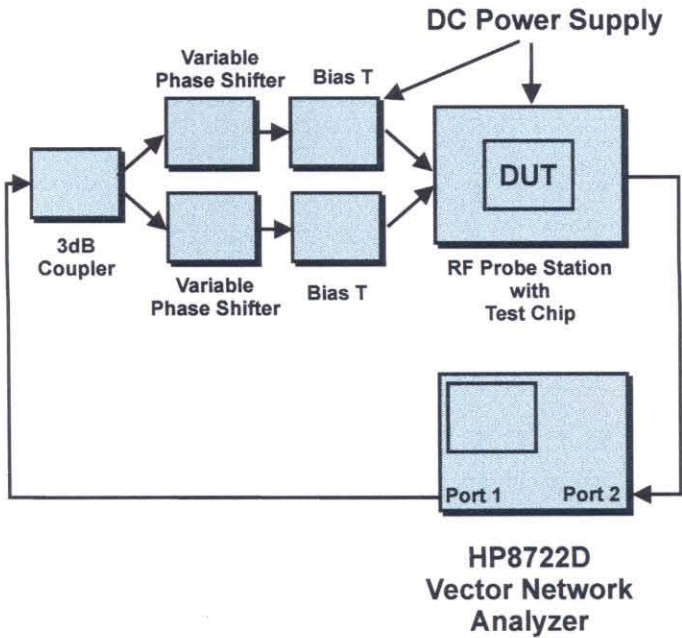
**Table 6.2:** Characteristics of the process used for 24GHz DAT amplifier.



capacitor [55] structure is used for the first time in this circuit for all necessary capacitances. The die area is  $0.6 \times 0.5 \text{ mm}^2$ .



**Figure 6.23:** Micrograph of the DAT power amplifier at 24GHz using 0.15 $\mu\text{m}$  CMOS technology with twisted power distribution network.



**Figure 6.24:** Measurement setup of the 24GHz/120mW DAT power amplifier.

The power amplifier is measured using an HP8722D network analyzer using the setup shown in Figure 6.24, with rf probes for input and output and wire bond connection for the supply, dc ground, and gate bias.

After a careful calibration, a gain of 3 dB at 24 GHz in two different dies is measured. Unfortunately, due to the aggressive design, the structure of the output pads limited the performance achieved in this measurement. The 3 dB gain is achieved with relatively light contact pressure between the rf probe and the pad, and the performance is observed to improve with increased pressure. Unfortunately, a dc bias line below the pads limits the contact pressure to a low value as higher pressure results in a short-circuit between the supply and the output.

## Chapter

## 7

*Conclusion*

The design of a fully-integrated power amplifier with a reasonable output power, efficiency and gain has been one of the major challenges in today's pursuit of a single-chip wireless integrated transceiver. In order to produce Watt-level output power into a  $50\Omega$  load using supply voltage of less than 3 V, designers are forced to use impedance transformations between the active device and the load. Such impedance transformation networks are fundamentally limited in ways which make conventional implementations on integrated circuits infeasible. Consequently, power amplifiers to date have either used external matching components or have been limited to low output power levels. As the breakdown voltage of future CMOS generations continues to decrease, reducing both the system supply voltage and the allowable voltage across the active device in the output stage, the need for impedance transformation becomes more acute and the problem associated with it become more challenging.

To overcome this problem, a novel *distributed active transformer* (DAT) is presented as a means for accomplishing simultaneous series power combining and impedance transformation using a topology which is compatible with integrated circuit implementations. This technique allows high-efficiency on-chip impedance matching while achieving high output powers from low supply voltages. Furthermore, the technique is easily adapted to future decreases in supply voltage without significantly affecting the efficiency. Additionally, the topology is compatible with many difference classes of operation including the transconductance amplifier classes A, B, and C as well as the new  $E/F_{\text{odd}}$  switching amplifier class. A thorough analytic analysis of the DAT performance is presented, and the results compared to similar analysis for the two most common impedance transformation techniques.

To demonstrate the viability of the DAT technique, several prototypes have been fabricated and tested, including the *first reported Watt-level GHz range fully-integrated CMOS RF power amplifier*. It uses 0.35- $\mu\text{m}$  CMOS transistors, achieves 2-W output power, and 41% power added efficiency (PAE) at 2.4-GHz. Its input and output are internally matched to 50 $\Omega$ . No off chip components are used. It can also produce 450 mW using a 1-V supply. In order to explore the potential of the DAT, several other versions of DAT power amplifiers at different frequencies, classes, topologies, and power levels have been fabricated and measured.

## 7.1 Recommendations for Future Investigations

The DAT presented in this work can be further explored at different frequencies, power levels, and technologies. Other variations of DAT may also be feasible such as DAT based spacial combining, oscillator, dual band amplifier, linear amplifier, etc.

Using a conventional silicon CMOS technology, it should be possible to implement power amplifiers at higher frequencies up to around 30GHz using 0.13 $\mu\text{m}$  technology. In terms of efficiency, by using process utilizing thicker metal and other efficiency enhancement methods presented in this work, such as interdigitation and external power distribution, it should be possible to achieve PAE up to around 70% at low microwave frequencies from 1 to 10GHz. Increasing the number of transistors combined, either with higher segmentation of the circular geometry and/or series combining of the transistors, it should be possible to achieve a significantly higher power level with integrated DAT up to around 10 W.

At lower frequencies, interesting discrete circuits can be fabricated using the DAT topology, which operates from 50MHz to 2GHz. Several LDMOS transistors may be combined in DAT operating in E/F<sub>odd</sub> class, achieving a very high output power, perhaps even several KWs with high efficiency and very compact size. Below 50MHz, several VDMOS can be combined to achieve even higher power, 10KW levels, with around 80%

efficiency. These might be useful for broadcast transmission or as a source for industrial plasma generators.

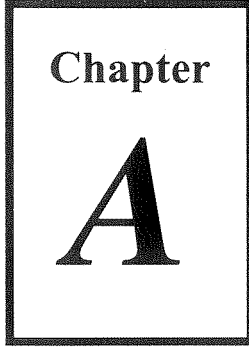
Another interesting project is to achieve a relatively high rf output power, around a few hundred Watts to KWs, using a standard supply voltage, such as 12 V or 24 V. This might be useful for applications such as HAM radio.

A very compact high-efficiency power amplifier might be fabricated using GaAs or InP MMIC technology. An amplifier using the DAT technique might be significantly smaller than ones using quarter-wavelength matching techniques. SOI technology might also be applied to DAT structures, obtaining higher efficiency, higher frequency, and/or ultra low supply voltage amplifiers.

Finally the DAT without a secondary loop, *the circular geometry*, CG, can be used to directly radiate the rf signal into space or waveguide, thus eliminating one of the power loss components, the secondary loop of the DAT. The current through the loop of the CG creates a magnetic field, which is coupled to the free-space or waveguide in a similar way to the operation of a loop antenna. The matching of CG into free-space can be facilitated by the use of a second larger matching passive metal loop placed around the CG, technique commonly used in UHF antennas.

Among the contributions offered by the DAT, the cost and size reductions realized by full integration using CMOS technology are the most significant. Due to these advantages, the most promising application for the DAT with immense potential to be explored lies in massive volume markets. Furthermore, since the DAT structure can be implemented in CMOS, the potential to provide integrated solutions to these markets with the power amplifier integrated into the same die as the other rf components is very high. Future investigations should explore the issue relating to this integration with other rf components.





# *Resonant Network Efficiency Computation*

To calculate the LC matching network efficiency  $\eta$  as a function of  $E$  and  $Q_{ind}$ , we eliminate the terms  $r$  and  $\eta$  from the definition (4.10), using (4.5) and (4.6), and isolate the term

$$\frac{1}{1 + R_{load}/R_{lp}} :$$

$$E = r\eta = \frac{\left(1 + \frac{R_{load}}{R_{lp}}\right)^2 + Q_{ind}^2 \left(\frac{R_{load}}{R_{lp}}\right)^2}{\left(1 + \frac{R_{load}}{R_{lp}}\right)^2} \quad (A.1)$$

$$\frac{1}{1 + \frac{R_{load}}{R_{lp}}} = 1 - \frac{\sqrt{E-1}}{Q_{ind}}$$

This isolated term is  $\eta$  by (4.5):

$$\eta = \frac{1}{1 + \frac{R_{load}}{R_{lp}}} = 1 - \frac{\sqrt{E-1}}{Q_{ind}} \quad (A.2)$$

(A.2) stands as  $E$  is approximately square of  $R_{load}/\omega L_p$  and  $Q_{ind}$  is  $R_{lp}/\omega L_p$ .

Substituting  $R_{lp}$  in the definition (4.4) using (A.1), we can find a solution for  $\omega L_p$ , as shown by (4.12).

For the multi section case, we have

$$\eta = \frac{P_{out}}{P_{in}} = \eta_1 \eta_2 \eta_3 \dots \eta_n = \left(1 - \frac{\sqrt{E_1-1}}{Q_{ind}}\right) \left(1 - \frac{\sqrt{E_2-1}}{Q_{ind}}\right) \dots \left(1 - \frac{\sqrt{E_n-1}}{Q_{ind}}\right) \quad (A.3)$$

If we assume that each individual  $E_k$ s are equal, we have

$$E = E_1 E_2 \dots E_n \quad (\text{A.4})$$

$$E_1 = E_2 = \dots = E_n = E^{\frac{1}{n}} \quad (\text{A.5})$$

and from the above, we obtain

$$\eta = \left( 1 - \frac{\sqrt{\frac{1}{E^n} - 1}}{Q_{ind}} \right)^n \quad (\text{A.6})$$

The total efficiency of the network is the product of the efficiency of each stage. Simultaneously, if the total PER is  $E$ , the PER of each stage will be  $E^{1/n}$ . Analyzing the Figure 4.5 we can calculate the inductor value for each stage in a similar way as in a single section network:

$$\omega L_{p,1} = \frac{R_{lp,1}}{Q_{ind}} = \left( \frac{1}{\sqrt{\frac{1}{E^n} - 1}} - \frac{1}{Q_{ind}} \right) R_{load} \quad (\text{A.7})$$

$$\omega L_{p,k} = \frac{R_{lp,k}}{Q_{ind}} = \left( \frac{1}{\sqrt{\frac{1}{E^n} - 1}} - \frac{1}{Q_{ind}} \right) R_{in,(k-1)} \quad (\text{A.8})$$

From (4.1), (A.1), and (A.2), we have

$$R_{in,k} = \frac{1 - \frac{\sqrt{\frac{1}{E^n} - 1}}{Q_{ind}}}{\frac{1}{E^n}} R_{in,(k-1)} \quad (\text{A.9})$$

From (A.7), (A.8) and (A.9), we have

$$\omega L_{p,k} = \left( \frac{1}{\sqrt{\frac{1}{E^n} - 1}} - \frac{1}{Q_{ind}} \right) \left( \frac{\frac{1 - \sqrt{\frac{1}{E^n} - 1}}{Q_{ind}}}{\frac{1}{E^n}} \right)^{k-1} R_{load} \quad (\text{A.10})$$

## Chapter

**B*****Transformer  
Efficiency  
Computation***

The transformer efficiency,  $\eta$ , is the ratio of power,  $P_{load}$ , dissipated in the load resistance  $R_l$  and total power,  $P_{total}$ , dissipated in  $R_1$ ,  $R_2$  and  $R_l$ .

$$\begin{aligned}\eta &\equiv \frac{P_{load}}{P_{total}} = \frac{|I_2|^2 R_l'}{|I_1|^2 R_1 + |I_2|^2 (R_2' + R_l')} = \frac{|I_2|^2 R_l'}{|I_2 + I_M|^2 R_1 + |I_2|^2 (R_2' + R_l')} \\ &= \frac{|I_2|^2 R_l'}{|I_2|^2 \left( \frac{(R_2' + R_l')^2 + (\omega L_2/n^2 - 1/(n^2 \omega C_l))^2}{(k\omega L_1)^2} \right) R_1 + |I_2|^2 (R_2' + R_l')} \quad (B.1)\end{aligned}$$

where

$$R_2' = \frac{R_2}{n^2} \quad R_l' = \frac{R_l}{n^2} \quad (B.2)$$

To maximize  $\eta$  in the above expression,  $C_l$  should resonate  $L_2$  at the frequency of interest, *i.e.*,

$$\frac{1}{\omega C_l} = \omega L_2 \quad (B.3)$$

This condition minimizes the current  $I_l$  through  $R_l$  and its dissipated power by resonating the inductors  $(1-k)L_2/n^2$  and  $kL_1$  with the capacitor  $C_l$ .

Assuming  $L_l \cong L_2/n^2$  and using and (B.3), we can further simplify (B.1) to

$$\eta = \frac{R_l/n^2}{\frac{(\omega L_1/Q_2 + R_l/n^2)^2}{(k\omega L_1)^2} \frac{\omega L_1}{Q_1} + \frac{\omega L_1}{Q_2} + R_l/n^2} \quad (B.4)$$

which is obtained by dividing the equivalent load resistance,  $R_l/n^2$ , by the sum of three equivalent resistances, which are  $R_2/n^2$ ,  $R_l/n^2$ , and  $R_I$  reduced by the ratio  $I_1/I_2$ .

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