Chapter 3

Molecular Electronic Crossbar Memory Circuits

3.1 Introduction

In chapter 2, I described the fabrication procedures for molecular switch tunnel junction (MSTJ) device at a single device level and also proved that bistable [2]rotaxane plays a crucial role in a decent conductance switching. The [2]rotaxane molecular switches hold several advantages over more traditional switching components such as ferroelectric (1) and ferromagnetic materials (2). However, a key application of these molecular switches is related to the extreme scaling of electronic circuitry to near molecular dimensions: since conductance switching within an MSTJ originates from the electrochemically driven molecular mechanical isomerization of the molecules, the switching relies purely on individual molecular properties. In both molecular dynamics (MD) and electrochemical investigations (3-5), the two molecular co-conformers are characterized by different HOMO-LUMO gaps, and therefore different tunneling probabilities (6, 7). By contrast, the switching of solid state materials such as ferroelectrics involves altering the polarization state of the crystallographic lattice upon the application of an external electric field. This polarization disappears for domains below a certain critical size. An analogous

phenomennon is the transition from ferromagnetic behavior to superparamagnetic behavior for magnetics, as the size of the ferromagnetic material is reduced. Therefore, these devices have a critical limitation in the scale-down. Second, solid state material switching depends upon a field-driven nucleation process and can be statistical in nature, especially for small crystallographic domain sizes. The molecular switches discussed in this thesis, by contrast, switch based upon electrochemical processes. These are current and voltage driven, and depend upon molecular properties such as redox potentials, molecular orbital energies, etc. Therefore, switching voltages for the ferroelectric device could vary from junction to junction, or during many cycles. In particular, at a smaller dimension, the reliability issues are expected be more serious. When the solid state materials are integrated into a 2D crossbar circuit that is a main architecture of the memory devices described here, their irregular switching characteristic will cause an additional problem, that is, 'a half select issue' (8). In the crossbar memory circuit, a switching voltage, V_A, is split into two components, +½ V_A and -½V_A, which are then applied to the top and bottom electrodes that define a designated cross-junction. As all of the junctions are interconnected in a crossbar circuit, every junction is subject to at least some field. For the case of the solid state materials, the field generated by ± ½ V_A is occasionally sufficient to perturb the state

of the nucleation event. This half-select problem is considered as a generic problem for the field-poled devices that function within a 2D crossbar circuit.

Taking advantage of the switching molecules, the next challenge is to integrate those switching molecules and electrodes into fully functional circuits, patterned at nanometer dimensions. When such a memory circuit is combined with other nanoscale functional circuits such as logic and routing, computing at nanometer dimensions, which is currently unachievable with standard CMOS technology, could be realized. Entire circuits for nanoscale computing were proposed as conceptualized in figure 3-1. While efforts in my research group have focused on developing and integrating the various components of this nano-computer (8-11), this chapter will address fabrication and testing of crossbar memory circuits exclusively.

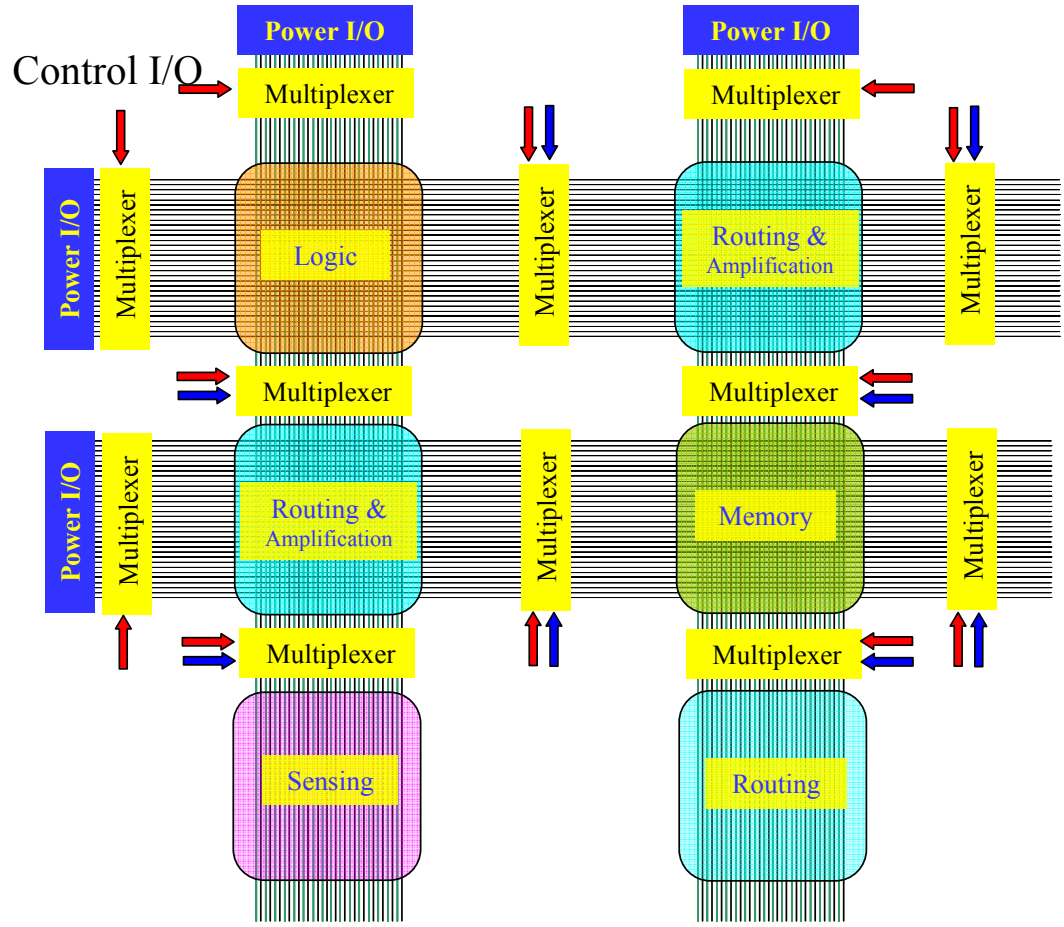

Figure 3-1. A nanoscale molecular computational platform. Tranditional computing functions are coupled to non-traditional elements, including sensors, actuator, etc., and are illustrated as individual tiles in a mosaic-like architecture. Muliplexers and demultiplexers control communication between various functions and provide the user interfaces. Copyright 2006 Royal Society of Chemistry.

As presented in figure 3-1, the proposed computing platform is based on the crossbar architecture. The crossbar geometry (12) provides a promising architecture for nanoelectronic circuitry (13-17). The crossbar is tolerant of manufacturing defects – a trait that becomes increasingly important as devices approach macromolecular

dimensions and non-traditional (and imperfect) fabrication methods are employed. For example, Teramac had nearly a quarter million hardware defects and yet could be configured into a robust computing machine (12). The crossbar is a periodic array of crossed wires, similar to a two-dimensional crystal, implying that non-traditional methods can be employed for its construction (18-20). Finally, the crossbar is the highest density, two-dimensional digital circuit for which every device can be independently addressed (12). This attribute enables the circuit to be fully tested for manufacturing defects and to be subsequently configured into a working circuit.

For these reasons, my research group has tried to utilize the crossbar architecture for memory circuits. The progress in this crossbar memory project has been made both in the switching molecules and in the contacting electrodes: more robust [2]rotaxanes with higher on/off ratios have been rationally designed and synthesized (21). At the same time, as an attempt to constitute a circuit with higher density, various electrode-patterning techniques have been developed and tested. In practice, the total number of bits fabricated within a single crossbar circuit increased from 16 to 64 (8) to 4,500 to 160,000 bits as the main electrode pattering techniques were improved from photo-lithography to electron-beam lithography (EBL) to recently developed nanowire array technique (11) (figure 3-2) , and as methods to increase the compatibility of our nanofabrication procedures with the molecular

switch components were improved. Notably, the resolution of the nanowire array (11) that has been developed by my research group is far beyond that of the conventional EBL. Hence, the memory circuits utilizing this nanowire array technique set a remarkable landmark in memory bit density. In this chapter, I will first describe the nanowire array technique, so called superlattice nanowire pattern transfer (SNAP) method, and then focus on fabrication and testing of 160 kbit crossbar memory circuits based on the SNAP technique and [2]rotaxanes.

The fabrication of the 160 kbit memory circuits at a bit density of 10^{11} bits/cm^2 was totally nontrivial. At this point, reviewing the history of molecular memory projects in my research group provides guidance for understanding our efforts toward device miniaturization, as well as understanding difficulties of the fabrication procedure. Until reaching this unexplored bit density, many scientists from several groups have contributed to different components of the circuits at each stage: In conjunction with Hewlett-Packard group, my research group initially proposed the concept of the defect-tolerant crossbar architecture. Since then, significant progresses in achieving the actual molecule-based devices were initiated by the former postdocs in my research group, Dr. Collier, Dr. Wong and Dr. Luo. They optimized conditions for many of the key fabrication steps, including monolayer deposition by the Langmuir-Blodgett technique and metal deposition to form the top electrical contact

to the molecules. They also established rational electrical measurement schemes such as the remnant molecular signature scan and the temperature-dependent volatility scan to test the switching and the activated nature of the molecular electronic switching mechanism. They also demonstrated relative robust molecular switches that could be cycled > 1,000 times. Dr. Luo developed next-generation fabrication procedures for the memory circuits based on the EBL-defined electrodes. He demonstrated that the molecular switching in EBL-defined circuits is still very robust, and he developed a number of procedures for the integration of Si SNAP nanowire bottom electrode arrays with EBL defined top electrodes. For my part, I was teamed up with another group member, Jonathan Green, to achieve the large-scale (160,000 bit) SNAP nanowire-based memory circuits at extreme density (10^{11} bitscm^{-2}).

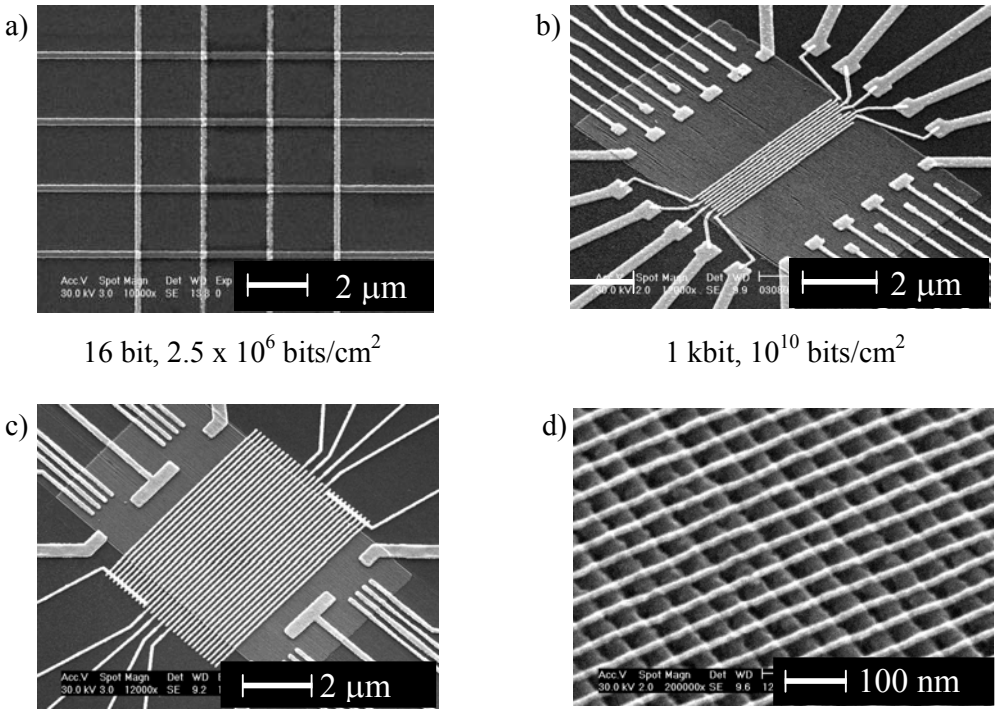

Figure 3-2. A series of crossbar molecular electronic memory circuits. These circuits are arranged a-d in accordance with the chronology of their fabrication. The total number of bits and the memory density of each memory circuit were denoted below scanning electron micrograph (SEM) pictures.

3.2 Superlattice Nanowire Pattern Transfer (SNAP) Method

As described in the previous subchapter, the scaling advantage of a [2]rotaxane molecular electronic switch would be best illustrated only when electrodes with molecular dimensions are integrated together to form the junction sandwiching the molecule. For this and other reasons, my research group has

developed unique nanowire array fabrication technique called superlattice nanowire pattern transfer (SNAP). For the SNAP method, the layer structure of a GaAl/$Al_xGa_{(1-x)}$As superlattice in which each layer is grown under atomic-level control, is translated into a variety of metals or silicon. The width and pitch of final nanowire array made of metals and/or silicon are defined by the initial superlattice film widths and spacings. With the SNAP method, my research group has demonstrated the fabrication of silicon nanowire arrays in which each wire is about 8 nm wide and at a pitch of about 16 nm. Also, nanowire arrays containing up to 1,400 nanowires have been demonstrated (figure 3-3). Moreover, in comparison to other nanowire growth methods, such as the vapor-liquid-solid growth method most fully developed in the Lieber group (22), the SNAP method has no limitation in length of the nanowires within arrays. A few millimeter long nanowire arrays are routinely produced.

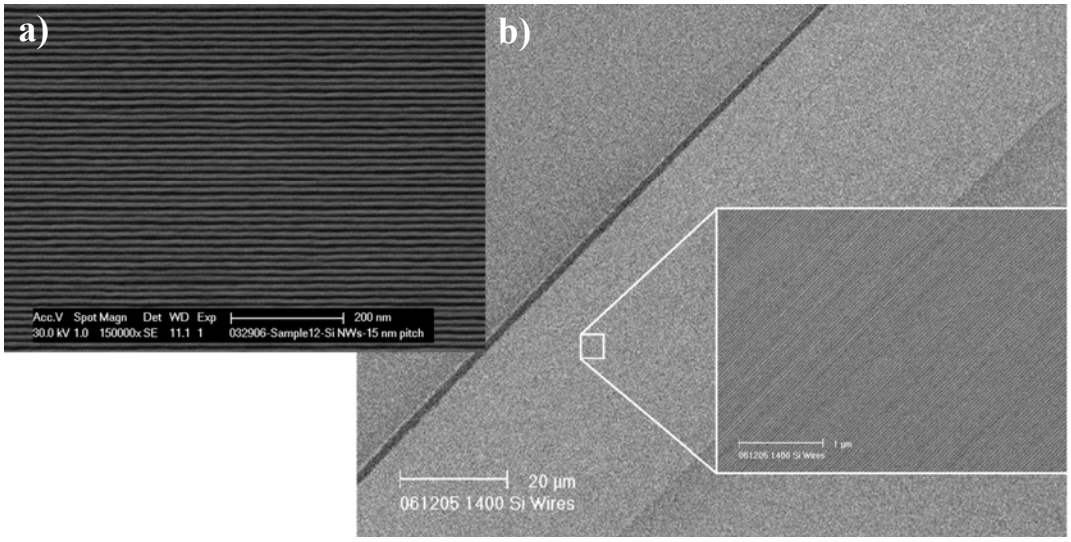

Figure 3-3. SEM images of Si nanowire arrays of (a) 15 nm pitch and (b) 1400 wires.

Here, I briefly go through the SNAP procedures (figure 3-4). More detailed procedures of the SNAP method are described in the thesis of Jonathan Green, who was also involved in the project as a leading member. First, a wafer containing the superlattice was diced into small pieces, which are referred to as masters. When turned on its side, a master is largely a GaAs wafer, with the top edge of the wafer containing the superlattice. When viewed from the edge, this superlattice structure is like a club sandwich, with alternating layers of GaAs and $Al_xGa_{(1-x)}As$ films substituting for the meat and bread layers in the sandwich. It is this superlattice edge that provides the initial template for the nanowires. This edge is first cleaned carefully in a class 1000 clean room using methanol and gentle swabbing, so that it is clean by eye when viewed under an optical microscope. Once the cross-section turns out to be

completely dust-free, a dilute mixture of buffered hydrofluoric acid (15 ml of 6:1 buffered oxide etchant, 50 ml of H_2O) is used to selectively etch the $Al_xGa_{(1-x)}As$, thus forming a comb-like structure as shown in figure 3-4b. Conversely, the GaAs could be selectively etched to form a complementary comb-like structure. Next, about 10 nm of Pt layer was deposited onto the superlattice side at about 45° tilted angle using electron beam evaporation of a Pt target. This angle could be varied to yield some control over the nanowire width. In preparing silicon substrates (using silicon-on-insulator wafers), the substrates were cleaned by rinsing with a series of solvents until the surface becomes completely dust-free. A mixture of epoxy and poly (methyl methacrylate) (PMMA) (10 drops of epoxy and 1 drop of curing agent, 0.18 g of 6 % (in weight) PMMA in chlorobenzene, additional 10 ml of chlorobenzene) was spincast onto prepared substrates at 8000 rpm. Pt deposited masters were dropped onto the epoxy coated substrates so that the superlattice side contacted and adhered to the epoxy layer. The epoxy was cured around 130 °C for half an hour or so. The substrates were then dipped into an etching solution for removing GaAs masters, but leaving behind the Pt nanowires, which were epoxy-adhered to the substrate. After ~ 4 hr of wet-etching, the GaAs masters were peeled off and the Pt nanowire array structure remained on the substrate. Once the quality of the Pt nanowire array was confirmed by SEM, the Pt pattern was transferred into the underlying silicon-on-

insulator substrate by reactive ion etching (RIE) (CF_4:He = 20:30 sccm, 5 mTorr, 40 W, ~ 4 min for 33 nm Si layer). Upon removing Pt by aqua resia ($HCl:HNO_3$ = 2:1 in volume), the Si nanowire array structure was complete.

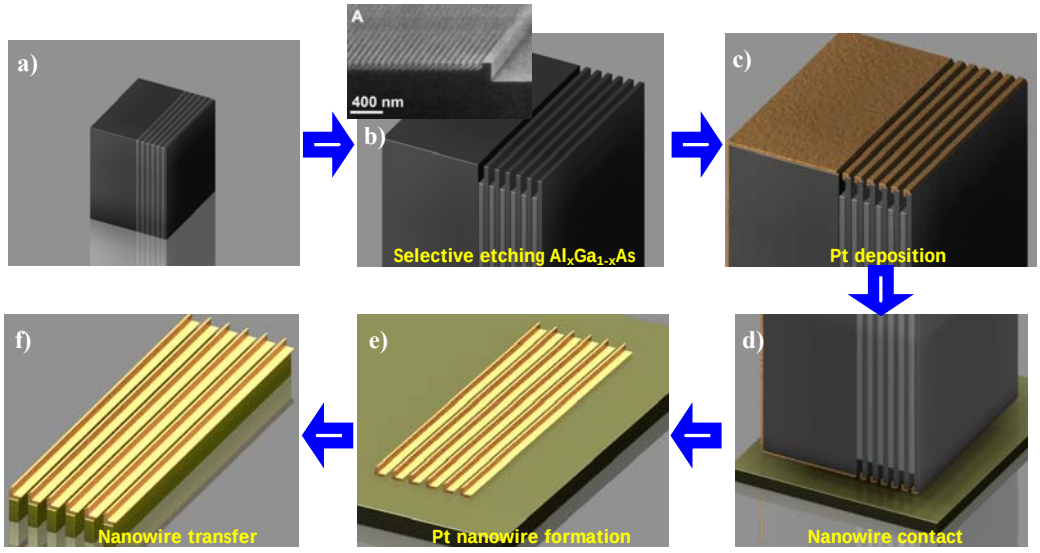

Figure 3-4. SNAP process flow. (a) The wafer containing the superlattice was diced into small pieces and the superlattice side was cleaned thoroughly. (b) $Al_xGa_{(1-x)}As$ was selectively wet-eched. (c) A Pt layer was deposited onto the superlattice side by electron beam evaporation. (d) Masters were dropped onto the epoxy coated substrates. (e) The superlattice was removed by a wet-etch, leaving the Pt nanowire-array structure on the substrates. (f) The Pt nanowire array structure was transferred to form an array of aligned and high aspect ratio silicon nanowires via RIE.

3.3 160 kbit Molecular Electronic Memory Circuits: Overview

The primary metric for gauging progress in the various semiconductor integrated circuit (IC) technologies is the spacing, or pitch, between the most closely spaced wires within a dynamic random access memory (DRAM) circuit (23). Modern DRAM circuits have 140 nanometer (nm) pitch wires and a memory cell size of 0.0408 square micrometers (μm^2). Improving IC technology will require that these dimensions decrease over time. However, by year 2013 a large fraction of the patterning and materials requirements for constructing IC technologies are currently classified as having 'no known solution' (23). Nanowires (24), molecular electronics (25), and defect tolerant architectures (12) have been identified as materials, devices, and concepts that might assist in continuing IC advances. This belief has largely been bolstered by single device (26-28) or small circuit demonstrations (20, 29). The science of extending such demonstrations to large scale, high density circuitry is largely undeveloped. In this and following sections, I describe a 160,000 bit molecular electronic memory circuit, fabricated at a density of 10^{11} bits/cm^2 (pitch = 33 nm; memory cell size = 0.0011 μm^2), which is roughly analogous to a projected year 2020 DRAM circuit. A monolayer of bistable, [2]rotaxane molecules (30) described in chapter 2 served as the data storage elements. Although the circuit had large numbers of defects, those defects could be readily identified through electronic

testing and isolated using software coding. The working bits were then configured to form a fully functional random access memory circuit for storing and retrieving information.

A few groups have reported on non-lithographic methods for fabricating crossbar circuits (18, 31), but most methods are not yet feasible for fabricating more than a handful of devices. Furthermore, the assembly of nanowires into narrow pitch crossbars without electrically shorting adjacent nanowires remains a challenge. Despite these challenges, my research group developed the SNAP method for producing ultra-dense, highly aligned arrays of high-aspect ratio metal or semiconductor NWs(11) containing up to 1400 NWs at a pitch as small as 15 nm (figure 3-3). The procedures for this SNAP method were described in the previous subchapter. For constituting ultra-dense memory circuits whose density is far beyond what is possible with current CMOS technology , I combined these patterning methods and extremely scalable [2]rotaxane switches, along with the defect-tolerance concepts learned from Teramac. I constructed and tested a memory circuit at extreme dimensions: the entire 160,000 bit crossbar is approximately the size of a white blood cell (~13×13 μm^2). At each cross-point of nanowire array, only several hundreds of [2]rotaxanes were incorporated.

3.4 160 kbit Molecular Electronic Memory Circuits: Fabrication Flow

A bottom-up approach was the key to the successful fabrication of this memory. This approach both minimized the number of processing steps following deposition of the molecular monolayer, as well as protected the molecules from remaining processing steps. In the following paragraphs, I describe the nanofabrication procedures utilized to construct the memory circuit.

Our 160,000 junction crossbar memory consists of 400 Si nanowire (NW) bottom electrodes of 16 nm width and 16.5 nm half-pitch, crossed with 400 Ti NW top electrodes of the same dimensions, and with a monolayer of bistable [2]rotaxane molecules sandwiched in between. My research group has previously reported on using the SNAP technique to fabricate highly ordered arrays of 150 metal and Si NWs (10). For this work, the SNAP technique was extended to create 400 element NW arrays of both the bottom and top electrode materials, and so was the primary patterning method for achieving the 10^{11} cm^{-2} bit density of the crossbar.

An overview of the process flow used to fabricate the memory is shown in figure 3-5.

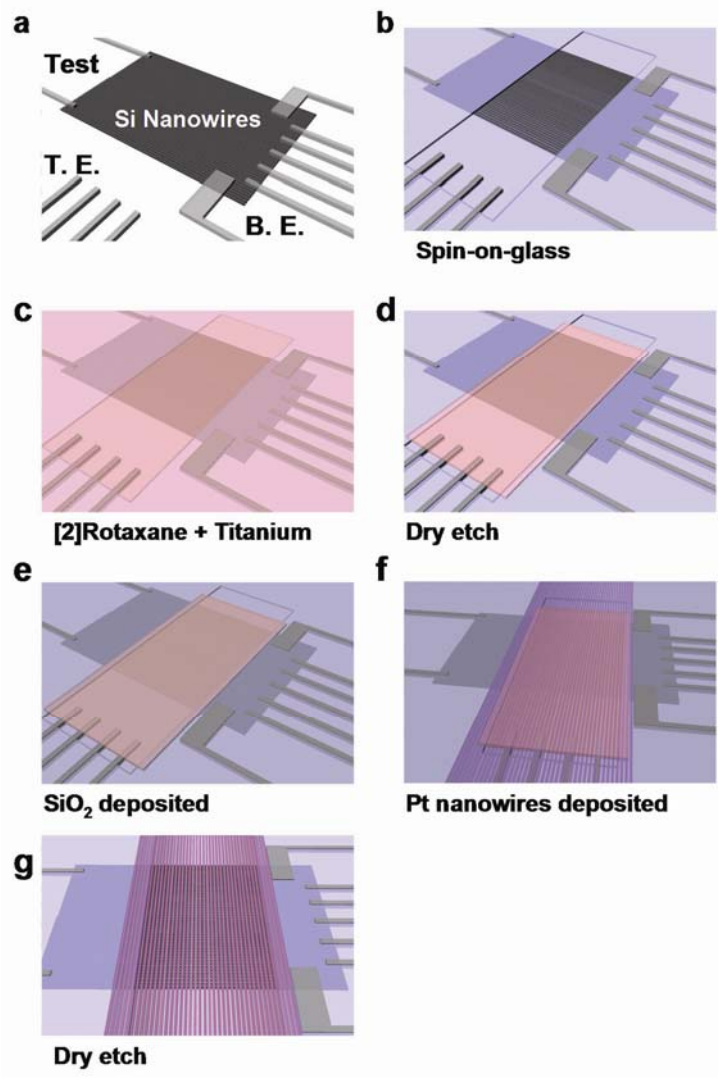

Figure 3-5. The process flow for preparing the 160 kbit molecular electronic memory circuit at 10^{11} bits/cm^2. (a) SNAP-patterned SiNW bottom electrodes are electrically contacted to metal electrodes. (b) The entire circuit is coated with SiO_2 (using spin-on-glass (SOG)) and the active memory region is exposed using lithographic patterning followed by dry etching. (c) The bistable [2] rotaxane Langmuir monolayer is deposited on top of the Si NWs and then protected via the deposition of a Ti layer. **(**d) The molecule/Ti layer is etched everywhere except for the active memory region. (e) A SiO_2 insulating layer is deposited on top of the Ti film. (f) An array of top Pt NWs is deposited at right angle to the bottom Si NWs using the SNAP method. (g) The Pt NW pattern is transferred, using dry etching, to the Ti layer to form an array of

top Ti NW electrodes, and the crossbar structure is complete.

Preparation of and contact to the bottom Si nanowire electrodes The Si NW array was fabricated as described previously (10, 11). The starting wafer for the Si NWs was a 33 nm thick phosphorous doped ($n=5x10^{19}$ cm^{-3}) silicon-on-insulator (SOI) substrate with a 250 nm thick buried oxide (Simgui, Shanghai, China). An array of Pt NWs was transferred onto this substrate using the SNAP method, and reactive ion etching was used to transfer the Pt NW pattern to form a ~2 millimeter long array of Si NWs. The Pt NWs were then removed, and the Si NW array was sectioned into a 30 μm long region. Electrical contacts to these bottom Si NWs, as well as contacts that are intended for the top Ti NWs were defined at this point using standard electron-beam lithography (EBL) patterning and electron-beam evaporation to produce electrodes consisting of a 15 nm Ti adhesion layer followed by a 50 nm thick Pt electrode (figure 3-5a). Immediately prior to metal evaporation, the Si NWs were cleaned using a gentle O_2 plasma (20 standard cubic centimeters per minute (sccm), 20 milliTorr, 10 Watts, 30 seconds) followed by a 5 second dip in an NH_4F/HF solution. After lift-off, the chip was annealed at 450 °C in N_2 for 5 min to promote the formation of ohmic contacts.

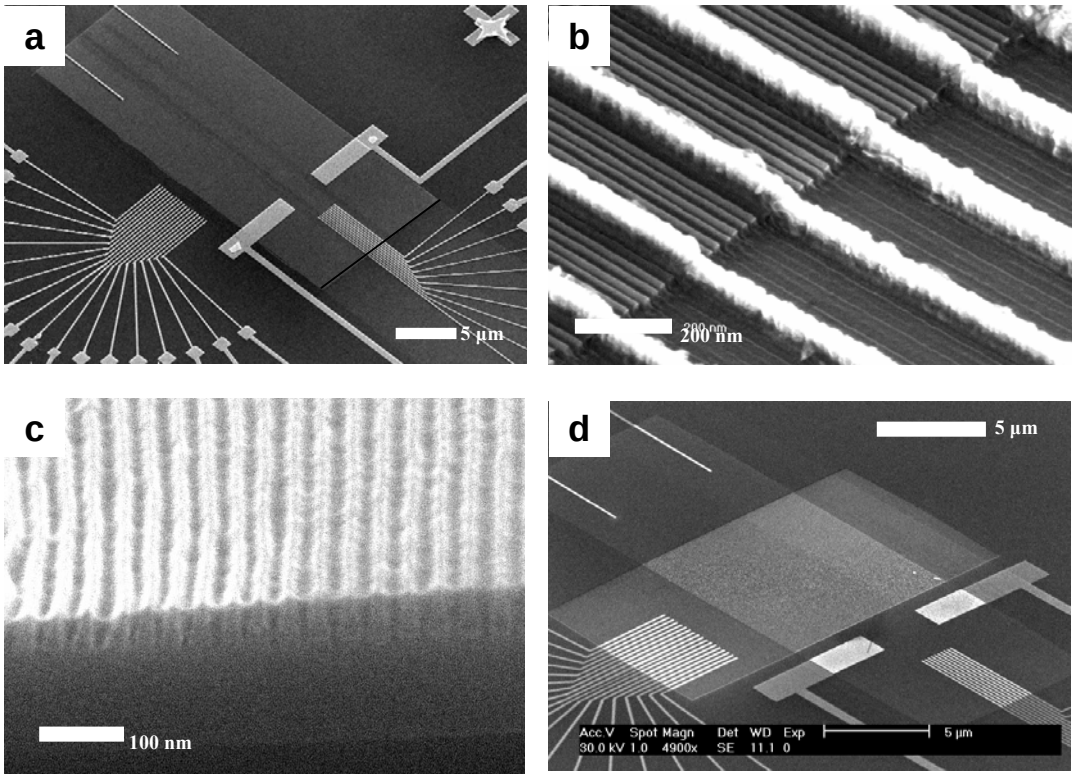

Figure 3-6. Scanning electron micrographs of the nanowire crossbar memory fabrication process. (a) A 30 micrometer long section of the SiNWs and its electrical contacts to metal leads were defined by electron-beam lithography (EBL). (b) Each electrode defined by EBL is about 70 nm wide contacting 2 ~ 4 NWs. This image illustrates that the intrinsic patterning of nanowire crossbar is beyond lithographic limits. (c) Progress-check of SOG window etching over the active memory region. This image verifies that SOG fills the gap of NWs and SEM is a valid tool for monitoring SOG etching. (d) SOG is etched by RIE over the active memory region. Detailed processes for monitoring this etching progress are described in the text.

Figure 3-6a shows an SEM image of the device at the stage in which the Si NWs and all of the external electrical contacts have been created. Note that there are four sets of EBL defined contacts. The 18 narrow contacts at the bottom left of the

image will eventually connect to the top Ti NW electrodes and are used for testing of the final memory circuit. The 10 narrow contacts to the Si NWs at the bottom right of the image are also used for testing of the memory circuit. Finally there are two narrow test electrodes at the top left and two wide electrodes at the bottom right. The wide electrodes contact about 2/3 of all the Si NWs and serve dual functions. First, they ground unused Si NWs during memory testing (this procedure approximates how a fully multiplexed crossbar circuit would be utilized). Second, when used in conjunction with the two narrow test-electrodes on the opposite side of Si NW array, they enable testing of the conductivity of the Si NWs throughout the fabrication processes. This testing procedure provided invaluable feedback for finely tuning and tracking many of the fabrication processes. Once these various contacts were established, robust Si NW conductivity was confirmed via current vs. voltage measurements. If the Si NWs were measured to be poor conductors (a very infrequent occurrence), the chip was discarded.

The device was then planarized using an optimized spin-on-glass (SOG) procedure (Accuglass 214, Honeywell Electronic Materials, Sunnyvale, CA). This planarization process was critical because the SOG not only protects Si NWs outside of the active memory region from damage that can arise during subsequent processing steps, but it also prevents evaporated Ti (explained below) from entering the gaps

between the Si NWs where it would be extremely difficult to remove (figure 3-6c). Due to the extremely narrow gap between the Si NWs, this SOG step was performed in a vacuum condition: For the first generation of the devices, the SOG was spin-coated at atmospheric pressure. However, the atmospheric spin-coating did not allow the gaps between the Si NWs to be filled completely with the SOG. The SOG penetrated only to the upper spacing of the trenches. For the complete filling, the process was done in a vacuum condition. The substrate containing the Si NWs was placed in a small glass container covered by a rubber stopper. A needle connected to a syringe and to a diffusion pump was plugged through the rubber stopper to employ a vacuum condition. During this vacuum process, the SOG was transferred to the container via another syringe. As soon as the SOG was sucked into the container by the vacuum and therefore the substrate was covered by the SOG, the substrate was taken out immediately for a spin-coating (~ 5000 rpm, 30 sec). Before starting the planarization steps described so far, all the glasswares including the container were cleaned very carefully because even a small dust particle could ruin the device. Especially, the top SNAP NWs process requires very clean and flat surfaces in a several millimeters range. In some cases, some dust particles appeared during the vacuum transfer despite the careful preparation. For that case, the SOG was stripped by methanol and then the substrates were cleaned intensively by spraying methanol

onto the substrates followed by blowing the dust particles off with nitrogen gas repeatedly. Upon confirming that the surface is completely dust-free, SOG was spin-coated again at an atmospheric condition. For this second SOG spin-coating, the vacuum condition was not necessary: As mentioned above, the trenches between Si NWs are not usually completely filled with the SOG if the substrate is spin-coated directly at atmospheric pressure. However, the second spin-coating performed at atmospheric pressure fills the trenches completely with the SOG, as indicated by figure 3-6c.

Next, SOG layer thinned down globally using a CF_4 plasma (20 standard cubic centimeters per minute (sccm), 10 milliTorr, 40 Watts). This etching was monitored periodically by ellipsometer and continued until the SOG layer became about 50 nm thick according to the ellipsometer. This final thickness is very critical because it affects the ensuing top SNAP and Ti layer dry-etching steps significantly. The detailed reasons are described in the paragraphs dedicated to those steps.

After globally thinning the SOG layer, an opening in photo resist was lithographically defined over the Si NWs and the tips of the 18 EBL defined contacts. The SOG was then further etched until the tops of the underlying Si NWs were exposed (Fig. 3-5b, 3-6c, d). This step was monitored by periodically measuring the Si NW conductivity using the test electrodes. The majority of the dopant atoms in the

Si NWs lie within the top 10 nm of the NWs (10, 32). This feature means it is very straightforward to etch back the SOG without thinning the Si NWs, since the conductivity of the NWs is very sensitive to their thickness. At this stage the entire memory circuit is under SOG (and thus electrically isolated from any further top processing) except for the lithographically defined opening over the Si NWs and the 18 contacts. This opening defines the active memory region.

Deposition of Molecules and Top Electrode Materials A monolayer of bistable [2]rotaxane switches (21) was prepared by Langmuir-Blodgett techniques and transferred onto the device as reported previously (8, 33). For the [2]rotaxane used herein, the Langmuir-monolayers were prepared on an aqueous (18 MΩ H_2O) subphase of Langmuir-Blodgett (LB) trough (Type 611D, Nima Technology, Coventry, UK). Before the trough was filled with the subphase, all the parts in the trough including compression barriers were cleaned very carefully by wiping with chloroform soaked wipes. Once the parts in the trough were wiped thoroughly, the filtered water was poured until the water level reached the compression barrier. From this point, the quality of the subphase was monitored by a brewster angle microscope (BAM). For further cleaning, the subphase was compressed to an area of about 50 cm^2 and then the surface of the subphase was sucked by a glass pipette connected to a pump to remove dust particles floating on the subphase surface. As the compression

and cleaning processes were repeated, the number of dust particles decreased and eventually, no dust particle was observed in the BAM image. Then, the barrier was moved back to the open position (~ 245 cm^2) and the prepared [2]rotaxane solution was dropped onto the subphase via a syringe. The [2]rotaxanes were prepared in a chloroform solution right before the transfer. After about 30 minutes of the chloroform evaporation, the barrier compression began at a rate of 5 cm^2/min. Once the surface pressure reached the target pressure (π = 30 mN/m), the surface pressure was fixed and the substrate started to be pulled out at a rate of 1 mm/min. When the entire substrate was pulled out of the subphase, the step for the preparation of the Langmuir-monolayer was complete.

20 nm of Ti was then evaporated over the entire device (figure 3-5c). This Ti layer serves to protect the molecules from further top processing. Using photolithographic techniques and BCl_3 plasma etching (10 sccm, 5 mTorr, 30 Watts), the molecule/Ti layer was then everywhere removed except for the memory active region where electrical contact to the underlying Si NWs is made (figure 3-5d). Next, a thin SiO_2 layer (~ 15 nm) was deposited over the entire substrate to isolate the EBL defined electrodes from the Pt NWs deposited in the next step (figure 3-5e). Remember that the SOG layer was about 50 nm thick after the SOG global etching

step as described in the previous paragraph so that the EBL defined electrodes as thick as 65 nm were exposed until the SiO_2 layer deposition.

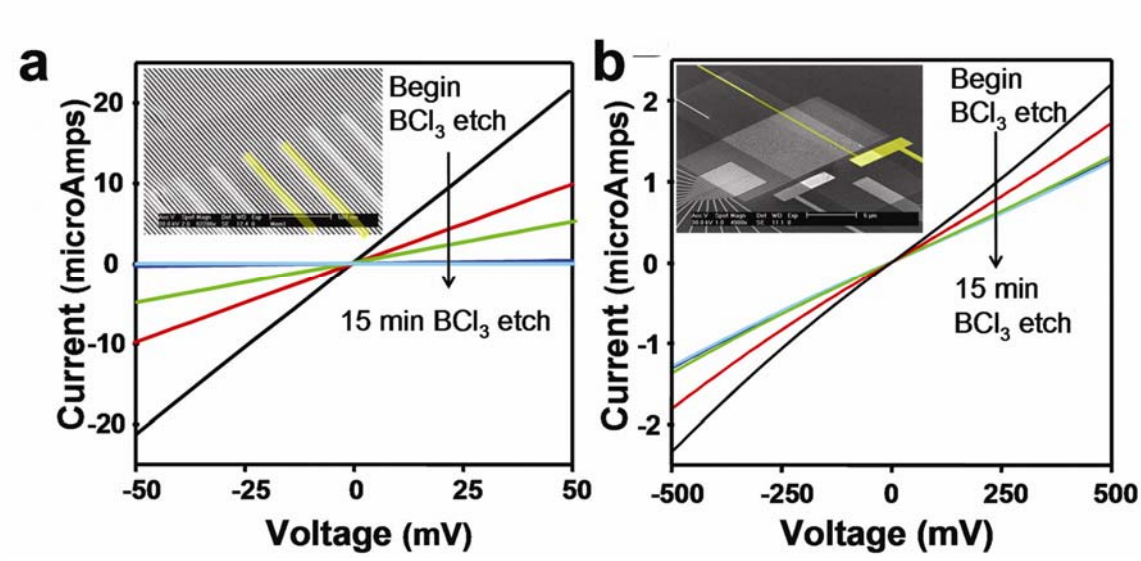

Figure 3-7. Conductance monitoring during the Ti layer etching. (a) Cross-conductance measurements between electrical contacts to the top nanowire array were performed to monitor the Ti layer etching. When the current drops to sub-10 nanoAmps, the top Ti electrodes are separated. The inset SEM image shows two representative contacts to the top Ti electrodes as highlighted in yellow. It is the cross-conductance between such contacts that was used for this measurement. (b) The conductivities of SiNWs were measured throughout the Ti layer etching to ensure that SiNWs were not damaged. The SEM image (inset) shows the current pathway that was measured.

Using the SNAP technique, an array of 400 Pt NWs was then deposited over the Ti/SiO_2 layer and perpendicular to the underlying Si NWs (figure 3-5f). For the

deposition of the Pt NWs, a different epoxy mixture (5 ml of THF, 5 drops of dibutylphthalate, 10 drops of epoxy and 1 drop of curing agent), compared to the one used for the Si NW generation, was used. A larger portion of epoxy in the new mixture enabled to hold the SNAP masters more firmly while the epoxy mixture was being cured on a hot plate and the GaAs masters were being wet-etched. Especially, the usage of the new epoxy mixture was essential for the deposition of the top SNAP nanowire array because the surface of the substrate became relatively rough throughout many previous steps. For the similar reason, the new mixture was less vulnerable to undercut in the following BCl_3 plasma etching step. The prevention of the undercut was most challenging task in the project because it could arise from many factors correlating one another (recess depth, strength of cured epoxy, directionality of plasma etching etc.). Finally, careful BCl_3 plasma etching (10 sccm, 5 mTorr, 30 W) was used to transfer the Pt NW pattern to the underlying SiO_2/Ti film, thus forming Ti NW top electrodes (figure 3-6 g). The global SOG etching down to ~ 50 nm thickness was also critical for this top SNAP nanowire pattern transfer. In the devices that maintained a thick SOG layer, thus a deep recess over the active memory region, the epoxy was trapped in the recess to form its thick layer. The thick layer of epoxy was susceptible to undercut during the BCl_3 plasma etching and thus to have shorting problems in the top SNAP nanowires. This shorting problem is very fatal in a

device performance because the yield of independent bits will decrease significantly. The etch endpoint was determined by monitoring the cross-conductance of the top Ti NWs (figure 3-7 a). Complete transfer of the Pt NW pattern to the underlying Ti film was indicated by a fall in the cross-conductance to about 10 nS. Note that the cross-conductance does not go to zero since the Ti electrodes, while physically separated, are still electrically coupled through the crossbar junctions and the underlying Si NWs. The health of the underlying Si NWs throughout the Ti-etching steps was also monitored as shown in figure 3-7b. In most cases, the devices that skipped the SOG planarization step lost the Si NW conductance completely before the cross-conductance fell down to a value corresponding to the complete NW pattern transfer, indicating that Si NWs were damaged significantly during the BCl_3 plasma etching. Once BCl_3 plasma etching is done, the device is ready for testing. SEM images for final devices are presented in figure 3-8 at different resolution.

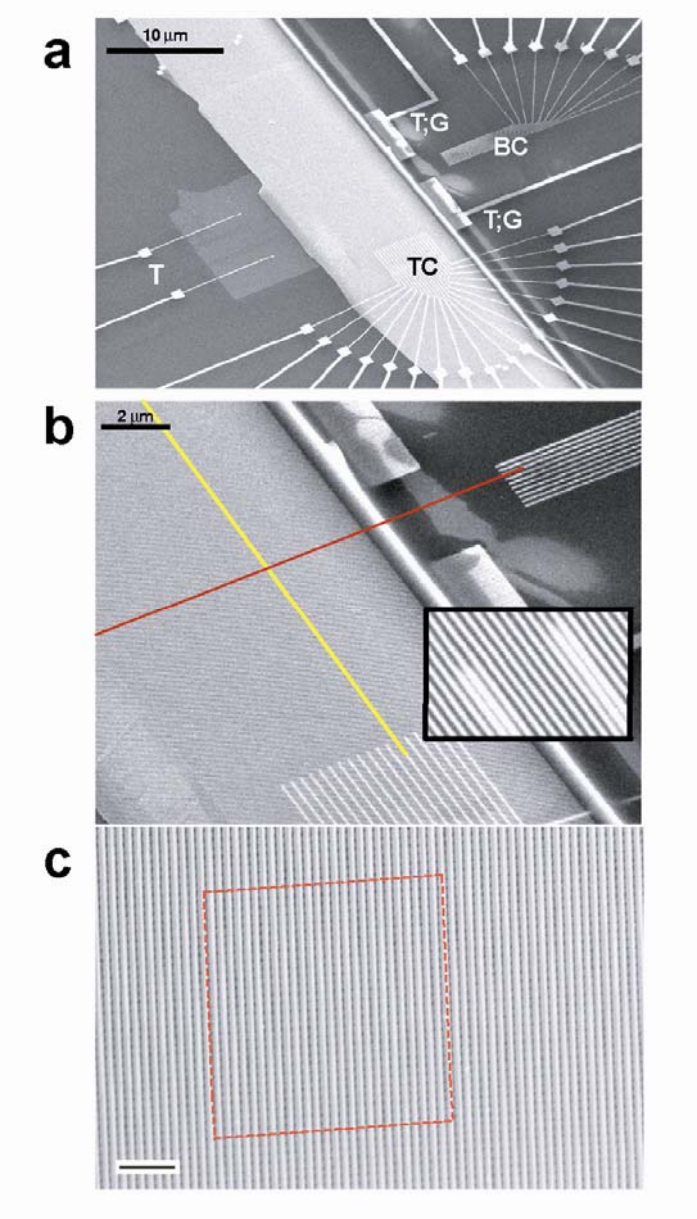

Figure 3-8. Scanning electron micrographs (SEMs) of the NW crossbar memory. (a) Image of the entire circuit. The array of 400 bottom Si NWs is seen as the light grey rectangular patch extending diagonally up from bottom left. The top array of 400 Ti NWs is covered by the SNAP template of 400 Pt NWs, and extends diagonally down from top left. Testing contacts (T) are for monitoring the electrical properties of the Si NWs during the fabrication steps. Two of those contacts are also grounding contacts (G), and are used for grounding most of the Si NWs during the memory evaluation,

writing, and reading steps. Electron beam lithography patterned 18 top (TC) and 10 bottom (BC) contacts are also visible. The scale bar is 10 micrometers. (b) An SEM image showing the cross-point of top and bottom NW electrodes. Each cross point corresponds to an ebit in memory testing. (inset) The electron-beam-lithography defined contacts bridged 2-4 nanowires each. The scale bar is 2 micrometers. (c) High resolution SEM of approximately 2500 junctions out of a 160,000 junction nanowire crossbar circuit. The red square highlights an area of the memory that is equivalent to the number of bits that were tested. The scale bar is 200 nanometers.

3.5 160 kbit Molecular Electronic Memory Circuits: Device Testing

The memory circuit was tested using a custom-built probe card and a Keithley 707A switching matrix for off-chip demultiplexing. Because SNAP NWs are patterned beyond the resolution of lithographic methods (34), each test electrode contacted between 2 and 4 NWs so that individual effective bit (ebit) contains between 4 and 16 crossbar junctions, but mostly 9 crossbar junctions. All ebits were electrically addressed within the 2D crosspoint array by the intersection of one Si NW bottom electrode and one Ti NW top electrode. Individual molecular junctions were set to their low resistance or “1” state through the application of a positive 1.5 – 2.3 V pulse (voltages are referenced to the bottom Si NW electrode) of 0.2 s duration. A junction was set to its “0” or high resistance state through application of a -1.5 V pulse, also of 0.2 s duration. To avoid switching an entire column or row of bits, the

switching voltage was split between the two electrodes defining the ebit. Thus, to write a “1” with +2 V, a single Si NW electrode is charged to +1 V, while a single Ti NW electrode is set to -1V, and only where they cross does the junction feel the full +2 V switching voltage. Half-selected bits, that is, bits receiving only half the switching voltage, were never observed to switch. This half-select issue, though being a clear drawback of crossbar architecture, is overcome by distinctive characteristic of [2]rotaxane: As introduced in the subchapter 3-1, the voltages required to switch on/off MSTJs were uniform over broad junctions such that a half of the voltage did not perturb the junctions. Individual ebits were read by applying a small, non-perturbing +0.2 V bias to the bottom Si NW electrode and grounding the top Ti NW electrode through a Stanford Research Systems SR-570 current pre-amplifier. Bits not being read were held at ground to reduce parasitic current through the crossbar array. Note that all the electrical writing and reading operations described herein were done sequentially. Schematic illustrations describing the device testing procedures composed of writing and reading bits are presented in figure 3-9. A LabWindow code used for the entire measurement procedures is also attached in Appendix B.

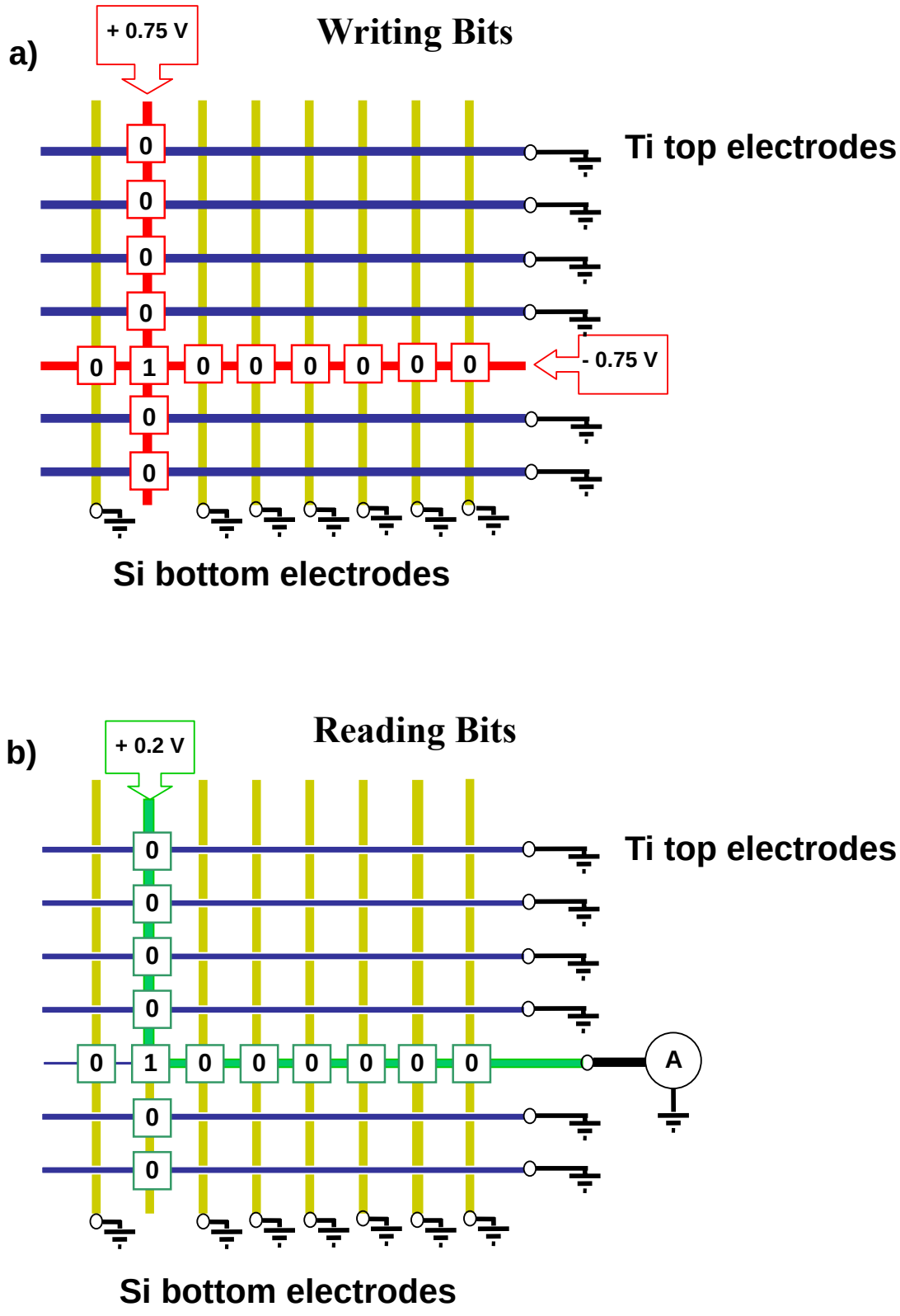

Figure 3-9. Writing and reading procedures in crossbar memory measurements. (a) Due to the half select issue, the writing bias was split into two halves of opposite

polarity and each half was applied to both top and bottom electrodes, respectively, defining a designated cross-point. Other bits along these top and bottom electrodes are not perturbed due to the sharp switch-on/off bias characteristic of [2]rotaxanes. (b) Before and after applying the writing voltages, the resistances of all bits are read at small non-perturbing reading bias to monitor the resistance change. Note that all other electrodes not involved in the switching of the designated cross junction stay grounded to minimize the parasitic current pathways.

By scanning electron microscopy inspection, the crossbar appeared to be structurally defect-free, with no evidence of broken, wandering, or electrically shorted NWs. Nevertheless, electrical testing identified a large number of defective bits and the nature of those defects. This testing was done by first applying a +1.5 V pulse relative to the Si NW bottom electrodes to set all bits to ‘1’, and then reading each ebit sequentially using a non-perturbing +0.2 V bias. A -1.5 V pulse was then applied to set all bits to ‘0’. The status of each of the ebits was again read. The raw data throughout these procedures and the 1/0 current ratios are presented in figure 3-10.

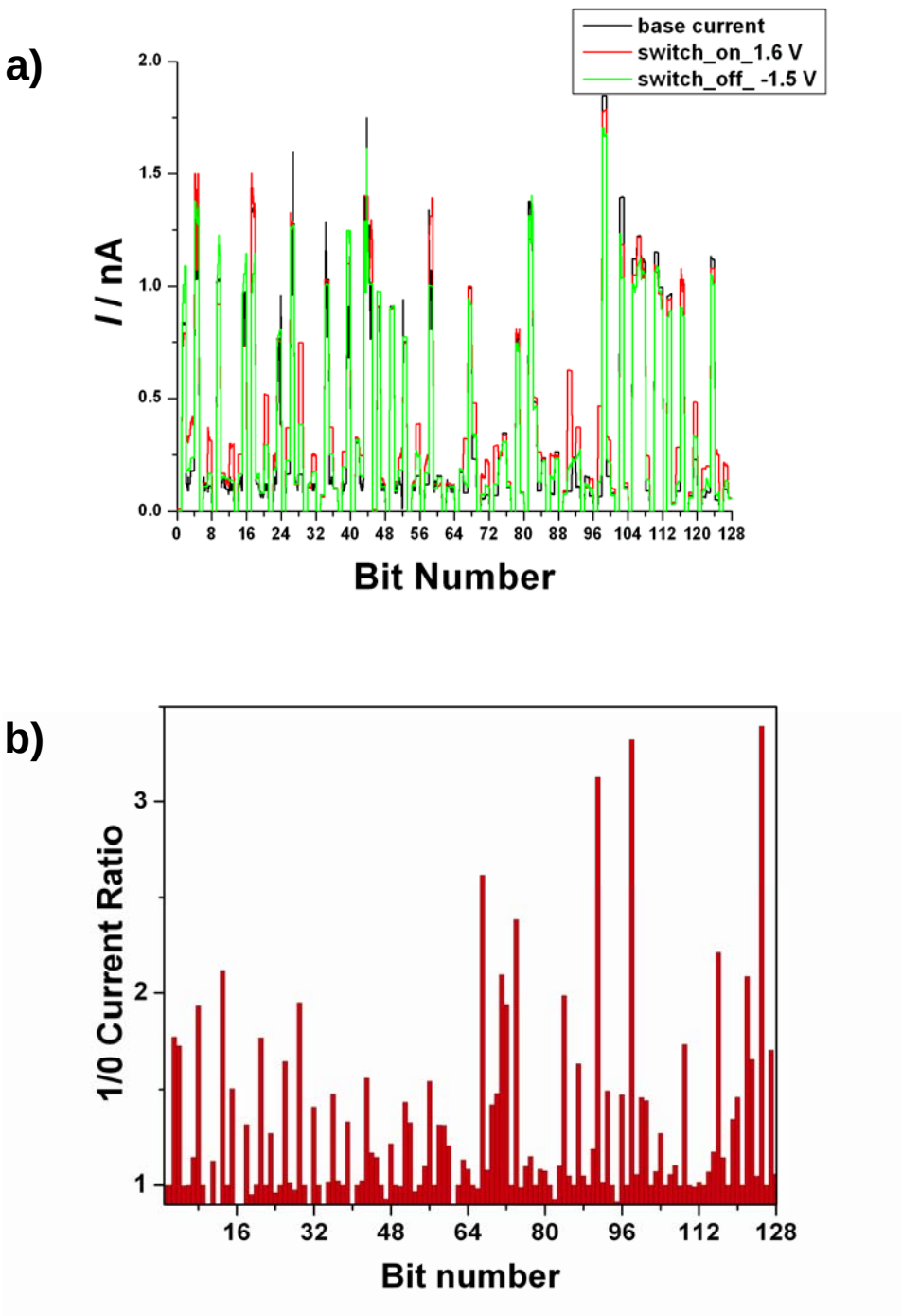

Figure 3-10. Data from evaluating the performance of the 128 ebits within the crossbar memory circuit. (a) raw current data when monitored at +0.2 V at the stage of before-switch on, after-switch-on and after-switch-off. (b) The current ratio of the

‘1’ state divided by the ‘0’ state of the tested ebits. Note that many of the ebits exhibit little to no switching response. Those ebits are defective.

About 50% of the bits yielded some sort of switching response. Some of that response, however, may have originated from parasitic current pathways through the crossbar array. This is an inherent drawback of crossbar architectures wherein each junction is electrically connected to every other junction. The standard remedy is to incorporate diodes at each crosspoint (35), and although the molecule/Ti interface yields some rectification (36), we additionally grounded all NW electrodes not being used during a read or write step. By the way, the amount of rectification is dependent upon the amount of titanium oxidation that occurs at the molecule/Ti interface which, in turn, depends upon the vacuum level of the metal deposition system. For the devices reported here, the Ti was deposited at a pressure of approximately 5e-7 Torr. For isolated devices, but constructed in a fashion similar to what was done here, this typically produces a rectification of about 10:1 at 1 V. We established a threshold for a ‘good’ bit based upon a minimum 1/0 current ratio of ~1.5. About 25% of the ebits passed this threshold.

Electrical testing revealed several types of defects (figure 3-11). Bad ebits fell into a few classes, with the two most common groups being ebits that were either poor

switches with little or no switching response or open circuits. Adjacent, shorted Ti top electrodes were identified when the ebits addressed by those electrodes were not independently addressable. Even though that type of defect is not completely fatal (i.e. two rows of fabricated ebits could still be utilized as a single row), we did not use ebits associated with shorted top electrode defects. The defects classified as 'switch defects' likely arose from sub-nanometer variations in the reactive ion etching process that was employed to define the top Ti crossbar NWs. Isolated devices, or crossbar memories patterned at substantially lower densities and with larger wires, can typically be prepared with a nearly 100% yield. The switch defects led to only a proportional loss in the yield of functional bits, while bad contacts or shorted nanowires removed an entire row of bits from operation. An important result from the defect map (figure 3-11) is that the good and bad bits are randomly dispersed, implying that the crossbar junctions are operationally independent of one another.

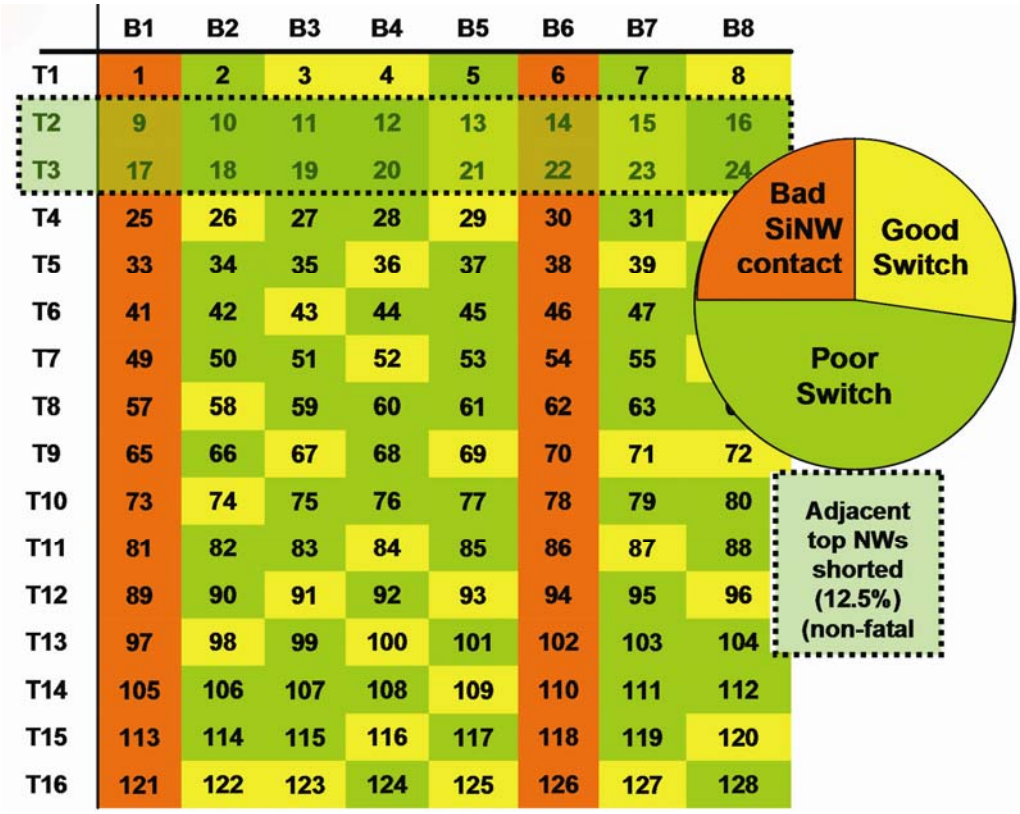

Figure 3-11. A map of the defective and useable ebits, along with a pie-chart giving the testing statistics. Note that, except for the bad Si NW contacts on bottom electrodes B1 and B6, and the shorted top electrodes T2 and T3, the defective and good bits are randomly distributed. Type I defects (26% of the 128 tested) are ebits that exhibited an open-circuit conductance and a low or zero amplitude switching response when tested. Type II defects (22%) are non-switchable bits that exhibited a conductance similar to that of a closed bit.

However, the ultimate test of any memory is whether it can be used to store and retrieve information. Based upon the defect map, we identified the addresses of the usable ebits, and from those addresses configured an operational memory (figure 3-12): the usuable bits were used to store and read out small strings of information

written in standard ASCII code. The maximum number of ebits that could be tested was 180, but our electronics were configured to test 128 ebits (< 1% of the actual crossbar), and that was sufficient to demonstrate the key concepts of this memory.

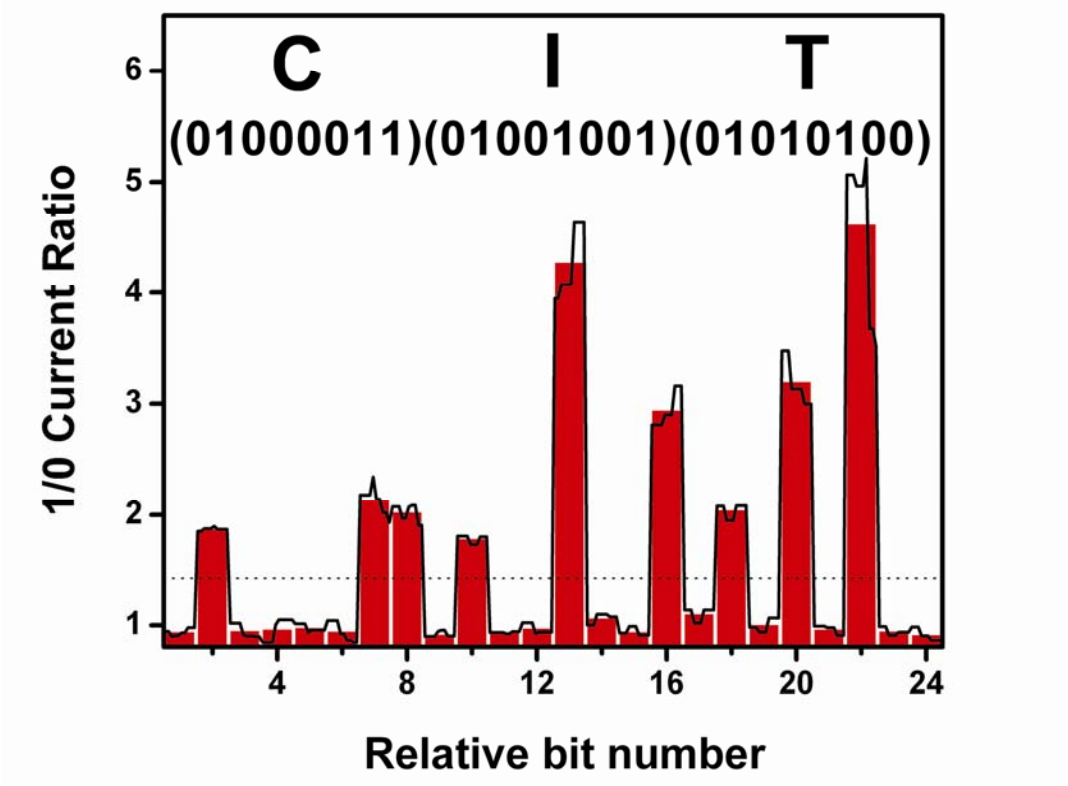

Figure 3-12. A demonstration of point-addressability within the crossbar. Good ebits were selected from the defect mapping of the tested portion of the crossbar. A string of '0's and '1's corresponding to ASCII characters for 'CIT' (abbreviation for California Institute of Technology) were stored and read out sequentially. The dotted line indicates the separation between a '0' and '1' state of the individual ebits. The black trace is raw data showing ten sequential readings of each bit while the red bars represent the average of those ten readings. Note that deviations of individual readings from their average are well separated from the threshold 1/0 line.

The solid-state switching signature of the bistable [2]rotaxanes that were used here has been shown to originate from electrochemically addressable, molecular mechanical switching for certain device structures (8, 30), but not for metal wire / molecule/metal wire junctions (37). In fact, our desire to utilize molecular mechanical bistable switches as the storage elements is what dictated our choice of the silicon NW / molecule / Ti NW crossbar structure. This switching signature should be effectively size-invariant, meaning that it should scale to the macromolecular dimensions of these crossbar junctions. Solid-state-based switching materials (1, 2) will likely not exhibit similar scaling since they arise from inherently bulk properties. The thermodynamic and kinetic parameters describing both the bistability and switching mechanism of the [2]rotaxane switch (and similar molecular mechanical switches (38)) have been quantified in a variety of environments(30), as described in chapter 2. Those measurements required robust switching devices that could be cycled many times and at various temperatures. The memory bits measured here were much more delicate – while all good ebits could be cycled multiple times (as evidenced by the testing and writing steps), most ebits failed after a half-dozen or so cycles, and none lasted longer than ten cycles. However, we measured the rate of relaxation from the 1→0 state for many of the ebits (figure 3-13). From a device perspective, this represents the volatility, or memory retention time, of the bits. With respect to the

bistable [2]rotaxane switching cycle, this represents a measurement of the rate limiting kinetic step within the switching cycle (30). Our measured rate (90±40 minutes; median decay = 75 minutes) was statistically equivalent to that reported for much larger (and more fully characterized) devices (58±5 minutes) (30). Thus, our results are consistent with a molecular mechanism for the switching operation (8, 30). The volatility measurements were carried out by switching selected bits to the "1" or low resistance state, and then reading the current through those bits as a function of time.

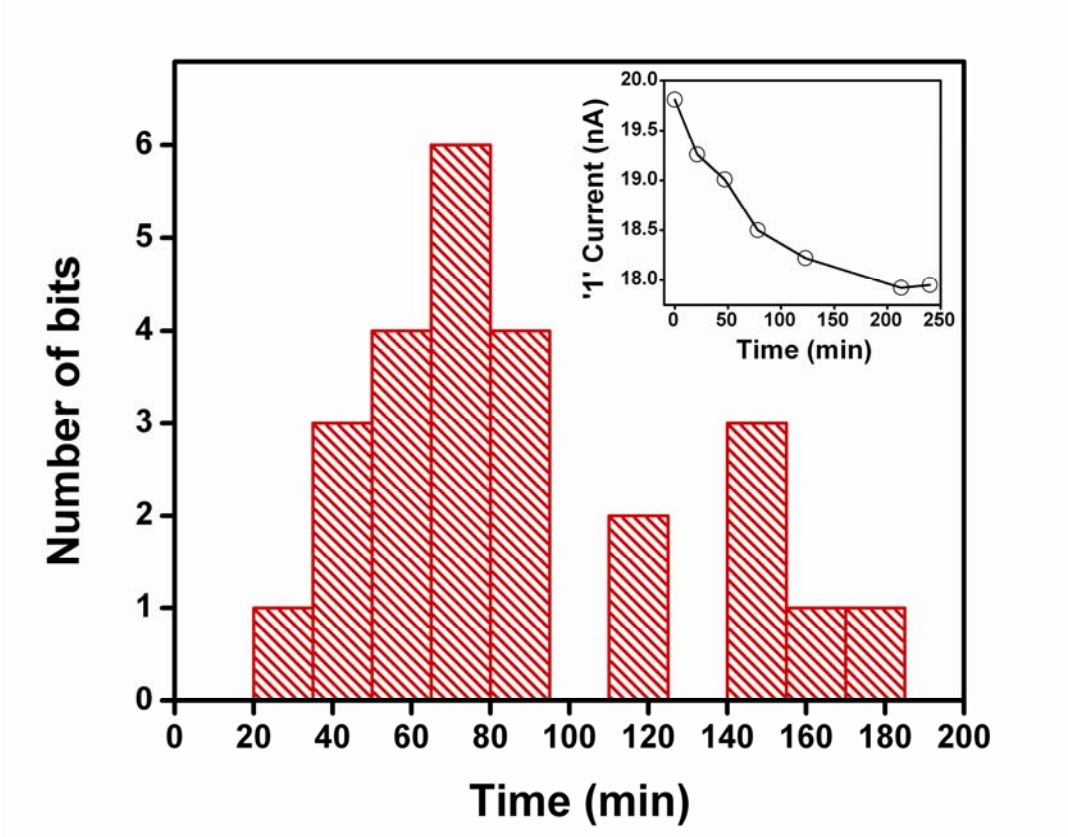

Figure 3-13. A histogram representing the 1/e decay time of the '1' state to the '0' state. The 25 ebits represented in the data were each 'large' ebits, comprised of approximately 100 junctions, to increase the measurement signal to noise. Raw data from a single large ebit is shown in the inset.

3.6 Limitations of the SNAP Process for Crossbar Memory Formation

The nanofabrication methods described in this chapter for creating the 160 kilobit crossbar memory circuit can be significantly extended in terms of both memory size and bit density. For our memories, the crossbar electrode materials choices have proven to be very important for successful memory operation. In other words, Si bottom electrodes and metallic top electrodes with a Ti adhesion layer were keys. Metal NWs at 8 nm half-pitch have been reported previously (11). Such NWs, formed by the SNAP process, only serve as templates for forming the crossbar electrodes. To be used in a crossbar memory, the SNAP NW pattern must be transferred to Si or Ti NWs for the bottom and top electrodes, respectively. Thus, it is not just the SNAP process, but the ability to translate the initially deposited SNAP NWs to form other NWs that ultimately limits the size and density of the circuitry that can be fabricated. In figure 3-3a, I present an array of 7 nm wide, 15 nm tall single crystal Si NWs patterned at 6.5 nm half-pitch. This corresponds to a crossbar that

would contain approximately 6×10^{11} bits cm^{-2}. While this array may not represent the density limit of what could be achieved, densities in excess of 10^{12} cm^{-2} will be very hard to obtain using these patterning methods.

Similarly, the 160,000 junction crossbar also doesn't represent any sort of limitation. In figure 3-3b, we present SEM images of 1400 Si NWs formed using the SNAP method. Such an array size permits the formation of a 2 million bit crossbar, and it is certainly possible to further expand the concept to substantially larger structures. As mentioned in the subchapter 3-2, the primary limitation is that the SNAP process is that, while it is a parallel patterning method – since all nanowires within an array are created simultaneously, each array must be fabricated one at a time using a labor intensive process. A single worker, for example, can fabricate only about 20 arrays of Si NWs in a single day. However, recent advances in using nanoimprinting (39) to replicate SNAP nanowires and to form crossbar structures indicate that high-throughput, parallel fabrication methods can be developed, even at the near molecular-densities described in this chapter.

3.7 Conclusion

This chapter focuses on molecular electronic memory circuits. The various generations of memory devices described in this chapter hold such common features

that the devices are based on the crossbar circuit and utilize [2]rotaxanes as information storage components. Through many generations, however, total number of bits within a single crossbar circuit and a bit density increased significantly. This scaling was possible due to the development of the fabrication procedures that allowed the integration of more delicate and higher density of electrodes with the [2]rotaxane molecular monolayer. Despite more complicated fabrication procedures, the devices containing higher bit densities still showed the molecular switching signature. Especially, the final generation devices fabricated based upon the ultra-dense SNAP nanowire arrays also retained the molecular switching signature and exhibited a point addressability within a crossbar circuitry. Although about 75 % of the tested bits in the SNAP nanowire-based device turned out to be defective, the functional part was identified through an electrical testing and configured to write and read specific information. Notably, due to the extremely small pitch (~ 33 nm) of the SNAP nanowire array, the resultant 160 kbit crossbar memory circuits set a remarkable record in a bit density (10^{11} bits/cm^2).

Many scientific and engineering challenges, including device robustness, improved etching tools, and improved switching speed, remain to be addressed before this ultra-dense crossbar memory described here can be practical. Nevertheless, this 160,000 bit molecular memory does provide evidence that at least some of the most

challenging scientific issues associated with integrating nanowires, molecular materials, and defect tolerant circuit architectures at extreme dimensions are solvable. While it is unlikely that these digital circuits will scale to a density that is only limited by the size of the molecular switches, it should be possible to significantly increase the bit density over what is described here. Recent nanoimprinting results suggest that high-throughput manufacturing of these types of circuits may be possible (39). Finally, these results provide a compelling demonstration of many of the nanotechnology concepts that were introduced by the Teramac supercomputer several years ago, albeit using a circuit that contained a significantly higher fraction of defective components relative to the Teramac machine (12).

3.8 References

1. Waser, R. & Rudiger, A. (2004) *Nat. Mater.* 3, 81-82.

2. Allwood, D. A., Xiong, G., Faulkner, C. C., Atkinson, D., Petit, D. & Cowburn, R. P. (2005) *Science* 309, 1688-1692.

3. Flood, A. H., Peters, A. J., Vignon, S. A., Steuerman, D. W., Tseng, H. R., Kang, S., Heath, J. R. & Stoddart, J. F. (2004) *Chem. Eur. J.* 10, 6558-6564.

4. Steuerman, D. W., Tseng, H. R., Peters, A. J., Flood, A. H., Jeppesen, J. O., Nielsen, K. A., Stoddart, J. F. & Heath, J. R. (2004) *Angew. Chem. Int. Ed.* 43,

6486-91.

5. Tseng, H. R., Wu, D., Fang, N. X., Zhang, X. & Stoddart, J. F. (2005) *Chemphyschem* 5, 111-6.

6. Deng, W. Q., Muller, R. P. & Goddard, W. A. (2004) *J. Am. Chem. Soc.* 126, 13562-13563.

7. Kim, Y. H., Jang, S. S., Jang, Y. H. & Goddard, W. A. (2005) *Phys. Rev. Lett.* 94.

8. Luo, Y., Collier, C. P., Jeppesen, J. O., Nielsen, K. A., Delonno, E., Ho, G., Perkins, J., Tseng, H. R., Yamamoto, T., Stoddart, J. F. & Heath, J. R. (2002) *Chemphyschem* 3, 519-525.

9. Beckman, R., Johnston-Halperin, E., Luo, Y., Green, J. E. & Heath, J. R. (2005) *Science* 310, 465-468.

10. Beckman, R. A., Johnston-Halperin, E., Melosh, N. A., Luo, Y., Green, J. E. & Heath, J. R. (2004) *J. Appl. Phys.* 96, 5921-5923.

11. Melosh, N. A., Boukai, A., Diana, F., Gerardot, B., Badolato, A., Petroff, P. M. & Heath, J. R. (2003) *Science* 300, 112-115.

12. Heath, J. R., Kuekes, P. J., Snider, G. S. & Williams, R. S. (1998) *Science* 280, 1716-1721.

13. DeHon, A., Goldstein, S. C., Kuekes, P. J. & Lincoln, P. (2005) *IEEE Trans.*

Nanotechnol. 4, 215-228.

14. DeHon, A. & Naeimi, H. (2005) *IEEE Des. Test Comput.* 22, 306-315.

15. Lee, M. H., Kim, Y. K. & Choi, Y. H. (2004) *IEEE Trans. Nanotechnol.* 3, 152-157.

16. Snider, G., Kuekes, P., Hogg, T. & Williams, R. S. (2005) *Appl. Phys. A* 80, 1183-1195.

17. Stan, M. R., Franzon, P. D., Goldstein, S. C., Lach, J. C. & Ziegler, M. M. (2003) *Proc. IEEE* 91, 1940-1957.

18. Diehl, M., Beckman, R., Yaliraki, S., and Heath, J. R. (2002) *Angew. Chem. Int. Ed.* 41, 353-356.

19. Wu, W., Jung, G. Y., Olynick, D. L., Straznicky, J., Li, Z., Li, X., Ohlberg, D. A. A., Chen, Y., Wang, S. Y., Liddle, J. A., Tong, W. M. & Williams, R. S. (2005) *Appl. Phys. A-Mater. Sci. Process.* 80, 1173-1178.

20. Zhong, Z. H., Wang, D. L., Cui, Y., Bockrath, M. W. & Lieber, C. M. (2003) *Science* 302, 1377-1379.

21. Tseng, H. R., Vignon, S. A., Celestre, P. C., Perkins, J., Jeppesen, J. O., Di Fabio, A., Ballardini, R., Gandolfi, M. T., Venturi, M., Balzani, V. & Stoddart, J. F. (2004) *Chem. Eur. J.* 10, 155-172.

22. Duan, X. F. & Lieber, C. M. (2000) *Adv. Mat.* 12, 298-302.

23. Fan, R., Yue, M., Karnik, R., Majumdar, A. & Yang, P. D. (2005) *Phys. Rev. Lett.* 95.

24. Yang, P. & Kim, F. (2002) *Chemphyschem* 3, 503-6.

25. Heath, J. R. & Ratner, M. A. (2003) *Physics Today* 56, 43-49.

26. Pop, E., Mann, D., Cao, J., Wang, Q., Goodson, K. & Dai, H. (2005) *Phys. Rev. Lett.* 95, 155505.

27. Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H. & Lieber, C. M. (2006) *Nature* 441, 489-93.

28. Zhou, X., Park, J. Y., Huang, S., Liu, J. & McEuen, P. L. (2005) *Phys. Rev. Lett.* 95, 146805.

29. Chen, Z., Appenzeller, J., Lin, Y. M., Sippel-Oakley, J., Rinzler, A. G., Tang, J., Wind, S. J., Solomon, P. M. & Avouris, P. (2006) *Science* 311, 1735.

30. Choi, J. W., Flood, A. H., Steuerman, D. W., Nygaard, S., Braunschweig, A. B., Moonen, N. N. P., Laursen, B. W., Luo, Y., DeIonno, E., Peters, A. J., Jeppesen, J. O., Xu, K., Stoddart, J. F. & Heath, J. R. (2006) *Chem. Eur. J.* 12, 261-279.

31. Huang, Y., Duan, X. F., Wei, Q. Q. & Lieber, C. M. (2001) *Science* 291, 630-633.

32. Wang, D., Sheriff, B. A. & Heath, J. R. (2006) *Nano Lett.* 6, 1096-100.

33. DeIonno, E., Tseng, H. R., Harvey, D. D., Stoddart, J. F. & Heath, J. R. (2006)

J. Phys. Chem. B 110, 7609-12.

34. Vieu, C., Carcenac, F., Pepin, A., Chen, Y., Mejias, M., Lebib, A., Manin-Ferlazzo, L., Couraud, L., Launois, H. (2000) *Appl. Surf. Sci.* 164, 111-117

35. Parkin, S. S. P., Roche, K. P., Samant, M. G., Rice, P. M., Beyers, R. B., Scheuerlein, R. E., O'Sullivan, E. J., Brown, S. L., Bucchigano, J., Abraham, D. W., Lu, Y., Rooks, M., Trouilloud, P. L., Wanner, R. A. & Gallagher, W. J. (1999) *J. Appl. Phys.* 85, 5828-5833.

36. McCreery, R. L. (2004) *Chem. Mater.* 16, 4477-4496

37. Chen, Y., Jung, G. Y., Ohlberg, D. A. A., Li, X. M., Stewart, D. R., Jeppesen, J. O., Nielsen, K. A., Stoddart, J. F., Williams, R. S. (2003) *Nanotechnology* 14, 462-468

38. Katz, E., Baron, R., Willner, I., Richke, N. & Levine, R. D. (2005) *Chemphyschem* 6, 2179-2189.

39. Jung, G. Y., Johnston-Halperin, E., Wu, W., Yu, Z. N., Wang, S. Y., Tong, W. M., Li, Z. Y., Green, J. E., Sheriff, B. A., Boukai, A., Bunimovich, Y., Heath, J. R. & Williams, R. S. (2006) *Nano Lett.* 6, 351-354.