Chapter 5

Silicon Nanowires as Highly Efficient Thermoelectric Materials

5.1 Introduction

Thermoelectrics is an old field, which is now experiencing a tremendous acceleration due to the development of new nanomaterials.[1-6] The principle of the field of thermoelectrics rests on two effects, discovered in the nineteenth century, which describe the conversion between thermal and electrical gradients in materials.[7, 8] In the Seebeck effect, the temperature difference across a material creates a voltage difference between the cold and hot ends due to the diffusion of thermally excited charged carriers down the temperature gradient. This effect is used for power generation. The Peltier effect, conversely, describes the development of a thermal gradient in the material in which an electrical current is present. The Peltier effect is used in the refrigeration/cooling applications. The major advantages of the thermoelectrics over conventional power generation and refrigeration methods are the absence of moving parts and toxic gases, robustness and the potential of power generation from waste heat. Scalability makes thermoelectric devices attractive for the thermal management of integrated circuits, which is the biggest challenge in microelectronics today. Widespread applications of thermoelectric devices, however, still remain elusive, owning to their poor efficiency in comparison with conventional power generators and compressor-based

refrigeration. Therefore, the limited applications where thermoelectrics found practical use to date are those where the convenience and reliability outweigh the economy. For example, portable beverage storage, computer CPU or an infrared detector cooling are accomplished with thermoelectric refrigerators with bismuth telluride alloys. Also, NASA's deep space probes use thermoelectric generators as power sources. Clearly, thermoelectrics is a very promising field; however, high efficiency devices are still a major bottleneck.

The efficiency of a thermoelectric material is described by the nondimensional figure of merit ZT,

$$ZT = \frac{S^2 \sigma T}{\kappa} \tag{5.1}$$

where σ is the electrical conductivity, κ is the thermal conductivity, T is the temperature and S is the thermoelectric power (a.k.a. Seebeck coefficient) defined as the thermoelectric voltage (V_p) produced per degree temperature difference:

$$S = \frac{dV_p}{dT} \tag{5.2}$$

The central issue in the thermoelectrics research is to increase ZT. From (5.1), this may be accomplished by increasing the Seebeck coefficient of the material (S), minimizing joule heating losses by maximizing σ, and minimizing κ to reduce heat leakage. However, the major challenge in maximizing ZT arises because the three material parameters comprising ZT are not mutually exclusive. The best thermoelectric materials were summarized as phonon-glass electron crystal. Traditionally, the best ZT materials have been heavily doped semiconductors. Insulators have low thermal conductivity, but

also very poor electrical conductivity. Metals, where the thermal diffusion of electrons and holes largely cancels the thermal voltage, have relatively low Seebeck coefficients. In addition, the thermal conductivity of a metal, which is dominated by the electrons at room temperature, is in most cases proportional to the electrical conductivity, as dictated by the Wiedmann-Franz law.[8] Metals, therefore, generally are poor thermoelectric materials. In semiconductors, the thermal conductivity has contributions from both electrons (κ_e) and phonons (κ_{ph}), with the majority usually coming from phonons. Therefore, phonon contribution to thermal conductivity can be reduced without causing significant reduction in the electrical conductivity. Lightly doped bulk semiconducting materials, in general, have large Seebeck coefficients, but poor electrical conductivities.[9] While heavily doped semiconductors in bulk do exhibit lower thermopower, it can be enhanced, as we show in this work, by nanostructuring the material to a 1D phonon confinement.

Traditionally, the way to reduce κ without affecting S and σ in bulk materials was to use semiconductors of high atomic weight, such as Bi_2Te_3 and its alloys with Sb, Sn and Pb. Thermal conductivity is reduced in the materials of high atomic weight due to the decrease in the speed of sound. However, such approach fails to produce bulk materials with ZT>3 required for a widespread application. The development of a better bulk material for thermoelectric applications has, at least for now, reached a deadend. Recent developments in nanomaterial science, nevertheless, hold a significant promise of improving the thermoelectric figure of merit beyond the current limits. Over the past decade, effects of quantum confinement on the thermoelectric properties have received increasing attention. [4, 10-13] Dresselhaus' work was the first to inspire the study of low-

dimensional structures as a means of improving the electronic performance of thermoelectric materials. The thermopower of a metal or a degenerately doped semiconductor is proportional to the derivative of the log of the density of states (DOS) n(E) with respect to energy, evaluated at the Fermi energy (E_F):[7]

$$S(T) \propto \left(\frac{\partial \ln n(E)}{\partial E} \right)_{E_F} \tag{5.3}$$

By nanostructuring semiconductors with sizes comparable to the electron wavelength, sharp peaks in the electronic density of states are produced. It has been hypothesized that by matching the location of E_F with the peak in the DOS, the thermopower may be tremendously enhanced. Moreover, the mobility and thus the electrical conductivity would also be increased, leading to a further enhancement of ZT. So far, metallic SWNT remains the only 1D system where the behavior described by the Mott formula has been clearly verified experimentally.[14]

It was realized early on that a potential improvement in ZT may rely less on quantum confinement of electrons and more on the phonon dynamics and transport.[5, 6] The size of the material may be tuned to be smaller than the mean free path of the phonons and larger than that of electrons and holes, thus reducing the thermal conductivity without significantly altering the electrical transport. However, while the charge transport in thermoelectricity is almost monoenergetic ($E=E_F \pm kT$), phonon-mediated heat transport is broadband.[5] The lowest thermal conductivity in crystalline solids is that of an alloy, and is referred to as the 'alloy limit,' which is dominated by the scattering of short-wavelength phonons. By using nanostructures such as superlattices,[15]

nanowires,[16] and nanoparticles,[17] it is possible to beat the alloy limit by means of the scattering of mid- and long-wavelength phonons in addition to short-wavelength phonons. At room temperature, the dominant heat-carrying phonons typically have mean free path of 10-100nm.[6] Thus, the nanostructures which effectively reduce the thermal conductivity have the dimensions of that order. Reports of enhanced ZTs of nanostructures have provided the first set of experimental evidence of the importance of controlling phonon dynamics in thermoelectric materials. Venkatasubramanian et al. have quoted ZT of ~2.4 at room temperature of thin-film supperlattices of Bi_2Te_3 and Sb_2T_3.[15] In addition, PbSeTe/PbTe quantum dot supperlattices with ZT ~1.3 to 1.6 were reported.[17] More recently, cubic $AgPb_mSbTe_{2+m}$ bulk nanocomposites with ZT ~2.2 at 800K were demonstrated.[18]

Besides the superlattice and quantum dot structures, nanowires are also capable of significantly reducing the phonon-mediated thermal conductivity compared with the bulk materials. Specifically, silicon nanowires (SiNWs)[16] were shown to exhibit size dependent reduction of thermal conductivity compared with thin-film[19, 20] and bulk[9] single-crystal silicon. The majority of the drop in thermal conductivity in silicon nanowires was attributed to boundary scattering. Being the workhorse of the microelectronic industry, silicon is extremely well studied and micro/nanofabrication techniques for silicon are well established. This makes silicon a desirable candidate material for thermoelectric applications. To date, however, no reports on the thermoelectric figure of merit of SiNWs have been published. This is not entirely surprising, since the simultaneous measurement of thermopower, electrical and thermal conductivities on the same nanowire as a function of temperature is very difficult. The

challenges are numerous, including precise control of the doping levels, diameter and length of the nanowires, as well as the high quality electrical contacts to the medium and lighly doped SiNWs. In addition, obtaining statistically significant values by measuring many identical nanowires is required. Current VLS technique for growing SiNWs,[21] while capable of creating high quality wires, falls short of the level of control over multiple parameters which is required for carrying out the comprehensive study into the thermoelectric properties of SiNWs. The SNAP method,[22] described in previous chapters of this thesis, is an ideal tool for such an endeavor.

In this work, we study the effects of doping, diameter and temperature on the figure of merit (ZT) of silicon nanowires. We demonstrate that, as previously shown,[16] the thermal conductivity of SiNWs is greatly reduced compared to the bulk material. This reduction occurs without a significant compromise of the electrical conductivity of heavily doped SiNWs, which remains quite high and comparable to the bulk. We further show that, while the thermopower of the heavily doped (~10^{20} cm^{-3}) nanowires is proportional to the temperature (similar to the bulk), the thermopower of the wires doped a bit lower, at a level of ~3e19 cm^{-3} exhibit evidence of phonon drag[7] below room temperature. Phonon drag in bulk semiconductor materials has only been observed at very low temperatures[23] and significantly lower doping levels.[9] We believe that the existence of phonon drag in nanowires is due to a combination of low thermal conductivity and increased relaxation times of long-wavelength phonons. Furthermore, we hypothesize that this may be generic to every 1D phonon system. Thus, the separate contributions of high thermopower (due to phonon drag), high electrical conductivity (due to high doping level) and low thermal conductivity (due to phonon boundary

scattering) together yield a significant enhancement of the figure of merit of SiNWs compared with the bulk silicon materials. The highest value of ZT observed is ~1.2 at 200K and 0.9 at 300K. We believe that the ZT above 3 at room temperature may be possible in silicon nanowires, and we discuss strategies to improve the efficiency beyond what is reported here.

5.2 Experimental Methods

5.2.1 Thermoelectric Device Fabrication

The starting substrate for fabrication was SOI Smart Cut wafer that has been thinned down to between 20 and 35 nm thick device layer by thermal oxidation followed by BOE wet etch. The wafers were p-type doped by the spin-on diffusion doping (SOD) method described in detail in chapter 1. Afterward, the remaining thin polymer film was removed by alternating washes with acetone, water and BOE. Platinum nanowires were deposited onto the wafer as described in chapter 1. For 7 to 10 nm wide wires, prior to pattern transfer to silicon epilayer, e-beam lithography (EBL) and Ti/Pt (5 nm/30 nm) evaporation were used to define two large pads approximately 1 μm apart for in-plane silicon contacts (chapter 1). For the thermopower measurements, each device consisted of approximately 10 nanowires, 3 μm long. Sometimes, particularly in the case of lighly doped 10 nm wires, more NW (40-100) were used in parallel to obtain reliable conductivity and thermal voltages. For the thermal conductivity measurements, usually 100 to 150 NWs were used to increase signal-to-noise ratio. While the thermal voltages are quoted here for a group of wires, the thermal conductivities and the electrical conductivities are per wire for every device. After sectioning the lattice into an appropriate number of NWs, electrical

heaters were defined by EBL and the evaporation of 10 nm Ti and 100 nm Pt. Next, four metal contacts were fabricated on top of the SiNWs by EBL and the evaporation of 10 nm Ti and 180 nm Pt. Immediately prior to metallization, the device was briefly treated in O_2 plasma (20 mTorr, 20 sccm, 10W) for 30 seconds, followed by the immersion into BOE solution for 4 seconds, water rinse and N_2 blow-drying. This step is necessary to obtain good quality electrical contacts between silicon and titanium. After the acetone liftoff, the device was annealed in forming gas (95% N_2, 5% H_2) for five minutes at 475 ^{o}C. Large gold pads (10 nm Ti, 250 nm Au) for wirebonding to the chip carrier were defined by photolithography. Scanning electron microscopy (SEM) images of the representative devices used to measure thermopower and electrical conductivity of 10 nm and 20 nm SiNWs are shown in Figure 5.1.

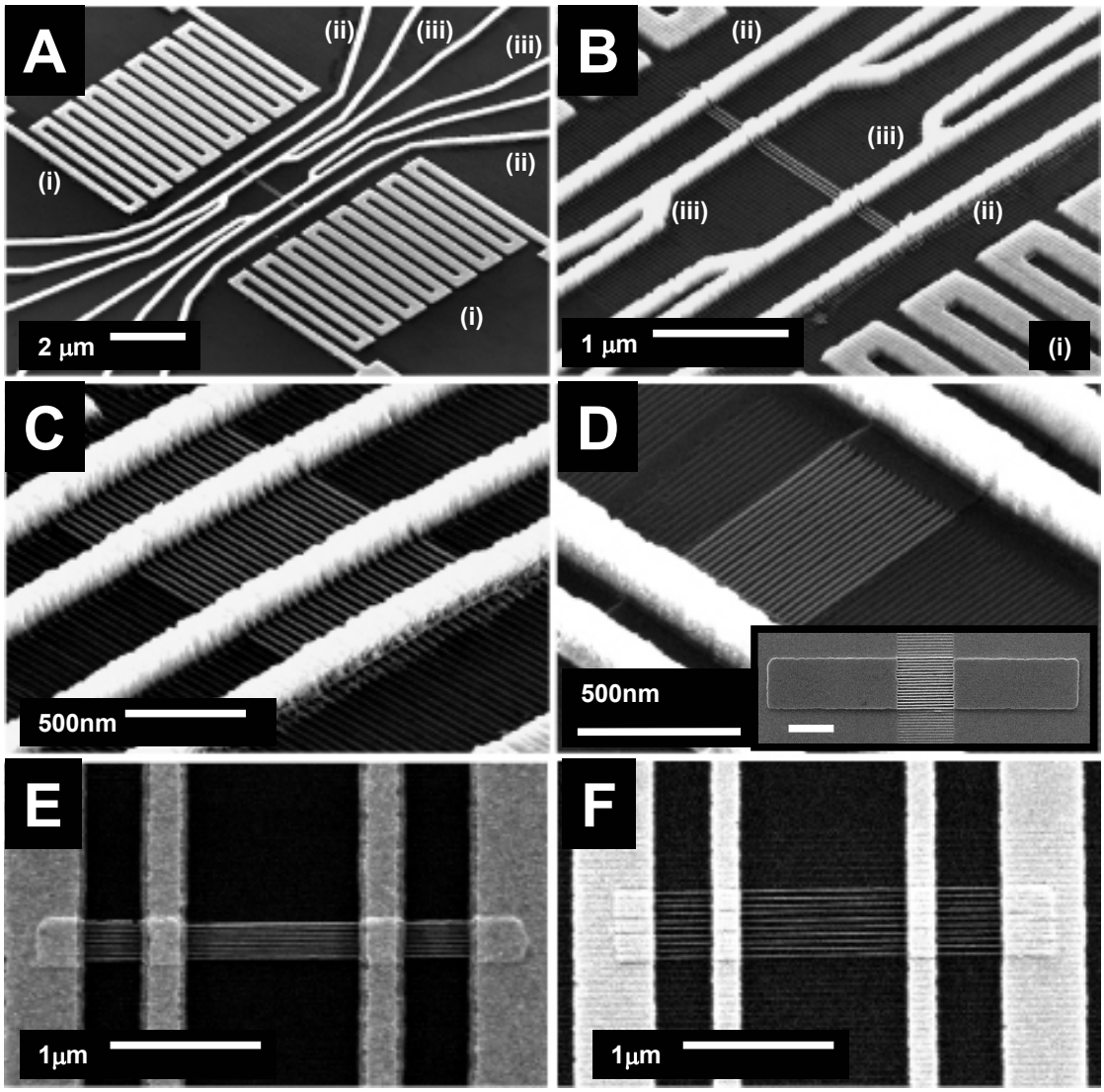
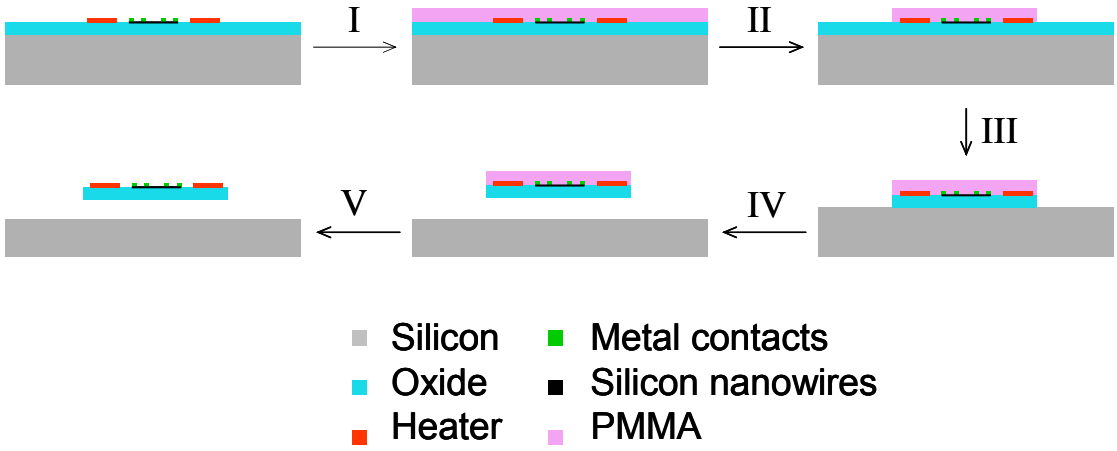


Figure 5.1: A) SEM of a device for measuring thermopower and electrical conductivity. Temperature gradient is created with either one of the two heaters (i) and measured with two 4-point resistive thermometers (iii). Thermal voltage is measured also between the two thermometers (iii). Nanowire resistance is measured with 4-point method, where the current is applied between the outer two leads (ii) and the voltage is measured between the inner two leads (iii). The heaters and all the leads are made of platinum, with a thin titanium adhesion layer. B) Zoomed-in image of A. C) Twenty-one 10 nm SiNWs connected in parallel. D) Eighteen 10 nm SiNWs in parallel with monolithic Si-metal contacts. Inset shows 10 nm SiNWs with monolithic contacts before the deposition of metal contacts. E) and F) are images of representative 20 nm and 10 nm SiNWs, respectively, used in this study. The pitch of the 10 nm SiNW lattice is 50 nm while that of 20 nm SiNW lattice is 35 nm.

For the thermal conductivity measurements, the nanowires and heaters were suspended on platinum leads over an approximately 600 μm by 600 μm area. Polymethylmethacrylate (PMMA 950, 6%) was spun on top of the wafer containing the device (Figure 5.1A). Scheme 5.1 demonstrates the fabrication steps used to suspend the



Scheme 5.1: An outline of the fabrication steps to suspend SiNWs. PMMA is spun on the device (I) and a large window excluding the nanowires and heaters is opened with EBL (II). Dry etch is used to remove oxide in the unprotected area (III), followed by the anisotropic etch with XeF_2 (IV). Finally, the PMMA mask is removed in O_2 plasma (V).

nanowires. A large window was opened in PMMA with EBL that included all of the area from the nanowires to large gold pads, but excluded a ~10 μm by 20 μm area containing the heaters and nanowires, which remained protected by the PMMA. A dry etch consisting of CF_4/He (20 sccm/30 sccm, 10 mTorr, 40W) was used to etch through ~150 nm of oxide (SOI box layer), exposing the silicon handle. Immediately after etch, the device was placed in a custom-made vacuum chamber and silicon was isotropically etched with XeF_2 (2.5 Torr) for 1.5 minutes, releasing the nanowires and heaters from the underlying silicon handle. The PMMA mask remaining on the device was etched in O_2 plasma (20 mTorr, 20 sccm, 55W) for 5 minutes. The device was wire bonded to a custom made chip carrier made from a copper piece with which the wafer made an intimate contact (Figure 5.2B).

The chip carrier was attached to a custom made chip carrier socket such that the copper piece of the chip carrier made intimate contact with the gold-plated copper holder of the cryostat (Figure 5.2 A,C). Before the measurement, the cryostat chamber (Janis VPF-475) was pumped down to ~10^{-7} Torr with Pfeiffer turbo pump TSH-071E.

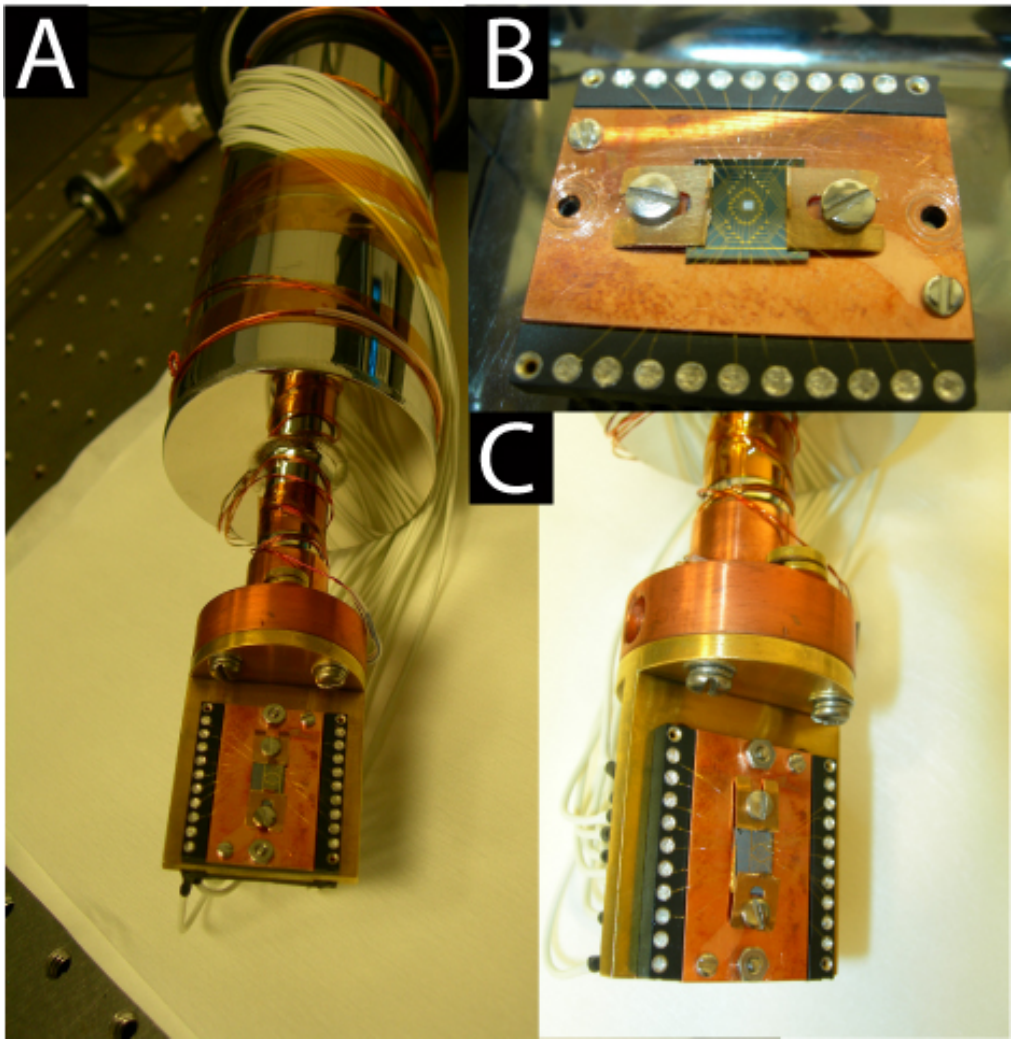


Figure 5.2: A) Cold finger liquid N_2 cryostat with gold-plated copper holder containing chip carrier socked which houses the chip carrier made from a copper piece. Silicon wafer with a fabricated device is fixed on top of the chip carrier. B) High resolution picture of a device wirebonded to a chip carrier. C) High resolution image of A, showing a copper chip carrier making intimate contact with the gold-plated cryostat holder. The temperature of the cryostat holder is controlled by PID temperature controller via a heater and a silicon diode thermocouple.

5.2.2 Electronic Measurements

A single suspended device pictured in Figure 5.3 can be used for the measurement of every parameter comprising the figure of merit (ZT), namely the thermopower, electrical conductivity and thermal conductivity.

Thermopower and electrical conductivity. A method described elsewhere[24] was adapted for the measurements of thermopower of SiNWs. Devices were fabricated as described in

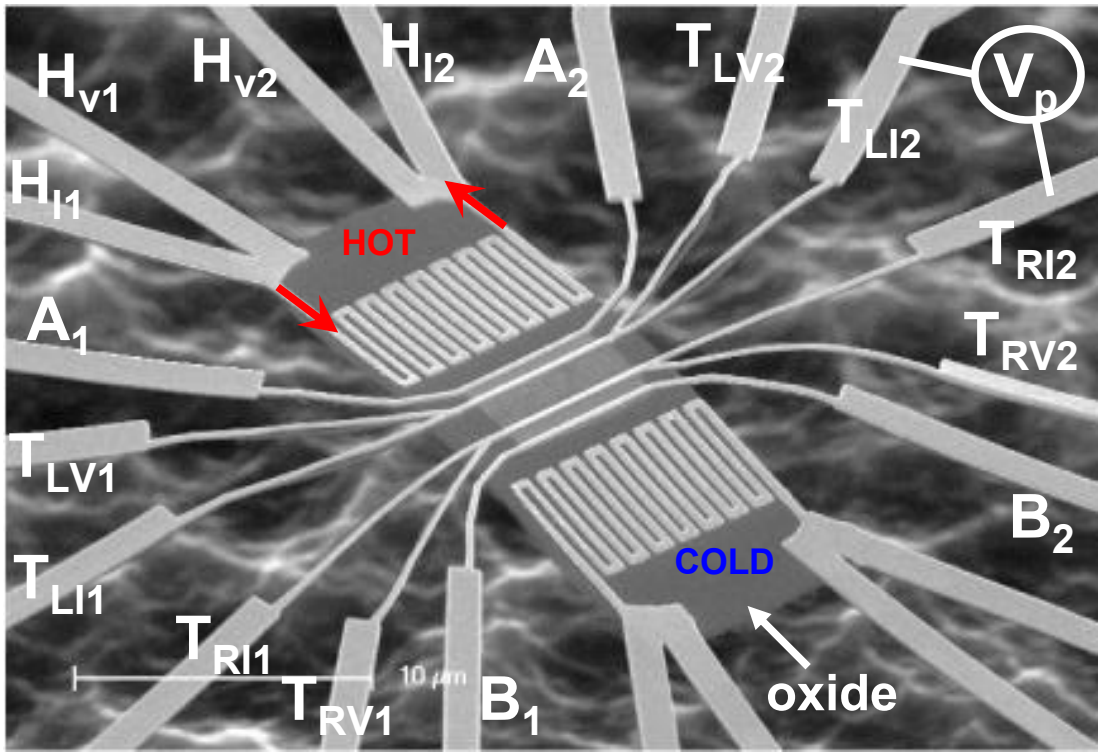


Figure 5.3: Suspended 10 nm SiNW device for the measurement of thermopower, thermal conductivity and electrical conductivity. Temperature gradient is set up by joule heating of the heater. Current is applied to one of the two heaters (red arrows, H_{I1}-H_{I2}), and the 4-point resistance of the heater is measured by determining the voltage drop (H_{V1}-H_{V2}). Thermal voltage (V_P) is measured between the two thermometers ($T_{LI1,2}T_{LV1,2}$-$T_{RI1,2}T_{RV1,2}$). The temperature difference between the two thermometers is measured by determining the 4-point resistances of both thermometers (left thermometer–voltage (T_{LV1}-T_{LV2}) and current (T_{LI1}-T_{LI2})) as a function of heater power and cryostat temperature. Electrical conductivity is measured as a 4-point, where the current is applied through the SiNWs between the outer leads (A_1A_2-B_1B_2) and the voltage is recorded between the inner leads ($T_{LI1,2}T_{LV1,2}$-$T_{RI1,2}T_{RV1,2}$).

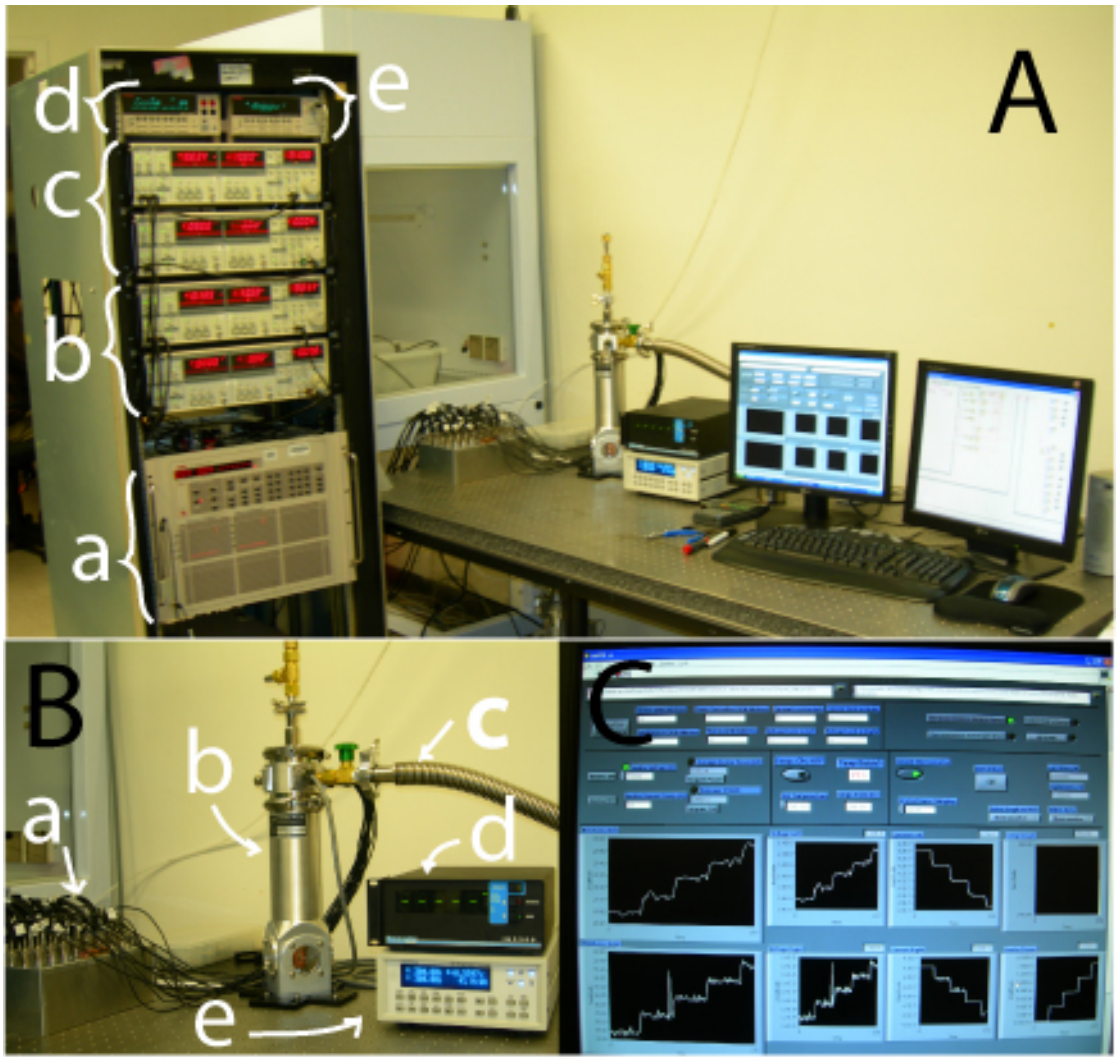


Figure 5.4: A) Experimental setup and instrumentation used for electronic measurements of thermoelectric properties of SiNWs. Keithley 707A switching matrix (a) is used to select between instruments and device connections. The 4-point resistances of the two Pt thermometers (right and left) are recorded with SR830 lockin amplifiers (two per thermometer), (b) and (c) respectively. The Keithley 2400 source-meter (d) is used to apply DC current to the heater for generating a temperature difference. Keithley 2182A nanovoltmeter (e) is used to either record thermal voltage between the two thermometers or to measure 4-point voltage of the suspended heater for thermal conductivity measurements. B) Break-out box (a) is used to connect all the leads on the device to the switching matrix. The device is kept in the cold finger liquid N_2 cryostat (b), and the temperature is controlled via a heater and a silicon diode sensor of a PID temperature controller (e). High vacuum (c) is maintained throughout the measurements, and the pressure is recorded with the ion gauge controller (d). C) All of the instrumentation and the temperature controller are controlled with the Labview program. The picture shows the simultaneous recording of the resistances of the two thermometers as the current through the e-beam fabricated heater is increased in a stepwise fashion.

section 5.2.1 (Figure 5.3). The experimental setup is shown in Figure 5.4. Joule heating ($P=I^2R$) from a single heater was used to locally heat the substrate and create a temperature gradient along the nanowires. To obtain thermopower, $S=dV_p/dT$, thermal voltage and temperature difference between identical points on the nanowires (inner metal leads, Figure 5.3) were independently obtained as a function of 2-point heater power. Keithley 2400 source-meter was used to apply DC voltage and measure DC current through two leads of the heater (Figure 5.3, H_{I1}-H_{I2}), while Keithley 2182A nanovoltmeter was used to measure the thermal voltage (an average of 6 measurements). For every device, we performed a test to make sure the recorded voltage is due to thermal gradient, and not to leakages, etc. While keeping the polarity of the two voltmeter leads the same, we measured the thermal

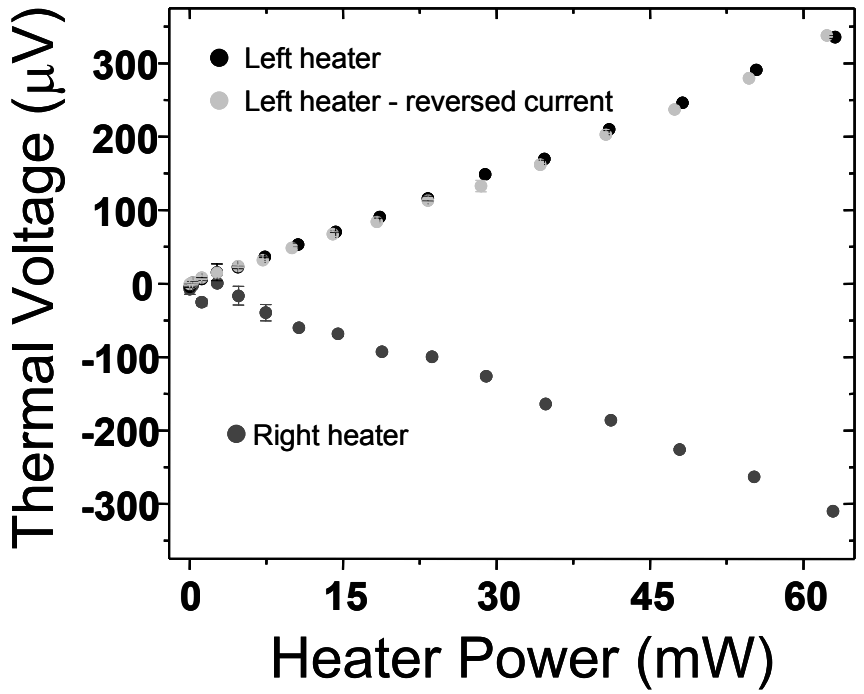


Figure 5.5: Thermal voltage of 20 nm SiNWs as a linear function of heater power. Both the right (dark grey) and left (black, light grey) heaters were used to confirm the correct sign reversal of the thermal voltage Because the heaters are identical and are approximately equidistant from the NWs, the temperature gradient and thus thermal voltages are identical for both heaters for the same power dissipated. Reversing the current in a heater does not alter the sign or the magnitude of the recorded thermal voltage. Error bars represent one standard deviation (σ) of six measurements.

voltage twice, first using one heater, then the other. As expected (Figure 5.5), the thermal voltage switches signs as the temperature gradient is reversed. Moreover, the sign of the thermal voltage was always consistent with p-type material where the holes are the majority charge carriers (Figure 5.5). In addition, since the joule heating is independent of the direction of the current, reversing the current in the heater does not alter the sign or the magnitude of the thermal voltage (Figure 5.5).

To convert thermal voltage (V_P) as a function of heater power (W_H) to thermal voltage as a function of temperature difference (dT), two additional measurements were carried out. With the first one, the resistances of two thermometers (R_{LT}-left, R_{RT}-right) were simultaneously measured as a function of heater power (either left or right heater) (Figure 5.6A). The DC current to the heater was supplied with Keithley 2400 source-meter (Figure 5.3, H_{I1}-H_{I2}) and the voltage was measured with both Keithely 2400 (for 2-point resistance, H_{I1}-H_{I2}) and the 2182A nanovoltmeter (for 4-point resistance, H_{V1}-H_{V2}). The second measurement provided the relationship between the resistances of the two thermometers and the cryostat holder temperature (dT), which was controlled with a Lake Shore 331 temperature controller (Figure 5.6B). The resistances of the thermometers in both measurements were obtained with four SR830 DSP lockin amplifiers, two for each thermometer. One lockin amplifier was used to measure the current (Figure 5.3, T_{LI1}-T_{LI2} or T_{RI1}-T_{RI2}) while the other was used to measure the voltage drop in a short section around the NWs (Figure 5.3, T_{LV1}-T_{LV2} or T_{RV1}-T_{RV2}). All measurements yielded linear functions, which were used to calculate the thermopower as follows (assume left heater was used):

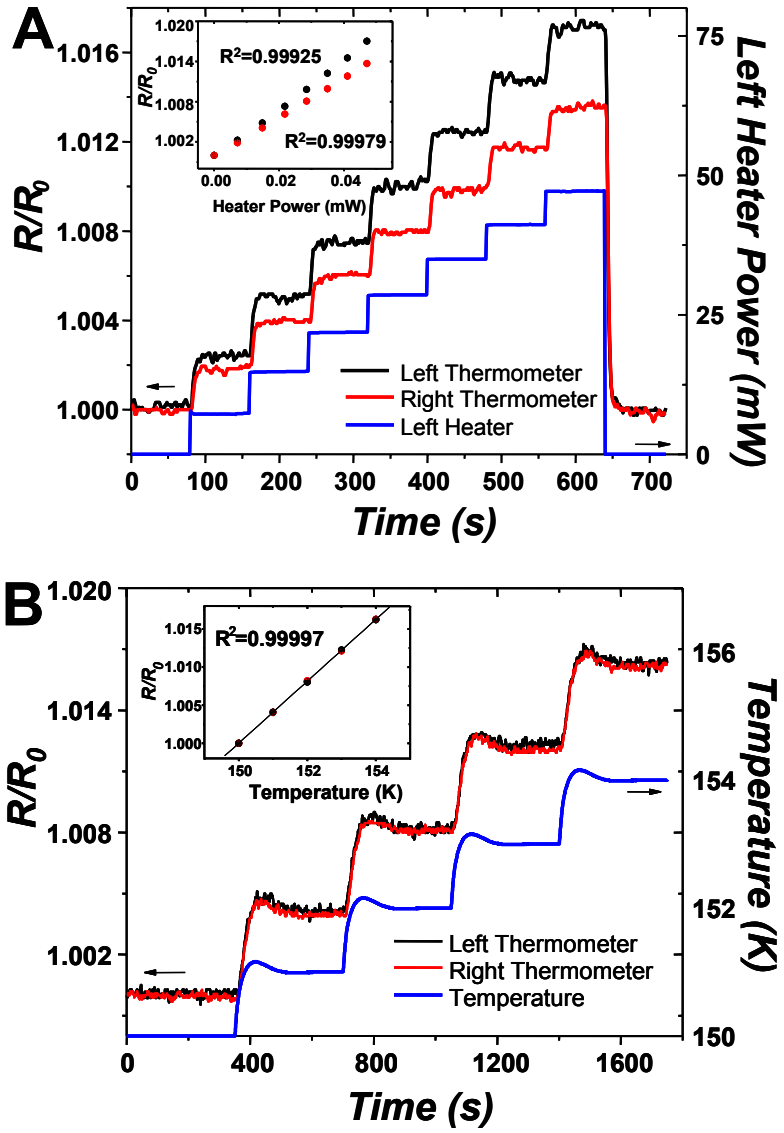


Figure 5.6: A) Simultaneous real-time measurement of resistances of both thermometers (black and red, left y-axis) as a heater power (blue, right y-axis) is increased stepwise. The left thermometer is more responsive because it is closer to the left heater. For each heater power, 80 resistance points were collected, and last twenty of those were averaged. Inset: Linear relationship between the thermometer resistance and heater power, dR_T/dW_{LH}. B) Simultaneous real-time measurements of resistances of both thermometers (black and red, left y-axis) as the cryostat temperature (blue, right y-axis) is increased stepwise by 1K. Both thermometers respond identically to the global temperature change. For each temperature, ~800 resistance points were collected and last 150 of those were averaged. Inset: Linear relationship between the thermometer resistance and global temperature, dR_T/dT. For convenience here, all resistances are normalized by the initial resistance, R_0. Error bars are normalized standard deviations of the thermometer resistances.

$$S = \frac{dV_P}{dT} = \frac{dV_P}{dW_{LH}} \times \left(\frac{dR_{LT}/dT}{dR_{LT}/dW_{LH}} - \frac{dR_{RT}/dT}{dR_{RT}/dW_{LH}} \right) \qquad (5.4)$$

Figure 5.6 demonstrates an example measurement for determining the temperature gradient along the NWs as a function of heater power (the term in parenthesis in equation 5.4).

The electrical conductivity of SiNWs was measured with a 4-point method, sourcing DC current through NWs between the outer metal leads (Figure 5.3, A_1A_2-B_1B_2) with Keithley 2400 source-meter and measuring the voltage drop between the inner leads (Figure 5.3, $T_{LI1,2}T_{LV1,2}$-$T_{RI1,2}T_{RV1,2}$) with Keithley 2182A nanovoltmeter. The voltage was averaged five times for each current. Monolithic in-plane silicon/metal contacts were used

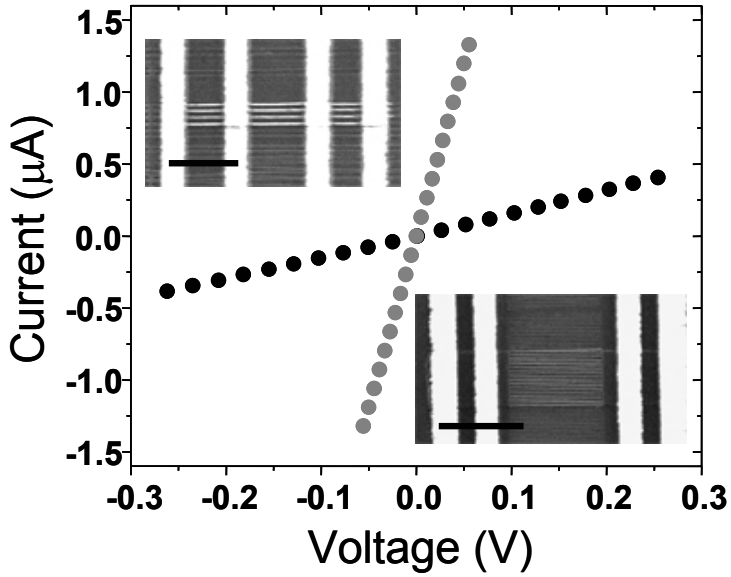


Figure 5.7: Current versus voltage (4-point) graphs of 10 nm wires doped at ~5e19 cm^{-3}. The resistance was significantly decreased when monolithic in-plane contacts (grey dots, lower inset) were used, as opposed to contacting nanowires directly (black dots, upper inset). The current was measured between the outer leads and the voltage was measured between the inner two leads. The current is normalized per wire per length for direct comparison. The scale bars in the insets are 500 nm.

for 10 nm SiNWs to minimize the contact resistance (Figures 5.1 C,D and 5.7). This was especially important for wires doped at $<10^{20}$ cm^{-3}. The monolithic contacts for 20 nm wires in the doping regime used in this study were not necessary due to negligible contact resistance.

Thermal conductivity. The method described elsewhere[25] was adapted for the measurements of thermal conductivity of SiNWs, with a few major differences. The method in reference 25 is tailored for nanowires and nanotubes which are fabricated separately (bottom up) from the rest of the device. Once the suspended heaters are fabricated, the nanostructure is then introduced between the two suspended Si_3N_4 membranes. Therefore, the 1D nanostructure is completely decoupled from the substrate except at the two points of attachment to the suspended membranes. Our SiNW fabrication procedure is top down. Therefore, the nanowires are fabricated attached to the underlying oxide, and should ideally be released from the substrate at some point prior to the measurements. We have found it very challenging to suspend both the two heaters and SiNWs. The only way to suspend the nanowires in our case is with the wet etch such as BOE. If the NWs are suspended first, all of the subsequent processing steps tend to cause the NWs to collapse. If the NWs are suspended as a last step, the rest of the suspended structure collapses as a result. We decided to circumvent this problem by only suspending one oxide island containing the SiNWs and both heaters (Figure 5.3), and performing two measurements, one with the wires and one without the wires. Isotropic etch with XeF_2 is specific to silicon, and does not etch oxide. Therefore, we first measured the thermal conductance of SiNWs plus the underlying oxide, and, after the selective etch of NWs, we repeated the measurement, obtaining the thermal conductance of oxide alone. Subtracting

the two values yields the thermal conductance of SiNWs. It is important to mention that, other than the XeF_2 etch, the samples were not perturbed between the measurements. In fact, the sample was etched in the XeF_2 chamber while remaining wire bonded to the chip carrier.

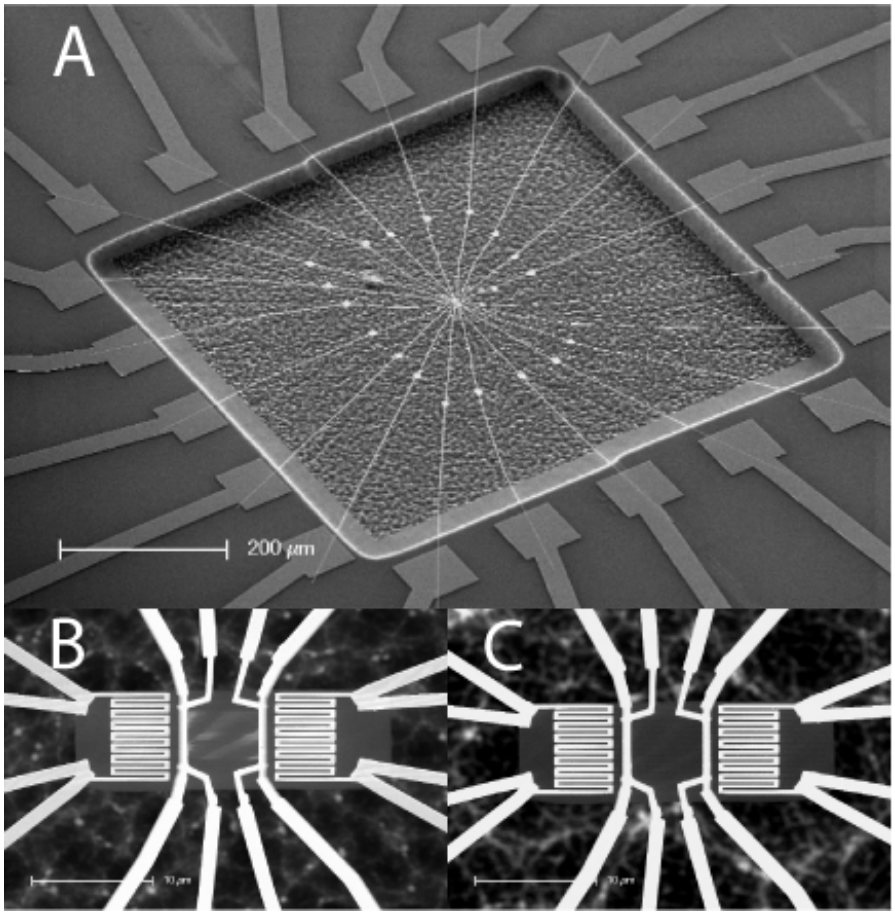


Figure 5.8: A) SEM of SiNW device suspended over ~600 μm by 600 μm area. B) Zoomed-in SEM of a suspended oxide island containing two heaters and two thermometers. The SiNWs are evident between the thermometers. C) The device from B, but after a selective SiNW etch with XeF_2. Scale bars in B,C are 10 μm.

Figure 5.8 demonstrates a typical suspended device used for the measurements of thermal conductivity of SiNWs before (Figure 5.8B) and after (Figure 5.8C) a XeF_2 etch. The isotropic dry etching of silicon nanowires is selective, and does not alter the device.

The second difference between the method described by Shi et al.[25] and our fabrication process is that the method described here allows the measurement of the full figure of merit, including thermopower, electrical and thermal conductivities, on a single device. Therefore, instead of utilizing the heaters as resistive thermometers,[25] we fabricated the thermometers separately from the heaters. This also allows us to more accurately measure the temperature gradient along the nanowires, since we cannot assume that the oxide underneath the heater is isothermal. The temperature change at the two thermometers (ΔT_h: thermometer closer to the heater, ΔT_s: thermometer further away from the heater) generated by a small increase in heater power (usually ~2-5 μW 2-point) is measured with SR830 lockin amplifiers as described above. For each thermometer, one amplifier supplies a 150-250nA, 913 Hz sinusoidal excitation current, while the other amplifier measures the voltage drop (on the order of 10-50μV) across a short section of the thermometer whose width is the width of the nanowire array (~5 μm). The joule heat (Q_h) produced by the heater on the oxide membrane is measured with 4-point method by sourcing a small DC current (50-100μA). The heat dissipated in both platinum leads carrying the DC current (Q_L) is measured by subtracting Q_h from the total (2-point) joule heat dissipated by the heater. According to the derivation performed by Shi et al.[25], the thermal conductance of the material between the two thermometers is

$$G_S = \left(\frac{Q_h + Q_L/2}{\Delta T_h + \Delta T_s} \right) \left(\frac{\Delta T_s}{\Delta T_h - \Delta T_s} \right) \tag{5.5}$$

$$G_{NW} = G_{S(oxide+NW)} - G_{S(oxide)} \tag{5.6}$$

where G_{NW} is thermal conductance of silicon nanowires. Then, the thermal conductivity of silicon nanowires (κ_{NW}) can be calculated in the following way:

$$\kappa_{NW} = G_{NW} \times \frac{L_{NW}}{nA_{NW}} \tag{5.7}$$

where n, L_{NW} and A_{NW} are number, length and cross-sectional area of nanowires, respectively.

5.3 Temperature Dependence of Silicon Nanowire Thermoelectric Properties

5.3.1 Electrical Conductivity

As mentioned above, the electrical conductivity of a thermoelectric device should be maximized for an optimum figure of merit. In semiconductors, the phonons carry a significant portion of heat, and, therefore, by reducing the diameter of the wires we are reducing the thermal conductivity of the material. If the doping is kept high enough, the electrical conductivity may be optimized without affecting the thermal conductivity. The Seebeck coefficient, however, is expected to decrease with the increase in carrier concentration. First, the electronic, or diffusion, component of the thermopower (S_d) for moderately doped semiconductors is affected by the hole concentration through the following relationship:[23]

$$S_d \propto \ln \frac{n_0}{n} \tag{5.8}$$

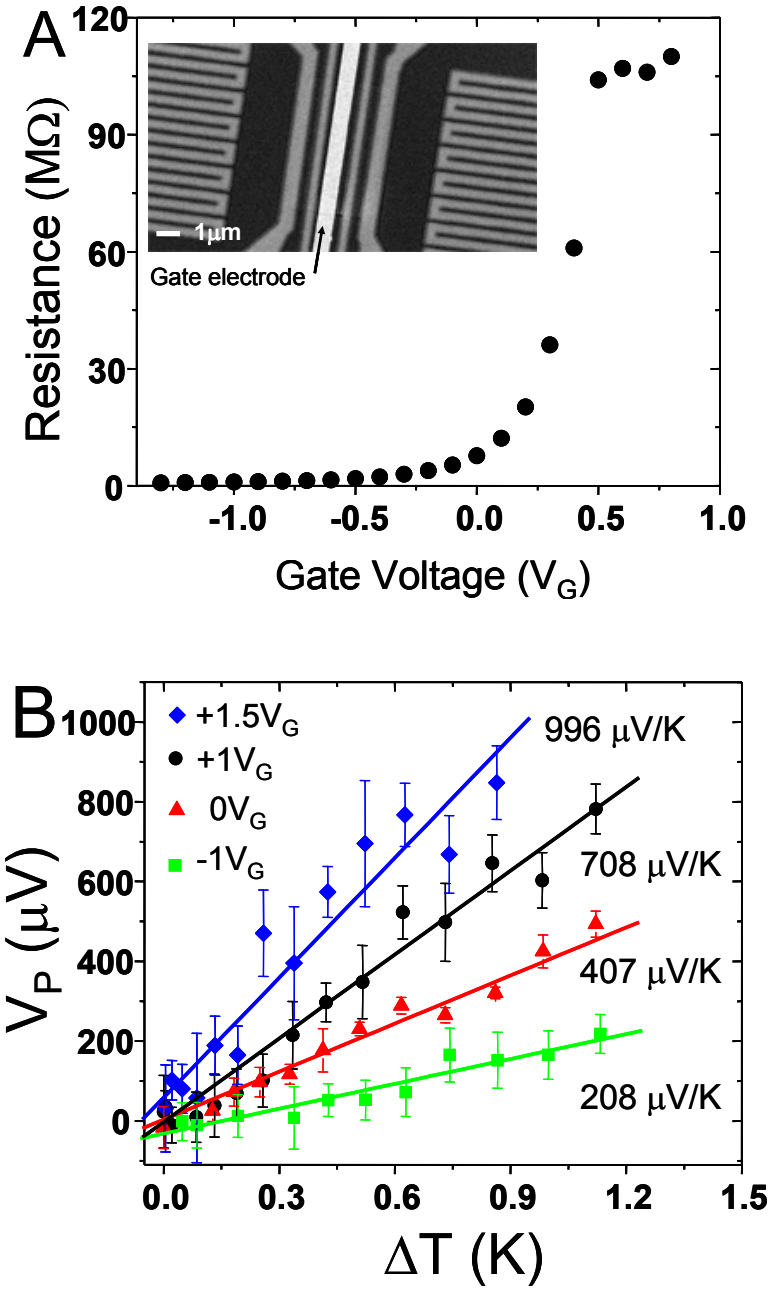


Figure 5.9: A) Four-point resistance of p-type (~5e18 cm^{-3}) 20 nm SiNWs as a function of gate voltage (V_G). Inset: SEM picture of the device demonstrating top gate Pt electrode separated from the NWs by 10 nm thick Al_2O_3 dielectric. B) Modulation of thermopower, $\Delta V_P/\Delta T$, with the top gate voltage. Each thermal voltage point was obtained by averaging six measurements of V_P, and the standard deviations are represented by the error bars. The Seebeck coefficients are obtained from the linear regression analyses, and represent the straight lines. Thermopower was measured for four values of the gate voltage: -1V (green squares), 0V (red triangles), +1V (black circles) and +1.5V (blue diamonds).

where n_0 is effective density of states in conduction band and n is the density of carriers (cm^{-3}). In addition, in bulk silicon[9] and germanium[26] the thermopower due to phonon drag (S_{ph}) has been shown to decrease significantly as the number of impurity atoms and charge carriers increased. Doping level is an important electronic parameter which is most easily tunable in our system. At the beginning of the project, with a large parameter space mainly unexplored, determining the maximum power factor, $S^2\sigma$, as a function of carrier concentration in SiNWs was crucial. We have studied the effect on the thermopower of carrier modulation inside SiNWs with a top gate. Ten nanometers of Al_2O_3 dielectric were deposited on top of the nanowires (p-type, ~5e18 cm^{-3}) and a platinum gate electrode was fabricated as shown in Figure 5.9A. Between the gate voltages of -1V and 1V, the resistance of the NWs increased by two orders of magnitude (Figure 5.9A). However, the thermopower was only increased 3.4 times, as indicated in Figure 5.9B. A small enhancement of thermopower, as suggested by equation 5.8 and Figure 5.9, argues that it is probably advantageous to maximize the electrical conductivity of the nanowires rather than attempt to enhance S_d. We also expected that possible advantages of phonon drag, evident in very low doped bulk silicon material[9] (a 2.4 times increase of S_{total} at room temperature– 1 mV/K from 0.4 mV/K–in n-type silicon doped at 10^{16} cm^{-3} versus 10^{19} cm^{-3}) would be completely offset by a dramatic reduction of the electrical conductivity of low doped SiNWs. Therefore, we chose to concentrate on the relatively high impurity concentration range between ~10^{19} and 10^{20} cm^{-3}. Figure 5.10 demonstrates the temperature dependence of typical electrical conductivities of 10 nm, 20 nm and 500 nm wide p-type nanowires, with approximate impurity concentrations between $5x10^{19}$ and $2x10^{20}$ cm^{-3}. In calculating the electrical conductivities, we assume that the NWs are effectively 10 nm thick, since the

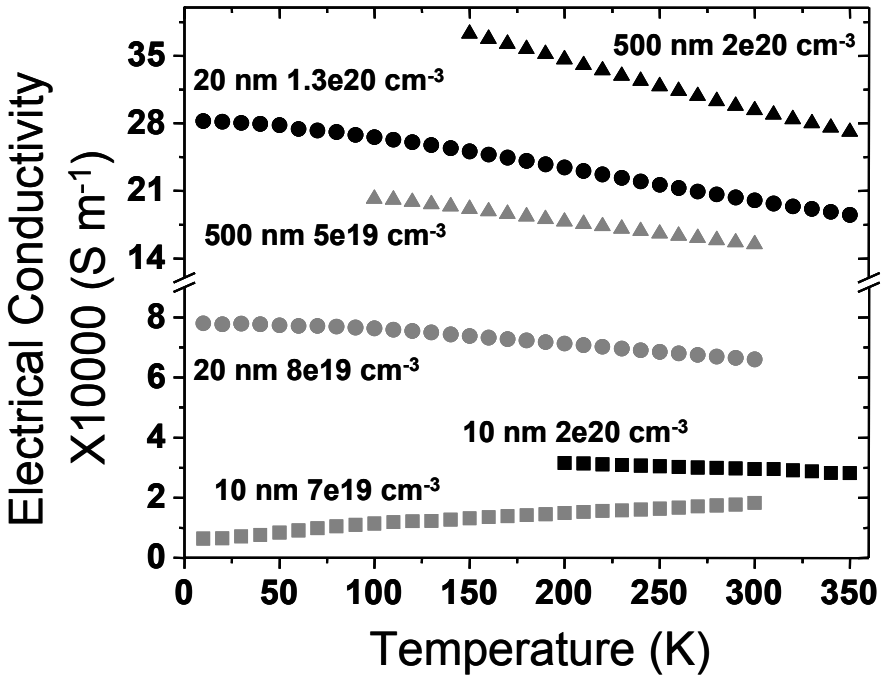


Figure 5.10: Electrical conductivity (per nanowire) versus temperature of typical nanowires with effective cross-sectional areas of 10 nm x 10 nm (squares), 20 nm x 10 nm (circles) and 500 nm x 10 nm (triangles). The doping level of each NW is indicated.

diffusion doping method (chapter 1) yields the majority of impurities in the top ten nanometers of the film. Degenerately doped (>10^{20} cm^{-3}) 10 nm and 20 nm wide SiNWs, like the bulklike 500 nm wide wires, exhibit metallic dependence of electrical conductivities on temperature, namely $\sigma \propto T^{-1}$. The 10 nm wide SiNWs doped below 10^{20} cm^{-3}, on the other hand, generally behave as semiconductors; their electrical conductivities vary as $\sim e^{-a/T}$. The metallic behavior in 10 nm wires is observed only when the SOI film is diffusion doped at ≥1000 ^{o}C. Clearly, large discrepancies between 10 nm and 20 nm wide NWs (equally doped, i.e., same doping temperature) in the values and the temperature dependences of their electrical conductivities argue for carrier scattering at the boundaries and possibly local fluctuations in the number of dopant atoms. Such fluctuations, or variance in the average number (N) of the dopant atoms, are expected to play an increasing role as the width of the wire (and N) is reduced, since the variance scales as $N^{-1/2}$. Our

attempts to fabricate wires with widths smaller than 10 nm (~5 to 7 nm) resulted in a further reduction of the electrical conductivities. Such drop in σ could not simply be accounted for by the decrease in the cross-sectional area of the nanowires. Therefore, generating nanowires with widths ≤10 nm and with bulk electrical conductivities is a major challenge. As will be demonstrated later in the text, this is the primary reason why at present 10 nm SiNWs doped below 10^{20} cm^{-3} consistently yield lower figures of merit compared to 20 nm NWs. As discussed above, low electrical conductivities of SiNWs doped at the level $<10^{19}$ cause these materials to exhibit a low figure of merit. A way to enhance the electrical conductivity of low doped NWs without affecting the Seebeck coefficient would certainly be beneficial in improving their efficiency. Recently, novel and significant linear electro-optic effect was observed in strained silicon.[27] Depositing Si_3N_4 layer on top of silicon compressively strains nitride layer and expands the underlying silicon. Such strain effect leads to the breaking of crystal symmetry of silicon. Jacobsen et al. demonstrated that in properly strained silicon, the bulk refractive index (n) varies linearly as a function of external applied electric field (E).[27] Thus, strained silicon is a novel material with new electrical and optical properties. We have applied this concept to SiNWs. The expectation is that lifting the degeneracy in the band structure of silicon strained with Si_3N_4 layer leads to an increase in electrical conductivity, with a negligible effect on the thermopower. Figure 5.11 demonstrates the electrical conductivities of 10 nm and 20 nm NWs (~5e18 cm^{-3} doping level) before and after the deposition of 0.7 μm PECVD silicon nitride layer on top of the wires. The electrical conductivity in both cases increases as the silicon is strained, with a more dramatic change observed for the 10 nm SiNWs. Initial attempts to measure thermopower after Si_3N_4 deposition suggest that there

are no significant effects on the S (data not shown). While more work must be done to understand fully the effects of strain on silicon thermoelectric properties, preliminary data

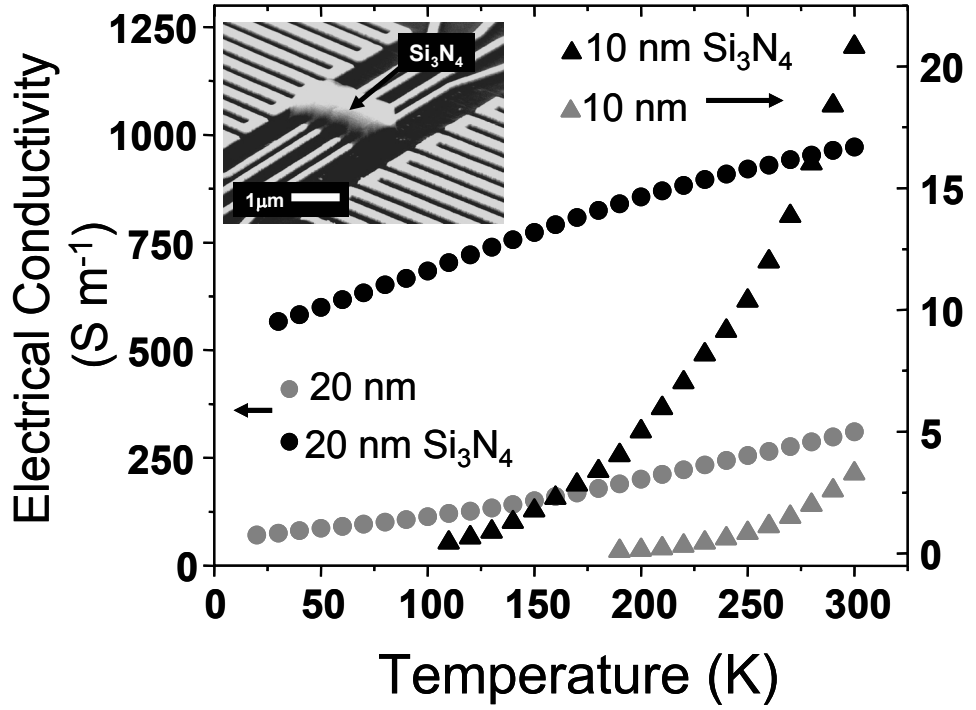


Figure 5.11: Electrical conductivity versus temperature of a 10 nm (triangles) and a 20 nm (circles) SiNW doped at ~5e18 cm^{-3}, before (grey) and after (black) the deposition of 0.7 μm thick Si_3N_4 layer. Inset: SEM of the device with the silicon nitride covering the nanowires.

clearly suggest that the electrical conductivity of SiNWs can be significantly improved under a proper strain.

5.3.2 Thermal Conductivity

As described in the introduction, the thermal conductivity should be minimized for an optimal ZT. Low thermal conductivity helps reduce the heat leakage down the temperature gradient. In semiconductors, heat is primarily carried by crystal vibrations (or phonons). Typically, at room temperature the dominant heat-carrying phonons have mean free paths of 10 to 100 nm.[6] Therefore, by reducing the diameter of a wire down to these

dimensions, it is expected that the thermal conductivity decreases dramatically. Model of phonon transport in silicon quantum wires yielded a reduction of the lattice thermal conductivity due to spatial confinement of acoustic phonons.[28, 29] The model took into account the modification of phonon dispersions due to spatial confinement and the change in nonequilibrium phonon distribution due to boundary scattering, leading to the prediction of reduced phonon group velocities and an order of magnitude reduction of the thermal conductivity of 20 nm cylindrical wires versus the bulk.[29] In addition, molecular dynamics

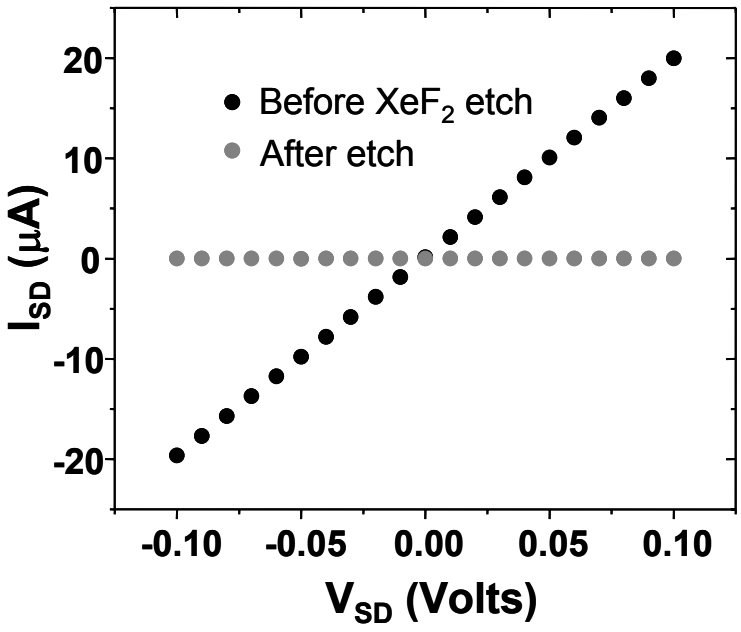


Figure 5.12: Current versus voltage graph of p-type 20 nm SiNWs (~7e19 cm^{-3}) suspended on an oxide membrane, before (black) and after 10 sec XeF_2 etch.

(MD) simulations[30] have demonstrated two orders of magnitude reduction in thermal conductivity of nanometer diameter NWs compared with the bulk Si thermal conductivity. Finally, the first experimental evidence of the thermal conductivity in SiNWs came from Majumdar et al.[16] As predicted by the theory, the thermal conductivity of 1D silicon nanowires was dramatically reduced. Since the drop in thermal conductivity strongly

correlated with the diameter of the wires, the authors concluded that phonon-boundary scattering was the primary reason for the reduction.

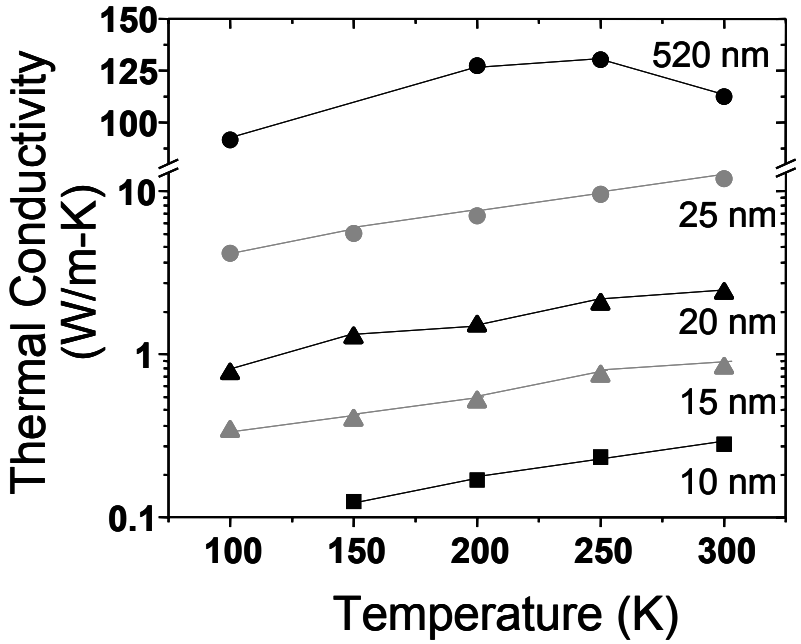


Figure 5.13: Measured temperature dependence of thermal conductivities of heavily doped (~1e20 cm^{-3}) SiNWs of different widths: 520 nm (black circles), 25 nm (grey circles), 20 nm (black triangles) and 15 nm (grey triangles).

We have carried out the measurements of the thermal conductivity of the SiNWs fabricated with the SNAP method. These nanowires have a rectangular cross section and, due to an RIE etch step in their fabrication, somewhat rougher sidewalls compared with the VLS SiNWs. As explained in the methods section of this chapter, releasing these NWs from the oxide substrate while maintaining the integrity of the suspended heaters presented a major challenge. We, therefore, obtained the thermal conductivities of nanowires on the oxide and of the oxide alone (Figure 5.8). The difference in the two values was attributed to the thermal conductivity of the NWs. The selective removal of the NWs with XeF_2 was confirmed once by the drop in the electrical conductivity (Figure 5.12) and again with the

SEM (Figure 5.8) after the measurement was completed. The thermal conductivities of wires of different widths are shown in Figure 5.13. At room temperature, the thermal conductivity of 520 nm wide (35 nm thick) wires was 112 $Wm^{-1}K^{-1}$, similar to the bulk value. Reducing the width of the wire had a profound effect on the thermal conductivity, which decreased to 0.28 $Wm^{-1}K^{-1}$ for 10 nm wide (20 nm thick) SiNW. This strongly corroborates the previous finding[16] of the dominance of phonon boundary scattering on the heat transport in 1D silicon nanowires. It is likely that the surface roughness of SiNWs fabricated with SNAP method significantly contributes to the reduction of NW thermal conductivity.

5.3.3 Thermopower and Phonon Drag

The thermopower of bulk silicon strongly depends on the impurity concentration.[9] It is difficult to achieve a Seebeck coefficient above ~400 to 500 μV/K at room temperature for heavily doped bulk (>10^{19} cm^{-3}) silicon. In this regime, the thermopower is purely due to carrier diffusion (S_e), and for a degenerately doped semiconductor, as for metals, is given by the Mott formula[7]:

$$S_e = \frac{\pi^2 k_B^2 T}{3e}\left(\frac{d\ln\sigma(E)}{dE}\right)_{E_F} \approx \left(283\,\mu V/K\right)\left(kT/E_f\right) \qquad (5.9)$$

where the derivative of the logarithm of the conductivity σ(ε) is the reciprocal of the energy scale over which it varies (the Fermi energy E_f for metals). Assuming hole doping occurs in the heavier Si valence band (mass 0.49) leads to E_f=0.076 eV=880K and k_f=0.1$Å^{-1}$ for n=3e19 cm^{-3}. This leads to an electronic term $S_e(T)$=aT where a=0.34 $\mu V/K^2$.

Figure 5.14 presents measured Seebeck coefficients versus temperature for SiNWs of different widths and doping levels. All of the degenerately doped ($\geq 10^{20} cm^{-3}$) SiNWs exhibit $S \propto T$ relation, indicative of the dominance of the carrier diffusion on the thermopower. However, the Seebeck coefficients of SiNWs with impurity concentrations less than 10^{20} cm^{-3} show very different temperature dependence. As the temperature is decreased from 300K, the thermopower increases, reaching a peak between 150K to 200K, and then continues to decrease below 150K. This behavior is observed in the 10 nm and 20 nm wide NWs, but not in the 500 nm samples. The inflection of thermopower is indicative of the phonon drag contribution (S_{ph}) to the thermopower.

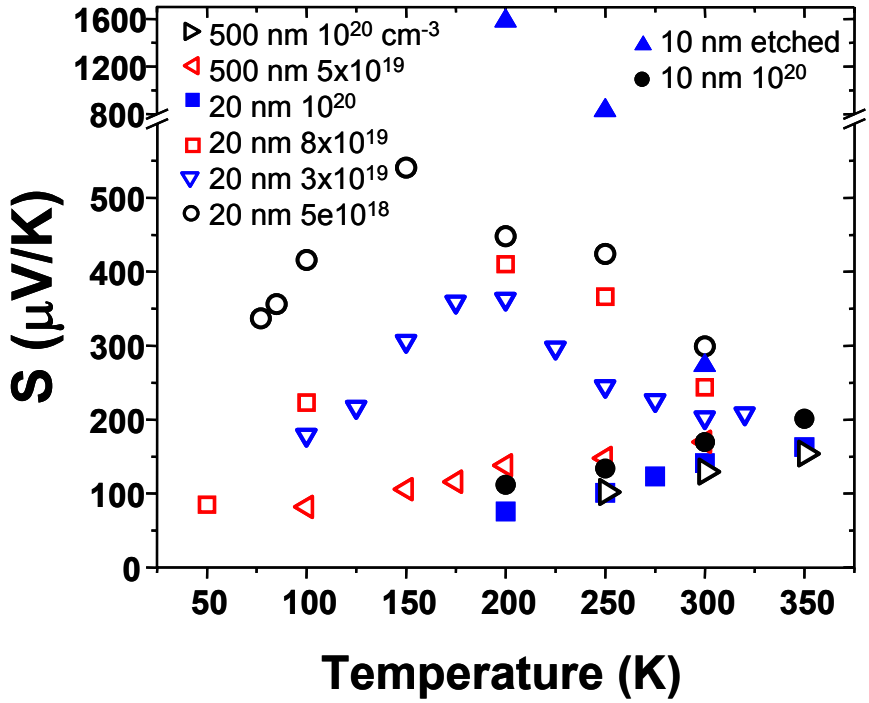


Figure 5.14: Measured thermopower (S) of 10 nm, 20 nm and 500 nm Si wires at different temperatures. The doping level for each sample is indicated. Seebeck coefficients of SiNWs doped below ~10^{20} cm^{-3} exhibit a peak between 150K and 300K, indicative of the phonon drag. This behavior is not observed in the 500 nm wide samples. The doping level of the 10 nm etched device is not known; however, it is probably between 10^{16} and 10^{17} cm^{-3}.

Phonon drag is observed in metals at low T because phonon lifetimes are long enough to make a measurable addition to the heat flux from electronic transport. At sufficiently low T (<20K), the phonon scattering length saturates to the dimensions of the sample leading to $S_{ph}\sim T^3$ from the phonon specific heat ($\sim T^3$). At high temperatures ($kT>>\Theta_{Debye}$), the specific heat becomes constant and the total number of phonons available for phonon-phonon scattering scales as ~T leading to $S_{ph}\sim 1/T$.

For p-type Si, the holes are near the valence band maximum at k=0 (Γ point). This leads to a Fermi surface with Fermi wavevector k_f. The largest momentum (shortest wavelength) phonon modes participating in phonon drag by being excited due to the holes scattering with phonons are longitudinal acoustic with wavevector, $k_{LA}=2k_f=0.2$ $Å^{-1}$ (assuming an impurity doping level of 3e19 cm^{-3}). The wavelength is $\lambda_{ph}=2\pi/k=31$ Å. The speed of sound in the (100) direction for Si is $c_L=8.43\times10^5$ cm/s, leading $\omega_{LA}=c_Lk=1.7\times10^{13}$ sec^{-1} with energy $\hbar\omega_{LA}=0.011$ eV=129K. Only phonon wavelengths larger than 31 Å can participate in phonon drag. In metals, k_f is on the order of the reciprocal lattice vector. Phonon wavelengths as short as a few lattice spacings participate in phonon drag. Short wavelength phonon lifetimes are less than long wavelength phonons leading to a small phonon drag contribution in metals.

Normal phonon-phonon scattering conserves crystal momentum and hence cannot dissipate heat. Thus Umklapp processes determine the rate of heat dissipation of the phonons. Umklapp scattering requires at least one phonon to have momentum of the size of the reciprocal lattice vector. The single parameter that sets the energy scale for Umklapp scattering is the Debye energy, Θ_{Debye}. Thus the number of Umklapp phonons available to

dissipate the long wavelength longitudinal phonons dragged by the holes is given by the Bose-Einstein function

$$N_U = \frac{1}{e^{\Theta_D/T} - 1} \qquad (5.10)$$

leading to a scattering rate $1/\tau_{ph} \sim N_U \sim 1/[\exp(\Theta_D/T)-1]$. When $T >> \Theta_D$, $1/\tau_{ph} \sim T$. Since Θ_D=640K for Si, the full Bose-Einstein expression must be applied for the temperature range of interest here, T<300K.

The total thermopower S is the sum of the electronic term (S_e) and the phonon term (S_{ph}). The high temperature (T>200K) data of the 20 nm wire wit doping n=3e19 cm^{-3} fits the expression

$$S = S_e + S_{ph} = aT + b\left[e^{\Theta_D/T} - 1\right] \qquad (5.11)$$

where a, b and Θ_D are varied to obtain the best fit (Figure 5.15). The maximum error is found to be 6.1 μV/K and the rms error is 1.8 μV/K. If the Debye energy is fixed at its experimental value, Θ_D=640K, the best fit occurs for a=0.4 $\mu V/K^2$ and b=12.2 μV/K. The maximum error and rms error are 8.9 μV/K and 2.1 μV/K respectively (data not shown).

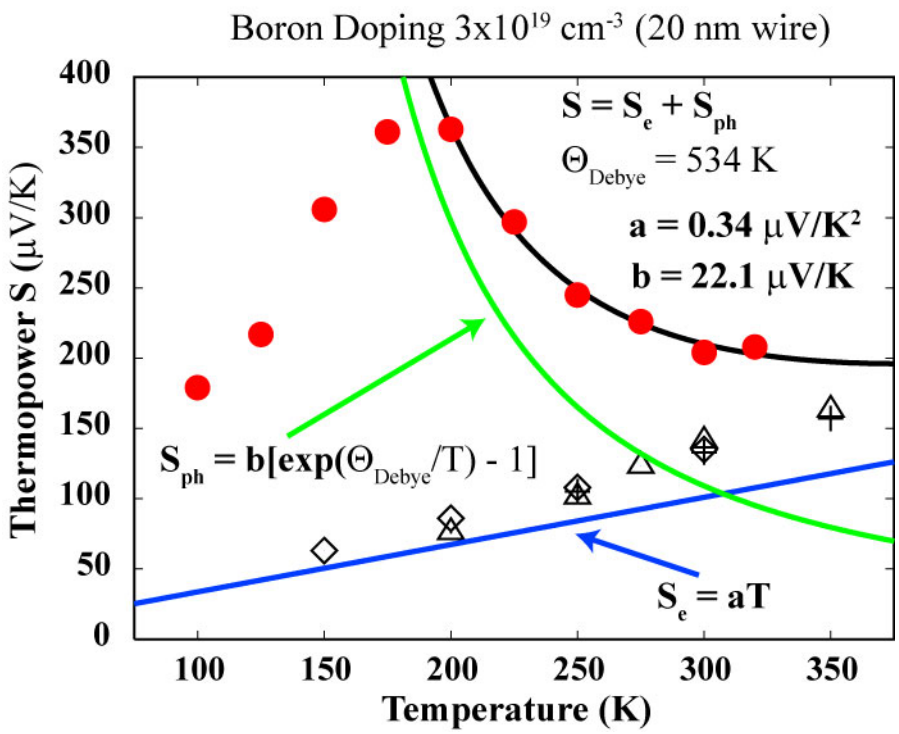


Figure 5.15: Thermopower calculation, plotted along with experimental data (red points) from a 400 nm^2 (20 nm× 20 nm) cross section Si NW p-type doped at 3×10^{19} cm^{-3}. The black curve is the fitted expression for the total thermopower shown by the red points. The green curve is the phonon contribution S_{ph} and the blue line is the electronic term S_e arising from the fit. The coefficients are a = 0.337 $\mu V/K^2$, b = 22.1 $\mu V/K$ and Θ_{Debye} = 534 K. The fitted electronic coefficient value is almost identical to our estimated value of a = 0.34 $\mu V/K^2$ assuming hole doping of Si with no Boron impurity band. This demonstrates that phonon drag provides a consistent explanation for the observed thermopower. Moreover, the black data points are experimental values for bulk wires with doping 2 x 10^{20} cm^{-3} (plus signs), 10nm wires with doping 7 x 10^{19} cm^{-3} (open diamonds), and 20nm wires with doping 1.3 x 10^{20} cm^{-3} (open triangles) for which only a linear T electronic contribution was observed. These data points are close to the linear electronic contribution from the red data points and demonstrate that the magnitude of the extracted electronic term is reasonable.

As stated above, the phonon drag in bulk heavily doped silicon is very small because of shorter lifetimes of dragged phonons. Only when the bulk silicon is weakly doped can the phonon drag contribute significantly to the thermopower, raising it to >1 mV/K at room temperature.[9] As Figure 5.14 demonstrates, heavily doped silicon nanowires exhibit phonon drag behavior at relatively high (200-300K) temperatures.

While the absolute thermopower of heavily doped nanowires is not significantly higher than the bulk value, phonon drag induced deviation from the linear $S \propto T$ behavior yields a 4 to 5 times increase in S at T~200K, translating into an order of magnitude increase in ZT. Importantly, a large electrical conductivity is maintained in these wires because of the high impurity concentration (Figure 5.10).

5.4 Discussion

The data presented in this chapter clearly suggest that there are multiple benefits of using nanostructured materials as thermoelectrics. Particularly, while bulk silicon has a poor thermoelectric figure of merit, nanowires made from single-crystal silicon exhibit ZT values that are over two orders of magnitude higher than those of the bulk Si (Figures 5.16 and 5.17). Such dramatic improvement arises in large part due to an ability to independently optimize the Seebeck coefficient, electrical conductivity and thermal conductivity in a nanowire–something that is impossible to accomplish in bulk semiconductors.

We believe that the electronic properties of 10 and 20 nm SiNWs are those of 3D material, and 1D DOS arguments do not apply in this case.[13] The improvement in the ZT, therefore, comes primarily from the modified phonon transport.[6] The drop in thermal conductivity is a number-one reason for improved efficiency in SiNWs (Figure 5.13). As others have reported,[16] and as has been verified by this work, the thermal conductivity of SiNWs decreases by over two orders of magnitude at room temperature compared to the bulk Si, evidently due to phonon-boundary scattering. The major challenge is to keep the electrical conductivity of SiNWs, especially those with diameters less than 20 nm, from

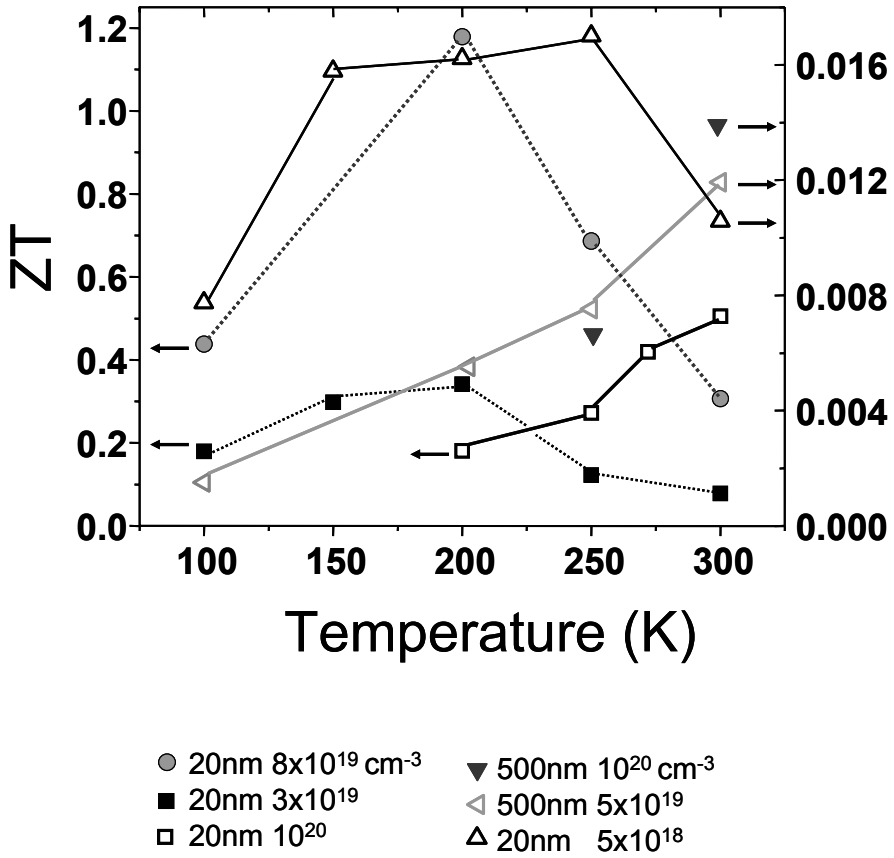


Figure 5.16: Figures of merit of 20 nm SiNWs compared with those of 500 nm x 20 nm bulk Si. The impurity concentrations are indicated in the legend. The left column of the legend is plotted on the left y-axis (grey circles, black squares, open squares), while the right legend column is shown on the right y-axis (black and open triangles).

drastically decreasing compared to the bulk (Figure 5.10). For 10 nm wires, this can only be accomplished at this time by degenerately doping the NWs, to a $>10^{20}$ cm^{-3} level, at temperatures $\geq$1000 ^{o}C (Figure 5.17). Any reduction in the impurity concentration below this level, or thinning the degenerately doped NWs via a dry etch, produces a sharp drop in the electrical conductivity and a corresponding decrease in the ZT (Figure 5.17). The Seebeck coefficient of these NWs is approximately the same as of the heavily doped bulk

(Figure 5.14), and varies as ~T. Therefore, as demonstrated in Figure 5.17, the ZT of degenerated doped 10 nm SiNWs approaches one at room temperature, and most likely increases further at higher temperatures, until the thermal conductivity becomes appreciable. Despite higher electrical conductivity, the figure of merit of 20 nm degenerately doped wires is somewhat smaller than 10 nm at room temperature because of higher thermal conductivity. However, when the doping of the wires is reduced to ~$5x10^{19}$ cm^{-3}, at temperatures between 150K and 300K, phonon drag contribution dramatically increases the thermopower (Figure 5.14), elevating the ZT at 200K above 1.0 (Figure 5.16). The phonon drag has only been observed in the lightly doped bulk silicon. We believe that 1D phonon confinement increases the lifetimes of long-wavelength phonons, presumably favoring phonon-hole scattering. Therefore, we are able to observe the phonon-drag effect in heavily doped SiNWs.

The results described above reaffirm that the field of thermoelectrics will benefit tremendously from the emerging progress in nanotechnology. No longer is the search for an ideal bulk material with the efficiency superior to Bi_2Te_3 alloys a bottleneck. Thermal and electrical properties of nanomaterials generally make them superior to the bulk materials in terms of the thermoelectric efficiency, as has already been demonstrated by several groups.[15, 17] Clever manipulation of the electronic[10] and phonon[6] transport in the nanomaterial to enhance the thermoelectric figure of merit is a critical new requirement. Here, we demonstrate that a ZT of ~1.0 over a broad temperature range is possible in p-type 10 nm and 20 nm wide silicon nanowires, a value which is over 100 times higher than that of the bulk silicon. Nevertheless, it is not unreasonable to think that the figure of merit of silicon may be improved even further.

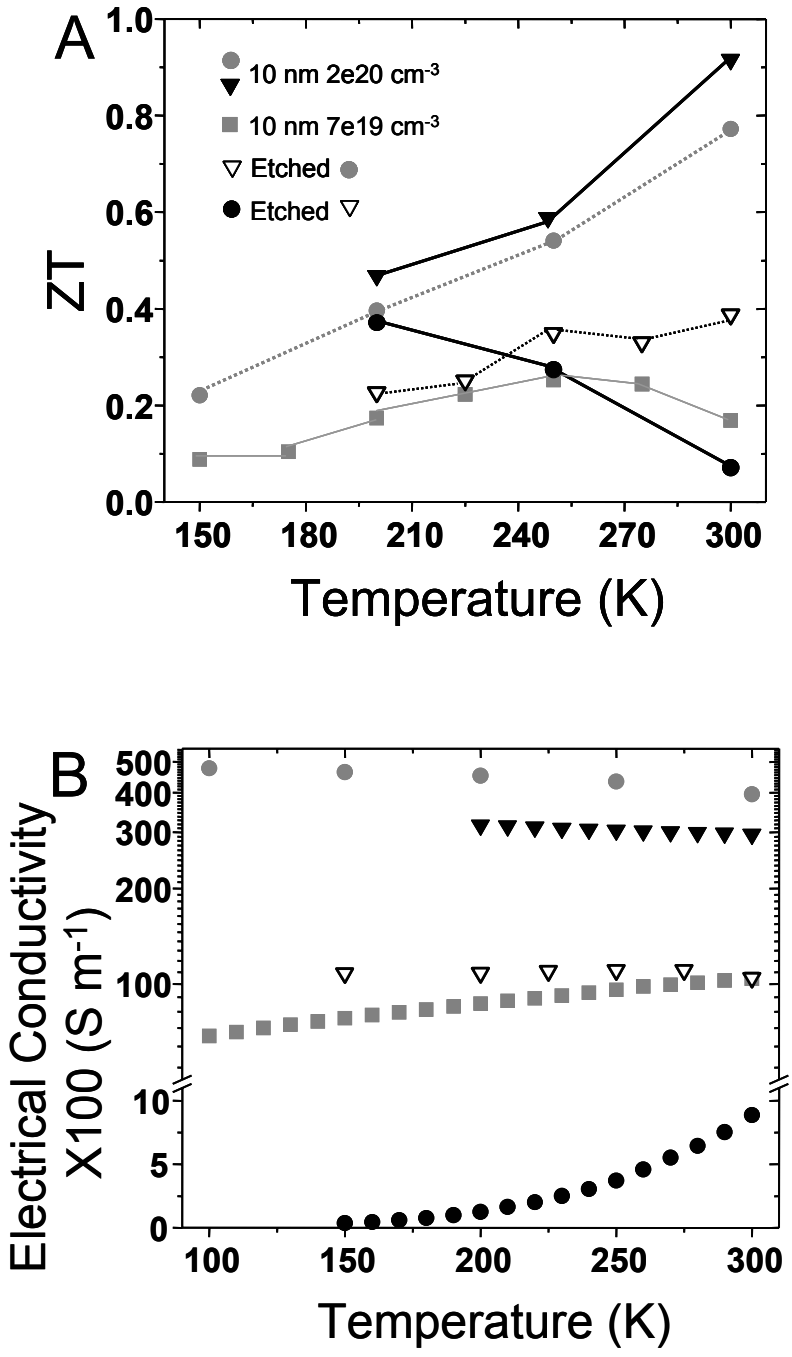


Figure 5.17: A) Measured ZT values of 10 nm SiNWs of different doping. Anisotropic etching of the NWs was done in the RIE using CF_4/He gases (20/30 sccm, 10 mTorr, 40W) for ~40 sec at a time, removing approximately top 3 to 4 nm (Si and B atoms). B) Electrical conductivity of the samples shown in B. Doping below 10^{20} cm^{-3} (or etching degenerately doped SiNWs) is accompanied by the reduction in the electrical conductivity and the emergence of a semiconductor behavior.

Bibliography

1. Mahan, G.; Sales, B.; Sharp, J., Thermoelectric materials: New approaches to an old problem. *Phys. Today* **1997,** 50, (3), 42-47.
2. Chen, G., Nanoscale heat transfer and nanostructured thermoelectrics. *IEEE Trans. Comp. Pack. Technol.* **2006,** 29, (2), 238-246.
3. Lin, Y. M.; Dresselhaus, M. S., Thermoelectric properties of superlattice nanowires. *Phys. Rev. B* **2003,** 68, (7).
4. Chen, G.; Dresselhaus, M. S.; Dresselhaus, G.; Fleurial, J. P.; Caillat, T., Recent developments in thermoelectric materials. *Int. Mater. Rev.* **2003,** 48, (1), 45-66.
5. Majumdar, A., Thermoelectricity in semiconductor nanostructures. *Science* **2004,** 303, (5659), 777-778.
6. Kim, W.; Wang, R.; Majumdar, A., Nanostructuring expands thermal limits. *Nano Today* **2007,** 2, (1), 40-47.
7. MacDonald, D. K. C., *Thermoelectricity: An Introduction to the Principles.* New York: Dover, 2006.
8. Ashcroft, N. W.; Mermin N. D., *Solid State Physics*. Saunders College Fort Worth, TX, 1976.
9. Weber, L.; Gmelin, E., Transport Properties of Silicon. *Appl. Phys. A* **1991,** 53, (2), 136-140.
10. Humphrey, T. E.; Linke, H., Reversible Thermoelectric Nanomaterials. *Phys. Rev. Lett.* **2005,** 94, (9), 096601.
11. Hicks, L. D.; Harman, T. C.; Dresselhaus, M. S., Use of quantum-well superlattices to obtain a high figure of merit from nonconventional thermoelectric materials. *Appl. Phys. Lett.* **1993,** 63, (23), 3230-3232.
12. Hicks, L. D.; Dresselhaus, M. S., Effect of quantum-well structures on the thermoelectric figure of merit. *Phys. Rev. B* **1993,** 47, (19), 12727-12731.
13. Hicks, L. D.; Dresselhaus, M. S., Thermoelectric figure of merit of a one-dimensional conductor. *Phys. Rev. B* **1993,** 47, (24), 16631-16634.
14. Small, J. P.; Perez, K. M.; Kim, P., Modulation of thermoelectric power of individual carbon nanotubes. *Phys. Rev. Lett.* **2003,** 91, (25).
15. Venkatasubramanian, R.; Siivola, E.; Colpitts, T.; O'Quinn, B., Thin-film thermoelectric devices with high room-temperature figures of merit. *Nature* **2001,** 413, (6856), 597-602.
16. Li, D.; Wu, Y.; Kim, P.; Shi, L.; Yang, P.; Majumdar, A., Thermal conductivity of individual silicon nanowires. *Appl. Phys. Lett.* **2003,** 83, (14), 2934-2936.
17. Harman, T. C.; Taylor, P. J.; Walsh, M. P.; LaForge, B. E., Quantum dot superlattice thermoelectric materials and devices. *Science* **2002,** 297, (5590), 2229-2232.
18. Hsu, K. F.; Loo, S.; Guo, F.; Chen, W.; Dyck, J. S.; Uher, C.; Hogan, T.; Polychroniadis, E. K.; Kanatzidis, M. G., Cubic AgPbmSbTe2+m: Bulk thermoelectric materials with high figure of merit. *Science* **2004,** 303, (5659), 818-821.
19. Liu, W.; Asheghi, M., Phonon-boundary scattering in ultrathin single-crystal silicon layers. *Appl. Phys. Lett.* **2004,** 84, (19), 3819-3821.

20. Ju, Y. S., Phonon heat transport in silicon nanostructures. *Appl. Phys. Lett.* **2005,** 87, (15), 153106.
21. Yang, P. D., The chemistry and physics of semiconductor nanowires. *MRS Bulletin* **2005,** 30, (2), 85-91.
22. Melosh, N. A.; Boukai, A.; Diana, F.; Gerardot, B.; Badolato, A.; Petroff, P. M.; Heath, J. R., Ultrahigh-density nanowire lattices and circuits. *Science* **2003,** 300, (5616), 112-115.
23. Herring, C., Theory of the thermoelectric power of semiconductors. *Phys. Rev.* **1954,** 96, (5), 1163.
24. Small, J. P.; Shi, L.; Kim, P., Mesoscopic thermal and thermoelectric measurements of individual carbon nanotubes. *Solid State Commun.* **2003,** 127, (2), 181-186.
25. Shi, L.; Li, D. Y.; Yu, C. H.; Jang, W. Y.; Kim, D. Y.; Yao, Z.; Kim, P; Majumdar, A, Measuring thermal and thermoelectric properties of one-dimensional nanostructures using a microfabricated device. *J. Heat Transfer* **2003,** 125, (5), 881-888.
26. Frederikse, H. P. R., Thermoelectric power of germanium below room temperature. *Phys. Rev.* **1953,** 92, (2), 248-252.
27. Jacobsen, R. S.; Andersen, K. N.; Borel, P. I.; Fage-Pedersen, J.; Frandsen, L. H.; Hansen, O.; Kristensen, M.; Lavrinenko, A. V.; Moulin, G.; Ou, H.; Peucheret, C.; Zsigri, B. t.; Bjarklev, A., Strained silicon as a new electro-optic material. *Nature* **2006,** 441, (7090), 199-202.
28. Khitun, A.; Balandin, A.; Wang, K. L., Modification of the lattice thermal conductivity in silicon quantum wires due to spatial confinement of acoustic phonons. *Superlatt. Microstruct.* **1999,** 26, (3), 181-193.
29. Zou, J.; Balandin, A., Phonon heat conduction in a semiconductor nanowire. *J. Appl. Phys.* **2001,** 89, (5), 2932-2938.
30. Volz, S. G.; Chen, G., Molecular dynamics simulation of thermal conductivity of silicon nanowires. *Appl. Phys. Lett.* **1999,** 75, (14), 2056-2058.