CALT 68-xxxx
DOE Research and
Development Report

Waveguide Packaging of Quasi-Optical Grid Amplifiers

Thesis by

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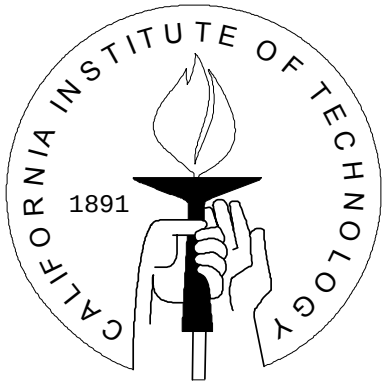
In Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy



California Institute of Technology

Pasadena, California

2003

(Submitted March 27, 2003)

March 27, 2003

Acknowledgements

First, I would like to thank my advisor, Professor David Rutledge, for providing me the opportunity to be a part of MMIC research group. His support, guidance and advice have made this thesis possible.

I would like to thank Jon Hacker at Rockwell Scientific and Roger Tsai at Northrop Grumman Space Technology for the fabricating and testing efforts of the Ka-band, V-band and W-band grid amplifiers.

I would especially like to thank Jeff Liu for his advice and support for my early research work. His guidance gradually led me into a better understanding of microwave and milli-meter wave. I also wish to thank Blythe Deckman for teaching me a lot of measurement and calibration skills as well as sharing with me numerous amounts of hilarious jokes. Unfortunately, I usually played the role as Vulcan. I am also indebted to Mike DeLisio and Jim Rosenberg for the fruitful discussions and precious involvement of the V-band and W-band grid amplifier designs. Many thanks also go to Ali Hajimiri for his suggestions and interesting conversations.

I am glad to have had the opportunity of working with many talented people in MMIC and CHIC group Ű Kent Potter, John Davis, Polly Preventza, Ichiro Aoki, Scott Kee, Masashi Nakatsugawa, Hui Wu, Donhee Ham, Hossein Hashemi, Dai Lu, Milan Kovacevic, Matthew Morgan, Feiyu Wang and Min Park. To the newer members of the MMIC group, Sanggeun Jeon and Patrick Cesarano, I wish them all the best. In addition, I wish to express my gratitude to visitors to the MMIC group, including Taavi Hirvonen, Kazuhiro Uehara, Shigeo Kawasaki and Toshihisa Kamei. Through our discussions, we not only shared technical and academic experience, but also our cultural and philosophical difference, which widen my eyes.

March 27, 2003

I would also like to take this opportunity to thank my friends here at Caltech as well as those overseas, including NGF (It is not a person's name), Patricia Fan, Suky Chow, mitochAndrea, Victor Po, Johnny Chong, Donald Sze, Chris Lee, Daniel Katz, Father Andrew, Leo Wong, Philip Hui and all the ACians. Their sincere friendship, spiritual sharing and technical discussions helped me through the difficult times in my studies and research.

I would like to thank my parents and sister for their unconditional support and love. Without their understanding and help, this endeavor would not be possible. Finally, I would like to especially thank Jesus Christ for he walked with me through this and numerous other journeys of life. His grace and passion guided me through my difficult times and granted me hopes.

March 27, 2003

The small things he was meant to do were important, somehow, in the big scheme of things

—Dragonlance Chronicles Volume 1

March 27, 2003

Abstract

Quasi-optical amplifiers combining the output powers of hundreds of transistors have demonstrated the capability to deliver more than 10 Watts of power at millimeter wave frequencies. However, these amplifiers are large and expensive to manufacture. In this work, we attempt to find a compact, low-cost approach using metallic waveguide to package a grid amplifier. This thesis details the design and implementation of a grid amplifier packaged in waveguide. Frequency and time-domain simulation methods are used to calculate the field flatness and the small signal gain of the amplifier. Four different active grids packaged in waveguide will be reported. The first grid, operating at Ka-band, is fed with a waveguide and radiates its output into free space. The amplifier chip design was previously measured in free-space. This work demonstrates a small signal gain of 7 dB with output power of 5.5 W at 3-dB compression. The performance is similar to the same grid design measured in free-space. A second Ka-band grid amplifier packaged in waveguide for both input and output gives a small signal gain of 6 dB. The 3-dB compressed output power is 670 mW while the same amplifier measured in free-space gave 1.2 W output power. In order to further verify our active grid and packaging design methods, a V-band single-stage monolithic grid amplifier was designed and fabricated. A transmission grid amplifier and a reflection grid amplifier using this chip were fabricated. Both amplifiers have 2 dB small-signal gain at 58 GHz. In order to increase small-signal gain, a two-stage monolithic grid amplifier was designed and fabricated. A reflection approach was used to package this chip. Measured small-signal gain was 2.7 dB at 82 GHz.

Contents

Chapter 1

Introduction

Traditionally, vacuum devices such as traveling wave tubes (TWT) and klystron amplifiers have been the mainstream high-power microwave amplifiers. Although recent advances in solid-state devices such as pseudomorphic-HEMT and HBT have improved performance, the low output power of a single transistor device limits the use of microwave monolithic integrated circuits (MMIC) to low power, low noise applications only. Furthermore, planar corporate power-combining using printed transmission lines has been shown by York [1] to have a theoretical combining limit when the transmission lines are lossy.

Quasi-optical power combining, a technique that combines the output powers of many solid-state devices in free-space has first proposed by Mink [2]. The combined output powers can either form a radiating beam, or can be collected into a waveguide. Active devices with hybrid or monolithic designs such as mixers [3], oscillators [4], and amplifiers [5-7] have been demonstrated. New figures-of-merit [8], modeling methods [9], measurement techniques [10] and diagnostic techniques [11] for quasi-optical arrays have been proposed and demonstrated as well. Recently, Deckman *et al.* [7] reported a 5 W, Ka-band monolithic grid amplifier with chip area of 1 cm square. The result shows the possibility of building low cost, compact, high-power, solid-state amplifiers suitable for applications such as satellite communications and wireless local-area networks (WLAN).

1.1 Motivation

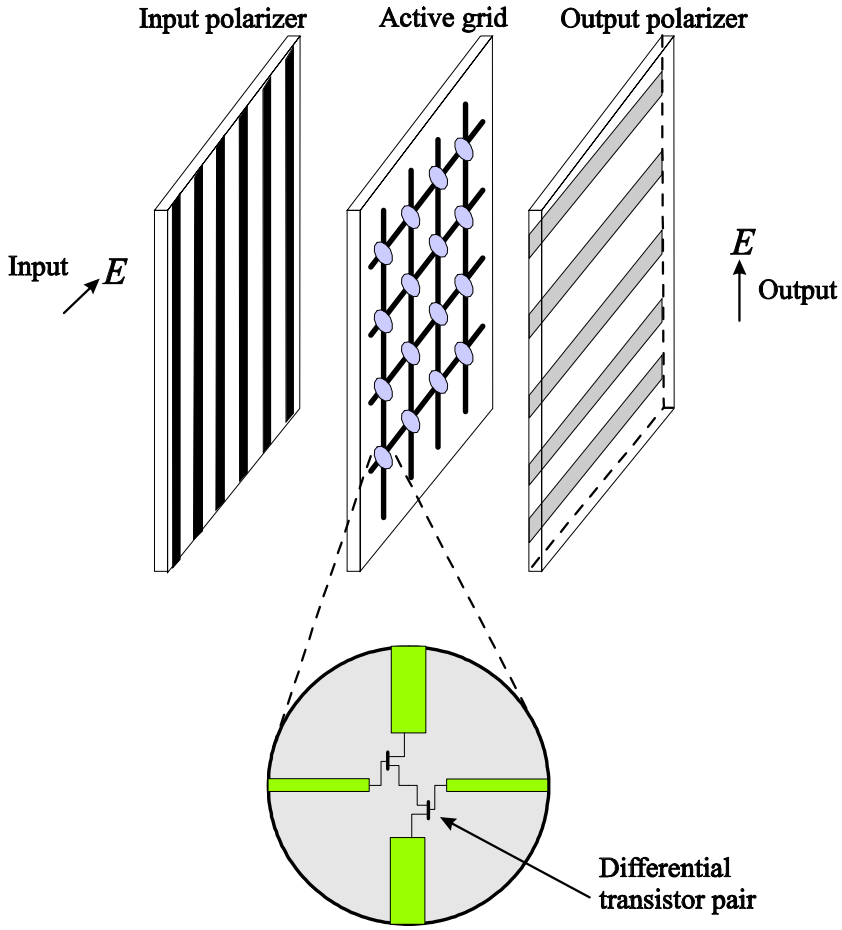


Figure 1.1: A general layout for active grids. The input and output beams are cross-polarized to provide isolation. Each unit cell consists of one or more differential transistor pairs as amplification stages.

This thesis is focused on using metallic waveguide to package a monolithic active amplifier that results in a low cost, compact design. The general layout of a quasi-optical active grid that we use in the following demonstration of amplifier packaging is as shown in Figure 1.1. It consists of the active grid, the input polarizer and the output polarizer. Usually both polarizers are patterned metallization fabricated on a dielectric. They are used as back-shorts for one of the polarizations while allowing the other polarization to penetrate through. The amplifier can be either a monolithic

chip or a hybrid amplifier. A thermal spreader may be mounted with the amplifier to remove heat. Deckman *et al.* [7] demonstrated a grid amplifier illuminated in free-space with a focused beam with 5 W output power at 37 GHz (Figure 1.2). The free-space measurement was carried out in a Gaussian focused-beam system that provides excellent phase and amplitude distributions but requires very large lenses. Furthermore, as discussed in [10], this measurement requires careful calibration due to scattering radiations from surrounding features such as bias lines, bypass capacitors or ferrite beads. Therefore, a closed, compact and low cost method is necessary for packaging grid amplifiers. In order to illuminate a grid amplifier in a closed environment, researchers have tried various techniques. In [6] and [12], tapered-waveguide feeds, of length 230 mm and 75 mm, respectively, excited the amplifiers. However, these tapered feeds are long, and in [12], there were rapid gain fluctuations across frequency because of multiple reflections of higher-order modes along the long taper. Ortiz *et al.* [5] successfully demonstrated a hard-wall waveguide horn to feed a hybrid spatial-power-combining amplifier with 10-dB gain at 25-W output power. Kim *et al.* [13] proposed an ingenious feed using a TEM waveguide with photonic-crystal walls, but this has not yet been demonstrated with an amplifier.

Our approach uses standard metal waveguide as the input and output and waveguide steps to expand the standard metal waveguide into over-moded waveguide to feed the active grid. Metal waveguide is low in cost, easy to manufacture and good in thermal conductivity. Furthermore, it provides a rugged mechanical support for the active grid and the DC-bias circuitry. The use of waveguide steps reduces length and avoids the generation of ripples across frequency due to high-Q multiple reflections along a lengthy over-moded waveguide. The over-moded waveguide walls were not loaded with dielectric to avoid the manufacturing and assembly difficulty and relax the required machining tolerance.

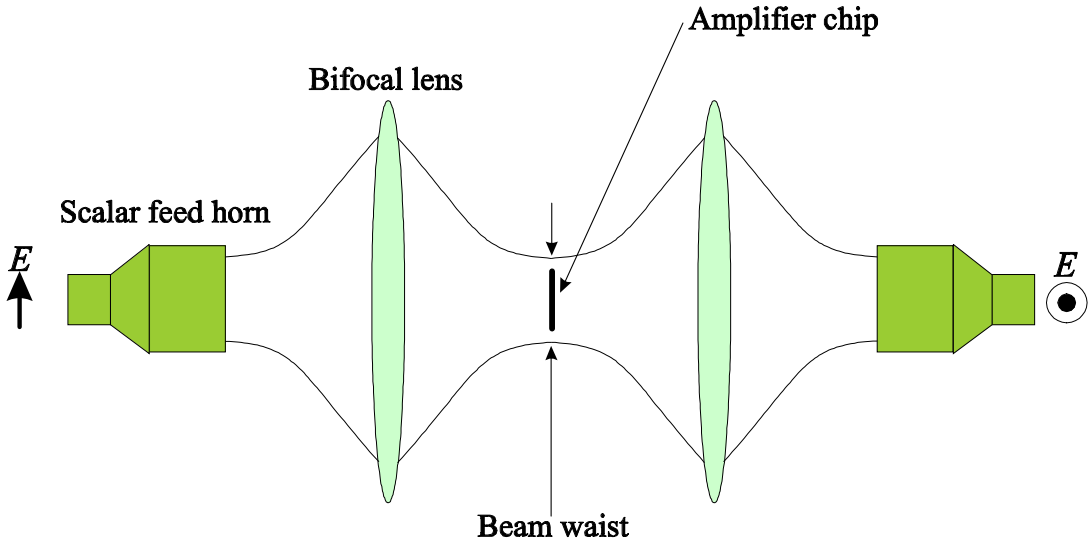


Figure 1.2: Drawing of a quasi-optical measurement setup. The scalar feed horn generates a Gaussian beam that is focused onto the amplifier chip. The beam waist can be adjusted by the distance between the scalar feed horns and the lenses.

1.2 Thesis Organization

We will first discuss the general simulation and modeling issues of a grid amplifier packaged in waveguide in the next chapter. Two simulation methods will be discussed. The first method, based on passive electromagnetic simulation, calculates the input and output return losses with the amplifier replaced by an impedance sheet. The second method uses anisotropic material to simulate the 2-port amplifier scattering parameters. This method computes both reflection and transmission scattering parameters and takes into account the variation of impedance across the grid amplifier aperture. In order to use the second simulation design approach, we wrote a finite-difference time-domain (FDTD) code that allows us to use non-reciprocal anisotropic material. To further resolve the numerical stability problem with FDTD, we derived the FDSS simulation that provides unconditionally stable electromagnetic simulation with anisotropic material.

Chapter 3 details the design, construction and measurement of a passive mode converter and two waveguide packaged grid amplifiers at Ka-band (Figure 1.3). The

design of the chip was the same as reported in [7] and was fabricated using Rockwell 0.18 μm pHEMT process. One of the amplifiers has its input packaged, while its output radiates and the other is a full-waveguide-packaged amplifier. Experimental results show that the input-packaged grid amplifier gives power, gain and efficiency comparable to that reported using a Gaussian-beam feed [7]. The fully waveguide packaged grid amplifier has similar small-signal gain but lower output power. Later diagnosis shows that the chip we used may have inherently low output power. Portions of this chapter have been published in [14]-[15].

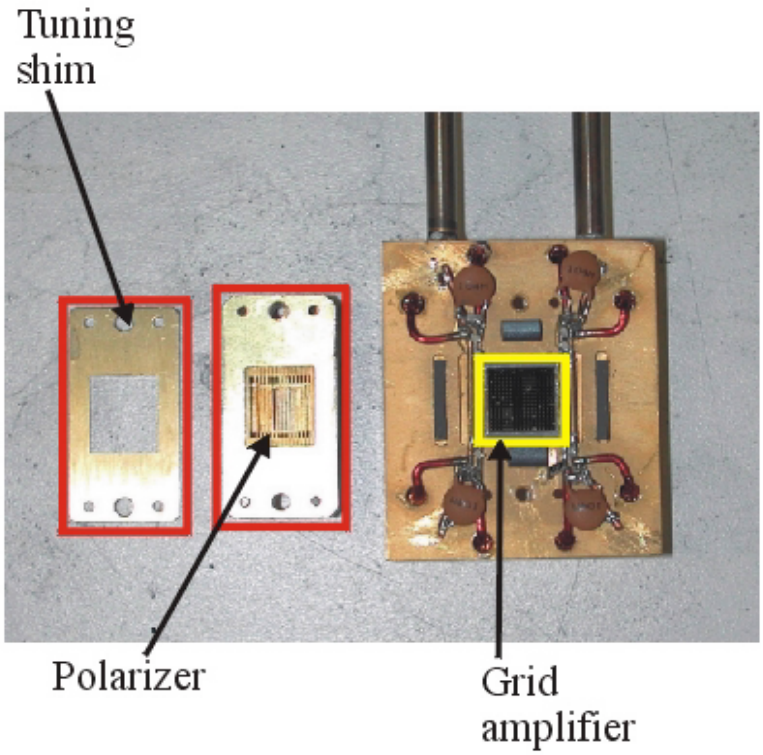


Figure 1.3: The Ka-band grid amplifier with input packaged in waveguide. This amplifier has 7.5 dB small signal gain and 5.4 W output power.

Chapter 4 details the design of a monolithic V-band single-stage grid amplifier chip and the construction and measurement of two packaged amplifiers. The chip was fabricated by TRW using their 0.15 μm InP HEMT process. We studied a transmission grid amplifier and a reflection grid amplifier and showed that both of them

performed similarly (Figure 1.4-1.5). The flange-to-flange system gains for both amplifiers are about 2 dB, which is lower than the simulated gain. It is concluded that the field may not be uniform and a single-stage design does not have enough gain to compensate losses in waveguide and power-combining at this frequency range. This work has been published in [16].

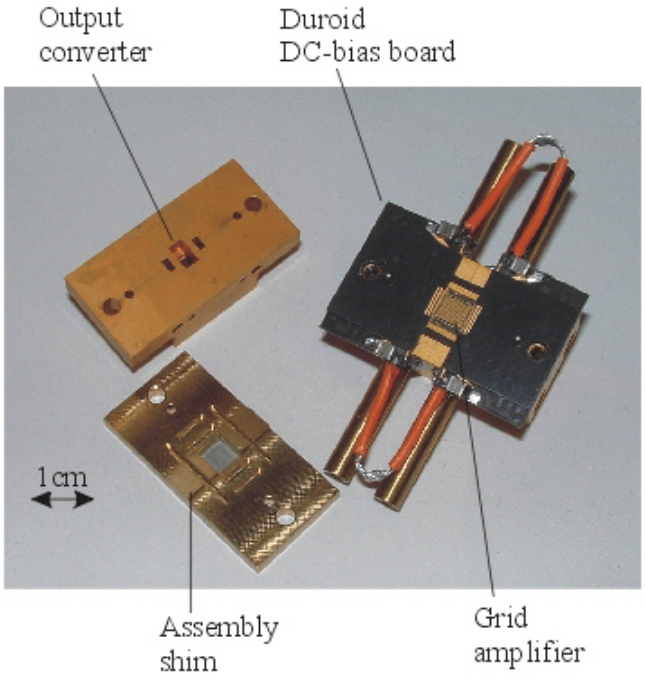


Figure 1.4: The V-band transmission grid amplifier.

Chapter 5 details the design and testing of a monolithic two-stage grid amplifier at W-band using a reflection approach. The amplifier was fabricated with the same process as the V-band chip. This is the first two-stage monolithic grid amplifier that has been packaged in waveguide and tested. The measured small-signal gain is 2.7 dB at 82 GHz. Finally, we will give a conclusion and discuss the possible future developments for improving the simulation and design of grid amplifiers in Chapter 6.

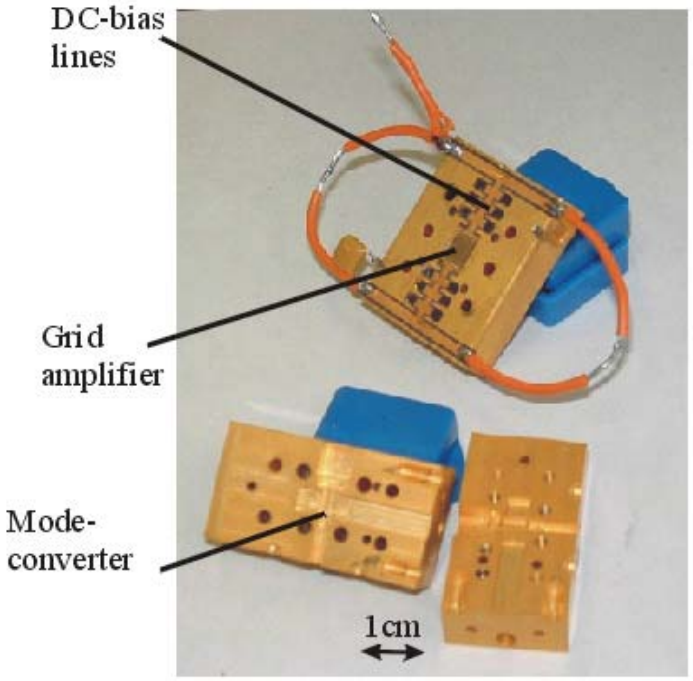


Figure 1.5: The V-band reflection grid amplifier.

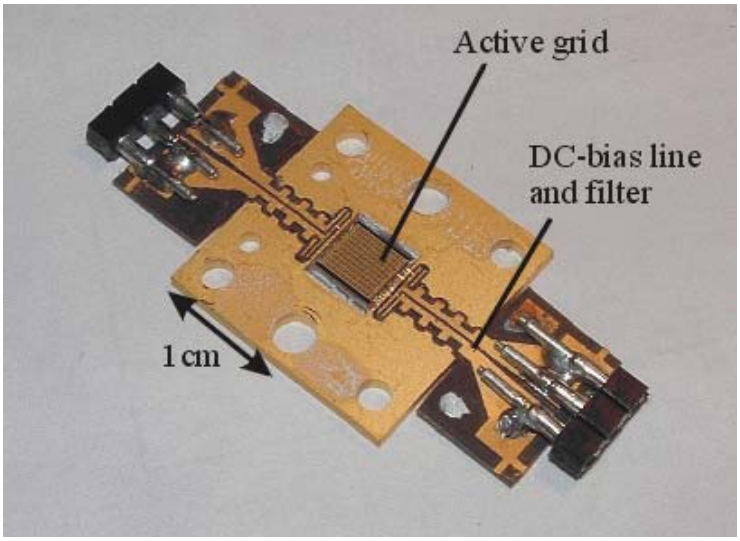


Figure 1.6: A two-stage grid amplifier mounted on an AlN which is attached to the brass over-moded waveguide. The measured small-signal gain is 2.7 dB at 82 GHz.

Reference

[1] R. A. York, "Some Considerations of Optimal Efficiency and Low Noise in Large Power Combiners," *IEEE Trans. Microwave Theory and Tech.*, Aug. 2001, pp. 1477-1482.

[2] J. W. Mink, "Quasi-Optical Power Combining of Solid-State Millimeter-Wave Sources," *IEEE Trans. Microwave Theory Tech.*, vol. 34 pp. 273-279, Feb. 1986.

[3] J. B. Hacker, R. M. Weikle, M. Kim, M. P. DeLisio, D. B. Rutledge, "A 100-Element Planar Schottky Diode Grid Mixer," *IEEE Trans. Microwave Theory Tech.*, Mar 1992, pp. 557-562.

[4] B. Deckman, J. J. Rosenberg, D. Rutledge, E. Sovero, D. S. Deakin, Jr., "A 1-Watt, 38-GHz Monolithic Grid Oscillator," 2001 Int. Microwave Symp. Dig., pp. 1843-1846.

[5] S. Ortiz, J. Hubert, L. Mirth, E. Schlecht, and A. Mortazawi, "A High-Power Ka-Band Quasi-Optical Amplifier Array," *IEEE Trans. Microwave Theory and Tech.*, Feb. 2002, pp. 487-494.

[6] J. J. Sowers, D. J. Pritchard, A. E. White, W. Kong, O.S.A. Tang, D. R. Tanner and K. Jablinskey, "A 36W, V-Band, Solid State Source," 1999 Int. Microwave Symp. Dig., pp. 235-238.

[7] B. Deckman, D. S. Deakin, Jr., E. Sovero, D. Rutledge, "A 5-Watt, 37-GHz Monolithic Grid Amplifier," 2000 Int. Microwave Symp. Dig., pp. 805-808.

[8] M. Gouker, "Toward Standard Figures-of-Merit for Spatial and Quasi-Optical Power-Combined Arrays," *IEEE Trans. Microwave Theory and Tech.*, Jul. 1995, pp. 1614-1617.

[9] P. Preventz, B. Dickman, E. Sovero, M. P. DeLisio, J. J. Rosenberg, D. B. Rutledge, " Modeling of Quasi-Optical Arrays," 1999 Int. Microwave Symp. Dig., pp. 563-566.

[10] B. Deckman, J. J. Rosenberg, D. Rutledge, "Ka-Band Quasi-Optical Measurements using Focused Gaussian Beams," 2001 ARFTG Dig., pp. 43-48.

[11] K. Y. Yang, T. Marshall, M. Forman, J. Hubert, L. Mirth, Z. Popović,L. P. B. Katehi, J. F. Whitaker, "Active-Amplifier-Array Diagnostics Using High-Resolution Electrooptic Field Mapping," *IEEE Trans. Microwave Theory and Tech.*, May 2001, pp. 849-857.

[12] E. A. Sovero, J. B. Hacker, J. A. Higgins, D. S. Deakin, and A. L. Sailer, "A Ka-band Monolithic Quasi-Optic Amplifier," 1998 Int. Microwave Symp. Dig., pp. 1453-1456.

[13] M. Kim, J. B. Hacker, A. L. Sailer, S. Kim, D. Sievenpiper and J. A. Higgins, "A Rectangular TEM Waveguide and Photonic Crystal Walls for Excitation of Quasi-Optical Amplifier," 1999 Int. Microwave Symp. Dig. pp. 543-546.

[14] T. Kamei, C-T Cheung, J. J. Rosenberg, D. B. Rutledge, "Design and Simulation of a Mode Converter for the Excitation of Quasi-optical Amplifiers," 2000 AP-S Symp. Dig.

[15] C-T Cheung, J. B. Hacker, G. Nagy, D. B. Rutledge, "A Waveguide Mode-Converter Feed for a 5-W, 34-GHz Grid Amplifier," 2002 IMS Symp. Dig., pp. 1523-1526.

[16] C-T Cheung, R. Tsai, R. Kagiwada, D. B. Rutledge, "V-band Transmission and Reflection Grid Amplifier Packaged in Waveguide," to be presented in 2003 IMS Symp.

Chapter 2

Design of Packaged Grid Amplifiers

In order to combine the power of hundreds of transistors using quasi-optical power combining, the size of the array is usually larger than the corresponding standard waveguide dimensions and the metallic waveguide that holds the grid becomes over-moded. A converter is required to couple the selected waveguide modes from the over-moded waveguide to a standard waveguide while avoiding excitation of unwanted modes. The use of such a mode converter has been reported in designing vacuum devices [1] and corrugated horns [2]. Our goal is to have the selected modes weighted in magnitude and aligned in phase to give maximum field flatness over the aperture of the active grid.

Waveguide steps take less space than long tapers and are easily programmed in optimization. In addition, short steps avoid multiple reflections of out-of-band frequencies by keeping a small distance between the active grid and standard waveguide. The design of a package starts with a passive mode converter design that would be used as an initial guess for the optimization with the active grid.

2.1 Passive Mode Converter

A drawing of the passive mode converter is shown in Figure 2.1. The number of waveguide sections to be used, in general, is determined by the number of higher-

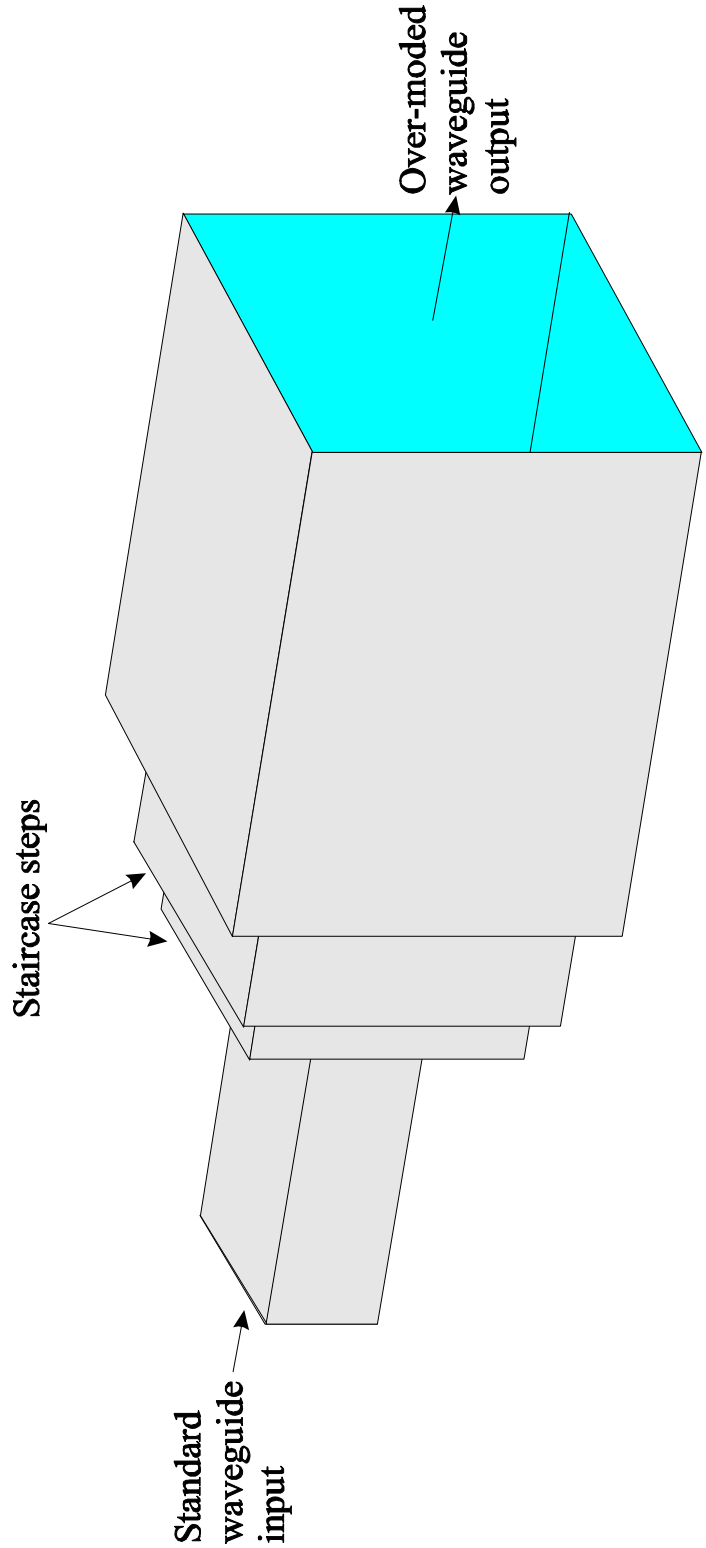


Figure 2.1: A passive mode converter with standard waveguide input and over-moded waveguide output. Rectangular waveguide step dimensions are found by optimization. The optimized dimensions for this example are included in Appendix B.

order modes that need to be incorporated in the optimization. For the aperture size of the active grid in Deckman *et al.* [3], TE_{30} is the only higher-order mode we may exploit to enhance field-uniformity with air-filled waveguide. The error function we used for minimization is

$$err = |S_{11}|^2 + \left(\frac{|S_{21TE30}|}{|S_{21TE10}|} - \alpha \right)^2 + \sum_{higher\ order} |S_{21TE}|^2 + \sum_{all\ modes} |S_{21TM}|^2 \qquad (2.1)$$

where α is set such that the field ratio results in a 2-dB ripple in the H-plane at equal phase planes across 70 % of the waveguide width. The particular fabricated and measured passive mode converter in Chapter 4 has α equal to 0.28. Since the two travelling modes have different phase velocities, the specified spatial distribution only occurs when the phases are equal. The distance between successive equal phase planes is given by

$$L = \left(\lambda_{TE10}^{-1} - \lambda_{TE30}^{-1} \right)^{-1} \qquad (2.2)$$

where λ_{mn} is the wavelength along the guide of the mn-mode. Figure 2.2 shows the optimization program flow chart of the passive mode converter. The field simulation was done at one or several frequencies using Ansoft's High Frequency Structure Simulator (HFSS) and the optimization update algorithm was obtained from Matlab. Typically, 200 to 500 steps are needed to have *err* converge to less than $1\text{x}10^{-3}$.

Figure 2.3 shows the H-plane and E-plane electric field distributions of a two-step waveguide. The H-plane field distribution shows that the field uniformity only appears at specific planes and repeats along the waveguide. The E-plane distribution in the over-moded waveguide is uniform, which shows that higher-order modes such as TM_{12} are not excited. However, one should note that any discontinuity in either the E-plane or the H-plane will immediately excite these unwanted higher-order modes. Therefore, it will be necessary to include the effect of the edge of an active array and to compensate or suppress unwanted higher-order mode excitation.

This port-to-port passive mode converter was fabricated and measured for verification of proper mode excitation in Chapter 3. The drawings of the optimized passive

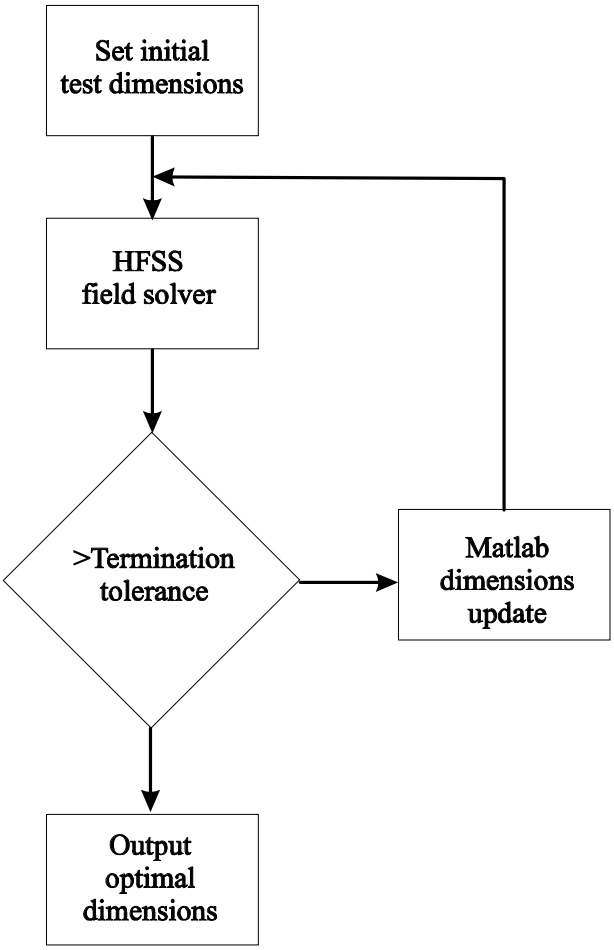


Figure 2.2: The flowchart for the optimization algorithm used in designing the passive mode-converter. Dimension updates include the change in heights and widths of waveguide steps.

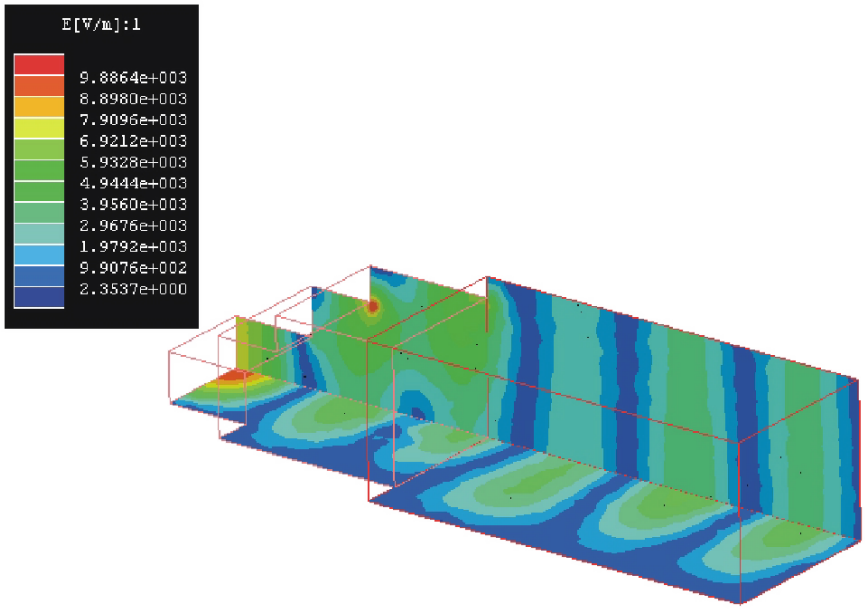


Figure 2.3: The HFSS simulated electric field magnitude distribution of the mode converter. The mode converter expands a WR-28 waveguide into a 10 mm×13 mm over-moded waveguide. The uniform E-plane field distribution indicates that undesirable higher-order modes such as TE_{12} are not excited.

mode converter are included in Appendix B. It is because of the successful demonstration of the agreement between measured and simulated field distribution and small signal s-parameters that we may proceed to design the mode-converter-fed-grid amplifier.

2.2 Active Mode Converter

The passive mode converter from the previous section is used as an initial guess for the active mode converter optimization. Initial values of dielectric constants and thicknesses of tuning slugs and polarizers can be obtained from circuit simulation with ideal transmission lines. Electrical lengths and characteristic impedances of ideal transmission lines are calculated using the fundamental mode propagation constant in the over-moded waveguide. Figures 2.4 and 2.5 show two different quarter-views of the grid simulation drawing in HFSS. The difference is that in the first drawing, output power radiates into free-space while in the second drawing the output power is collected by a similar mode converter into a waveguide flange. In both cases, the goal is to minimize the input or output return loss and the field non-uniformity across the grid.

As mentioned in the previous section, the active grid may not cover the entire waveguide aperture. In fact, this is more desirable because waveguide walls impose a boundary condition on all parallel electric fields such that they must be zero on the walls. Therefore, there exists no solution to excite a transistor which lies along the edge of the wall for any mode combinations within the over-moded waveguide. Thus we need a field uniformity criterion over the grid aperture. Kim *et al.* [4] proposed to use Field Flatness Efficiency (FFE) that is defined as

$$FFE = \frac{1}{a}\int_0^a \left[\frac{E_y(x)}{E_{\max}}\right]^2 dx \tag{2.3}$$

It is the sum of the power deviation from its peak value E_{max} integrated over the width of the guide a. However, we found that when we discretize and apply this

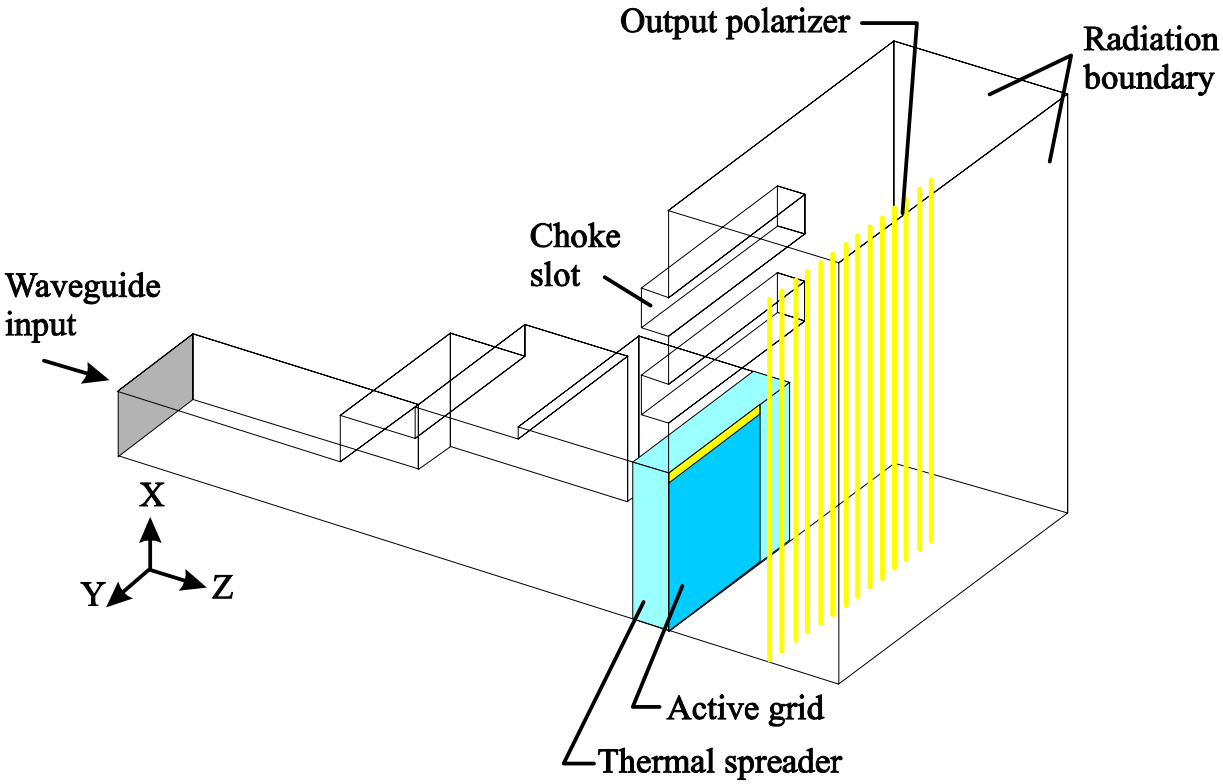


Figure 2.4: A quarter-view of HFSS simulation of a 35 GHz active grid fed by a mode converter from a WR-28 waveguide input. Output power radiates into free-space. Thermal spreader and polarizers have been incorporated for proper modelling. Choke slots are used to prevent RF current leaks from the side.

equation to the field simulation results, sometimes the edge discontinuity around the grid aperture gives rise to an enormously large peak over a very small region. The value of FFE fluctuates severely even with minor dimension modifications and can not show the flatness in the rest of the region. Hence we use the equation of variance for the electric field magnitude and phase. Assuming that the incident fundamental mode electric field is polarized along the x-axis, the computation of magnitude and

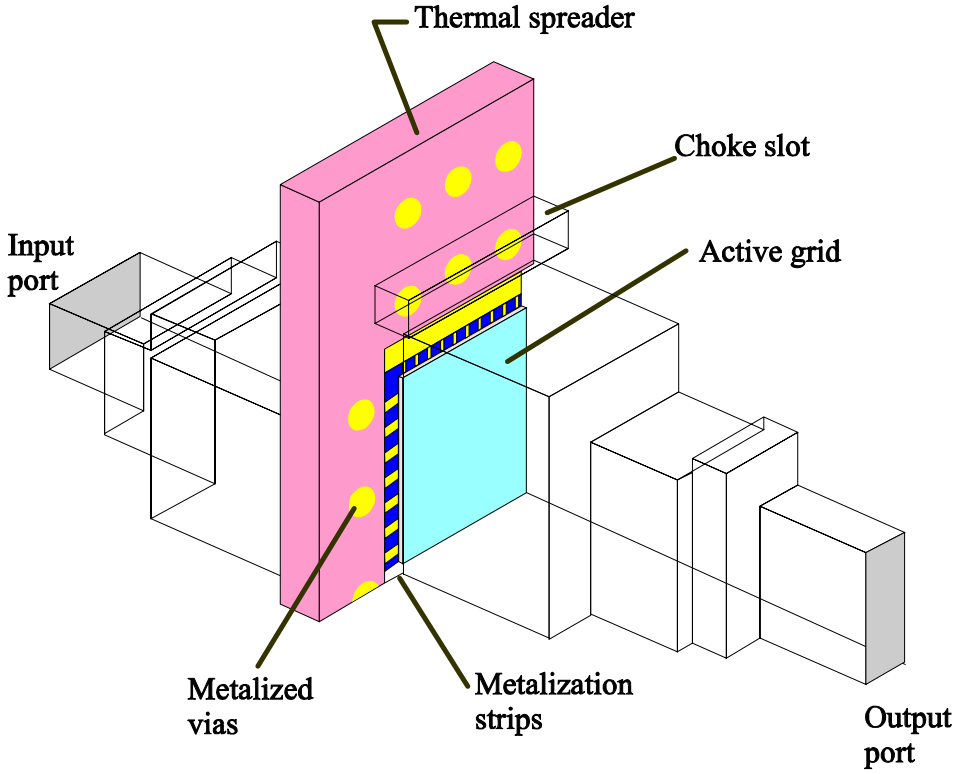


Figure 2.5: A quarter-view of a complete waveguide fed 35 GHz active grid design. Input and output are standard WR-28 waveguide. Metalized vias and choke slots are used to stop RF leakage. DC-bias circuitry is sandwiched between the thermal spreader. The metalization strips help flatten the field distribution for one of the polarizations by providing RF current continuity while the counterpart passes through without intervention.

phase non-uniformity over the aperture is

$$\sigma_{mag} = \frac{\frac{1}{xy}\int\int |E_x(x,y)|^2\, dxdy - \left[\frac{1}{xy}\int_0^x\int_0^y |E_x(x,y)|\, dxdy\right]^2}{\left[\frac{1}{xy}\int_0^x\int_0^y |E_x(x,y)|\, dxdy\right]^2} \tag{2.4a}$$

$$\sigma_{phase} = \frac{1}{xy}\int_0^x\int_0^y \theta(x,y)^2\, dxdy - \left[\frac{1}{xy}\int_0^x\int_0^y \theta(x,y)\, dxdy\right]^2 \tag{2.4b}$$

where x and y are the height and width of the grid aperture. σ_{mag} gives the variance of the field across the aperture with the mean field magnitude normalized to unity. σ_{phase} is not normalized because the average of the phase can be close to zero. This does not impose a problem because a deviation of $\pm 10^\circ$ about 0° or 90° has the same

meaning as opposed to the case with magnitude. Furthermore, $\theta(x,y)$ is the phase of the distribution in radians which means that σ_{phase} is less intuitive to read. A more intuitive parameter for understanding the phase non-uniformity is

$$std(\theta(x,y)) = \frac{180^\circ \times \sqrt{\sigma_{phase}}}{\pi} \tag{2.5}$$

which is the standard deviation of phase in degrees. However, the branch cut of phase that has a jump at 180° causes error in 2.4b or 2.5 when they are applied to the field data. Another similar quantity that is less intuitive but requires only one value to represent field non-uniformity and avoid the branch cut problem is

$$\sigma_{\text{complex}} = \frac{\begin{array}{c}\frac{1}{xy}\int_0^x\int_0^y \{\text{Re}[E_x(x,y)]\}^2 dxdy - \left\{\frac{1}{xy}\int_0^x\int_0^y \{\text{Re}[E_x(x,y)]\} dxdy\right\}^2 \\ +\frac{1}{xy}\int_0^x\int_0^y \{\text{Im}[E_x(x,y)]\}^2 dxdy - \left\{\frac{1}{xy}\int_0^x\int_0^y \{\text{Im}[E_x(x,y)]\} dxdy\right\}^2\end{array}}{\left[\frac{1}{xy}\int_0^x\int_0^y |E_x(x,y)| dxdy\right]^2}$$

where Re[E] and Im[E] are real and imaginary parts of the complex field distribution E. With the definition of field non-uniformity of 2.4a and 2.4b, the new minimization equation becomes

$$err = |S11|^2 + |S22|^2 + \sigma_{mag}^{input} + \sigma_{phase}^{input} + \sigma_{mag}^{output} + \sigma_{phase}^{output} \tag{2.6}$$

Note that low input and output reflection may be obtained by additional matching in standard waveguide that sometimes relaxes the competing constrains between reflection coefficients and field uniformity at the expense of bandwidth reduction.

Since the active grid is large, details of the array cannot be put into HFSS. An equivalent input or output impedance sheet is placed at the location to imitate the loading of the amplifier. In order to obtain the impedance values of a single unit cell, we used the method suggested by Preventza *et al.* [5], which we briefly describe here. The method starts by assuming that our single unit cell topology is as shown in Figure 2.6 and 2.7. The unit-cell is one of the elements of an infinitely extending grid amplifier. Then depending on the field's polarization, we assign E(Dirichlet) or

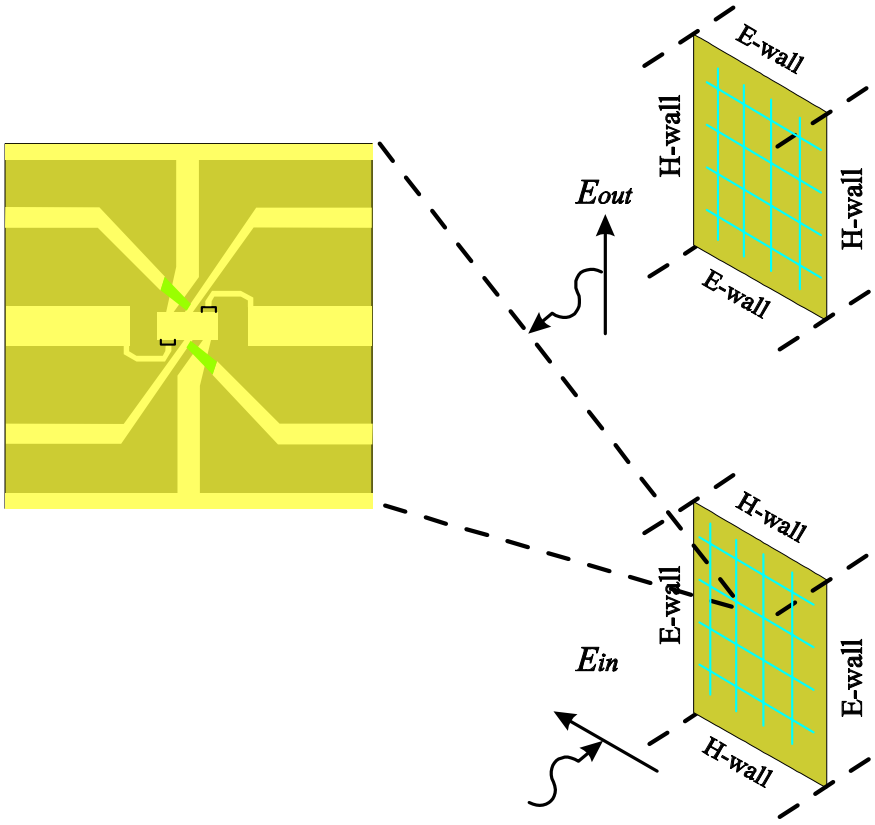


Figure 2.6: The general unit cell layout in a periodic active grid. Depending on the field polarization, we apply different boundary conditions for HFSS simulation.

H(Neumann) boundaries to the edges of the unit cell. The self and mutual inductances are calculated as shown in Figure 2.7. We use the lumped element equivalent circuit in Agilent's Advanced Design System (ADS) with a stabilized transistor to simulate the unit cell. The transistor is made unconditionally stable ($K > 1, |\Delta| < 1$, [6]) by drain-gate feedback. The combined ADS half unit-cell equivalent circuit without input and output tuning is shown in Figure 2.8, and impedance values are obtained with conjugate matching. As shown in Figure 1.1 and 2.6, one unit cell consists of two transistors connected differentially. On the other hand, the equivalent circuit in ADS simulates only one of the two transistors (Figure 2.8), therefore it should be noted that the conjugate matching impedance values in the ADS simulation are equal to one half of the unit cell conjugate matching impedance. Finally, bias circuitry and choke slots have to be included to prevent parallel plate mode leakage into the ther-

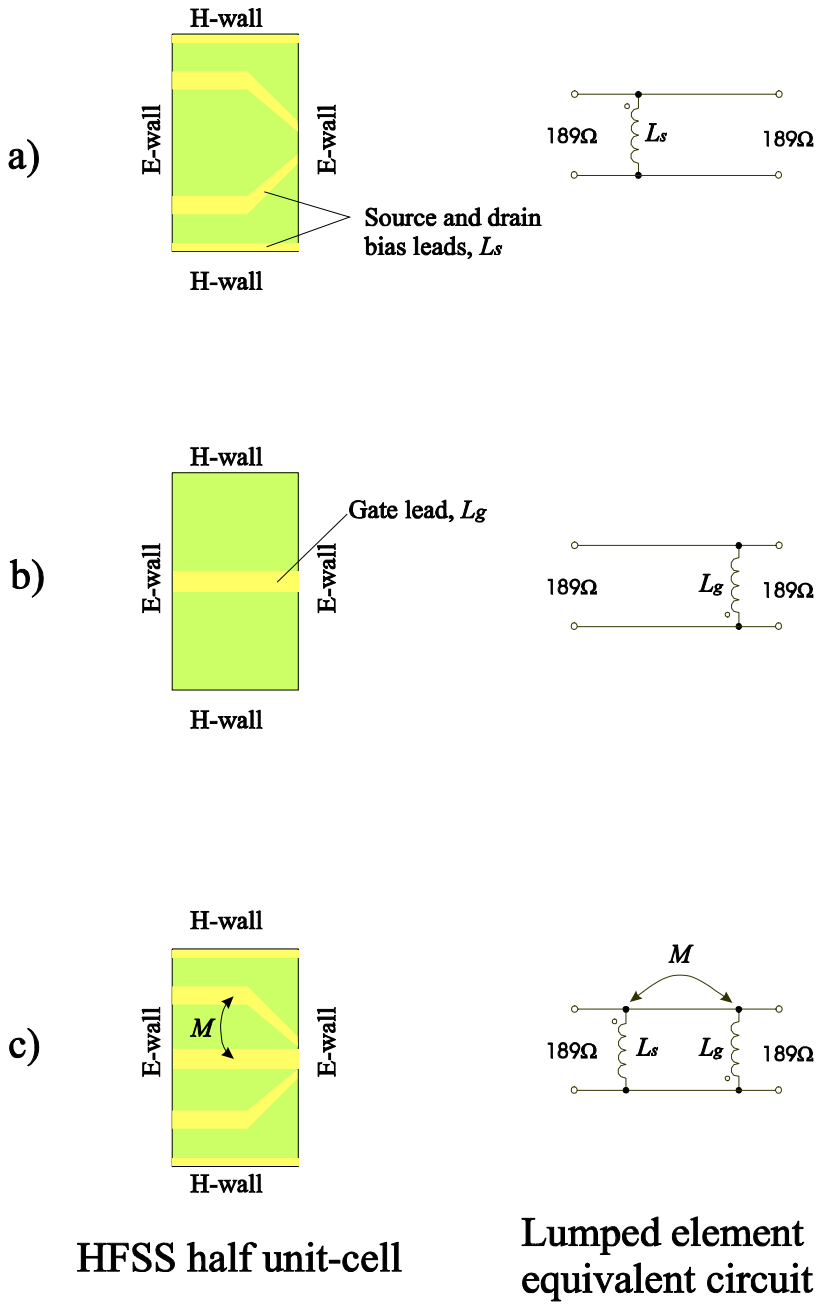


Figure 2.7: An example of HFSS simulations and equivalent circuits for a) source and drain bias lead, L_s, b) gate lead inductance, L_g, and c) overall inductance. Mutual inductance, M, can be found from the total inductance of the equivalent circuit.

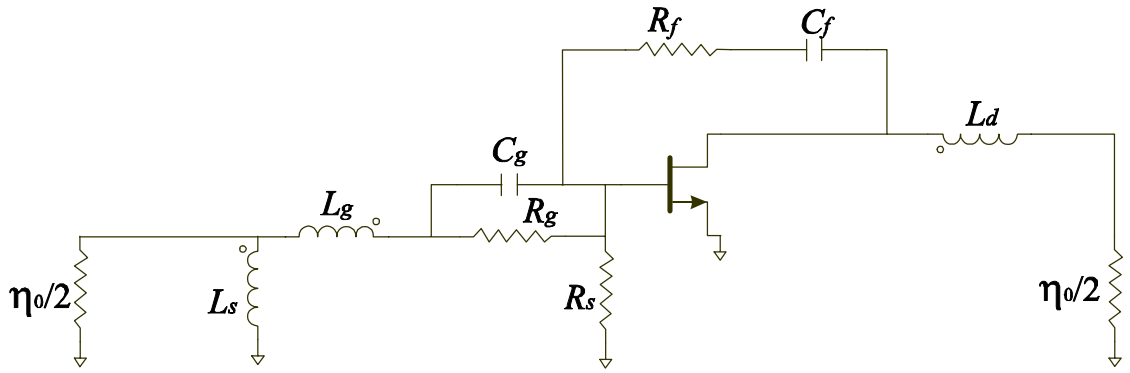


Figure 2.8: The half unit-cell equivalent circuit in ADS for unit-cell amplifier modeling. It should be noted that, due to symmetry of the differential pair, the actual output impedance of the full uni-cell is doubled.

mal spreader or bias striplines. These features are usually evaluated after the first few rounds of optimization to reduce the complexity of the model and increase the speed of convergence. Furthermore, evaluation of field uniformity around adjacent frequencies helps identify the sensitivity of the circuit and sometimes speeds up the optimization.

Figures 2.9 and 2.10 shows the magnitude and phase electric field distribution, E_x, over the grid aperture for the waveguide-fed input, radiating output active grid as shown in Figure 2.4 with output side polarizers modelled as metal strips. Since the dielectric constant of AlN is 8.6, higher-order modes such as TE_{50} and TE_{70} may be excited due to the presence of the edge of the grid. The calculated σ_{mag} and σ_{phase} are 0.0083 and 0.0085, respectively. The output field distribution of this model was not simulated due to the difficulty of constructing the proper incident field from the output. On the other hand, the full waveguide packaged grid in Figure 2.5 can be simulated for both input and output and the results are shown in Figures 2.11 to 2.14 for both magnitude and phase distributions. In both models, because of the limitations of HFSS, the overall system gain from flange-to-flange can be estimated only with circuit simulation using ideal transmission lines. However, higher order mode matching and non-uniform impedance distribution are not taken into account in the circuit simulation.

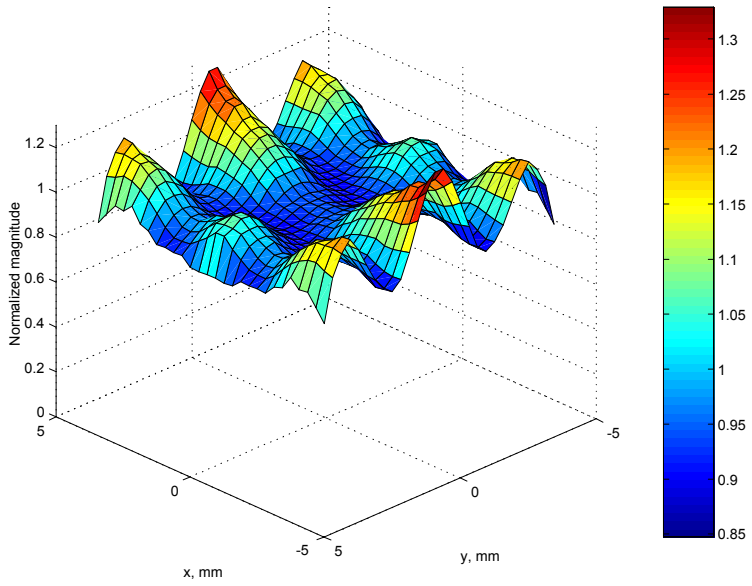


Figure 2.9: The input magnitude distribution of the grid amplifier with input packaged in waveguide and output radiating into free-space. The variance of magnitude, σ_{mag}, equals to 0.0083.

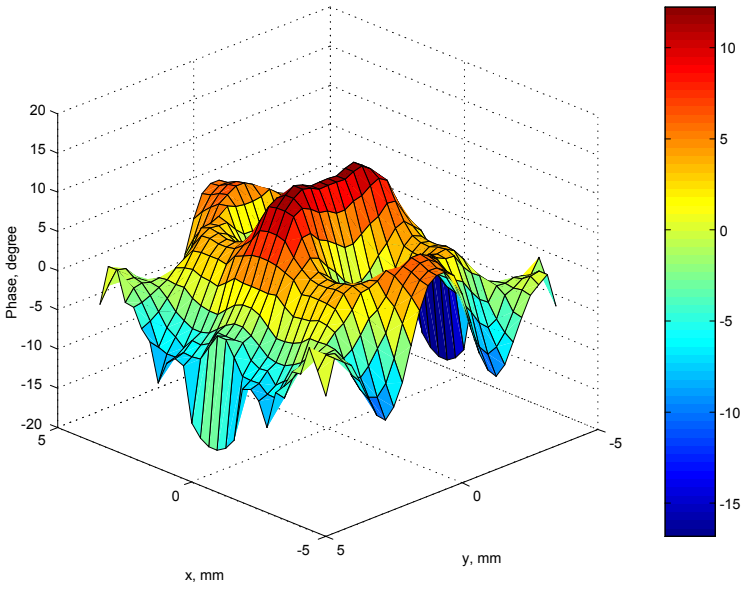


Figure 2.10: The input phase distribution of the grid amplifier with input packaged in waveguide and output radiating into free-space. The phase standard deviation is 5.3°.

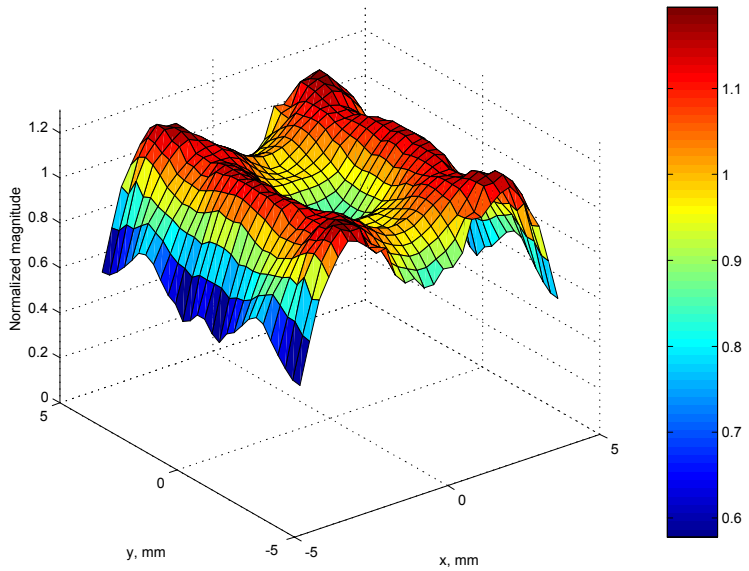


Figure 2.11: The input magnitude distribution across the grid amplifier packaged in waveguide with σ_{mag} equal to 0.019.

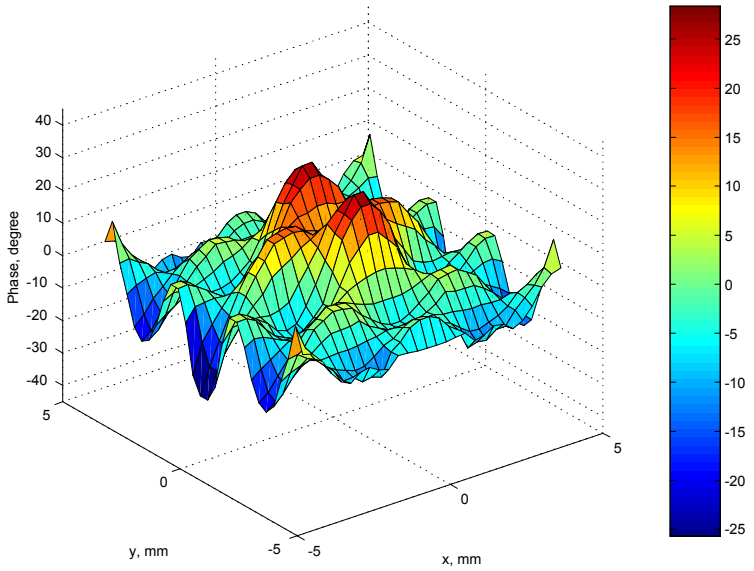


Figure 2.12: The input phase distribution of the grid amplifier packaged in waveguide with phase standard deviation equal to 9.2°.

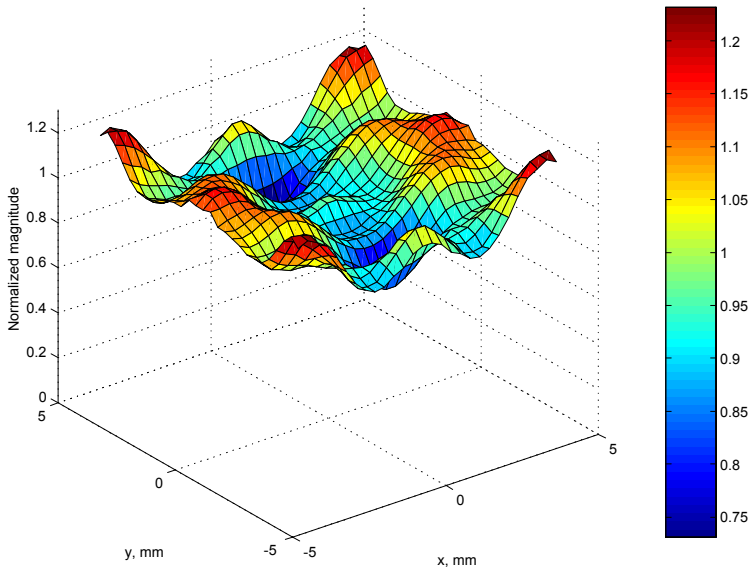


Figure 2.13: The output magnitude distribution of the grid amplifier packaged in waveguide with σ_{mag} equal to 0.011.

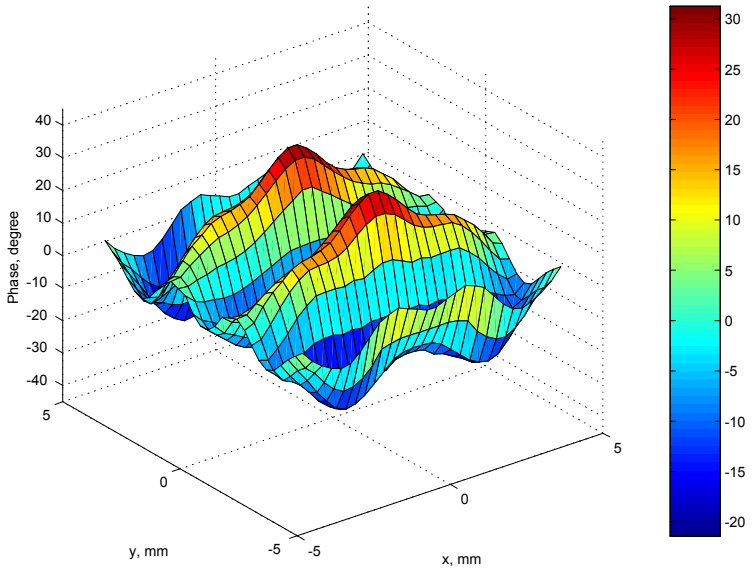


Figure 2.14: The phase distribution of the grid amplifier packaged in waveguide with standard deviation equal to 11.8°.

2.3 Simulation with Anisotropic Material

In the previous section, we have presented a design method for the mode converter and bias circuitry of a grid amplifier using HFSS. However, two problems exist with the previous design method. Firstly, for a radiating output packaged grid as shown in Figure 2.4, output matching cannot be easily taken into account with HFSS. We may only use circuit simulation such as ADS to calculate the matching circuit for the output. In addition, overall system gain of the amplifier cannot be computed easily because we can only apply an impedance boundary to the grid aperture. Secondly, although the unit cell design based on the infinite array assumption may be valid, the output or input loading variation across the grid aperture in the presence of an over-moded waveguide and DC-bias lines may affect the matching. Therefore, the field-uniformity calculated with a single uniform impedance sheet across the grid aperture may not be valid. In the following sections, we will discuss a method to use an anisotropic, non-reciprocal material to model our on-chip amplifier circuit and to show the field simulation results of the grid array. This program can also predict the small-signal amplifier gain and radiation pattern of the grid amplifier that is packaged with input only which cannot be achieved by HFSS in the previous section.

Before we begin to discuss the modelling of the grid amplifier using an anisotropic material, we need to understand the various aspects of field simulations and the choices we made for the implementation.

2.3.1 Finite Difference (FD) versus Finite Element (FE)

Using the finite-difference (FD) method is entirely driven by programming simplicity. A typical finite-difference Yee's cell proposed in [8] is shown in Figure 2.15. The finite-element (FE) method requires adaptive meshing, matrix assembly and matrix condensing routines in order to be effective in numerical computation. These programming routines are considerably more time consuming than finite-difference update equations. On the other hand, the FE method provides a more elegant way of dividing the spatial region. Furthermore, the FE method using Galerkin's procedure

minimizes the residuals between the actual and the numerical field equation solutions [9]. However, we believe the waveguide structure is regular enough that lower flexibility is acceptable. The use of the FD or FE code does not affect, in principle, the discussion about amplifier modelling and structure optimization.

2.3.2 Time Domain versus Frequency Domain

Time-domain simulation, in general, is suitable for low-Q wide-band applications while frequency domain simulation is for high-Q narrow-band applications. Even though our amplifier is not wide in bandwidth, the capability to compute a larger frequency band is most desirable for designing and searching for a uniform-field-distribution frequency. In addition, time-domain simulation easily incorporates transient analysis with a non-linear amplifier model.

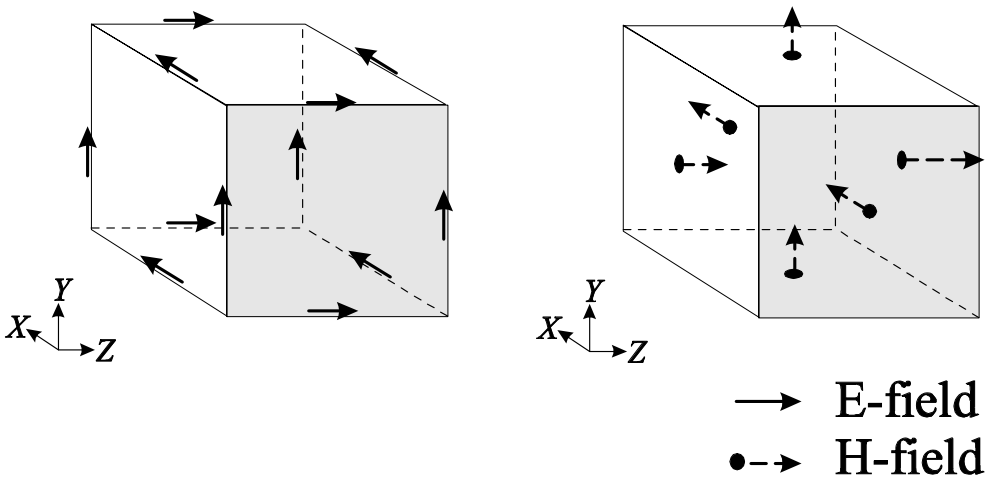


Figure 2.15: The electric (E) and magnetic (H) field assignment to a Yee's unit-cell. All E-field components are on the edge of the cube and H-field components are on the surface of the cell. Therefore H-field components are offset by half of a unit-cell. This is most favourable when a leap-frog scheme [10] is used for solving the difference equations.

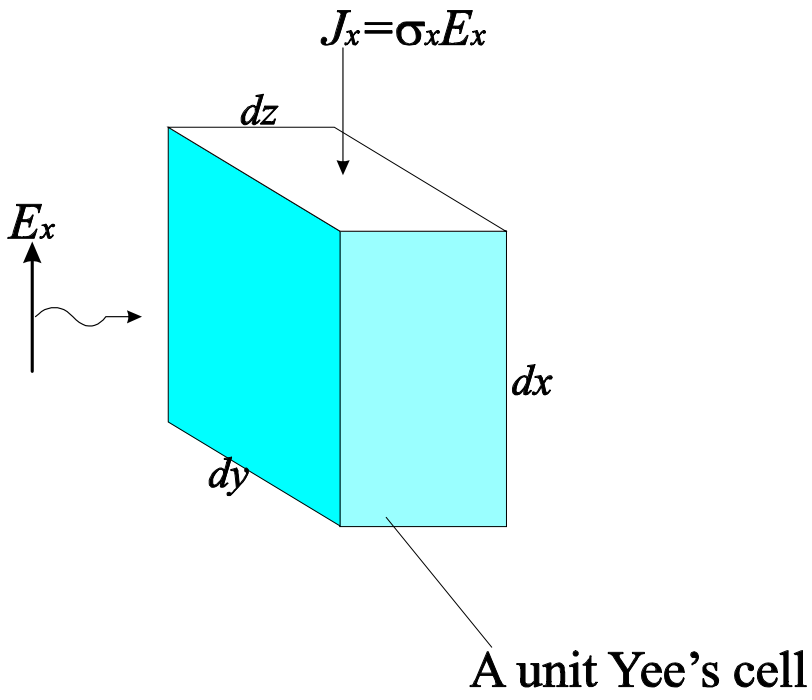


Figure 2.16: The modeling of lumped components in FDTD. Resistors can be translated into corresponding conductivities by $R = V_x/I_x = dx/(\sigma_x \cdot dy \cdot dz)$.

2.3.3 Anisotropic Material

In order to compute a 2-port amplifier response at the input and output, we decide to model the on-chip 2-port amplifier circuit with an anisotropic, non-reciprocal material. Kunz *et al.* [10] suggested a simple way to model a lumped capacitor and resistor in parallel using electric conductivity and permittivity as shown in Figure 2.16. The lumped capacitance and resistance of this single Yee's cell are

$$C = \frac{\epsilon_r \epsilon_0 dzdy}{dx} \tag{2.7}$$

$$R = \frac{\sigma dzdy}{dx} \tag{2.8}$$

The parallel-connected inductive element can be modelled by adding the equation

$$I_x = \frac{1}{L_{xy}} \int_0^t V_y d\tau \tag{2.9}$$

into the field update equations where I is the current that flows through one Yee's cell cross section, V is the voltage across the cell and L is the inductance of the cell.

The modelling of the unit-cell transistor amplifier extends the use of a co-polarized lumped element model into its cross-polarized counterpart. The capacitance and resistance (or conductance) can be translated into off-diagonal elements of a permittivity and electric conductivity tensor matrix. The inductive element can be added in a similar manner by adding appropriate integration equations into the update equations. Using the model in Figure 2.17, we calculate the Y-matrix values at the input and output and specify the permittivity and conductivity accordingly. Figure 2.18 shows the comparison of scattering parameters between unit-cell design using the method in [5] and the anisotropic material equivalent model between 33-37 GHz.

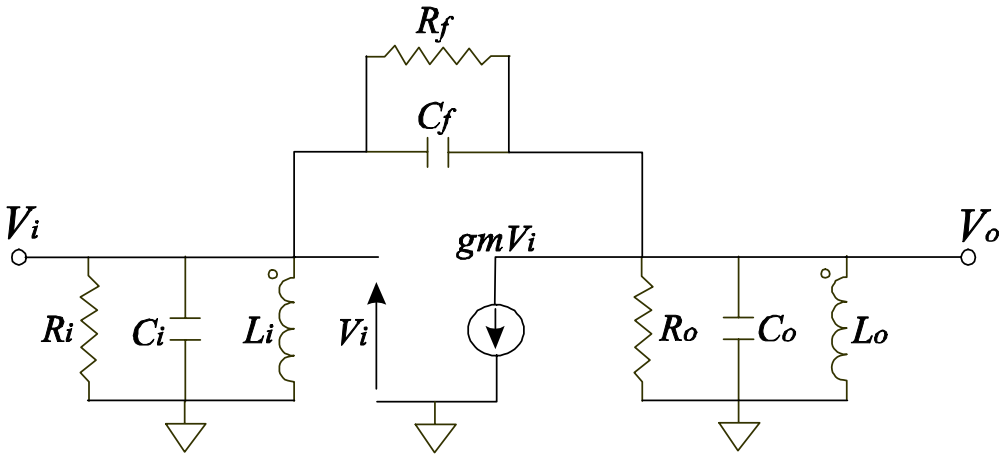


Figure 2.17: The equivalent circuit model of anisotropic material used in FDTD. The s-parameters are matched to the transistor amplifier. Circuit element values are then converted into material parameters using equations in [10].

In addition, according to [11] and [12], if the material parameters satisfy

$$\frac{\sigma}{\epsilon_0} = \frac{\sigma^*}{\mu_0} \tag{2.10}$$

then the impedance of this media equals vacuum and no reflection occurs with a plane wave incident normal to the medium interface. σ^* is the magnetic conductivity of the

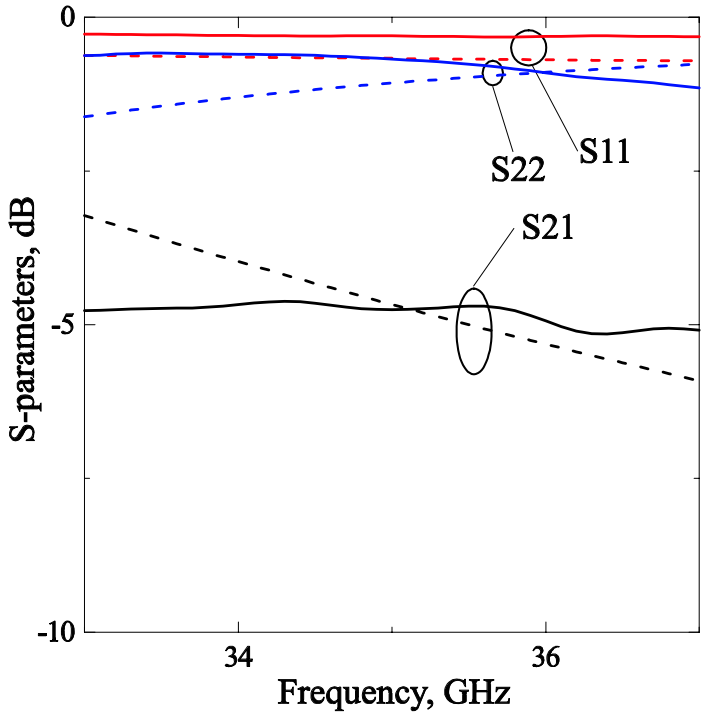


Figure 2.18: The unit-cell model (solid line) and the matched anisotropic equivalent model (dashed line) scattering parameters between 33-37 GHz for the 35 GHz grid amplifier designed in Deckman *et al.* [3].

material. This is most easily understood by checking the solution of a plane wave travelling in this material

$$Z = \sqrt{\frac{\sigma^* + j\varpi\mu_0}{\sigma + j\varpi\epsilon_0}} \tag{2.11a}$$

$$\gamma = \sqrt{(\sigma + j\varpi\epsilon_0)(\sigma^* + j\varpi\mu_0)} \tag{2.11b}$$

If we apply equation 2.10 to equation 2.11, the results are

$$Z = \sqrt{\frac{\mu_0}{\epsilon_0}} = Z_0 \tag{2.12a}$$

$$\gamma = \alpha + j\beta = \sigma\sqrt{\frac{\epsilon_0}{\mu_0}} + j\omega\sqrt{\mu_0\epsilon_0} \tag{2.12b}$$

which show that the wave travels at the speed of light with the free-space characteristic impedance. This implies a plane wave travelling through the interface between free-space and this material will experience no reflection from this interface, but will gradually diminish to zero in this material due to a non-zero α in Equation 2.12b. We set the electric and magnetic conductivity of the remaining axis in the anisotropic material according to Equation 2.10. This does not affect the wave propagation at normal incidence but attenuates the surface wave travelling along the anisotropic material sheet which may cause numerical stability problems. Thus they become free parameters to be adjusted to improve our numerical stability requirement.

2.4 Numerical Stability of Anisotropic Material in FDTD

In the previous section, we showed how we design an anisotropic material to fit our transistor circuit. However, numerical simulation with FDTD requires us to ensure the model is stable. For an isotropic, homogenous material, the Courant stability

criterion [8],[10]

$$\Delta t \leq \sqrt{\mu\epsilon\left(\frac{1}{\Delta x}^2 + \frac{1}{\Delta y}^2 + \frac{1}{\Delta z}^2\right)^{-1}} \tag{2.13}$$

gives a theoretical bound on the largest time step that may be taken in the simulation for explicit methods. For an anisotropic, frequency-dependent, homogenous material without the inductor modifying equation, Beck *et al.* [13] offer a procedural method to check the stability by looking into the complex temporal frequency at each spatial frequency vector $\overrightarrow{k}$. In our case, we need to use the inductive element to correctly account for the phase of the amplifier. This modified update equation for an isotropic, homogenous material with an inductive lumped element is given in Kunz *et al.* [10] without a stability analysis. Thus we need to derive the new procedure to check our numerical stability for an anisotropic material with an inductive element. The modified update equation for an anisotropic, nonreciprocal, homogenous material is

$$E_i^{n+1} = A \cdot E_i^n + B \cdot \left(H_i^{n+1/2} - H_{i-1}^{n+1/2}\right) - \Delta t \cdot S \cdot (1/L) \cdot P_i^n \tag{2.14a}$$

$$H_i^{n+1/2} = C \cdot H_i^{n-1/2} - D \cdot \left(E_i^n - E_{i-1}^n\right) \tag{2.14b}$$

$$P_i^{n+1} = P_i^n + E_i^{n+1} \tag{2.14c}$$

where E_i^n and H_i^n are the vector electric and magnetic fields at time step n and vector spatial location i. Furthermore, the closed form of P_i^n is $P_i^n = \sum_{j=0}^{n} E_i^j$. The analysis here extends the methods in [10]. Using Von Karman analysis, taking the Fourier transform of the spatial variable, the equations are combined and become a gain matrix equation in the form

$$F^{n+1} = G\left(\overrightarrow{k}\right) \cdot F^n \tag{2.15}$$

where

$$F = \begin{pmatrix} E^n \\ H^n \\ P^n \end{pmatrix} \tag{2.16a}$$

$$\overline{G} = \begin{pmatrix} \Delta_1^{-1}\left[\frac{\epsilon_0\bar{\epsilon}}{\Delta t} - \Delta_2^{-1}\bar{K}\left(\overrightarrow{k}\right)\right]^2 & \frac{\mu_0}{\Delta t}\Delta_1^{-1}\bar{K}\left(\overrightarrow{k}\right)\Delta_2^{-1} & -\Delta_1^{-1}\Delta t\bar{L}_{inv} \\ -\Delta_2^{-1}\bar{K}\left(\overrightarrow{k}\right) & \frac{\mu_0}{\Delta t}\Delta_2^{-1} & 0 \\ \Delta_1^{-1}\left[\frac{\epsilon_0\bar{\epsilon}}{\Delta t} - \Delta_2^{-1}\bar{K}\left(\overrightarrow{k}\right)\right]^2 & \frac{\mu_0}{\Delta t}\Delta_1^{-1}\bar{K}\left(\overrightarrow{k}\right)\Delta_2^{-1} & 1 - \Delta_1^{-1}\Delta t\bar{L}_{inv} \end{pmatrix} \tag{2.16b}$$

$$\Delta_1 = \frac{\epsilon_0\overline{\epsilon}}{\Delta t} + \bar{\sigma}\Delta t\overline{L}_{inv} \tag{2.16c}$$

$$\Delta_2 = \frac{\mu_0}{\Delta t} + \bar{\sigma}^* \tag{2.16d}$$

$$\overline{L}_{inv} = \begin{pmatrix} \Delta x/\left(\Delta y\Delta z L_{xx}\right) & \Delta y/\left(\Delta y\Delta z L_{xy}\right) & \Delta z/\left(\Delta y\Delta z L_{xz}\right) \\ \Delta x/\left(\Delta x\Delta z L_{yx}\right) & \Delta y/\left(\Delta x\Delta z L_{yy}\right) & \Delta z/\left(\Delta x\Delta z L_{yz}\right) \\ \Delta x/\left(\Delta x\Delta y L_{zx}\right) & \Delta y/\left(\Delta x\Delta y L_{zy}\right) & \Delta z/\left(\Delta x\Delta y L_{zz}\right) \end{pmatrix} \tag{2.16e}$$

$$\overline{K}\left(\overrightarrow{k}\right) = \begin{pmatrix} 0 & -jk_z\mathrm{sinc}\left(\theta_z\right) & -jk_y\mathrm{sinc}\left(\theta_y\right) \\ -jk_z\mathrm{sinc}\left(\theta_z\right) & 0 & -jk_x\mathrm{sinc}\left(\theta_x\right) \\ -jk_y\mathrm{sinc}\left(\theta_y\right) & -jk_x\mathrm{sinc}\left(\theta_x\right) & 0 \end{pmatrix} \tag{2.16f}$$

$$\overrightarrow{k} = \begin{pmatrix} k_x \\ k_y \\ k_z \end{pmatrix} \tag{2.16g}$$

$$\theta_i = \frac{k_i\Delta i}{2}, \quad i = x, y, z$$

If all the eigenvalues for each spatial frequency vector $\overrightarrow{k}$ are smaller than unity, the limit of F is bounded and thus guarantees the stability of the simulation. Similarly, if we use a frequency-dependent Debye, Drude, or Lorentz material with an inductive lumped-element, we need to change our update equation and apply the analysis again. The definition of Debye, Drude and Lorentz materials can be found in [10] and [13]. Figure 2.19 shows the calculated eigenvalues of the anisotropic material model derived for a 35GHz grid amplifier with the time step of 0.3 ps. This model uses frequency

independent parameters and lumped inductive components listed in Table 2.1.

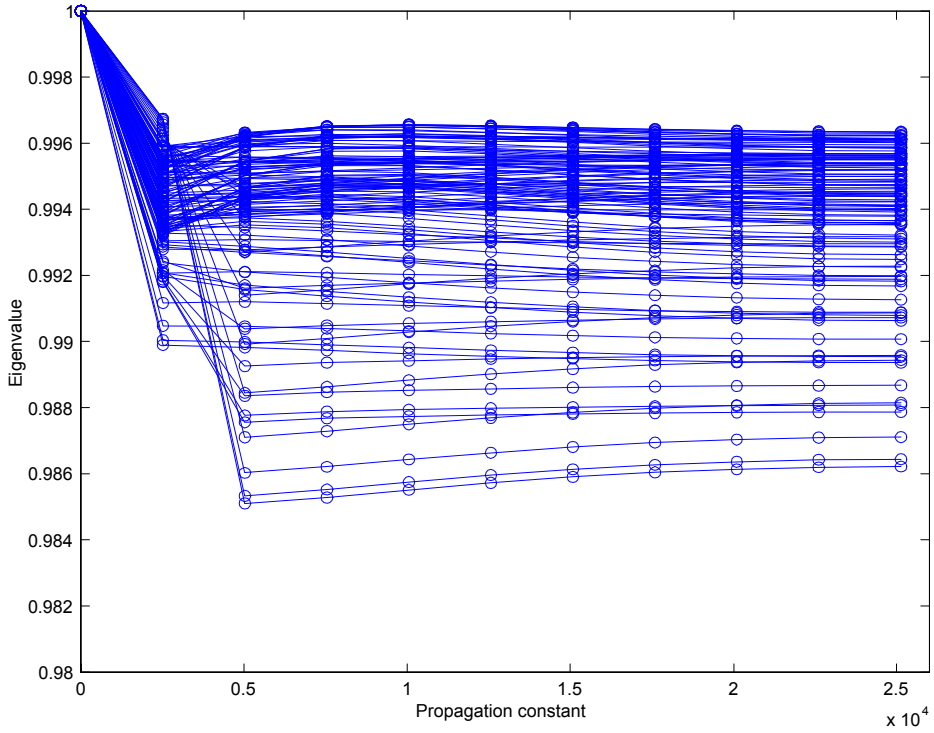


Figure 2.19: The calculated eigenvalues of the gain matrix as a function of propagation constant with model parameters derived from a 35 GHz grid amplifier unit cell. All the eigenvalues are less than 1 and the scheme is stable. The time step Δt equals to 0.3 ps, Δx and Δy equal 0.325 mm and Δz equals 0.125 mm.

Model components	component values
g_m, mS	217
R_i, Ω	10
R_o, Ω	176
R_f, Ω	449
C_i, fF	113
C_o, fF	324
L_i, pH	76
L_o, pH	103

Table 2.1. The component values of an anisotropic model derived from a 35GHz grid amplifier. These values are transformed into $\overline{\sigma}$, $\overline{\epsilon_r}$ and $\overline{L_{inv}}$ using Equations 2.7 to 2.9.

2.5 Simulation Results of FDTD for Grid Amplifiers

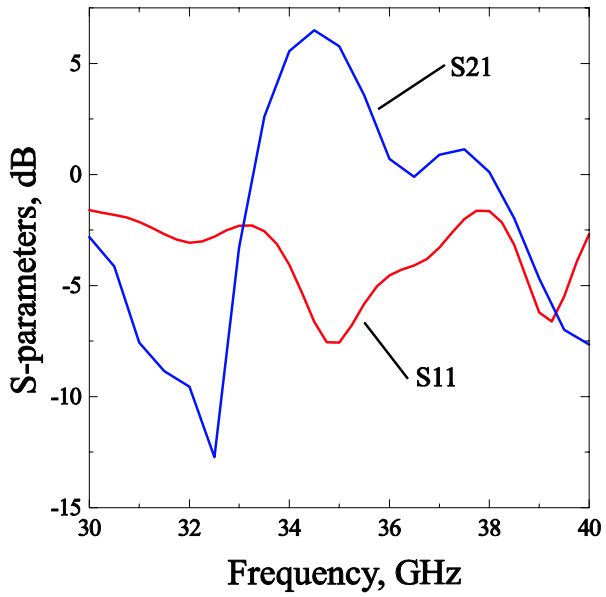


Figure 2.20: The FDTD simulated small-signal gain and return loss of the grid amplifier with input packaged in waveguide. The gain is 7 dB with an input match of -7.5 dB.

We apply the design we made using HFSS to our FDTD simulation. The geometry is discretized into Yee's cells with dx, dy and dz equal to 325 μm, 325 μm and 125 μm respectively, and the time step, dt, is 0.35 ps. The simulated return loss and gain of the amplifier shown in Figure 2.4 are shown in Figure 2.20. The gain was calculated by integrating the Poynting's vector calculated from the output polarized field distribution around the radiation boundaries. In addition, the surface integration around the radiation boundaries can compute the radiation pattern of the amplifier which cannot be achieved by HFSS due to polarization rotation of the grid amplifier. Figure 2.21 shows the E and H-plane radiation patterns for this grid amplifier. The radiation pattern and antenna gain allow us to separate the amplifier gain from the active antenna gain, which is actually measured. The simulation results will be compared with the measured data in Chapter 3.

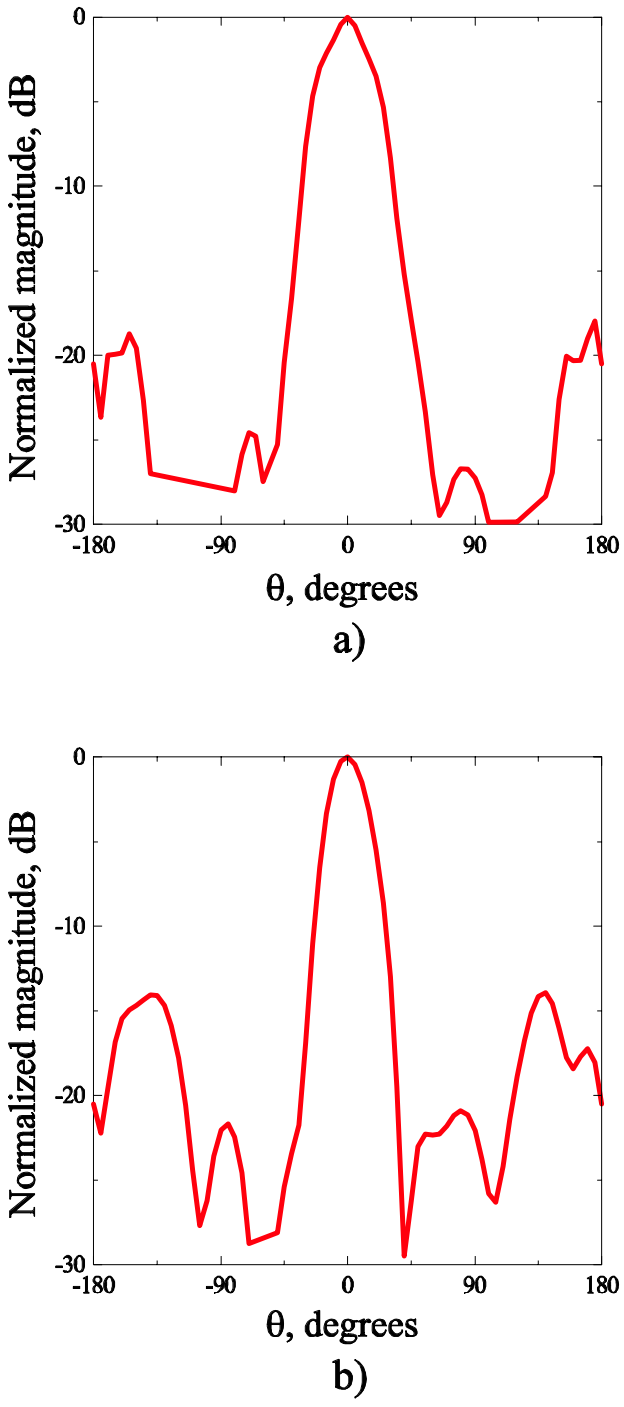


Figure 2.21: The normalized a) H-plane and b) E-plane radiation patterns of the grid amplifier with input packaged in waveguide.

2.6 FD/FE State-space (SS) Approach

In the previous section, we concluded that the most severe limitation of the FDTD method is that it is not unconditionally stable. Therefore we try to obtain an unconditionally stable field simulation method to implement the anisotropic material model.

The state-space approach is based on the analytical solution of a set of first order ordinary differential equations. For a set of differential equations arranged in a matrix form,

$$\frac{dF(t)}{dt} = \overline{A} \cdot F(t) + \overline{B} \cdot f(t) \tag{2.17}$$

where $F(t)$ is a column vector of variables, $f(t)$ is the time varying forcing functions and boundary conditions. If the matrix $\overline{A}$ is invertible, the general solution to this equation is

$$F(t) = e^{\overline{A}t} \cdot F(0) + e^{\overline{A}t} \int_0^t e^{\overline{A}^{-1}\tau} \cdot f(\tau) d\tau \tag{2.18}$$

where $e^{\overline{A}t} \equiv \sum_{i=0}^{\infty} \frac{(\overline{A}t)^i}{i!}$

For either the FD or FE spatial discretization approach, if we arrange the discretized spatial variables into a column vector and apply source functions and boundary conditions accordingly, we may cast our temporal ordinary differential equations into the form of Equation 2.17. We may then discretize the temporal solution 2.18 as

$$F^{n+1} = e^{\overline{A}\cdot(n+1)\cdot\Delta t} \cdot F^0 + e^{\overline{A}\cdot(n+1)\cdot\Delta t} \sum_{i=0}^{n} e^{\overline{A}^{-1}\cdot i\cdot\Delta t} \cdot f(i\cdot\Delta t)\cdot\Delta t \tag{2.19}$$

Furthermore, note that $e^{\overline{A}\cdot(n+1)\cdot\Delta t} = e^{\overline{A}\cdot\Delta t}\cdot e^{\overline{A}\cdot n\cdot\Delta t}$. Therefore we may have an iterative update equation

$$F^{n+1} = e^{\overline{A}\cdot\Delta t} \cdot F^n + f((n+1)\cdot\Delta t)\cdot\Delta t \tag{2.20}$$

If the given physical system is bounded-input, bounded-output (BIBO) stable, the solution of the continuous-time discrete-space system $F(t)$ is bounded. In addition, the second part of the discretized solution in equation 2.19 can be regarded as the

numerical integration of equation 2.18 using the rectangular rule. The integration error can be shown to be bounded and converge to $F(t)$ as Δt approaches zero (Appendix A) and hence the numerical solution F^n is bounded. Thus the time step Δt only controls the accuracy of the numerical integration of the forcing function. The disadvantage of this scheme is that the matrix $\overline{A}$ increases quadratically as the size of the spatial domain increases linearly. Therefore, the computational effort to find $e^{\overline{A}\cdot\Delta t}$ is fairly large when the structure is bigger than one wavelength of the lowest frequency of interest. On the other hand, the numerical stability problem associated with FDTD method is resolved.

2.7 Implementation and Simulation Results

A simple 1-D FDSS simulation has been implemented using Matlab with anisotropic material to check the stability of the algorithm. We use the two first-order Maxwell differential equations and assume variation only in the z direction. The spatial variables are discretized with the leap-frog scheme [10] and we arrange the field variables into column vectors of the form

$$F = \begin{pmatrix} E \\ H \\ P \end{pmatrix}$$

where $P = \int_0^t E dt$. The current status of each field variable along the line depends only on the adjacent field variables and the previous status of the variable. Thus at

point i, the continuous-time discrete-space system can be written as

$$\begin{pmatrix} \dot{E}_x^i \\ \dot{E}_y^i \end{pmatrix} = \frac{1}{\epsilon_0}\left(\overline{\epsilon}_r^T\overline{\epsilon}_r\right)^{-1}\overline{\epsilon}_r^T \left[\begin{array}{c} -\overline{\sigma}\begin{pmatrix} E_x^i \\ E_y^i \end{pmatrix} + \begin{pmatrix} 0 & 0 & \frac{1}{dz} & \frac{-1}{dz} \\ \frac{-1}{dz} & \frac{1}{dz} & 0 & 0 \end{pmatrix}\begin{pmatrix} H_x^{i-1/2} \\ H_x^{i+1/2} \\ H_y^{i-1/2} \\ H_y^{i+1/2} \end{pmatrix} \\ -\begin{pmatrix} \frac{1}{L_{xx}} & \frac{1}{L_{xy}} \\ \frac{1}{L_{yx}} & \frac{1}{L_{yy}} \end{pmatrix}\begin{pmatrix} P_x^i \\ P_y^i \end{pmatrix} \end{array} \right] \tag{2.21a}$$

$$\begin{pmatrix} \dot{H}_x^{i-1/2} \\ \dot{H}_y^{i-1/2} \end{pmatrix} = \frac{1}{\mu_0}\left[\begin{pmatrix} 0 & 0 & \frac{-1}{dz} & \frac{1}{dz} \\ \frac{1}{dz} & \frac{-1}{dz} & 0 & 0 \end{pmatrix}\begin{pmatrix} E_x^{i-1} \\ E_x^{i+1} \\ E_y^{i-1} \\ E_y^{i-1} \end{pmatrix} - \overline{\sigma}^*\begin{pmatrix} H_x^{i-1/2} \\ H_y^{i-1/2} \end{pmatrix} \right] \tag{2.21b}$$

$$\begin{pmatrix} \dot{P}_x^i \\ \dot{P}_y^i \end{pmatrix} = \begin{pmatrix} E_x^i \\ E_y^i \end{pmatrix} \tag{2.21c}$$

Furthermore, the implementation of Berenger's perfectly matched layer (PML) is the same as with the FDTD scheme.

We first demonstrate the stability of the program by calculating the reflection coefficient due to a half-wavelength thick dielectric with permittivity of 10 (Figure 2.22). The input pulse contains frequencies from 15 to 35 GHz with a Gaussian distribution. The spatial step, dz, is 0.1 mm and the time step is 1 ps. According to the Courant stability limit 2.13, the maximum allowable time step for this 1-D problem is 0.33 ps. However, as shown in the figure, the simulation agrees with the theoretical reflection coefficient. It shows that the time step does not affect the stability of the numerical scheme. However, in order to maintain good accuracy, the minimum number of samples per period is about 30 to 40 points. For example, an incident signal with a maximum frequency of 50 GHz would be recommended to use a time step less than 0.5 ps instead of 1 ps for this example.

Using this program, we apply the anisotropic material derived for the 35 GHz

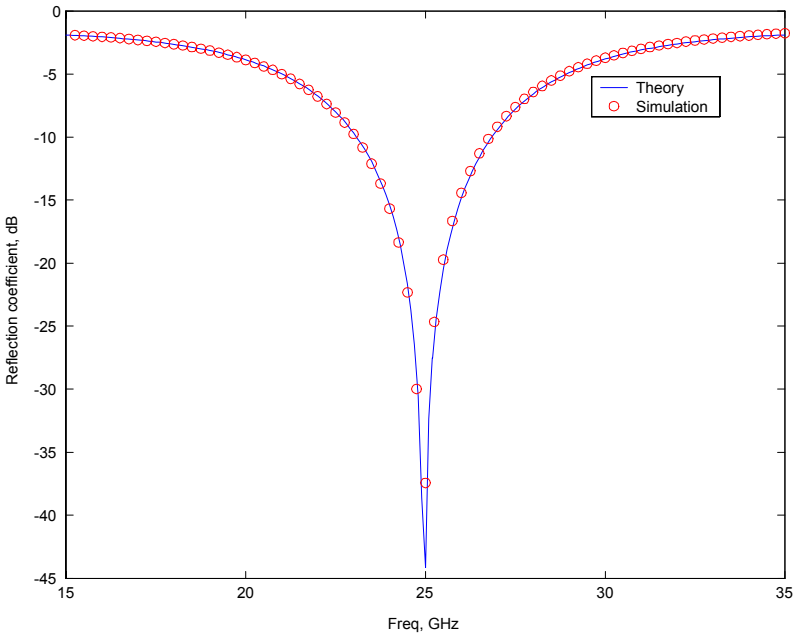


Figure 2.22: The theory and simulation results of the reflection coefficient of a wave incident on a piece of dielectric with permitivity of 10. Δt is 1 ps which is larger than the Courant stability limit of 0.33 ps for FDTD method.

grid amplifier unit cell. Figure 2.23 shows the scattering parameters of the ADS and the FDSS simulation with the same matching layers and anisotropic material model. This simulation has Δz equal to 125 μm and it is corresponding to a Courant limit of 0.42 ps for isotropic, homogenous material. We apply an input from 30 GHz to 40 GHz and we use Δt=0.6 ps to maintain good accuracy. The good agreement shows that the method of translating lumped circuit components into anisotropic material properties is correct. Besides, it also shows that the maximum time step is not limited by numerical stability. The FDSS program took 2 minutes to calculate the forward and reverse scattering parameters on a 300 MHz Intel PC. It is possible to expand this code to 3-D simulation and keep the capability of simulating a grid amplifier with gain. This FDSS program as well as the previous FDTD program provides a way to simulate and understand the dynamics of large transistor arrays with local boundary conditions and impedance variations taken into account properly. They also demonstrate that electromagnetic simulations can be expanded to study complicated

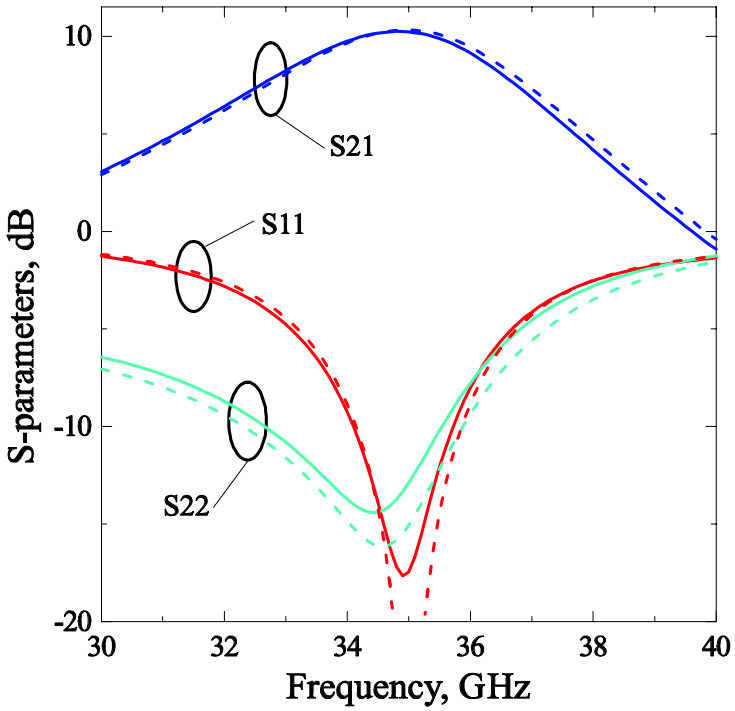


Figure 2.23: The comparison between ADS (solid line) and FDSS (dashed line) simulation results. Both simulations are based on the same anisotropic material model and matching circuit. The FDSS program took 2 minutes to calculate the forward and reverse scattering parameters.

active and non-linear components.

Reference

[1] G. Dammertz, E. Borie, C. T. Iatrou, M. Kuntze, B. Piosczyk, and M. K. Thumm, "140-GHz Gyrotron with Multimegawatt Output Power," *IEEE Trans. Plasma Sci.*, Jun. 2000, pp. 561-566.

[2] R. C. Johnson, "Antenna Engineering Handbook," 3rd Edition, *McGraw Hill, Inc.,* 1993.

[3] B. Deckman, D. S. Deakin, Jr., E. Sovero, D. Rutledge, "A 5-Watt, 37-GHz Monolithic Grid Amplifier," 2000 Int. Microwave Symp. Dig., pp. 805-808.

[4] M. Kim, J. B. Hacker, A. L. Sailer, S. Kim, D. Sievenpiper and J. A. Higgins, "A Rectangular TEM Waveguide and Photonic Crystal Walls For Excitation of Quasi-Optical Amplifiers," 1999 Int. Microwave Symp. Dig., pp. 543-546.

[5] P. Preventza, B. Dickman, E. Sovero, M. P. Delisio, J. J. Rosenberg, D. B. Rutledge, "Modeling of Quasi-Optical Array," 1999 Int. Microwave Symp. Dig., pp. 563-566.

[6] D. M. Pozar, "Microwave Engineering," 2nd Edition, *John Wiley & Sons,* Chap. 11.

[7] R. A. York, "Some Considerations for Optimal Efficiency and Low Noise in Large Power Combiners," *IEEE Trans. Microwave Theory and Tech.*, Aug. 2001, pp. 1477-1482.

[8] K. S. Yee, "Numerical Solution of Initial Boundary Value Problems Involving Maxwell's Equations in Isotropic Media," *IEEE Trans. Antennas Propagation*, vol. 14, 1966, pp. 302-307.

[9] J. L. Volakis, A. Chatterjee, L. C. Kempel, "Finite Element Method for Electromagnetics," *IEEE Press*, 1998.

[10] K. S. Kunz, R. J. Luebbers, "The Finite Difference Time Domain Method for Electromagnetics," *CRC Press.*

[11] J. P. Berenger, "A Perfectly Matched Layer for the Absorption of Electromagnetic Waves," *Journal of Comp. Physics*, vol. 114, 1994, pp. 185-200.

[12] D. K. Cheng, "Field and Wave Electromagnetics," 2nd Edition, *Addison Wesley,* Chapter 9.

[13] W. A. Beck and M. S. Mirotznik, "Generalized Analysis of Stability and Numerical Dispersion in the Discrete-Convolution FDTD Method," *IEEE Trans. Antennas Propagation,* vol. 48, 2000, pp. 887-894.

[14] J. N. Franklin, "Matrix Theory," *Prentice-Hall, Inc.*

Chapter 3

Ka-band Grid Amplifiers Packaged in Waveguide

This chapter details the implementation and measurement results of the following devices described earlier: the passive mode converter, the grid amplifier packaged for input only, and the grid amplifier packaged for input and output.

3.1 Passive Mode Converter

As mentioned in Chapter 2, we first fabricated a passive mode converter for verification measurement. Figure 3.1 shows the mode converter fabricated out of brass. The waveguide steps, field sampling holes and extended over-moded waveguide section can be seen. The sampling holes were designed with HFSS to give less than 50 dB leakage in the absence of a probe and have 30 dB coupling to an inserted probe. Figure 3.2 shows the probes and their use to measure the fields inside the over-moded waveguide. H-plane monopole and E-plane loop probes were made with 1.19 mm semi-rigid coaxial cable. The H-plane monopole probe samples the electric field, E_x, along the y-axis, while the E-plane loop probe samples the magnetic field ,H_z, along x-axis. This field probing technique was the same as in [1], which describes an earlier tapered mode converter.

Unfortunately, there is no standard over-moded waveguide termination available. The dominant mode may be terminated into free space through open-ended guide and give sufficient return loss. However, terminating the TE_{30} mode with an open-

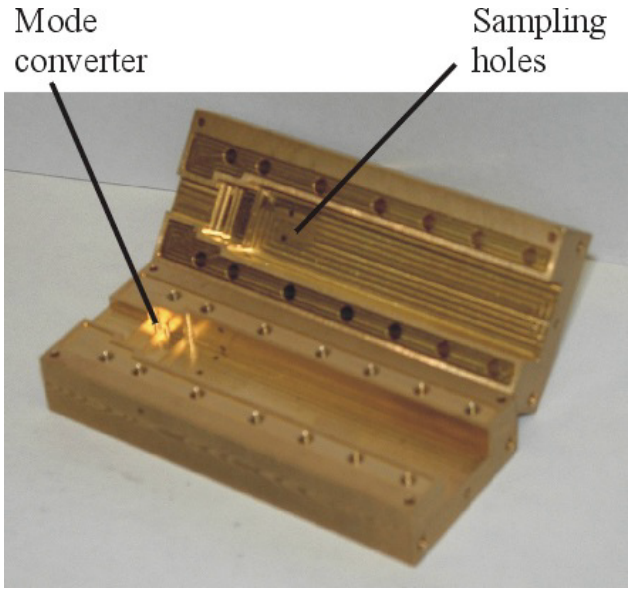


Figure 3.1: The fabricated passive mode converter with sampling holes. The over-moded waveguide section is extended beyond the uniform phase plane to accomodate insertion of absorber to match-terminate the guide.

ended guide results in large reflection. Thus, the over-moded waveguide section was extended to allow the insertion of absorber as a terminating load. Figures 3.3 and 3.4 show a quarter view of the HFSS model and the field solution, respectively, with an absorber at the end. The simulated absorber material was derived from Emerson & Cuming Microwave Product's ECCOSORB material specifications. The material's relative permittivity is 2.25, and its loss tangent is 0.4. The dimensions of the pyramid are measured from ECCOSORB absorber. The field solution, as seen in Figure 3.4, shows no significant reflection associated with the absorber termination within the over-moded waveguide section. The return loss in standard waveguide has negligibly small deviation from the original simulation results as well.

Figure 3.5 shows the measured and simulated return loss at the standard waveguide input. The simulation is as described in Chapter 2 with a perfect matched load assumed at the over-moded waveguide port. Both phase and magnitude are in good agreement, confirming that the termination does not distort the field within over-moded waveguide section. The measured return loss 20-dB bandwidth is 10 %

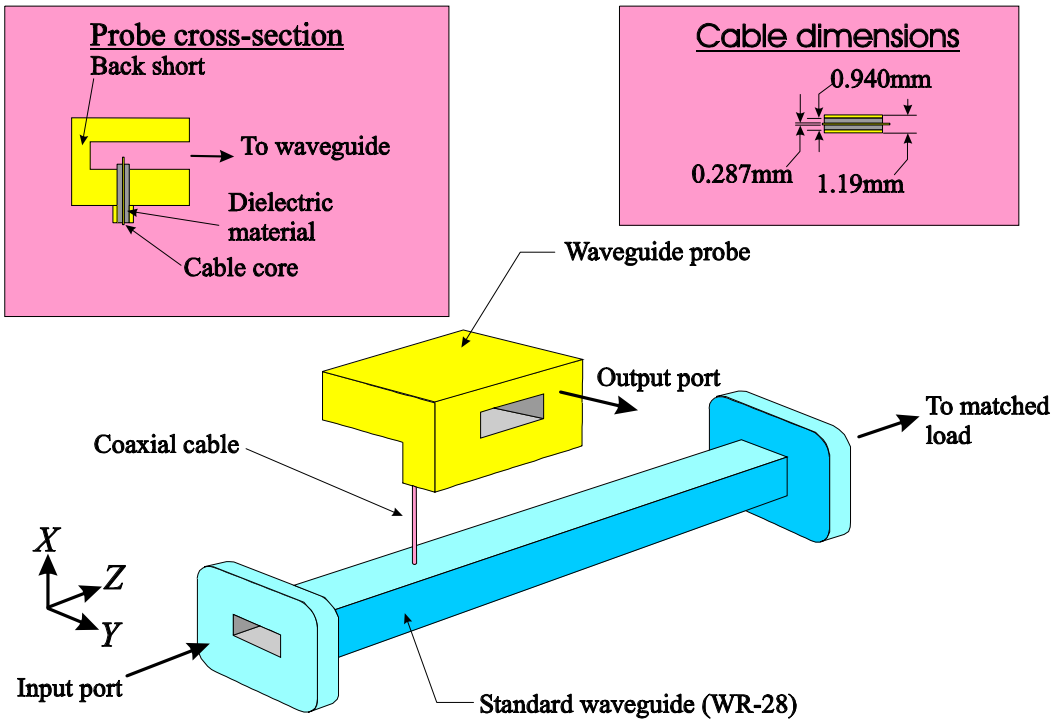


Figure 3.2: The general field probing setup. The device under probe can be a standard waveguide as shown or an over-moded waveguide. The probe was designed with HFSS and has low return loss when two of them are connected back-to-back through the coaxial cable.

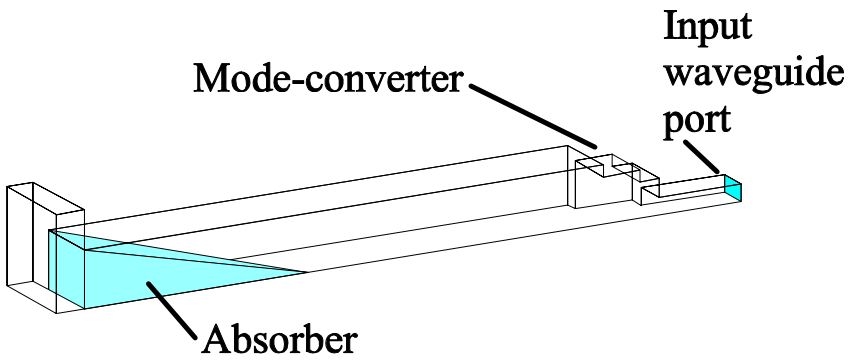


Figure 3.3: The HFSS drawing of the absorber terminated mode-converter. The region beyond the over-moded waveguide flange is defined as radiation boundary. Only a quarter of the full structure was simulated because of the symmetry of the waveguide.

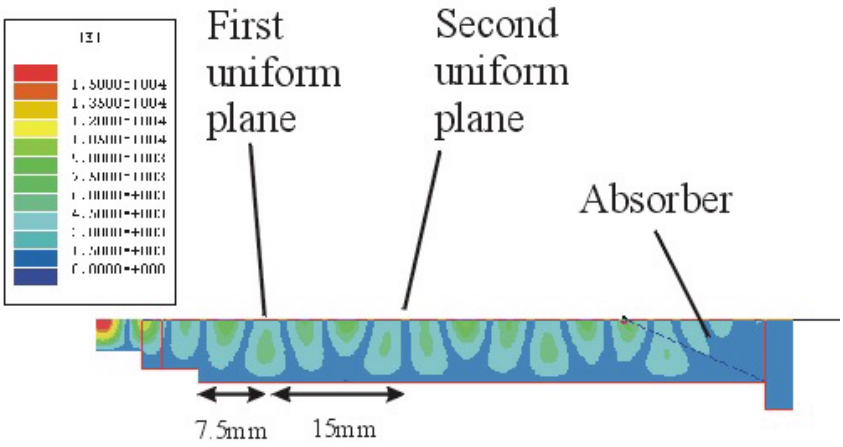


Figure 3.4: HFSS simulation of the mode-converter with absorber. The absorber material has relative permitivity 2.25 and loss tangent 0.4 which gives -50dB reflection at 35GHz with a thickness of 2cm as specified in Emerson & Cummings' ECCOSORB product manual.

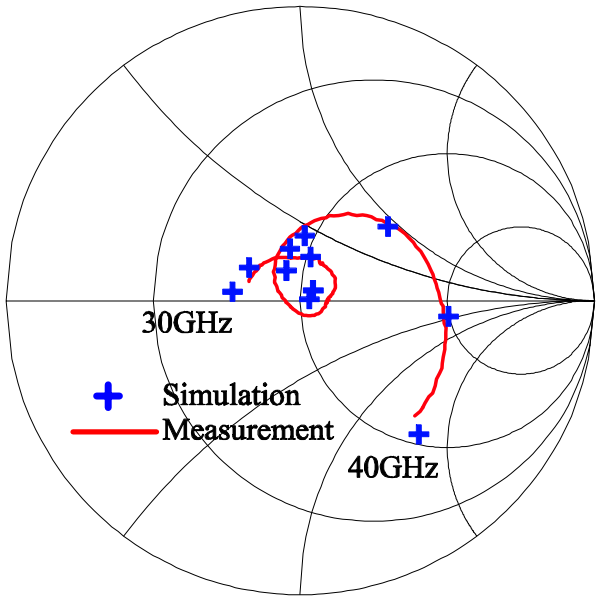


Figure 3.5: The modeled and measured return losses of a passive mode converter from 30 to 40 GHz. The 20 dB bandwidth is 10 %. The measured mode converter was terminated with absorber at the end of the over-moded waveguide section.

compared to a 3.5 % bandwidth for the chip to be placed in it [2], which implies that the passive mode converter does not impose major bandwidth reduction. The probed E-plane and H-plane field distributions at two different uniform field planes at 35 GHz are shown in Figure 3.6 and Figure 3.7, respectively. The good measurement results of different uniform field planes assures that the phase velocity of both TE_{10} and TE_{30} modes are accurately predicted in our simulations.

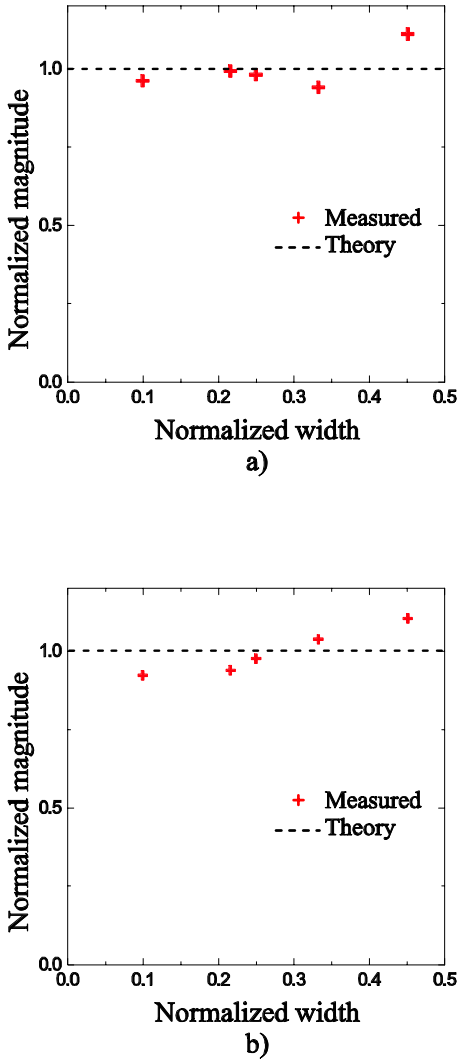


Figure 3.6: The E-plane field probing measurement results of a) the first uniform field plane and b) the second uniform field plane. The uniformity implies higher order modes such as TM_{12} were not excited.

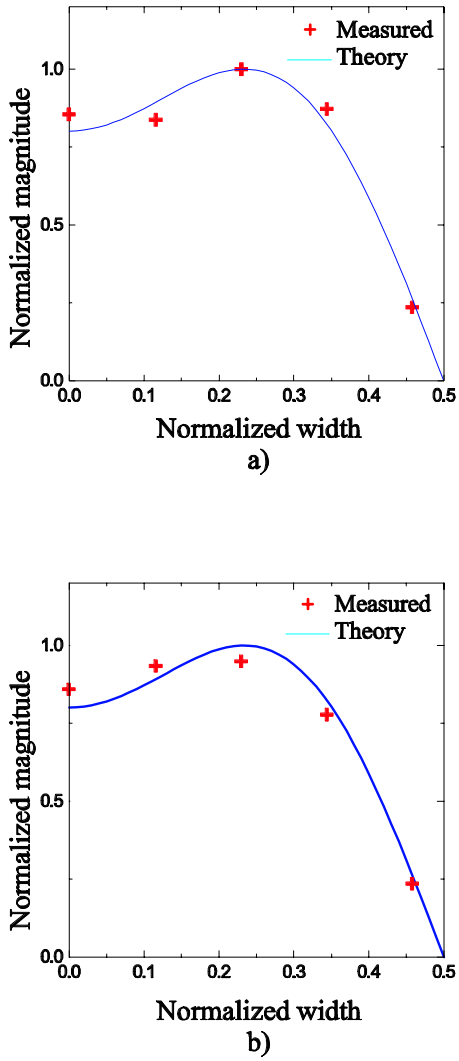


Figure 3.7: The H-plane field probing measurement results of a) the first uniform field plane and b) the second uniform field plane. The measured ratio of TE_{30} to TE_{10} agrees with the simulated results from HFSS.

3.2 A Ka-band Grid Amplifier Packaged for Input Only

3.2.1 Package Assembly

The grid amplifier with packaged input and radiating output is fabricated as shown in Figure 3.8. Waveguide shims and polarizers can be inserted to tune the input and output matching. The polarizer was fabricated lithographically on a piece of 127 μm thick copper shim stock and then gold plated. In order to mount the thermal spreader, the brass over-moded waveguide unit was heated beyond 200 °C. It is important to have the temperature sufficiently high because the thermal glue, which is used to mount the chip after the spreader is set, cures at 125 °C. Since AlN has a lower thermal expansion coefficient than brass, the brass waveguide expands faster and allows the AlN to be inserted inside. Cooling the unit back to room temperature holds the thermal spreader tightly within the aperture. In order to increase the thermal conduction of the contact, a thin layer of thermal grease was painted between the AlN and the brass unit before insertion. Bias microstrips are made on duroid and DC-bias connectors are installed after mounting and wire-bonding the chip. Bypass ceramic capacitors as shown in Figure 3.8 are used to reduce RFI. The output-side polarizer is patterned on a piece of duroid 254 μm thick with a relative permittivity of 10.2. An additional duroid tuning slab with a relative permittivity of 2.2 follows the output-side polarizer to obtain additional output tuning. The amplifier chip design is the same as Deckman *et al.* [2] and was fabricated by Rockwell with 0.18 μm pHEMTs on a GaAs substrate.

3.2.2 Measurement Setup of the Amplifier

For radiated output power and amplifier gain, we use the effective transmitter power (ETP) and system gain defined by Gouker [3]

$$P_{eff} = \frac{EIRP}{D_{trans}} \tag{3.1}$$

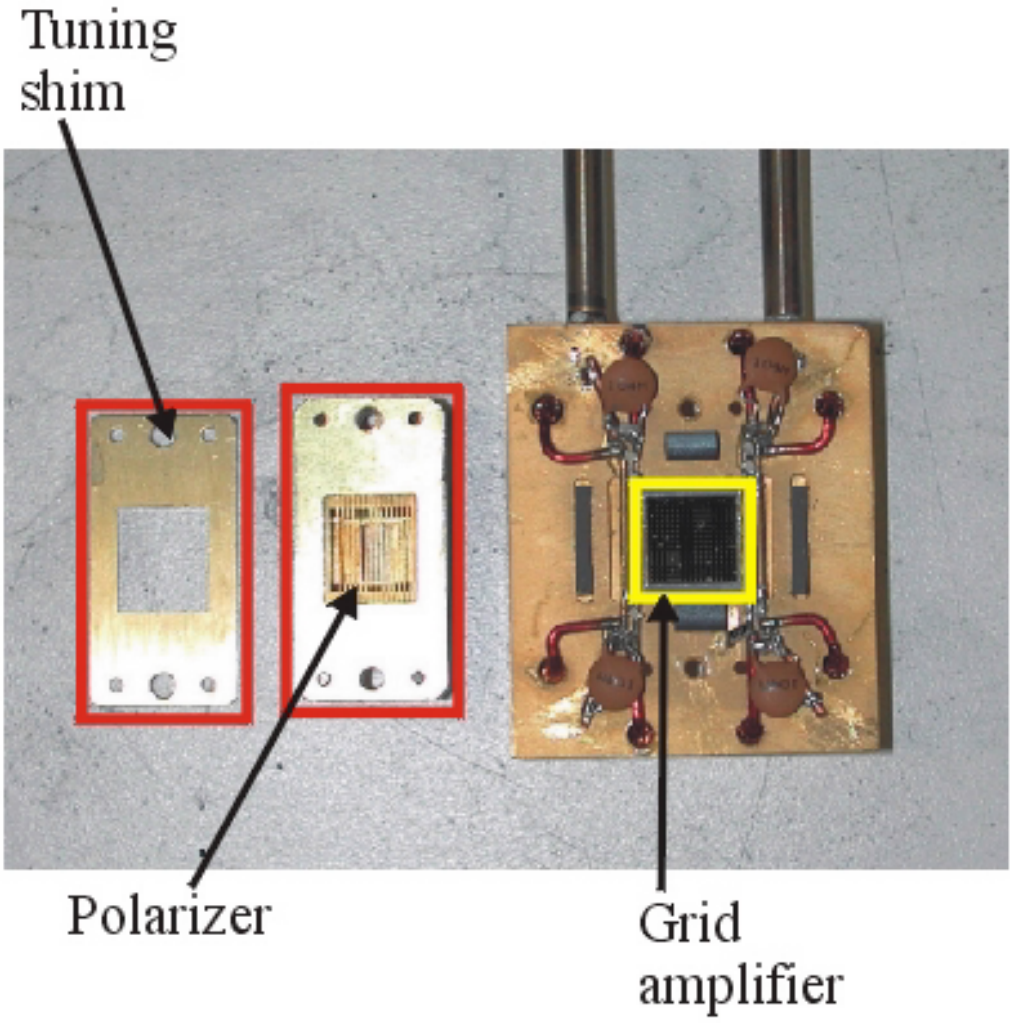


Figure 3.8: The fabricated mode-converter-fed-input active grid. The amplifier chip was the same design by Deckman et al. [2] and fabricated by Rockwell Scientific using their 0.18 μm pHEMT process on a GaAs substrate.

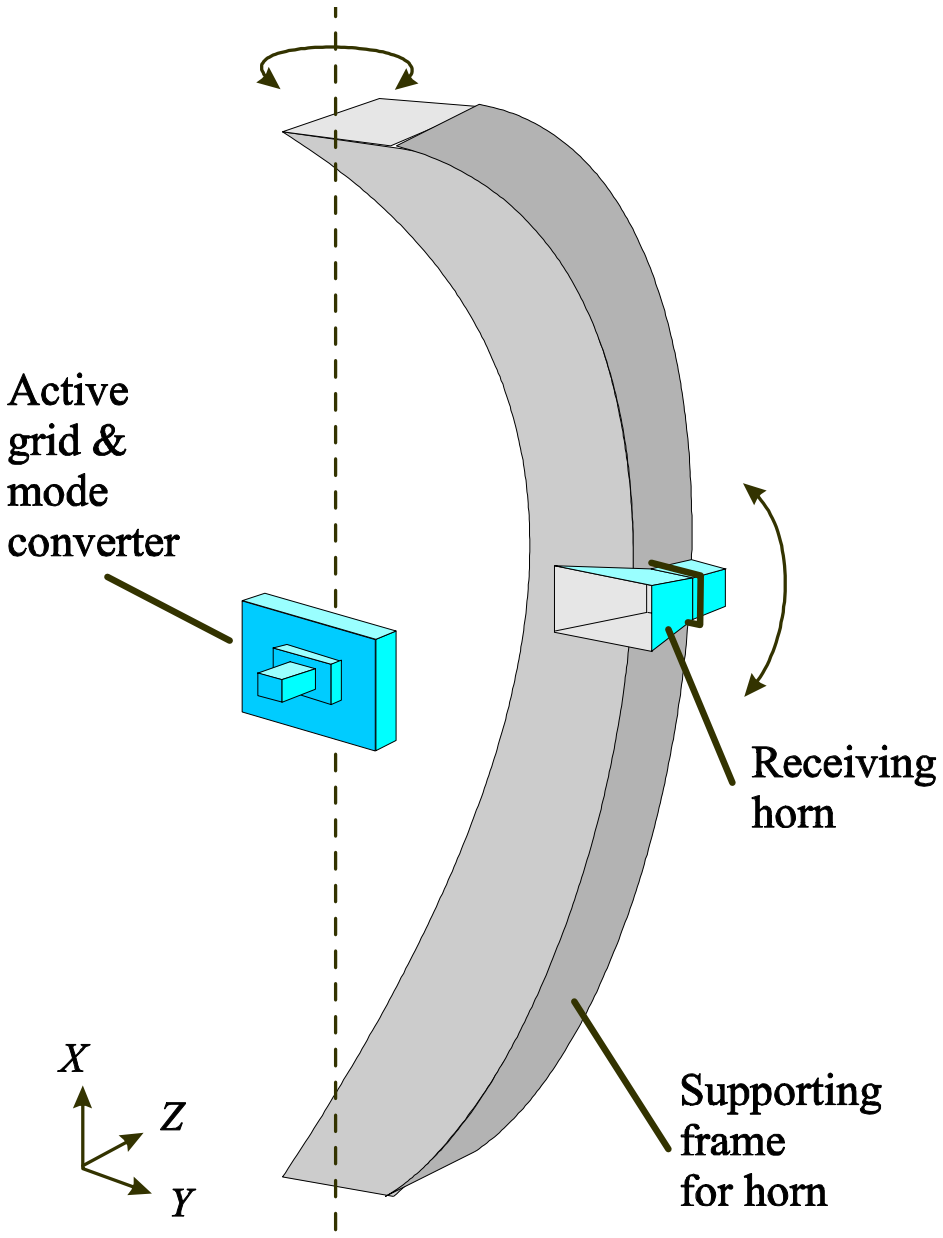


Figure 3.9: The receiving horn antenna is mounted on a semi-circular frame made of plastic and covered with absorber. The frame allows the horn to revolve around the amplifier so that the amplifier and its tuning elements can remain fixed. This technique prevents the amplifier and tuning elements from vibrating and hence improves the repeatability of the measurement.

where D_{trans} is the directivity of the array. The geometric area A_g of the grid, 100-mm square, was used to obtain

$$D_{trans} = \frac{4\pi A_g}{\lambda_0^2} \tag{3.2}$$

In order to have a repeatable measurement setup, the active grid assembled into the mode converter is mounted on a fixed pole and the receiving horn antenna revolves around it as shown in Figure 3.9. The supporting frame for the receiving antenna is made of plastic and covered with absorber. After measuring the active antenna gain of the overall packaged system using Friis transmission formula, we use equation 3.1 to calculate the gain and power of the grid.

3.2.3 Measurement Results

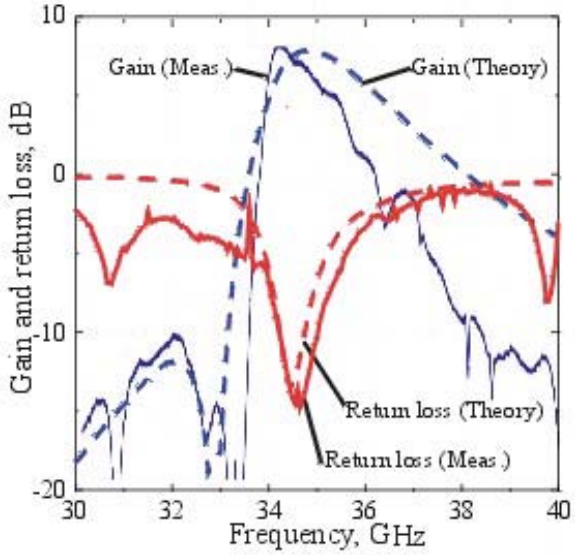


Figure 3.10: Simulated and measured small-signal gain and return loss.

The maximum small-signal gain is 7.5 dB at 34.4 GHz with a 5 % 3 dB bandwidth (Figure 3.10). The measured and calculated input return loss are also shown on the

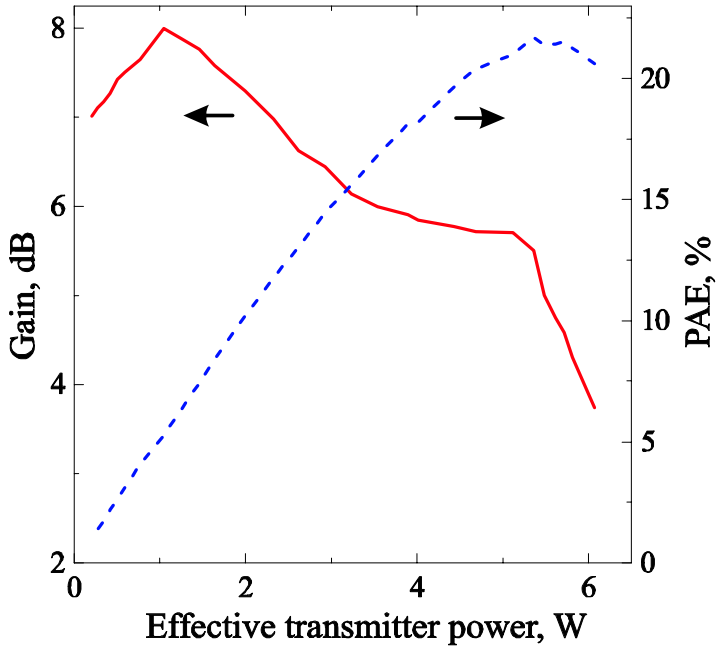


Figure 3.11: Measured gain and power-added efficiency (PAE) versus output effective transmitter power (ETP) at 34.4 GHz

same plot. The system gain and efficiency measured versus output power at 34.4 GHz is shown in Figure 3.11. The maximum power added efficiency (PAE) is 22 % with 5.4 W ETP and 5.5 dB gain. The third-order intermodulation was measured at 34.4 GHz with 10 MHz separation between two carrier tones, and the carrier to intermodulation ratio is plotted in Figure 3.12. The calculated third-order intercept from the measured data is 5 W. The measured AM-to-PM conversion is 10 °/W (Figure 3.13). The power, efficiency, and gain normalized by the physical aperture and free-space measurements previously made are compared in Table 3.1, and are shown to be similar.

The normalized antenna pattern is measured at 3 dB gain compression and 5.5 W ETP for the E and H-planes. It may be used to verify the assumption of using A_g for equation 3.2. As shown in Figure 3.14, the corresponding uniform field aperture size of the beam is bigger than 10 mm. Using the FDTD code and the equivalent circuit model developed in Chapter 2, the simulated and measured normalized radiation

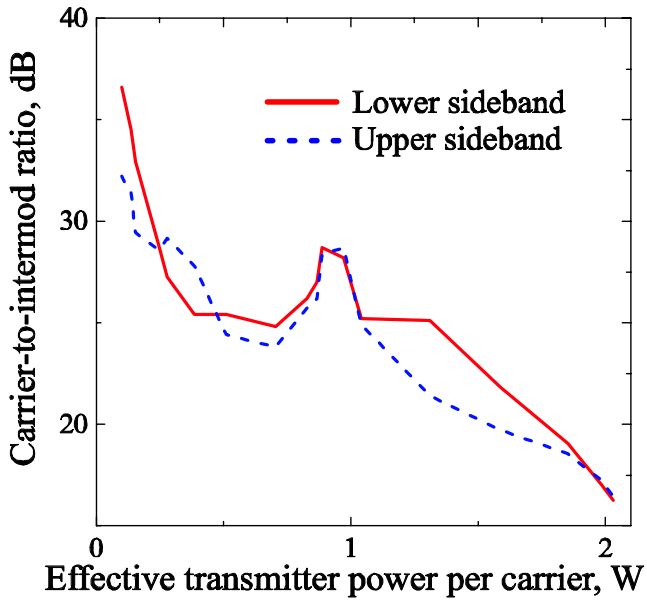


Figure 3.12: The third-order intermodulation measurement. The third-order intercept is at 5 W ETP.

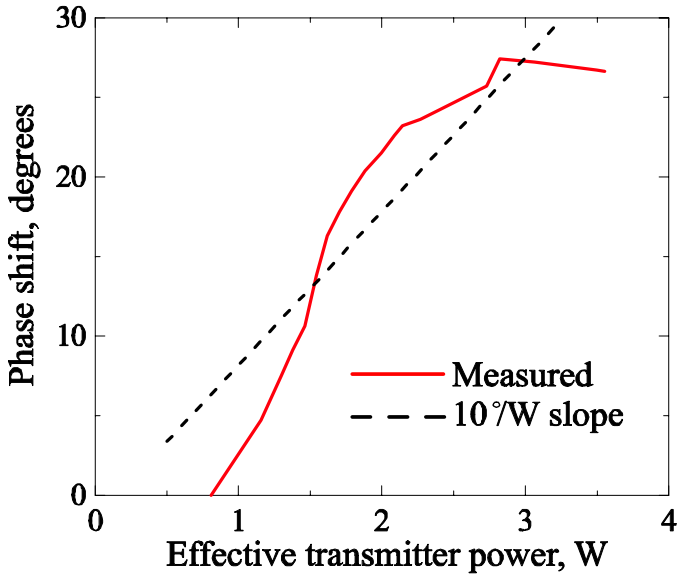


Figure 3.13: Measured and fitted AM-to-PM conversion. A line with a 10 °/W slope is shown for comparison.

	Free-space	Waveguide
Drain voltage, V	2.7	3
Drain current, A	6.5	5.6
Frequency, GHz	37	34
3–dB bandwidth, %	3.5	5
Maximum small signal gain, dB	8	7.5
PAE at 5W output, %	17	21
3rd–order intercept, W	32	5
AM–PM modulation, °/W	4	10

Table 3.1: Comparison of free-space gaussian-beam and waveguide mode converter measurements. The free-space data are taken from [2] and [4].

patterns of the E and H-planes are plotted in Figure 3.15. The plot indicates that the gain of the grid may be over-estimated by about 2 dB. According to the antenna gain obtained from this FDTD simulation, the ETP versus gain is renormalized and plotted with the previous normalization as a comparison in Figure 3.16. We think that this may be the result of the choke slots not completely stopping the RF current from leaking along the surface outside the grid. However, inserted ferrite beads or ferrite rubber do not alter the radiation pattern significantly.

There were spurious oscillations at 33.6 GHz with an effective isotropic radiated power (EIRP) of 23 mW (Figure 3.17). The radiation patterns of the oscillation are broad and we think the oscillation is a common-mode oscillation described in [5]. Therefore, we need a bigger common-mode stability factor in order to avoid oscillation due to process and mounting variations. The spurious oscillation is compressed at high ETP and is completely eliminated for ETP above 4.5 W.

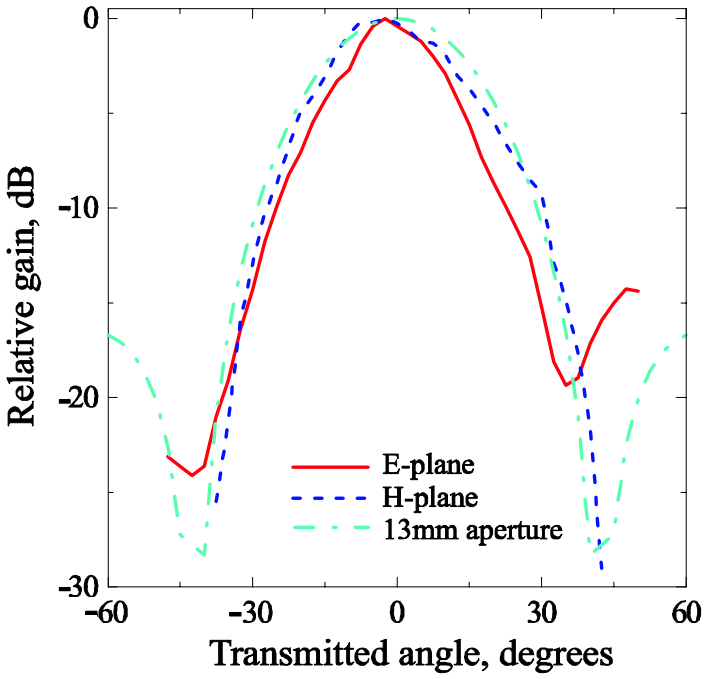
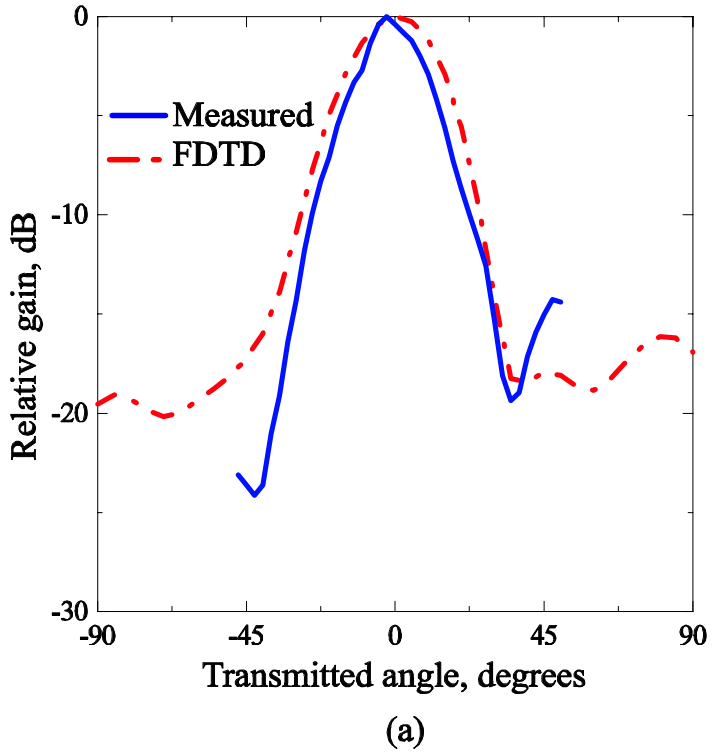


Figure 3.14: Measured normalized radiation pattern of the output radiating beam in E and H-planes. A 13 mm uniform field aperture is plotted for comparison.



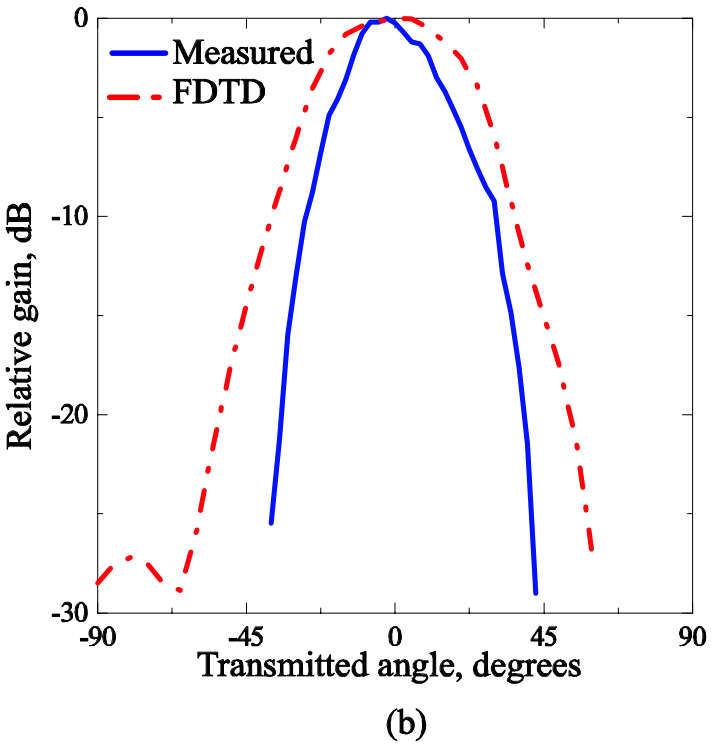


Figure 3.15: The FDTD simulated and measured normalized radiation patterns. The plots indicate that the normalization antenna aperture A_g may be bigger than 10 mm.

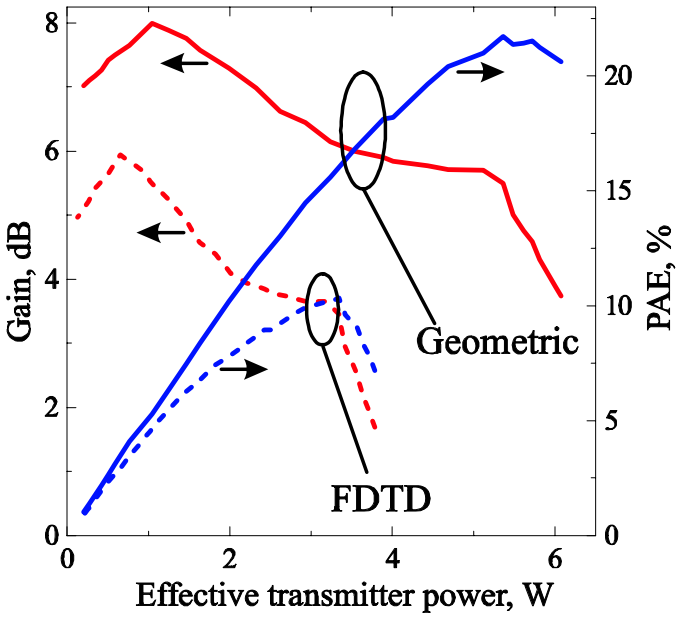


Figure 3.16: The system gain and PAE versus ETP for the grid with antenna gain obtained from geometric area and FDTD respectively. The geometric antenna gain is 2 dB lower than the results from FDTD. This may be the result of RF current, not completely stopped by the choke slots, flowing along the surface of the brass unit.

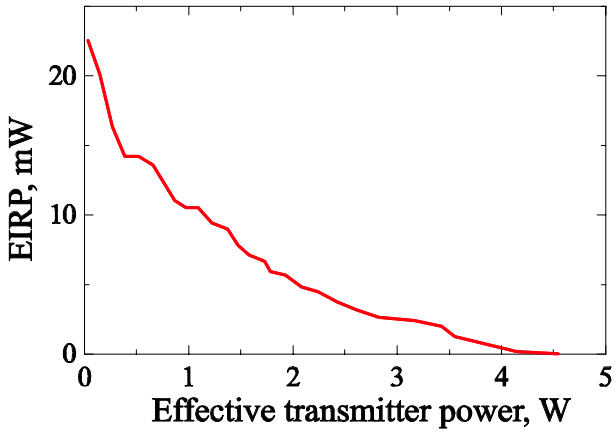


Figure 3.17: Effective isotropic radiated power (EIRP) of spurious oscillations at 33.6 GHz, plotted against carrier output power. The oscillation is suppressed at high output powers.

3.3 A Ka-band Grid Amplifier Packaged in Waveguide

3.3.1 Package Assembly

With the successful demonstration of the grid amplifier packaged for input, we proceeded to implement a grid amplifier packaged for both input and output. Figures 3.18 and 3.19 show the fabricated brass waveguide mode converter and the beryllium oxide (BeO) thermal spreader with via holes and DC-bias lines. In order to fabricate via holes on the thermal spreader, the thickness is limited to less than 1mm. Therefore, AlN, used in the previous amplifier, is replaced by BeO which has higher thermal conductivity. The chip that is mounted on BeO is the same as in the previous amplifier. We measured a chip with the gate biased to the source by a resistor (self-biased) and a chip with the gate biased by a gate voltage supplied by DC-bias (non-self-biased). The polarizer thickness and placement found in Chapter 2 are used as guidelines for tuning. The input and output polarizers are fabricated similar to the previous amplifier.

3.3.2 Measurement Results

The measured waveguide flange-to-flange small-signal scattering parameters for the self-biased and non-self-biased grid amplifiers are shown in Figures 3.20 and 3.21. The self-biased grid has a peak gain of 6.1 dB with 3 dB bandwidth of 1.4 %. It is biased at the drain with 2 V and 6.2 A. The non-self-biased grid has a peak gain of 6 dB with 3 dB bandwidth of 0.7 %. It is biased at the drain with 2.5 V and 7 A and gate voltage of 0.05 V. The small-signal gain for both chips are comparable with the results shown in the previous section. However, the measured power performance in Figure 3.22 shows that the 3 dB compressed output power for the self-biased and non-self-biased chips are 0.8 W and 0.65 W, respectively, and are much less compared to the previous measurements.

In order to investigate the problem, a free-space quasi-optical measurement was

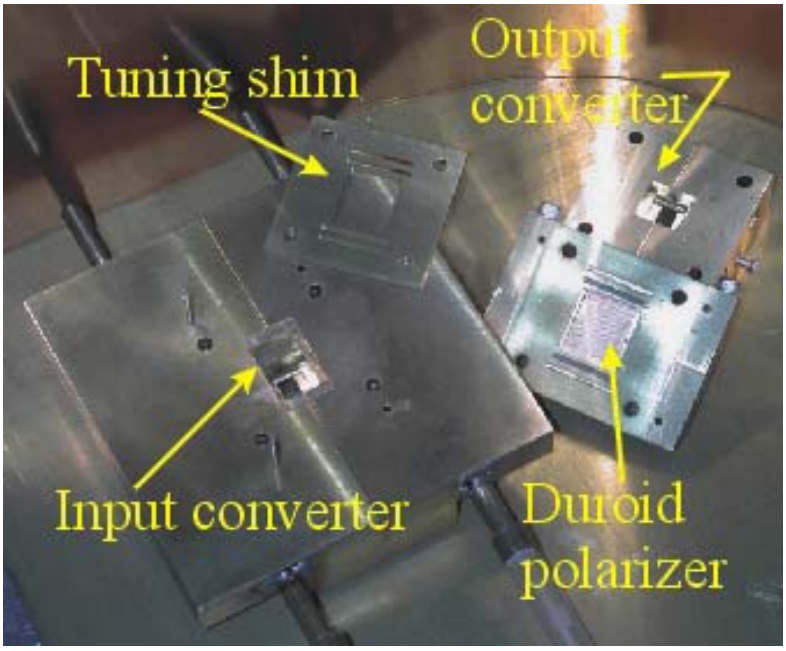


Figure 3.18: The input and output converters and the tuning shims. The input converter is also used for supporting the thin BeO thermal spreader and to remove heat from it.

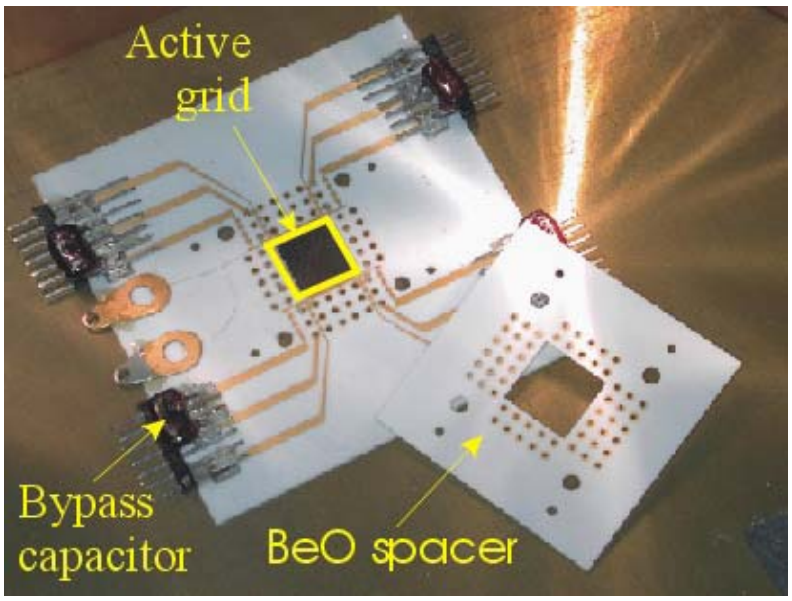


Figure 3.19: The grid amplifier mounted on BeO with the DC-bias lines and metalized vias. The bypass capacitors are to reduce RFI. The thermal spreader is 0.7 mm thick and the spacer is 0.5 mm thick.

performed for the non-self-biased chip. Figure 3.23 shows the power measurement with lens system loss correction at 31 GHz. The polarizers of the quasi-optical measurement are different from the waveguide measurement because of the difference in the surrounding environment. The beam waist was adjusted to be 2 cm, which is twice the size of the chip. The 3 dB compressed power is 1.6 W, which is also much less than the power reported in [2]. The discrepancy in output power is believed to be related to the degradation of the transistors. Due to design and fabrication delay of the mode converter and BeO thermal spreader, there are three months between dicing and testing of the chips. Nevertheless, the third-order intermodulation test for the self-biased chip was made. The third-order intercept of the amplifier is at 1 W output power.

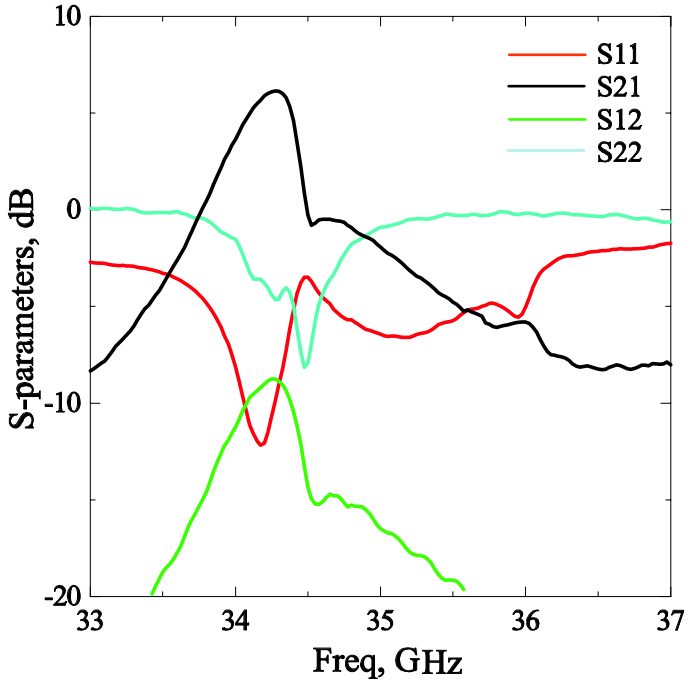


Figure 3.20: The measured scattering parameters for the self-biased grid. The maximum gain is 6.1 dB at 34.3 GHz. The 3 dB bandwidth is 1.4 %.

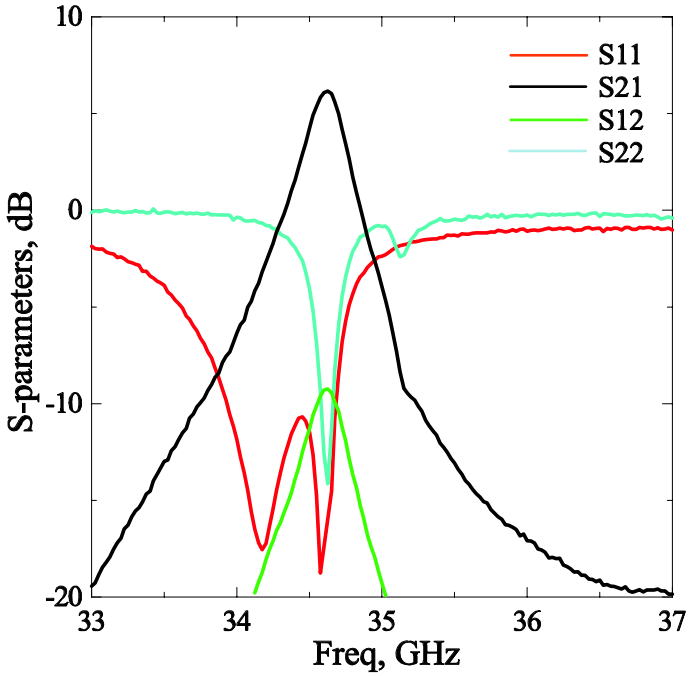


Figure 3.21: The measured scattering parameters for non-self-biased grid amplifier. The peak gain is 5.9 dB at 34.6 GHz. The 3 dB bandwidth is 0.7 %.

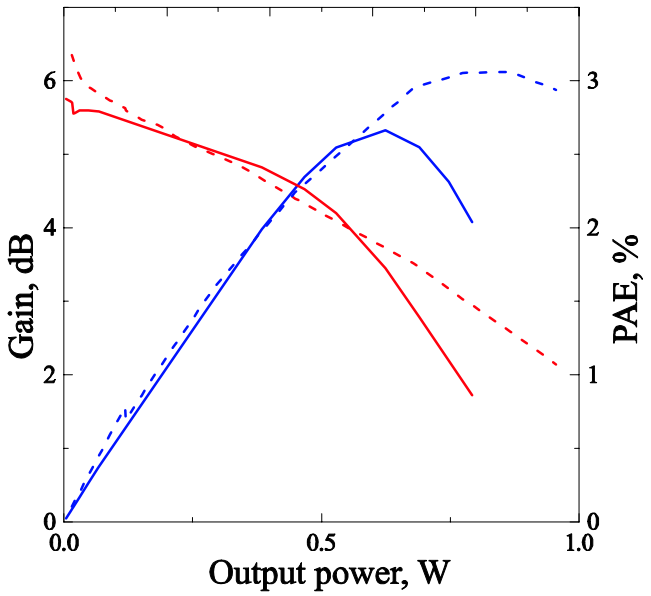


Figure 3.22: The measured gain and PAE versus output power for self-biased (dashed line) and non-self-biased (solid line) chips. The 3 dB compressed output power is 0.65 W and 0.8 W respectively.

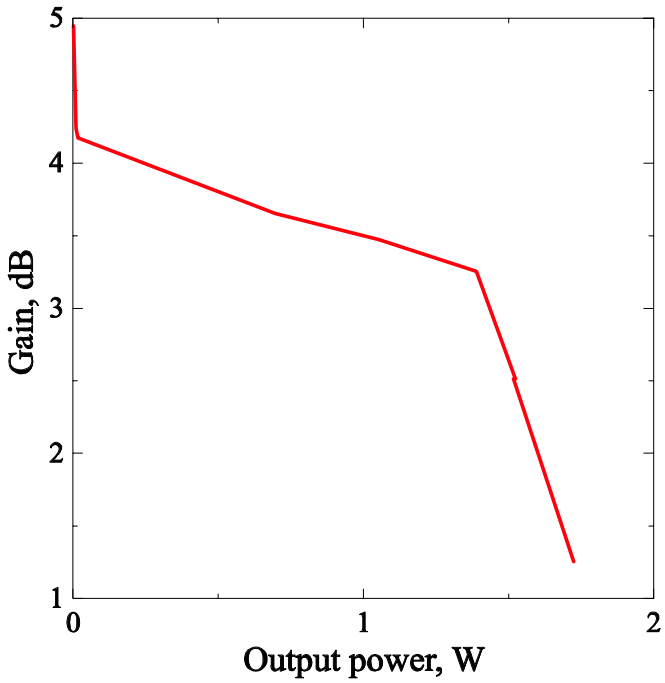


Figure 3.23: The free-space quasi-optical power measurement at 31 GHz for the non-self-biased chip measured in waveguide. The 3 dB compressed output power is 1.6 W.

Reference

[1] T. Kamei, H. Morishita, C-T Cheung, D. B. Rutledge, "Design of a Mode Converter for Quasi-Optical Amplifiers by Using 3-D EM Simulation Software," *IEICE Trans. Electron.*, vol. E84-C, 2001, pp. 955-960.

[2] B. Deckman, D. S. Deakin, Jr., E. Sovero, D. Rutledge, "A 5-Watt, 37-GHz Monolithic Grid Amplifier," 2000 Int. Microwave Symp. Dig., pp. 805-808.

[3] M. A. Gouker, "Toward Standard Figures-of-merit for Spatial and Quasi-Optical Array," *IEEE Trans. Microwave Theory Tech.*, vol. 43, 1995, pp. 1614-1617.

[4] J. Harvey, E. R. Brown, D. B. Rutledge, R. A. York, "Spatial Power Combining for High-Power Transmitters," *IEEE Microwave Magazine*, vol. 1, 2000, pp. 48-59.

[5] C. M. Liu, M. P. Delisio, A. Moussessian, D. B. Rutledge, "Stability of Grid Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 46, 1998, pp. 769-774.

Chapter 4

V-band Transmission and Reflection Grid Packaged in Waveguide

This chapter details the design, construction and testing of a transmission grid amplifier and a reflection grid amplifier at V-band. The monolithic chip was originally designed to operate at 60 GHz with 7 dB small signal gain. The chip consists of 100 unit cells and each unit cell uses two 200 μm transistors driven differentially. The transmission and reflection amplifiers assembled and tested showed 2 dB small signal gain at 57 GHz and 58 GHz, respectively.

4.1 Transmission and Reflection Amplifiers

The transmission approach has been used for many amplifiers [1]-[2] as well as for our work in the previous chapter. Recently, Guyette *et al.* [3] reported a reflection approach and measured 15 dB gain at X-band. A layout illustrating the two techniques is shown in Figure 4.1. In a transmission amplifier, the polarizer provides polarization isolation as well as back short tuning. The active grid provides gain and polarization rotation. In a reflection amplifier, the back short tunes the input and output. Polarization separation was done by a pair of cross-polarized horn antennas or an orthomode transducer.

For use with a transmission amplifier, polarizers can be fabricated either on low

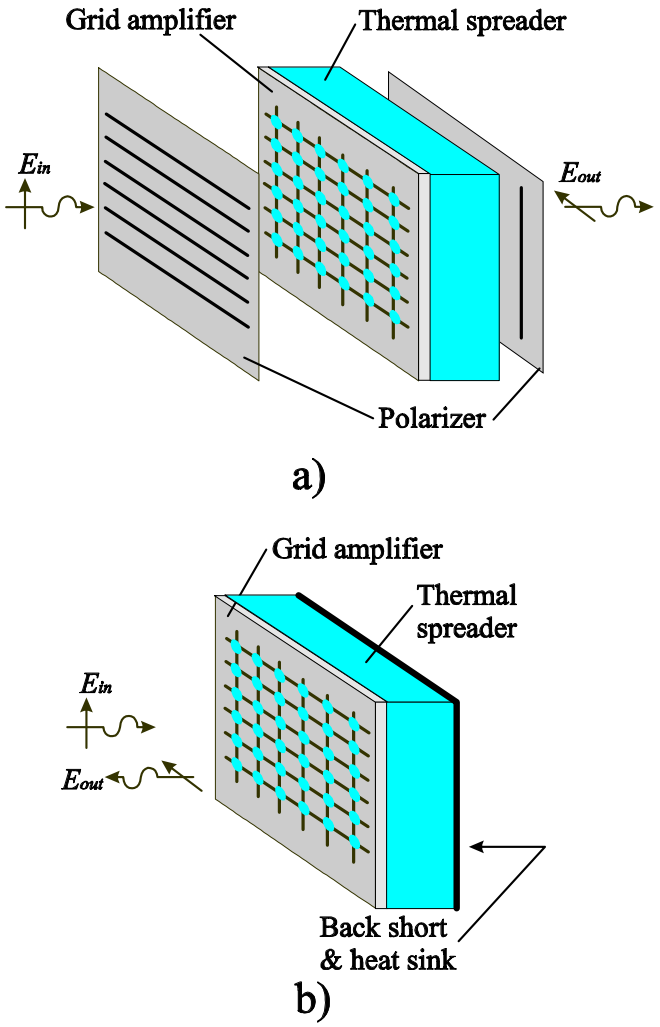


Figure 4.1: Layout of a) the transmission and b) the reflection amplifier. The polarizers of the transmission amplifier provide polarization isolation and back short tuning. The polarizers are replaced in the reflection amplifier by a dedicated back-short and a polarization isolation device at the input.

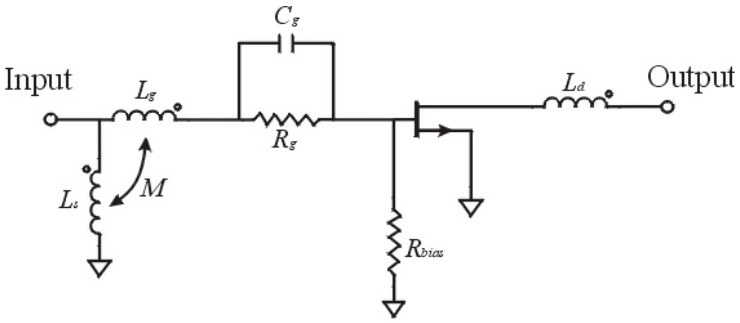
loss dielectric or metallic shim stock. The machining tolerance of the input and output mode converter can be looser because only one polarization is involved on each side. Drain and gate circuits can be tuned independently, allowing the two impedance to be different.

Reflection amplifies have excellent thermal performance as the substrate to which the active grid is mounted directly attaches to a heat sink. Additionally, input and output signals share the same over-moded waveguide section which reduces the size. However, in order to assure good matching and low leakage loss, the drain and gate impedance are preferably equal. This point will be further elaborated when we discuss the design of the package. Furthermore, the machining tolerance must be higher because the orthomode transducer has to maintain low cross-coupling. In this work, we designed a transmission grid amplifier and a reflection grid amplifier to study the advantages and limitations of each design.

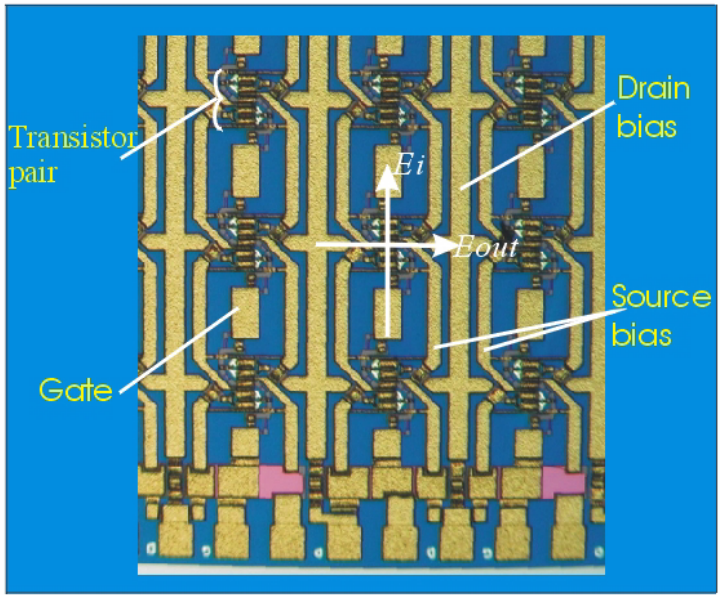
4.2 A V-band Single-stage Monolithic Grid Amplifier

The V-band amplifier is a single-stage 100-cell 60-GHz grid fabricated using the TRW 0.15 μm InP power HEMT process [4]. TRW's baseline InP process was modified from standard 75- μm thick to 125- μm final thickness in this work. Each cell contains a pair of transistors driven differentially. The design of this amplifier follows Preventza *et al.* [5]. Figure 4.2a shows the half unit-cell circuit. An 800-Ω resistor, R_g, in parallel with a 70-pF capacitor, C_g, at the gate provides stabilization of the transistor. The gate is biased by a resistor to source because of the gate leakage current. The photograph of a section of the fabricated 5-mm square chip is shown in Figure 4.2b. The thick drain and source bias lines are necessary to reduce metal loss and maintain a uniform bias across the grid. The height and width of a cell is 400 μm and the gate width of each transistor is 200 μm.

Figure 4.3 shows a thermal image of the chip at a drain bias of 0.7 V and 3.3 A. A



a)



b)

Figure 4.2: a) The circuit diagram of a half unit-cell and b) a photograph of a section of the fabricated V-band single-stage grid amplifier on an InP substrate with the TRW 0.15 μm HEMT process. The design of the circuit follows [5]. E_i and E_{out} indicate the input and output polarizations of the field. The unit-cell width and height are 400 μm.

heat sink and cooling fan were used to remove heat from the chip. The temperature distribution across the grid aperture is smooth and it indicates that the chip is biased uniformly and the thermal glue attached to the InP substrate without problems. The thermal resistance is found to be 3 °C/W between the grid surface and the brass mounting unit.

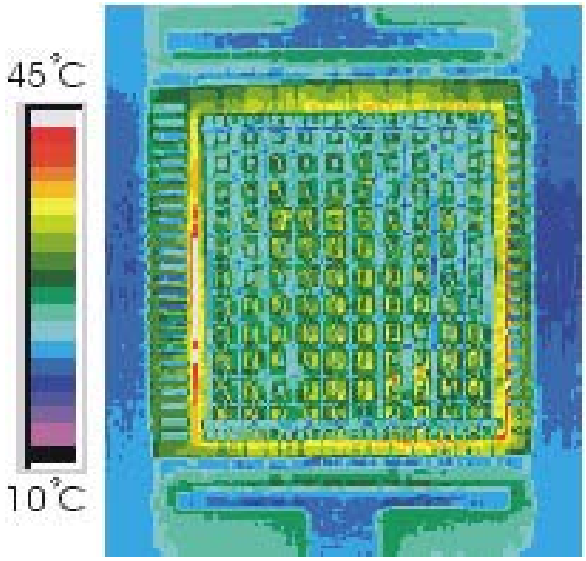


Figure 4.3: The thermal image was taken at a drain bias of 0.7 V and 3 A. The thermal resistance is 3 °C/W between the chip and the brass mounting unit.

4.3 A Transmission Amplifier

A transmission amplifier packaged by a mode converter at Ka-band has been demonstrated in the previous chapter. A drawing of the packaged waveguide grid amplifier is shown in Figure 4.4. The design of the V-band mode converter is very similar to its Ka-band counterpart. However, due to a smaller chip size relative to the standard waveguide, the air-filled over-moded waveguide section does not support the TE_{30} mode. Instead, we rely only on the edge of the chip to excite higher order modes. It should be noted that, while the area of the amplifier scales nearly inversely as frequency, the thickness of the substrate remains almost constant. Therefore, the edge

effect discontinuity for the V-band grid will be larger than its Ka-band counterpart. The optimization goal is to achieve high field-uniformity over the aperture of the grid. Choke slots and DC-bias-line filters are included in our simulation. Metalized vias were not used in this design because the wavelength is so short that the minimum achievable spacing between vias cannot prevent leakage. The final design has a length from input to output standard waveguide of about 2 cm.

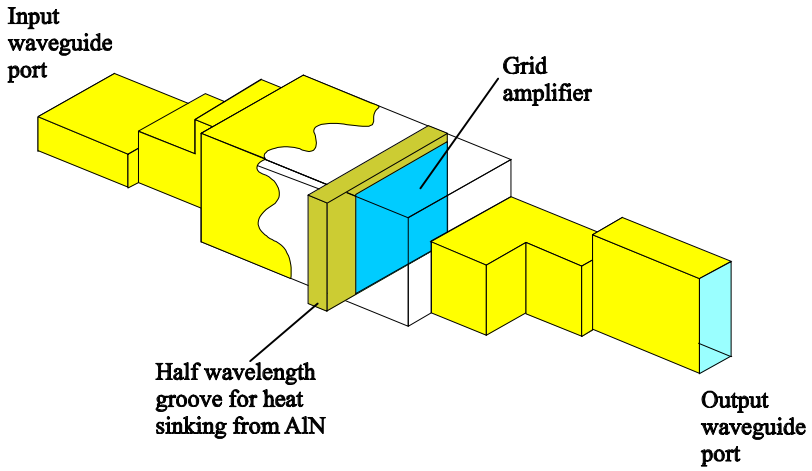


Figure 4.4: A drawing of the quarter-view waveguide packaged grid amplifier. The input and output are cross-polarized. The simulation includes a half-wavelength deep groove that is used for sinking heat from the AlN thermal spreader into brass unit.

The transmission grid amplifier brass units and duroid DC-bias board are shown in Figure 4.5. The AlN thermal spreader was set in a half-wavelength deep groove to provide a large area for transferring heat. The bias lines were wire bonded to the grid and bypass capacitors were used to reduce RFI. Duroid polarizers were placed in the over-moded waveguide sections. We used the simulations as a guide to where to put the polarizer sections. The grid was biased at 1.2 V with a drain current of 6.7 A. Figure 4.6 shows the measured scattering parameters of the amplifier. The measured maximum small signal gain for the transmission grid amplifier is 2.1 dB at 58.5 GHz. The positive gain bandwidth is 2 %.

The FDTD simulation developed in Chapter 2 was used to analyze this design, and the predicted system gain is compared to measured results in Figure 4.7. Since the

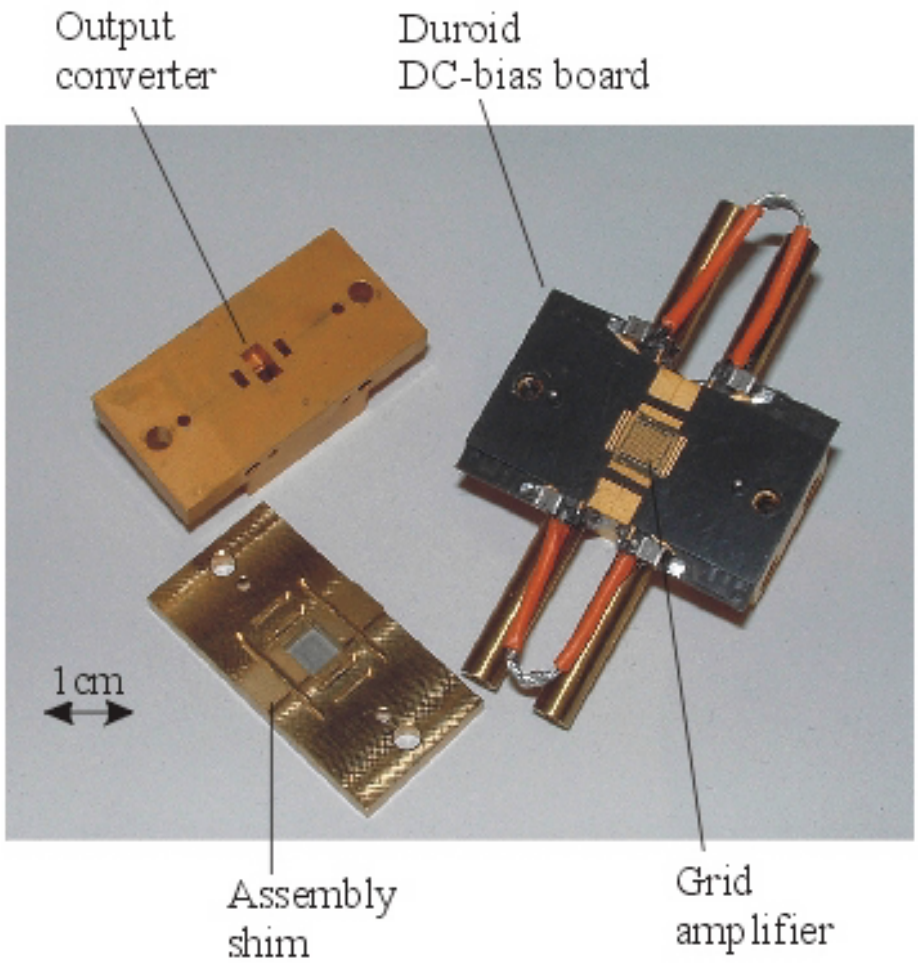


Figure 4.5: The fabricated transmission grid amplifier. A heat sink is installed at the back to remove heat.

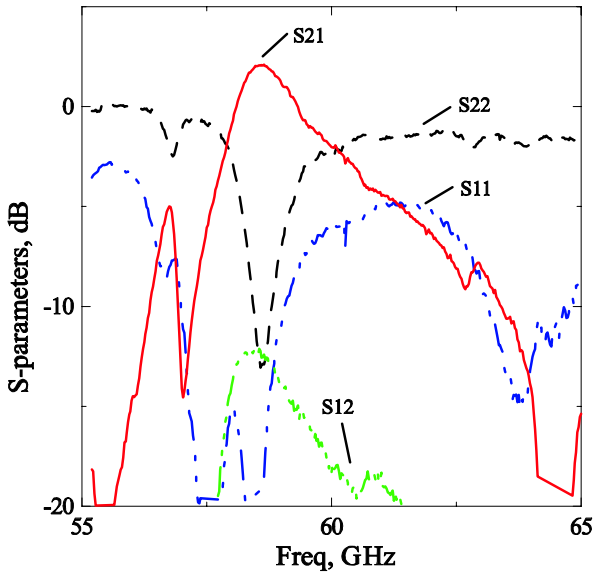


Figure 4.6: The measured scattering parameters of the transmission grid. The maximum small signal gain is 2.1 dB at 58.5 GHz. The corresponding input and output return losses are 19 dB and 13 dB, respectively.

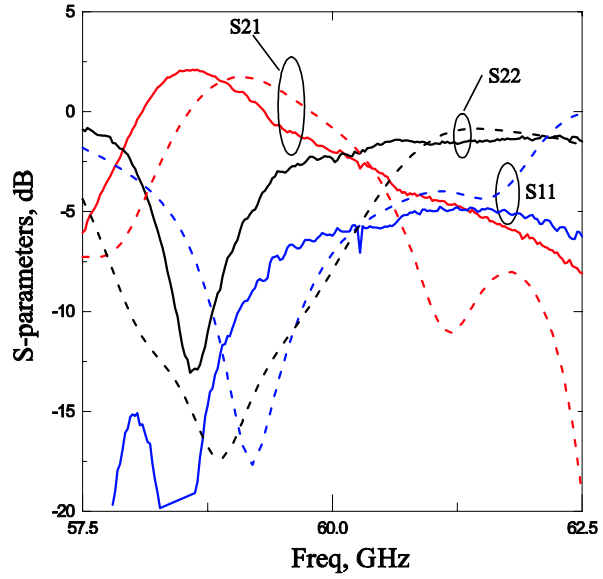


Figure 4.7: The measured (solid line) and simulated (dashed line) scattering parameters of the transmission grid amplifier. The predicted bandwidth and gain are similar to the measured results. The quantization error of the mode converter and dielectric thickness is the cause of the 0.5 GHz frequency offset.

anisotropic material model only matched between 55-60 GHz, the figure is limited to a narrower frequency range. The V-band amplifier chip model has a maximum stable gain (MSG) of 7 dB. The modeled waveguide is lossless and the DC-bias lines are not included in the simulation. Therefore, the low small-signal gain is believed to be a result of the field non-uniformity across the grid aperture. The FDTD simulation uses time step of 0.2 ps and uniform spatial step of 127 μm. The program spent about 1.5 hours to calculate the forward and reverse scattering parameters on a 2.4 GHz Intel PC. The equivalent HFSS simulation with frequency sweep and using impedance boundary conditions across the grid aperture took a similar amount of time.

4.4 A Reflection Amplifier

In order to feed a reflection grid amplifier, we need a mode converter that separates the two polarizations into two standard waveguide ports, as proposed by DeLisio *et al.* [6]. Furthermore, the converter should suppress unwanted higher order modes and give high return loss and low cross-coupling between polarizations. Figure 4.8a shows a drawing of a mode converter that excites only the TE_{10} and TE_{01} modes and couples to x and y-polarized standard waveguide. The dimensions of the intermediate waveguide section are chosen so that TE_{10} and TE_{01} modes combine efficiently before expanding into the over-moded waveguide section. This simplifies the design by restricting the optimizer from exciting higher order modes and compensate it with successive waveguide steps. The tuner section in Figure 4.8 provides a symmetric cutoff waveguide for E_x and a tuner for E_y. This tuner limits the –10 dB return loss bandwidth of E_y to about 7 %. On the other hand, due to similarity to a transmission mode converter, E_x can obtain a bandwidth of more than 10 %.

The bias striplines were designed as quarter-wavelength resonator band-stop filters suppressing leakage by 30dB between 52 and 65 GHz. The HFSS simulation included the effects of the filters. In addition, we chose the thickness of the AlN thermal spreader to help flatten the field distribution, taking the different propagation constants of the modes into account. Furthermore, the thermal spreader provides an

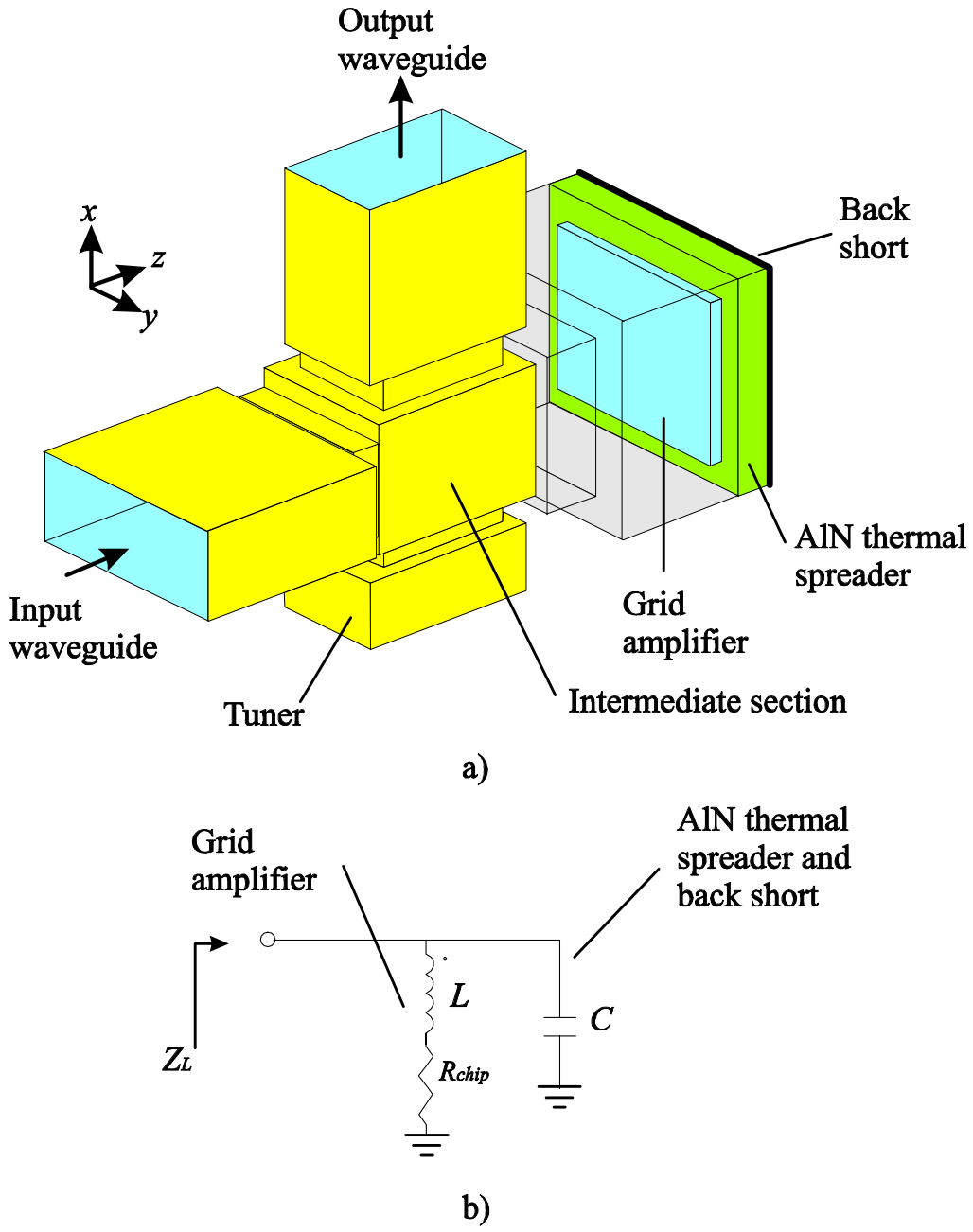


Figure 4.8: a) Layout of the mode-converter for the reflection grid amplifier and b) the lumped equivalent model of the grid amplifier with AlN thermal spreader and back short.

impedance transformation that can be understood as a simple resonator circuit as shown in Figure 4.8b. The typical output impedance of the chip looks like a series connected RL circuit. The back short resonates the inductor of the chip at the design frequency. Calculation shows that the impedance at resonance is equal to

$$Z_L = R_L = R_{chip} + \frac{\omega^2 L^2}{R_{chip}} \tag{4.1}$$

which transforms the load to a larger value. This provides the subsequent matching circuit from coupling the energy into losses along the over-moded waveguide and DC-bias lines. In order to take the full advantage of this method, the drain and gate conjugate matching impedances have to be similar in both real and imaginary parts, imposing additional constraints on the unit-cell level design. The designed mode converter has a length of about 1 cm.

The mode converter was fabricated in brass as shown in Figure 4.9. The calculated AlN thickness to give ideal impedance transformation is 635 μm. Since we only excited the fundamental mode for both polarizations, the distance between mode converter and grid amplifier was pre-determined and no waveguide shims were used. This also minimizes the possibility of misalignment and energy leakage. Figure 4.10 shows the measured scattering parameters for the reflection amplifier. The measured maximum small signal gain is 2.5 dB at 58 GHz. The positive gain bandwidth is 1 %. The grid was biased at 1.2 V with a drain current of 9 A.

Using the same anisotropic material developed for transmission amplifier simulation in the previous section, the measurement and simulation results of the reflection amplifier are shown in Figure 4.11 with good agreement. The time step is 0.2 ps and the spatial step is 190.5 μm. The simulation time was about 2 hours on a 2.4 GHz Intel PC.

The small measured system gain may be caused by field non-uniformity inside the over-moded waveguide section. Furthermore, it also suggests a necessity of an on-chip two-stage grid amplifier design for this frequency range. In addition, the bandwidth of the reflection amplifier is smaller than the transmission amplifier because the input

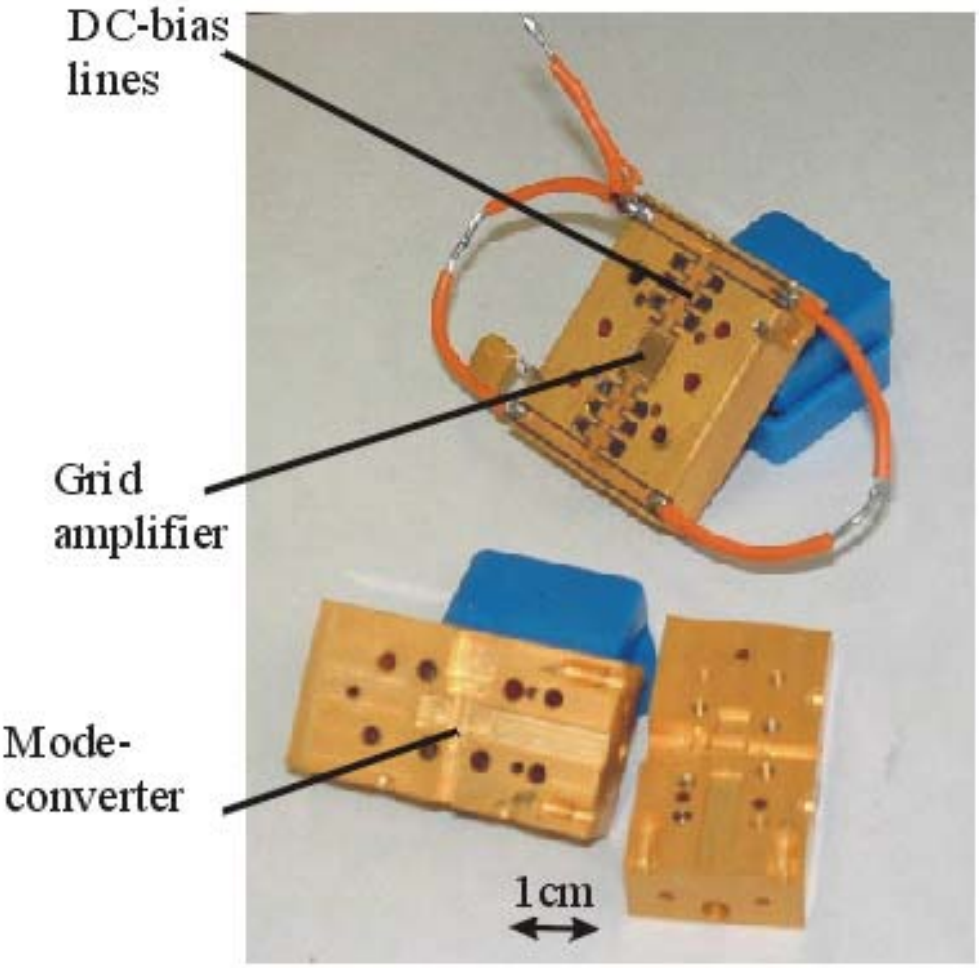


Figure 4.9: The fabricated reflection grid amplifier with mode converter and DC-bias lines.

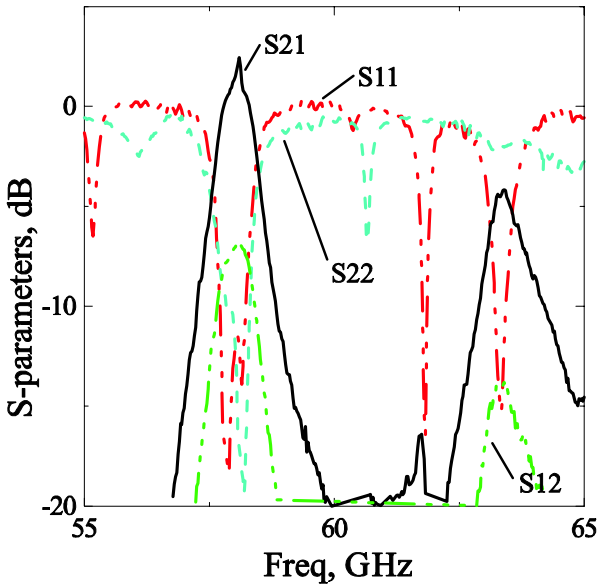


Figure 4.10: The measured scattering parameters of the reflection grid. The maximum small signal gain is 2.5 dB at 58 GHz. The corresponding input and output return losses are 13 dB and 17 dB, respectively. The bandwidth of the reflection amplifier is small because tuning slabs were used in both input and output following the mode-converter.

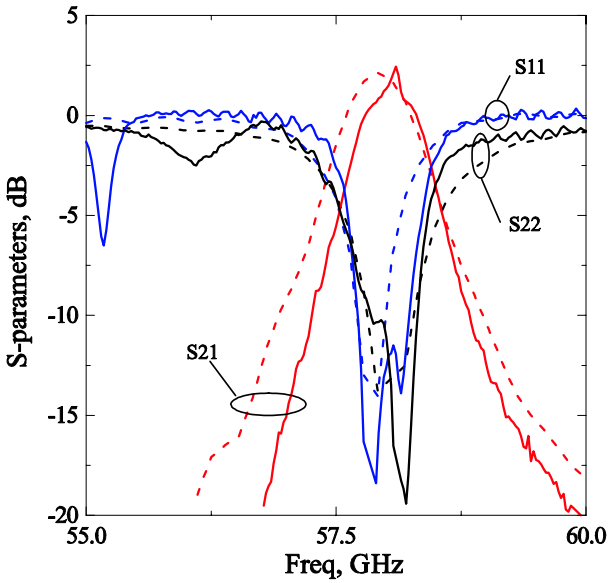


Figure 4.11: The measured (solid line) and FDTD simulated (dashed line) results. The low small signal gain as opposed to single unit cell ADS simulation is believed to be the result of non-uniform field distribution across the aperture.

and output cannot be tuned independently and proper matching requires additional tuning in the standard waveguide sections after polarization separation by the mode converter.

Reference

[1] B. Deckman, D. S. Deakin, Jr., E. Sovero, D. Rutledge, "A 5-Watt, 37-GHz Monolithic Grid Amplifier," 2000 Int. Microwave Symp. Dig., pp. 805-808.

[2] S. C. Ortiz, J. Hubert, L. Mirth, E. Schlecht, A. Mortazawi, "A High-Power Ka-band Quasi-Optical Amplifier Array," *IEEE Trans. Microwave Theory Tech.*, Feb 2002, pp. 487-494.

[3] A. Guyette, R. Swisher, F. Lecuyer, A. Al-Zayed, A. Kom, S.-T. Lei, M. Oliveira, P. Li, M. DeLisio, K. Sato, A. Oki, A. Gutierrez-Aitken, R. Kagiwada, J. Cowles, "A 16-Element Reflection Grid Amplifier with Improved Heat Sinking," 2001 Int. Microwave Symp. Dig., pp. 1839-1842.

[4] Y. C. Chen, D. L. Ingram, R. Lai, M. Barsky, R. Grundbacher, T. Block, H. C. Yen, and D. C. Streit, "A 95-GHz InP HEMT MMIC Amplifier with 427-mW Power Output," *IEEE Microwave & Guided wave Lett.,* Nov 1998, pp. 399-401.

[5] P. Preventza, B. Dickman, E. Sovero, M. P. DeLisio, J. J. Rosenberg, D. B. Rutledge, " Modeling of Quasi-Optical Arrays," 1999 Int. Microwave Symp. Dig., pp. 563-566.

[6] M. DeLisio, B. Deckman, J. Rosenberg, "Reflection Mode, Quasi-optical Grid Array Waveguiding System," patent pending (assignee Wavestream Wireless Technologies).

Chapter 5

W-band Two-stage Grid Amplifiers

From the previous chapter, we realized that at high frequencies the gain of the transistor may not be sufficient to overcome the effects of input and output matching loss and field non-uniformity. Two- or multiple-stages amplifiers can be implemented in two ways. We can either cascade several single-stage grid amplifiers in over-moded waveguide or put more than one stage on a single monolithic chip. The first option has the advantage of simplicity in terms of testing and verification. However, the control of higher order modes in long over-moded waveguide with multiple chips and bias circuits is rather difficult. The second option is more compact and potentially can re-use the same mode converter and over-moded waveguide matching and mounting designed for a single-stage amplifier at the same frequency. In this work, we detail the design and testing of a single-chip two-stage monolithic grid amplifier packaged in waveguide at W-band. We use a reflection type grid amplifier described in previous chapter with a new orthomode transducer mode converter for W-band. This work was a joint effort with visiting associates Dr. Jim Rosenberg and Dr. Mike DeLisio at Caltech, who were involved in design, simulation and layout of the grid amplifiers.

5.1 Two-stage Monolithic Grid Amplifier Chip

We considered the design of both cascode and cascade amplifiers (Figure 5.1). A cascode amplifier needs only one pair of bias lines to drive the differential stage similar to our original one-stage amplifier. Hence it allows us to use the same bias

circuit with no modifications. Unfortunately, the design was very sensitive to the capacitor connected to the gate for the common-gate stage (Figure 5.1a). A small variation could destabilize the circuit and it was determined to be unacceptable with the fabrication tolerance we had. The cascade amplifier requires, in principle, one bias line for each stage. This problem was overcome by allowing feedback between the stages. The feedback stabilizes the amplifier and provides bias for the first stage. Although the bias voltage is lower, the first stage also has a smaller signal to be amplified. It is because of the lower component sensitivity in general that we used a cascade amplifier topology.

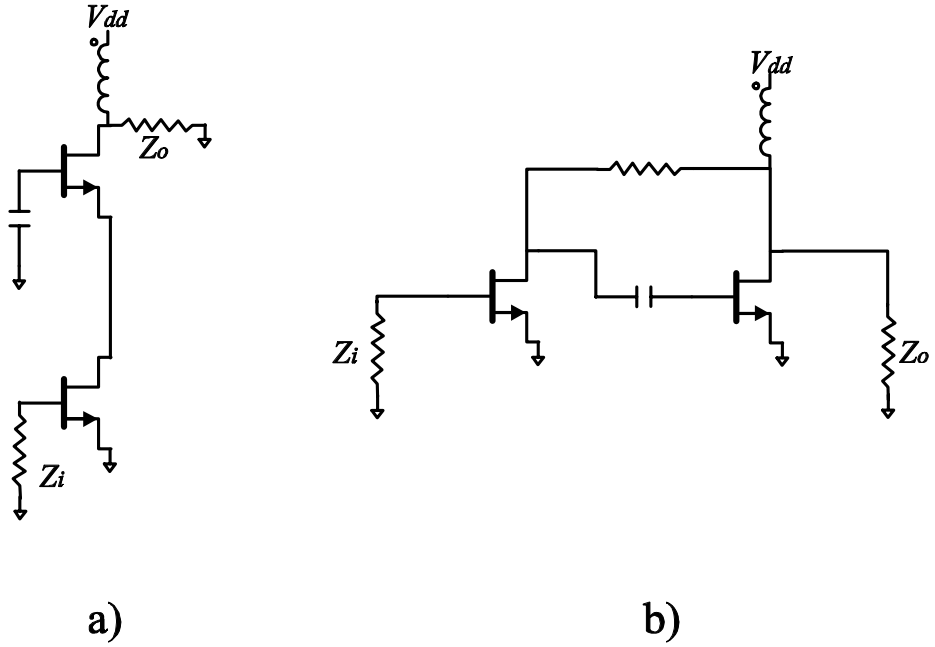


Figure 5.1: The circuit drawing of a) cascode and b) cascade amplifier. We use a cascade amplifier because of the relatively lower component sensitivity.

The input and output inductors coupling to free-space can be designed following Preventza [1]. However, the inter-stage reactance and the feedback could not be calculated accurately using Ansoft's High Frequency Structure Simulation (HFSS). It is because the calculation of these components need to use Floquet's theorem and periodic boundary conditions [2]-[3], which are not supported by HFSS, in order to

take into account the breaking of symmetry by the inter-stage and feedback circuit. Figure 5.2 illustrates this by showing the HFSS simulation for gate polarization. Since the inter-stage and feedback circuit are not symmetrical with respect to the excitation, E_{in}, a net differential coupling from the input lead to the inter-stage and feedback circuit exists. Therefore, the output differential circuit is not isolated from the input and vice versa. Hence, an estimated impedance sheet was added to the corresponding ports in the unit-cell simulation in order to represent the loading effects.

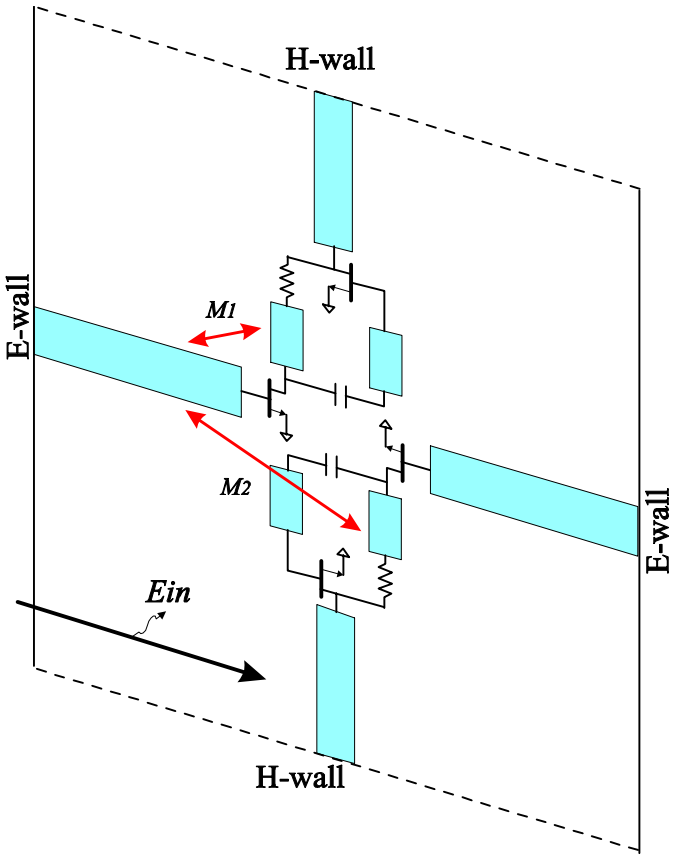


Figure 5.2: The HFSS simulation for unit cell with boundary conditions assigned for input polarization. There is a net differential coupling due to the breaking of symmetry of the inter-stage circuit. The effect of the loading of the output circuit is introduced by adding a shunt impedance loading at the output lead.

We designed two similar unit cells such that the larger cell is targeted at a lower frequency range while the smaller cell is for higher frequencies. (Figures 5.3 and 5.4). In addition, all the inter-stage components were kept within a source bias-line ring in

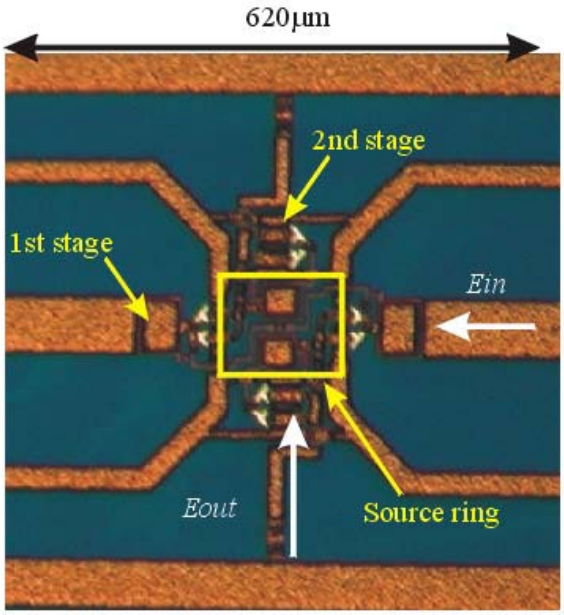


Figure 5.3: The layout of the fabricated cell of the two-stage cascade grid amplifier designed at 77 GHz. All inter-stage components are inside the source ring to avoid breaking the cell's symmetry and to reduce unexpected inter-stage coupling.

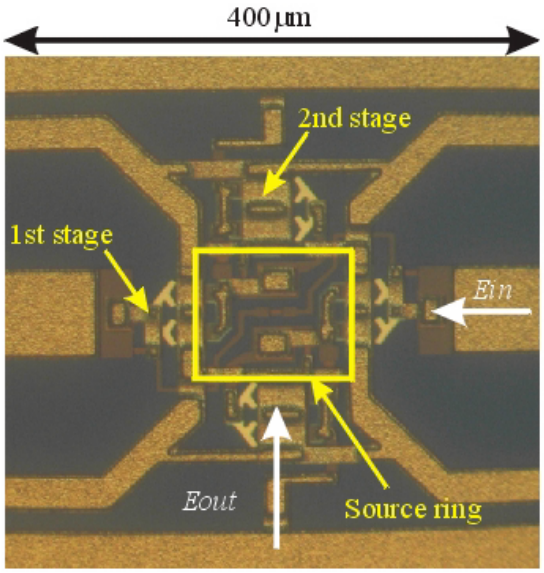


Figure 5.4: The layout of the fabricated cell of the two-stage cascade grid amplifier designed at 94 GHz. All inter-stage components are inside the source ring to avoid breaking the cell's symmetry and to reduce unexpected inter-stage coupling.

order to reduce the symmetry violation. In order to have an estimated output power of 1W, the transistor gate periphery needed was 150 μm for a 100-cell grid array. We also estimated that an 80 μm first stage transistor would be sufficient to saturate the second stage at 1 W output power. The gate of the first stage was controlled by an external gate bias voltage (non-self-biased) while the gate of the second stage was connected to the source through a 300 Ω resistor (self-biased). The TRW 0.15 μm HEMT process was used to fabricate this grid amplifier.

5.2 A W-band Reflection Grid Amplifier

The simulated drain and gate conjugate matching impedance of the cell are similar at 83 GHz. Hence, the converter and off-chip matching and tuning were designed for this frequency. Nevertheless, the simulated maximum stable gain at 83 GHz was 10 dB. The design of the reflection grid amplifier at W-band was similar to the V-band design (Figure 5.5). The ortho-mode transducer mode converter was designed using HFSS. The design goal is to excite the TE_{10} and TE_{30} modes in the appropriate ratio for both polarizations and maintain a low cross-coupling level. An intermediate section was used, as in the previous chapter, to combine the TE_{10} and TE_{01} modes efficiently before expanding into larger over-moded waveguide sections. In this case, since the ratio of the over-moded waveguide to the standard WR-10 is bigger than the V-band counterpart, two additional waveguide steps followed the intermediate section.

The impedance transformation technique in the previous chapter could not be used because of additional higher order modes and the field flatness requirement. Instead, the AlN thermal spreader was used as quarter wavelength transformer and the back short was set to one quarter wavelength away from the grid amplifier. The disadvantage of this method is that heat cannot be transported from the grid to the metallic back short through the AlN. Furthermore, one quarter wavelength at 83 GHz inside AlN is about 300 μm and the InP substrate, which has a dielectric constant of 12, is 127 μm thick. Therefore a 3/4 wavelength thick thermal spreader was used in order to dissipate 10 W of estimated waste heat from the grid. In order to enhance

the heat dissipation efficiency, a 1/2 wavelength groove was used to provide bigger contact surface area between the waveguide and the thermal spreader (Figure 5.5). DC bias line filters were also designed for 80-90 GHz to suppress leakage.

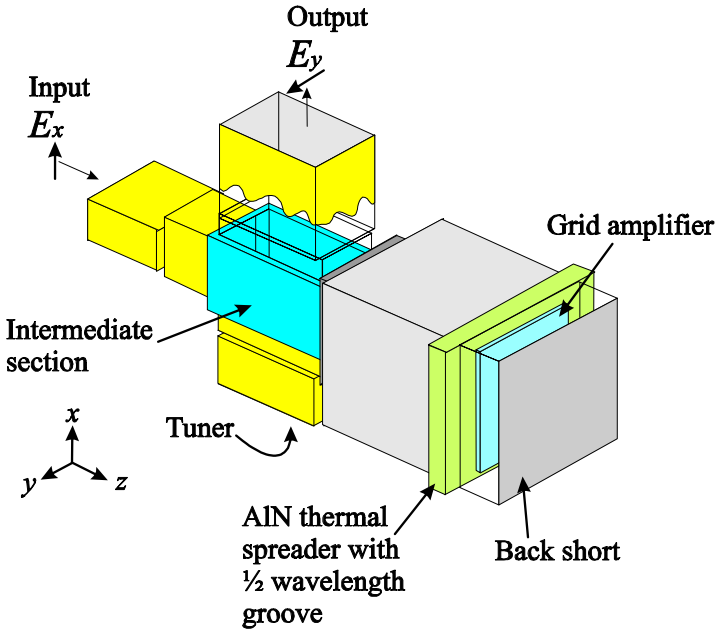


Figure 5.5: Layout of the mode converter, thermal spreader and the chip. The thermal spreader was not mounted on the back short to obtain better input and output matching.

5.3 Amplifier Assembly and Measurement Results

Figures 5.6 and 5.7 show the brass made mode converter and the fixture for holding the AlN thermal spreader. The brass fixture was gold plated to allow wire bonding the source of the chip to the chassis. The AlN was attached to the brass fixture by the same technique used in Chapter 3 for the waveguide input, radiating output mode converter. Over-moded waveguide shims were used for tuning the distance between the converter and the active grid. The DC bias line filters were fabricated on 254 μm thick Duroid with relative permittivity of 2.2. Bypass ceramic capacitors were soldered to the bias pads to prevent RFI. Finally, the InP chip was mounted on

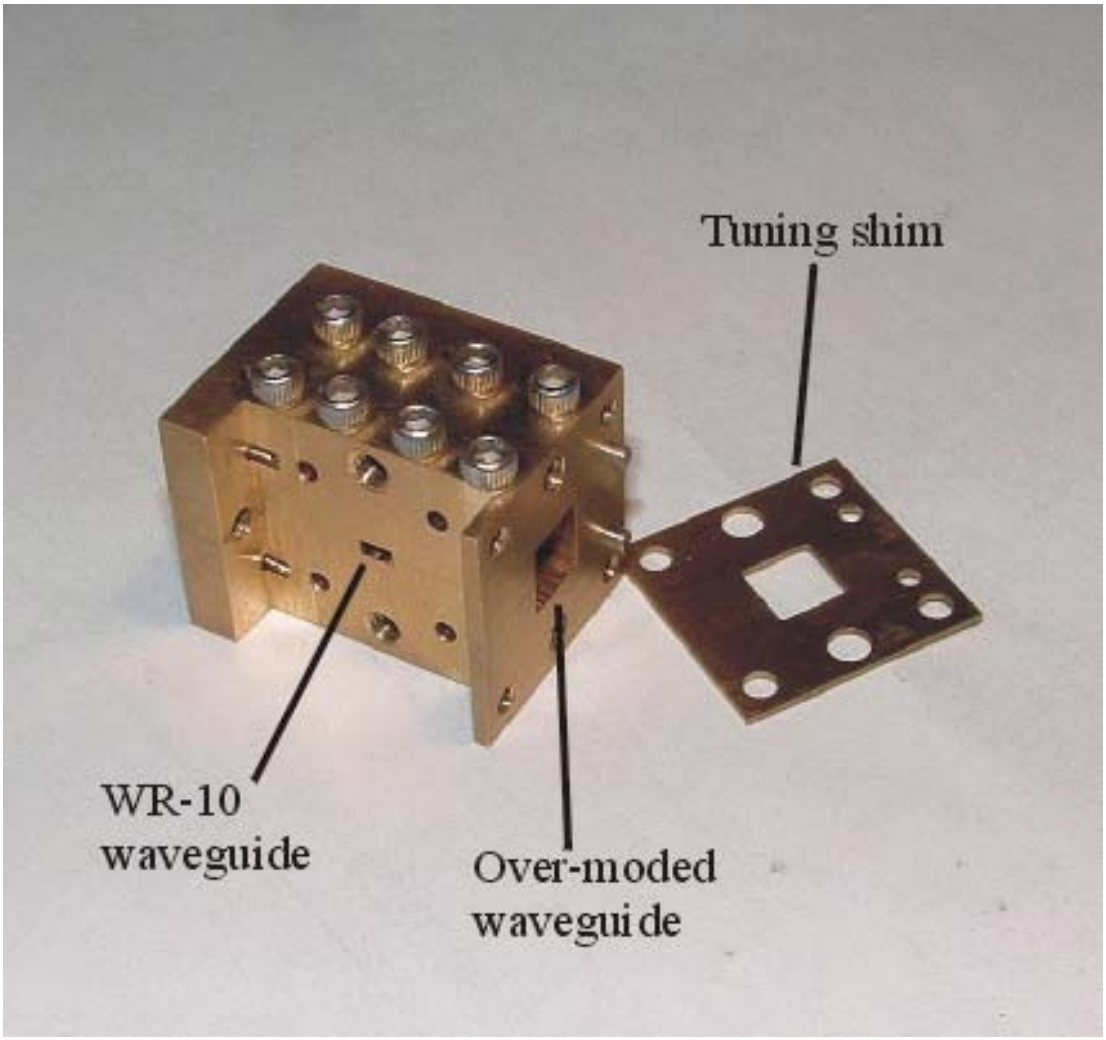


Figure 5.6: The fabricated mode-converter and the tuning shim. The shim adjusts the distance between the converter and the active grid.

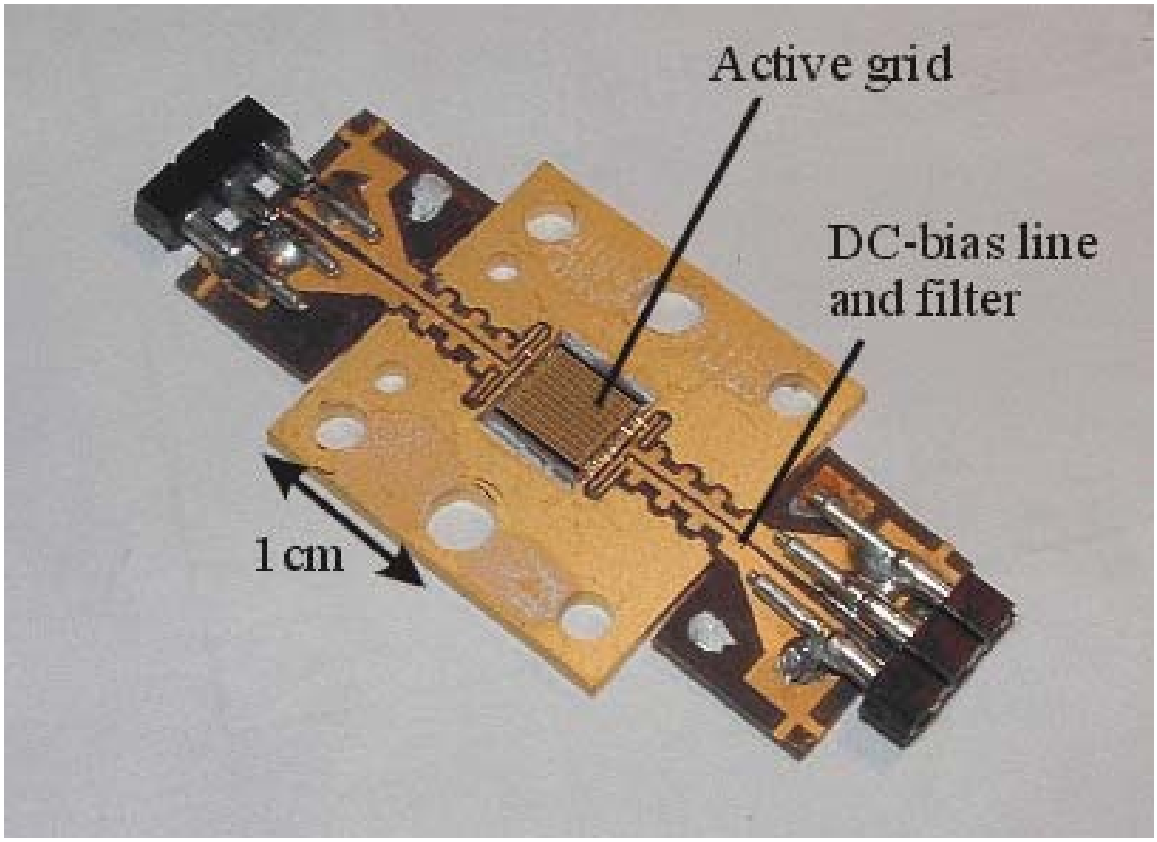


Figure 5.7: It shows the brass unit for thermal spreader and chip mounting. The two-stage InP grid amplifier was mounted at the center. DC-bias-line filters were used to reduce leakage.

AlN using thermal glue and wire-bonded to bias lines for DC bias. The assembled unit has a size of about 2 cm ×2 cm × 2.5 cm.

Figure 5.8 shows the thermal image of the grid measured with drain voltage and current of 0.352 V and 3.0 A, respectively. The temperature variation across the grid is due to thermal glue non-uniformity. Measurement shows that the thermal resistance between the grid and brass chassis is about 3 °C/W. The result implies that we need to maintain the chassis below 10 °C in order to prevent over-heating at full bias. Therefore, dry ice is used throughout the measurement to cool down the chassis.

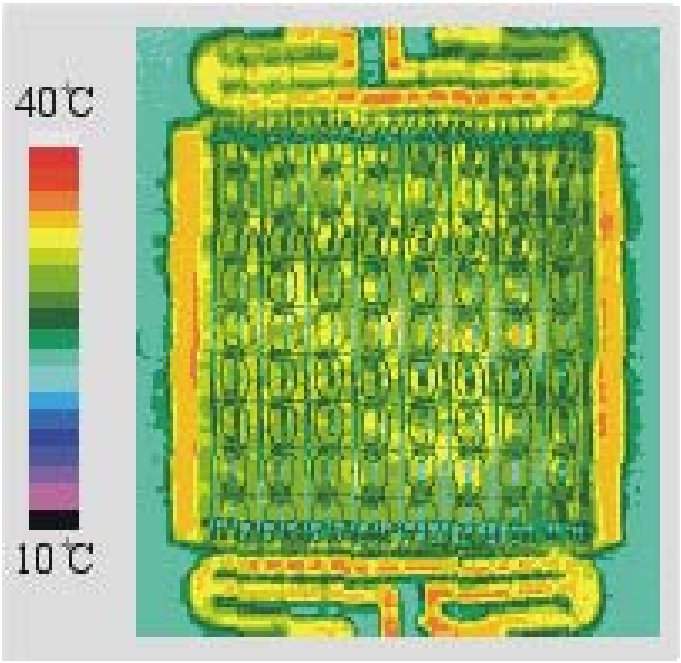


Figure 5.8: The thermal image of the active grid with drain bias voltage of 0.352 V while the drain current is 3.0 A. The temperature variation across the grid is due to the thermal glue non-uniformity under the active grid.

The measured small-signal gain for the larger cell is 2.7 dB at 82.1 GHz with a positive gain bandwidth of 0.37 % (Figure 5.9). This narrow bandwidth is due to a small gate input impedance of the cell and required two duroid tuning slaps, which had dielectric constant of 10.2 and 2.2, respectively, in the standard waveguide. The gate of the first stage amplifier is biased at -0.1 V while the drain is biased at 1.8 V. The total DC power consumption is 11.5 W.

We also tested the smaller cell design and it gives no small-signal gain. The failure of this design is believed to be the improper simulation of the loading effects. While the same problem exists for the larger cell, the breaking of symmetry is substantially less because of the ratio of the area of the source ring to cell area is smaller. Therefore, the cell size should be large enough to minimize the breaking of symmetry. Nevertheless, we have demonstrated a two-stage monolithic grid amplifier packaged in waveguide using reflection approach.

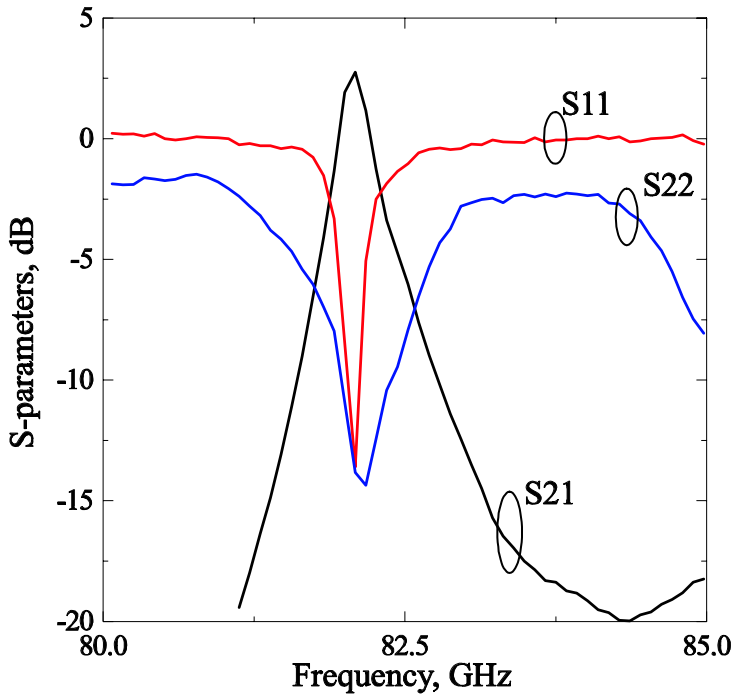


Figure 5.9: Small-signal scattering parameters of the two-stage grid amplifier. The gain is 2.7 dB at 82.1 GHz with 0.37 % bandwidth.

Reference

[1] P. Preventza, B. Dickman, E. Sovero, M. P. Delisio, J. J. Rosenberg, D. B. Rutledge, "Modeling of Quasi-Optical Array," 1999 Int. Microwave Symp. Dig., pp. 563-566.

[2] R. E. Collin, "Foundations for Microwave Engineering," 2^{nd} Edition, *Mc Graw-Hill, Inc.*, 1992, pp. 569-571.

[3] N. Amitay, V. Galindo, C-P Wu, "Theory and Analysis of Phased Array Antennas," *John Wiley & Sons, Inc.*, 1972.

Chapter 6

Conclusions and Future Developments

6.1 Conclusions

Since Mink [1] first proposed the idea of quasi-optical power combining, researchers have resolved many technical problems and learned the advantages and limitations of various active grid topologies, configurations and packaging issues.

As shown in previous chapters, we detailed the design and testing of grid amplifiers packaged in waveguide. In particular, our method used over-moded metal waveguide with pre-selected mode excitation to achieve uniform field distribution for grid amplifiers. In Chapter 3, we demonstrated that higher order modes can be excited and controlled in order to flatten the fields at a selected plane. A grid amplifier with its input packaged in waveguide, and another fully packaged in waveguide were demonstrated with small-signal gains of 7.5 dB and 6 dB. An output power of 5.5 W was measured with the first amplifier which is comparable to the results reported in [2]. Although the output power of the second amplifier was only 0.6 W, diagnosis revealed that the amplifier chip we used was low in output power. In Chapter 4, we demonstrated the transmission and reflection approach of grid amplifier packaging. Both amplifiers had 2 dB small-signal gain, which appeared to be the results of non-uniformity of the fields and low single-stage gain for amplifiers at V-band. In order to resolve the low single stage gain for grid amplifiers at higher frequencies, we

designed and demonstrated a two-stage monolithic grid amplifiers in Chapter 5. The measured small-signal gain is 2.7 dB at 82 GHz. Although the gain is not substantially higher, the frequency of operation of this amplifier is much higher than the V-band counterpart.

As shown in our work, the grid amplifier packaging problem is tied tightly to the design of the grid amplifier itself. With careful consideration of field-uniformity, matching and thermal management, and applying proper simulation methods, grid amplifiers can be packaged in a compact, low cost waveguide unit at microwave and millimeter-wave frequencies.

6.2 Future Developments

We may pursue several different directions in our developments of grid amplifiers. Firstly, simulation and characterization methods for two- or multi-stage grid amplifiers on a single substrate are needed. Better use of geometrical symmetry and circuit topology may also be an alternative solution to the lack of appropriate simulation tools. A design that may posses this characteristic will be presented. Furthermore, as we have seen in the previous chapters, the power-added efficiency (PAE) of grid amplifiers under class-A operation is inherently low. As soon as we are able to design two or multi-stage amplifiers, higher efficiency operating classes such as class-C or E may be utilized. Secondly, we should expand our 1-D FDSS code, which is unconditionally stable, to full 3-D simulation. Since this method is unconditionally stable, it is also suitable for the prediction of large signal behaviors of grid amplifiers and oscillators. Further discussions and simulation results of 1-D FDSS for an oscillator will be presented in the following section.

6.3 Unit-cell Modeling of a Two-stage Amplifier

As shown in Chapter 4, at higher frequencies, the gain of a single unit cell is too low. This low system gain can be resolved by either reducing the return loss of

the passive waveguide and matching circuits or increasing the gain of the unit cell. The first approach is limited by the design of the mode converter that needs to satisfy higher order mode excitation and matching constrains. The second approach, which we demonstrated in Chapter 5, opens up the opportunity of making a highly integrated amplifier module on a single substrate with system gain that is comparable with MMIC amplifiers. The design in Chapter 5 did not perform as well as initially expected which was due to the lack of appropriate simulation tools and insufficient understanding of two-stage grid amplifier design.

Since the design of the unit-cell with inter-stage circuitry needs to have both polarizations, the solution is to write simulation software that incorporates periodic boundary conditions. However, under the current situation, we decided to remove the feedback of the cascade amplifier in Chapter 5 in order to prevent the coupling between stages and hence the ambiguity of the loading effect.

Figure 6.1 shows a layout of the new two-stage amplifier unit cell. The upper second stage transistor output radiates a current I_1. There is inductive coupling between the bias lines such that an induced current I_2 flows out of the first stage transistor. However, the lower second stage transistor generates an equal-magnitude opposite-phase current component under differential operation. Therefore, at node N, the net current coupling into the first stage transistor is theoretically zero. Furthermore, these bias lines act as shunt inductors for the first stage drain output which become part of the inter-stage matching as shown below.

The design of the inter-stage matching can be simplified when there is no inter-stage feedback. Figure 6.2 shows two lumped element matching circuits designed by the method in Pozar [3]. We used the design in Figure 6.2b for the inter-stage matching because of the topology we chose above and the difficulty in realizing the component values of the first design. Furthermore, this design already includes an isolation capacitor to separate the bias between the two stages. We applied the method proposed by Preventza *et al.* [4] for the input and output. The difference from the previous single-stage design is that the output of the second stage will have a parasitic inductor similar to the input. In addition, we extracted parasitic capacitors

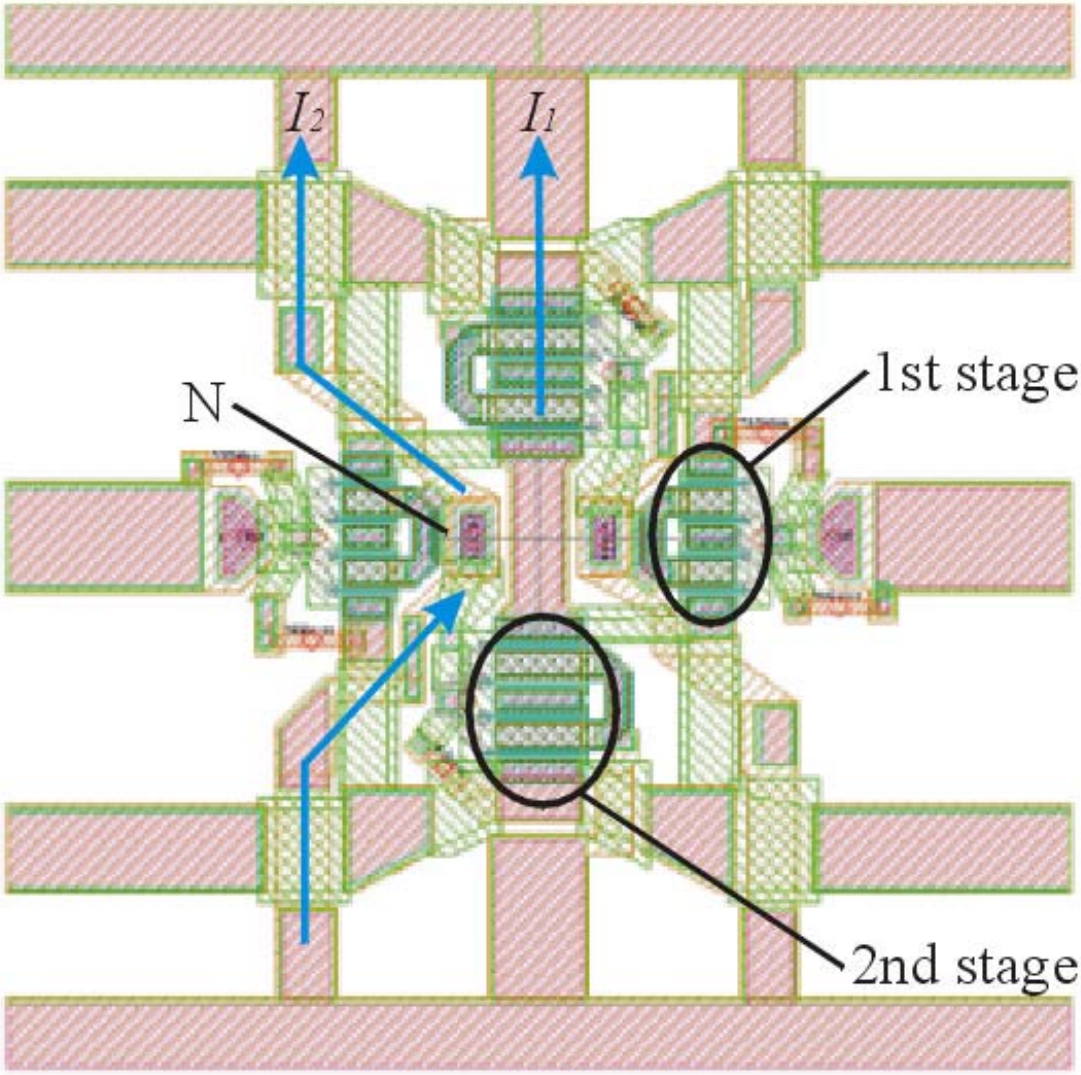


Figure 6.1: Biasing the first stage as shown avoids feedback by using the symmetry of the layout and the differential operation of the transistor pair. At node N, no net current couples into the drain of the first stage.

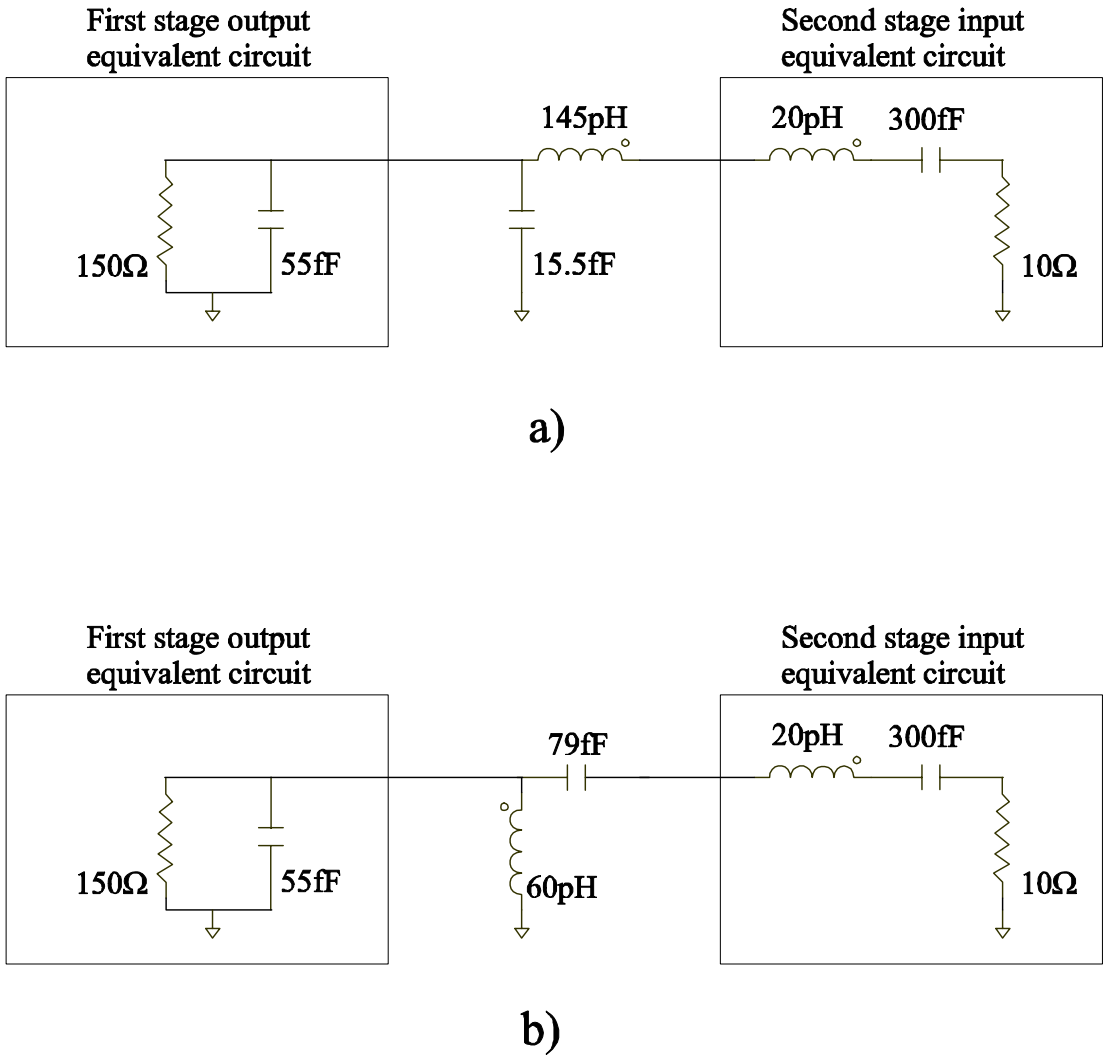


Figure 6.2: Two lumped element matching circuits for inter-stage matching. The first design is difficult to realize for an MMIC chip. Hence the second design is used. Furthermore, it satisfies the requirements of biasing the first stage and isolation of DC-bias between the stages.

connected to inductor strips and bias lines from HFSS simulations. Shunt parasitic capacitors, unlike the Ka-band single-stage design, significantly affect the scattering parameters of the amplifier in V and W-bands. Furthermore, finite conductivity of inductor strips and bias lines were also taken into account in HFSS and were translated into series resistors in the equivalent circuit model. Transistors with gate peripheries of 80 μm and 150 μm were used for first and second stage, respectively. Figure 6.3 shows the differential mode stability factor and maximum stable gain (MSG) across frequencies. The stability factor is bigger than 2.7 from 45 GHz to 75 GHz and MSG is 19 dB at 55 GHz. Although the design frequency was 58 GHz, in order to satisfy the common mode stability requirement as shown in Figure 6.4, the peak MSG was shifted to a lower frequency. The gain and phase margins for common-mode stability are 0.22 dB and 29° from unity [5]. About 0.75 dB in MSG was lost due to output on-chip circuit losses. The input and output impedance at 58 GHz are conjugate matched with 50 Ω and 20-j20 Ω loads, respectively. This design was submitted to TRW for fabrication at the time of this writing.

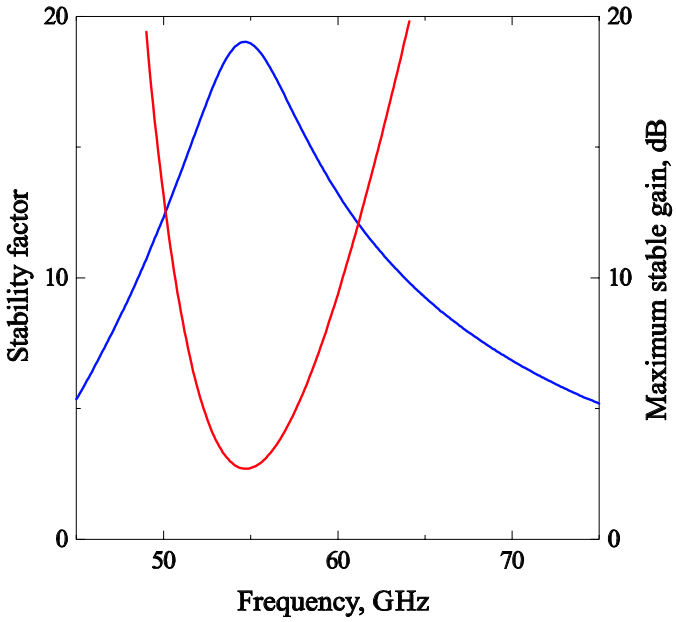


Figure 6.3: The stability factor and maximum stable gain (MSG) of the new 60 GHz two-stage grid amplifier design. The stability factor is bigger than 3.5 across the frequency band and the MSG is 18 dB at 55 GHz.

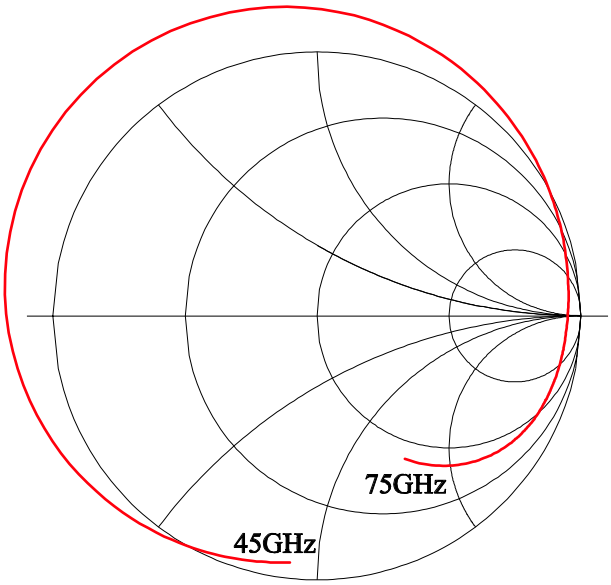


Figure 6.4: The common mode oscillation analysis for the new 60 GHz design. The curve has a gain and phase margin of 0.22 dB and 90° from unity.

6.4 Simulation of a Grid Oscillator

Time-domain simulation tools are capable of simulating the transient responses of a given system. If we incorporate the magnitude-dependent gain compression into the model, time-domain simulation can study the gain compression characteristic and oscillator power versus tuning. Following the layout of the grid oscillator reported in Deckman *et al.* [6] with the anisotropic material model developed for the Ka-band grid amplifier, we apply the 1-D FDSS simulation to this grid oscillator. Figure 6.5 shows the time transient response with no gain compression. It is found that the magnitude grows exponentially and the frequency of this oscillation is 37.5 GHz.

In order to represent the gain compression, we need to incorporate a magnitude-dependent transconductance, g_m, which transforms our problem in Chapter 2 into a set of nonlinear first order differential equations. This turns out to be complicated and needs further studies of the properties of the non-linear differential equation sets and

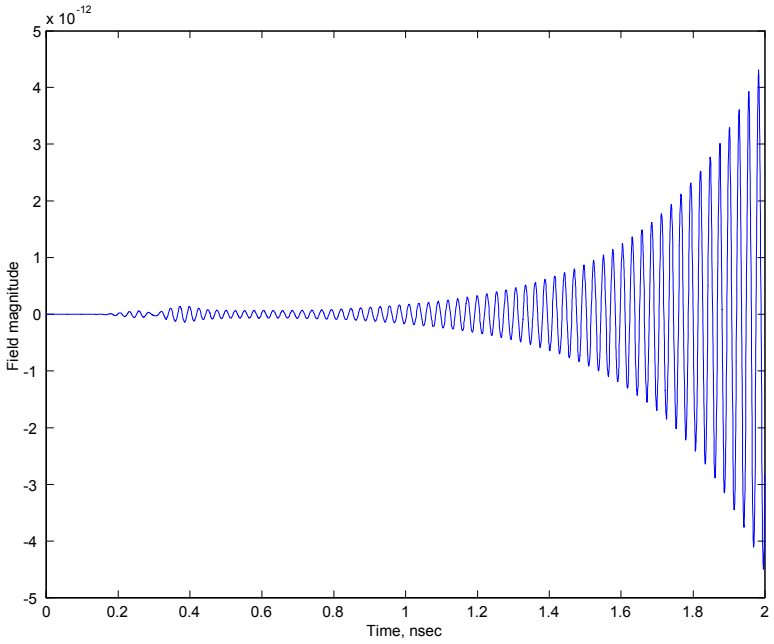


Figure 6.5: The transient response of the oscillator with no gain compression using the FDSS code developed in Chapter 2. The frequency of this oscillation is at 37.8 GHz.

the methods to solve them analytically. An ad hoc alternative method is to compute a number of exponential characteristic matrix, $\overline{A}(F_i)$, for different transconductance values where F_i is the field component that is measured over the anisotropic material. The update equation of 2.20 becomes

$$F^{n+1} = e^{\overline{A}(F_i)\cdot\Delta t} \cdot F^n + f((n+1)\cdot\Delta t)\cdot\Delta t \tag{6.1}$$

Figure 6.6 shows the transconductance variation of the anisotropic material model as a function of gate voltage. The variation is estimated from the DC transconductance measurements of a single transistor. A symmetrical Gaussian distribution with input gate voltage dependence was used,

$$g_m = g_{m0} \times \exp\left(-0.5\left(\frac{V_g}{\sigma}\right)^2\right) \tag{6.2}$$

where g_{mo} is the maximum transconductance, V_g is the input gate voltage and σ is

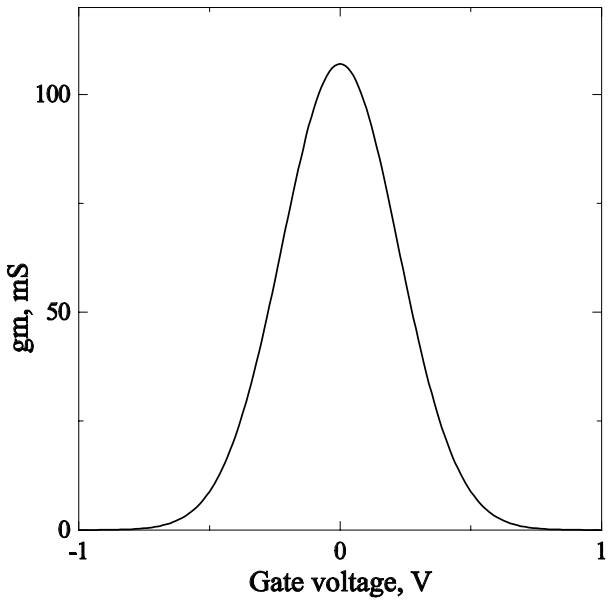


Figure 6.6: The variation that is used for transconductance, g_m. Note that this g_m is plugged into the equivalent anisotropic material model.

the standard deviation of the voltage about zero. We calculate the gate voltage by the equation

$$V_g = E \times d \tag{6.3}$$

where d is the height of an amplifier cell and is equal to 0.625 mm for Ka-band grid. E is the electric field of the input polarization at the anisotropic material. This curve was quantized into 10 equally spaced levels and the rest of the geometry was not changed for different values of g_m. The result shows that the unit cell stably oscillates at 37.4 GHz with output power density of 2000 W/m^2 (Figure 6.7). Since the Ka-band grid has an area of 1 cm^2, the estimated output power is 0.2 W. Since the result differs from [6], the method of evaluating input-dependent parameters and the actual variation dependence of transconductance need further studies. Nevertheless, it shows the possibility of expanding FDSS simulation for large signal calculations for grid amplifiers and oscillators without the necessity of worrying about the numerical instability.

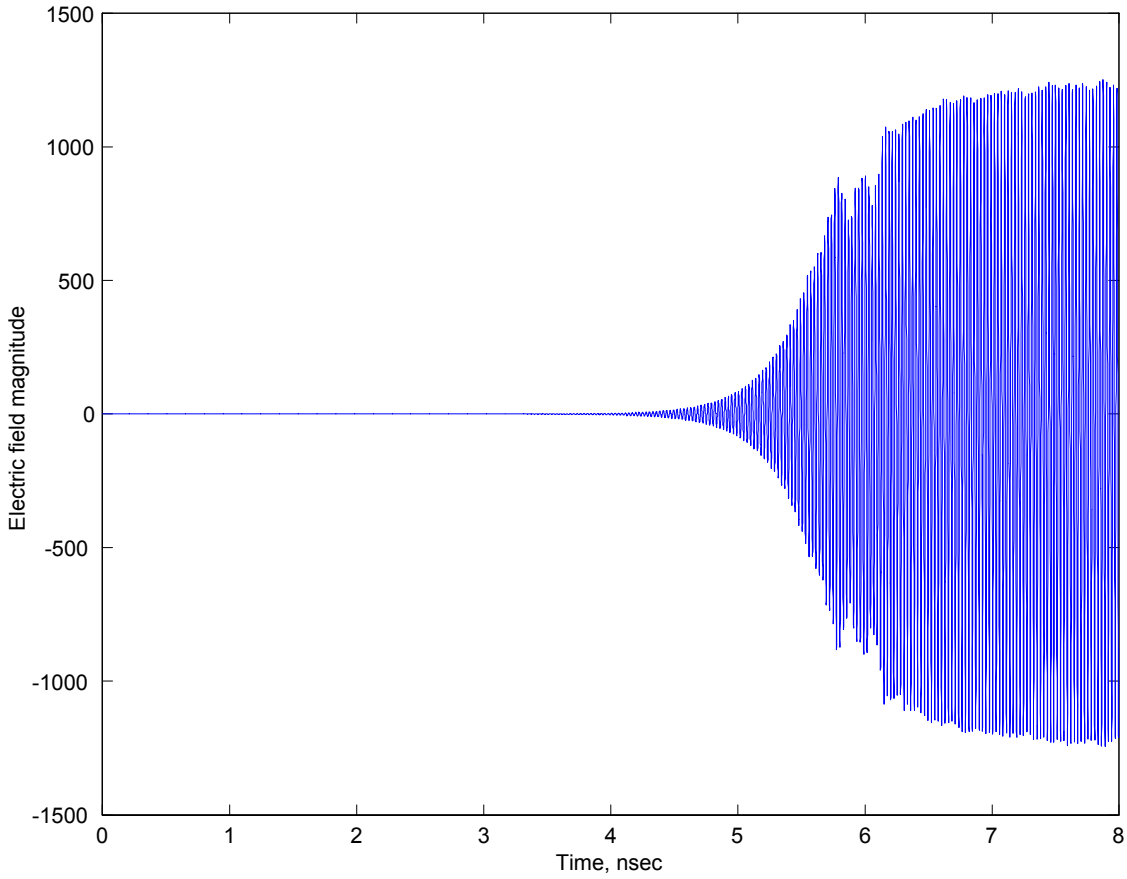


Figure 6.7: The input-dependent transconductance simulation using 1-D FDSS. The estimated power for a $1\,\mathrm{cm}^2$ grid would be $0.2\,\mathrm{W}$.

Reference

[1] J. W. Mink, "Quasi-Optical Power Combining of Solid-State Millimeter-Wave Sources," *IEEE Trans. Microwave Theory Tech.*, vol. 34 pp. 273-279, Feb. 1986.

[2] B. Deckman, D. S. Deakin, Jr., E. Sovero, D. Rutledge, "A 5-Watt, 37-GHz Monolithic Grid Amplifier," 2000 Int. Microwave Symp. Dig., pp. 805-808.

[3] D. M. Pozar, "Microwave Engineering," 2^{nd} Edition, *John Wiley & Sons, Inc.*

[4] P. Preventza, B. Dickman, E. Sovero, M. P. DeLisio, J. J. Rosenberg, D. B. Rutledge, " Modeling of Quasi-Optical Arrays," 1999 Int. Microwave Symp. Dig., pp. 563-566.

[5] C. M. Liu, E. A. Sovero, M. P. DeLisio, A. Moussessian, J. J. Rosenberg, D. B. Rutledge, " Gain and Stability Models for HBT Grid Amplifiers," 1995 IEEE AP-S Int. Symp. Dig., pp. 1292-1295.

[6] B. Deckman, J. J. Rosenberg, D. Rutledge, E. Sovero, D. S. Deakin, Jr., "A 1-Watt, 38-GHz Monolithic Grid Oscillator," 2001 Int. Microwave Symp. Dig., pp. 1843-1846.

Appendix A
Numerical Integration Using Rectangle Rule

The problem here is to find out the error and convergence of numerical integration with the rectangle rule. The analysis here follows [1]. We start by assuming the original integration equation is

$$I(f) = \int_a^b f(x)dx \tag{A.1}$$

and $f(x)$ is differentiable and we sought to find an estimation with the rule

$$I(f) \approx R = (b-a)f(a) \tag{A.2}$$

then the error of this estimated integrand is

$$E = I(f) - R = \int_a^b [f(x) - f(a)]\, dx \tag{A.3}$$

By mean value theorem,

$$[f(x) - f(a)] = f'(\eta)(x-a) \tag{A.4}$$

where $\eta \in (a, x)$. Thus

$$\begin{aligned} E &= \frac{f'(\eta)(b-a)^2}{2} \\ \eta &\in (a, b) \end{aligned} \tag{A.5}$$

This result suggests that the error converges to zero as the integration step $(b - a)$ decreases while $f'(\eta)$ is finite. The solution equation of the state-space method introduced in Chapter 2 is

$$F^{n+1} = e^{\overline{A}\cdot(n+1)\cdot\Delta t} \cdot F^0 + e^{\overline{A}\cdot(n+1)\cdot\Delta t} \sum_{i=0}^{n} e^{\overline{A}^{-1}\cdot i\cdot\Delta t} \cdot f(i\cdot\Delta t)\cdot\Delta t \tag{A.6}$$

The second part of this equation is in the form of A.2. This implies if the original function $f(x)$ is differentiable and $f'(x)$ is bounded, the numerical integration converges to the exact value of the integral as Δt decreases and it is bounded. Therefore if the field distribution of the discrete-space continuous-time system is bounded, the numerical field distribution is also bounded. Thus the state-space method provides unconditional stability for anisotropic nonreciprocal material in Chapter 2.

Reference

[1] S. D. Conte, Carl de Boor, "Elementary Numerical Analysis, An Algorithmic Approach," 3^{rd} Ed., McGraw-Hill International Book Co.

Appendix B
Drawings of Passive Waveguide Mode Converter

The drawings included are produced according to the optimized simulation results in Chapter 2. The measurement results were reported in Chapter 3. The manufactured passive mode converter contains two parts (Figures B.1 and B.2), which is the result of the split-block design approach.

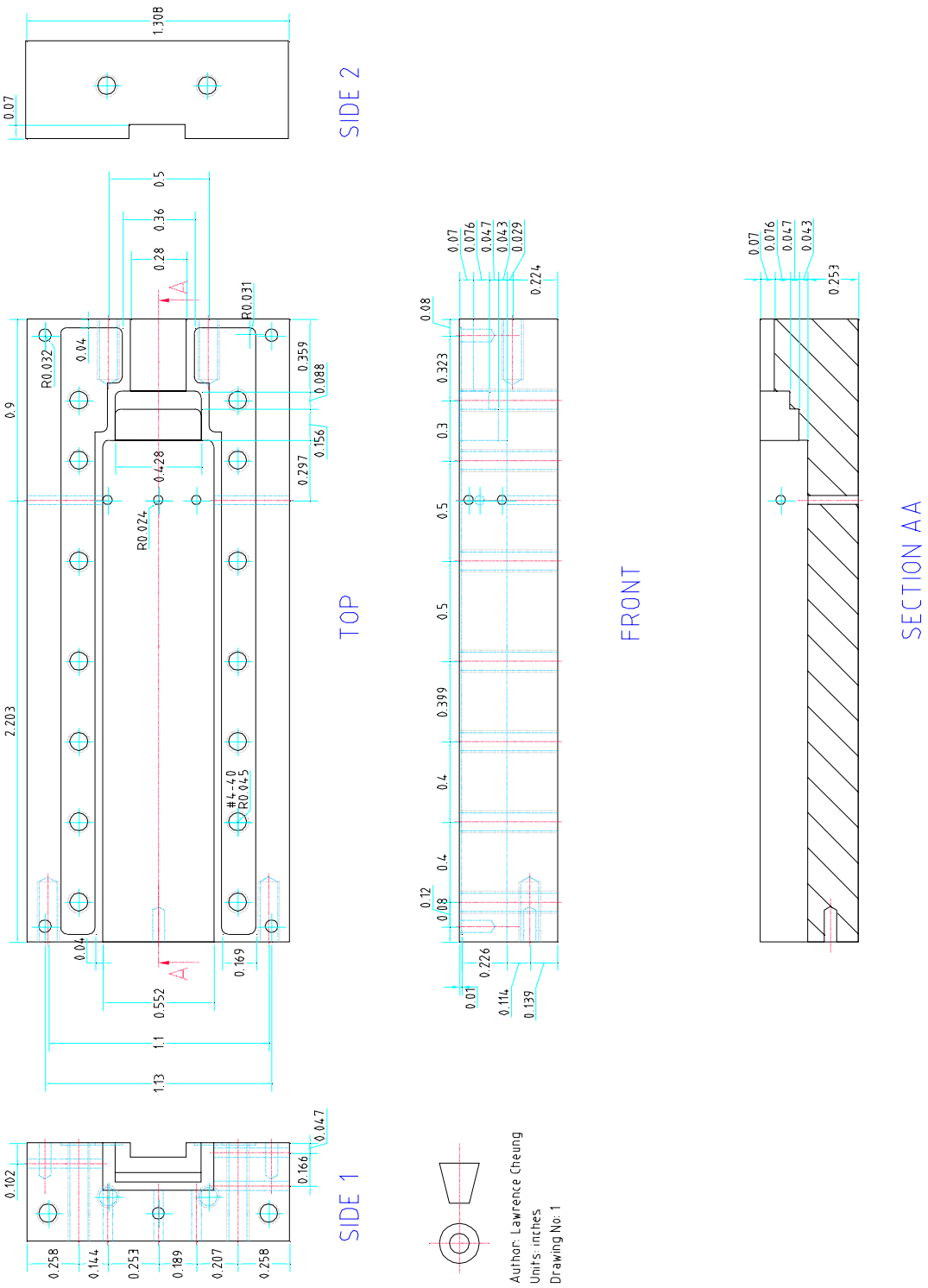


Figure B.1: Drawing of the passive mode converter

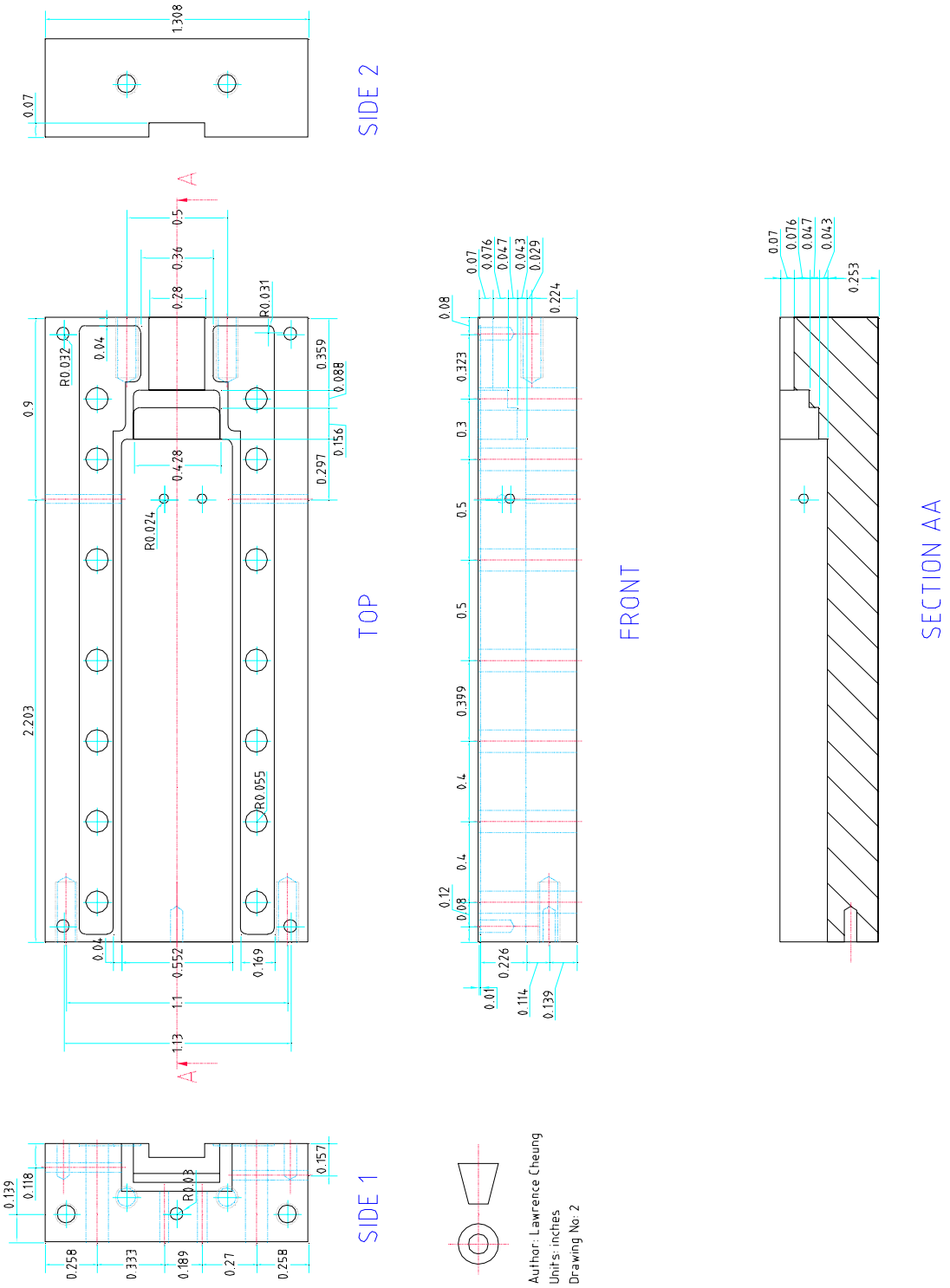


Figure B.2: Drawing of the passive mode converter