Chapter 4

High Aspect-Ratio Silicon Wire Array Photoelectrochemical Cells

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4.1 Abstract

In an effort to develop low-cost solar energy conversion techniques, high uniformity vertically oriented silicon wire arrays have been fabricated. These arrays, which allow for radial diffusion of minority charge carriers, have been measured in a photoelectrochemical cell. Large photovoltages (~400 mV) have been measured, and these values are significantly greater than those obtained from the substrate alone. Additionally, the wire array samples displayed much higher current densities than the underlying substrate, demonstrating that significant energy conversion was occurring due to the absorption and charge-carrier transport in the vertically aligned Si wires. This method therefore represents a step toward the use of collection-limited semiconductor materials in a wire array format in macroscopic solar cell devices.

4.2 Introduction

A key constraint in photon absorbers for solar energy conversion is that the material must be sufficiently thick to absorb most of the solar photons with energies above the material's band gap, yet sufficiently pure to have a high minority-carrier diffusion length for effective collection of the photogenerated charge carriers. This constraint imposes a cost floor on the absorber material by dictating the minimum required purity of the absorber phase. The situation is especially severe for indirect band-gap absorbers, such as Si which requires over 100 μm of thickness to absorb 90% of the energy in sunlight above the 1.12 eV band gap of Si.[1,2]

One approach to circumventing this constraint is to orthogonalize the directions of light absorption and charge-carrier collection.[2] One attractive realization of such an approach involves high aspect-ratio cylindrical absorbers, such as nanowires. A preferred implementation would involve the use of wires that are sufficiently long to absorb most of the incident light, but which have sufficiently small diameters to facilitate efficient radial collection of carriers, even for relatively impure absorber materials. To fabricate such a solar cell, methods are required to prepare large area arrays of vertically aligned nanowires, to make electrical junctions to such wire arrays, and to make electrical contacts to the backsides of these devices. These challenges have been investigated by various means, including chemical vapor deposition (CVD) growth of wire arrays,[3,4] etching of flat substrates to produce wire arrays,[5,6] and conductive-polymer electrical junctions with wires.[7,8] Nanowires have also been used to facilitate collection of majority carriers in ZnO-based dye-sensitized solar cells.[9] We report herein the demonstration of all of these steps for absorbers that consist of arrays of high aspect-ratio, CVD-grown, crystalline Si wires. Silicon is used in most current solar cells, and the fabrication of devices from Si is technologically well-developed, so methods for using less pure Si in solar energy conversion devices are of significant interest.

4.3 Experimental

4.3.1 Fabrication of Wire Array Samples and Controls

Degenerately doped N-type Si(111) wafers (0.004 Ω-cm) were thermally oxidized to produce a 285 nm oxide film. These wafers were then coated with S1813 photoresist (Microchem), exposed to the pattern (square array of 3 µm holes, 7 µm center to center), and developed in MF319 (Microchem). The wafers were then etched for 4 min in buffered-HF improved (Transene) (CAUTION: fluoride-containing solutions such as 11 M (40% by weight) NH_4F, buffered HF, and 27 M (48% by weight) HF pose a serious contact hazard. Hydrofluoric acid is highly toxic and corrosive and may cause serious burns which may not be immediately painful or visible. Fluoride ions readily penetrate the skin and can cause destruction of deep tissue and bone), followed by thermal evaporation of 500 nm gold and lift-off of the photoresist, to leave the catalyst islands separated by an oxide buffer. The samples were then brought into a tube furnace at 1050°C and annealed in H_2 for 20 min at a flow rate of 1000 sccm. The wires were subsequently grown for 20 min in a mixture of H_2 (1000 sccm) and $SiCl_4$ (20 sccm). Control samples consisted of oxidized wafers that contained patterned openings in the oxide, but no gold was deposited, and wires were not grown on such samples.

4.3.2 Photoelectrochemical Measurements

Following growth, the wire array samples were etched for 10 s in 10% HF(aq) to remove the native oxide. The samples were then soaked for 10 min in TFA solution (Transene), which contains I^-/I_3^-, to etch away the gold particles. SEM images confirmed removal of the bulk of the Au catalyst particle, although a hollow shell of material appeared to remain (See Figure 4.1 A). The wire array samples were subsequently dipped in 1 M HCl(aq) and rinsed with H_2O. The samples were then etched for 10 s in 10% HF(aq) to remove native oxide, rinsed with H_2O, and dried under a stream of N_2. Ga/In was immediately rubbed onto the back of the sample, and the samples were attached to a wire coil using silver paint. The samples were then sealed inside a glass tube, leaving ~ 2 mm^2 of exposed front surface area, using 20-3004 LV epoxy (Epoxies, Etc.) to coat the front face and sealing the rest of the sample with Hysol 1C epoxy (Loctite). Control samples were prepared similarly.

The photoelectrochemical measurements were performed in a solution consisting of 200 mM of dimethylferrocene (Me_2Fc), 0.5 mM of Me_2FcBF_4, and 1 M of $LiClO_4$ in methanol. Methanol was clearly observed to wet the wire array surfaces during both processing and photoelectrochemical measurements. The working electrode was either a wire array sample or a control sample. The counter electrode was a Pt mesh, and the reference electrode was a Pt wire enclosed in a Luggin capillary that contained the same solution as the main cell. All cell components were assembled under an inert atmosphere and were sealed before being placed under positive pressure of Ar. During measurements, the cell was illuminated using a 300 W ELH-type projector bulb. The light intensity was calibrated using a Si photodiode to produce a photocurrent equivalent to that obtained under 100 mW cm^{-2} of AM1.5 illumination at the working electrode surface. The solution was stirred vigorously during measurement, and a stream of air was used to keep the cell temperature constant under illumination.

Photoelectrochemical measurements were conducted using a Solartron 1287 potentiostat and the CoreWare software. To measure the open-circuit voltage in the light, the open-circuit potential was first allowed to equilibrate in the dark (always to within 10 mV of 0 V). The light was then switched on and the sample was allowed to equilibrate in the light. The reported V_{oc} is the difference between the potential in the dark and the potential in the light. J-V data were then recorded in the light at a scan rate of 10 mV s^{-1}. The short-circuit photocurrent densities were recorded as the current density measured at a bias of 0 V vs the Nernstian potential of the cell. The electrode area used to calculate the current density was measured using a flatbed scanner. Averages shown are for six wire array samples and four control samples, with the indicated error equal to the standard error of the mean.

4.3.3 Single Wire Measurements

The as-grown wires were removed from the growth substrate by sonication in isopropanol, and were then spin-coated onto a degenerately doped (n-type) silicon wafer that was covered with 100 nm of Si_3N_4. The substrate was then coated with lift-off resist (LOR3A, Microchem), followed by photoresist (S1813, Microchem). The electrodes were aligned to the wire samples using a Suss MA-6 mask aligner. Following pattern development, the wire samples were etched for 20 s in buffered HF(aq) to remove the native oxide, and 300 nm of Al, followed by 800 nm Ag, was then thermally evaporated onto the sample. The contacts were subsequently annealed at 250°C for 30 min in forming gas (90% N_2, 10% H_2). An example device is shown in the inset of Figure 4.3. Ohmic behavior was observed for the annealed Al contacts, and the resistivity was calculated based on the probe spacing and wire diameter (as determined by SEM). To determine the carrier type, the conductivity of the sample was measured at various back gate bias potentials between -60 V and 60 V. The samples were found to be n-type, based on the increase in conductivity with increasing gate bias.

4.4 Results and Discussion

Arrays of Si wires were grown using the vapor-liquid-solid (VLS) growth method, with Au as the VLS catalyst.[10-12] A 285 nm thick SiO_2 buffer layer was first thermally grown on the substrate, which was a degenerately doped n-type Si(111) wafer. Oxide deposition was followed by application of a resist layer. A pattern of holes in the resist and oxide was then formed using photolithography and subsequent etching through the oxide. The Au catalyst was then thermally evaporated onto the substrate, and excess Au removed during resist lift-off. VLS growth was then performed at 1050°C using $SiCl_4$ diluted in H_2, producing 10-30 μm long Si wires having the desired radii and pitch. Following growth, the remaining Au catalyst was removed from the wires.[13] As shown in Figure 4.1, the resulting Si wires were nearly completely oriented normal to the substrate and were highly regular, in both diameter and pitch, over a large (~2 mm^2) area.[11]

Although gold is a deep-level trap in silicon, the wires grown in this study are nevertheless expected to allow effective carrier collection. Because the solubility limit of

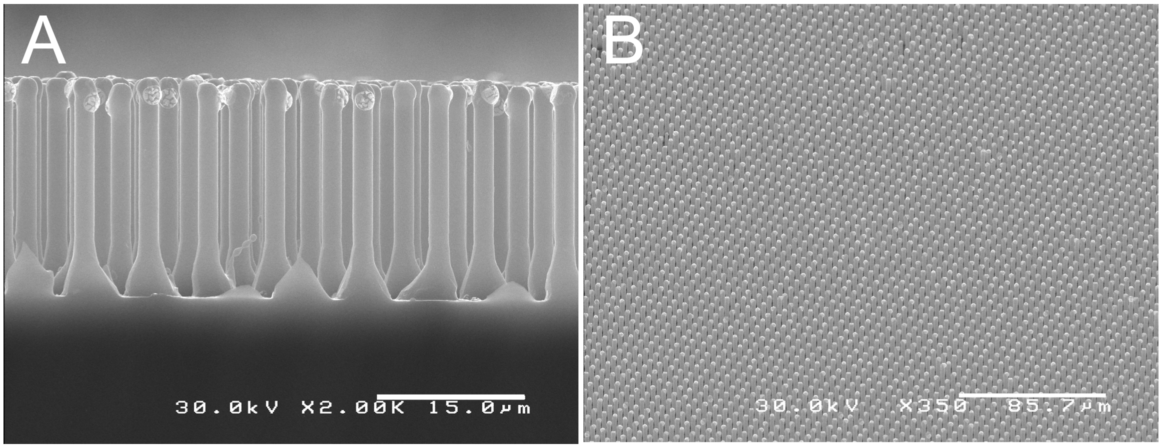

Figure 4.1. *Scanning electron microscopy images of silicon wire arrays. (A) Cross section. Scale bar, 15 μm. (B) 45° view. Scale bar, 85.7 μm.*

Au in Si at 1050°C is ~10^{16} cm^{-3}, the trap cross-section of Au is expected to produce carrier lifetimes of 2 ns.[1,14] This short lifetime would greatly restrict carrier collection in planar Si absorbers, but nevertheless is adequate to provide carrier collection for distances of at least 1 μm.[1] A theoretical treatment has shown that optimal efficiencies are expected when the wires have a diameter comparable to the minority-carrier diffusion length.[2] Smaller diameters produce increased surface area, and thus increase surface and junction recombination with little concomitant improvements in carrier collection. Hence, micron-diameter Si wires were grown and used in the array junction measurements.

Transmission electron microscopy (TEM) characterization of the wires indicated that they were single crystalline and grew in the <111> direction, as expected from the orientation of the substrate wafer (Figure 4.2).[11] Four-point probe measurements and field-effect measurements on individual nanowires indicated that the as-grown wires were n-type, with resistivities of 0.32 Ω-cm, corresponding to dopant densities of 2.5×10^{16} cm^{-3} (Figure 4.3).[15]

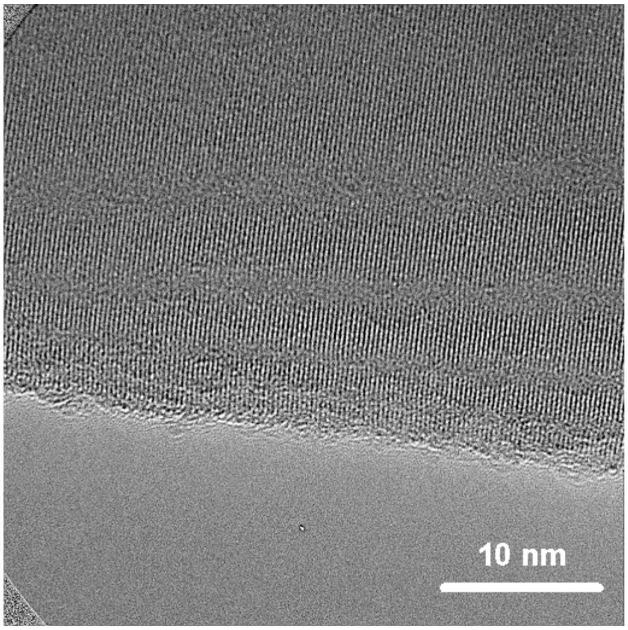

Figure 4.2. *TEM image of a Au-catalyzed, $SiCl_4$-grown, nanowire.[11] The scale bar is 10 nm. The vertical lines are lattice fringes; the horizontal bands are due to the curved surface of the wire causing interference fringes. No crystal defects were observed by TEM in the wires. A lattice spacing of 0.307 ± 0.004 nm is inferred from these images. This lattice spacing, combined with the fact that the wires grew as single crystals normal to a Si(111) wafer, is consistent with the growth being in the <111> direction (the Si (111) lattice parameter is ~0.314 nm).*

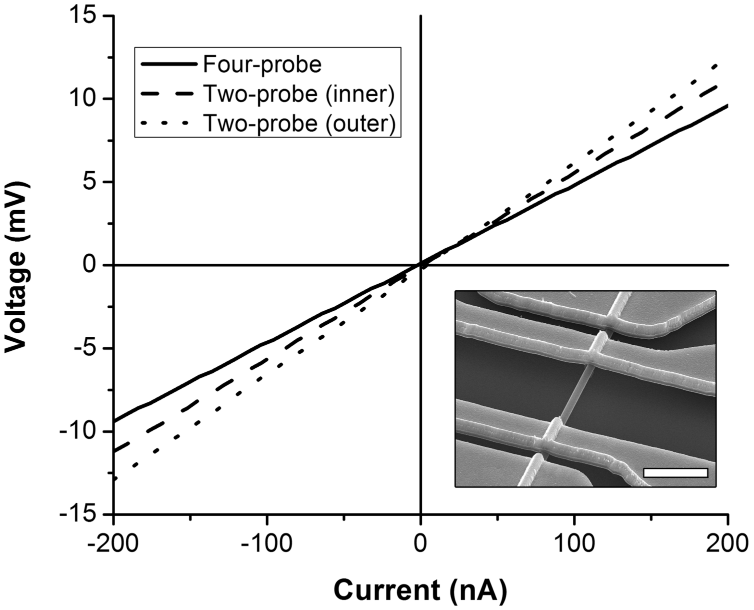

Figure 4.3. *Typical I-V measurement for an individually contacted wire using the four-point probe technique.[15] The wire resistance was 50 kΩ for this sample, corresponding to a doping level of 2.9×10^{16} cm^{-3}, assuming the same carrier mobility as in bulk Si. Inset: a SEM image of a four-point probe measurement device, viewed at 45°. The scale bar is 6 µm.*

The junction properties of such Si wire arrays were probed using a liquid electrolyte. The liquid electrolyte provided a convenient, conformal method of contacting the Si wires, and allowed measurements of the performance of the wires without requiring a diffused metallurgical junction to the Si wires in the array. In particular, the 1,1'-dimethylferrocene $(Me_2Fc)^{+/0}$ redox system in CH_3OH has been shown to yield excellent junctions with n-type Si, providing bulk diffusion-recombination limited photovoltages in excess of 670 mV under 100 mW cm^{-2} of AirMass (AM) 1.5 conditions.[16-20] Such junctions also form an in situ inversion layer in the n-Si, in essence forming an in-situ p^+ emitter layer, while also producing a highly passivated surface.[21] Hence these liquid junctions are well-suited as systems for providing initial probes of the solar device conversion properties of arrays of n-type Si wires. This expectation has been verified by measurements of photoelectrodes made from n-type macroporous Si, which have shown that high photovoltages can be obtained even with significant increases in surface area of the junction relative to the geometric projected area of the substrate, through use of the $Me_2Fc^{+/0}$-CH_3OH liquid contact.[22]

Table 4.1 summarizes the average values for the open-circuit voltage (V_{oc}) and short-circuit current density (J_{sc}) of the Si wire array photoelectrodes. To generate control samples, an oxidized substrate wafer was patterned with holes, but no catalyst

Table 4.1. *Photocurrent and photovoltage of wire array cells*

	V_{oc} **(mV)**	J_{sc} **(mA/cm^2)**
Wire Array	389 ± 18	1.43 ± 0.14
Control	232 ± 8	0.28 ± 0.01

was deposited into the openings, and wires were not grown on the samples. The V_{oc} in the wire array samples was relatively large (350-400 mV) given the high surface area per unit projected area. This value of V_{oc} reflects the relatively low surface recombination velocity of the Si/$Me_2Fc^{+/0}$-CH_3OH interface and good bulk properties of the Si wires, without which much lower V_{oc} values would be observed. The short-circuit photocurrent densities of the wire array samples were relatively low, 1-2 mA cm^{-2}. However, the wires were only 20 μm in length, so the expected J_{sc} of 43 mA cm^{-2} that could be attained for complete absorption and collection of all solar photons with energies above the 1.12 eV band gap of Si is reduced to 34 mA cm^{-2} for a 20 μm thickness of Si absorber.[1,2] In addition, the array of 2 μm diameter wires on a 7 μm pitch only fills 6.5% of the projected surface plane, thereby producing an expected maximum J_{sc} of 2.2 mA cm^{-2}, in agreement with the observed J_{sc}.

Representative current density vs voltage curves are shown in Figure 4.4. The fill factor was relatively low, and presumably reflects either a shunt or residual recombination at the junction that could potentially be reduced through improved surface passivation methods. The observed photoactivity was not dominated by the substrate, because the degenerately doped substrate produced only a low photovoltage and nearly no photocurrent. In addition, the wide bases of the wires suggest that relatively little, if any, direct contact was formed between any remaining oxide-free substrate and the liquid electrolyte. Thus, it is likely that all of the observed photocurrent and photovoltage are due to the wires rather than the substrate.

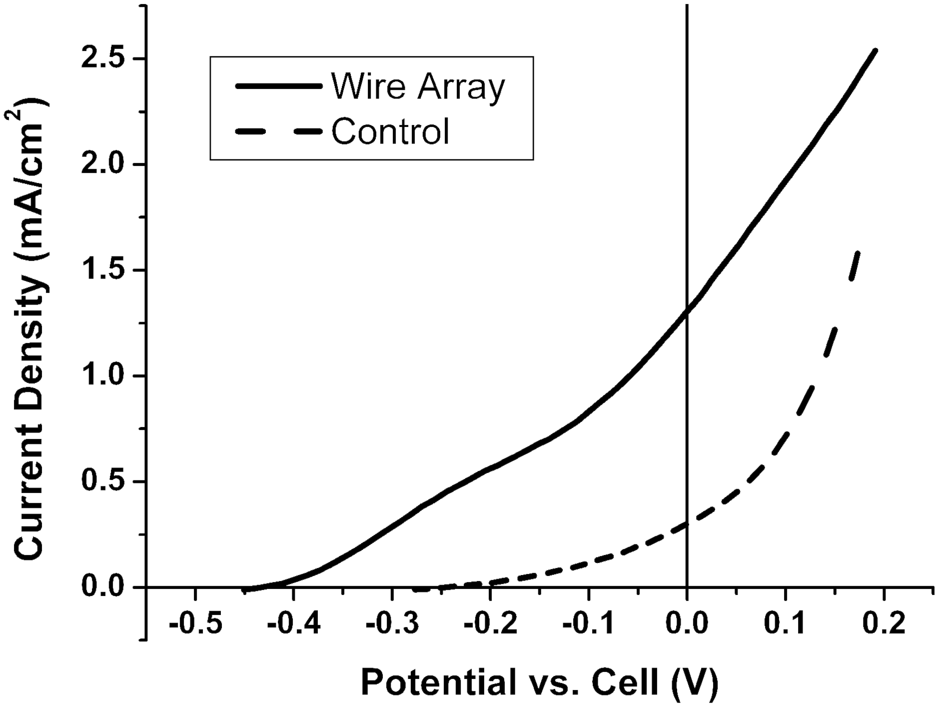

Figure 4.4. *Current density vs. voltage behavior for Si wire array (solid) and control samples (dashed). The electrode potential was measured vs. a Pt reference poised at the Nernstian potential of the 0.2 M* Me_2Fc*-0.5 mM* Me_2Fc^+*-1.0 M* $LiClO_4$*-*CH_3OH *cell.*

In summary, high fidelity, vertically aligned arrays of high aspect-ratio silicon wires have been fabricated over relatively large areas, and their energy conversion properties have been measured in a photoelectrochemical cell. Although the wires were grown with Au as the catalyst, the wire array samples showed significantly higher photocurrents and photovoltages than the control samples. Hence, as described herein, a nearly photoinactive substrate has been rendered photoactive by the scalable, relatively low cost, VLS growth of arrays of Si wires.

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