

Chapter 3

Physical Model Systems of Wire Array Solar Cells: Low Minority Carrier Diffusion Length Materials and Reactive Ion Etched Pillars

3.1 Abstract

In order to understand the fundamental constraints of using structured materials to enable cost-effective solar energy devices, both macroporous silicon and reactive ion etched (RIE) silicon pillars have been used as photoelectrodes. Macroporous Si was doped with Au in order to systematically lower the minority carrier diffusion length for the purpose of mimicking devices made from structured low-cost materials. Control over the charge carrier lifetime was demonstrated, with lifetimes between 1 and 15 μs achievable by varying the Au drive-in temperature. Photoelectrochemical measurements in methanol with dimethylferrocene⁺⁰ showed significant decreases in both short circuit current density (J_{sc}) and open circuit voltage (V_{oc}) with increasing Au doping. Furthermore, at the highest Au concentrations tested, the porous samples outperformed the planar samples, demonstrating that structuring of the absorber can lead to improvements in charge carrier collection, as expected from computational models. Finally, in order to independently test the claim that the increased junction area per unit of projected area found in structured electrodes gives rise to a decrease in the V_{oc} , pillars were etched in high quality silicon by cryogenic RIE, and photoelectrochemical measurements were made.

3.2 Introduction

Chapter 2 presents a comparison of the performance of high quality crystalline silicon in structured (macroporous) form and planar form.¹ The results shown there demonstrate primarily that there is a small but significant impact of creating structured samples on the measured open circuit voltage (V_{oc}) under illumination. This chapter continues the exploration of physical model systems of silicon wire arrays by exploring two consequences of using structured materials as the absorber in energy conversion devices. These studies are motivated by theoretical work suggesting that significant efficiency gains can be expected by employing radial junctions in materials with diffusion lengths of about 1-10 μm .² Reactive ion etching has been used to produce pillars of high quality silicon,^{3,4} which were designed to verify the reduction of V_{oc} with increased junction area per unit of projected area. Additional studies have also been pursued with macroporous silicon, including photolithographic templating of pores as a method for producing well-defined materials. Furthermore, doping with Au was pursued as a means to measure the performance of low-quality materials in both porous and planar structures.

3.2.1 Macroporous Silicon

The formation of porous silicon was originally discovered by Uhlir and Turner at Bell Labs in the 1950s, but its study was not popularized until the discovery of the photoluminescent properties of porous silicon.⁵⁻⁸ Although many studies have explored the synthesis and applications of microporous silicon,⁹⁻¹⁴ we are primarily concerned with macroporous silicon, which makes a better model of wire array solar cells due to the

highly vertical nature of the pores that are formed. Lehmann et al. originally reported that n-type silicon could be etched to produce long, straight-walled, uniform pores with micron-sized dimensions by etching in aqueous HF solutions under back-side illumination.¹⁵⁻¹⁹ Although there are several theories about why pores form on n-type silicon surfaces under these conditions, it is widely believed that a hole-limited silicon dissolution reaction is primarily responsible for pore formation in n-type silicon.^{10,15,18-24} In the presence of fluoride anions and holes, Si-H surface bonds can be converted to Si-F bonds with the release of H₂ (Figure 3.1).^{10,23} The polarity of the Si-F bonds weakens the Si-Si bonds to the lattice, allowing HF to attack and release SiF₄ from the surface. SiF₄ is then quickly converted to SiF₆²⁻, which is the reported product of dissolution.^{10,18} In the presence of water, it is also postulated that oxidation of the Si-Si bond to the lattice may follow the initial Si-F bond formation and that subsequent dissolution of this oxide by HF may be responsible for the dissolution process (Figure 3.1).²³ For both of these

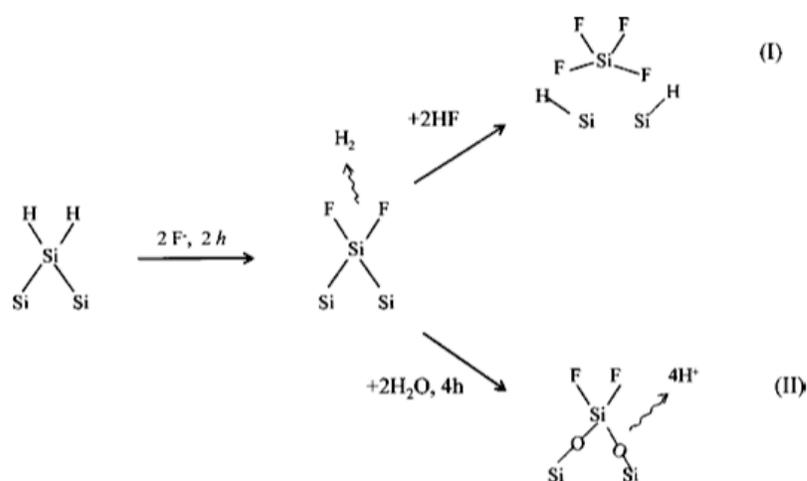


Figure 3.1. Proposed mechanisms of Si dissolution under anodic conditions.²³ The initial step requires the presence of both holes and fluoride ions, and the subsequent step can proceed both in the absence (I) or presence (II) of water.

mechanisms, it is necessary that both holes and fluoride ions be present at the interface for the initial step, and therefore the reaction rate will be limited in the absence of either.

Examining a typical J - E curve of p-type Si in HF reveals that the current increases with increasing anodic potential to a peak, commonly labeled as J_{ps} (Figure 3.2).^{10,23} The J - E curves of n-type Si in HF are found to match those of p-type silicon, but the n-type Si are hole limited in the dark.^{18,25} Therefore the current in n-type Si is limited by the hole supply provided by illumination, and the J - E curve reaches a plateau at the hole supply limit.^{10,18} It is found that for all current densities below J_{ps} , porous silicon can form, but that at J_{ps} , electropolishing occurs.^{10,23} Thus, J_{ps} is believed to be the point at which the hole supply is no longer limiting and the HF supply has become

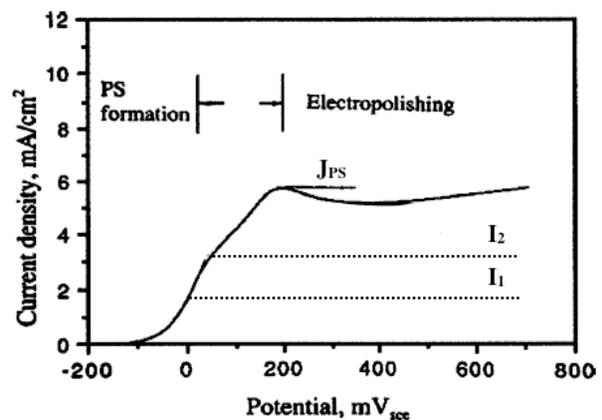


Figure 3.2. Typical J - E curve for p-type Si in aqueous HF solution (Solid line).²³ J_{ps} indicates the onset of electropolishing. For n-type Si, the curves are limited by the light, and two cases are shown by dotted lines, with $I_2 > I_1$.

limiting.^{10,22} In n-type silicon under back-side illumination, pore formation occurs by preferential collection of holes at the curved pore tips, where the electric field is the highest (Figure 3.3).^{10,23,24} Pores formed on polished substrates first proceed through an initiation period where etch pits are formed, and some of these pits subsequently develop into pores.¹⁸ However, by producing lithographically defined etch pits in the surface, the pore positions can be templated because the photogenerated holes will be preferentially harvested at the highly curved etch pit tips.¹⁸

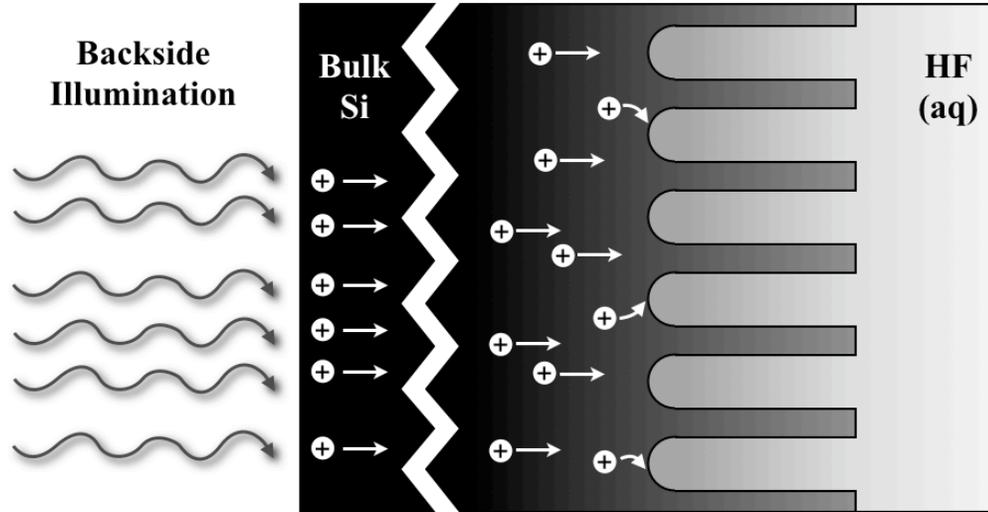


Figure 3.3. Schematic of pore etching in n-type Si. Illumination incident from the back of the sample generates holes that subsequently diffuse through the bulk of the Si. At the Si/HF(aq) interface, the holes enable the dissolution of Si, and they are preferentially harvested at the curved pore tips.

Under anodic etching conditions, there will be a significant space charge layer in n-type Si, and it has been proposed that the size of this space charge layer is roughly half of the pore-pore spacing.¹⁸ If the pores were spaced farther apart, holes would be able to diffuse into the neutral region between pores and would then be collected at the pore side walls rather than at the pore tips, causing etching of the side walls. Thus, the pore spacing is expected to be twice the depletion width, given for n-type Si by:²⁶

$$W = \sqrt{\frac{2\epsilon_s (V_{bi} + V_{app})}{qN_d}} \quad (3.1)$$

where W is the depletion width, ϵ_s is the static dielectric constant of silicon, q is the charge on an electron, N_d is the donor density, V_{bi} is the built-in voltage (band bending), and V_{app} is the applied voltage. Thus the pore-pore spacing will depend on $N_d^{-1/2}$ and $V_{app}^{1/2}$, but much greater variability in the dopant density is accessible (orders of magnitude) as compared to the accessible range of applied voltages. Therefore, the

primary mechanism of controlling pore spacing is to change the dopant density of the Si used. It has been found that when pores are templated by photolithography, if the pore spacing is too large (depletion region too small for the template), then the pores will branch to form pores with smaller spacing.^{10,18} Similarly, joining of pores is observed when the templated pits are too close together. Since the pore spacing depends on the depletion width, it is important to match the doping of the samples used with the lithographic template to be employed.

It has also been found that the pore area is related to the current density, J , used for etching by:¹⁵

$$\rho = J/J_{ps} \quad (3.2)$$

where ρ is the porosity of the sample—the ratio of the total projected pore area to the total projected surface area. Thus, if the pore spacing is set by the dopant density, different porosities will generate different pore sizes with the unit cell dimensions remaining approximately constant.¹⁰ The pore shape can also be controlled to some extent by changing the applied voltage (which will also change the depletion width), but round pores—which are obtained at relatively low voltages—are usually desired for their uniformity.^{10,18} Finally, the pore length is controlled by the etching time without greatly affecting the pore diameter, shape, or pore-pore distance.¹⁰ Thus, with anodic etching of n-type Si under back-side illumination, the pore size, pore-pore distance, pore shape, and pore length can all be controlled independently by varying the etching current (set by the illumination intensity), the sample doping, the applied voltage, and the etching time, respectively. Since these structures can be made from silicon of known quality and

materials properties, macroporous silicon is an ideal system for studying the effects of structure on device performance, keeping all other factors the same.

Both microporous silicon and macroporous silicon have found application in many areas. Microporous silicon has been studied extensively due to its luminescent properties and therefore its potential integration into optoelectronic systems.^{7,11,12} Microporous silicon has also been used in conjunction with solar cells, but not as the absorbing medium. Instead, it has been explored as a potential antireflective coating^{27,28} and as a method for layer transfer of thin-layer planar silicon solar cells.²⁹ The applications of macroporous silicon, which has a much smaller surface area/volume ratio, have been largely optical in nature. Etching all the way through a sample to produce long, narrow, and uniform channels enabled the production of optical short-pass filters with cutoffs in the near UV range.³⁰ Macroporous silicon has also been used as a photonic band-gap material—porous samples with straight pore walls have been used to produce 2D photonic band-gap materials,³¹ and porous structures with controlled pore deletion defects have been used to produce waveguides.³² More advanced etching techniques also allow the production of pores with widely varying diameter along the length of the pore, enabling the fabrication of cubic lattice materials that show 3D photonic band-gaps.³³⁻³⁶

For solar energy applications, most work on macroporous silicon has focused on its antireflective properties, and it has not typically been used as the absorber layer in solar energy conversion devices.³⁷⁻⁴⁵ To the best of our knowledge, there is only one other report, aside from the work presented in Chapter 2,¹ in which macroporous silicon was used as the absorber layer in a solar energy conversion device.⁴⁶ In this work a solid state

junction was produced in macroporous n-type Si for the purpose of both photovoltaic and betavoltaic energy conversion. In this case p-type Si was used as the absorber layer, giving rise to much thinner pore walls than those produced in n-type Si, and the primary goal was to increase the diode junction area in order to increase the area for injection of beta particles.⁴⁶

In addition to silicon, other semiconductors can be etched anodically to produce porous structures, including GaP.⁴⁷ The principle of improving the carrier collection properties of a material by decoupling the directions of light absorption and charge carrier collection was demonstrated in porous GaP as an increase in current following porous etching.^{48,49} These studies show that carrier collection can be significantly increased by increasing the junction area in a collection-limited material having the right minority carrier diffusion length ($\sim 1\text{-}10\ \mu\text{m}$). The efforts reported in this chapter to controllably lower the minority carrier diffusion length of macroporous Si complement this work because the detailed effects of diffusion length on collection can only be ascertained in a semiconductor than can be made with very long diffusion lengths, such as Si.

3.2.2 Photoelectrochemistry of Silicon

Liquid junctions present a natural way to make conformal junctions to structured materials, and they have been used exclusively in this chapter to make contact to both macroporous silicon and silicon pillars produced by reactive ion etching. For n-Si in methanol, ideal behavior of the V_{oc} with changing barrier height has been demonstrated, and ferrocene and some of its derivatives (dimethyl- and acetyl-) are known to give bulk-limited values of V_{oc} .^{50,51} Furthermore, studies of the surface recombination velocity

(SRV) of various silicon interfaces showed that the SRV for n-Si while in contact with ferrocene⁺⁰/methanol is on the order of 20 cm s⁻¹, which is comparable to or lower than the value found for Si in HF.⁵² Both formation of an inversion layer at the surface and possible methoxylation of the surface in the presence of a one-electron oxidant are thought to be responsible for the low SRV values observed.^{52,53}

Given the high barrier heights and low SRV values obtainable, the n-Si/methanol/ferrocene⁺⁰ system is expected to produce excellent photoelectrochemical energy conversion devices. When using this system with ferrocene or its derivatives, over 10% energy conversion efficiency was found for single crystalline samples,⁵⁴⁻⁵⁶ and efficiencies as high as 7.2% were achieved on polycrystalline Si.⁵⁷ Given these characteristics, the use of dimethylferrocene⁺⁰/methanol as the contacting phase when studying structured Si samples is a promising route to readily form high quality junctions. Much of the work presented in this chapter concerns the *J-E* curves of macroporous Si and reactive ion etched Si pillars in contact with this phase.

3.3 Experimental

3.3.1 Reagents

Methanol (BakerDry, Baker, Phillipsburg, NJ), sodium dodecylsulfate (SDS) (Sigma-Aldrich, St. Louis, MO), AZ-5214-E photoresist (Clariant, Somerville, NJ), AZ-300MIF developer (Clariant), 1,1,1,3,3,3-Hexamethyldisilazane (Sigma-Aldrich), potassium hydroxide (Mallinckrodt, Hazelwood, MO), 99.9+% gold wire (Aldrich), 49% (27 M) HF(aq) (Transene, Inc., Danvers, MA), and buffered HF(aq) (Transene) were used without further purification. Water (18 M Ω cm resistivity) was obtained from a

Barnstead Nanopure system. Lithium perchlorate, LiClO_4 (Sigma-Aldrich), was fused under vacuum and stored under an inert atmosphere until use. Dimethylferrocene (Me_2Fc , Sigma-Aldrich) was sublimed at $\sim 45^\circ\text{C}$ under vacuum and was stored under an inert atmosphere until use. Dimethylferrocenium tetrafluoroborate (Me_2FcBF_4) was synthesized from Me_2Fc by addition of excess HBF_4 in the presence of 0.5 equivalents of benzoquinone. The reaction was conducted under argon in an ice-water bath. The resulting solid was dried under vacuum and stored in an inert atmosphere. Me_2Fc and Me_2FcBF_4 were stored in light-protected bottles.

Silicon (Czochralski, n-type, (100)-oriented, P-doped) was obtained from either Virginia Semiconductor (Fredericksburg, VA, 1-10 Ω cm resistivity) or Wacker Siltronic (Munich, Germany, 4-8 Ω cm resistivity). These wafers were 500 ± 25 μm thick, polished on one side, and had measured resistivities between 5 and 7 Ω cm. Silicon (float zone, n-type, (111)-oriented, 4-8 $\text{k}\Omega$ cm resistivity, 350 ± 25 μm) was obtained from Topsil (Santa Clara, CA).

3.3.2 Photolithographic Patterning of Etch Pits

When lithographic etch pits were produced, a thermal oxide was first grown on n-type (100), 4-8 Ω -cm silicon. Silicon wafers were first rinsed with water, methanol, acetone, methanol, and then water and then dried under a stream of N_2 and transferred to a clean quartz slide. Samples were then oxidized in a tube furnace under wet air for 2.5 hours at 1000°C . Thermally oxidized samples were then cleaned with water, methanol, acetone, methanol, and water, and dried under a stream of N_2 . 1,1,1,3,3,3-hexamethyldisilazane (HMDS) was then spin-coated onto the samples for 10 s at 3000

rpm. AZ-5214-E photoresist was then immediately spin-coated onto the samples for 30s at 4000 rpm. The photoresist was soft baked for 60 s at 105°C on a temperature controlled hot plate, allowed to cool for 60 s, and exposed to the pattern for 30 s in a Karl Suss mask aligner. The pattern (3 μm holes in a dark background, spaced in a square array with 7 μm center-center distance) was chosen to be commensurate with the approximate pore size and spacing found when samples were etched without pre-patterning. Following exposure, the samples were developed for 30 s in undiluted AZ-300MIF developer, rinsed with water and dried. At this point, the patterned samples were subjected to a reversal step to harden the photoresist—the resist was exposed with no mask for 140 s, and then baked for 120 s at 120°C.

Clear nail polish (Sally Hansen Hard as Nails, with Nylon) was applied to the back of the patterned samples to protect the oxide layer and allowed to cure for 30 min. The pattern was developed in the front oxide layer by etching 65-70 s in buffered HF, and the samples were rinsed with water. The patterned samples were subsequently etched in KOH (10% w/w) for 11-12 min at $\sim 80^\circ\text{C}$ with vigorous stirring. During this step, both the photoresist and the clear nail polish were removed from the surface within the first few seconds of etching. The samples were rinsed with water and dried under a stream of N_2 and then examined under an optical microscope to verify the presence of fully developed pyramidal etch pits. Finally, the remaining oxide on both the front and back of the samples was removed by etching 60-70 s in buffered HF.

3.3.3 Fabrication of Macroporous Silicon

Macroporous silicon samples were produced both with and without lithographically defined etch pits. Etching of planar Si was performed in an aqueous solution of 5% HF(aq) that contained 10 mM SDS. The etching was performed potentiostatically at 5 V, with vigorous stirring, in a teflon cell equipped with a Pt counter/pseudoreference electrode. Prior to etching, the teflon cell, o-rings, and Pt mesh counter electrode were cleaned in aqua regia (3:1 HCl:HNO₃ by volume) for 30 min. Silicon samples were rinsed sequentially with water, methanol, acetone, methanol, and water, and were then dried under a stream of N₂(g). Approximately 2 cm² of the polished side of the Si was then exposed to the etching solution.

The illumination intensity was adjusted to maintain a constant 10 mA cm⁻² of current during etching, with the light intensity controlled by connecting the lamp power supply to a variable resistor. Samples were etched for 15, 30, 45, or 60 min. The samples were then rinsed thoroughly in water and dried under a stream of N₂(g). To remove the microporous Si layer, the samples were etched in 10% KOH(aq) for 10-20 s, and were then rinsed sequentially with water, methanol, acetone, methanol, and water, followed by drying under a stream of N₂(g).

3.3.4 Doping of Planar and Macroporous Samples with Gold

Gold was introduced into both planar and macroporous samples in order to reduce the minority carrier lifetime in a controlled fashion. Gold was diffused into both float-zone, double-side polished (DSP), 4-8 kΩ-cm n-type (111) samples, having thickness 350 ± 25 μm and both planar and porous samples composed of Czochralski, single-side

polished (SSP), 4-8 Ω -cm n-type (100) silicon with thickness $525 \pm 25 \mu\text{m}$. The float-zone samples were used to calibrate the gold concentration in the samples (given by the diffusion temperature and the solubility limit of Au in Si at that temperature) with the observed minority carrier lifetime as determined by RF photoconductivity measurements.

SSP samples (planar or porous), were placed face down in a thermal evaporator and 5-20 nm Au was deposited onto the backside, as measured by a quartz crystal microbalance (QCM). For DSP samples, this procedure was performed twice to deposit Au on both polished surfaces of the sample. Following deposition, the Au was driven into the Si samples in a tube furnace at various temperatures under N_2 or 95%/5% N_2/H_2 (forming gas). Since the solubility limit of Au in Si at various temperatures is known,⁵⁸⁻⁶⁰ the temperature of the tube furnace was used to set the Au doping level. The amount of time to allow to reach a relatively flat diffusion profile was calculated by solving the diffusion equation, Fick's Second Law:

$$\frac{\partial C(x, t)}{\partial t} = D \frac{\partial^2 C(x, t)}{\partial x^2} \quad (3.3)$$

where $C(x, t)$ is the concentration of Au with position and time, and D is the diffusion coefficient of Au in Si. If we take the sample width to be W , then $x = 0$ is the front face of the sample, and $x = W$ is the back face. For samples with Au on both sides, the initial conditions were:

$$C(0, t) = C(W, t) = C_{max} \quad (3.4)$$

$$C(0 < x < W, 0) = 0 \quad (3.5)$$

where C_{max} indicates the solubility limit of Au in Si at the desired temperature. In the case of samples having Au on only one side, the boundary conditions employed were:

$$C(0, t) = C_{max} \quad (3.6)$$

$$C(x > 0, 0) = 0 \quad (3.7)$$

$$\left. \frac{\partial C(x, t)}{\partial x} \right|_{(W, t)} = 0 \quad (3.8)$$

The condition on the derivative of $C(x, t)$ ensures that there is no concentration gradient at the back face of the sample and therefore no diffusion of Au out of the back face, which is the expected condition when Au is present on only the front face.

By numerically solving the diffusion equation as described above for a series of time points, the time at which the total variation in concentration across the sample width was less than 5% could be calculated. This was taken to be the minimum necessary time at the target temperature in order to guarantee a uniform concentration of Au. Typically samples were held at the target temperature for 2-3 times longer than the calculated time to ensure a consistent diffusion profile. Table 3.1 lists values of C_{max} and D for Au in Si as well as the calculated times for one- or two-sided diffusion for the two widths of interest in these studies (350 μm for DSP, float-zone wafers, and 500 μm for SSP planar or porous Czochralski wafers).

Following deposition and drive-in of Au, the excess Au was removed by a variety of procedures. In a typical treatment, the samples were first etched 10 s in 49% HF to remove any surface oxide that might have formed during drive-in. They were subsequently treated for 30 min in aqua regia (3:1 concentrated HCl:concentrated HNO_3)

Table 3.1 - Maximum solubility and diffusion coefficients of Au in Si.⁵⁸⁻⁶⁰ Times shown are calculated by solving the diffusion equation.

T (°C)	C_{max} (cm ⁻³)	D (cm ² s ⁻¹)	Two-Sided		One-Sided	
			350 μ m Time (h)	500 μ m Time (h)	350 μ m Time (h)	500 μ m Time (h)
1100	6.3×10^{16}	1.3×10^{-6}	0.11	0.19	0.36	0.72
1000	1.0×10^{16}	6.1×10^{-7}	0.19	0.39	0.75	1.50
900	1.8×10^{15}	2.6×10^{-7}	0.44	0.92	1.78	3.58
800	5.0×10^{14}	9.0×10^{-8}	1.25	2.53	4.97	10.11
700	1.0×10^{14}	2.6×10^{-8}	4.36	8.86	17.39	35.47
600	2.0×10^{13}	5.5×10^{-9}	20.22	41.28	80.86	165.03

to remove the outer layer of Au. The samples were subsequently oxidized in piranha solution (3:1 conc. H₂SO₄:30% H₂O₂), etched in 49% HF to remove the oxide formed, and soaked again for 30 min in aqua regia to further remove Au from the surface. Samples were finally etched one more time in 49% HF prior to photoconductivity measurements or electrode fabrication.

3.3.5 RF Photoconductivity Measurements

Radio-frequency (RF) photoconductivity decay measurements are a contactless way to measure the minority carrier lifetime in a semiconductor sample. In the basic operation of the RF photoconductivity instrument a sample of Si is used as a resonant element in an RF circuit driven by a high-frequency signal generator. A 10 ns pulse of light from an Nd:YAG (1064 nm) laser induces an increase in the number of charge carriers and thus an increase in the conductivity of the Si, and the decay back to steady state is measured after the pulse. A detailed description of the instrument and its

components is available in the literature.⁵² In order to mitigate contributions from surface recombination, all samples were measured with a thin layer of HF on both faces of the sample. The HF/Si interface is known to have a low surface recombination,⁵² so the bulk lifetime can be measured in this way.

Some processes involved degreasing float-zone samples in order to remove an organic contaminants prior to measurement in the RF photoconductivity system. In this case, DSP samples were degreased by sonication for 5 min each in water, methanol, acetone, 1,1,1-trichloroethane, dichloromethane, 1,1,1-trichloroethane, acetone, methanol, and water, with a rinse in the next solvent in between each sonication step. They were subsequently etched in hot piranha (in a boiling water bath) for at least 60 min.

3.3.6 Production of Si Pillars by RIE

Reactive ion etching (RIE) was used to produce silicon pillar arrays from n-type $\langle 100 \rangle$ Si with a resistivity of 1-10 Ω -cm. The arrays consisted of 5, 10, 20, and 50 μm diameter spots in a hexagonal pattern with the spot to spot separation (edge to edge) equal to the spot diameter in each array. Each of the arrays was patterned over an area of about 2 x 2 mm^2 , with multiple areas of each size of array patterned simultaneously on one sample. The hexagonal pillar arrays were photolithographically defined by using AZ-5214-E as an etch mask. Following exposure and development of the photoresist, the silicon sample was mounted on a carrier silicon wafer using a thin film of Fomblin oil (Solvay-Solexis, Thorofare, NJ). The Fomblin oil was found to make excellent thermal contact to the silicon carrier wafer. Prior to RIE, the chamber was cleaned with a high

pressure SF₆ plasma and then conditioned for 30 minutes under the etching conditions with a blank wafer. The RIE was then carried out cryogenically in an Oxford Instruments PlasmaLab System100 ICP-RIE 380. Typical conditions for etching are shown in Table 3.2. For the samples shown here, the etching was carried out in two steps of ~35 minutes each. Between the two etching steps, the samples were removed and blown with a stream of N₂ to remove any residual SF₆ that had accumulated near the base of the pillars. This was found to be an effective way to extend the growth of the pillars to longer dimensions.

Following reactive ion etching, the samples were treated for 60 min in piranha (3:1 conc. H₂SO₄:30% H₂O₂) to remove the thermal paste and etched in buffered HF for 4 min. The samples were then oxidized in a tube furnace under wet air at 850°C for 90 min, etched in buffered HF 3 min and dried under a stream of N₂. Finally, the samples were annealed at 400°C in the tube furnace under 95%:5% N₂:H₂ (forming gas).

Table 3.2 - Reactive ion etching parameters used for typical samples.

SF ₆	O ₂	He	ICP	RIE	Temp	Pressure
70 sccm	6 sccm	10 Torr	900 watts	5 watts	-140 °C	10 mTorr

3.3.7 Scanning Electron Microscopy

Scanning electron microscopy (SEM) data were obtained using a LEO 1550 VP Field Emission SEM (FE SEM) using the in-lens detector at an accelerating voltage of 10 kV. Samples were scored on the back and cracked along the (100) directions to obtain cross sectional images, and the resulting pieces were mounted to the SEM stub using carbon or copper tape.

3.3.8 Preparation of Photoelectrodes

For photoelectrochemistry, the samples were scored and cracked to produce ~5 mm x 5 mm electrodes. The samples were then etched for 10-30 s in buffered HF(aq), rinsed with water, and dried under a stream of N₂(g). Ga/In eutectic was then immediately scratched into the back side of the samples. Ag paint was then used to affix the back of each sample to a coil of tinned Cu wire. In the case of macroporous silicon electrodes, the front surface of the samples was covered with Epoxies, Etc. (Cranston, RI) 20-3004 LV epoxy to leave an exposed area of ~1-2 mm². The silicon sample and the Cu wire were then sealed in a glass tube using Hysol 1C epoxy (Loctite, Rocky Hill, CT), with the sample surface oriented perpendicular to the long axis of the glass tube. When the LV epoxy was applied, most of it was covered with Hysol epoxy. The LV epoxy was needed due to the tendency of the Hysol epoxy to form bubbles on the porous Si surface. Both epoxies are opaque and resistant to methanol, and the Hysol epoxy provided strong structural support. Before use in photoelectrochemical experiments, electrodes were allowed to cure for at least 24 h at room temperature. For RIE pillar array samples, the same procedure as above was followed, except that LV epoxy was not use. The projected area of each electrode was measured by taking an image at 800 dpi of the electrodes and a 1 cm x 1 cm calibration square, using a flat-bed scanner, and analyzing the resulting image using the Image SXM software.

3.3.9 Photoelectrochemistry

Photoelectrochemical experiments were conducted in a sealed glass cell under a positive pressure of Ar. The standard measurement solution (CH₃OH, 1 M LiClO₄, 200

mM Me_2Fc , ~ 0.1 mM Me_2FcBF_4) was prepared and introduced into the measurement cell under an inert atmosphere. Silicon electrodes were etched (10-30 s in buffered $\text{HF}(\text{aq})$ for planar or RIE-etched pillar samples; 2 min in 1:1 (v:v) 27 M $\text{HF}(\text{aq})$:ethanol for porous samples) to remove the native oxide, rinsed with water, and then thoroughly dried under a stream of $\text{N}_2(\text{g})$. The electrodes were then immediately introduced into the cell (Figure 3.4), under a positive flow of Ar. The reference electrode was a Luggin capillary, with an outer tip diameter of ~ 100 μm , that contained a Pt wire and a sample of the same solution as in the working electrode compartment. A Pt mesh was used as a counter electrode.

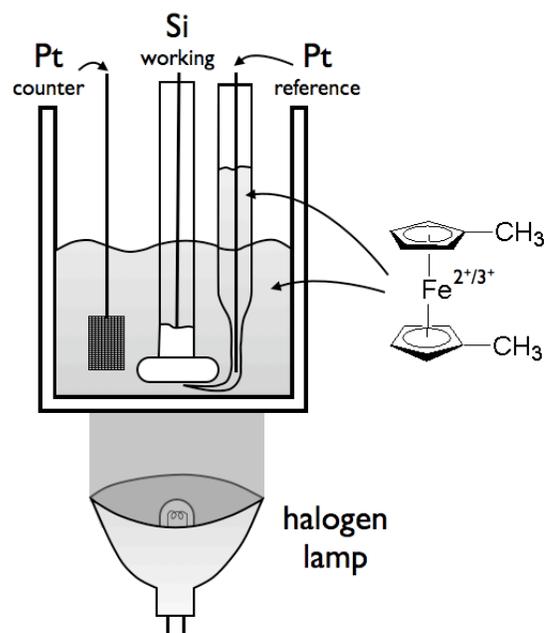


Figure 3.4. Schematic diagram of the cell used. The filling solution is 1 M LiClO_4 , 200 mM Me_2Fc , and ~ 0.1 mM Me_2FcBF_4 in methanol.

The cell had a flat quartz bottom, and the working and reference electrodes were positioned as close as possible to the bottom of the cell, with the tip of the Luggin capillary directly underneath the Si surface and as close as possible to the Si without touching its surface. The solution was stirred vigorously during all data collection.

Illumination of the bottom of the cell was provided by a 300 W ELH-type W-halogen bulb equipped with a dichroic rear reflector.⁶¹ The illumination intensity was measured using a calibrated Si photodiode that was in turn calibrated relative to a

secondary standard Si solar cell. The secondary standard Si solar cell had been calibrated by an independent calibration laboratory with respect to a reference AM 1.5 spectrum at 100 mW cm^{-2} of illumination intensity. For Si photoelectrodes in this same cell configuration and electrolyte/redox system, this calibration method has been shown previously to produce short-circuit photocurrent densities that are very close to those obtained under the same intensity of actual sunlight.^{54,55}

All current density-potential (J - E) measurements were recorded using a Solartron model 1287 potentiostat. In a typical experiment, the J - E behavior of the electrode was measured at 10 mV s^{-1} in the dark, then under 100 mW cm^{-2} of illumination, and then measured again in the dark. The open-circuit voltage, V_{oc} , was measured between each J versus E measurement. The short-circuit current density, J_{sc} , was calculated as the average current density for potentials within 10^{-4} V of 0 V versus the Nernstian potential of the cell. The values of V_{oc} and the presented J - E behavior are reported with respect to the Nernstian cell potential, which was measured with respect to the reference electrode for each working electrode. The Nernstian potential was typically 10 - 30 mV versus the reference electrode potential, due to drift in the composition of the cell solution compared to the composition of the solution in the Luggin capillary. The point of maximum power was calculated as the average of 10 data points, after eliminating the 10 largest measured points (to remove any erroneous spikes). The efficiency and fill factor were calculated by conventional methods.

3.3.10 Correction for Series Resistance

To correct curves for a series resistance, equation (3.9) was employed:

$$E_{corr} = E_{meas} - iR_s \quad (3.9)$$

where E_{corr} is the corrected potential, E_{meas} is the measured potential, i is the signed current, and R_s is the series resistance. The potential was corrected at each point based on the absolute current and plotted as J vs. E as usual.

3.4 Results and Discussion

3.4.1 Photolithographic Pore Definition

In many studies of macroporous n-type silicon, photolithography and etch pit definition was used to produce ordered arrays of pores rather than the randomly arranged pores shown in Chapter 2.^{10,15,18,19,33} In order to template pore growth, n-type, (100) Si

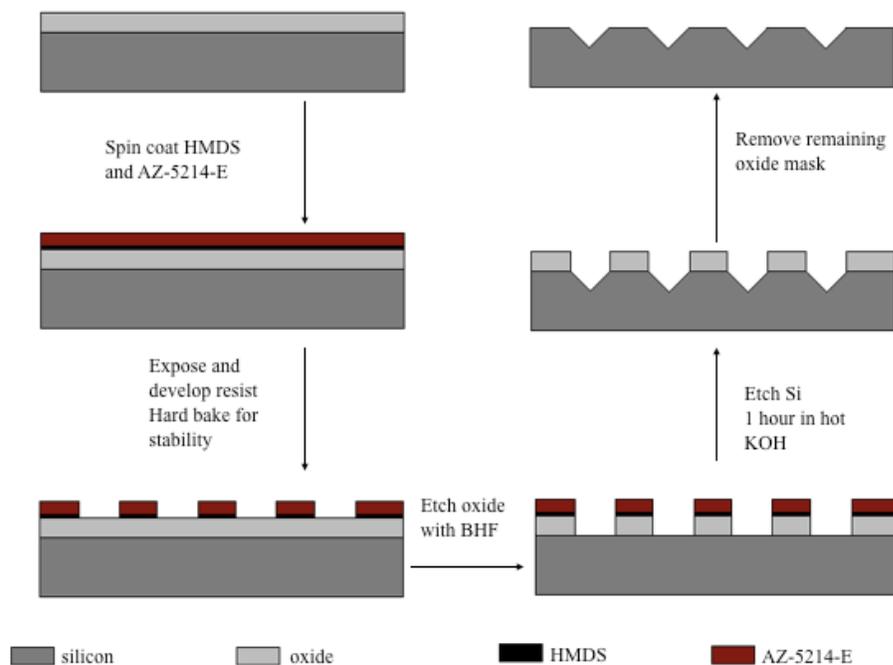


Figure 3.5. Schematic of etch pit preparation. The photoresist mask is used to etch the oxide layer, and the oxide layer is used to etch the silicon pits.

was first patterned with an array of pyramidal etch pits. It is expected that pyramidal etch pits will act as seed points for the growth of macropores due to the high electric field at the tips of the pyramids.¹⁰ Thus, a higher degree of control over the structure of the porous samples is attainable through photolithographic templating.

A schematic illustration of the patterning procedure is shown in Figure 3.5. Photolithography is used to define openings in the SiO₂ layer, after which the SiO₂ layer serves as a mask for the KOH etching step. Both SiO₂ and Si₃N₄ serve as effective etch masks for KOH, allowing the definition of pits, but SiO₂ was chosen due to the ease of growing a thermal oxide layer on unmodified Si wafers. As shown in Figure 3.6, pyramidal pits are formed on the (100) surface after KOH etching. The formation of pyramidal pits is expected due to the enhanced stability of the (111) plane to KOH etching compared to the other low index planes of Si. Starting with a (100)-oriented wafer and assuming the etch planes are (111) planes, then we expect to see an angle of about 55°, and we observe an angle of about 52°. The slight deviation from the expected

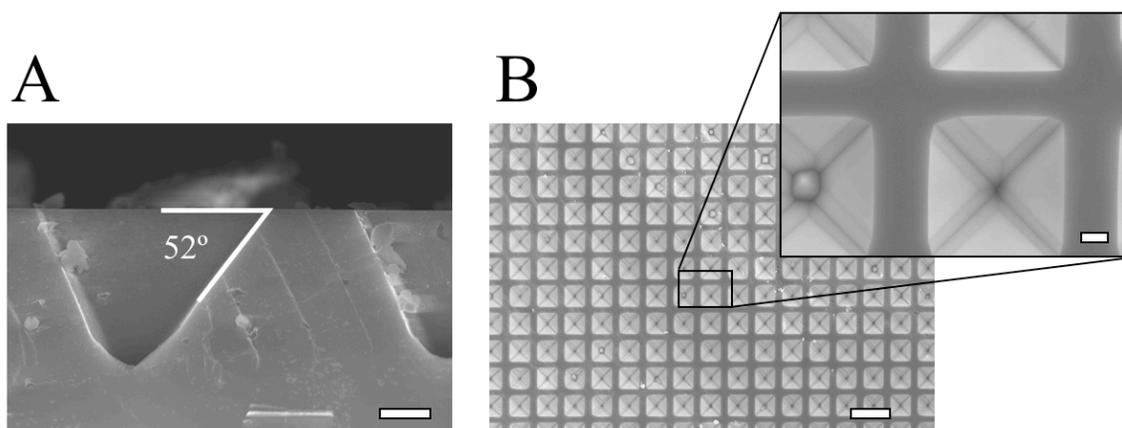


Figure 3.6. SEM images of etch pits. A) Cross section showing the angle between the (100) surface and the pit side wall, which should be a (111) plane. Scale bar, 1 μm . B) Plan view showing the pyramidal nature of the etch pits. Scale bar, 10 μm . The inset is a higher-resolution image of the indicated area. Scale bar, 1 μm .

value, as well as the asymmetry observed in the cross section may be due to slightly off-axis cleaving of the wafer prior to SEM.

When patterned samples were anodized in HF in the presence of surfactant, it was found that pore growth was initiated from the etch pits, as expected (Figure 3.7). The pores are wide near the surface of the sample and show a smooth transition from the surface etch pits into the pores. However, there is significant branching observed in the pore side walls, which indicates a mismatch between the pattern dimensions and the natural pore size and spacing given by the etching conditions employed.^{10,18} It has been shown previously that the pore spacing is primarily influenced by the dopant concentration in the sample, and that pore branching is observed when the doping of the sample is too high for the pattern employed.^{10,18}

The mismatch between the pattern used and the sample doping was unexpected because the pattern was designed based on the previous etching behavior of the silicon used. The mask used to generate the etch pit pattern consisted of 3 μm pores in a square

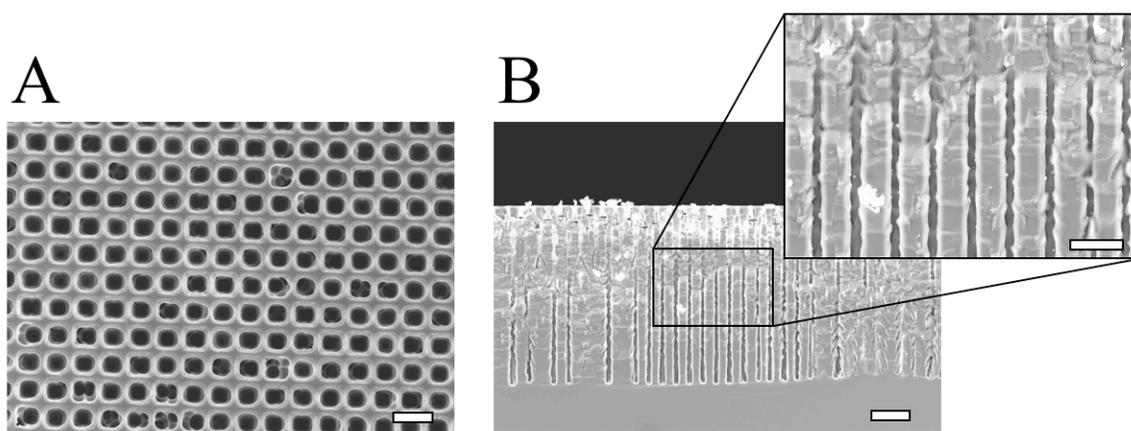


Figure 3.7. SEM images of photolithographically templated pores. A) Plan view showing the visible pore branching and the wide pore mouths. Scale bar, 10 μm . B) Cross section showing pores etched for 60 minutes. Scale bar, 20 μm . The inset shows the pore branching in the cross section. Scale bar, 10 μm .

array, with 7 μm center-to-center distance. These values were chosen after a careful examination of the growth tendencies of randomly seeded macropores (e.g., the porous samples considered in Chapter 2). By counting the number of pores in a given area of the sample, the unit cell for each pore was determined to be about 49 μm^2 in area, giving a square unit cell 7 μm to a side. Furthermore, the average pore diameter was found to be 3 μm in randomly initiated pores. Thus, the pattern used was expected to be appropriate for the doping level and etching conditions employed, but significant branching was still observed.

Although the templated macropores produced here do not show the uniformity and fidelity of those shown in the literature, they do demonstrate pore initiation from patterned etch pits. Further optimization of the mask used or the dopant concentration of the Si employed would produce samples consistent with those that have been shown in the past. However, given the care that must be taken in matching the mask to the dopant concentration, further studies conducted on macroporous silicon were carried out using randomly initiated pores. The possibility for radial charge carrier collection, which is the key property of macroporous Si being explored in this work, should be available in an average sense in randomly initiated pores. In fact, a square array of pores leads to more large contiguous areas of Si that might actually increase the average distance minority carriers must travel before being collected relative to a random arrangement of pores. Thus, all other results involving macroporous silicon, both in this chapter and in Chapter 2, refer to macroporous Si with randomly initiated pores.

3.4.2 Gold Doping of Macroporous Silicon

In order to demonstrate the principle that structured materials enable the orthogonalization of light absorption and charge carrier collection, macroporous silicon samples and planar silicon samples were doped with Au and the resulting low lifetime materials were tested to ascertain their photoelectrochemical properties. In the course of trying to produce materials with well-defined minority carrier lifetimes, however, there were significant challenges in material preparation. Both the challenges faced and the initial photoelectrochemistry results will be presented below.

3.4.2.1 Bulk Lifetime of Pure Samples

In order to demonstrate the controlled reduction of the sample lifetime by introduction of Au dopants into the Si lattice, samples consisting of double-side polished (DSP) float-zone Si were used. With high-purity float-zone Si, extremely long bulk minority carrier lifetimes are expected, typically on the order of 1 ms or greater.⁵² Starting with (111)-oriented, n-type 4-8 k Ω -cm Si, lifetimes of about 1 ms were consistently measured when both faces of the sample were immersed in HF, which is known to create a low surface recombination velocity (SRV) interface with Si.⁵² In n-type Si, the hole diffusion coefficient, D_p , is about 10 cm² s⁻¹.⁶² Therefore, we calculate the minority carrier diffusion length from⁶²

$$L_p = \sqrt{D_p \tau} \quad (3.10)$$

This gives a minority carrier diffusion length of approximately 1.4 mm. This implies that minority carriers can traverse the width of the sample several times over before recombining, thus further confirming the low SRV of the HF-Si contact. This

measurement does not eliminate the possibility that the observed value is still limited by surface recombination, but in either case, the measured lifetime gives a lower bound on the bulk lifetime of the starting material used.

In order to demonstrate that the reduction in lifetime observed after Au doping (see below) is due to the presence of deep-level trap states introduced by Au, pristine Si wafers from the same stock that gave 1 ms minority carrier lifetimes were subjected to the conditions of the Au drive-in step, but in the absence of any Au. This consisted mainly of heating the samples in a tube furnace at various temperatures under ultra high-purity Ar or forming gas (95%:5% N₂:H₂). Heating degreased Si samples under inert gas caused a dramatic decrease in the measured lifetime. After heating at 700°C for 4.5 hours, the minority carrier lifetime was measured to be about 15 μs, corresponding to a minority carrier diffusion length of about 170 μm. After heating at 1000°C for less than an hour, the measured lifetime was only 10 μs. The reduction in lifetime was found to be independent of the surface treatment of the samples either before or after the heating step.

It should be possible to thermally treat Si in this way without significantly impacting the minority carrier diffusion length of the material. Thus, there must be an impurity that is introduced during the treatment. Careful degreasing of the wafers by sonication in series of organic and aqueous solvents, coupled with cleaning in piranha solution, should remove any surface contaminants prior to placing the samples in the tube furnace, but presence of such contaminants cannot be ruled out without further characterization. It is also possible that contaminants have been introduced to the samples from either the quartz tube (which is only used for pure Si, never with Au

contaminated samples) or from the gas delivery system itself. Any impurities introduced into the Si lattice during heating under an inert atmosphere are not likely due to the inert gas supply because different inert atmospheres produced the same drop in diffusion length.

This reduction in lifetime in the absence of the intentional introduction of impurities severely limits our ability to controllably produce Si samples having lifetimes between 10 μs and 1 ms. However, this does not preclude the possibility of studying the effects of Au impurity concentration on the photoelectrochemical properties of planar and porous samples. Even with a lifetime of 10 μs , the the minority carrier diffusion length is expected to be on the order 140 μm , which is enough that even the planar samples should retain most of their photoactivity. For porous samples, the pore-pore spacing is on the order of 5 μm , so diffusion lengths of 140 μm should give nearly 100% quantum yield.

3.4.2.2 Bulk Lifetime After Gold Doping

By controllably introducing Au into the Si samples, the lifetime could be lowered from the value measured after only heating the samples. A schematic of the diffusion process is shown in Figure 3.8. It has been shown previously that the equilibrium solubility of Au in Si is strongly dependent on temperature.^{58,60} Therefore, by depositing Au on the Si surface at low temperature and driving it in at high temperature, the bulk concentration of Au should be set at the solubility limit of the drive-in temperature. After drive-in, any remaining Au film was removed from the Si surface. Furthermore, the near-surface region is expected to have a higher concentration of Au due accumulation of excess Au at surface defect sites. For that reason, after an initial treatment in aqua regia

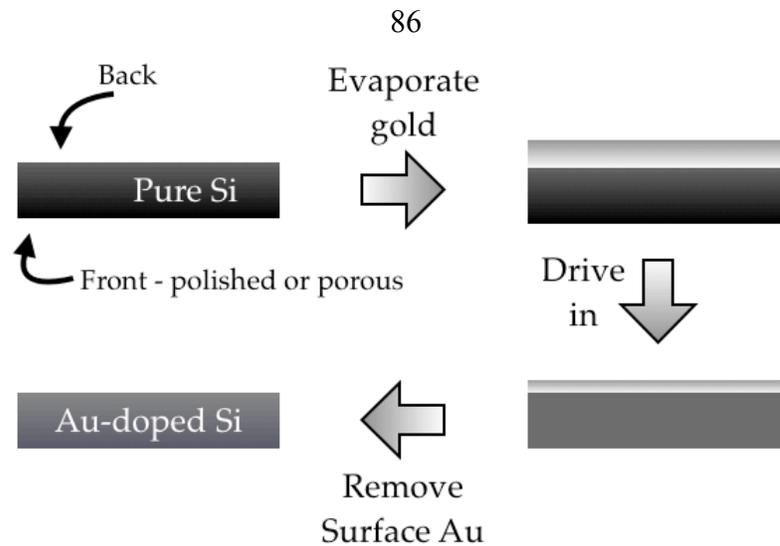


Figure 3.8. Schematic of Au doping process. Au is evaporated on one or both sides, (one side shown), then driven in at elevated temperatures. Subsequent removal of the Au film leaves the doped substrate.

to remove the film of excess Au, the samples were oxidized briefly in piranha solution and the resulting oxide layer removed in HF. Finally, any exposed surface Au was removed in aqua regia again. Since the bulk lifetime was measured by the contactless RF photoconductivity decay method, it was important to produce clean interfaces that could be well passivated in HF. As above, the observed lifetimes give a lower bound on the bulk lifetime and surface recombination.

Float-zone Si samples with Au diffused from both sides were used to calibrate the dependence of the bulk minority carrier lifetime on the expected Au concentration based on the drive-in temperature. As shown in Table 3.3, there was a significant effect of the drive-in temperature on the measured lifetime. The expected solubility limits at each temperature are also given in the table as C_{max} . However, as described in Section 5.2.1, the expected lifetime at a Au concentration of 10^{16} cm^{-3} is much smaller than the measured lifetime. Thus, it is expected that the actual Au concentration in the samples was significantly lower than the solubility limit.

Table 3.3. Lifetime values measured by RF photoconductivity decay and the corresponding calculated values of the diffusion length at each temperature for Au drive in. The drive-in time was calculated as described in the Experimental Section.

Temperature (°C)	C_{max} (cm ⁻³)	τ (μ s)	L_p (μ m)
1000	6.3×10^{16}	1.3	51
900	1.0×10^{16}	1.4	53
800	1.8×10^{15}	6.7	120
600	5.0×10^{14}	15	170
1000 (No Au)	-	10	140
No bake, No Au	-	1000	1400

It is evident from Table 3.3 that controlling the temperature of the drive-in step affords some control over the lifetime, and therefore the minority carrier diffusion length, in these DSP float-zone samples. However, even at the highest temperature used, the minority carrier diffusion length is still an order of magnitude larger than the approximate pore-pore spacing found in randomly templated macroporous Si. Thus, little decrease in the photoelectrochemical performance of porous silicon samples is expected, even with the highest concentrations of Au explored. For planar Si, the penetration depth of white light exceeds 100 μ m, so a significant reduction in current is expected for planar samples with the highest concentrations of Au.

3.4.2.3 Photoelectrochemical Measurements of Gold Doped Samples

Photoelectrochemical measurements were carried out on planar and macroporous samples derived from Czochralski-grown (100) n-type Si with a resistivity of 4-8 Ω -cm. The macroporous samples were etched for 60 min to produce pores with a length of approximately 85 μ m (see Chapter 2).¹ For the porous samples, it was found that the

porous structure had to be produced first before the Au diffusion step—when anodizing Au-doped samples, the light intensity needed to produce the desired current was not achievable with the typical pore etching setup. Since the mechanism of pore etching on n-type Si is proposed to be due to a hole-limited reaction at the pore tips,^{10,18} the inability to pass enough current through Au-doped samples during etching further corroborates the lowering of the minority carrier diffusion length by Au doping, implying recombination of photogenerated holes in the bulk. Since the pores could not be etched after Au doping, the drive-in step was carried out in a one-sided fashion from the back of porous samples. Au is only evaporated onto the back of the sample to avoid contamination of the highly structured front surface. The drive-in time was corrected appropriately for the one-sided diffusion process.

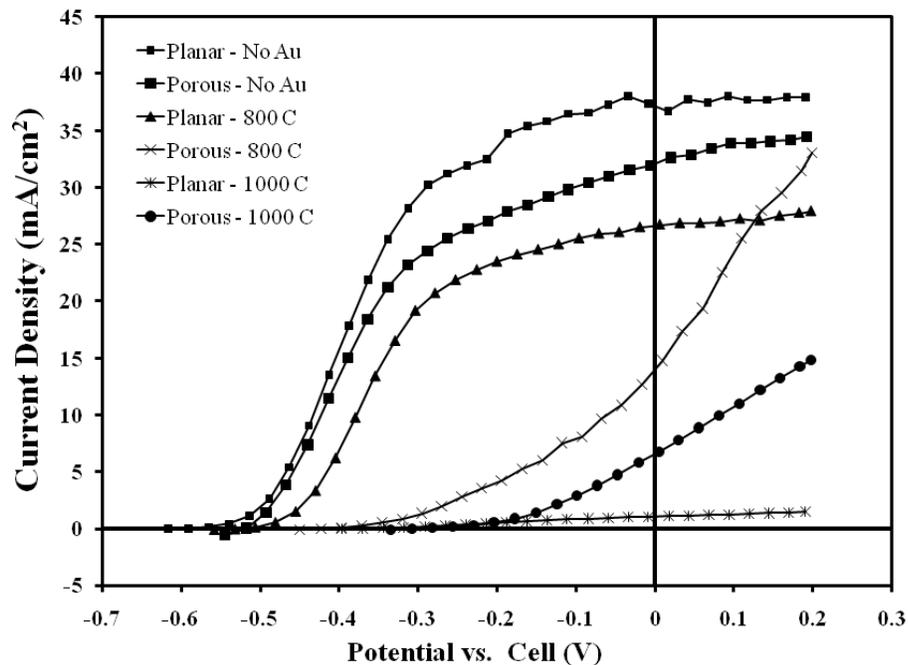


Figure 3.9. *J-E curves for porous and planar samples with various levels of gold doping. The curves were taken in the cell as described in the Experimental Section. All curves were collected under simulated AM 1.5 illumination, and the Au drive-in temperature is indicated. Samples designated as “No Au” were never in contact with Au and were not heated. These curves are representative for each type of sample.*

Representative J - E curves obtained under AM 1.5 illumination with both planar and porous Au-doped samples are shown in Figure 3.9. Samples were produced at two different drive in temperatures—800°C and 1000°C. It is apparent from the figure that the planar sample with drive in at 800°C still shows good performance. The planar samples are expected to perform well at this Au concentration due to the long minority carrier diffusion lengths, as calculated above ($\sim 120 \mu\text{m}$). The macroporous Si samples, however, show significant degradation even at the low concentration of Au. In particular, there seems to be a significant shunt or a very high resistance present. It is possible that the behavior observed is due to a high resistance at the back contact of the sample and not to poor performance in the porous sample. It is also possible that Au accumulates at defect sites on the porous front surface, and that these defect sites are not efficiently etched by the Au removal procedure.

Both the macroporous and planar samples show decreased performance when the Au drive-in temperature is increased to 1000°C, particularly in the fill factor. A summary of the relevant solar cell figures of merit is given in Table 3.4. In particular, we note that,

Table 3.4. Figures of merit for Au-doped Si electrodes. Temperatures indicated in the Sample Type column are the drive-in temperatures. Data are the mean of three electrodes (six for Au-free electrodes) and errors are the standard error of the mean.

Sample Type	J_{sc} (mA cm ⁻²)	V_{oc} (mV)	Fill Factor (%)	Efficiency (%)
Planar	36.2 ± 2.6	566 ± 2	44.6 ± 1.6	9.1 ± 0.5
Porous	31.5 ± 1.8	485 ± 12	41.3 ± 0.8	6.3 ± 0.5
Planar 800°C	26.0 ± 0.8	517 ± 1	44.0 ± 0.9	5.9 ± 0.1
Porous 800°C	10.4 ± 2.1	380 ± 0.1	22.5 ± 1.7	0.9 ± 0.2
Planar 1000°C	1.9 ± 1.1	362 ± 10	29.0 ± 7.4	0.1 ± 0.1
Porous 1000°C	7.2 ± 0.3	291 ± 14	18.7 ± 1.0	0.4 ± 0.1

after driving Au in at 1000°C, the macroporous samples show significantly higher J_{sc} and efficiency than the planar sample. In spite of the poor fill factors, these data show that, at low minority carrier diffusion lengths, structuring of the junction can lead to an improvement in charge carrier collection.

Given the consistently poor fill factor in all but the planar, 800°C samples, we explored the possibility that Au doping or one of the processing steps was causing an increase the sample resistivity. To accomplish this, planar samples were doped with Au as usual at 1000°C, and two ohmic contacts were made to the same sample with Ga/In eutectic by the usual procedure (see Experimental). Measurement of the two-point I-V curves on each sample then yielded linear plots from which the total resistance of the contacts and samples could be extracted. The values found from these measurements were typically quite high, in the range of k Ω . When the same experiment is conducted on Si that has not been treated in any way, the contact resistance is usually 10-15 Ω per contact, and the Si resistance is usually about 100-200 Ω for this geometry. Thus, either poor contact is being made to the electrodes, or the resistivity of the Si has increased significantly.

Further studies using the four-point probe technique, which should eliminate any contact resistance,⁶² showed very high resistivities in Au-doped Si, on the order of 100 Ω -cm. This is more than an order of magnitude higher than what is observed before Au doping (typically 5-7 Ω -cm). Furthermore, the observed increase in resistivity is certainly due to the evaporation and drive in of Au as heating samples in the absence of Au does not produce a measurable change in their resistivity. The increase in resistance

of samples with high concentrations of gold has been shown previously, where it was observed that the sample resistivity could increase by up to four orders of magnitude when the Au concentration was comparable to or greater than the dopant level in n-type Si.⁵⁸ This effect is believed to originate from the ionization of donor atoms into the Au state that is slightly above midgap in Si.^{58,62} Thus, for the samples used in this study, which have a doping level near 10^{15} cm^{-3} , a large increase in resistance is expected at high Au concentrations. In this case, the increase is only a little more than one order of magnitude, which provides further evidence that the Au concentration is not as high as expected based on the solubility limit at the drive-in temperature.

The observation of very high resistivity in Au-doped Si accounts only in part for the poor fill factors observed. Even with a resistivity of $100 \text{ } \Omega\text{-cm}$, the dimensions of the

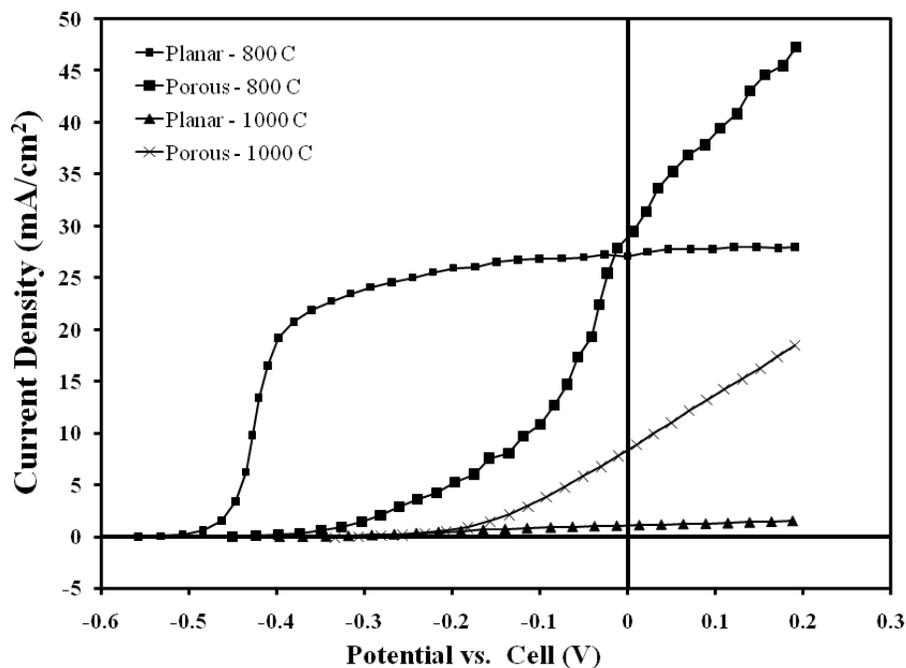


Figure 3.10. *J-E curves for porous and planar samples with significant Au doping after correction for $300 \text{ } \Omega$ series resistance. These samples are still not corrected for the expected solution resistance or the concentration overpotential losses. Representative samples are shown.*

electrodes are such that the uncompensated resistance due to the sample is expected to be around 300 Ω . The data from Figure 3.9 are replotted in Figure 3.10 after correction for 300 Ω series resistance. For the planar sample driven in at 800°C, the correction for this resistance is probably too much since the concentration overpotential loss has not been accounted for in this plot, and we expect the resistance to be less for samples treated at 800°C. For the other Au-doped samples, the fill factor remains quite poor in spite of the correction for the expected resistance. Thus, it is likely that there are other contributors to the observed low fill factors. Nevertheless, these data do show some improvement when changing from planar to porous in samples driven in at 1000°C.

3.4.2.4 *Continuation Advice*

Continuation of this work would necessitate the understanding of the two key issues faced in reliably making and measuring Au-doped structured samples as photoelectrodes. First, the mechanism responsible for the decrease in lifetime observed upon heating pristine Si under an inert atmosphere would need to be elucidated. A good starting point for this would be to use a different tube and tube furnace in order to eliminate the equipment used as a possible source of contamination. Even with fine control over the Au doping procedure, the nature of the increased resistivity observed in the presence of high Au concentrations may be another barrier to producing reliable photoelectrochemical measurements. One avenue to pursue on this front would be to use more highly doped Si, although this would significantly change the size of the pores produced during anodization. As another avenue, one could perform diffusion doping on the porous samples after Au doping to lower the sample resistivity. Control of this

system and its further study may also prove beneficial as a method for understanding the materials properties of Si wires grown by chemical vapor deposition from metal catalysts (see chapters 4 and 5).

3.4.3 Reactive Ion Etched Pillars

In order to show experimental evidence that increased junction area leads to a decreased V_{oc} , with all other factors being the same, reactive ion etching (RIE) was used to produce Si pillars from high quality n-type Si with known materials properties.^{3,4} A cryogenic inductively coupled plasma (ICP) RIE system was used to produce pillars with extremely high aspect ratios by etching away the surrounding Si (Figure 3.11). The ring visible halfway up the pillars in Figure 3.11 is due to the two-step etching approach that was used to make the wires longer. The initial phase of the etching undercuts the pattern

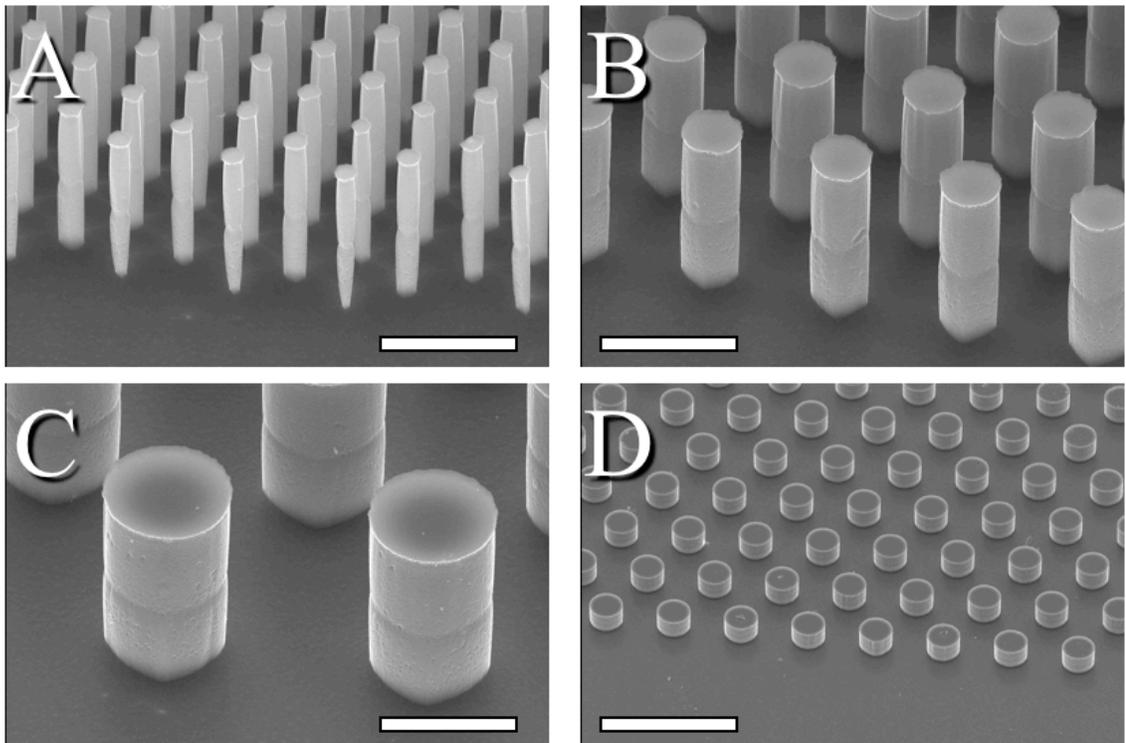


Figure 3.11. SEM micrographs of RIE pillars. All are shown at a 45° angle. A) 5 μm pillar mask. Scale bar, 20 μm. B) 10 μm pillar mask. Scale bar, 20 μm. C) 20 μm pillar mask. Scale Bar, 20 μm. D) 50 μm pillar mask. Scale bar, 200 μm.

slightly, giving rise to a ring at the top, and the process is reinitiated after some etching has been accomplished to increase the pillar length, causing another ring in the middle of the pillars. Four different pillar arrays were fabricated with pillar diameters of 5, 10, 20, and 50 μm . Each of the arrays of pillars produced was hexagonally arranged with the closest edge-to-edge distance equal to the diameter of the pillars. In this way, fractional filling area of Si in the pillar layer is the same in each array, so that the primary change is in the total junction area of the array. Thus, we expect to see a decrease in V_{oc} with decreasing pillar diameter due to the increased junction area.

Representative J - E curves for RIE pillar arrays are shown in Figure 3.12. The planar sample shown is derived from the sections of the sample that were not patterned and is therefore representative of the state of the wafer surface after the RIE procedure. It

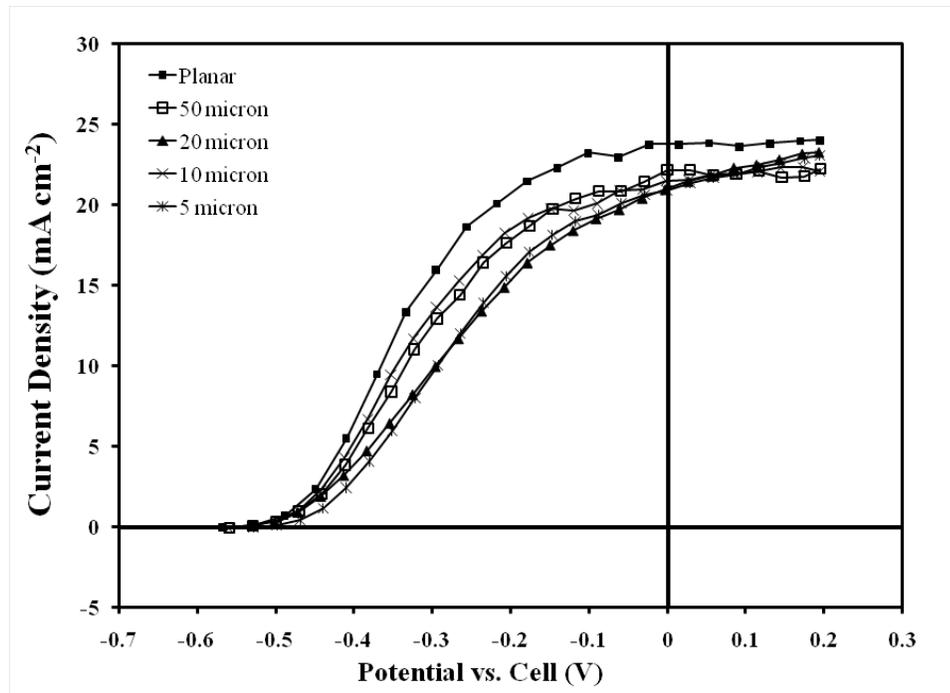


Figure 3.12. J - E curves of RIE pillar array samples under simulated AM 1.5 illumination. Representative samples are shown. Note that the curves are similar for all array dimensions tested. Cell setup and contents are described in the Experimental Section.

was found to be vitally important to the photoelectrochemical behavior of the pillar arrays to remove the near surface layer of the Si. Therefore, the results shown in Figure 3.12 are for samples that have been thermally oxidized and etched back to remove approximately the top 50 nm of Si from the surface. From this figure, it is apparent that the J - E curves show similar characteristics across all of the pillar diameters tested.

The solar cell performance figures of merit for the pillar arrays are shown in Table 3.5. Most of the figures of merit are the same across all conditions tested to within the error of the measurements. In particular, the measured voltages are indistinguishable. With pillars that are 5 μm in diameter and only 30 μm long, the surface area enhancement factor, γ , is approximately 12 (See Section 1.3.1). Thus, we would expect a decrease in V_{oc} of ~ 64 mV for 5 μm diameter pillars as compared with the planar sample. Clearly, this trend is not observed in the data presented here. However, the calculation of 60 mV V_{oc} loss per decade of surface area enhancement assumes that the charge carriers are harvested uniformly across all of the junction area. Any deviation from this assumption is expected to decrease the total voltage reduction observed. This is because non-uniform

Table 3.5. Solar cell figures of merit for pillar arrays. Values reported are the average of three independent electrodes. Planar samples were taken from the same substrate as the pillar array samples. Errors reported are the standard error of the mean.

Pillar Diameter	J_{sc} (mA cm ⁻²)	V_{oc} (mV)	Fill Factor (%)	Efficiency (%)
Planar	26.6 \pm 1.9	532 \pm 10	37.0 \pm 0.4	5.2 \pm 0.4
5 μm	22.4 \pm 1.5	523 \pm 15	34.6 \pm 0.9	4.1 \pm 0.5
10 μm	20.6 \pm 0.8	538 \pm 1	37.6 \pm 2.0	4.2 \pm 0.1
20 μm	18.2 \pm 1.3	535 \pm 5	34.0 \pm 2.9	3.3 \pm 0.1
50 μm	21.1 \pm 0.2	538 \pm 2	37.8 \pm 1.5	4.3 \pm 0.2

harvesting of minority carriers across the junction will lead to areas with high voltages and areas with low voltages. These localized areas will then behave like diodes connected in parallel with each other, in which case the total observed voltage is expected to be only slightly lower than that in the high voltage regions.⁶³ Coupled with the fact that a reduced V_{oc} was observed with increasing pore length in Chapter 2, the results presented here therefore imply that there is a nonuniform voltage generated across the sample. Given that the pillars are only 30 μm tall and spaced relatively far apart, we suggest that the observed constant V_{oc} is due to the contribution of the substrate, which is probably absorbing most of the carriers in this geometry. Since the arrays used were designed to have a constant filling fraction of wires, the substrate makes the same contribution in all array sizes. Therefore, we propose that the effect of increased junction area in the pillars is not the primary factor being probed in these experiments, but rather the constant junction area of the underlying substrate.

In order to use RIE pillars to demonstrate the desired dependence of V_{oc} on junction area, it would be necessary to use significantly longer pillars packed much closer together. With more light absorbed by the pillars, their effect on the observed photoelectrochemical properties will be larger. Furthermore, these results demonstrate the danger in assuming uniform distribution of carriers across the junction area when using a light source that is incident from the tops of the structures. In future studies, it will be important to optimize the structures used and to use wavelengths of light that give rise to relatively uniform carrier generation throughout the volume of the structured sample.

3.5 Conclusions

The studies contained in this chapter were directed toward proving that the possibility for radial charge carrier collection should increase J_{sc} in materials of low quality and that increasing junction area at a constant light flux should lead to a lowered V_{oc} . By diffusing Au into Si at high temperatures, an improvement in J_{sc} for porous samples over planar samples was shown for materials with low minority carrier diffusion lengths. However, the performance of both porous and planar samples with high concentrations of Au showed poor fill factors which could not be explained by the observed increase in the resistivity of the substrates following Au drive in. It is interesting to note that low fill factors have also typically been observed in Si wire arrays grown by the chemical vapor deposition method from Au catalyst (see chapters 4 and 5). It is possible that there is a common mechanism leading to the observed poor fill factors in samples having high concentrations of metals, even accounting for a change in the resistivity of the material. Future research on the photoelectrochemical performance of Si wire arrays would benefit from a more detailed understanding of this phenomenon.

Silicon pillar array samples with a range of diameters were found to have nearly identical values of V_{oc} for all sizes of pillars tested and for planar samples. This result does not invalidate the expectation that increased junction area per unit of projected surface area will lead to a decrease in V_{oc} . Rather, it points to the fact that care must be taken in design of physical model systems. In this case, it is likely that the photoelectrochemical behavior of the samples was dominated by contributions from the substrate rather than from the pillars themselves. Thus, further physical model systems

will require either separation of the structured material from the substrate or densification of the structured material so that the majority of the incident radiation is absorbed in the structured layer.

3.6 References

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