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Marc Riedel

Education

[1997 - 2003] California Institute of Technology Pasadena, CA
Ph.D. , *Electrical Engineering (*defended Nov. 17, 2003*)*
Dissertation: Cyclic Combinational Circuits.
Teaching: CNS 188, Computation Theory and Neural Systems.

[1995 - 1997] California Institute of Technology Pasadena, CA
Master's of Science, *Electrical Engineering*
Grade-Point Average: 3.9 (on a scale of 4.0)

[1991 - 1994] McGill University Montreal, Quebec
Bachelor's of Engineering (*Electrica*l)
Minor in Mathematics
Grade-Point Average: 3.8 (on a scale of 4.0), ranked 2nd in class.
J.W. McConnell Scholarship.

[1988 - 1991] Champlain College Montreal, Quebec
Diploma of Collegiate Studies, *Pure & Applied Sciences*
Medal of the Governor General of Canada for highest achievement.
Grade average: 94%, ranked 1st in graduating class of 654 students.

Professional experience

[1993, 4 mos.] Fujitsu Laboratories Kawasaki, Japan
Research Internship, *Neural Networks Group, Intelligent Systems Laboratory*.
Devised a novel algorithm for combinatorial optimization with Hopfield neural networks.

[1992, 1991, 8 mos.] Toshiba Systems Center Fuchu, Japan
Student Researcher*, Vision Group, Engineering Automation Section*
Developed an object recognition algorithm for an automated subway platform monitoring system.

[1990, 1989, 8 mos.] CAE Electronics Montreal, Quebec
Programmer Analyst*, Nuclear Simulations Dept.*
Coded auxiliary control modules for a real-time simulation model of a nuclear power plant.

[1988 3 mos.] Marconi Canada Montreal, Quebec
Student Intern*, Avionics Division*
Structured a database for organizing and retrieving information on Avionics expenditures.

Publications and Patents

Refereed Research Papers

- **Cyclic Combinational Circuits:**
  Timing Analysis and Synthesis for Delay
  Marc Riedel and Jehoshua Bruck
  International Workshop on Logic Synthesis, 2004.

- **The Synthesis of Cyclic Combinational Circuits**
  Marc Riedel and Jehoshua Bruck
  Design Automation Conference, 2003, received Best Paper Award

- **Cyclic Combinational Circuits: Analysis for Synthesis**
  Marc Riedel and Jehoshua Bruck
  International Workshop on Logic Synthesis, 2003.

- **Computing in the RAIN: A Reliable Array of Independent Nodes**
  V. Bohossian, C. Fan, P. LeMahieu, M. Riedel, L. Xu, and J. Bruck
  IEEE Transaction on Parallel and Distributed Computing, 2001

- **Tolerating Faults in Counting Networks**
  Marc Riedel and Jehoshua Bruck
  International Workshop on Dependable Network Computing, 1998

- **Fault Coverage Analysis of RAM Test Algorithms**
  Marc Riedel and Janusz Rasjki
  IEEE International VLSI Test Symposium, 1995

Patents

- **Method and Means for the Synthesis of Cyclic Combinational Circuits**, , U.S. Patent (*pending*)
  Marc Riedel and Jehoshua Bruck

- **A Reliable Array of Distributed Computing Nodes**, U.S. Patent **6,128,277,** *Oct. 3, 2000*
  V. Bohossian, C. Fan, P. LeMahieu, M. Riedel, L. Xu, and J. Bruck

Languages English and French