Nanoscale Field Emission Devices for High-Temperature and High-Frequency Operation

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ABSTRACT

Field emission—the quantum-mechanical tunneling of electrons from the surface of a material into vacuum by means of a strong electric field—has been studied for over a century. However, the usage of devices based on this mechanism has been limited to a handful of niche applications such as high-power RF systems and field emission displays. The preference for solid-state devices relies on their low cost, long lifetimes, reduced power consumption, ease of integrability, and simple and scalable fabrication. Nonetheless, with the advent of modern fabrication techniques, it has been possible to build field emission devices with nanoscale dimensions that offer several advantages over traditional semiconductor devices. The use of vacuum allows ballistic transport with no lattice scattering. As device capacitance can be engineered by tuning the geometry, these devices are appealing for high-frequency operation. Vacuum is also inherently immune to harsh operating conditions such as high temperature and radiation, which is desirable for aerospace, nuclear, and military applications. In addition, even though field emission requires substantial electric fields, by exploiting the nanoscale gaps that can be easily fabricated with state-of-the-art lithographic capabilities, we can expect operating voltages comparable to CMOS. Thus, vacuum emission devices have the potential to greatly improve upon the limitations of current technologies.

In this work, we experimentally demonstrate various design paradigms to develop nanoscale field emission devices for high-temperature environments and high-frequency operation. First, we propose suspended lateral two- and four-terminal devices. By removing the underlying solid substrate, we aim to increase the resistance of the leakage current pathways that emerge at elevated temperatures. Tungsten is the chosen electrode material due to its low work function and ability to withstand high temperatures. Our next architecture consists of a multi-tip two-terminal array, which exclusively relies on the inherent fast response of field emission. Due to the strong non-linearity in the emission characteristic, frequency mixing is measured. Lastly, we combine field emission with plasmonics to conceive devices that can be modulated both electrically and optically at telecommunication wavelength. By taking advantage of the strong confinement and significant optical field enhancement of surface plasmon polaritons, we seek to minimize the applied voltages required for field emission as well as the necessary laser powers for photoemission towards the development of high-speed, low-power, nanoscale optoelectronic systems.

PUBLISHED CONTENT AND CONTRIBUTIONS

[1] L. B. De Rose, W. M. Jones, and A. Scherer. "Lateral nanoscale field emission comb for frequency mixing." *[Manuscript submitted]* (2023).
L.D. participated in the conception of the experiments. L.D. led the sample fabrication, measurements, and writing of the manuscript.

[2] L. B. De Rose et al. "Effect of praseodymium coating on electron emission from a nanoscale gold field emitter array." *[Manuscript submitted]* (2023).
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[3] S. M. Lewis et al. "Tuning the performance of negative tone electron beam resists for the next generation lithography." *Advanced Functional Materials* 32.32 (2022), p. 2202710. DOI: 10.1002/adfm.202202710.
L.D. performed the tungsten etch.

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L.D. participated in the sample fabrication and measurements.

[5] L. B. De Rose, A. Scherer, and W. M. Jones. "Suspended nanoscale field emitter devices for high-temperature operation." *IEEE Transactions on Electron Devices* 67.11 (2020), pp. 5125–5131. DOI: 10.1109/TED.2020.3019765.
L.D. participated in the conception of the experiments. L.D. performed the simulations, led the sample fabrication, and wrote the manuscript.

[6] S. M. Lewis et al. "Plasma-etched pattern transfer of sub-10 nm structures using a metal–organic resist and helium ion beam lithography." *Nano Letters* 19.9 (2019), pp. 6043–6048. DOI: 10.1021/acs.nanolett.9b01911.
L.D. performed the tungsten etch.

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LIST OF ABBREVIATIONS

BHF Buffered hydrofluoric acid
BS Beamsplitter
CCP Capacitively coupled plasma
CMOS Complementary metal–oxide–semiconductor
CNT Carbon nanotube
Cr Chrome
CVD Chemical vapour deposition
EBL Electron beam lithography
EDFA Erbium-doped fiber amplifier
FEA Field emitter array
FED Field emission display
FEM Finite element method
FET Field effect transistor
FFT Fast Fourier Transform
FIB Focused ion beam
FinFETs Fin field-effect transistors
FN Fowler-Nordheim
FP Frenkel-Poole
GAA Gate-all-around transistors
HF Hydrofluoric acid
HIM Helium ion micrographs
IC Integrated circuit
ICP Inductively coupled plasma
ICP-RIE Inductively-coupled plasma reactive-ion etcher
IF Intermediate frequency
IPA Isopropyl alcohol
IV Current-voltage
LO Local oscillator
MIBK Methyl isobutyl ketone
MIM Metal-insulator-metal
MOSFET Metal–oxide–semiconductor field-effect transistor
NEA Negative electron affinity
NIR Near-infrared
PCB Printed circuit board

PEC Proximity effect correction

PECVD Plasma-enhanced chemical vapour deposition

PMMA Poly(methyl methacrylate)

Pr Praseodymium

RD Richardson-Dushman

RF Radio frequency

RIE Reactive-ion etching

SEM Scanning electron micrograph

Si Silicon

Si_3N_4 Stoichiometric silicon nitride

SiN_x Amorphous silicon nitride

SN Schottky-Nordheim

SOG Spin-on-glass

SOI Silicon-on-insulator

SPP Surface plasmon polariton

SSE Solid-state electronic

TE Transverse electric

Ti Titanium

TM Transverse magnetic

UHV Ultra-high vacuum

UNCD Ultrananocrystalline diamond

W Tungsten

WKB Wentzel-Kramers-Brillouin

Chapter 1

INTRODUCTION

Electronics constitutes the backbone of modern life. For the last 100 years, it has transformed almost every aspect of society. It has facilitated global communication, increased human lifespan, enabled space exploration, simplified trade, and improved numerous areas such as defense, education, utilities, and food production and distribution to name a few. Due to its versatility, the applications of this technology are so extensive that it is easier to think of where electronic devices are used than where they are not. From phones and navigation devices, to heart-rate monitors and chicken feeding systems, electronics has become an indispensable and ubiquitous part of humankind, making it impossible to imagine a world without it.

In the first half of the twentieth century, all electronic devices used vacuum tubes in their circuits. Some of the most important technological accomplishments attributed to vacuum tubes include the development of the radio, television, radar equipment, and long-distance telephone. Vacuum tubes were also a key component in the world's first electronic general-purpose programmable digital computer, the ENIAC (more formally known as the Electronic Numerical Integrator And Computer). This computer was built between 1943 and 1945 for the U.S. Army. It used almost 17,500 vacuum tubes, weighed 30 tons, covered around 170 square meters of floor space, and consumed 150 kilowatts of electric power [1]. Due to its unprecedented ability to be programmed to execute complex sequences of operations at electronic speed, the ENIAC launched a new era: the Information Age.

However, the emergence of the transistor and later integrated circuit (IC) technology quickly replaced vacuum tubes in almost all areas. Solid-state electronic (SSE) devices were less fragile, more energy efficient, smaller, and, above all, able to be mass-produced. Consequently, vacuum electronic devices based on thermionic emission were displaced to a handful of niche applications such as microwave power amplifiers, cathode ray tubes, and high-temperature and radiation environments.

Today, transistors are deeply embedded in almost all electronic devices. They can be manufactured so small that billions of them can be packed into a single microprocessor. Yet, despite the apparent pushover of the transistor, vacuum technology did not perish. Paradoxically, the same fabrication and processing tools developed to

reduce the size of solid-state ICs also enabled the miniaturization of vacuum technology, giving rise to the fields of vacuum micro and nanoelectronics. By reducing their physical dimensions, vacuum devices can leverage some distinct inherent advantages including ballistic electron transport and resilience in harsh environments. The resurgence of this technology appears to be timely, as SSEs seem to be reaching their technical limitations. The steady shrinkage of the transistor has become detrimental, as issues related to heat dissipation and quantum effects are emerging.

In this chapter, we reference some key historical events to better understand the context that brought about the electronics revolution of the last century, beginning with the invention of the vacuum tube. We also discuss the current state of SSE devices as well as their technical limits. Finally, we provide an overview of some exciting prospects for vacuum nanoelectronics to help overcome these limitations.

1.1 Over a Century of Vacuum Tubes

The first measurement of atmospheric pressure has been attributed to E. Torricelli in 1643. He carried out his famous experiment with a mercury-filled tube, becoming the first person to successfully produce a vacuum. A couple of years later, O. von Guericke made the first functional piston pump, the precursor of all vacuum technologies. While some improvements were made, the design of the solid-piston pump remained unchanged for about 200 years. Yet, the second half of the 19^{th} century saw an accelerated development of vacuum pumps and pressure gauges, as well as advancements in seal technology, largely fueled by the demands of the growing incandescent lamp industry. Two of the most important inventions include the mercury-piston pump as well as the McLeod gauge [2].

In 1883, T. Edison was studying the cause of uneven blackening inside his carbon filament incandescent lamp that affected the efficiency and lifetime of the bulb. He experimented by adding an extra electrode to the setup, observing that current would only flow to it when it was positively biased. This observation became known as the "Edison effect" and is regarded as one of the most important experiments in thermionic emission. However, unable to satisfactorily explain his discovery, he did not conduct further research on this topic. In 1904, J. Fleming used Edison's findings to develop the first practical vacuum tube device, the thermionic diode. It consisted of an evacuated glass bulb with two terminals: an electron-emitting cathode and an anode. Current would flow through the cathode electrode causing it to heat, leading to some electrons gaining enough kinetic energy to escape via

thermionic emission. The anode electrode would be positively biased to collect these emitted electrons. However, if a negative voltage was applied, no current would flow through the anode. This unidirectional behaviour was then used to rectify high-frequency electromagnetic waves, which became particularly useful in telegraph-receiving stations to detect radio signals. Because of this invention, Fleming is considered by many to be the "father of electronics" [3, 4].

In the years that followed, significant progress was made to the diode. In 1906, L. De Forest added a wire grid between the anode and the cathode, known as the control grid, and invented the triode. By adjusting the grid voltage, the electron current between the other two terminals was controlled, thus enabling signal amplification, which was crucial for long-distance radio and telephone communication [5]. A fourth grid, known as the screen grid, was added between the control grid and the anode to reduce the capacitance between these two terminals caused by the Miller effect [6]. An additional grid, called the suppressor grid, was placed closer to the anode to prevent secondary electron emission from the anode to the screen, which caused instability. These devices became known as the tetrode and the pentode, respectively. Further improvements to vacuum tubes included the replacement of carbon filaments with tungsten filaments and later by thoriated tungsten and oxide-coated filaments, which increased the emission efficiency as well as the lifetime. Moreover, multiple advances in vacuum techniques were made, including the invention of the rotary oil pump, the molecular drag pump, and the mercury diffusion pump, as well as the introduction of getters [7, 8].

The hegemony of the vacuum tube lasted almost half a century. The urge to operate at higher frequencies than those attainable with vacuum tubes, as well as the significant advancements made in quantum mechanics during the 1920s, especially the development of electronic band structure, encouraged the research in SSEs. In 1947, J. Bardeen, W. Brattain, and W. Shockley demonstrated the first working point-contact transistor at Bell Labs. A year later, Shockley also developed the junction transistor. Two other breakthroughs in SSE technology came with the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) by D. Kahng and M. Atalla, and the introduction of the IC by J. Kilby [9]. Due to their smaller size, higher efficiency, longer lifetimes, ability to be mass-produced, and ease of integration, transistors quickly displaced the bulky vacuum tubes. Only in a handful of niche applications did vacuum technology still prevail, such as microwave power amplifiers and X-ray tubes.

1.2 Dennard Scaling and Moore's Law and the Future of Electronics

For more than 50 years, the semiconductor industry has followed Moore's law, which states that the number of transistors per die doubles approximately every two years. This prediction was originally proposed by G. Moore in 1965 and has since been the operating principle at the forefront of microchip development, as it describes a commitment of developers to continuously advance the performance of ICs. Owing to the exponential improvement outlined in Moore's law, the primitive and exclusive personal computers manufactured in the 70s quickly gave rise to the advanced and ubiquitous smartphones available today [10, 11].

The success of Moore's law can be greatly attributed to the ability to shrink solid-state devices. The basic principle of geometric scaling was originally proposed by R. Dennard in 1975, and it is commonly referred to as Dennard scaling. A summary of Dennard scaling is outlined in Table 1.1 where κ is a unitless scaling factor. The core concept consists in simultaneously scaling three variables of a device, namely its physical dimensions, doping concentration, and voltage. All linear dimensions are reduced by the common factor κ. This includes horizontal dimensions such as channel length and width, as well as vertical dimensions such as gate insulator thickness. In addition, the substrate doping concentration is increased by κ, and the voltages applied are reduced by κ. As a consequence, the electric field of the scaled device remains constant, which is vital to maintaining reliability in terms of hot-carrier injection. Additionally, both the current and capacitance decrease by κ, which in turn decreases the circuit delay by κ and the power dissipation by κ^2. Ultimately, this results in the power per unit area, i.e., the power density,

Device or Circuit Parameter	**Scaling Factor**
Physical dimension L, W, t_{ox}	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $C = \epsilon A/t$	$1/\kappa$
Delay time per circuit VC/I	$1/\kappa$
Power dissipation per circuit VI	$1/\kappa^2$
Power density VI/A	1

Table 1.1: Basis of Dennard scaling for circuit performance (adapted from [12]).

remaining constant. This geometrical scaling allowed the number of transistors per chip to double with every new technology generation as well as to operate at higher maximum frequencies so that the overall performance was improved [12].

Continuous advances in semiconductor process technology were made to shrink the device dimensions. Most notably, new and improved lithographic techniques were developed to pattern smaller feature sizes. Lenses of higher numerical apertures and illumination sources with shorter wavelengths have been introduced. One major breakthrough has been the launch of extreme ultraviolet (EUV) lithography in chip manufacturing, which uses a wavelength of 13.5 nm to obtain higher resolution [13]. Moreover, significant progress has been made in the fabrication techniques to grow thinner gate oxides and to reduce defect levels at the ambitious dimensions demanded.

Furthermore, in 1991 the National Technology Roadmap for Semiconductors (NTRS) was created. The NTRS was a major cooperative effort of the semiconductor industry to coordinate what manufacturers and suppliers were doing so that targets and expectations for coming technology generations could be set. Every couple of years, a report predicting the rate of transistor scaling and technical challenges for the incoming years was released. In 1998, the NTRS was extended to include countries in Europe and Asia, becoming the International Technology Roadmap for Semiconductors (ITRS). In this way, the semiconductor industry ensured that new chips would stay on track with Moore's law.

However, reducing operating voltages to achieve high performance became steadily more problematic. As threshold voltages were reduced, subthreshold leakage currents–the current that flows from the source to the drain in a transistor when it is supposed to be off–exponentially increased. Consequently, static power dissipation became a dominant component of the total power consumption. In Fig. 1.1, the effect of reduced gate length in dynamic and subthreshold-leakage-power density is shown.

Moreover, gate oxide thickness reached its physical limit when Intel released its 65 nm generation transistor in 2005. The thickness of the gate dielectric of the device was 1.2 nm, which is equivalent to about 5 silicon (Si) atomic layers. At this thickness, gate leakage currents due to direct tunneling and hot-carrier injection from the substrate to the gate oxide became significant.

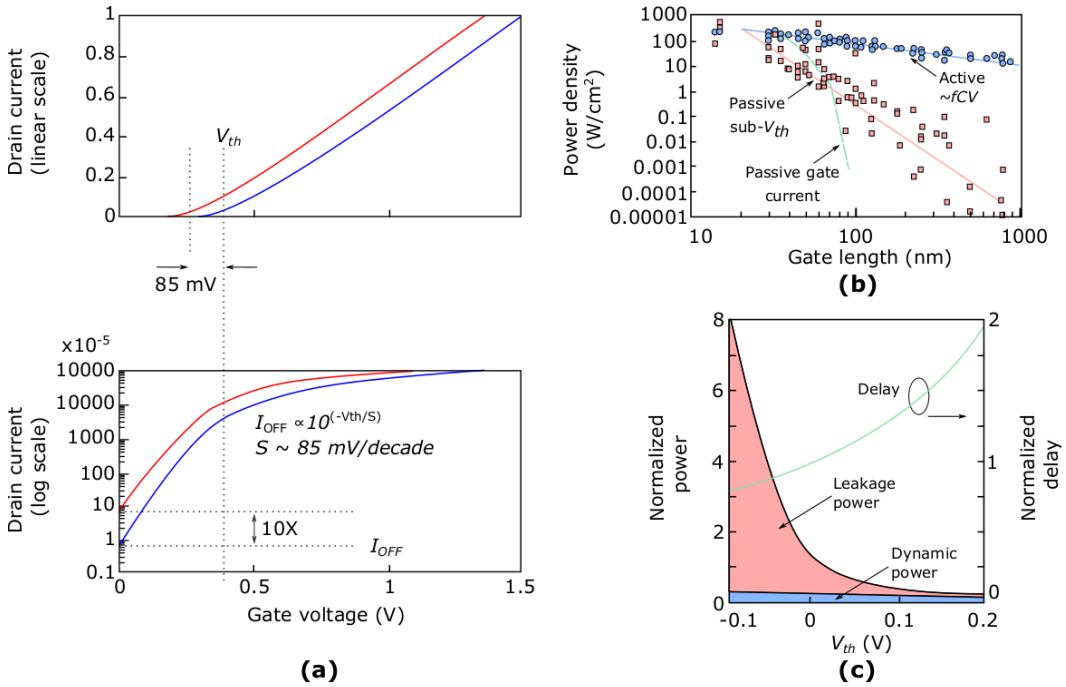

Figure 1.1: Effect of reduced gate length and operating voltages: (a) relationship between threshold voltage (V_{th}) and subthreshold leakage current (I_{OFF}) [14], (b) power density versus gate length [15], and (c) power and delay as a function of threshold voltage (V_{th}) with V_{DD} = 0.5V for 0.35 μm process [16].

Dennard scaling also considered that channel doping concentration could be continuously increased. At sufficiently high dopant concentrations, carrier mobility decreases as a result of increased impurity scattering, which deteriorates device operation. In addition, direct band-to-band tunneling increases reverse bias-pn junction leakage from the source/drain into the body [17].

Ultimately, the rapid growth in overall power consumption due to increased leakage currents became unfeasible. Thus, as fundamental thermal limits were reached by the early 2000s, Dennard voltage scaling came to an end. Because it became impossible to simultaneously increase the number of transistors per chip as well as the maximum operating frequency, clock frequencies plateaued as illustrated in Fig. 1.2 [18]. To keep up with Moore's law, multi-core architectures were introduced. In this type of parallel architecture, the operating frequency scaled down inversely proportionally to the number of cores, so that several processors working at a lower frequency were equivalent to a single processor working at its aggregate frequency. In 2001, IBM introduced the first commercially available dual-core microprocessor chip, the Power4 [19]. Performance was also improved by increasing caches sizes,

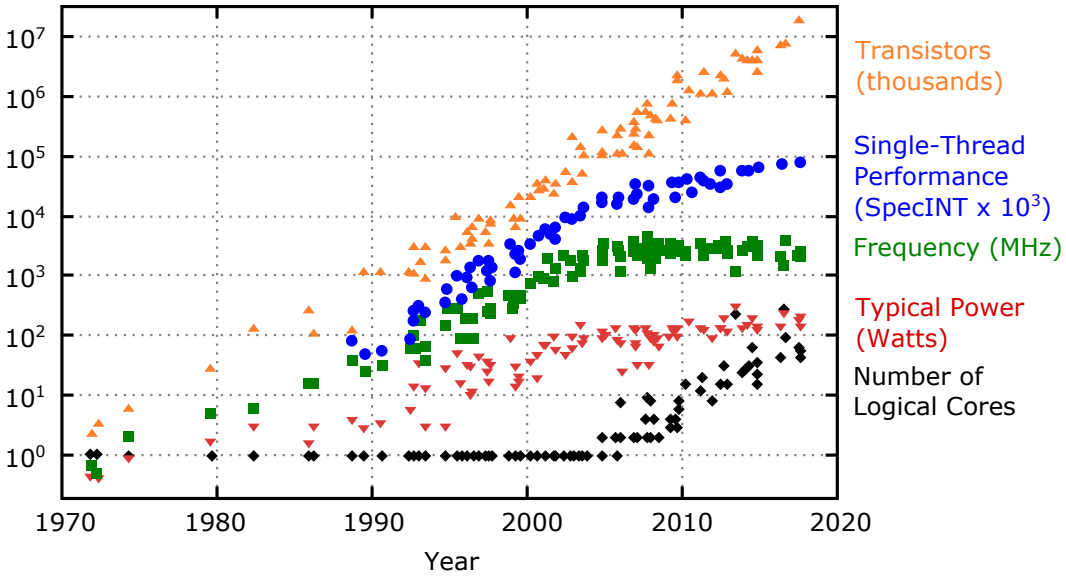

Figure 1.2: 42 years of microprocessor trend data [18].

as they are more energy efficient than main memory access [20]. Another ingenious concept to conserve power was developed, namely dark silicon, wherein a fraction of the die is underutilized [21]. Furthermore, much research has been conducted in developing new materials with higher dielectric constants and in stress engineering for enhanced channel mobility. Lately, new transistor designs have been driving the latest generation process nodes in which planar devices have given way to 3D architectures, including fin field-effect transistors (FinFETs), and most recently, gate-all-around transistors (GAA), as shown in Table 1.2 [22].

Even though dimensions are still shrinking and device performance is still improving, quantum and fundamental 3D topological limits will be reached soon. This can be seen in Fig. 1.3 [22], which predicts metal and gate pitch scaling ebbing away in the upcoming years. Thus, it seems that completely new computing paradigms should be embraced. Two very promising candidates are neuromorphic engineering and quantum computing. Yet, these technologies are still in their early stages and have a long way to go before they can be released for mass use and become mainstream. In the meantime, there is room to explore other options, especially for the applications in which solid-state devices do not excel. One such alternative are nanoscale field emission devices, which is the focus of this thesis.

YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
Logic device technology naming	G48M36	G45M24	G45M20	G40M16	G38M16T2	G38M16T4
Logic industry "node range" labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0nm eq"	"0.7nm eq"
LOGIC DEVICE GROUND RULES						
MPU/SoC M0 1/2 pitch (nm)	15	12	10.5	8	8	8
Physical gate length for HP logic (nm)	18	16	14	12	12	12
Lateral GAA (nanosheet) minimum thickness (nm)	-	-	7	6	5	5
Minimum device width (FinFET fin, nanosheet, SRAM) or diameter (nm)	7	6	7	6	5	5
LOGIC DEVICE ELECTRICAL						
Vdd (V)	0.7	0.7	0.65	0.65	0.6	0.6
LOGIC TECHNOLOGY ANCHORS						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, high-NA EUV	193i, high-NA EUV	193i, high-NA EUV
Beyond-CMOS as complimentary to platform CMOS	-	-	-	2D device, FeFET	2D device, FeFET	2D device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat
Process technology inflection	Conformal doping, contact	Channel, RMG	Lateral/ Atomic Etch	Non-Cu Mx	3D VLSI	3D VLSI
Stacking generation inflection	2D	3D stacking: W2W, D2W Mem-on-Logic	3D stacking: W2W, D2W Mem-on-Logic	3D stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D stacking, 3D VLSI: Mem-on-Logic with Intercon-nect	3D stacking, 3D VLSI: Logic-on-Logic

Notes: GxxMxxTx notation refers to Gxx—contacted gate pitch, Mxx—tightest metal pitch in nm, Tx—number of tiers, MPU—microprocessor unit, SoC—system on chip, HP—high performance,193i—193nm immersion lithography, DP—double patterning, FeFET—ferroelectric field-effect transistor, Ge—germanium, SiGe—silicon germanium, RMG—replacement metal gate, VLSI—very large scale integration, W2W—wafer to wafer, D2W—die to wafer, Mem-on-Logic—memory on logic

Table 1.2: Overall technology progression forecast (adapted from [22]).

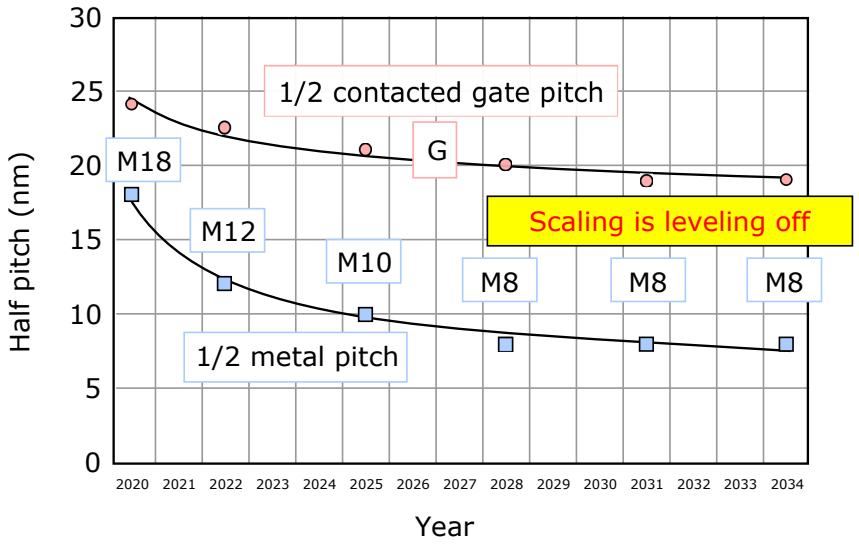

Figure 1.3: Metal and gate half pitch predictions (adapted from [22]).

1.3 The Emergence of Vacuum Micro and Nanoelectronics

After the invention of the transistor and subsequent ICs, it seemed that the days of vacuum technology were over. Solid-state devices were smaller and easier to fabricate and integrate. However, somewhat ironically, the same fabrication techniques that advanced SSEs also allowed for the miniaturization of vacuum technology, and thus, the field of vacuum micro and nanoelectronics was born.

The first person to conceive the idea and lay down the foundations of vacuum microelectronic devices was K. Shoulders of Stanford Research Institute (SRI) [23]. In 1961, he suggested reducing the size of electronic components by three orders of magnitude using microfabrication techniques and envisioned vertical and lateral field emission micro-triodes. Unlike the mature thermionic cathodes that needed an external source of heat to emit electrons from their surface, these devices just required a high enough electrostatic field that would cause the electrons to quantum mechanically tunnel and escape into vacuum. Even though devices based on field emission had existed for some time before (for instance, the field emission microscope had been invented by E. Müller in 1936), they had various weaknesses. The main issue was that they required high voltages (i.e., thousands of volts) due to their large cathode-to-anode separation, which often led to vacuum arcing and destruction.

In Shoulder's foresight, the smaller device dimensions would substantially reduce the operating voltage and considerably improve switching times. Another major

consequence of lower voltage operation would be a significant increase in lifetime, as sputtering damage due to ion bombardment would be minimized. Among the fabrication techniques, he comprehensibly described various material deposition methods, electron-beam lithography, dry etching, electron-beam microscopy, and integration with ultra-high vacuum (UHV) systems. These ideas were very innovative at the time as many of these microfabrication techniques had not been thoroughly developed yet. Overall, his objective was to fundamentally show vacuum ICs.

In spite of Shoulder's clear vision, it was not until 1968 when C. Spindt, who also worked at SRI, successfully fabricated and tested the first thin-film field emission cathodes [24]. The device consisted of a molybdenum/aluminum oxide/molybdenum sandwich with an array of open micro-size cavities fabricated on top of a sapphire wafer. A single conical molybdenum emitter tip was deposited at the center of each cavity. In this way, each emitter was surrounded by its own gate to modulate the emission current, which was in turn collected by an anode positioned above the array. The first set of devices consisted of an array of approximately 50 cathode tips over an active area of about 10^{-3} cm^2. Due to the sharp geometry of the emitter and the small gap between the emitter and the gate electrode, high local electric fields were produced at gate voltages of around 100 V. Another advantage of these emitters was that noise from a single emitter was statistically reduced by virtue of the large number of identical emitter tips. This field emitter array (FEA) became known as the Spindt emitter.

In the years that followed, the Spindt cathode was further improved, with packing densities increased to 1.5×10^7 cm^2 and current densities over 1000 A/cm^2 being measured. In addition, lifetimes of over 8 years of continuous operation with tip loading of 20 μA/tip (which was later increased to 50 μA/tip) were reported [25]. In 1972, N. Thomas et al. demonstrated Si-based FEAs. Silicon was a very convenient material for FEAs as it enabled manufacturers to take advantage of the highly developed microfabrication technology for mass production of Si ICs, such as preferential etching and polishing techniques [26]. Furthermore, in 1986 H. Gray and co-workers fabricated the first planar Si field emitter array vacuum field effect transistor [27]. In this device, the solid channel of a standard Si FET was replaced with vacuum, while the source consisted of an array of micron-size Si field emitters. This transistor not only produced voltage and power gain from gate modulation but also promised ultra-short transit times due to the faster electron transport inherent in vacuum at micron-scale cathode-to-anode separations. A breakthrough in electron

field emission came in 1982 when G. Binnig and H. Rohrer at IBM Zurich Research Laboratory invented the scanning tunneling microscope (STM), which allowed to image surfaces with atomic resolution [28]. A couple of years later, they were awarded the Nobel prize for their invention. In terms of commercial attention, FEAs only started to become popular in the late 80s when LETI successfully demonstrated a flat panel field emission display (FED) using molybdenum FEAs [29, 30]. Thanks to their high brightness, resolution, and quick response, research in FEDs was very promising.

As fabrication techniques continued to improve, devices could be manufactured with nanoscale dimensions, resulting in further reductions of turn-on voltages. For instance, Han et al. reported a surround gate nanoscale vacuum channel transistor with a sub-50 nm vacuum gap and a turn-on voltage under 5 V [31]. Additionally, when the cathode-to-anode separation is smaller than the mean free path of electrons in air under atmospheric pressure, the vacuum requirement can be effectively relaxed. The first successful operation of a field emission device at atmospheric pressures was demonstrated by Driskill et al. [32].

1.4 Could Nothing Be Better Than Something?

Devices based on field emission have several advantages as compared to their solid-state counterpart. First, field emission devices enable ballistic transport of electrons. In contrast to solid-state devices that employ semiconductor channels, field emission devices use vacuum as their transport medium. In semiconductors, electrons suffer from phonon scattering, which limits the maximum velocity a charge carrier can attain. The saturation velocity for Si is in the order of 1×10^7 cm/s and for gallium arsenide it is 1.2×10^7 cm/s, while the velocity of an electron in vacuum is theoretically about 3×10^{10} cm/s [33]. Consequently, higher cutoff frequencies could be achieved in vacuum devices. Additionally, due to the lack of energy dissipation in the channel, vacuum enables higher power operation than equivalent solid-state devices.

Second, vacuum devices are inherently more resilient to extreme temperatures. In semiconductors, the concentration of intrinsic carriers n_i depends exponentially on temperature T, as given by

$$n_i = \sqrt{n_c n_v} e^{-E_g/2k_B T} \tag{1.1}$$

where n_c and n_v are the effective density of states for electrons in the conduction band and holes in the valence band of the semiconductor, respectively, E_g is the

bandgap energy, and k_B is the Boltzmann constant. Fig. 1.4 illustrates the effect of temperature on the concentration of intrinsic carriers for various semiconductors. Thus, at sufficiently high temperatures, dopant atoms become overwhelmed by the uncontrollable concentration of intrinsic carriers, which ultimately renders the device ineffective at controlling carrier flow. Additionally, the leakage current of a reverse-biased pn junction is tied to the concentration of intrinsic carriers in semiconductors. Hence, at high temperatures, junction leakage current becomes a major problem in device operation, as performance is degraded and power consumption is subsequently increased. In order to circumvent these issues, the semiconductor industry has moved toward wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN). In this way, while the maximum operating temperature for Si devices is around 300 °C, this limit is extended to approximately 600 °C in SiC [34]. Metal field emitters, on the other hand, do not rely on chemical doping for their device operation. Therefore, they are relatively insensitive to temperature changes until the onset of thermionic emission. At the other extreme, vacuum devices are also better suited for low-temperature operation. This is because, at low temperatures, semiconductor devices freeze out due to the lack of thermal energy to fully ionize impurity atoms.

Moreover, vacuum devices are more resistant to radiation. Incident energetic heavy particle radiation can dislodge atoms and create a vacancy-interstitial pair, i.e., a

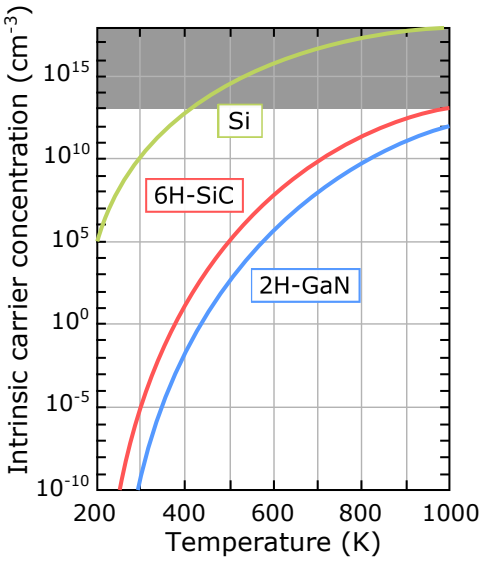

Figure 1.4: Intrinsic carrier concentration as a function of temperature for various semiconductors [34]. The shaded grey area corresponds to typical doping range.

Frenkel pair, in a crystalline semiconductor. This displacement damage creates deep-level traps in the band gap that serve as scattering and trapping centers, which increases junction leakage currents, reduces carrier mobility, and decreases minority carrier lifetime. This effect is particularly detrimental for minority carriers and optoelectronic devices. These collisions are irrelevant in vacuum devices as they can be manufactured with amorphous materials. Ionizing radiation can generate electron-hole pairs in gate oxides, which are quickly separated by the electric field. However, slow holes get easily trapped in oxide and interface traps. As a consequence of this charge buildup, parasitic fields are slowly created, which may irreversibly alter device properties such as the threshold voltage. Another type of radiation-induced damage is single-event effects caused by direct ionization. When a high-energy charged particle travels through a device, a high-density electron-hole plasma is created along its path due to the energy it loses by ionizing the device material. This can cause the device to malfunction, especially if it happens in a depletion region. The collected anomalous charge can also cause latch-ups, which can permanently damage ICs if the current is not quickly limited. The incident-charged particle can also damage thin gate oxides by creating a conduction path through it, which can lead to dielectric breakdown and subsequent device destruction. Several of these problems become trivial when vacuum is used instead of a gate dielectric [35, 36].

Field emission devices also enjoy some advantages over thermionic vacuum tubes. Cold field emission is a quantum mechanical process that does not require heating, thus reducing power consumption and eliminating the need for thermal management. As heating is not necessary, the distance between the electrodes can be very small. If the dimensions of the device are smaller than the elastic mean free path of electrons in air, which is around 200 nm at low electron energies [37], and the voltages are kept under the first ionization potential of molecules present in air (12.1 eV, 12.7 eV, 14.4 eV, and 15.6 eV for O_2, H_2O, CO_2, and N_2, respectively) [38], the device can potentially be operated at atmospheric pressures. Field emission devices can nowadays be easily miniaturized by employing the same fabrication techniques that are used to manufacture solid-state devices, offering a cost reduction in comparison to vacuum tubes. If CMOS-compatible materials are chosen, field emission devices could be integrated with SSEs for enhanced functionality.

In this way, field emission devices combine the advantages of traditional vacuum tubes and modern solid-state nanofabrication technology. Potential applications include sources in electron beam lithography (EBL) [39], microwave power ampli-

fiers [40], X-ray sources [41], free electron laser [42], and logic circuits for space communications. Due to its non-linear current-voltage (IV) characteristic and fast response time, field emission devices could also be used for high-frequency multipliers and converters. Lastly, the nanoscale vacuum transistor could potentially be a candidate to keep up with Moore's law.

1.5 Objective of This Work

The objective of this work is to experimentally study the phenomenon of electron field emission. Two- and four-terminal devices for use in high-temperature environments are designed, fabricated, and electrically characterized. In addition, two types of structures are demonstrated for high-frequency operation: a two-terminal device for frequency mixing, and a plasmonically-enhanced field emission device at telecommunications wavelength.

There are six chapters in this thesis and they are organized as follows:

Chapter 1 provides a brief introduction to vacuum technology. The history of the rise and fall of early vacuum devices is presented, followed by a discussion on the current state of SSEs. A description of the development of micro and nano field emission electronic devices is given, and the potential advantages over both solid-state and thermionic devices are discussed.

Chapter 2 details the theoretical background of various electron emission mechanisms. The processes of Fowler-Nordheim field emission, thermionic emission, and photoemission are analyzed. Bulk-limited conduction mechanism and space charge effect are also succinctly introduced.

Chapter 3 presents the fabrication, experimental results, and analysis of suspended lateral two-terminal diode-like and four-terminal triode-like vacuum field emitters for high-temperature environments. A description of early efforts as well as a discussion of suggestions for improvement and avenues for future work are included.

Chapter 4 experimentally demonstrates the use of multi-tip field emission devices for frequency conversion. Device design paradigms based on simulation results are detailed. In addition, preliminary results illustrating the effect of praseodymium thin film coating to reduce the work function and enhance emission current are reported.

Chapter 5 describes the efforts in combining Fowler-Nordheim emission with plasmonics to develop high-frequency optoelectronic devices. The design for efficient photonic mode to hybrid plasmonic mode conversion as well as nanofocusing is

presented, along with the fabrication steps and results for the proposed structure. Various ways to further optimize the architecture are examined.

Chapter 6 concludes the proposed research in nanoscale vacuum field emission devices.

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Chapter 2

THEORETICAL BACKGROUND OF ELECTRON EMISSION

Electron emission is the process by which electrons are extracted from the surface of a condensed phase, such as a metal, into another (usually a vacuum) through the use of an external energy source [1]. To free these bound electrons, an energy equal to the work function has to be provided, which is the minimum energy needed to remove an electron originally at the Fermi level from a solid to a point at rest in free space just outside the surface [2]. There are three main methods of electron emission: thermionic emission, field emission, and photoemission. In thermionic emission, the material is heated to sufficiently high temperatures, which causes the electron distribution to broaden so that some higher energy electrons can semi-classically overcome the work function and emit into vacuum [3, 4]. In field emission, a high electrostatic field is applied to the surface of the material allowing electrons to quantum-mechanically tunnel through the surface potential barrier [5, 6]. In photoemission, one or multiple photons are absorbed by the electron, providing the required energy to exceed the interfacial potential barrier [7, 8]. Note that a combination of several of these emission processes can also occur. Fig. 2.1 displays a general potential energy diagram as well as the Fermi-Dirac distribution function, $f(E)$, for the three individual processes of electron emission from a metal into vacuum. E_F is the Fermi level, ϕ is the metal work function, U is the vacuum potential level, and F is an externally applied electric field. In Fig. 2.1 (a), the Fermi-Dirac distribution function is plotted for a sufficiently high temperature, which, for illustration purposes, has been greatly exaggerated. In Figs. 2.1 (b) and (c), the thermal distribution considers the metal to be at room temperature.

In the following sections, the various emission phenomena are analyzed, with a special emphasis given to field emission, as it constitutes the underlying operating mechanism of all devices considered in this thesis. Furthermore, bulk-limited conduction mechanisms and the space charge effect are described.

2.1 Field Electron Emission

The phenomenon of field electron emission is quantitatively described by the Fowler-Nordheim (FN) theory, which was first introduced in 1928 by R. Fowler and L. Nordheim [9]. The FN theory is based on the quantum tunneling of electrons

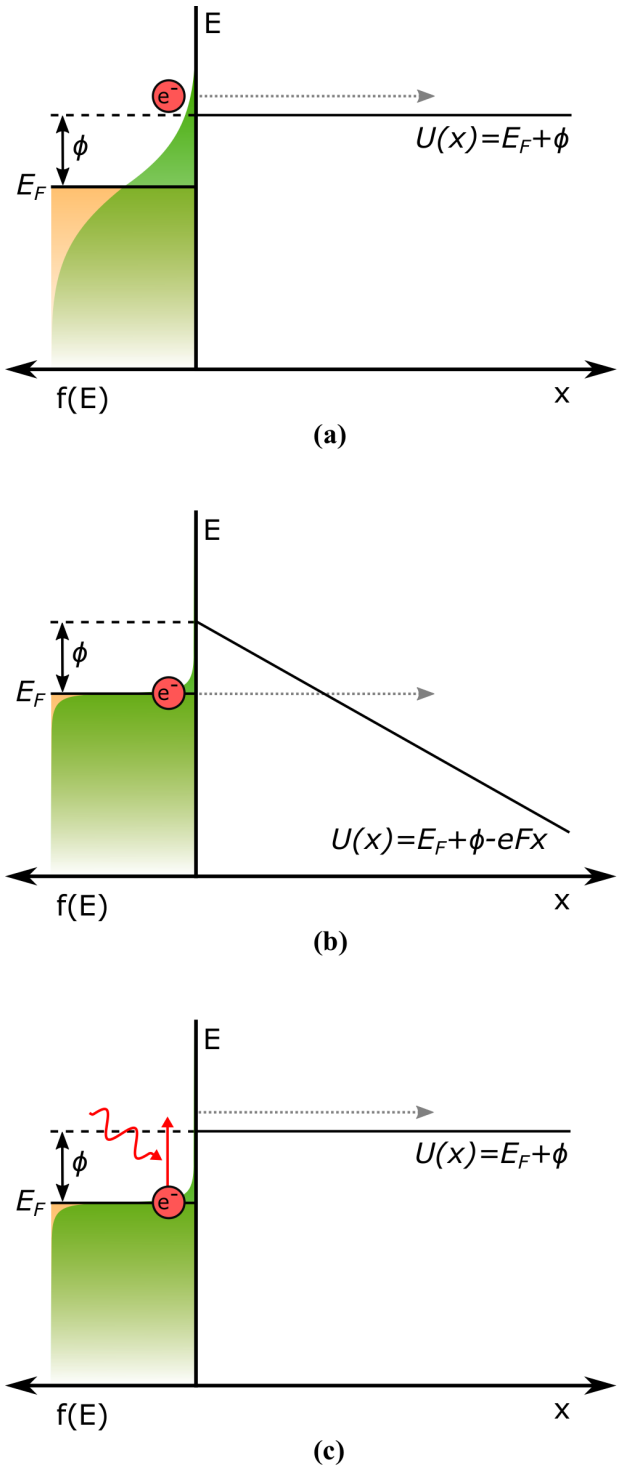

Figure 2.1: The three main electron emission mechanisms from metal to vacuum: (a) thermionic emission, (b) field emission, and (c) photoemission. E_F is the Fermi level, ϕ is the metal work function, U is the vacuum potential level, F is an externally applied electric field, and $f(E)$ is the Fermi-Dirac distribution function.

through the surface potential barrier when a high electric field is applied ($10^7 - 10^8$ V/cm). This high electric field causes the potential barrier at the metal-vacuum interface to become narrow enough so that electrons have a significant probability of tunneling into free-space. Thus, the FN theory essentially provides a mathematical formula that depicts the dependence of the emission current density on the strength of the applied external field.

To develop the FN theory, the following assumptions are made [10, 11]:

1. The Sommerfeld free-electron model with Fermi-Dirac statistics is used to model the behavior of the electrons in the metal, which are in thermodynamic equilibrium at the temperature $T = 0$ K.

2. The metal surface is smooth, flat, and planar. In this way, the effects of impurities, defects, and geometric shape of the emitter are ignored. This assumption also reduces the problem to tunneling in one dimension.

3. The metal work function, ϕ, is uniform. Since the applied electric field does not penetrate the metal, the electron states within the metal are independent of the external field. Outside the metal, the vacuum potential barrier can be regarded as an exact triangular potential.

Consider a metal emitter in the yz-plane occupying the half-space from $x = -\infty$ to $x = 0$, as shown in Fig. 2.2. Since the field emission phenomenon is fundamentally a quantum-mechanical tunneling process, the number of electrons incident on the potential barrier and the probability of those electrons tunneling through the surface barrier have to be determined. Therefore, the emission current density J_{FN} is given by [6]

$$J_{FN} = \int_0^\infty N(E_x)D(E_x)dE_x \tag{2.1}$$

where $N(E_x)dE_x$ is the number of electrons that cross a unit area from left to right in a direction parallel to the yz-plane per unit time with normal energy E_x between E_x and $E_x + dE_x$, and $D(E_x)$ is the probability of electrons tunneling through the vacuum potential barrier with normal energy E_x. $N(E_x)$ is more commonly known as the 'supply function' and $D(E_x)$ as the 'transmission coefficient.' Note that the lower limit of integration is 0 because no electrons are incident from the vacuum side, i.e., from right to left.

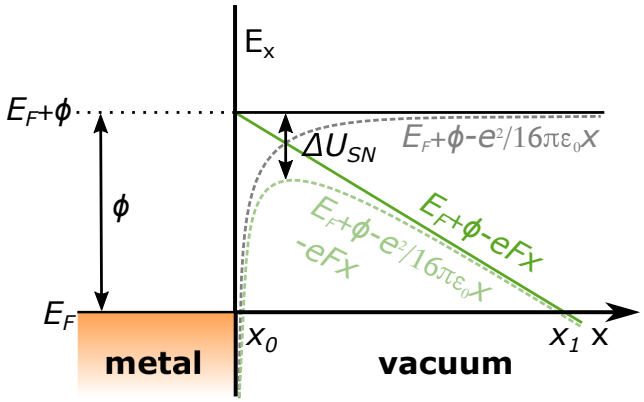

Figure 2.2: Field emission model: FN (solid) and SN (dashed) barriers.

In the free-electron model, the conduction band electrons are treated as free particles that do not interact with one another or with the ion cores. Considering the metal to be a sufficiently large rectangular box of volume L^3, where L denotes the length of its sides, and assuming Born-von Karman periodic boundary conditions, the electronic states are described by plane waves given by [12, 13]

$$\psi_{\mathbf{k}}(\mathbf{r}) = \frac{1}{\sqrt{L^3}} e^{i\mathbf{k}\cdot\mathbf{r}} \tag{2.2}$$

where the wave vector $\mathbf{k}$ is

$$\mathbf{k} = \frac{2\pi}{L}(n_x, n_y, n_z) \tag{2.3}$$

and n_x, n_y, and n_z are integers. In addition, the energy eigenvalues are

$$E_{\mathbf{k}} = \frac{\hbar k^2}{2m} \tag{2.4}$$

where m is the mass of the electron. This total electron kinetic energy E can also be separated into its normal E_x and transverse component E_p as [14]

$$E = E_x + \frac{\hbar k_p^2}{2m} \tag{2.5}$$

where $k_p^2 = k_y^2 + k_z^2$. The wave function $\psi_{\mathbf{k}}(\mathbf{r})$ is also an eigenstate of the momentum operator $\mathbf{p} = \frac{\hbar}{i}\nabla$ with eigenvalue

$$\mathbf{p} = \hbar\mathbf{k}. \tag{2.6}$$

Thus, the group velocity $\mathbf{v} = \frac{\mathbf{p}}{m}$ can be expressed as

$$\mathbf{v} = \frac{\hbar\mathbf{k}}{m}. \tag{2.7}$$

In order to calculate the supply function, we first define a supply function density $n(E, E_x)$ as

$$n(E, E_x) \equiv \frac{dN(E_x)}{dE}. \tag{2.8}$$

With this definition, the supply function as L goes to infinity can be expressed as

$$N(E_x)dE_x = dE_x \int_{E_x}^{\infty} n(E, E_x)dE. \tag{2.9}$$

The probability that an electron state with total energy E will be occupied in an ideal electron gas at equilibrium is given by the Fermi-Dirac distribution function

$$f(E) = \frac{1}{1 + e^{[(E-E_F)/k_BT]}} \tag{2.10}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, and E_F is the Fermi level. In reciprocal space, the supply function density can be written as

$$n(E, E_x)dE\,dE_x = 2j_x f(E)\frac{d^3k}{(2\pi/L)^3} \tag{2.11}$$

where j_x is the current density per unit cross-sectional area given by $j_x = \rho_e v_x$. ρ_e is the volume charge density, namely e/L^3, where e is the electronic charge, and v_x is the component of the group velocity of the electron normal to the unit area under consideration. Note that the factor of 2 in the equation is to account for spin degeneracy. Thus, Eq. (2.11) becomes

$$\begin{aligned} n(E, E_x)dE\,dE_x &= 2\left(\frac{ev_x}{L^3}\right) f(E)\frac{d^3k}{(2\pi/L)^3} \\ &= 2e\left(\frac{\hbar k_x}{m}\right) f(E)\frac{d^3k}{(2\pi)^3}. \end{aligned} \tag{2.12}$$

The differential d^3k can also be expressed as $d^3k = d^2k_p dk_x$. For a given E_x, d^2k_p can be expressed in cylindrical coordinates as $d^2k_p = 2\pi k_p dk_p$ or, in terms of energy, as $d^2k_p = 2\pi\frac{m}{\hbar^2}dE$. Consequently, the supply density function can be written as

$$n(E, E_x)dE\,dE_x = \frac{em}{2\pi^2\hbar^3} f(E)dE\,dE_x, \tag{2.13}$$

which can be substituted back into Eq. (2.9) to yield

$$\begin{aligned} N(E_x) &= \frac{em}{2\pi^2\hbar^3}\int_{E_x}^{\infty} \frac{dE}{1 + e^{(E-E_F)/k_BT}} \\ &= \frac{emk_BT}{2\pi^2\hbar^3} \ln\left[1 + e^{\left(-\frac{E_x-E_F}{k_BT}\right)}\right]. \end{aligned} \tag{2.14}$$

The next step is to calculate the transmission coefficient. The most widely used approach is to approximate $D(E_x)$ utilizing the Wentzel-Kramers-Brillouin (WKB) method [15].

The general problem is to find solutions to the time-independent Schrödinger equation for the exact triangular potential shown in Fig. 2.2 given by

$$U(x) = (E_F + \phi - eFx)\theta(x) \tag{2.15}$$

where $\theta(x)$ is the Heaviside step function. With this potential, the Schrödinger equation for $x > 0$ becomes

$$\left[\frac{d^2}{dx^2} + \frac{p^2(x)}{\hbar^2}\right]\psi(x) = 0 \tag{2.16}$$

where $p(x) = \{2m[E - U(x)]\}^{1/2}$. If the potential $U(x)$ varies slowly in comparison to de Broglie wavelength λ given by $\lambda = 2\pi\hbar/p(x)$, it can be expected that over a region small compared to the distance over which $U(x)$ varies considerably, ψ will closely approximate the free particle state. Yet, since λ changes slowly with x, the change in wavelength over a length λ is

$$\delta\lambda = \frac{d\lambda}{dx}\lambda. \tag{2.17}$$

In the classical domain, this only makes sense if $\delta\lambda \ll \lambda$, so that

$$\begin{aligned}\left|\frac{\delta\lambda}{\lambda}\right| &= \left|\frac{(d\lambda/dx)\cdot\lambda}{\lambda}\right| \\ &= \left|\frac{d\lambda}{dx}\right| \ll 1.\end{aligned} \tag{2.18}$$

The expression $\frac{d\lambda}{dx}$ can also be written as

$$\begin{aligned}\frac{d\lambda}{dx} &= -\frac{2\pi\hbar}{p^2}\frac{dp}{dx} \\ &= \frac{2\pi\hbar}{2m[E - U(x)]}\frac{(2m)^{1/2}}{2[E - U(x)]^{1/2}}\frac{dU}{dx} \\ &= \frac{2\pi m\hbar}{p^3}\frac{dU}{dx}.\end{aligned} \tag{2.19}$$

Therefore, the semi-classical calculation provided by the WKB method is valid as long as [16]

$$\left|\frac{\delta\lambda}{\lambda}\right| = \left|\frac{2\pi m\hbar}{p^3}\frac{dU}{dx}\right| \ll 1. \tag{2.20}$$

The ansatz of the solution to Schrödinger equation that is valid in the near-classical domain is assumed to be of the form [17, 18]

$$\psi(x) = e^{\frac{iS(x)}{\hbar}} \tag{2.21}$$

with $S(x)$ an unknown complex function. Inserting this function into Eq. (2.16) yields

$$-\left(\frac{1}{\hbar}\frac{\partial S}{\partial x}\right)^2 + \frac{i}{\hbar}\frac{\partial^2 S}{\partial x^2} + \frac{p^2(x)}{\hbar^2} = 0. \tag{2.22}$$

Expanding $S(x)$ in powers of $\hbar$ gives

$$S(x) = S_0(x) + \hbar S_1(x) + \hbar^2 S_2(x) + \ldots \tag{2.23}$$

In the limit $\hbar \to 0$, λ tends to zero, so the spatial variation of the potential can be regarded to be small. Inserting Eq. (2.23) into Eq. (2.22) and grouping the terms with the same power of $\hbar$ gives

$$\frac{1}{\hbar^2}\left[p^2 - \left(\frac{\partial S_0}{\partial x}\right)^2\right] + \frac{1}{\hbar}\left(i\frac{\partial^2 S_0}{\partial x^2} - 2\frac{\partial S_0}{\partial x}\frac{\partial S_1}{\partial x}\right) + O(\hbar^0) = 0. \tag{2.24}$$

Note that the coefficients for each power of $\hbar$ must vanish independently. The $\hbar^{-2}$ term gives

$$\left(\frac{\partial S_0}{\partial x}\right)^2 = p^2 \tag{2.25}$$

or

$$S_0(x) = \pm \int_{x_0}^{x_1} |p(x)|\, dx. \tag{2.26}$$

The $\hbar^{-1}$ terms yields

$$i\frac{\partial^2 S_0}{\partial x^2} = 2\frac{\partial S_0}{\partial x}\frac{\partial S_1}{\partial x}. \tag{2.27}$$

Substituting Eq. (2.26) into this expression gives

$$S_1(x) = i \ln\left[|p(x)|\right]^{1/2}. \tag{2.28}$$

In this way, $\psi(x)$ becomes

$$\begin{aligned}\psi(x) &= Ce^{-\ln[p(x)]^{1/2}} e^{\left[\pm\frac{i}{\hbar}\int_{x_0}^{x_1}|p(x)|dx\right]} \\ &= \frac{C}{[p(x)]^{1/2}} e^{\left[\pm\frac{i}{\hbar}\int_{x_0}^{x_1}|p(x)|dx\right]}\end{aligned} \tag{2.29}$$

where the constant $C = \psi(x_0)p(x_0)^{1/2}$ is found by setting $x = x_0$. The transmission coefficient is calculated by

$$D(E_x) = \frac{j_{\text{tra}}}{j_{\text{inc}}} \tag{2.30}$$

where j_{tra} and j_{inc} are the transmitted and incident probability current densities, respectively. In general [19, 20],

$$j_\alpha = \text{Re}(\psi^\dagger \hat{v}_\alpha \psi) \tag{2.31}$$

or

$$j_\alpha = \frac{i\hbar}{2m}\left(\psi_\alpha \frac{\partial}{\partial x}\psi_\alpha^\dagger - \psi_\alpha^\dagger \frac{\partial}{\partial x}\psi_\alpha\right) \tag{2.32}$$

which gives the formula

$$D(E) = \exp\left[-\frac{2}{\hbar}\int_{x_0}^{x_1} |p(x)|\, dx\right] \tag{2.33}$$

so that

$$D(E_x) = \exp\left\{-\frac{2}{\hbar}\int_{x_0}^{x_1} \{2m[U(x) - E_x]\}^{1/2} dx\right\} \tag{2.34}$$

where the limits of integration are $x_0 = 0$ and $x_1 = \frac{\phi + E_F - E_x}{eF}$. In order to evaluate the definite integral

$$D(E_x) = \exp\left\{-\frac{2}{\hbar}\int_0^{\frac{E_F+\phi-E_x}{eF}} \{2m[E_F + \phi - eFx - E_x]\}^{1/2} dx\right\} \tag{2.35}$$

let $y \equiv \frac{eF}{E_F+\phi-E_x}x$. Eq. (2.35) then becomes

$$\begin{aligned} D(E_x) &= \exp\left\{-\left(\frac{2\sqrt{2m}}{\hbar}\right)\left[\frac{(E_F + \phi - E_x)^{3/2}}{eF}\right]\int_0^1 (1-y)^{1/2} dy\right\} \\ &= \exp\left\{\left(\frac{2\sqrt{2m}}{\hbar}\right)\left[\frac{(E_F + \phi - E_x)^{3/2}}{eF}\right]\left(\frac{2}{3}\right)(1-y)^{3/2}\Big|_{y=0}^{y=1}\right\} \\ &= \exp\left\{-\left(\frac{4\sqrt{2m}}{3\hbar}\right)\left[\frac{(E_F + \phi - E_x)^{3/2}}{eF}\right]\right\}. \end{aligned} \tag{2.36}$$

Note that

$$(E_F + \phi - E_x)^{3/2} = \phi^{3/2}\left(1 - \frac{E_x - E_F}{\phi}\right)^{3/2}. \tag{2.37}$$

The approximation $(1-x)^{3/2} \approx 1 - \frac{3}{2}x$ can be used to expand E_x at E_F so that

$$\begin{aligned} \phi^{3/2}\left(1 - \frac{E_x - E_F}{\phi}\right)^{3/2} &\approx \phi^{3/2}\left[1 - \frac{3}{2}\left(\frac{E_x - E_F}{\phi}\right)\right] \\ &= \phi^{3/2} - \frac{3}{2}(E_x - E_F)\phi^{1/2}. \end{aligned} \tag{2.38}$$

Let $b_{FN} \equiv \frac{4}{3e}\sqrt{\frac{2m}{\hbar^2}}$ and $\frac{1}{d_F} \equiv 2\sqrt{\frac{2m}{\hbar^2}}\frac{\phi^{1/2}}{eF}$. The transmission coefficient then becomes

$$D(E_x) \approx \exp\left(-\frac{b_{FN}\phi^{3/2}}{F}\right)\exp\left(\frac{E_x - E_F}{d_F}\right). \tag{2.39}$$

The final step is to combine the results of Eq. (2.14) and Eq. (2.39) with Eq. (2.1) to obtain the field emission current density

$$J_{FN} \approx \frac{emk_BT}{2\pi^2\hbar^3}\exp\left(-\frac{b_{FN}\phi^{3/2}}{F}\right)\int_0^\infty \exp\left(\frac{E_x - E_F}{d_F}\right)\ln\left[1+\exp\left(-\frac{E_x - E_F}{k_BT}\right)\right]dE_x. \tag{2.40}$$

Notice that near $T = 0$K, the expression $k_BT\ln\left[1+\exp\left(-\frac{E_x-E_F}{k_BT}\right)\right]$ can be approximated as

$$\begin{aligned} k_BT\ln\left[1+\exp\left(-\frac{E_x - E_F}{k_BT}\right)\right] &\approx k_BT\left(-\frac{E_x - E_F}{k_BT}\right) \\ &= E_F - E_x. \end{aligned} \tag{2.41}$$

As the emission process is dominated by electrons near the Fermi energy, the emission current density becomes

$$\begin{aligned} J_{FN} &\approx \frac{em}{2\pi^2\hbar^3}\exp\left(-\frac{b_{FN}\phi^{3/2}}{F}\right)\int_0^{E_F}\exp\left(\frac{E_x - E_F}{d_F}\right)(E_F - E_x)dE_x \\ &= \frac{em}{2\pi^2\hbar^3}\exp\left(-\frac{b_{FN}\phi^{3/2}}{F}\right)\left(d_F^2 - d_FE_Fe^{-\frac{E_F}{d_F}} - d_F^2e^{-\frac{E_F}{d_F}}\right). \end{aligned} \tag{2.42}$$

For field emission, $E_F \gg d_F$, thus $e^{-\frac{E_F}{d_F}} \approx 0$. Also, let us define $a_{FN} \equiv \frac{e^3m}{16\pi^2\hbar}$. Therefore, the current density ultimately becomes

$$J_{FN} \approx a_{FN}\frac{F^2}{\phi}\exp\left(-\frac{b_{FN}\phi^{3/2}}{F}\right) \tag{2.43}$$

This is the basic field emission equation, also known as the FN equation. The constants a_{FB} and b_{FB} given by

$$\begin{aligned} a_{FN} &= \frac{e^3m}{16\pi^2\hbar} \approx 1.54[\mu\text{A}][\text{eV}][\text{V}]^{-2} \\ b_{FN} &= \frac{4}{3e}\sqrt{\frac{2m}{\hbar^2}} \approx 6.83[\text{V}][\text{nm}]^{-1}[\text{eV}]^{-3/2} \end{aligned}$$

are the so-called first and second FN field emission constants, respectively. It is important to notice that the two most important variables in field emission are the

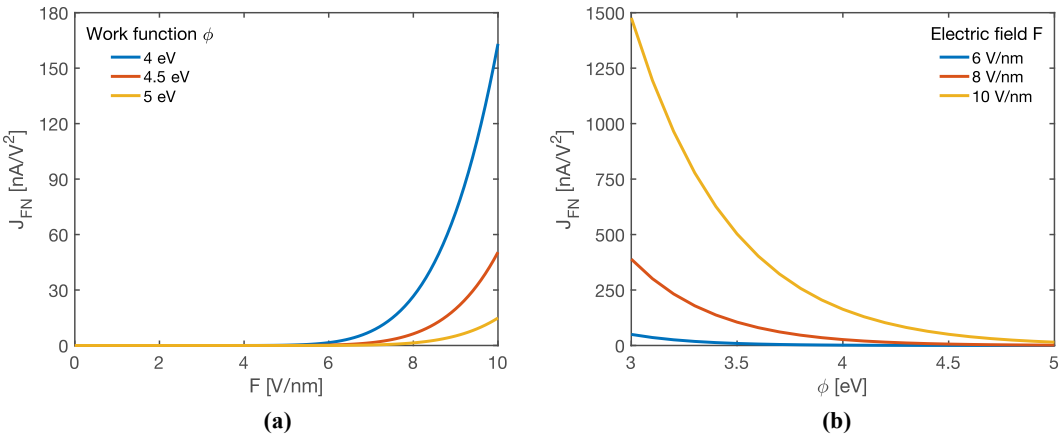

Figure 2.3: Emission current density as (a) a function of electric field for various work function values and (b) as a function of work function for various electric field values.

magnitude of the electric field and the work function. Fig. 2.3 shows the effect of these two parameters on the emission characteristic.

As we can see in Eq. (2.43), the FN equation relates current density and electric field intensity. Unfortunately, these quantities are hard to measure experimentally, especially at the nanoscale. Therefore, Eq. (2.43) is usually expressed in terms of the applied voltage V and the measured current I [21]. The applied voltage is related to the electric field by

$$F = \beta V \tag{2.44}$$

where β is the so-called field factor. As the emission does not take place from a single point on the emitter but rather an area, the current is obtained by integrating the current density J_{FN} over the whole emitting surface

$$I = \int_{(S)} J_{FN} dS \tag{2.45}$$

where S is the total surface of the emitting area. Often, it is assumed that the observable current is simply proportional to its density, i.e.,

$$I = S J_{FN}. \tag{2.46}$$

It is important to mention that the emission current density depends on the position at the emitter, so the relation shown above is just an estimate based on the fact that the derivation of the FN equation ignored the emitter dimension and shape. A more detailed study on the effective emission area is given in [22–25].

With these two relations, Eq. (2.43) is written as

$$I = a_{FN} S \frac{(\beta V)^2}{\phi} \exp\left(-\frac{b_{FN}\phi^{3/2}}{\beta V}\right). \tag{2.47}$$

In practice, measured field electron emission IV data is often analysed by means of the so-called FN plot, which allows us to quickly distinguish the field emission characteristic from other emission mechanisms. The FN plot is obtained by linearizing Eq. (2.47) to [26, 27]

$$\ln\left(\frac{I}{V^2}\right) = \ln\left(\frac{a_{FN} S \beta^2}{\phi}\right) - \frac{b_{FN}\phi^{3/2}}{\beta}\left(\frac{1}{V}\right). \tag{2.48}$$

In the FN plot, the y-axis is given by $\ln\left(I/V^2\right)$ and the x-axis by $(1/V)$, so that the emission data in this semi-logarithmic plot forms a straight line. The slope is given by

$$\text{slope} = -\frac{b_{FN}\phi^{3/2}}{\beta} \tag{2.49}$$

and the y-intercept by

$$y\text{−intercept} = \ln\left(\frac{a_{FN} S \beta^2}{\phi}\right). \tag{2.50}$$

Notice that there are three variables present in these two parameters: the work function ϕ, the emission area S, and the field factor β. If one of them is known a priori, the other two can be estimated from the values of the slope and intercept.

According to classical electrodynamics, the macroscopic electric field F_M between two planar structures, e.g., a parallel-plate capacitor, is given by $F_M = V/d$, where d is the separation between the two electrodes. However, it has been experimentally found that certain geometries support electron emission at fields smaller than the expected F_M. Sharp structures, such as lightning rods, can distort and bend the equipotential lines that exist from F_M in the proximity of the sharpened point, leading to an augmented electric field. The ratio between the local electric field F and the macroscopic field F_M is known as the field enhancement factor γ

$$\gamma = \frac{F}{F_M}. \tag{2.51}$$

The local field F can also be expressed as a function of the distance between the emitter and collector electrodes, d, by the relation $F = \gamma\frac{V}{d}$ [28].

So far, the derivation of the FN equation has assumed a simple triangular barrier. However, a more realistic model should include the exchange-and-correlation interaction between the electron just outside the emitter and the emitter surface [29].

In electrostatics, this image potential arises because an escaped electron located at a distance x away from the surface of the metal induces a charge distribution on the surface to screen the electric field of the electron inside the bulk. Effectively, this surface charge behaves as if there were a positive electron equidistant from the emitter surface. As a consequence, this interaction modifies the barrier potential function so that outside the surface of the metal it becomes

$$U(x) = E_F + \phi - eFx - \frac{e^2}{16\pi\epsilon_0 x} \tag{2.52}$$

where ϵ_0 is the vacuum permittivity [30]. This barrier potential is often referred to as the Schottky-Nordheim (SN) barrier. As seen in Fig. 2.2, the addition of this image potential has the effect of rounding the triangular potential, so that the peak of the barrier is reduced by $\Delta U_{SN} \equiv \left(\frac{e^3 F}{4\pi\epsilon_0}\right)^{1/2}$. The emission current density can also be derived using the WKB approximation to obtain

$$J_{FN} = a_{FN} \frac{F^2}{[\tau(y_F)]^2 \phi} \exp\left(-\nu(y_F) \frac{b_{FN}\phi^{3/2}}{F}\right) \tag{2.53}$$

where $\tau(y)$ and $\nu(y)$ are barrier shape correction factors that have been approximated to [31]

$$\nu(y) \approx 1 - y^2 + \frac{1}{3} y^2 \ln y \tag{2.54}$$

$$\tau(y) \approx 1 + \frac{1}{9} y^2 - \frac{1}{9} y^2 \ln y \tag{2.55}$$

with

$$y = \frac{1}{(E_F + \phi - E_x)} \sqrt{\left(\frac{e^3 F}{4\pi\epsilon_0}\right)} \tag{2.56}$$

and noting that y_F indicates that y is evaluated at $E_x = E_F$. The SN barrier is considered to be a better model, as it has been shown that the basic FN equation under-predicts current densities by a factor of order 100, and also leads to incorrect estimates of the emitting area [32].

Furthermore, recall that the temperature was assumed to be 0 K so mere field emission was studied. This assumption has been shown to be accurate up to well above room temperature [33, 34]. Because of this approximation, the emission process is commonly known as 'cold field emission.' If the effects of temperature on the FN model were to be considered, Eq. (2.43) can be modified to include a correction

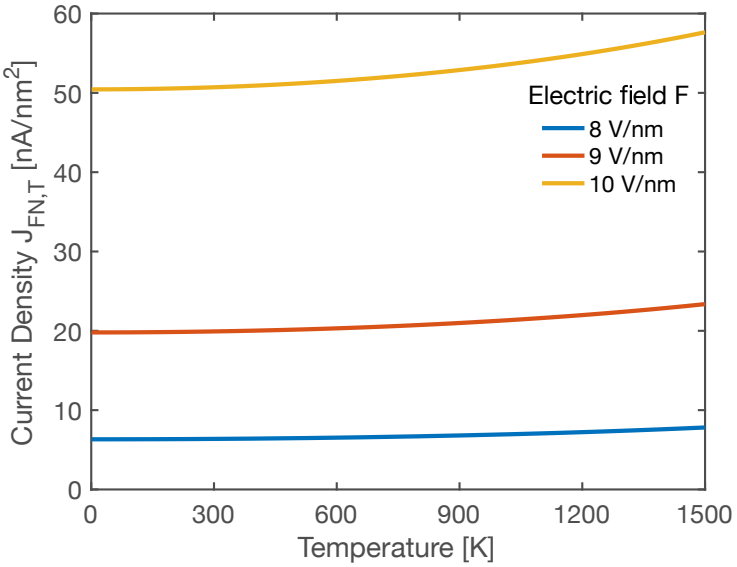

Figure 2.4: Emission current density as a function of temperature for various field values and a representative work function of 4.5 eV.

factor $\Theta_{FN}(T)$ so that the field emission current density at finite temperature $J_{FN,T}$ becomes

$$J_{FN,T} = \left[\frac{k_B T\pi/d_F}{\sin\left(k_B T\pi/d_F\right)}\right] J_{FN} \tag{2.57}$$

with $\Theta_{FN}(T) \equiv \frac{k_B T\pi/d_F}{\sin\left(k_B T\pi/d_F\right)}$. Fig. 2.4 illustrates the effects of finite temperature on the characteristics of field emission for various electric fields. We can see that even at relatively high temperatures, the variation in $J_{FN,T}$ is small so temperature effects can usually be neglected.

2.2 Thermionic Emission

The first equation for the emission current density from metal surfaces was proposed by O. Richardson using the Clausius-Clapeyron equation [35]. It was later modified by S. Dushman using quantum mechanics theory, leading to the renowned Richardson-Dushman (RD) equation for thermionic emission [36, 37], given by

$$J_{RD} = AT^2 \exp\left(-\frac{\phi}{k_B T}\right) \tag{2.58}$$

where A is a constant equal to

$$A = \frac{emk_B^2}{2\pi^2\hbar^3} \approx 120[\mathrm{A}][\mathrm{cm}]^{-2}[\mathrm{K}]^{-2}. \tag{2.59}$$

Eq. (2.58) is derived assuming that the electrons inside the metal behave as free particles and that the Fermi-Dirac distribution can be replaced by Maxwell-Boltzmann's distribution because at high temperatures only the electrons in the thermal tail of the supply function can escape from the metal, i.e., electrons with $E \gg E_F$ [38].

As we can see in Eq. (2.58), thermionic emission is strongly dependent on temperature. Therefore, to obtain significant electron emission, the metal emitter must be held at sufficiently high temperatures (over 1000 K). Also, similarly to FN, thermionic emission depends on work function, so materials with low work functions are desired to enhance emission.

2.3 Photoemission

The first experiments on the photoelectric effect were done by H. Hertz in 1887, years before the discovery of the electron by J. Thompson. In his experiment, he generated electromagnetic waves by spark discharge using an induction coil connected to a pair of capacitor plates attached to two metal spheres. The primary spark generated by this apparatus would then induce a secondary spark in a receiving circuit consisting of a micrometer spark gap attached to an open ring of wire. To see the spark better, he placed the secondary spark gap in a dark box and noticed that the voltage at which the sparking took place changed. He concluded that light produced by the primary spark was affecting the receiving spark. By using a quartz prism, he dispersed the radiation from various light sources and discovered that ultraviolet radiation was the cause for the increase in sparking. At the time, he could not explain his observations [39, 40]. Further experiments were later carried out by W. Hallwachs and P. Lenard. Yet, they were only explained in 1905 with A. Einstein's quantum theory of the photoelectric effect, for which he received the Nobel Prize in 1921 [41, 42].

In his article, Einstein suggested that the energy of light is not distributed continuously in space as J. Maxwell's theory dictated, but rather quantized [43]. The derivation of the concept of a quantum of light—the photon—was not based on experimental results but rather on statistical mechanics. Specifically, he considered that an isothermal change in volume from an initial volume V_1 to a final volume V_2 would cause a change in entropy due to radiation equal to $(k_B dE/h\nu) \ln(V_1/V_2)$, where dE is the total energy of the radiation in a frequency interval ν to $\nu + d\nu$, in which Wien's radiation law is satisfied. This expression showed the same logarithmic dependence on volume as the equation for the entropy of a monoatomic ideal gas as long as the number of particles in the gas is $dE/h\nu$, leading Einstein to conclude

that light must consist of particles with energy $h\nu$. This concept allowed him to explain several experiments, such as photoluminescence, the ionization of gases by ultraviolet radiation, and black-body radiation, which could not be explained using continuous spatial functions to describe light. He also ventured to explain the energy transfer from photons to electrons, leading him to the fundamental equation that is now known as the "photoelectric effect," given by

$$E_{kin} = h\nu - P \tag{2.60}$$

where E_{kin} is the maximum kinetic energy of the emitted electrons and P is the amount of work an electron must do to leave a solid and is characteristic of that solid, which is currently known as the work function ϕ. Even though this linear frequency relation was consistent with Lenard's experiments, which Einstein referred to in his publication, it was not until several years later that experiments conducted by A. Hughes, O. Richardson, K. Compton, and R. Millikan finally led to Einstein's model being generally accepted by the scientific community.

In the photoelectric effect, the absorption of photons by bound electrons in solids causes these electrons to transition to higher energy levels. If the energy of the photon is sufficiently large to overcome the material work function, the excited electrons can travel above the potential barrier and become free electrons. This is commonly referred to as photoemission [44, 45]. In the simplest case, one photon provides the required energy to overcome the work function, as shown in Fig. 2.5 (a). If multiple photons are absorbed to lift the electron over the potential barrier, the process is known as multi-photon emission. Moreover, in the special case where a greater number of photons than required for emission are absorbed, i.e., $N > \phi/h\nu$, the process is termed above-threshold photoemission. Both cases of multi-photon emission are depicted in Fig. 2.5 (b). It has been shown that in multi-photon emission, the photoelectron current density J_{multi} is proportional to the nth power of laser intensity I, i.e., $J_{multi} \propto I^N$, where N denotes the total number of photons absorbed [46–48].

In addition, an electron can be emitted into free space even if $Nh\nu < \phi$. In this case, the electron is promoted to a non-equilibrium electron distribution by the absorption of one or more photons and tunnels through the potential barrier, which has been narrowed by an applied DC bias [49, 50]. The emitted current density can

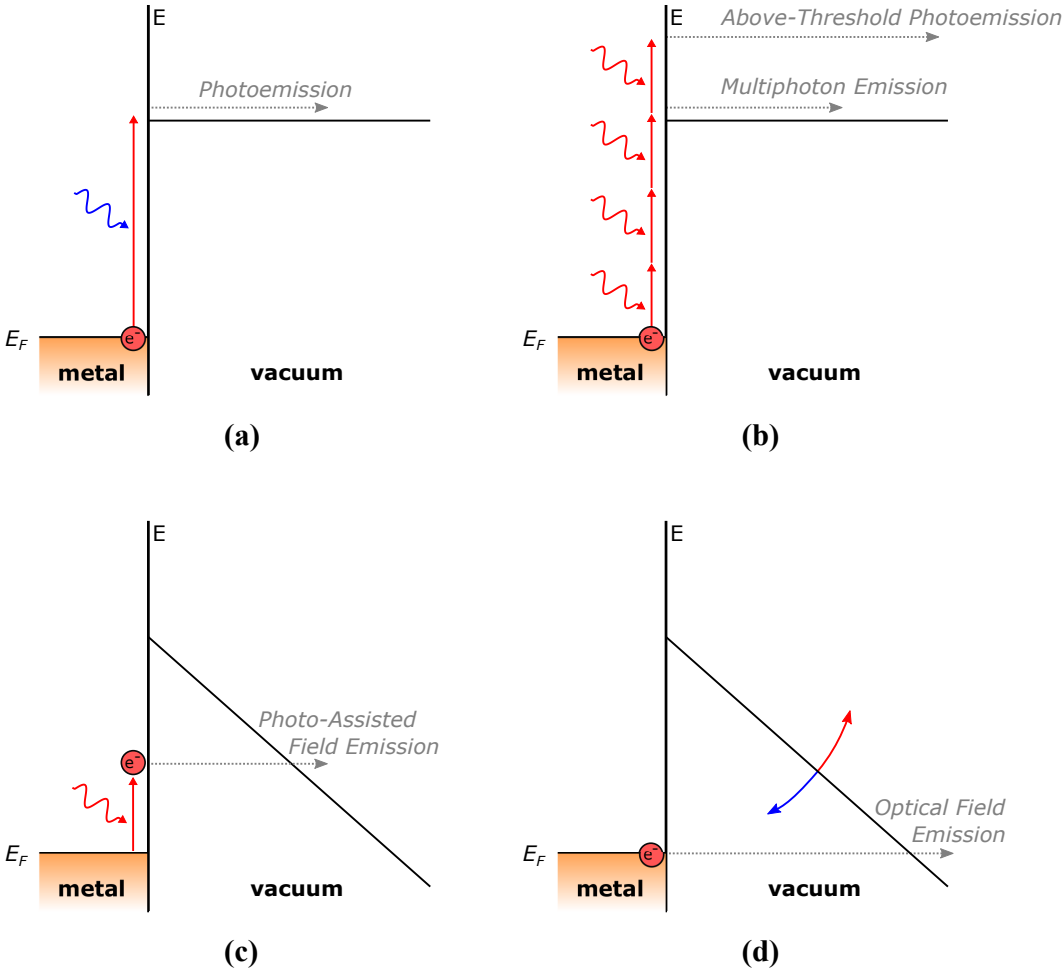

Figure 2.5: Electron emission processes from metal to vacuum under optical illumination: (a) single photon photoemission (photoelectric effect), (b) multi-photon emission and above-threshold photoemission, (c) photo-assisted field emission, and (d) optical field emission.

be described using Eq. (2.43) with an effective work function $\phi_{eff} = \phi - Nh\nu$. This process is called photo-assisted field emission and is illustrated in Fig. 2.5 (c).

Furthermore, there is another way in which an electron can interact with an optical field. If the laser intensity is sufficiently high, the local electric field associated with the optical field modulates the potential barrier such that during part of the optical cycle, the barrier becomes narrow enough to allow an electron from the Fermi level to tunnel through it [51–53]. This process is known as optical field emission and is displayed in Fig. 2.5 (d). The emitted current density can also be expressed using Eq. (2.43), where the total field is now given by the sum of the DC and AC electric fields: $F \rightarrow F + F_{laser}$.

To distinguish between emission regimes, L. Keldysh proposed a dimensionless adiabaticity parameter γ_k given by the ratio of the optical driving frequency ω to the tunneling frequency ω_t [54]

$$\gamma_k = \frac{\omega}{\omega_t}. \tag{2.61}$$

The tunneling frequency can be determined by the mean free time of the electron traversing a barrier of width $l = \phi/eF_{laser}$ with an average electron velocity proportional to $(\phi/m)^{1/2}$, thus allowing γ_k to be expressed as

$$\gamma_k = \frac{\omega\sqrt{2m\phi}}{eF_{laser}}. \tag{2.62}$$

In addition, γ_k can be written in terms of the ponderomotive energy of electrons U_p, i.e., the cycle-averaged kinetic energy of a free electron in an alternating electric field

$$\gamma_k = \sqrt{\frac{\phi}{2U_p}} \tag{2.63}$$

with $U_p = \frac{e^2F_{laser}^2}{4m\omega^2}$. Therefore, for relatively weak fields, the field decay length is larger than the quiver amplitude, yielding $\gamma_k \gg 1$ [55]. In this regime, electron emission is governed by photoemission processes. In the strong field regime, the ponderomotive energy becomes comparable to the electron binding energy, and $\gamma_k < 1$. In this limit, the electron tunneling adiabatically follows the instantaneous optical field, and the dominant process is optical field emission [56].

2.4 Bulk Conduction in Dielectrics

The conduction mechanisms studied so far have focused on the metal-vacuum interface. However, practical electronic devices are fabricated on top of a substrate, which is generally chosen to be an insulator. When high temperatures or high electric fields are applied, electron transport through the supporting insulator can occur. One of the most common bulk-limited conduction mechanisms in dielectric films is Frenkel-Poole (FP) emission [57]. In this emission mechanism, electron transport is assisted by traps from stored charges or structural defects. In terms of trap topology, the trap sites are positively charged when empty and uncharged

when filled so that the electron interaction with the positively charged trap leads to a Coulombic potential barrier as shown in Fig. 2.6 [58].

If the trap sites are sufficiently close together, the wave function of the electrons can overlap so that the charge carriers can "jump" between trapping centers. In a system of trapping centers at equilibrium, the emission and capture processes are balanced so that there is a constant density of localized electrons. Assuming thermally activated emission and using the principle of detailed equilibrium, the emission rate from the localized levels within the band gap e_T is related to the ionization energy E_i by an Arrhenius-type relationship [59]

$$e_T = AT^2 \exp\left(-\frac{E_i}{k_B T}\right) \tag{2.64}$$

where A is a constant.

When an external potential $+Fx$ across the insulator is applied, the Coulombic potential energy of an electron in a trapping center is reduced. Thus, the potential energy of the electron is given by

$$U(r) = -\frac{e^2}{4\pi\epsilon_r\epsilon_0 r} - eFx \tag{2.65}$$

where ϵ_r is the effective dielectric constant of the insulator [60]. Notice that the external electric field distorts the electrostatic interaction potential between the

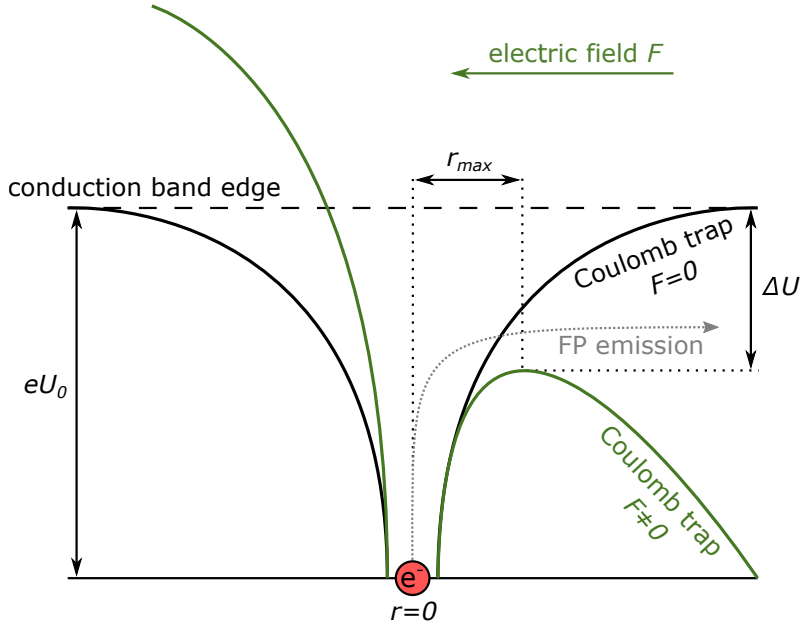

Figure 2.6: Schematic of FP emission: Coulombic trap potential at equilibrium (grey) and under an external field (green).

electron and trap center, such that the barrier is lowered in the direction of the applied field, as illustrated in Fig. 2.6. Consequently, the amount of energy required by an electron to escape the trap is reduced. This field-assisted thermal ionization of trapped electrons into the conduction band is known as FP emission [61, 62].

In the absence of the externally applied electric field, the potential barrier has a maximum value of $U_{\text{max,F=0}} = 0$ at an infinite distance from the trap. In the presence of the applied field, the maximum value of the potential barrier $U_{\text{max,F}\neq 0}$ occurs at a distance

$$r_{\text{max}} = \sqrt{\frac{e}{4\pi\epsilon_r\epsilon_0 F}} \tag{2.66}$$

and the potential barrier is reduced by an amount ΔU given by

$$\begin{aligned}\Delta U &= U_{\text{max,F}\neq 0} - U_{\text{max,F=0}} \\ &= -eFr_{\text{max}} \\ &= -\left(\frac{e^3}{\pi\epsilon_r\epsilon_0}\right)^{1/2}\sqrt{F}.\end{aligned} \tag{2.67}$$

The ionization energy becomes field-dependent so that

$$E_i(F) = E_i(0) - \left(\frac{e^3F}{\pi\epsilon_r\epsilon_0}\right)^{1/2} \tag{2.68}$$

where $E_i(0) = E_T$ is the binding energy of the electron on the trap when $F = 0$. As a consequence, the emission rate given in (2.64) becomes

$$e_T(F) = e_T(0)\exp\left(\frac{\Delta U}{k_BT}\right). \tag{2.69}$$

As the emission rate is proportional to the electrical conductivity, by making use of a modified form of Ohm's law, the FP current density is proportional to

$$J_{FP} \propto F\exp\left[\frac{-e\left(U_0 - \sqrt{eF/\pi\epsilon_r\epsilon_0}\right)}{k_BT}\right] \tag{2.70}$$

where eU_0 $(= E_i(0))$ is the ionization potential at zero field. Because FP emission is caused by thermal activation when an external field is applied, this conduction mechanism is often found at both high fields and high temperatures. In a similar

fashion to FN emission, the FP effect can be identified by the so-called FP plot where $\ln(J_{FP}/E)$ versus $E^{1/2}$ is plotted and a straight line indicates FP emission.

In addition, two other bulk-limited conduction mechanisms in dielectrics include hopping conduction and Ohmic conduction. In hopping conduction, trapped electrons "hop" between trap sites by tunneling through them. In this way, unlike in FP emission where electrons in trap sites acquire sufficient thermal energy to overcome the potential barrier, in hopping conduction the electrons tunnel through trap sites since they lack the necessary energy to surpass the trap barrier. Mathematically, the expression for hopping conduction is

$$J_{hop} = ena\nu_T \exp\left(\frac{eaF}{k_B T} - \frac{E_a}{k_B T}\right) \tag{2.71}$$

where n is the electron concentration in the conduction band of the dielectric, a is the mean spacing between trap sites, ν_T is the frequency of thermal vibration of electrons at trap sites, and E_a is the activation energy of traps.

Lastly, in Ohmic conduction, a small number of electrons from the valence band of the dielectric or some impurity level become thermally activated and are excited to the conduction band. The current density is linearly proportional to the applied electric field and the relationship is defined as

$$J_{ohmic} = en\mu F \tag{2.72}$$

where μ is the electron mobility. Since the band gap is large for a considerable intrinsic conductivity, the contribution from this conduction mechanism is very small and mainly detected at small fields [63].

2.5 Space Charge Effects

As described above, there are multiple ways in which the emission current from a cathode can increase, such as higher emitter temperature, larger applied electric fields, and radiation. However, as this current increases, the emitted electrons form a cloud of negative charge in the vicinity of the cathode, which in turn limits the electric field at the emitting surface. This is known as the space charge effect [30, 64]. Note that space charge is not an emission mechanism but rather a current limitation mechanism.

The effects of space charge on thermionic emission were first recognized by C. Child and I. Langmuir [65, 66]. They solved the one-dimensional Poisson's equation for a planar diode geometry subject to a zero electric field on the cathode surface boundary condition, and (neglecting the effect of initial velocities of the electrons) obtained the following relation for the maximum steady-state current density:

$$J_{CL} = \frac{4\sqrt{2}}{9}\epsilon_0\sqrt{\frac{e}{m}}\frac{V^{3/2}}{d^2} \tag{2.73}$$

where d is the diode gap separation. This equation is known as the Child-Langmuir law.

For field emission, the boundary condition of zero cathode field is not valid. A detailed mathematical treatment on space charge effects in field emission can be found in [67, 68]. It has been shown that, when the applied field is large compared with the value required for significant field emission, the emission current density approaches the Child-Langmuir law. In terms of the FN plot, the effects of space charge can be seen as the characteristic straight line turning over at high fields. However, in real-life emitters, the space charge limited regime is hard to attain because Joule heating and electromigration in the emitter would ultimately lead to device self-destruction.

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Chapter 3

FIELD EMISSION DEVICES FOR HIGH-TEMPERATURE OPERATION

Semiconductor devices face several challenges in harsh conditions including extreme temperatures and radiation environments. To circumvent these adversities, currently a considerable amount of electronic components are located remotely or cooled to below 125 °C. However, if high-temperature or radiation-proof electronics would be employed, costs and weight would substantially decrease, and apparatus reliability and performance would improve.

Continuous proper operation in hostile surroundings is crucial for various applications in the automotive, nuclear, down-hole, and aerospace industries. Historically, the main driving force in the development of high-temperature electronics has been the down-hole oil and gas industry, which can encounter temperatures of around 300 °C. Geothermal drilling operations can experience temperatures of 500 °C and even higher for deeper wells. Well-logging requires refined data acquisition instruments to obtain information about the surrounding geologic formations as well as sophisticated sensors to monitor various parameters such as temperature, pressure, and vibrations, all of which must be able to withstand the high surrounding temperatures. In the automotive industry, in particular with drive-by-wire technology, sensors and actuators are required close to the engine, exhaust, and brakes, where temperatures can range between 200 °C to 850 °C. Similarly, sensors and instrumentation are used in jet engines for monitoring and control, which can face temperatures over 300 °C. Other aircraft parts that could benefit from robust electronics placed in their vicinity include braking systems and landing gear, as well as densely packed high-power electronics that release a lot of waste heat. Nowadays, the avionics and aerospace industry has become a fairly substantial market for high-temperature electronics [1–3].

Space exploration is another field that would benefit from more resilient electronics. In particular, extended missions to Venus are incredibly challenging, which explains why it remains almost completely unexplored. The record for the longest-lasting lander on its surface has been set at 127 minutes by the Soviet Venera 13 in 1982. Even though pressure vessels and cooling systems were used, Venus' ambient condi-

tions were too harsh for the electronics to properly function. The daily temperature approaches 500 °C and it has a corrosive 92 atm caustic atmosphere. Its very thick atmosphere is mainly composed of supercritical CO_2 and N_2, and it also supports greenhouse warming as it contains sufficient SO_2 to form sulfuric acid clouds. Despite its very different climate, Venus is commonly referred to as the Earth's twin due to its similar density, distance to the Sun, and size. Therefore, a long-term mission to Venus to deeper study its geology and greenhouse effect atmosphere would provide a better understanding of the Earth [4, 5].

Furthermore, electronics that can operate in very cold temperatures would also be valuable. Examples of extremely cold environments in space include the moon's permanently shadowed regions with a temperature of -230 °C, Neptune's moon Triton at -250 °C due to its extreme distance from the Sun, and comet nuclei that can reach temperatures of -270 °C.

Unlike carrier transport in semiconductors, field emission is essentially independent of temperature and resistant to radiation. Therefore, devices based on this emission process could prove to be a good candidate to develop robust electronics for harsh environments. In terms of high-temperature environments, since elevated temperatures promote the desorption of surface contaminants, field emission devices should even have more stable electrical performance in these environments than at room temperature.

In this chapter, suspended in-plane two- and four-terminal field emission devices for high-temperature operation are demonstrated. Tungsten, a refractory metal, is the chosen electrode material due to its theoretical low work function ($\sim$ 4.5 eV) and high-temperature tolerance. A brief description of early proposals is also included. Finally, a discussion, as well as directions for future research, is provided.

Parts of this chapter were adapted from [6].

3.1 General Design Paradigm

While the conventional design of field emission devices relies on vertical Spindt emitters, wherein electron emission is out-of-plane, a lateral geometry was chosen instead for the devices discussed in this chapter. This design allows for taking advantage of high-resolution lithography, which simplifies the fabrication process and provides greater control over the main physical dimensions, namely the separation between the electrodes and the cathode geometry. Consequently, lower turn-on voltages can be achieved, thus decreasing power consumption and potentially increasing

device lifetime by reducing the harmful impact of ion sputtering. Furthermore, lateral devices are more practical and easier to integrate with widespread CMOS technology.

Tungsten was selected as the electrode material because it has a relatively low work function ($\sim$ 4.5 eV [7]) and the highest melting point of all metals (3,422 °C). These two properties are critical for developing devices with high current density emission for high-temperature operation. It also has high electrical and thermal conductivity. Other common alternatives for field emission devices include Si and carbon nanotubes (CNTs). Si is an attractive material due to its ease of fabrication and advanced micro processing technology. However, emission from Si is inferior due to its higher work function ($\sim$ 4.85 eV), and poor mechanical and thermal properties. Additionally, impurity adsorption from residual gaseous molecules can affect emission stability, so UHV environments are generally required [8–11]. CNTs are becoming increasingly popular due to their high mechanical, thermal, and chemical stability. Their high aspect ratio yields large local electric field enhancement, which, combined with their intrinsically low work function of $\sim$ 4.5 eV, provides high field emission currents at moderately low applied biases. Nonetheless, CNTs have several drawbacks. The presence of metallic and carbonaceous impurities, which occur regardless of the synthesis method employed, can have unfavourable effects on their thermal, electric, and mechanical properties. Specific and reproducible geometries are required to fabricate field emission devices; yet, achieving uniform chirality and precise sizes within a batch of CNTs as well as their controlled placement can prove to be challenging. Poor interfacial interaction with metals can result in high contact resistance and lower electron emission currents than predicted. Furthermore, temperatures over 500 °C are necessary to grow CNTs, which hinders the use of polymer substrates [12, 13].

Two types of devices were made: two (diode-like) and four (triode-like) terminal devices. A schematic of both devices is shown in Fig. 3.1. In both cases, one of the terminals, the so-called 'emitter,' is sharpened so that it has a larger field enhancement factor γ compared to the other terminals and thus, emits at a smaller applied bias [14]. The effect of various radii of curvature on the emitter tip can be seen in Fig. 3.2, which was simulated using COMSOL Multiphysics 5.4. The blunt electrode located in line with the emitter is referred to as the 'collector.' In the two-terminal device, we intended that this asymmetric geometry created by the sharp emitter and the blunt collector would mimic the IV curves characteristic of diodes. The other

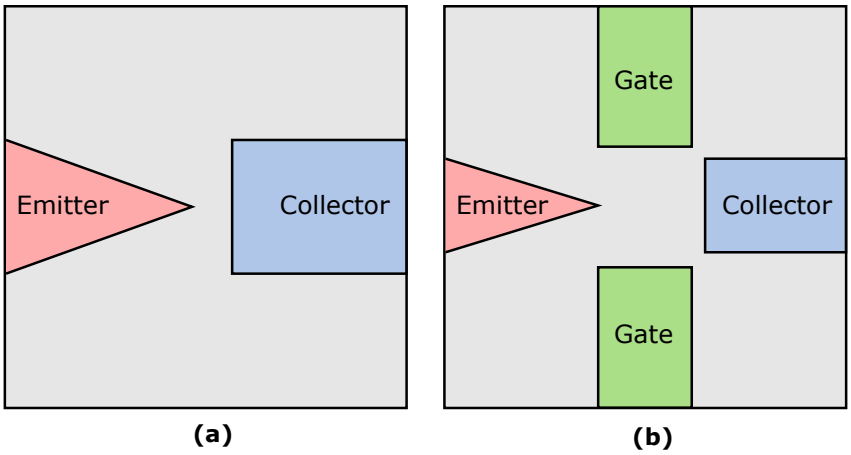


Figure 3.1: Top-view of schematic for two types of proposed devices: (a) two-terminal diode-like device and (b) four-terminal triode-like device.

two blunt electrodes of the four terminal device were oriented perpendicularly to the emitter and collector. These are referred to as 'gate' electrodes. The gates act by modulating the electric field at the tip of the emitter, which affects the tunneling probability [15]. Fig. 3.3 shows a two-dimensional finite element method (FEM) simulation (COMSOL Multiphysics 5.4) of the electric field norm and streamlines of a schematic for a gated device at two different gate biases. The collector was grounded while the emitter was biased negatively to induce electron emission. In (a), the gates were biased negatively, which ultimately steered the electrons toward the collector terminal, while in (b) they were grounded, which caused no emission toward the collector. Furthermore, ideally the non-axial component of the electric field between the emitter and collector cancels out, which minimizes the leakage of field-emitted current into the gates. Yet, asymmetries inevitably arise during the fabrication process. To account for this unevenness, the gates were electrically separated and their biases were independently controlled. In the four-terminal device, we concentrated on maximizing the field enhancement factor to reduce the leakage of field-emitted current from either the on-axis collector or the off-axis gates.

Yet, even though field enhancement was maximized for the emitter tip, the main focus was to fabricate the smallest gap between the emitter and collector. This would yield less resistive heating, which increases the lifetime of the device. A low operating voltage can also be achieved with small gaps.

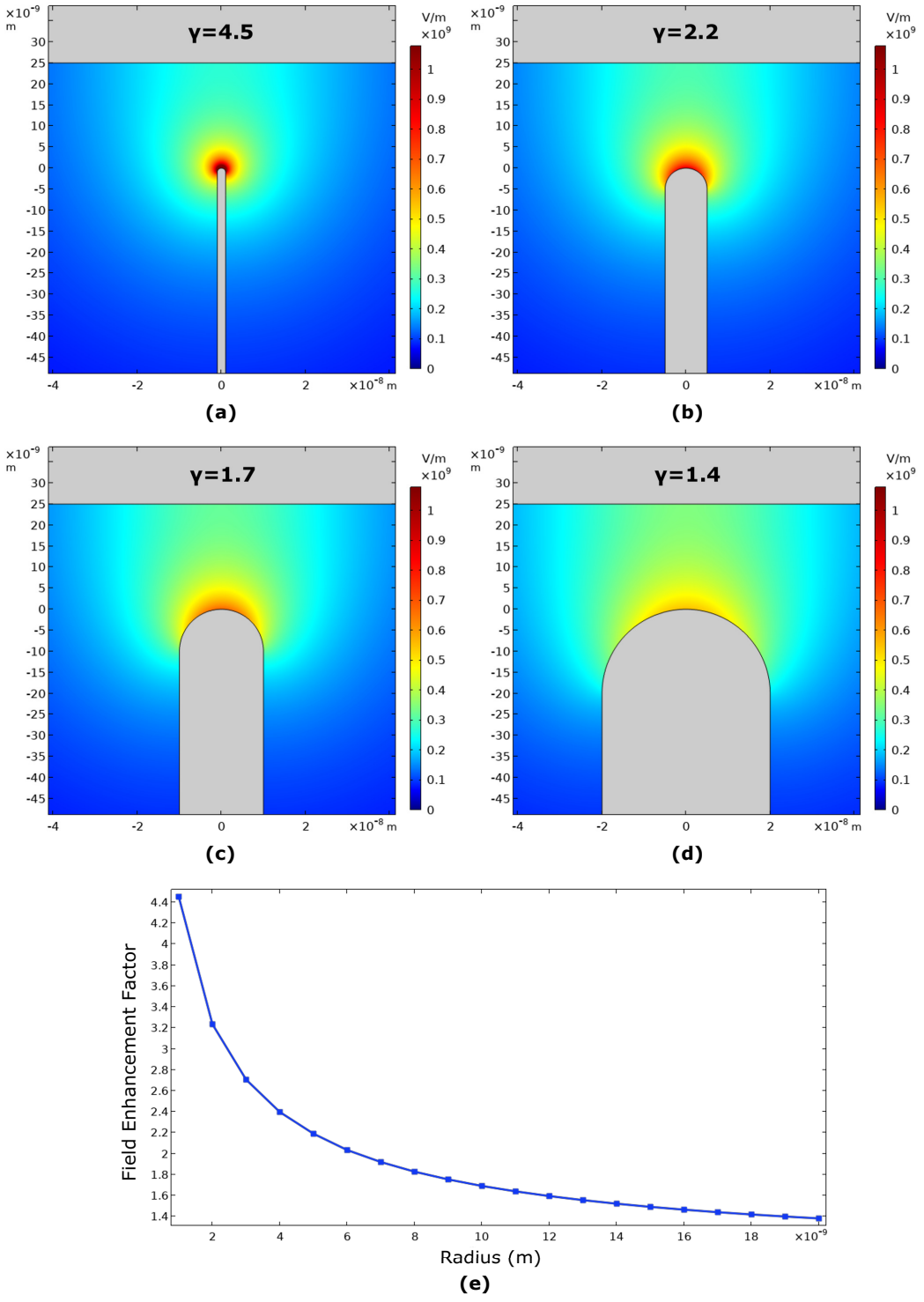


Figure 3.2: Electric field norm and calculated field enhancement factor for various emitter radius of curvature: (a) 1 nm, (b) 5 nm, (c) 10 nm, and (d) 20 nm. Field enhancement factor as a function of emitter radius of curvature.

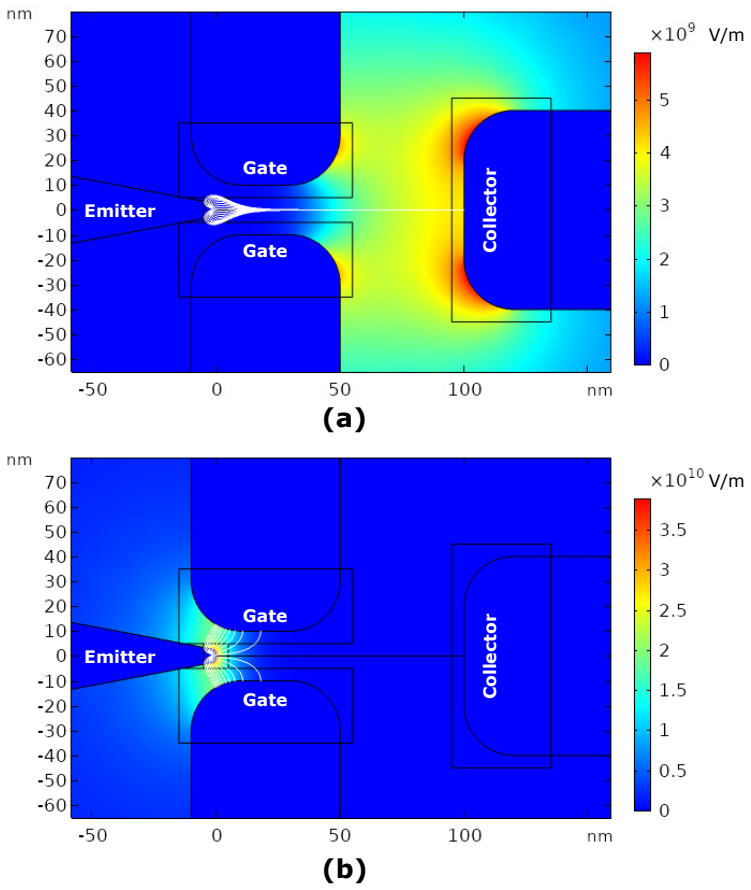


Figure 3.3: Simulated electric field norm with streamlines (white lines) for a general four-terminal device. The collector was grounded while the emitter was biased negatively to induce electron emission. In (a) the gates were biased negatively, and in (b) they were grounded.

3.2 Early Work on PECVD SiN_x Substrate

The first device fabricated was a lateral metallic four-terminal triode-like field emission device. Plasma-enhanced chemical vapour deposition (PECVD) silicon nitride (SiN_x) was selected as the supporting dielectric material due to its high dielectric breakdown and fast deposition rate. However, the combination of the large electric field required for field emission with a high-temperature environment in an insulator can be detrimental to device operation, as it leads to undesirable FP current leakage [16, 17]. This is the field-assisted thermal ionization effect by which an insulator becomes electrically conductive before reaching dielectric breakdown [18, 19]. One approach to reducing the effect of this parasitic leakage pathway that competes with FN field emission is to distance the insulator from the emission area [20]. Thus, to avoid the increased surface leakage currents across dielectric layers that come

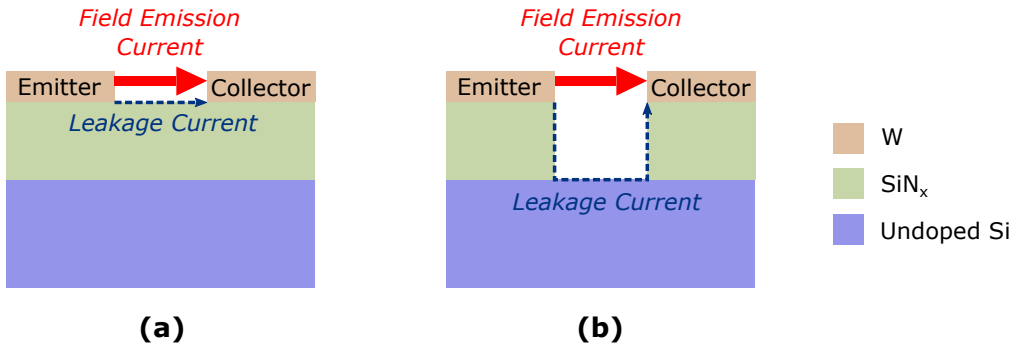


Figure 3.4: Emission and leakage current pathways for: (a) unetched substrate, (b) deeply etched substrate.

along higher temperatures, deep nanoscale anisotropic dry etching was employed. Long etched paths decrease the parasitic leakage pathways that compete with FN emission, as shown in Fig. 3.4.

The fabrication steps are summarized in Fig. 3.5. The devices were fabricated on an undoped Si wafer (resistivity of 10 Ω·m) to minimize leakages across the substrate. A layer of 500 nm amorphous SiN_x was deposited by PECVD (Oxford Instruments Plasmalab System 100) using silane and ammonia gas chemistry at 350 °C and 1 Torr. The resistivity of this SiN_x layer was measured to be 229 Ω·m. Following the dielectric deposition, a layer of 200 nm of tungsten (W) was sputtered in a custom-made deposition chamber at 7 mTorr in an argon atmosphere with the RF power set to 200 Watts. The resistivity of the sputtered W was measured to be 6.83×10^{-7}Ω·m. The sample was cleaned using a hydrogen plasma at 50 Watts and 30 mTorr (Plasma-Therm SLR 720) to remove oxides that may have formed on the surface of tungsten during processing [21, 22]. Standard EBL using poly(methyl methacrylate) (PMMA)–a positive-tone e-beam resist–was employed to pattern the devices. 950 PMMA A2 (MicroChem) was spin-coated on the substrate immediately after the H_2 plasma at 1500 rpm for 40 s and subsequently baked at 180 °C for 4 minutes, which yielded a thickness of approximately 100 nm. The devices were written using direct-write EBL (Raith EBPG 5200) at an acceleration voltage of 100 keV, followed by development in a freshly made 1:3 solution of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) at room temperature. A layer of 35 nm chrome (Cr) was e-beam evaporated (CHA Industries Mark 40) at a rate of 0.5 Å/s and lifted-off in hot PG-remover to be used as an etching hard mask. The devices were dry etched using a mixture of SF_6 and C_4F_8 at a ratio of 26 sccm/35 sccm with a chamber pressure of 10 mTorr and a capacitively coupled

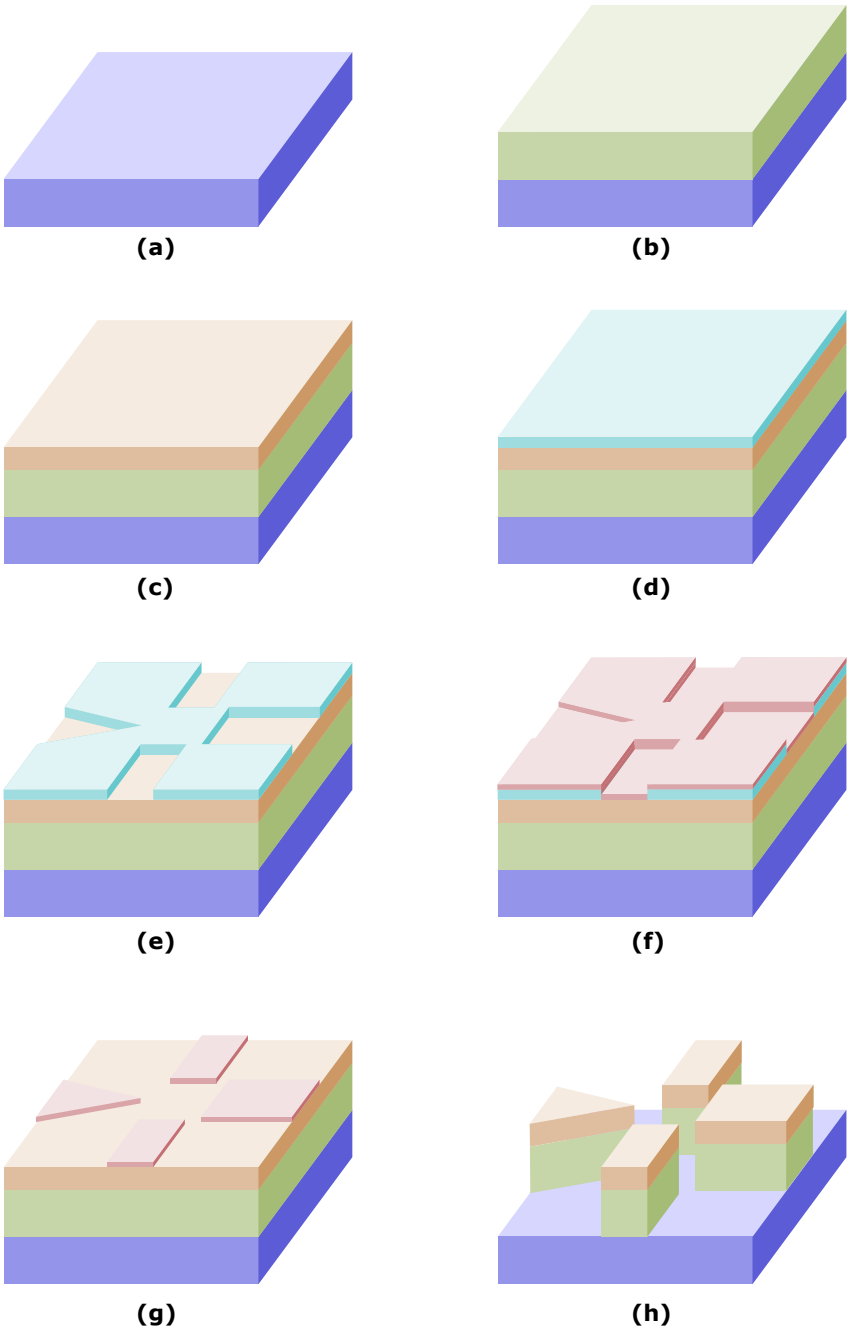
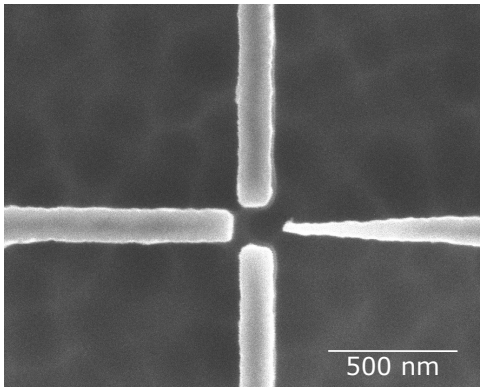


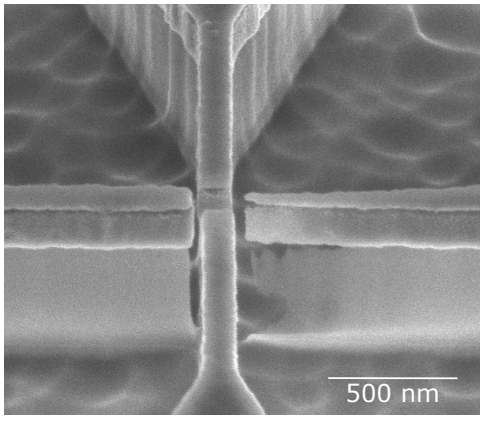
Figure 3.5: Fabrication steps: (a) initial undoped Si substrate, (b) deposition of 500 nm PECVD SiN_x layer, (c) sputtering of 200 nm W, (d) spin-coating of 100 nm 950 PMMA A2 e-beam resist, (e) EBL and development, (f) evaporation of 35 nm Cr hard-mask, (g) lift-off, and (h) dry etching in pseudo Bosch process. Note that the sketch is not to scale.

plasma (CCP) power of 50 Watts and an inductively coupled plasma (ICP) power of 1500 Watts (Oxford Instruments Plasmalab System 100 ICP-RIE 380). The 200

nm thick W electrodes, the 500 nm SiN_x layer, as well as 500 nm of the Si substrate were etched to increase the length of the leakage pathway. To wire-bond, contact



(a)



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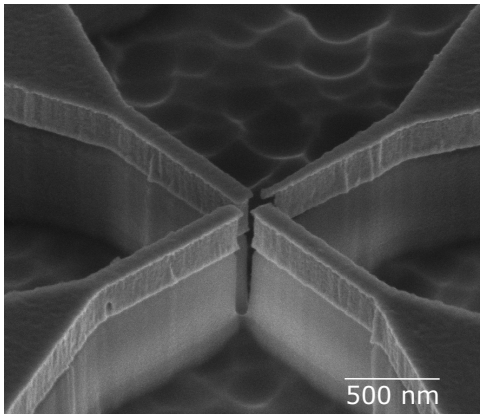


(c)

Figure 3.6: SEM of fabricated W triode-like device on SiN_x: (a) top-view (b) 52° tilt, (c) 52° tilt and rotation.

pads were photolithographically defined. AZ9245 (MicroChem) was spin-coated on the sample at 2000 rpm for 30 seconds, followed by a 2-minute 110 °C soft bake. Exposure for 30 seconds at a wavelength of 405 nm and a dose of 25 mW/cm^2 was done using a contact mask aligner (Suss MicroTec MA6), and the sample was developed in a 1:3 mixture of AZ400K and water for 2 minutes. Any leftover Cr was removed using Cr-7S (Cyantek) to improve the adhesion and contact conductivity. An adhesion layer of 7 nm titanium (Ti) (rate of 0.5 Å/s) and 200 nm gold (Au) (rate of 1 Å/s) were evaporated (CHA Industries Mark 40), followed by lift-off in hot PG-remover. Fig. 3.6 shows a scanning electron micrograph (SEM) of a representative fabricated device.

The device was ultrasonically wedge wire-bonded with aluminum wires to a ceramic pin grid array package (Spectrum Semiconductor Materials CPG15504). The chip carrier was then placed over a ceramic heater (ThorLabs HT24S2), and a thermocouple was attached to the back of the chip carrier. To reduce sample contamination that could alter the work function and affect electron emission and stability, the setup was loaded into a custom stainless-steel vacuum chamber, which was pumped to $\sim 10^{-6}$ Torr. The four terminals on the device were connected to separate sourcemeters (Keithley 2450) to independently control the bias and measure the current at each terminal. The measurement acquisition was automated using serial communication and MATLAB scripts.

Several IV scans per device were done to remove further adsorbates from the emitting surfaces. This ‘conditioning’ [23] process was repeated until the emission characteristics appeared to be stable. For all measurement runs, the collector bias was kept at 0 V while the emitter voltage was negatively swept to promote electron emission. An initial current limit of 100 nA was imposed to prevent excessive resistive heating and potential tip destruction. Fig. 3.7 shows the IV curve of the triode-like device for several gate biases tested at room temperature. Three independent measurements for each voltage setting were taken, and the average values along with error bars are depicted in the plots. The emitter-to-collector distance for the specific device tested measured 212 nm. The measured currents for all four terminals of the device are displayed to accurately monitor any leakage. Owing to the field enhancement factor of the sharp emitter tip, the operating voltage was under 10 V, which is comparable to CMOS technology. In 3.7 (a), both gates were kept at 0 V. With this bias configuration, most of the emitted current was directed to both gates and only a small fraction went to the collector. This was

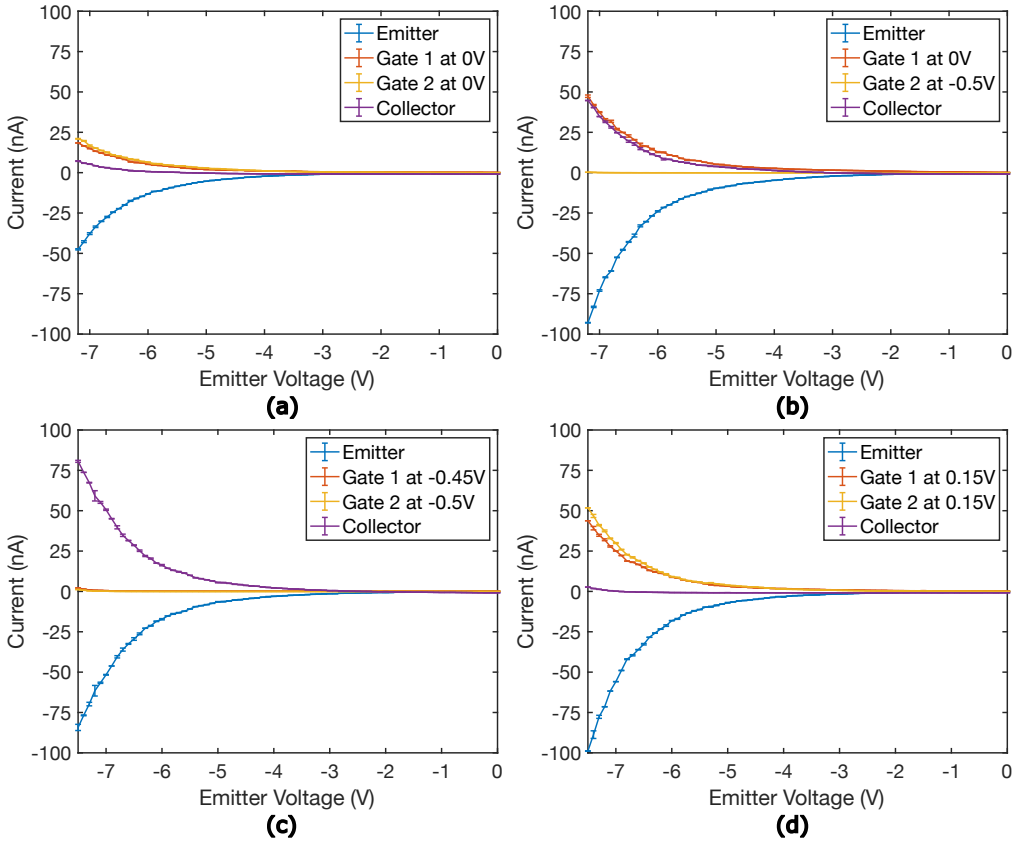


Figure 3.7: IV characteristic for triode-like device on SiN_x for various gate bias: (a) both gates were grounded, (b) one gate we negatively biased to repel electrons, (c) both gates were biased to steer electrons exclusively towards the collector, (d) both gates were biased to prevent electron emission to the collector. In all cases, the collector was kept grounded and the measurements were taken at room temperature.

expected, as the gates were located closer to the emitter compared to the collector, and all three terminals were grounded. In (b), the bias on one of the gate terminals was changed to -0.5 V to reflect electrons that would otherwise be emitted to it. This was successful, as more electrons were directed toward the collector terminal. Several combinations for gate bias were tested to steer all electron emission exclusively toward the collector terminal to attain an 'on' state. This was achieved at -0.45 V for one gate and -0.5 V for the other, as depicted in (c). Lastly, in (d), the gate bias was chosen to achieve an 'off' state, wherein no current would be directed towards the collector. These measurements successfully showed that the gates did modulate the electric field at the emitter tip, confirming that the emission mechanism was FN emission.

Next, emission at various temperatures was studied. Fig. 3.8 (a) shows the IV characteristic for the same device at temperatures ranging from 33 °C to 125 °C. As adsorbates can alter the work function of the emitter tip and, consequently, affect electron emission, the temperature was initially raised to the maximum testing

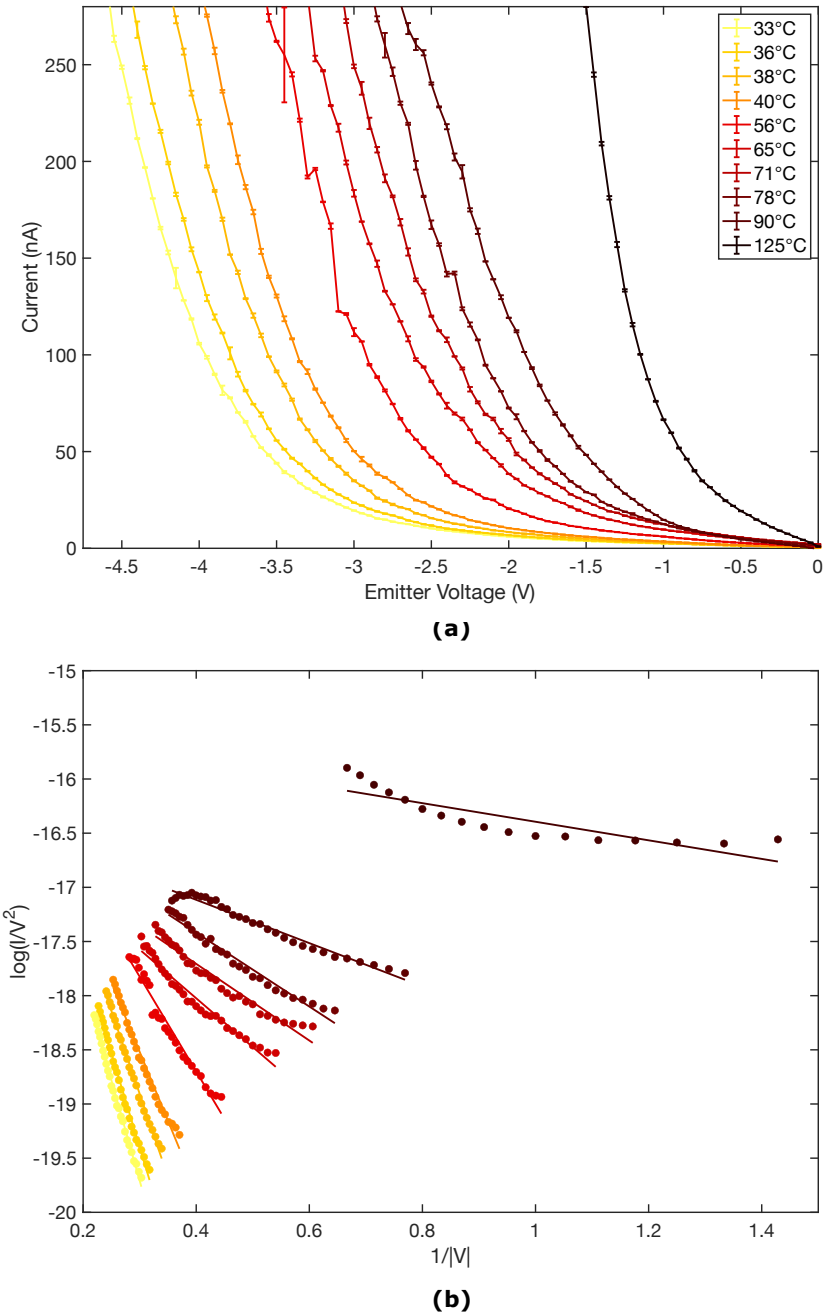


Figure 3.8: Effect of temperature on electron emission: (a) IV characteristic, and (b) FN plot.

Temperature (°C)	**Parallel Leakage Resistance (MΩ)**	**Slope**	***y*-intercept**	**R^2 value**
33	394	-18.53	-14.15	0.994
36	333	-17.33	-14.20	0.993
38	271	-15.33	-14.31	0.994
40	217	-12.72	-14.71	0.984
56	116	-8.75	-15.20	0.971
65	63	-4.50	-16.22	0.963
71	45	-3.54	-16.29	0.959
78	34	-3.41	-16.06	0.974
90	19	-2.00	-16.32	0.973
125	5	-0.86	-15.54	0.744

Table 3.1: Device data as a function of temperature.

value of 125 °C. At this temperature, the first IV characteristics was measured. Subsequently, the temperature was slowly lowered, and the rest of the measurements followed in order of decreasing temperature. A low-field linear leakage current was observed that increased with increasing temperature. The values from this parasitic series resistance as a function of temperature were extracted by performing a linear fit from the small field data and are presented in Table 3.1. A decrease of almost two orders of magnitude for the resistance was seen between the data measured at both extremes of the measured temperature range, which indicated that the substrate was not suitable for high temperatures. Fig. 3.8 (b) depicts the data in FN coordinates for currents above 30 nA. This value was chosen to remove the effects of the small field leakage current. Additionally, least squares regression lines were fitted to the resulting data. The corresponding coefficients of determination are included in Table 3.1, as well as the extracted values for the slope and y-intercept. The experimental data exhibited linear behaviour in accordance with the FN emission mechanism up to 90 °C. This provided further proof that the substrate was not adequate for high-temperature applications. Moreover, as illustrated in Table 3.1, the magnitude for the extracted slope decreased as a function of temperature while the magnitude for the extracted y-intercept increased. These two parameters are related to physical parameters, namely γ and φ. Their relations are given by Eq. (2.49) and Eq. (2.50). Therefore, it seemed that either γ was increasing, φ was decreasing, or a combination of both. This is further addressed in Section 3.4.

3.3 Suspended Devices: Design and Fabrication

After the work on deep anisotropic etch on SiN_x, the next attempt to increase the resistance of the leakage current pathways that became notably troublesome at high temperatures was to fabricate suspended devices. This design would eliminate the current leakage pathway in the vertical direction.

The devices were fabricated on a suspended, stoichiometric silicon nitride (Si_3N_4) membrane with planar dimensions of 5 mm × 5 mm, and a thickness of 200 nm (Norcada QX10500DS). The membrane was laterally supported by a 200 μm thick Si frame. The main fabrication steps are sketched in Fig. 3.9. Standard EBL was used to pattern connected terminals, interconnect lines, alignment marks, and contact pads. The membrane was stuck face-up on a piece of blue low tack tape (commonly used with the scriber-breaker) so that it could be spin-coated. 950 PMMA A8 (MicroChem) was spun at 4000 rpm for 1 minute. This yielded a thickness of approximately 1 μm. A layer of a conductive polymer, namely AquaSAVE (Mitsubishi Chemical Corporation), was spun at 1500 rpm for another minute to avoid charging effects during EBL. The blue tape was removed before baking the membrane at 180 °C for 5 minutes. The devices were written using direct-write EBL (Raith EBPG 5200) at an acceleration voltage of 100 keV, a beam current of 100 nA, and a dose of 1500 μC/cm^2. The contact pads were written on the supporting Si frame. An SEM showing the resulting connected terminals for a two-electrode device is shown in Fig. 3.10. After lithography, the layer of AquaSAVE was removed in water, and the resist was developed in 1:3 solution of MIBK and IPA at room temperature. Oxygen treatment was used for descum in a plasma cleaner in remote mode (PIE Scientific Tergeo Plus).

Next, a conducting layer consisting of 150 nm of W with a 7 nm Ti adhesion layer was sputtered. Due to the high tensile stress of the membranes (1.0 GPa as stated by the manufacturer), various attempts to sputter W at low pressure failed as the deposited layer would quickly peel off. The sputter conditions had to be optimized to reduce the stress of the deposited layer [24, 25]. A quick method to determine if the deposited layer has too much residual stress is to first sputter on a test sample that has been spin-coated with a layer of photoresist. Due to the softness of the resist layer, cracks appear if the deposited W layer has residual tensile stress while buckling delamination would occur if the sputtered layer has residual compressive stress. Fig. 3.11 shows photos of the test samples at various sputtering conditions. Silicon chips coated with a uniform layer of photoresist were used as

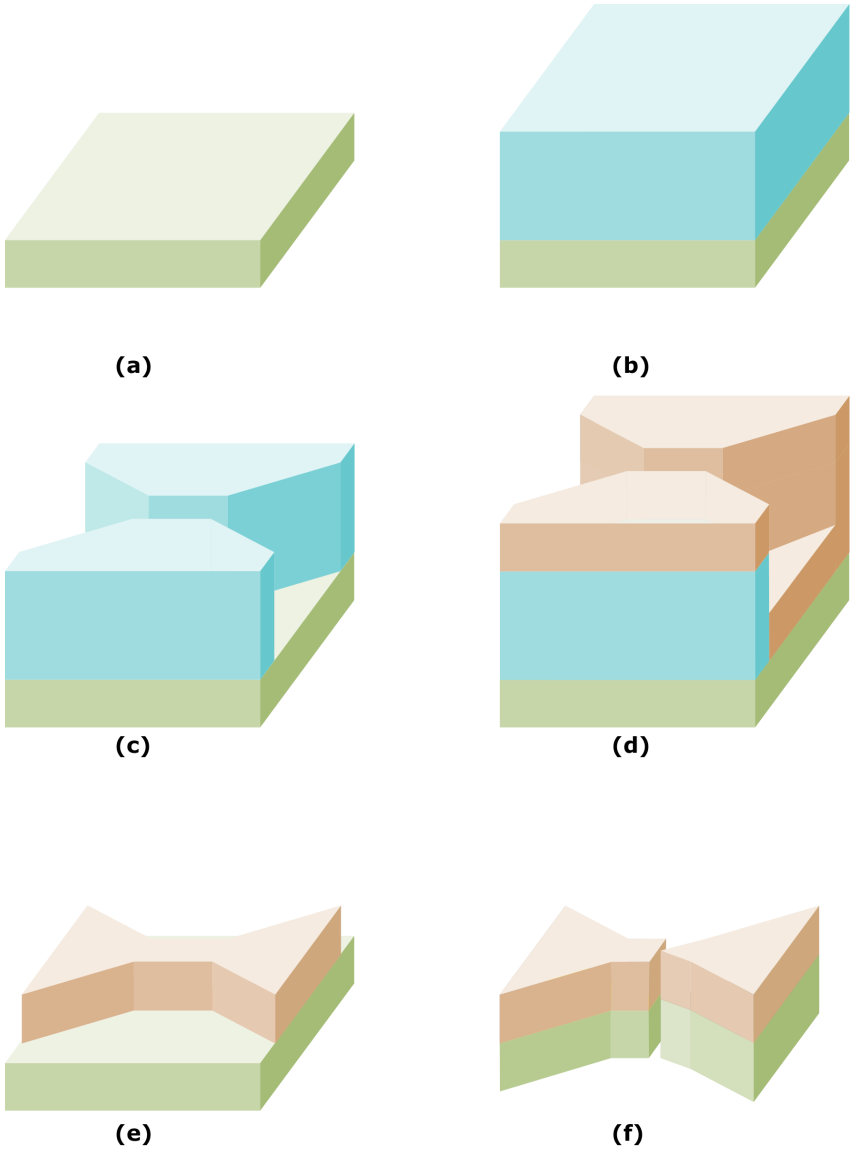


Figure 3.9: Fabrication steps for diode-like device: (a) initial Si_3N_4 membrane, (b) spin-coating of 1 µm 950 PMMA A8 electron beam resist, (c) EBL and development, (d) sputtering of 150 nm of W, (e) lift-off, (f) Ne focused ion beam milling. Note that the sketch is not to scale.

test substrates. The deposition was carried out in a UHV magnetron sputtering system (AJA) with argon as the sputtering gas. The optimal sputtering condition was found at an RF power of 300 Watts and a sputtering pressure of 40 mTorr. A high power was desired to increase the deposition rate. While higher sputtering pressures were also tested, the minimum pressure at which we observed no stress was chosen as the resistivity of the deposited W increased with higher sputtering pressures. The resistivity of the deposited W layer at the optimal conditions was

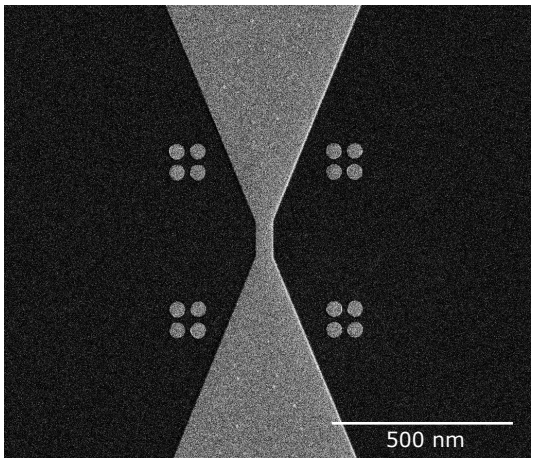
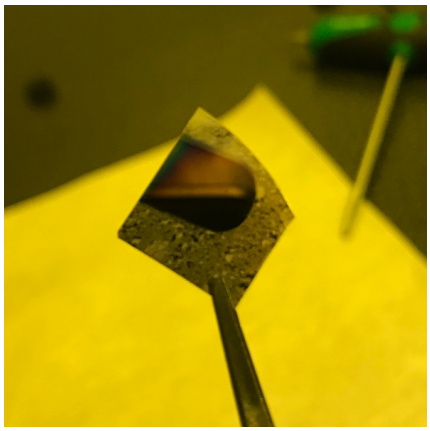


Figure 3.10: SEM of the two-terminal device after first lithography step. At this point, the two terminals were connected.

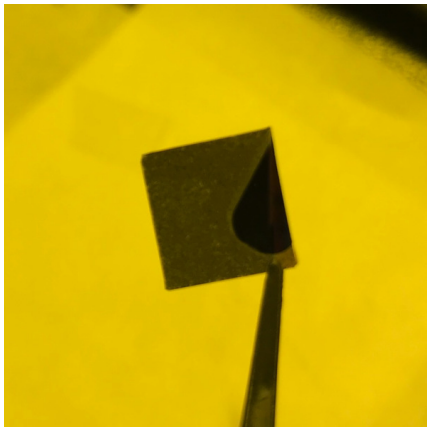
$1.1\times10^{-5}\Omega\cdot$m. Unfortunately, this was two orders of magnitude more resistive than the W deposited in the custom vacuum chamber at lower power and pressure for the device on PEVCD SiN_x substrate.

Once the electrode material layer had been deposited, lift-off was performed in acetone. Aligned EBL was employed to redefine the electrical contact pads with the same recipe as previously. A layer of 150 nm gold with a 10 nm Ti adhesion layer was deposited using electron beam evaporation at a pressure of $\sim 10^{-7}$ Torr (Kurt J. Lesker Labline). This thicker contact layer enabled ultrasonic wire-bonding to connect the devices without punching through the silicon nitride layer to the partially-conductive silicon frame.

The connected terminals were separated manually using neon focused ion beam (FIB) patterning (Zeiss Orion NanoFab). This enabled the creation of two-terminal diode-like (Fig. 3.12 (a)) and four-terminal triode-like lateral devices (Fig. 3.12 (b)). The circles in Fig. 3.10 were used as focusing marks to align the column. Neon was chosen instead of gallium FIB due to better milling precision and to avoid undesired Ga implantation and contamination. As previously described in Section 3.1, the emitter terminal was sharpened to obtain a higher field enhancement factor compared to the other terminals. This resulted in a macroscopic tip diameter of approximately 10 nm in (a) and around 40 nm in (b). Before ion milling, the membrane was coated with a $\sim$ 10 nm conductive carbon layer for charge dissipation using a carbon evaporator (Leica EM ACE600). To prevent crack propagation and relieve stress, two stop holes on the off-axis plane of the terminals were milled before



(a)



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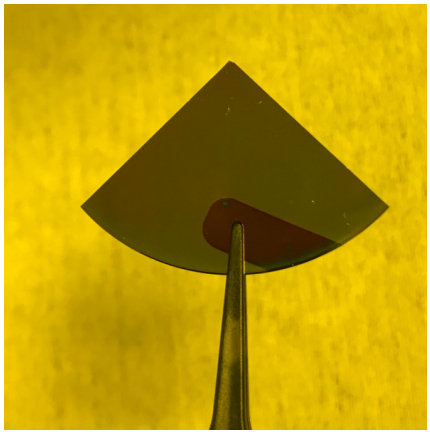
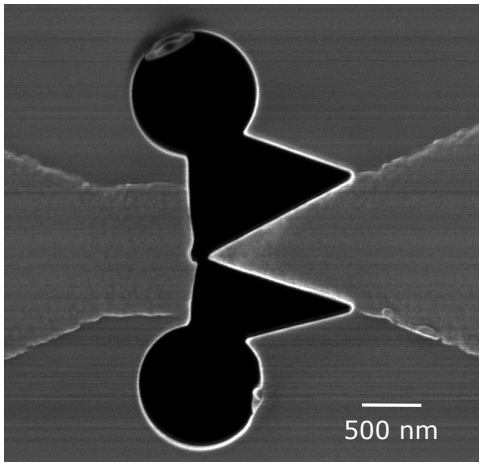
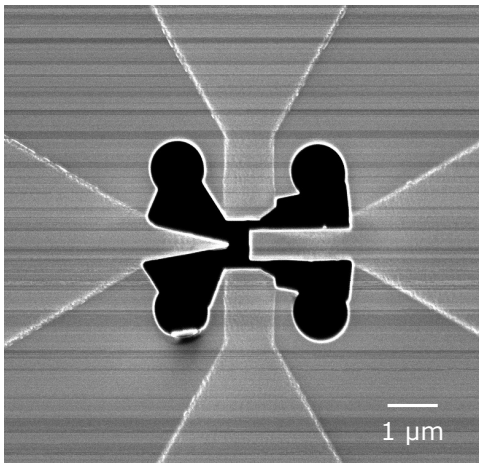


(c)

Figure 3.11: Various sputtering conditions on test samples: (a) RF power: 100 Watts; pressure: 2 mTorr, (b) RF power: 250 Watts; pressure: 3 mTorr, (c) RF power: 300 Watts; pressure: 40 mTorr.



(a)



(b)

Figure 3.12: Ion micrograph of suspended (a) two-terminal diode-like device and (b) four-terminal triode-like device. In (a), the emitter-collector gap measured 95 nm, and in (b) the emitter-collector gap measured 367 nm.

the terminals were separated. This eliminated the possibility of sharp corners that could serve as nucleation sites for cracks in the Si_3N_4 [26]. The FIB patterning was also used to remove the silicon nitride membrane near the terminals, thus minimizing potential leakage pathways across the insulating substrate. The milling current was 14 pA, the acceleration voltage was 20 keV, the pressure was 4×10^{-6} Torr, and the working distance was 8 mm. For the annuli used to mill the stop holes and the polylines used to remove the rest of the big features, a dose ranging between 4-25 nC/μm^2 was used, while for the thin lines used to define the gap separating the emitter from the collector a dose of 1 nC/μm^2 was employed.

Temperature (°C)	Parallel Leakage Resistance (MΩ)
80	16200
158	357
204	44

Table 3.2: Measured resistance values of membrane and ceramic pin grid array package at low fields as a function of temperature.

Finally, the membrane was subjected to an oxygen plasma at 80 Watts and 20 mTorr using reactive-ion etching (RIE) (Plasma-Therm SLR 720) to remove the conductive carbon layer. To prevent heating of the membrane, the cleaning was divided into four intervals of 5 minutes each with a 1-minute pause in between.

3.4 Suspended Devices: Results and Discussion

The membrane was ultrasonically wedge wire-bonded with aluminium wires to the ceramic pin grid array package previously used (Spectrum Semiconductor Materials CPG15504). The parallel resistance at low voltages as a function of temperature was measured to determine whether the membrane and chip carrier would be suitable. A hot plate with a T-type thermocouple were used to set the desired temperature. The results are given in Table 3.2. Additionally, the pin connected to the membrane that sourced the current was disconnected and connected to a randomly chosen pin on the chip carrier at 204 °C, and the resistance was measured to be 120 MΩ. This indicated that the chip carrier was leaking at modest temperatures, so a substitute was needed.

Next, a custom-made, high-temperature chip was fabricated. Macor, a glass-mica ceramic sheet, was chosen as the material since it can sustain temperatures up to 1,470 °C, is easy to machine, and is electrically insulating. The membrane was ultrasonically wedge wire-bonded with aluminium wires to conductive strips on a one-inch square Macor plate. The conductive strips were attached to the ceramic board using UHV and high-temperature conductive silver paste (Ted Pella Pelco 16047). The membrane and the substrate were placed on top of a vacuum-safe heater (HeatWave Labs) with a thermocouple attached to the surface of the ceramic substrate. The experimental setup was loaded in a stainless-steel vacuum system at the Jet Propulsion Laboratory (JPL). The membrane, ceramic substrate, and thermocouple were held via compression by temperature-resistant molybdenum

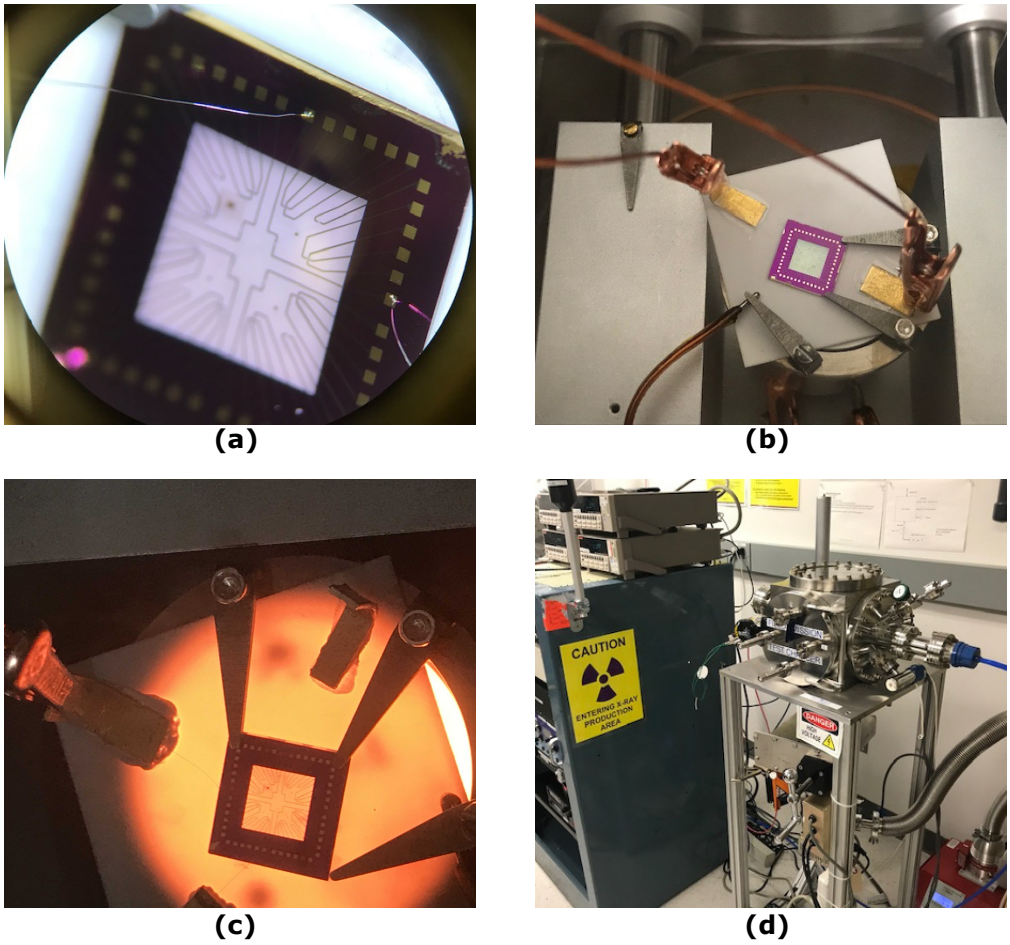


Figure 3.13: Photograph of (a) wire-bonded membrane, (b) membrane on ceramic substrate sitting on top of heater with the heater off, (c) membrane on ceramic substrate sitting on top of heater with the heater on, and (d) testing setup at JPL.

springs, as shown in Fig. 3.13. The strips on the ceramic substrate were connected to an electrical feedthrough of the vacuum chamber, and each terminal was linked to individual picoammeters/voltage sources (Keithley 6487). Additionally, 10 MΩ current-limiting resistors were placed in series with each terminal as ballast resistors to avoid thermal runaway and surge currents. The vacuum chamber was pumped to $\sim 10^{-7}$ Torr and baked at 150 °C for several hours before testing, which helped with the desorption of water vapour and other contaminants from the surface of the terminals.

Multiple IV scans per device with a forward and reverse sweep were initially conducted at 150 °C to remove adsorbates from the emitting surfaces until the turn-on voltage stabilized. The turn-on voltage was defined as the voltage that yields a current above the noise floor (approximately 5 nA). This threshold current was chosen

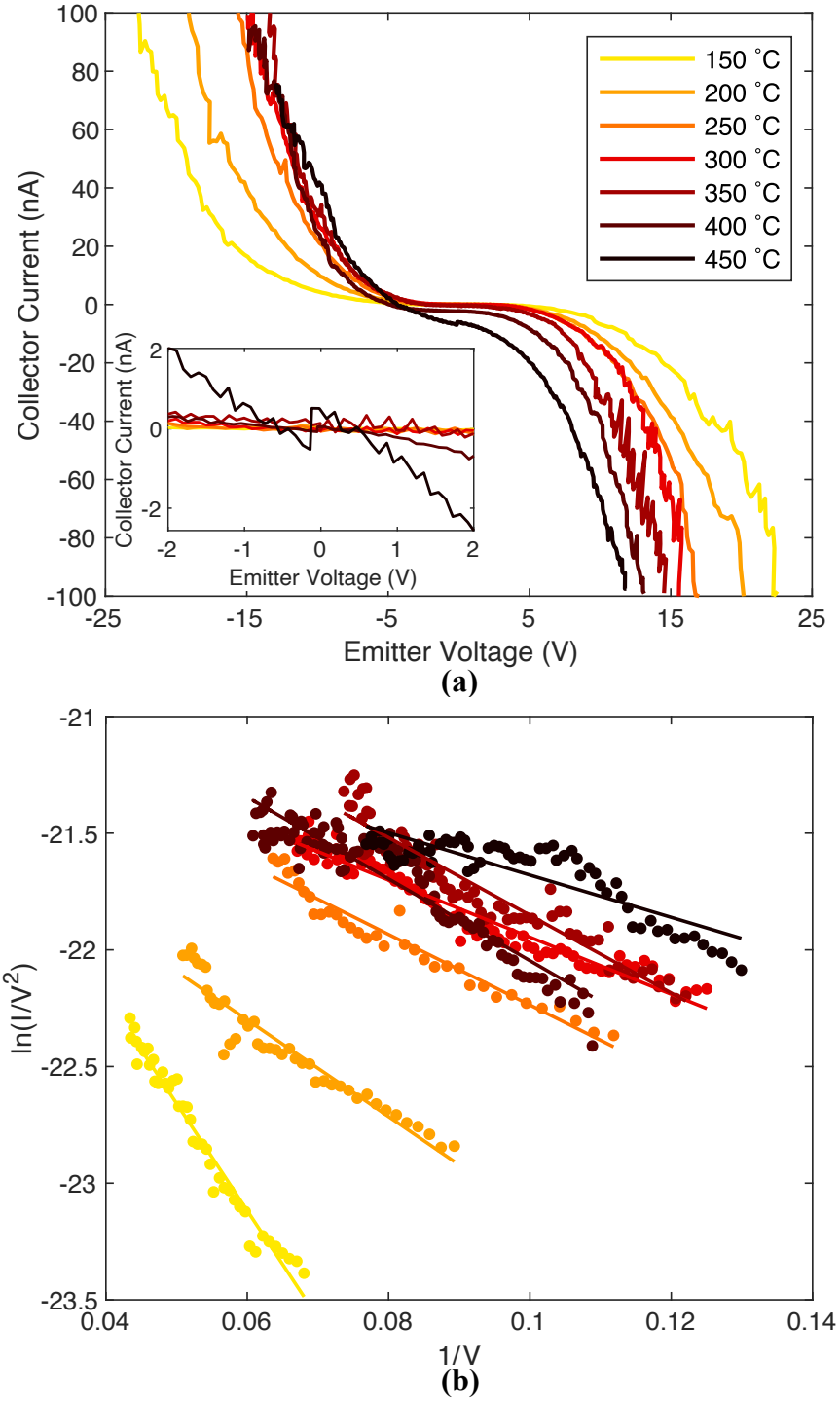


Figure 3.14: Electrical measurements for the tow-terminal device as a function of temperature: (a) IV characteristic removing the series resistance and (b) its FN plot for currents over 15 nA for temperatures between 150 °C to 450 °C. The lines correspond to the least-squares regression.

as 15 nA. Fig. 3.14 (a) shows the IV plot for the diode-like device shown in Fig. 3.12 (a) tested from 150 °C up to 450 °C in increments of 50 °C. The emitter-to-collector gap measured 95 nm. The emitter voltage V is calculated as $V = V_A - IR$, where V_A is the applied voltage on the emitter, I is the emission current, and R is the series resistance of the ballast resistors. A current limit of 100 nA was imposed to prevent excessive resistive heating and potential tip destruction.

The device displayed turn-on voltages of less than 13 V, which is desirable for atmospheric pressure operation [27]. As the energy of the electrons is not high enough to ionize the atoms present in the atmosphere, ion bombardment of the terminals can be diminished. Additionally, the turn-on voltage can be reduced further by decreasing the size of the emitter-to-collector gap [28].

Unfortunately, the emission from either terminal was symmetric. This could be explained by the fact that the collector terminal was not completely blunt but rather had an undesired sharp protrusion, which effectively yielded a γ comparable to the one at the emitter tip.

The inset of Fig. 3.14 (a) shows a magnified view of the zero-corrected IV curve for voltages near 0 V. It can be observed that before the onset of field emission, current increased linearly with increasing voltage. In a similar fashion to the devices described in Section 3.2, parasitic leakage dominated at these small fields. A linear fit of the small field data was performed and the values for the parasitic series resistance at the various temperatures were extracted and presented in Table **??**. This parasitic resistance decreased with increasing temperature. Since the substrate in the vicinity of the high fields was removed, the likely leakage pathway was via the supporting silicon ring, which had a resistivity of 1-30 Ω·cm at room temperature, as stated by the manufacturer.

Fig. 3.14 (b) shows the IV characteristic in FN coordinates for currents above 15 nA to focus exclusively on field emission current. The experimental data displayed linear behaviour up to 300 °C, in agreement with FN emission mechanism. At temperatures above 350 °C, the fit deteriorated and the measured current did not seem to follow a purely FN behavior. To confirm that the emission current was not thermionic, the current was plotted in RD coordinates ($\ln\left(I/T^2\right)$ versus $1/T$) [29] for various applied voltages on the emitter, as shown in Fig. 3.15. Since the resulting plot was clearly non-linear for all potentials shown, thermionic emission was ruled out. This could suggest thermally-promoted field emission. At higher temperatures, thermally excited electrons transmit through a thinner potential barrier as these

Temperature (°C)	Parallel Leakage Resistance (MΩ)	Slope	y-intercept	R^2 value
150	94.0	-45.95	-20.36	0.970
200	45.2	-20.73	-21.05	0.916
250	17.6	-15.12	-20.72	0.948
300	7.6	-12.22	-20.72	0.946
350	8.9	-16.64	-20.18	0.909
400	5.4	-17.52	-20.29	0.886
450	0.8	-9.05	-20.77	0.753

Table 3.3: Suspended two-terminal device data as a function of temperature.

electrons have the tail of the energy distribution above the Fermi energy. This contribution of thermal electrons and resultant deviation from merely FN emission is particularly noticeable for low currents [30], as for higher fields FN emission dominates [31]. Additionally, this enhanced tunneling probability may explain the lower turn-on voltages observed at higher temperatures, as for the same potential the emission current was larger [32, 33].

Table 3.3 shows the values for the slope and y-intercept of the least squares regression line, along with the value for the coefficient of determination for all measured temperatures. Based on the reported literature work function of tungsten ($\varphi = 4.5$

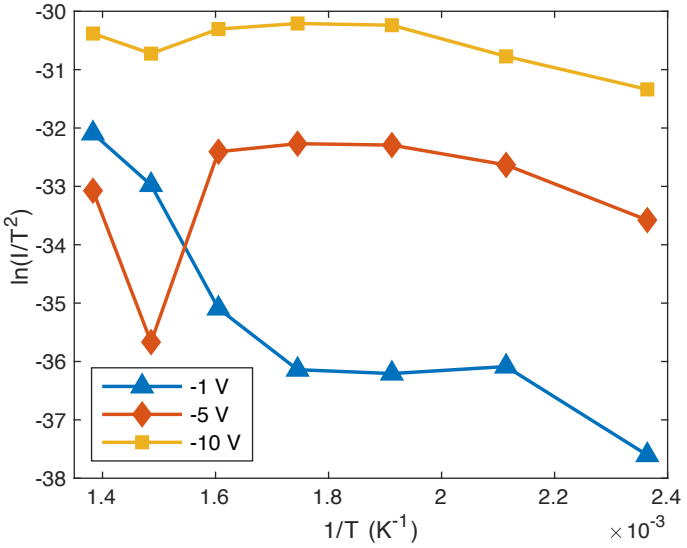


Figure 3.15: Emission current in RD coordinates for various applied voltages.

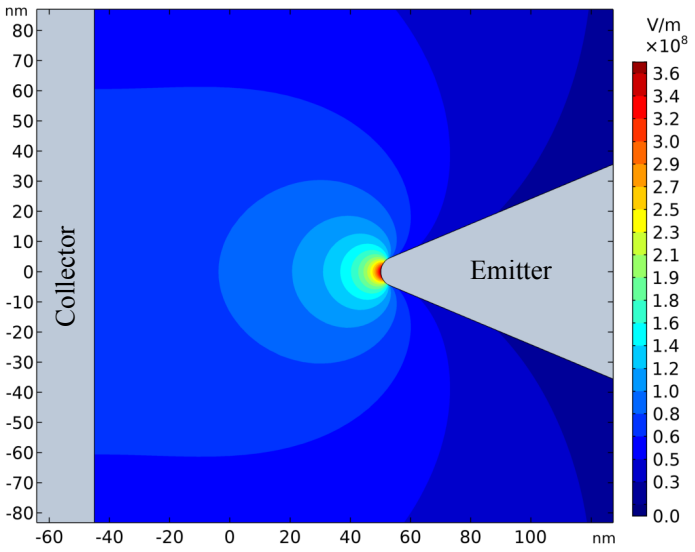


Figure 3.16: COMSOL simulation of the component of the electric field normal to the emitting surface in V/m for the diode-like device. The emitter was set to -10 V.

eV) and the slope of the FN plot, a value of 133 for the field enhancement factor γ was calculated at 150 °C. A two-dimensional FEM simulation (COMSOL Multiphysics 5.4) was performed based on the device dimension values extracted from the ion micrograph to numerically compute the normal component of the electric field at the emission tip, as illustrated in Fig. 3.16. The simulation suggested a more modest γ of 3.5, a value two orders of magnitude smaller than that obtained experimentally. This discrepancy could be due to uncertainty in the efficient emitter tip radius, as emission may be taking place locally at nanoprotusions, grain boundaries, or groups of atoms [34], which may not be accurately resolved via an ion micrograph.

Overall, the magnitude of the slope decreased as a function of temperature. As the slope depends on both γ and φ, it is possible that with increasing temperature either γ increased, φ decreased, or a combination of both. An increasing γ could be a consequence of temperature-dependent desorption of residual molecules that alter the surface roughness of the emitter tip [35]. Temperature-induced release of gaseous adsorbates may also explain the potential decrease in φ [36, 37]. Electronegative adsorbates in the emitter surface, such as oxygen, have been shown to increase the work function. In this way, traditional techniques to analyze FN plots are challenging to apply [38], as it is hard to remove all contaminants and produce an atomically clean surface. We should also consider the possibility that electromechanical motion due to the suspended nature of the devices as well as thermal expansion of the electrode materials could shrink the gap, which would impact the extracted parameters.

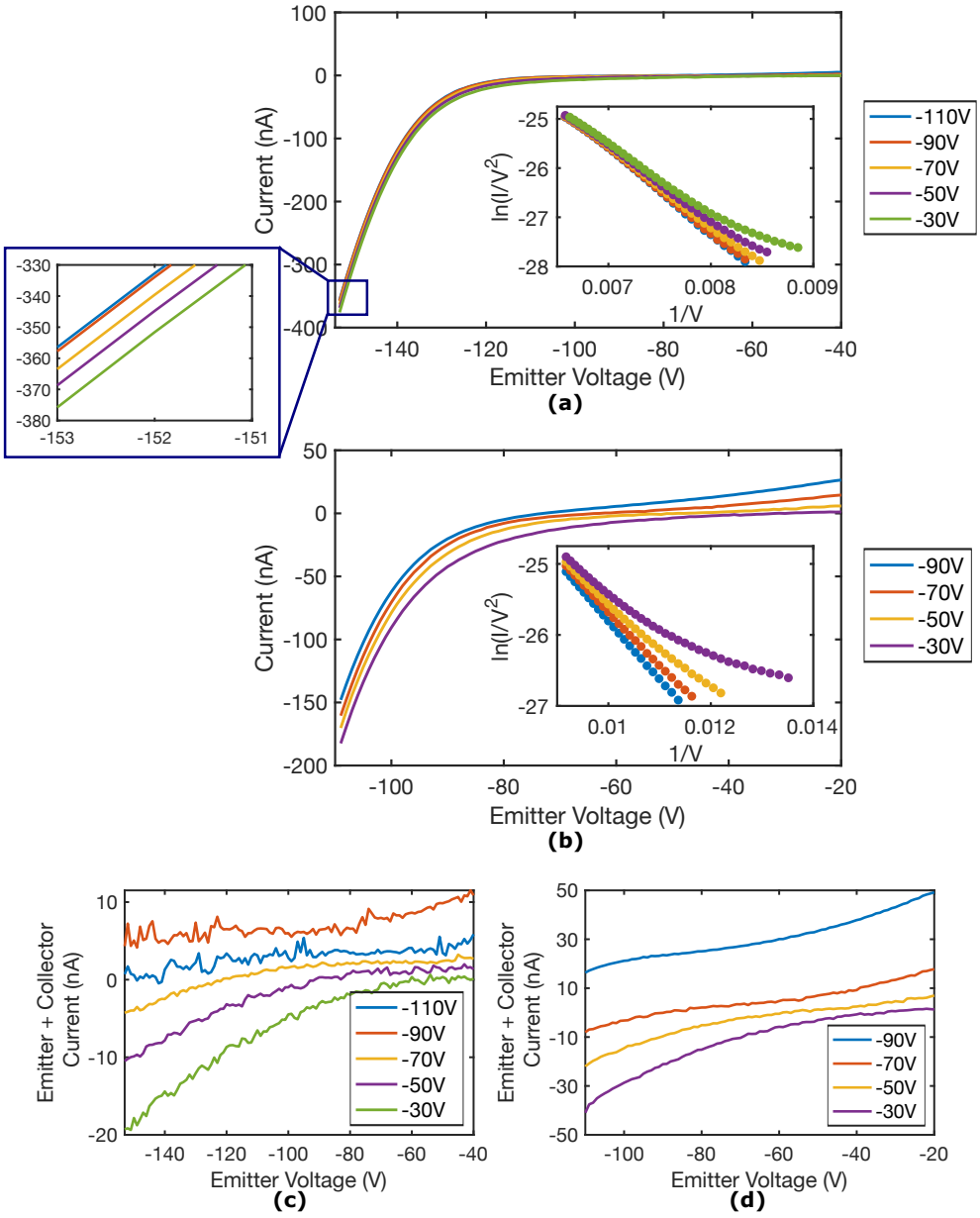


Figure 3.17: Electrical measurements for triode-like device: (a) IV characteristic at various gate bias at 150 °C and (b) for 300 °C, respectively. The insets present the data in FN coordinates for currents over 15 nA. (c) Summed emitter and collector currents to illustrate leakage to the gate terminal for 150 °C and (d) for 300 °C. All legends indicate the gate voltages.

Next, building upon our two-terminal device, we also fabricate in-plane four-terminal triode-like structures, as shown in Fig. 3.12 (b). The emitter-to-collector distance is 367 nm. In addition, the top gate is 442 nm away from the emitter tip, while the bottom gate is separated by 462 nm. Even though we attempted to achieve

symmetry in fabrication, we can overcome any disparity by independently biasing the terminals.

Fig. 3.17 shows the IV curve of the triode-like device for various gate biases tested at (a) 150 °C and (b) 300 °C. The current shown is the emitter current. In this way, we concentrated on FN currents between the emitter and collector and ignored leakage of field-emitted currents to the gates, which is addressed later. For both (a) and (b), the collector was kept at ground. Various combinations for gate bias were tested to minimize the preferential current leakage to an individual gate and achieve as close to a symmetric behavior as possible. Ultimately, this condition was achieved when the bias offset between them was set to +10 V for (a) and +50 V for (b), such that the top gate was at a more negative potential compared to the bottom gate. The gate voltage reported in the plot corresponds to the top gate bias. The runs were not performed in a monotonically decreasing gate bias sequence as the legend suggests but in a randomized sequence to rule out heating effects of the emitter tip as the justification for any observed gating. The device displayed turn-on voltages at around -120 V for (a) and -80 V for (b). Once again, we observed thermally-promoted field emission, as the turn-on voltage became smaller at higher temperatures. However, these devices displayed larger turn-on voltages compared to the two-terminal devices previously discussed due to the larger emitter-to-collector distance. The insets correspond to the data plotted in FN coordinates. The linearity of the plots for higher emitter voltages confirmed FN current as the emission mechanism. As the gate bias became more negative, the measured current was reduced for a given emitter potential. This illustrates the effect of gating at the emitter tip–as the potential difference between the emitter and gates decreases, the magnitude of the electric field at the emission tip is reduced, thus diminishing the emitted current.

Fig. 3.17 (c) and (d) show the addition of the emitter and collector currents (with signs) as a function of emitter bias for the various gate biases at 150 °C and 300 °C, respectively. The purpose of these graphs is to show the field-emitted current leakage from either the emitter to the top gate or from the top gate to the collector. We can ignore the leakage to the bottom gate, as it was measured for all emitter voltages to consistently be under 1 nA at 150 °C and under 7 nA at 300 °C (this value was measured when the leakage to the top gate was the largest). This may be due to the greater distance between the emitter tip and the bottom gate. A positive value in the plots corresponds to collector leakage, while a negative value corresponds to

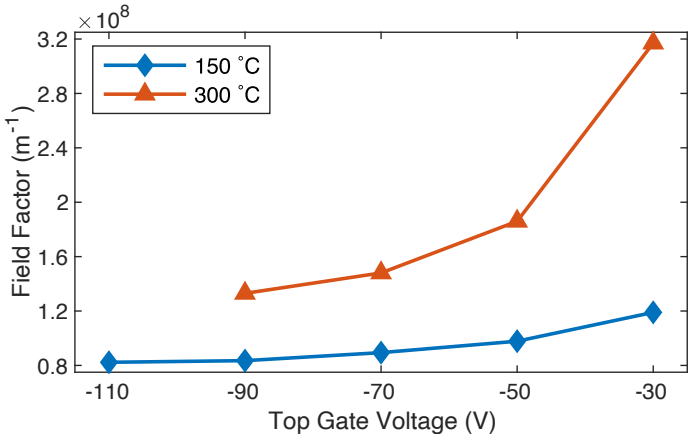


Figure 3.18: Calculated field factor for the four-terminal device as a function of top gate voltage at 150 °C and 300 °C.

emitter leakage. When the potential difference between the emitter and the gates was increased, current leaked from emitter to the gate. The leakage path then shifted, with most leakage occurring from gate to collector, when the potential difference between the emitter and gates was decreased. We tracked all currents to make sure that none were unaccounted for. To reduce the emitter-to-gate leakage, we should improve the symmetry of the gates so that no gate is favoured electrically. To prevent gate-to-collector leakage, we may consider fabricating the gates with a metal of a higher work function, which would hinder the onset of exponential emission.

We fitted a linear regression model to the data and extracted the vertical axis intercept and slope. We assumed $\varphi = 4.5$ eV and calculated β, as seen in Fig. 3.18. For both temperatures, an increase in the potential difference between the emitter and the gates led to a greater β. This agreed with the increase in current for a given emitter voltage when the gate voltage became more positive, which confirmed that the gate electric field modulated the emission current.

Next, we compared the measured data to a simulation of our device operation. We selected the lower temperature data with the smallest average leakage current to the gates (top gate at -70 V) and calculated an emission area A of 6.5 nm^2. Using COMSOL, we determined that an emitter tip radius of 0.25 nm was necessary to achieve the β previously calculated (Fig. 3.18) for the specific potential configuration. We then simulated the expected gating as shown in Fig. 3.19 (a) and (b). We calculated the expected DC transconductance g_m using

$$g_m = \frac{\Delta I}{\Delta V_g} \tag{3.1}$$

where V_g is the gate voltage. From the simulation at -153 V, the computed transconductance was 24.5 nS. From the data in Fig. 3.17 (a), we calculated an experimental transconductance of 0.3 nS at the same emitter potential. This value was 0.1 nS if we used the collector current. Similarly, the simulated g_m was 4.9 nS at -110 V, while the experimental at 300 °C for the same potential was 0.7 nS (and 0.6 nS if we had considered collector current). A potential reason for the discrepancy between the simulated and the experimental values is that the simulated transconductance did not take into account leakage to or from the gate, which was present in the experimental data. The simulated Maxwell's capacitance C was 7.059 $\times 10^{-17}$ F, and we calculated the experimental cut-off frequency f_c given by [39]

$$f_c = \frac{g_m}{2\pi C} \tag{3.2}$$

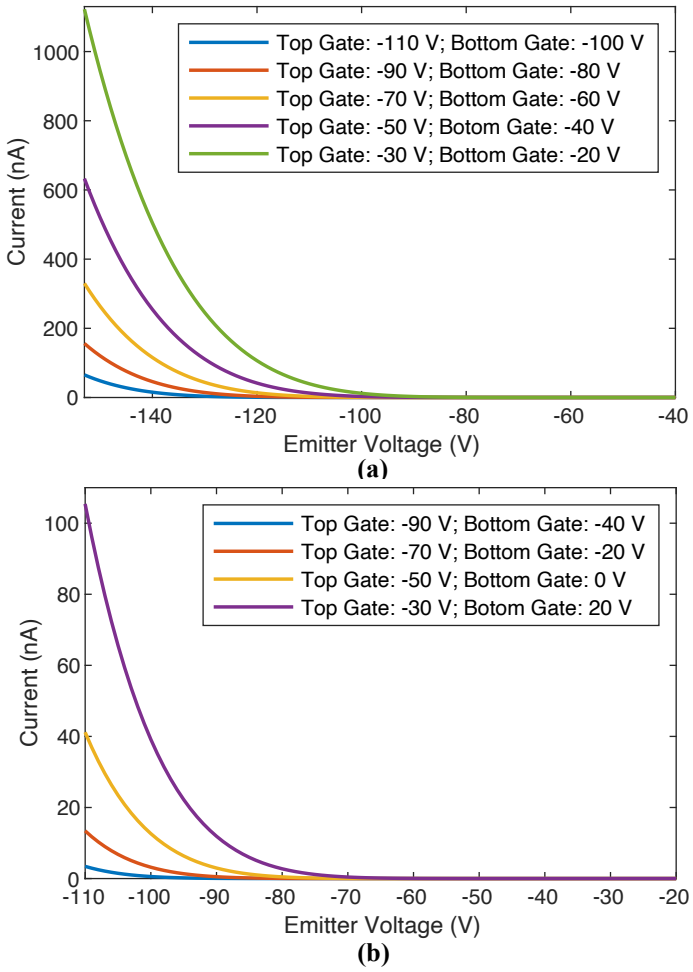


Figure 3.19: Simulated IV characteristics for the current device geometry for the various gate potential configurations experimentally tested at (a) 150 °C and at (b) 300 °C.

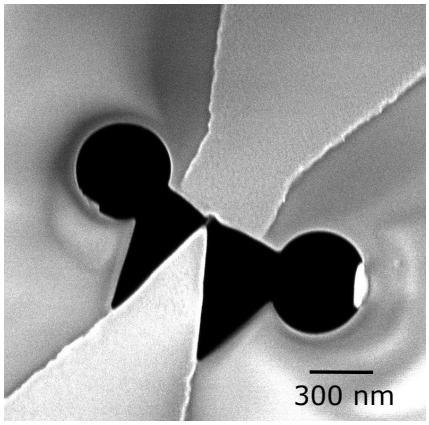
to be 0.676 MHz at 150 °C and 1.578 MHz at 300 °C. Using the simulated g_m, f_c for this geometry, values of 55.23 MHz and 11.05 MHz, respectively, could be achieved. This g_m is much lower than previously reported values for single-tip field emission transistors. For example, Han et al. [40] demonstrated a gate-insulated vacuum channel transistor with $g_m = 0.2$ μS. To increase f_c, we need to increase the transconductance. As the distance between the gates and the emitter affects the field between them, reducing this distance can enhance the control of the emitted current. For instance, if we move the gates away from the collector and closer to the emitter, such that the distance between the gates and the emitter is 100 nm, the simulated transconductance becomes 130 nS. However, this would unfortunately also increase the capacitance to 8.456 $\times 10^{-17}$ F. Additionally, since FN current increases exponentially, a larger emitter bias can also increase g_m. Lastly, g_m has been found to exponentially increase with the gate potential [41], although this may come at the cost of a higher leakage current.

Note that after all tests were completed on the membrane, there were no visible changes in morphology when inspected via scanning electron microscopy. Fig. 3.20 shows an SEM of the same devices portrayed in Fig. 3.12 after all measurements presented in this section were conducted.

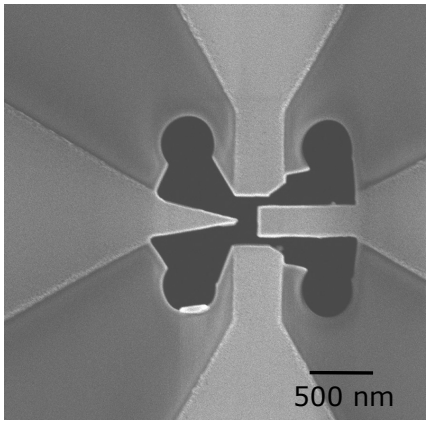
3.5 Challenges and Suggestions for Improvement

In this chapter, we have presented various two- and four-terminal devices based on field emission for high-temperature applications. All devices were made of tungsten due to its low work function and high-temperature tolerance. Initially, devices on PECVD SiN_x on undoped Si substrate were fabricated. Unfortunately, they were unsuccessful for operation at elevated temperatures due to the increase in substrate conductivity and current leakages, which altered the emission characteristic so it no longer resembled pure FN emission. The next set of devices was fabricated on stoichiometric Si_3N_4 membranes. To increase the resistance of the leakage pathway, the dielectric substrate in the vicinity of the emission site was removed. The emission characteristic at higher temperatures was improved compared to the first device up to temperatures around 300 °C. However, above that, the detrimental effects of high temperatures began to occur again.

Field emission devices should, in theory, be able to withstand high temperatures. However, several practical factors can make this difficult. One of these is the dependence of field emission on the work function. At higher temperatures, residual



(a)



(b)

Figure 3.20: SEM after testing for (a) diode-like and (b) triode-like devices.

gases that have chemisorbed or physisorbed onto the surface of the emitter can desorb, which changes the work function and affects the emission characteristics. Additionally, the adsorption and desorption of gases can randomly modulate field emission and cause burst noise in the emission current. Consequently, circuit design can become problematic as a fluctuating or noisy IV characteristic is not desirable. One possible solution is to heat the device under test to a high enough temperature to boil off contaminants, but this may lead to the redeposition of adsorbates if they are not pumped out quickly enough before the temperature is lowered. Encapsulating the devices during the fabrication process may be helpful [42]. Ideally, this should be done in the same deposition run as the electrode material deposition, so that the devices do not become contaminated after leaving the deposition vacuum chamber. However, this may be difficult to achieve because the pattern must first be transferred to the substrate, which requires the chip to be briefly at atmospheric

pressure. An alternative solution might be to perform the encapsulation at a later step in a deposition chamber that has substrate heating capability, which can remove contaminants before encapsulation.

Tungsten and other refractory metals are prone to surface oxidation [43, 44], which can be problematic. Tungsten trioxide (WO_3) is the most thermodynamically stable tungsten oxide, and its reported work function ranges between 4.7 and 6.4 eV [45]. The rate of oxidation increases with temperature, particularly above 300 °C. As a result, tungsten devices are typically used in vacuum environments or inert atmospheres. One potential solution is to use anti-oxidation coatings. Surface coatings made from silicon and boron have been suggested for this purpose [46–48].

Additionally, as temperature increases, diffusion effects arise, which is particularly problematic for vacuum field emission devices. Atoms on the surface of the emitter tip can move more easily due to thermal fluctuations because there are fewer bonds at the solid/vacuum interface compared to the bulk. This surface diffusion can change the morphology of the sharp emitter tip and affect the field enhancement factor, which in turn alters the emission characteristics. Electromigration, in which atom diffusion is caused by a high current density, is also a concern for field emission devices because of the high fields involved. The strong fields at the emitter tip can cause deformational sharpening, as well as nanoscale protuberances due to spontaneous surface migration. These changes in electrode surface geometry can increase Joule heating on the cathode due to heat localization. Field emission current density is also increased as a result of the increase in the local strength of the electric field. Ultimately, heating of the emitter tip by high field emission

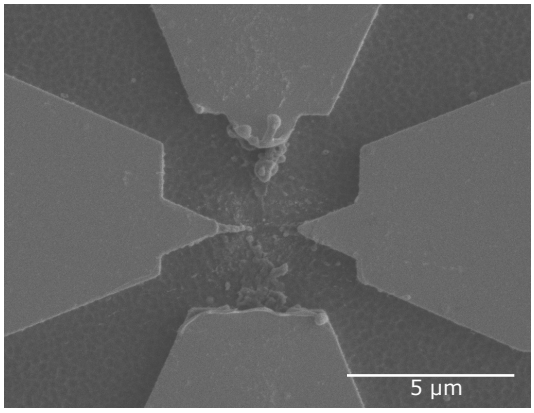


Figure 3.21: SEM that shows device destruction due to electromigration that occurred during emission testing.

current densities can lead to electrical breakdown in the form of low-impedance vacuum arcing, resulting in device destruction [49, 50]. Fig. 3.21 shows an SEM of a four-terminal early-work device fabricated according to the steps outlined in Fig. 3.5. The micrograph was taken after the emission characteristic no longer resembled FN emission during high-temperature measurements, and it unveiled the catastrophic demise.

In addition to the emission electrodes, vacuum field emission devices also have other materials and components. At high temperatures, leakages from these parts may cause parasitic-dominated measurements, which can mask electron field emission, as the devices discussed in this chapter have experienced. Some of these other components are discussed below.

The device is usually fabricated on an insulator substrate, which may allow leakages through it, such as FP emission, at high temperatures and fields that could interfere with FN emission. Even if the substrate conduction at high fields and elevated temperatures is not a problem, packaging can be challenging. Metal interconnects, bond pads, and bond wires must be carefully chosen. In this chapter, Ti/Au pads and Al wires, which are readily available in the cleanroom and are a popular choice, were used. However, these materials become incompatible at temperatures above 300 °C due to intermetallic formation and Kirkendall voiding, which can weaken the bonds' strength and increase their electrical resistance [51]. Aluminum is also not a good choice because it readily electromigrates at moderate temperatures. Gold is a better choice for wire bonds, but it can alloy with the adhesion layer at high temperatures. Therefore, metal layers with low mutual diffusivities are needed. A promising metallization scheme that has been successful as a diffusion barrier against oxidation, has good adhesion, and prevents gold from wire bonds from intermixing with other metal layers is Ti/$TaSi_2$/Pt. Ti forms a good Ohmic contact and has great adhesion, and Pt can be easily wire bonded using Au wires. The $TaSi_2$ layer also reacts with Pt to form Pt_2Si, which serves as a diffusion barrier [52, 53].

A package that can withstand the stresses of elevated temperatures and does not contribute to parasitic conduction is also needed. Traditional plastic PCB materials, such as FR4, can only tolerate temperatures below the glass transition, which are usually moderately low. A prototype ceramic package made with 96% polycrystalline aluminum oxide and thick gold metallization has successfully operated over 10,000 hours at 500 °C [53]. However, a more commercially available package would be preferred. High-temperature co-fired ceramic (HTCC) alumina packages

are a good option, but they can be hard to come by, especially for custom-sized dies [54]. The choice of die-attach material is also important, as the coefficient of thermal expansion between the substrate die material, die-attach, and package must be matched to avoid stresses or fractures.

Moreover, uniformity in the fabrication of the suspended devices discussed in this chapter is challenging due to the custom nature of the milling process. Consequently, the emission characteristic between fabricated devices varies a lot, which can be burdensome for circuit design. Membranes are also fragile, so the fabrication yield is lower compared to devices made on bulk substrate. Fig. 3.22 shows an example of a membrane that broke during the milling step. Therefore, the fabrication process must be modified if mass production is desired. Nonetheless, nanoprotrusions are inevitable, which can cause noise in the emission characteristic in the form of discrete jumps in the measured current. In many cases, these emission instabilities go away over time as ion bombardment can blunt these nanoprotrusions [55]. However, there are some instances wherein the large field enhancements caused by these nanoprotrusions can lead to device destruction. In any case, as the field enhancement factor is tightly connected to the presence of nanoprotrusions, which are impossible to predict, it is very hard to model field emission currents a priori. Also, the effects of surface roughness and nanoprotrusions become more significant as the emitter-to-collector gap is reduced to the smallest attainable dimensions.

As mentioned in Section 3.1, we aimed to fabricate the smallest emitter-to-collector gap as this would yield low turn-on voltages. This was easier to achieve with the devices fabricated on a thick substrate, as we used high-resolution standard EBL.

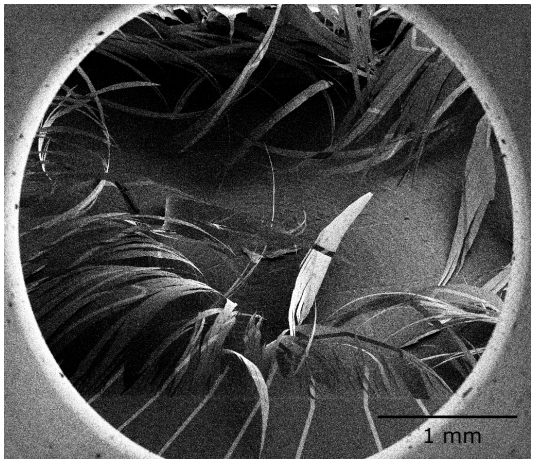


Figure 3.22: Suspended device that broke during milling.

However, it was hard to accomplish with the devices on membranes due to the residual stress that would oppose this effort. As a result, the operating voltages were higher than our desired < 10 V. One way to achieve a shorter electrode separation is to use the stress to our advantage by patterning stress-release cuts in the vicinity that shrink the gap rather than expand it [56].

One approach that has been shown to reduce the operating voltage is to coat the emitter terminal with a thin layer of an electropositive element relative to the cathode material. This layer reduces the barrier for electron emission by lowering the work function. The deposited layer must be thin enough so that the electropositive material is ionically bonded to the substrate and forms a surface dipole layer through the redistribution of electron density, which helps the electrons escape into vacuum. If the coating is too thick, the work function becomes closer to the coating work function as the coating becomes metallic [57]. Common electropositive materials used to enhance cathode performance include alkali metals, alkaline earth metals, and their oxides, such as cesium [58, 59], barium [60], and cesium oxide [61]. Other pure elements and oxides can also be used; for example, the deposition of monolayers of zirconium (work function ~4.1 eV) on W has been shown to reduce the work function to 2.62 eV [62]. In addition, surface coating has the potential to reduce outgassing as the coating layer can act as a barrier at the surface. However, this may not be a permanent solution to enhance emission current as high operating voltages can eventually erode the coating layer through ion sputtering.

The field emission devices reported in this chapter were prone to flicker noise that cause current instabilities. Unlike thermionic emitters that operate in a space charge limited regime, the nanoscale single-tip emitters described in this chapter are exposed to the statistical fluctuation and randomness of electron field emission. While the specific reason for the observed current instabilities is not known with certainty, several plausible causes include the sharpening and blunting of nanoprotrusions on the emitter tip, changes on an atomic scale in the work function due to the adsorption and desorption of gas molecules, and electromigration of impurities. Emission stability has been shown to improve with lower ambient pressures [63] so a better vacuum is desired. Another potential improvement is to increase the number of emitter tips. The benefit of having multiple identical tips is that current fluctuation from a single emitter can be statistically reduced by ensemble averaging the emission current from a group of emitters operating simultaneously [64]. Additionally,

having many emitter tips allows for higher currents to be sourced, improving device parameters. This concept is further discussed in the following chapter.

Generally, the emission characteristic can be modified by either engineering the material properties, specifically the work function of the electrodes, or by manipulating the physical geometry. In this way, either of these approaches could be used to improve the efficiency of the four-terminal devices and reduce power consumption. Materials with higher work function, such as Pt, could be deposited onto the collector and gate terminals to minimize leakage currents from the gate into the collector and achieve rectifying behaviour. A wrap-around gate could be fabricated to reduce operating voltages and maximize the gate control in electron emission [65]. Overall, these refinements should improve the transconductance of the devices.

In our analysis, it is important to note that while we tried to extract physical meaningful parameters from the linear fit of the FN plot in line with the field emission community, it is difficult to make definite claims on the specifics of the emission process. This is because the linearized FN equation is degenerate, as both the slope and the y-intercept are needed to describe it. However, these two parameters are related to three physical variables: the field enhancement factor, the emission area, and the work function. Therefore, even though we kept the value of one physical parameter constant (i.e., the work function) to extract the other two, it is possible that all three of them changed as experimental conditions were modified.

Further work should extend to studying the radiation hardness performance of the proposed lateral nanoscale field emission devices for space and nuclear applications, as well as studying the emission characteristic at low temperatures for the design of cryogenic electronic circuits. Operating at cold temperatures may reduced leakage currents associated with high temperatures, leading to more stable emission.

3.6 An Attractive Material: Diamond

Diamond is a promising material for robust field emission devices that has attracted significant attention due to its interesting properties, including:

- high thermal conductivity, which prevents overheating (particularly useful for high-power and high-temperature operation),
- chemical inertness (advantageous for stable emission current),
- high physical hardness to withstand ion bombardment (and thus, avoid tip erosion and improve device lifetime),

- large intrinsic breakdown field (good for high-power applications),
- large band gap (suitable for high-temperature operation).

However, its most fascinating property for field emitter fabrication is its negative electron affinity (NEA) or low positive electron affinity. The electron affinity is the energy needed to remove an electron from the conduction band minimum of a semiconductor and escape into vacuum. A NEA is attractive due to the small barrier for field emission, which results in low voltage operation. This efficient electron emission, in theory, removes the need to fabricate sharp tips to achieve large field enhancement factors, increasing the durability of field emitters and facilitating fabrication.

It has been reported that partially hydrogenated (100) and (111) diamond surfaces have effective NEA [66, 67]. Thin metallic films, such as titanium, cobalt, copper, nickel, and zirconium, can also induce effective NEA in diamond [68–71]. Even though the work function of cobalt is higher than that of zirconium or titanium, it is less reactive. While surface coatings, such as cesium and barium, have been used on silicon and metal field emitters to lower their effective work functions [57, 72], they tend to be chemically reactive, limiting their lifetime. In contrast, diamond surfaces offer the benefits of chemical stability and mechanical strength.

However, undoped diamond cannot support sustained electron emission due to its wide band gap ($\sim$ 5.5 eV). Thus, a continuous source of electrons is needed to supply charge carriers into the conduction band of diamond. To take advantage of diamond's NEA and induce emission with a low applied electric field, the Fermi level must be close to the conduction band, requiring n-type donor impurities, which is an experimentally challenging task. Introducing such impurities into diamond is limited by the solubility and ionizability of donors used, as well as by the host crystal's difficulty in spontaneously creating defects to compensate the dopant species due to the tight lattice structure [73]. Lithium, phosphorous, and sodium have been predicted to be shallow donors that occupy interstitial sites, but their low solubility makes in-diffusion processes unsuccessful, requiring ion-implantation [74]. However, ion-implantation can cause substantial damage, leading to poor film quality and irreversible graphitization in diamond crystallites, which can adversely affect field emission [75, 76].

Substitutional nitrogen in nanocrystalline diamond is a promising donor candidate due to its small covalent radii and high solubility. Even though it forms a deep

donor level around 1.7 eV below the conduction band of diamond, as the donor energy level still lies above the Fermi energy of several metals, a depletion layer of ionized donors forms in equilibrium. If the donor concentration is sufficiently high, band bending causes the tunneling barrier to narrow so that electrons emit into diamond [77–79]. Fig. 3.23 illustrates the energy levels for n-type diamond when it is positively biased to induce electron emission. For electrons to emit from the metal into vacuum through diamond, they must first tunnel through the metal-diamond interface, which depends on the donor concentration and choice of metal, then conduct through the diamond layer, which is affected by the content of sp^3 and sp^2 phase (this is discussed below) and impurity doping concentration, and finally tunnel from diamond into vacuum, which is controlled by the geometry [80, 81].

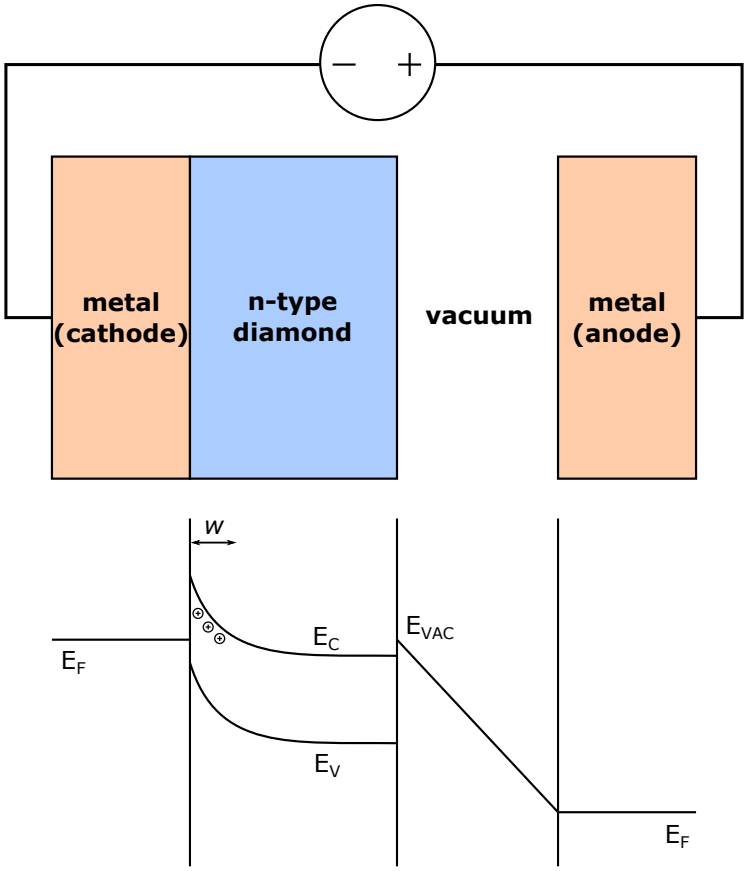


Figure 3.23: Simplified band diagram illustrating the field electron emission mechanism from a metal cathode coated with n-type diamond with an effective NEA under forward bias. A depletion layer of width w with ionized donors forms at the metal-diamond interface.

Traditional diamond thin films are usually synthesized by hot filament chemical vapour deposition (HFCVD), which requires substrate temperatures above 500 °C. In addition, mechanical substrate polishing is often required to enhance diamond's nucleation density [82, 83]. The high deposition temperatures and added fabrication steps needed for a high-quality film have deterred the fabrication of diamond field emitters. Instead, a simpler manufacturing process that can easily combine diamond with other materials is preferred. Ultrananocrystalline diamond (UNCD) synthesized using microwave plasma-assisted chemical vapour deposition (MPCVD) has emerged as a very promising material. UNCD diamond can be deposited at temperatures as low as 350 °C on a wide range of substrates including Si, SiO_2, Ta, Ti, W, and SiN. While it preserves the robustness of the mechanical, thermal, and chemical properties of conventional CVD microcrystalline diamond films, UNCD has ultrasmall (3–5 nm) grain size and a higher volume density of grain boundaries [83–85]. This facilitates the incorporation of nitrogen dopants for n-type conductivity. It has also been reported that diamond films with high defect contents and smaller grain sizes have higher electron emission than films with fewer defect structures and larger grain sizes [86, 87]. Additionally, smaller grains improve the mechanical resistance to breakdown. UNCD is smoother, eliminating the need for mechanical polishing. By controlling the deposition parameters such as the gas flow rate and gas concentration, the size and sp^2 phase content can be easily controlled [88]. This is particularly beneficial as it has been shown that an optimal content of sp^3 and sp^2 exists for improved field electron emission. If the sp^3 content is too high, then the effective supply of electrons is too low for sustained field emission. If the sp^2 content is too high, the electron affinity increases and the tunneling barrier becomes higher [89]. UNCD is synthesized using a $CH_4/N_2/Ar/H_2$ gas mixture plasma. CH_4 is the carbon source gas due to its high purity and shared tetrahedral structure with diamond, Ar modifies the grain size, H_2 introduces the surface hydrogen termination for NEA, and N_2 adds the n-type dopant [90]. Moreover, UNCD can be easily etched using ICP-RIE techniques in an oxygen plasma with good selectivity [83].

Electron emission experiments using MPCVD n-type diamond have shown lower threshold fields, and improved emission stability compared to conventional Si or metal emitters. For example, Subramanian et al. [91] have demonstrated a lateral field emission diamond diode fabricated on silicon-on-insulator (SOI) wafer with an anode-to-cathode separation of 3 μm. The device exhibited a low turn-on voltage of 5.9 V and a high emission current of 1.1 mA at an anode voltage of 100 V from a six-finger configuration. The electron emission was stable with a $\sim 4\%$ current

fluctuation over 10 hrs at a vacuum pressure of 10^{-6} Torr. They also showed high radiation tolerance of diamond field emitters [92, 93]. In a separate experiment, they demonstrated a lateral vacuum field emission microtriode utilizing nanocrystalline diamond with a measured anode current of 4 μA and a transconductance of 0.3 μS from a single emitter-finger at a gate voltage of 40 V and anode voltage of 65 V. The gate-cathode spacing was 3 μm and the anode-cathode spacing was 12 μm [41]. These are very promising results that illustrate the suitability of MPCVD n-type diamond as a field emitter material for harsh environment operation. Moreover, if higher-resolution lithography is used to achieve even smaller device dimensions [94, 95], improved device operation is expected.

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Chapter 4

FIELD EMISSION DEVICES FOR HIGH-FREQUENCY OPERATION

Field emission devices are promising candidates for high-frequency electronics due to the intrinsic superiority of vacuum as a transport medium. While carriers in semiconductor channels suffer from acoustic and optical phonon scattering, electrons in vacuum can, in theory, travel ballistically. This means that the saturation velocity for electrons is restricted to about 1×10^7 cm/s in Si, the most widely-used semiconductor material, whereas it can reach 3×10^{10} cm/s in vacuum. In addition, advanced nanofabrication techniques used in the solid-state industry can be employed to manufacture the smallest nanoscale vacuum channels, potentially leading to the production of field emission devices that can operate at GHz frequencies or higher.

The FN theory, which is based on the time-independent Schrödinger equation, forms the foundation of field electron emission theory. When an AC field is applied, the FN theory is still valid as long as the tunneling time, τ_{tun}, is small relative to the rate of change of the applied field so that the tunneling electron does not feel the changing vacuum potential barrier. Thus, the value of the instantaneous electric field is used in the conventional FN equation. This adiabatic condition can be expressed as $\omega|\tau_{tun}| \ll 1$, where ω is the frequency of the dynamic field [1]. For practical devices based on the direct interaction of field emission and electromagnetic waves, it has been shown that for frequencies up to about 10^{14} Hz, the FN equation still holds [2], and the time-dependent transmission coefficient preserves phase with the electric field. Therefore, field emission devices are an attractive option for microwave cathode applications because their response to applied electric fields is virtually instantaneous, as the emission is a quantum mechanical process that does not require heating.

Additionally, high-frequency operation of field emission devices reduces ion bombardment. This is due to an effective repulsive potential that forms near the surface of the cathode when a microwave field is applied, making emission under a fast AC field more stable [3]. This can ultimately increase the lifetime of the device. Another interesting characteristic of field electron emission is its non-linear rela-

tionship between the applied electric field and the emitted current, which enables the development of cold cathodes as practical microwave devices that can perform non-linear operations such as frequency mixing and harmonic generation.

In this chapter, we demonstrate a multi-tip field emission two-terminal device for frequency mixing. We describe the fabrication steps, testing setup, and results. We also introduce some preliminary results in work function reduction by thin-film praseodymium (Pr) evaporation.

Parts of this chapter were adapted from [4, 5].

4.1 Fundamentals of Frequency Multipliers and Mixers

Frequency multipliers and mixers are essential components of modern electromagnetic technology. They are used in radar and high-bandwidth communication industries for military, radio astronomy, and civil use, as well as in high-speed transmitters and receivers in sensing systems.

To achieve frequency conversion, an element with a non-linear IV characteristic is required. Fig. 4.1 illustrates a generalized field emission IV plot. Due to its non-linear nature, FN electron emission is a good candidate for achieving harmonics-rich current. When an applied small AC voltage, $V_1(t) = v\cos(\omega t)$, is superimposed on a large DC bias, V_0, defining the Q point shown (an operating point located on the non-linear part of the IV characteristic), the resulting field emission current, $I_1(t)$,

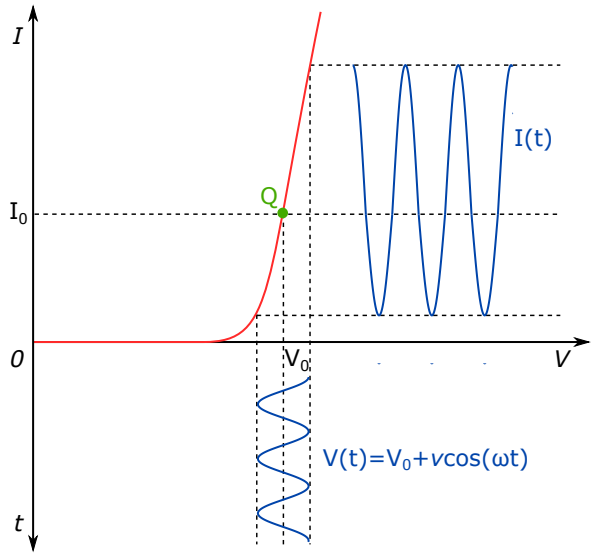

Figure 4.1: Generalized FN emission IV characteristic and harmonic-rich resulting current due to the inherent non-linearity of the transfer function.

is not symmetric about I_0 but rather has different amplitudes on the positive and negative half-cycles. This distortion is mainly due to a second harmonic component at frequency 2ω [6].

For a quantitative analysis of frequency conversion, consider the simplified FN equation given by

$$I = AV^2 \exp\left(-B/V\right) \tag{4.1}$$

where A and B are constants that incorporate the work function, field enhancement factor, emitting area, and the FN constants. Let the input voltage, $V(t)$, be represented by the sum of a DC bias component, V_0, and a small AC signal, $v\cos\left(\omega t\right)$, so that

$$V(t) = V_0 + v\cos\left(\omega t\right) \tag{4.2}$$

where $|v| \ll |V_0|$. A Taylor series expansion of Eq. (4.1) about V_0 yields

$$I(t) = I_0 + \frac{dI}{dV}\Big|_{V=V_0}\left[v\cos\left(\omega t\right)\right] + \frac{1}{2}\frac{d^2I}{dV^2}\Big|_{V=V_0}\left[v\cos\left(\omega t\right)\right]^2 + \cdots \tag{4.3}$$

where $I_0 = AV_0^2\exp\left(-B/V_0\right)$. If we compute the derivatives, we obtain

$$\frac{dI}{dV}\Big|_{V=V_0} = 2AV_0\exp\left(-B/V_0\right) + AB\exp\left(-B/V_0\right) \tag{4.4}$$

and

$$\frac{d^2I}{dV^2}\Big|_{V=V_0} = \frac{AB^2}{V_0^2}\exp\left(-B/V_0\right) + \frac{2AB}{V_0}\exp\left(-B/V_0\right) + 2A\exp\left(-B/V_0\right) \tag{4.5}$$

so that

$$\begin{aligned} I(t) = {} & AV_0^2\exp\left(-B/V_0\right) + \left(2AV_0\exp\left(-B/V_0\right) + AB\exp\left(-B/V_0\right)\right)\left[v\cos\left(\omega t\right)\right] + \\ & \left(\frac{AB^2}{V_0^2}\exp\left(-B/V_0\right) + \frac{2AB}{V_0}\exp\left(-B/V_0\right) + 2A\exp\left(-B/V_0\right)\right)\left[v\cos\left(\omega t\right)\right]^2 + \cdots \end{aligned} \tag{4.6}$$

If we use the trigonometric identity: $\cos^2\left(\theta\right) = \frac{1}{2} + \frac{1}{2}\cos\left(2\theta\right)$, we can rewrite Eq. (4.6) as

$$\begin{aligned} I(t) = {} & I_0\left(1 + \frac{v^2}{V_0^2} + \frac{Bv^2}{V_0^3} + \frac{B^2v^2}{2V_0^4} + \cdots\right) + I_0\left(\frac{2v}{V_0} + \frac{Bv}{V_0^2} + \cdots\right)\cos\left(\omega t\right) + \\ & I_0\left(\frac{v^2}{V_0^2} + \frac{Bv^2}{V_0^3} + \frac{B^2v^2}{2V_0^4} + \cdots\right)\cos\left(2\omega t\right) + \cdots \end{aligned} \tag{4.7}$$

The first term corresponds to the DC bias current that leads to rectification, the second term is the attenuator or amplifier of the fundamental frequency, and the

third term is the second harmonic that arises due to the non-linearity in the transfer function. Higher-order terms can also be present, but they were omitted for simplicity as their power decreases with increasing multiplication factors in resistive multipliers. This is the basic principle of operation of a frequency multiplier, in which a non-linear device is used to generate harmonic frequencies that were not present in the original AC or fundamental signal.

Next, we consider a two-tone input signal given by

$$V(t) = V_0 + v_1 \cos(\omega_1 t) + v_2 \cos(\omega_2 t). \tag{4.8}$$

Similarly to the previous analysis, if we apply this voltage to a non-linear device whose output current is obtained by performing a Taylor expansion around the Q point at (V_0, I_0), we get

$$\begin{aligned} I(t) =& I_0 + \frac{dI}{dV}\Big|_{V=V_0} [v_1 \cos(\omega_1 t) + v_2 \cos(\omega_2 t)] + \\ & \frac{1}{2}\frac{d^2 I}{dV^2}\Big|_{V=V_0} [v_1 \cos(\omega_1 t) + v_2 \cos(\omega_2 t)]^2 + \cdots \end{aligned} \tag{4.9}$$

If we plug in the results from Eq. (4.4) and Eq. (4.5), and recall the trigonometric identity: $2\cos\theta\cos\phi = \cos(\theta - \phi) + \cos(\theta + \phi)$, we obtain

$$\begin{aligned} I(t) =& I_0 \left(1 + \frac{v_1^2}{V_0^2} + \frac{B v_1^2}{V_0^3} + \frac{B^2 v_1^2}{2V_0^4} + \frac{v_2^2}{V_0^2} + \frac{B v_2^2}{V_0^3} + \frac{B^2 v_2^2}{2V_0^4} \cdots\right) + \\ & I_0 \left(\frac{2v_1}{V_0} + \frac{B v_1}{V_0^2} + \cdots\right) \cos(\omega_1 t) + I_0 \left(\frac{2v_2}{V_0} + \frac{B v_2}{V_0^2} + \cdots\right) \cos(\omega_2 t) + \\ & I_0 \left(\frac{v_1^2}{V_0^2} + \frac{B v_1^2}{V_0^3} + \frac{B^2 v_1^2}{2V_0^4} + \cdots\right) \cos(2\omega_1 t) + \\ & I_0 \left(\frac{v_2^2}{V_0^2} + \frac{B v_2^2}{V_0^3} + \frac{B^2 v_2^2}{2V_0^4} + \cdots\right) \cos(2\omega_2 t) + \\ & I_0 \left(\frac{2v_1 v_2}{V_0^2} + \frac{2B v_1 v_2}{V_0^3} + \frac{B^2 v_1 v_2}{V_0^4} + \cdots\right) \cos((\omega_1 - \omega_2) t) + \\ & I_0 \left(\frac{2v_1 v_2}{V_0^2} + \frac{2B v_1 v_2}{V_0^3} + \frac{B^2 v_1 v_2}{V_0^4} + \cdots\right) \cos((\omega_1 + \omega_2) t) + \cdots \end{aligned} \tag{4.10}$$

Therefore, a signal that has a frequency equal to the sum of both input frequencies, $\omega_1 + \omega_2$, and a signal that has a frequency equal to the difference of both input frequencies, $\omega_1 - \omega_2$, have been generated. For simplicity, only the square term in the Taylor expansion has been considered to solely focus on the second-order

intermodulation products (i.e., mixing terms). If the cube term is used, third harmonics as well as higher-order intermodulation products are created.

Thus, the main function of a frequency mixer is to convert information from one frequency to another frequency. If the second frequency is higher, making the information easier to transmit or radiate, the process is known as up-conversion, while if the second frequency is smaller, making the information easier to receive or capture, the process is called down-conversion. In down-conversion, the two input signals are more commonly referred to as the local oscillator (LO) signal and the radio frequency (RF) signal, while the output signal is known as the intermediate frequency (IF). In up-conversion, the LO and the IF signals are mixed to generate the RF signal. The first case illustrates a device that is used as a receiver, while the second scenario depicts a device that is used as a transmitter. In both cases, the LO port is usually driven with a sinusoidal continuous wave or square wave signal. The process of heterodyning is depicted in Fig. 4.2 [7].

One of the most important figures of merit that define the performance of a mixer is the conversion loss, which is defined as the ratio of the available input power, $P_{in}(RF)$, over the obtained IF power, $P_{out}(IF)$:

$$\text{Conversion loss in dB} = 10\log_{10}\left[\frac{P_{in}(RF)}{P_{out}(IF)}\right]. \tag{4.11}$$

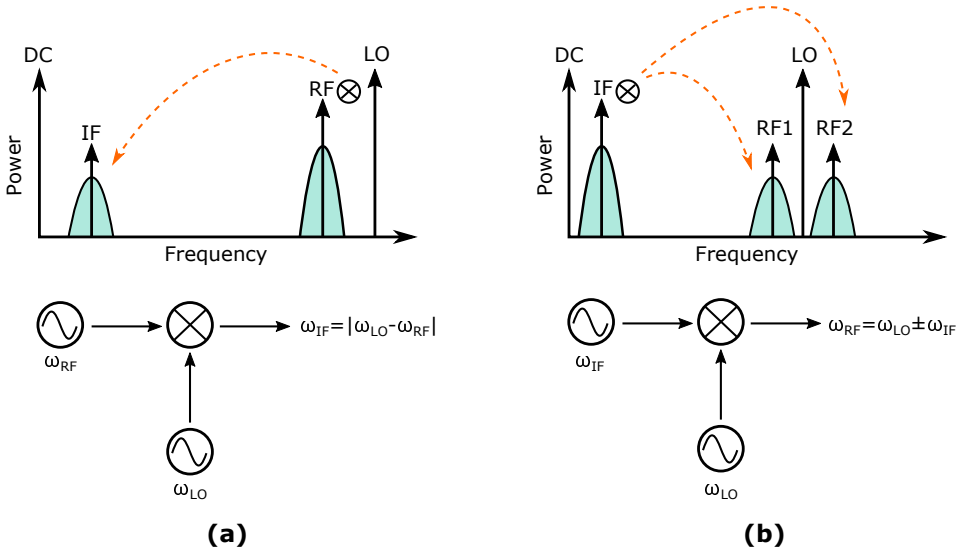

Figure 4.2: Generalized frequency mixer: (a) down-conversion, and (b) up-conversion. Note that in (a) the product $\omega_{LO} + \omega_{RF}$ also forms but is not shown.

The most simple frequency mixer can be made by using a single diode in its design. While single-diode mixers tend to have poor isolation and low conversion efficiency, they are particularly useful at very high frequencies and wide bandwidths.

4.2 General Design Paradigm

One of the most important considerations when designing high-frequency devices is minimizing the capacitance, as this parameter is inversely proportional to the maximum speed of operation. There have been multiple attempts to fabricate field emission devices for high-frequency operation, but most of them have employed traditional Spindt-type vertical field emitter arrays, which have a large overlapping area between the electrodes. As a result of the large capacitance between the gate and the base electrode, their operation has been limited to a few gigahertz [8, 9].

To minimize the overlapping area between the electrodes and reduce the capacitance, lateral devices were fabricated, which provide more design freedom compared to vertical devices. Using advanced nanofabrication techniques and high-resolution electron lithography [10, 11], nanoscale gap spacings between the emitter and collector terminals were achieved. This allows for operation at low voltages, which is desirable to reduce power consumption and Joule heating, increase device lifetime by minimizing ion sputtering, and produce high transconductance devices that are essential for practical electronic devices [12, 13]. Additionally, low voltage operation can reduce leakage currents that arise at high fields and compete with field emission, such as Frenkel-Poole emission or Ohmic conduction [14]. Small gaps also shorten the electron transit time for high-speed operation.

Furthermore, devices with many emitter tips per device were fabricated to source higher currents. This enables operation at a higher Q point along the non-linear IV characteristic for better mixing and lower conversion loss. Emission from multiple tips should also decrease flicker noise by number averaging, which is desirable for a more stable emission. Additionally, devices with 10, 20, 30, 40, 50, 60, and 70 tips were fabricated to study the effect of the number of tips on field emission current. It is expected that higher currents are achieved for a given voltage and a more stable emission with devices that have higher number of emitter tips.

Gold was selected as the electrode material. Even though it has a relatively high work function (~5.3 eV [15]), Au was chosen due to its chemical unreactivity, ensuring that the value of the work function would not vary and affect emission stability. In addition, lift-off is relatively easy and results in clean edges and reproducible

fabrication. Pt was also considered, but lift-off unfortunately resulted in a large number of flags that caused device shorting and inconsistent fabrication results.

Fused silica was chosen as the substrate due to its low loss tangent, which makes it a suitable low-loss material at microwave frequencies. It is also easy to undercut with wet HF etching, allowing for the creation of a trench-like structure in the vicinity of the emitting region to increase the length of the leakage pathway. Removing any insulating material near high electric fields prevents charging effects that cause hysteretic behavior, as well as avoids dielectric breakdown and device failure. Undercutting the substrate near the emitter also minimizes electron collisions onto the substrate and back-scattering. Fused silica is also an appealing material due to its low cost.

Two kinds of geometries were considered: a symmetric structure, in which the emitter and collector were indistinguishable, and an asymmetric structure, in which one terminal consisted of a multi-tip array (i.e., the emitter) while the other terminal was blunt (i.e., the collector). The sharp terminal was expected to start emitting electrons at a smaller voltage compared to the blunt terminal due to the field enhancement it experiences. The goal of such a device was to mimic the asymmetric IV characteristic of traditional solid-state diodes. However, due to the increased size of the collector terminal, the capacitance of such a structure was expected to be higher than that of the symmetric structure.

For high-frequency measurements, the input signal was coupled to the device via a coplanar waveguide. The widths of the trace and ground plane spacing were chosen to match the characteristic impedance of 50 Ω.

4.3 Selection of Physical Design Parameters

COMSOL Multiphysics 6.0, a three-dimensional FEM simulator, was used to determine the optimum dimensions for the lateral field emitter multi-tip array. The goal was to maximize the field enhancement factor and minimize the capacitance of the device. Fig. 4.3 sketches the design parameters that were optimized:

- tip length
- tip base
- metal thickness
- undercut radius

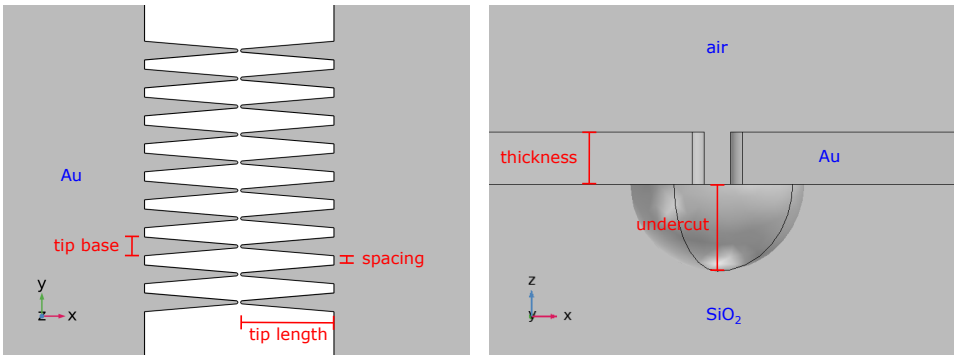

Figure 4.3: Simulation geometry: (a) top-view, and (b) cross-sectional view.

- spacing (period)

The undercut was modeled as a semi-sphere to roughly mimic an isotropic wet etch. Only the symmetric geometry was considered due to its lower expected capacitance. For all simulations, the gap dimension was set to 30 nm.

First, an individual tip with no undercut was modeled, as shown in Fig. 4.4 (a). Before proceeding with any design parameter sweep, a mesh study was conducted to optimize for accuracy and speed of the simulation. A box enclosing the gap between the terminals was defined to create a finer mesh at the region of interest, as shown in Fig. 4.4 (b). A mesh with a maximum element size of 2 nm was chosen for this box. Note that to achieve realistic modeling results and avoid electromagnetic field singularities, a fillet with a radius of 15 nm was used to round the edges of the tip. This provided a lower bound for the field enhancement factor, as nanoprotrusions created during fabrication give rise to higher field enhancement factors that are impossible to determine a priori. In addition, a cut line within the gap bounded by the two electrodes and located halfway up the metal layer, as illustrated in Fig.

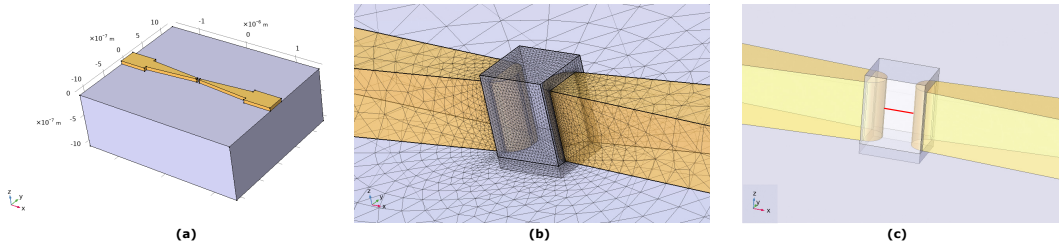

Figure 4.4: Single-tip simulation: (a) overall geometry, (b) fine mesh box, and (c) cut line (red line).

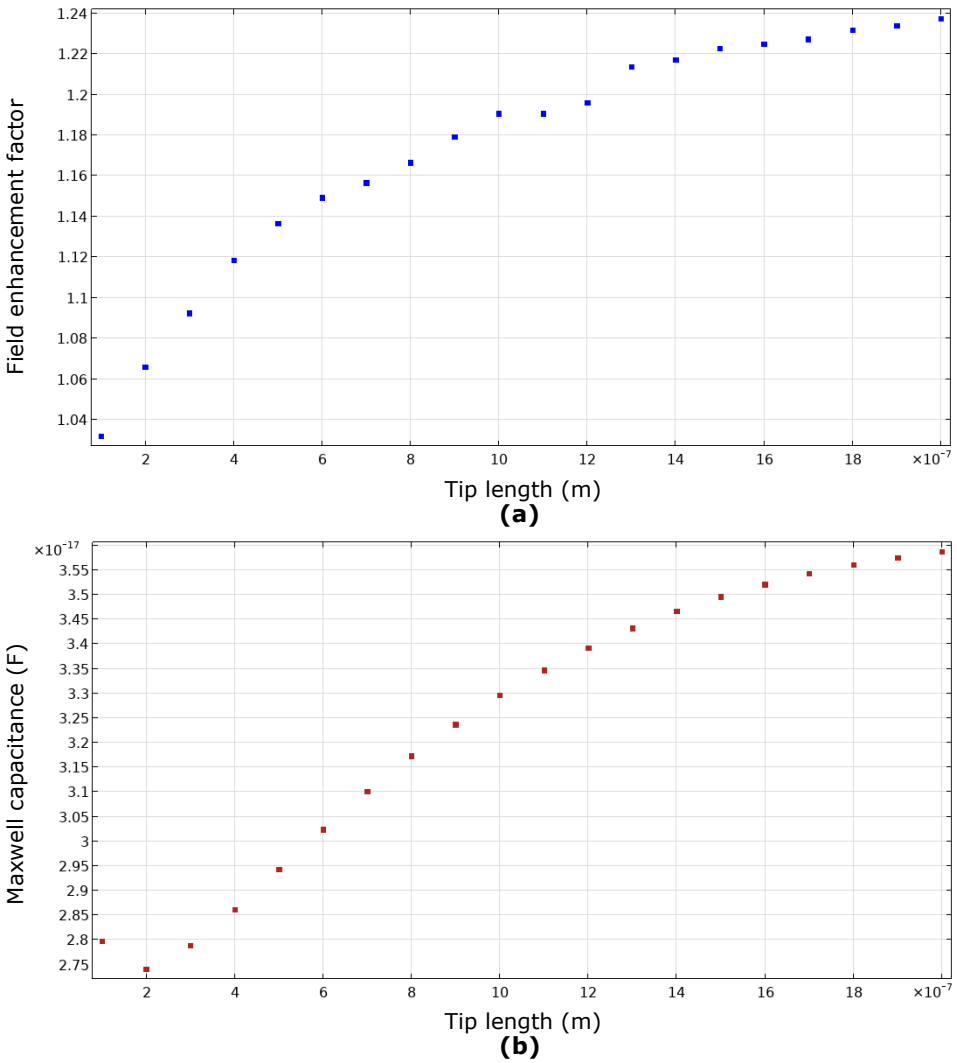

Figure 4.5: Single-tip simulation results: (a) field enhancement factor and (b) Maxwell capacitance as a function of tip length.

4.4 (c), was used to determine the field enhancement factor to avoid anomalous enhancement from the bottom and top layers.

For the studies, only one variable was swept at a time and the rest were kept constant. The results for the field enhancement factor and Maxwell capacitance for tip length, tip base, and metal thickness are shown in Figs. 4.5, 4.6, and 4.7, respectively. It was observed that for a shorter tip length, the field enhancement factor decreased while the capacitance increased. However, it was interesting to see that when the tip length became too short, the capacitance increased again, as it became dominated by the parallel plate capacitance of the connecting terminal rather than the tip. Ultimately,

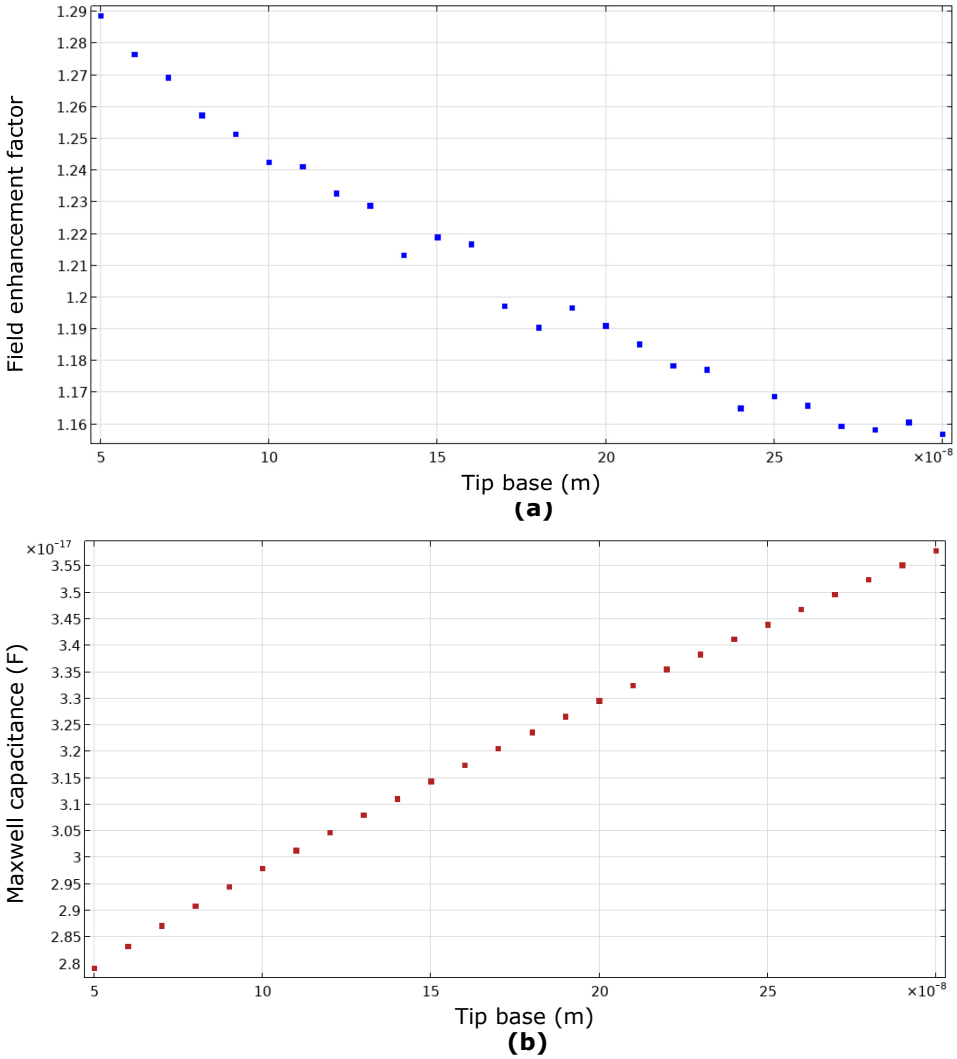

Figure 4.6: Single-tip simulation results: (a) field enhancement factor and (b) Maxwell capacitance as a function of tip base.

a tip length of 1000 nm was selected to compromise between the field enhancement factor and capacitance.

In terms of tip base dimension, a narrower base led to both decreased capacitance and increased field enhancement factor. While at first it would seem best to fabricate emitter tips with the smallest base as it would also provide the advantage of more tips per device, a very narrow tip also suffers from high resistance. This can adversely affect the speed of operation of the devices as well as the lifetime, as Joule heating can become problematic. In this way, a tip base of 200 nm was chosen.

The effect of varying metal thickness on the field enhancement factor became considerable when the thickness was < 30 nm. In addition, the capacitance increased

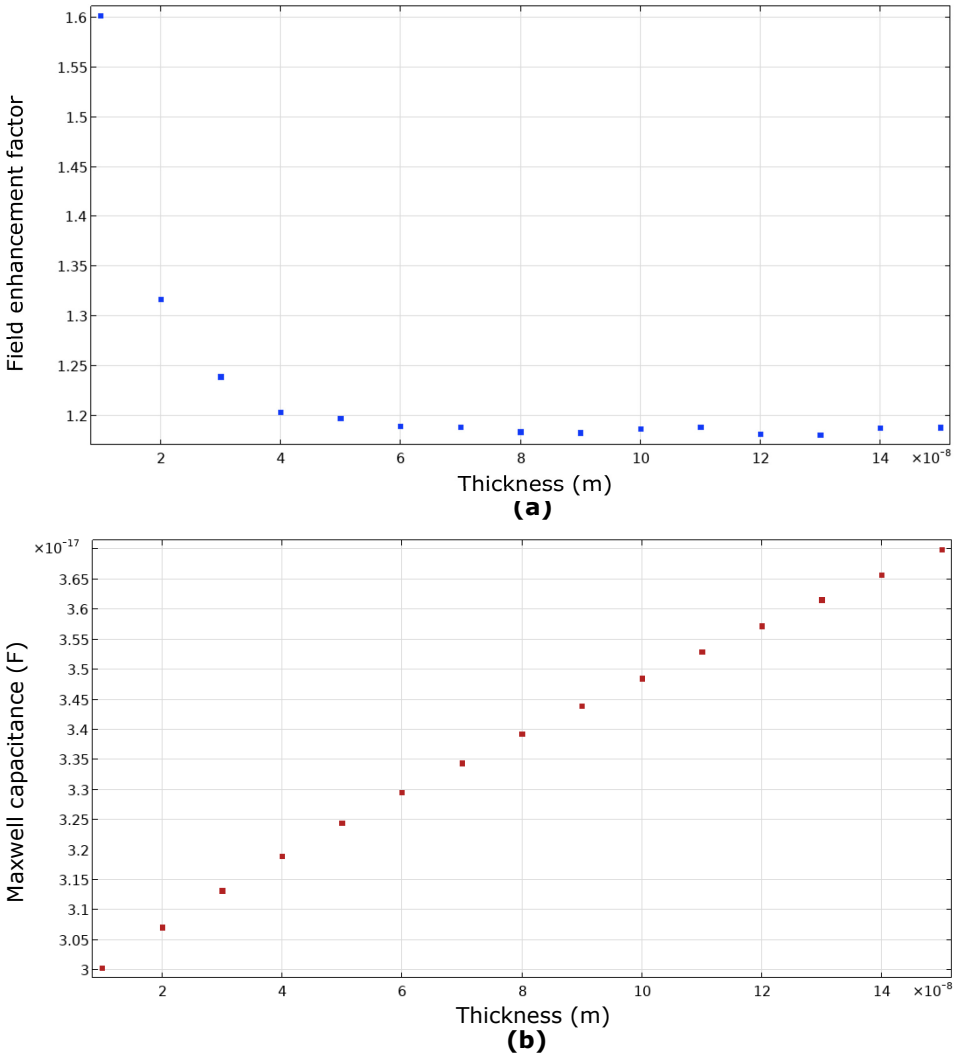

Figure 4.7: Single-tip simulation results: (a) field enhancement factor and (b) Maxwell capacitance as a function of metal thickness.

with increasing thickness. This was expected as a thicker device meant more overlapping electrode area. A further advantage of thin devices is that lift-off is easier. However, due to the considerable increase in resistance that very thin structures may bring about, a metal thickness of 60 nm was selected for the gold arrays.

Next, the effect of isotropic undercut was studied. The results are presented in Fig. 4.8. Varying the undercut had a considerably less significant effect on the overall change of the field enhancement factor. This is valuable because it is hard to control the exact amount of undercut when a wet etch at such small dimensions is used. However, it is worth noting that the capacitance decreased roughly by half when

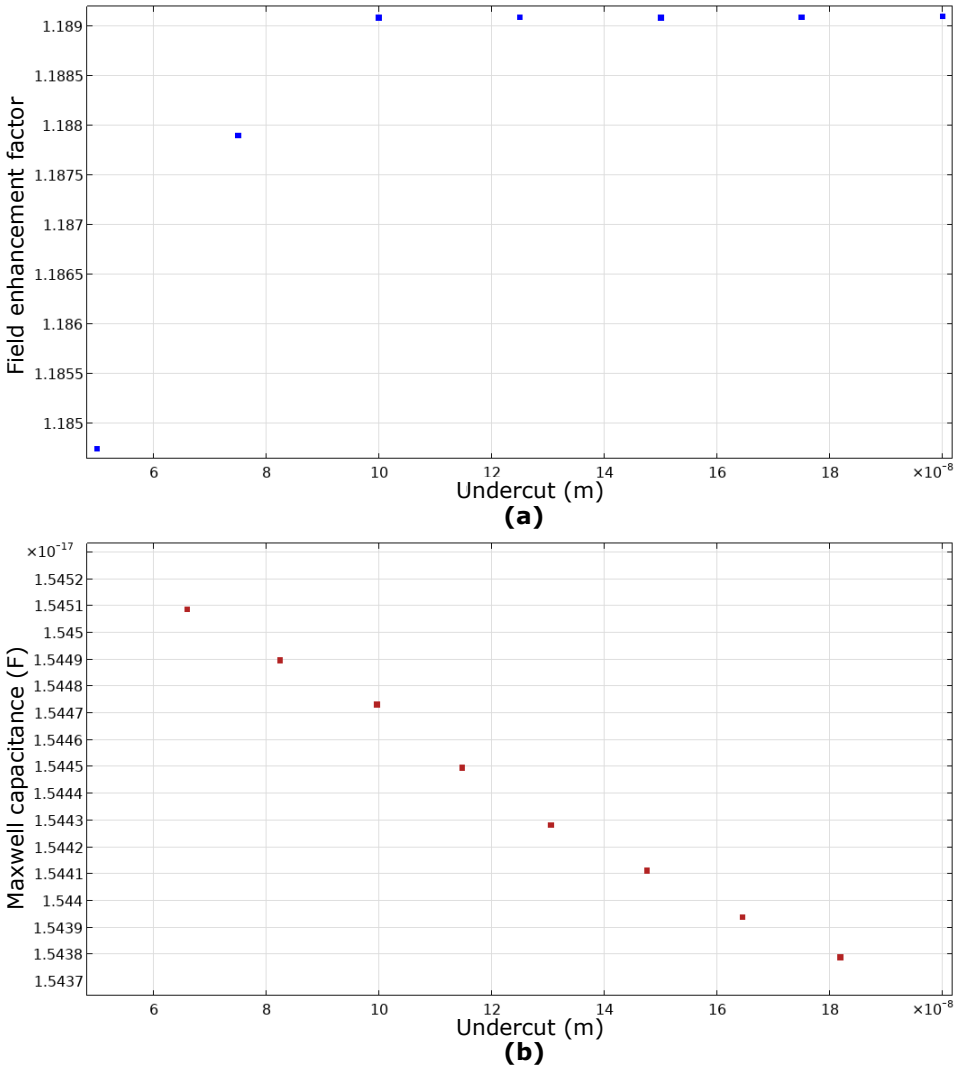

Figure 4.8: Single-tip simulation results: (a) field enhancement factor and (b) Maxwell capacitance as a function of substrate undercut.

the sample was undercut, as expected due to the decrease in the dielectric constant when air replaces fused silica. While it is desirable to undercut the structures as much as possible in terms of capacitance, a tip that is too suspended can lose structural stability during the wet etch and bend. The devices may also experience electromechanical motion when high fields are applied and could ultimately become electromechanical switches. Therefore, an undercut of around 100 – 200 nm was attempted for the structures.

For the single-tip structure with a tip length of 1 μm, a tip base of 200 nm, a metal thickness of 60 nm, and an undercut of 100 nm, the simulated field enhancement factor was 1.189 and the capacitance was 15 aF.

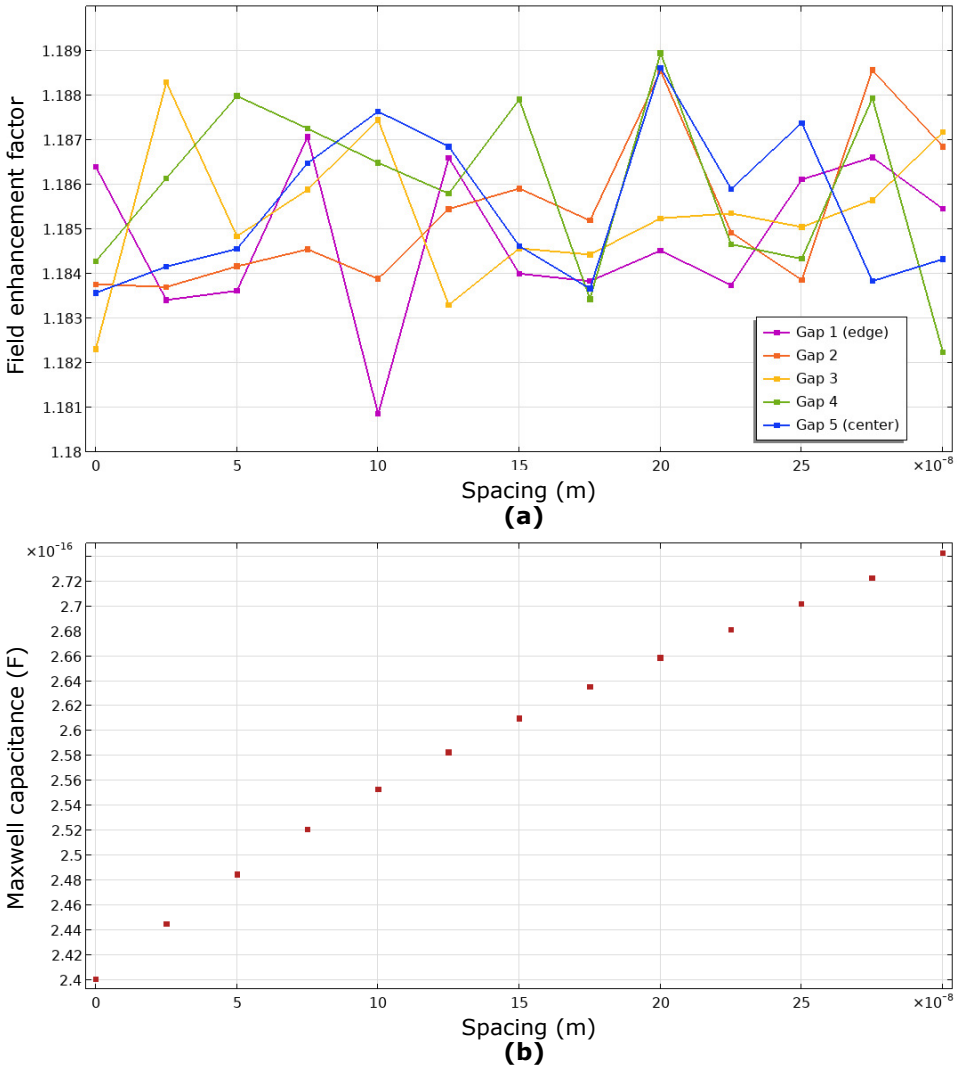

Figure 4.9: Multi-tip simulation results: (a) field enhancement factor and (b) Maxwell capacitance as a function of tip spacing.

To study the effect of shielding due to closely spaced emitters, an array of 10 tips with varying separation between them, i.e., period, was modeled. The connecting terminal for the sweep had a constant size so a larger period did not mean that the connecting terminal became wider. The results are given in Fig. 4.9. The field enhancement factor was plotted for the top half of the tips as it was expected that the same results would be obtained for the bottom half due to symmetry. The numbering in the legend is in order. In this way, “gap 1” corresponds to the tip at the edge of the array (only has one neighbour), and “gap 5” corresponds to the tip at the center of the array. It was observed that there was no effect of changing the spacing on the field enhancement factor, so shielding at these dimensions does not seem to be an

issue. The capacitance increased when the spacing was increased. Therefore, no spacing between the tips returned a capacitance of 24 aF/tip for a multi-tip device.

4.4 Device Fabrication

The fabrication steps for the field emission multi-tip arrays are illustrated in Fig. 4.10. The devices were fabricated on 1.3 mm square chips that were diced from a 500 μm-thick JGS2 fused silica wafer. The chips were first cleaned using acetone and IPA, as they had been previously coated with resist for protection during dicing. To remove any leftover organics, a 20-minute-long oxygen plasma clean was performed at 80 Watts and 20 mTorr using RIE (Plasma-Therm SLR 720).

Next, the devices were coated with a 25 nm layer of Cr, which was deposited using electron beam evaporation at a rate of 0.5 Å/s and a base pressure of $\sim 10^{-7}$ Torr (CHA Industries Mark 40). The purpose of this thin metal layer was twofold. Due to the highly insulating nature of glass, a charge dissipation layer was needed for subsequent EBL. In addition, glass is transparent to the laser wavelength used during EBL height measurement. An inaccurate substrate height measurement can lead to a defocused beam at the top of the chip surface, which is detrimental to high-resolution patterning. Therefore, the metal layer also provided sufficient reflectivity for the height check.

The devices were patterned using standard EBL. A pre spin-coating clean using acetone and IPA was performed immediately before spin-coating the substrate. 950 PMMA A4 (MicroChem) at 4000 rpm for 45 s was used, and the sample was baked at 180 °C for 4 minutes. Direct-write EBL (Raith EBPG 5200) was carried out at an acceleration voltage of 100 keV. To achieve high-resolution and optimal pattern transfer, proximity effect correction (PEC) with Genisys Beamer software and the "bulk & sleeve" technique were used. This technique consists of using a lower current beam to write the boundary of the features (i.e., the sleeve) and a larger current beam to write the center of the pattern (i.e., the bulk). A current of 20 nA (300 μm aperture) was used for the sleeve and a current of 200 nA (400 μm aperture) was used for the bulk, with a dose of 900 $\mu C/cm^2$ for both. In addition, the emitter tips were patterned with a dose of 675 $\mu C/cm^2$ and a current of 500 pA (300 μm aperture). The sample was developed for 60 s in a 1:3 solution of MIBK and IPA at room temperature, followed by a 20 s IPA bath as a stopper. The sample was constantly agitated in the developing solution to aid with the process.

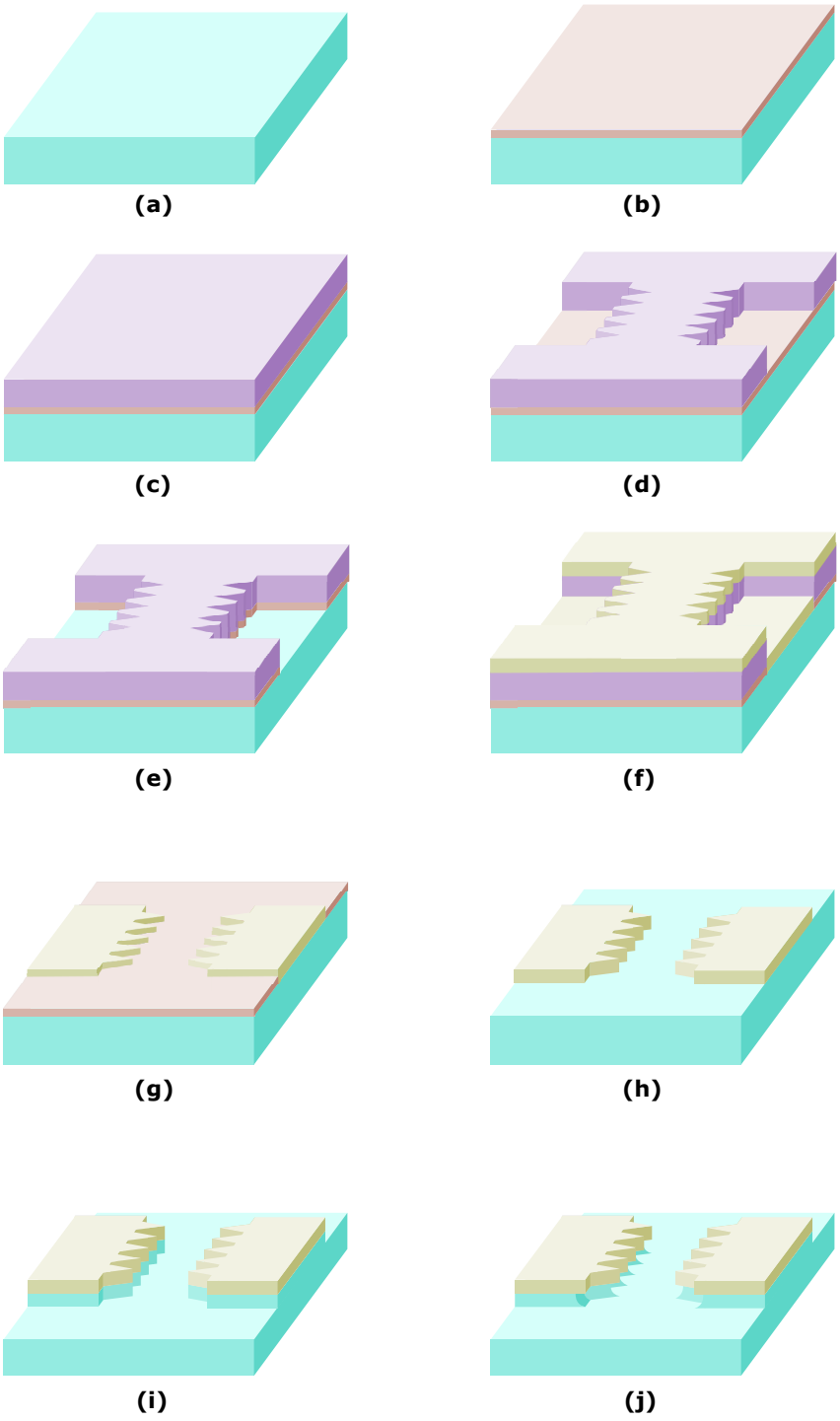

Figure 4.10: General fabrication steps for field emitter multi-tip array: (a) initial fused silica substrate, (b) evaporation of 25 nm Cr, (c) spin-coating of 200 nm 950 PMMA A4 electron beam resist, (d) EBL and development, (e) Cr etch, (f) evaporation of 6 nm Ti, 60 nm Au, and 20 nm Ti, (g) lift-off, (h) residual Cr removal, (i) dry etching, and (j) wet etching in BHF. Note that the sketch is not to scale.

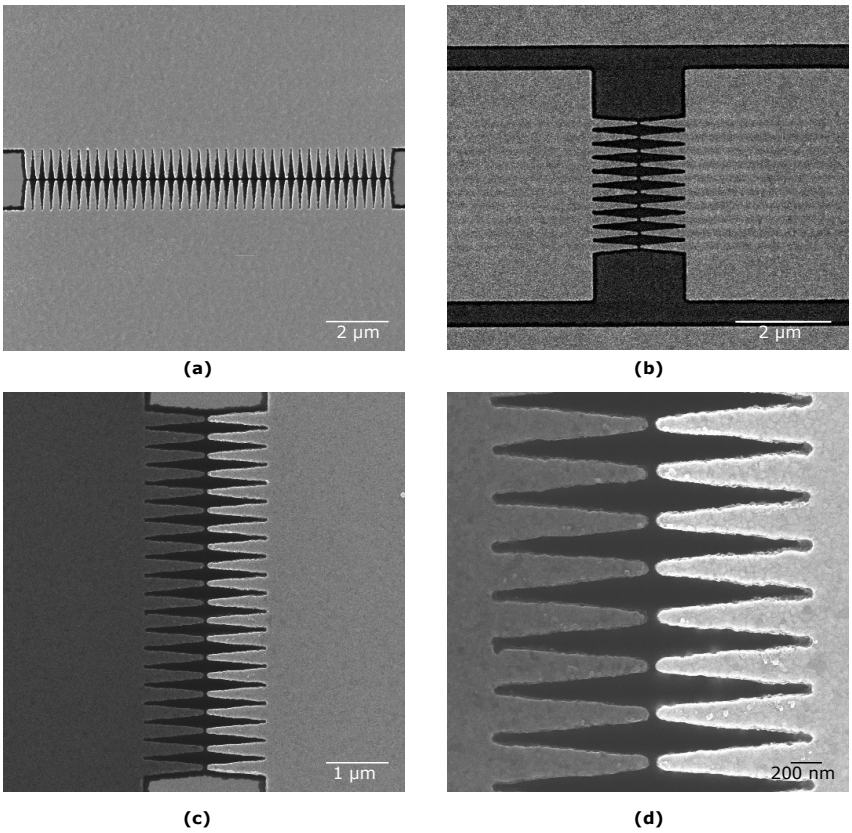

Figure 4.11: Images of representative devices after lift-off. (a) HIM of a device with 40 tips. (b) SEM of a device with 10 tips and ground planes in the vicinity. (c) and (d) are HIM of a device with 20 tips (same device). Voltage contrast arises due to the difference in surface potential between both tips once they were separated.

Next, the Cr over the exposed pattern was removed using Cr-7s (Cyantek). A 6 nm adhesion layer of Ti (rate of 1 Å/s), a 60 nm electrode layer of Au (rate of 1 Å/s), and a 20 nm etch mask layer of Ti (rate of 1 Å/s) were deposited using electron beam evaporation at a pressure of $\sim 10^{-8}$ Torr (Kurt J. Lesker Labline). Ti was chosen as an etch mask due to the limited evaporation sources available in the chamber. The sample was left in acetone overnight for the lift-off process, which was aided by sonication. A lift-off process was chosen for ease of fabrication and to help form sharp tips. Fig. 4.11 shows images of the devices after lift-off.

All the leftover Cr that remained under the now-removed resist was etched away in Cr-7s. The next step of the fabrication process was to remove the substrate material in the area surrounding the emission sites. To help the hydrofluoric acid (HF) in undercutting the structures, a dry etch was first used to increase the exposed surface area. A C_4F_8/O_2 etch chemistry at a ratio of 40 sccm/3 sccm, a substrate temperature

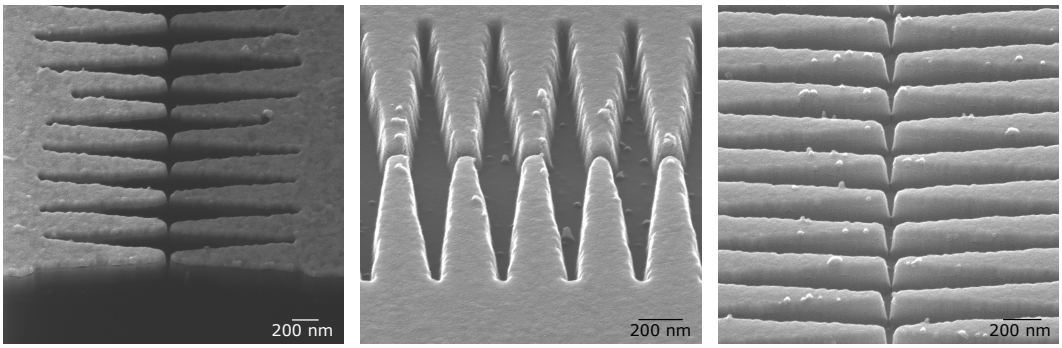

Figure 4.12: HIMs of representative devices after dry etch: (a) 45 s etch (DC bias: 186 V) for a depth of ~200 nm (image at 50° tilt), and (b) and (c) 40 s etch (DC bias: 206 V) for a depth of ~120 nm (images at 52° tilt).

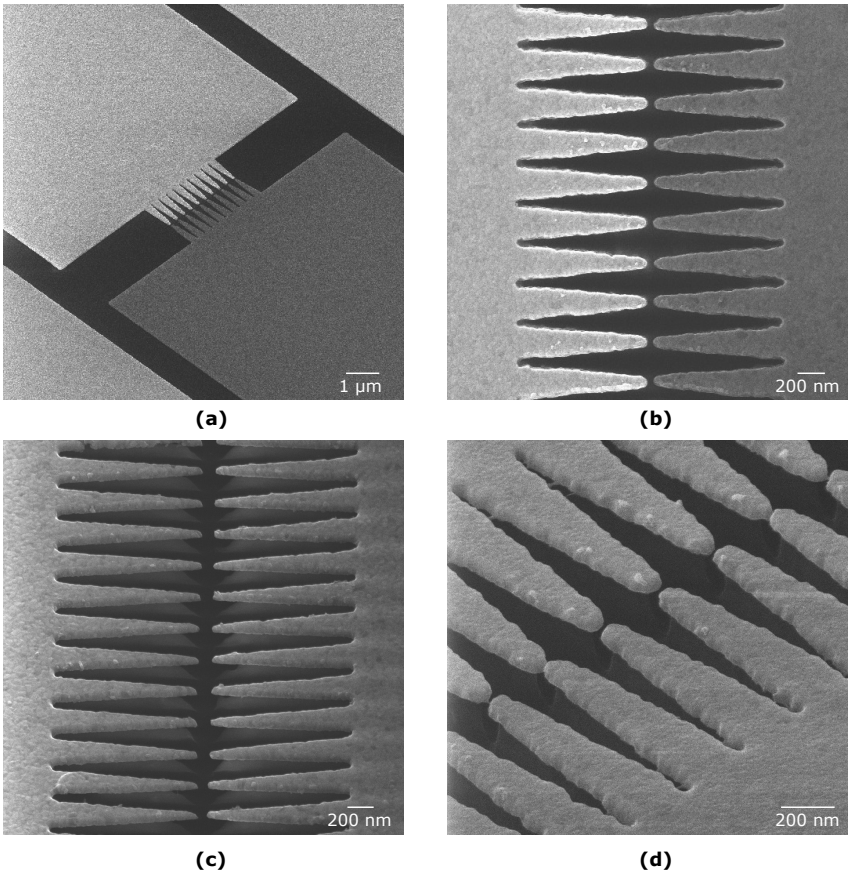

Figure 4.13: HIMs of a finished field emission multi-tip arrays. (a) device with ground planes at 45° tilt and rotation; (b) device as seen at 0° tilt and (c) at 45° tilt. The undercut measured in average 130 nm in depth. (d) Image at 52° tilt and rotation. On average, the gaps between the two terminals measured 30 nm.

of 20 °C, and a chamber pressure of 7 mTorr were used to perform the etch (Oxford Instruments Plasmalab System 100 ICP-RIE 380). The CCP power was set to 200 Watts and the ICP power to 2100 Watts. Fig. 4.12 shows helium ion micrographs (HIMs) of various devices after the dry etch step.

After the dry etch step, the sample was undercut using buffered hydrofluoric acid (BHF) (Transene Company, Inc.) for 20 s. To prevent bubble formation during the wet etch that leads to a non-uniform undercut, the sample was first dipped into a mixture of Triton 100X (Sigma-Aldrich) and water. The surfactant also helped BHF reach the very small gaps between the emitter and collector tips for a more reproducible etch. To avoid damage from surface tension, the devices were gently dried using a critical point dryer (Tousimis 915B). Fig. 4.13 shows HIMs of the final undercut devices. The distance between the emitter and collector varied between tips, ranging from 20 nm to 40 nm, with an average vacuum gap of 30 nm. Fig. 4.14 also shows devices with asymmetric geometry. Note that the fabrication throughput was lower for these devices compared to the symmetric devices, as lift-off became

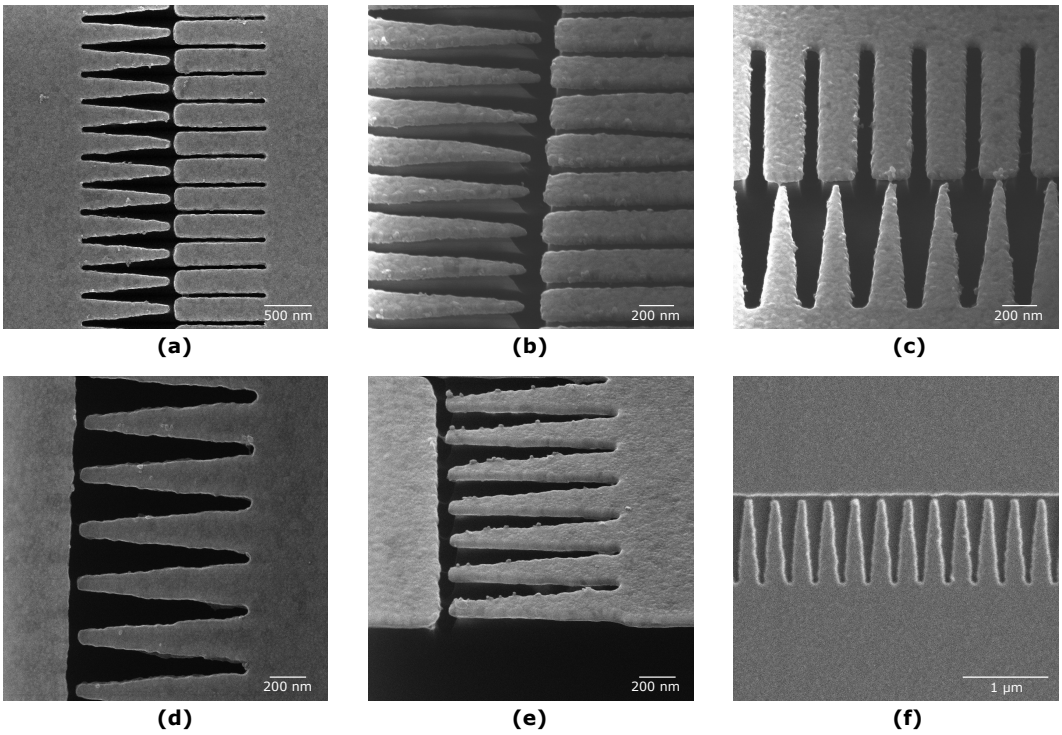

Figure 4.14: Images of asymmetric devices. HIM of finished device with a blunt multi-finger collector structure at (a) 0° tilt, and at (b) and (c) 45° tilt. HIM of a finished device with a block collector design at (d) 0° tilt and at (e) 52° tilt. (e) is a less-magnified SEM of the device after lift-off.

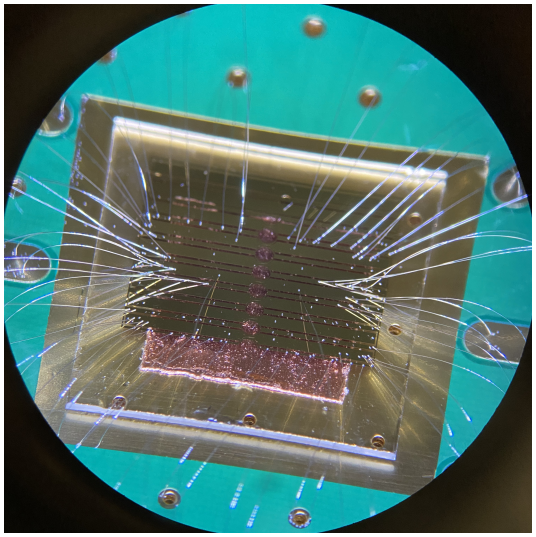

Figure 4.15: Chip wire-bonded to signal lines and ground plane of custom PCB.

more challenging with the denser structure. The average distance between the two terminals for both structures was around 40 nm.

Lastly, the devices were ultrasonically wedge wire-bonded with aluminum wires to the gold pads of a custom-designed printed circuit board (PCB), as shown in Fig. 4.15. The PCB design is discussed in the following section.

4.5 PCB Design

The through-hole PCB was designed using EAGLE software (Autodesk). It consisted of three coplanar waveguides with a ground reference plane that route from

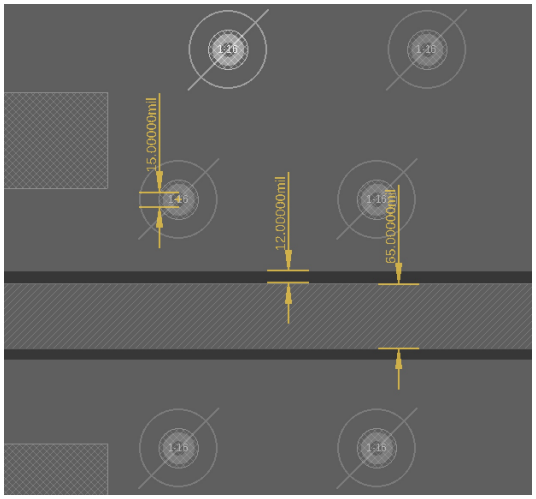

Figure 4.16: Relevant PCB design dimensions.

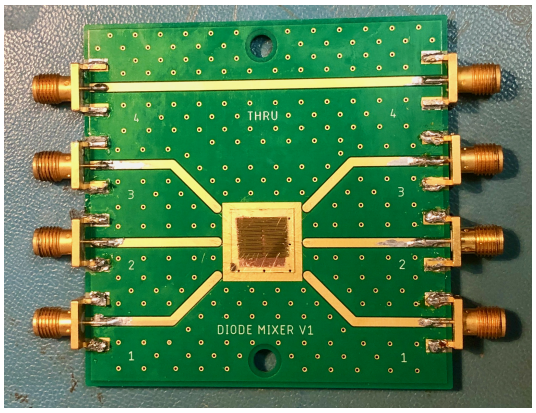

Figure 4.17: Photo of PCB with soldered SMA edge connectors and wire-bonded chip.

SMA edge connectors to a ground pad where the device was attached using double-sided copper tape. The dimensions for the signal trace width, spacing between the return ground, and via diameter are shown in Fig. 4.16. These were optimized for 50 Ω impedance matching. Only three signal traces were included on the PCB due to size limitations inside the testing chamber. The stitching vias were designed to be spaced no more than 1/8th of the maximum testing wavelength from each other. For a maximum frequency of 3 GHz, or a maximum wavelength of 100 mm, the vias were separated by a maximum of 12.5 mm. In addition, a through transmission line for PCB calibration was included.

Tg 170 FR-4 was selected as the dielectric material, with a dielectric constant of ~4.3 and a thickness of 1.6 mm. While FR-4 is not usually the material of choice for high-frequency measurements due to its high losses, it should still perform well up to frequencies below 5 GHz [16]. The copper thickness was 1 oz. and the surface finish was electroless nickel immersion gold (ENIG) with a thickness of 2U". Fig. 4.17 shows a photo of the final PCB with the soldered SMA edge connectors and wire-bonded chip.

The S-parameters were measured using a vector network analyzer (Keysight P9372A) and the real impedance was calculated. The results are shown in Fig. 4.18.

4.6 DC and AC Measurements

The PCB with the wire-bonded chip was loaded into a custom stainless-steel vacuum chamber to prevent contamination that could affect emission stability. The chamber was pumped to a pressure of $\sim 10^{-6}$ Torr. The PCB was connected to a custom-made

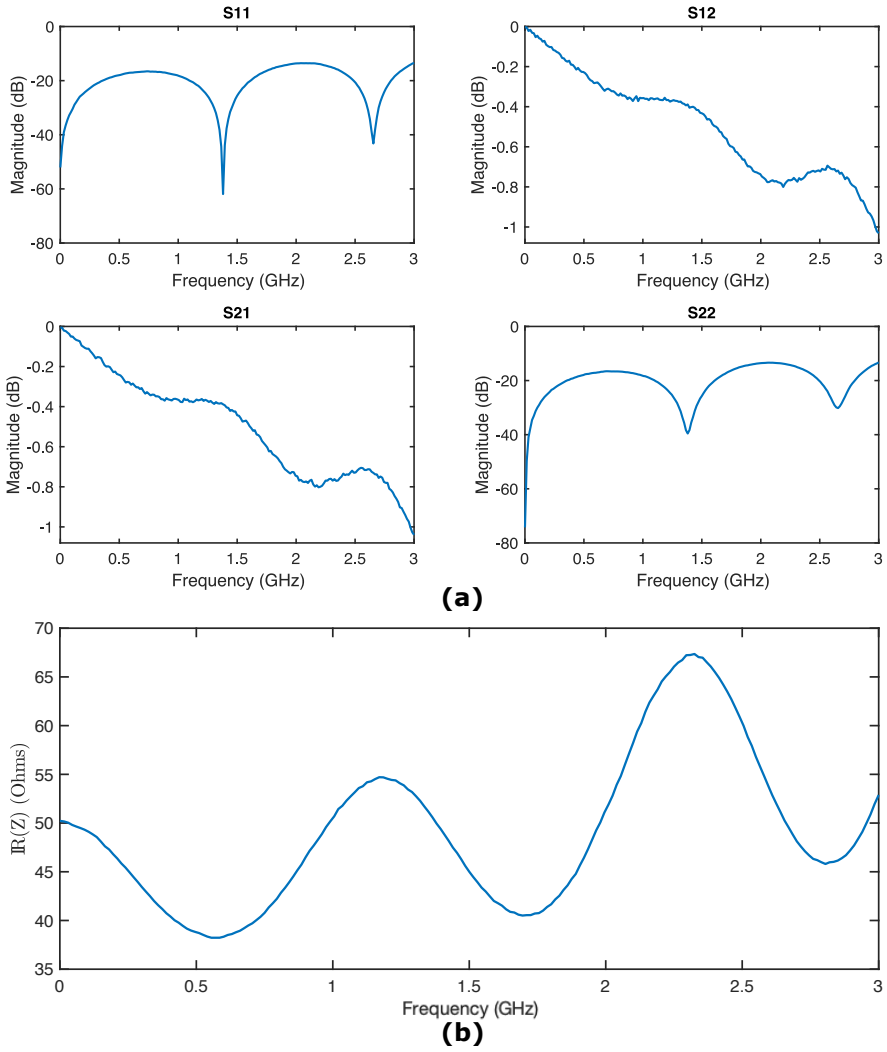

Figure 4.18: PCB experimental data: (a) S-parameters and (b) calculated real impedance using S11.

electrical feed-through using Kapton-insulated UHV coaxial cables (Accu-Glass Products Inc. 110755). The electrical feed-through was built using a blank KF flange with holes drilled into it to fit hermetically-sealed RF adapters (Pasternack PE9184). Fig. 4.19 shows the custom-built feed-through for frequency measurements up to 18 GHz.

The DC voltage needed to bias the field emission tips was provided by two picoammeter/voltage sources (Keithley 6487), which also monitored the emission current independently at each terminal to check that all currents were accounted for and that there were no significant leakages. Two independent AC voltages for the high-frequency measurements were supplied by function generators (Keysight N5171B

Figure 4.19: Custom-built electrical feed-through for frequency measurements up to 18 GHz.

and Rohde & Schwarz SMC100A), which have a maximum frequency of operation of 3 GHz. These two sources were coupled using a power combiner (Mini-Circuits ZAPD-30-S+), which also provided isolation between them. A bias tee (Mini-Circuits ZFBT- 4R2GW-FT+) was used to insert both DC and AC power into the device, while another identical bias tee was employed to deconvolute the two signals at the output. Lastly, the output AC signal was measured using a digital phosphor oscilloscope (Tektronix DPO7254). All AC components were connected using 50 Ω coaxial cables. The DC sourcemeters were controlled via GPIB interface and data acquisition was automated using MATLAB scripts. Control of the AC equipment

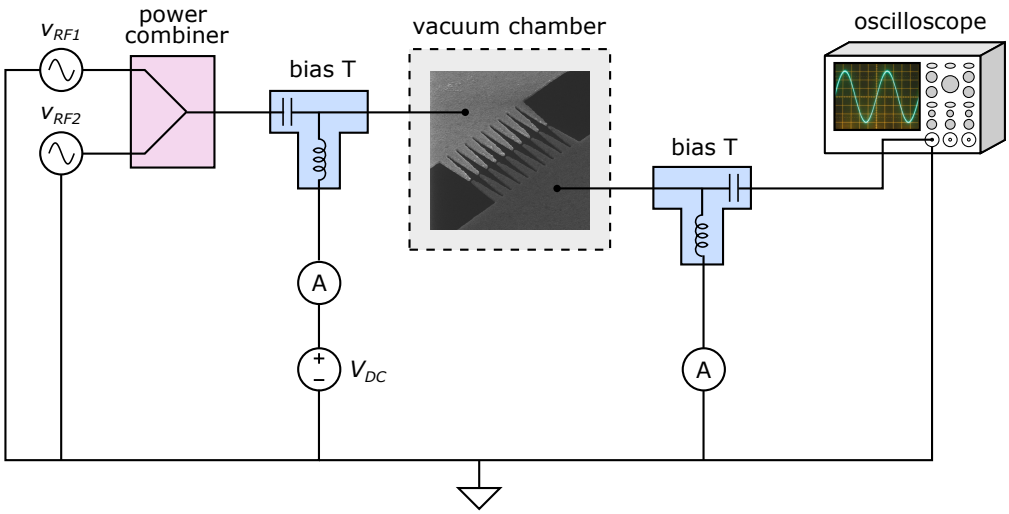

Figure 4.20: Schematic diagram of the test circuitry.

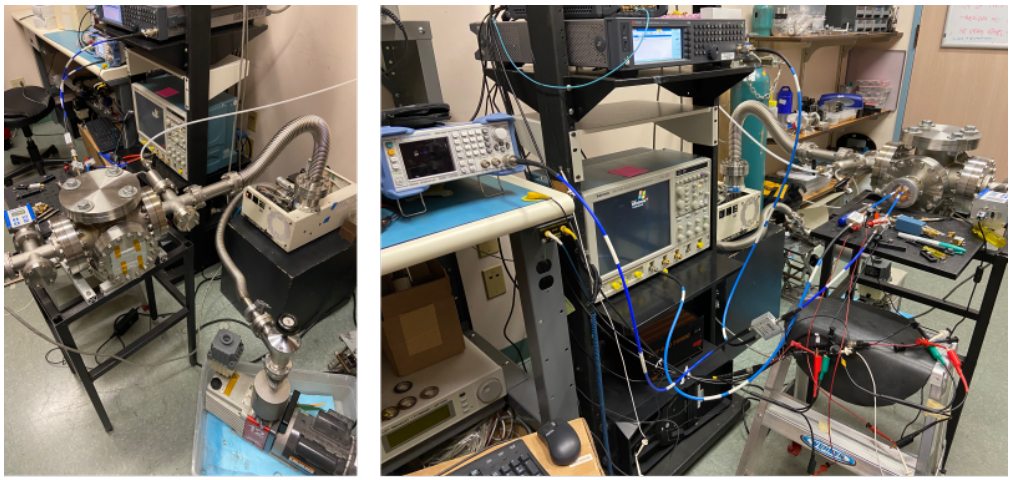

Figure 4.21: Photos of the experimental setup: (a) vacuum chamber (front view) and (b) electrical connections (back view).

including signal generators and oscilloscope was done manually. A schematic of the equivalent circuit of the measurement system is provided in Fig. 4.20, and photos of the experimental setup are shown in Fig. 4.21.

Examination of electron emission to confirm that the conduction mechanism was FN emission and not an alternative process was initially carried out. The DC power supplies were connected and the AC lines were shorted, followed by a conditioning process identical to that of the previous chapter, for which multiple IV sweeps were taken until there was no discernible change between consecutive runs. No resistor in series with the emitter for protection was added to this experimental setup, as it would significantly limit high-frequency modulation.

The effect of geometry on the emission process was first studied to determine whether an asymmetric structure could recreate the IV characteristic profile of existing solid-state diodes for rectification. Two designs for the collector terminal, a blunt multi-finger structure and a block structure, were considered. Despite the slightly smaller capacitance of the first design, the second structure was also taken into account due to its higher fabrication throughput. For these measurements, the bias on the emitter terminal was kept at 0 V, while the voltage on the collector terminal was swept. Positive voltages induced emission from the emitter and negative voltages promoted emission from the collector.

Fig. 4.22 shows the output IV characteristics of both asymmetric devices, with a representative SEM of the design considered included on the top left corner of each

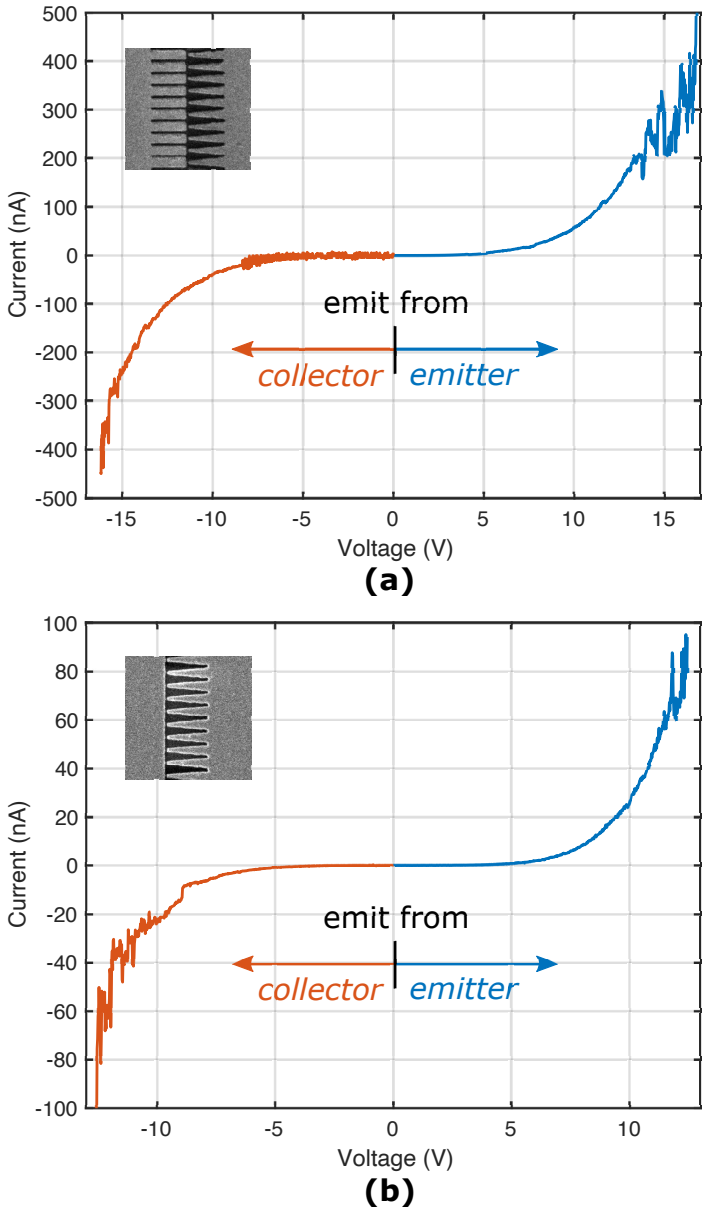

Figure 4.22: IV curves for both asymmetric designs considered: (a) blunt multi-finger collector structure and (b) block collector structure.

sub-figure. Unfortunately, the curves for the forward and backward sweeps had the same turn-on voltage, which was likely due to nanoprotrusions that formed on the surface of the collector terminal, dominating emission at the nanoscale and rendering any macroscopic geometry ineffective. In light of these results, we decided to focus on symmetric structures from here on out.

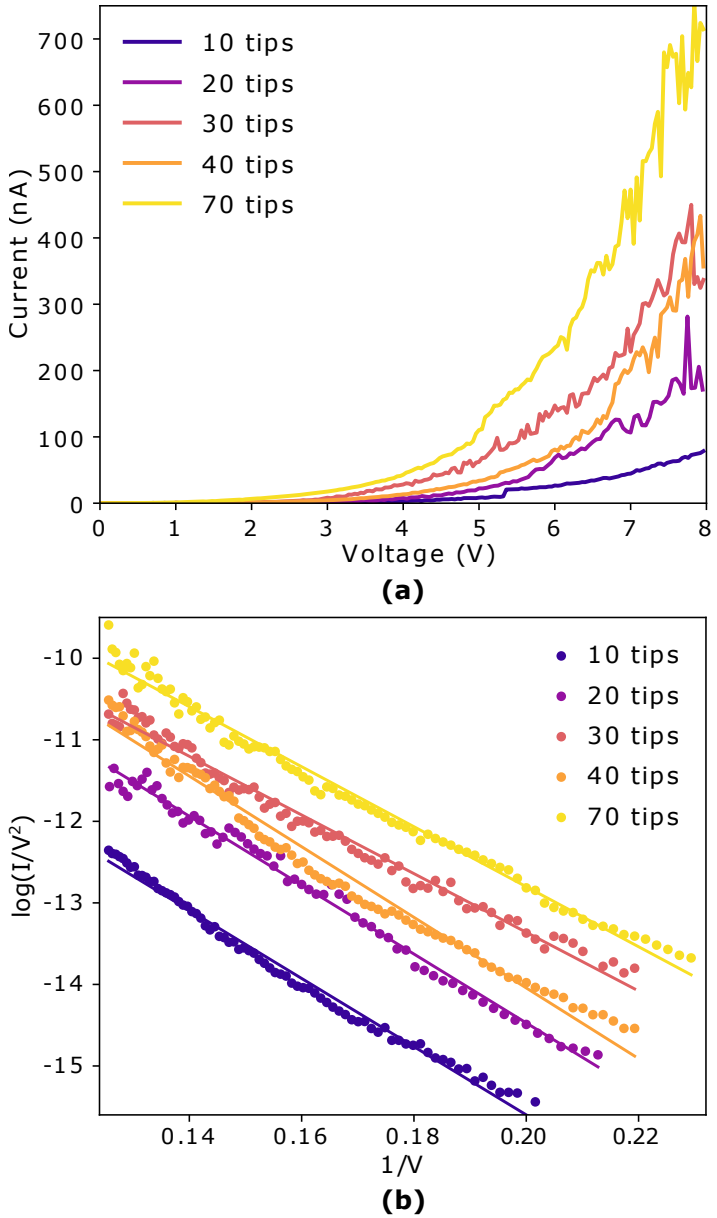

Figure 4.23: Electrical characterization as a function of the number of tips per device: (a) IV characteristics and (b) FN plot.

The effect of the number of field emission tips on the measured current was examined. Fig. 4.23 displays the experimental result for electron emission as a function of the number of tips per device. Unfortunately, the devices with 50 and 60 tips blew up early on during testing so no useful data could be acquired. Also, a maximum current of 100 nA per tip was deliberately imposed to prevent overheating and potential damage. It was shown that, at a given applied bias, the measured current increased as a function of the number of emitter tips. Therefore, by increasing the number of

Number of tips	Slope	y-intercept	Number of tips (effective)	R^2 value
10	-41.82	-7.235	10	0.989
20	-42.24	-6.023	33	0.990
30	-35.97	-6.166	29	0.985
40	-43.30	-5.383	63	0.981
70	-37.27	-5.370	64	0.988

Table 4.1: Linear regression analysis data as a function of number of tips.

tips per emitter, the turn-on voltage for electron emission was successfully lowered, which is beneficial in terms of power consumption and lifetime considerations.

In addition, data was plotted using FN coordinates, as illustrated in Fig. 4.23 (b). Currents lower than 10% of the maximum measured current were ignored, as these are usually associated with other types of emission such as FP leakage [17], unaccounted resistance paths [18], or Schottky emission [19]. A linear model was well fit to the measured data, affirming FN emission process. As the multi-tip array is equivalent to having many individual emitters in parallel, the overall FN current for the multi-tip array, I_{MT}, can be expressed in terms of a single-tip emitter current, I_{ST}, as

$$\begin{aligned} I_{MT} &= nAV^2 \exp\left(-B/V\right) \\ &\equiv nI_{ST} \end{aligned} \tag{4.12}$$

where n is the number of emitter tips, and A and B are constants that depend on, among others, the emission area, field enhancement factor, and work function. In FN coordinates this becomes

$$\ln\left(\frac{I_{MT}}{V^2}\right) = \ln\left(nA\right) - B\left(\frac{1}{V}\right). \tag{4.13}$$

Roughly the same slope was obtained from the linearization of the measured data for all devices. This agrees with Eqn. (4.13), as the slope is independent of the number of emitter tips. Furthermore, the magnitude of the y-intercept decreased as the number of emitter tips per device increased, also in agreement with Eqn. 4.13, as the vertical intercept of a multi-tip device changes by a fixed amount given by $\ln\left(n\right)$ compared to single-tip emission. Using the y-intercept value of the 10-tip device, the efficient number of emitter tips was calculated and presented

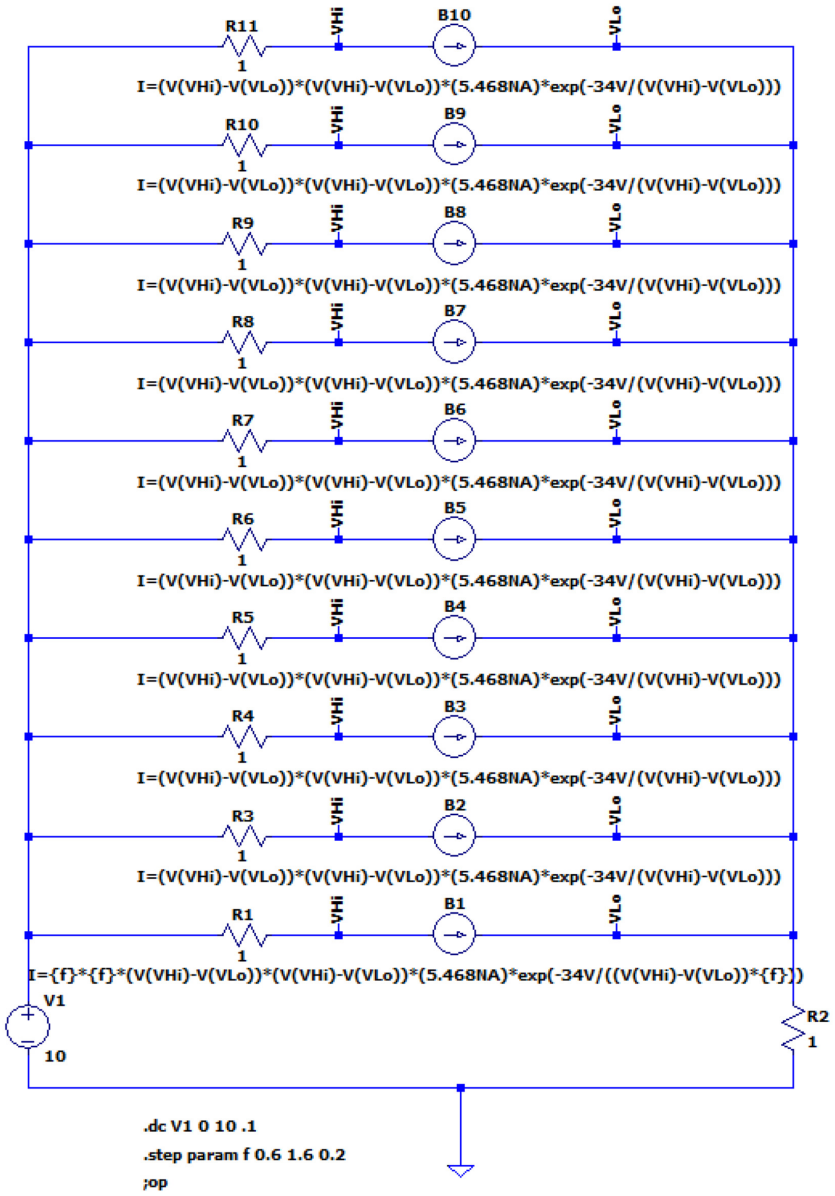

Figure 4.24: SPICE schematic for a 10 tip device.

in Table 4.1, alongside the values for the slope, y-intercept, and R^2 of the least squares regression line. A smaller value of effective emitter tips was expected due to fabrication discrepancies between gaps of individual tips, which ultimately cause only a fraction of the fabricated tips per device to turn on at a given bias. However, a higher effective number of tips than the actual number of tips was observed for some devices. Note that the analysis in Eq. (4.12) assumed an equal field enhancement factor for all tips. While this may seem an oversimplification, due to the highly sensitive dependence of field emission on the atomic structure of

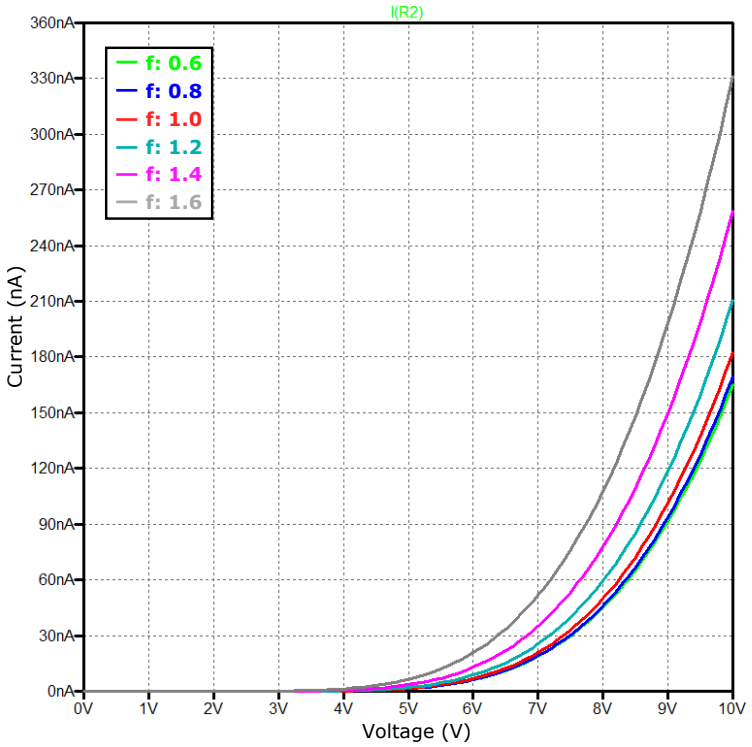

Figure 4.25: Result of SPICE simulation illustrating effect of fractional change in field enhancement factor for a single tip within an array in measured total current.

the emitter tip, it is hard-if not impossible-to achieve controllable field enhancement [20]. In this way, the devices with a larger effective number of tips probably had a higher field enhancement factor as a result of any local nanoprotrusions created during fabrication. Figs. 4.24 and 4.25 show a SPICE schematic and simulation result (LTspice XVII, Analog Devices Inc.) portraying the effect of fractional change in field enhancement factor for a tip within a 10-tip device with the representative field emission tip modeled as a voltage-controlled current source. The parameters in the emission current equation were obtained by curve fitting to data from an early device using MATLAB. A 1 Ω resistor was placed in series before each tip to account for their inherently small resistance. The simulation results concluded that the total emission current of a multi-tip device can be dominated by a single emitter tip with a higher field enhancement factor, which is problematic as tips with higher field enhancements can easily blow up. It also increases noise in the measurements, which is troublesome for some applications such as amplification.

Lastly, for the frequency mixing experiments, the AC lines were connected as illustrated in Figs. 4.20 and 4.21. Before any AC power was coupled in, a static analysis was performed on the device under test to confirm the FN emission process

and determine the dynamic resistance of the device at the current level that would be sourced. Fig. 4.26 shows the IV curve, corresponding FN plot, and dynamic conductance right before the AC tests were carried out for a 10-tip device. The dynamic conductance as a function of voltage was calculated by differentiating the IV curve. From (c), a dynamic impedance of $R = 0.67$ MΩ was calculated. Recalling the simulated capacitance of C =24 aF/tip, an RC cutoff frequency, f_c, given by [21]

$$f_c = \frac{1}{2\pi RC} \tag{4.14}$$

of ∼1 GHz was estimated.

Once an estimate for the cutoff frequency of the specific device under test was calculated, we proceeded with the mixing experiments as follows. The DC bias was

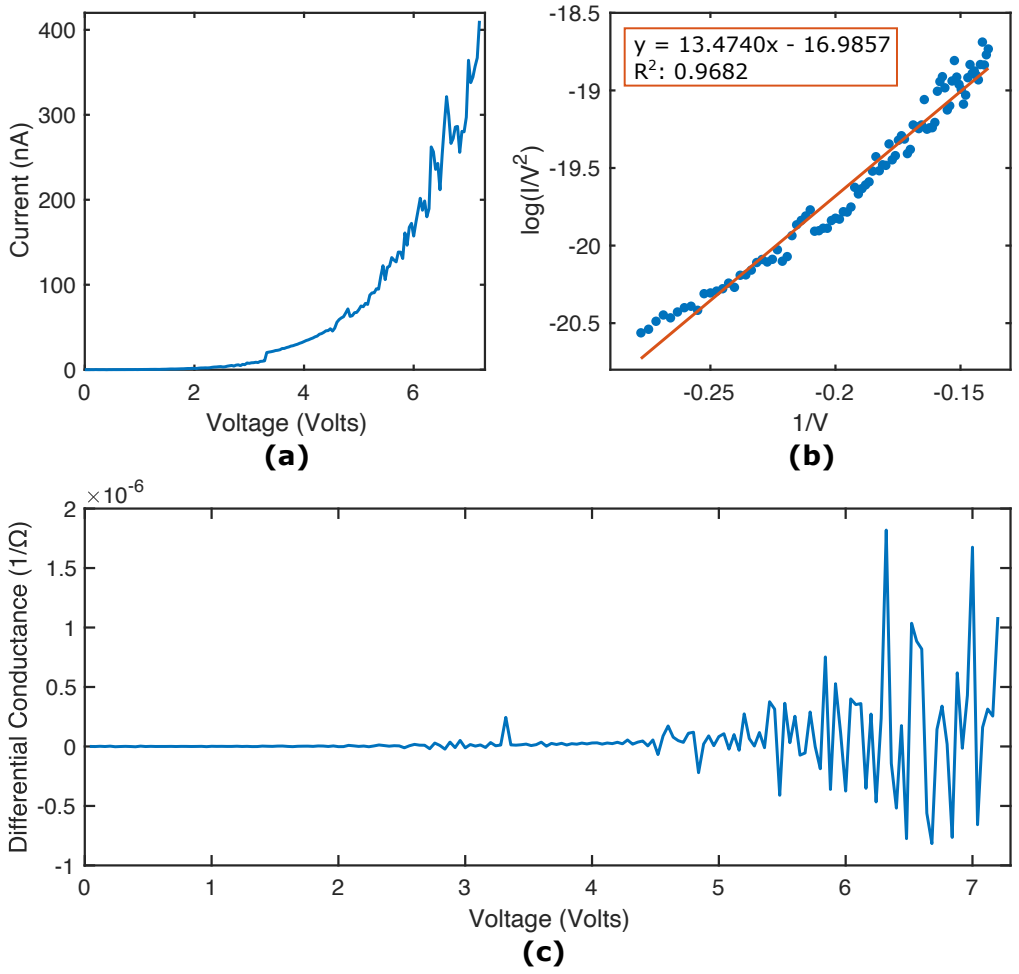

Figure 4.26: Electrical measurements before frequency mixing experiment: (a) static characteristic, (b) corresponding FN plot, and (c) differential conductance.

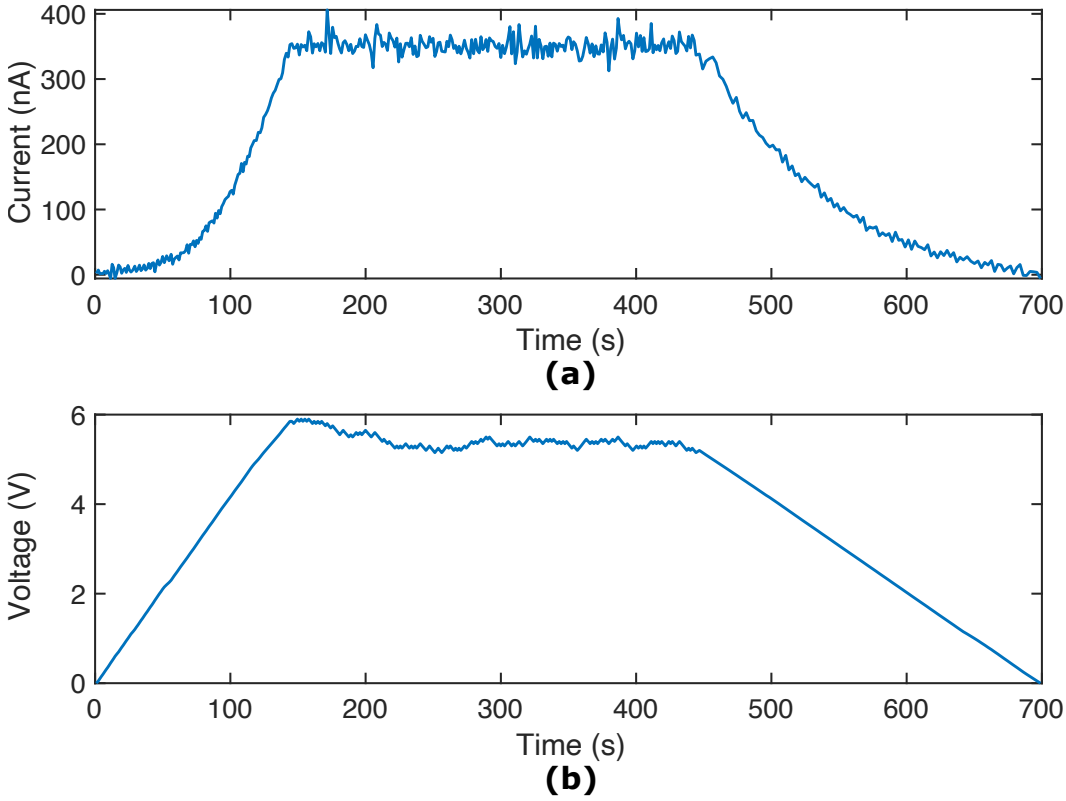

Figure 4.27: DC bias feedback loop to stabilize emission current for frequency mixing measurements: (a) shows the DC current as a function of experiment duration, and (b) illustrates how the voltage was adjusted to maintain the current constant at some chosen level.

	Fig. 4.28 (a)		**Fig. 4.28 (b)**		**Fig. 4.28 (c)**	
Label	**Frequency (MHz)**	**Power (dBm)**	**Frequency (MHz)**	**Power (dBm)**	**Frequency (MHz)**	**Power (dBm)**
f_1	35	-79.6	35	-79.5	30	-80.9
f_2	50	-75.1	45	-76.5	35	-79.6
$f_1 + f_2$	85	-95.1	80	-99.1	65	-115.3
$\|f_1 - f_2\|$	15	-97.9	10	-98.0	5	-110.7
$2f_1$	70	-103.0	70	-102.4	60	-108.0
$2f_2$	-	-	90	-103.5	70	-111.4
$2f_1 - f_2$	20	-113.9	25	-101.6	25	-109.6
$2f_2 - f_1$	65	-98.5	55	-102.5	40	-124.2

Table 4.2: Measured power for all frequencies of interest shown in Fig. 4.28.

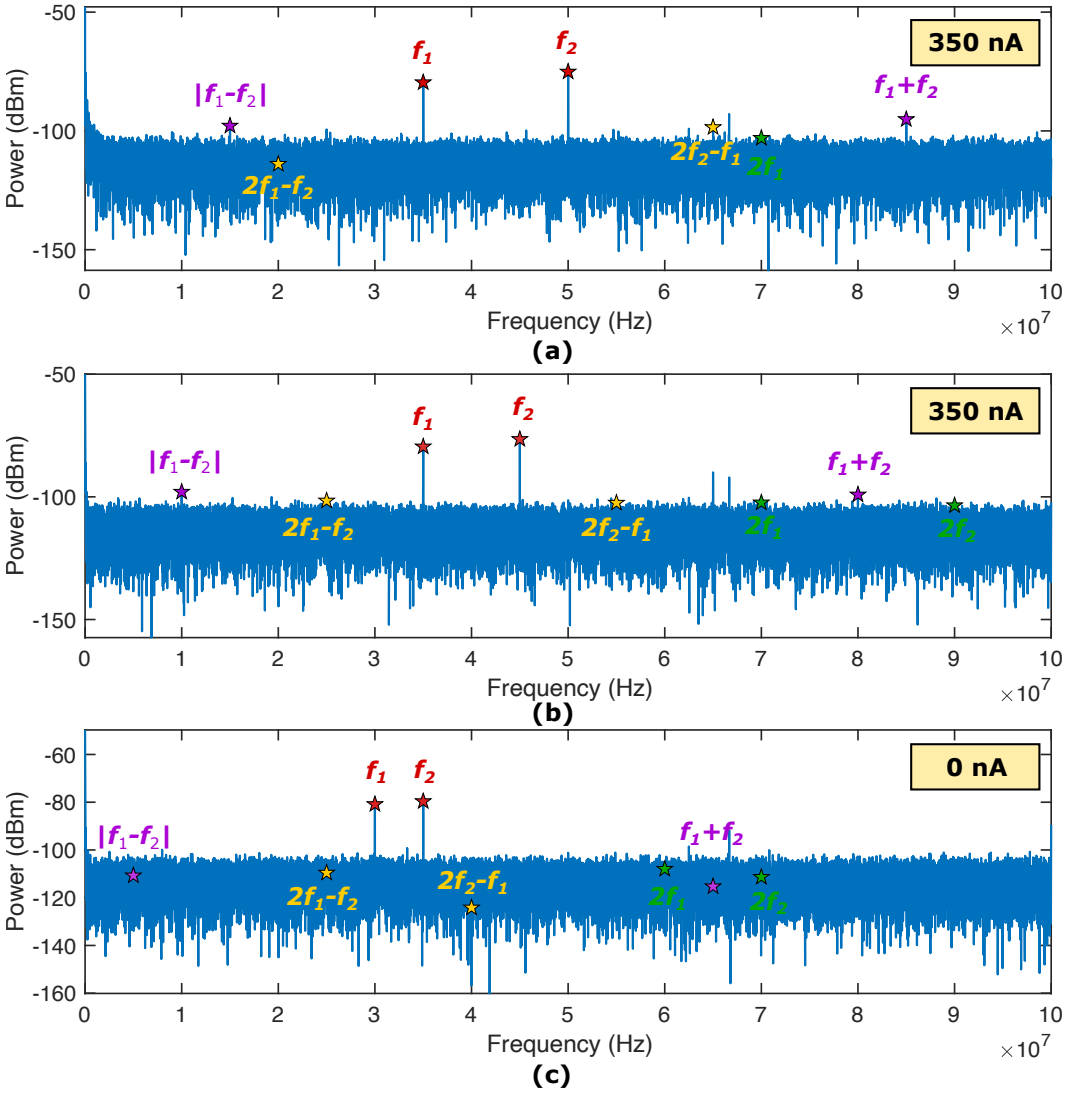

Figure 4.28: Power spectra of the output signal. Each AC signal has an amplitude of 1 V_{RMS}. (a) f_1 = 35 MHz and f_2 = 50 MHz with 350 nA DC current, (b) f_1 = 35 MHz and f_2 = 45 MHz with 350 nA DC current, and (c) f_1 = 30 MHz and f_2 = 35 MHz when the device is 'off' (0 nA).

gradually increased up to a set current level of 350 nA, at which the current was kept constant for a specified time interval. A feedback loop was created, in which the voltage was automatically modified if the measured current dropped or increased from the specified value, due to possible emission instabilities. Fig. 4.27 portrays both the measured current and automatically set voltage as a function of time. With the current stable at the set value, two AC signals with an amplitude of 1 V_{RMS} at frequencies f_1 = 35 MHz and f_2 = 50 MHz were applied. Fig. 4.28 (a) shows the power spectrum obtained by computing the Fast Fourier Transform (FFT) with the

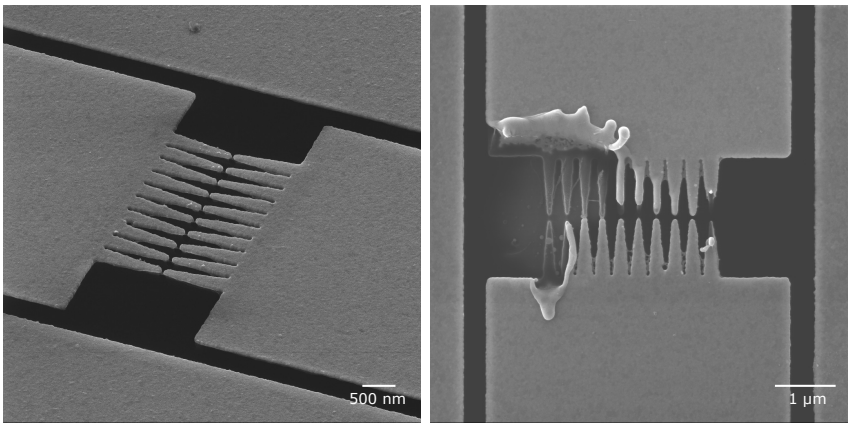

Figure 4.29: HIM (a) before and (b) after testing.

oscilloscope. Power values at all frequencies of interest are included in Table 4.2. We observed peaks at the sum ($f_1 + f_2 = 85$ MHz) and difference ($|f_1 - f_2| = 15$ MHz) frequencies, confirming that the field emitter array successfully achieved frequency mixing. The conversion loss, due to the high impedance of the device, was about 108 dBm. However, this value only serves as a worst-case scenario as the input signal frequencies were not matched to the device. Therefore, significantly better results are expected if impedance matching is attempted. Moreover, due to the considerable loss, neither harmonics nor third-order terms could not be measured. We also changed the input frequencies to $f_1 = 35$ MHz and $f_2 = 45$ MHz and measured similar results as illustrated in Fig. 4.28 (b). In addition, we confirmed that no peaks at the sum or difference were present when the device was 'off' (i.e., no DC bias was applied and no field emission current was measured), as exhibited in Fig. 4.28 (c). Lastly, we verified that no peaks at the input frequencies f_1 and f_2 were measured when the device was 'on' (i.e., DC bias was applied and field emission current was measured) but the AC sources were switched off.

After various experiments, the device ultimately blew up. Fig. 4.29 shows an HIM of the tested device before and after measurements were taken.

4.7 Work Function Reduction

There are various mechanisms by which the emission current can be increased, such as:

1. Increasing the bias voltage

2. Increasing the field enhancement factor
3. Increasing the emission area
4. Reducing the separation between the emitter and collector terminals
5. Reducing the emitter work function.

Increasing the potential can be problematic if the device is not under UHV, as electrons can ionize ambient gases and cause sputtering that can lead to device destruction. Additionally, this option is not ideal due to power consumption and device lifetime. Moreover, an increase in the field enhancement factor can cause overheating and device failure. In terms of emission area, in the previous section we described how fabricating multi-tip devices successfully led to an augmentation of the total emission current. Furthermore, despite our attempts to create the smallest vacuum gaps, fabrication constraints limited the separation between the emitter and collector terminals.

In this section, we explore the effect of lowering the emitter work function to increase field emission current. In particular, we present preliminary results of coating the emitter with Pr, which has a work function of 2.7 eV [22]. To our knowledge, improvements in field emission current using Pr have not been previously reported.

Let us examine the effect in the emission characteristics of reducing the emitter work function by a factor c ($c < 1$), so that the new work function ϕ_{new} can be expressed as $\phi_{new} = c\phi_{old}$, where ϕ_{old} is the original high work function. From the FN emission equation given in Eq. (2.47), the measured current is increased by

$$\frac{I_{new}}{I_{old}} = \frac{1}{c} \exp\left[-\frac{b_{FN}\phi^{3/2}}{F}\left(c^{3/2} - 1\right)\right] \tag{4.15}$$

where I_{new} is the current with the reduced work function ϕ_{new}, and I_{old} is the current with the original work function ϕ_{old}. Fig. 4.30 shows a SPICE simulation that illustrates the effect in emission current when the emitter work function is decreased by a factor c.

Furthermore, consider the following simplified version of Eq. 2.48 given by

$$\ln\left(\frac{I}{V^2}\right) = A\left(\frac{1}{V}\right) + B \tag{4.16}$$

where A and B are the slope and y-intercept, respectively. In terms of physical parameters, these are given by

$$A = -\frac{b_{FN}\phi^{3/2}}{\beta} \tag{4.17a}$$

$$B = \ln\left(\frac{a_{FN}S\beta^2}{\phi}\right). \tag{4.17b}$$

By reducing the emitter work function by a factor of c while keeping the field factor β fixed, the slope A is reduced by a factor $c^{3/2}$ while the y-intercept B is modified by $\ln(c)$. Thus, the new slope A_{new} and y-intercept B_{new} can be expressed by the original slope A_{old} and y-intercept B_{old} as

$$A_{new} = c^{3/2}A_{old} \tag{4.18a}$$

$$B_{new} = B_{old} - \ln(c). \tag{4.18b}$$

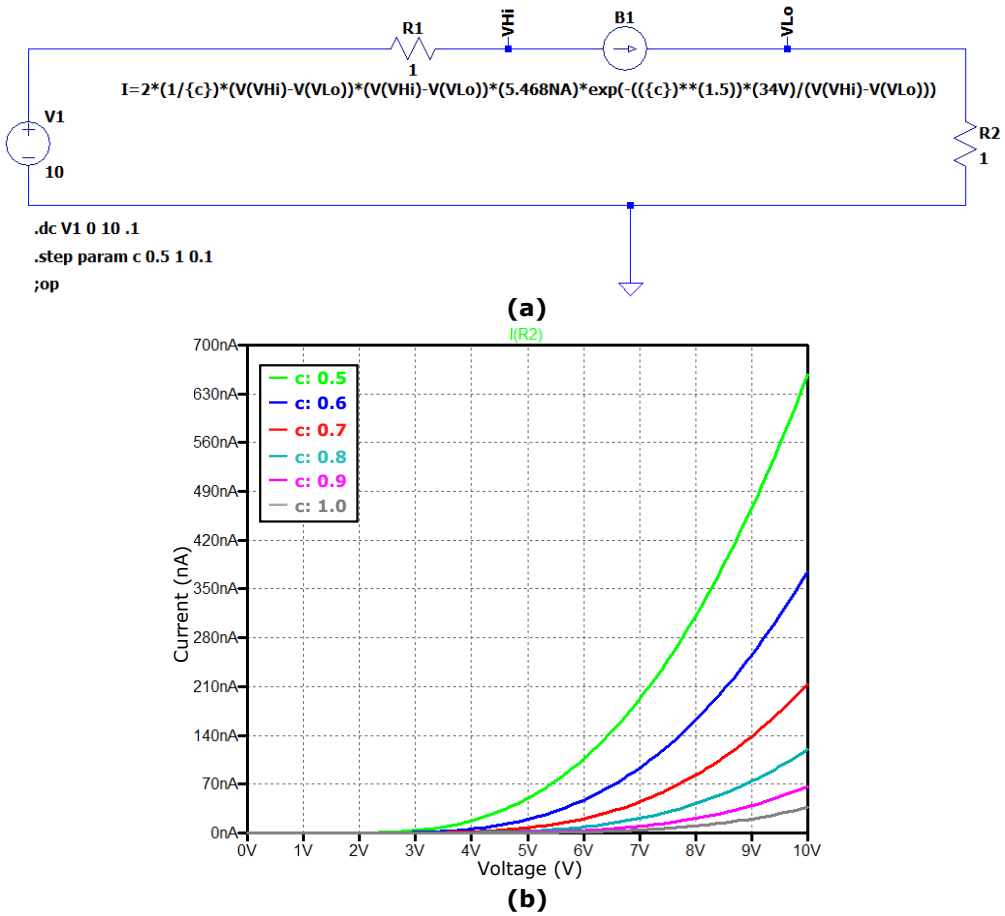

Figure 4.30: SPICE (a) circuit schematic and (b) IV characteristic simulation showing the effect of reducing the work function by a factor c.

For the experimental verification, the same device design employed in the frequency mixing experiments was used, so all fabrication steps are found in Section 4.4. The chip was ultrasonically wedge wire-bonded with aluminum wires to a ceramic pin grid array package (Spectrum Semiconductor Materials CPG15504).

A 10 nm-thick layer of Pr was deposited on the samples via thermal angle evaporation in a custom-built deposition chamber at a base pressure of 6×10^{-6} Torr. The angle of evaporation was about 45° with respect to the sample plane to achieve conformal coating of the emitter tip. To prevent oxidation or contamination that could modify Pr work function due to air exposure, a feedthrough with electrical connections for in situ measurements was added to the chamber. Two sourcemeters (Keithley 2450) measured the IV characteristic of the devices before and after Pr evaporation. Measurement acquisition was automated using serial communication and MATLAB scripts.

Fig. 4.31 (a) shows the IV characteristic of the non-coated and Pr-coated field emitter device. The Pr coating reduced the turn-on voltage, defined as the voltage required to measure a current of 10 nA, from 8.2 V to 4.3 V. This indicates that, for a given bias, the emission current is drastically increased by the Pr layer compared to the bare device. Fig. 4.31 (b) plots the measured data using FN coordinates along with the fitted least squares regression lines. After the Pr coating, the slope in the FN plot becomes significantly less steep. As the slope is related to the work function and the field factor, a decrease in the observed slope corresponds to either a reduction in

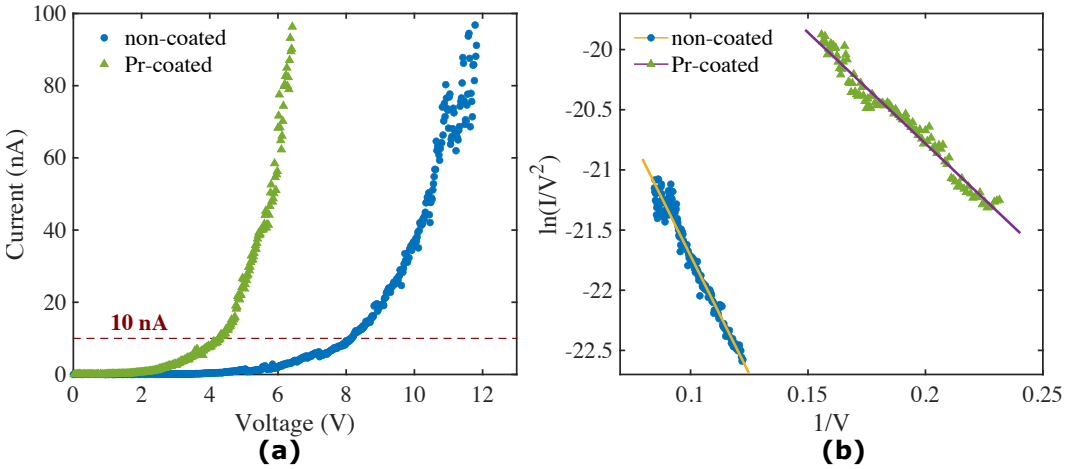

Figure 4.31: Effect of Pr coating in field emission: (a) IV characteristics of Pr coated and non-coated device and (b) FN plots. A dashed line at 10 nA is included in (a) to determine the turn-on voltage.

the effective work function, an increase in the field factor, or a combination of both. The values for the expected and measured slope, y-intercept, and R^2 value obtained from the regression lines fitted to the FN plot before and after the deposition of Pr on the sample are included in Table 4.3. From the ratio of the slopes, we infer the following experimentally measured $c_{m,A}$:

$$c_{m,A} = \left(\frac{A_{new}}{A_{old}}\right)^{\frac{2}{3}}. \tag{4.19}$$

Based on our experimental results, we obtain a value of $c_{m,A} = 0.605$, which is slightly larger than the expected $c_x = 0.509$ that was calculated using the work functions of pristine Au ($\phi_{Au} = 5.3$ eV) and Pr ($\phi_{Pr} = 2.7$ eV). However, if we consider the difference between the y-intercepts before and after Pr coating so that

$$c_{m,B} = e^{B_{old} - B_{new}}, \tag{4.20}$$

we obtain $c_{m,B} = 0.497$. The difference between $c_{m,A}$ and $c_{m,B}$ likely arises from the assumption of a constant field factor and emission area, which may be an oversimplification since the surface roughness of the Pr film can easily modify them.

Let us assume that the field factor is modified after the Pr evaporation by a factor f so that

$$\beta_{new} = f\beta_{old}. \tag{4.21}$$

Thus, we have the following relations between the non-coated and Pr-coated regression coefficients

$$\frac{A_{new}}{A_{old}} = \frac{c_m^{3/2}}{f_m} \tag{4.22a}$$

$$B_{new} - B_{old} = \ln\left(\frac{f_m^2}{c_m}\right), \tag{4.22b}$$

where f_m corresponds to the experimentally measured field factor modification. Solving the system of equations leads to the values $c_m = 0.667$ and $f_m = 1.159$, indicating that the Pr coating not only reduced the effective work function but also increased the field factor.

An attempt to add another 10 nm of Pr unfortunately shorted the device. Fig. 4.32 shows an HIM of the device, which displays the formation of a thin bridges between the terminals. It also showcases the roughness of the evaporated film, which may explain the deviation between expected and measured FN fit parameters.

Parameter	Before Pr	Expected	After Pr
Slope (A)	-39.26	-15.11	-18.45
y-intercept (B)	-17.79	-17.15	-17.09
R^2 value	0.966	NA	0.968

Table 4.3: Expected and extracted FN parameters.

4.8 Discussion

In this chapter, we discussed the design, fabrication, and experimental testing of multi-tip emitters for frequency conversion, to determine if vacuum field emitters can effectively operate at RF frequencies. Multi-tip devices were studied due to their increased emission area, which should enhance emission current. Gold was chosen as the electrode material owing to its unreactivity, providing good emission stability. The empirical results showed that, due to the strong non-linearity in the FN emission equation, the devices are capable of frequency mixing in the MHz range. Furthermore, the effect of Pr evaporation to reduce the emitter work function for higher emission current was investigated. The preliminary measurements were promising, as a considerable enhancement in emission current and reduction in turn-on voltage were observed. Nevertheless, further experiments for repeatability should be conducted. Moreover, a study on deposition conditions and resulting film roughness (e.g., via atomic force microscopy) should be undertaken to determine

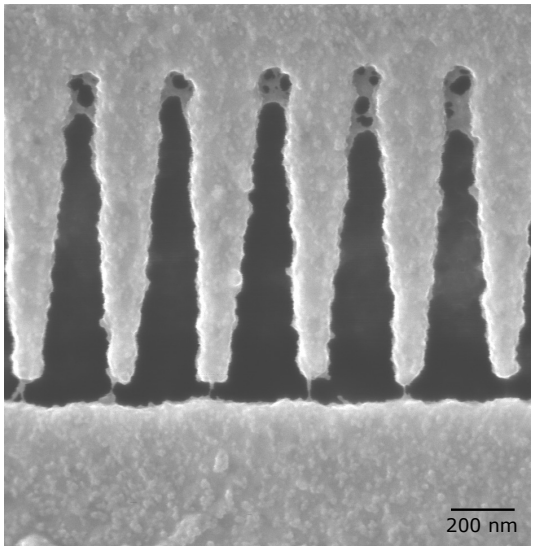

Figure 4.32: HIM of the device after a second layer of Pr was evaporated.

whether the improvement in emission was solely due to the reduced work function of Pr or if it was also a result of the atomic-level roughness of the film.

Although frequency mixing was observed, the conversion loss was excessively high for any practical application. This loss can be attributed to the lack of impedance-matching circuitry in the measurement setup. As a result of the high impedance in the system, it is especially difficult to impedance match to the traditional 50 Ω impedance of the external circuitry because conventional techniques, such as impedance matching transformers, LC networks, or matched attenuators, cannot be used. One possible solution for distributed impedance matching is to use a short stub tuner, which involves adding a specific length of transmission line in either open-circuit or short-circuit configuration at a particular distance from the load [23–26]. An advantage of such a method is that parasitic effects, such as stray capacitances, are minimized. Even though a single stub can be used for simplicity, its matched bandwidth is very narrow, as the reflection coefficient is minimized for the specific load only at the chosen centre frequency. Therefore, stubs should be added to all three ports for maximum power transfer. Additionally, several stubs could be used for wider bandwidth impedance matching at the expense of increased complexity.

Another way to improve the impedance of the device is to fabricate more tips per device. In this chapter, we have shown that an increase in measured current for a given voltage can be achieved when larger arrays of field emitters are used. Consequently, if even more tips are designed per device such that the total current sourced is increased beyond our reported values, the dynamic resistance could be further reduced, thereby improving the RF performance of the device. Although the overall device capacitance would increase, this cost could be tolerated due to the considerably small device capacitance. Furthermore, more tips enable operation at a higher bias, which is advantageous in terms of cutoff frequency.

Further improvements to the measurement setup include adding circulators to prevent noise from reflecting back to the source and/or sample as well as to improve isolation. Additionally, filters in the output port should be employed for additional verification of the integrity of the measurement setup. This will be done in subsequent experiments.

In addition, the emission stability could be improved with a better vacuum. Flicker noise manifested as pulses of random duration at arbitrary intervals is presumed to be related to the adsorption and desorption of gases that modify the local work function at the emitter tip. This is in agreement with the observed data, as fluctuations in the

current were considerably more noticeable during the conditioning process before Pr was deposited compared to the mixing experiments, which had an order of magnitude better vacuum. This illustrates how tiny amounts of contamination can have strong effects on emission. Similarly, the chamber and PCB could be baked to evaporate contaminants before measurements are taken. Note that the PCB can only be baked at a maximum temperature of 170°C, as stated by the manufacturer, to avoid exceeding the glass transition temperature.

One distinct problem of nanoscale vacuum field emission arrays is their poor emission uniformity. It is very difficult, if not impossible, to fabricate all tips within an array with identical field factors. Small variations in gap sizes and nanoprotrusions greatly modify the electric field between tips, which can lead to a single tip dominating emission within the device. This is highly undesirable, as this "hot" tip becomes particularly vulnerable to destruction due to ion bombardment or overheating. Conditioning processes, used to clean the emitter tips, can also erode nanoprotrusions and in some cases, the sharpest emitter tips. Even though this may diminish the measured current, emission can become more stable. However, repeatable performance between different devices remains a major challenge, making it difficult to develop practical devices.

Furthermore, recall that the applied voltage limits the energy to accelerate the electrons. Owing to the nanoscale dimensions, we have successfully decreased the applied voltage to sub-10 V operation, which is favourable in terms of power consumption. However, decreasing voltages also reduces the maximum velocity the electron can be accelerated, regardless of the transport medium. Therefore, even though transport in vacuum is faster than in any other material due to the lack of scattering, the maximum attainable velocity is limited by the applied voltage. Hence, the increase in device performance may not be as large-scale as hoped, which may hinder the path for field emission devices to prosper in high-density applications, such as storage and processors [27].

Lastly, it is worth noting that, even though gold was used for the electrical terminals, the fabrication process can also be extended to other metals that can be evaporated. Gold is not a hard metal and thus, can experience self-diffusion at high temperatures. This can, in turn, sharpen the emitter tip, which ultimately reduces the threshold voltage for emission and affect stability and reliability. Even though the measurements were carried out at room temperature, Joule and/or Nottingham heating can significantly elevate the device temperature and damage the device.

Therefore, harder materials or protective coatings could be used [28, 29]. Additionally, post-processing schemes, such as high-temperature annealing in hydrogen and argon atmosphere, may be useful in further strengthening the gold structures [30].

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Chapter 5

PLASMONICALLY-ENHANCED FIELD EMISSION

So far we have only discussed devices that operate solely through FN electron emission. Thanks to advancements in fabrication capabilities, nanoscale gaps between the electrical terminals can be manufactured, allowing for ballistic transport and very short transit times. However, even though field emission is inherently a fast process, data modulation and transmission is still limited by electronic interconnects. To increase bandwidth and speed, as well as reduce power consumption, the ideal approach would be to use light to modulate and carry electrical signals, effectively creating optoelectronic circuits.

Nonetheless, the integration of photonics and field emission circuits is limited by their spatial dimensions, as the Abbe's diffraction limit places a fundamental constraint on the attainable spatial confinement of light to dimensions below half the wavelength [1]. To overcome this limit and combine electronics and photonics at the nanoscale, surface plasmon polaritons (SPPs) can be used. SPPs are propagating surface waves confined within a dielectric-metal interface. They arise due to the coupling between an incident electromagnetic wave propagating parallel to a metallic surface with appropriate momentum and the coherent collective oscillation of the free electrons at this surface. SPPs have a shorter wavelength (and higher momentum) compared to the incident light, resulting in deep sub-wavelength confinement and strong local electromagnetic field intensities.

In this chapter, we merge field emission and plasmonics on-chip and introduce devices that can be modulated by both electrical and optical fields. Fabricated on SOI substrates for compatibility with current silicon photonics, these devices take advantage of a hybrid geometry for adiabatic nanofocusing of the photonic mode into the plasmonic mode to guide light into the nanoscale field emitting region and obtain sub-wavelength confinement. Due to the strong plasmonic field enhancement as well as the nanoscale separation between emitter and collector terminals, a suggested application for the proposed device is as an ultra-fast, low-power photodetector for the C-band.

5.1 Plasmonics Review

Before diving into the specifics of the device, we first provide a theoretical introduction to the field of plasmonics. We summarize the most important aspects of the response of noble metals to incident electromagnetic fields, as well as the generation and propagation of SPPs based on Maxwell's equations. Additionally, a brief review of the metal-insulator-metal (MIM) waveguide upon which the hybrid plasmonic waveguide is built, is included.

The Drude Model

In the simplest case, the optical properties of noble metals can be described by the Drude or plasma model. In this model, the electrons within the metal are treated as a gas of free electrons that move in opposition to a background of fixed positive ion cores [2, 3]. The equation of motion for an electron when an electromagnetic field is applied is given by

$$m\frac{d^2\mathbf{r}}{dt^2} + m\gamma\frac{d\mathbf{r}}{dt} = -e\mathbf{E} \tag{5.1}$$

where γ is a frictional damping constant to include the effect of collisions with other electrons. If we consider a time-dependent driving electric field of the form $\mathbf{E}(t) = \mathbf{E_0}\exp(-i\omega t)$ with frequency ω, a solution to Eq. (5.1) is given by

$$\mathbf{r} = \mathbf{r_0}\exp(-i\omega t) = \frac{e}{m(\omega^2 + i\gamma\omega)}\mathbf{E}. \tag{5.2}$$

Therefore, the incident field causes the electrons to oscillate with respect to the immobile ion cores. The resulting polarization can be expressed as

$$\mathbf{P} = -ne\mathbf{E} = -\frac{ne^2}{m(\omega^2 + i\gamma\omega)}\mathbf{E} \tag{5.3}$$

where n is the concentration of electrons. Recall that the dielectric displacement $\mathbf{D}$ in linear, isotropic, and non-magnetic media is given by $\mathbf{D} = \epsilon_0\epsilon(\omega)\mathbf{E}$, where $\epsilon(\omega)$ is the dielectric function, and it is related to $\mathbf{P}$ by $\mathbf{D} = \epsilon_0\mathbf{E} + \mathbf{P}$. In this way, if we substitute our result for $\mathbf{P}$ given in Eq. (5.3), the dielectric function for the Drude model is given by

$$\epsilon(\omega) = 1 - \frac{\omega_p^2}{\omega^2 + i\gamma\omega} \tag{5.4}$$

where ω_p is the plasma frequency given by $\omega_p = \sqrt{\frac{ne^2}{\epsilon_0 m}}$. For noble metals, to improve the fit with empirical data in the region $\omega > \omega_p$, we include a background dielectric constant ϵ_∞. In this way, Eq. (5.4) is slightly modified to

$$\epsilon(\omega) = \epsilon_\infty - \frac{\omega_p^2}{\omega^2 + i\gamma\omega}. \tag{5.5}$$

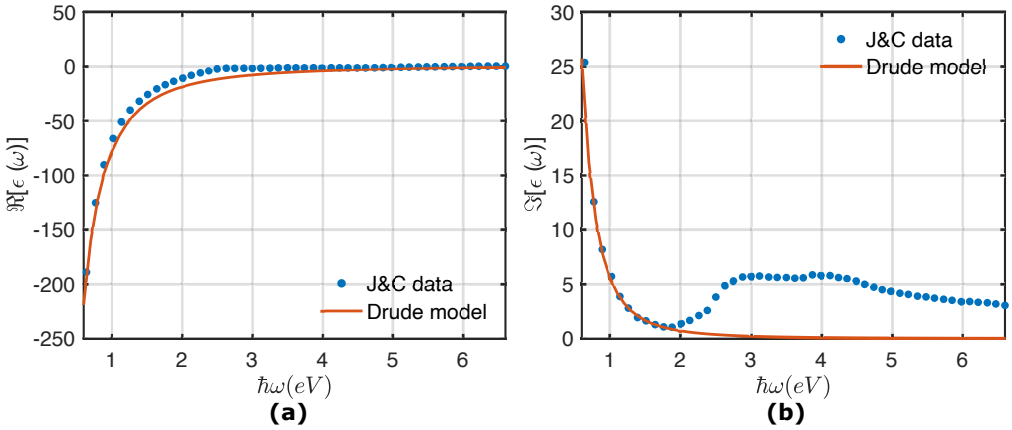


Figure 5.1: Complex dielectric function of gold: (a) real and (b) imaginary components. A comparison between the Drude model (solid line) and empirical data adapted from Johnson & Christy [4] is shown.

This modification is included to account for the residual polarization resulting from the positive ion core background. We can also separate the dielectric function into its real and imaginary components as

$$\epsilon_1(\omega) = \epsilon_\infty - \frac{\omega_p^2}{\omega^2 + \gamma^2} \tag{5.6}$$

$$\epsilon_2(\omega) = \frac{\omega_p^2 \gamma}{\omega(\omega^2 + \gamma^2)}. \tag{5.7}$$

The real part of the dielectric constant is associated with the degree of polarization, while the imaginary part is related to dissipative energy losses into the medium. Fig. 5.1 illustrates the real and imaginary components of the dielectric function for gold based on Drude model and empirical data from Christy & Johnson [4]. It is noteworthy that for optical frequencies, $\epsilon_1(\omega)$ is negative and large. Above the plasma frequency, the Drude model is no longer valid due to interband transitions that cause an increase in $\epsilon_2(\omega)$.

Table 5.1 shows ω_p, γ, and the complex dielectric constant at 1550 nm for the four most commonly used metals in plasmonics. The onset of interband transitions has also been included. The data has been adapted from [5–7]. Silver has the lowest dissipative losses at telecom wavelengths and is capable of supporting plasmons throughout the entire visible spectrum; however, it is known for its quick degradation and fabrication challenges [8]. Copper is an especially attractive material because of its compatibility with CMOS fabrication processes but it oxidizes quickly, a disadvantage that is shared with aluminium. Additionally, the interband transition

Material	ω_p (eV)	γ (eV)	ϵ_1	ϵ_2	Onset of interband transition (eV)
Ag	9.04	0.02125	-131.31	8.6156	3.9
Al	12.04	0.1287	-238.80	34.966	1.4
Au	8.89	0.07088	-116.17	12.943	2.3
Cu	8.76	0.0955	-114.90	16.069	2.1

Table 5.1: Drude model parameters, complex dielectric constant at 1550 nm, and onset of interband transition for common noble metals. Adapted from [5–7].

energy for aluminium is the lowest of all, so its use for plasmonic applications is restricted to the blue and UV range. Gold is the most popular material choice for plasmonic devices due to its chemical stability and relatively low losses.

Surface Plasmon Polaritons

As briefly described in the introduction of this chapter, SPPs are formed at the interface between a conductor and a dielectric. When an incident electromagnetic wave propagating in free space with appropriate momentum strikes the interface, it penetrates slightly into the conductor. The resulting lateral displacement of the free electrons causes a net separation of charge. The electromagnetic wave that arises due to the coupling between the incident electromagnetic field and the coherent electron plasma oscillation modes is referred to as an SPP. These waves propagate in the direction tangential to the interface and are evanescently bound in the perpendicular direction, as shown in Fig. 5.2.

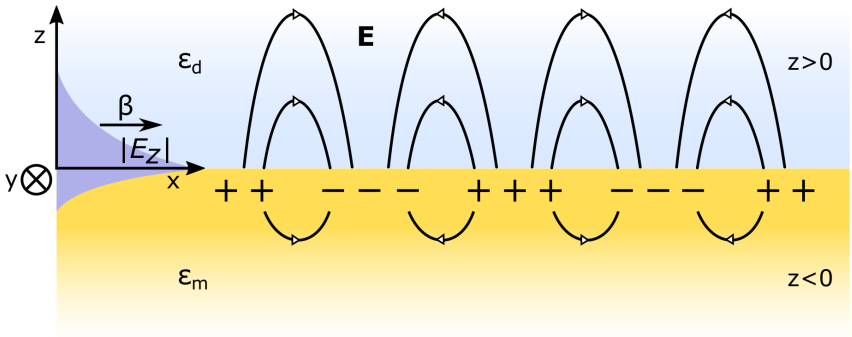


Figure 5.2: Illustration of the SPP propagation along the x-axis. The evanescent confinement on both sides of the interface is shown by the purple exponential decay curves.

To describe their propagation, we must resort to Maxwell's equations at the metal-dielectric interface. In the absence of any external current densities or charges,

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{5.8a}$$

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} \tag{5.8b}$$

$$\nabla \cdot \mathbf{D} = 0 \tag{5.8c}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{5.8d}$$

where $\mathbf{B}$ is the magnetic induction, $\mathbf{H}$ is the magnetic field, and $\mathbf{D}$ is the electric displacement field. If we assume a linear, non-magnetic, and isotropic medium, we further have

$$\mathbf{D} = \epsilon_0 \epsilon \mathbf{E} \tag{5.9a}$$

$$\mathbf{B} = \mu_0 \mathbf{H}. \tag{5.9b}$$

If we combine Eqs. (5.8a) and (5.8b), we obtain

$$\nabla \times \nabla \times \mathbf{E} = -\mu_0 \frac{\partial^2 \mathbf{D}}{\partial t^2}. \tag{5.10}$$

Recall the identities $\nabla \times \nabla \times \mathbf{E} \equiv \nabla(\nabla \cdot \mathbf{E}) - \nabla^2 \mathbf{E}$ and $\nabla \cdot (\epsilon \mathbf{E}) \equiv \mathbf{E} \cdot \nabla \epsilon + \epsilon \nabla \cdot \mathbf{E}$. If we assume that the dielectric profile is homogeneous so that $\nabla \epsilon = 0$, Eq. (5.10) reduces to the wave equation

$$\nabla^2 \mathbf{E} = \frac{\epsilon}{c^2} \frac{\partial^2 \mathbf{E}}{\partial t^2}. \tag{5.11}$$

A solution to the wave equation is a time-harmonic plane wave $E(\mathbf{r}, t) = \mathbf{E}(\mathbf{r}) e^{-i\omega t}$, where $\mathbf{k}$ is the wave vector of the propagating wave. If we insert this into Eq. (5.11), we obtain the famous Helmholtz equation

$$\nabla^2 \mathbf{E} + k_0^2 \epsilon \mathbf{E} = 0 \tag{5.12}$$

where $k_0 = \frac{\omega}{c}$ is the free space wave vector. Without loss of generality, let us assume for simplicity a one-dimensional problem in which the geometry consists of a metal-dielectric interface at $z = 0$ and parallel to the xy plane. The waves propagate along the x direction in the xz plane so that $\mathbf{E}(x, y, z) = \mathbf{E}(z) e^{i\beta x}$, where $\beta = k_x$ is the propagation constant and is the same in both regions. The geometry is illustrated in Fig. 5.2. Therefore, Eq. (5.12) simplifies to

$$\frac{\partial^2 \mathbf{E}(z)}{\partial z^2} + (k_0^2 \epsilon - \beta^2) \mathbf{E} = 0. \tag{5.13}$$

Due to the harmonic time dependence, $\frac{\partial}{\partial t} = -i\omega$. Additionally, we have $\frac{\partial}{\partial x} = i\beta$ as the propagation is along the x direction, and $\frac{\partial}{\partial y} = 0$ due to the homogeneity of the y direction. We can then use Eqs. (5.8a) and (5.8b) to obtain

$$\frac{\partial E_y}{\partial z} = -i\omega\mu_0 H_x \tag{5.14a}$$

$$\frac{\partial E_x}{\partial z} - i\beta E_z = i\omega\mu_0 H_y \tag{5.14b}$$

$$i\beta E_y = i\omega\mu_0 H_z \tag{5.14c}$$

$$\frac{\partial H_y}{\partial z} = i\omega\epsilon_0\epsilon E_x \tag{5.14d}$$

$$\frac{\partial H_x}{\partial z} - i\beta H_z = -i\omega\epsilon_0\epsilon E_y \tag{5.14e}$$

$$i\beta H_y = -i\omega\epsilon_0\epsilon E_z. \tag{5.14f}$$

This system has two sets of self-consistent solutions: transverse magnetic (TM) modes, in which the only non-zero components are E_x, E_z, and H_y, and transverse electric (TE) modes, in which the only non-zero components are H_x, H_z, and E_y.

For the TM mode, Eq. set (5.14) yields

$$E_x = -i\frac{1}{\omega\epsilon_0\epsilon}\frac{\partial H_y}{\partial z} \tag{5.15a}$$

$$E_z = -\frac{\beta}{\omega\epsilon_0\epsilon}H_y \tag{5.15b}$$

and Eq. (5.13) reduces to

$$\frac{\partial^2 H_y}{\partial z^2} + (k_0^2\epsilon - \beta^2)H_y = 0 \tag{5.16}$$

while for the TE mode we have

$$H_x = i\frac{1}{\omega\mu_0}\frac{\partial E_y}{\partial z} \tag{5.17a}$$

$$H_z = -\frac{\beta}{\omega\mu_0}E_y \tag{5.17b}$$

and

$$\frac{\partial^2 E_y}{\partial z^2} + (k_0^2\epsilon - \beta^2)E_y = 0. \tag{5.18}$$

If we return to the geometry shown in Fig. 5.2, where the top half-space ($z > 0$) consists of dielectric material with $\Re(\epsilon_d) > 0$ and the bottom half-space is metal with $\Re(\epsilon_m) < 0$, then the solutions for the TM mode become

$$H_y(z) = A_d e^{i\beta x} e^{-k_d z} \tag{5.19a}$$

$$E_x(z) = iA_d \frac{1}{\omega\epsilon_0\epsilon_d} k_d e^{i\beta x} e^{-k_d z} \tag{5.19b}$$

$$E_z(z) = -A_d \frac{\beta}{\omega\epsilon_0\epsilon_d} e^{i\beta x} e^{-k_d z} \tag{5.19c}$$

for $z > 0$ and

$$H_y(z) = A_m e^{i\beta x} e^{k_m z} \tag{5.20a}$$

$$E_x(z) = -iA_m \frac{1}{\omega\epsilon_0\epsilon_m} k_m e^{i\beta x} e^{k_m z} \tag{5.20b}$$

$$E_z(z) = -A_m \frac{\beta}{\omega\epsilon_0\epsilon_m} e^{i\beta x} e^{k_m z} \tag{5.20c}$$

for $z < 0$. Note that $k_{d,m}$ refers to the k_z component of the wave vector in the dielectric and metal, respectively. If we insert Eqs. (5.19a) and (5.20a) into Eq. (5.16), then

$$k_d^2 = \beta^2 - k_0^2\epsilon_d \tag{5.21a}$$

$$k_m^2 = \beta^2 - k_0^2\epsilon_m. \tag{5.21b}$$

Moreover, as a result of the continuity of H_y and ϵE_z at the interface, it follows that for TM modes

$$A_d = A_m \tag{5.22a}$$

$$\frac{k_d}{k_m} = -\frac{\epsilon_d}{\epsilon_m}. \tag{5.22b}$$

Therefore, SPPs can only exist if the real component of the dielectric permittivity changes sign at the interface. The dispersion relation of SPPs is

$$\beta = k_0 \sqrt{\frac{\epsilon_m \epsilon_d}{\epsilon_m + \epsilon_d}}. \tag{5.23}$$

If we follow the same analysis for TE modes and apply the continuity of E_y and H_x at the interface, we obtain

$$A_m(k_m + k_d) = 0. \tag{5.24}$$

Bound modes require that the real component of the wave vectors be positive, implying that $A_m = A_d = 0$. Hence, there are no TE SPPs for $\mu = 1$.

The dispersion relation given in Eq. (5.23) is plotted in Fig. 5.3 for air and SiO_2 interfaces. The Drude model with negligible loss was used to describe the dielectric function of the metal, as given by Eq. (5.4). We observe an energy splitting between two branches that lie on either side of the light line. The upper branch has frequencies above the plasma frequency $\omega > \omega_p$, corresponding to unbound modes where radiation can propagate into the metal; these are known as bulk or

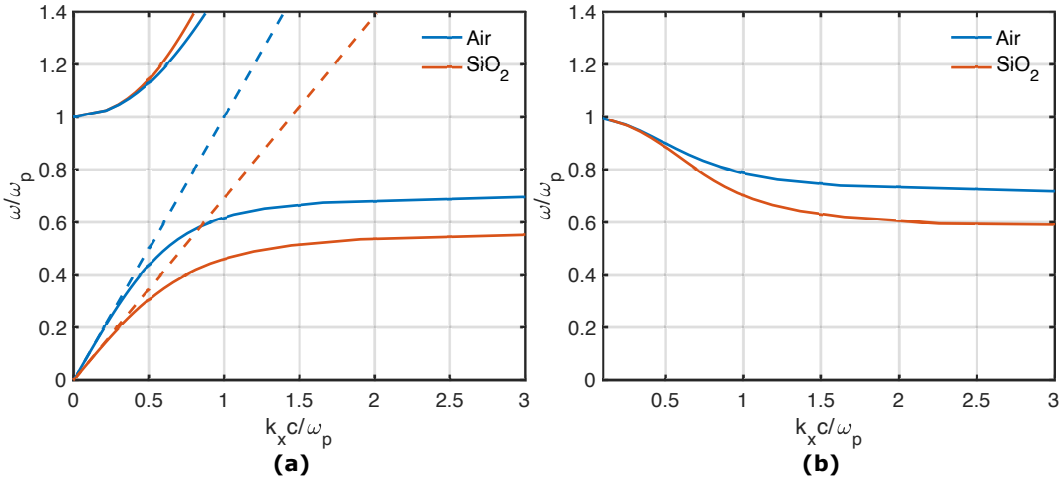


Figure 5.3: Normalized SPP dispersion relation assuming Drude model with negligible damping for propagation in air (blue) and SiO_2 (red): (a) real and (b) imaginary components. Note that the light lines (dashed lines) with $\omega = ck$ are also included.

volume plasmon polaritons. The lower branch has frequencies below the plasma frequency $\omega < \omega_p$, representing the bound solutions corresponding to SPPs. Due to the mismatch between the wave vector of the incident light and of the SPP, special wave vector matching techniques, such as prism coupling or gratings, must be used to excite SPPs at higher frequencies. A frequency gap with purely imaginary wave vectors that forbids propagation separates both branches.

For small wave vectors at low frequency, the SPP branch lies close to the light line. Here, the nature of the SPP resembles an electromagnetic plane wave propagating parallel to the interface. This wave propagates for many wavelengths into the dielectric, barely penetrating the metal. These are the Sommerfeld-Zenneck waves [9]. For large wave vectors, the dispersion curve for the SPP asymptotically approaches the characteristic surface plasmon frequency

$$\omega_{SP} = \frac{\omega_p}{\sqrt{1+\epsilon_d}}. \tag{5.25}$$

If we consider no losses in the metal such that $\Im[\epsilon_m(\omega)] = 0$, then the wave vector β approaches infinity and the group velocity goes to zero. This also corresponds to $\Re(\epsilon_m) = -\Re(\epsilon_d)$. At ω_{SP}, the mode becomes a stationary electron oscillation known as the surface plasmon [10]. For wave vectors between these two limiting cases, the resulting polariton behaves like a hybrid of both extremes.

To make the model more realistic, we should consider metal losses due to free electrons and interband damping effects so that $\Im(\epsilon_m) \neq 0$. Consequently, the

propagation constant becomes complex, so that $\beta = \beta_1 + i\beta_2$, with β_1 related to the confinement of the mode and β_2 associated with the losses. We can rewrite our expression for the propagating wave as

$$\mathbf{E}(x, y, z) = \mathbf{E}(z)e^{i\beta_1 x}e^{-\beta_2 x}. \tag{5.26}$$

Therefore, the wave becomes exponentially attenuated in the direction of propagation. The resulting propagation length, i.e., the distance at which the intensity of the SPP decreases to $1/e$ of its initial value, is given by

$$L = \frac{1}{2\beta_2}. \tag{5.27}$$

When losses are included, β_1 does not approach infinity, but rather a finite maximum value at ω_{SP}. As a result, the wavelength of the surface plasmon becomes finite with a minimum value of $\lambda_{SP} = 2\pi/\beta_1$. Additionally, the z-component of the wave vector at either side of the interface, given by Eqs. (5.21), decays exponentially. The penetration depth into either half-space, which corresponds to the distance perpendicularly from the interface where the amplitude of the field has decreased to $1/e$ of its value at $z = 0$, is given by

$$\delta_{d,m} = \frac{1}{|k_{d,m}|} = \frac{1}{k_0}\sqrt{\left|\frac{\epsilon_m + \epsilon_d}{{\epsilon_{d,m}}^2}\right|} \tag{5.28}$$

with $\epsilon_d\delta_d = |\epsilon_m|\delta_m$ [11, 12]. The penetration depth is related to the energy confinement of the mode on either side. Generally, $|\epsilon_d| < |\epsilon_m|$, so that the mode is mainly confined in the dielectric.

In conclusion, at frequencies close to ω_{SP}, the energy confinement at the interface, as gauged by the penetration depth, is strong; however, this comes at the cost of small propagation distances due to the increased interaction with the metal and its associated damping losses. This inseparable connection between confinement and loss is the main limitation of plasmonics so a trade-off is always required.

The Metal-Insulator-Metal Waveguide

So far, we have studied the case of a single dielectric-metal interface, which only supports bound TM modes. Now, let us consider what would happen if we add another metallic layer, such that the resulting system consists of a dielectric slot between two metal planes, as shown in Fig. 5.4. When the slot width w is comparable to or smaller than the penetration depth of the single interface mode

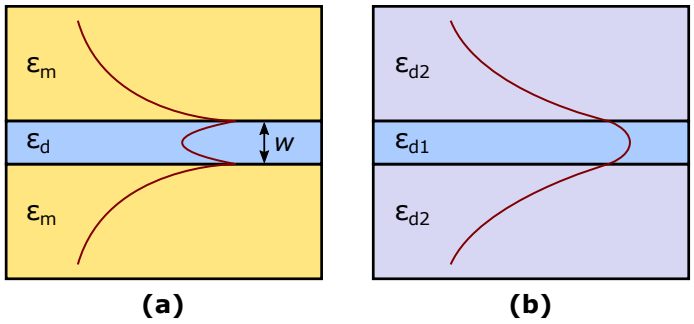


Figure 5.4: Field distribution of the fundamental mode for (a) MIM structure and (b) all dielectric multilayer with $\epsilon_{d1} > \epsilon_{d2}$ for comparison.

δ_d, the field overlap causes the modes to interact, resulting in hybridized modes. Following the same analysis described in the previous section based on solving the Helmholtz equation under the appropriate boundary conditions for the tangential and normal electric field components at the interface, we arrive at the following dispersion relation [13]

$$\tanh(k_d w) = -\frac{\epsilon_d k_m}{\epsilon_m k_d} \tag{5.29}$$

with $k_{d,m} = \sqrt{\beta^2 - k_0^2 \epsilon_{d,m}}$. Note that the system supports both symmetric and antisymmetric modes; however, we focus on the symmetric mode, which exhibits odd symmetry of the longitudinal electric field component E_x and even symmetry of the transverse field component E_z, as this mode extends for all slot values. This mode is sketched in Fig. 5.4. For sufficiently small slot widths (i.e., $w \to 0$), we can approximate $\tanh x \approx x$, allowing us to express the wave vector as

$$\beta \approx k_0 \sqrt{\epsilon_d + \left(\frac{\epsilon_d}{w k_0 \epsilon_m}\right)^2}. \tag{5.30}$$

An interesting characteristic of these structures is that as the slot width goes to zero, the propagation wave vector increases indefinitely as $\beta \approx -\epsilon_d/(w\epsilon_m) \to \infty$. This implies that the hybrid mode allows for tighter confinement that can be modified by merely adjusting the geometry. Fig. 5.5 depicts the normalized electric field intensity of the fundamental mode for various slot widths. The mode is strongly confined within the dielectric slot and rapidly decreases at the metallic interfaces. The mode confinement for an all-dielectric waveguide (Fig. 5.4 (b)) is also included for comparison. While the all-dielectric waveguide is limited by diffraction, the MIM geometry is capable of achieving extreme confinement below this limit. This

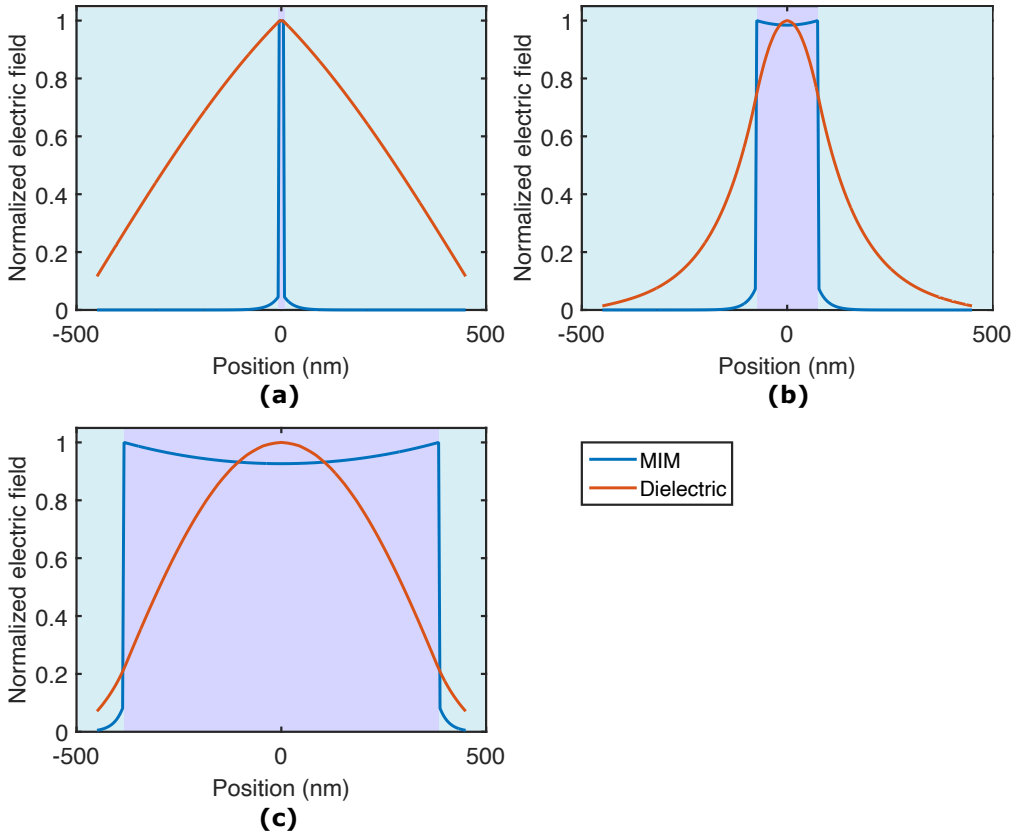


Figure 5.5: Normalized electric field of the fundamental mode for the MIM structure (blue) and all-dielectric geometry (red) for various slot widths: (a) $\lambda/100$, (b) $\lambda/10$, and (c) $\lambda/2$, where $\lambda = 1550$ nm.

characteristic is especially useful for designing metal waveguides for sub-wavelength guided mode propagation.

5.2 The Hybrid Plasmonic Waveguide

In this section, we describe the hybrid plasmonic waveguide, which forms the basis of the device explored in this chapter. For a more detailed review of the structure, refer to [14–16]. Note that their hybrid plasmonic waveguides were capped with SiO_2. Since our devices experience very large fields at the metallic terminals due to the merging of plasmonics with field emission, we replaced the oxide that surrounds the structure with air to avoid dielectric breakdown of the insulator.

Building upon the MIM geometry, we aimed to create a waveguide with a two-dimensional lateral sub-wavelength confinement of the mode in the plane normal to the propagation direction. An approach that is compatible with traditional silicon photonics platform and can achieve strong field enhancements is the hybrid

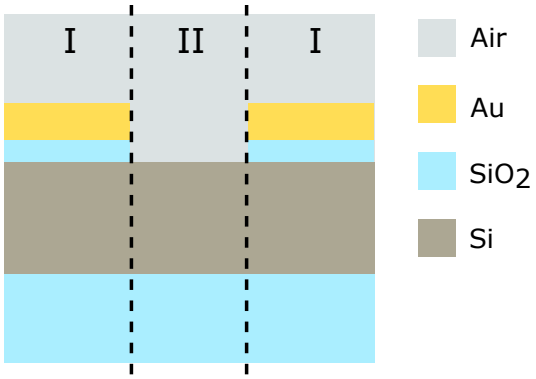


Figure 5.6: Illustration of the cross-section of the hybrid plasmonic waveguide.

plasmonic waveguide. This system consists of a MIM plasmonic slot coupled to an underlying photonic waveguide, as shown in Fig. 5.6. A low refractive index dielectric spacer between the top MIM structure and the bottom photonic waveguide was included to modify the effective refractive index and provide strong mode confinement. It was also useful in mitigating plasmonic propagation losses, which scale with the real part of the dielectric permittivity as $\propto \epsilon_d^{3/2}$ [14, 17].

To confine the in-plane mode, metal loading was employed to spatially modify the effective refractive index n_{eff}. The effect of metal loading a silicon slab for both TE and TM polarizations is shown in Fig. 5.7. In the case of TE polarization, the metal layer pushed the mode down into the underlying SiO_2 substrate layer, resulting in a decrease of n_{eff} since a larger fraction of the energy now resides in the lower layer. For TM polarization, metal loading the Si waveguide caused the mode to be confined in the metal-dielectric interface. Boundary conditions require that the perpendicular component of the displacement field be continuous across interfaces.

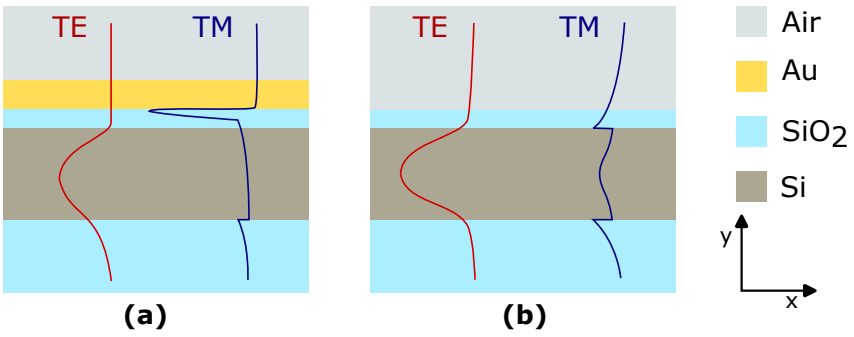


Figure 5.7: Effect of metal loading a Si slab for both TE and TM polarizations. (a) Shows a metal-loaded Si slab waveguide and (b) illustrates an unloaded Si slab waveguide.

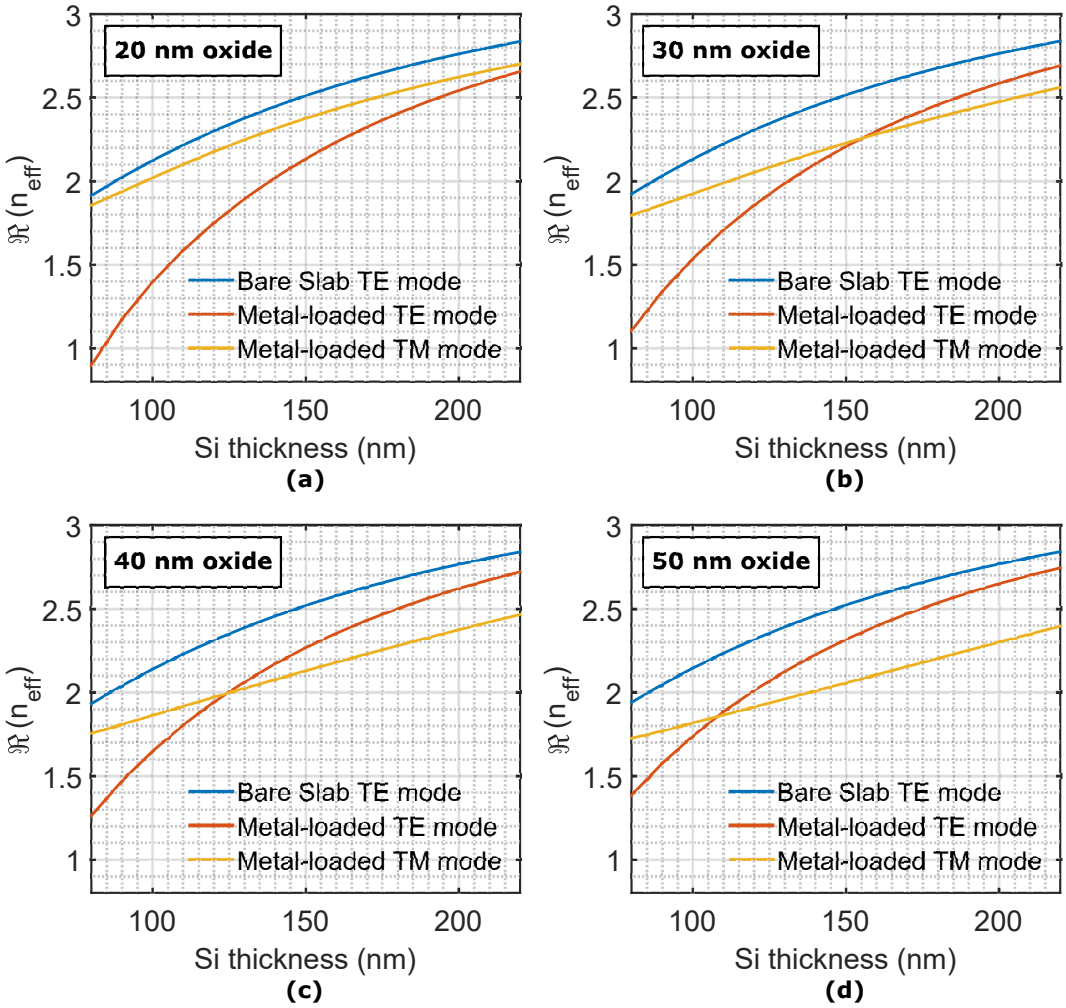


Figure 5.8: Real component of n_{eff} for the bound TE mode of region II and both TE and TM modes of region I as a function Si thickness and the following spacer oxide thicknesses: (a) 20 nm, (b) 30 nm, (c) 40 nm, and (d) 50 nm.

As the magnitude of the real component of the dielectric permittivity of the metal and the Si is larger than that of the SiO_2 layer, the electric field in the SiO_2 region was enhanced to satisfy the interface condition. This strong confinement increased n_{eff} compared to the TM mode in the bare Si slab.

For simplicity, we considered the overall structure to be composed of three regions: two identical metal-loaded Si slab waveguides on either side and a bare Si slab waveguide in the center. These corresponded to region I and region II, respectively, as shown in Fig. 5.6. Confinement in the center slot was achieved when n_{eff} of the fundamental mode in region II was larger than in region I. This is analogous to how confinement is accomplished in a Si photonics ridge waveguide, wherein n_{eff}

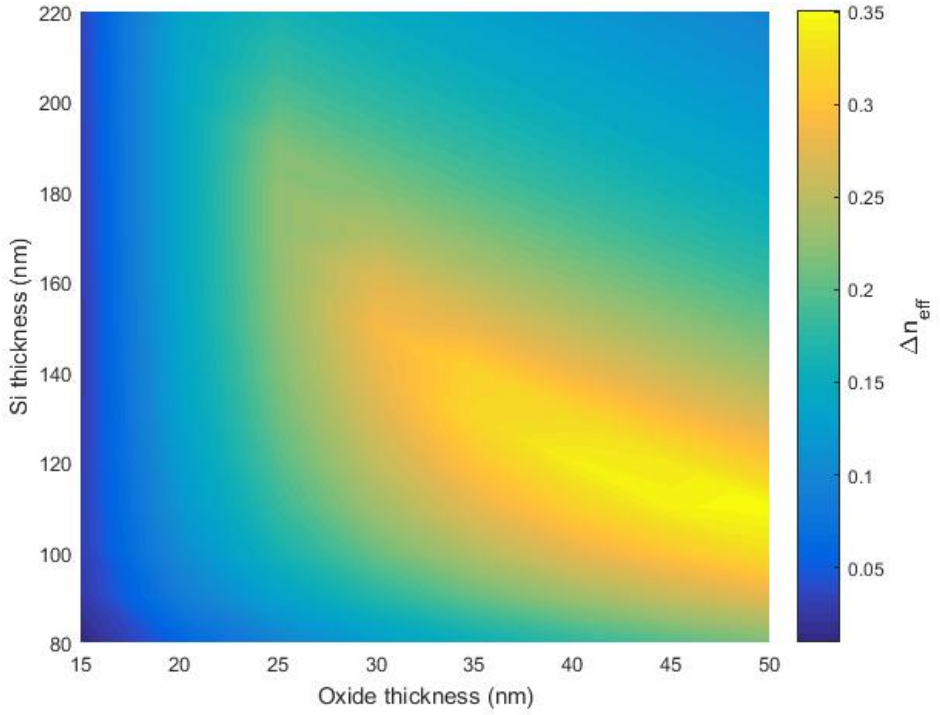


Figure 5.9: Difference in the n_{eff} between the bound TE mode of the bare Si slab waveguide of region II and the largest of either TE or TM modes of the metal-loaded waveguide of regions I as a function of Si and oxide thickness.

is modified by selectively etching away parts of the Si. n_{eff} was further modified by tuning the spacer oxide and the underlying Si thicknesses. Fig. 5.8 illustrates the effect of varying Si and spacer oxide thicknesses on n_{eff} for the bound TE mode of the bare Si slab, which had the highest n_{eff} in region II, and for both TE and TM modes of the metal-loaded waveguide of region I. A two-dimensional FEM simulation (COMSOL Multiphysics 5.4) was used to extract these values. Note that $\lambda = 1550$ nm and the thickness of gold was set to 50 nm. The material properties used were obtained from empirical data by Johnson et al. for gold [4], Gao et al. for SiO_2 [18], and Li for Si [19]. Next, the difference in the real component of n_{eff} between the bound TE mode of the bare Si slab and the largest of the metal-loaded TE or TM mode was plotted as shown in Fig. 5.9 as a function of oxide and Si thickness. The graph shows that the difference was small for either thin spacer oxide due to the large metal-loaded TM mode and for large Si thickness as a result of the large metal-loaded TE mode. The maximum confinement occurred for oxide thicknesses larger than 40 nm with a Si thickness of approximately 110 nm. For

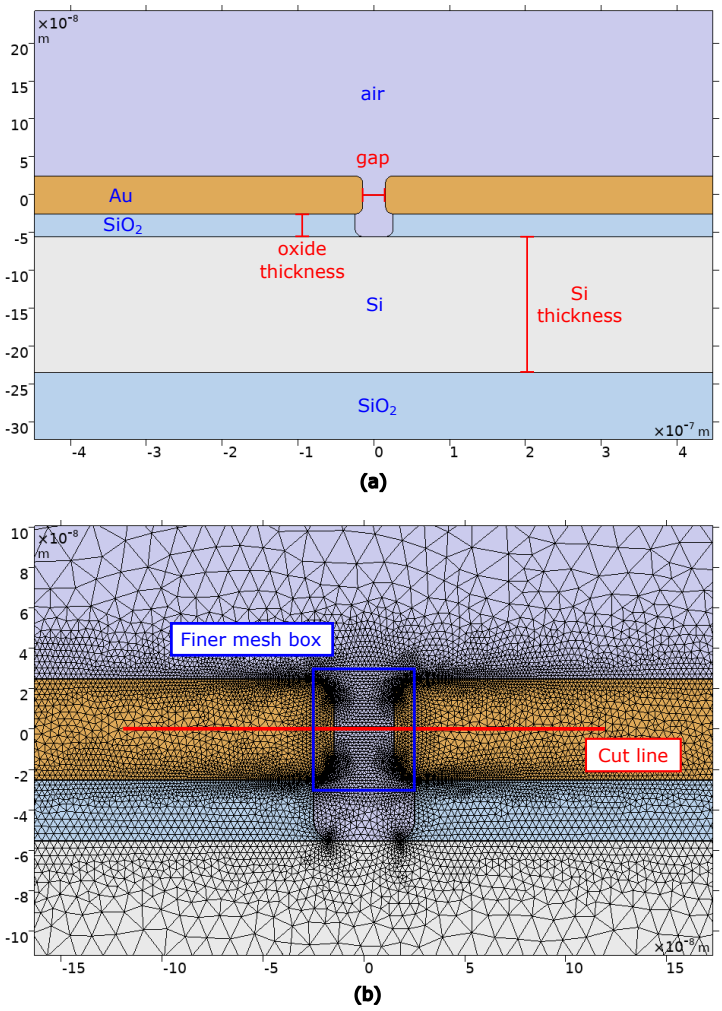


Figure 5.10: Simulation parameters: (a) two-dimensional geometry and (b) mesh employed.

practical photonics applications, a slab thickness of 110 nm may be too slim, so we chose a Si thickness of 160 nm and an oxide thickness of 30 nm.

We studied mode confinement for the full device using the previously selected Si and oxide thickness with a two-dimensional COMSOL simulation to model the cross-section of our structure. The geometry and the mesh employed are presented in Fig. 5.10. Sharp corners were rounded to avoid calculation singularities that could produce anomalous results, and a box surrounding the gap between both metal layers that penetrated 10 nm in the metal layers was defined to create a finer optimized mesh. Fig. 5.11 shows the real and imaginary components of n_{eff} as a function of gap width. Both the highest confinement and the largest loss were computed for the smallest gap (10 nm). At this gap width, the mode was mainly plasmonic in

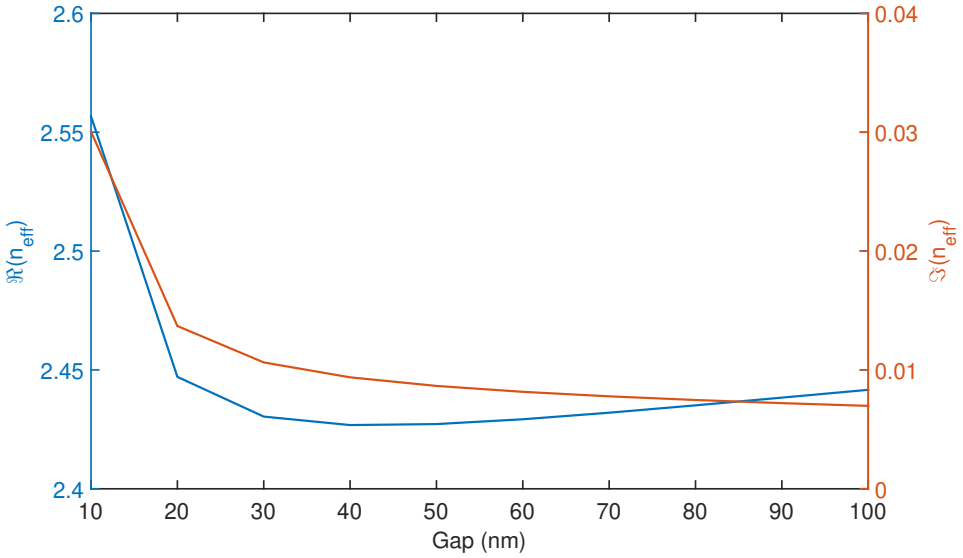


Figure 5.11: Complex n_{eff} for the proposed structure as a function of gap size: (a) real and (b) imaginary components.

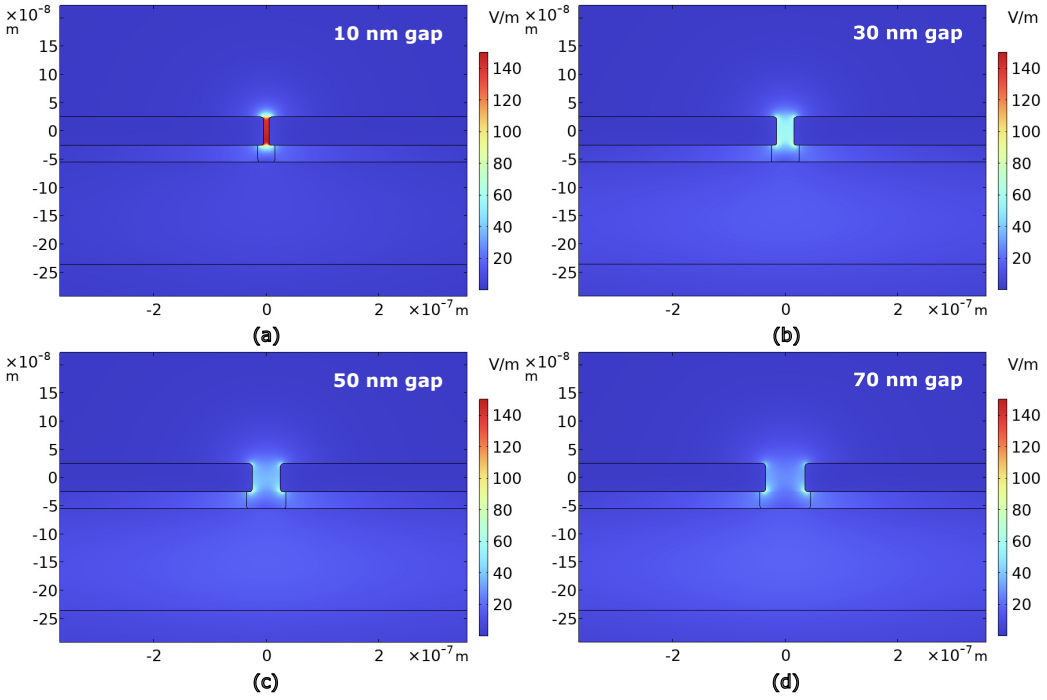


Figure 5.12: Electric field distribution as a function of gap width: (a) 10 nm gap, (b) 30 nm gap, (c) 50 nm gap, and (d) 70 nm gap. Note that all figures have the same intensity scale.

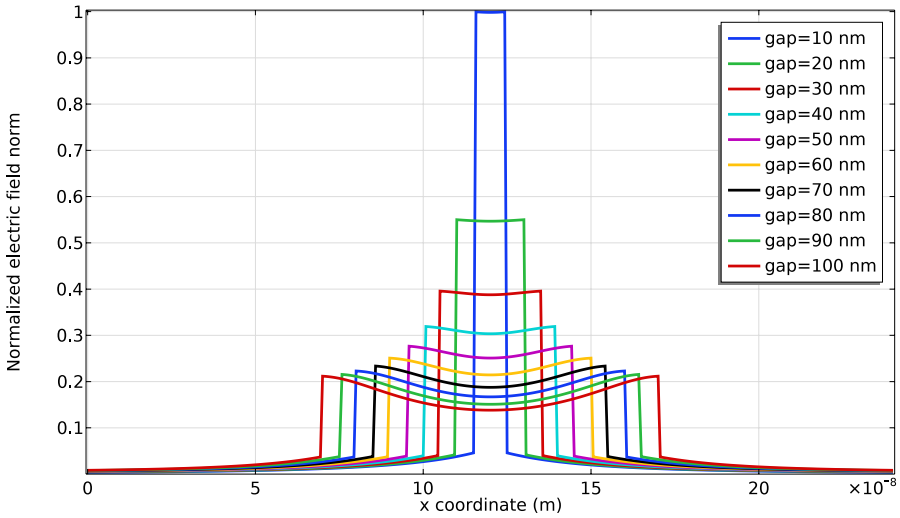


Figure 5.13: Normalized field energy distribution along cut line as defined in Fig. 5.10 for various gap widths.

nature, resembling that of the MIM waveguide described in the previous section. The lowest loss was calculated for the largest gap size (100 nm), as illustrated by the electric field distribution in Fig. 5.12. The structure with the smallest gap had the largest proportion of the mode energy residing within the slot, which explained the large n_{eff}. Conversely, the design with the widest gap had the highest fraction of the mode energy existing in the underlying Si. Furthermore, the normalized field intensity distribution for various gap widths is presented in Fig. 5.13. A cut line in the middle of the gap, as shown in Fig. 5.10 (b), was used to avoid anomalous high field regions in the corners. As expected, the largest field was located at the interface between the metal and vacuum gap, decaying exponentially away from it. As the gap width decreased, the coupling between both sets of interfaces increased. Therefore, the energy storage was highest for the smallest gap and decayed as the gap widens, as the coupling between both sets of interfaces weakened.

For a more quantitative analysis, the percentage of the mode in the gap region and in the metal tips was computed. This corresponds to the fraction of the mode that influences field emission. Recall that the time-average stored energy density $\langle W \rangle$ for a non-magnetic, dispersive medium is given by [20]

$$\langle W \rangle = \frac{1}{4}\left(\Re\left[\frac{d}{d\omega}(\omega\epsilon(\omega))\right]|\mathbf{E}|^2 + \mu_0|\mathbf{H}|^2\right). \tag{5.31}$$

The total time-average field energy within a cross-sectional plane with respect to the direction of propagation is calculated by integrating across the desired area

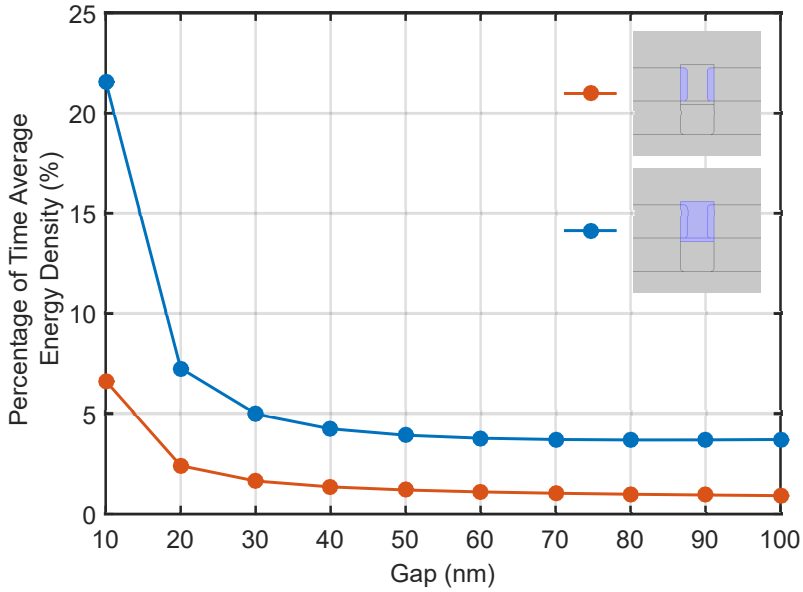


Figure 5.14: Percentage of time average energy density in metal tips and all gap area as a function of gap width.

A, i.e., $\langle W \rangle_{total} = \int_A \langle W \rangle dA$. Fig 5.14 shows the computed percentage of the total electromagnetic energy in the mode for the gap region and the metal tips as a function of varying gap width. Both areas of integration are shown in the top right corner. As the previous qualitative analysis concluded, when the gap decreased in size, the mode became more plasmonic in nature, characterized by a significant fraction of the total mode energy residing in the slot area. Additionally, the fraction of the mode energy that was found within the metal tips also increased, which explains the high losses. Consequently, the propagation length of the mode was adversely impacted, as exhibited in Fig. 5.15.

To couple free-space light into (as well as out of) the TE mode of a photonic Si slab waveguide, a gold grating was used, which enabled matching the wavenumber of the incident light beam to the propagation constant of the waveguide. This technique has several advantages compared to other k-vector matching methods, such as prism coupling, end-fire coupling, and nanoparticle coupling [21, 22], one of which is the grating coupler's fairly relaxed positioning tolerance of the input beam. Additionally, it allows for both the device as well as the grating to be patterned in a single lithographic step. For normal incidence, the grating period, Λ, is given by [23]

$$\Lambda = \frac{\lambda}{n_{eff}} \tag{5.32}$$

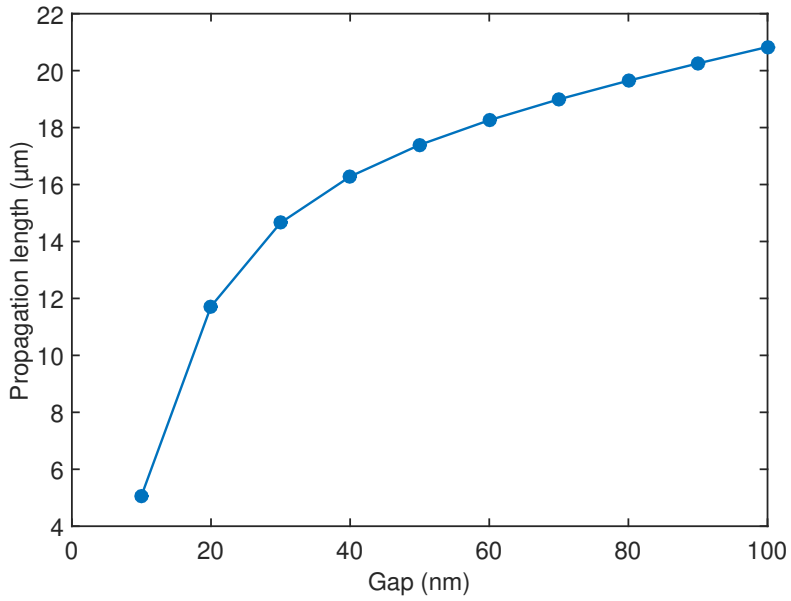


Figure 5.15: Propagation length as a function of gap size.

where λ is the wavelength of the incident light.

Next, nanofocusing of the photonic mode into the plasmonic mode was employed to mitigate the large size mismatch between both modes. Nanofocusing was achieved through an adiabatic taper that gradually increased the energy confinement of the mode by slowing down its group velocity. As shown in Fig. 5.16, by reducing the width of the central region bounded by metal layers on either side, the Si slab photonic mode hybridized with the plasmonic mode. This technique also allowed the generation of very high optical field intensities at the apex due to the energy accumulation from the considerable reduction of the mode area and the slow-down of the local group velocity of the hybrid mode. For example, Güsken et al. calculated an optical enhancement of over 400 in a simulated structure with a 20 nm gap [15], while Nielsen et al. experimentally measured via photoluminescence of three-photon excited CdSe/ZnS quantum dots an enhancement of about 170 in a 24 nm gap [16]. This strong optical field confinement can be particularly attractive for various non-linear effects in the nanoscale, as usually large-scale interaction lengths are needed to obtain detectable signals.

Two types of losses need to be considered when designing the taper: propagation losses and back-reflections. Propagation losses arise due to the strong interaction of the mode with the nearby lossy metal, so the taper must be as short as possible

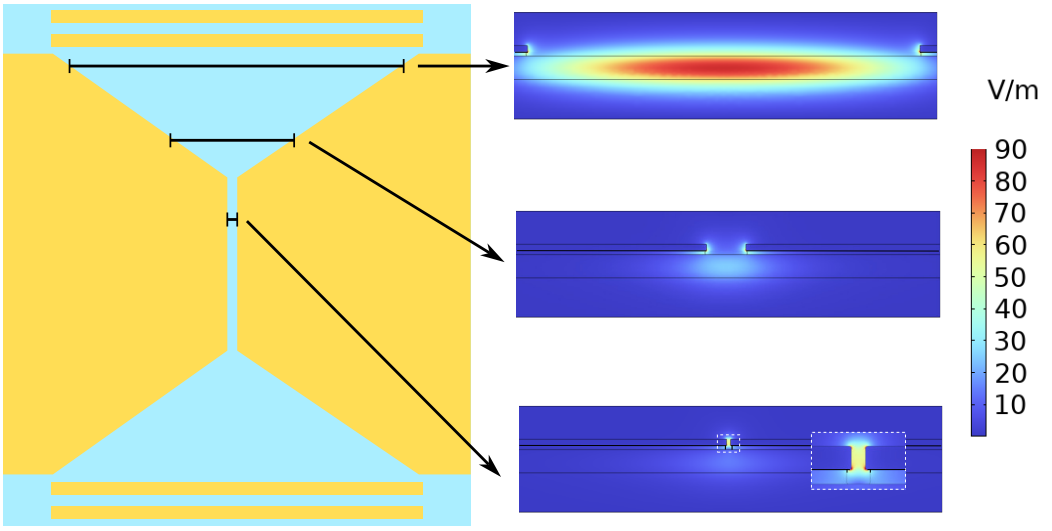


Figure 5.16: Top-view of the hybrid plasmonic structure. A grating coupler was used to couple free space light into the photonic mode of the waveguide, which was subsequently adiabatically converted into a plasmonic mode by means of an metallic taper. Simulations of the electric field at various locations along the taper to depict mode hybridization were also included.

to minimize these losses. However, as the gap width is reduced, the effective index is increased. If this rate is too high, back-reflections occur, which adversely affect mode confinement. Thus, effective nanofocusing requires that the taper angle be large enough to minimize dissipative losses, but also small enough to reduce back-scattering losses. Following the analysis presented in [24], a mathematical criterion for adiabaticity, given by the Eikonal parameter, can be calculated as follows:

$$\delta(z) = \frac{1}{k_0}\left|\frac{d(\Re(\beta(z))^{-1})}{dz}\right| \tag{5.33}$$

where z is the distance along the taper direction. Adiabatic nanofocusing is achieved when $\delta(z) < 1$. The derivation of the Eikonal parameter assumed that the length scale over which the mode varies is much larger than the SPP wavelength so the WKB approximation can be used to study the propagation of the mode along the taper. Hence, as long as δ remains below the limit for the entire length of the taper, energy loss due to back-reflections or scattering is negligible. Fig. 5.17 shows the computed Eikonal parameter as a function of gap width for a taper angle of 45°. As the adiabatic condition was satisfied for all gap widths, the chosen taper angle was adequate for nanofocusing.

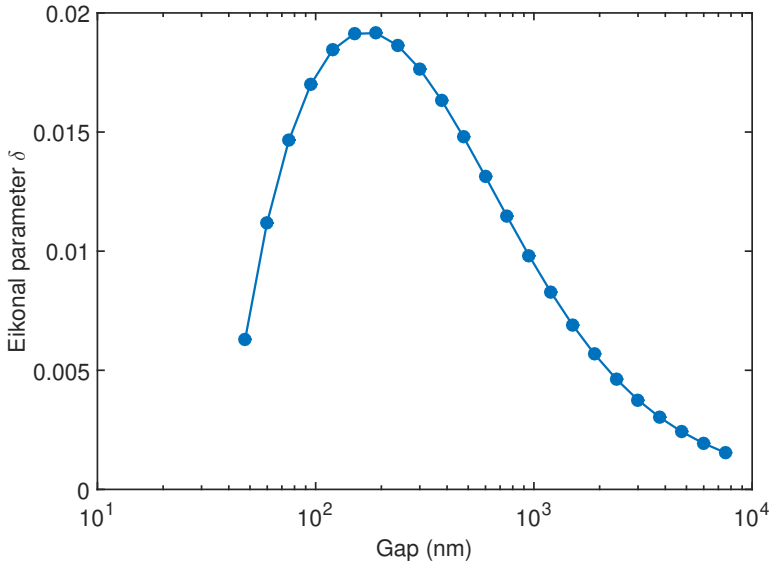


Figure 5.17: Computed Eikonal parameter as a function of gap width for a taper angle of 45°.

5.3 Field Emission Simulations

Previously, the optical properties of the proposed device were analyzed. In this section, the electrostatic properties related to field emission are discussed. The thicknesses for the various layers chosen are as follows: 160 nm for Si, 30 nm SiO_2, and 50 nm Au.

Fig. 5.18 displays the three electrical terminals. The gold metal layer used to confine the mode in the center region served as the emitter and collector terminals, which were indistinguishable from one another due to the symmetry of the device. The underlying Si, which carried the photonic mode, was doped to make it conductive and act as an electrical gate, allowing for field emission to be modulated. The

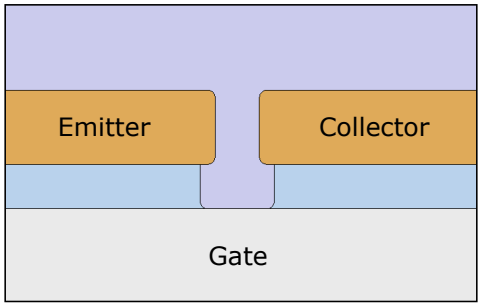


Figure 5.18: Cross-sectional view of the schematic for the proposed device with electrical terminals.

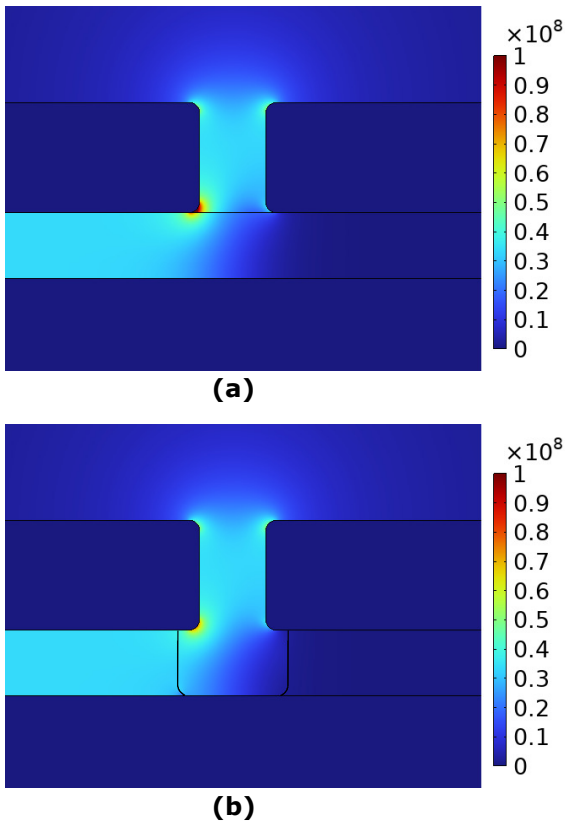


Figure 5.19: Electric field distribution (a) without and (b) with undercut. The chosen gap was 30 nm.

metal terminals were separated from the gate by the spacer oxide, as required by the hybrid plasmonic waveguide. To prevent dielectric breakdown due to the large static electric fields experienced at the emitter tip, the oxide was undercut in the vicinity of the metal. Fig. 5.19 shows the electric field distribution for a device with a 30 nm gap, where the emitter voltage was set to 1 V while the other terminals were grounded. The largest electrostatic field was located at the bottom corner of the emitter terminal. Notice that when no undercut was present, this hot spot was larger and it extended into the oxide region.

Thus far, devices whose geometry had been carefully chosen to induce static field enhancement at the emitter apex have been described. Unfortunately, the structures proposed in this chapter were blunt to accommodate the hybrid plasmonic waveguide. Fig. 5.20 plots the static field enhancement factor as a function of gap width. Note that the same cut line as in fig. 5.10 was used to determine the field at the emitter tip. As expected, no static field enhancement due to geometry was present. The apparent enhancement was the result of the superposition of fields experienced

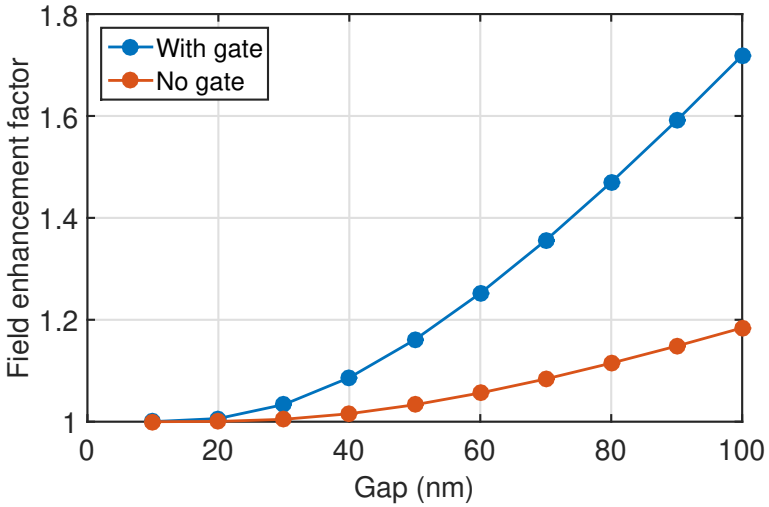


Figure 5.20: Static field enhancement factor as a function of gap width.

by the emitter tip E_{total}

$$E_{total} = E_{EC} + E_{EG} \tag{5.34}$$

where E_{EC} is the field due to the potential difference between the emitter and collector, and E_{EG} is the field due to the potential difference between the emitter and gate. The structure composed of the emitter and gate created a parallel plate capacitor. In this way, the magnitude of E_{EG} resembled that of its fringing field, in agreement with Fig. 5.20.

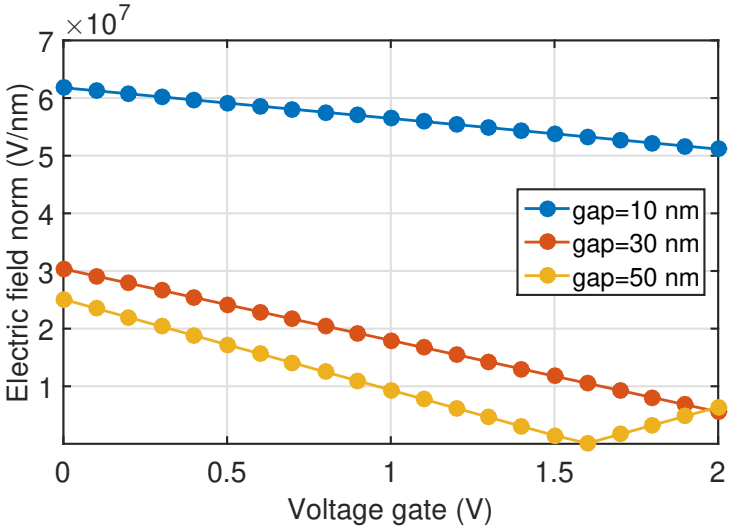


Figure 5.21: Maximum electric field norm on the emitter tip as a function of gate voltage for various emitter-to-collector gaps.

The effect of gating on the maximum electric field norm on the emitter tip for various gaps is demonstrated in Fig. 5.21. The maximum field was obtained when the gate was set to the same bias as the collector, resulting in the highest potential difference between the emitter and the other terminals. As the gate voltage was increased, the potential difference between the emitter and gate decreased, leading to a reduced maximum field on the emitter tip. Once the emitter and gate were at the same voltage, emission was controlled by the potential difference between the emitter and collector. If the gate voltage surpassed the emitter voltage, E_{EG} reversed direction

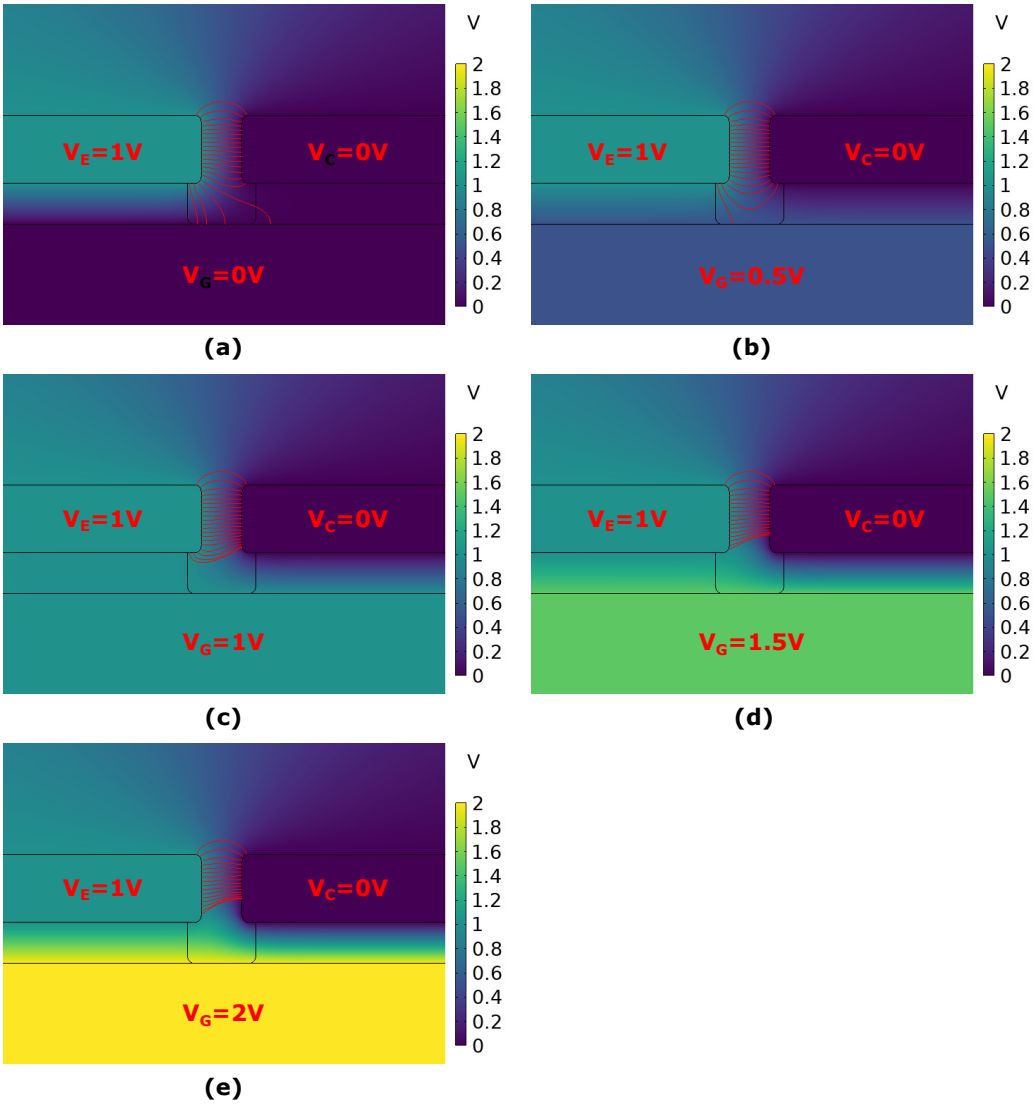


Figure 5.22: Potential distribution for various gate bias: (a) $V_G = V_C = 0$ V, (b) $V_G = V_E/2$, (c) $V_G = V_E$, (d) $V_G = 1.5V_E$, and (e) $V_G = 2V_E$. The red lines are streamlines illustrating the electron trajectory under the specified bias.

and impeded field emission, further reducing the maximum field at the emitter tip. It is also noteworthy that the gate was more effective at modulating emission in devices with wider gaps, as E_{EC} increased for smaller emitter-to-collector separations. For example, the gate modified the field at the emitter tip by more than an order of magnitude in a device with a gap of 50 nm only being able to modify the field by a factor of 1.2 when the gap was 10 nm. Lastly, Fig. 5.22 depicts streamlines based on the Cartesian components of the electric field for various potential configurations. These serve as an approximation for the electron trajectories leaving the emitter tip in a device in a device with a 30 nm gap. As expected, electrons were emitted to the collector and gate when both terminals were set to ground. With increasing potential of the gate terminal, electrons were discouraged from going to the gate. However, due to symmetry, it is important to note that at high enough gate biases, the gate may start emitting electrons to the collector if the separation between the emitter and collector is similar to that between the gate and collector (not pictured).

5.4 Device Fabrication

The devices were fabricated on SOI wafers, consisting of a 220 nm top silicon layer and a 2 μm buried oxide layer (SOITEC). Native oxide was removed using 6:1 buffered hydrofluoric acid (BHF) (Transene Company, Inc.), and the top silicon layer was doped with phosphorous using spin-on-glass (SOG) P-250 (Desert Silicon, Inc.). The SOG was applied by spin-coating at 500 rpm for 5 seconds and 3000 rpm for 35 seconds to achieve a thickness of approximately 210 nm. The sample was then baked on a hotplate for 15 min at 200°C and pre-deposition was carried out in a tube furnace at 700°C in a nitrogen atmosphere for 40 min. Subsequently, the SOG was removed by immersing the sample in BHF 6:1 for 5 minutes. Four-point probe measurements yielded a surface resistance of 6.12 ±0.98 kΩ, corresponding to a resistivity of 0.13 Ω·cm and a dopant concentration of 5.7×10^{16} cm^{-3}.

Photolithography was performed to electrically isolate individual devices, for which AZ 5214E (EMD Electronics) was spin-coated on the sample at 3000 rpm for 30 seconds and then baked for 1 minute at 110 °C on a hot plate. The pattern was exposed for 4 seconds at 15 mW/cm^2 using a contact mask aligner (Suss MicroTec MA6) in soft-contact mode at a wavelength of 365 nm, and subsequently developed in Microposit MF 319 developer (Rohm and Haas Electronic Materials) for 2 minutes. The pattern was transferred to the underlying Si via ICP-RIE (Oxford Instruments PlasmaLab 100 ICP-RIE 380) using SF_6 and C_4F_8 at a ratio of 35 sccm/57 sccm. The chamber pressure and temperature were set to 10 mTorr and

15 °C, respectively, while the CCP and ICP powers were set to 20 Watts and 1200 Watts, respectively. Afterward, the sample was immersed in acetone to remove residual resist.

The silicon was thinned down to a thickness of approximately 172 nm by means of a dry oxidation at 1000°C (Tystar Tytan Horizontal Diffusion Furnace) and subsequent oxide etch in BHF. This was followed by another dry oxidation to grow a thermal oxide layer approximately 30 nm thick, leaving an underlying Si layer of 160 nm. Additionally, the SiO_2 was annealed for 12 hours in a nitrogen atmosphere to improve its electrical properties and minimize gate leakage. Then, a 400 nm SiO_2 layer was deposited on a pair of opposite sides of the substrate where the emitter and collector terminals would later be located via PECVD (Oxford Instruments Plasmalab System 100). The deposition was carried out at a temperature of 350 °C and a pressure of 1000 mTorr with a flow rate of 170 sccm and 270 sccm of 5% SiH_4 in Ar and N_2O, respectively. The RF power generator was set to 20 Watts. The purpose of this thick oxide layer was to prevent shorting of the gate to the other electrical terminals during ultrasonic wire-bonding. Shadow-masking with a smaller piece of Si over the substrate was used to selectively deposit the oxide layer on the sides.

Standard EBL at 100 keV (EBPG 5200, Raith GmbH) with 950 PMMA A8 (MicroChem) was employed to pattern the junction region (which at this point was joined as shown in Fig. 5.24), electrical connections to the emitter and collector pads, optical gratings with a 626 nm period and 67% duty cycle, as well as small arrays of circles for later FIB alignment in the junction vicinity. A pre spin-coating clean with acetone and IPA was followed by a 5 minutes bake at 180 °C and PMMA spin-coating at 4000 rpm for 60 seconds and baking at 180 °C for 4 minutes. The same "bulk & sleeve" lithography technique used to fabricate the devices described in the previous chapter was used, with a 1700 μC/cm^2 dose and 150 nA beam current for the bulk, and 1000 μC/cm^2 dose and 10 nA beam current for the sleeve. Development was done in a 1:3 MIBK/IPA at room temperature for 30 seconds. Then, a 5 nm Ti adhesion layer and a 50 nm Au device layer were deposited via electron beam evaporation in a UHV evaporation chamber at a pressure of $\sim 10^{-7}$ Torr (Kurt J. Lesker Labline). The deposition rate for both materials was 0.5 Å. Lift-off was done in hot PG-remover, and sonication for a few seconds was also utilized to facilitate the process.

Photolithography was performed on thick oxide rails to define the gate contact pads, and then a BHF bath was used to remove the oxide for Ohmic contact with

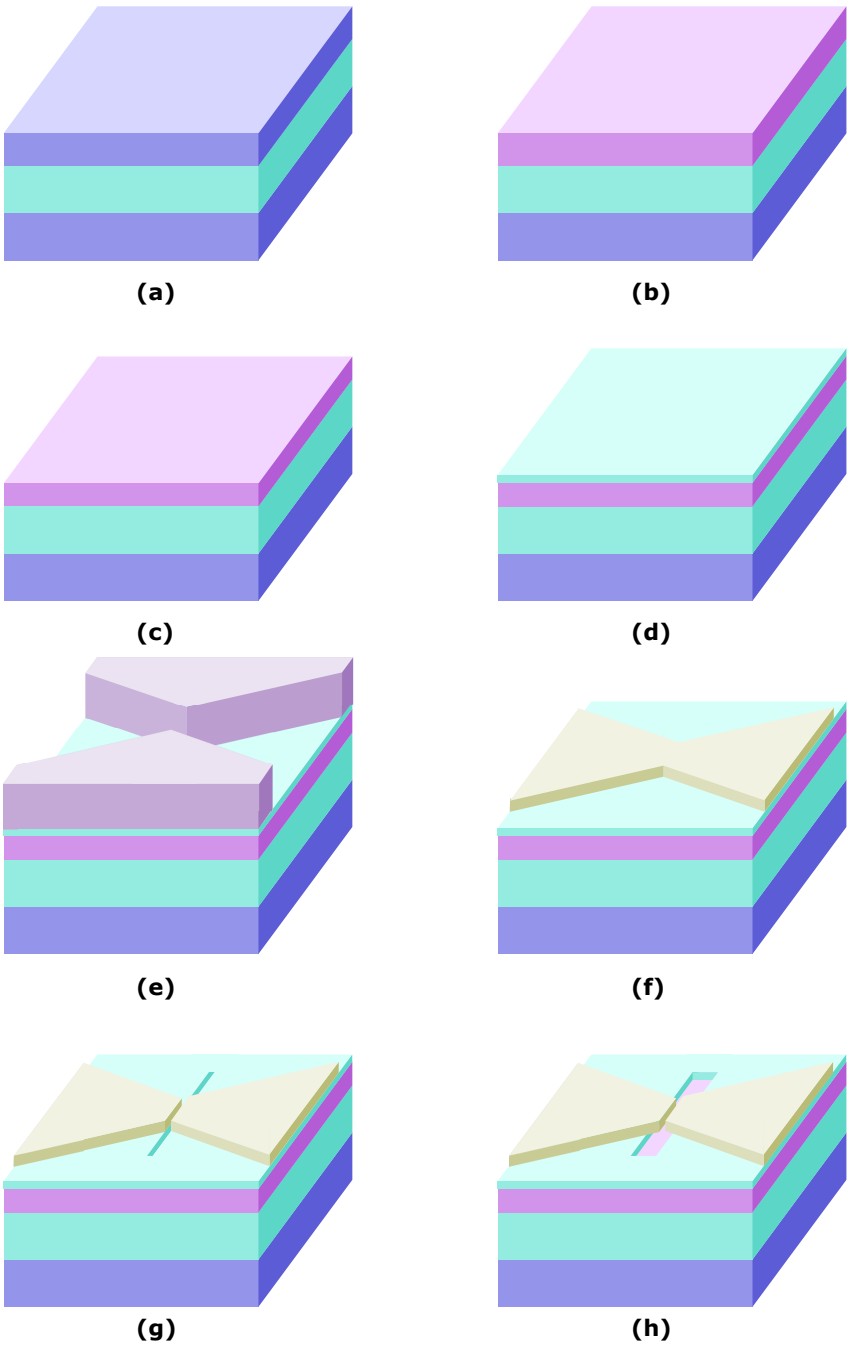


Figure 5.23: Main fabrication steps for plasmonically-enhanced field emission device: (a) initial SOI substrate, (b) doping of top Si layer, (c) Si thinning via thermal oxidation and subsequent HF etch, (d) thermal oxidation to grow spacer oxide layer, (e) EBL and development using 950 PMMA A8, (f) gold electron beam evaporation and lift-off, (g) Ne focused ion beam milling, and (h) undercut in HF of cut area. Note that the sketch is not to scale.

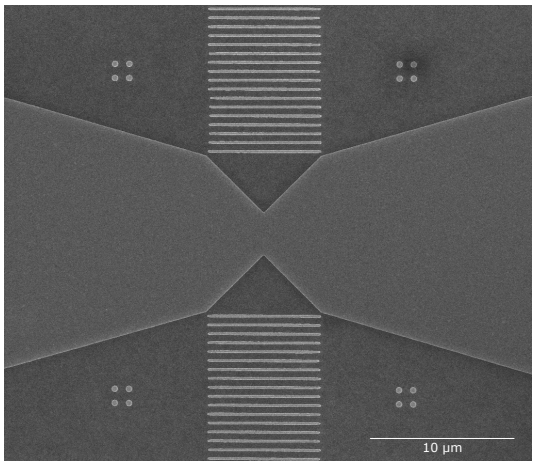


Figure 5.24: SEM of device before milling the gap between the emitter and collector. Grating and focusing marks are also visible.

the doped silicon layer. The photoresist was removed with solvent, and a second photolithography step was done to define the electrical contact pads. A 10 nm Ti adhesion layer and a 400 nm Au layer were electron beam evaporated to prevent punching through the 30 nm oxide layer during ultrasonic wire-bonding, followed by overnight lift-off in acetone.

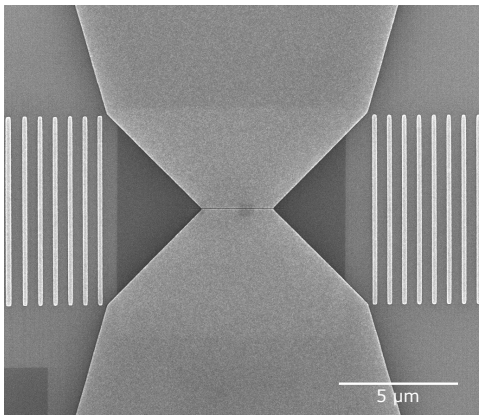
The plasmonic waveguides were defined using neon FIB lithography (Carl Zeiss Orion NanoFab) at 20 keV and a pressure of 4 $\times 10^{-6}$ Torr with a 6 mm working distance, 10 μm aperture, 2.5 pA current, 0.011 nC/μm dose, step spacing of 1 nm, and a dwell time of 10 μs. Fig. 5.25 shows top-view (a)-(b) and (c) 52° tilt view of SEMs of a representative device after being milled. To reduce the likelihood of dielectric breakdown due to the high fields, we removed the oxide in the gap area. 10 μm square boxes were defined with photolithography to enclose the gap region and thus protect the device. The devices were then immersed in 50:1 BHF for 80 seconds to undercut the gaps, followed by a solvent and oxygen plasma clean to remove the leftover photoresist. Fig. 5.25 (d) shows a cross-sectional view of a finished device with a 12 nm gap. Note that Pt was used to protect the gold surface during the fibbing process.

Finally, each individual device was wedge wire-bonded (WestBond 7476D-79) to a side-brazed dual in-line (DIP) ceramic package (Spectrum Semiconductor Materials CSB02842) using Al wires at a low power of 230 for the chip bonds to be as gentle as possible and avoid damaging the thin oxide layer. The power for chip carrier bonds was set to 350.

5.5 Results

The devices were loaded into a 4.5-inch-cube vacuum chamber and pumped to a pressure of about 3×10^{-6} Torr. To aid with the desorption of water molecules and other contaminants, the chamber walls were heated to a temperature of around 120 °C. The pins of the chip carrier were connected to a multi-pin electrical feedthrough on the vacuum chamber, which routed to a BNC patch panel. This setup allowed us to easily change the device under test.

We proceeded with the electrical characterization of our devices by first measuring the gate resistance via two separate contact pads on the doped Si layer located at either side of the junction region to guarantee its ohmicity (yielding a typical value of 4.2 kΩ). We used three sourcemeters (Keithley 2400 and 2410) with a common ground to simultaneously measure all currents flowing into and out of all terminals, monitoring surface leakage currents. Fig. 5.26 shows the schematic of this setup. The IV characteristic of the device was recorded by negatively sweeping the voltage of the emitter terminal while fixing the voltage of the other two terminals at ground (the emitter terminal was arbitrarily chosen due to symmetry). To clean the devices



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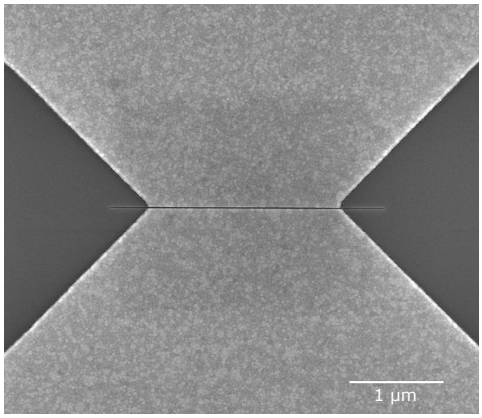

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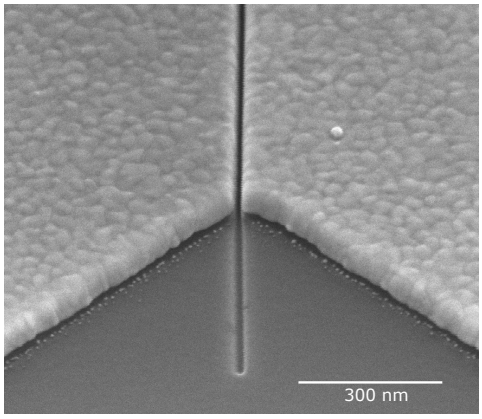

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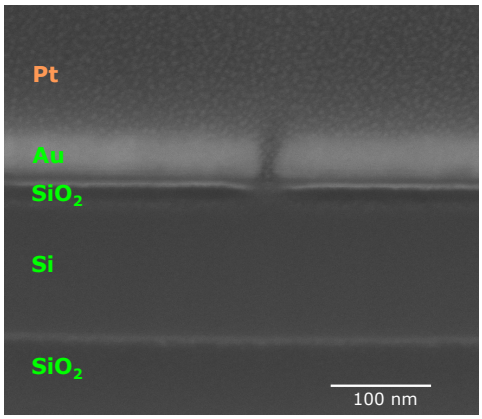


(d)

Figure 5.25: SEM of fabricated device: (a) top view of a device after milling the plasmonic waveguide, (b) zoomed-in view of the gap region illustrating the extent of the mill cut line, (c) side view at 52° of the edge of the plasmonic waveguide before HF undercut, and (d) cross-sectional view of the hybrid plasmonic waveguide of the finished device. The separation between the emitter and collector measured 12.1 nm in its narrowest region. Pt was used to protect the top surface of the device during ion cross-section milling.

from surface contaminants and obtain stable field emission, multiple forward and reverse sweeps were performed until no significant hysteresis between both sweeps was measured, as shown in Fig. 5.27.

The device exhibited a low turn-on voltage of ~1.5 V, likely caused by its larger emission surface compared to previously discussed devices. With a larger surface area, contaminants that could reduce the work function were more likely to be adsorbed, thus decreasing the onset of field emission. Nanoscale protrusions that experience higher field enhancements may have also contributed to the lower turn-

on voltage. The results were plotted in FN coordinates, yielding a straight line that indicated field emission as the electron transport mechanism.

We then tested the doped Si layer as an electrical gate, as shown in Fig. 5.28. The current on all three terminals is plotted as a function of emitter voltage for two different gate biases. No significant leakage into the gate terminal was observed. As expected, decreasing the potential difference between the emitter and gate increased the turn-on voltage due to the reduced electric field at the emitter.

We studied the effect of gate modulation on the emission current by applying a time-varying voltage signal on the gate terminal. It should be noted that the previous device blew up during testing; hence, these measurements were taken using another device with a slightly different IV characteristic. Fig. 5.29 shows the input voltage signal on the gate terminal and the measured currents as a function of time on all terminals. The FFTs of all measured data were computed to discern any modulation in the current that may hide under the flicker noise in the emission characteristic. The presence of a peak at the same frequency as the applied voltage signal on all measured currents confirmed successful electrical gate modulation. Unfortunately, the device blew up before tests at higher frequencies could be conducted.

We then analyzed the optical properties of the device. A schematic of the measurement setup is depicted in Fig. 5.30. Light from a C-band tunable laser (Keysight 81689A) was amplified by an erbium-doped fiber amplifier (EDFA) (Calmar Optcom) and launched into free-space via a fiber-optic collimator (ThorLabs F230FC-

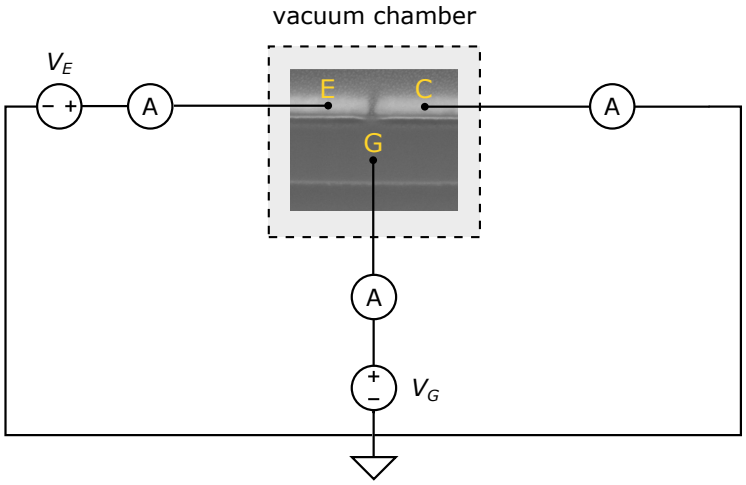
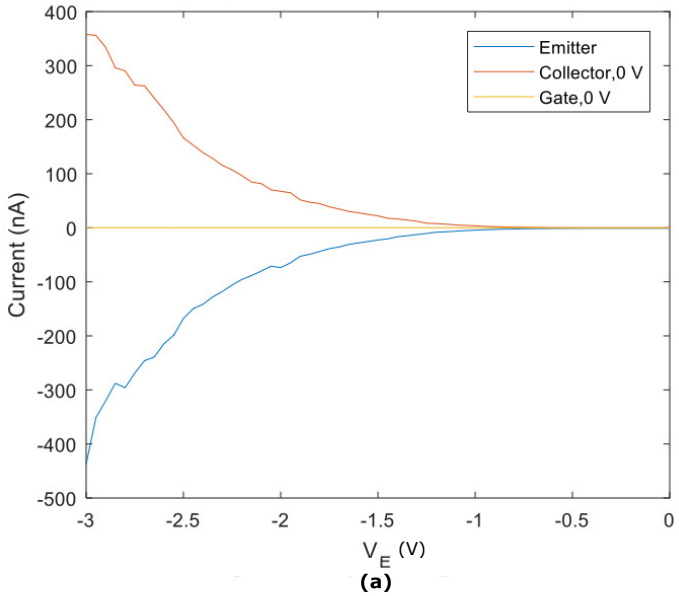
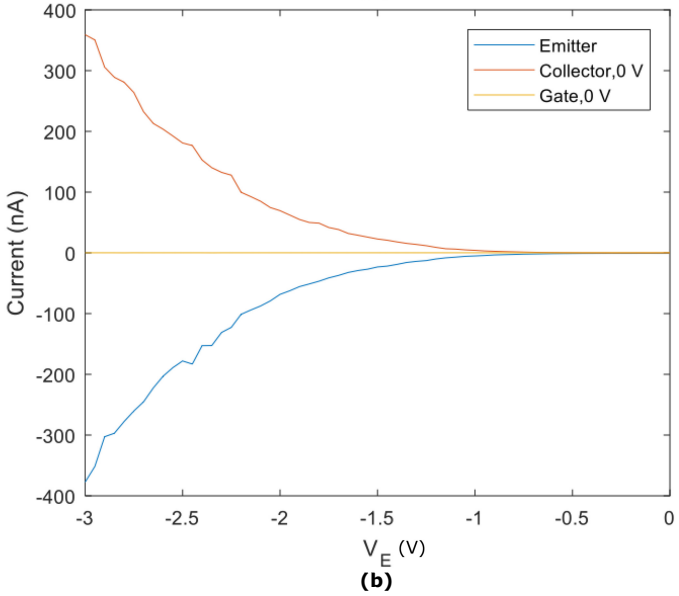


Figure 5.26: Schematic of the measurement setup to electrically characterize the devices. The collector was fixed at 0 V for all tests.

1550). A linear polarizer was included to eliminate any residual unwanted polarization. A periscope assembly was used to redirect and change the height of the beam, shown by a dotted line in Fig. 5.30, to guide it into the vacuum chamber where the devices were loaded. A half wave-plate was employed to shift the input beam polarization and maximize the power coupled into the grating. The beam was then focused onto the device input grating via a 100X near-infrared (NIR) objective (Mitutoyo M Plan Apo) mounted on a micrometer adjustable stage for fine focus adjustment. The free-space polarized light entered the vacuum chamber through a 7056 Borosilicate glass viewport (~ 90% transmission at 1550 nm). Reflected and out-coupled light was collected by the same objective and directed with a 50:50



(a)



(b)

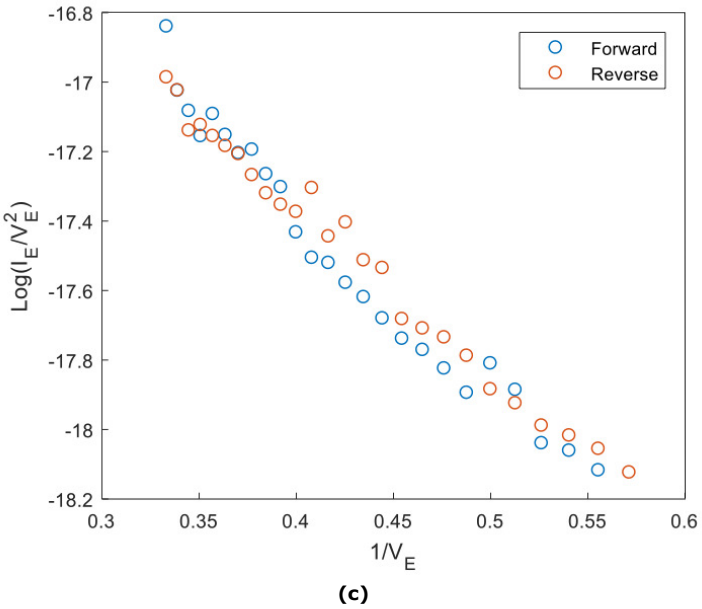


Figure 5.27: IV characteristic of a representative plasmonically-enhanced field emission device during (a) forward and (b) reverse voltage sweeps. The gate and collector were grounded. No leakage from the emitter into the gates was measured. In (c), the data for both sweeps is plotted in FN coordinates, indicating that field emission is the electron transport mechanism, as evidenced by the straight line.

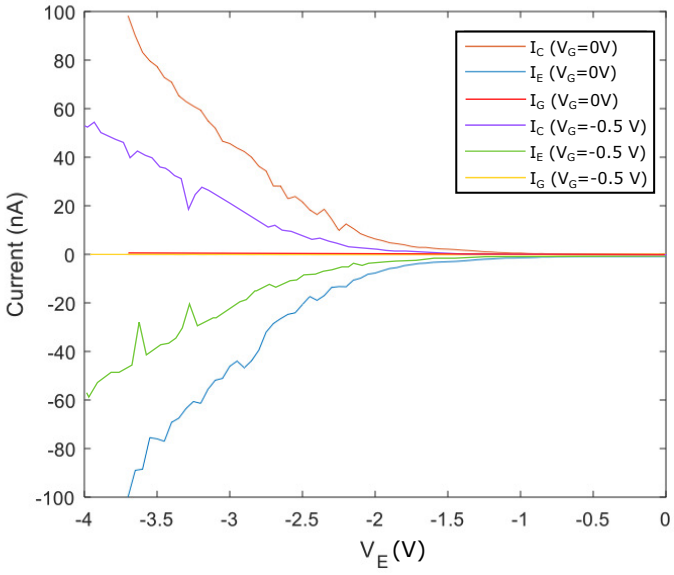
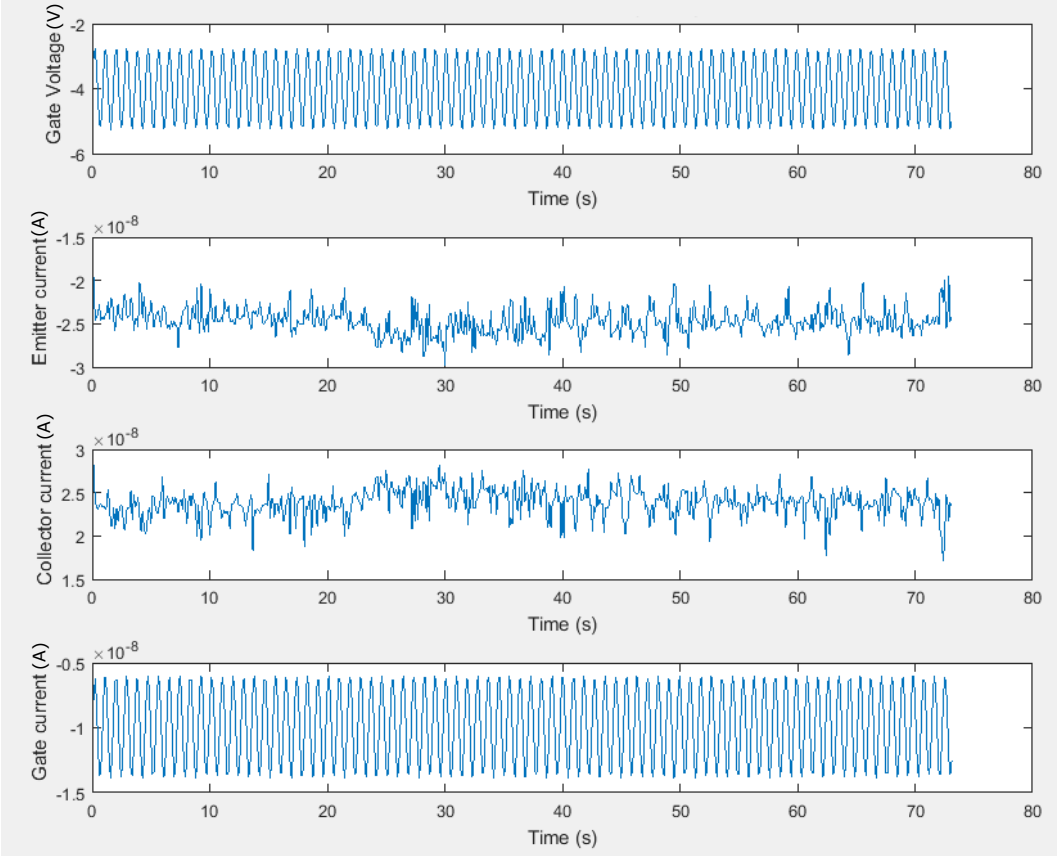


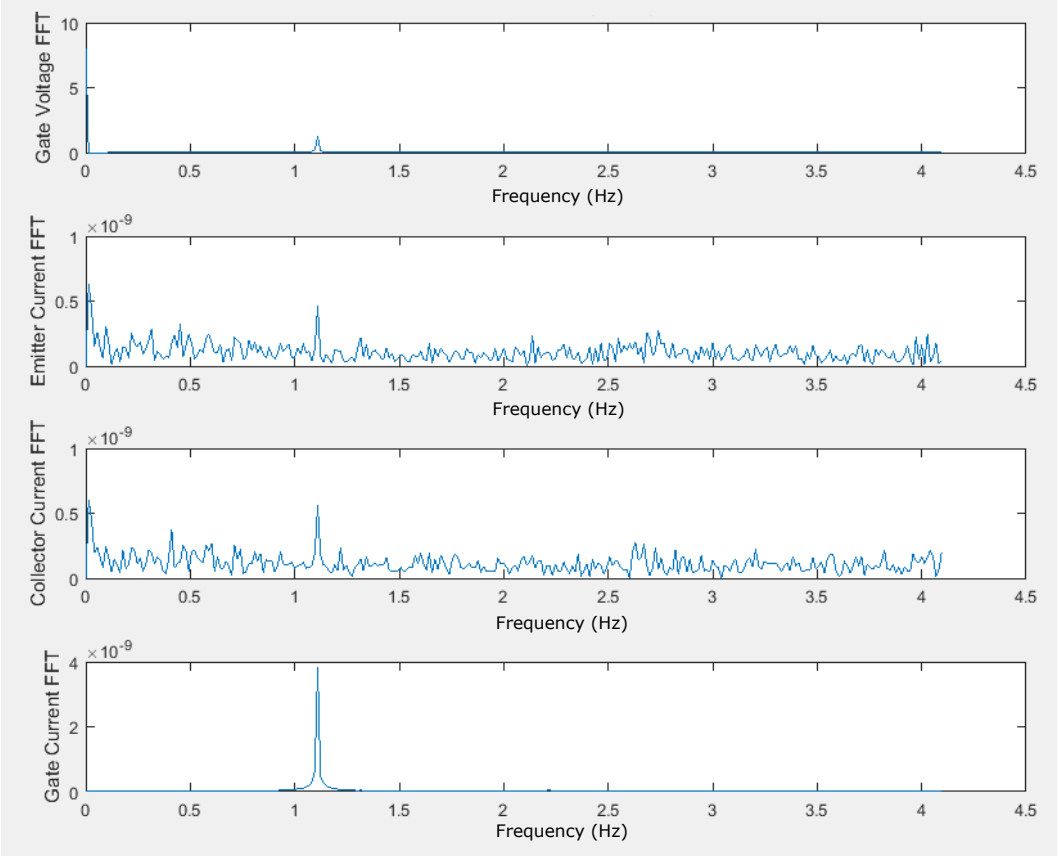
Figure 5.28: IV characteristic for two different gate biases: 0 V and -0.5 V. No significant leakage into the gate terminal was measured.

beamsplitter (BS) into a NIR camera (Merlin Indigo) for focusing the NIR beam. Natural density filters were added to the beam path as needed to avoid saturation on the camera. This free-space beam path is shown in red. Moreover, a white light source (ThorLabs SLS201L/M) was added to the beam path by means of a second 50:50 BS on a flip mount to navigate through the samples, as shown by the green line. To minimize signal loss during data acquisition, this second BS was removed from the beam path before the measurements. Furthermore, the vacuum chamber was mounted on a two-axis linear stage for navigation (Newport Model 401). Photos of the measurement assembly are shown in Fig. 5.31.

A mechanical chopper (ThorLabs MC1000) was added to the setup to modulate the input optical signal, which was also used as the reference frequency for a lock-in amplifier (Stanford Research Systems SR810 DSP) to accurately measure the optically-induced current from the collector terminal. The emitter and gate terminals' electrical connections were not modified. Similarly to the first electrical measurements, the emitter voltage was swept negatively while the gate and collector terminals were held at 0 V. The chopper speed was set to 3169 Hz. Fig. 5.32 shows



(a)



(b)

Figure 5.29: Effect of applying a time-varying voltage signal on the electrical gate. In (a), the signal applied to the gate and the measured currents in all three terminals as a function of time are shown. In (b), the Fourier transforms for all time-varying measured data were computed.

the effect of various EDFA output powers on emission. As the optical power was increased, emission was enhanced, demonstrating the sensitivity of the device to optical input.

The response of the grating coupler to the input polarization was also analyzed. Fig. 5.33 shows two NIR camera images when the 1550 nm laser was on and focused on the input grating. Coupling was minimized in (a), while it was maximized in (b). During coupling maximization, light entering the plasmonic waveguide was visible on the right side of the input beam. The isolated optically-induced current for the two perpendicular polarizations as a function of emitter voltage is shown in Fig. 5.34. The EDFA output power was set to 1000 mW. The results demonstrated the effectiveness of the grating, as little optically-induced current was measured when the coupling was minimized compared to when it was maximized.

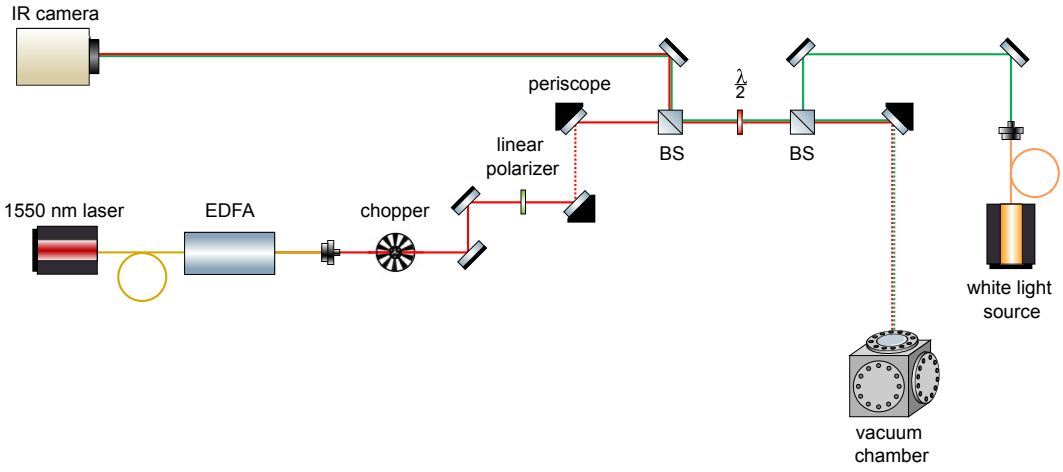


Figure 5.30: Schematic of the setup for optical measurements. The path of the 1550 nm free-space beam that is coupled to the device is shown in red. For sample navigation, a white light source is also focused onto the sample during measurement setup, as shown by the green line. The dotted lines represent an elevation change in the beam.

Unfortunately, after multiple consecutive runs, the device was destroyed, as shown in Fig. 5.35.

5.6 Discussion

In this chapter, we demonstrated a waveguide-integrated plasmon-assisted field emission device, developed on the SOI platform to achieve compatibility with existing Si photonics and reduce costs. The waveguide couples the TE photonic mode of an underlying Si slab waveguide to the plasmonic mode of a slot in a thin gold layer via an adiabatic taper that minimizes losses in the metal and avoids back-reflection and scattering. Geometry-induced nanofocusing results in efficient sub-wavelength spatial confinement of light and strong optical field enhancement. These high electromagnetic fields can modulate FN emission, which is exponentially dependent on the electric field perpendicular to the electron-emitting surface. Field emission can be readily integrated into the optical structure since thin metal layers serving as the hybrid plasmonic waveguide can also be used as emitter and collector terminals, while doping the Si photonic waveguide forms an electrical gate. This enables our proposed device to emit electrons both electrically and optically.

First, we measured the IV characteristics of the device under no illumination and successfully demonstrated low voltage operation due to the nanoscale gap between the emitter and collector. We verified that emission occurred via FN tunneling

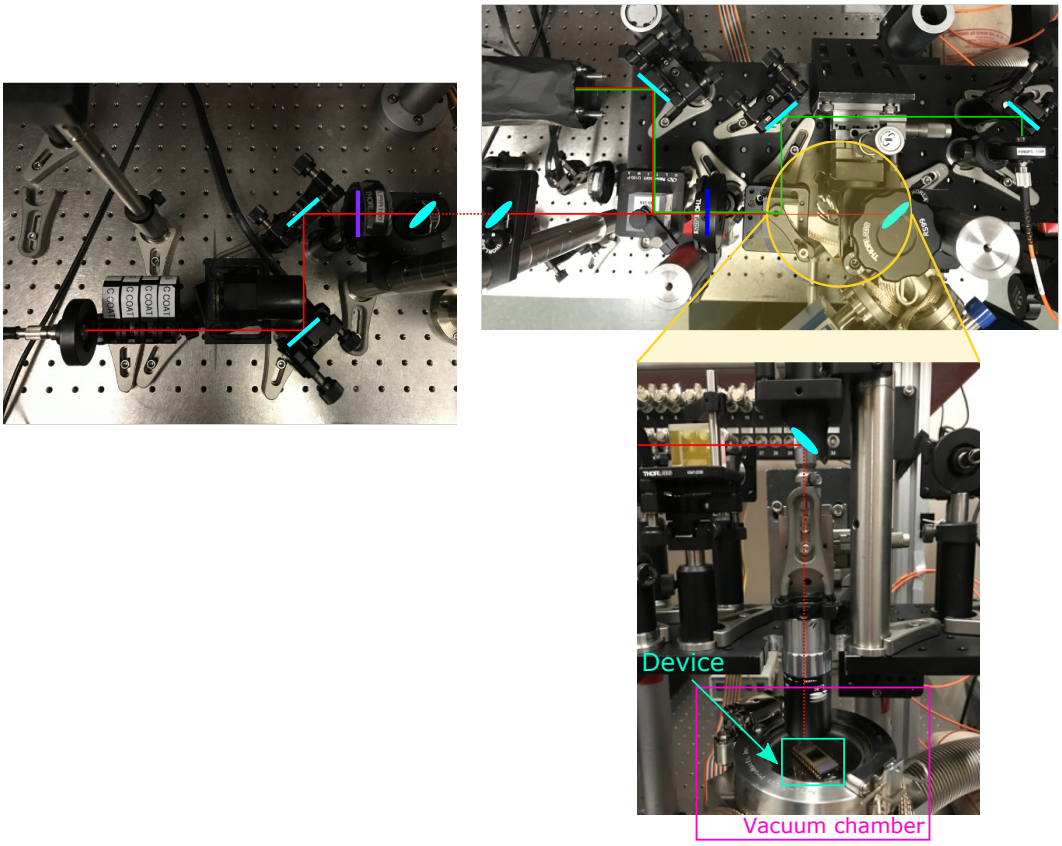


Figure 5.31: Photos of the (a) free-space optical setup and (b) electronic rack.

by plotting the IV characteristic in $1/V$ versus $\log(I/V^2)$ and excluded thermally-enhanced emission as a significant contribution due to the large electrode surface area and gold's high thermal conductivity. We would also like to note that the

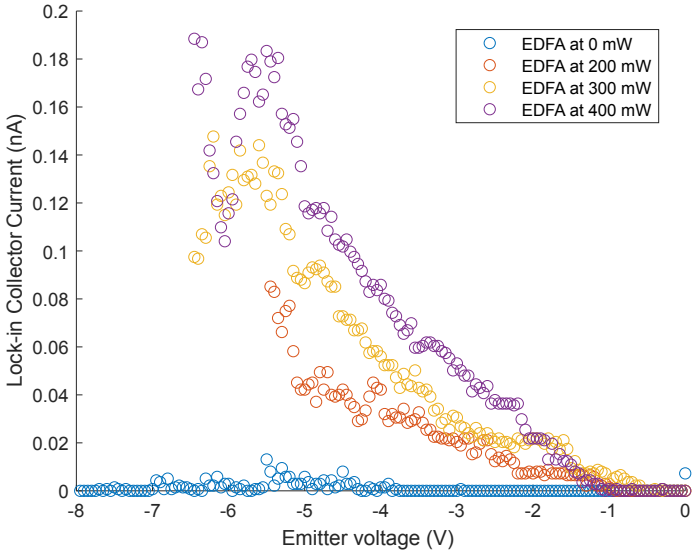


Figure 5.32: Optical response of the field emission device to various EDFA output powers as a function of emitter voltage.

underlying doped Si layer would have collected any thermally-generated leakage current.

We confirmed that the underlying doped Si layer acts as an electrical gate that modifies the maximum electric field at the emitter tip without significant leakage into the collector. We also applied a time-varying voltage signal on the gate and observed current modulation. Unfortunately, we measured a device capacitance of 1.49 nF, which severely limits our maximum operating frequency to less than 1 kHz. A way to significantly reduced the capacitance is to minimize the overlapping area between the vertical terminals, which forms a large parallel plate capacitor. By

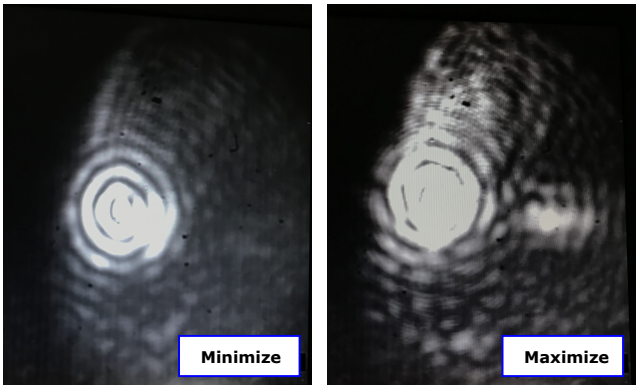


Figure 5.33: NIR camera images of the input beam when coupling into the grating is (a) minimized and (b) maximized via a 90° rotation of the half wave-plate.

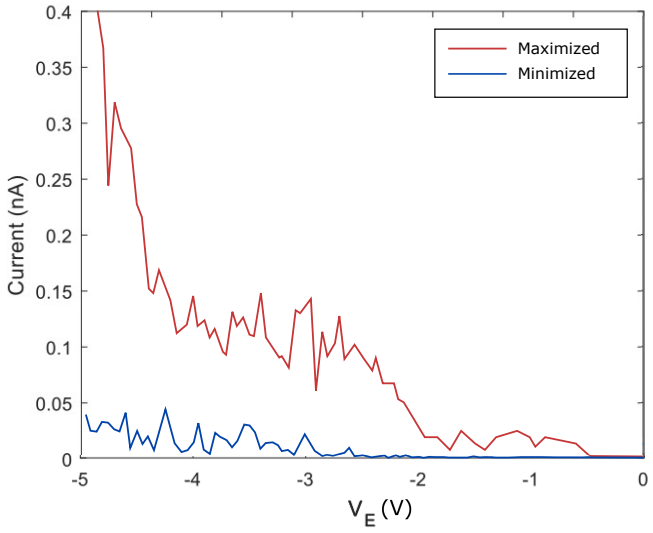


Figure 5.34: Optically-induced current measured by the lock-in amplifier as a function of emitter voltage when coupling into the grating is minimized and maximized.

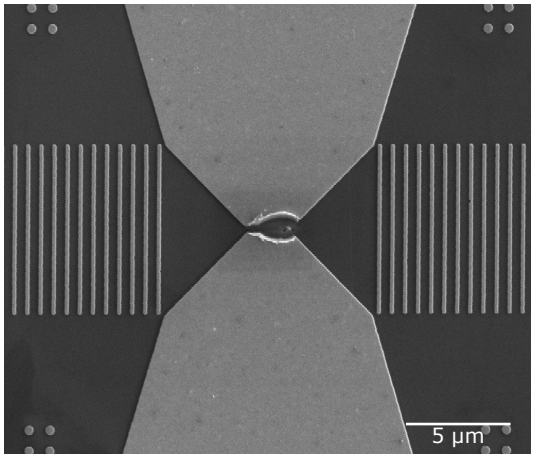


Figure 5.35: SEM of the blown device after multiple continuous measurements.

replacing the planar Si waveguide that constitutes the gate with a ridge waveguide, we could drop the capacitance to less than 1 fF.

Furthermore, we demonstrated optically-induced field emission by modulating the input optical signal with a chopper and using a lock-in amplifier to isolate the optically-induced contribution to the measured current. However, our optically-induced currents did not exceed 0.2 nA even at laser output powers of 400 mW. We characterized the loss in our free-space setup (up to the chamber) to be -7.57 dBm with an optical power meter mounted on a flip mirror. In addition, we employed a confocal setup to separately estimate the efficiency of our grating using our 100X

microscope, which yielded an 8% coupling efficiency. This resulted in an overall system loss of over -18.54 dBm, which did not include the losses from the coupling between the photonic mode and the hybrid plasmonic mode.

There are several ways to improve the system's efficiency. Firstly, we can remove the Ti adhesion layer for Au, as adhesion layers have been shown to significantly increase losses [8]. Additionally, we can replace our lossy gold flat gratings with curved Si gratings, which can increase the grating efficiency to 80% [15], as they significantly minimize the amount of incident energy scattered into higher order modes [15]. Curved Si gratings could be easily integrated into our system in an additional lithographic and etching step. Furthermore, we could replace the gratings altogether with edge coupling. A single-mode ridge waveguide would replace the slab waveguide, and an inverted taper clad in polymer would be used to couple light from a lensed fiber. This coupling mechanism comes with additional fabrication steps, as the waveguide and taper need to be patterned and etched on the Si layer and the polymer overlay for spot size conversion has to be selectively deposited. However, edge coupling eliminates free-space setup losses and improves the overall system coupling efficiency into the photonic mode to over 80% [25, 26], with losses mainly due to reflections at the chip facet and spot-size converter losses.

In Chapter 2, we discussed electron emission resulting from optical illumination. This process can be either field-driven, wherein the potential barrier is modulated and emission occurs by electron tunneling, or photon-driven, wherein the electrons acquire the necessary energy by photon absorption. Unfortunately, in practical devices, photoemission is still challenging, requiring lasers with very high powers or short wavelengths. For instance, in the mid-IR range, photoemission has been demonstrated in metallic nanostructures using femtosecond pulse irradiation at laser intensities on the order of 1 TW/cm^2 [27]. However, if SPPs are excited, laser intensities of about 1 GV/cm^2 [28] are sufficient due to the high plasmonic field confinement and enhancement, which facilitate electron emission and augment the ponderomotive forces caused by the large electric field gradients.

The application of a static bias to optical emission can further reduce the necessary fields to instigate vacuum electron transport by field-assisted photoemission. For instance, it has been demonstrated that static and optical fields under 1 GV/m are sufficient to cause emission from a tungsten tip with no plasmonic enhancement [29]. This is due to the strong non-linearity of field emission wherein a weak optical field can substantially enhance emission.

These experiments paved the way to combine field emission with plasmonically-enhanced photoemission in order to reduce the required applied voltages and laser power. For instance, Piltan et al. observed multiphoton emission by using a DC bias of 10 V and optical powers on the order of W/cm^2 at 785 nm in resonant plasmonic structures with optical field enhancements of 3 orders of magnitude [30]. Similarly, Turchetti et al. demonstrated that with the usage of the large static fields that arise in nanoscale vacuum gaps, ultra-fast optical field emission can occur in weak-field (under 10 V/nm) with a Keldysh parameter of $\gamma_k = 898$ in a plasmonic bow-tie nanoantenna with mid-IR excitation [31]. Additionally, the larger DC field compared to the optical field sets the emission direction from cathode to anode, preventing electrons from being back-accelerated at each half-cycle of the optical field. Although our proposed structure requires considerable optimization (our current optical field of ≈ 1 MV/m and the barrier-reduced work function of 4.3 eV result in a Keldysh parameter of about 8500), the concept of merging field emission and plasmonics at the nanoscale constitutes a major step towards the development of ultra-high-speed, low-power, nanoscale optoelectronic systems.

An interesting application for the proposed device is as an ultra-fast photodetector for THz electronics [32, 33], integrated microwave photonics [34], and carrier-envelope phase (CEP) detection [35, 36]. Thermoelectric detectors have a wide spectral bandwidth and are relatively inexpensive. However, they suffer from slow response times due to a phonon-dominated transport [37, 38]. Superconducting detectors have ps response times and single-photon sensitivity [39–41], but require cryogenic cooling, limiting system integration and increasing costs. Furthermore, conventional semiconductor photodetectors are laterally constrained by the diffraction limit and vertically confined by the required absorption depth, limiting their maximum speed and efficiency. Additionally, complex band structure engineering is required to effectively detect IR signals [42]. In this way, as field emission depends on the material work function and the maximum field at the surface, and the device capacitance can be adjusted by tuning its geometry, plasmonically enhanced field-assisted photoemission detectors can be sensitive, fast, and easy to integrate with practical systems.

Finally, we could pair our proposed optoelectronic devices with non-linear electro-optic polymers to convert electric signals into optical pulses at high frequencies. By using optical interconnects, Tbit/s signal transmission speed could be achieved. Therefore, thanks to the miniaturization provided by plasmonics, we could con-

ceivable develop full optical circuits on SOI platform with chip-level, high-density integration.

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Chapter 6

CONCLUDING REMARKS

Despite the revolution vacuum technology brought to the field of electronics in the early 20th century, leading to industrial growth and improvements in quality of life, it has since been almost entirely replaced by SSEs. This transition was spurred by the ease of fabrication, integration (e.g., ICs), long lifetime, and decreased power consumption of semiconductors, rather than any intrinsic advantage as a charge carrier transport medium. Moreover, novel applications and the demand for new capabilities led to an astonishing improvement in the fabrication techniques that progressively shrank the size of SSDs to achieve higher operating speeds following Moore's Law scaling.

However, the steady miniaturization and proposed complex architectures are hindering further optimization of semiconductor devices. Effective thermal management challenges are limiting their speed, power, and minimum dimensions, as inherent constraints imposed by electron mobility and bandgap are reached. In this context, the work presented in this thesis seeks to employ the same fabrication techniques that allowed SSDs to scale down to unprecedented dimensions to design nanoscale field emission devices that could address some of these issues.

Vacuum nanoelectronics offers several intrinsic advantages compared to SSEs. For instance, electron mobility in vacuum is higher than in any other material as it theoretically supports ballistic transport and suppresses phonon scattering. Moreover, device capacitance and impedance can be tailored through geometry design, which makes them highly appealing for high-frequency operations. Vacuum devices are also more robust to high-temperature environments and radiation exposure. In addition, while substantial electric fields are required to induce emission, low-voltage operation can be enabled by exploiting the nanoscale gaps that can be easily fabricated using state-of-the-art lithographic equipment, thereby resulting in increased efficiency and reduced power consumption. Furthermore, it is often claimed that the vacuum channel dimensions under the mean free path of the electron in air combined with sub-10 V bias to avoid ionization of gas molecules removes the need for packaging and allows atmospheric operation. Consequently, these devices have the potential to surpass the limitations of current technologies.

In this work, we experimentally demonstrated design paradigms for nanoscale field emission devices. We studied how various physical parameters affect the performance of vacuum devices and provided comprehensive guidelines for reproducible fabrication. Ultimately, these devices were designed for two distinct applications: high-temperature environments and high-frequency operation.

The development of robust technology capable of withstanding high temperatures is especially attractive to the aerospace, military, nuclear, and automotive industries, among others. To tackle the usual SSEs' shortcomings in such extreme conditions, we developed suspended lateral two- and four-terminal vacuum field emission devices. Constructed with tungsten due to its heat-resistant capability, we strove to increase the resistance of the leakage current pathways that arise at high temperatures by removing the underlying solid substrate. Moreover, we opted for planar architectures for their convenience in manufacturing with current lithographic capabilities and conventional semiconductor fabrication techniques.

Furthermore, two distinct architectures were considered for high-frequency operation. The first proposal relied solely on the fast response of field emission and consisted of a two-terminal multi-tip array for frequency conversion. To improve its efficiency, we analyzed the effect of thin-film coating with Pr to reduce the work function and boost the emission current. For the second proposal, we augmented FN emission with plasmonics, developing plasmonically-enhanced field emission optoelectronic devices at telecommunication wavelengths on SOI platform. By utilizing the strong confinement and significant optical field enhancement of plasmons, we sought to create devices that can be modulated electrically and optically at dimensions smaller than those of purely photonic architectures.

Nonetheless, we have also demonstrated that several challenges must be addressed to realize the potential of the proposed field emission devices for practical applications and be competitive with modern semiconductor technology. However, we are optimistic that further refinements will let us overcome these limitations and enable us to combine the inherent advantages of vacuum as a transport medium with the integrability and fabrication ease favoured by SSEs to revolutionize high-speed telecommunication and provide resilient, long-lasting operation in harsh conditions. While in the short-term vacuum field emission devices could work alongside SSEs and complement it, in the long-term we aspire to create full vacuum electronic circuits and systems. Overall, the research and development of nanoscale field

emission devices is an exciting field and holds significant potential for advancing the field of electronics.