The Class E/F Family of Harmonic-Tuned Switching Power Amplifiers

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Abstract

A new family of harmonic-tuned switching amplifiers is introduced having the beneficial features of the class-E tuning while allowing improved performance to be achieved through additional harmonic tuning. This E/F family may be tuned to achieve the ZVS/ZdVS switching features characteristic of the class-E amplifier and, like the class-E tuning, accounts and compensates for the effect of the switch parallel capacitance. By tuning one or more overtones to the class-F^{-1} tuning, however, the switching waveforms may be improved, lowering the peak voltage and reducing the RMS current. Additionally, the tolerance to large switch parallel capacitance is generally improved so that a larger switching device may be used, allowing reduction of the on-resistance. Due to these factors, the efficiency of E/F amplifiers is expected to exceed that of class E.

To demonstrate these advantages, methods of estimating the optimal efficiency of switching amplifiers using waveform properties are given. A general solution technique is then presented which allows the calculation of the ZVS tuning requirements and the resulting switching waveforms for an arbitrary harmonic tuning. Using these two tools, switching waveforms and resulting efficiency estimates are calculated for E/F amplifier tunings, which are then compared to class E.

Finally, potential application areas of the E/F technique are explored, and measured results of several first-generation E/F amplifiers are presented. Aside from efficiency benefits, E/F amplifiers also may achieve load-invariance, dual- and multi-band operation, high volumetric power densities, and efficient integrated circuit implementation using the Aoki distributed active transformer power combining structure.

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Chapter 1 *Introduction*

Due to the ever-increasing demand for communications, wireless connectivity, industrial power, and power conversion technology, the demand for high-efficiency, high-frequency power amplifiers has never been greater. Wireless markets demand high-efficiency amplifiers for portable units in order to extend battery lifetime. Wireless base-stations and other high-power RF transmitters require improved efficiency in order to increase reliability and lower the cost of heat-sinking. Industrial power applications such as RF plasma generation and RF induction heating units demand high efficiency to reduce power consumption and eliminate expensive forced-flow cooling techniques. Power converter applications in both the industrial and consumer markets demand amplifiers (and rectifiers) achieving higher efficiency, smaller size, and higher-frequency thereby allowing smaller, more efficienct power converters with faster response times.

In order to meet these demands, designers must select the technologies best suited to meet their various requirements. Unfortunately, there is often a trade-off between amplifier efficiency and amplifier linearity. In many applications, such as industrial RF power and power converters, linearity of the amplifier is not important and high-efficiency modes of operation such as class-C or class-E are attractive. In applications requiring significant amplification linearity, such as most wireless communication products, traditional transconductance amplifier technologies such as class-A and class-AB [1] are commonly used. Unfortunately, these techniques severely limit the power efficiency, making the desired cost and size reductions difficult to achieve.

In applications for which AM/AM and AM/PM distortion are tolerable [2] or compensated for [3], harmonic-tuned saturated and switching amplifiers provide a

higher-efficiency alternative. Amplifiers operating in class-E and class-F modes may routinely achieve efficiencies above 80%, sometimes approaching 100%, making them attractive when efficiency is paramount.

Unfortunately, only two types of amplifier tunings appropriate for high-frequency operation have been studied in the literature. Class-E amplifiers [4,5] have found most application as a higher-performance alternative to class-D amplifiers, due to their compensation for transistor output capacitance and elimination of turn-on switching losses. Additionally, the class-E design may be implemented with a relatively simple circuit. As a result, this class has been implemented over a wide range of frequencies from HF to microwave with great success [e.g. 7-14].

Class F [15,16] and its recently popularized dual, class F^{-1} [17,20], have been presented and developed primarily as a means of increasing the saturated performance of class AB or class-B designs. As a result, the operating frequencies attainable have usually been somewhat higher, but the performance limitations due to the tuning requirements [25] and the lack of a simple circuit implementation suitable for nearly-ideal switching conditions have made this design a poor alternative at frequencies where class-E can be implemented.

Nevertheless, it has been noted [e.g. 17] that the waveforms which could in principle be achieved by class F and/or F^{-1} would allow performance benefits over class-E designs. Additionally, limitations of the class E approach at high frequencies due to a finite tolerance for large transistor output capacitance have been identified [21].

This dissertation presents a new family of harmonic tunings with the promise of achieving the promised performance benefits of class F^{-1} in the frequency range wherein the transistor is switching nearly ideally. Additionally, this tuning method may increase the amplifier's tolerance to large transistor output capacitance, improving the high frequency performance and extending the frequency range of this new tuning beyond that of class E. This new E/F family of tunings unifies class E and class F^{-1} into a single

framework, and demonstrates varying degrees of trade-off between the simplicity of class-E and the high-performance of class F^{-1}. All members of the E/F family have exact time-domain solutions, can be made to achieve class-E switching conditions, and have circuit implementations wherein the output capacitance of the switch is explicitly accounted for. Finally, some members of this tuning family have properties making them more appropriate for use in applications where class-E tunings might be difficult or impossible to implement.

1.1 Organization of the Dissertation

Chapter 2 presents a background discussion of the nature and limitations of amplifier power efficiency and a comparison between the efficiencies of most commonly used amplifier classes. The low efficiencies achievable in non-switching amplifier classes is quite limited, motivating the introduction of switching amplifiers as discussed in Chapter 3. This chapter also presents background material, but with more depth and with a focus on switching amplifiers. General properties of switching amplifiers are presented, as well as more specific investigations of the well-known D and E switching amplifier classes.

Chapter 4 discusses some simple methods to compare the performance (i.e. efficiency and gain) of different switching amplifiers from the shapes of the voltage and current waveforms through the active device. Since some design choices affect the efficiency, the correct choices for optimal performance are derived, so that the comparisons made between tunings will take into account the optimal parameter choices for each tuning.

Chapter 5 introduces a new technique for analytical or numeric determination of the voltage and current switching waveforms for any user-defined harmonic tuning. Using this technique, harmonic tuning strategies may be treated generally, rather than being solved in a case-by-case basis as has been done in the past. The technique is

computationally efficient and variations of the technique allow for the calculation certain important design parameters, avoiding the need to discover them empirically.

Chapters 6 and 7 introduce the new E/F family of switching amplifier tunings. This family, which is a generalization of the class E and class F^{-1} concepts, is the result of applying additional harmonic tuning to the basic class-E amplifier circuit. Using the solution technique of Chapter 5 and the estimation techniques of Chapter 4, the performance of tunings of this family are compared to that of class E, showing that performance may be significantly improved in certain applications. Finally, implementation strategies for these tunings are proposed.

Lastly, Chapter 8 highlights some of the applications where the E/F technique may allow for performance enhancement or desirable new design features. Several prototype amplifiers from 7MHz to 2.4GHz using E/F tunings are presented, illustrating that the technique is already being successfully applied in demanding applications.

Chapter

2

Efficiency of Power Amplifiers

One of the most important aspects of a power amplifier is its *power efficiency*, i.e. the ratio between the useful power generated by the amplifier and the power that the amplifier consumes. By increasing this ratio, the amplifier will consume less supply power and require less heat sinking, allowing a reduction of battery size and cost of portable units. Similarly, this reduces the operating cost of high-power equipment, and the manufacturing costs associated with heat sinking. For instance, if an amplifier with efficiency η is operated in a situation where the battery charge is limited to energy E_{charge}, and output power of P_{out} is required, the operation time t_{charge} is limited to:

$$t_{charge} = \eta \cdot \frac{E_{charge}}{P_{out}} \tag{2.1}$$

In other words, increase in efficiency results in a proportional increase in battery lifetime. A more striking condition is where a very large output power is desired, but the design limitation is a maximum tolerable dissipated power P_{diss}. In this case, the maximum achievable output power is:

$$P_{out} = \frac{\eta}{1-\eta} \cdot P_{diss} \tag{2.2}$$

Thus, increased efficiency can result in a substantial increase in output power in industrial applications where heat removal is a driving factor in the design. Normalized results of battery discharge time and dissipation-limited output power are plotted in Fig. 2.1.

In order to improve the efficiency, it is necessary to identify the power dissipation mechanisms in the amplifier and reduce their effect to whatever degree possible. This chapter provides a brief overview of power amplifier efficiency issues, focusing on the

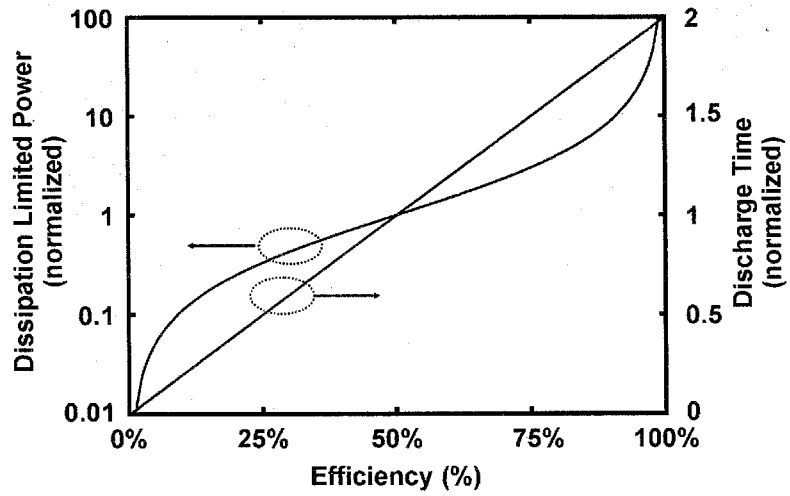


Figure 2.1: Dissipation-limited output power and battery discharge time vs. amplifier efficiency. Values are normalized to the performances of a 50% efficiency amplifier.

special case of the *narrowband* power amplifier, i.e. an amplifier whose operation can be reasonably assumed to be periodic.

2.1 Amplifier Loss Mechanisms

In the most general sense, an amplifier is a frequency conversion device, wherein dc power is converted into power with a spectrum reproducing that of its input signal with some reasonable degree of accuracy. Thus the amplifier receives dc power, receives some amount of ac power to its input port, and supplies ac power to the load. An ideal amplifier[1] would require an infinitesimally small amount of input power, and convert all of the dc power consumed into ac power delivered to the load. The ability to approximate these characteristics is measured by various amplifier efficiency measures.

In order to perform the frequency conversion, the amplifier requires one or more active devices, and a passive – usually linear and time invariant – network which provides

1. The ideal amplifier would have one additional property, namely the ability to produce an output exactly reproducing its input. This property is quantified by various distortion figures of merit.

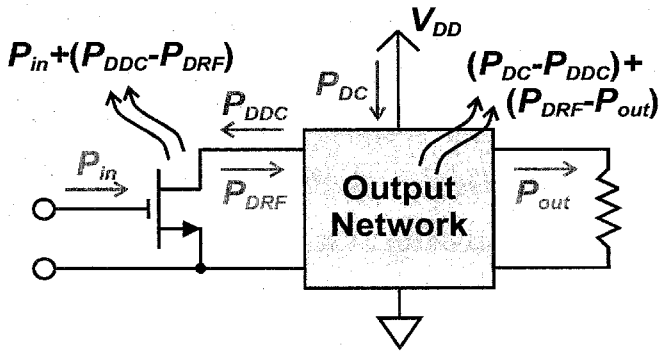


Figure 2.2: Power flow in a generalized power amplifier.

connection to the dc power supply and any necessary impedance transformation between the active device(s) and the load. Such an amplifier is shown in Fig. 2.2. Normally, some method of input matching is also required. This aspect of amplifier design will be largely ignored in this work since its effect on amplifier efficiency is relatively small, as long as care is taken [22], and acceptable methods are well known [e.g. 1,23].

The power flow for the amplifier begins with dc power P_{DC} entering the passive network. Of this power, some is dissipated by the network and the remainder, P_{DDC}, is supplied to the active device. The active device receives this dc power and some amount of input ac power, P_{in}. It dissipates some portion of this power, and converts the remainder into ac power, P_{DRF}, which it delivers to the output network. The output network, in turn, dissipates some portion of this power and delivers the remainder, P_{out}, to the load. The object of power amplifier design is to minimize the power loss associated with each step of this power transfer while at the same time achieving a desired level(s) of output power P_{out} and a tolerable level of distortion.

2.1.1 Drive Power Loss

The amplifier requires some reference signal in order for it to determine the output waveform to generate. This signal consists of power delivered to and dissipated on the device input port. The active device then generates a similar signal with greater power

which it delivers to the output passive network. The gain – the ratio G_D between the input power P_{in} and the generated power P_{DRF} – is determined by a number of factors, including the device technology, bias conditions, frequency of operation, and the characteristics of the load presented to the device. Usually the gain of a power amplifier is relatively high, and so the input power loss is of secondary importance to other losses.

2.1.2 Device Conduction Loss

All of the popular solid-state active devices in use today are controlled resistors of some sort. To be more specific, the core of the device consists of a resistor[1] across the output port whose conductance is varied by the instantaneous values of the input and output waveforms. A simple device model appropriate for both bipolar and field-effect devices is shown in Fig. 2.3. Although this model incorporates the device output capacitance C_d, the analysis is generally simpler if this component is treated as being part of the output passive network, so that the resistive control mechanism can be dealt with independently of the passive parasitic components. Thus, in the following analysis any reference to the active device current should be understood to mean the current I_D through the controlled resistance.

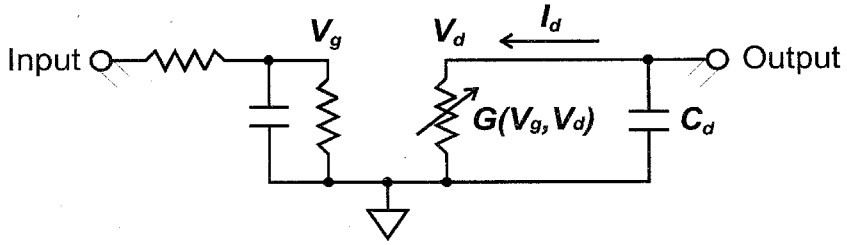


Figure 2.3: Simple device model disregarding feedback parasitics.

The consequences of the resistive nature of the control mechanism in active devices has important implications in the design of high-efficiency power amplifiers. First, any

1. Most treatments introduce the transistor as a dependent **current source** rather than a dependent resistor. If the device operates as a current source, the resistor model is valid using $R(t) = V(t)/I(t)$.

power absorbed by this resistance is truly dissipated, rather than stored for later recovery, motivating the desire to have as little power as possible being absorbed into the drain of the device at all times. This knowledge also allows the simple calculation of the power dissipated by the device as the product of the drain voltage V_d and the drain current I_d. To find the average power loss, the mean value of this product should be used. In the narrowband case, the waveforms may be assumed to be periodic with frequency f_0 and so this average, P_{DD}, may be taken over a single cycle:

$$P_{DD} = P_{DDC} - P_{DRF} \approx f_0 \cdot \int_0^{1/f_0} (I_d V_d)\, dt \tag{2.3}$$

In most cases, the conduction loss of the amplifier is the largest source of dissipation, as the designs which are most commonly used tend to have significant times during which the drain voltage and current attain high values simultaneously. If reducing the loss were the only consideration, however, it would be desirable to ensure that whenever the drain current is significant that the drain voltage is nearly zero and vice-versa.

2.1.3 Output Network Loss

Although not strictly necessary in all applications, amplifier design tends to demand the use of a network of passive, usually linear, devices between the active device and the load. The primary purpose of this network is usually to perform an impedance transformation so that the device is presented an impedance more compatible with the device characteristics and design goals than the desired load impedance. The second purpose served by these networks is to provide some level of signal filtering so that out-of-band distortion products and spurious signals are not delivered to the load. Finally, in high-efficiency amplifiers employing harmonics in the voltage and current waveforms, the network provides waveshaping by selectively tuning the harmonic impedances.

To see why impedance transformation is necessary, it is worthwhile to consider its effect on amplifier efficiency and maximum output power. Consider a narrowband class-A amplifier wherein the active device is a MOSFET operated as a controlled current source with output resistance r_{out}. Suppose that the drain voltage V_d must not exceed 10V due to device breakdown limitations and that it is desired to achieve 1W of output power into a 50Ω load. The requiredc ac voltage signal on the load may be computed:

$$v_{ac} = \sqrt{2 \cdot (50\Omega) \cdot (1W)} = 10V \tag{2.4}$$

Unfortunately, if the load presented to the transistor is the 50Ω load, this ac voltage signal in class-A operation requires a peak voltage of at least $2v_{ac}$ or 20V. In fact, the maximum output power achievable in class-A operation under these constraints is:

$$P_{out} = \frac{(5V)^2}{2 \cdot (50\Omega)} = 0.25W \tag{2.5}$$

Now consider the case wherein it is desired to achieve the 1W output power using a fixed supply voltage of 100V using a MOSFET capable of withstanding 250V. If the 50Ω load is directly presented, the voltage swing will again be ±10V and the current swing will be ±200mA. The resulting minimum bias current for class-A operation is 200mA, and so the dc power consumed from the supply will be:

$$P_{dc} = (100\text{V}) \cdot (200\text{mA}) = 20\text{W} \tag{2.6}$$

This represents an efficiency of only 5%, due primarily to the fact that the dc voltage is unnecessarily high for the small ac voltage swing required. If the supply voltage is fixed by other constraints, the efficiency must be improved by means other than reducing the supply voltage.

In order to achieve the desired output power and efficiency respectively, the 50Ω load must be transformed into a more desirable impedance. In the first case, the impedance presented to the MOSFET must be lowered, so that the output power can increase without increasing the peak voltage. In the second case, the impedance must be made higher, so

that the voltage can achieve a full ±100V drain voltage swing without increasing the output power.

This transformation can be accomplished by any number of well-known passive networks, such as coupled-inductor transformers, resonant lumped element networks, and many varieties of transmission line networks. Each has the same purpose, shown in Fig. 2.4, that being to transform its input power at one impedance into output power at another.

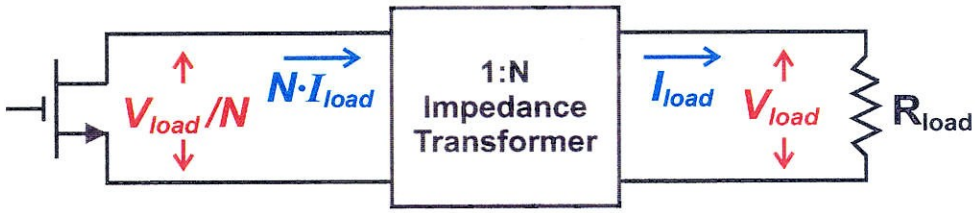


Figure 2.4: Impedance transformer component.

As will be shown later in this chapter, the efficiency of an amplifier generally improves with increasing generation of harmonics. Even in the event that harmonics are not intentionally generated to improve efficiency, the nonlinearity of most active devices is often sufficient to generate enough harmonic power to be troublesome in communications applications. It is usually undesirable to allow these harmonics to reach the load, and so the output passive network is often also used to filter the undesirable harmonic components out of the signal. In harmonic-tuned amplifiers, the network not only serves to reject the harmonic transmission to the load, but also will present desired impedance levels to the active device at some of the harmonic frequencies, allowing the designer a means to control the waveform shapes.

Unfortunately, the impedance transformation and filtering functions do not come without cost. The network will introduce additional power loss, degrading the overall efficiency. Generally, the efficiency of this network gets worse as the impedance

transformation ratio is increased, the harmonic rejection is increased, and the number of tuned harmonics is increased.

2.2 Efficiency Measures

There are several measures of amplifier efficiency in general use today. The simplest is probably the *drain (collector) efficiency*, denoted here as η_D, which is defined as the ratio between the output power P_{out} and the dc power consumed P_{DC}:

$$\eta_D \equiv \frac{P_{out}}{P_{DC}} \tag{2.7}$$

This measure is appropriate in situations where the amplifier gain is high or where the input power comes at no cost, and can therefore be safely ignored. Additionally, the drain efficiency is useful in evaluating the conduction loss in isolation of input power loss. Since the drain efficiency ignores the effect of the input power, this measure helps measure the effectiveness of the amplifier in avoiding dissipation on the controlled resistance of the output port. Since this loss is significantly affected by choices made by the designer, such as the class of operation used and the harmonic tuning employed, the drain efficiency measures the effectiveness of this design choice in isolation from the device gain.

Somewhat less commonly used, but of perhaps more physical significance, is the *total efficiency*, denoted here as η_T, which is simply the ratio between the output power P_{out} and the sum of all powers delivered to the amplifier. Using the simplified model of Section 2.1, this would be:

$$\eta_T \equiv \frac{P_{out}}{P_{in} + P_{dc}} \tag{2.8}$$

By truly evaluating the effectiveness of the net power flow in the amplifier, this measure can be used to measure the effectiveness of an amplifier in reducing the need for heat removal. This can be seen by noting that the total dissipated power is a simple function of the total efficiency and the output power:

$$P_{diss} = P_{DC} + P_{in} - P_{out} = \left(\frac{1}{\eta_T} - 1\right) \cdot P_{out} \tag{2.9}$$

Finally, the most commonly used measure is the *power added efficiency*, or PAE. This measure is computed as the ratio between the added power $P_{out} - P_{in}$ and the dc power:

$$PAE \equiv \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.10}$$

An equivalent form for PAE is expressed in terms of the amplifier drain efficiency η_D and gain G:

$$PAE = \frac{P_{out}}{P_{DC}} \cdot \left(1 - \frac{P_{in}}{P_{out}}\right) = \eta_D \cdot \left(1 - \frac{1}{G}\right) \tag{2.11}$$

To see why this measure is useful and physically significant, consider a chain of N amplifiers, each with the same drain efficiency η_D and power gain G. The efficiency of such an arrangement can be computed. Counting from the final amplifier, k=1, to the first amplifier k=N, the input power of the k^{th} amplifier is found to be:

$$P_{in}(k) = \frac{P_{out}}{G^k} \tag{2.12}$$

The output power of each stage is simply the input power of the next stage:

$$P_{out}(k) = \frac{P_{out}}{G^{k-1}} \tag{2.13}$$

The dc power consumed by each amplifier can be computed using the drain efficiency:

$$P_{dc}(k) = \frac{P_{out}}{\eta_D \cdot G^{k-1}} \tag{2.14}$$

Thus the total dc power consumed by the chain is:

$$P_{DC} = \sum_{k=1}^{N} P_{DC}(k) = \left(\frac{P_{out}}{\eta_D}\right) \cdot \left(\frac{1 - \frac{1}{G^N}}{1 - \frac{1}{G}}\right) \tag{2.15}$$

The total input power is simply the input power to the first stage:

$$P_{in} = \frac{P_{out}}{G^N} \tag{2.16}$$

Now the three efficiency measures may be computed:

$$\begin{aligned} \eta_{D,\,chain} &= \eta_D \cdot \left(1 - \frac{1}{G}\right) \cdot \left(\frac{G^N}{G^N - 1}\right) \\ &= PAE \cdot \left(\frac{G_{chain}}{G_{chain} - 1}\right) \end{aligned} \tag{2.17}$$

$$\begin{aligned} \eta_{T,\,chain} &= \eta_D \cdot \left(1 - \frac{1}{G}\right) \cdot \left[\frac{G^N}{G^N - (1 - \eta_D)}\right] \\ &= PAE \cdot \left[\frac{G_{chain}}{G_{chain} - (1 - \eta_D)}\right] \end{aligned} \tag{2.18}$$

$$PAE_{chain} = \eta_D \cdot \left(1 - \frac{1}{G}\right) = PAE \tag{2.19}$$

As can be seen from (2.19), the PAE of the amplifier chain is identical to the PAE of each individual amplifier in that chain. Additionally, if the gain of the chain is sufficiently high, both the drain efficiency and the total efficiency of the chain approach the PAE of the individual amplifiers used, as can be seen from (2.17) and (2.18). Thus PAE is an effective measure of the efficiency that could be achieved using a chain of similarly performing amplifiers.

2.3 Some Important Relationships

Before discussing in detail the various strategies which are commonly employed to implement power amplifiers, some helpful theorems regarding fundamental power amplifier limitations will be presented. Again, it should be understood that the amplifiers in question are assumed to be narrowband in nature, i.e. the desired output can be accurately modelled as a slowly changing sinusoidal signal so that the signals present in the circuit can be assumed to effectively consist only of this fundamental frequency sinusoid and its harmonics. Additionally, the output passive network is assumed to be a linear and time-invariant (LTI) circuit. There is assumed to be only one power source present, which is a dc voltage (or current) generator. Although some of the conclusions drawn in the next few sections may seem trivial, it is important to keep them in mind as even these simple conclusions provide fundamental limitations on power amplifier performance.

2.3.1 Power Flow Relationships

A generalized power amplifier can be seen in Fig. 2.5. The amplifier consists of a three port LTI matching network with the active device connected to port one, the dc power supply connected to port two, and the load connected to port three. The voltage and current on the device port are denoted V_{dev} and I_{dev} respectively, the voltage and current on the supply port are denoted V_{sup} and I_{sup} respectively, and the voltage and current on the load port are labelled V_{load} and I_{load} respectively.

As the amplifier is narrowband, the voltages and currents on these ports can all be represented by a Fourier series consisting of the desired fundamental frequency f_0 and its harmonics:

$$V_{dev} = V_{DC} + \sum_{k=1}^{\infty} v_k \cdot \cos(k \cdot \theta + \alpha_k) \tag{2.20}$$

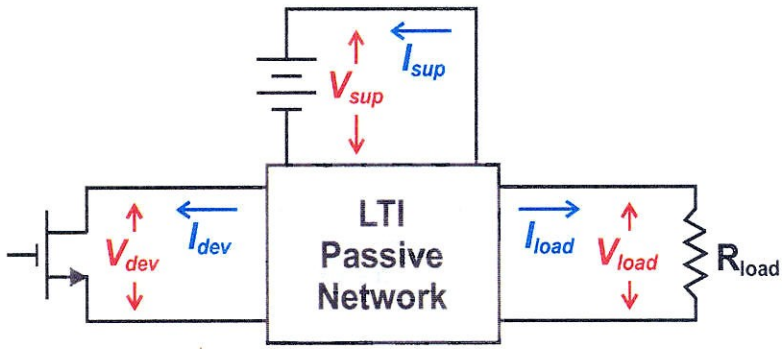


Figure 2.5: Generalized single-transistor power amplifier.

$$I_{dev} = I_{DC} + \sum_{k=1}^{\infty} i_k \cdot \cos(k \cdot \theta + \beta_k) \tag{2.21}$$

where the v_k's are the voltage harmonic amplitudes, the i_k's are the current harmonic amplitudes, the α_k's are the phases of the voltage harmonics, the β_k's are the phases of the current harmonics, V_{DC} is the dc voltage, I_{DC} is the dc current, and θ is the normalized time variable defined as:

$$\theta = 2\pi f_0 t \tag{2.22}$$

Since the matching network is both passive and LTI, it cannot generate power at any harmonic, nor can it convert power from one harmonic to another. It can, however, dissipate some portion of the power at each frequency. These conditions can be stated precisely:

$$\underbrace{P_{dev}[k] + P_{sup}[k] + P_{load}[k] + P_{diss}[k] = 0}_{\forall k \in \{0 \ldots \infty\}} \tag{2.23}$$

where $P_{dev}[k]$ is the power delivered to the active device at the k^{th} harmonic, $P_{sup}[k]$ is the power delivered to the dc supply at the k^{th} harmonic, $P_{load}[k]$ is the power delivered to the load at the k^{th} harmonic, and $P_{diss}[k]$ is the (non-negative) power dissipated by the matching network at the k^{th} harmonic.

The dc power source enforces a constant voltage (or current) on its port, and therefore it cannot dissipate or deliver power except at dc. Since it is the only power source in the system, presumably it is delivering power, and so $P_{sup}[0]$ must be negative:

$$\underbrace{P_{DC}[k] = 0}_{\forall k \neq 0} \tag{2.24}$$

$$P_{DC}[0] < 0 \tag{2.25}$$

The load is passive and linear, and so the power absorbed at each harmonic must be non-negative:

$$\underbrace{P_{load}[k] \geq 0}_{\forall k \in \{0 \ldots \infty\}} \tag{2.26}$$

The active device, being the only non-LTI device in the system, is the only means by which power can be converted from one frequency to another. It is not, however, a power source, and so the net power absorbed by the device must be non-negative:

$$\sum_{k=0}^{\infty} P_{dev}[k] \geq 0 \tag{2.27}$$

There are several conclusions to be drawn from (2.23) - (2.27). The first observation is that the power absorbed by the active device $P_{dev}[k]$ must be non-positive except for dc since there are no other power sources in the system at these frequencies:

$$\underbrace{P_{dev}[k] \leq 0}_{\forall k \neq 0} \tag{2.28}$$

Constraints on the output power can now be found. Combining (2.23) with (2.24) and (2.27). Keeping in mind that $P_{load}[1]$ is the useful generated output power P_{out}:

$$P_{out} \leq P_{dev}[0] + \sum_{k=2}^{\infty} P_{dev}[k] - P_{diss}[1] \tag{2.29}$$

This relationship is already useful, showing that generation of harmonic power by the active device degrades the efficiency, consisting of (at best) merely wasted power at undesired frequencies. This will have an effect on the selection of device waveforms later. The relationship can be strengthened by utilizing (2.28):

$$P_{out} \leq P_{dev}[0] \tag{2.30}$$

which simply indicates that the output power cannot exceed the dc power supplied to the active device. Although seemingly obvious, this also has important implications on waveform selection.

2.3.2 Waveform Limitations: Power Consumption at Harmonics

The results of the previous section, although useful, can be made more explicit in terms of the actual active device waveforms. In particular, using (2.20) and (2.21), the $P_{dev}[k]$ terms can be explicitly specified in terms of the harmonic components of the device waveforms:

$$P_{dev}[0] = V_{DC}I_{DC} \tag{2.31}$$

$$\underbrace{P_{dev}[k] = \frac{1}{2}v_k i_k \cos(\alpha_k - \beta_k)}_{\forall k \neq 0} \tag{2.32}$$

Using these relations, (2.29) becomes:

$$P_{out} \leq V_{DC}I_{DC} + \frac{1}{2} \cdot \underbrace{\sum_{k=2}^{\infty} v_k i_k \cos(\alpha_k - \beta_k)}_{\text{all negative terms}} - P_{diss}[1] \tag{2.33}$$

Similarly, (2.30) becomes:

$$P_{out} \leq V_{DC}I_{DC} \tag{2.34}$$

These two relationships establish what should be intuitive, but should still be kept closely at hand during the quest for high-efficiency amplification. Since power must be conserved, the device waveforms will always be such that the output power is at most equal to the dc power consumed minus the power generated at the harmonics.

Since generated harmonic power leads to reduced efficiency, it is advisable to establish the conditions which can be imposed in order to eliminate this loss. From (2.32), the conditions on the harmonic components rendering the generated power at that harmonic equal to zero can be found by inspection. If either the voltage or the current amplitude at that harmonic is equal to zero then the power generated is zero. Likewise, if the phase angle between the voltage and current is $\pm 90°$ there will be no power generated at this frequency. Since the design of the matching network is under the control of the designer, and since the network connected to the active device is LTI, the characteristics of the load are uniquely specified by the input impedance presented by the network to the active device. This impedance $Z_{in}[k]$ is independent of the active device or the drive conditions, and places necessary constraints on the relationship between the voltage and current harmonics:

$$Z_{in}[k] = \frac{v_k}{i_k} \cdot [\cos(\alpha_k - \beta_k) + j \cdot \sin(\alpha_k - \beta_k)] \tag{2.35}$$

Using the above conditions on the waveforms, the conditions on the load network making the harmonic dissipation zero can be found. If the voltage amplitude is zero (and the current is nonzero), the input impedance is short-circuit. if the current amplitude is zero (and the voltage is nonzero) the impedance is open-circuit. If the phase angle difference is $\pm 90°$ then the impedance is purely reactive. The only other possibility is if both the voltage and the current are zero due to the harmonic not being excited by the device. In this case, the input impedance at that harmonic has no effect. Again, the conclusion reached is obvious in retrospect: By adjusting the input impedances at the harmonics to be either purely reactive, open-circuit, or short-circuit, the waveforms will

necessarily be such that the power generated at the harmonics will be zero. The only other means to eliminate harmonic power generation is to assure the harmonic is simply not excited by the device.

One final waveform constraint is that, due to the essential resistive nature of the active device, the device voltage and current waveforms must at all times have the same sign as each other. If at any time, the voltage and current were to have opposite sign, the device would be delivering instantaneous power into the load.

In summary, the following principles should be kept in mind:

Physicality constraints:

- The output power may not exceed the dc power delivered to the device.
- The output power may not exceed $v_0 \cdot i_0$.
- Waveforms should not be such that harmonic power need be delivered to the device.
- The waveforms should be such that $v_k i_k \cos(\alpha_k - \beta_k)$ is less than or equal to zero for all $k \neq 0$.
- The voltage and current waveforms should always have the same sign, so that the voltage is never positive when the current is negative and vice-versa.

Efficiency considerations:

- Generation of harmonic power by the active device either increases the dc power consumed or decreases the output power, thereby reducing efficiency.
- To minimize the harmonic power generated, the device waveforms should either have no voltage at that harmonic, no current at that harmonic, or the phase angle α-β between the voltage and current components at that harmonic should be $90°$.
- Harmonics for which current or voltage exist in the waveforms should be tuned so that the device is presented with a pure reactance, a short-circuit, or an open-circuit.

Failure to keep in mind these seemingly obvious lessons can result in a designer choosing device operating conditions that are either non-physical or that have performances below initial expectations.

2.4 Efficiency of Common Amplifier Classes

2.4.1 Transconductance Amplifiers

The simplest and most common types of amplifiers are transconductance amplifiers. In these amplifiers, the active device is operated as a current source whose current is dependant almost entirely on the voltage presented to its input. This is made possible by the propensity of solid state devices to contain large regions of their transfer characteristic wherein the output current is largely independent of the output voltage[1].

Typical output characteristics of a solid state active device, applicable to both bipolar and FET devices, is shown in Fig. 2.6. The plot consists of three regions, called here the *triode region,* the *transconductance region*, and the *breakdown region*. In the triode region, the device conducts large currents with relatively little voltage drop, and the current is very sensitive to the drain voltage V_D, increasing rapidly as this voltage is increased. In this region, the device acts effectively as a controlled resistor. Upon applying sufficiently large drain voltage, the device enters the transconductance region, wherein the device's current becomes insensitive to the drain voltage, being determined almost entirely by the input voltage V_g. In this region, the device acts effectively as a controlled current source. The voltage at which the transition occurs between the triode and transconductance regions is generally known as the *knee voltage*, V_k. As can be inferred from Fig. 2.6, this voltage is usually to some degree dependant on the drive level.

1. Most of the analysis in this section is also applicable to linear amplifiers constructed of devices, such as triode vacuum tubes, that do not effectively behave as transconductors. Such devices are encountered rarely today, so the specific case applicable to solid state devices is presented here.

Upon application of enough further voltage, the device enters a breakdown regime. This region is almost always to be avoided as it is accompanied by very high currents in conjunction with high voltages, and so leads to high power dissipation and often performance degradation or destructive failure of the device. The voltage at which the transition into this region occurs is usually referred to as the *breakdown voltage*, V_{bk}. Like the knee voltage, this value can also be somewhat dependant on the drive level.

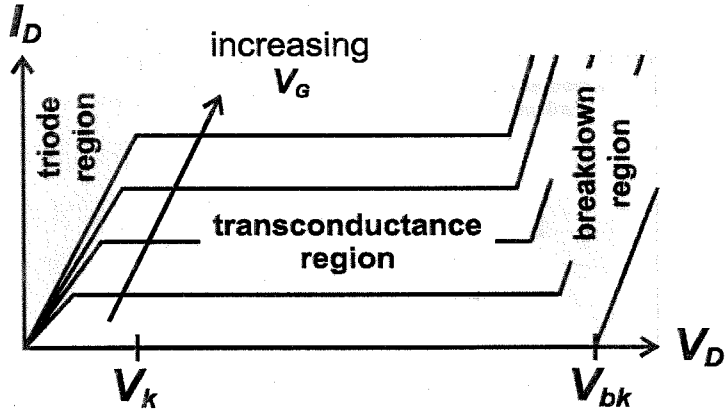


Figure 2.6: Typical active device output port characteristics.

The fourth "region" of operation is the *subthreshold* region. This region is entered by lowering the input signal level sufficiently so as to effectively reduce the device's conductivity to zero. In this region, any voltage up to the breakdown voltage will essentially conduct no current.

Typical transconductance amplifiers are constructed using a circuit functionally similar to the circuit in Fig. 2.7. The active device is used as a current source, driving a controlled current into a load network consisting of a harmonic filter and the resistive load to be driven. The harmonic filter is constructed so that its impedance at the fundamental frequency is very high, whereas the impedance at the harmonics is low. Typically, this filter is a parallel inductor/capacitor filter tuned to be resonant at the fundamental frequency. Using this arrangement, the impedance presented to the active device at the fundamental frequency is simply the load resistance, whereas the impedance at the

harmonics is much lower due to the filter. This has the effect of forcing the voltage across the output of the active device to be effectively sinusoidal for almost any current waveform driven by the active device, as the fundamental harmonic component of the current waveform is passed into the load resistance, whereas the higher harmonics of the current are passed through the much lower impedance of the filter and are therefore their representation in the voltage waveform is significantly reduced.

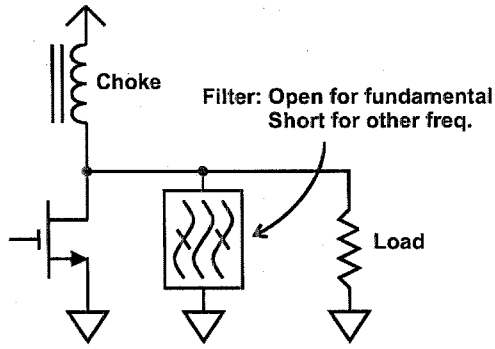


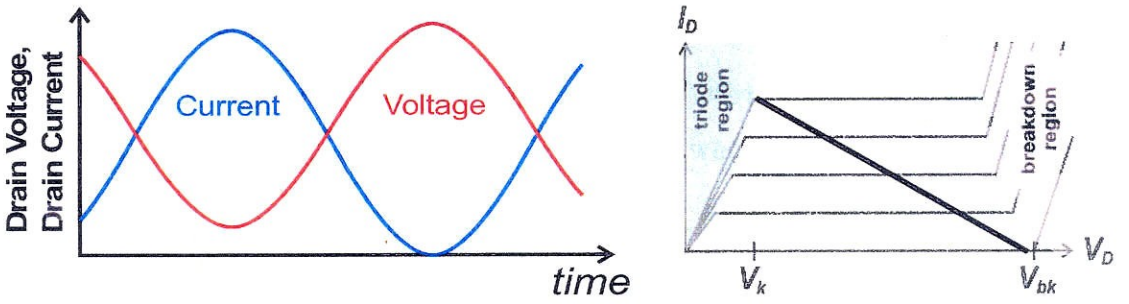
Figure 2.7: Transconductance amplifier circuit topology.

As the essential shape of the voltage waveform is constrained, the primary means whereby the amplifier performance may be varied is by modification of the current waveform used. A more complete discussion [1] of the various considerations involved in this choice would surely exceed the scope of this work, but the following sections highlight the effect that the most common choices have on the amplifier efficiency.

2.4.1.1 Class A

In class-A mode, the active device is biased so that the device is continuously conducting current at all times. Ideally, the current through the device should duplicate exactly the shape of the input voltage signal and the dc bias current should be sufficient to ensure that the device continuously conducts positive current, and that the device remains at all times in the transconductance region, i.e. the voltage never falls below the knee voltage. Additionally, the waveforms should have a sufficiently low peak voltage to keep

the device out of the breakdown region. For the narrowband case, class-A waveforms and load line are shown in Fig. 2.8.



(a) (b)

Figure 2.8: Class-A drain waveforms (a) and load line (b).

The maximum efficiency of a narrowband class A amplifier can be computed readily. The current waveform in this case is a sinusoid varying from zero to $2I_{dd}$:

$$I_D = I_{DD} \cdot (1 + \sin(\omega t)) \tag{2.36}$$

Similarly, the voltage is a sinusoid varying from the knee voltage V_k and V_{bk}:

$$V_D = \left(\frac{V_{bk} + V_k}{2}\right) - \left(\frac{V_{bk} - V_k}{2}\right) \sin(\omega t) \tag{2.37}$$

Using (2.36) and (2.37), the dc power delivered to the transistor is:

$$P_{dc} = I_{DD} \cdot \left(\frac{V_{bk} + V_k}{2}\right) \tag{2.38}$$

Similarly, the rf power delivered to the load is:

$$P_{out} = \frac{1}{2} \cdot I_{DD} \cdot \left(\frac{V_{bk} - V_k}{2}\right) \tag{2.39}$$

The drain efficiency is then found to be:

$$\eta_D = \frac{P_{out}}{P_{dc}} = \frac{1}{2} \cdot \left[\frac{1 - V_k/V_{bk}}{1 + V_k/V_{bk}}\right] \tag{2.40}$$

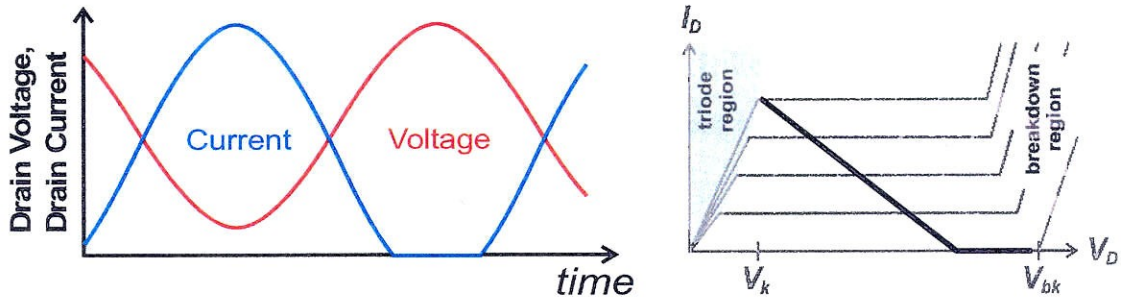
2.4.1.2 Class AB, class B, class C

In order to further increase the efficiency of the transconductance amplifier, it is necessary to have at least one of the waveforms be non-sinusoidal. One common approach is to keep the voltage waveform the same as in the class-A approach, but change the current waveform so that there are periods of time wherein the active device is in a non-conducting state.

There are several advantages of this technique. First, the distortion of the current waveform can be readily generated by simply lowering the input bias to the active device so that the input voltage is sufficiently low during a part of the cycle to turn the device fully off (i.e. bring it into the subthreshold region). Thus, a sinusoidal input signal may still be used, and the input bias adjusted to vary the time during which the device is open. Additionally, by having a sinusoidal voltage waveform, the harmonic filtering requirements are relaxed.

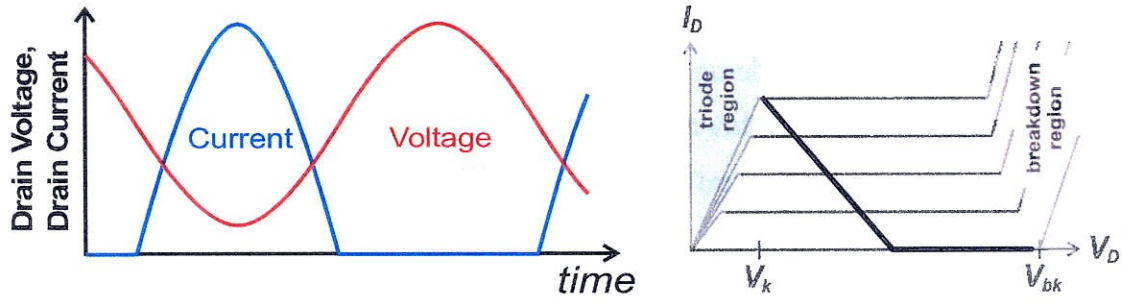
The waveforms and load-line for such an amplifier are shown in Fig. 2.9. The voltage waveform is sinusoidal as in the class-A case, but the current waveform has a period of time during which the current is zero (i.e. the device is acting as an open-circuit). As can be seen, this occurs during the time where the voltage is maximum, and so removing the current during this portion of the cycle can have a dramatic impact on the efficiency of the amplifier. This effect can also be seen in the load line, which shows the device spending the times of highest voltage in the subthreshold region, causing the line to bend away from the high loss areas of simultaneous high voltage and current.

Clearly this strategy represents a continuum of amplifier operating conditions running from the class-A case wherein the device is conducting for all but a single point in the cycle to very extreme cases wherein the device is conducting only for short pulses. In order to sensibly discuss these various cases, a terminology has been developed to classify these operating conditions. Class-A is used to denote the amplifier which conducts for a full cycle, class-B operated devices conduct for exactly half of the cycle, and class-C



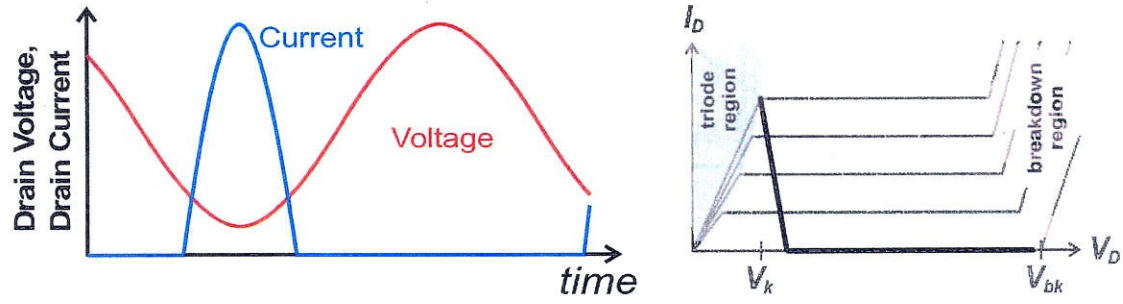
(a) (b)

Figure 2.9: Class-A/B waveforms (a) and load line (b).



(a) (b)

Figure 2.10: Class-B waveforms (a) and load line (b).



(a) (b)

Figure 2.11: Class-C waveforms (a) and load line (b).

operated devices conduct for less than half of the cycle. Similarly, the term class A/B is often used to denote devices which are non-conducting for less than half of the cycle. Representative waveforms and load lines for these operating classes can be seen in Figs. 2.8 to 2.11.

The efficiency achievable by this range of amplifiers is readily computed in a manner similar to the class-A case developed in Section 2.4.1.1. For the sake of brevity, the full analysis will not be given here, but a thorough treatment can be found in any number of texts, [e.g. 1]. The results are as follows:

$$\eta_D = \frac{1}{2} \cdot \left[\frac{1 - V_k/V_{bk}}{1 + V_k/V_{bk}} \right] \cdot \left[\frac{\alpha - \sin\alpha}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \right] \tag{2.41}$$

$$P_{out} = \frac{1}{8\pi} \cdot \left[\frac{\alpha - \sin\alpha}{1 - \cos\alpha/2} \right] \cdot \left[1 - \frac{V_k}{V_{bk}} \right] \cdot V_{bk} \cdot I_{max} \tag{2.42}$$

where α is the *conduction angle* defined to be the total number of radians during the cycle wherein the device is conducting, V_{bk} is the maximum voltage in the device waveforms, and I_{max} is the maximum current in the device waveforms. These results are plotted in Fig. 2.12.

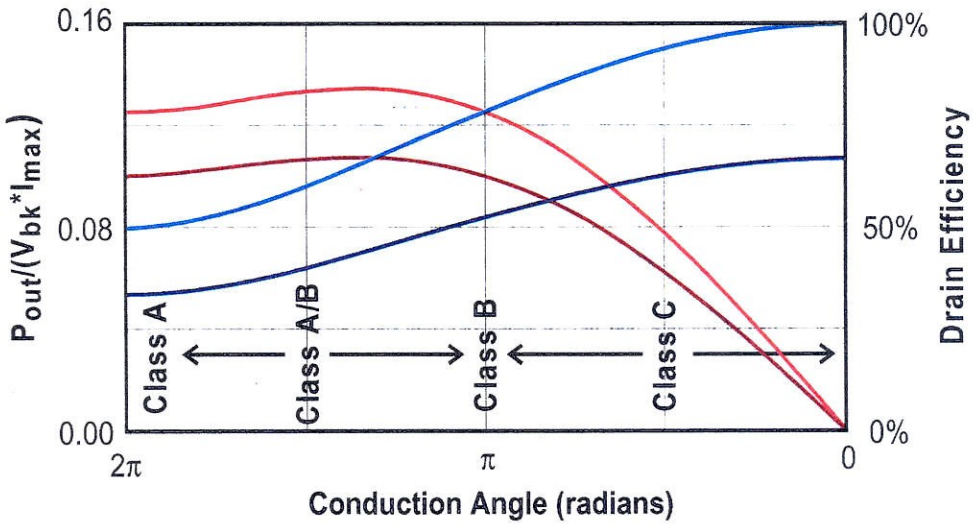


Figure 2.12: Drain efficiency (blue) and output power (red) vs. conduction angle. The lighter shaded curves represent the ideal case where the knee voltage is zero, whereas the darker represents the case where the knee voltage is 20% of the breakdown voltage.

As can be seen, the efficiency of the amplifier can be increased arbitrarily by reducing of the conduction angle to increasingly concentrate the current into those parts of the cycle

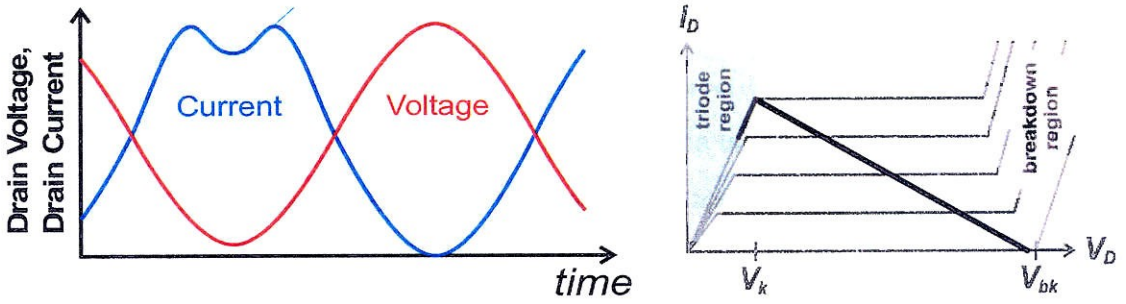
where the voltage is low. Unfortunately, the effect of this concentration is that either the output power must be reduced or the peak current must increase, as is reflected in the falling red normalized output power curve in Fig. 2.12. Additionally, since the conduction angle is normally reduced by decreasing the bias voltage on the device input, the input rf amplitude must be increased as the conduction angle is reduced if the peak current is to remain the same. This effectively reduces the gain of the amplifier, making this technique limited to use only where the device gain is relatively high.

2.4.2 Saturated Transconductance Amplifiers

Although the analysis presented in Section 2.4.1 assumes that the device voltage will not drop below the knee voltage V_k at any point during the cycle, this is not a necessary condition. An amplifier which is currently operating with the minimum voltage at the knee voltage can certainly be driven with a yet larger input, and it might be supposed that the efficiency might increase under this condition. The question then arises as to how the device waveforms will change under this *overdrive* condition.

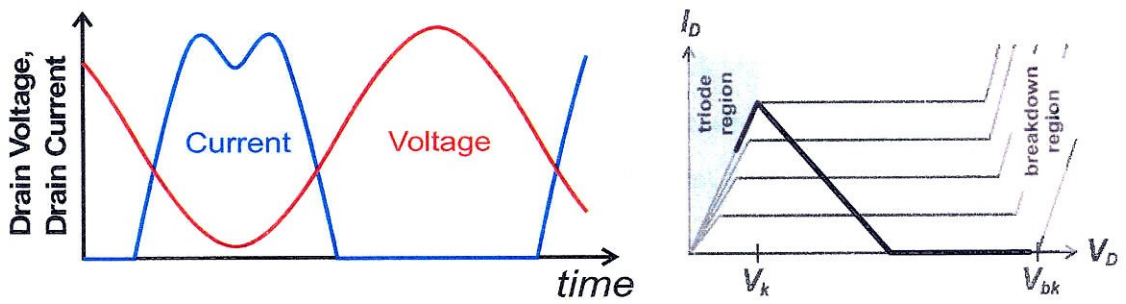
The effect can be readily evaluated by remembering that the knee voltage is defined as the transition between the transconductance and linear regions of the device operating characteristic. If the amplitude of the voltage waveform is to increase, and if the resonator forces the voltage to remain sinusoidal, then the voltage will be forced to drop below the knee voltage and the device will enter the triode region. Since the current in this region is always lower than the current that would be expected from the device for the same drive level, had the voltage been high enough for it to be operating in the transconductance region, the current waveform will begin to distort due to current reductions during the times where the voltage is below the knee. This effect can be seen in two example device waveforms of Fig. 2.13, a class-A example, and Fig. 2.14, a class B example.

This waveform distortion has several effects. Most obviously, the output power is higher, which is readily seen since the amplitude of the voltage waveform has been increased. The effect on efficiency is not so easy to evaluate, however. The distortion of



(a) (b)

Figure 2.13: Saturated class-A waveforms (a) and load-line (b).



(a) (b)

Figure 2.14: Saturated class-B waveforms (a) and load-line (b).

the current waveform has resulted in a redistribution of the current away from those times wherein the voltage is lowest, tending to reduce the efficiency. At the same time, the voltage for all points in the "negative" half of the cycle is reduced, so that the loss associated with this part of the cycle where the currents are the highest will to decrease, tending to increase the efficiency. The overall effect on efficiency is a result of these two processes, the net effect being to increase the efficiency very slightly for small levels of overdrive but to actually reduce it for significant levels of overdrive. The benefits in efficiency and output power for overdriving this type of amplifier are relatively modest, and the performance after design optimization is usually similar to the non-overdriven case analyzed previously [1].

2.4.3 Saturated Amplifiers with Harmonic Tuning

In evaluating the saturated amplifier in the previous section, it should be clear that the principle shortcoming of the technique is its insistence on keeping a sinusoidal voltage waveform. This limits the fundamental voltage component of the voltage waveform to an absolute maximum of $V_{bk}/2$, limiting the achievable output power for a given peak voltage. More importantly, it limits the time period during which the voltage is near zero to only the small portion of the conduction angle where the sinusoidal voltage is at a minimum. In order to improve efficiency, then, the designer is forced to concentrate the device's current into this time period in order to achieve efficiency. Since the average (dc) current must be kept high enough to supply the active device with dc power according to (2.34), the peak current then must be made very high, causing excessive device strain and a lower achievable output power for a given peak current level.

In order to achieve additional efficiency under overdrive conditions, it is necessary to allow the waveform to take on non-sinusoidal shapes. Conceivably, under such relaxed constraints, the voltage waveform may be able to also take on a shape wherein it is nearly zero for some considerable time during which the device conducts current, thereby increasing the efficiency in much the same way as is done by reducing the current waveform duty cycle of transconductance amplifiers. By suitably adjusting the drive conditions and the impedances presented to the active device at the harmonic frequencies, harmonics could be added in the correct amplitude and phase so that the valley of the voltage waveform becomes "flatter".

There are any number of ways of doing this [17-19], but perhaps the most conceptually simple and certainly the most well studied is the class-F amplifier [15,16,1]. The basic idea of the class-F amplifier is to start with the class-B amplifier explored in Section 2.4.1.2, and begin to add odd harmonics to the voltage waveform so that it begins to increasingly resemble a square wave. Since the half-sinusoid current waveform contains no even harmonic overtones, the impedance at these added odd harmonics should be tuned to open-circuit, in principle allowing the harmonic voltages to exist without

harmonic currents. The class-F amplifier, then, attempts to achieve an N harmonic approximation to a square voltage waveform by open-circuiting the odd overtones up to the N^{th} harmonic. As in the class-B case, the even harmonics are tuned to short-circuit, allowing the even harmonics in the half-sinusoidal class-B current waveform to exist without resulting in undesirable even harmonic voltages. A circuit implementing this tuning is shown in Fig. 2.15.

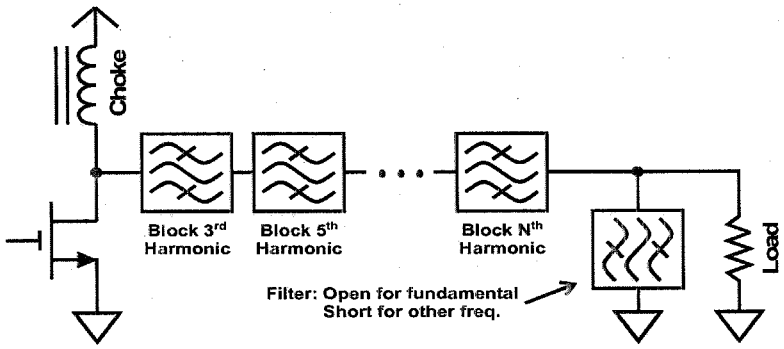
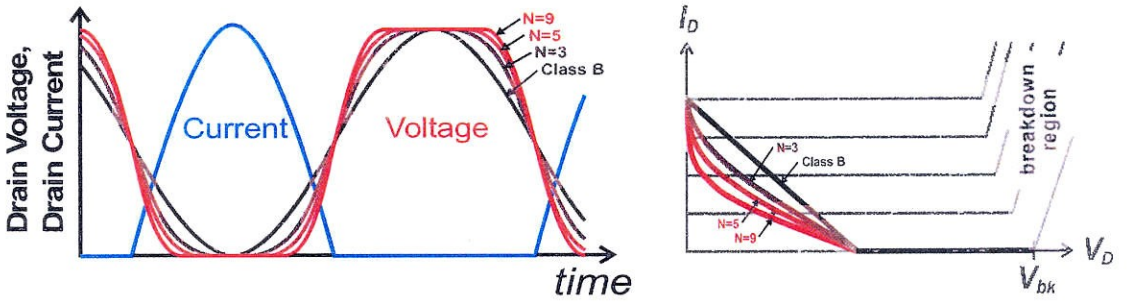


Figure 2.15: Class-F circuit conceptual implementation.

Although it is not at first obvious what the amplitudes and phases of these odd harmonic voltage components will be under the idealized class-F conditions, the effect under real conditions is that the harmonics arrange themselves in order to flatten the bottom of the voltage waveform due to the sharp change in the incremental conductivity between the triode and transconductance regions [15,24]. Due to the symmetry of the odd harmonics, this flattening of the bottom of the voltage waveform results also in a flattening of the waveform top. Idealized results, assuming maximally flat [24] voltage waveforms for various class-F amplifiers are shown in Fig. 2.16. Results assuming a somewhat less realistic efficiency-optimal distribution of harmonics shows a similar pattern [25].

The advantages of class F are twofold. First, and most obviously, the desired efficiency increase is achieved. In principle, the efficiency increases as more harmonics are tuned, approaching the ideal of 100% for the case where *all* of the harmonics are tuned



(a) (b)

Figure 2.16: Maximally flat class-F waveforms (a) and load-lines (b), showing curves for the cases N=1 (i.e. class B), N=3, N=5, and N=9. For sake of simplicity, the effect of the knee voltage is neglected.

making the voltage a true square wave. As can be seen from the load lines in Fig. 2.16, the efficiency improvement is accomplished by increasingly pushing the load line out of the transconductance region, so that the active device is acting more and more like a switch, i.e. it is spending more time in regions of very high or very low conductivity. The efficiency of the idealized maximally-flat class-F amplifiers tuned up to various numbers of harmonics N, from N=1 (i.e. class-B) to N=19 is shown in Fig. 2.17.

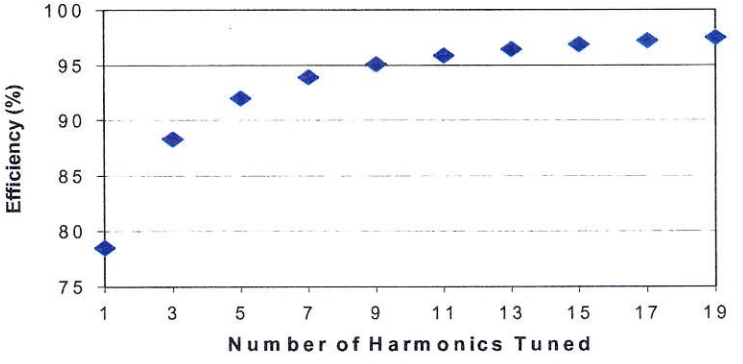


Figure 2.17: Efficiency of maximally-flat voltage waveform class-F amplifiers with half-sinusoidal current for various numbers of voltage harmonics tuned.

The second potential advantage allowed by the class-F approach is the increase in output power which can be achieved without increasing the peak voltage or peak current. Since the fundamental frequency amplitude of a square wave is a factor of $4/\pi$ greater than

the peak value of the square waveform, the voltage delivered to the output can be increased by the same factor without increasing the peak voltage. This results in a potential increase in output power by 27% – about 1 dB. This increase in output power while simultaneously increasing efficiency clearly distinguishes the class-F efficiency enhancement technique from the more traditional class-C approach, wherein output power is traded for efficiency. This effect can be seen in Fig. 2.18, plotting the normalized output power vs. efficiency for transconductance and class-F amplifiers.

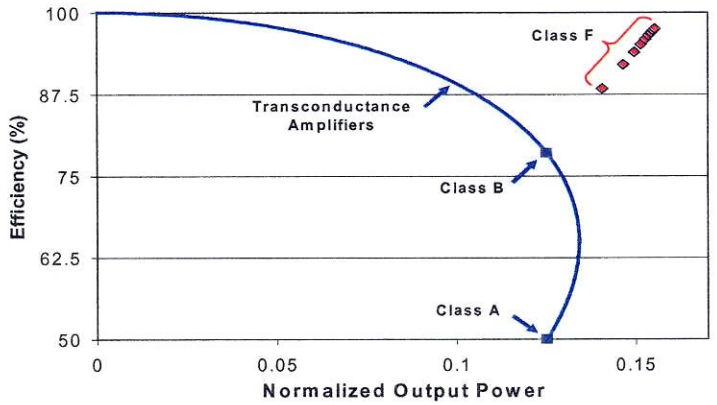


Figure 2.18: Efficiency vs. normalized output power for transconductance and class-F amplifiers. The output power is normalized to constant peak voltage and peak current.

There are also disadvantages to the class-F approach. Most obviously, the promise of increasingly higher efficiency can only be bought with increasing circuit complexity [26] as more resonators are required with each additional tuned harmonic[1]. This added circuit complexity not only increases the cost of the device, but the additional tuning elements inevitably add their own loss. Due to this factor, at some point increasing the number of tuned harmonics will actually decrease the overall amplifier efficiency as the reduced

1. There is a very elegant circuit [27] utilizing a quarter-wave transmission line which, in principle, achieves the required tuning for all harmonics using this single tuning component. This circuit fails, however, to account for the active device output capacitance, and as such is useful only when this capacitance is negligibly small.

conduction loss of the active device is less than the increased loss of the more complex output matching (and tuning) network

Another disadvantage is the lack of a simple means to incorporate the active device's output capacitance into the tuning network. Although the circuit presented in Fig. 2.15 seems simple enough, this kind of implementation strategy is effective only if the active device output capacitance is small enough to be neglected, i.e. the conductance it presents is small enough to be considered "open circuit". Unfortunately, this is almost certainly not the case, and so even the circuit of Fig. 2.15 is inadequate in most situations. In order to achieve the class-F tuning in the presence of a reasonable output capacitance C_s, the designer is forced to design a network presenting a conductance of $-j\omega C_s$ at the tuned odd harmonics. Such networks can certainly be designed, but the design is less straightforward and the tuning of the various harmonics tends to be more interactive. In light of these disadvantages, it is relatively rare to see class-F amplifiers tuned higher than the 3rd harmonic. In essence the diminishing returns of the additional harmonic tuning makes the additional cost and effort unjustified. Nonetheless, the additional efficiency to be had [e.g. 28] by even this low-order tuning makes this amplifier and its recently popularized dual, class F^{-1} [17,20], a subject of some recent interest [29,30].

2.4.4 Switching Amplifiers

Since the additional efficiency of harmonic-tuned saturated amplifiers seems to lie in the keeping the active device out of the transconductance region of simultaneously high voltage and current, the natural thing to do is to attempt the design of an amplifier that spends absolutely no time (or at least a very small fraction of the time) in this region. Such an amplifier would employ the active device as a switch, driving it with a sufficiently large input signal so that it is either in the completely open subthreshold region or in the low resistance triode region at all times. By doing this, the active device literally forces the voltage and current waveforms to be non-overlapping, in principle allowing 100% efficiency to be achieved not just asymptotically as in the class-F case, but in practical and

realizable circuit configurations. It is this type of amplifier which is the focus of the remainder of this dissertation, and the remainder of this chapter is meant to give a short overview before the more careful examination of the next chapter.

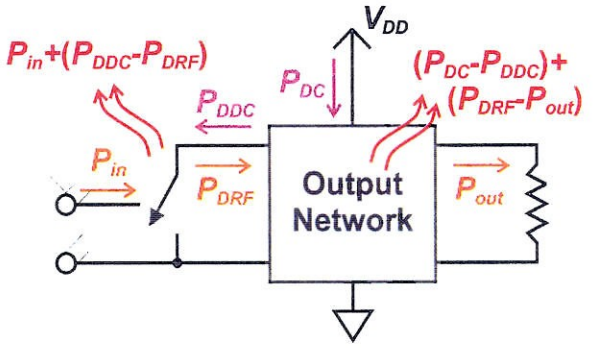
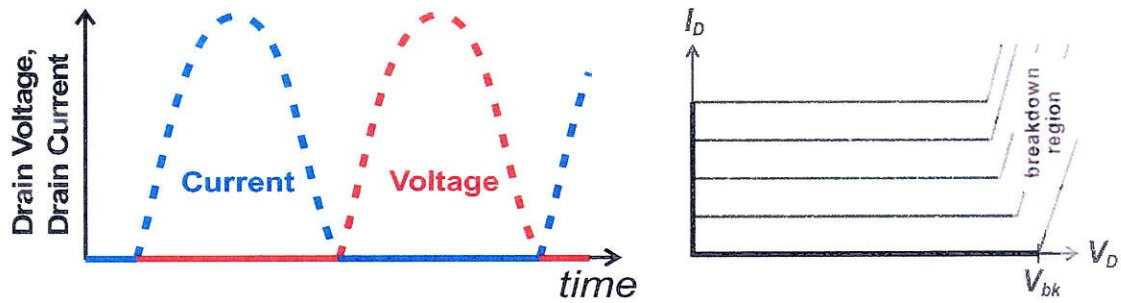


Figure 2.19: Generalized switching amplifier, showing power flow.

A generalized single-ended switching amplifier is shown in Fig. 2.19. Not surprisingly, it is identical to the generalized power amplifier discussed earlier, except that the active device is explicitly a controlled switch. Thus the active device alternates between states of high conductivity (switch "closed") and high impedance (switch "open") in a manner controlled by an input signal. In the narrowband case, the switch is assumed to be driven periodically, usually as a square wave, i.e. the switch is "open" for a half-period, then closed for a half-period, etc. Practically, this can be achieved by choosing a very large active device and providing it with a sufficiently large sinusoidal or square-wave input signal. If this is done, the resulting waveforms, whatever they turn out to be, will contain one duration of high-current and low voltage, and a second of high-voltage and low current. The actual shape of the high-voltage and high-current portions of the waveforms remain to be determined (this will be the primary objective of chapter 5), but this property of non-overlapping voltage and current waveforms is enough to promise an ideal device efficiency of 100% and a load-line that spends no time in any region wherein the active device dissipates any power. Hypothetical voltage and current waveforms meeting this condition and their resulting load-line are presented in Fig. 2.20.



(a) (b)

Figure 2.20: Switching amplifier conceptual waveforms (a) and load-line (b).

Unfortunately, switching amplifier design is not as simple as drawing non-overlapping voltage and current waveforms and declaring the efficiency to be 100%. The first stumbling point is the non-achievability or non-desirability of the vast majority of arbitrarily drawn waveforms such as these, due to the waveform constraints developed in Section 2.3. In particular, it is likely that the arbitrarily selected waveforms will be such that they require the active device to be either receiving or delivering power at some harmonic overtone[1], resulting in non-achievable (efficiency > 100%) or a non-desirable (efficiency < 100%) waveforms respectively. For instance the hypothetical nearly half-sinusoid waveforms shown in Fig. 2.20 have an output power exceeding their dc power consumed. The additional power would need to be supplied to the active device at higher even-harmonic frequencies, making these waveforms nearly impossible to achieve in practice since only dc supplies are normally available. If the hypothetical waveforms had been two square waves, on the other hand, the position would be the reverse and the active device would be forced to deliver power at odd harmonic overtones, making these waveforms perfectly achievable, but limiting their efficiency to below 100% (in this case, $8/\pi^2 \approx 81\%$).

1. It should be noted that, if the output passive network is not LTI, these waveforms could in principle be achieved since the passive network could convert power from one frequency to another.

A clever designer might hope to avoid these problems by making use of the waveform limitations as stated in impedance form. Such a designer might hope to simply design a load network with purely reactive impedances at the harmonic overtones and take whatever waveforms he gets, knowing that the harmonic power related issues will not be a problem. The new stumbling point is then encountered: Not all waveforms are equally desirable. If the harmonic impedances are tuned to arbitrary reactances, it is likely that the waveforms will be very poorly behaved. For instance, the waveforms might have very high peak values relative to the output power, resulting in excessive device stress. Likewise, the shape of the waveforms helps determine such properties as the amplifier gain and the dissipated power due to second-order considerations (developed in Chapter 4), and so an arbitrarily selected reactive tuning is likely to perform more poorly in these respects than a carefully selected one. An example of undesirable waveforms is shown in Fig. 2.21, wherein the designer has foolishly short-circuited the second, third, and fourth harmonics while tuning the higher-order harmonics to a fixed capacitance. This results in waveforms with extremely high peak values relative to the output power, and two different occurrences of negative voltage, which most solid-state switching devices are incapable of blocking..

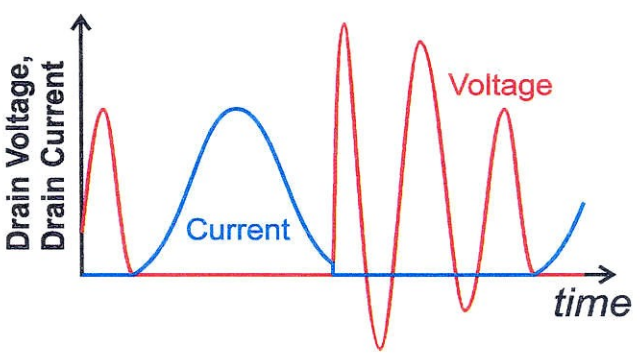


Figure 2.21: Undesirable switching amplifier waveforms.

Switching amplifier design has thus been relegated to use with tunings which are well-known and thoroughly investigated. In this case there are really only four known tunings, *class D* (closely related to class-F as will be seen in the next chapter) and its dual,

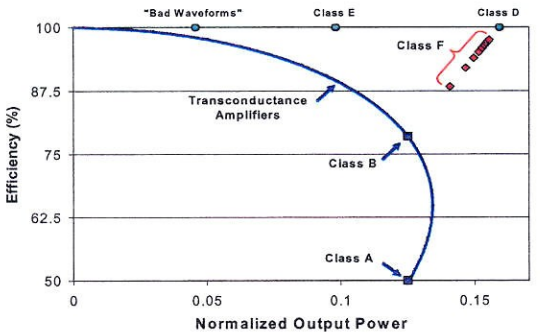


Figure 2.22: Efficiency vs. normalized output power for transconductance, class-F, and several switching amplifiers. The output power is normalized to constant peak voltage and peak current.

current-mode class D (also known as *inverse class-D* or *class* D^{-1}), along with *class E* (also known as *ZVS class E*) and its dual, *inverse class E* (also known as *class* E^{-1} or *ZCS class E*). These classes will be introduced properly in the next chapter, along with a more general treatment of switching amplifiers. Leaving the analysis aside for the moment, their performance is plotted along with other amplifier classes in Fig. 2.22. As can be seen, the efficiency achievable in-principle is always 100%, but their performance can vary significantly with the tuning with regard to other measures (in this case, the peak-normalized output power).

Chapter

3

Switching Amplifier Properties

To evaluate the performance and explore the tuning possibilities of switching amplifiers, it will first be necessary to develop some of their general properties. This chapter provides a basic analysis of the general properties of switching amplifiers, followed by an overview of the several well-known switching amplifier implementations.

3.1 Fundamental Operation.

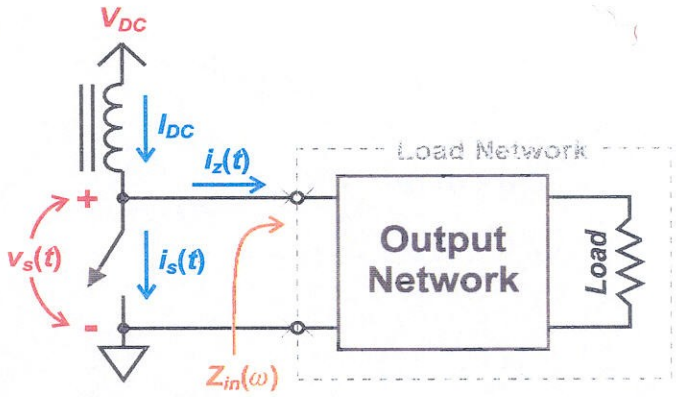


Figure 3.1: Generalized switching amplifier.

The most general single-ended switching amplifier topology is shown in Fig. 3.1. This topology contains a switch, loaded with an arbitrary linear time-invariant (LTI) passive load network. Additionally, there must be a means of supplying dc power, so for the sake of analysis an ideal choke (i.e. infinite inductance) is used for the supply connection. In practical circuits, this dc feed is part of the output network, but for the purposes of this analysis it is simpler to provide the same effect by use of this ideal choke. This removes all power sources from the passive load network, so that from the switch's perspective it can

be treated as an effective one-port as indicated by the dashed box in the figure. As such, the properties of this network are completely specified by its frequency-dependent port impedance $Z_{in}(\omega)$. The circuit's internal construction is an important implementation issue, but as far as the operation of the switch is concerned, totally irrelevant

3.1.1 Periodicity

Under the assumption of narrowband operation, the switching pattern will be treated as being effectively periodic, so that if at any time t_0 the switch is in a given state then for all times $nT + t_0$ the switch is in that same state, for any integer n and for some fundamental period T. Similarly, the waveforms will be assumed to be periodic, having the same fundamental period.

By utilizing this assumption, the switch voltage and current waveforms, v_s and i_s respectively, may be expressed in terms of a Fourier series:

$$v_s(\theta) = V_{DC} + \sum_{k=1}^{\infty} v_k \cos(k\theta + \alpha_k) \tag{3.1}$$

$$i_s(\theta) = I_{DC} + \sum_{k=1}^{\infty} i_k \cos(k\theta + \beta_k) \tag{3.2}$$

for some values of the parameters V_{DC}, I_{DC}, v_k, i_k, α_k, and β_k, and where the normalized time variable θ is defined as:

$$\theta \equiv 2\pi f_0 t = 2\pi \frac{t}{T} \tag{3.3}$$

3.1.2 Waveform Constraints

The determination the voltages and currents for the a switching amplifier can be reduced to determining the voltages and currents on the switch itself. Once these waveforms are known, the other circuit waveforms follow readily using standard linear

network theory. Additionally, if the loss imposed by the switch itself is to determined, the switch waveforms provide the necessary data for the calculation, as will be shown in the next chapter.

Unfortunately, the switching waveforms are not found as easily as in the amplifier classes discussed in Chapter 2. In transconductance amplifiers the current through the active device is known a priori, and so the voltage waveform is simply the voltage resulting from that known current forced through the known load impedance. In class-F amplifiers, the waveforms are assumed to be composed entirely of low-order harmonic components with simple constraints (such as being maximally flat at a certain point, etc.). The solution for switching amplifiers is less obvious because the constraint imposed by the active device is on the voltage waveform for part of the cycle and on the current waveform for the remainder. Specifically, when the switch is closed the switch voltage v_s is forced to zero, but when open the current is i_s forced to zero. If the set of times during which the switch is conducting is denoted $\boldsymbol{D}$ and the set of non-conducting times denoted $\overline{\boldsymbol{D}}$, then these conditions can be written as:

$$(\theta \in \boldsymbol{D}) \Rightarrow (v_s = 0) \tag{3.4}$$

$$(\theta \in \boldsymbol{D}) \Rightarrow (i_s = 0) \tag{3.5}$$

Aside from these two constraints, the switch makes no demands on the waveforms, and so while the constrained portions of the waveform are trivial to generate, the unconstrained non-zero portions require additional effort.

It is intuitively obvious that the form of the non-zero portions of the waveform must be determined somehow by the properties of the load network. The load network is LTI, and therefore described completely by its frequency-dependent input impedance, and so the only possible influence it could have on the waveforms is to demanding that, at all frequencies, the ratio between the voltage and current on its port be equal its port impedance. Since the waveforms only contain harmonic frequencies, this becomes a

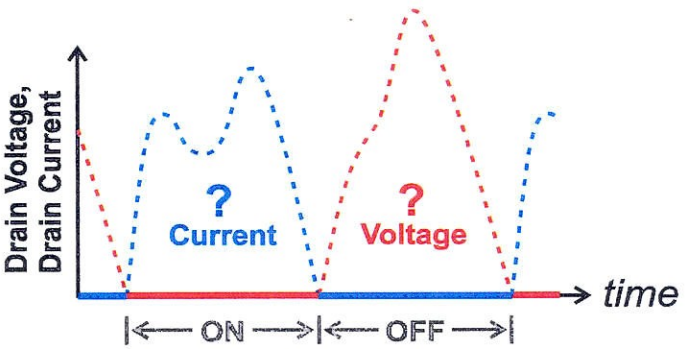


Figure 3.2: Switching amplifier waveforms after applying switching constraints. Non-zero values of current and voltage are not yet determined.

constraint imposed only at the harmonics. Letting $Z_{in}(k)$ denote the impedance at the k^{th} harmonic:

$$\underbrace{(v_k/i_k)e^{j(\alpha_k-\beta_k)} = Z_{in}(k)}_{\forall k \in \{1,2,3,4,\ldots\}} \tag{3.6}$$

Although this condition is easily written down, it is still not obvious how to apply it in order to determine the waveforms. The difficulty lies in the fact that (3.6) is really an infinite number of independent frequency domain conditions which must be reconciled with the very tight time-domain conditions demanded by the switch. Considerable effort has been exerted to solve for these waveforms even for specific cases such as the myriad of class-E solutions [4,31-42] each solving for a slightly different circuit topology or using different approximations and assumptions. Typically the solutions are derived in the time domain using network theory, utilizing different simplifying assumptions for each topology, making generalization or comparison difficult. To date, there has been no known technique for solving this system exactly, although work has been done on solving it under a finite-harmonic assumption [17].

3.1.3 Treatment as a Time-Varying Linear Circuit

One interesting aspect of the switching amplifier is that it is, from a certain point of view, a linear circuit. Usually, switching amplifiers are viewed as nonlinear circuits, since there is a strong nonlinearity from the input to the output of the active device. For instance, a sinusoidal signal driving the gate results in an obviously non-sinusoidal signal on the drain, indicating strong generation of harmonics. Furthermore, the active device is fully saturated so that changes in input amplitude have almost no effect on the output amplitude, resulting in extremely high AM/AM intermodulation distortion between input and output of the active device. In practical implementations, the AM/PM conversion is similarly high.

The linearity on the drain side of the device, however, is a different case. If the switch drive is treated as being an internal property of the switch so that it switches autonomously, the resulting circuit is linear but time varying. The switch itself represents two states, one with effectively zero conductance and the other with effectively infinite conductance. From this definition, then, the switch can be treated as an autonomously time-varying conductance surrounded by LTI circuit elements. Consider the current $i_G(t)$ through a time-varying conductance $G(t)$ excited with a linear superposition of two voltage signals $v_a(t)$ and $v_b(t)$:

$$\begin{aligned} i_G(t) &= G(t) \cdot [\lambda_a v_a(t) + \lambda_b v_b(t)] \\ &= \lambda_a [G(t) v_a(t)] + \lambda_b [G(t) v_b(t)] \end{aligned} \tag{3.7}$$

As can be seen, a time-varying conductance is a linear device, since its response to a linear superposition of stimuli is the linear superposition of the responses to the individual stimuli. Since the other components in the circuit are also linear, the linearity of the system follows. Thus, for any combination of stimuli – for instance, a changes in the bias voltage or an injected harmonic-frequency currents – on the drain side of the circuit, the response of the circuit may be computed as the superposition of the individual responses.

This linearity has its most obvious effect on the behavior of the circuit for different dc bias voltages, as will be explored in the next section, but it also allows the seemingly complex problem of waveform solutions to be stated in the form of a linear algebra problem as will be shown in Chapter 5.

3.1.4 Complementary Tunings

In developing the waveform constraints in Section 3.1.2, the switching amplifier solution is converted into a set of mathematical constraints (3.4)-(3.6). In these expressions, there is a certain symmetry between the current and the voltage. In fact, it is possible to interchange the role of the current and voltage waveforms, thereby generating a *dual* or *inverse* switching amplifier tuning. This can be done by simply inverting the drive of the switch (so that the switch will be "on" at times where before it was "off" and vise-versa) and by using a tuning network presenting, at each harmonic, an input admittance numerically equal to the original load network's impedance. To see this more clearly, consider (3.1)-(3.6) rewritten as follows:

$$i_s(\theta) = I_{DC} + \sum_{k=1}^{\infty} i_k \cos(k\theta + \alpha_k) \tag{3.8}$$

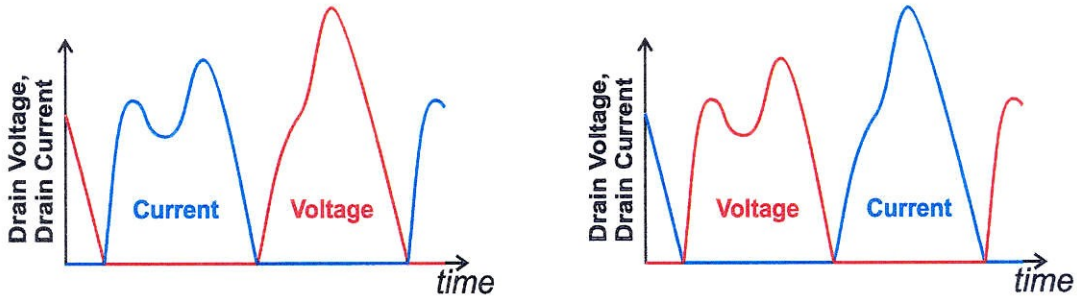
$$v_s(\theta) = V_{DC} + \sum_{k=1}^{\infty} v_k \cos(k\theta + \beta_k) \tag{3.9}$$

$$(\theta \in \boldsymbol{D}) \Rightarrow (i_s = 0) \tag{3.10}$$

$$(\theta \in \boldsymbol{D}) \Rightarrow (v_s = 0) \tag{3.11}$$

$$\underbrace{(i_k / v_k) e^{j(\alpha_k - \beta_k)} = Y_{in}(k)}_{\forall k \in \{1, 2, 3, 4, \ldots\}} \tag{3.12}$$

Clearly this mathematical specification is equivalent to (3.1)-(3.6), only with a different physical interpretation of the various terms. As a result, for any switching amplifier tuning, there is a dual tuning having the voltage and current waveforms interchanged. To generate the dual amplifier, it is only necessary to invert the switching pattern and to invert the impedances presented to the switch. This effect is shown in Fig. 3.3.



(a) (b)

Figure 3.3: Dual amplifier waveforms. Original switching amplifier (a) and complementary switching amplifier (b).

3.2 Scaling Properties

Setting aside for the moment the problem of solving for the waveforms of a switching amplifier, it is now possible to investigate the general behavior of these solutions. Supposing that the waveforms for one switching amplifier are known, it is useful to understand how the waveforms would change under simple scaling conditions. This way, if the waveforms can be found for a given case, cases which are scaled solutions may be found with little effort.

3.2.1 Bias Scaling

The first scaling rule of interest is *bias scaling*. Consider an amplifier whose solution is known for a given load network and dc bias voltage V_{DC}. Suppose it is desired to determine the waveforms for the same amplifier when the bias is changed to λV_{DC} for

some real number λ. Recalling from Section 3.1.3 that the circuit behaves linearly, the scaled solution must be the original voltage and current waveforms each scaled by a factor of λ. Specifically, if the un-scaled current and voltage waveforms are $i_s(\theta)$ and $v_s(\theta)$ respectively, the scaled current and voltage waveforms $\hat{i}_s(\theta)$ and $\hat{v}_s(\theta)$ will be:

$$\hat{i}(\theta) = \lambda i_s(\theta) \tag{3.13}$$

$$\hat{v}_s(\theta) = \lambda v_s(\theta) \tag{3.14}$$

or, stated as a causal relationship:

$$V_{DC} \rightarrow \lambda V_{DC} \Rightarrow \begin{cases} i_s(\theta) \rightarrow \lambda i_s(\theta) \\ v_s(\theta) \rightarrow \lambda v_s(\theta) \end{cases} \tag{3.15}$$

This effect is shown in Fig. 3.4.

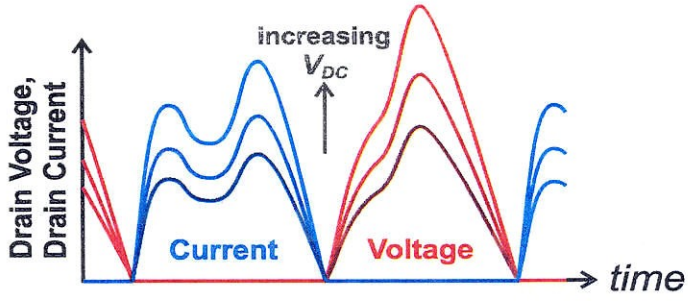


Figure 3.4: Effect of bias scaling in switch voltage and current waveforms.

3.2.2 Impedance Scaling

The second scaling rule is impedance scaling. Consider an amplifier whose solution is known for a given load network, presenting impedances of $Z_{in}(k)$, and dc bias voltage. Suppose it is desired to determine the waveforms for an amplifier operating at the same bias voltage, but with a load network presenting impedances $\lambda Z_{in}(k)$ for some real number λ. It is easily verified that the following scaled current and voltage, $\hat{i}_s(\theta)$ and $\hat{v}_s(\theta)$ respectively, provide the correct waveforms provided that $i_s(\theta)$ and $v_s(\theta)$ were waveforms for the un-scaled amplifier's current and voltage:

$$\hat{i}(\theta) = i_s(\theta)/\lambda \tag{3.16}$$

$$\hat{v}_s(\theta) = v_s(\theta) \tag{3.17}$$

or, stated slightly differently:

$$\underbrace{Z_{in}(k) \rightarrow \lambda \cdot Z_{in}(k)}_{\forall k \in \{1, 2, 3, \ldots\}} \Rightarrow \begin{cases} i_s(\theta) \rightarrow i_s(\theta)/\lambda \\ v_s(\theta) \rightarrow v_s(\theta) \end{cases} \tag{3.18}$$

This effect is shown in Fig. 3.5.

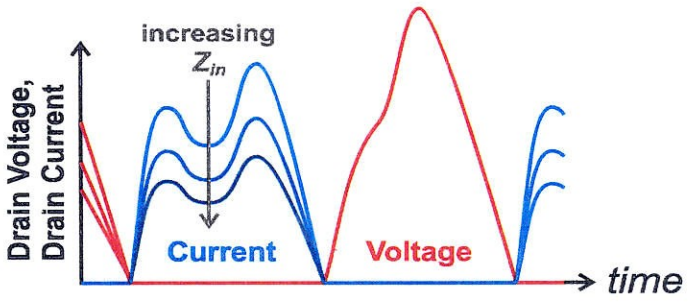


Figure 3.5: Effect of impedance scaling in switch voltage and current waveforms.

3.2.3 Arbitrary Scaling: Concept of a "Tuning"

By utilizing these two scaling rules, the initial solution may be transformed to have any desired independent voltage and current amplitudes. Thus there is a set of related switching amplifiers, each having the same waveform shapes but scaled to different voltage and/or current amplitudes. Additionally, the circuit topology of each amplifier in the group may be identical to one another, since the only necessary change from one to the other is to resize all of the components and/or adjust the bias voltage. As a result of these similarities, all amplifiers of the same group are considered to be utilizing the same *tuning* or *class of operation*.

Utilizing the scaling techniques will usually affect the circuit performance. For instance two different amplifiers in the group may have the same output power but

different gains and/or power efficiencies. The intelligent designer, then, would make use of these scaling techniques to maximize the performance. As a result, when comparing harmonic tuning methods, it is implicit that the comparison should not necessarily be between two individual amplifiers, but between those amplifiers providing the best possible performance in each tuning group given the design constraints.

3.3 Switching Losses

Aside from conduction losses due to the switch on-resistance as will be discussed in the next chapter, the drain-side loss on the switch occurs during the transitions from the off to the on-states.

3.3.1 Turn-On Losses and ZVS Switching

An important switching loss mechanism occurs if there is a capacitance C_s parallel to the switch and if this capacitor has charge on it just before switch closes. This charge must leave the capacitor if the switch is to enforce zero voltage. As a result, there is a large current through the switch as the switch rapidly drains the charge to ground, resulting in the stored energy in the capacitor being dissipated on the switch. This effect is shown in Fig. 3.6.

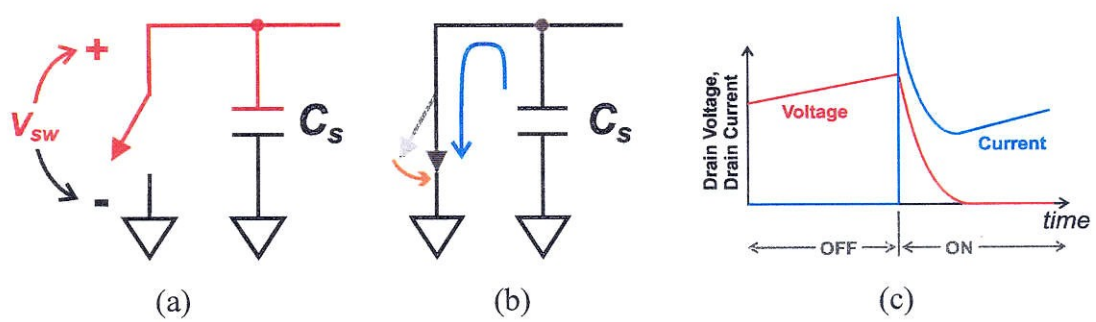


Figure 3.6: Capacitive discharge loss. Capacitor just before turn-on has stored charge (a). During turn-on charge is sinked through switch (b). Exponential discharge waveforms result (c) leading to power loss.

The power loss due to this mechanism can be calculated by considering that the capacitor's stored energy is dissipated once per cycle. If the voltage just prior to turn-on is V_{sw}, then the energy E_{sw} stored prior to discharge is:

$$E_{sw} = \frac{1}{2} C_s V_{sw}^2 \tag{3.19}$$

Considering that this energy is dissipated once per cycle, the resulting time-average power loss P_{sw} is:

$$P_{sw} = \frac{1}{2} C_s V_{sw}^2 f_0 \tag{3.20}$$

Switching transistors typically have significant output capacitance, especially if a large sized device is employed for low on-resistance, and operating frequencies continually increase due to system-level demands such as increased data bandwidth or power-converters with faster response times and/or smaller inductors. Since this discharge loss increases with both the frequency and with the capacitance, the effect can be crippling for high-frequency switching power amplifiers. The designer is forced to either avoid using switching amplifiers at high frequencies, leaving him to choose a less-efficient class of operation, or to reduce the capacitance. Since the parallel capacitance is usually dominated by output capacitance of the switching device itself, choosing to reduce this capacitance will force a reduction in the transistor size and a corresponding increase in the on-state resistance of the switch, increasing conduction loss.

Fortunately, there is another route to reducing the loss. If the voltage across the switch just prior to turn-on is kept small, the loss can be made reasonable. As a result, much effort [e.g. 4,5,43] has gone into finding techniques to avoid having *any* voltage across the switch prior to the switch closing. Collectively, these techniques are known as *zero voltage switching* (ZVS). An example of a ZVS transition is depicted in Fig. 3.7.

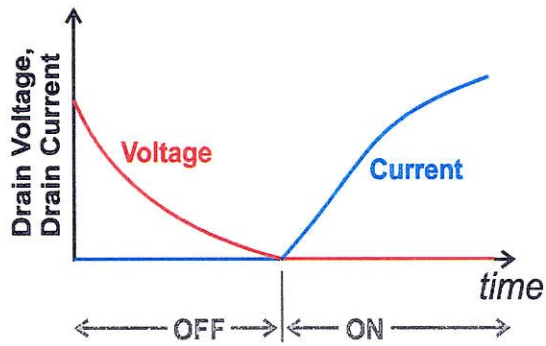


Figure 3.7: ZVS turn-on transition. The switch voltage is driven to zero by the passive network just as the switch begins to conduct, eliminating capacitive discharge.

3.3.2 Turn-Off Losses and ZCS Switching

The dual of capacitive discharge is inductive discharge, wherein an inductor in series with the switch is conducting current just prior to turn-off. The energy stored in the inductor, in this case, will be dissipated by the switch when the inductor generates a voltage spike causing the transistor to go into breakdown for a short duration. Although this situation is not encountered often in high-frequency power amplifier design, occasionally lower frequency circuits such as motor drives may exhibit this problem to an extent that it becomes an issue [44]. Additionally, with minority-carrier devices such as bipolar transistors (or in switching rectifiers, junction diodes) there is often a problem with the finite lifetime of the stored minority-carrier charges. Even if there is no significant inductance in series with the switch, the discharge of the minority carriers can reduce the efficiency at turn-off [44,45] if the switch is forced to switch from large current to zero current very quickly.

In both cases, a convenient solution is to utilize a switching amplifier for which the current is zero just before turn-off, a technique known as *zero current switching* (ZCS) [46,47]. Clearly, the dual of a ZVS amplifier will be a ZCS amplifier, so any advance made in the understanding of ZVS amplifiers will immediately result in a corresponding increase in the understanding of ZCS amplifiers. Since the conditions leading to the need

for ZVS switching tend to occur more often in practice, the remainder of this dissertation will focus on ZVS switching designs. If conditions demand ZCS switching instead, the required amplifier is found by impedance inversion as discussed in Section 3.1.4.

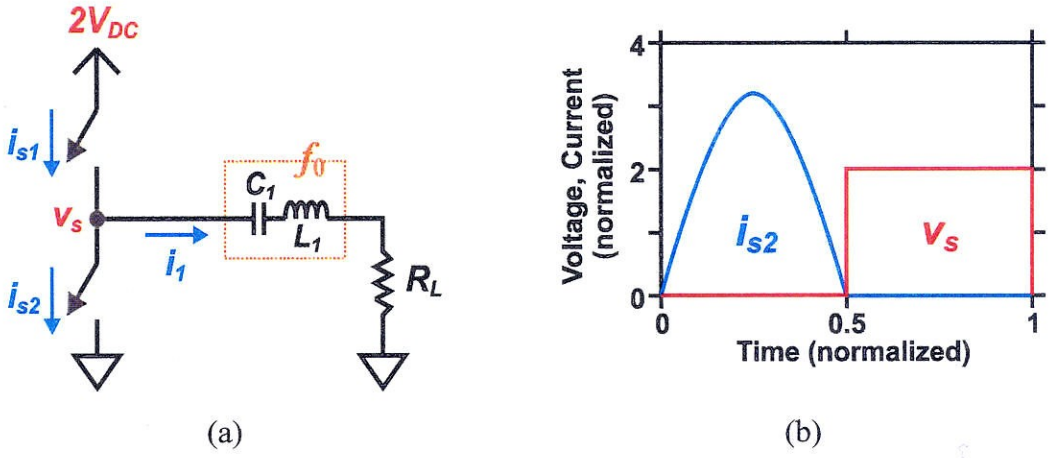
3.3.3 Known Switching Amplifier Tunings

Having surveyed the general properties of switching amplifiers, a survey now follows of the basic types of known switching amplifier tunings. Although there countless variations on each of the circuits that follow, the essential characteristics clearly place all of the known methods into two types: class D and class E.

3.3.4 Class-D Amplifiers

Class-D amplifiers have a close relationship with the class-F amplifiers discussed briefly in Chapter 2. In particular, class D presents a method to achieve the same waveforms as the limiting case of class-F amplifiers using relatively simple push/pull circuits. The class-D switching amplifier technique has been known since at least 1959 [48], and are well established in many applications at relatively low frequencies.

3.3.4.1 Class-D



(a) (b)

Figure 3.8: Class-D amplifier circuit (a) and waveforms (b). Waveforms are normalized to unit dc current and voltage on each switch.

The class-D amplifier [48,46], shown in Fig. 3.8, uses two switches in series, between the voltage supply and ground in order to force a square-wave voltage on their common node. This is done by driving the switches in a complementary fashion, so that for half of the cycle the lower switch shorts the node to ground while the upper switch shorts the node to the supply for the remainder of the cycle. This square wave voltage provides the fundamental frequency voltage needed to drive the load, but also contains undesirable odd harmonic voltages. In order to avoid passing these harmonics to the load, a filter is employed to connect the load to the switches. This filter, shown here as a series LC tank, provides a short-circuit between the switches and the load at the fundamental, while blocking the harmonics. As a result, the load current i_1 is a fundamental frequency sine waveform, This current conducts through whichever switch is closed, passing either to ground or to the supply. This results in half-sinusoidal current waveforms for each switch.

By allowing a square wave voltage and a half-sinusoid current, it would seem that class-D amplifiers deliver the performance promised by the limiting case of class-F. In some cases – especially at very low frequencies – it does, but unfortunately for high frequency designers, the basic class-D design takes no precautions to avoid problems with

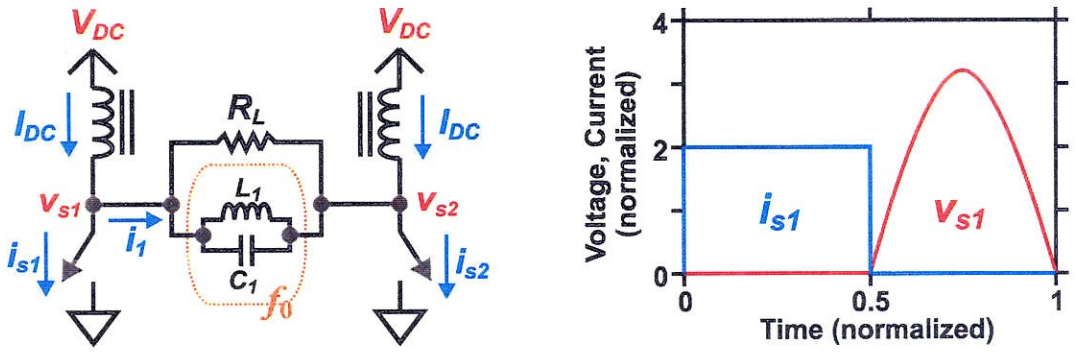
the switch output capacitance. As a result, simple class-D designs at high frequencies are plagued by capacitive discharge losses occurring during each step voltage transition. Further exacerbating the problem, each switch must discharge not only its own output capacitance, but the output capacitance of the other switch as well, further increasing the loss.

There are advantages, however, particularly the extremely low peak voltage, and so at relatively low frequencies where parasitic capacitance is not a significant problem (less than 100kHz-10MHz, depending on the transistor technology) class-D amplifiers are commonly used [e.g. 49,50]. In order to increase the frequency range and improve efficiencies of class-D amplifiers, several techniques [46,43] have been developed to achieve ZVS operation using this circuit topology. The essential feature of these techniques is to reduce the switch duty cycle, resulting in some time where neither switch is closed during which the output capacitance can be discharged by the load current i_1. By properly adjusting this "dead time", this technique can eliminate the discharge loss, but the usefulness of this technique is a somewhat limited since the conduction time of each switch must be reduced, increasing the conduction loss. Additionally, since the capacitors must be discharged completely during only a short portion of the cycle, the amount of capacitance that can be effectively corrected by this technique is fairly small.

3.3.4.2 Class-D^{-1} ZVS Amplifier

As its name suggests, the class-D^{-1} (inverse class-D, current source class-D) amplifier [46] is the dual tuning of the class-D amplifier. Accordingly, the waveforms should have a square wave current and a half-sinusoidal voltage.

Just as class-D tuning is achieved by using two switches to generate the square wave voltage by alternating the connection to the supply voltage, class D^{-1} achieves a square wave current by using two switches to reroute the supply current. In the most straightforward implementation, shown in Fig. 3.9, chokes supply dc current I_{DC} to each switch, which either conduct the current themselves or open-circuit to re-route the current



(a) (b)

Figure 3.9: Class-D^{-1} amplifier circuit (a) and waveforms (b). Waveforms are normalized to unit dc current and voltage on each switch.

through a differential load network to the other, conducting switch. The switches are driven in a complementary fashion with 50% duty cycle, so that the current through each switch is a 50% duty-cycle square wave:

$$i_{s1} = \begin{cases} 2I_{DC} & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{3.21}$$

$$i_{s2} = \begin{cases} 0 & 0 < \theta < \pi \\ 2I_{DC} & \pi < \theta < 2\pi \end{cases} \tag{3.22}$$

The current i_1 through the differential load can be determined by Kirchhoff's current law. This results in the square wave current:

$$i_1 = \begin{cases} -I_{DC} & 0 < \theta < \pi \\ I_{DC} & \pi < \theta < 2\pi \end{cases} \tag{3.23}$$

This current passes through the differential network consisting of the load resistance connected in parallel with a filter, shown here as a parallel LC tank. The filter's function is to short-circuit all harmonic frequencies, while remaining open-circuit at the fundamental. As a result, the fundamental frequency current must pass through the load resistance R_L, while the harmonic currents pass through the filter. This results in a differential voltage

which is a fundamental frequency sinusoid. Since the ratio of the fundamental frequency amplitude to peak value for a square wave is $4/\pi$, this differential voltage is found to be:

$$v_{s1} - v_{s2} = -\frac{4}{\pi} I_{DC} R_L \sin(\theta) \tag{3.24}$$

Since each switch voltage is zero during the time it is conducting, the switch voltages may be found:

$$v_{s1} = \begin{cases} 0 & 0 < \theta < \pi \\ -\frac{4}{\pi} I_{DC} R_L \sin(\theta) & \pi < \theta < 2\pi \end{cases} \tag{3.25}$$

$$v_{s1} = \begin{cases} \frac{4}{\pi} I_{DC} R_L \sin(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{3.26}$$

While useful at relatively low frequencies, Class D^{-1} has the same problem as class D in that it does not incorporate the transistor output capacitance into circuit configuration. Thus, while class-D^{-1} waveforms are ZVS, the property is relatively impotent since the analysis only holds for zero output capacitance. Unlike class-D, however, there is a simple method to compensate the class-D^{-1} circuit for the effect of this output capacitance, so that ZVS switching conditions can be achieved without resorting to bootstrap tricks like the dead time used in the class-D case. This method will be developed in Chapter 7.

3.3.5 Class-E Amplifiers

The class E amplifier is the result of an attempt to improve and simplify the design of class-D circuits. First, a single ended circuit is used, reducing the number of active devices to one and avoiding difficulties with synchronizing the drive signals for the two devices. What is most important, however, is the conscious attempt to take into account the effect the parasitic properties of the transistor, so that these effects might be accounted for and/or eliminated. The technique was first proposed and rather fully developed by Ewing as a

Ph.D. topic in 1964 [4], but went unnoticed until 1975 when it was brought to back to attention by Sokal [5]. Since then, it has been successfully employed in a wide range of designs [e.g. 7-14] and is generally regarded as being the best well-known method for switching power amplifier implementation for HF to microwave frequencies.

3.3.5.1 Class E

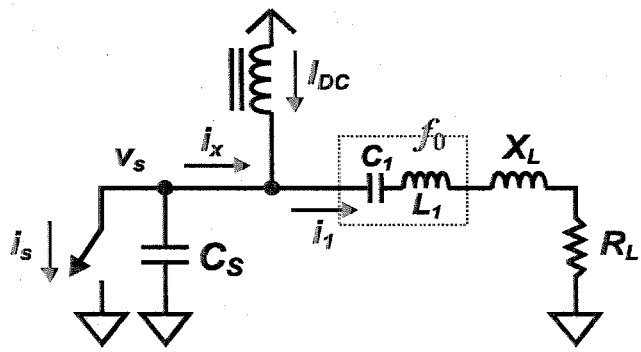


Figure 3.10: Class-E circuit topology.

The class-E amplifier is a simple switching amplifier tuning to achieve ZVS conditions while using 50% duty cycle. In the class-E circuit, shown in Fig. 3.10, the voltage across the switch during the "off" cycle is driven to zero by means of a resonant circuit tuned near the operating frequency of the switch. The switch is driven with 50% duty cycle at constant frequency f_0, and its parasitic output capacitance is absorbed into the switch parallel capacitance C_S. The resonator consisting of L_1 and C_1 is assumed to be designed in order to effectively block the harmonic frequencies and dc, forcing the current I_1 to be a sinusoid with frequency f_0. The choke is assumed to be ideal, so that it will only conduct the dc current I_{DC}. By conservation of charge, the current into the switch/capacitor combination i_x must be a dc offset sinusoid. Symbolically, for some value of α and β, i_x must be:

$$i_x = -I_{DC} + \alpha\cos(\theta) + \beta\sin(\theta) \tag{3.27}$$

This current will be commutated between the capacitor and the switch, depending on the switch's state. When the switch is closed, the voltage is forced to zero, and so the capacitor charge is fixed, necessitating the current to go through the switch. When the switch is open, its current is forced to zero, and therefore the capacitor conducts i_x. The switch voltage v_s is found by integrating the current through the capacitor. Without loss of generality it may be assumed that the switch is closing at $\theta = 0$, making the switch and capacitor currents i_s and i_{cs} equal to:

$$i_s = \begin{cases} I_{DC} - \alpha\cos(\theta) - \beta\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{3.28}$$

$$i_{cs} = \begin{cases} 0 & 0 < \theta < \pi \\ I_{DC} - \alpha\cos(\theta) - \beta\cos(\theta) & \pi < \theta < 2\pi \end{cases} \tag{3.29}$$

The switch voltage may be found by integrating the capacitor current i_{cs}:

$$\frac{dv_s}{dt} = \frac{1}{C_s} \cdot \begin{cases} 0 & 0 < \theta < \pi \\ I_{DC} - \alpha\cos(\theta) - \beta\cos(\theta) & \pi < \theta < 2\pi \end{cases} \tag{3.30}$$

$$v_s = \frac{1}{2\pi f_0 C_s} \cdot \begin{cases} I_{DC} \cdot (\theta - \pi) - \alpha\sin(\theta) + \beta[\cos(\theta) + 1] & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{3.31}$$

In order to achieve ZVS, the voltage must be continuous at $\theta = \pi$, but since there are two degrees of freedom it is possible to set another condition as well. The "optimal" class-E tuning also sets the slope of the voltage at the switching instant to zero, which has the advantage of ensuring that the current waveform begins with zero current. This switching characteristic of simultaneous zero voltage switching (ZVS) and zero-voltage slope switching (ZdVS) has become known as the *class-E switching conditions*. The values of α and β achieving these conditions are readily found to be:

$$\alpha = I_{DC} \tag{3.32}$$

$$\beta = -\frac{\pi}{2} \cdot I_{DC} \tag{3.33}$$

Using these values, the switch voltage and current waveforms can be found:

$$v_s = \frac{I_{DC}}{2\pi f_0 C_s} \cdot \begin{cases} 0 & 0 < \theta < \pi \\ \theta - \sin(\theta) - (\pi/2)\cos(\theta) - 3\pi/2 & \pi < \theta < 2\pi \end{cases} \tag{3.34}$$

$$i_s = \begin{cases} I_{DC} - \cos(\theta) + (\pi/2)\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{3.35}$$

These waveforms are depicted in Fig. 3.11.

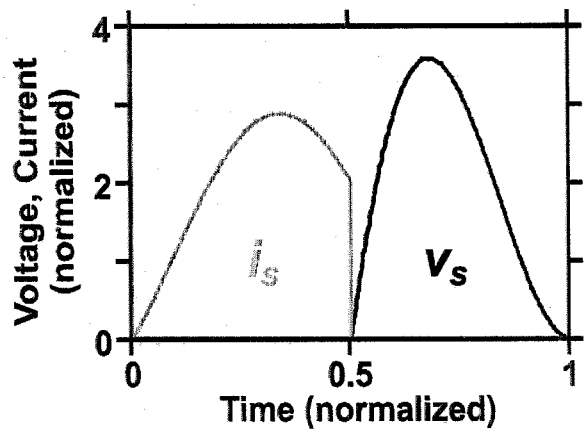


Figure 3.11: Class-E power amplifier waveforms. Waveforms are normalized to unity dc voltage and dc current, and the time axis is normalized to unity frequency.

The value of the required fundamental frequency load may now be calculated by finding the Fourier series representation of the voltage and current waveform v_s and i_1. Taking the ratio of the fundamental frequency components of this current and voltage results in the required impedance. Performing this calculation, one finds that an inductive impedance is required, corresponding to the need to supply a controlled phase shift in the fundamental frequency current in order to achieve the ZVS operation.

The class-E circuit primarily has the advantage of providing a means to accommodate the effect of the transistor output capacitance on the waveforms, as well as allowing for

ZVS operation so that the discharge of this capacitance may be avoided. Additionally, this is done with an extremely simple circuit topology, making implementation relatively simple and limiting the number of filters and other tuning elements. As a result, it has become popular for the implementation of high-frequency switching power amplifiers, from high power HF and VHF designs [e.g. 7-10,51] to high-efficiency microwave implementations [e.g. 12-14].

3.3.5.2 Even Harmonic Resonant Class-E

An interesting variation on the class-E concept is the "even harmonic resonant" class-E circuit [52]. This amplifier, published to little notice in 1996, is the only apparent attempt in the literature to improve upon the class-E by using additional harmonic tuning. The author's description actually encompasses a set of amplifiers, each being resonant at one even-order harmonic. Due to certain questionable assumptions made in the analysis, and due to the circuit topology, it is unlikely that the higher-harmonic implementations would produce satisfactory results[1], and so the remainder of this analysis will focus on the version for which the second harmonic has been tuned.

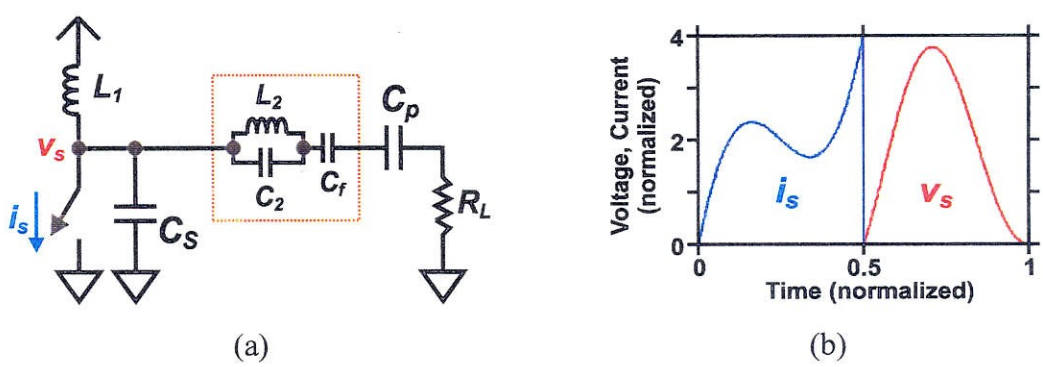


Figure 3.12: Second harmonic resonant class-E amplifier. Circuit topology (a) and waveforms (b). Waveforms are normalized to unity dc voltage and current.

1. Specifically, harmonic leakage currents into the load have not been accounted for, and become worse with higher-harmonic tunings. Furthermore, the values of the circuit elements quickly become unreasonable, inductor L_1, for instance, decreasing in size as the square of the harmonic number tuned. Finally, the waveforms for the predicted second-harmonic tuned version are by far better than for any other tuned-harmonic, making the other circuits of little interest.

The basic circuit configuration and the resulting waveforms are shown in Fig. 3.12. Similar to the class-E amplifier, the active device is represented as a switch, and a parallel capacitance absorbs the switch output capacitance. Unlike class-E, however, the choke has been replaced with a tuning inductor, which serves to both provide phase shifting for the fundamental frequency current and to resonate with the capacitance C_S at the second harmonic. A dual-resonant circuit consisting of L_2, C_2, and C_r is placed between the switch and the load. This circuit is designed so that L_2 and C_2 resonate at the second harmonic, effectively disconnecting the load from the switch at that frequency. Additionally, the three elements together resonate at the fundamental frequency so that the this frequency passes freely between the switch and the load. Finally, to provide phase-control of the fundamental frequency load current, a tuning capacitor *Cp* is placed in series with the load.

The waveforms have the familiar class-E turn-on switching conditions and the same general voltage shape, but the current waveform has been changed significantly. This is due to the resonance between L_1 and C_s at the second harmonic, providing an open-circuit to the switch at this frequency. As a result, the current waveform must change shape to not have any second harmonic component. The result is that the waveform takes on a visual characteristic somewhat between the original class-E shape and the class-F^{-1} square wave. This is not completely surprising, since the tuning at the second harmonic is the same as for the class-F^{-1} amplifier.

The performance advantages are subtle. As can be seen by comparing the waveforms with those of class-E, both the peak voltage and the peak current are much higher in the second-harmonic resonant class-E. On the other hand, the current seems to spend less time at those high levels, and generally seems more like a square-wave than the class-E current. Perhaps if the current has less RMS value the conduction loss of the second harmonic class-E will be less than for class-E? Has the performance improved with this tuning or has it gotten worse?

The answer is that the performance may, in fact, improve significantly, but for a different reason than was argued by the authors[1]. Unfortunately, the authors failed to clearly and convincingly demonstrate the performance benefits, and their exposition failed to even mention that harmonic-tuning of the drain impedance is to open-circuit, only giving component values from which this might be calculated by the reader. In addition, the authors failed to explain why high peak values of voltage and current don't render the performance actually *worse* than class-E, as might be expected from conventional analyses such as used in Chapter 2. Finally, the point most emphasized in the paper was the lack of a choke inductor, a result which had been reported in a conventional class-E circuit previously [36,38]. As a result of these issues, this amplifier has received almost no attention by other investigators.

3.3.5.3 Class-E^{-1} ZCS Amplifier

Like any other tuning, class E has a dual tuning [46] known as ZCS class E or class E^{-1}, which was first published by Kazimierczuk in 1981 [53]. Since class-E is a ZVS amplifier, the class-E^{-1} amplifier allows for ZCS operation, which may be desirable in certain situations. Since the amplifier does allow for ZVS operation, this tuning is not popular for use in high frequency amplifiers.

1. The author's argument is that for the same ratio between the load resistance and the on-resistance of the switch, their efficiency is better than class-E. Since by this measure, the class-E circuit could easily outperform itself by simply putting a suitable impedance transformer in front of the load, the value of this calculation is questionable.

Chapter

4

Predicting Switching Amplifier Performance

The motivation driving the choice between different amplifier tunings and operating conditions is always to achieve the best possible performance. If a switching amplifier is ultimately selected, efficiency is almost certainly one of the dominant factors. The basic switching amplifier theory indicates that all switching amplifier tunings can in principle achieve 100% efficiency since there is no mathematical reason why the waveforms cannot maintain the condition at each point in the cycle of having either zero voltage or zero current. In fact, if the device used were an ideal switch, the efficiency of every tuning would be identical and there would be no reason to select one tuning over another for reasons of efficiency. This is in stark contrast to the other amplifier classes explored in Chapter 2, where the tuning itself places fundamental limits on the achievable efficiency, even if an idealized active device (for instance, an ideal voltage-controlled current source with zero knee voltage) were to be used.

Unfortunately, it seems unlikely that an ideal switch is going to become available, and so the efficiency of the active device can not achieve 100%. This returns the designer to the question of which tuning strategy to pursue, since one tuning may conceivably accommodate the device non-ideality better than another, resulting in a significant efficiency difference between the two. Thus a means to compare the efficiencies of different tunings is required so that an amplifier designer may choose the best tuning for the application.

Similarly, switching amplifier tunings are not necessarily equal in other regards. For instance, some tunings will place higher peak voltage or current stresses on the active

device than others. Occasionally, such a consideration might become a limiting factor. Again, a method to evaluate the various tunings with respect to these situations is needed.

To address these needs, the remainder of this chapter will focus on simple ways to evaluate various performance demands which may arise so that informed comparisons may be made between amplifier classes and harmonic tuning strategies. The results focus on ZVS amplifiers, but using the loss model provided, these results may easily be extended to the lower-efficiency non-ZVS case if desired.

4.1 Switch & Resistor Model

Although bipolar switches have been popular and are suitable for many applications, the most promising switching devices are field effect transistors (FETs). A simple model suitable for FET switching devices is shown in Fig. 4.1. This model consists of an ideal switch with series resistance R_{on} and a parallel output capacitance C_{out}. The resistance models the conduction loss of the device, and consists of the combined channel, diffusion, and contact resistances of the FET when in the conducting state. The input is modeled as a input impedance Z_{in}, to which a power P_{in} must be applied in order to drive the device into switching operation. Although not explicitly shown, it should be understood that the input

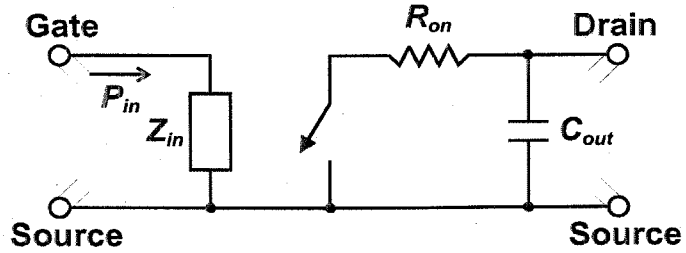


Figure 4.1: Switch & resistor model for a FET switching device.

power is a function of the desired frequency of operation. Up to the breakdown voltage V_{bk} of the switch, the off-state conductance of the switch is assumed to be zero.

While this model should not be expected to predict performance with great accuracy, it is useful for comparisons between competing tuning strategies as it captures the first order non-ideal effects of FET switches. The simple resistance model is appropriate in cases where the device is operated well into the triode region, which is normal for switching amplifiers. The output capacitance is linear, unlike the drain-source junction capacitance which dominates the output capacitance of most FET devices. Unfortunately, the treatment of a nonlinear capacitance [55,56] is sufficiently difficult, particularly in the general case, that it is customary to treat the capacitance as being effectively linear.

The assumption of an input power proportional only to the size of the device (as opposed to some property of the current waveform) may seem strange to designers familiar with transconductance designs where the input power is strongly related to the current waveform. In switching devices, however, much of the gate current is used to merely invert the channel region from a insulating depletion mode into a conducting inversion mode. Furthermore, the on-resistance of FET switching devices, particularly ones designed for high voltage, tend to be limited by the channel resistance. High voltage devices often find the on-resistance limited by lightly-doped drift regions needed for high breakdown voltage and by parasitic JFET-action found in vertical current devices [57]. Low voltage devices, on the other hand, tend to become limited by the resistance imposed by the source and drain contacts, the die metallization, and bonding wires [57]. In each case, there is a point of diminishing returns wherein increased gate voltage (or, equivalently, gate charge) reaches a point of severely diminishing returns with regard to on-resistance since this increase only effects the resistance of the channel.

In the context of switching power amplifiers, this suggests that there is an optimal input power to be used for any given transistor size. Supposing that a designer were using a device at this "optimal" point and desired to decrease the on-resistance. Due to the rapidly diminishing returns on investment of input power beyond the "optimal" drive point, decreasing the resistance by using the same device with increased drive voltage

quickly becomes impractical. Instead, the designer would be better advised to use a larger device size retain the "optimal" drive voltage, since this method results in a larger decrease in on-resistance for the same additional investment of input power. Suppose, on the other hand, that the designer found that the on-resistance was well below what was required, but desired to decrease the input power to the amplifier. The designer would be well-advised in this case to choose a smaller device size driven by the "optimal" drive voltage rather than keeping the same size device and decreasing the input voltage since for the same decrease in input power the first option results in a smaller increase in the on-resistance. This is due to the previously mentioned channel-inversion charge which is dependent only on the transistor size, whereas the channel charge is proportional to the channel conductivity. If the device size is reduced, both the inversion charge and the channel charge are reduced to achieve any increase in on-resistance, whereas decreasing the drive level on the same device only results in a decrease in the channel charge. As a result of these two effects, the drive voltage used for any particular sized device in a switching amplifier is reasonably well-known even without needing to consider the current waveforms since the designer would either choose this "optimal" drive level or choose a different sized device. Therefore, to first order, the input power of an optimally designed switching amplifier can be reasonably assumed to be a function only of the transistor size as assumed in this model.

While this model should not be expected to predict performance with great accuracy, it is useful for comparisons between competing tuning strategies as it captures the first order non-ideal effects on-resistance, output capacitance, and input power effects of FET switches. More complex models might include the effects of turn-on and turn-off times, the need to vary input power in some cases due to channel current saturation effects, thermal effects, etc. These effects are of secondary importance, however, and so are not included here for the sake of clarity and simplicity.

4.1.1 Device technology model

Usually, the designer has access not just to a single device, but to a *device technology* from which different sized devices are available with larger sized devices offering higher current ratings and lower on-state resistance. If device size constraints such as cost or die area are not issues, the designer is free to choose the device size achieving the best performance. Accordingly, a model is needed which captures the effect of device scaling within a given technology.

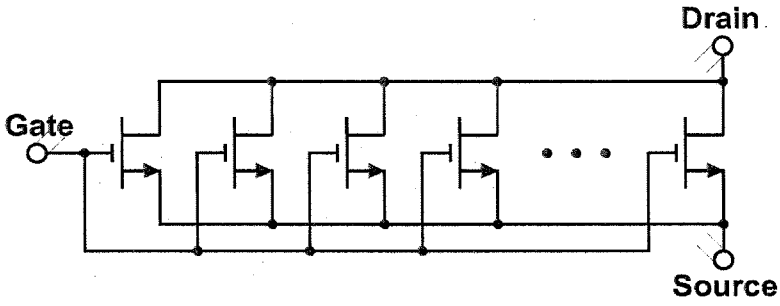


Figure 4.2: Power device as a parallel connection of small "cell" devices.

The proper scaling laws are apparent upon reflecting how the device size scaling is accomplished. Power devices are typically constructed as a parallel connection of many device *cells*. These cell devices are designed so that they may be tiled on the semiconductor substrate, allowing for simple and area-efficient layout on dice of various shapes and sizes. A device containing more cells, then, will have a lower on-state resistance but at the price of larger die area and input drive power.

The device properties can be easily found according to the properties of each unit cell and the number of cells, λ, used. If the cell's on-state resistance, output capacitance, and required input drive power are $\overline{R}_{on}$, $\overline{C}_{out}$, and $\overline{P}_{in}$ respectively, the entire device's properties will be:

$$R_{on} = \frac{\overline{R}_{on}}{\lambda} \tag{4.1}$$

$$C_{out} = \lambda \bar{C}_{out} \tag{4.2}$$

$$P_{in} = \lambda \bar{P}_{in} \tag{4.3}$$

The only other important property is the breakdown voltage, which will be the same as the breakdown voltage of each cell. Using this scalable model, the designer can select the value of λ achieving the best performance.

4.1.2 Efficiency Estimation

Using this switch/resistor model, a switching amplifier efficiency estimate is readily calculated. First it is assumed that the effect of the resistance R_{on} on the shape of the waveforms is small enough to be neglected, being a small perturbation on the ideal analysis for which the resistance is zero. Next, the power dissipation P_{diss} resulting from the current through this resistance is calculated. If the tuning is ZVS so that there is no capacitive discharge, the only loss is from the conduction of the drain current i_s through the on-resistance. This loss may be calculated as the square of the root-mean-square (RMS) current I_{RMS} through the switch multiplied by the resistance R_{on}.

$$P_{diss} \approx I_{RMS}^2 R_{on} \tag{4.4}$$

$$I_{RMS} \equiv \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} i_s^2 d\theta} \tag{4.5}$$

In the non-ZVS case, it is necessary to consider the effects of the capacitive discharge power loss. Unless the voltage is zero just prior to switching, the capacitance C_S parallel to the switch – consisting of the output capacitance C_{out} in addition to any capacitance added by the designer – will be discharged through the switch as the switch closes. The loss associated with this discharge can be calculated by considering the energy stored in the capacitance before and after discharge. If the voltage before discharge is V_{SW}, the energy E_{SW} stored in the capacitance is:

$$E_{SW} = \frac{1}{2} C_S V_{SW}^2 \tag{4.6}$$

The stored energy after discharge is zero, and so the energy E_{SW} is dissipated once each cycle. If the operating frequency is f_0, the resulting power loss from this discharge is:

$$P_{SW} = \frac{1}{2} \cdot C_S V_{SW}^2 f_0 \tag{4.7}$$

This can be restated in frequency-independent units by expressing the result in terms of the magnitude of the capacitor's impedance, Z_{CS}, at the fundamental frequency:

$$P_{SW} = \frac{1}{4\pi} \cdot \frac{V_{SW}^2}{Z_{CS}} \tag{4.8}$$

$$Z_{CS} \equiv \frac{1}{2\pi f_0 C_S} \tag{4.9}$$

Using this formula, the result of equation (4.4) may be modified to account for the total loss including conduction loss of the main body of the waveform in addition to the discharge loss. It should be understood that the RMS current I_{RMS} is not calculated to include the discharge current, which in the ideal zero-resistance case is represented as a Dirac current impulse at the moment the switch closes[1].

$$P_{diss} \approx I_{RMS}^2 R_{on} + \frac{1}{4\pi} \cdot \frac{V_{SW}^2}{X_{CS}} \tag{4.10}$$

The dc power P_{DC} delivered to the device can be calculated using waveform properties as well, being the product of the dc current I_{DC} and dc voltage V_{DC}:

$$P_{DC} = V_{DC} I_{DC} \tag{4.11}$$

1. Calculating the RMS current this way would result in an infinite value due to the Dirac impulse rather than the exponential discharge of a finite-resistance case. Even if the result were finite, using this value would count the discharge loss twice, as the P_{SW} term already accounts for it.

$$V_{DC} \equiv \frac{1}{2\pi} \cdot \int_0^{2\pi} v_s d\theta \tag{4.12}$$

$$I_{DC} \equiv \frac{1}{2\pi} \cdot \int_0^{2\pi} i_s d\theta \tag{4.13}$$

where v_s is the instantaneous drain-source voltage of the FET.

The output power can be determined from energy conservation considerations. If the switching amplifier has been designed correctly, the power delivered by the transistor to the load network at the overtone harmonics should be effectively zero. Therefore, the difference between the power delivered to the transistor from the dc supply and the power dissipated on the transistor must be the output power:

$$P_{out} = P_{DC} - P_{diss} \tag{4.14}$$

From this, the drain efficiency can be written as:

$$\eta_D \equiv \frac{P_{out}}{P_{DC}} = 1 - \frac{P_{diss}}{P_{DC}} \tag{4.15}$$

Combining this with (4.4) and (4.11), the drain efficiency estimate is found:

$$\eta_D \approx 1 - \left(\frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}} + \frac{V_{SW}^2}{4\pi X_{CS} V_{DC} I_{DC}} \right) \tag{4.16}$$

which in the ZVS case becomes:

$$\eta_D \approx 1 - \frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}} \tag{4.17}$$

The gain may be found by utilizing (4.14):

$$G = \frac{P_{DC} - P_{diss}}{P_{in}} = \frac{V_{DC} I_{DC} - I_{RMS}^2 R_{on}}{P_{in}} \tag{4.18}$$

Using this, the PAE may be estimated by using (2.11) and the drain efficiency (4.16):

$$PAE \approx \left(1 - \frac{P_{in}}{V_{DC}I_{DC} - I_{RMS}^2 R_{on}}\right) \cdot \left[1 - \left(\frac{I_{RMS}^2 R_{on}}{V_{DC}I_{DC}} + \frac{V_{SW}^2}{4\pi X_{CS} V_{DC} I_{DC}}\right)\right] \tag{4.19}$$

The first term may be further simplified under the assumption that the drain efficiency is close to unity[1], thereby neglecting the effect of the dissipated power on the gain:

$$PAE \approx \left(1 - \frac{P_{in}}{V_{DC}I_{DC}}\right) \cdot \left[1 - \left(\frac{I_{RMS}^2 R_{on}}{V_{DC}I_{DC}} + \frac{V_{SW}^2}{4\pi X_{CS} V_{DC} I_{DC}}\right)\right] \tag{4.20}$$

which for the ZVS case becomes:

$$PAE \approx \left(1 - \frac{P_{in}}{V_{DC}I_{DC}}\right) \cdot \left(1 - \frac{I_{RMS}^2 R_{on}}{V_{DC}I_{DC}}\right) \tag{4.21}$$

4.2 Waveform Figures of Merit

With this simple model of the active device in hand, knowedge of the waveforms generated by the harmonic tuning strategy now allows the performance of the tuning to be estimated under various design constraints.

4.2.1 Peak Amplitude Limited Output Power

The first figure of merit introduced here is the measure of the amplifier's ability to generate the highest possible output power under the constraints of maximum peak current and peak voltage. This figure of merit is commonly used, in fact it was the only one introduced earlier in Chapter 2 as a simple means of comparing amplifiers of various

1. This assumption will be made several times, and results in efficiency expressions correct to the first order. Since these results are intended for comparison purposes between tunings, the simplifications allowed by this approximation are justified. Neglecting the second order term results in a slight underestimation of efficiency differences between tunings.

classes. Unfortunately, it is probably less useful for the evaluation of switching power amplifiers, since its motivating conditions are somewhat different than those normally found switching amplifier applications. Specifically, it corresponds to the condition wherein the most important factor in the design is achieving the required output power with the smallest transistor die size possible. Since switching amplifiers are usually employed in situations where power efficiency is the most important factor, the active devices used tend to be sized much larger than would be necessary strictly based on a maximum peak current handling capability since the drain efficiency generally increases with device size. Nonetheless, there may be situations wherein this figure of merit proves useful, and so it is given here as a simple introduction as well as for completeness.

The development of this measure is actually quite simple. Using (2.32), the output power is:

$$P_{out} = \frac{1}{2} v_1 i_1 \cos(\alpha_1 - \beta_1) \tag{4.22}$$

In the specific case of the high efficiency amplifier, wherein $P_{out} \approx P_{DC}$, the output power can also be approximated by using the dc voltage and current amplitudes:

$$P_{out} \approx V_{DC} I_{DC} \tag{4.23}$$

To include the reference to the peak voltage V_{pk} and peak current I_{pk}, (4.22) and (4.23) may be rearranged as follows, respectively:

$$P_{out} = (V_{pk} I_{pk}) \cdot \left(\frac{v_1 i_1 \cos(\alpha_1 - \beta_1)}{2 V_{pk} I_{pk}} \right) \tag{4.24}$$

$$P_{out} \approx (V_{pk} I_{pk}) \cdot \left(\frac{V_{DC} I_{DC}}{V_{pk} I_{pk}} \right) \tag{4.25}$$

These equations can, in turn, be re-arranged to yield a unitless figure of merit E_P:

$$E_P \equiv \frac{P_{out}}{V_{pk} I_{pk}} = \left(\frac{v_1}{V_{pk}}\right) \cdot \left(\frac{i_1}{I_{pk}}\right) \cdot \left[\frac{1}{2}\cos(\alpha_1 - \beta_1)\right] \tag{4.26}$$

$$E_P \equiv \frac{P_{out}}{V_{pk} I_{pk}} \approx \left(\frac{V_{DC}}{V_{pk}}\right) \cdot \left(\frac{I_{DC}}{I_{pk}}\right) \tag{4.27}$$

To calculate this figure of merit for switching amplifiers, then, only two properties of the waveforms need be known: the ratio between the peak and dc voltages, and the ratio between the peak and dc currents. Performance improves with smaller ratios of peak to dc amplitude. Since these ratios appear several times, it will be useful to name these *waveform figures of merit*:

$$F_V \equiv V_{pk} / V_{DC} \tag{4.28}$$

$$F_{PI} \equiv I_{pk} / I_{DC} \tag{4.29}$$

Using these definitions, (4.27) becomes:

$$E_P \equiv \frac{P_{out}}{V_{pk} I_{pk}} \approx \frac{1}{F_V F_{PI}} \tag{4.30}$$

4.2.2 Efficiency Figures of Merit

The preceding case measures the ability of the amplifier to generate power under peak waveform constraints. While this measure is valuable in many cases, usually the primary goal of a switching amplifier designer is to achieve power efficiency. Accordingly, the maximum achievable efficiency under several different constraints will be developed. As noted previously, the cases developed here will assume ZVS tunings, although they may be extended to include the effect of discharge if non-ZVS amplifiers are to be studied.

4.2.2.1 Device Size Limited Drain Efficiency

The first case is the simplest, representing a situation wherein the designer is asked to produce a given output power using a specified active device in such a way as to achieve

the highest drain efficiency. At relatively low frequencies, the gain of the transistor will be high enough that the input power may be safely neglected as a consideration, making the drain efficiency a suitable efficiency measure. Additionally, although there is an efficiency-optimal sized device for any given device technology and tuning, in certain situations the device size may be limited to far below optimal due to cost or practicality constraints. This could, for instance, occur in relatively low-frequency amplifiers for which the optimal device size may consume an entire semiconductor wafer or more, but even much smaller die sizes achieve acceptable performance. Thus it is interesting to consider the case where the designer is limited to a given "small" device and wishes to achieve the best possible performance using that size device. It will be assumed that the supply voltage is under the designer's control, so long as the peak voltage does not exceed the device's breakdown voltage V_{bk}.

Rearranging (4.17), the following drain efficiency expression results:

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}}\right)^2\left(\frac{V_{pk}}{V_{DC}}\right)^2\left(\frac{R_{on}}{V_{pk}^2}\right)(V_{DC}I_{DC})\right] \tag{4.31}$$

Although at first seeming to only add useless complication, this manipulation serves to separate the effects of the tuning strategy from the effects of the transistor. The first term – the ratio between the RMS and dc currents through the switch – is a property determined solely by the tuning strategy, being invariant under both impedance and bias scaling. Similarly, if V_{pk} is the peak voltage across the switch during the cycle, the second term is similarly a function only of the tuning strategy. The final term is simply the dc power consumed by the switch, which is to first order equal to the output power, a design constraint. This leaves only the third term. Noticing that the efficiency increases with increasing peak voltage, the designer would be advised to choose this voltage as high as possible. Physically, this occurs because the loss results from currents, not voltages, so if the voltage is increased while the current is simultaneously decreased, the output power can remain constant while decreasing the loss. This voltage/current trade-off can be made

only so long as the peak voltage remains tolerable. Since the peak voltage limitation is a function solely of the transistor technology, the optimized third term is a function only of the transistor technology. This optimum occurs when the peak voltage is equal to the device breakdown V_{bk}:

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{V_{pk}}{V_{DC}}\right)^2 \left(\frac{\bar{R}_{on}}{\bar{V}_{bk}^2}\right)(P_{out})\right] \tag{4.32}$$

This expression indicates that a desirable tuning strategy would have a low RMS to dc current ratio and a low peak to dc voltage ratio. Similarly, a desirable FET device would have low on resistance relative to the square of its breakdown voltage. Introducing the waveform figure of merit F_I and using the existing F_V, this becomes:

$$\eta_D \approx 1 - \left[(F_I^2 F_V^2)\frac{P_{out}}{(\bar{V}_{bk}^2/\bar{R}_{on})}\right] \tag{4.33}$$

where:

$$F_I \equiv \frac{I_{RMS}}{I_{DC}} \tag{4.34}$$

It is also interesting to note that the transistor property $(\bar{V}_{bk}^2/\bar{R}_{on})$ has units of power, and its value relative to the desired output power has a direct effect on the loss. As should be expected, as the output power is increased, the transistor size needs to be proportionally increased to keep the same efficiency.

4.2.2.2 Capacitance Limited Drain Efficiency

Another important case is where the designer desires to achieve maximum drain efficiency using a given transistor technology where he may freely choose the optimal device size [21]. This might occur in cases where the cost of incremental device area is small, and the device gain is relatively large so that the drive power may be neglected. Using a similar technique as before, (4.17) may be rearranged to become:

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{V_{DC}I_{DC}}{2\pi f_0 C_s V_{DC}^2}\right)(R_{on}C_{out})(2\pi f_0)\left(\frac{C_S}{C_{out}}\right)\right] \tag{4.35}$$

As before, the purpose of this manipulation is to separate the effects of waveform and transistor technology. The first term is simply the F_I waveform figure of merit encountered earlier. The second term, upon inspection, is also found to be a property of only the tuning, being invariant under both bias and impedance scaling techniques. The third term is a function only of the transistor technology, and is invariant under changes in transistor size. The next term simply indicates that the optimal performance degrades linearly with increasing frequency.

This leaves the final term, representing the proportion of the switch parallel capacitance C_S made up by the switch's own output capacitance C_{out}. Since the transistor size is determined by the designer, this term represents a degree of freedom to be optimized, under the constraint that C_{out} cannot be larger than C_S. Since the efficiency improves with increasing C_{out}, it is clearly best to choose C_{out} as large as possible. The optimal sized device is therefore the one with output capacitance equal to C_S:

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{V_{DC}I_{DC}}{2\pi f_0 C_s V_{DC}^2}\right)(\bar{R}_{on}\bar{C}_{out})(2\pi f_0)\right] \tag{4.36}$$

The further illuminate the meaning of the somewhat mysterious second term, consider that $V_{DC}I_{DC}$ is approximately the equal to the output power and that the $1/(2\pi f_0 C_S)$ is the magnitude Z_C of the switch parallel capacitance's impedance at the fundamental frequency:

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{P_{out}}{V_{DC}^2/Z_C}\right)(\bar{R}_{on}\bar{C}_{out})(2\pi f_0)\right] \tag{4.37}$$

$$Z_C \equiv 1/(2\pi f_0 C_S) \tag{4.38}$$

Shown this way, the term can be viewed as a ratio between the output power and the reactive power stored in the capacitance C_S. The term measures the tuning strategy's ability to utilize a large output capacitance (with a high reactive power) without necessitating a very large output power. A smaller value for this term allows a larger device size to be used for any given output power, reducing the on-resistance and the conduction loss.

From (4.37) it may be concluded that it is desirable to have tunings with low RMS to dc ratio in the current waveforms, and which use a relatively large switch parallel capacitance to produce a given output power.

Interestingly, the properties of the voltage waveform are of no consequence in this case. Unlike the previous case where current could be traded for voltage with a resulting gain in efficiency, increasing the voltage and decreasing the current in this case has no effect on the efficiency. This is due to the fact that the transistor size is not constant under this change. In order to trade voltage for current, a combination of impedance and bias scaling must be used. During this process, the RMS current scales inversely with the voltage level, whereas the circuit impedances scale proportionally to the square of the voltage level. The capacitance C_S therefore scales inversely with the voltage level. The transistor size – proportional to C_S in this case – must then scale inversely with the square of the voltage level, causing the on-resistance to scale proportionally to the square of the voltage level. Thus for an increase in the voltage by a factor of k under the conditions of constant output power, there is a decrease in the RMS current by a factor of k and an increase in the on-resistance by a factor of k^2. The product $I_{RMS}^2 R_{on}$ therefore stays constant.

As before, the efficiency may be expressed as waveform figures of merit:

$$\eta_D \approx 1 - \left[(F_I^2 F_C) \frac{2\pi(\bar{R}_{on}\bar{C}_{out})}{1/f_0} \right] \tag{4.39}$$

where:

$$F_C \equiv \frac{P_{out}}{V_{DC}^2 / Z_C} \tag{4.40}$$

The transistor property of interest in this case is the $R_{on}C_{out}$ product, which is the time constant of the exponential discharge waveform occurring when the transistor discharges its own output capacitance. This has units of time, and a desirable transistor technology would have a very small $R_{on}C_{out}$ time constant relative to the switching period.

4.2.2.3 Gain Limited Power Added Efficiency

The next two cases to be considered are both related to the maximum power added efficiency (PAE) for a given transistor technology where the designer is free to choose the optimal sized device. These are similar to the previous case, except that the gain is considered low enough to be a consideration.

As explored in the previous case, increasing the transistor size results in lower on-resistance and therefore higher drain efficiency. Unfortunately, this increased transistor size also results in higher input power. Since the output power is unchanged, the gain reduces as the transistor size is increased. In cases where the intrinsic device gain is very high, this may not be an issue and the result of the previous section will be adequate. In cases where the device gain is not so large, however, a more realistic efficiency measure such as PAE must be used. The question then becomes how to choose the device size for best PAE.

Since the drain efficiency increases whereas the gain decreases with increasing device size, it is not unreasonable to suspect that there is a device size beyond which the increased drain efficiency is more than offset by the decreased gain. This is in fact the case, and an amplifier which has reached this point is said to be operating under *gain limited PAE* conditions. This minimum may not be achievable, however, since it is possible that the output capacitance of a device with gain-limited size might exceed the switch parallel capacitance C_S. Under this *capacitance limited* condition, the best size will

be the largest possible given the capacitance constraint, i.e. wherein $C_{out} = C_s$. The remainder of this section explores the gain limited case, leaving the capacitance limited case to the next section.

Starting from (4.17), the transistor scaling rules of (4.1)-(4.3) are introduced:

$$PAE \approx \left(1 - \frac{\bar{P}_{in}}{P_{out}} \cdot \lambda\right) \cdot \left(1 - \frac{I_{RMS}^2 \bar{R}_{on}}{V_{DC} I_{DC}} \cdot \frac{1}{\lambda}\right) \tag{4.41}$$

Optimizing over λ for maximum PAE results in:

$$\lambda = \sqrt{\frac{I_{RMS}^2 \bar{R}_{on} P_{out}}{V_{DC} I_{DC} \bar{P}_{in}}} \tag{4.42}$$

$$PAE \approx \left(1 - \sqrt{\frac{I_{RMS}^2 \bar{R}_{on} \bar{P}_{in}}{P_{out} V_{DC} I_{DC}}}\right)^2 \tag{4.43}$$

Using the approximation that the dc power and the output power are approximately equal, this becomes:

$$PAE \approx \left[1 - \left(\frac{I_{RMS}}{I_{DC}}\right)\left(\frac{V_{pk}}{V_{DC}}\right)\left(\sqrt{\frac{\bar{P}_{in}}{V_{pk}^2 / \bar{R}_{on}}}\right)\right]^2 \tag{4.44}$$

The first two terms of this expression have been encountered previously, being the waveform figures of merit F_I and F_V. The third term contains a degree of freedom, i.e. the peak voltage of the waveform. As before, the best performance is achieved by choosing this value as high as possible, with the limiting case being the breakdown voltage of the technology. Setting $V_{pk} = V_{bk}$ renders the third term a function only of the transistor technology, invariant under scaling of the transistor size:

$$PAE \approx \left[1 - (F_I F_V)\left(\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2 / \bar{R}_{on}}}\right)\right]^2 \tag{4.45}$$

If the loss is small, this may be approximated as:

$$PAE \approx 1 - (2F_I F_V)\left(\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}\right) \tag{4.46}$$

From this result, it is clear that tunings with low RMS to dc ratios on the current waveform and low peak to dc ratios on the current waveform are desirable. The waveform's effect is in fact very similar to fixed device size case of Section 4.2.2.1.

The transistor technology's effect is also interesting, appearing in the expression as a ratio between the input drive power and the same "power" measure of transistor performance found in Section 4.2.2.1. Since this ratio is invariant under scaling of the transistor size, it represents a true figure of merit for the switching performance of the device in situations where the input power is a significant constraint.

4.2.2.4 Capacitance Limited Power Added Efficiency

As mentioned in the preceding section, it is possible that the "optimal" device size calculated using (4.42) results in a transistor so large that the output capacitance C_{out} is larger that the capacitance C_S set by the tuning. In this case, the optimal device size will be limited by the constraint that C_{out} must not be greater than C_S. In this case, the designer would be happy to trade more gain for increased drain efficiency, but is unable to because the output capacitance of the larger device is too large to absorb it into the capacitance C_S.

This capacitance-limited case is very similar to the case of capacitance-limited drain efficiency explored in Section 4.2.2.2. In particular, the transistor size will be the same, being limited by the same process, so that the drain efficiencies are identical. Thus, to calculate the PAE, it is only necessary to calculate the input power in the case wherein $C_{out} = C_s$. First noticing that the ratio of C_{out} to P_{in} is constant over changes in the transistor size, the input power may be expressed as:

$$P_{in} = \frac{C_{out}}{\bar{C}_{out}} \cdot \bar{P}_{in} = \frac{C_s}{\bar{C}_{out}} \cdot \bar{P}_{in} \tag{4.47}$$

Using this, along with the PAE expression (2.11) and the capacitance-limited drain efficiency (4.39), the following PAE expression results:

$$PAE \approx \left(1 - \frac{C_s \bar{P}_{in}}{\bar{C}_{out} P_{out}}\right) \cdot \left[1 - (F_I^2 F_C)\left(\frac{2\pi \bar{R}_{on} \bar{C}_{out}}{1/f_0}\right)\right] \tag{4.48}$$

Rearrangement yields:

$$PAE \approx \left[1 - \left(\frac{\bar{P}_{in}}{\bar{C}_{out} V_{pk}^2}\right)\left(\frac{2\pi C_s V_{DC}^2}{P_{out}}\right)\left(\frac{V_{pk}}{V_{DC}}\right)^2\left(\frac{1}{2\pi f_0}\right)\right] \cdot \left[1 - (F_I^2 F_C)\left(\frac{2\pi \bar{R}_{on} \bar{C}_{out}}{1/f_0}\right)\right] \tag{4.49}$$

This can be simplified by replacing the waveform figures of merit with their symbolic representations:

$$PAE \approx \left[1 - \left(\frac{\bar{P}_{in}}{\bar{C}_{out} V_{pk}^2}\right)\left(\frac{F_V}{F_C}\right)^2\left(\frac{1}{2\pi f_0}\right)\right] \cdot \left[1 - (F_I^2 F_C)\left(\frac{2\pi \bar{R}_{on} \bar{C}_{out}}{1/f_0}\right)\right] \tag{4.50}$$

Now it may be noted that increasing the peak voltage has a positive effect on the PAE by means of increasing the gain. Physically, this corresponds to the use of a smaller transistor size for the same output power as voltage is traded for current. It is best, then, to choose this value as high as possible, with the limit being the transistor breakdown voltage V_{bk}. Choosing $V_{pk} = V_{bk}$ also has the effect of rendering the first term in the gain expression a function only of the transistor technology:

$$PAE \approx \left[1 - \left(\frac{\bar{P}_{in}}{\bar{C}_{out} V_{bk}^2}\right)\left(\frac{F_V}{F_C}\right)^2\left(\frac{1}{2\pi f_0}\right)\right] \cdot \left[1 - (F_I^2 F_C)\left(\frac{2\pi \bar{R}_{on} \bar{C}_{out}}{1/f_0}\right)\right] \tag{4.51}$$

Of note also is the amplifier gain in this case:

$$G = \left(\frac{\bar{C}_{out}V_{bk}^2}{\bar{P}_{in}}\right)\left(\frac{F_C}{F_V^2}\right)(2\pi f_0) \tag{4.52}$$

Although it may first appear that gain is increasing with frequency, it should be remembered that $\bar{P}_{in}$ is itself a function of frequency. If a simple resistor/capacitor model of the input is used, this dependence is inverse with the square of the frequency. Thus the gain of the optimally sized amplifier will reduce inversely proportional to the frequency since the optimal device size in this case is reducing as frequency is increased.

Reviewing the results of (4.51), the following conclusions are reached. As before, tunings with low RMS to dc ratio on the current waveform benefit from higher drain efficiency. A low peak to dc ratio on the voltage waveform, primarily benefits the gain in capacitance-limited situations. Having a large tolerance to output capacitance (i.e. low F_C) allows for higher drain efficiency as well, but at a cost of reduced gain due to the associated increase in transistor size.

4.3 Summary

The results of this chapter are summarized here for easy reference:

$$PAE \approx (1 - W_G D_G) \cdot (1 - W_D D_D) \tag{4.53}$$

$$P_{diss} \approx W_D D_D P_{out} \tag{4.54}$$

$$G \approx \frac{1}{W_G D_G} \tag{4.55}$$

Design Constraint	Drain Loss WF Factor (W_D)	Gain WF Factor (W_G)	Drain Loss Device Factor (D_D)	Gain Device Factor (D_G)
device size limited η_D	$F_I^2 F_V^2$	N/A	$\frac{P_{out}}{(\bar{V}_{bk}^2/\bar{R}_{on})}$	N/A
capacitance limited	$F_I^2 F_C$	$F_V{}^2/F_C$	$\frac{2\pi \bar{R}_{on}\bar{C}_{out}}{1/f_0}$	$\frac{\bar{P}_{in}}{2\pi f_0 \bar{C}_{out} V_{bk}^2}$
gain limited PAE	$2F_I F_V$	$2F_I F_V$	$\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}$	$\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}$

Table 4.1 Efficiency and gain factors for harmonic-tuned switching amplifiers under different design conditions. Waveform factors are functions only of the tuning strategy, whereas device factors are a function only of the transistor technology. Smaller numbers indicate better performance.

F_V	F_I	F_C	F_{PI}
V_{pk}/V_{DC}	I_{RMS}/I_{DC}	$\frac{P_{out}}{V_{DC}^2/Z_C}$	I_{pk}/I_{DC}

Table 4.2 Waveform figure of merit definitions. Smaller values indicate better performance.

Chapter

5

Predicting Switching Amplifier Waveforms

In order to predict the performance of harmonic-tuned switching amplifiers using the techniques of the previous chapter, the amplifier's waveforms must first be found. Although numerical tools such as SPICE or harmonic balance simulations may be employed, these methods are time consuming and may present difficult simulation challenges. Transient simulations such as employed by SPICE, for instance, can require long simulation times due to the inevitably long settling time exhibited in the waveforms under changes in operating conditions. Being fundamentally resonant circuits, harmonic-tuned switching amplifiers may require hundreds or even thousands of rf cycles in order for the switching waveforms to achieve steady-state conditions. Furthermore, each rf cycle must contain enough time steps to accurately capture the complex harmonic structure of the waveforms.

Harmonic balance simulations avoid these difficulties, but instead have the limitation of only using a relatively small number of harmonics to represent the waveforms. If the number of harmonics employed is small, the voltage and current waveforms will be distorted due to the missing effect of the higher harmonics. Switching amplifiers are also generally capable of generating unwanted signals at very high harmonic frequencies if care is not taken in the design, an effect which harmonic balance simulations employing only a small number of harmonics will be unable to predict. Although large numbers of harmonics may in principle be employed in the simulation, the resulting large memory requirements and convergence problems with this approach tend to reduce its effectiveness.

To further exacerbate the problem, the tuning impedances needed to generate waveforms with desired conditions – notably ZVS and/or ZdVS switching conditions – are not usually known. In class-E amplifiers, the appropriate component values are available as well-known closed-form expressions (3.34) - (3.35), but the values needed for other harmonic-tunings are not readily available. As a result, use of a traditional simulator would require multiple trial-and-error simulations in order to converge to the desired tuning.

Solution techniques specifically intended for amplifiers tend to either target a very specific circuit topology as in the myriad of class-E solutions [4,31-42,54], or assume a limited number of harmonics such as the well-known class-F solution [1,15,24,25] and Raab's more recent solution technique for harmonic-tuned amplifiers [17]. These methods have the same waveform distortion as in the harmonic balance approach, and Raab's general technique is currently unsuitable for use with some tunings, particularly ones generating negative voltages and/or currents.

This chapter presents an elegant approach for the exact solution of a broad class of switching amplifiers, suitable for both highly-efficient numerical studies as well as for derivation of closed-form analytic solutions. The steady-state solution is shown to be equivalent to finding the nullspace of an underdetermined linear system with the number of real-valued unknowns being approximately twice the number of tuned harmonics, yielding an extremely efficient computation. If desired, the null-vector calculation may be performed analytically resulting in a closed-form solution. Additionally, the technique is easily adapted to determine tuning requirements for conditions such as ZVS and ZdVS, allowing these tunings to be found without trial-and-error searches.

5.1 Generalized Switching Amplifier

A general harmonic-controlled switching amplifier circuit topology is shown in Fig. 5.1. In this network, the active device is presented a load consisting of a capacitance

C_S, a dc feed, and a harmonic tuning network. This network, represented here as a bank of bandpass filters[1] and tuned loads, provides impedances selected by the designer at various harmonics to be tuned while remaining open-circuit at other, un-tuned frequencies. The active device is assumed to operate as a perfect switch, driven periodically at fundamental frequency f_0 with duty cycle D. Without loss of generality, it will be assumed that the switch is closing at time t=0.

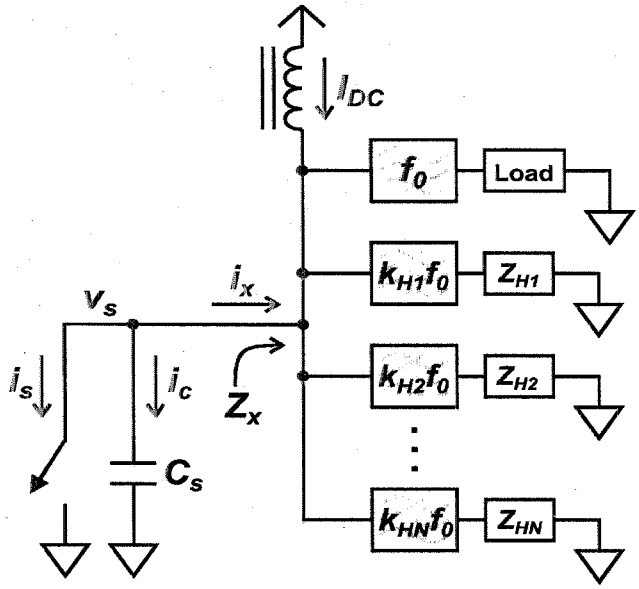


Figure 5.1: Generalized switching amplifier with switch parallel capacitance and harmonic tuning at selected frequencies.

This network is applicable to an broad array of tuning networks. First, the explicit incorporation of a capacitance in parallel with the switch ensures that the simulation will take into account the effect of the transistor output capacitance, since this capacitance may be incorporated into the capacitance C_S. The broadness of the description is in the ability to choose arbitrary impedances of as many harmonics as desired. Essentially, any passive structure presenting non-negligible impedances (i.e. having comparable or lower

1. Practical implementations would usually use a simpler structure providing the same impedances. The structure shown here is used for conceptual simplicity.

magnitude than the impedance presented by C_S) only at a finite number of harmonics may be treated as such a network. These "tuned" harmonics need not be consecutive or need even include the fundamental (e.g. if a frequency multiplier is to be simulated). For instance, a class-E simulation would require only one filter for the fundamental frequency, whereas a class-E amplifier modified by short-circuiting the 3rd harmonic with a high-Q series LC resonator would require an additional filter for the 3rd harmonic tuning. To treat such an amplifier employing a *low-Q* third harmonic resonator, additional filters at the second and fourth harmonics might be employed to introduce the effects of the low filter selectivity.

5.2 Solution Method

The solution technique introduced here is somewhat similar to the well-known class-E solution found independently by Ewing [4] and Raab [31] in that it employs the idea of commutation of a current of known form between the switching device and its parallel capacitance. Unlike the class-E solution where the bulk of the calculations take place in the time domain, the method presented here uses almost exclusively a frequency domain representation. This has two advantages. The first and most important is that an arbitrary specification of the impedances of the harmonics can be solved for, unlike the various class-E solutions which are each applicable to only a specific circuit topology. Secondly, the load tuning resulting in ZVS/ZdVS switching conditions is found in a manner which is independent of the waveform solution, this method having the advantages of providing insight into the behavior of the amplifier and avoiding the need to calculate the Fourier representation of the complex switching waveforms as is done in class-E solutions. Essentially, the necessary transformation into the frequency domain is done in a systematic way at the early stages of the solution.

First, the solution will be assumed to be periodic with fundamental frequency f_0. Since the exact value of the frequency is not important to the results of the simulation, it will be convenient to introduce the normalized time variable θ:

$$\theta = 2\pi f_0 t \tag{5.1}$$

The periodic nature will be exploited in the solution by use of a Fourier series representation over set of harmonic frequencies $f = k \cdot f_0$ for all integer k, defined by the following transform pair:

$$F_k = \frac{1}{2\pi} \int_0^{2\pi} \mathrm{f}(\theta) \cdot e^{-jk\theta} d\theta \tag{5.2}$$

$$\mathrm{f}(\theta) = \sum_{k=-\infty}^{\infty} F_k \cdot e^{jk\theta} \tag{5.3}$$

Although the current i_x into the filter network is not yet known, its form can be deduced. Noting that the network is constructed in such a was as to only admit significant currents at some subset T of the harmonics, the current must be of the form:

$$i_x = a_0 + \sum_{k \in T} [a_k \cos(k\theta) + b_k \sin(k\theta)] \tag{5.4}$$

for some coefficients a_k and b_k. Applying (5.2), the resulting Fourier coefficients may be found to be:

$$I_x = \begin{cases} a_0 & k = 0 \\ (a_k/2) - j \cdot (b_k/2) & k \in T \\ (a_k/2) + j \cdot (b_k/2) & -k \in T \\ 0 & |k| \notin T \end{cases} \tag{5.5}$$

The relationship between this current and the currents through the switch and the capacitor C_S, i_s and i_{cs} respectively, may now be found. For times during which the switch

is conducting, the voltage is forced to zero and so the capacitor current is likewise forced to zero. As a result, the current i_x has no alternative than to conduct through the switch. Similarly, when the switch is open, the current must conduct through the capacitor. The sole exception to these rules might occur at the instants during which the switch is changing state. Although nothing unusual will occur at the turn-off transition, the turn-on may exhibit a discharge current if there is charge stored in the capacitor the moment just prior to turn-on. Since the switch forces the voltage to zero at the instant of turn-on, this capacitor charge Q must leave the capacitor through the switch in the form of a Dirac impulse. This current commutation and discharge behavior is depicted graphically in Fig. 5.2.

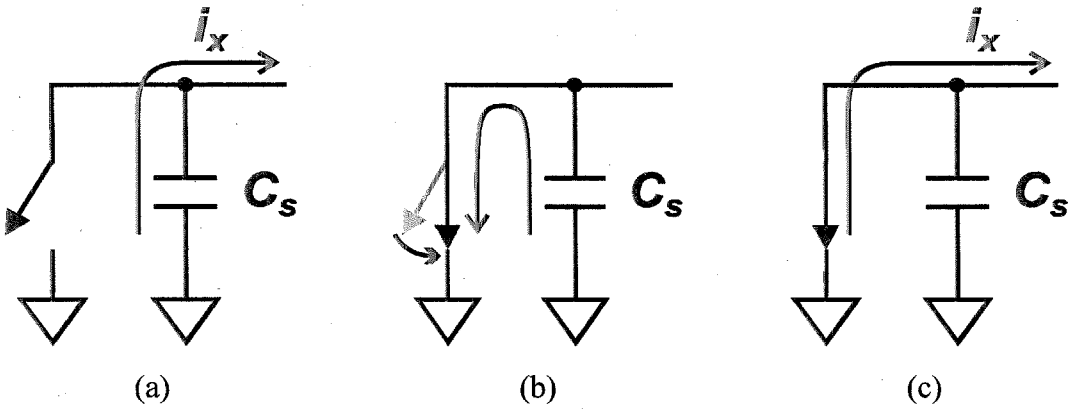


Figure 5.2: Commutation behavior of the harmonic filter current i_x. While the switch is open, current conducts through the capacitor (a). As the switch closes, a discharge current occurs (b). While the switch is closed, current conducts through the switch (c).

This results in the following expressions for the switch and capacitor currents and their Fourier coefficients:

$$i_s = -s(\theta) \cdot i_x(\theta) + Q \cdot \delta(\theta) \tag{5.6}$$

$$\begin{aligned} I_s(k) &= \frac{1}{2\pi}Q - S_k \otimes I_x(k) \\ &= \frac{1}{2\pi}Q - \sum_{|l| \in \{0,\, T\}} S_{k-l} I_x(l) \end{aligned} \tag{5.7}$$

$$i_{cs} = -\bar{s}(\theta) \cdot i_x(\theta) - Q \cdot \delta(\theta) \tag{5.8}$$

$$\begin{aligned} I_{cs}(k) &= -\frac{1}{2\pi}Q - \bar{S}_k \otimes I_x(k) \\ &= -\frac{1}{2\pi}Q - \sum_{|l| \in \{0,\, T\}} \bar{S}_{k-l} I_x(l) \end{aligned} \tag{5.9}$$

where $s(\theta)$ is a square waveform taking on values of unity for times during which the switch is conducting and zero otherwise:

$$s(\theta) = \begin{cases} 1 & 0 < \theta < 2\pi D \\ 0 & 2\pi D < \theta < 2\pi \end{cases} \tag{5.10}$$

$$S(\theta) = \begin{cases} D & k = 0 \\ \dfrac{\sin(2\pi D k)}{2\pi k} - j\dfrac{\sin^2(\pi D k)}{\pi k} & k \neq 0 \end{cases} \tag{5.11}$$

and where $\bar{s}(\theta)$ is a square waveform taking on unit values when the switch is open:

$$\bar{s}(\theta) = \begin{cases} 0 & 0 < \theta < 2\pi D \\ 1 & 2\pi D < \theta < 2\pi \end{cases} \tag{5.12}$$

$$\bar{S}(\theta) = \begin{cases} 1 - D & k = 0 \\ \dfrac{\sin(2\pi \bar{D} k)}{2\pi k} + j\dfrac{\sin^2(\pi \bar{D} k)}{\pi k} & k \neq 0 \end{cases} \tag{5.13}$$

$$\bar{D} \equiv 1 - D \tag{5.14}$$

Now that the current into capacitor C_s is known, the switch voltage v_s may be found by integration of the current i_s:

$$v_s(\theta) = \begin{cases} 0 & 0 < \theta < 2\pi D \\ Z_{cs} \int_{2\pi D}^{\theta} i_{cs}(\theta) d\theta & 2\pi D < \theta < 2\pi \end{cases} \tag{5.15}$$

$$V_s(k) = -j\frac{Z_{cs}}{k} I_{cs}(k) \tag{5.16}$$

where Z_{cs} is the magnitude of the capacitor's impedance at the fundamental frequency:

$$Z_{cs} = 1/(2\pi f_0 C_s) \tag{5.17}$$

As can be seen, if the charge Q and the filter current coefficients, a_k and b_k, were known, the solution could be generated by use of (5.15) for the switch voltage and (5.6) for the current. The constraints needed to set these values are found in the harmonic impedance specification for the filter bank. The impedance Z_k looking into the filter bank at each harmonic number k imposes a proportional relationship between the filter current i_x and the switch voltage v_s:

$$\underbrace{Z_k I_x(k) = V_s(k)}_{\forall k \in T} \tag{5.18}$$

Using (5.16), this becomes:

$$\underbrace{jk\frac{Z_k}{Z_{cs}} I_x(k) - I_{cs}(k) = 0}_{\forall k \in T} \tag{5.19}$$

One additional condition may be added, that being the dc current into the capacitor must be zero:

$$I_{cs}(0) = 0 \tag{5.20}$$

Comparing (5.19) and (5.20), it becomes apparent that these two expressions may be merged into one:

$$\underbrace{jk\frac{Z_k}{Z_{cs}}I_x(k) - I_{cs}(k) = 0}_{\forall k \in \{0, T\}} \tag{5.21}$$

Finally, (5.9) may be used to yield the required conditions:

$$\underbrace{jk\frac{Z_k}{Z_{cs}}I_x(k) + [\bar{S}_l \otimes I_x(l)]\Big|_{l=k} + \frac{1}{2\pi}Q = 0}_{\forall k \in \{0, T\}} \tag{5.22}$$

This linear homogeneous system of $|T|$ complex-valued equations and one real-valued equation in $|T|+2$ real-valued unknowns may be solved to yield the appropriate coefficients of i_x and the charge Q. Since the system is underdetermined and homogeneous, a solution must always exist. Additionally, scaling this solution by any integer multiple will also yield a valid solution. This physically corresponds to bias scaling as discussed in Chapter 3 and is a consequence of neither the dc bias voltage nor the dc bias current having been set during the solution. Each solution vector corresponds to the solution under a different bias condition.

5.3 Real-Valued Linear Algebra Implementation

To solve this system in an efficient manner, it is best to convert the one-line expression (5.22) into a form suitable for real-valued linear algebra routines. First, the convolution sum may be expanded:

$$\underbrace{jk\frac{Z_k}{Z_{cs}}I_x(k) + \sum_{|l| \in \{0, T\}} S_{k-l}I_x(l) + \frac{1}{2\pi}Q = 0}_{\forall k \in \{0, T\}} \tag{5.23}$$

This may be further expanded using (5.5):

$$\underbrace{jk\frac{Z_k}{Z_{cs}}I_x(k)+a_0S_k+\sum_{l\in T}\left[S_{k-l}\left(\frac{a_k}{2}-j\frac{b_k}{2}\right)\right]+\sum_{l\in T}\left[S_{k+l}\left(\frac{a_k}{2}+j\frac{b_k}{2}\right)\right]+\frac{1}{2\pi}Q=0}_{\forall k\in\{0,\,T\}} \tag{5.24}$$

This expression may be expanded into the following real-valued system of equations:

$$Da_0+\sum_{l\in T}\left[\frac{\sin(2\pi\bar{D}l)}{2\pi l}a_l-\frac{\sin^2(\pi\bar{D}l)}{\pi l}b_l\right]+\frac{1}{2\pi}Q=0 \tag{5.25}$$

$$\underbrace{\begin{aligned}&\left[\frac{\bar{D}}{2}+\frac{\sin(4\pi\bar{D}k)}{8\pi k}-\frac{kX_k}{2}\right]\cdot a_k+\left[\frac{kR_k}{2}-\frac{\sin^2(2\pi\bar{D}k)}{4\pi k}\right]\cdot b_k\\&+\frac{\sin(2\pi\bar{D}k)}{2\pi k}\cdot a_0+\sum_{l\in\{T-k\}}[A_{k,l}a_l+B_{k,l}b_l]+\frac{1}{2\pi k}Q=0\end{aligned}}_{\forall k\in T} \tag{5.26}$$

$$\underbrace{\begin{aligned}&\left[\frac{\sin^2(2\pi\bar{D}k)}{4\pi k}+\frac{kR_k}{2}\right]\cdot a_k+\left[\frac{\sin(4\pi\bar{D}k)}{8\pi k}+\frac{kX_k}{2}-\frac{\bar{D}}{2}\right]\cdot b_k\\&+\frac{\sin^2(\pi\bar{D}k)}{\pi k}\cdot a_0+\sum_{l\in T-k}[\hat{A}_{k,l}a_l+\hat{B}_{k,l}b_l]=0\end{aligned}}_{\forall k\in T} \tag{5.27}$$

where:

$$A_{k,\,l}\equiv\frac{\sin(2\pi\bar{D}(k-l))}{4\pi(k-l)}+\frac{\sin(2\pi\bar{D}(k+l))}{4\pi(k+l)} \tag{5.28}$$

$$B_{k,\,l}\equiv\frac{\sin^2(\pi\bar{D}(k-l))}{2\pi(k-l)}-\frac{\sin^2(\pi\bar{D}(k+l))}{2\pi(k+l)} \tag{5.29}$$

$$\hat{A}_{k,\,l}\equiv\frac{\sin^2(\pi\bar{D}(k-l))}{2\pi(k-l)}+\frac{\sin^2(\pi\bar{D}(k+l))}{2\pi(k+l)} \tag{5.30}$$

$$\hat{B}_{k,\,l}\equiv\frac{\sin(2\pi\bar{D}(k+l))}{4\pi(k+l)}-\frac{\sin(2\pi\bar{D}(k-l))}{4\pi(k-l)} \tag{5.31}$$

and where R_k and X_k are the normalized tuning resistance and reactance for the k^{th} harmonic:

$$R_k\equiv\Re(Z_k)/Z_{cs} \tag{5.32}$$

$$X_k \equiv \Im(Z_k)/Z_{cs} \tag{5.33}$$

Here, (5.25) represents the real-valued equation resulting from the $k = 0$ case, while (5.26) and (5.27) are the real and imaginary parts of the remaining, complex-valued equations.

This system (5.25)-(5.27) may be solved using any conventional linear algebra solution technique appropriate for homogeneous systems, or with software packages such as MATLAB or MAPLE. If a solved manually, or if a symbolic solution routine is used, the coefficients may be found without resorting to floating-point numerical approximations.

In most cases, the amplifier is operated with a switch duty cycle of 50%, in which case, the system (5.25)-(5.27) becomes:

$$\frac{1}{2}a_0 - \sum_{l \in T} \frac{\gamma_l}{\pi l} b_l + \frac{1}{2\pi} Q = 0 \tag{5.34}$$

$$\underbrace{\left[\frac{1}{4} - \frac{kX_k}{2}\right] \cdot a_k + \frac{kR_k}{2} b_k + \sum_{l \in \{T-k\}} \left[\frac{l \cdot \gamma_{k+l}}{\pi(k^2 - l^2)} b_l\right] + \frac{1}{2\pi k} Q = 0}_{\forall k \in T} \tag{5.35}$$

$$\underbrace{\frac{kR_k}{2} a_k + \left[\frac{kX_k}{2} - \frac{1}{4}\right] \cdot b_k + \frac{\gamma_k}{\pi k} a_0 + \sum_{l \in \{T-k\}} \left[\frac{k \cdot \gamma_{k+l}}{\pi(k^2 - l^2)} b_l\right] = 0}_{\forall k \in T} \tag{5.36}$$

where:

$$\gamma_k \equiv \begin{cases} 0 & k \text{ even} \\ 1 & k \text{ odd} \end{cases} \tag{5.37}$$

As a concrete example, a matrix equation implementing (5.34)-(5.36) for $T = \{1, 2, 3, 4\}$ follows. As can be seen, the system is underdetermined, the matrix having $2|T| + 2 = 10$ columns but only $2|T| + 1 = 9$ rows:

$$\begin{bmatrix} \frac{1}{2} & 0 & -\frac{1}{\pi} & 0 & 0 & 0 & -\frac{1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\ 0 & \left(\frac{1}{4}-\frac{X_1}{2}\right) & \frac{R_1}{2} & 0 & -\frac{2}{3\pi} & 0 & 0 & 0 & -\frac{4}{15\pi} & \frac{1}{2\pi} \\ \frac{1}{\pi} & \frac{R_1}{2} & \left(\frac{X_1}{2}-\frac{1}{4}\right) & -\frac{1}{3\pi} & 0 & 0 & 0 & -\frac{1}{15\pi} & 0 & 0 \\ 0 & 0 & \frac{1}{3\pi} & \left(\frac{1}{4}-X_2\right) & R_2 & 0 & -\frac{3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\ 0 & \frac{2}{3\pi} & 0 & R_2 & \left(X_2-\frac{1}{4}\right) & -\frac{2}{5\pi} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{5\pi} & \left(\frac{1}{4}-\frac{3X_3}{2}\right) & \frac{3R_3}{2} & 0 & -\frac{4}{7\pi} & \frac{1}{2\pi} \\ \frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & \frac{3R_3}{2} & \left(\frac{3X_3}{2}-\frac{1}{4}\right) & -\frac{3}{7\pi} & 0 & 0 \\ 0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \left(\frac{1}{4}-2X_4\right) & 2R_4 & \frac{1}{2\pi} \\ 0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & \left(2X_4-\frac{1}{4}\right) & 0 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ a_2 \\ b_2 \\ a_3 \\ b_3 \\ a_4 \\ b_4 \\ Q \end{bmatrix} = \mathbf{0} \tag{5.38}$$

5.3.1 Finding the Waveforms

Having found the necessary coefficients, it is now necessary to find the switching waveforms. The switching current waveform may be found using (5.6):

$$i_s(\theta) = \begin{cases} Q\delta(\theta) - a_0 - \sum_{k \in T} [a_k \cos(k\theta) + b_k \sin(k\theta)] & 0 < \theta < 2\pi D \\ 0 & 2\pi D < \theta < 2\pi \end{cases} \tag{5.39}$$

The capacitor current i_{cs} may be found, if desired, using (5.8):

$$i_{cs}(\theta) = \begin{cases} -Q\delta(\theta) & 0 < \theta < 2\pi D \\ -a_0 - \sum_{k \in T} [a_k \cos(k\theta) + b_k \sin(k\theta)] & 2\pi D < \theta < 2\pi \end{cases} \tag{5.40}$$

The voltage waveform may be found by using (5.15) and (5.40):

$$v_s(\theta) = \begin{cases} 0 & 0 < \theta < 2\pi D \\ -Z_{cs} \int_{2\pi D}^{\theta} \left[a_0 + \sum_{k \in T} (a_k \cos(k\phi) + b_k \sin(k\phi)) \right] d\phi & 2\pi D < \theta < 2\pi \end{cases} \tag{5.41}$$

Evaluation of this integral yields:

$$v_s(\theta) = \begin{cases} 0 & 0 < \theta < 2\pi D \\ Z_{cs} a_0 (2\pi \bar{D} - \theta) + \sum_{k \in T} \left[\begin{array}{l} Z_{cs} \frac{a_k}{k} (\sin(2\pi k D) - \sin(k\theta)) \\ + Z_{cs} \frac{b_k}{k} (\cos(k\theta) - \cos(2\pi k D)) \end{array} \right] & 2\pi D < \theta < 2\pi \end{cases} \quad (5.42)$$

5.3.2 Solving for a Given I_{DD}

The above solution technique is complete when taken together with the bias scaling rules introduced in Chapter 3, since the solution for any desired dc bias level may be found by finding any non-zero solution and scaling the waveforms appropriately. A more elegant way is to simply introduce the dc bias condition into the system to be solved. The formula for the dc bias current in terms of the unknowns in the solution is quite simple:

$$I_{DC} = -a_0 \quad (5.43)$$

By introducing this additional constraint into (5.25)-(5.27) or (5.34)-(5.36) will yield an inhomogeneous system with the same number of equations as variables. Assuming this system is determined (i.e. a solution exits with non-zero bias current), the system may be solved with standard numerical techniques appropriate for inhomogeneous systems. As a more concrete example, with this additional condition the matrix equation (5.38) would become:

$$\begin{bmatrix}
\frac{1}{2} & 0 & -\frac{1}{\pi} & 0 & 0 & 0 & -\frac{1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \left(\frac{1}{4}-\frac{X_1}{2}\right) & \frac{R_1}{2} & 0 & -\frac{2}{3\pi} & 0 & 0 & 0 & -\frac{4}{15\pi} & \frac{1}{2\pi} \\
\frac{1}{\pi} & \frac{R_1}{2} & \left(\frac{X_1}{2}-\frac{1}{4}\right) & -\frac{1}{3\pi} & 0 & 0 & 0 & -\frac{1}{15\pi} & 0 & 0 \\
0 & 0 & \frac{1}{3\pi} & \left(\frac{1}{4}-X_2\right) & R_2 & 0 & -\frac{3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{2}{3\pi} & 0 & R_2 & \left(X_2-\frac{1}{4}\right) & -\frac{2}{5\pi} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{2}{5\pi} & \left(\frac{1}{4}-\frac{3X_3}{2}\right) & \frac{3R_3}{2} & 0 & -\frac{4}{7\pi} & \frac{1}{2\pi} \\
\frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & \frac{3R_3}{2} & \left(\frac{3X_3}{2}-\frac{1}{4}\right) & -\frac{3}{7\pi} & 0 & 0 \\
0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \left(\frac{1}{4}-2X_4\right) & 2R_4 & \frac{1}{2\pi} \\
0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & \left(2X_4-\frac{1}{4}\right) & 0 \\
-1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ a_2 \\ b_2 \\ a_3 \\ b_3 \\ a_4 \\ b_4 \\ Q \end{bmatrix}
=
\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ I_{DC} \end{bmatrix} \tag{5.44}$$

5.3.3 Solving for a Given V_{DC}

A similar approach may be used to determine the solution for a given dc bias voltage. Integrating (5.42) to find the average value of the voltage waveform yields:

$$V_{DC} = \pi Z_{cs} \bar{D}^2 a_0 + Z_{cs} \sum_{k \in T} \left[\begin{array}{c} \left(\frac{D \sin(2\pi k D)}{k} + \frac{1 - \cos(2\pi k D)}{2\pi k^2} \right) a_k \\ -\left(\frac{D \cos 2\pi k D}{k} + \frac{\sin 2\pi k D}{2\pi k^2} \right) b_k \end{array} \right] \tag{5.45}$$

for the case of 50% duty cycle, this becomes:

$$V_{DC} = \frac{\pi Z_{cs}}{4} a_0 + Z_{cs} \sum_{k \in T} \left[\frac{\gamma_k}{\pi k^2} a_k + \frac{2\gamma_k - 1}{k} b_k \right] \tag{5.46}$$

Since this dc voltage is also a linear function of the unknowns in the solution, this constraint may be added to either (5.25)-(5.27) or (5.34)-(5.36) to yield a inhomogeneous system with the same number of conditions as unknowns. Again, this solution may be

found if the system is determined. A more concrete example follows, again adding the bias condition to the matrix equation (5.38):

$$\begin{bmatrix}
\frac{1}{2} & 0 & -\frac{1}{\pi} & 0 & 0 & 0 & -\frac{1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \left(\frac{1}{4}-\frac{X_1}{2}\right) & \frac{R_1}{2} & 0 & -\frac{2}{3\pi} & 0 & 0 & 0 & -\frac{4}{15\pi} & \frac{1}{2\pi} \\
\frac{1}{\pi} & \frac{R_1}{2} & \left(\frac{X_1}{2}-\frac{1}{4}\right) & -\frac{1}{3\pi} & 0 & 0 & 0 & -\frac{1}{15\pi} & 0 & 0 \\
0 & 0 & \frac{1}{3\pi} & \left(\frac{1}{4}-X_2\right) & R_2 & 0 & -\frac{3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{2}{3\pi} & 0 & R_2 & \left(X_2-\frac{1}{4}\right) & -\frac{2}{5\pi} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{2}{5\pi} & \left(\frac{1}{4}-\frac{3X_3}{2}\right) & \frac{3R_3}{2} & 0 & -\frac{4}{7\pi} & \frac{1}{2\pi} \\
\frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & \frac{3R_3}{2} & \left(\frac{3X_3}{2}-\frac{1}{4}\right) & -\frac{3}{7\pi} & 0 & 0 \\
0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \left(\frac{1}{4}-2X_4\right) & 2R_4 & \frac{1}{2\pi} \\
0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & \left(2X_4-\frac{1}{4}\right) & 0 \\
\frac{\pi Z_{cs}}{4} & \frac{1}{\pi} & 1 & 0 & -\frac{1}{2} & \frac{1}{9\pi} & \frac{1}{3} & 0 & -\frac{1}{4} & 0
\end{bmatrix}
\begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ a_2 \\ b_2 \\ a_3 \\ b_3 \\ a_4 \\ b_4 \\ Q \end{bmatrix}
=
\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_{DC} \end{bmatrix} \tag{5.47}$$

5.4 Determining a ZVS Tuning

Although the results of the previous section allow the analysis of switching amplifiers in a very general sense, the problem of design synthesis has not yet been addressed. Fortunately, the method can be modified to allow the proper choice of the load impedances to be found which achieve certain waveform conditions. In this section, two such conditions will be analyzed, namely the class-E switching condition requirements: zero-voltage switching (ZVS) and zero-voltage slope switching (ZdVS).

The ZVS condition demands that the voltage on the switch at the instant prior to the switch closing should be zero. This condition allows the amplifier to avoid additional loss due to discharge of the switch's output capacitance. This condition is equivalent to the demand that the discharge Q should be zero:

$$Q = 0 \tag{5.48}$$

This condition may be added to either (5.25)-(5.27) or (5.34)-(5.36) to generate a set of linear homogeneous equations which the ZVS switching amp would have to satisfy, but the system then would have the same number of equations as unknowns. Therefore, the system is not guaranteed to have a non-trivial solution, corresponding to the reality that not just any tuning can generate ZVS waveforms. For a non-trivial solution to exist, the system must be underdetermined, a condition which may be imposed by demanding that the determinant of the coefficient matrix be zero. In the case of the matrix equation (5.38), for instance, the condition may be written as:

$$\begin{vmatrix}
\frac{1}{2} & 0 & -\frac{1}{\pi} & 0 & 0 & 0 & -\frac{1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \left(\frac{1}{4}-\frac{X_1}{2}\right) & \frac{R_1}{2} & 0 & -\frac{2}{3\pi} & 0 & 0 & 0 & -\frac{4}{15\pi} & \frac{1}{2\pi} \\
\frac{1}{\pi} & \frac{R_1}{2} & \left(\frac{X_1}{2}-\frac{1}{4}\right) & -\frac{1}{3\pi} & 0 & 0 & 0 & -\frac{1}{15\pi} & 0 & 0 \\
0 & 0 & \frac{1}{3\pi} & \left(\frac{1}{4}-X_2\right) & R_2 & 0 & -\frac{3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{2}{3\pi} & 0 & R_2 & \left(X_2-\frac{1}{4}\right) & -\frac{2}{5\pi} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{2}{5\pi} & \left(\frac{1}{4}-\frac{3X_3}{2}\right) & \frac{3R_3}{2} & 0 & -\frac{4}{7\pi} & \frac{1}{2\pi} \\
\frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & \frac{3R_3}{2} & \left(\frac{3X_3}{2}-\frac{1}{4}\right) & -\frac{3}{7\pi} & 0 & 0 \\
0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \left(\frac{1}{4}-2X_4\right) & 2R_4 & \frac{1}{2\pi} \\
0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & \left(2X_4-\frac{1}{4}\right) & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1
\end{vmatrix} = 0 \tag{5.49}$$

Values must be chosen for the tuning impedances which satisfy this expression if a ZVS tuning is to result. The most common case is where the impedances of the harmonic overtones are fixed, but it is desired to adjust the fundamental frequency load to achieve the ZVS conditions. As can be observed in (5.49), the fundamental frequency load impedance only shows up as a term in four matrix entries, two R_1 entries and two X_1 entries corresponding to the resistance and reactance respectively. This implies that the

determinant is at most quadratic in each of these variables. Furthermore, these entries are located in such a way such that every R_1 entry is located in the same row as one X_1 entry and in the same column as the other X_1 entry, and that every X_1 entry is located in the same row as one R_1 entry and in the same column as the other. This implies that the coefficient of the X_1R_1 term must be zero. Also, the coefficient of each X_1 and R_1 term is identical save for a negative sign on one, and so the coefficients of the X_1^2 and R_1^2 components are identical. As a result, (5.49) must be in the form:

$$(X_1 - C_X)^2 + (R_1 - C_R)^2 - C_Z^2 = 0 \tag{5.50}$$

Although the analysis has been applied to the specific case of equation (5.49), this result is true in general, following from the same arguments. The resulting equation indicates that the fundamental frequency impedance must lie on a circle in the impedance plane, where the center of the circle (C_X,C_R) and the radius C_Z are determined by the impedances of the tuned overtones. The constraint that this shape must be a circle has important consequences in design for load-invariant ZVS amplifiers since any change in the load must follow a path which can be mapped into a circle in the impedance plane if ZVS is to be preserved. It may be possible also that the value of the squared radius C_Z^2 may turn out to be negative, indicating that no ZVS solution is possible for that particular tuning of the overtones, although this condition has never been encountered by this author in practice. There is also the possibility that the positioning of the circle is such that contains no points with $R_1 > 0$, which would also indicate that no ZVS amplifier[1] solution is possible using that tuning for the overtones. Again, this has never been encountered by this author in practice. Fig. 5.3 shows the ZVS circle for the case of class-E tuning of the overtones (i.e. there is no tuning of the overtones).

1. Interestingly, the solution technique is also feasible for use in solving the waveforms of synchronous resonant rectifiers [46]. With suitable interpretation of the result, an amplifier "solution" having a negative load resistance – e.g. one receiving power from the load rather than delivering power to it – is equivalent to the solution for a similarly tuned rectifier.

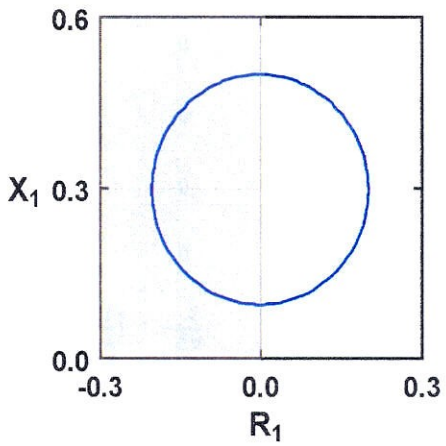


Figure 5.3: Class-E ZVS circle in the (normalized) impedance plane. The shaded area is non-physical for amplifiers since the load resistance is negative.

As in the class-E case, this ZVS solution is actually a continuous range of solutions due to the fact that there are two available degrees of freedom being used to set only a single condition. The second degree of freedom may be utilized to set an additional condition, such as the ZdVS zero voltage slope switching condition. Fortunately, the slope of the voltage is also a linear function of the current coefficients:

$$\frac{dV_s}{d\theta} = Z_{cs} i_{cs} \tag{5.51}$$

Evaluating this expression at the turn-on time yields:

$$\left.\frac{dV_s}{d\theta}\right|_{\theta = 0} = Z_{cs} \sum_{k \in \{0.\, T\}} a_k \tag{5.52}$$

The required condition for achieving ZdVS switching conditions is then:

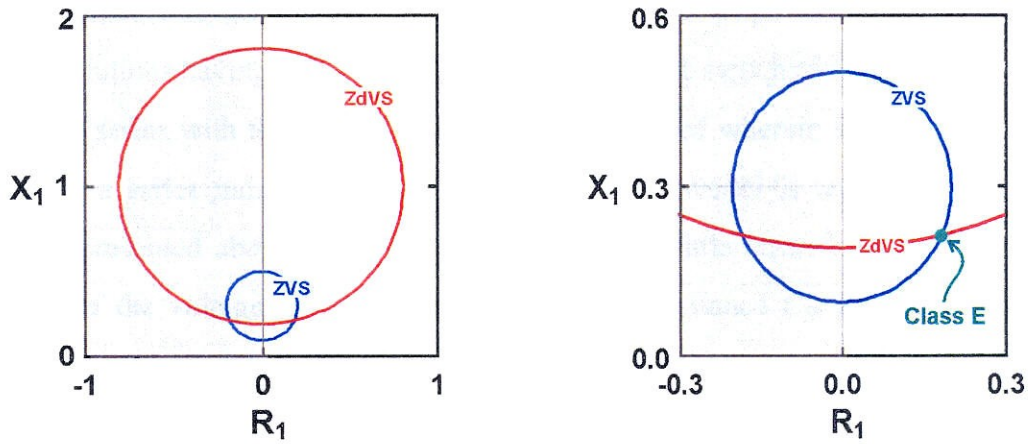
$$\sum_{k \in \{0.\, T\}} a_k = 0 \tag{5.53}$$

Adding this condition to (5.38) would result in:

$$\begin{vmatrix}
\frac{1}{2} & 0 & -\frac{1}{\pi} & 0 & 0 & 0 & -\frac{1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \left(\frac{1}{4}-\frac{X_1}{2}\right) & \frac{R_1}{2} & 0 & -\frac{2}{3\pi} & 0 & 0 & 0 & -\frac{4}{15\pi} & \frac{1}{2\pi} \\
\frac{1}{\pi} & \frac{R_1}{2} & \left(\frac{X_1}{2}-\frac{1}{4}\right) & -\frac{1}{3\pi} & 0 & 0 & 0 & -\frac{1}{15\pi} & 0 & 0 \\
0 & 0 & \frac{1}{3\pi} & \left(\frac{1}{4}-X_2\right) & R_2 & 0 & -\frac{3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{2}{3\pi} & 0 & R_2 & \left(X_2-\frac{1}{4}\right) & -\frac{2}{5\pi} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{2}{5\pi} & \left(\frac{1}{4}-\frac{3X_3}{2}\right) & \frac{3R_3}{2} & 0 & -\frac{4}{7\pi} & \frac{1}{2\pi} \\
\frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & \frac{3R_3}{2} & \left(\frac{3X_3}{2}-\frac{1}{4}\right) & -\frac{3}{7\pi} & 0 & 0 \\
0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \left(\frac{1}{4}-2X_4\right) & 2R_4 & \frac{1}{2\pi} \\
0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & \left(2X_4-\frac{1}{4}\right) & 0 \\
1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0
\end{vmatrix} = 0 \qquad (5.54)$$

Finding a set of harmonic impedances satisfying this condition will guarantee a ZdVS solution exists. This expression must also be in the form of a circle in the fundamental frequency impedance plane, for the same reasons as in the ZVS case[1]. If this circle and the ZVS tuning circle intersect, the tuning corresponding to that intersection point will have a ZVS and ZdVS solution. This author has never encountered a case for which this ZVS/ZdVS tuning point cannot be achieved, but it is reasonable to suspect that this may occur in some special cases. Fig. 5.4 shows the ZVS and ZdVS circles for a class-E tuning. The intersection point of the ZVS and ZdVS circles in the positive resistance half-plane is the "optimal" ZVS/ZdVS class-E tuning.

1. Generally, constraints expressible as a linear homogeneous equation of the a_k, b_k, and Q coefficients will lead to a circular locus of solutions in the impedance plane of any harmonic if the impedances of the other harmonics are kept fixed.



(a) (b)

Figure 5.4: Class-E ZVS and ZdVS circles in the (normalized) impedance plane (a) and close-up of the ZVS circle (b). The green point at the intersection of the circles is the location of the well-known "optimal" class-E amplifier. The shaded areas are non-physical for amplifiers since the load resistance is negative

5.5 Other Applications

Although the application of this solution technique in this work concentrates on its use in 50% duty cycle switching amplifiers, the solution technique itself allows for any duty cycle to be used. Furthermore, the technique may be extended to even include more than two switch transitions per fundamental period, provided that an additional discharge basis function is added for each additional turn-on transition. It is likely that there are performance benefits associated with duty cycles other than 50%, and an analytic technique to treat more complex switching behaviors may open up new applications for resonant switching power systems [58].

By utilizing the negative resistance region of the impedance plane, the technique may predict performance of harmonic-tuned rectifiers. Such rectifiers are primarily useful in dc/dc converters where they play an essential role [1, e.g. 59]. By appropriately modifying this technique, a tool for exploration of potential performance enhancements for resonant synchronous rectifiers may be found.

Also, much like the duality between ZVS and ZCS amplifiers, there is a duality between solutions having a capacitance in parallel with the switch and solutions having an inductor in series with the switch. If a case is encountered wherein the dominant switch parasitic is a series inductance and a resonant ZCS converter is required, the solution technique presented above may be modified with very little effort by interchanging the functions of the voltages and currents. The shunt capacitance C_S, having conductance proportional to the frequency becomes a series inductor having impedance proportional to the frequency. The harmonic tuning network presents specified conductances at selected harmonics, but short-circuit at other, un-tuned ones. The voltage is commutated between the switch and the inductor, with a discharge voltage ensuring a Volt-second balance in the inductor.

It may be possible to extend the solution technique to also treat other switching amplifier problems. For instance, it may be possible to explicitly include the effect of the switch on-resistance, providing a means to find the switching waveforms even when significantly distorted by the presence of this resistance. It may also be possible to incorporate the effect of a time-varying on-resistance in order to predict the effect of the finite time required for the switch to change states. Furthermore, it may be possible to solve a system including several switches with capacitances both across each switch and between each switch. This would allow an extension of the push/pull concept used in the class E/F_{odd} amplifiers introduced in Chapter 7. Each of these extensions would require an understanding of how the filter current(s) i_x commutate between the various elements, and how discharge currents behave when there is a finite and possibly time-varying on-resistance.

Chapter 6

The E/F Switching Amplifier Family

With methods in hand for the prediction of switching amplifier waveforms and for comparisons between candidate tunings, the discussion turns toward finding these candidates. If, for instance, class E were the only possible tuning having the benefits of ZVS switching and output capacitance compensation, the discussions of other possible tunings would be rendered academic, being intellectually interesting but relatively useless. This is equally true if other tunings exist, but achieve performance equal to or worse than class E. Due to the simplicity of the basic class-E circuit, it is unlikely that other tunings are implementable with less circuit complexity[1], and so a new tuning would have to improve upon the class-E performance. This chapter presents a first attempt to identify broad classes of candidate tunings in the quest to improve upon class E.

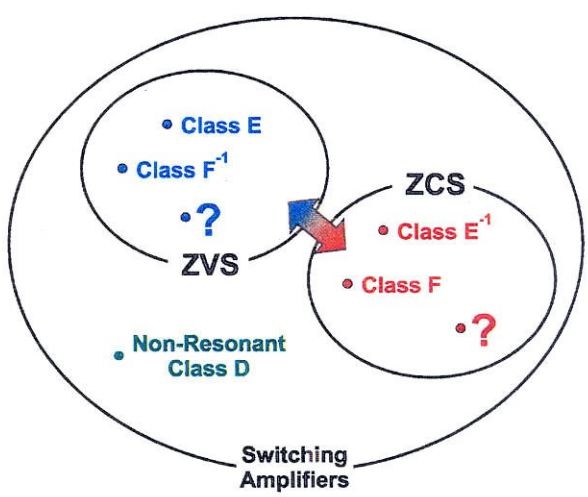


Figure 6.1: Taxonomy of known switching amplifiers.

1. Actually, the push/pull Class E/F_{odd} tuning discussed in the following chapter achieves considerably improved performance without the need for a larger number of passive elements, albeit using two switches instead of one.

Fig. 6.1 depicts a taxonomy of sorts for the presently known harmonic-tuned switching amplifiers. The particularly useful subset of ZVS amplifiers, for which the ZCS subset is a dual, is known to contain both the class F^{-1} (class D^{-1}) and class E tunings. The first question to be resolved is whether there are other tunings located in this subset which are not merely minor variations of these two basic classes. This question has actually been answered by the second harmonic resonant class-E amplifier [52] discussed in Chapter 3, but this merely shifts the question: Are there more than just these *three* tunings? It would not be unreasonable to suspect that there are, in fact, more tunings which achieve ZVS conditions. Supposing these tunings could be found, it is not unlikely that some may allow for performance improvements according to the measures introduced in Chapter 4. Since the tools developed in Chapter 5 allow for rapid and accurate investigation, the stage is set exploration.

6.1 Desired Properties

Before proceeding, it is prudent to clearly state the properties of a desirable tuning. First, it should obviously have all the advantages afforded by class-E tuning:

- ZVS switching.
- Compensation for the effect of output capacitance.
- Simple (as possible) circuit implementation.

In addition, the tuning should achieve better performance according to the measures introduced in Chapter 4. Thus, better waveform figures of merit are desired:

- Lower peak voltage (lower F_V)
- Lower RMS current (lower F_I)
- Improved capacitance tolerance (lower F_C)

6.2 The Class E/F Concept

An obvious first line of inquiry might attempt to achieve a hybrid between class F or class F^{-1}, these having the benefit of improved waveforms, and class E, it having the benefits of capacitance tolerance and circuit simplicity. The class E/F amplifier, as its name suggests, is such a strategy, being constructed as a frequency-domain hybrid between class E and class F^{-1}. Class F^{-1} is a more natural choice than class F as a target for a ZVS amplifier since the ideal waveforms of this class are ZVS, unlike class F waveforms which for the ideal case (i.e. all harmonics tuned, or class D) have discontinuities in the voltage waveform during the switching events.

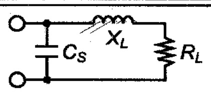
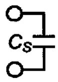
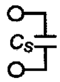
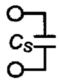
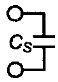
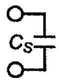
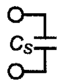
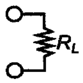
Tuning	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	$6f_0$	$7f_0$	$8f_0$
Class E								
Class F^{-1}		open	short	open	short	open	short	open
New Hybrid	?	?	?	?	?	?	?	?

Table 6.1: Frequency-domain specifications for class E and Class F^{-1}.

The harmonic-tuning specifications for class E and class F^{-1} are shown in Table 6.1. As can be seen, class E is constructed so that, except for the fundamental frequency, the only load seen by the switch is the switch parallel capacitance C_s. The fundamental frequency load is then adjusted to achieve ZVS switching conditions. Class F^{-1}, in contrast, tunes all harmonics to open-circuit or odd-circuit for even and odd harmonics respectively. Under this tuning, the optimal load impedance is purely resistive.

To accomplish a hybrid of these two tunings, an approach has been developed which seems at first somewhat haphazard, but ultimately justifies itself. The method is simple: at each overtone choose to tune that harmonic as if it were either class E or class F^{-1}. For instance, one might construct an amplifier for which each overtone is tuned to a

capacitance except for the second harmonic which is open-circuited. Alternatively, one might short-circuit the third harmonic and open-circuit the sixth, while leaving all others capacitively loaded. By tuning some harmonics as to class F^{-1} impedances, it is hoped that the waveforms may take on some of the desirable qualities of this tuning.

It might be imagined that this rule would also apply to the fundamental frequency, so that the designer would arbitrarily choose either the class-E or class-F^{-1} load for that frequency. This would be foolish, however, since it is almost certain this would not result in a ZVS tuning. Instead, it has been found empirically that the required fundamental frequency tuning is one having the same form as in class-E – i.e. a load consisting of resistance and inductance – but having values dependent on the tuning of the overtone harmonics. By choosing the appropriate values for the fundamental frequency load resistance R_L and the reactance X_L, the waveforms are made to switch at zero voltage and, if desired, zero voltage slope.

Since this hybridization approach results in not just one new class, but an infinite number of variations according to which harmonics have been tuned, a naming system is required which uniquely identifies each variation. The naming system proposed is class E/F_x where the subscript is the list of harmonics tuned to class F^{-1} impedances. For instance, if the second and fifth harmonics are open-circuited and short-circuited respectively while all other harmonics are tuned to a capacitive load, a class $E/F_{2,5}$ results. It should also be noted that class E and class F^{-1} are themselves members of the E/F family, corresponting to the extreme cases of no tuned harmonics and all harmonics tuned respectively. In this sense, the E/F concept is a generalization of the E and F^{-1} tunings. Examples of class E/F tuning requirements are shown in Table 6.2.

6.3 Class E/F Waveforms

Using the results of Chapter 5, the fundamental frequency load required for ZVS/ZdVS switching conditions and the resulting switching waveforms may be

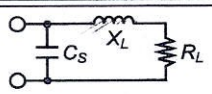
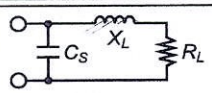
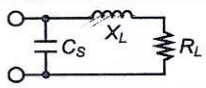
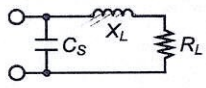
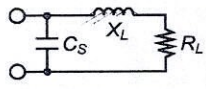
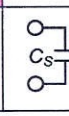
Tuning	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	$6f_0$	$7f_0$	$8f_0$
Class E								
Class F^{-1}		open	short	open	short	open	short	open
Class E/F_2		open						
Class E/F_3			short					
Class $E/F_{2,4,7}$		open		open			short	
Class $E/F_{2,3,4,5}$		open	short	open	short			

Table 6.2: Frequency-domain specifications for several class E/F amplifiers

calculated. In fact, such an exercise effectively demonstrates the utility of this solution method. Early investigations of E/F amplifiers using PSPICE could easily require several hours of simulation and parameter tuning to find the circuit for ZVS operation and special care was required to avoid convergence problems. Using a MAPLE program implementing the Chapter 5 solution technique results in effectively instantaneous determination of the appropriate tuning and the resulting waveforms.

Sample E/F waveforms are depicted in Fig. 6.2. As hoped, the waveforms contain features both of class-E and class-F^{-1} amplifiers. Like class E, the voltage waveform switches at zero voltage and zero voltage slope, while the current waveform has a discontinuity at the switch turn off, as is required in a ZVS amplifier [60,61]. Immediately promising features include an obviously lower peak voltage in many cases, as well as several cases of current waveforms closely approximating a square waveform. Before examining these features more closely, the general behavior of the waveforms with respect to the harmonic tuning will be explored.

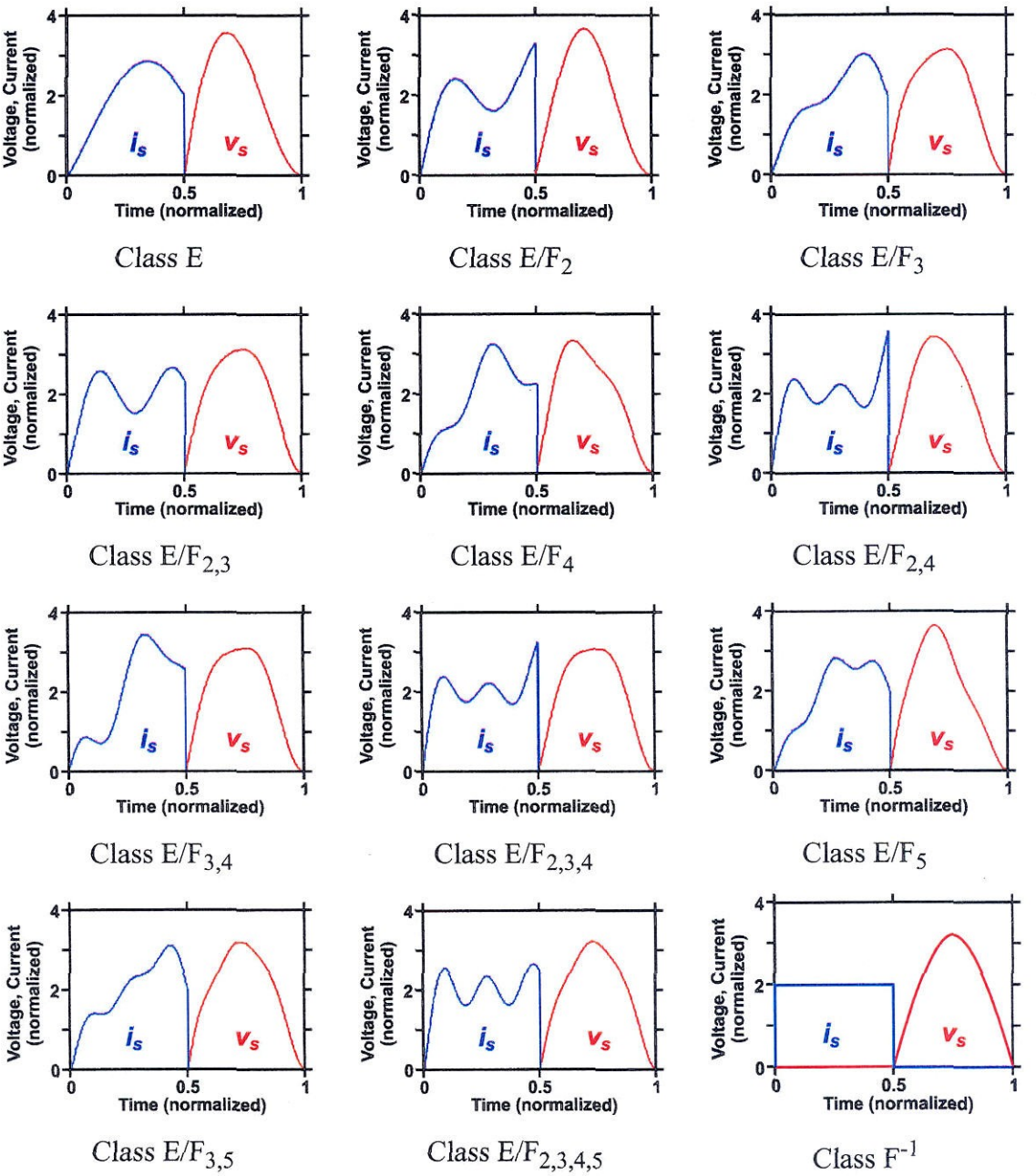


Figure 6.2: Switching waveforms for some members of the class E/F ZVS switching amplifier family. Each amplifier (excepting class F^{-1}) is tuned for ZVS/ZdVS (class-E) switching conditions. Waveforms are normalized to unity dc voltage and current.

6.3.1 Individual Tuned Harmonics

The first case of interest is the effect of tuning a single harmonic at a time. Waveforms for individual tuned harmonics up to the 6^{th} are presented in Fig. 6.3. Tuning of low order harmonics result in waveforms which are clearly different from class E. E/F_2, which is similar to the second harmonic resonant class E discussed earlier, shows a substantially improved current waveform. E/F_3 provides much lower peak voltage. In these cases, waveform improvements are apparent.

Higher harmonic tunings do not present such advantages. E/F_4, for instance, does not show any obvious improvement in either the voltage or the current waveform. E/F_5 has a slightly better current waveform, but an obviously higher peak voltage. Additionally, as is apparent in E/F_5 and E/F_6, tuning of the higher harmonics begins to take the form of a ringing superimposed on the basic class-E waveforms. This is consistent with the observations of class-E designers [51] who often notice such ringing on measured waveforms due to high frequency resonances.

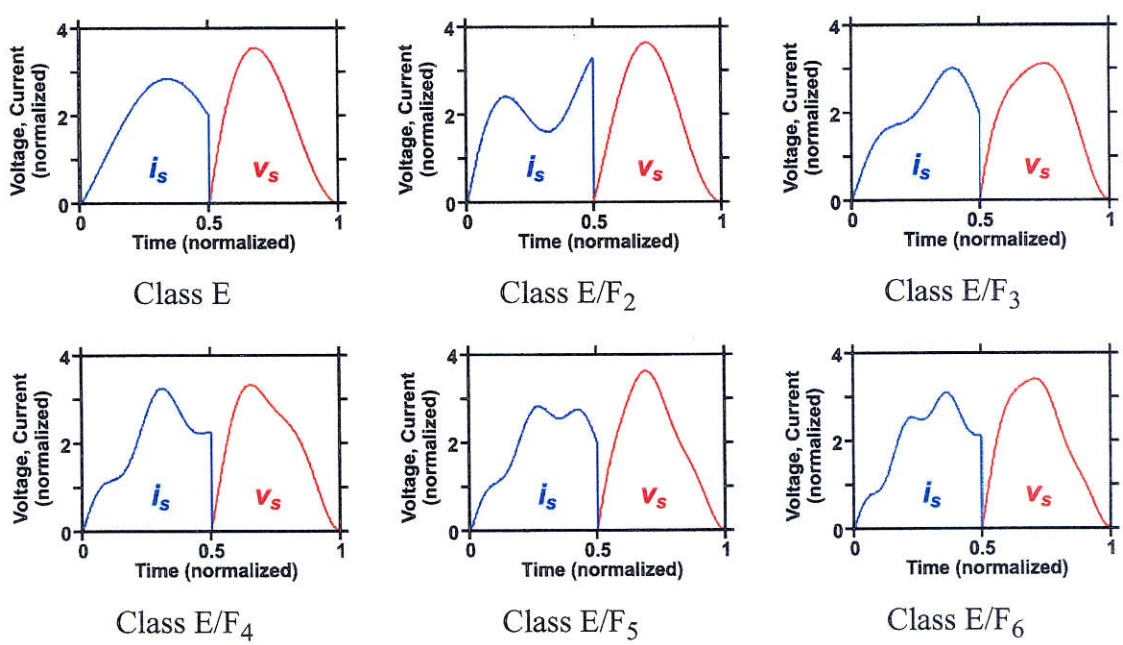


Figure 6.3: Single-harmonic class E/F ZVS switching amplifiers. Each amplifier is tuned for ZVS/ZdVS (class-E) switching conditions. Waveforms are normalized to unity dc voltage and current.

6.3.2 Odd Harmonics

The next case of interest is the effect of tuning increasing numbers of odd harmonics. Waveforms corresponding to increasingly tuning odd harmonics are presented in Fig. 6.4. The most obvious feature is that the waveforms seem to be converging to a limiting case as additional odd harmonics are tuned, a speculation which will be verified in the next chapter. The voltage waveform converges rapidly to the half-sinusoidal waveform of class-F^{-1}, being nearly indistinguishable from the 9^{th} harmonic onward. This indicates that even-harmonic tuning is unnecessary to achieve the voltage waveforms of class F^{-1}.

The limiting current waveform seems to be an almost trapezoidal shape, although it will be shown in the next chapter to be a square wave superimposed with a half-cosine. The class-E characteristic "leaning" of the current waveform towards the turn-off point is retained, and if there appears to be little improvement with regard to the RMS current.

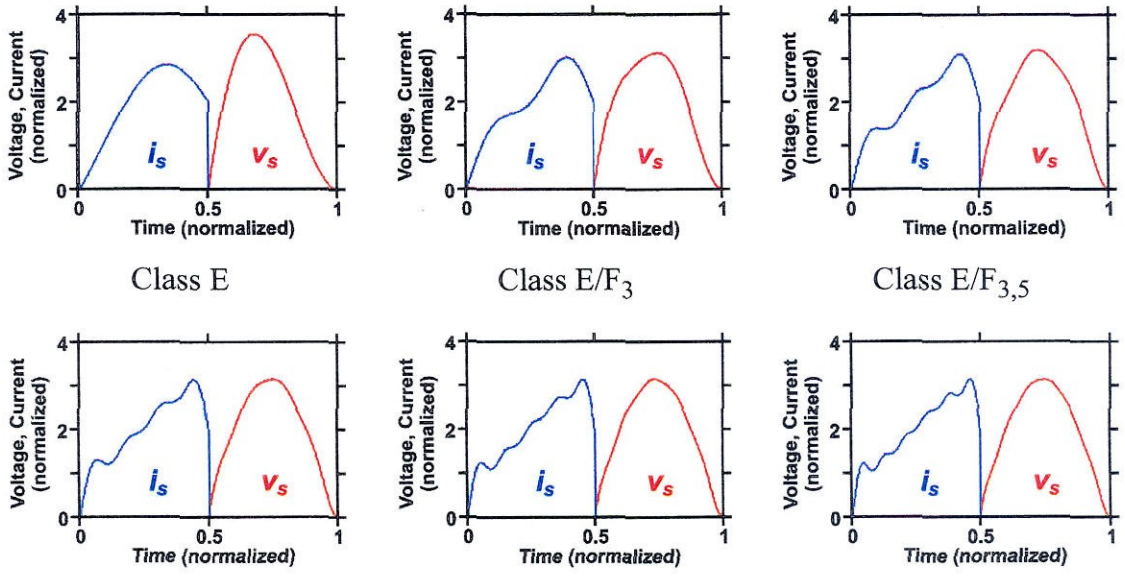


Figure 6.4: Odd-harmonic class E/F ZVS switching amplifiers. Each amplifier is tuned for ZVS/ZdVS (class-E) switching conditions. Waveforms are normalized to unity dc voltage and current.

6.3.3 Even Harmonics

Fig. 6.5 shows waveforms resulting from increasing numbers of even harmonics tuned. As might be expected, since the voltage waveform primarily effects the odd harmonics, the effect of the even harmonics is primarily on the current waveform. In this case, the current waveform rapidly converges to a square wave, with the voltage waveform remaining largely unaffected.

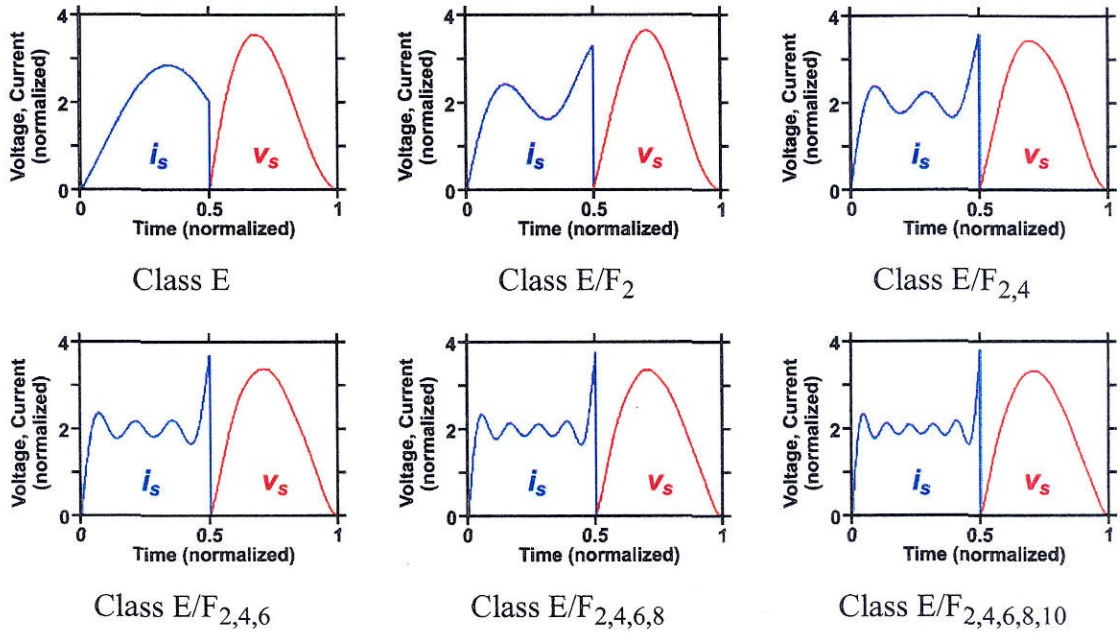


Figure 6.5: Even-harmonic class E/F ZVS switching amplifiers. Each amplifier is tuned for ZVS/ZdVS (class-E) switching conditions. Waveforms are normalized to unity dc voltage and current.

6.3.4 Complete N-Harmonic Tunings

In order to achieve the benefits of class F^{-1} in both the voltage *and* current waveforms, then, it seems that both the even and odd harmonics need to be tuned. Similar to the class-F idea of tuning all lowest order harmonics up to a number N, the complete N-harmonic class E/F amplifiers may be generated. The resulting waveforms, shown in Fig. 6.6, indicate that these tunings have similar characteristics to the class-F^{-1} tuning

strategy, the voltage and current waveforms increasingly resembling a half-sinusoid and a square wave respectively as additional harmonics are tuned.

It should be stressed that, unlike class-F^{-1}, harmonics with higher number than N *are* present in the waveforms and serve to increase the efficiency by reducing the voltage and current waveform overlap achievable in principle to zero. Thus this set of amplifiers may take on the class F -like characteristic of tuning additional harmonics to more closely approximate square and half-sinusoidal waveforms, while also achieving the efficiency benefits of having higher, capacitively-tuned harmonics present in the waveforms.

This suggests a different approach to class-F^{-1} design. Conventional analysis of class-F^{-1} assumes that 100% efficiency can be achieved only by carefully tuning a large number of harmonics to alternating short and open circuits. As these waveforms show, however, it is only necessary to tune a few harmonics to achieve class F^{-1} -like waveforms while eliminating waveform overlap allowing 100% efficiency in principle. The only required change is a slightly inductive load at the fundamental to achieve ZVS switching.

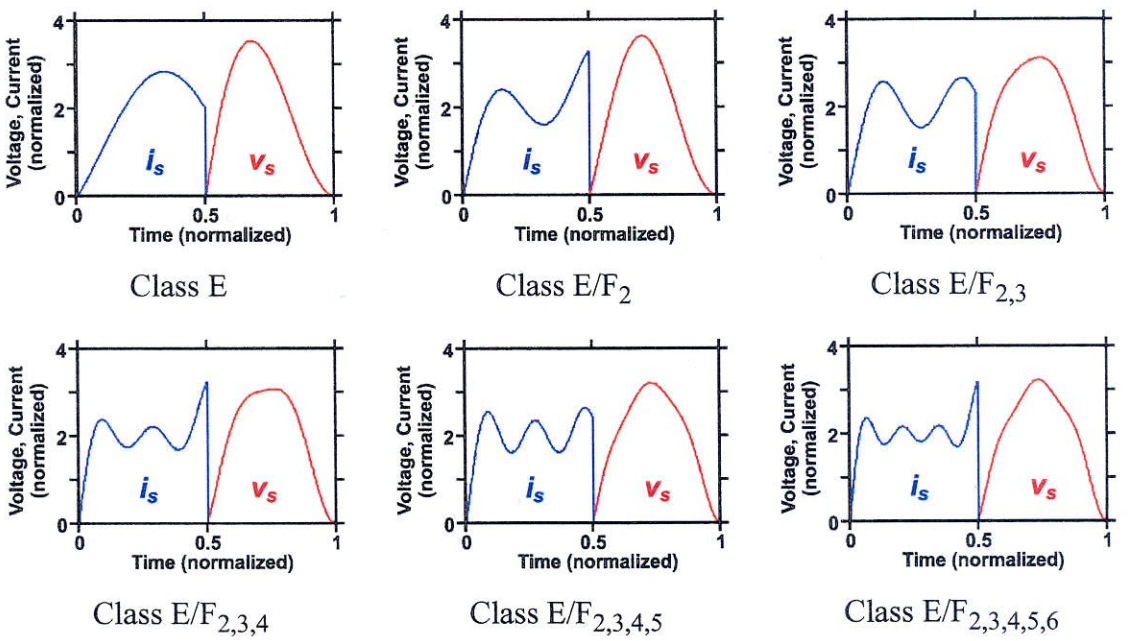


Figure 6.6: Complete N-harmonic class E/F ZVS switching amplifiers. Each amplifier is tuned for ZVS/ZdVS (class-E) switching conditions. Waveforms are normalized to unity dc voltage and current.

6.4 Class E/F Performance Figures of Merit

Having established the existence of this new E/F family of switching amplifier classes, and visually observed encouraging characteristics in the waveforms, a more careful analysis of the waveform properties is in order.

	Waveform Merit				Performance Merit (normalized to unity for Class E)				
Tuning	F_V	F_I	F_C	F_{PI}	$F_V^2F_I^2$	$F_I^2F_C$	F_V^2/F_C	$2F_VF_I$	F_VF_{PI}
E	3.56	1.54	3.14	2.86	1.00	1.00	1.00	1.00	1.00
E/F_2	3.67	1.48	**1.13**	3.33	0.98	**0.33**	2.94	0.99	1.20
E/F_3	**3.14**	1.52	3.14	3.06	**0.76**	0.97	**0.78**	0.87	0.94
$E/F_{2,3}$	**3.13**	1.47	2.31	2.67	**0.71**	**0.67**	1.05	**0.84**	**0.82**
E/F_4	3.34	1.55	2.45	3.27	0.89	0.79	1.13	0.94	1.07
$E/F_{2,4}$	3.43	1.46	**0.97**	3.60	0.84	**0.28**	3.00	0.91	1.21
$E/F_{3,4}$	**3.10**	1.62	1.93	3.45	0.84	0.68	1.23	0.91	1.05
$E/F_{2,3,4}$	**3.08**	1.45	**1.18**	3.26	**0.67**	**0.34**	1.99	**0.82**	0.99
E/F_5	3.65	1.53	3.14	2.84	1.04	0.99	1.05	1.02	1.02
$E/F_{3,5}$	3.20	1.51	3.14	3.12	0.78	0.97	**0.78**	0.87	0.94
$E/F_{2,3,4,5}$	3.20	1.45	2.11	2.65	**0.72**	0.60	1.20	**0.85**	**0.83**
F^{-1}	3.14	1.41	N/A	2.00	0.66	N/A	N/A	0.81	0.62

Table 6.3: Waveform and performance figures of merit for several ZVS/ZdVS E/F tunings. Performance figures listed relative to class E. In all cases, smaller numbers indicate better performance.

Waveform and performance figures of merit are listed in Table 6.3. Consistent with the visual observations, the waveform figures of merit are generally quite good. For the tunings selected, only a few of the amplifiers perform worse than class E in the important F_V (peak voltage) or F_I (RMS current) categories. Several tunings actually achieve better peak voltage performance than the class F^{-1} target, and many have comparable performance with regard to RMS current. The peak current in most cases is worse than

class E, but since this measure does not appear in any of the efficiency or gain figures of merit, the performance effect is minimal.

The most striking difference, however, is the capacitance tolerance (F_C). None of the tunings listed has worse tolerance than class E, and several outperform it by a factor of two or even three. Intuitively this is not terribly surprising, since the capacitance is being essentially tuned out at selective frequencies.

Efficiency and gain factors show corresponding improvements. In the case of size-limited drain loss ($F_V^2 F_I^2$), all but one tuning achieve better performance than class E. Some tunings such as $E/F_{2,3,4}$ reduce the drain loss to about 67% that of class E. This improvement puts several class-E/F tunings into the same performance range as ideal class F^{-1} for this measure, potentially reducing the heat sinking requirements by one third.

The gain-limited PAE case ($F_V F_I$), tells a similar story, although the improvements are more modest. Due to the similarity of the size-limited and gain-limited expressions, the same tunings achieve the best performance in both, but the gain-limited improvements are more limited, achieving down to 82% of the class-E loss, or an 18% reduction in heat sinking. Although this is modest, it is nearly equal that of the ideal class F^{-1} case, so the small performance benefit is to be expected.

Due to the greatly improved FC numbers, the greatest improvement is in capacitance-limited performance. By allowing a much greater transistor size to be used, the capacitance-limited drain loss ($F_I^2 F_C$) may be improved greatly, with class $E/F_{2,4}$ achieving a loss just 28% that of class E. Since this improvement is gained largely by an increase in the transistor size, the gain (F_V^2 / F_C) is correspondingly lowered, but in many cases this is tolerable. If the gain is an issue, tunings such as $E/F_{2,3}$ allow a drain loss reduction without significantly reducing the gain. This is accomplished since the lowered peak voltage increases the gain by almost the same factor that the increased size lowers it. In this case, the drain loss may be reduced by 33% while only decreasing the gain by 5%. Of course, even in the other cases, designer is not forced to make full use of the available

gain/efficiency trade-off, being free to choose any transistor size having an output capacitance smaller than the capacitance C_S with the remainder being made up by discrete capacitors.

6.5 Practical Strategies for Implementing E/F

Up to this point, the E/F family has been discussed only in reference to the harmonic tuning impedances. To be usefully employed as a high-efficiency amplifier, it is necessary to implement a circuit to provide this harmonic tuning. Furthermore, it would be desirable if this circuit would have as little complexity as possible (in terms of the number of components required) and introduce as little loss as possible.

6.5.1 Direct Implementations

The most obvious implementation strategy is to simply build the circuit employing a separate bandpass filter and load for each harmonic to be tuned. In essence, the equivalent circuit model of Fig. 5.1 used in calculating the waveforms is constructed. This results in an implementation identical to the class-E circuit except that an additional high-Q resonator is used for each tuned harmonic. For instance, a simple class E/F_3 implementation might use the circuit shown in Fig. 6.7, using a single third-harmonic series LC resonator connected between the switch output and ground.

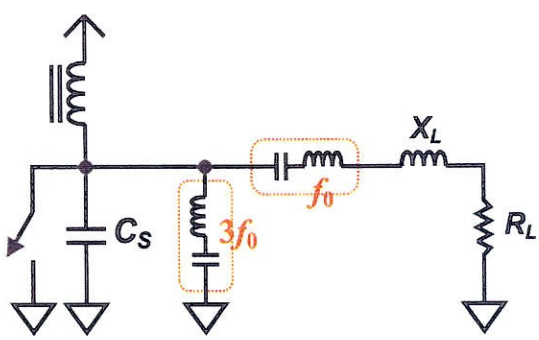


Figure 6.7: Direct E/F_3 implementation using high-Q resonators.

Tuning of even harmonics requires that the capacitor be resonated out at that harmonic, so the filter would not connect to ground, but to an appropriately sized inductor, as shown in Fig. 6.8. Although this tuning inductor L_2 is depicted as a discrete circuit element in the schematic, it would almost certainly be combined with the inductor of the second-harmonic LC tank, reducing the component count.

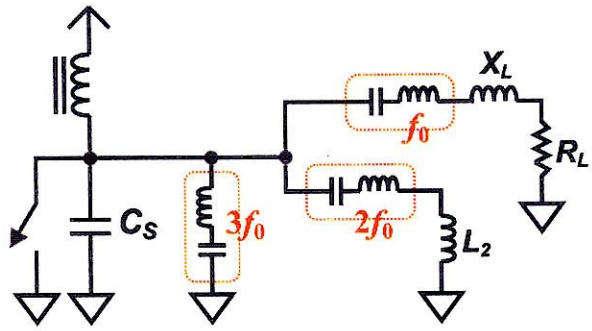


Figure 6.8: Direct E/$F_{2,3}$ implementation using high-Q resonators.

6.5.2 Multi-Resonant Implementations

The direct implementation, although simple, has its disadvantages. First, the circuit complexity is unnecessarily complicated. Rather than employing separate resonators for each harmonic, a suitable multi-resonant circuit might be employed to reduce the number of components. For instance, a simple E/$F_{2,3}$ implementation might employ a single series/parallel resonator to simultaneously tune the second and third harmonics using only three circuit elements. This circuit, shown in Fig. 6.9, has the additional advantage of using a resonator which conducts dc current, allowing it to also replace the rf choke.

6.5.3 Symmetric Push/Pull Implementations

The second problem is the difficulty of tuning harmonics in a way that is both reasonably simple and low-loss. Because each additional resonance added to the circuit introduces additional loss, it is desirable to reduce the stored energy in the resonators, i.e. make their loaded quality factors (Qs) relatively low. Unfortunately, this causes the effect

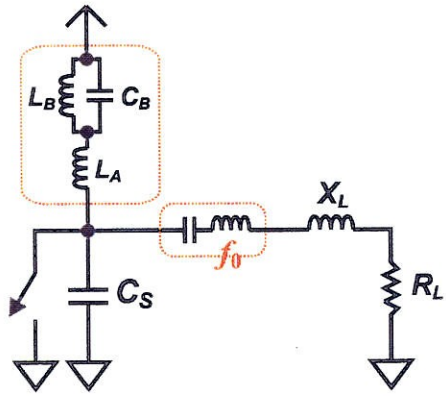


Figure 6.9: Class E/$F_{2,3}$ implementation using a multi-resonant tuning circuit.

of the tuning circuit to be relatively broad in the frequency domain, spilling over into adjacent harmonics, usually with adverse effects. For instance, if a low-Q third-harmonic LC resonator is employed in the circuit of Fig. 6.7, the resonator will present a capacitance at the second harmonic, reducing the impedance at this harmonic where it would actually serve better to increase it. This causes all three waveform figures of merit to degrade, particularly F_C. The designer is thus forced to either utilize a very high-Q resonant circuit or to introduce additional resonances into the circuit, either way increasing the passive component loss.

There is, however, a more clever way to short-circuit an odd harmonic without adversely affecting the impedances of the adjacent even harmonics. By utilizing a push/pull circuit of two identically-tuned switching amplifiers [62], the differing symmetries of the even and odd harmonics in the switching waveforms may be employed.

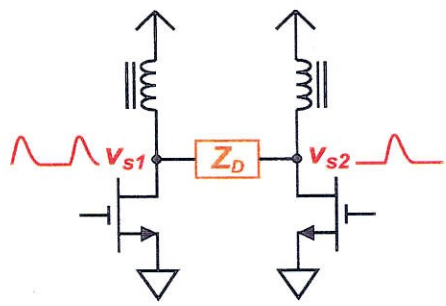


Figure 6.10: Push/pull switching amplifier with differential load.

Consider, for instance, the circuit depicted in Fig. 6.10. This circuit employs two switches, each with 50% switching duty cycle but operated in a complementary fashion so that when one switch is conducting the other is open. As the circuit is constructed symmetrically, it is reasonable to assume that the waveforms of each switch are identical except for a time delay difference of a half cycle between them. Consider now, what effect the differential load impedance Z_D has on the effective impedance seen by each switch at the various harmonic frequencies.

Due to the time-delay symmetry of the waveforms, the odd harmonic voltage components of each switch must be equal in amplitude but opposite in phase. Consequentially, a virtual ground develops at the center of the differential impedance and each switch "sees" an impedance at this frequency equal to $Z_D/2$. At the even harmonics, however, the harmonic voltage components must be equal in amplitude and equal in phase. As a result, a virtual open-circuit develops at the line of symmetry and no current flows through the impedance Z_D. Thus the effective impedance seen by each switch at even harmonic frequencies is unaffected by the presence of this differential load. These effects are depicted in Fig. 6.11.

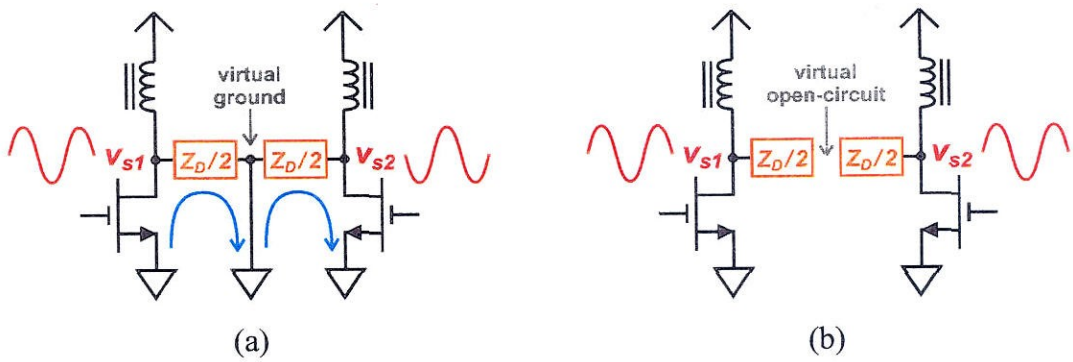


Figure 6.11: Effect of differential load at odd harmonics (a) and even harmonics (b).

Utilizing this principle, a clever designer might construct his E/F_3 amplifier in a manner similar to that shown in Fig. 6.12. By placing the third harmonic short circuit as a

differential load, this harmonic may be properly terminated using a low-Q resonator without adversely affecting the impedances of any even harmonic.

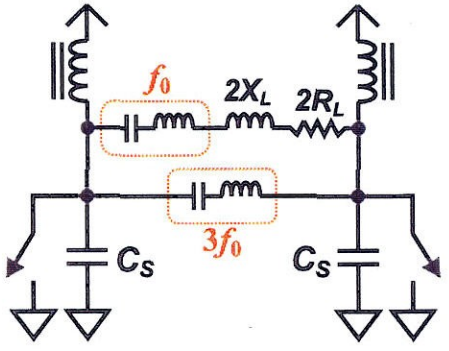


Figure 6.12: Class E/F_3 push/pull implementation allowing the use of low-Q resonators.

A similar strategy may be used to selectively tune the impedances of even harmonics. Consider, for example the circuit shown in Fig. 6.13. In this case, the differential load has been augmented with a common mode conductance Y_C placed between the center of the differential load and ground. Consider now what effect this circuit has for both even and odd harmonics.

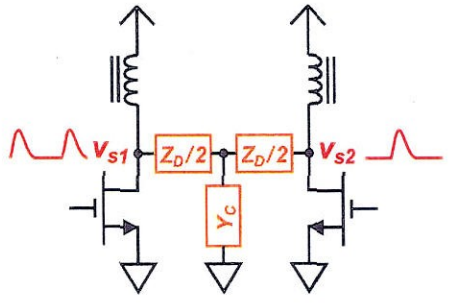


Figure 6.13: Push/pull switching amplifier with T network load.

As before, a virtual ground develops for odd harmonic frequencies at the symmetry line of the circuit, effectively shorting the conductance Y_C at these frequencies. Thus the common mode conductance has no effect for the odd harmonic, resulting in the same effective impedance as in the previous, fully-differential case. At the even harmonics, however, the symmetry line represents a virtual open circuit, and any current injected into

the T network must be conducted through the conductance Y_C. By separating this conductance into two parallel conductances each of value $Y_C/2$, the effective impedance at the even harmonics is easily found to be $(Z_C/2)+(2/Y_C)$. By choosing the common mode conductance appropriately, even harmonics may thus be tuned without affecting the impedances of odd harmonics. These effects are depicted in

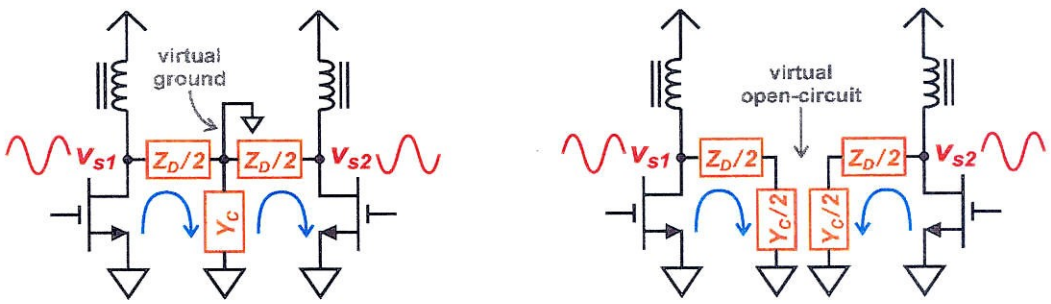


Figure 6.14: Effect of differential load at odd harmonics (a) and even harmonics (b).

Utilizing this technique, an $E/F_{2,3}$ amplifier might be constructed using the circuit topology shown in Fig. 6.15. In this circuit, the third harmonic is short-circuited using a differential load as before. The second harmonic is tuned to open circuited using the T network consisting of the L_1 and L_2, which also serves to supply the required fundamental frequency inductance through the L_1 components. As in the multi-resonant case, the circuit also allows the chokes to be replaced by passing the dc current through the tuning inductors.

6.6 Class F/E ZCS Amplifiers

Like any other tuning, the E/F family members each have dual tunings wherein the voltage and current waveforms are interchanged. In this case, the dual may be referred to as the F/E family, since these tunings are a hybrid between class F and class E^{-1} in every sense that E/F is a hybrid between class E and class F^{-1}. This family consists of ZCS amplifiers, and as such are of limited use in high-frequency design. Nevertheless, in

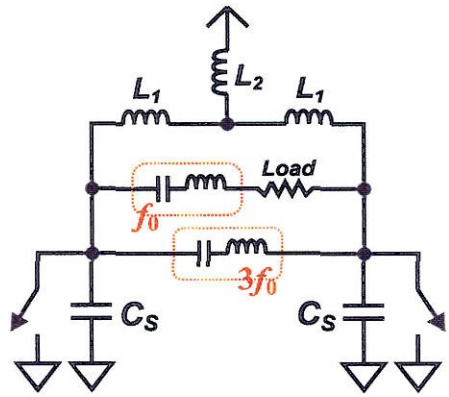


Figure 6.15: Class $E/F_{2,3}$ push/pull implementation allowing the use of low-Q resonators. L_1 provides the fundamental frequency inductance, while L_2 provides the second harmonic tuning.

applications where class E^{-1} would normally be employed, amplifiers from this F/E family may offer performance advantages similar to those E/F offers for applications demanding ZVS switching.

6.7 Updated Switching Amplifier Taxonomy

One of the results of the explorations detailed in this chapter has been to greatly expand the number of known tunings. As a result, the taxonomy of harmonic-tuned switching amplifiers may now be augmented with these new tunings, as depicted in Fig. 6.16.

As can be seen, the E/F and F/E families form subsets of the ZVS and ZCS amplifier groups respectively. Since all of the ZVS tunings presented so far are now members of the E/F subset, it might be inquired whether there are ZVS tunings which are *not* in the E/F family or whether the E/F family is the only method to achieve ZVS. In fact, there are many such tunings, although most have poor waveforms and/or exhibit poor capacitance tolerance. In fact, this author has never encountered a tuning of the overtones for which it is mathematically impossible to achieve ZVS conditions by appropriately adjusting the fundamental frequency load. Amongst these tunings, the class E/F family seem to be

among the best performing, but additional exploration may yield other tunings with yet greater performance advantages.

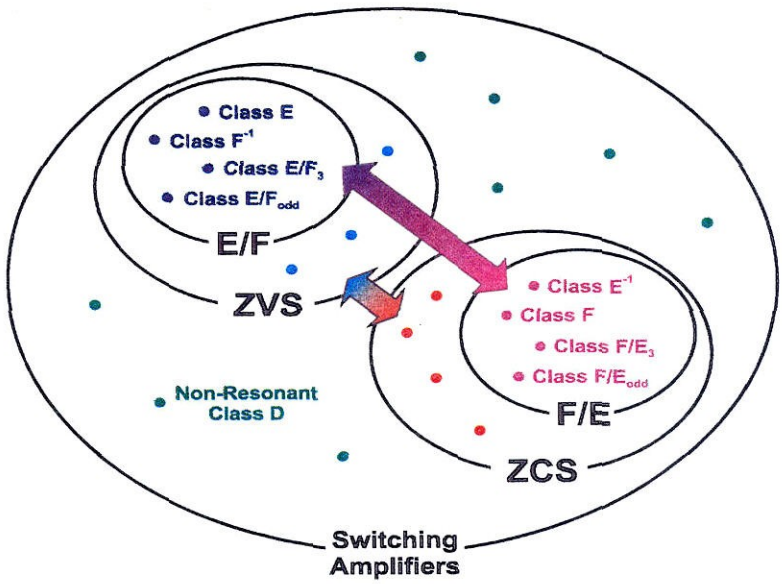


Figure 6.16: New switching amplifier taxonomy, including the new E/F and F/E families.

Also, it should be noted that there are a great many tunings which are not either ZVS or ZCS. This is hardly surprising, since any passive circuit connected to a switch will produce *some* waveform, and it is hardly to be expected that an arbitrarily constructed circuit will operate with ZVS or ZCS switching. Due to their inability to reduce the effect of switch parasitics, these tunings are of little interest for high-frequency power amplifier design.

Chapter 7

The E/F$_{odd}$ Switching Amplifier Family

In the previous chapter, a push/pull implementation strategy was developed for efficient implementation of E/F amplifiers by utilizing the differing symmetries of the even and odd harmonics. Besides allowing improved implementations over single-ended E/F family, this technique also presents the very interesting possibility of utilizing these symmetries to achieve tunings which are impossible in single-ended designs. This chapter details one such technique, wherein E/F amplifiers with an infinite number of tuned harmonics are achieved using a simple push/pull implementation.

7.1 Class E/F$_{odd}$ Amplifiers

7.1.1 E/F$_{odd}$ Concept

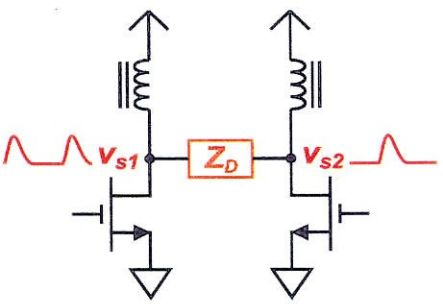


Figure 7.1: Push/pull switching amplifier with differential load.

Consider the differentially-loaded push/pull amplifier circuit, as depicted in Fig. 7.1. As noted previously in Section 6.5.3, the differential load Z_D only has effect on the odd harmonics, being effectively removed from the circuit at the even harmonics by the virtual open-circuit developed at the line of symmetry for those frequencies. Since the desired tuning for odd harmonics is short-circuit, it is intriguing to consider the possibility of

short-circuiting large numbers of harmonics using a single differential load. For instance, if the differential load Z_D is a wideband filter constructed to provide a short-circuit between the switches for all harmonics between the 3rd and the 7th, an E/F$_{3,5,7}$ amplifier would result. At the 3rd, 5th, and 7th harmonics, the switches will each see an effective impedance of short-circuit, since the differential load short-circuits each switch to the virtual ground at the circuit's line of symmetry[1]. The even harmonics, however, will not be affected by the short circuit between the switches at the 4th and 6th harmonics since their voltages at these harmonics are already identical to each other.

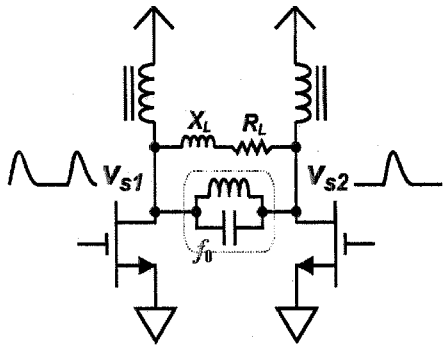


Figure 7.2: Class E/F$_{odd}$ circuit implementation using a parallel LC resonator.

The extreme case of this would be to short-circuit *all* of the odd harmonics by simply using a true short-circuit as the differential load. Such a circuit could in principle achieve E/F tuning for an infinite number of odd harmonics with almost zero circuit complexity. It would, of course, also short-circuit the fundamental frequency, rendering the resulting "amplifier" useless. This may be remedied by using circuit such as that shown in Fig. 7.2, wherein a bandstop filter such as a parallel LC tank is used to short the two switches together at all frequencies *other than the fundamental.* This technique would have the potential to yield an E/F$_{3,5,7,9,...}$ amplifier, denoted hereafter as E/F$_{odd}$ so as to indicate the tuning of all odd harmonics.

1. Or, equivalently, the voltages must be equal amplitude and opposite phase. Since they're short-circuited together the only possibility is that each amplitude is zero, i.e. a virtual short-circuit.

7.1.2 E/F$_{odd}$ Waveform Solution Technique

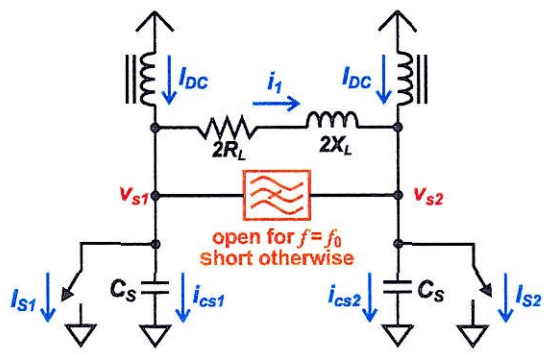


Figure 7.3: Class E/F$_{odd}$ circuit model for analysis.

Unlike the class E/F amplifiers with finite numbers of harmonics tuned explored in Chapter 6, the waveforms for the E/F$_{odd}$ tuning are derived with relative ease in the time domain. Consider the E/F$_{odd}$ amplifier depicted in Fig. 7.3. Due to the presence of the bandstop filter between the two switches, the differential voltage $v_{s1} - v_{s2}$ between the two switches must be a fundamental frequency sinusoid. Letting the amplitude and phase of the sinusoid be denoted V_S and ϕ respectively:

$$v_2 - v_1 = V_S \sin(\theta + \phi) \tag{7.1}$$

Since the switches are each conducting for alternating halves of the cycle, this differential voltage determines the switch voltages v_{s1} and v_{s2} since at all times at least one of them is zero. Without loss of generality, it may be assumed that the left-most switch is closed for $0 < \theta < \pi$:

$$v_{s1} = \begin{cases} 0 & 0 < \theta < \pi \\ -V_S \sin(\theta + \phi) & \pi < \theta < 2\pi \end{cases} \tag{7.2}$$

$$v_{s2} = \begin{cases} V_S \sin(\theta + \phi) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.3}$$

Assuming a ZVS tuning is to be found, these voltage waveforms must be continuous and zero at the switching turn-on times, which can only be accomplished if either V_S or ϕ

is zero. Since $V_S = 0$ results in an all-zero solution, it must be concluded that ϕ is zero. This results in a half-sinusoidal voltage, the limiting case for class F^{-1}, which is reasonable since the half-sinusoidal waveform is well-known to have only fundamental frequency and even harmonic components:

$$v_{s1} = \begin{cases} 0 & 0 < \theta < \pi \\ -V_S \sin(\theta) & \pi < \theta < 2\pi \end{cases} \tag{7.4}$$

$$v_{s2} = \begin{cases} V_S \sin(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.5}$$

Since each switch is connected to the dc supply through an inductor, the dc value of the switch voltage waveforms must each be the dc voltage V_{DC}. Since the peak to average ratio of a half-sinusoid is equal to π, the voltage waveforms must be:

$$v_{s1} = \begin{cases} 0 & 0 < \theta < \pi \\ -\pi V_{DC} \sin(\theta) & \pi < \theta < 2\pi \end{cases} \tag{7.6}$$

$$v_{s2} = \begin{cases} \pi V_{DC} \sin(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.7}$$

Now that the voltages across the capacitances C_{s1} and C_{s2}, each with capacitance C_s, are known, their currents I_{cs1} and I_{cs2} may be calculated[1]:

$$i_{cs1} = \begin{cases} 0 & 0 < \theta < \pi \\ -\pi \omega_0 C_s V_{DC} \cos(\theta) & \pi < \theta < 2\pi \end{cases} \tag{7.8}$$

1. Although a linear output capacitance is assumed here, it should be noted that the case of a non-linear capacitance [55] is readily solved [56] so long as the current resulting from the known voltage waveform may be calculated.

$$i_{cs2} = \begin{cases} \pi\omega_0 C_s V_{DC}\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.9}$$

The frequency dependence may be removed by expressing the currents in terms of the capacitances' fundamental frequency impedance magnitude Z_C:

$$i_{cs1} = \begin{cases} 0 & 0 < \theta < \pi \\ -\dfrac{\pi V_{DC}}{Z_C}\cos(\theta) & \pi < \theta < 2\pi \end{cases} \tag{7.10}$$

$$i_{cs2} = \begin{cases} \dfrac{\pi V_{DC}}{Z_C}\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.11}$$

With these currents known, the switch currents may be calculated using Kirchhoff's current law (KCL). Since at least one switch is non-conducting (i.e. zero current) at all times, and since the chokes only conduct dc current I_{DC}, all currents except for that of the conducting switch are known. Clearly this switch must conduct both choke currents as well as that of the capacitor parallel to the non-conducting switch:

$$i_{s1} = \begin{cases} 2I_{DC} - \dfrac{\pi V_{DC}}{Z_C}\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.12}$$

$$i_{s2} = \begin{cases} 0 & 0 < \theta < \pi \\ 2I_{DC} + \dfrac{\pi V_{DC}}{Z_C}\cos(\theta) & \pi < \theta < 2\pi \end{cases} \tag{7.13}$$

With the voltage and current waveforms determined, the only remaining task is to determine the value of the fundamental frequency load. The load current i_1 is readily calculated using KCL:

$$i_1 = \begin{cases} -I_{DC} + \dfrac{\pi V_{DC}}{Z_C}\cos(\theta) & 0 < \theta < \pi \\ I_{DC} + \dfrac{\pi V_{DC}}{Z_C}\cos(\theta) & \pi < \theta < 2\pi \end{cases} \tag{7.14}$$

This is actually the sum of a square wave and a cosine:

$$i_1 = \frac{\pi V_{DC}}{Z_C}\cos(\theta) + \begin{cases} -I_{DC} & 0 < \theta < \pi \\ I_{DC} & \pi < \theta < 2\pi \end{cases} \tag{7.15}$$

The fundamental frequency Fourier component of the differential current follows by inspection. Noting that the ratio between the fundamental frequency component and amplitude of a square waveform is $4/\pi$, the fundamental frequency load current I_1 is:

$$I_1 = \frac{\pi V_{DC}}{Z_C} + j \cdot \frac{4I_{DC}}{\pi} \tag{7.16}$$

The load voltage $v_{s1} - v_{s2}$ is a sine wave with amplitude πV_{DC}, and so the differential fundamental frequency load voltage V_1 is:

$$V_1 = j\pi V_{DC} \tag{7.17}$$

The admittance of the fundamental frequency load is simply the ratio of I_1 and V_1:

$$\begin{aligned} Y_1 = \frac{I_1}{V_1} &= \frac{4I_{DC}}{\pi^2 V_{DC}} - j \cdot \frac{1}{Z_C} \\ &= \frac{1}{R_L} - j \cdot \frac{1}{Z_C} \end{aligned} \tag{7.18}$$

where:

$$R_L \equiv \frac{\pi^2}{4} \cdot \frac{V_{DC}}{I_{DC}} \tag{7.19}$$

From this expression, it is apparent that the required fundamental frequency differential load is a resistance in parallel with an inductance having the same impedance at the fundamental frequency as the capacitance C_S does. Equivalently, the inductance must be sized to resonate at the fundamental frequency with the capacitance of one switch.

Equation (7.18) also leads to an interesting conclusion: The formula for the load conductance does not contain any dependence on the capacitor C_s while the load susceptance is a function only of this capacitance. Thus the amplifier will operate in ZVS mode for *any* value of the load conductance without the need to re-tune as the conductance is changed. Furthermore, the voltage waveform across the load is constant under these changes in conductance since it is determined only by the dc voltage and the switching phase. The current waveforms do change, however. Expressing (7.12) in terms of the load resistance and the dc voltage yields:

$$i_{s1} = V_{DC} \cdot \begin{cases} \frac{\pi^2}{2R_L} - \frac{\pi}{Z_C}\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.20}$$

This expression indicates that, if the load resistance is varied while the switch capacitance and tuning network are unchanged, the square wave component of the current waveform varies with the changing load while the half-cosine component remains unchanged, being only a function of the switch capacitance. This effect on the switching waveforms is depicted in Fig. 7.4.

This load invariance may be useful in many applications, but even for systems utilizing a fixed load the ability to vary the capacitance and load independently is important. The loose relationship between the load resistance and the capacitance C_s may be utilized to allow a change in the switch output capacitance without necessitating a change in the load resistance. Re-arranging (7.20) results in:

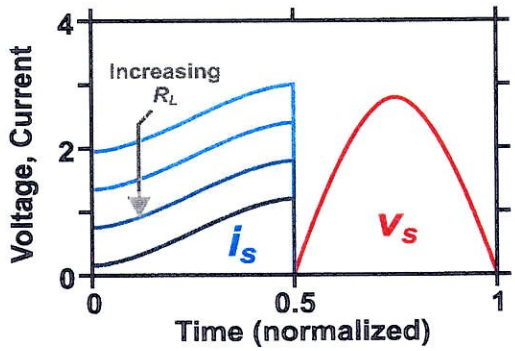


Figure 7.4: Behavior of the E/F$_{odd}$ switching waveforms as the load is varied.

$$i_{s1} = \frac{\pi^2 V_{DC}}{4R_L} \cdot \begin{cases} 2 - \dfrac{4R_L}{\pi Z_C}\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.21}$$

This expression indicates that the shape of the current waveform is determined by the ratio between the load resistance and the switch output capacitance. For very small capacitance, the current is a square waveform, as should be expected since for negligible output capacitance the circuit is identical to class D^{-1} as discussed in Chapter 3. As the capacitance is increased, however, the half-cosine waveform begins to increase in amplitude. This effect is depicted in Fig. 7.5.

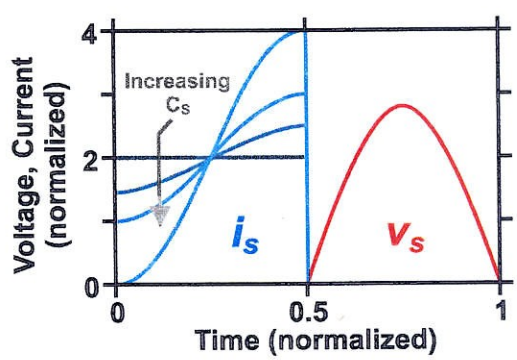


Figure 7.5: Class E/F$_{odd}$ waveforms as output capacitance is varied.

There are several results to conclude from this. First, it is clear that the RMS current increases as the capacitance is increased. Thus a designer, if given the option of reducing

the output capacitance without adversely affecting the on-resistance, would be foolish to not do so. Thus, unlike class E and single-ended E/F amplifiers wherein choosing too small of a value for C_s results in negative switch voltages - especially undesirable in FET devices with parasitic drain-bulk diodes - the E/F_{odd} circuit waveforms only improve as the capacitance is decreased. As a result, unlike the class E case wherein discrete capacitance is often added in parallel to the switch, it would be inadvisable to do so in the E/F_{odd} case.

This is not to say that the capacitance will necessarily be small, however. Although the current waveforms improve with decreased capacitance, low on-resistance may often demand a large transistor size, as discussed, in Chapter 4. The freedom to freely choose a range of values for the output capacitance – in essence a range of different tunings – without introducing negative switch voltage or current gives the designer an additional degree of freedom when optimizing performance. The tuning for each output capacitance will have different values of F_I and F_C, and accordingly will have different performances.

The current waveform shape can actually be expressed in terms of the capacitance tolerance parameter F_C. Rearranging (7.12) results in:

$$i_{s1} = I_{DC} \cdot \begin{cases} 2 - \pi \cdot \dfrac{V_{DC}}{I_{DC} Z_C} \cos\theta & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.22}$$

Recalling the definition[1] of FC from Chapter 4, this can be re-expressed as:

$$i_{s1} = I_{DC} \cdot \begin{cases} 2 - \dfrac{\pi}{F_C} \cos\theta & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.23}$$

1. The waveform figures of merit, in order to be used consistently, should be calculated on a per-switch basis, and so the dc voltage, dc current, peak voltage, output capacitance, etc. should be the appropriate value for a single switch. The analysis in this section has been set up so that, for instance, I_{DC} is the dc current for a single switch, simplifying the analysis.

$$F_C \equiv \frac{V_{DC} I_{DC}}{V_{DC}^2 / Z_C} \tag{7.24}$$

As can be seen, there is a one-to-one correspondence between the F_C value and the waveform shape. As a result, it is convenient to label the tunings for difference relative capacitor sizes according to their F_C value relative to that of class E (for which $F_C = \pi$). Accordingly, an "E" sized tuning has $F_C = \pi$ while a "2E" sized tuning would have $F_C = \pi/2$, etc. From (7.23) it is apparent that using a "2E" sized device results in a current waveform beginning from a zero value. In fact, the "2E" device is the largest for which there are no negative currents. So in this crude sense, E/F$_{odd}$ has twice the capacitance tolerance of E, being capable of absorbing twice the capacitance before negative currents result. The E/F$_{odd}$ waveforms corresponding to "E" sized and "2E" sized devices are depicted in Fig. 7.6.

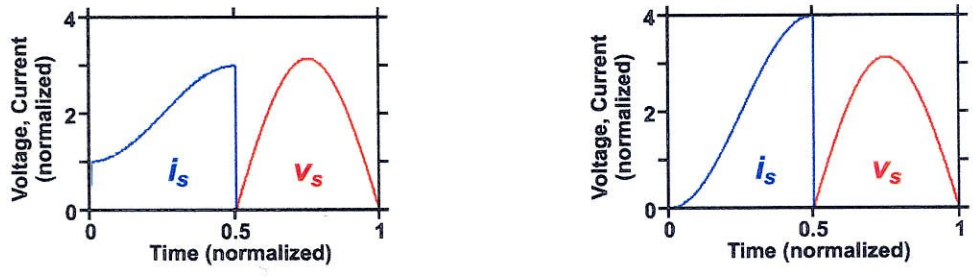


Figure 7.6: Class E/F$_{odd}$ tunings for "E" (a) and for "2E" sized (b) devices.

7.2 Class E/F$_{odd}$ Family

Having determined that it is possible to provide short circuits for all odd harmonics to produce E/F$_{odd}$, it is natural to wonder whether additional even harmonics may be tuned to increase the performance. Thus, it is desired to evaluate the operation of an E/F$_{x,odd}$ amplifier tuning, where x is a list of additional tuned even harmonics. In this way, the E/F$_{odd}$ concept may be generalized to produce an E/F$_{odd}$ family of tunings.

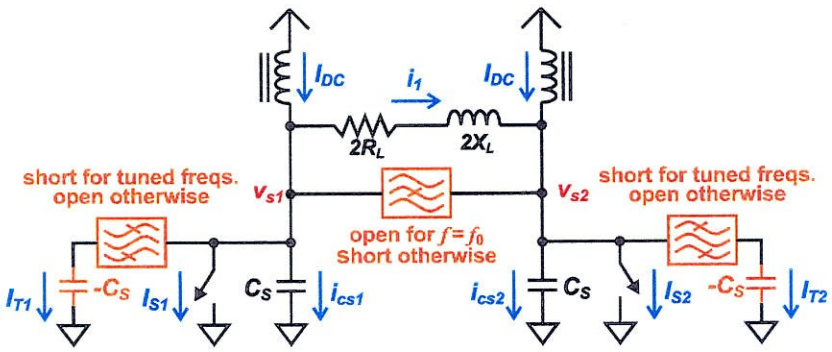


Figure 7.7: E/F$_{x,odd}$ conceptual circuit implementation.

A circuit implementation by which a number of even harmonics may in principle be open-circuited is shown in Fig. 7.7, wherein the E/F$_{odd}$ circuit of Fig. 7.3 has been augmented with additional resonators in parallel with each switch. Each resonator may be treated analytically as a bandpass filter in series with a capacitor having a negative capacitance $-C_S$. The filter connects this negative capacitance in parallel with the switch parallel capacitance at those even harmonics to be tuned, canceling this capacitance at these frequencies. For each even harmonic thusly tuned, the switch will be presented an open-circuit.

As before, the switching waveforms are readily calculated using a time-domain approach. The voltage waveforms for this circuit are identical to those for the class E/F$_{odd}$ amplifier (7.6)-(7.7) found previously, following from the same arguments. The capacitor currents i_{cs1} and i_{cs2} are therefore also identical to the E/F$_{odd}$ case (7.8)-(7.9). The resonator currents i_{T1} and i_{T2} may be calculated easily as the resonator impedance and the voltage across it are both known. To this end, the switch voltage waveforms may be decomposed into the following Fourier series:

$$v_{s1} = V_{DC} \cdot \left[1 - \frac{\pi}{2}\sin(\theta) - \sum_{k \in \{2,4,6,\ldots\}} \left(\frac{2}{k^2 - 1}\cos(k\theta) \right) \right] \tag{7.25}$$

$$v_{s1} = V_{DC} \cdot \left[1 + \frac{\pi}{2} \sin(\theta) - \sum_{k \in \{2, 4, 6, \ldots\}} \left(\frac{2}{k^2 - 1} \cos(k\theta) \right) \right] \tag{7.26}$$

The admittance $Y_T(k)$ of the tuning network at the k^{th} harmonic is:

$$Y_T(k) = -j \cdot \frac{k}{Z_C} \tag{7.27}$$

Using this, along with (7.25)-(7.26), the even-harmonic tuning network currents i_{T1} and i_{T2} may be calculated. Letting T denote the set of even harmonics to be tuned:

$$i_{T1} = i_{T2} = -\frac{V_{DC}}{Z_C} \cdot \sum_{k \in T} \left[\frac{2k}{k^2 - 1} \sin(k\theta) \right] \tag{7.28}$$

To find the switching current waveforms, KCL is invoked. As before, this is possible since at any given time every current is known except for the conducting switch:

$$i_{s1} = \begin{cases} 2I_{DC} - \frac{\pi V_{DC}}{Z_C} \cos(\theta) + \frac{V_{DC}}{Z_C} \cdot \sum_{k \in T} \left[\frac{2k}{k^2 - 1} \sin(k\theta) \right] & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{7.29}$$

$$i_{s2} = \begin{cases} 0 & 0 < \theta < \pi \\ 2I_{DC} + \frac{\pi V_{DC}}{Z_C} \cos(\theta) + \frac{V_{DC}}{Z_C} \cdot \sum_{k \in T} \left[\frac{2k}{k^2 - 1} \sin(k\theta) \right] & \pi < \theta < 2\pi \end{cases} \tag{7.30}$$

Now the fundamental frequency load may be determined. Current through the differential load, i_1, is found by KCL:

$$i_1 = \begin{cases} -I_{DC} + \frac{\pi V_{DC}}{Z_C} \cos(\theta) + \frac{V_{DC}}{Z_C} \cdot \sum_{k \in T} \left[\frac{2k}{k^2 - 1} \sin(k\theta) \right] & 0 < \theta < \pi \\ I_{DC} + \frac{\pi V_{DC}}{Z_C} \cos(\theta) - \frac{V_{DC}}{Z_C} \cdot \sum_{k \in T} \left[\frac{2k}{k^2 - 1} \sin(k\theta) \right] & \pi < \theta < 2\pi \end{cases} \tag{7.31}$$

The fundamental frequency Fourier component I_1 of this current may now be found:

$$I_1 = \frac{\pi V_{DC}}{Z_C} - \frac{V_{DC}}{\pi Z_C} \cdot \sum_{k \in T} \left[\frac{8k^2}{(k^2-1)^2} \right] + j\frac{4I_{DC}}{\pi} \tag{7.32}$$

To determine the load conductance, the ratio of this current to the fundamental frequency voltage (7.17) is taken:

$$Y_1 = \frac{4I_{DC}}{\pi^2 V_{DC}} - j \cdot \left(\frac{1}{Z_C}\right) \left[1 - \frac{1}{\pi^2} \cdot \sum_{k \in T} \left(\frac{8k^2}{(k^2-1)^2} \right) \right] \tag{7.33}$$

As in the case of E/F_{odd}, the required fundamental frequency load for the $E/F_{x,odd}$ amplifier is a resistance in parallel with an inductive susceptance. Also like E/F_{odd}, it can be seen that the impedance of this susceptance is a function only of the output capacitance C_S, and the harmonics which have been tuned, and not a function of the output power or the load resistance. As a result, these amplifiers show the same load-invariance as E/F_{odd}. As in the E/F_{odd} case, the square wave component of the current scales with the load resistance R_L while the "ripple" current scales with the output capacitance C_S. Unlike Class E/F_{odd}, the shape of this "ripple" current is no longer half-cosinusoidal, but is more complex.

7.2.1 Class E/F_{odd} Family Waveforms

Using (7.29) and (7.6), the waveforms for class E/F_{odd} amplifiers may be generated. Since there is a choice of the transistor size to use, three sizes have been selected, "E" to indicate performance when a class-E sized device is used, "2E" to indicate performance for the maximum sized device not resulting in negative currents, and "0.5E" to indicate performance for a small device. Selected waveforms are depicted in Fig. 7.8.

As can be seen, much like in the single-ended class E/F amplifiers, the effect of open-circuiting even harmonics is to cause the current waveform to more closely approximate a square wave. While for small values of capacitance, the simple E/F_{odd}

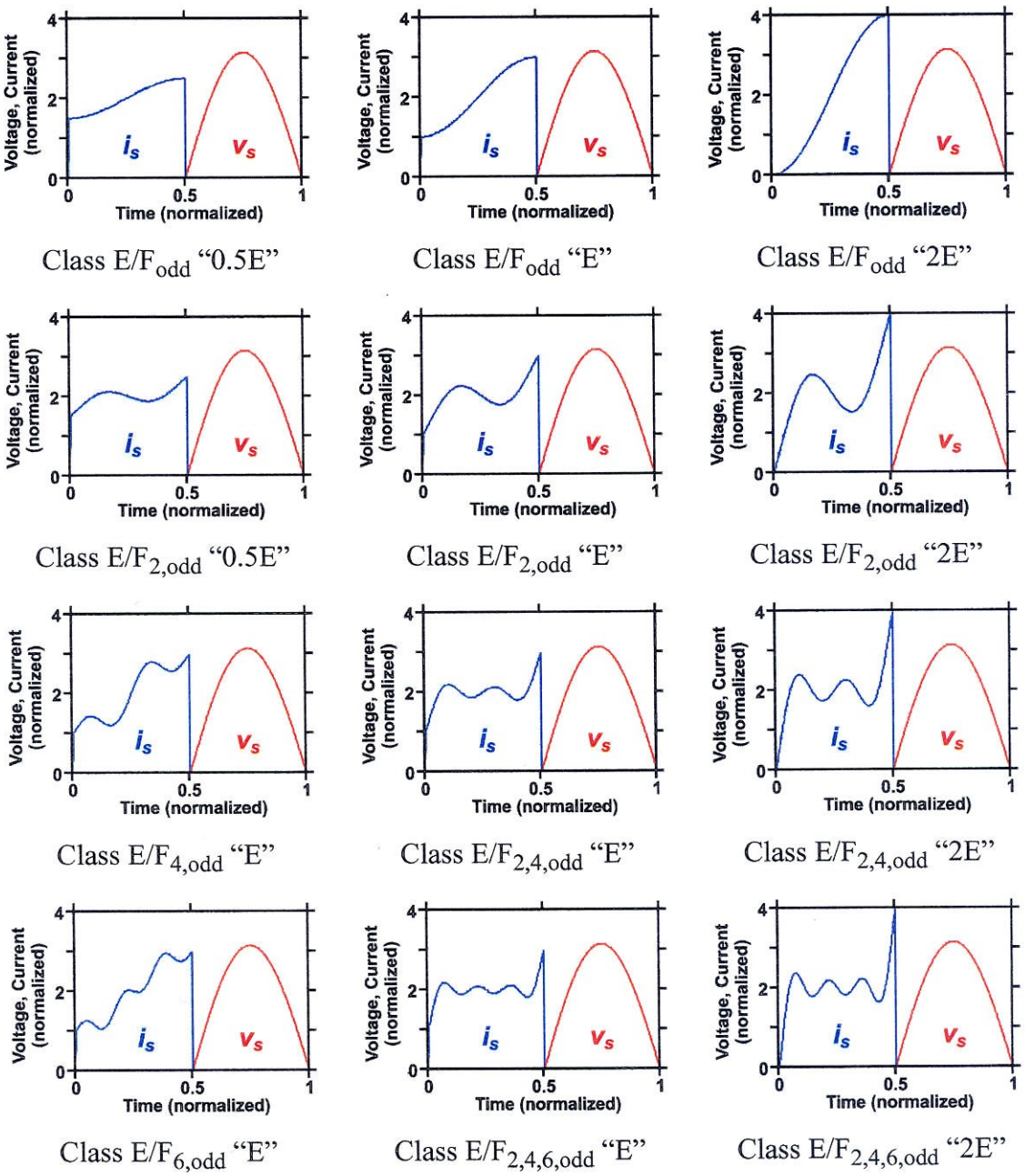


Figure 7.8: Switching waveforms for some members of the E/F_{odd} ZVS switching amplifier family. Each amplifier is tuned for ZVS switching conditions. Waveforms are normalized to unity dc voltage and current.

circuit is sufficient to achieve a nearly square-wave current, for larger sized devices the additional harmonic tuning presents a clear advantage. In this way, the even harmonic tuning is helpful for achieving even larger transistor sizes while keeping reasonable RMS

currents. Also of note is that tuning of individual harmonics such as the 4th or 6th, while not hurting the performance, fails to yield significant improvements. The most effective harmonic to tune is the second, followed by the fourth, etc.

7.2.2 Class E/F_{odd} Performance Figures of Merit

Waveform and performance figures of merit for selected E/F_{odd} amplifiers are presented in Table 7.1. The voltage waveform is in all cases equal to the half-sinusoid of the class F^{-1} limiting case, and the RMS currents in many cases are nearly ideal. As in the case of the single ended E/F amplifiers, the biggest improvement is in the capacitance tolerance factor F_C which may be reduced by a factor of two in all cases without introducing negative currents.

	Waveform Merit				Performance Merit (normalized to unity for Class E)				
Tuning	F_V	F_I	F_C	F_{PI}	$F_V^2F_I^2$	$F_I^2F_C$	F_V^2/F_C	$2F_VF_I$	F_VF_{PI}
E/F_{odd} "0.5E"	**3.14**	1.44	6.28	2.50	**0.68**	1.74	0.39	**0.82**	**0.77**
$E/F_{2,odd}$ "0.5E"	**3.14**	1.42	6.28	2.50	**0.66**	1.70	0.39	**0.81**	**0.77**
E/F_{odd} "E"	**3.14**	1.50	3.14	3.00	0.74	0.95	**0.78**	0.86	0.92
$E/F_{2,odd}$ "E"	**3.14**	1.44	3.14	3.00	0.68	0.87	**0.78**	**0.82**	0.92
$E/F_{2,4,odd}$ "E"	**3.14**	1.43	3.14	3.00	0.67	0.86	**0.78**	**0.82**	0.92
$E/F_{2,4,6,odd}$ "E"	**3.14**	1.42	3.14	3.00	0.67	0.86	**0.78**	**0.82**	0.92
$E/F_{4,odd}$ "E"	**3.14**	1.49	3.14	3.00	0.73	0.94	**0.78**	0.85	0.92
$E/F_{6,odd}$ "E"	**3.14**	1.50	3.14	3.00	0.74	0.95	**0.78**	0.86	0.92
E/F_{odd} "2E"	**3.14**	1.73	**1.57**	4.00	0.99	**0.63**	1.56	0.99	1.23
$E/F_{2,odd}$ "2E"	**3.14**	1.51	**1.57**	4.00	0.75	**0.48**	1.56	0.87	1.23
$E/F_{2,4,odd}$ "2E"	**3.14**	1.47	**1.57**	4.00	0.71	**0.46**	1.56	0.84	1.23
$E/F_{2,4,6,odd}$ "2E"	**3.14**	1.45	**1.57**	4.00	0.70	**0.45**	1.56	0.83	1.23
F^{-1}	3.14	1.41	N/A	2.00	0.66	N/A	N/A	0.81	0.62

Table 7.1: Waveform and performance figures of merit for several E/F_{odd} tunings. Performance figures listed relative to class E. In all cases, smaller numbers indicate better performance.

Efficiency and gain factors show corresponding improvements. As can be seen, E/F_{odd} tunings may excel in each performance category. Where transistor size is limited by cost, the low F_V and F_I values for small capacitance tunings allow E/F_{odd} to approach the performance of class F^{-1} utilizing a circuit with only one resonator. In the gain-limited case, the lower peak voltage and the reduced RMS current similarly benefit performance. As noted before, it is always inadvisable to add additional output capacitance when designing E/F_{odd} circuits, and so an E/F design should never truly be gain or size limited in the sense that single-ended E/F tunings will be. Thus, in the sense that the transistor output capacitance C_{out} will always be equal to the switch parallel capacitance C_S, even gain limited and size limited designs will be simultaneously capacitance limited. This presents an additional advantage of E/F_{odd} tunings in that by not insisting on the addition of extra capacitance in parallel to the switch in these situations, the waveforms may be improved.

The capacitance limited case also provides potential advantages. With the combination of double sized transistors and nearly ideal current waveforms, drain loss may be reduced in some cases to just half that of class E.

Chapter

8

New Opportunities and Applications

In order to highlight some of the potential advantages and new opportunities opened up both by the class E/F technique and the increased understanding of switching amplifiers afforded by the new analytic solution technique, this chapter details some of the applications where these techniques have already been employed. In addition, some promising application areas for future exploration are presented for which work has only just begun. For some of these application areas, new techniques and tunings simply offer improved performance, while others allow for design features not possible (or very difficult) to achieve with class E designs.

8.1 Improved Efficiency

The most obvious improvement, and the one which has been stressed in previous chapters is efficiency improvement. Thus, it is desired to simply replace a class E design with a better-performing alternative using the same transistor technology. In Chapters 6 and 7, data is presented from which the efficiency improvements might be calculated, but for the sake of illustration, a more concrete example is given here.

Suppose it is desired to replace an HF class-E design, which had previously been optimized to achieve 80% drain efficiency and 20dB of gain, resulting in a PAE of 79%. This amplifier is clearly capacitance limited, as the drain efficiency is overwhelmingly dominating the loss. Noting that several E/F amplifiers promise to perform much better than class E in this situation, a design study of several E/F amplifier tunings might be undertaken to calculate what advantage each has on maximum PAE.

Tuning	Gain	η_D	PAE
class E	20dB	80%	79%
class E/F_2	15dB	**93%**	**90%**
class E/F_3	21dB	81%	80%
class $E/F_{2,3}$	20dB	**87%**	**86%**
class E/F_{odd} "2E"	18dB	87%	86%
class $E/F_{2,odd}$ "2E"	18dB	**90%**	**89%**

Table 8.1: Relative optimized performances of class E/F power amplifiers at the same frequency.

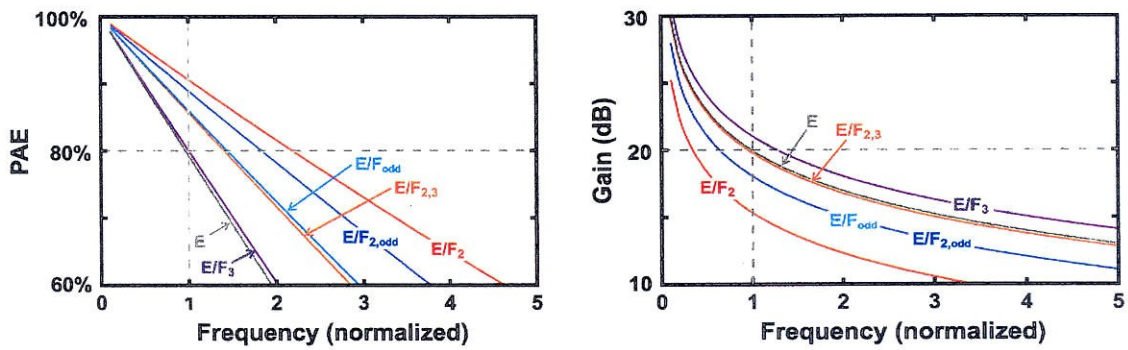
The results of such a study, calculated according to the techniques introduced in Chapter 4, are presented in Table 8.1. In order to minimize the additional design complexity, the table shows only those tunings which are achievable in relatively simple circuits. The first alternative, class E/F_2, shows the greatest improvement in PAE, but this is only at the cost of a 5dB decrease in the gain. In most cases, this would be acceptable. The E/F_3 amplifier does not show significant improvement. This tuning's primary advantage over E is its much lower peak voltage, which in the capacitance limited case shows up as a 1 dB increase in gain. Since the gain is already very high, the E/F_3 makes a poor choice for this application, since the performance improvements hardly justify the increased design complexity. Next, is $E/F_{2,3}$, which is an excellent choice as it presents a significant efficiency improvement with no gain reduction. The combination of a larger transistor size, a lower RMS current waveform, and a lower peak voltage combine to produce this result. Finally, the push/pull E/F_{odd} and $E/F_{2,odd}$ amplifiers each trade 2dB of gain for increased performance, but the much better current waveform of the $E/F_{2,odd}$ allows for almost as high of a PAE as the E/F_2 but with 3 dB more gain.

The advantage of the E/F tunings is clear in this case. By choosing $E/F_{2,odd}$ or E/F_2, the loss may be reduced to under half that of the class E amplifier to be replaced, at the price only of a reduction in the gain. Even in the case where the gain may not be

sacrificed, an $E/F_{2,3}$ (or a smaller sized $E/F_{2,odd}$) will allow the loss to be reduced by almost 40%.

8.2 Higher Frequency

In addition to being able to achieve higher performance at the same frequency, another advantage of higher-efficiency tunings is the ability to achieve similar performance while increasing the frequency of operation [21]. The achievable efficiency of a switching amplifier is a decreasing function of frequency, due to the decreasing gain and the need to reduce the transistor size due to the frequency-dependent impedance of the output capacitance[1] Changing to a tuning with higher efficiency at any given frequency will allow this frequency/efficiency trade-off to be utilized in order to achieve the same efficiency but at a higher frequency than the original tuning.



(a) (b)

Figure 8.1: Capacitance limited switching amplifier performance for the given device technology as a function of frequency.

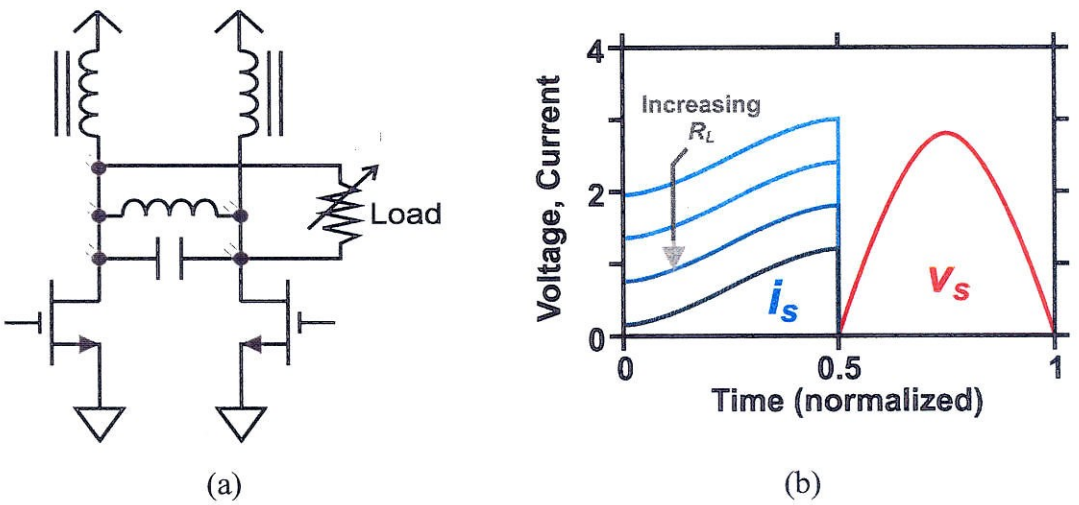
This effect is depicted in Fig. 8.1, wherein the optimized performance of the same tunings and transistor technology as the previous case are shown as a function of

1. As has been stressed in previous chapters, the tuning is a function of the *impedance magnitude*, Z_C, of the switch parallel capacitance. As the frequency increases, the transistor size in a capacitance limited case must be reduced to keep the same impedance relative to the other circuit elements.

frequency. In this calculation it is assumed that the input power to a fixed-sized switch has a square-law frequency dependence or, equivalently, 6dB reduction in gain per octave. As can be seen, the tunings for which the performance is the best at the original frequency (normalized to one on the plot), allow the frequency to be increased by a factor of two in some cases while achieving the same PAE performance as the original class E.

8.3 Load-Invariant ZVS Amplifiers/Inverters

One of the capabilities of the E/F_{odd} amplifier family which has already been touched on is the inherent load-invariant ZVS switching which may be achieved if the fundamental frequency load is designed so as to connect the load in parallel with the required ZVS tuning inductance. If this is done, the load may be changed to any value, in principle from open circuit to short-circuit, and the voltage waveforms across the transistors and across the load remain unchanged.



(a) (b)

Figure 8.2: Class E/F_{odd} amplifier with changing load: schematic (a) and waveforms (b)

Such a load-invariant switching amplifier is depicted in Fig. 8.2. The circuit is simply the basic E/F_{odd} topology wherein the load resistance is allowed to change. There has been some interest in load-invariant class E amplifiers [63,64], but unlike these techniques, the

basic circuit structure and operational characteristics such as the duty cycle need not be changed. Furthermore, the E/F_{odd} amplifier has a significant continuous range of load resistances for which neither negative voltage nor negative currents result, unlike class E load-invariant designs which have only a single such load resistance value. It should be noted, however, that like the load-invariant class-E case, this load invariance applies only to changes in the *resistance* of the load. If changes in load reactance are made, the tuning will depart from ZVS operating characteristics.

This technique, while not likely to find much application in amplifiers for communications applications, is useful for amplifiers (power inverters) used in resonant dc/dc power converters, wherein the load value is often unknown and/or changing as a function of time. By ensuring that the amplifier continues to operate in high-efficiency ZVS mode for the whole range of possible loads, the conversion efficiency may be sustained over a wide range of output currents.

8.4 Frequency Diversity

One application where the E/F_{odd} tuning's load invariance is particularly interesting is in the construction of power amplifiers for operation in several different frequency bands without the need for retuning. Such a capability might be useful for applications from high power frequency-agile industrial power generators to multi-band cellular handsets. Wide bandwidth amplifiers are required for applications such as chirped RADAR systems and may be commercially viable in VHF broadcast applications.

8.4.1 Dual- and Multi-Band ZVS Amplifiers

The concept of a dual- or multi-band amplifier is simple: construct an amplifier which may be driven at any of the design frequencies to produce output power at high efficiency without the need to change any circuit parameters. This is difficult to achieve in transitional class-E designs due to the tight relationship between the switch parallel

capacitance C_S and the load resistance R_L. In class-E designs, the impedances of these components must be in a fixed ratio in order to achieve the "optimal" ZVS/ZdVS switching conditions. Since the impedance of the capacitance varies inversely with the frequency, a multi-band class-E amplifier would require a load resistance which is similarly varying inversely with the frequency. If this is done, the class-E switching conditions may be preserved for each frequency in the band, but the different conductances at each frequency necessitate that the output power be linearly increasing with the frequency in each band. Thus, for instance, if an amplifier were designed to achieve class-E operation at 7MHZ and 14MHz, the output power in the 14MHz band would need to be twice that of the 7MHz band. While this may in principle be rectified by allowing non ZdVS tunings in some of the bands, the result will be that all but at most one of the bands would require negative currents and/or negative voltages in the switching waveforms.

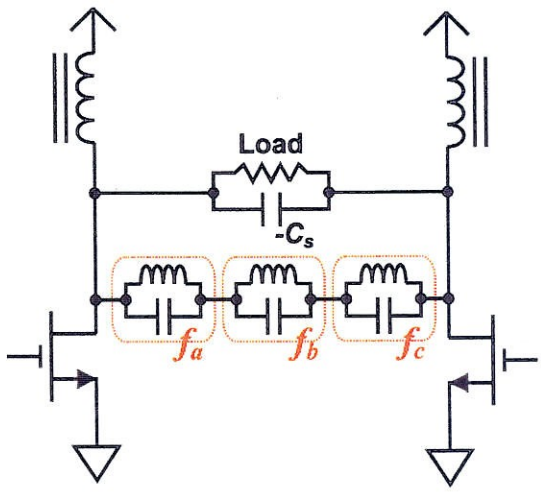


Figure 8.3: Tri-band class E/F_{odd} amplifier conceptual schematic.

Fortunately, the E/F_{odd} amplifier family provides an alternative solution. Since the output capacitance and the load resistance need not be in any particular ratio in these tunings, the load resistance may have any desired variation over frequency without having

significant effect on the circuit's voltage waveforms. If, for instance, the same power is desired in each band, the load resistance should be the same in each band.

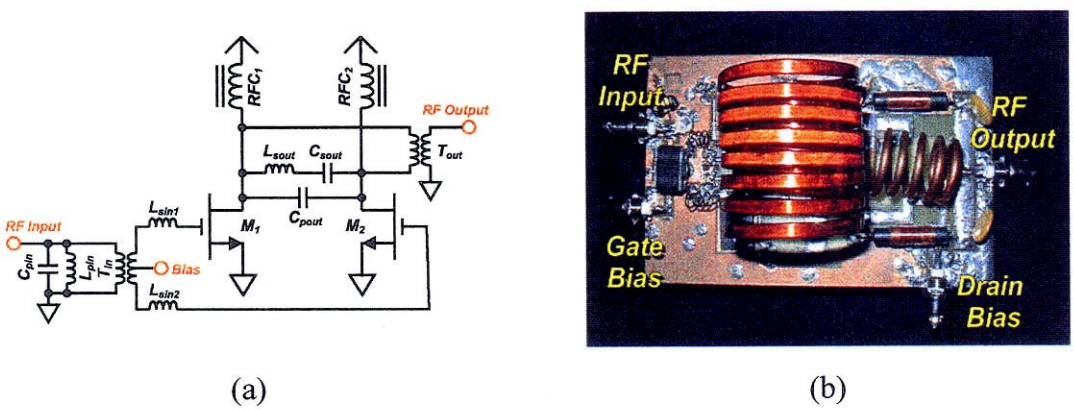
In order to achieve this ZVS tuning, however, the susceptance of the fundamental frequency load must be a function of the operational frequency. Since, for each member of the E/F_{odd} family, this susceptance is in a fixed ratio (7.33) with the output capacitance, the suscpetance must mimic a negative capacitance, having a value which is linearly increasing with the frequency in each band.

In this way, a tri-band amplifier with equal power in each band, for instance, may be achieved with the conceptual circuit shown in Fig. 8.3. Using three bandstop filters in the form of LC tanks, the drains of the two transistors are short-circuited together for all but the three operational frequencies, ensuring that the odd harmonic overtones of each band are terminated with short-circuits. The load is a fixed conductance in parallel with a capacitance having a value opposite that of the capacitance in parallel with each switch. Although this negative capacitance is not realizable due to causality violations, its effect is only expressed in the several fundamental frequency bands, and so its effect may be duplicated by an appropriate resonant circuit having the same impedance at those three frequencies.

The circuit has limitations, however. The bands used must be selected so that no band is an odd harmonic of another, and it is unlikely that simultaneous operation of more than one frequency band will result in satisfactory performance. The higher frequency bands, will have lower efficiency due both the transistor's lower gain as well as the increased amplitude of the "ripple" in the current waveforms. For the same reason, the F_C waveform figure of merit will be different for each band, and so the optimal device size for each band is different. As a result, the performance of a multi-band amplifier will necessarily be less than a similar single-band amplifier in all but one of the bands.

This concept has been successfully tested in a prototype [65,66] developed by Florian Bohn at Caltech, who had previously been working on dual-band class-E designs with

limited success. This amplifier, shown in Fig. 8.4, was developed for operation in the 7MHz and 10MHz HAM bands, using commercially available vertical MOSFETs The input and output employ dual-resonant circuits to match the input and provide the correct ZVS tuning in each band. Instead of using the arrangement of two parallel LC tanks in series as shown in the Fig. 8.3, an alternative equivalent design has been chosen, primarily so that the magnetizing inductance of the output transformer T_{out} may be utilized as an element in the resonant circuit. The prototype is constructed on FR4 printed circuit board, and utilizes a backside heatsink.



(a) (b)

Figure 8.4: Dual band class E/F_{odd} amplifier implemented by Florian Bohn. Circuit schematic (a) and prototype photo (b).

Upon achieving the correct tuning in each band, not a simple task as any changes of component values result in significant effects in both bands, the measured performance shown in Table 8.2 is achieved. As can be seen, the output power in each band is similar. The efficiency is around 90% in both bands, and the performance is slightly worse in the higher frequency band as expected.

	7.15MHz	10.1MHz
Output Power	250W	225W
Drain Efficiency	94%	90%
Gain	16dB	15dB
PAE	92%	87%

Table 8.2: Dual-band amplifier measured performance.

8.4.2 Wideband ZVS Amplifiers

Since multi-band amplifiers are achievable, it is not unreasonable to suspect that amplifiers achieving good performance in a continuous range of frequencies may be possible [67]. In order to achieve this, the conceptual circuit must be modified to employ a bandpass filter short-circuiting all frequencies not in the operational band, and to supply the negative capacitance required for ZVS tuning for all frequencies inside this band. This circuit is shown in Fig. 8.5.

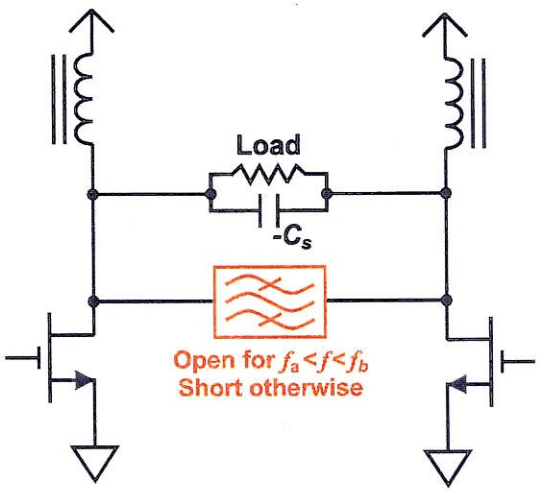


Figure 8.5: Wideband class E/F_{odd} amplifier concept.

Since this circuit requires a negative capacitance over a continuous range of frequencies, it is not possible to implement it exactly. As a result, it is necessary to be content with an approximation, resulting in operation that is not exactly, but close to ZVS over the frequency band.

Such a matching circuit may be implemented using a bandpass ladder filter as shown in Fig. 8.6. Unlike a standard ladder filter design, wherein the component values are adjusted to achieve a fixed load input resistance over the passband, the values are selected so that the filter is slightly detuned, providing a slightly inductive input impedance. It has been found that a sixth-order filter such as the one shown is suitable for achieving flat

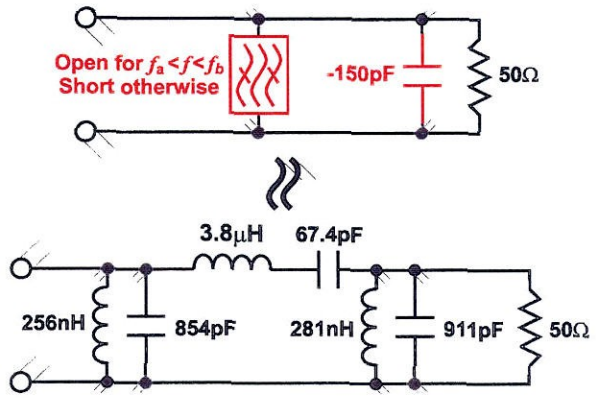


Figure 8.6: Ladder filter to approximate negative capacitance over the operation band.

output power and efficiency, although filters with lower or higher order also may be employed.

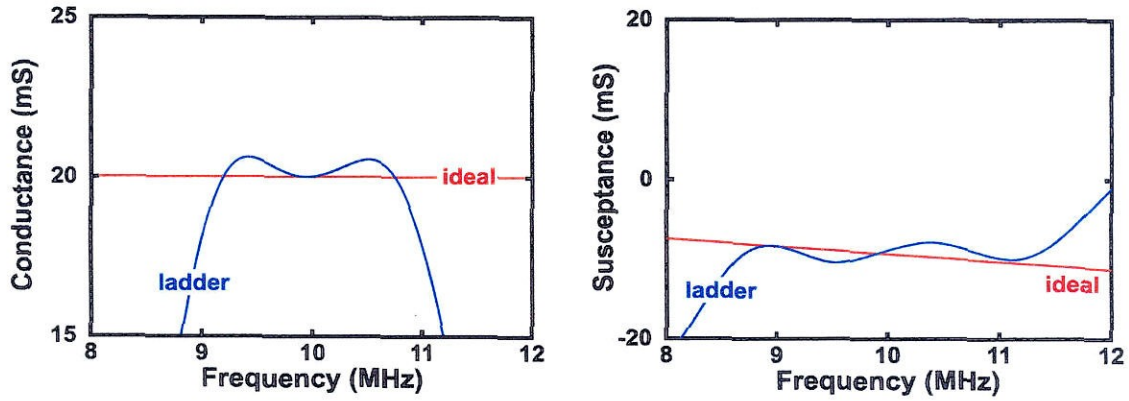


Figure 8.7: Input admittance of the ladder filter: conductance (a) and susceptance (b).

The component values may be found using a circuit simulator such as ADS, first adjusting the tuning by hand followed by a gradient optimization routine for fine-tuning. In the case of this example, the design was optimized for a best fit to the ideal (non-causal) input admittance over a band from 9MHz to 11MHz. The resulting input admittance, plotted with the ideal ZVS, constant power tuning is shown in Fig. 8.7.

A switching amplifier utilizing this matching circuit has been simulated in PSPICE to predict the performance. The results, shown in Fig. 8.8, are very promising, predicting consistently high efficiency over the entire 9MHz-11MHz band, and a 3dB bandwidth

well in excess of the desired 20%. More impressively, however, is that over a 15% bandwidth, better than 0.5dB of flatness in output power and 1% variation in efficiency is predicted.

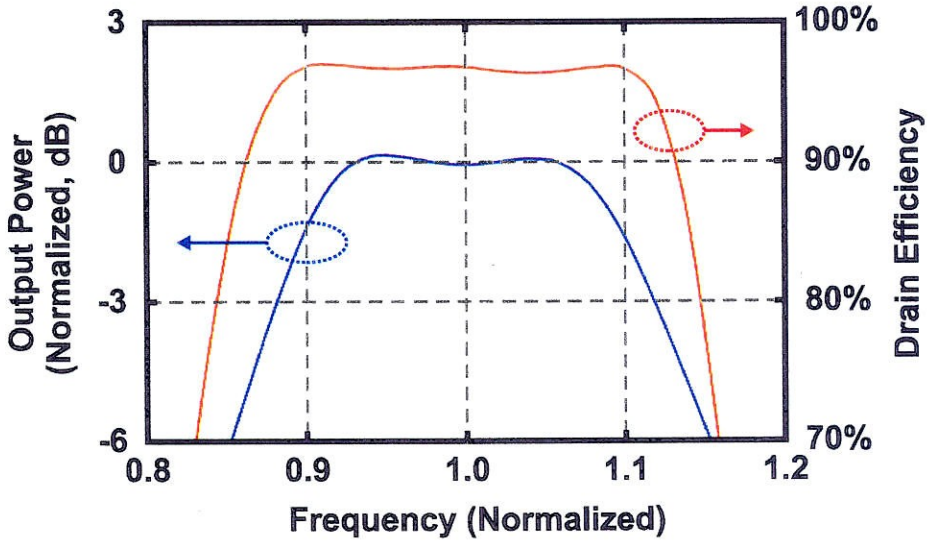


Figure 8.8: Wideband Class E/F_{odd} circuit (a) and simulated performance (b).

8.5 Integrated Circuit Implementation

One of the most promising applications for class E/F amplifiers is in the realization of integrated circuit power amplifiers for use in low-cost consumer products such as wireless handsets and wireless networking applications where ultra-low cost and high power efficiency are required. There have been many attempts to implement class E amplifiers using integrated circuit approaches [e.g. 2,55,68], but the ability to integrate the passive components of the output matching network onto a lossy substrate such as found in low-cost silicon technologies has been elusive. In order to further reduce the cost and size, and to allow higher levels of integration, such a technique is required. Furthermore, once such a technique is found, a power amplifier tuning compatible with this integration technique is required.

8.5.1 Circular Geometry / DAT

The first successful method for integration of a Watt-level, GHz-range power amplifier in silicon has been discovered recently by Ichiro Aoki at Caltech. This technique, known as the circular-geometry *distributed active transformer* (DAT) [69-72] elegantly combines impedance transformation and power combining to achieve much higher power levels and efficiencies in a fully-integrated design than was formerly possible.

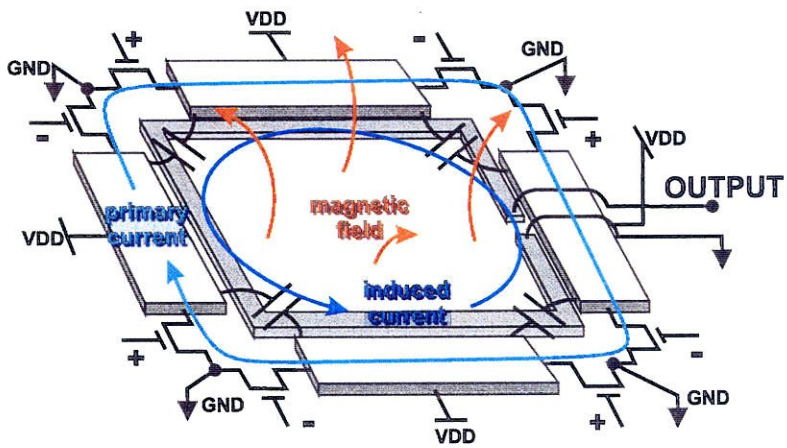


Figure 8.9: Aoki circular-geometry distributed active transformer power combining circuit.

The basic DAT circuit geometry as implemented on a silicon substrate is shown in Fig. 8.9. Functionally, the circuit consists of two parts: a distributed primary circuit whose purpose is to drive ac current around the structure so as to generate magnetic fields in the center, and a single-turn secondary conductor on which the magnetic field generates an EMF to be delivered to the load. From the perspective of the currents and the magnetic fields, the circuit is indistinguishable from a single-turn coupled-inductor transformer. The difference lies in the fact that the EMF on the primary circuit is dropped not at a single point as in a traditional transformer, but across some number N points so that the voltage drop at each gap in the primary conductor is N times smaller than the total EMF around the loop. By driving each gap in the primary with a push/pull pair of transistors,

even relatively low voltage devices can generate significant voltage on the secondary due to the factor of N multiplication. Additionally, due to the circular geometry structure allowing the use of high-Q slab inductors and the inherent low stored energy in the structure relative to traditional LC matching techniques, the power transfer efficiency is considerable better than traditional on-chip matching techniques.

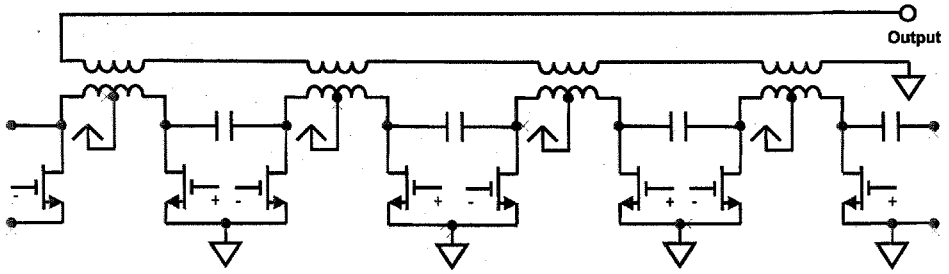


Figure 8.10: DAT equivalent circuit model.

An equivalent circuit model of the DAT is shown in Fig. 8.10. The primary and secondary conductors in this model are represented by four coupled-inductor transformers, which on the secondary side are connected in series while being driven independently on the primary side by four push/pull transistor pairs. To compensate for the magnetizing inductance of the transformer structures, capacitors have been added between the drains of the transistors in adjacent push/pull pairs. Due to the symmetry of the circuit, this has the same effect as if the capacitors were placed in parallel with the primaries of the transformer structures.

The resulting equivalent circuit for a single push/pull pair is depicted in Fig. 8.11. The two transistors are connected together with a differential load consisting of a capacitor, a transformer having significant magnetizing susceptance, and a load resistance connected through the transformer. The difficulty with such a circuit topology – developed from the need to optimize the passive circuit design, not to provide any particular harmonic tuning – for building class-E type amplifiers is readily apparent. There is no obvious method to either connect a series LC filter between the switch and the power combining circuit, nor is there an obvious method to provide the same effect. A series LC filter would require a

large-valued inductor which, even if it were acceptable from an efficiency standpoint, simply would not fit into the compact layout of the DAT structure. To provide the same tuning without using a series inductor would require that, at the very least, the effect of the differential load capacitor be significantly reduced at the third and fifth harmonics.

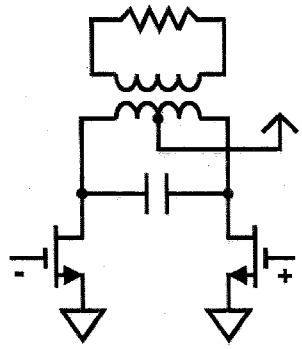


Figure 8.11: Equivalent circuit for one DAT push/pull pair.

Fortunately, due to the knowledge of E/F tunings, it becomes unnecessary – in fact counterproductive – to attempt to force the circuit into class-E operation. The basic circuit structure is ideal for the implementation of the E/F_{odd} tuning, having the differential load of a resistance and a parallel LC tank as essential elements in the power combining circuit structure. In fact, no additional components are needed for this tuning, and the only requirement is that the tank be slightly detuned to achieve the ZVS switching conditions. In this way, the choice of E/F tunings for the DAT amplifier has less to do with the performance advantages of the E/F tuning than the accommodation of the circuit topology set by other constraints. Although the performance advantages of the E/F_{odd} tuning are of great value, particularly due to the larger capacitance tolerance allowing the use of large sized FET devices, the essential advantage of E/F in this case is the improved understanding of general classes of ZVS switching amplifiers. Rather than attempting to force the circuit topology to achieve a class-E tuning, the tuning is selected to best match the constraints set by the circuit topology.

To test both the DAT structure and the feasibility of microwave CMOS E/F amplifiers, a prototype amplifier has been designed and tested by Ichiro Aoki. Fabricated in a standard 0.35um CMOS process, this four-section DAT amplifier is designed to produce over two Watts of output power at 2.4GHz using around $3mm^2$ of die area and no external matching components. A die photo of the fabricated prototype is shown in Fig. 8.12.

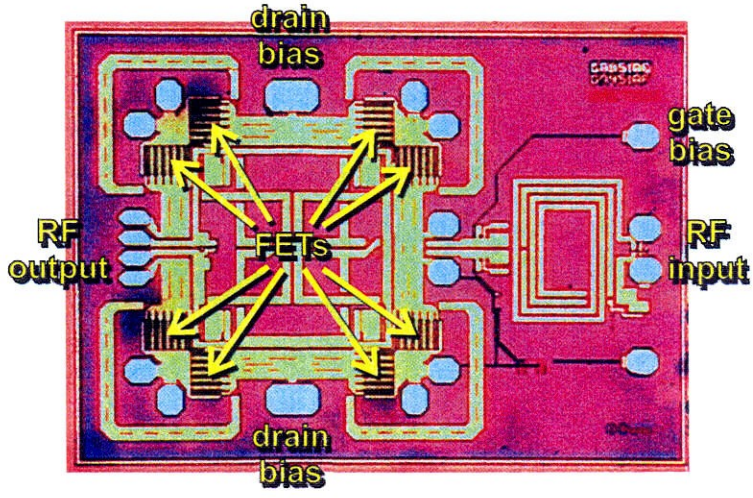
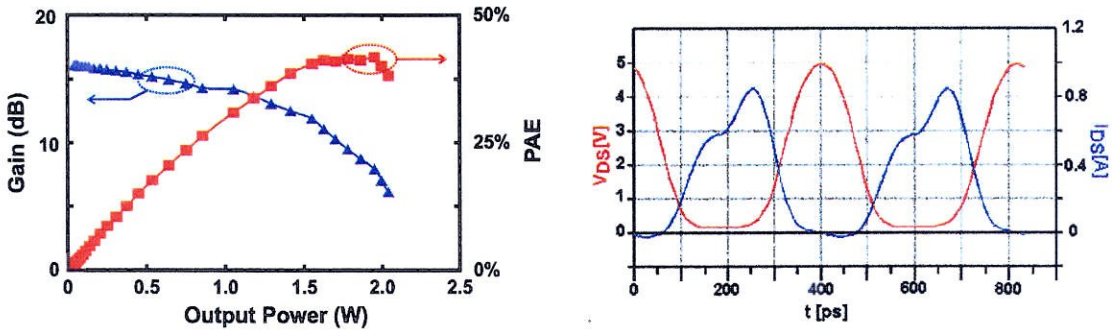


Figure 8.12: Die photo of E/F CMOS power amplifier using DAT power combining.

The measured amplifier performance is plotted in Fig. 8.13a. In order to maximize the gain, the amplifier is biased so that in small-signal it is operating in class-A mode, entering E/F operation as the amplifier begins to reach gain compression. The PAE when operating at the maximum power in switching mode is 41%, out of which the actual efficiency of the switch is expected to be 65%-70%. The remainder of the power loss comes from the low gain (<10dB) and the loss of the on-chip passive components.

The drain switching waveforms as simulated using the ADS harmonic balance simulator are shown in Fig. 8.13b. The operation of the circuit is actually somewhere between E/F_3 and E/F_{odd} due to a resonance in the circuit short-circuiting the third harmonic much more strongly than the fifth.



(a) (b)

Figure 8.13: DAT measured performance (a) and simulated large-signal drain waveforms (b).

8.6 High Power HF/VHF Implementations

One of the applications where class E has found the most application is in the efficient amplification in the HF and VHF frequency ranges [e.g. 7-10,51]. Using low-cost, high-voltage high-current MOSFET transistors developed for lower frequency power converter applications, high power HF designs have been implemented with output powers ranging from tens of Watts to over a kilowatt with efficiencies above 80% [7-9]. Similarly, LDMOS transistors developed for use in cellular phone base stations have been used to implement class-E designs in the VHF region, achieving 620W of output power with 60% efficiency at 144 MHz [10]. Due to the theoretical performance advantages of E/F tunings, it is expected that improved performance may be achieved. This section presents the first E/F_{odd} family amplifier developed for use in this frequency region. Additionally, a wideband high-power VHF design is proposed with potential for commercial use in broadcast systems.

8.6.1 7-MHz, 1-kW Class $E/F_{2,odd}$ Prototype

To verify the performance of the $E/F_{2,odd}$ amplifier class, as well as to explore its potential for high power HF use, a 7-MHz design with output power of 1kW has been undertaken [56]. For the active device, the STW20NB50 500V, 20A MOSFET from

STMicroelectronics has been used. This transistor is from the company's standard line of switching devices intended for use in dc/dc converters at frequencies in the 100kHz range, and is packaged in a standard TO-247 package. As of the time of this writing, the price per unit is under $4 in small quantities.

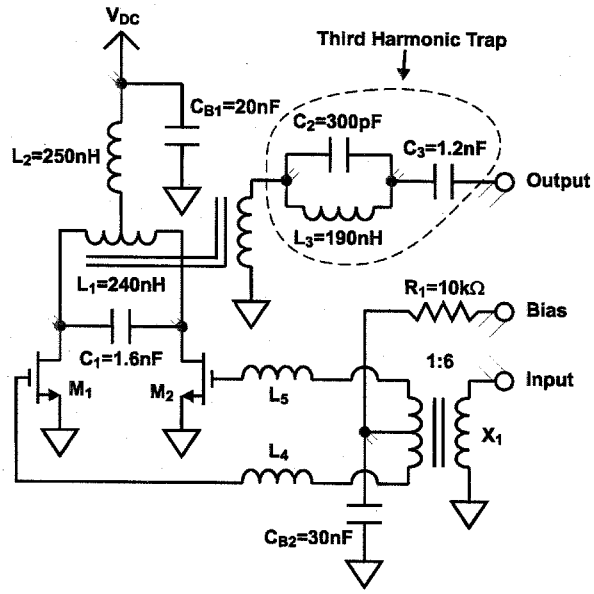


Figure 8.14: Circuit schematic of the prototype $E/F_{2,odd}$ amplifier.

A schematic representation of the implemented circuit is depicted in Fig. 8.14. Since the E/F_{odd} circuit topology relies on a balanced load – not convenient for most applications – an output transformer is used as a balun. The magnetizing inductance L_1 of this air-core transformer is used to provide the inductance required for the parallel resonant tank.

Modeling has been performed using a simple switch model in PSPICE. The transistor's conductance characteristics are modeled as a switch in series with a resistance. To model the output capacitance, the drain-source capacitance has been measured as a function of the drain voltage, holding the gate voltage at zero. This data has been fit to a model consisting of the parallel combination of two varactors and a linear capacitance. Since the

gain of this device in this frequency is high enough that the input power can be safely ignored in the simulation stage, the gate characteristics have not been modeled.

By use of the simulation, the values of the tank components have been adjusted to achieve ZVS conditions. To account for the parasitic package inductances, the simulation is performed with a 5nH inductance in series with each transistor. This results in a ringing transient superimposed on the voltage and current waveforms. This ringing, depicted in Fig. 8.15, is a result of the resonance between the two package inductors, the tank capacitor C_1, and the drain-source capacitor of the non-conducting transistor.

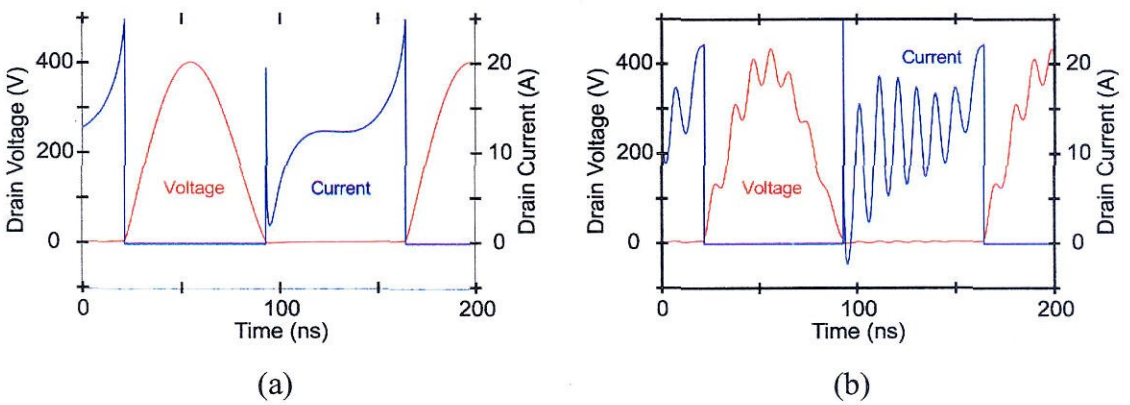


Figure 8.15: Simulated waveforms with (a) no package inductance and (b) with 5nH package inductance.

This ringing increases the RMS current through the switch, and it may cause the parasitic drain-source diode to conduct if the current becomes temporarily negative. Since both effects are undesirable, this ringing amplitude was reduced by lowering the loaded Q (quality factor) of the resonator consisting of L_1, C_1, and the load resistance to a value of approximately 3.6. The second harmonic tuning also helps to keep the current positive by giving additional peaking in the early part of the current cycle where the ringing has the highest amplitude.

Lowering the tank Q, however, has an undesirable effect on the harmonic filtering. Since this tank serves to divert the odd harmonic currents away from the load, the lowered Q results in more of these currents conducting through the load. To avoid an unacceptably

high third harmonic as a result of this, a third harmonic trap was added in series with the load. Even with the lowered Q, the simulation predicted acceptable performance at the other harmonics. The even harmonics are rejected by circuit symmetry and the higher odd harmonics are rejected sufficiently by the LC tank

Assuming passive component quality factors of 150, simulation results predict an output power of 1.4kW at an operation frequency of 7MHz, with 90% drain efficiency using a 125V supply. Harmonic levels were predicted to be at least 40dB below the fundamental for all harmonics. The simulated waveforms are shown in Fig. 8.15.

A prototype amplifier using this design, shown in Fig. 8.16, has been constructed for performance verification. This amplifier is constructed on patterned FR4 circuit board with the transistors directly mounted to a backside aluminum heatsink through holes cut in the circuit board. This makes for a compact and solid package, and allows for extremely good thermal performance. An integrated fan attached to the back of the heatsink allows for continuous operation at this high power density. The resulting amplifier is small at approximately $11\,\text{cm} \times 9\,\text{cm} \times 9\,\text{cm}$ (including fan), due to the lack of large-valued inductors made possible by using only parallel LC resonances in this topology.

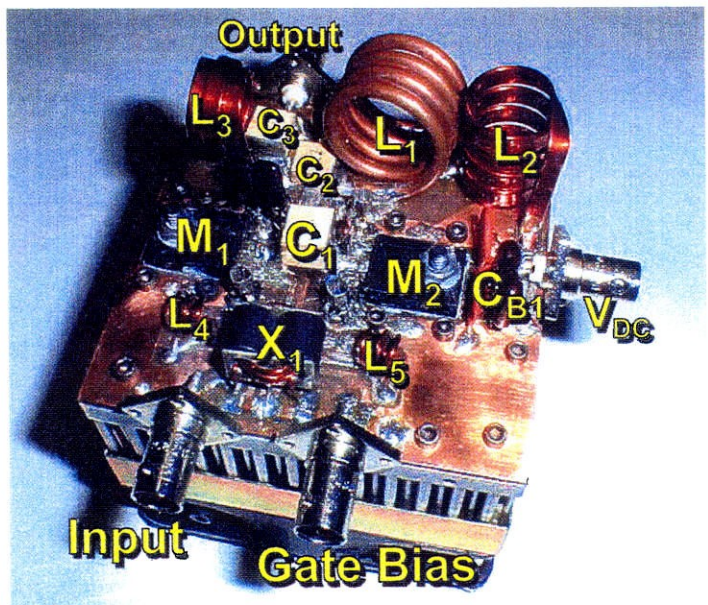


Figure 8.16: Photo of fabricated $E/F_{2,odd}$ 7MHz, 1kW prototype.

Performance is measured using a Kenwood TS-850S RF Transceiver as the input power source using a Bird 2kW, 30dB attenuator as the load. Power measurements are taken with Bird 4421 power meters equipped with Bird 4021 inline power sensors. The (attenuated) output spectrum is measured using an HP 8592A spectrum analyzer.

Fig. 8.17a shows the amplifier's measured drain efficiency as a function of drive power for several different output power levels. Fig. 8.17b shows efficiency and gain as a function of output power as varied by changing the drain supply voltage. The amplifier performs with similar efficiency over a wide range of drive powers, and the efficiency is consistently high over a wide range of output powers, suggesting that the amplifier might be used effectively in an envelope elimination and restoration system [1,73,3]. The drain efficiency is around 87% up to 800W where it begins to degrade, probably as a result of transistor saturation at the higher current levels. Due to limitations of the power meters, measurements could only be taken up to 1.2kW.

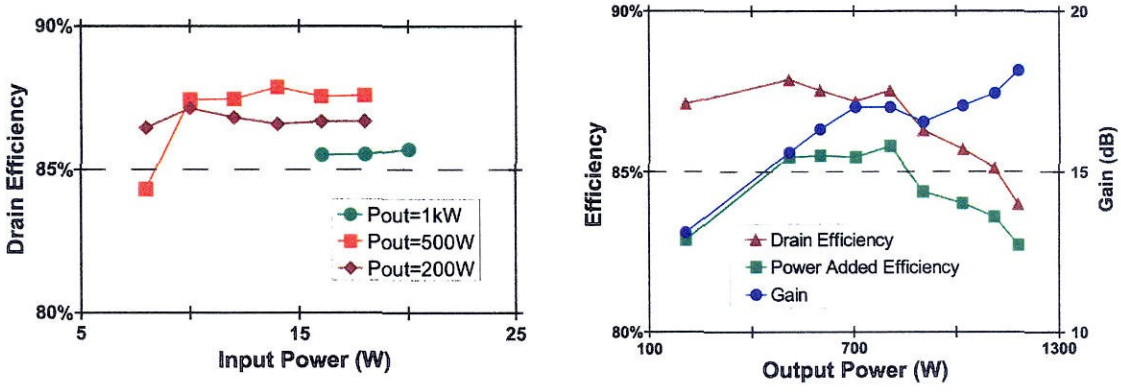


Figure 8.17: Measured $E/F_{2,odd}$ amplifier performance at 10MHz.

As should be expected with a switching amplifier, the gain increases with the output power since the optimal input power remains relatively constant over the full range of output powers. The output power shows a very clear square law dependence on the supply voltage, as is consistent with the bias scaling rule developed in Chapter 8. The input

voltage standing wave ratio (VSWR) is between 2:1 and 3:1 depending on output and input powers. If desired, the gain might be further improved by better matching the input.

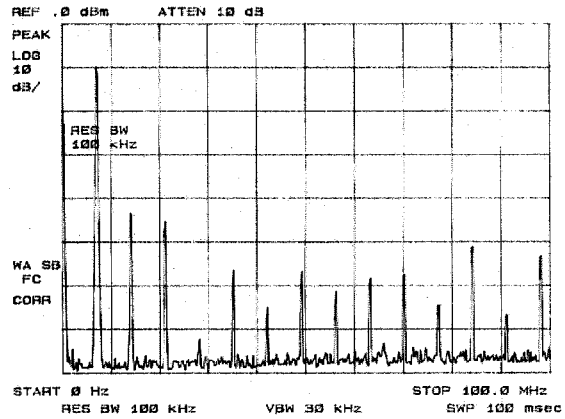


Figure 8.18: Measured output spectrum at 1kW output power.

The output spectrum measured at 1kW power level is shown in Fig. 8.18. This spectrum is typical of the performance for all power levels above 50W. The second and third harmonics are approximately 33dB and 35dB below the fundamental respectively, and all other harmonics are at least 40dB below the fundamental. The second harmonic is unusually high for a push/pull amplifier, probably the result of an imbalance in the impedances presented to the two transistors. As a result, this harmonic may be additionally suppressed by increasing the symmetry of the layout or adding compensation for the asymmetry. The third harmonic is present due to the output third-harmonic trap being imperfectly tuned, which should be correctable by additional tuning of this component. A previous version using a different inductor in the third harmonic trap reduced this harmonic to under 50dB below the fundamental, so it is expected that additional circuit tuning would allow this harmonic to be further reduced.

The measured and simulated drain voltage waveforms for the two transistors are shown in Fig. 9. The ringing caused by the package inductance is clearly visible. The accuracy of even this simple simulation model in predicting the switching waveforms is

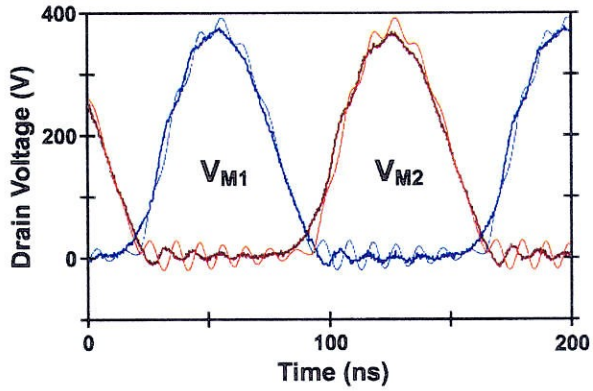


Figure 8.19: Measured and simulated drain voltage waveforms.

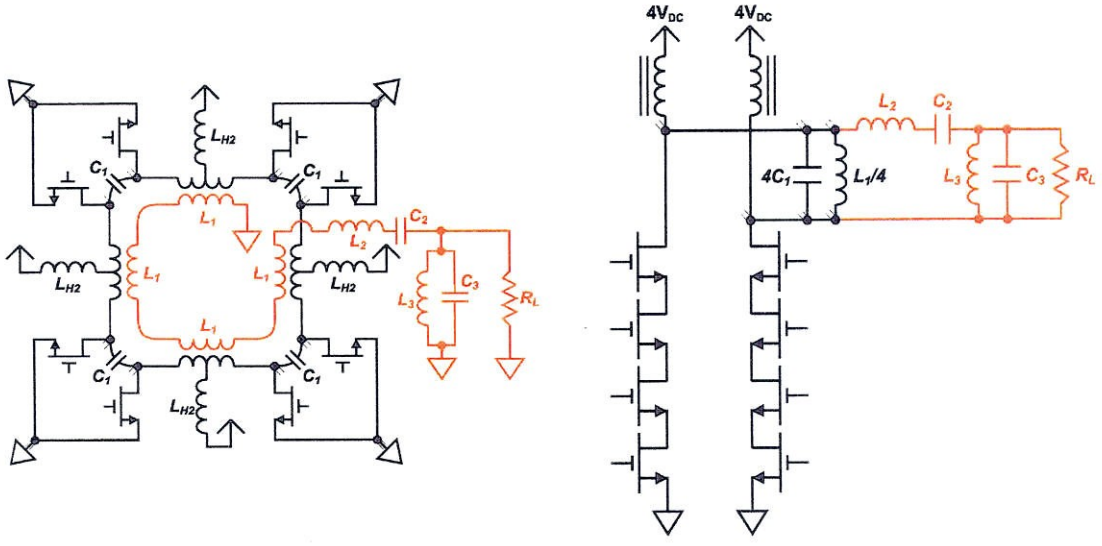
clearly quite acceptable. Unfortunately, the current waveforms have not been measured, since techniques for this measurement are sufficiently more difficult.

In addition to demonstrating the feasibility of the E/F_{odd} family, this amplifier exhibits high efficiency at high power levels in an extremely compact design. The achievement of 1kW in such a small package is unlikely to be matched with a similarly-performing class-E design.

8.6.2 DAT Implementations

In addition to allowing a power-efficient technique for integration circuit amplifiers, the DAT technique might also be used in the design of high power amplifiers constructed from discrete components. In doing so, the output power achieved by a given tuning from a given bias voltage may be increased by a factor of N^2 without necessitating excessive use of resonant impedance matching techniques which reduce the efficiency and limit the operational bandwidth. Additionally, since the DAT uses power combining, thermal issues should be significantly less problematic since the heat sources may be spread more uniformly across the heatsink surface rather than being concentrated into a single location. Finally, for a factor of E increase in output power, the DAT technique requires a reduction of the drain impedances of a factor of $\sqrt{E}$ whereas any technique using a single transistor must reduce the impedance seen by that transistor by a factor of E. Thus the power can be

increased by far greater factors using the DAT technique before impedances become unreasonably low.



(a) (b)

Figure 8.20: Wideband DAT Class E/$F_{2,odd}$ implementation for HF/VHF transmitter applications: circuit schematic (a) and equivalent circuit (b).

An promising application of this technique might include high power VHF amplifiers for commercial broadcast use. For instance, FM radio transmitters require several kilowatts of power at frequencies around 100MHz. Using 100V breakdown LDMOS transistors to construct a class E/F_{odd} power amplifier without any impedance transformation would result in an output power of:

$$P_{out} = \frac{(100\text{V})^2}{2 \cdot 50\Omega} = 100\text{W} \tag{8.1}$$

This power level is not sufficient even for a small transmitter, and to reach kilowatt levels the load impedance would have to be transformed by at least a factor of ten. If, on the other hand, a DAT implementation such as the one shown in Fig. 8.20 is used, where four class E/F_{odd} amplifiers are power combined, the output power without the need for additional impedance matching is 1.6kW. Since the DAT technique does not rely on high-Q tuned circuits and thus does not result in significant bandwidth reduction, a wideband

tuned load such as that described in Section 8.4.2 might be used to allow the amplifier to transmit on different channels without the need for retuning of the load network. As before, this tuning may be accomplished by the means of a detuned ladder filter, shown here as the inductors L_2 and L_3, and the capacitors C_2 and C_3. This circuit not only provides tuning for wideband ZVS operation, but also serves to assist in rejecting harmonics at the load.

8.7 Compact Implementations

In the HF/VHF region, one of the chief disadvantages of the class-E approach is the need for a large-valued inductor as part of a series LC tank. Other amplifier classes, such as class A, class B, and class C usually accomplish the harmonic filtering with a parallel LC resonance. For the same resonator loaded Q, Q_L, this results in an inductor with a value a factor of Q_L^2 smaller than the one required for class E. The result is that, in HF/VHF class E circuits, the size is usually dominated by this fist sized inductor.

Supposing that a smaller, more compact design was desired, it would be useful to have a switching amplifier tuning relying on only small-valued inductors so that the high efficiency of a switching amplifier might be combined with the compact package of a class-C design. Fortunately, since the E/F family allows a choice from a large variety of different tunings and implementation strategies, this goal can be realized by choosing from this expanded pool of options the tunings implementable using parallel LC resonances.

The most obvious such tunings are in the E/F_{odd} family. This entire family accomplishes the harmonic filtering of the load by means of a parallel LC tank placed in parallel with the differential load, potentially allowing a very small inductor to be used. Furthermore, the push/pull nature of the circuit provides a factor of four increase in the output power using transistors of the same breakdown voltage without the need for impedance transformation (which would require additional inductors). These two factors

combine to allow a very high output power per unit volume to be achieved. To show the order of size improvement possible, the class $E/F_{2,odd}$ prototype from the previous section is displayed in Fig. 8.21 with the inductor from a 500W class-E kit amplifier until recently supplied by Caltech as a service to the HAM community. As can be seen, just this single component is comparable in size to the entire $E/F_{2,odd}$ amplifier including the heatsink and cooling fan.

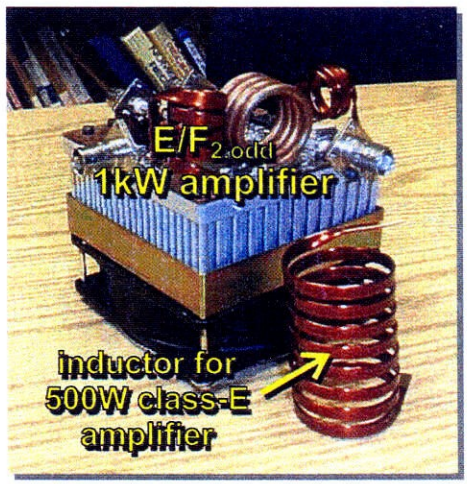
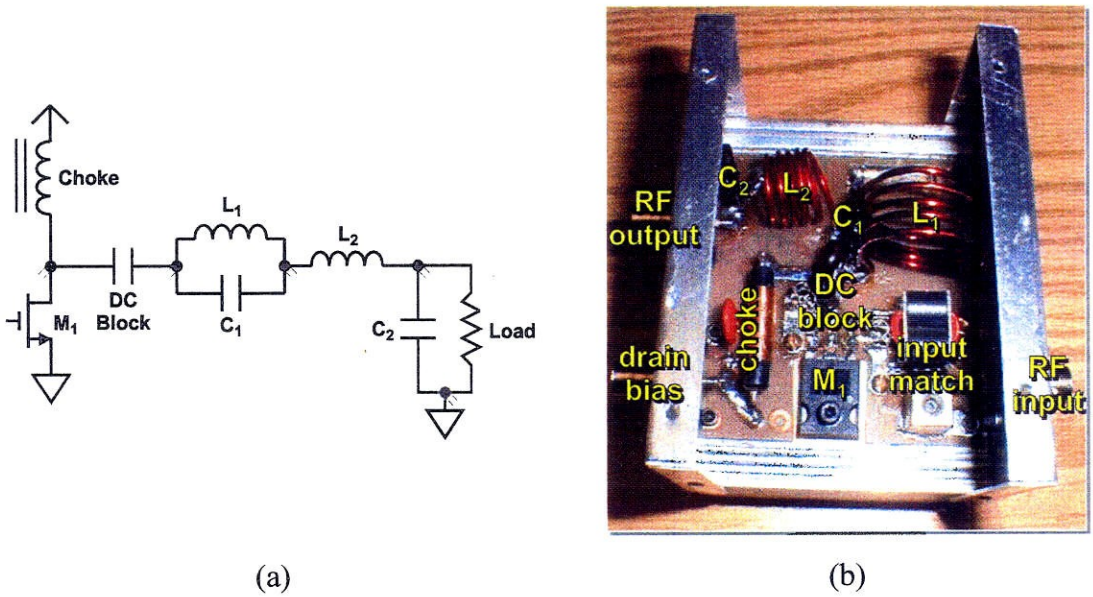


Figure 8.21: Photo of 1 kW $E/F_{2,odd}$ amplifier and inductor from 500 W class-E kit.

The E/F_{odd} family, however, is not the only means to accomplish a considerable size reduction. In some cases it may be more cost-effective to produce a single-ended design for lower power levels, reducing the number of transistors and the complexity of the input matching circuit.

One prototype amplifier, shown in Fig. 8.22, has been constructed to explore this possibility. This amplifier is designed with the goal to reduce the size as much as possible while achieving high power efficiency in an industrial power application. Since the primary goal is to produce power into a industrial load rather than for wireless transmission, the acceptable harmonic levels are relaxed to 30 dB below the fundamental.

Due to the relaxed requirements of harmonic power levels, several techniques may be advantageously employed. First, it may be noted that the most problematic harmonic is



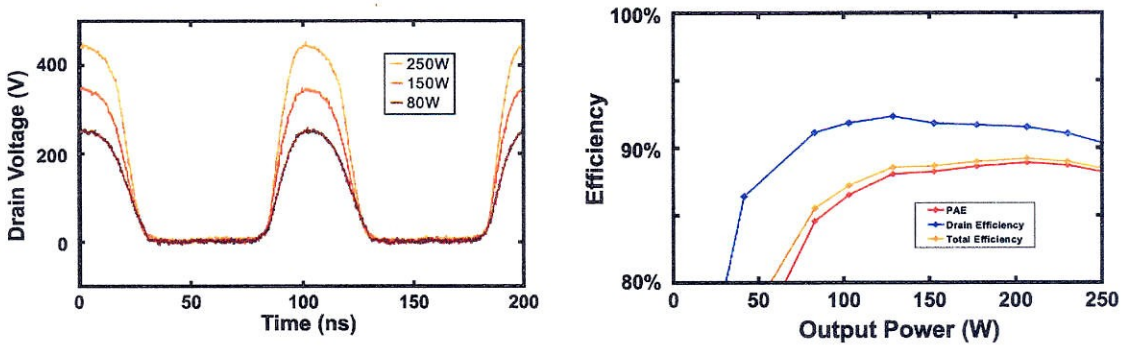
(a) (b)

Figure 8.22: Quasi-E/$F_{2,3}$ compact power amplifier: schematic (a) and photo (b)

usually the second, and so blocking this harmonic is the first priority. To this end, a parallel LC resonator consisting of L_1 and C_1 is employed, and to block the second harmonic from entering the load. Since this tank will have an inductive impedance at the fundamental, it may be used to also supply the some of the necessary load reactance for ZVS operation at this frequency. To provide some impedance transformation in order to increase the output power, capacitor C_2 and part of the inductance of L_1 and L_2 provide a resonant LC match. This takes care of the fundamental and second harmonic. The third and higher harmonics, while not blocked completely from the load, are attenuated to some degree by the LC filter consisting of L_2 and C_2. Although this does not provide enough harmonic rejection for use in communications applications, it is enough that no significant power is delivered at these frequencies.

In order to provide some harmonic tuning, the elements of the circuit may be slightly detuned so that the network presents a slightly inductive impedance at the second harmonic and a slightly capacitive impedance at the third. When placed in parallel with the switch's output capacitance, this will have the effect of increasing the impedance of the second harmonic and decreasing that of the third. While this proves advantageous in

terms of the switching efficiency, such detuning in this network increases the levels of the harmonics at the load. Thus, the detuning may be increased until the second and third harmonics are at their maximum acceptable level. This results in a circuit where the second and third harmonics are not completely open and short -circuited, but increased and decreased in impedance relative to class E respectively. This results in a sort of quasi-class E/F amplifier.



(a) (b)

Figure 8.23: Measured performance of quasi-E/$F_{2,3}$ prototype: drain voltage waveforms for various output power levels (a) and efficiency (b).

The measured amplifier performance is shown in Fig. 8.23. The voltage waveforms are clearly better than class E, with a much lower peak to dc ratio of around three. This is primarily due to the tuning of the third harmonic and the use of a slightly non-ZdVS tuning, both of which function to reduce the peak voltage. The efficiency is around 90% over a wide range of output powers, from 100W to over 250W.

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