TOPOLOGY AND ANALYSIS IN PWM INVERSION, RECTIFICATION, AND CYCLOCONVERSION

Thesis by

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In Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

California Institute of Technology

Pasadena, California

1984

(Submitted May 14, 1984)

to my parents

ACKNOWLEDGEMENTS

I would like to thank my advisors, Professors S. M. Ćuk and R. D. Middlebrook for welcoming me to their group at Caltech and bringing me up in Power Electronics. They have offered me the opportunity to explore an area still new and challenging to many of us. They have given me the freedom to select the research direction and to pursue it to our mutual satisfaction. I wish I could contribute more than just this small thesis to deserve their generous givings.

I am indebted to the Office of Naval Research and Naval Ocean Systems Center for their financial supports during the last few years. My special thanks go to Caltech for the Graduate Teaching Assistantships and the President's Fund that initiates research activities in the ac conversion field.

I would like to give credits to other members of the Caltech Power Electronics Group for their contributions to the content and format of this thesis. I am particularly grateful to Mr. X. L. Ma who suggests the six-stepped PWM for the buck rectifier.

I appreciate the generosity of all who have made my days at Caltech a unique, valuable experience. My gratitude to the Institute and memory of those yesterdays shall last.

ABSTRACT

Topologies and *analysis techniques* in switched-mode *dc conversion (dc-to-dc)*, *inversion (dc-to-ac)*, *rectification (ac-to-dc)*, and *cycloconversion (ac-to-ac)* are unified in this thesis. The *buck*, *boost*, *buck-boost*, and *flyback topologies* are used to demonstrate that familiar dc converters can be extended into *equivalent ac converters*. Although some of these are presented as fast-switching circuits, they have also been found in slow-switching applications. Thus, *topology* is the unifying factor not only over four fields of power electronics, but also within each field itself.

Describing equations are used to characterize *low-frequency* components of the inputs and outputs in fast-switching networks containing *filters*, excited by *dc* or *balanced sinusoidal* sources, and *pulse-width-modulated* by *dc* or *balanced sinusoidal duty ratios*. They are first written in the stationary (abc) reference frame and then *transformed to the rotating (ofb) coordinates*. In the ofb coordinates, all balanced *ac* converters with any number of phases are reduced to a set of *continuous*, *time-invariant* differential equations describing a two-phase equivalent.

Steady-state, *dynamic*, and *canonical models* are then solved in the rotating frame of reference. Emphasis is stressed on circuit ideality - *sinusoidal outputs for sinusoidal inputs* even though a switched network is nonlinear - and effects of *filters* on *steady-state* and *small-signal frequency responses*. These results are similar for a dc converter, inverter, rectifier, and cycloconverter of the same topology; this similarity again confirms that

the four converters are closely related. The *cycloconverter* is thus established as the *generalized converter* that degenerates to the other three under special input and output frequencies.

Practical issues discussed include the realization of the switches, modification of drive and topology for bidirectionality of power flow, isolation, switched-mode impedance conversion, and measurement techniques.

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INTRODUCTION

The four areas of switched-mode power conversion are *dc conversion* (dc-to-dc), *inversion* (dc-to-ac), *rectification* (ac-to-dc), and *cycloconversion* (ac-to-ac). Although dc converters as well as inverters, rectifiers, and cycloconverters have been coexisting for a long time, their applications and advances in semiconductor technology have led them to flourish in different directions. Dc converters serve delicate and low-power circuits, such as signal-processing ones, that require tight regulation, high-quality outputs, and fast dynamic responses. Owing to these high standards, dc power supplies have evolved to a close-to-ideal stage. Inverters, rectifiers, and cycloconverters, on the other hand, encounter more rugged and higher power applications, such as motor drives, that can tolerate poor waveforms and slow dynamic performance. Thus, harmonic heating, torque pulsation, poor power factor, electromagnetic interference, sluggish response, and so on, have been common problems generated by these high-power units.

The difference in application specifications, however, is only an excuse for the outperformance of dc converters over ac converters (i.e., inverters, rectifiers, and cycloconverters). *The power-speed limitation* of semiconductor devices, used to realize the switch, is the principal force that segregates the disciplines of power electronics. Current developments in switching devices, for instance, allow the transistor to switch a few tens of kVA below $20\,kHz$; the gate-turn-off (GTO) device, a few hundreds of kVA below $5\,kHz$; and the thyristor, a few thousands of kVA below $500\,Hz$. Dc

converters fall in the low-power range and, hence, enjoy the advantages given by the fast bipolar junction transistor (BJT) and field-effect transistor (FET). High-power ac converters lose these benefits because they can use only the slow thyristor. The performance of medium-power converters, fortunately, has been improved recently owing to progress made in GTO fabrication.

Many advantages of fast switching are apparent from comparison of existing dc and ac power processors. First, *filters* are used more freely because their size diminishes with increasing switching frequency. They attenuate switching harmonics and, hence, smooth out terminal waveforms. They also absorb mismatches between stiff voltage or current sources to suppress excessive current or voltage spikes.

Second, reactive elements, together with high switching frequency, allow the development of *novel topologies* with *new operating principles*. This development can be carried out in two forms. In the simpler one, existing topologies are preserved, but their switches are operated according to some new strategies easier to implement with fast switching. *Pulse-width modulation (PWM)* and *resonance* are two well-known examples of such high-frequency energy processing techniques; the PWM category itself consists of a variety of drive policies. In the more advanced development method, innovative topologies are synthesized by topological manipulation of inductors, capacitors, and switches [3 and 4]. The number of useful circuit configurations increases quickly as more reactive components enter the power stage. A proof of this expansion is the large family of converters that have evolved in the dc conversion area.

Third, a larger number of topologies introduces a more diversified list of properties that encompass a broader range of applications. Thus, the *dc gain* does not have to be only of buck (step-down), but can also be of boost (step-up) or buck-boost type. Additional *control parameters* are available so that, for instance, the output amplitude can be adjusted not at the expense of input power factor. *Dynamic response* can be made very fast by increasing the switching frequency and, consequently, reducing the value of energy-storage components. *Isolation* is feasible because the isolation transformer is small and economical.

Fourth, it is *possible* to generate *dc* or *sinusoidal* waveforms at the input and output of the power processor in an *open-loop* fashion using only *dc* or *sinusoidal* control functions. This property is to be distinguished from the *smoothness* of waveshape discussed earlier; the dc or sinusoidal characteristic describes the low, useful frequency components of the spectrum while the smoothness property refers to the attenuation of switching harmonics. The high-quality output alleviates harmonic stresses at both the load and source, facilitates the understanding of the power stage, and simplifies the design of the overall system.

In the last few decades, the aforementioned attributes have been confined to dc converters because a sufficiently fast switch has not been available at the power level of most ac applications. Recently, however, breakthroughs in semiconductor fabrication have improved the speed of the switches in medium-power range. These progresses, together with the growing concern to reduce the contamination of the electrical environment by slow-switching circuits, have motivated the extension of fast-switching technology from the dc conversion into the inversion, rectification, and

cycloconversion fields. As dc conversion, ac conversion can be accomplished by either the *resonance* or the *PWM* principle. Although original steps have been reported in both directions, a great deal of fundamental works still need to be done. Since this task certainly takes more than the scope of one thesis, only the PWM area is enlightened here. It is hoped that analogous studies will be carried out for resonance conversion in the near future.

As many other new disciplines, fast-switching PWM ac conversion has started slowly. One of the first efforts parallels many dc regulators to create a multiple-input or multiple-output structure [19 and 28]. Such an approach has not received much attention because it ignores the polyphase synergism and, hence, uses too many components inefficiently. More thoughts are put in [37] to synthesize *genuine*, basic polyphase cycloconverters that require a minimal amount of switches to synthesize sinusoidal input and output waveforms. Nevertheless, reactive elements are assigned only secondary importance, and their *topological function* ignored. Because of this de-emphasis of the role of inductors and capacitors, [37] fails to discover a host of more useful ac-to-ac converters. Therefore, *a unified, complete picture that describes basic and derived PWM topologies in all four areas of switched-mode conversion, explains their performance systematically, and displays their relationship* still needs to be proposed.

A survey of the previous references reveals further that the analysis of fast-switching ac converters has been inadequate. *State-space-averaging* [2], intended for dc converters that have simple switching structures periodic at the switching frequency, cannot be generalized naturally to ac converters that contain a *large* amount of switches whose operations are *not* periodic at the switching frequency. Another modeling method has been

introduced recently in [1] for circuits without (or with negligible) filter components. Regrettably, it does not cover most practical cases in which filter corners, placed sufficiently low to attenuate the switching noise, do interfere with *steady-state* as well as dynamic performances. Therefore, *a generalized analysis technique that represents with improved accuracy the steady-state and dynamic behaviors of fast-switching PWM dc converters, inverters, rectifiers, and cycloconverters* still needs to be established.

Fortunately, the *describing equation technique* [10] has been devised for slow-switching ac converters. Since this method is very general, it applies to *fast-switching PWM dc and ac* networks as well. Describing equation is thus the unified analysis technique over all areas of power electronics and all ranges of switching frequency. Accuracy depends, of course, on the switching strategy, e.g., six-stepped, PWM, or something else.

The preceding two paragraphs embody the overall objectives of this thesis. The details of these objectives are:

- to revise *analysis* techniques for fast-switching PWM converters;
- to describe fast-switching *open-loop*
    - *inverter* topologies that invert a *dc* input into *sinusoidal* balanced polyphase outputs,
    - *rectifier* topologies that rectify *sinusoidal* balanced polyphase inputs into a *dc* output, and
    - *cycloconverter* topologies that convert *sinusoidal* balanced polyphase inputs into *sinusoidal* balanced polyphase outputs

  all using *sinusoidal pulse-width modulation*; and

- to establish a *topological relationship* among dc converters, inverters, rectifiers, and cycloconverters.

Most important in the above are the *open-loop* and *sinusoidal control* constraints imposed upon the power processors destined to generate ideal inputs and outputs. These strict criteria exclude the simplistic use of topologies with distorted outputs, for sinusoidal inputs, and then relying on feedback loops to suppress nonlinear harmonics. This thesis proposes to solve a more fundamental problem: to search for *open-loop* switched-mode networks that require only easy-to-synthesize *sinusoidal* functions to produce dc or sinusoidal quantities. Closed-loop operation is reserved to *regulate*, not to purify, output waveforms.

Since the analysis technique is universal to all fast-switching PWM converters whose useful bandwidth is restricted sufficiently below the switching frequency, it is discussed first in Chapter 1 without reference to any class of circuits. The *describing equation* method is established as the standard modeling procedure for the rest of the thesis. A procedure to derive the describing equations of a switched network is explained, and subsequent manipulations of these equations toward steady-state, dynamic, and canonical models investigated.

The next nine chapters are grouped into three parts: Part I for Inversion; Part II, Rectification; and Part III, Cycloconversion. The first chapter of each part reviews previous contributions in the respective field. The second details the topologies and studies their performance using the analysis technique outlined in Chapter 1; the topological relationship among the four kinds of converters is formulated in the last section of Chapter 9. The third chapter discusses practical aspects of the converters, such as

switch implementation, isolation, bidirectionality of power flow, impedance conversion, measurement principle, and so on, and verifies experimentally the theory predicted in the previous chapter.

The appendices at the end review dc conversion and the abc-ofb coordinate transformation used to simplify the analysis of balanced polyphase ac converters.

CHAPTER 1

ANALYSIS OF FAST-SWITCHING PWM CONVERTERS

This chapter consists of six sections. The first section reviews the characterization of a switch: its throws, switching functions, and *duty ratios*. The second section derives the *describing equations* of a switched-mode converter which identify duty ratios as control parameters. The third section transforms these equations to a new coordinate system in which all balanced polyphase ac circuits are represented by their *dc equivalents*. The last three sections then solve the transformed, time-invariant equations for their *steady-state* formulas, perturb them for their *small-signal dynamics*, and linearize them for their *canonical model*.

In what follows, the "boost inverter" merely serves as a concrete example of the general results. To fully appreciate the *analysis* methodology, it is best to disregard such *topological* issues as where this topology comes from, what it does, and, above all, *how it is switched*. As throughout the thesis, the switches here are assumed to be lossless, infinitely fast, and four-quadrant (i.e., they block and conduct in both directions); likewise, the components of all phases match and are ideal.

1.1 Characterization of the Switch

Unlike many dc converters, which have only one double-throw switch, most polyphase ac converters contain two or more multiple-throw switches. Ac structures are thus more difficult to comprehend unless their switches are characterized in a systematic manner. Hence, this section is dedicated to the specification of a switch. To start, "switch" in this study is *not* used interchangeably for "transistor" as in the literature; instead, it simply refers to the device described below.

As is delineated in Fig. 1.1, an *N-throw switch* consists of N *throws* that connect *pole* w to terminals 1, ..., k, ..., and N in each switching period. The operation of each throw is specified by the *switching function* d_{wk}^*, where asterisk (*) denotes switching function, which is one when the throw is closed and zero when the throw is open; the set of switching functions for the switch of Fig. 1.1 is illustrated in Fig. 1.2. A switch thus satisfies two constraints: only *one* switching function is high, and all switching functions must add up to *one* at any instant. The first constraint means that the position of the *pole* is always *determinate* while that of a *throw* is *not*. In other words, the pole is always connected to one of the N throws while a throw may be attached to nowhere. Hence, the open end of an inductor, whose current must flow somewhere, must be assigned to the pole, not a throw, of a switch.

The average of the switching function d_{wk}^* over each period T_s is the *duty ratio* d_{wk}. If d_{wk} varies at a frequency sufficiently slower than the switching frequency, it can be approximated to the *continuous low-frequency* component of the "quasi-periodic (at period T_s)" d_{wk}^*. In accordance with

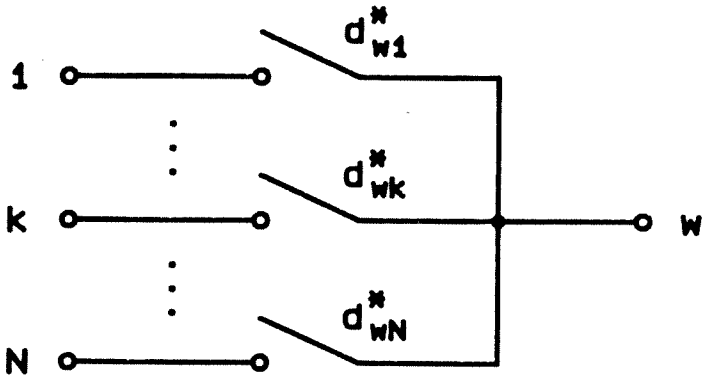


Fig. 1.1 N-throw switch connecting pole w to positions 1,..., k,..., N.

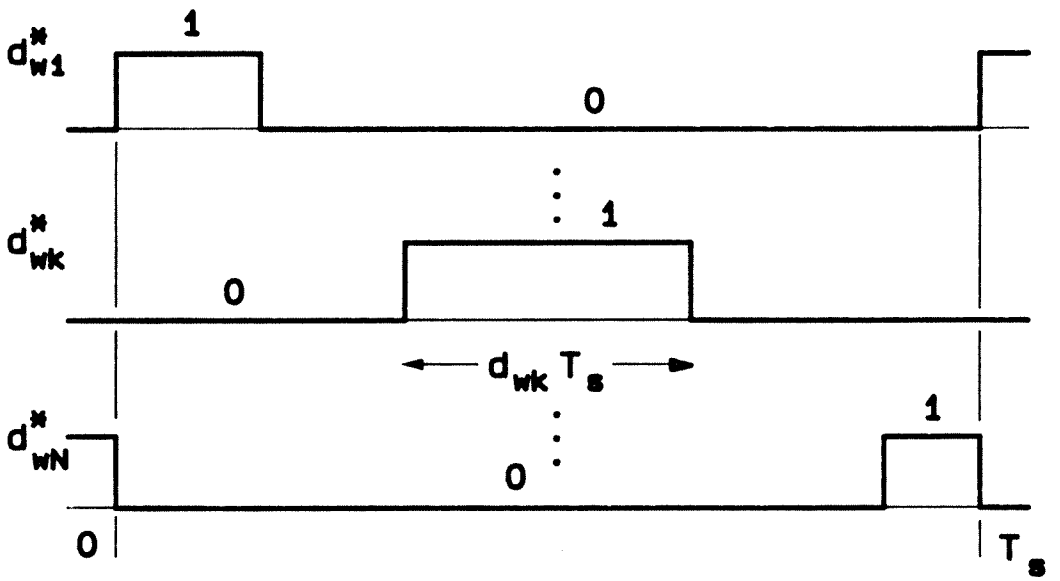


Fig. 1.2 Switching function d_{wk}^* and duty ratio d_{wk}.

the second constraint in the previous paragraph, all duty ratios of the same switch should add up to one:

$$\sum_{k=1}^{N} d_{wk} = 1 \tag{1.1}$$

Therefore, at most $(N-1)$ of the N throws can be controlled independently.

In summary, a multiple-throw switch can be characterized by its *switching functions* and *duty ratios*. The switching function, either one or zero, describes the on or off state of each throw. The duty ratio is the average of the switching function over a switching period; there are $(N-1)$ independent duty ratios for an N-throw switch.

1.2 Describing Equations of Fast-Switching PWM Converters

This section first obtains the *switching equations* of a *general* switched network, which can be of resonance, PWM, or any other type. The restriction to PWM is then invoked to derive the *describing equations* of fast-switching PWM converters.

As an example, consider the M-phase boost inverter illustrated in Fig. 1.3. This circuit consists of two M-throw switches that invert the inductor current, supplied by the dc source, into polyphase currents driving an M-phase RC load. Note that the switch arrangement is classified as *two M-throw*, not *M double-throw*, switches so that the current in the inductor always has some place to flow to. Correct classification is essential in later assignment of modulations to the throws. States in the network are the inductor current i^* and capacitor voltage $v_w{}^*$, where asterisk (*) implies an exact value and $1 \le w \le M$.

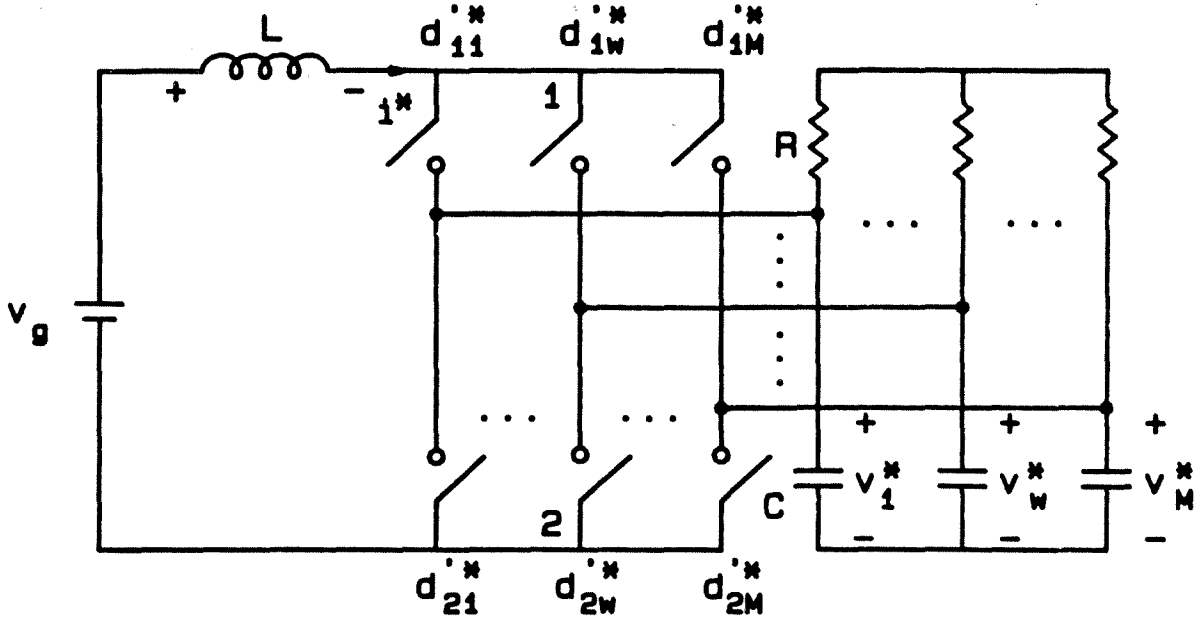


Fig. 1.3 M-phase boost inverter with two M-throw switches pulse-width-modulated by sinusoidal functions.

If the common of the capacitors is selected as reference point, then the voltage at the upper pole is

$$\sum_{w=1}^{M} d'_{1w}{}^{*} v_w{}^{*}$$

and at the lower pole is

$$\sum_{w=1}^{M} d'_{2w}{}^{*} v_w{}^{*}$$

where prime (') is used on functions of the switches at the output side of a topology. Note that the above have been obtained *without* any knowledge of *switching details*. Therefore, this step is applicable to any topology that consists of switches and reactive elements, regardless of how the switches

are operated.

Application of Kirchhoff's voltage law around the loop containing the source, inductor, and switches yields the following *exact* state-space *switching equation* for the inductor:

$$L\dot{i}^* = -\sum_{w=1}^{M}(d'_{1w}{}^* - d'_{2w}{}^*)v_w{}^* + v_g \tag{1.2}$$

where $\dot{i}^*$ means "the first time derivative of i^*." Note that this result is independent of the choice of reference point. The analogous equation for the capacitor is

$$C\dot{v}_w{}^* = (d'_{1w}{}^* - d'_{2w}{}^*)i^* - \frac{1}{R}(v_w{}^* - \frac{1}{M}\sum_{w=1}^{M} v_w{}^*) , \quad 1 \le w \le M \tag{1.3}$$

In the above, the inductor current is switched into the capacitor via the first term, and the resistor current is drawn out by the second term.

In general, a switched-mode converter contains S switches, each of T_m throws, where $1 \le m \le S$. The number of *controllable* throws T_C is then

$$T_C = \sum_{m=1}^{S}(T_m - 1) \tag{1.4}$$

If T_C independent switching functions $d_n{}^*$ (just for compactness, only one, instead of two, subscript is used to identify each switching function), where $1 \le n \le T_C$, are assigned to these T_C independent throws, the *exact* state-space *switching equation* of an ideal converter can be expressed as

$$\mathbf{P}\dot{\mathbf{x}}^* = \sum_{n=0}^{T_C} d_n{}^*(\mathbf{A}_n\mathbf{x}^* + \mathbf{B}_n\mathbf{u}) \tag{1.5}$$

where

$$d_0^* = 1 \tag{1.6}$$

$\mathbf{x}^*$ is the $Q\times1$ state vector (denoted by boldface),

$\mathbf{P}$ is the $Q\times Q$ LC matrix (denoted by boldface),

$\mathbf{A}_n$ is the $Q\times Q$ constant matrix,

$\mathbf{u}$ is the $R\times1$ source vector,

$\mathbf{B}_n$ is the $Q\times R$ constant matrix,

and the terms with subscript 0 account for the dependent throws in the topology. Equations (1.2) and (1.3) can be cast in the form of Eq. (1.5) if desired.

Equation (1.5) is *exact* and *general* in the sense that no particular mode of control has been specified for the switching function d_n^*. It is difficult to analyze because the switching functions are only piecewise continuous. Nevertheless, it does reduce to a manipulable form for those converters of the *fast-switching PWM* family.

By definition, the sources and duty ratios of a fast-switching PWM converter vary at a rate much slower than the switching frequency. By design, the LC corners of the circuit, usually compatible with the frequencies of the source and duty ratio vectors, are also placed well below the switching frequency to minimize the switching ripple. Thus, a fast-switching PWM topology receives slowly-varying inputs, further restricted to being dc or sinusoidal in this thesis, to generate slowly-varying outputs, expected to be dc or sinusoidal with a small amount of high-frequency ripple. Under these conditions, the modeling theorems in [1], proved under the assumption of negligible filter values, still apply. Therefore, the

switching function d_n^* can be approximated by its duty ratio d_n ; and the exact state vector $\mathbf{x}^*$ by the principal component $\mathbf{x}$ of its "Fourier series." Within a modeling bandwidth sufficiently lower than the switching frequency and a modeling error sufficiently small, then, the useful, low-frequency variables of the system represented by Eq. (1.5) are related by the following *describing equation*:

$$\mathbf{P}\dot{\mathbf{x}} = \sum_{n=0}^{T_C} d_n(\mathbf{A}_n\mathbf{x} + \mathbf{B}_n\mathbf{u}) \tag{1.7}$$

where asterisks have been dropped in going from the exact switching to the low-frequency describing equation. A more compact form of Eq. (1.7) is

$$\mathbf{P}\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{1.8}$$

where

$$\mathbf{A} = \sum_{n=0}^{T_C} d_n\mathbf{A}_n \quad \text{and} \quad \mathbf{B} = \sum_{n=0}^{T_C} d_n\mathbf{B}_n \tag{1.9a,b}$$

A comparison of Eqs. (1.5) and (1.7) reveals that they are similar in form, the only difference being the asterisks in the former. Therefore, the two steps are essentially one, and the describing equation can be obtained expediently by inspection of the topology and use of basic definitions of circuit elements, Kirchhoff's laws, principle of superposition, and so on. Note, however, that the describing equation is *continuous* and, hence, more tractable than the switching equation.

It is obvious from the describing equation that only ***duty ratios***, not exact switching details, influence the low-frequency behavior of fast-switching converters. Since many distinct switching functions may share the same

duty ratio, there is no unique switching strategy to synthesize a given set of outputs. Topologically independent switches in a fast-switching network are thus also *functionally independent* in the sense that each of them requires simply its own duty ratios and does not have to be synchronized with the other switches. Hence, one more advantage of fast switching over slow switching is the infinite number of flexible drive policies available.

Now that the describing equation technique has been presented, it is proper to review the modeling history of switched-mode structures. Describing equation is actually a classical concept introduced to approximate the characteristics of nonlinear devices and systems. It has been applied to model slow-switching inverters [10], rectifiers, and cycloconverters [24]. Recently, along with the advent of fast-switching technology, the describing equation method has been extended to and, for the first time, justified mathematically in the *frequency* domain for fast-switching converters with negligible filter values in [1]. The results in [1] are simply extended in this thesis to include the effect of reactive components difficult to ignore in most practical designs.

The transition of the describing equation technique from slow switching to fast switching, however, has not been continuous. In between, state-space-averaging [2] has been proposed to treat dc and other simple converters. Its derivation is based on low-frequency approximation of the transition matrix in the *time* domain. When state-space-averaging is used, all possible switched topologies are first enumerated and assigned *topological duty ratios*. Linear equations of these topologies are then weighted by their respective topological duty ratios and summed up to provide the averaged state-space equation. State-space averaging clarifies the operation of simple

dc converters with only a few switched topologies repeated in every switching cycle. Because of its detailed topological description, however, it is not used here to model complex ac converters that have a large number of throws and, hence, switched networks. There are just so many of these switched circuits to enumerate and more-than-necessary topological duty ratios to consider, the *number* and *type* of which keep on varying from one switching period to another while the duty ratios are modulated. Describing equation escapes all these problems and, hence, is the proper modeling approach to reinstate.

A special case of Eq. (1.8) is the describing equations of Eqs. (1.2) and (1.3) for the boost inverter; the corresponding vectors and matrices are:

$$\mathbf{P} = \begin{bmatrix} L & \mathbf{o}_M^T \\ \mathbf{o}_M & C\mathbf{I}_M \end{bmatrix}, \qquad \mathbf{x} = \begin{bmatrix} i \\ [v_w] \end{bmatrix} \tag{1.10a,b}$$

where $\mathbf{I}_M$ is the $M \times M$ unity matrix, $\mathbf{o}_M$ is the $M \times 1$ zero vector, and $1 \leq w \leq M$;

$$\mathbf{A} = \begin{bmatrix} 0 & -[d_w']^T \\ [d_w'] & 1/R\,[1/M - \delta_{wz}] \end{bmatrix}, \qquad \mathbf{B} = \begin{bmatrix} 1 \\ \mathbf{o}_M \end{bmatrix} \tag{1.10c,d}$$

where δ_{wz} is 1 when $w = z$ and is 0 otherwise; and

$$\mathbf{u} = v_g \tag{1.10e}$$

In the above, d_w' is the *effective duty ratio* and is related to the duty ratios

of the switching functions d'^{*}_{1w} and d'^{*}_{2w} by

$$d'_w = d'_{1w} - d'_{2w} \tag{1.11}$$

The performance of the inverter depends on what is assigned to d'_w or d'_{1w} and d'_{2w}. In this thesis, only easy-to-synthesize *sinusoidal* functions are considered; in this chapter, they are restricted further to being *continuous*.

In general, then, the duty ratio of each throw consists of a sinusoidal modulation and a dc component sufficiently large to make the duty ratio positive. Since the two switches are topologically independent, they can be modulated by *numerous* sets of balanced polyphase sinusoids that have independent amplitudes and phases:

$$d'_{kw} = \frac{1}{M} + \frac{d'_{mk}}{M} \cos\left[\, \theta'_k - (w-1)\,\frac{2\pi}{M} \,\right] \tag{1.12}$$

where

$$\theta'_k = \int_0^t \omega'(\tau)\,d\tau + \varphi'_k \,, \qquad d'_{mk} \le 1 \tag{1.13a,b}$$

for

$$k = 1,2 \qquad \text{and} \qquad 1 \le w \le M \tag{1.13c,d}$$

Note that this kind of duty ratio assignment allows all duty ratios of one switch to sum up to one. In the above, $\frac{d'_{mk}}{M}$ is the *instantaneous modulation amplitude*, and ω' the *instantaneous modulation frequency*. The frequency can be any real number, where a negative frequency reverses the phase sequence.

Out of different selections of d'_{1w} and d'_{2w}, the one that maximizes the effective duty ratio should be chosen. An efficient d'_w results when d'_{1w} and d'_{2w} have equal amplitudes and opposite phases and can be expressed as

$$d'_w = \frac{2d'_m}{M} \cos\left[\theta' - (w-1)\frac{2\pi}{M}\right] \tag{1.14}$$

where

$$\theta' = \int_0^t \omega'(\tau)d\tau \qquad \text{and} \qquad d'_m \leq 1 \tag{1.15a,b}$$

Again, this is just one choice of d'_w; other interesting ones are discussed later.

To recap, *low-frequency* components of the inputs and outputs of a fast-switching PWM converter are related by the *describing equations* of the circuit. These equations identify the independent *duty ratios* of the switches as control variables. Therefore, the performance of the converter depends on duty ratios, not different combinations of switched networks, if all circuit parameters vary sufficiently slower than the switching frequency.

1.3 Transformation

The describing equations written in the ordinary (or stationary or "abc") frame of reference may contain constant, if the converter is dc, or time-varying, if the converter is ac, duty ratios. Since a system of equations with constant coefficients is easier to analyze, especially dynamically, with standard techniques, it is beneficial to transform an ac system to an equivalent *dc* one whenever possible. With the "abc-ofb" transformation

introduced below, the existence of the dc equivalent also means that the ac converter possesses ideal (i.e., dc or sinusoidal) solutions.

A variety of transformations exist to convert a set of balanced sinusoids into its dc equivalent [23]. The one chosen here is the complex abc-ofb transformation (Appendix B). A complex transformation is preferred to a real one because the former allows the model of a converter using only *one* circuit while the latter requires *two* circuits coupled through dependent generators. Furthermore, the complex model is symmetrical while the real one is not. A result of real transformation frequently found in the literature is the dq equivalent circuit of an ac machine, composed of one network on the d-axis and another on the q-axis.

In general, the describing equation of a fast-switching PWM converter in one reference frame - abc, for instance - takes the form

$$\mathbf{P}\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{1.16}$$

Under the transformation

$$\mathbf{x} = \tilde{\mathbf{T}}\tilde{\mathbf{x}} \qquad or \qquad \tilde{\mathbf{x}} = \tilde{\mathbf{T}}^{-1}\mathbf{x} \tag{1.17a,b}$$

where tilde ($\tilde{}$) denotes a transformed or complex variable, Eq. (1.16) becomes

$$\tilde{\mathbf{P}}\dot{\tilde{\mathbf{x}}} = \tilde{\mathbf{A}}\tilde{\mathbf{x}} + \tilde{\mathbf{B}}\tilde{\mathbf{u}} \tag{1.18a}$$

or, to highlight control parameters:

$$\tilde{\mathbf{P}}\dot{\tilde{\mathbf{x}}} = \sum_{m=0}^{T_T} d_{Tm}(\tilde{\mathbf{A}}_m\tilde{\mathbf{x}} + \tilde{\mathbf{B}}_m\tilde{\mathbf{u}}) \tag{1.18b}$$

where

$$\tilde{\mathbf{A}} = \tilde{\mathbf{T}}^{-1}\mathbf{A}\tilde{\mathbf{T}} - \tilde{\mathbf{T}}^{-1}\mathbf{P}\dot{\tilde{\mathbf{T}}}\,, \qquad \tilde{\mathbf{P}} = \tilde{\mathbf{T}}^{-1}\mathbf{P}\tilde{\mathbf{T}} \tag{1.19a,b}$$

$$\tilde{\mathbf{B}}\tilde{\mathbf{u}} = \tilde{\mathbf{T}}^{-1}\mathbf{B}\mathbf{u}\,, \quad \text{and} \qquad d_{T0} = 1 \tag{1.19c,d}$$

In Eq. (1.18b), T_T is the number of independent transformed controls d_{Tm} and is generally less than or equal to the number of independent throws T_C. The transformed control vector containing d_{Tm} is the transformation of the duty ratio vector containing d_n by $\tilde{\mathbf{T}}$; it is related to the transformed state vector $\tilde{\mathbf{x}}$ via $\tilde{\mathbf{A}}_m$ and the transformed source vector $\tilde{\mathbf{u}}$ via $\tilde{\mathbf{B}}_m$.

As an example of complex transformation, consider again the boost inverter characterized by Eqs. (1.10) through (1.15). If the topology is ideal, its inductor current is dc and its capacitor voltages sinusoidal. Therefore, the transformation takes the form

$$\tilde{\mathbf{T}} = \begin{bmatrix} 1 & \mathbf{o}_M^T \\ \mathbf{o}_M & \tilde{\mathbf{T}}_v \end{bmatrix} \tag{1.20}$$

Note that $\tilde{\mathbf{T}}$ consists of two smaller transformations that act separately on the inductor and capacitor states. The first one is a unity transformation that passes the inductor current intact to the new frame of reference. The second one is the M-phase abc-ofb transformation, Eqs. (B.2) and (B.3), that converts the real voltage vector $[v_w]$ in the stationary (abc) frame of reference to the complex vector

$$[\; v_0 \;\; \tilde{v}_f \;\; \tilde{v}_3 \;\; \cdots \;\; \tilde{v}_{M-1} \;\; \tilde{v}_b \;]^T$$

in the rotating (ofb) coordinate system.

Substitution of Eqs. (1.10) through (1.15) and Eq. (1.20) into Eq. (1.19) results in

$$C\dot{v}_0 = 0 \tag{1.21a}$$

and

$$C\dot{\tilde{v}}_w = -\frac{\tilde{v}_w}{R}, \qquad 3 \le w \le M-1 \tag{1.21b}$$

The trivial relationship in Eq. (1.21a) suggests that v_0 is indeterminate, i.e., all phase voltages may contain equal arbitrary dc offset components. These components, however, do not deliver any power because their differentials, seen by the load, are always zero. In practical circuits, the arbitrariness can be fixed to any known voltage by pulling the outputs to a dc level through large resistors. If this is not done, the leakage resistance across the capacitor forces v_0 to zero.

The 3^{rd} through $(M-1)^{th}$ capacitor states are also trivial, as is evident from Eq. (1.21b). Unlike v_0, they are identically zero under all conditions. Therefore, they, as well as v_0, are ignored in the remainder of the discussion.

The only significant capacitor voltages that remain are the backward phasor $\tilde{v}_b$, proportional to the phasor characterizing the first capacitor voltage, and the forward phasor $\tilde{v}_f$, complex conjugate of $\tilde{v}_b$. The order of the balanced polyphase states thus reduces from M^{th} to 2^{nd}, an important simplification found whenever the states constitute a balanced polyphase set. Therefore, ***all converters with three or more balanced phases are reducible to a two-phase equivalent.*** An analogous statement is well-known in the theory of ac machines, namely, all machines with three or

more windings on the stator or rotor are equivalent to the two-phase machine. Owing to this reducibility of polyphase systems, only the simple two-phase circuit needs be considered in place of much more complicated M-phase topologies, where M can go to infinity. The realization of two-phase converters to be coupled to two-phase motors or generators is treated in later chapters.

After the elimination of $(M-2)$ capacitor states, the boost inverter becomes third-order: one for the inductor current and two for the capacitor voltages. If $\tilde{\mathbf{T}}_v$ is in-phase with the effective duty ratio d_w', the reduced matrix equation can be manipulated into

$$\mathbf{P}_r \dot{\tilde{\mathbf{x}}}_r = (\mathbf{A}_r + \mathbf{A}_d d_e' + \mathbf{A}_\omega j\omega') \tilde{\mathbf{x}}_r + \mathbf{B}_d v_g \tag{1.22}$$

where

$$d_e' = \frac{\sqrt{M}}{2} \frac{2d_m'}{M} = \frac{d_m'}{\sqrt{M}} \tag{1.23}$$

is the *transformed duty ratio*, the transformation of the effective duty ratio d_w' by $\tilde{\mathbf{T}}_v$:

$$\mathbf{P}_r = \begin{bmatrix} L & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & C \end{bmatrix}, \quad \tilde{\mathbf{x}}_r = \begin{bmatrix} i \\ \tilde{v}_f \\ \tilde{v}_b \end{bmatrix}, \quad \mathbf{A}_r = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -1/R & 0 \\ 0 & 0 & -1/R \end{bmatrix} \tag{1.24a,b,c}$$

$$\mathbf{A}_d = \begin{bmatrix} 0 & -1 & -1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}, \quad \mathbf{A}_\omega = \begin{bmatrix} 0 & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & -C \end{bmatrix}, \quad \mathbf{B}_d = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{1.24d,e,f}$$

In this formulation, all matrices are real even though the original $\tilde{\mathbf{A}}$ and $\tilde{\mathbf{B}}\tilde{\mathbf{u}}$ are complex. Resistance is contained in $\mathbf{A}_r$; capacitance and inductance, $\mathbf{A}_\omega$; constants describing the duty ratios, $\mathbf{A}_d$; and constants related to the

source, $\mathbf{B}_d$.

All control parameters are placed outside the matrices so that they can be identified easily as d_e', ω', and v_g, where lower case signifies an instantaneous value. Therefore, rotating coordinates emphasize what is not apparent in stationary axes, namely, only the amplitude and frequency of duty ratio modulations influence the outcome and, hence, are the ones to control. Analysis and design problems are thus simple because both d_e' and ω' are *constant* under steady-state condition. Note that d_e' is a control factor peculiar to fast-switching PWM and does not exist in low-frequency drives.

In retrospect, polyphase converters with dc or sinusoidal waveforms in the abc (or stationary) reference frame can be modeled by differential equations with *constant* coefficients in the ofb (or rotating) coordinate system. One method to transform from the abc to the ofb representation is the complex abc-ofb transformation. This transformation reduces the number of balanced polyphase sinusoidal states in the stationary axes from larger-than-two to just *two* and allows the model of converters with an *arbitrary* number of balanced phases by the *two*-phase converter. It replaces sinusoidal duty ratio modulations by their amplitude and frequency, dc under steady-state condition, and sinusoidal outputs their amplitude and phase.

1.4 Steady-State Analysis

Under steady-state condition, the inputs in Eq. (1.18b) take on the *dc* values D_{Tm} and $\tilde{\mathbf{U}}$, where upper case indicates a steady-state variable. The corresponding output vector $\tilde{\mathbf{X}}$ is also dc and is computed by letting its derivative be zero in Eq. (1.18b):

$$\tilde{\mathbf{X}} = -\left[\sum_{m=0}^{T_T} D_{Tm}\tilde{\mathbf{A}}_m\right]^{-1}\left[\sum_{m=0}^{T_T} D_{Tm}\tilde{\mathbf{B}}_m\right]\tilde{\mathbf{U}} \tag{1.25}$$

An application of this result is demonstrated below for the boost inverter.

Steady-state results of the boost inverter are found by replacement of d_e', ω', v_g, and $\dot{\tilde{\mathbf{x}}}_r$ in Eq. (1.22) by D_e', Ω', V_g, and 0, respectively, and solving for $\tilde{\mathbf{X}}_r$ from the corresponding algebraic equation. The formula for the inductor current is

$$I = \frac{V_g}{2D_e'^2 R}\left[1 + \left(\frac{\Omega'}{\omega_p}\right)^2\right] \tag{1.26}$$

where

$$\omega_p = \frac{1}{RC} \tag{1.27}$$

Since the transformed current is *real*, the actual current in the inductor is purely *dc*. This result confirms the ideality of the topology: dc input current is the only way to guarantee constant instantaneous power flow and, hence, promise sinusoidal outputs.

The backward voltage phasor can be proved to be

$$\tilde{V}_b = \frac{V_g}{2D_e'} \left[1 - j \frac{\Omega'}{\omega_p} \right] \tag{1.28}$$

Unlike the inductor current, the capacitor voltage in the ofb frame is *complex* to signify that phase outputs in the abc axes are indeed *sinusoidal*. The true capacitor voltage v_w can be reconstructed from Eq. (1.28):

$$v_w = V \cos[\Omega' t - \Phi_v - (w-1) \frac{2\pi}{M}] \tag{1.29}$$

where, from Appendix B:

$$V e^{-j\Phi_v} = \frac{2}{\sqrt{M}} \tilde{V}_b = \frac{V_g}{D_m'} \left[1 - j \frac{\Omega'}{\omega_p} \right] \tag{1.30}$$

It is apparent from Eq. (1.30) that the output amplitude is always higher than the input dc voltage; the inverter thus deserves its name. Note that unlike dc converters, ac converters depend on circuit impedances even under steady-state condition - L is the only element absent from the above results since its impedance is zero. Therefore, an ac converter can be classified neither as a voltage nor as a current source. The boost topology, however, does belong to the "current-fed" family because the output is fed by a dc current converted from the voltage source by the inductor.

The very existence of ideal solutions, Eqs. (1.26) through (1.30), for a *nonlinear* structure like the boost inverter, Eqs. (1.22) through (1.24), should not be taken for granted. Most ac topologies produce low-frequency distortion because of the nonlinearity inherent in switched-mode converters [20] and, hence, do not satisfy the objectives of this thesis. The recognition of the remaining few ideal switching networks is thus an important task to be pursued in later chapters.

In review, *steady-state* solutions in the rotating coordinates are provided by homogeneous algebraic equations relating constant inputs to constant outputs. *Real* results correspond to *dc* values while *complex* results represent balanced polyphase *sinusoidal* states in the stationary reference frame.

1.5 Small-Signal Dynamics

This section examines the dynamics introduced by filters used to attenuate the switching ripple in switched-mode converters. Because the converter is generally nonlinear (Eq. (1.22), for instance), dynamic study is restricted to only the *small-signal* sense. In other words, it predicts the responses of the system to small perturbations around a quiescent operating point. The ofb frame of reference provides a perfect medium for perturbed dynamics since the equations of the network already have constant coefficients there. Thus, there is no need to invoke the "quasi-dc" approximation [28] that has limited accuracy and allows only inefficient worst-case designs.

Let the input and output in Eq. (1.18b) consist of a steady-state and a perturbed component:

$$\tilde{\mathbf{x}} = \tilde{\mathbf{X}} + \hat{\tilde{\mathbf{x}}}\ , \quad d_{\mathcal{T}m} = D_{\mathcal{T}m} + \hat{d}_{\mathcal{T}m}\ , \text{ and } \tilde{\mathbf{u}} = \tilde{\mathbf{U}} + \hat{\tilde{\mathbf{u}}} \qquad (1.31a,b,c)$$

where caret implies small-signal perturbation. Substitution of these relations into Eq. (1.18b) and neglect of the resulting steady-state and second-order terms then yield the following response for the state vector in the Laplace domain:

$$\hat{\tilde{\mathbf{x}}}(s) = (s\tilde{\mathbf{P}} - \sum_{m=0}^{T_T} D_{Tm}\tilde{\mathbf{A}}_m)^{-1}[\sum_{m=0}^{T_T}(\tilde{\mathbf{A}}_m\tilde{\mathbf{X}} + \tilde{\mathbf{B}}_m\tilde{\mathbf{U}})\hat{d}_{Tm}(s) + (\sum_{m=0}^{T_T} D_{Tm}\tilde{\mathbf{B}}_m)\hat{\tilde{\mathbf{u}}}(s)] \tag{1.32}$$

This state vector, however, is generally complex. Therefore, it is accompanied by a state-to-output equation that changes states into measurable real outputs:

$$\hat{\mathbf{y}}(s) = \tilde{\mathbf{C}}\hat{\tilde{\mathbf{x}}}(s) + \tilde{\mathbf{D}}_d\hat{\mathbf{d}}(s) + \tilde{\mathbf{D}}_u\hat{\tilde{\mathbf{u}}}(s) \tag{1.33}$$

For the boost inverter of Eq. (1.22), the perturbed state vector $\hat{\tilde{\mathbf{x}}}_r$ is expressed as a function of the excitations $\hat{d}_e'$, $\hat{\omega}'$, and $\hat{v}_g$ according to

$$\hat{\tilde{\mathbf{x}}}_r(s) = (s\mathbf{P}_r - \tilde{\mathbf{A}}_o)^{-1}[\mathbf{A}_d\tilde{\mathbf{X}}_r\hat{d}_e'(s) + \mathbf{A}_\omega\tilde{\mathbf{X}}_r j\hat{\omega}'(s) + \mathbf{B}_d\hat{v}_g(s)] \tag{1.34}$$

where

$$\hat{\tilde{\mathbf{x}}}_r(s) = \begin{bmatrix} \hat{i}(s) \\ \hat{\tilde{v}}_f(s) \\ \hat{\tilde{v}}_b(s) \end{bmatrix}, \qquad \tilde{\mathbf{X}}_r = \begin{bmatrix} I \\ \tilde{V}_f \\ \tilde{V}_b \end{bmatrix} \tag{1.35a,b}$$

and

$$\tilde{\mathbf{A}}_o = \mathbf{A}_r + D_e'\mathbf{A}_d + j\Omega'\mathbf{A}_\omega \tag{1.35c}$$

In the above, the current can be used directly as an output because it is already real. The voltages, however, are complex and need be converted into their real equivalents before they can be measured by conventional setups.

The real representations of a phasor are its real and imaginary components or its amplitude and phase:

$$\tilde{v}_b(t) = v_r(t) + j\,v_i(t) = v_m(t)\,e^{-j\varphi_v(t)} \tag{1.36}$$

From this equation, the output vector $\hat{\mathbf{y}}(s)$ can be related to the state

vector $\hat{\tilde{\mathbf{x}}}_r(s)$ by

$$\hat{\mathbf{y}}(s) = \tilde{\mathbf{C}}\hat{\tilde{\mathbf{x}}}_r(s) \tag{1.37}$$

where

$$\hat{\mathbf{y}}(s) = \begin{bmatrix} \hat{\imath}(s) \\ \hat{v}_r(s) \\ \hat{v}_i(s) \\ \hat{v}_m(s) \end{bmatrix} \quad \text{and} \quad \tilde{\mathbf{C}} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1/2 & 1/2 \\ 0 & j/2 & -j/2 \\ 0 & \tilde{V}_b/2V_m & \tilde{V}_f/2V_m \end{bmatrix} \tag{1.38a,b}$$

Equations (1.34) and (1.37) are used together to compute the control-to-output and line-to-output frequency responses. For instance, if only one input is perturbed at a time,

$$\frac{\hat{v}_m}{\hat{d}'_e} = -\frac{V_g}{2D_e'^2}\left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]^{\frac{1}{2}} \frac{\left[1-\frac{s}{\omega_z}\right]\left[1+\frac{s}{\omega_{z1}}\right]}{K(s)} \tag{1.39a}$$

$$\frac{\hat{\imath}}{\hat{\omega}'} = \frac{V_g}{D_e'^2 R}\frac{\Omega'}{\omega_p{}^2}\frac{1+\frac{s}{\omega_{z2}}}{K(s)} \tag{1.39b}$$

or

$$\frac{\hat{v}_r}{\hat{v}_g} = \frac{1}{2D'_e}\frac{1+\frac{s}{\omega_p}}{K(s)} \tag{1.39c}$$

where

$$\omega_p = \frac{1}{RC} \quad , \qquad \omega_z = \frac{2D_e'^2 R}{\left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]L} \tag{1.40a,b}$$

$$\omega_{z1} = \left[1 + \left(\frac{\Omega'}{\omega_p}\right)^2\right]\omega_p \qquad \omega_{z2} = 2\omega_p \tag{1.40c,d}$$

and

$$K(s) = 1 + \left[RC + \frac{\Omega'^2 LC^2 R}{2D_e'^2} + \frac{L}{2D_e'^2 R}\right] s + \frac{LC}{D_e'^2} s^2 + \frac{LC^2 R}{2D_e'^2} s^3 \tag{1.41}$$

The denominator $K(s)$, common to all transfer functions, is proportional to the characteristic polynomial of $\tilde{\mathbf{A}}_0$. It emerges real amid all complex variable manipulations as the original system is realizable from real L, C, and R. It is of third order as expected. Since the topology is nonlinear, all dynamic corners are sensitive to the quiescent operating condition.

To summarize, dynamic analysis of switched-mode ac converters, both nonlinear and time-varying in the abc coordinates, can be studied conveniently in the ofb reference frame where the describing equations have constant coefficients. The nonlinearity is still there, but the system can be *linearized* by restriction of all perturbations to only small-signal. Equations have been developed to predict all control-to-output and line-to-output frequency responses. Dynamic corners are generally sensitive to steady-state parameters, such as modulation amplitude and frequency.

1.6 Canonical Model

The combination of steady-state (Eq. (1.25)) and perturbed (Eq. (1.32)) equations, or the dynamic equation without second-order terms, is the *linearized* system equation:

$$(s\tilde{\mathbf{P}} - \sum_{m=0}^{T_T} D_{Tm}\tilde{\mathbf{A}}_m)\tilde{\mathbf{x}}(s) = \sum_{m=0}^{T_T} (\tilde{\mathbf{A}}_m\tilde{\mathbf{X}} + \tilde{\mathbf{B}}_m\tilde{\mathbf{U}})\hat{d}_{Tm}(s) + (\sum_{m=0}^{T_T} D_{Tm}\tilde{\mathbf{B}}_m)\tilde{\mathbf{u}}(s) \tag{1.42}$$

The pictorial representation of this linearized equation is the *canonical model*, a powerful tool that not only predicts steady-state and dynamic performances, but also illuminates the interaction between the input, load, filters, and switches.

Since the rotating coordinates have been more versatile than the stationary ones in the two previous analyses, they are retained here to discuss the equivalent circuit. Again, in the rotating frame of reference, an ideal converter is described by differential equations with constant coefficients. In particular, the complex ofb axes promise a *single symmetrical* model, instead of two unsymmetrical coupled circuits as the real dq axes. Therefore, the ofb coordinates are the most convenient common ground for later comparison of topologies in all four areas of power electronics.

To be "canonical", the model should identify correctly the output variable, input variable, conversion function, and filter topology. The output variable is usually the output voltage phasor, and the input variable the source current phasor. The conversion function is the heart of the model: it portrays how the switches convert power from one form to another and what the accompanying steady-state gain is. The filter topology explains the effects of reactive elements on steady-state and dynamic results and, in doing so, clarifies the conversion function. A step-by-step procedure to cast the linearized equations into the canonical model is explained below for the boost inverter.

First, select the capacitor voltage phasor $\tilde{v}_b$ as the output and recall the linearized dynamic equation for this state:

$$[\frac{1}{R}+(s+j\Omega')C]\tilde{v}_b = D_e'i + I\hat{d}_e' - jC\tilde{V}_b\hat{\omega}' \tag{1.43}$$

Since no controlled generators are allowed at the output, the right-hand side of Eq. (1.43) is defined as an effective inductor current

$$\tilde{\imath} = D_e'i + I\hat{d}_e' - jC\tilde{V}_b\hat{\omega}' \tag{1.44}$$

so that $\tilde{v}_b$ now satisfies

$$[\frac{1}{R}+(s+j\Omega')C]\tilde{v}_b = \tilde{\imath} \tag{1.45}$$

The above relation between $\tilde{v}_b$ and $\tilde{\imath}$ suggests that the impedance in square brackets is the first element of the model, as is shown in Fig. 1.4. Substitution of Eq. (1.44) into the linearized equation for $\tilde{v}_f$, the complex conjugate of Eq. (1.43), yields

$$[\frac{1}{R}+(s-j\Omega')C]\tilde{v}_f = \tilde{\imath} + jC(\tilde{V}_b+\tilde{V}_f)\hat{\omega}' \tag{1.46}$$

Again, to push the controlled source by $\hat{\omega}'$ to the input side of the model requires the definition

$$\tilde{v}_f' = \tilde{v}_f - j\frac{V_g}{D_e'}\frac{RC\hat{\omega}'}{1+(s-j\Omega')RC} \tag{1.47}$$

Equation (1.46) then becomes

$$[\frac{1}{R}+(s-j\Omega')C]\tilde{v}_f' = \tilde{\imath} \tag{1.48}$$

The impedance in Eq. (1.48) relating $\tilde{v}_f'$ and $\tilde{\imath}$ thus becomes the second component of the model in Fig. 1.4.

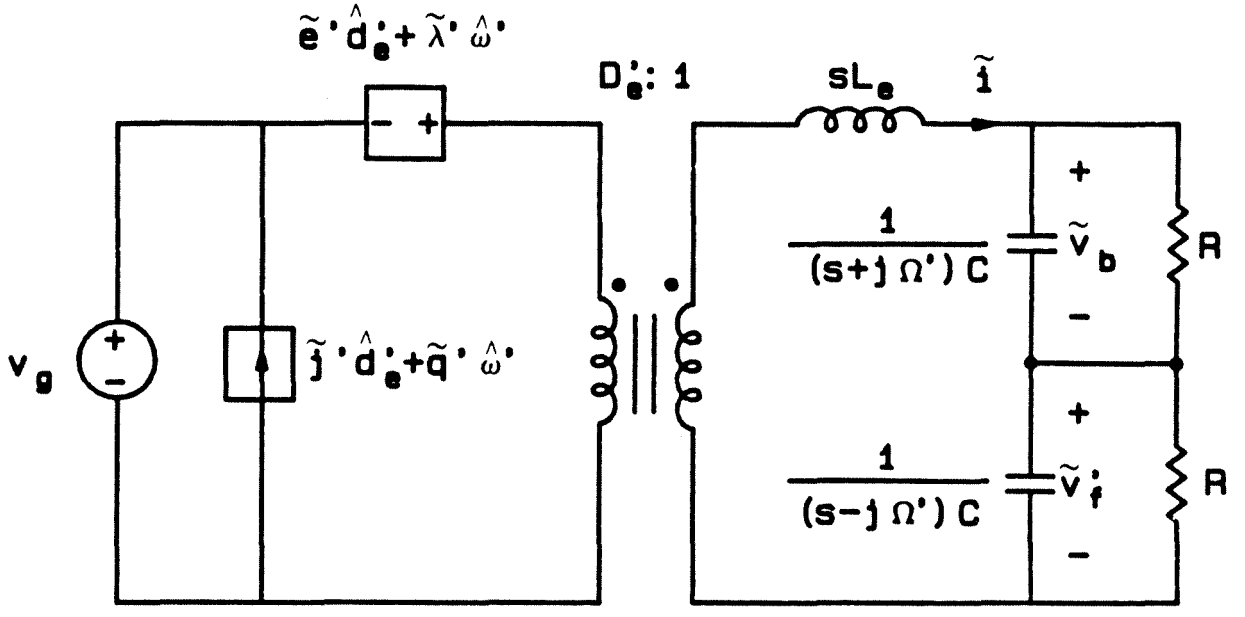


Fig. 1.4 Linearized, continuous, and time-invariant canonical model of the boost inverter.

From the previous steps, it is clear that the true inductor current i and forward capacitor voltage $\tilde{v}_f$ have to be sacrificed so that the physical output $\tilde{v}_b$ is preserved as the model output *and* all controlled generators are eliminated at the output half of the model. Therefore, care must be taken *not* to interpret model states, except for the output, as converter states. The true states can be retrieved from the model via Eqs. (1.44) and (1.47).

There still remains the linearized equation of the inductor:

$$sL\,i = -D_e'\tilde{v}_b - D_e'\tilde{v}_f - (\tilde{V}_f + \tilde{V}_b)\,\hat{d}_e' + v_g \qquad (1.49)$$

Replacement of i and $\tilde{v}_f$ in the above by $\tilde{i}$ and $\tilde{v}_f$, respectively, and

manipulation of the resulting form to expose $\tilde{\imath}$, $\tilde{v}'_f$, $\tilde{v}_b$, and v_g give the following for the inductor in the model:

$$sL_e\tilde{\imath} = -\tilde{v}'_f - \tilde{v}_b + \frac{1}{D'_e}\left(\tilde{e}'\hat{d}'_e + \tilde{\lambda}'\hat{\omega}' + v_g\right) \tag{1.50}$$

where

$$L_e = \frac{L}{D'^2_e}, \qquad \tilde{e}' = D'_e sL_e I - \frac{V_g}{D'_e} \tag{1.51a,b}$$

and

$$\tilde{\lambda}' = -j\,RC\left[\frac{V_g}{1+(s-j\,\Omega')RC} + D'_e\tilde{V}_b\,\frac{sL_e}{R}\right] \tag{1.51c}$$

Note that Eq. (1.50) automatically insures that the voltage source v_g in the model represents truthfully the actual dc supply, also v_g. At this stage, no more new current or voltage states can be defined. Nonetheless, the last term in this equation may be treated as the secondary voltage of a transformer whose turn ratio is the *inversion ratio* $\frac{1}{D'_e}$ and whose primary is fed by the source and dependent voltage generators inside the parentheses. The inductor, transformer, and voltage generators involved in Eq. (1.50) are illustrated in Fig. 1.4.

The one parameter that the procedure outlined above may not account for correctly is the *source current*. Actually, this current is irrelevant as long as the source is assumed to be ideal - this is why the modeling process ignores it completely in the first place. Nevertheless, the source current should be modeled properly so that the equivalent circuit is useful in the presence of source impedance.

From Fig. 1.4, the reflected current on the primary side of the transformer is

$$\frac{\tilde{i}}{D_e'} = i + \frac{I}{D_e'}\hat{d}_e' - \frac{jC\tilde{V}_b}{D_e'}\hat{\omega}' \tag{1.52}$$

Since the correct line current is only i, a controlled *current* generator must be inserted as shown in Fig. 1.4 to absorb the last two terms in the primary current. Thus,

$$\tilde{j}' = \frac{I}{D_e'} \qquad \text{and} \qquad \tilde{q}' = -j\frac{C\tilde{V}_b}{D_e'} \tag{1.53a,b}$$

The complete model thus characterizes faithfully both the output voltage and input current. It highlights the principal attributes of a power processor, namely, the control functions, conversion mechanism, and low-pass filters. Most importantly, it represents the nonlinear, switched, and time-varying converter by a *linear*, *continuous*, and *time-invariant* circuit.

In conclusion, *describing equation*, long used to study slow-switching drives and recently extended to model fast-switching converters, is adopted here as the generalized analysis technique. This method characterizes with a high degree of accuracy the *dynamic* relation between *duty ratios* and *low-frequency* components of the waveforms in fast-switching PWM converters with reactive elements. State-space describing differential equations can be obtained, by inspection, in the abc frame of reference and then transformed, by the abc-ofb transformation, to the ofb coordinates in which they have constant coefficients. The transformed equations are set to zero for *steady-state* solutions, perturbed for small-signal *dynamics*, and linearized for a linear, time-invariant, and continuous *canonical model*.

PART I

SWITCHED-MODE INVERSION

CHAPTER 2

REVIEW OF EXISTING INVERTERS

Many industrial applications, such as motor drives and uninterruptible power supplies, require the conversion of dc into ac power. This dc-to-ac power transformation is broadly called *inversion*, and the corresponding power processor the *inverter*. Although an inverter can have single-phase or balanced polyphase ac output, only the later type is considered in this thesis in accordance with the restriction of *constant instantaneous power flow* set forth in the Introduction. The terms "balanced polyphase" thus describe a set of two or more *sinusoidal* quantities that have the same amplitude and are displaced in phase by $\pm 90°$, for a two-phase (or semi-four-phase) system, or $\pm \frac{360°}{M}$, for an M (≥ 3)-phase system.

Inverters can be divided into three groups according to the ratio of their switching to output (or inversion) frequency. The "slow-switching" group, reviewed in Section 2.1, consists of inverters switched at the inversion frequency. Although these circuits, topologically ideal, are free from *nonlinear* distortion, they suffer from *switching* harmonics too close to the useful frequency to be filtered. The "medium-switching" group, treated in Section 2.2, consists of inverters switched in the order of a decade above the inversion frequency. Although the switching harmonics in these circuits start at a higher frequency, they are still not separated far enough from the desired component to be attenuated effectively by filters of reasonable size.

The "fast-switching" group, surveyed in Section 2.3, consists of inverters switched above two decades of the output frequency. Although most of these topologies suppress the *switching* ripple easily by small filters, they are not genuinely balanced polyphase and, hence, generate *nonlinear* distortion as troublesome as the switching noise in the slow-switching family.

2.1 Inverters Switched at Low Frequency

This section deals with inverters whose switching frequency is of the same order as, and often equal to, the output frequency. A great deal of operation fundamentals, harmonic analysis techniques, and design procedures for these inverters can be found in [6] and [26]. Recent advances in the inversion field on both theoretical and practical grounds have been edited in [7]. A survey of these and other documents in the literature suggests that the voltage-source, current-source, and, to a lesser extent, step-synthesis inverters are typical of the slow-switching category.

2.1.1 Voltage-Source Inverter

The voltage-source inverter [8] has been widely used as a variable-voltage, variable-frequency drive for ac machines. A three-phase topology simply consists of three double-throw switches permanently attached to the load, as is shown in Fig. 2.1a. In a practical circuit, each throw is realized by a pair of anti-parallel thyristor and diode ; and the variable voltage source, a phase-controlled rectifier followed by an LC filter.

The three independent switching functions associated with the switches are sketched in Fig. 2.1b. Recall that according to the convention established in Section 1.1, d_{21}^{*} is the switching function for the first throw

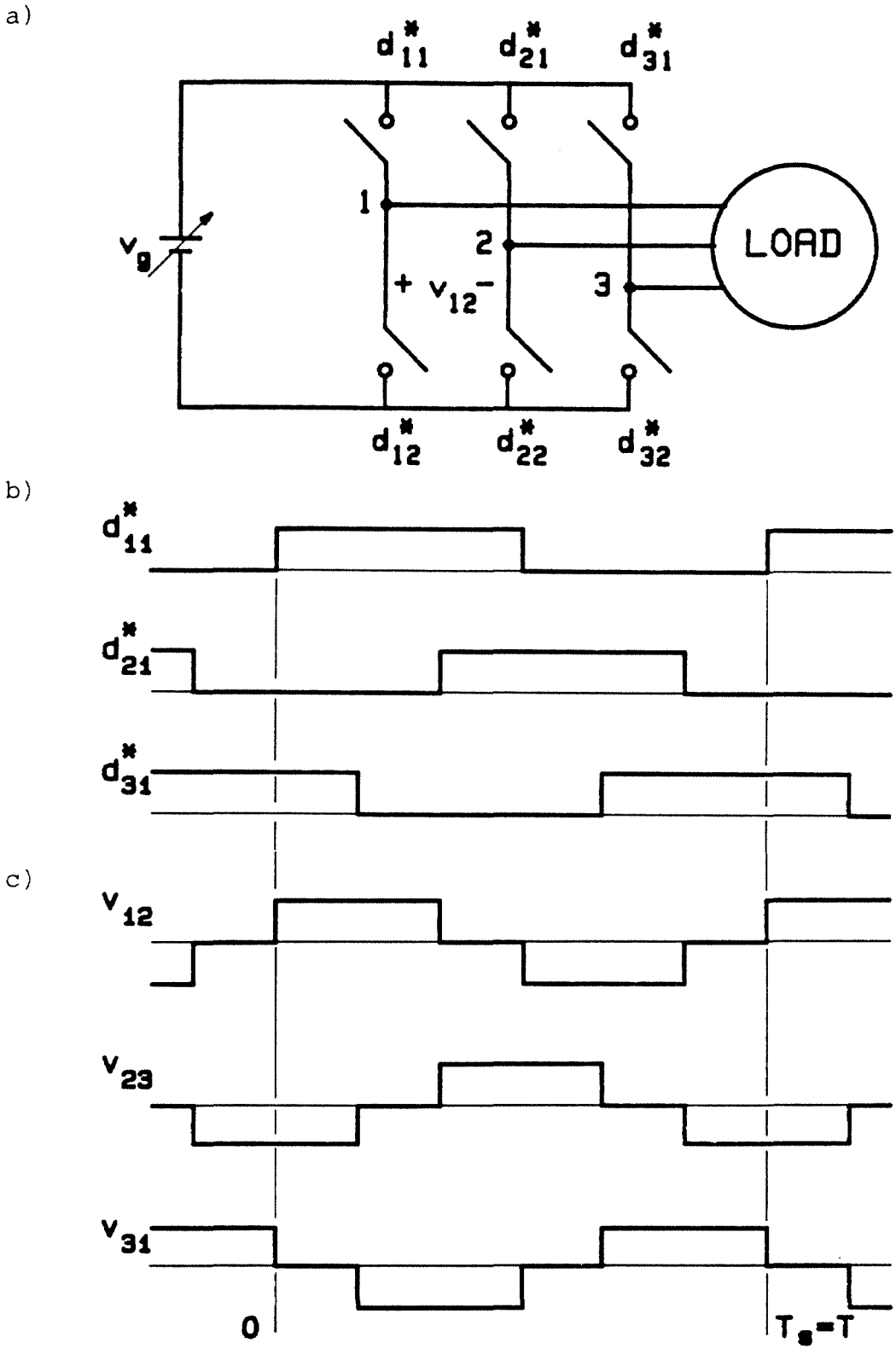


Fig. 2.1 (a) Voltage-source inverter, (b) six-stepped switching functions, and (c) line voltages.

of the second pole (switch), which brings the second phase of the load to the positive end of the source. Although the switches are functionally independent, their timing must follow the *six-stepped* schedule in Fig. 2.1b and *cannot be arbitrary* because three-phase symmetry needs be preserved. The resulting line-to-line, or line, voltages are illustrated in Fig. 2.1c. The frequency of these voltages is controlled by the switching frequency as the two are equal. Their amplitude, however, cannot be changed via the switches in the topology and, hence, must be adjusted via the dc supply which, therefore, is either a phase-controlled rectifier or a chopper.

The voltage-source inverter has been famous for its simplicity in drive and control. It, however, generates a fair amount of harmonics that cause additional heating and torque pulsation in motor loads. The use of phase control to regulate the amplitude draws current harmonics from the main and degrades the input power factor, generally lagging. These drawbacks have led to the gradual substitution of the six-stepped by the PWM drive in medium-power applications.

It is important to recognize that the harmonic problem in the voltage-source inverter is due to the low switching frequency, not the nonlinear distortion. In other words, the topology is already ideal and has the potential to synthesize sinusoidal waveforms if properly switched. This ideality is proved in the next chapter where the voltage-source *topology* itself is preserved, but the switches are operated at a much faster frequency and under the PWM principle.

2.1.2 Current-Source Inverter

The current-source inverter [9] has gained considerable attention in the last several years. As is described in Fig. 2.2a, it consists of two triple-throw switches, instead of three double-throw switches as in the voltage-source inverter, permanently attached to a variable current source. In a practical circuit, each throw is realized by a thyristor; and the current source, a phase-controlled rectifier in series with a large inductor.

Although they are topologically independent, the two switches must be synchronized as in Fig. 2.2b to ensure three-phase symmetry. Whenever a phase of the load is contacted by a throw, it receives a current identical in form to the switching function of that throw. Therefore, each net phase current is simply the scaled difference between the switching functions associated with that phase, as is illustrated in Fig. 2.2c. Control of the output frequency is exercised via the switching frequency because the two are identical; adjustment of the amplitude is provided by the dc input.

The current-source inverter is free from the shoot-through faults found in the voltage-source inverter; in other words, no destruction occurs should more than one throw of the same switch be simultaneously activated. It also allows quick reversal of power flow when a phase-controlled rectifier is used at the input end. In spite of these merits, it still introduces low-frequency harmonics at both input and output ports. The output harmonics incur heating loss and electrical torque pulsation, which further excites mechanical resonance detrimental to ac machines. The input noise propagates through the finite line impedance and distorts the bus waveform, creating interference problems. The power factor is generally lagging

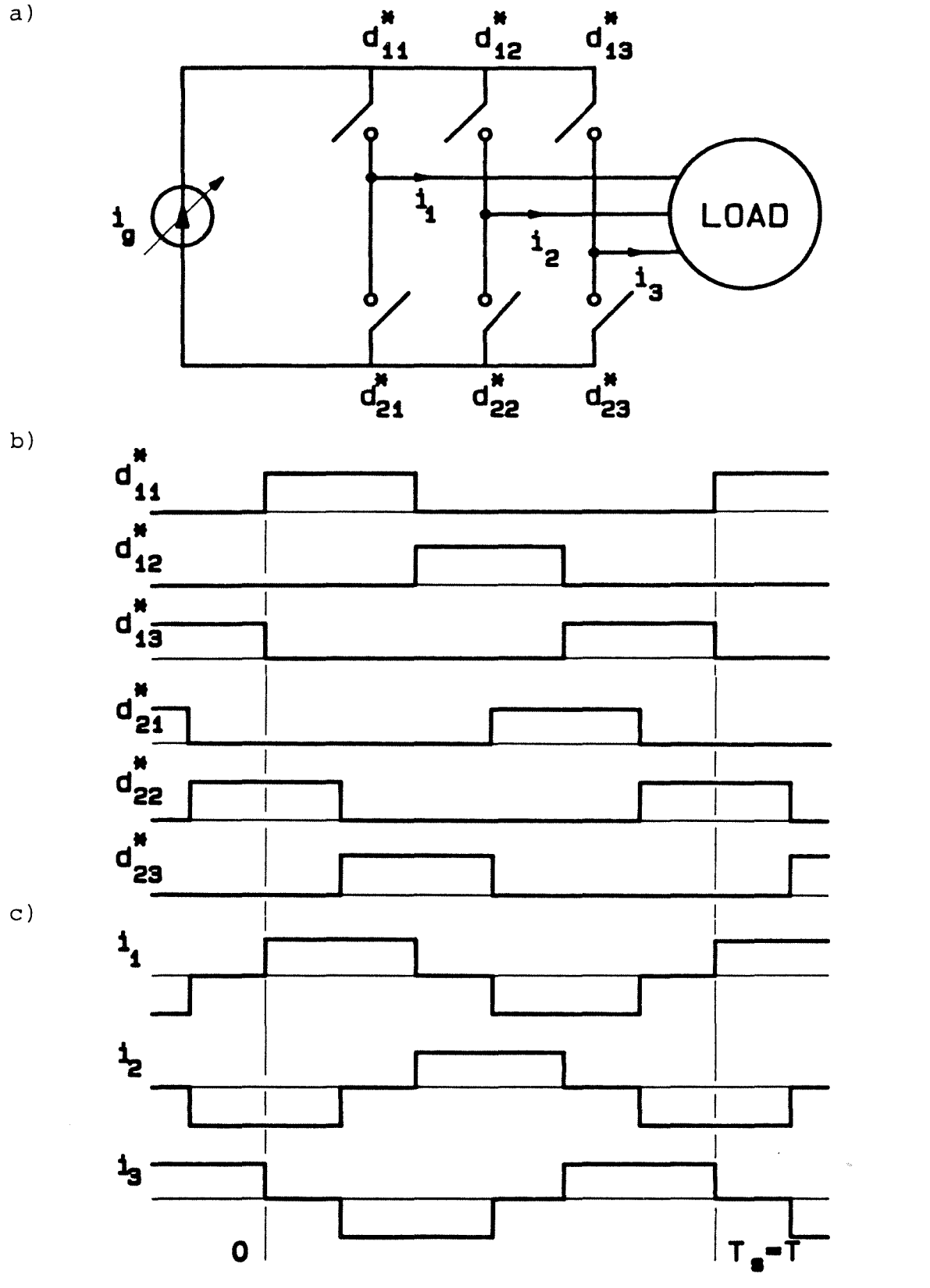


Fig. 2.2 (a) Current-source inverter, (b) six-stepped switching functions, and (c) phase currents.

because of phase control. Besides the harmonic drawback, the current-source inverter requires a bulky and expensive 60 *Hz* inductor. The size of the inductor, in turn, results in a very sluggish drive with poor dynamic performance. The inductive current source also induces large voltage spikes across the switches if it is fed directly into an inductive load, such as an induction motor.

As the voltage-source inverter, the current-source inverter is an ideal topology capable of synthesizing very clean power if it is switched at sufficiently high frequency and driven by PWM, instead of six-stepped, waveforms. Surprisingly, although the PWM voltage-source inverter has been proposed for a long time, the dual PWM current-source inverter still has not been reported. The major difficulty probably lies in the correct identification of the switches: if the switches in Fig. 2.2a were mistakenly represented as three double-throw switches, used for voltage-fed inverters, instead of two triple-throw switches, used for current-fed inverters, the synthesis of a PWM strategy would be impossible. PWM techniques for voltage- and current- fed dc-to-ac converters are studied in the next chapter and applied to the topologies in Figs. 2.1a and 2.2a to make them ideal.

2.1.3 Step-Synthesis Inverter

The step-synthesis inverter utilizes many slow throws to achieve the effect of a fast switch. Therefore, it may as well be placed in the fast-switching category if the classification is based on the step, instead of throw, frequency. The principle of step-synthesis is explored in Fig. 2.3 for one phase of a four-stepped circuit; the extension to three-phase is obvious.

The inverter is composed of a multiple-throw switch attached to the load, as is seen in Fig. 2.3a. The throws connect the load to different voltage levels created by the bank of power supplies, realized by an autotransformer with the required amount of taps in practice [11]. In each cycle, the top five throws are activated according to the timing waveforms in Fig. 2.3b; the bottom four throws are controlled by functions 180° out-of-phase with those of the top four. The duty ratios are programmed to minimize the distortion in the "quantized" sine wave of Fig. 2.3c. Voltage control can be achieved through the source as in the previous two cases. Alternatively, two sinusoids like that in Fig. 2.3c can be synthesized and added to provide one output; their phases are then adjusted to vary the summed amplitude [12].

In principle, the quality of the output improves with a higher number of steps. This improvement, however, is at the expense of an excessive amount of switches and complex control circuitry. The step-synthesis inverter is thus justified only for high-power applications that require sinusoidal waveforms.

In summary, this section has reviewed the voltage-source, current-source, and step-synthesis inverters. The first topology is of the voltage-fed type and uses three double-throw switches to feed six-stepped voltages to the load. The second one is of the current-fed type and consists of two triple-throw switches that invert the input current into six-stepped output currents. The last inverter is of the voltage-fed type as the first one, but it adds more steps to the output voltage waveform to reduce the total harmonic distortion.

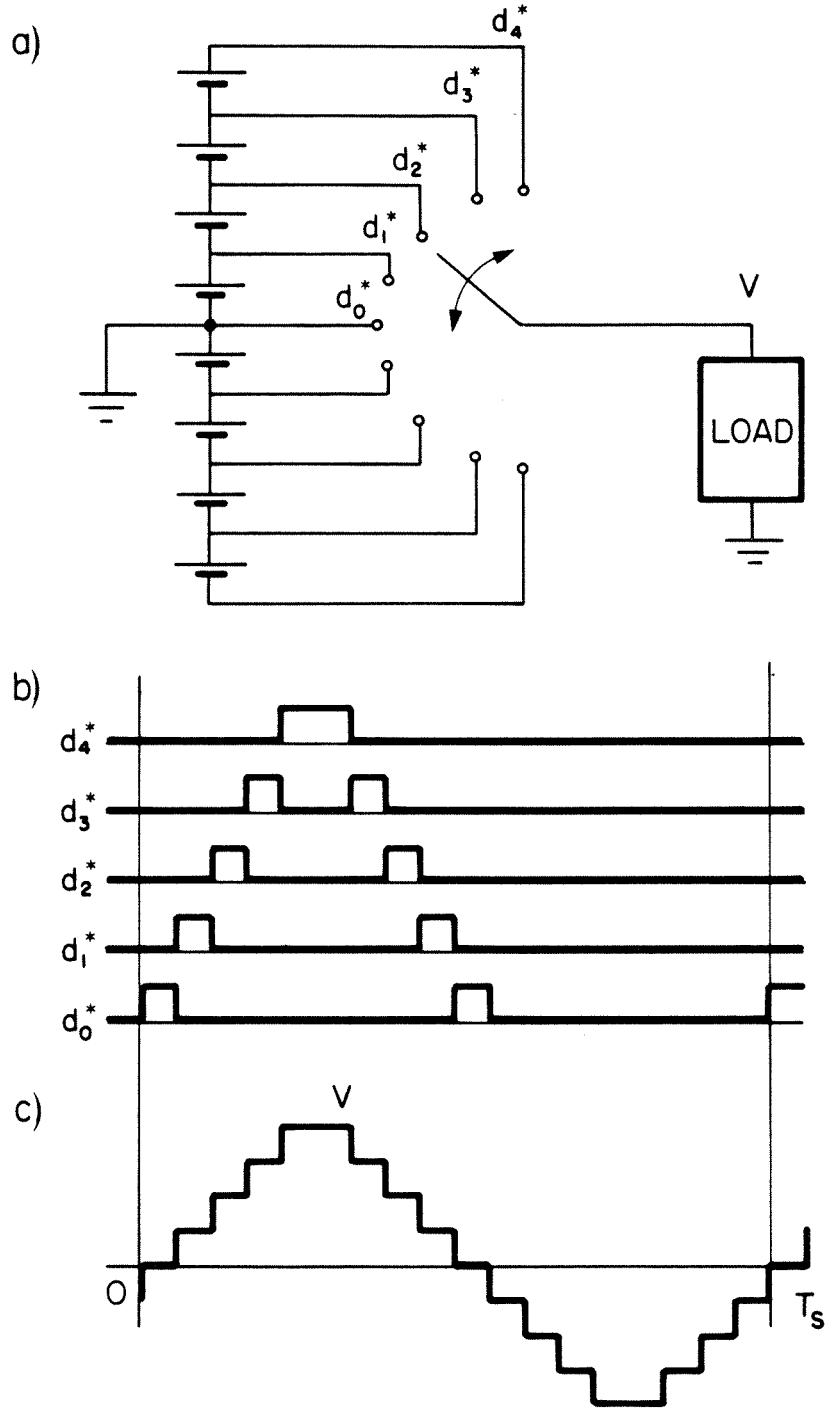


Fig. 2.3 (a) Stepped-synthesis inverter (b) four-stepped switching functions, and (c) phase voltage.

2.2 Inverters Switched at Medium Frequency

In the medium switching frequency range, "PWM inverter" refers generically to a *voltage-source inverter* (Fig. 2.1a) whose duty ratio varies from one switching cycle to the next. Even the switching frequency does not have to be constant. In 60 *Hz* applications, for instance, the practical switching speed may be anywhere from 60 *Hz* to 1 *kHz*, the upper bound being imposed by the slow speed of high-power semiconductor devices and the heat loss at high switching frequency [13 and 14]. Because of this medium switching frequency, it is impractical to separate the switching noise from the desired frequency component unless bulky inductors and capacitors can be tolerated. Therefore, ever since the introduction of the "sinusoidal PWM" (also called "triangulation method" or "subharmonic control") [13], a variety of other PWM schemes have been born mainly to optimize the harmonic figure. These ramifications include the "multimode" [14], "optimal" [15], "selective-harmonic-elimination" [16], "current-controlled" [17], and so on PWM strategies. The sinusoidal PWM is deferred until the next chapter where it is studied in depth (although the switching frequency there is much higher, the basic principle is still the same). The other kinds of PWM are reviewed below.

2.2.1 Multimode PWM

The power-speed limitation of the thyristor and the switching loss usually restrict the switching frequency of PWM inverters below 500 *Hz*. Although this carrier frequency is sufficient if the desired output is only 10 *Hz*, it is hardly satisfactory if the load requires 100 *Hz*. In the later case, there are so few pulses in each inversion cycle that the performance of

the converter is highly sensitive to the pulse number and the synchronization between the carrier and modulation signals. Without any synchronization, the difference between the switching and inversion frequencies accumulates into a slow beat frequency that modulates the output waveform. The resulting beat power gives rise to the troublesome fluctuation in the steady-state torque and speed of ac machines. Even if the two frequencies are perfectly synchronized, the purity of a PWM spectrum deteriorates to that of a six-stepped spectrum as the modulation frequency approaches the carrier frequency. Under this circumstance, the six-stepped drive is preferred to PWM drive because the former provides higher amplitude.

The above considerations have motivated the development of the *multimode PWM* in [14]. Five modes of operation are proposed, the selection of which depends on the operating frequency and amplitude. The first mode is the conventional sinusoidal PWM and is applied when the output frequency and amplitude are low. The carrier is a triangular waveform of constant frequency. As the modulation index of Mode 1 is exhausted, Mode 2 comes in. The carrier ceases to be triangular and is maintained at a fixed multiple of the inversion frequency. As the modulation amplitude exceeds the carrier peak in Mode 2, Mode 3 arrives. The triangular waveform is brought back and still synchronized to the reference frequency. The process continues with Mode 4 that retains only one notch in each half line cycle. Mode 5 eventually takes over when the circuit behaves as a genuine voltage-source inverter.

The multimode approach thus tries to select the best waveform for each range of amplitude and frequency. It starts at the sinusoidal PWM and gradually phases out all modulations until it reaches the six-stepped style. Needless to say, it demands a great deal of complicated circuitry to implement each mode, decide when to switch mode, and ensure smooth transitions.

2.2.2 Optimal PWM

In the *optimal PWM* [15], the number and positions of the pulses or notches within each switching cycle are selected so that the corresponding spectrum optimizes some performance index of the system. The performance index can be any function that depends on the modulation policy; examples are the harmonic loss, torque pulsation, or load currents. In [15], the rms (root-mean-squared) value of current harmonics is chosen as the index and calculated as a function of the number of commutation pulses and the commutation angles. The proper placement of the commutation angles then minimizes the influence of harmonics on the load.

Since the functions involved are generally complicated and load-dependent, they can only be solved numerically. Thus, computation power from a microprocessor is needed to synthesize the correct switching functions in this type of PWM.

2.2.3 Selective-Harmonic-Elimination PWM

Unlike the optimal PWM, the *selective-harmonic-elimination* technique [16] attacks the harmonics more directly by suppressing an arbitrary number of them in the output spectrum. The problem is formulated around a waveform that is chopped M times and possesses odd quarter-wave symmetry. Such a waveshape is characterized by M angles describing where the pulses start or end. Consequently, all harmonics can be computed in terms of these M pulse angles, and any M harmonics can be nullified by solution of the corresponding M simultaneous transcendental equations.

Closed-form solution of these equations, however, poses a formidable task, especially as the number of harmonics to be eliminated increases. Therefore, a computer is essential for numerical solution. If high performance is desired, a considerable amount of digital integrated circuits are involved to translate the mathematical results into the switching functions for the inverter.

2.2.4 Current-Controlled PWM

Instead of optimizing some performance index or eliminating some harmonics, the *current-controlled PWM* [17] cleans up the output currents directly by closed-loop regulation. In this scheme, the currents with superimposing ripples are fed back and compared with hysteresis levels placed around the reference signal to determine the switching frequency. As the ripple is regulated within the hysteresis band, the average output follows the average reference.

Three independent regulators are closed around the inverter in [17] to control three line currents; each has its own switching frequency related to its output. During some intervals, however, only two loops actually work while the third stays idle at zero switching frequency: the three loops are not all needed as the regulated quantities always sum up to zero (assuming no neutral-return path).

It is shown in the next chapters that at high switching frequency, the feedback problem can be formulated and solved differently. Describing equation can be used to predict the effects of energy-storage elements on closed-loop performance. The circuit implementation is much simpler since the principle requires only one regulator loop with one switching frequency.

In review, PWM inverters use the voltage-source topology and modify the six-stepped drive to achieve cleaner output waveforms. Different modulation strategies have been proposed. The multimode PWM starts out with sinusoidal PWM at low inversion amplitude and frequency and gradually alters its carrier to return to six-stepped operation at high output amplitude and frequency. The optimal and selective-harmonic-elimination techniques synthesize switching functions with proper pulse angles to optimize some performance index or suppress a certain amount of harmonics. The current-controlled PWM incorporates three-phase ripple regulators that force the average output currents to track the reference signals. All these efforts thus rely on either exotic open-loop switching functions or closed-loop regulation to purify the output spectrum.

2.3 Inverters Switched at High Frequency

This section consists of two parts. The first reviews the switched-mode power amplifier, an earlier effort in PWM dc-to-polyphase conversion. The second examines the resonant inverter, an example of energy inversion with a resonance link.

2.3.1 Switched-Mode Power Amplifier

As is illustrated in Fig. 2.4, a three-phase *switched-mode power amplifier* [19] is composed of three dc regulators that amplify three-phase reference signals into three-phase power for the load. Each block labeled "Two-Quadrant Dc Regulator" actually consists of any dc topology and a feedback loop designed to match the output to the reference with very little error. Closed-loop operation is necessary because the nonlinearity of dc

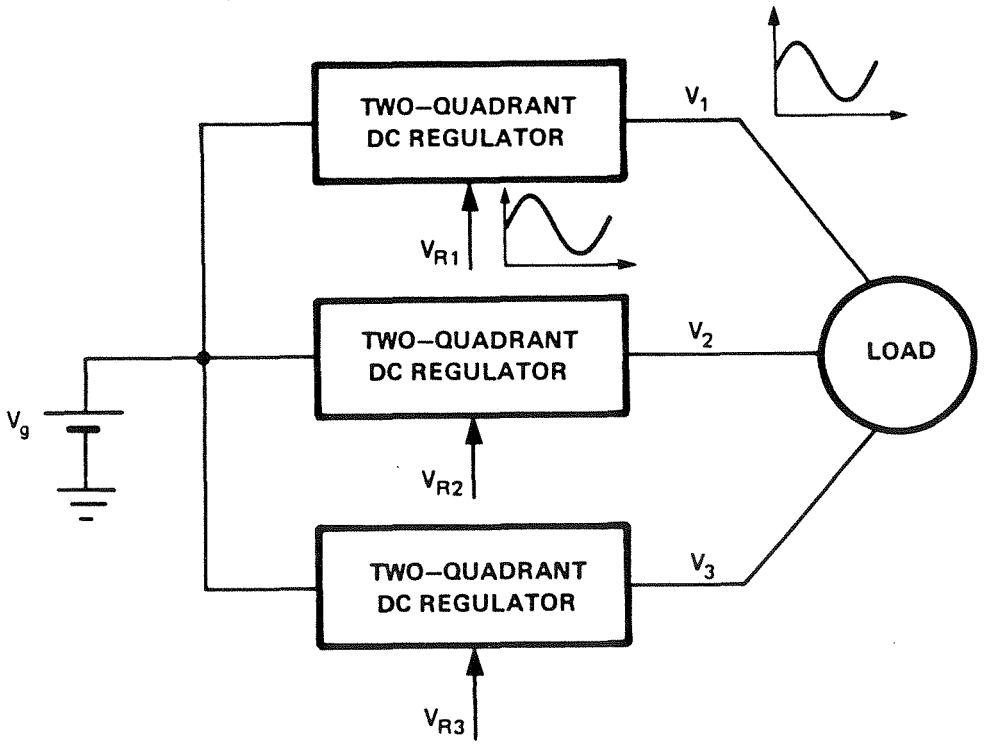


Fig. 2.4 Switched-mode amplifier with sinusoidal phase voltage riding on dc offset.

power stages prevents sinusoidal outputs for open-loop sinusoidal duty ratio modulation [20]. Note that the amplifier as a whole is four-quadrant even though each dc block is current two-quadrant. Current bidirectionality is realized by two-quadrant-in-current switches in the individual topology; and voltage bidirectionality, the back-to-back arrangement of all three topologies.

If the loop is closed properly, the feedback complexity is compensated by clean output waveforms. The overall system is rugged in the presence of unbalanced load because the regulators essentially operate independently from each other. Since each block is two-quadrant, only two-quadrant switches are required. The switch simplicity, however, is at the expense of many power stages and reactive elements, a result of the simplistic conglomeration of many smaller units without taking advantage of the topological simplification offered by polyphase synergism. Additional circuitry is also needed in the feedback loops to correct the nonideality of the dc topologies.

It must be cautioned that since each converter can synthesize only one polarity of voltage, the phase voltage always carries a dc offset in addition to the wanted ac. This dc offset, although it contributes no power to the load, raises the phase voltage to an unexpectedly high level hazardous should a fault occur across the regulator. It necessitates dc feedback loops to ensure all large dc levels closely match so that no dc differential is passed to low-resistance, such as motor, loads. It forces the amplifier to be designed for *four* times the load power (assuming the optimistic unity power factor) because during the course of operation, each dc block has to supply the *whole* load *and* the other two blocks. The large power requirement eventually means high stress on circuit components. This is usually

reflected in the rating of the output capacitors and semiconductor devices. Even the elements buried inside the topology also have to be designed to carry extra circulating harmonics.

Genuinely polyphase topologies that produce sinusoidal outputs from sinusoidal controls in an open-loop fashion are introduced in the next chapter. They require considerably less components, and their components withstand lower stress. Feedback is incorporated only for regulation, not improvement of the waveform, and is implemented in a single loop common to all phases, not one loop per phase as in the amplifier scheme.

2.3.2 Resonant Inverter

As is proposed in [22] and [35], a *resonant inverter* contains a high-frequency resonant link that extracts power from the source and delivers this power to the load. The essential elements of the circuit are thus a resonant tank, a set of "modulation" switches, and a set of "demodulation" switches, as is demonstrated in Fig. 2.5. High-frequency filters are also present to attenuate the switching noise at the input and output.

Energy is fed to the resonant circuit by the input switches usually operated below resonance at 50 percent duty ratio. Control is achieved by modulation of the switching frequency. The resulting pulse-area modulation then codes the carrier waveform with the desired output information. The signal transported by the carrier is demodulated by the controlled bridge at the output. The bridge is supplied with the signs of the wanted output currents so that it knows which way to steer the current pulses of both polarities. For instance, if the inverter is in the positive half inversion cycle,

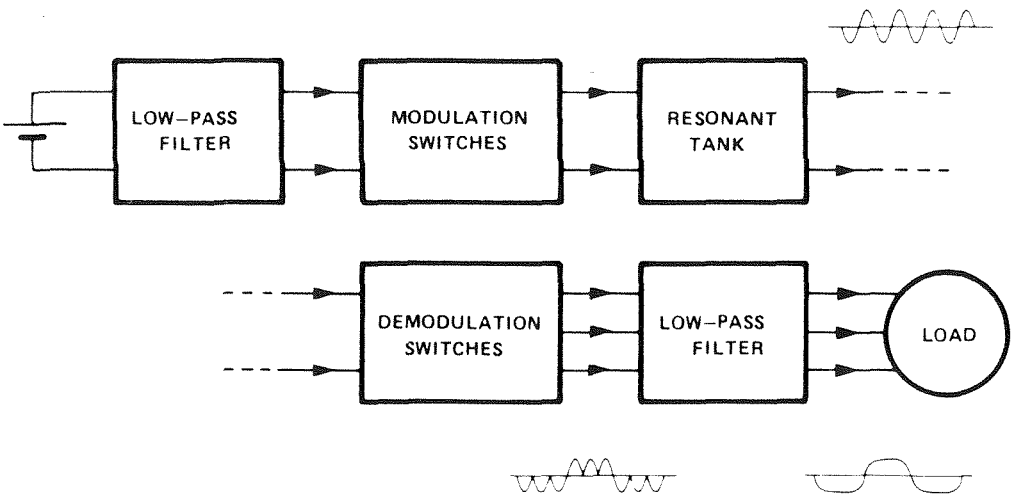


Fig. 2.5 Functional diagram of a resonant inverter showing a resonant link surrounded by modulation and demodulation switches.

all positive current pulses are passed directly to the load while all negative pulses are rectified first before going to the output.

Resonant circuits have been praised for impressing low stress on their switches. Therefore, they are excellent candidates for high-frequency, high-power applications. Despite this advantage, however, the resonant inverter is less popular than the PWM inverter because of the complexity in both implementation and understanding of the circuit. It generally requires more switches and reactive components in the power stage as well as electronics in the feedback and control circuitry. Since no rigorous open-loop analysis has been attempted, it is not clear whether the principle can synthesize sinusoidal outputs for sinusoidal (or simple) frequency

modulation. In [22], the source voltage, load condition, resonant current, and so on, have to be fed back to determine the switching algorithm. Even in closed-loop operation, the output currents are still square since the demodulation is still six-stepped.

Lack of proper understanding of the resonance principle has been the major hindrance to the progress of this potential field. Not until recently has [36] identified and analyzed the various steady-state modes of operation for the simpler dc resonant converters. Since it is well-known that resonant behavior is highly sensitive to loading condition, a useful result has been the characterization of this load sensitivity. It is expected that similar studies are extended to explain all aspects of resonant inversion and, hence, encourage the application of resonant inverters.

In conclusion, inverters have been classified, according to the ratio of their switching to inversion frequency, into the slow-, medium-, and fast-switching categories. Examples of slow-switching circuits are the voltage-source and current-source inverters switched at the output frequency according to the six-stepped strategy. These topologies introduce no nonlinear distortion even though they suffer from switching harmonics. The harmonic spectrum of the voltage-source inverter is partially improved by pulse-width modulation below a decade of the output frequency in the PWM inverters. Some PWM techniques are sinusoidal, multimode, optimal, selective-harmonic-elimination, and current-controlled schemes. Recently, the inversion field has been revolutionized by circuits switched above two decades of the inversion frequency. Examples are the switched-mode power amplifier, which integrates many PWM dc regulators into a polyphase structure, and resonant inverter, which processes energy via a resonant link.

Although switching ripple is attenuated considerably in these fast-switching converters, nonlinear distortion is also easily introduced unless the topology is ideal. Some ideal topologies capable of generating sinusoidal outputs from sinusoidal controls are recognized in the following chapter.

CHAPTER 3

FAST-SWITCHING SINUSOIDAL PWM INVERTERS

This chapter describes and analyzes topologies that invert a dc input into balanced polyphase sinusoidal outputs from balanced polyphase sinusoidal duty ratio modulations. The number of phases is any integer greater than one. The phases of a two-phase (or semi-four-phase) system are $\pm 90°$ out-of-phase while any two adjacent phases of an M-phase circuit are displaced by $\pm \frac{360°}{M}$, where $M>2$. Strictly speaking, a two-phase inverter is not "balanced" since its sequence angle is not 180°. Therefore, its topology and equations do not fit in the general framework shared by the balanced polyphase inverters. Nevertheless, it does provide constant instantaneous power with sinusoidal outputs as the balanced circuits do.

The first section is the heart of the chapter: it describes the *topologies* in terms of their switches, filters, and continuous duty ratio modulations. Examples include the *buck*, *boost*, *buck-boost*, and *flyback inverters* - the names originate from their dc equivalents - all synthesizing ideal waveforms when operating open-loop. The last three sections explain qualitatively the performance of these circuits by interpretation of the *steady-state*, *dynamic*, and *canonical* models produced by the describing equation technique (Chapter 1). Quantitative aspects, although they are accurate, are not emphasized.

3.1 Description of Topologies

Each of the following three subsections presents the topology and explains how it is conceived; both M (>2)-phase and two-phase cases are considered. The first two subsections are devoted to the buck and boost inverters, examples of direct conversion (or conversion without any intermediate energy storage); the last one, the buck-boost and flyback inverters, examples of indirect conversion. Since only duty ratios, not exact timing waveforms, influence circuit behavior, switch description is in terms of *duty ratio*, not switching function, assignment.

3.1.1 Buck Inverter

The M (>2)-*phase buck inverter* is the equivalent of the fast-switching buck dc converter or the slow-switching voltage-source inverter in *high-frequency inversion*. As is portrayed in Fig. 3.1, the principal components of the topology are M *double-throw* switches that invert the dc input into balanced polyphase outputs. The duty ratio of the upper throw of any switch consists of a dc offset and a *continuous*, *sinusoidal* modulation:

$$d_{w1} = \frac{1}{2} + d_w \qquad , \qquad 1 \le w \le M \tag{3.1}$$

where the *effective duty ratio* d_w, which truly governs the describing equations of this topology, is

$$d_w = d_{w1} - \frac{1}{M}\sum_{z=1}^{M} d_{z1} = \frac{d_m}{2}\cos\left[\theta - (w-1)\frac{2\pi}{M}\right] \tag{3.2}$$

where

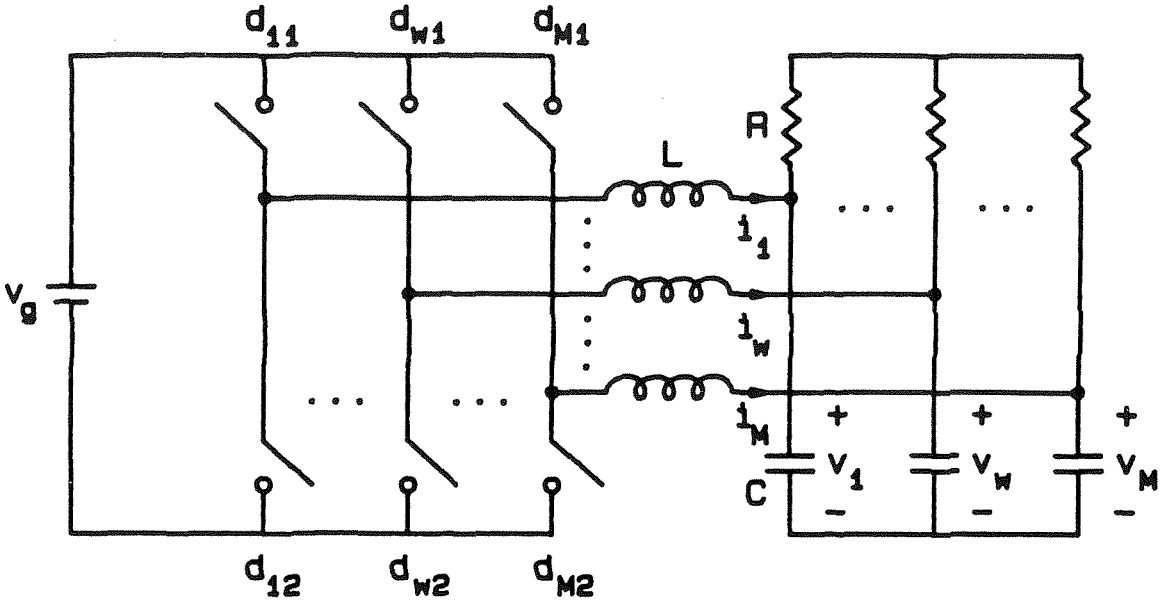


Fig. 3.1 M-phase buck inverter with M double-throw switches pulse-width-modulated by sinusoidal functions.

$$\theta = \int_0^t \omega(\tau)\, d\tau \qquad \text{and} \qquad d_m \leq 1 \tag{3.3a,b}$$

In the above, the dc offset is fixed at $\frac{1}{2}$ to maximize the *instantaneous effective modulation amplitude* $\frac{d_m}{2}$; it can be any value between zero and one instead. The *instantaneous modulation frequency* ω can be any real number, where a negative frequency corresponds to a reversal of phase sequence. As far as ω is sufficiently below the switching frequency, the set of duty ratios d_{w1} can be realized by a variety of switching functions. The selection of the drive strategy then depends upon circuit simplicity or second-order harmonic effects. Note that the duty ratios do *not* have to be

continuous as in Eq. (3.1). *Six-stepped PWM* is introduced in the next chapter as an example of a *piecewise continuous* drive capable of synthesizing sinusoidal outputs.

Although the voltage-source inverter (Fig. 2.1a) and buck inverter have *identical switch arrangement*, they operate on entirely *different switching principles*. The former is switched at low frequency by the six-stepped drive while the latter is switched at high frequency by pulse-width-modulated waveforms. The switching harmonics in the voltage-source inverter cannot be filtered effectively since they are so close to the fundamental component; those in the buck inverter, on the other hand, can be easily attenuated once pushed two decades above the desired output frequency.

As can be seen from Fig. 3.1, the switching noise in the buck topology is smoothed out by the LC filters in series with the switches. The filter size, of course, is small and diminishes as the switching frequency increases. As in the buck dc converter, the output currents are continuous thanks to the inductors; the input current can be made nonpulsating with an input filter. Since the inductors carry fluxes that always add up to zero, they can be integrated into a high-frequency polyphase inductor to save magnetics. The capacitors can be connected in either wye or delta configuration, and the former case is illustrated here. The load can be an ac machine, the utility line, or, in this case, a simple resistor bank. Under steady-state condition, the load and capacitor neutrals are virtually at the same potential. Note that if a type of load can be driven by the voltage-source inverter, it should work with the buck inverter as well because the two inverters differ only in switching mechanisms and share the same

topology. Fast switching thus improves the *waveform quality*, not drastically modifies the basic *topological characteristics* of these voltage-fed structures.

It has been concluded in Chapter 1 that all inverters with more than two phases are *mathematically* reducible to a two-phase equivalent. The M-phase buck inverter in Fig. 3.1, however, cannot be *topologically* simplified to a two-phase circuit since the output currents in the former sum up to zero while those in the latter do not. Therefore, a neutral return and, hence, one more switch need be added at the positions shown in Fig. 3.2.

Out of the numerous duty ratio assignments, the most efficient one is

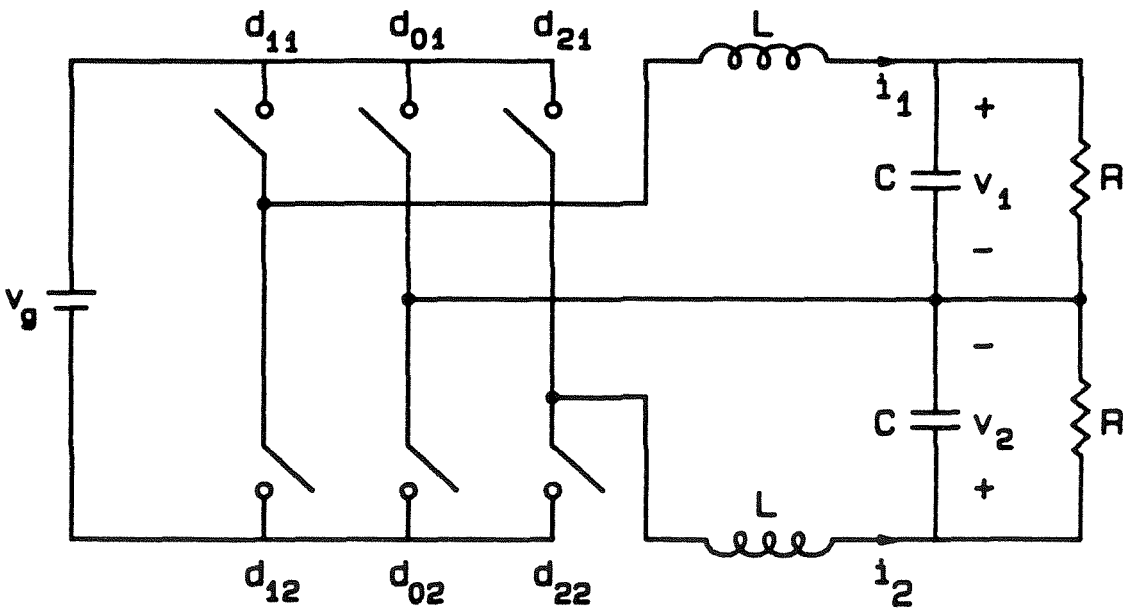


Fig. 3.2 Two-phase buck inverter.

$$d_{01} = \frac{1}{2} - \frac{d_{m0}}{2}\cos\theta_0 \tag{3.4a}$$

$$d_{11} = \frac{1}{2} + \frac{d_{m0}}{2}\cos(\theta_0 + \frac{\pi}{2}) \tag{3.4b}$$

and

$$d_{21} = \frac{1}{2} + \frac{d_{m0}}{2}\cos(\theta_0 - \frac{\pi}{2}) \tag{3.4c}$$

where

$$d_{m0} \leq 1 \qquad \text{and} \qquad \theta_0 = \int_0^t \omega(\tau)\, d\tau + \varphi_0 \tag{3.5a,b}$$

The resulting effective duty ratio can be expressed as

$$d_w = d_{w1} - d_{01} = \frac{d_m}{2}\cos[\theta - (w-1)\frac{\pi}{2}] \quad , \qquad w = 1,2 \tag{3.6}$$

where, owing to the extra switch, the upper bound of the effective modulation amplitude is improved according to

$$d_m \leq \sqrt{2} \tag{3.7}$$

In summary, the M (>1)-*phase buck inverter* consists mainly of *double-throw* switches pulse-width-modulated by continuous balanced *sinusoids* whose frequency is much lower than the switching frequency. These switches thus invert a dc source into balanced polyphase voltages superimposed by switching noise. Low-pass LC filters then follow the voltage-fed switches to attenuate the high-frequency harmonics and pass the desired fundamental sinusoids relatively unaffected to the load.

3.1.2 Boost Inverter

The M (>2)-*phase boost inverter* shown in Fig. 3.3 is the equivalent of the fast-switching boost dc converter or the slow-switching current-source inverter in *high-frequency inversion*. Since the topology is current-fed, an inductor is placed before the switches to transform the dc voltage source into a dc current source (Eq. (1.26)). The input current is then inverted into balanced polyphase currents for the RC combination by *two M-throw switches*. In general, the duty ratio of each throw consists of a sinusoidal modulation and a dc component:

$$d'_{kw} = \frac{1}{M} + \frac{d'_{mk}}{M} \cos[\theta'_k - (w-1)\frac{2\pi}{M}] \tag{3.8}$$

where

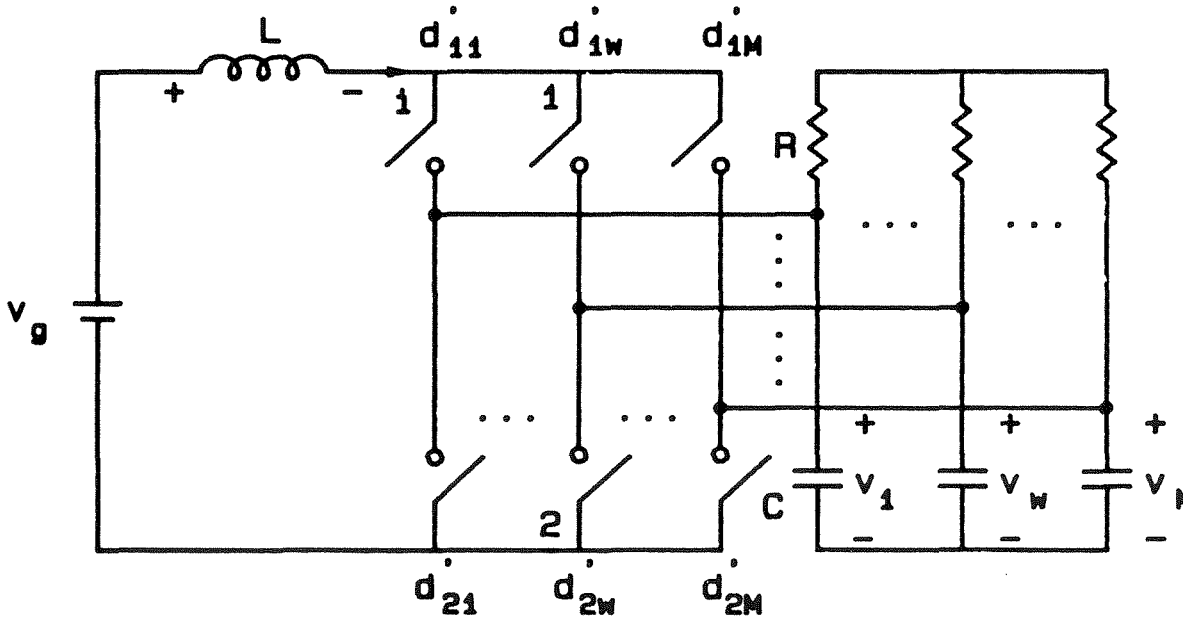


Fig. 3.3 M-phase boost inverter with two M-throw switches pulse-width-modulated by sinusoidal functions.

$$d'_{mk} \leq 1 \qquad \text{and} \qquad \theta'_k = \int_0^t \omega'(\tau)\, d\tau + \varphi'_k \tag{3.9a,b}$$

for

$$k = 1,2 \qquad \text{and} \qquad 1 \leq w \leq M \tag{3.9c,d}$$

where prime (') signifies that the switch lies at the output side of the circuit. Note that all modulations of the same switch must constitute a set of balanced polyphase sinusoids; the modulations of the two switches, nevertheless, can have *different* instantaneous modulation amplitudes and phases because the switches are topologically independent. The optimal *effective duty ratio* results when the two amplitudes equal and the two phases oppose:

$$d'_w = d'_{1w} - d'_{2w} = \frac{2d'_m}{M} \cos[\,\theta' - (w-1)\,\frac{2\pi}{M}\,] \tag{3.10}$$

where

$$d'_m \leq 1 \qquad \text{and} \qquad \theta' = \int_0^t \omega'(\tau)\, d\tau \tag{3.11a,b}$$

It must be reminded that this optimality is only relative to other *continuous* modulation schemes; in the next chapter, *six-stepped PWM* is introduced as an example of a *piecewise continuous* drive capable of producing ideal waveforms and a higher effective modulation amplitude.

The switches output pulses of current that contain low-frequency sinusoidal components and high-frequency harmonics. The switching harmonics, however, are absorbed right at the capacitors, and only smooth, sinusoidal currents continue to the load. The load does not have to be a

resistor as shown in Fig. 3.3: it can be an ac motor, the utility line, or other polyphase impedances. If a load can be controlled by the current-source inverter, so can it with the boost inverter; likewise, problems found in the former may exist in the latter. The boost inverter, however, provides much cleaner waveforms, owing to filtered fast-switching PWM, and responds much faster, thanks to the reduction in filter size at high frequency. Note that if the load is inductive, the capacitors, although they can be small unless the ripple is of prime concern, should be there to absorb switching spikes between two inductive current sources.

The two-phase boost inverter is described in Fig. 3.4. It consists of two triple-throw switches that feed the inductor current into the output section. One throw in each switch is dedicated to the common of the capacitors and the load. This common is made available because two-phase

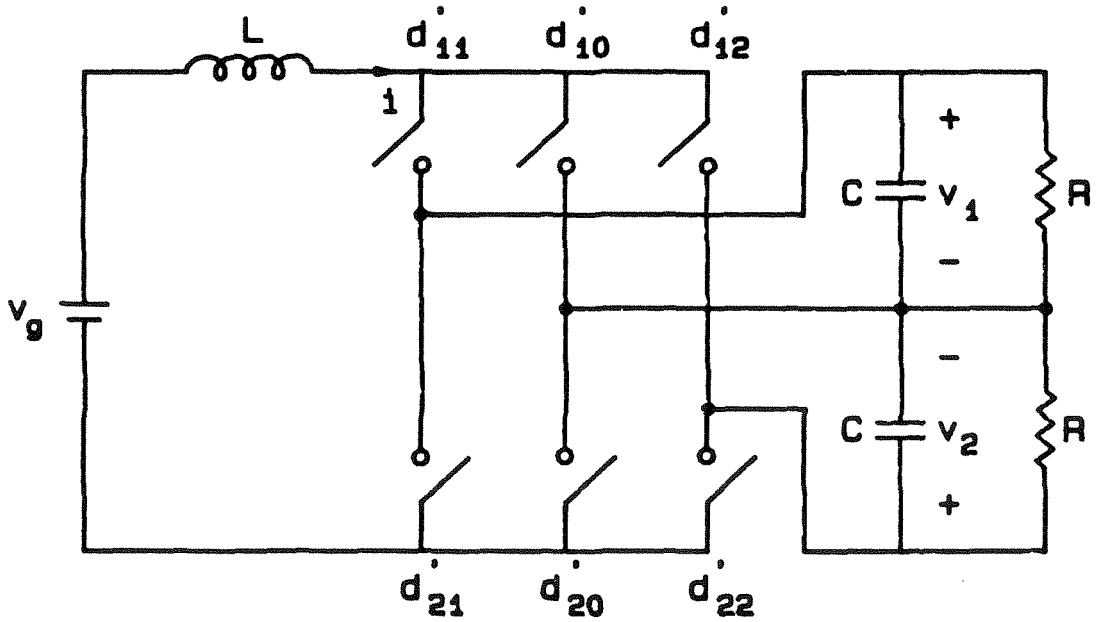


Fig. 3.4 Two-phase boost inverter.

currents do not sum up to zero and need a return path.

The duty ratio distribution is less straightforward in this case. A choice that makes all duty ratios positive and maximizes the effective modulation amplitude is

$$d'_{1w} = \frac{1}{2+\sqrt{2}} + \frac{d'_m}{2}\cos[\theta' - (w-1)\frac{\pi}{2}] \qquad (3.12a)$$

and

$$d'_{2w} = \frac{1}{2+\sqrt{2}} - \frac{d'_m}{2}\cos[\theta' - (w-1)\frac{\pi}{2}] \qquad (3.12b)$$

where

$$w = 1,2 \qquad \text{and} \qquad d'_m \le \frac{2}{2+\sqrt{2}} \qquad (3.13a,b)$$

In review, the *M* (>1)*-phase boost inverter* places an inductor in series with the dc source to transform the input voltage into *current*. The inductor current, open-loop *dc* by virtue of the topology, is inverted into polyphase currents by *two multiple-throw* switches *sinusoidally* pulse-width-modulated at much lower than the switching frequency. The pulsating currents from the current-fed switches are filtered by a capacitor bank so that highly sinusoidal waveforms feed the load.

3.1.3 Buck-Boost and Flyback Inverters

Many derived inverter topologies can be synthesized by cascade of a dc converter (buck, boost, flyback, Ćuk, etc.) and the buck or boost inverter just described and simplification of the result. Two examples studied below are the buck-boost inverter, the combination of a buck dc converter and a

boost inverter, and the flyback inverter, the topological kin to the buck-boost circuit.

An M (>2)-*phase buck-boost inverter* is illustrated in Fig. 3.5. Its output section is identical to that of Fig. 3.3: there are two familiar M-throw switches that guide the inductor current into the junctions of the capacitor bank and the load. A double-throw switch, however, is added to allow the adjustment of the dc source. The topology thus has the step-up/down capability much more desirable and safer than simply the boost gain of the original boost inverter.

The three switches are totally independent of each other. Therefore, the circuit is always simultaneously charged by the input duty ratio d and discharged by the output duty ratio d'_{kw} of Eq. (3.8). Under steady-state condition, d is dc while d'_{kw} is modulated sinusoidally to

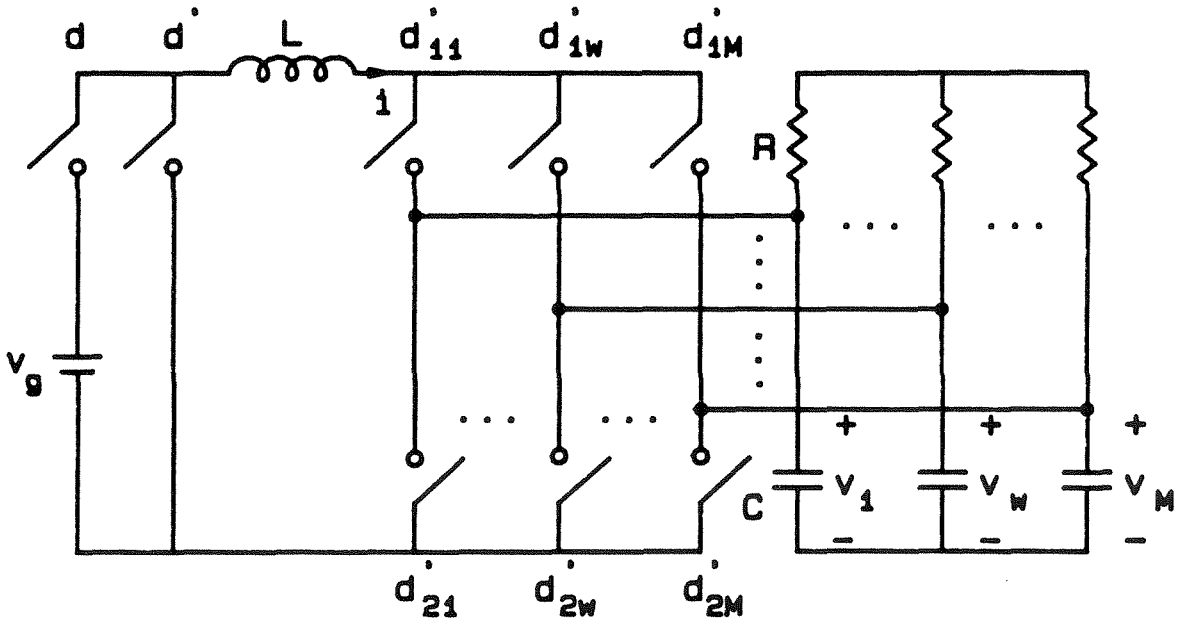


Fig. 3.5 M-phase buck-boost inverter, cascade of a buck dc converter and an M-phase boost inverter.

generate balanced polyphase voltages.

The two-phase buck-boost inverter is the cascade of a buck dc converter and a boost two-phase inverter (Fig. 3.4), as is realized in Fig. 3.6. Again, the input switch is run by d, completely independent of the output duty ratios optimized according to Eq. (3.12).

The buck-boost topology does not provide isolation because the inductor connects the source to the load during the operation. Isolation is incorporated by separation of the energy storage from the energy transfer interval, as is implemented in the M (>2)-*phase flyback inverter* in Fig. 3.7 (drawn non-isolated for for the mean time to facilitate switch identification and explanation). Thus, the inductor here first stays at v_g during dT_s, where T_s is the switching period, to get charged and then moves among the output lines during $(1-d)T_s$ to distribute power to the load.

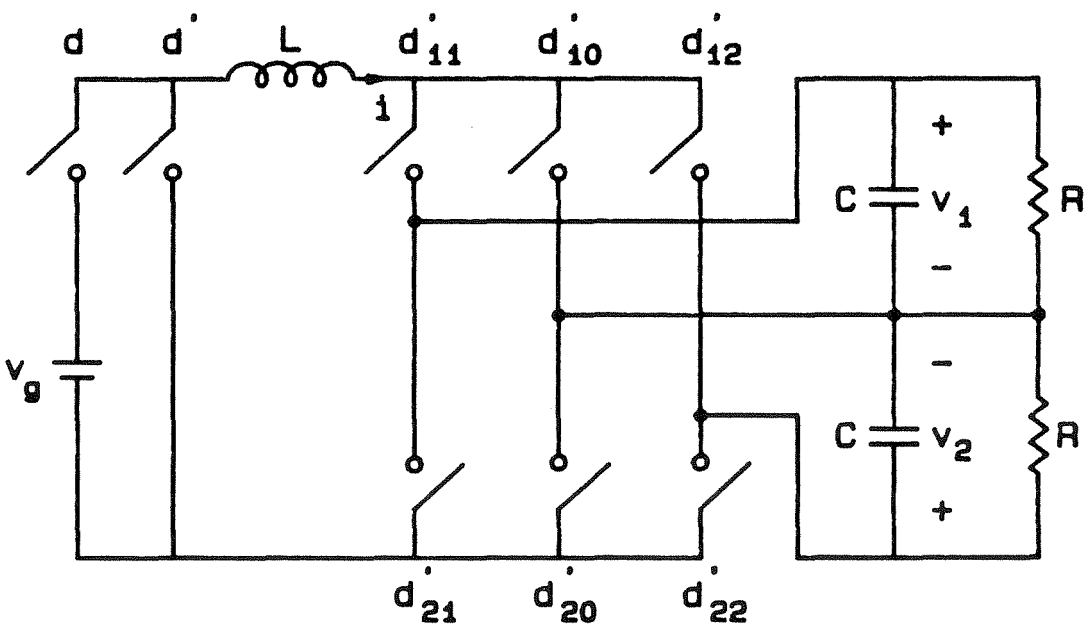


Fig. 3.6 Two-phase buck-boost inverter.

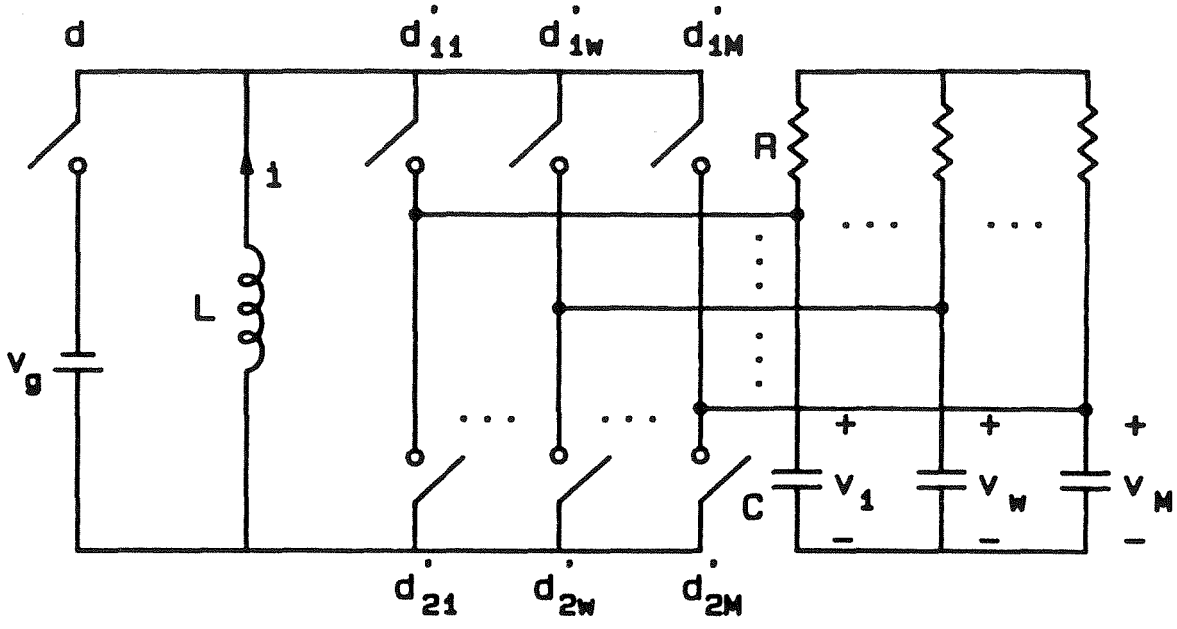


Fig. 3.7 M-phase flyback inverter with one M-throw and one (M+1)-throw switch pulse-width-modulated by sinusoidal functions.

In contrast to the buck-boost topology, the flyback inverter groups its throws into only *two* independent switches. Originally, each switch in Fig. 3.7 has $(M+1)$ throws, M at the output and one at the input. The two input throws, however, are combined since they are always in series. The result is an upper switch with $(M+1)$ throws and a lower switch with only M throws as shown.

Since the topology is still current-fed, the duty ratio assignment of the output throws is analogous to that defined in Eq. (3.8). The only modifications are in the dc offset and the upper bound for the modulation amplitude to account for the charging duty ratio d. Therefore,

$$d'_{kw} = \frac{d'}{M} + \frac{d'_{mk}}{M} \cos\left[\theta'_k - (w-1)\frac{2\pi}{M}\right] \qquad (3.14)$$

where

$$d' = 1 - d \qquad \text{and} \qquad d'_{mk} \leq d' \qquad (3.15a,b)$$

and the remaining terms are as specified by Eq. (3.9). Even though d and d'_{mk} of the flyback inverter cannot be varied independently and over the entire range from zero to one as those of the buck-boost inverter, the two circuits do share the *same describing equations* and, hence, *performance*.

The reduction of Fig. 3.7 to the two-phase flyback inverter is delineated in Fig. 3.8. It contains one triple-throw and one four-throw switch; in each switch one throw is reserved for the neutral return. In any switching period, the input throw is closed for dT_s while the output ones are

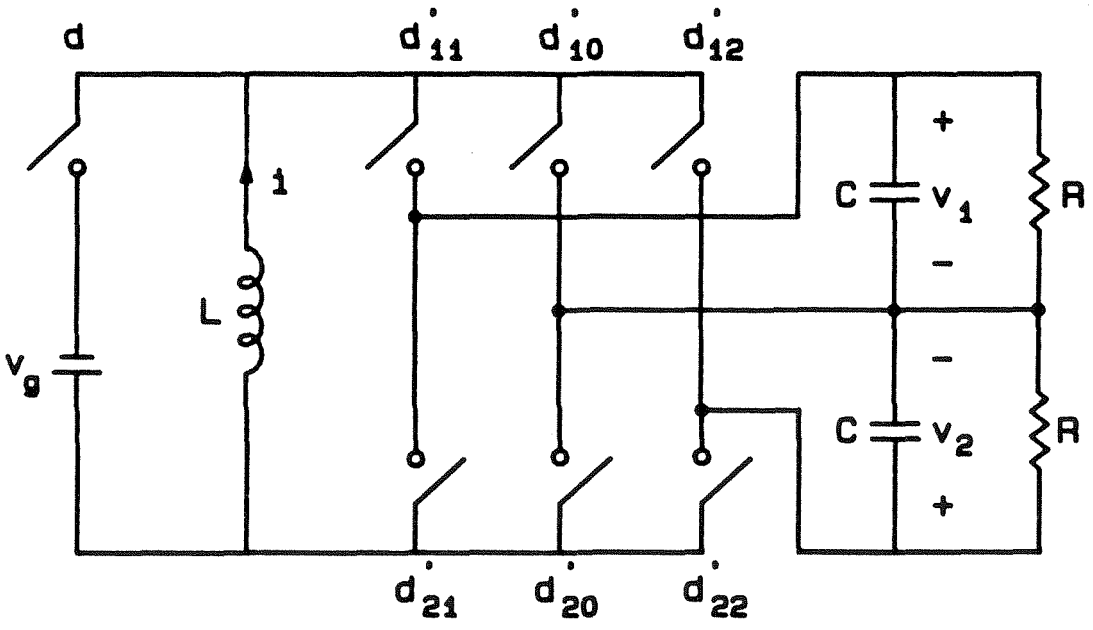


Fig. 3.8 Two-phase flyback inverter.

open. The output throws are then activated during $d'T_s$ according to

$$d'_{1w} = \frac{d'}{2+\sqrt{2}} + \frac{d'_m}{2}\cos[\theta' - (w-1)\frac{\pi}{2}] \qquad (3.16a)$$

$$d'_{2w} = \frac{d'}{2+\sqrt{2}} - \frac{d'_m}{2}\cos[\theta' - (w-1)\frac{\pi}{2}] \qquad (3.16b)$$

where

$$w = 1,2 \qquad \text{and} \qquad d'_m \leq \frac{2}{2+\sqrt{2}}d' \qquad (3.17a,b)$$

Earlier remarks regarding the optimal selection of duty ratios and the type of load for the boost inverter still apply to the buck-boost and flyback topologies. Thus, the duty ratios, which may or may not be continuous, should be chosen to maximize the effective modulation amplitude. The output throws, being current-fed, can also be driven by the six-stepped PWM detailed in the next chapter in conjunction with the boost-type switches. The load can be any impedances that the boost inverter can handle since all equations of the three circuits are similar.

In retrospect, the *buck*, *boost*, *buck-boost*, *and flyback inverters* have been described as examples of *fast-switching PWM* inverters capable of generating sinusoidal outputs from *sinusoidal* controls. The number of phases in each topology extends from two to infinity. The minimal number of reactive elements and switches have been arranged such that input and output properties of these inverters are analogous to those of their corresponding dc counterparts. Fast switching means energy storage elements are small and economical.

Operation has been characterized solely in terms of *duty ratios*. The duty ratios always contain *simple, easy-to-synthesize* dc or sinusoidal values. Just as there is no unique switching function to realize a duty ratio, there are many ways to assign functions to the duty ratios. Consequently, the drive schemes for these fast-switching topologies are numerous and flexible.

3.2 Steady-State Performance

The procedure for steady-state analysis of fast-switching PWM converters has been outlined in Chapter 1. It involves obtaining the *describing equations* of the circuit in the abc reference frame and *transformation* of these equations to the *ofb* coordinates where the system appears *time-invariant*. The steady-state solution is thus *constant* and either real or complex; constant scalar in the rotating coordinates means dc waveform in the stationary axes, and constant phasor corresponds to sinusoidal outputs.

An important conclusion has been all balanced polyphase converters with any number of phases are reducible to the two-phase equivalent. Therefore, all circuits of the same topology share common steady-state formulas. Inductor currents and capacitor voltages for the buck, boost, buck-boost, and flyback inverters obtained following the prescribed method are tabulated in Table 3.1. Remember that these solutions correspond only to the optimal continuous duty ratio functions discussed in the previous section; other PWM strategies (six-stepped PWM, for instance) necessarily modify the phasor amplitude via the effective duty ratio. Results are stated in terms of abc parameters so that they can be used directly for design

Inverter	Capacitor Voltage $V e^{-j\Phi_v}$	Inductor Current $I e^{-j\Phi_i}$
Buck	$\frac{D_m V_g}{2} \frac{1}{1+\frac{1}{Q}\frac{j\Omega}{\omega_o}+(\frac{j\Omega}{\omega_o})^2}$	$\frac{D_m V_g}{2R} \frac{1+\frac{j\Omega}{\omega_p}}{1+\frac{1}{Q}\frac{j\Omega}{\omega_o}+(\frac{j\Omega}{\omega_o})^2}$
Boost	$\frac{V_g}{D_m'}(1-\frac{j\Omega'}{\omega_p})$	$\frac{MV_g}{2D_m'^2R}[1+(\frac{\Omega'}{\omega_p})^2]$
Flyback	$\frac{DV_g}{D_m'}(1-\frac{j\Omega'}{\omega_p})$	$\frac{MDV_g}{2D_m'^2R}[1+(\frac{\Omega'}{\omega_p})^2]$
where $\omega_p = \frac{1}{RC}$, $\omega_o = \frac{1}{\sqrt{LC}}$, and $Q = \frac{R}{\omega_o L}$		

TABLE 3.1 Steady-state capacitor voltages and inductor currents in the buck, boost, and flyback (or buck-boost) inverters.

purpose.

It is obvious from Table 3.1 that inverters are not perfect voltage or current sources unless their filter inductance, capacitance, and frequency are zero. Therefore, the *steady-state frequency responses* provided by Table 3.1 are important because they not only predict dc gains, but also characterize the variation of output amplitudes and phases as functions of the inversion frequency. They also suggest how to place the steady-state poles and zeros to minimize the interaction between load and inverter impedances or to neglect filter effects over the frequency range of interest.

For the buck inverter, the output voltage is independent of the number of phases since the effective duty ratio stated in Eq. (3.2) is so. The dc gain of the phase voltage, however, is always below $\frac{1}{2}$ because the effective modulation amplitude is only $\frac{D_m}{2}$. Nevertheless, this peak is competitive to the $\frac{2}{\pi} \approx .64$ of the three-phase voltage-source inverter, which can give only square outputs. Later on, six-stepped PWM is shown to preserve sinusoidal quality and improve the dc gain to $\frac{1}{\sqrt{3}} \approx .58$.

As the inversion frequency Ω increases, the load and LC filters influence the steady-state responses as functions of Ω. For a resistive load, the voltage response is simply a second-order roll-off with the corner at $\frac{1}{\sqrt{LC}}$. Similar functions for more complicated loads, such as ac machines, can be found easily because the buck inverter is modeled as a sinusoidal excitation, created by sinusoidally modulated switches, driving the load through an LC filter.

The currents through the inductors of the buck inverter are generally ac because they are the sum of the capacitor and load currents. The switches, which *invert voltage* in the forward direction, *rectify* these *currents* in the reverse direction so that the average current drawn from the source is dc.

In contrast to the voltage-fed buck, the current-fed buck-boost, also representative of the boost and flyback, inverter exhibits more intriguing steady-state behavior. As is confirmed by Table 3.1, its inductor current must be *dc* so that, in the presence of dc input duty ratio, the instantaneous power flow is constant. For the inductor to carry dc current, its average voltage must be zero. Therefore, the output throws effectively *rectify* the sinusoidal polyphase voltages into a dc voltage that matches the value of the input supply. Dc current also means the steady-state reactance of the inductor is zero; this is why L never appears in the entries for the buck-boost, boost, and flyback inverters in Table 3.1.

The constant inductor current is fed into the RC load as sinusoidal currents by the sinusoidally modulated output switches. As in a linear circuit, the voltage thus generated across the RC impedance is obviously *sinusoidal*. The steady-state response of the voltage phasor, however, is shaped by a *right-half-plane (rhp) zero*, instead of a left-half-plane (lhp) pole as in the linear case. This peculiarity certainly cannot be explained adequately by linear circuit theory because the inverter, after all, is nonlinear. Actually, the decline in phase toward $-90°$ at high inversion frequency is just the familiar first-order lag of a capacitive voltage relative to the corresponding capacitive current, the corner being at $\frac{1}{RC}$, as is

agreed by Table 3.1. Much less obvious is the *rise* in voltage amplitude that accompanies the drop in phase.

One explanation for this trend is the volt-second-balance requirement for the inductor; this requirement translates into the *equality* between the input and output voltages across the inductor. It can be shown that the output volt-second is proportional to $V\cos\Phi_v$, and this quantity must always be *constant*. As the output waveform slips away from the duty ratio with increasing frequency, $\cos\Phi_v$ decreases to reflect the less efficient volt-second mechanism from the capacitors. The capacitor amplitude V then has to increase to compensate for this loss, and hence the rhp zero. At high Ω', the inductor current has to increase as Ω'^2 so that the output voltage can go up as Ω' while the capacitive reactance drops as $\frac{1}{\Omega'}$.

At zero inversion frequency, the dc gain of the buck-boost inverter is $\frac{D}{D'_m}$. The flyback and buck-boost topologies thus can step the input down via D or up via D'_m; the boost topology can only step up through D'_m. A variable V_g is no longer necessary, and so the circuits can be powered by a battery in case of line failure. Many units also can share the same dc source. Note that the output amplitude is independent of the number of phases M because any change in M is compensated by an inverse change in the modulation amplitude $\frac{d'_m}{M}$. More phases thus mean more power and higher inductor current.

To recap, steady-state performance of inverters depends on their nonzero *steady-state reactances*. The phasors in the voltage-fed buck inverter are the solutions of a per-phase model consisting of a constant

voltage exciting the load through an LC filter. The phasors in the current-fed buck-boost (or boost and flyback) inverter are the results of a per-phase network composed of an impedance-dependent current feeding the parallel capacitor and load. The current-fed variables tend to become unbounded at any inversion frequency where the angle of the impedance seen by the switches is ±90°. The dc voltage gains of all inverters are as implied by their names: below unity for the buck, above unity for the boost, and any nonnegative values for the buck-boost or flyback inverter; they are independent of the number of phases.

3.3 Small-Signal Dynamics

The starting point of dynamic analysis is the *describing equations* in the *ofb* reference frame. Although these equations have *constant* coefficients, they are *nonlinear* owing to the products between the controls and states or sources. Therefore, dynamic study is restricted to the small-signal sense: it calculates the transfer functions from various input to various output perturbations around a quiescent operating condition. Examples of the procedure have been demonstrated in Section 1.5; more results and discussions are pursued here.

First, consider the current-fed buck-boost, also representative of the boost and flyback, inverter. Its perturbed equation is the following modification of Eq. (1.34):

$$\hat{\tilde{\mathbf{x}}}_r(s) = (s\mathbf{P}_r - \tilde{\mathbf{A}}_o)^{-1}[\mathbf{A}_d\tilde{\mathbf{X}}_r\hat{d}'_e(s) + \mathbf{A}_\omega\tilde{\mathbf{X}}_r j\hat{\omega}'(s) + \mathbf{B}_d V_g\hat{d}(s) + D\mathbf{B}_d\hat{v}_g(s)] \tag{3.18}$$

where all matrices and vectors have been defined in conjunction with Eq. (1.34); the new terms model the input duty ratio d. The characteristic

polynomial of the system has been given in Eq. (1.41) and is repeated here for convenience:

$$K(s) = 1 + \left[RC + \frac{\Omega'^2 LC^2 R}{2D_e'^2} + \frac{L}{2D_e'^2 R}\right] s + \frac{LC}{D_e'^2} s^2 + \frac{LC^2 R}{2D_e'^2} s^3 \tag{3.19}$$

Three eigenvalues are expected as there are three independent states - one from the inductor and two from all the capacitors. A complete picture of pole migration as functions of steady-state parameters involves the plot of root loci or solution for the exact roots of Eq. (3.19). Fortunately, if the design allows

$$\left(\frac{\Omega'}{\omega_o}\right)^2 \ll 1 \tag{3.20}$$

where the LC corner is located at

$$\omega_o = \sqrt{2}\,\frac{D_e'}{\sqrt{LC}} \tag{3.21}$$

where the transformed duty ratio D_e' of the sinusoidally modulated duty ratios is

$$d_e' = \frac{\sqrt{M}}{2}\,\frac{2d_m'}{M} = \frac{d_m'}{\sqrt{M}} \tag{3.22}$$

it suffices to approximate the poles by

$$K(s) \approx \left[1 + \frac{s}{\omega_p}\right]\left[1 + \frac{1}{Q}\,\frac{s}{\omega_o} + \left(\frac{s}{\omega_o}\right)^2\right] \tag{3.23}$$

where

$$\omega_p = \frac{1}{RC} \quad \text{and} \quad Q = \frac{2D_e'^2 R}{\omega_o L} \tag{3.24a,b}$$

What left in the pole polynomial resembles the dynamic corners of an ideal boost-type dc converter, namely, a pair of complex LC poles directly proportional to the transformed duty ratio D_g'. Thus, a high dc gain requires a reduction of the small-signal bandwidth. A real pole also exists at the steady-state RC corner. This pole can stay dominantly below ω_0 at light load or move beyond ω_0 under heavy load.

The zeros of the current-fed topologies are of second order at most and can be cast in closed form. As an example, consider the $\hat{d}$- transfer functions important in the control of the input duty ratio of the buck-boost and flyback inverters (results for $\hat{v}_g$ are similar to those for $\hat{d}$). As can be seen from Table 3.2, these frequency responses are very simple owing to the *linear* participation of d in the describing equations. All zeros lie in the left half-plane and are relatively insensitive to operating condition. In particular, the $\frac{\hat{i}}{\hat{d}}$ response has a pair of complex zeros that cancel out the two poles and shape the high-frequency roll-off to essentially single-pole. Therefore, d is a good control parameter for fine regulation of inductor current, which relates to power or torque in ac machines, or output voltage.

Besides d, the amplitude of the duty ratio modulation is also a control variable. In the abc coordinates, it is not obvious that this quantity should be perturbed because it is overshadowed by the large-signal sinusoidal *modulation* in the duty ratios. In the ofb reference frame, however, Eq. (3.18) justifies that dynamics of *amplitude perturbation* is well-defined and easy to compute.

Function	Dc Gain	Zeros
$\frac{\hat{i}}{\hat{d}}$	$\frac{V_g}{2D_e'^2R}\left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]$	$1+\frac{1}{Q_{z3}}\frac{s}{\omega_{z3}}+\left(\frac{s}{\omega_{z3}}\right)^2$
$\frac{\hat{v}_r}{\hat{d}}$	$\frac{V_g}{2D_e'}$	$1+\frac{s}{\omega_p}$
$\frac{\hat{v}_i}{\hat{d}}$	$-\frac{V_g}{2D_e'}\frac{\Omega'}{\omega_p}$	$1+\frac{s}{\infty}$
$\frac{\hat{v}_m}{\hat{d}}$	$\frac{V_g}{2D_e'}\left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]^{1/2}$	$1+\frac{s}{\omega_{z1}}$

where $\omega_p = \frac{1}{RC}$, $\omega_{z1} = \left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]\omega_p$

$\omega_{z3} = \omega_p\left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]^{1/2}$, and $Q_{z3} = \frac{1}{2}\left[1+\left(\frac{\Omega'}{\omega_p}\right)^2\right]^{1/2}$

TABLE 3.2 $\hat{d}$-transfer functions of the buck-boost or flyback inverter.

The perturbation of modulation amplitude results in the $\hat{d}_e'$-transfer functions listed in Table 3.3. Again, the inductor current displays the most favorable dynamics of all frequency responses thanks to its two lhp zeros, one of which is stationary relative to D_e' and Ω'. All voltage formulas possess the same rhp zero that arises from some effective $\frac{L}{R}$ time constant. This zero poses problem to voltage regulation because it not only locates in the wrong half-plane, but also migrates with output frequency and modulation amplitude. Overall, $\hat{d}_e'$- dynamics are complex because d_e' comes in nonlinearly in the describing equations.

Since $\hat{\omega}'$ appears as another control parameter in Eq. (3.18), it defines yet another mode of dynamics that involves *frequency perturbation*. The corresponding transfer functions are peculiar to the inversion field and have no counterparts in the dc conversion area where ω' is not even meaningful. They are important in motor drive applications where the inversion frequency is often found in the feedback loops.

The simple appearance of $\hat{\omega}'$ in Eq. (3.18) actually conceals much more sophisticated pictures in the stationary coordinates and the transformation procedure. If the problem were to be studied by the abc equations, it would be tedious because of the complexity of the Fourier spectrum of a frequency-modulated carrier. The abc-ofb transformation relieves the difficulty by substitution of a *single scalar*, ω', for all frequency-modulated sinusoids in the exact time domain.

This simplification, however, is achieved only when *the angular velocity of the rotating axes is equal to the modulation frequency*. Thus, the ofb reference frame actually shakes with velocity $\hat{\omega}'$ while rotating at velocity

Function	Dc Gain	Zeros
$\frac{\hat{i}}{\hat{d}_e'}$	$-\frac{DV_g}{D_e'^3 R}[1+(\frac{\Omega'}{\omega_p})^2]$	$(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})$
$\frac{\hat{v}_r}{\hat{d}_e'}$	$-\frac{DV_g}{2D_e'^2}$	$(1-\frac{s}{\omega_z})(1+\frac{s}{\omega_p})$
$\frac{\hat{v}_i}{\hat{d}_e'}$	$\frac{DV_g}{2D_e'^2}\frac{\Omega'}{\omega_p}$	$(1-\frac{s}{\omega_z})$
$\frac{\hat{v}_m}{\hat{d}_e'}$	$-\frac{DV_g}{2D_e'^2}[1+(\frac{\Omega'}{\omega_p})^2]^{1/2}$	$(1-\frac{s}{\omega_z})(1+\frac{s}{\omega_{z1}})$
where $\omega_p = \frac{1}{RC}$, $\omega_{z1} = [1+(\frac{\Omega'}{\omega_p})^2]\omega_p$		
$\omega_{z2} = 2\omega_p$, and $\omega_z = \frac{2D_e'^2 R}{[1+(\frac{\Omega'}{\omega_p})^2]L}$		

TABLE 3.3 $\hat{d}_e'$*-transfer functions of the buck-boost or flyback inverter.*

Ω'! This locking property between the transformation and the stationary waveforms allows an observer in the rotating coordinates to see only ω' instead of all the fluctuations caused by ω'.

The $\hat{\omega}'$- transfer functions are summarized in Table 3.4. Note that since the real part V_r of the voltage phasor is independent of Ω', the dc gain for $\frac{\hat{v}_r}{\hat{\omega}'}$ is zero, as is confirmed by the zero at the origin in the frequency response; thus, the quotation marks in the gain column signify a pseudo dc gain. Most interesting is $\frac{\hat{v}_i}{\hat{\omega}'}$ with a pair of complex zeros that station in the left half-plane when Ω' stays below ω_p, but drift into the right half-plane as soon as Ω' passes ω_p. The cure for these potential rhp zeros is the placement of the RC corner beyond the range of operating frequencies.

Transfer functions for the buck inverter have also been developed but are not presented here because their significance does not deserve more space. Their closed-form solutions for dynamic corners are formidable since the polynomials involved are at least of third order. The difference in orders of the voltage-fed and current-fed topologies also forbids meaningful comparison of small-signal results for these two classes of inverters.

In general, dynamic bandwidth is finite owing to the reactive elements in the network. Nevertheless, this bandwidth can be made very wide by reduction of the filter size or increase of the switching frequency. Thus, the sluggishness of the current-source inverter, caused by a large dc choke, is not a problem for fast-switching inverters. In high-power applications, the load eventually imposes its own dynamics on the entire inverter-load combination.

Function	Dc Gain	Zeros
$\frac{\hat{i}}{\hat{\omega}'}$	$\frac{DV_g}{D_e'^2 R}\frac{\Omega'}{\omega_p^2}$	$(1+\frac{s}{\omega_{z2}})$
$\frac{\hat{v}_r}{\hat{\omega}'}$	$-\frac{DV_g}{D_e'}\frac{\Omega'}{\omega_o^2\omega_p}$	$s\,(1+\frac{s}{\omega_{z2}})$
$\frac{\hat{v}_i}{\hat{\omega}'}$	$-\frac{DV_g}{2D_e'\omega_p}$	$1+\frac{1}{Q_q}\frac{s}{\omega_o}+(\frac{s}{\omega_o})^2$
$\frac{\hat{v}_m}{\hat{\omega}'}$	$\frac{DV_g}{2D_e'}\frac{\Omega'}{\omega_p^2[1+(\frac{\Omega'}{\omega_p})^2]^{1/2}}$	$(1-\frac{s}{\omega_z})$
where $\omega_{z2}=2\omega_p$, $\omega_z=\frac{2D_e'^2R}{[1+(\frac{\Omega'}{\omega_p})^2]L}$		
$\omega_o=\frac{\sqrt{2}D_e'}{\sqrt{LC}}$, and $Q_q=\frac{2D_e'^2R}{\omega_o L[1-(\frac{\Omega'}{\omega_p})^2]}$		

TABLE 3.4 $\hat{\omega}'$-transfer functions of the buck-boost or flyback inverter.

Implied in the wide-band property is the advantage that *the small-signal bandwidth can be much higher than the inversion frequency*. Thus, if the inverter switches at 20 kHz, the dynamic corners can be at 1 kHz while the output sine waves are at only 100 Hz. Furthermore, the dynamic information within and above this bandwidth can be predicted with a high degree of accuracy, the range of validity and the tolerance being limited solely by the switching frequency. This benefit is not shared by six-stepped inverters: if a voltage-source inverter outputs, say, 100 Hz, its bandwidth is neither meaningful nor predictable above 50 Hz (an optimistic figure!).

To summarize, the principal contributions of this section are not the locations of the poles and zeros of the circuits, especially since the load is only resistive. The points to be remembered are the *definition* of dynamics and the *procedure* to solve for the transfer functions. The tool employed is the describing equation technique coupled with the stationary-to-rotating coordinate transformation. The result is an accurate description of the small-signal information over the broad dynamic range of these fast-switching inverters.

3.4 Canonical Model

The canonical model is a *linear*, *time-invariant* representation of the *linearized* describing equations in the rotating reference frame. The procedure to establish the model for the boost inverter has been detailed in Section 1.6. More results for other current-fed and voltage-fed topologies are presented and commented on below.

The model for the buck-boost inverter, typical of current-fed structures, is the modified Fig. 1.4 and is sketched in Fig. 3.9 with the following identification:

$$\tilde{\imath} = D_e' i + I \hat{d}_e' - jC\tilde{V}_b \hat{\omega}' \tag{3.25a}$$

$$\tilde{v}_f' = \tilde{v}_f - j \frac{DV_g}{D_e'} \frac{RC\hat{\omega}'}{1+(s-j\Omega')RC} \tag{3.25b}$$

$$L_e = \frac{L}{D_e'^2}, \quad \tilde{e} = \frac{V_g}{D}, \quad \tilde{e}' = \frac{D_e'}{D} sL_e I - \frac{V_g}{D_e'} \tag{3.25c,d,e}$$

$$\tilde{\lambda}' = -j\,RC \left[\frac{V_g}{1+(s-j\Omega')RC} + \frac{D_e'}{D} \tilde{V}_b \frac{sL_e}{R} \right] \tag{3.25f}$$

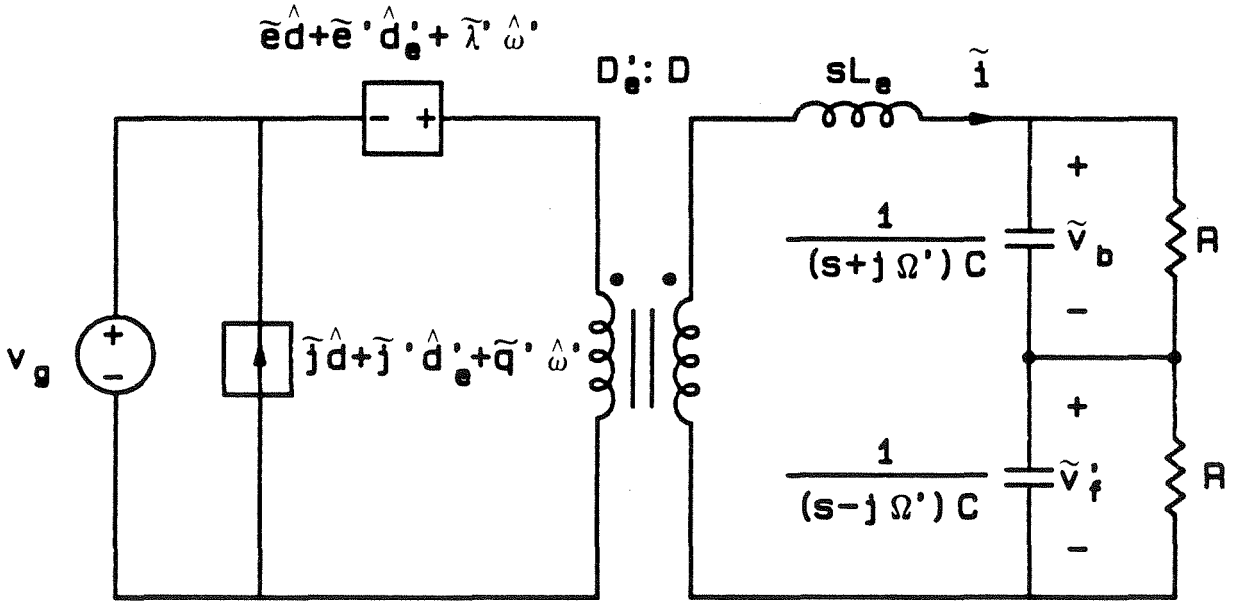


Fig. 3.9 Linearized, continuous, and time-invariant model of the current-fed boost, buck-boost, and flyback inverters showing excitation and control generators, an inversion transformer, and a complex low-pass filter.

$$\tilde{j} = -I \ , \quad \tilde{j}' = \frac{D}{D_e'} I \ , \quad \text{and} \quad \tilde{q}' = -j \frac{D}{D_e'} C\tilde{V}_b \qquad \text{(3.25g,h,i)}$$

The model highlights the principal functions of a power processor, namely, the *inversion mechanism* and *low-pass filtering action*. The inversion process, done by the switches in the topology, is characterized partly by an *ideal transformer*. The *inversion ratio* of the transformer is related directly to the *constant* input duty ratio and transformed duty ratio (proportional to the modulation amplitude) of the switches. The low-pass filter consists of a real inductor feeding into a pair of *complex-conjugate* capacitors connected in *series*. The inductor has only a real part sL_e, which corresponds to *dynamic inductive reactance*, because its steady-state reactance is zero. Each capacitor, on the other hand, consists of both a real part sC, which signifies *dynamic capacitive susceptance*, and an imaginary part $\Omega' C$, which characterizes *steady-state capacitive susceptance*. The steady-state susceptance exists to model the states that are time-varying under quiescent condition.

The series connection of the capacitive impedances with the polarities shown reduces the *complex* output voltages to a *real* voltage that is then seen by the input section, which consists of only real components under steady-state condition. Complex modeling thus reflects truly the switching phenomenon that matches polyphase ac, represented by phasors, at the output to single-phase dc, characterized by a scalar, at the input of the physical topology.

There are three *voltage generators* and three *current generators* associated with three control parameters d, d_e', and ω'. As the filter, these dependent sources are generally complex. While some merely modify the dc gains, others affect the zeros of the frequency responses. It must be cautioned that they are *not* totally responsible for the zeros of the system: their coefficients interact with the complex transfer function of the output filter to determine the zeros of the responses.

The steady-state version of Fig. 3.9 can be extended to the model in Fig. 3.10 to treat the steady-state solution of a buck-boost inverter driving a *general impedance* $\tilde{Z}_b$. The impedance $\tilde{Z}_b$ is actually the parallel combination of the steady-state capacitive reactance of the inverter and the per-phase impedance of the generalized load. Its complex conjugate $\tilde{Z}_f$ is also present in *series* so that reactive power is confined within the inverter

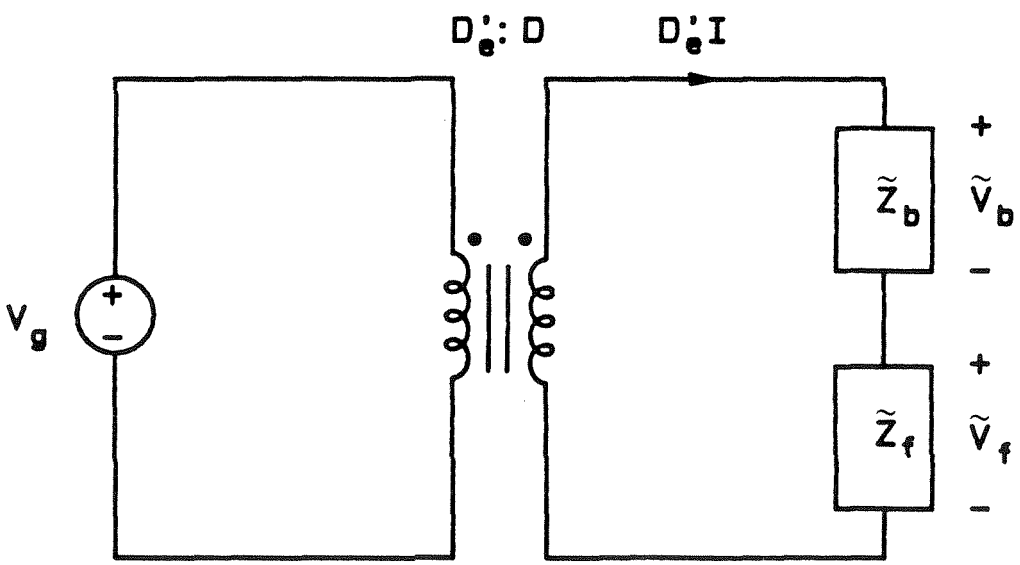


Fig. 3.10 Steady-state model of a flyback, or boost or buck-boost, inverter driving an arbitrary impedance $\tilde{Z}_b$.

and only *real* power is drawn from the dc source.

From Fig. 3.10, the backward voltage phasor is

$$\tilde{V}_b = \frac{D}{D_e'} \frac{V_g}{2} \frac{e^{j\Phi_z}}{\cos\Phi_z} \tag{3.26}$$

where

$$\tilde{Z}_b = Z e^{j\Phi_z} \tag{3.27}$$

Note that the amplitude of $\tilde{V}_b$ is *inversely* proportional to the *cosine* of its phase which, in turn, is identical to the *phase of* $\tilde{Z}_b$. If the load has poor power factor within the frequency range of interest, some shaping of $\tilde{Z}_b$ is necessary to avoid small $\cos\Phi_z$ and large output voltage.

If D equals unity, Eq. (3.26) describes the capacitor voltage of a boost inverter. The boost gain is thus influenced by two parameters, namely, the modulation amplitude and the cosine of the load angle (assuming the capacitance is negligible). The modulation amplitude alone makes the output of a boost inverter fed by the rectified line voltage higher than the line itself. Such an excessive amplitude inevitably saturates ac machines designed to take only line conditions. Therefore, the buck-boost or flyback topology, which allows an attenuation of the source through the input duty ratio d, is more suitable for motor drives.

The inverse dependence on cosine of the load angle shapes the amplitude response into a direction generally objectionable to the load itself. Hence, feedback of load data to determine d or d_e', or some equivalent action, is essential in constructing a prescribed output.

The canonical model for the buck inverter is illustrated in Fig. 3.11 with the following specifications:

$$\tilde{\imath}_b' = \tilde{\imath}_b - jC\tilde{V}_b\hat{\omega} \quad , \qquad \tilde{e}_b = \frac{V_g}{D_e} \tag{3.28a,b}$$

where $\tilde{\imath}_b$ is the backward inductor current phasor, and $\tilde{v}_b$ the backward capacitor voltage phasor;

$$\tilde{\lambda}_b = \frac{L}{D_e}\left[\Omega C\tilde{V}_b - j\left(\tilde{I}_b + sC\tilde{V}_b\right)\right] \tag{3.28c}$$

$$\tilde{\jmath} = -\left(\tilde{I}_b + \tilde{I}_f\right) \quad , \text{ and } \quad \tilde{q} = -jD_eC\left(\tilde{V}_b - \tilde{V}_f\right) \tag{3.28d,e}$$

where the *transformed duty ratio* d_e for the buck topology is the ofb transformation of the effective duty ratio d_w defined in Eq. (3.2):

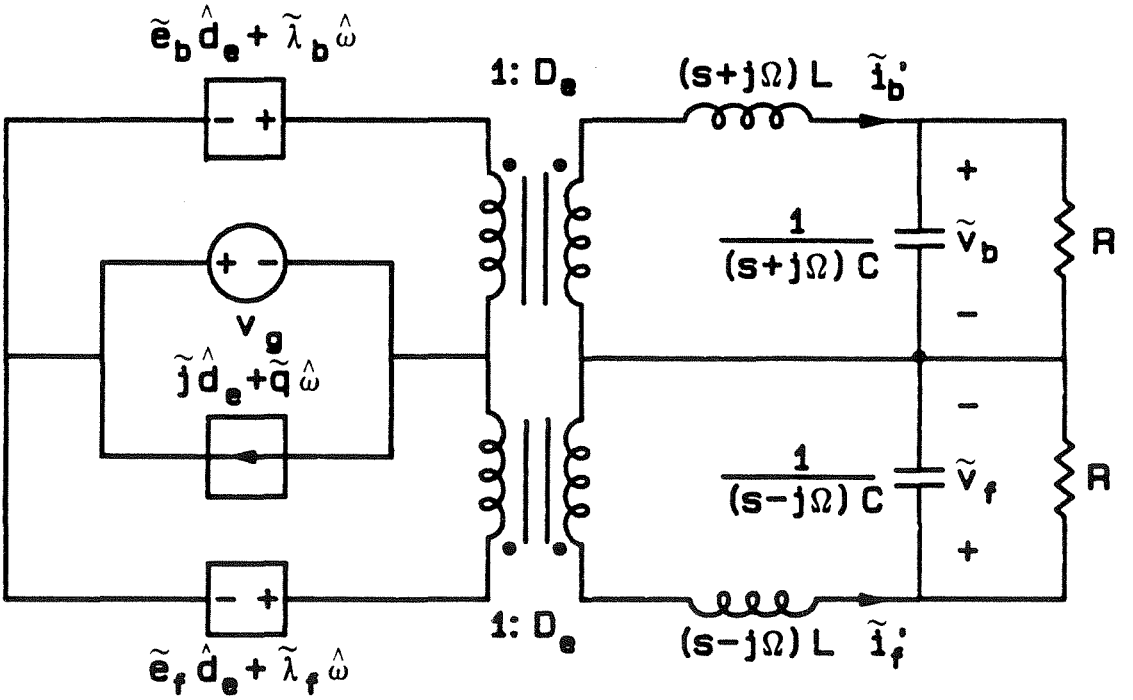


Fig. 3.11 Linearized, continuous, and time-invariant model of the voltage-fed buck inverter showing excitation and control generators, inversion transformers, and complex low-pass filters.

$$d_e = \frac{\sqrt{M}}{2}\,\frac{d_m}{2} = \frac{\sqrt{M}\,d_m}{4} \tag{3.29}$$

Canonical properties still include the input generators, ideal transformers, and complex low-pass filters. The *current generators* have to be as specified in Eqs. (3.28d,e) to model the *source current* accurately. The *inversion ratio* of the transformers is simply the steady-state transformed duty ratio, related to the effective modulation amplitude and number of phases according to Eq. (3.29). Both inductive and capacitive reactances are *complex* because inductor and capacitor states are sinusoidal in the real inverter. Note that the inductor currents in the model and in the actual circuit *differ*: they are related by Eq. (3.28a); the difference exists so that the voltage phasor is faithfully preserved and all controlled generators are merged into the primary side of the transformer. The transfer function of the filter and coefficients of the controlled sources together determine the corners of the frequency responses.

As is obvious from the two *decoupled* complex-conjugate halves of Fig. 3.11, the backward and forward components of the buck inverter do *not* interact. Thus, if only the inductor current phasor $\tilde{i}_b$ or capacitor voltage phasor $\tilde{v}_b$ needs be solved, any half-circuit suffices. *Both* half-circuits, however, must be *paralleled in front of the source* as shown in Fig. 3.11 so that the imaginary parts of the complex-conjugate currents on the source (primary) sides of the transformers cancel out and only *real* current is drawn from the source. This parallel connection thus models the *rectification* of the *sinusoidal* inductor currents into the *dc* source current by the switches. Note that if a source impedance is present, the forward

and backward circuits interact and must be both included.

If the generalized load $\tilde{Z}_b$ in the previous buck-boost example is applied to Fig. 3.11, Fig. 3.12 results under steady-state condition. Again, $\tilde{Z}_f$ is effectively in *parallel* with $\tilde{Z}_b$ so that reactive power is confined within the inverter and only *real* power is extracted from the dc supply. The voltage phasor $\tilde{V}_b$ is obviously

$$\tilde{V}_b = D_e V_g \frac{\tilde{Z}_b}{\tilde{Z}_b + j\Omega L} \tag{3.30}$$

In practical situations where $j\Omega L$ is negligible compared to $\tilde{Z}_b$, the phasor amplitude is $D_e V_g$ regardless of the operating frequency: the inverter behaves more as a voltage source. This voltage-fed topology is thus easier to use than the current-fed configurations considered earlier. Nevertheless, it

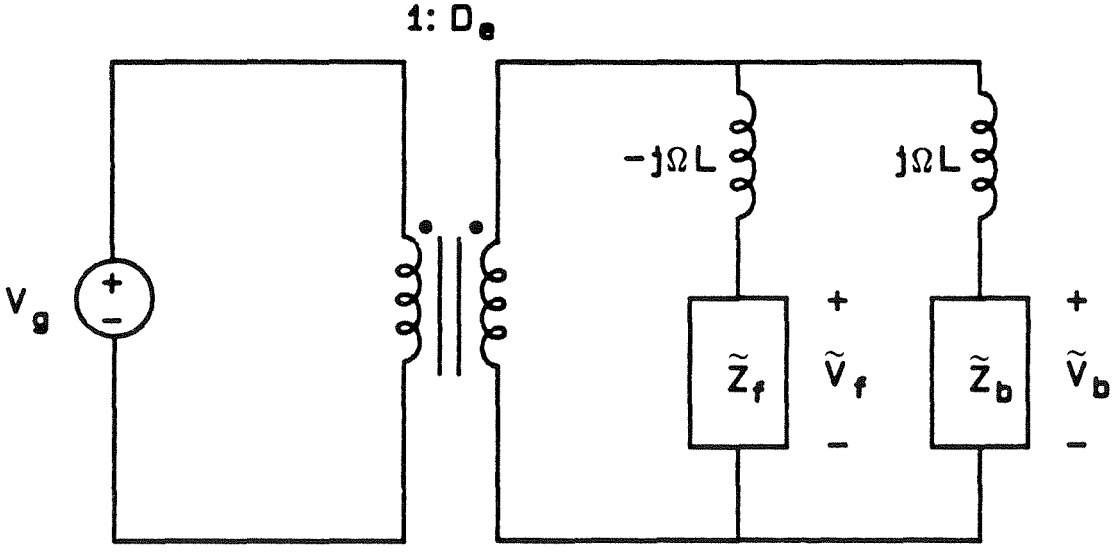


Fig. 3.12 Steady-state model of a buck inverter driving an arbitrary impedance $\tilde{Z}_b$.

only steps down, and its peak amplitude is only $\frac{V_g}{2}$ (for continuous sinusoidal PWM). Therefore, practical applications prefer the *boost-buck*, the dual of the buck-boot, or *isolable boost-buck*, the dual of the flyback, to the original buck inverter.

A comparison of Figs. 3.10 and 3.12 shows the distinction between current-fed and voltage-fed topologies. In the former case, the input voltage is applied to the load *and its complex conjugate*, instead of the load itself; the load is thus fed by the source *current*, rather than the source voltage. In the later case, the dc voltage is applied directly to the load through a small filter reactance; the load is thus fed by the source *voltage* itself if the filter is small.

If the models are interpreted in the reverse direction, however, forward voltage-fed inversion becomes reverse current-fed rectification, and vice versa. Reverse current rectification in the buck inverter is represented by the *parallel* connection of the forward and backward inductor *currents*. Reverse voltage rectification in the buck-boost (or boost and flyback) topology, on the other hand, is embodied in the *series* connection of the forward and backward capacitor *voltages*.

In conclusion, this chapter has described the *buck*, *boost*, *buck-boost*, and *flyback* examples of *fast-switching sinusoidal PWM inverters*, where "sinusoidal" is the quality of both control and output waveforms. The arrangement of reactive elements and switches has been specified for any number of output phases greater than one. The throws in an M-phase buck inverter are grouped into M *double-throw* switches for forward *voltage* inversion and reverse current rectification. Those in an M-phase boost

topology are classified as *two M-throw* switches for forward *current* inversion and reverse voltage rectification.

Switch specification has been in terms of *duty ratios* since they are the ultimate control variables. Simplicity dictates that each duty ratio consists only of a dc component and a *sinusoidal* modulation. Owing to high switching frequency, a given gain function can be realized by several duty ratio assignments, each of which, in turn, can be implemented by a variety of switching functions. Thus, the independent switches in a topology can be driven by a multitude of simple strategies that are free from synchronization constraints.

The duty ratios are used to derive the *describing equations* of the inverters in the abc reference frame. These equations are next transformed to the *ofb coordinates* where they have *constant* coefficients. The ofb describing equations are then solved for steady-state, small-signal dynamic, and canonical models.

Steady-state results generally depend on circuit impedances, which involve the inversion frequency and reactive components of the inverter and load. This dependence leads to unexpected steady-state frequency responses, such as the buck-boost amplitude response that blows up when the power factor seen by the switches approaches zero. The dc gains of all topologies are as implied by their names.

Definition of dynamics is clear in the rotating coordinates owing to the correct identification of control parameters. The transfer functions in the inverters exemplified originate from the small-signal perturbations in the *dc duty ratio*, the *modulation amplitude* and *frequency* of the ac duty ratios, and the *dc line*. Dynamic corners are generally sensitive to quiescent

operating condition if the system equation is nonlinear.

Two distinct canonical models have been developed: one for the *voltage-fed* (buck-type) and the other for the *current-fed* (boost-type) topologies. Controlled generators, inversion transformers, and low-pass filters are arranged properly to identify input and output variables, account for steady-state and dynamic behavior, and reflect the physical inversion process. Forward and backward *currents* are connected in *parallel* to characterize the forward voltage inversion and reverse current rectification in the voltage-fed inverter. Forward and backward *voltages* are connected in *series* to model the forward current inversion and reverse voltage rectification in the current-fed inverter.

CHAPTER 4

PRACTICAL ASPECTS OF FAST-SWITCHING SINUSOIDAL PWM INVERTERS

This chapter consists of four sections. The first section *realizes the switches* for three-phase versions of the topologies described in the preceding chapter. Some *modulation strategies* for these switches for both forward and reverse energy transfers are discussed; attention is called to the *six-stepped PWM* scheme. The second section incorporates *isolation* into the original inverters and introduces some other isolable circuits. The third section defines the *measurement* problem: how waveforms should be conditioned so that their steady-state and dynamic information can be extracted by standard techniques established for dc converters. The last section applies the measurement procedure to confirm theoretical results predicted for an *experimental three-phase flyback inverter*.

4.1 Three-Phase Implementation

This section is divided into three parts. The first one *implements the switches* in the buck and buck-boost inverters with transistors and diodes and tabulates the stress on these components using the steady-state formulas developed in Section 3.2. The second describes some *continuous* and *piecewise continuous modulation policies* for the switching functions. The last subsection modifies the drive or the switches themselves so that the inverter is ready for *regeneration*.

4.1.1 Switch Realization and Stress

The high-quality waveforms in the topologies described earlier require fast semiconductor devices. At the present, the bipolar transistor (BJT), field-effect transistor (FET), and gate-turned-off thyristor (GTO) have the right combination of speed, for the theory to be valid, and power, for the circuit to be useful. The bipolar transistor is exemplified here although the FET should be considered for speed and the GTO for power.

Switches in an inverter are generally *two-quadrant* in either voltage or current. Those in a voltage-fed, such as buck, topology are *current-two-quadrant* because they block *dc* voltage and conduct *ac* current. Those in a current-fed, such as boost, buck-boost, or flyback, circuit are *voltage-two-quadrant* since they conduct *dc* current and block *ac* voltage.

A current-two-quadrant throw is implemented by anti-parallel connection of a transistor and a diode. Six such throws are used to realize a three-phase buck inverter in Fig. 4.1. From the circuit, the voltage stress of the transistor and diode is V_g (Table 4.1), and the current stress the peak inductor current (Table 3.1). Note that even though each throw is only two-quadrant, the whole bridge is *four-quadrant*, i.e., both line current and voltage of the bridge are *bidirectional*.

The switch configuration of Fig. 4.1 has been frequently criticized for its *shoot-through* faults. The fault occurs when two transistors of the same switch are simultaneously on - because the storage time of the base-emitter junction keeps the out-going transistor on while it is supposed to be off - and short out the power supply. The problem can be cured by providing some dead time so that one transistor is completely deactivated

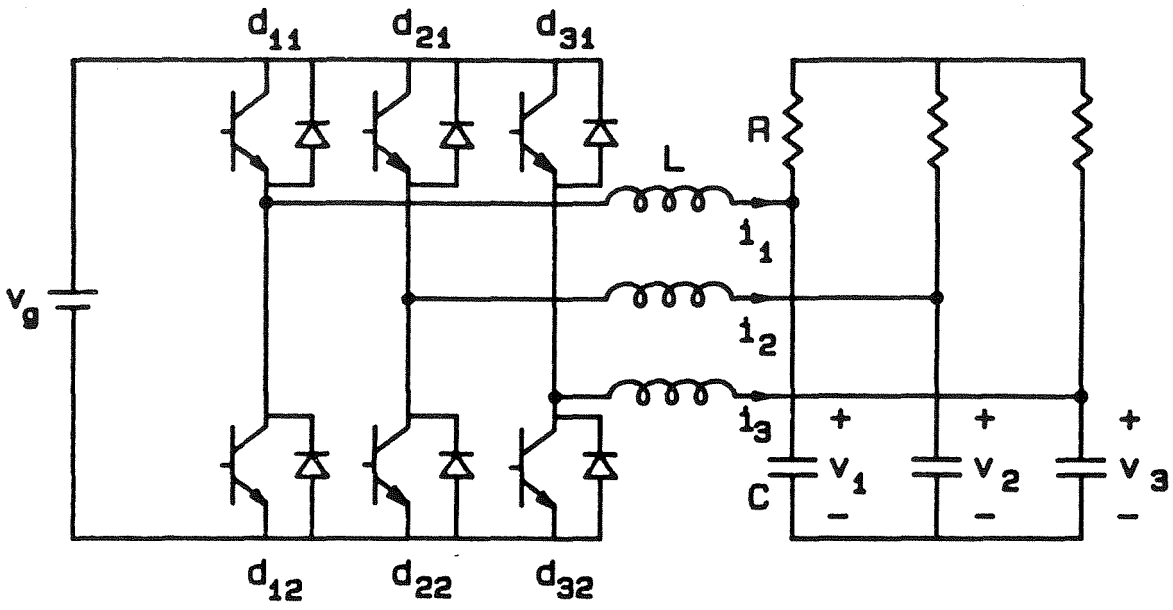


Fig. 4.1 Three-phase buck inverter with each current-two-quadrant throw realized by a transistor and a diode in anti-parallel.

before the other comes in; the diodes free-wheel the inductor current during this time.

Another drawback from the use of BJT in Fig. 4.1 is the cross-over distortion born from the difference in finite drops across the transistor and diode. This distortion, however, is not a major concern in high-voltage applications. The problem does not exist if FET is used because the FET, its drop being lower than that of the diode, always conducts at cross-over.

A voltage-two-quadrant throw is built from series connection of a transistor and a diode. Six such throws are used to realize the output switches of a buck-boost inverter in Fig. 4.2. The voltage stress across each output transistor or diode is the line voltage $\sqrt{3}\,V$ (Table 4.1), and the

Inverter	Input		Output	
	Transistor	Diode	Transistor	Diode
Buck	V_g	V_g		
Boost			$\sqrt{3}\,V$	$\sqrt{3}\,V$
Buck-boost	V_g	V_g	$\sqrt{3}\,V$	$\sqrt{3}\,V$
Flyback	$\sqrt{3}\,V + V_g$	$\max\,(\sqrt{3}\,V - V_g, 0)$	$\sqrt{3}\,V$	$\sqrt{3}\,V$

TABLE 4.1 Voltage stresses across the transistors and diodes of the buck, boost, buck-boost, and flyback inverters.

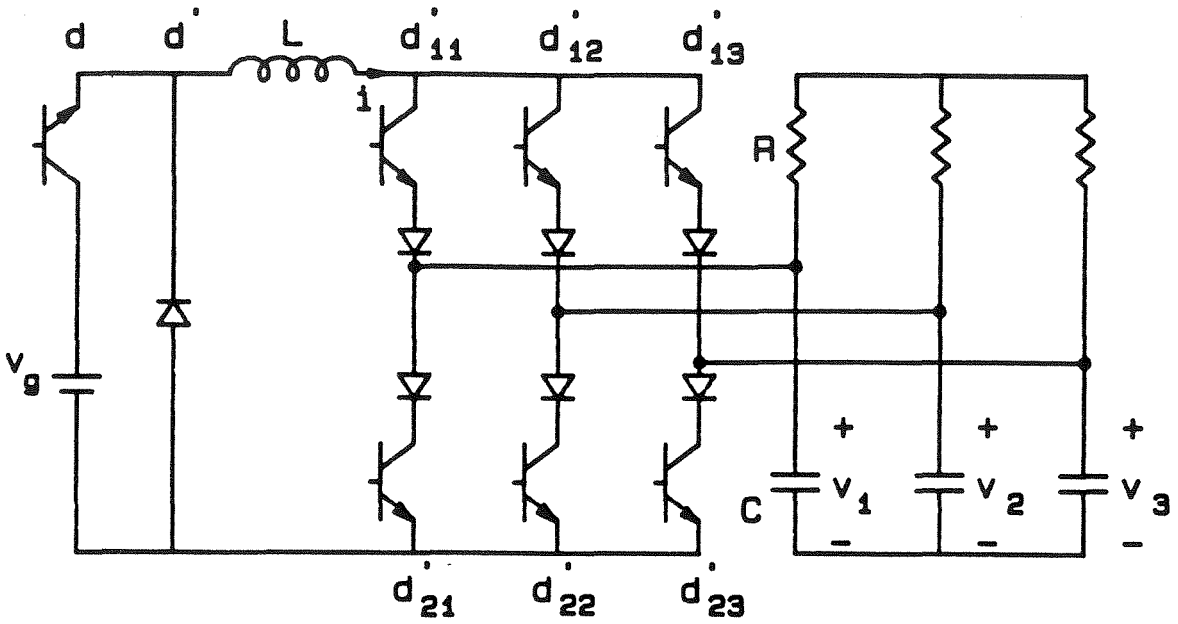


Fig. 4.2 Three-phase buck-boost inverter with each voltage-two-quadrant throw realized by a transistor and a diode in series.

current stress the inductor current (Table 3.1). The input transistor and diode in the same picture create the one-quadrant throws of the input switch; they have to block V_g and carry the inductor current. Note that the six output throws considered together are actually *four-quadrant* although each throw is only two-quadrant.

The practical implementation of current-fed switches is *free from shoot-through faults*: any number of throws of the same switch can be simultaneously on without any destruction since the back-to-back diodes prevent current to circulate within the throws. This is why the current-source inverter has been hailed for its ruggedness. In contrast to the buck case, no dead time is allowed; in fact, some *overlapping* interval may be

needed to guarantee the inductor current always has some place to flow to.

It has been shown that the inductor current is always *dc* even though the load currents, being ac, do pass through zero. Therefore, the output of boost-type inverters is *free from cross-over distortion*.

Voltage stresses for the buck, boost, buck-boost, and flyback topologies are compared in Table 4.1, where the line amplitude has been provided by Table 3.1. Current stress is simply the peak inductor current, the sum of the ideal amplitude in Table 3.1 and ripple magnitude.

4.1.2 Modulation Strategies

The PWM process involves two different time scales: a *fast* one at the *switching* frequency and a *slow* one at the *modulation* frequency. Both of these should be concurrently displayed if the switching and modulation processes are to be correlated. The specification of drive strategies for ac converters thus requires a graph that displays high-frequency information on one axis and low-frequency information on the other. Such a graph is the *switching diagram*.

As an example, consider the description of *continuous sinusoidal PWM* for the two triple-throw switches in a boost inverter. Suppose an effective modulation amplitude of $\frac{D_m'}{3}$, where $D_m' \leq 1$, is desired. Many sets of d_{kw}' specified in Eq. (3.8) provide this amplitude, and one that simplifies circuitry is

$$d_{1w}' = \frac{1}{3} + \frac{D_m'}{3} \cos\left[\Omega' t - (w-1)\frac{2\pi}{3}\right] \tag{4.1a}$$

and

$$d'_{2w} = \frac{1}{3} \quad , \qquad 1 \le w \le 3 \tag{4.1b}$$

Since switching harmonics are strongly attenuated if they are much higher than filter corners, the above duty ratios can be realized by a variety of switching functions. One that is easy to build simply has each switch start a cycle at phase 1, move to phase 2, and end at phase 3 with the prescribed duty ratios (any other two completely random sequences also qualify).

All the aforementioned details, and many more, are delineated compactly in the switching diagram of Fig. 4.3. The *horizontal* axis of the diagram uses the *slow* time scale $\frac{2\pi}{\Omega'}$ to encompass *all switching cycles* within *one modulation period*. Each point on the axis thus represents a compressed switching period as the switching frequency approaches infinity. Switching instants and duty ratios within each switching period are stretched

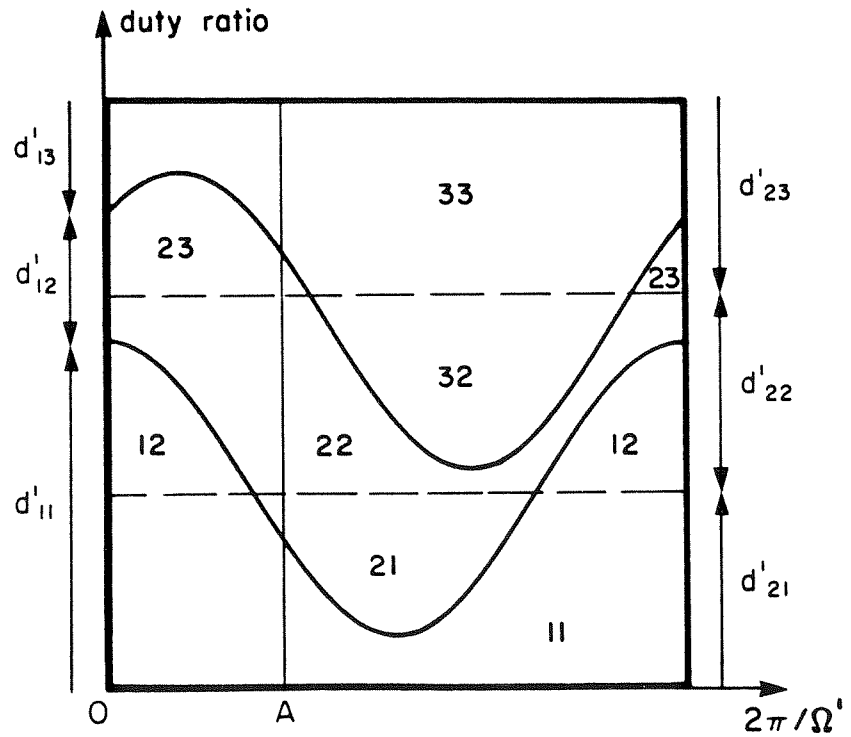


Fig. 4.3 Switching diagram for continuous PWM of a boost inverter showing switch 1 modulated by continuous sinusoids and switch 2 not modulated.

out and exposed on the *vertical* axis, which is then the *fast* duty ratio (or time normalized to the switching period) scale.

On a switching diagram, each *independent throw* is characterized by its *duty ratio curve* that describes its *duty ratio* as well as *switching instants*. Since the boost inverter has four independent throws, four curves exist on the diagram. The lower solid one describes $d_{11}^{'*}$, and its distance from the *bottom* axis is $d_{11}^{'}$ (Eq. (4.1a)); the upper solid one $d_{13}^{'*}$, and its distance from the *top* axis $d_{13}^{'}$; the space between these two curves $d_{12}^{'*}$, and the distance $d_{12}^{'}$. The dashed curves carry the same connotation, but for the second switch.

The switching diagram identifies all *switched topologies* that exist with a given drive scheme and all *combinations* of these topologies that can be found over *all time*. There can be as many switched topologies as there are areas on the diagram. Each topology is recognized by a double-digit number because there are two switches; the first digit specifies the active throw of the first switch, and the second digit the active throw of the second switch. For instance, "21" is the topology with the first switch (first digit) at the second output ("2") and the second switch (second digit) at the first output ("1"), as is shown in Fig. 4.4b. The combination of topologies in any switching period consists of the areas traversed by a vertical line drawn at the point representing that period. For instance, the sequence at cycle A consists of five topologies 11, 21, 22, 23, and 33, as are listed in Fig. 4.4. If duty ratio curves are specified, switched topologies (or areas) can be deduced, and vice versa. Duty ratio and topology designations are thus equivalent and can be used interchangeably. The second method, however, is

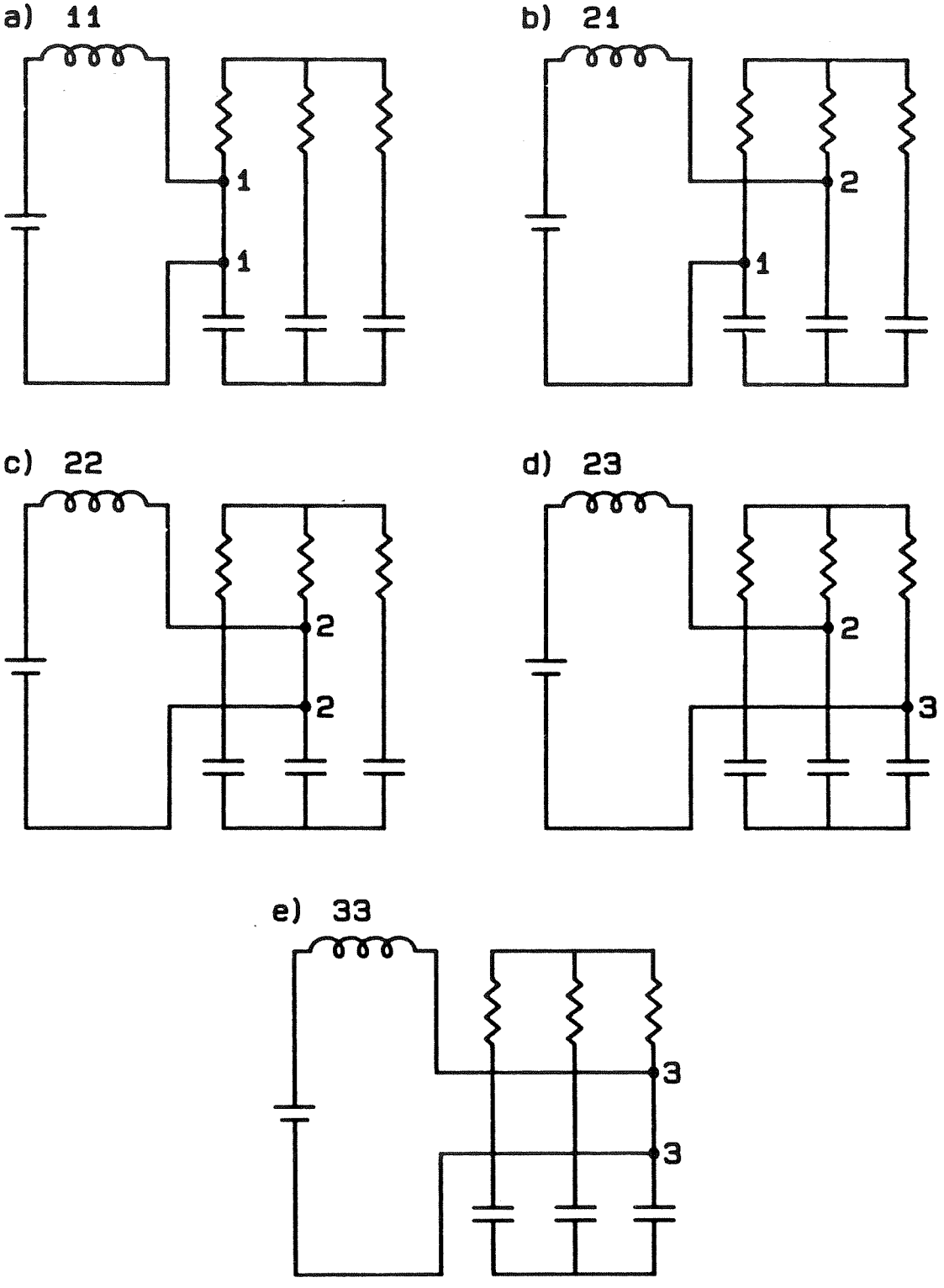


Fig. 4.4 Five switched topologies at cycle A of Fig. 4.3.

more convenient for piecewise continuous duty ratios.

It can be observed from Figs. 4.3 and 4.4 that continuous PWM is inefficient because there are so many idling intervals during which no power is transferred to the load. This is why the peak output current of the boost inverter is only $\frac{2}{3}(\approx .67)I$ while that of the current-source inverter is $\sqrt{3}\frac{2}{\pi}(\approx 1.1)I$, where I is the inductor current in both cases. The output of the former, however, is sinusoidal while that of the latter is six-stepped. It is thus desirable to have another switching scheme that combines the sinusoidal quality of the boost and high amplitude of the current-source inverter. This unique scheme is called *six-stepped PWM* - the name reflects the union between *piecewise sinusoidal PWM* and *six-stepped symmetry*, which has been beautifully exploited in slow-switching inverters.

As is introduced in Fig. 4.5, six-stepped PWM divides each inversion cycle into *six equivalent intervals.* In each interval, one switch stays *stationary* on one of the three capacitors while the other sweeps through all three. The *positions* of the stationary switch as well as the throws of the sweeping one are determined by *six-stepped* sequence. For instance, switch 1 feeds the inductor current into phase 1 while switch 2 pulls current out of phases 2, 3, and 1, in that order, in interval 1; this sequence then permutates in a three-phase, six-stepped manner throughout the remaining five intervals and repeats itself at the end of the sixth interval.

In interval n or n', where $1 \le n \le 3$, the throw kw connected without modulation to one of the capacitors is the one with

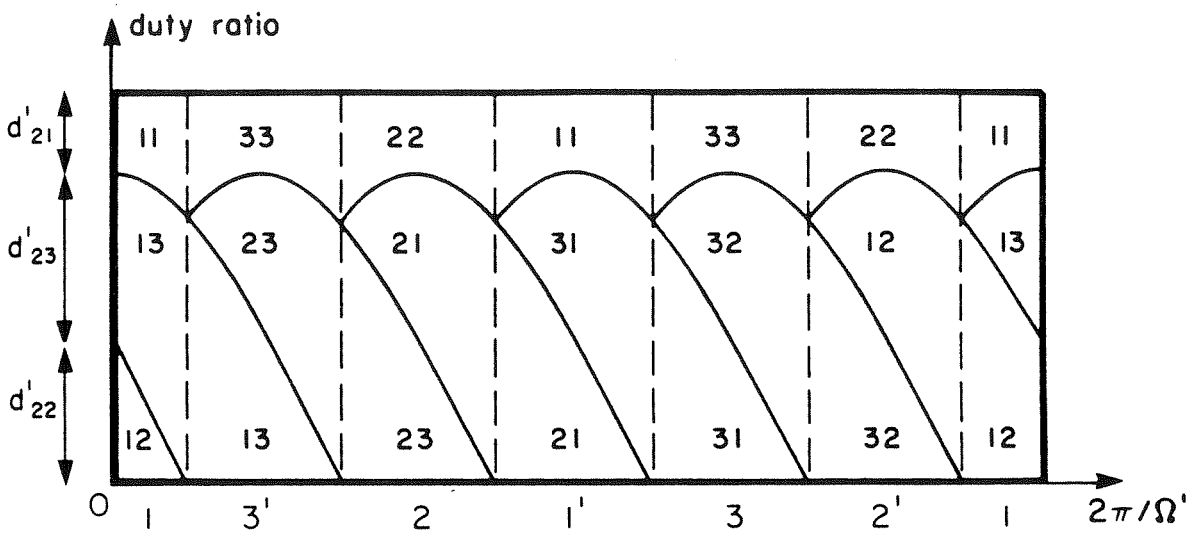


Fig. 4.5 Switching diagram for six-stepped PWM of a boost inverter showing two sinusoidal segments used to modulate all throws.

$$w = n \quad \text{and} \quad k = \begin{cases} 1 & \text{in interval } n \\ 2 & \text{in interval } n' \end{cases} \tag{4.2a,b}$$

The throw $k_1 w_1$ that is modulated by

$$d'_{k_1 w_1} = d'_m \cos\theta' \quad , \qquad 30° \le \theta' < 90° \tag{4.3}$$

is the one with

$$k_1 = \begin{cases} 2 & \text{in interval } n \\ 1 & \text{in interval } n' \end{cases} \quad \text{and} \quad w_1 = \begin{cases} w+1 & \text{if } w = 1,2 \\ 1 & \text{if } w = 3 \end{cases} \tag{4.4a,b}$$

The throw $k_1 w_2$ that is modulated by

$$d'_{k_1 w_2} = d'_m \cos(\theta' - 120°) \quad , \qquad 30° \le \theta' < 90° \tag{4.5}$$

is the one with

$$w_2 = \begin{cases} w_1+1 & \text{if } w_1=1,2 \\ 1 & \text{if } w_1=3 \end{cases} \tag{4.6}$$

These *same* two functions are used for all six intervals, the two throws receiving them being picked by six-stepped rotation.

From the above duty ratio specification, the *effective duty ratio* in *any* interval is

$$d_w' = d_{1w}' - d_{2w}' = d_m' \cos[\theta' - (w-1)\frac{2\pi}{3}] , \quad 1 \le w \le 3 \tag{4.7}$$

The effective modulation amplitude is now d_m' instead of merely $\frac{2}{3} d_m'$ as is given by Eq. (3.10) for continuous PWM. Therefore, if the inductor current is I, the peak output current is also I, very competitive with the $1.1\,I$ of the current-source inverter; the minimum dc gain is lowered to $\frac{2}{3}$ from the 1 obtained in continuous PWM. Note that *sinusoidal quality* is still *preserved* with this improvement because all equations for continuous and six-stepped PWM are *identical in form*, the *only difference* being the increase in effective modulation amplitude.

Six-stepped PWM also applies to the three-phase buck inverter. The interpretation of the buck six-stepped PWM, however, is *different* from that just discussed because the six throws in Fig. 4.1 are grouped into three voltage-fed double-throw switches, instead of two current-fed triple-throw switches. Therefore, although the modulation curves in Fig. 4.6 are identical to those in Fig. 4.5, the areas there have new meaning. Each area is identified by three digits because there are three independent switches.

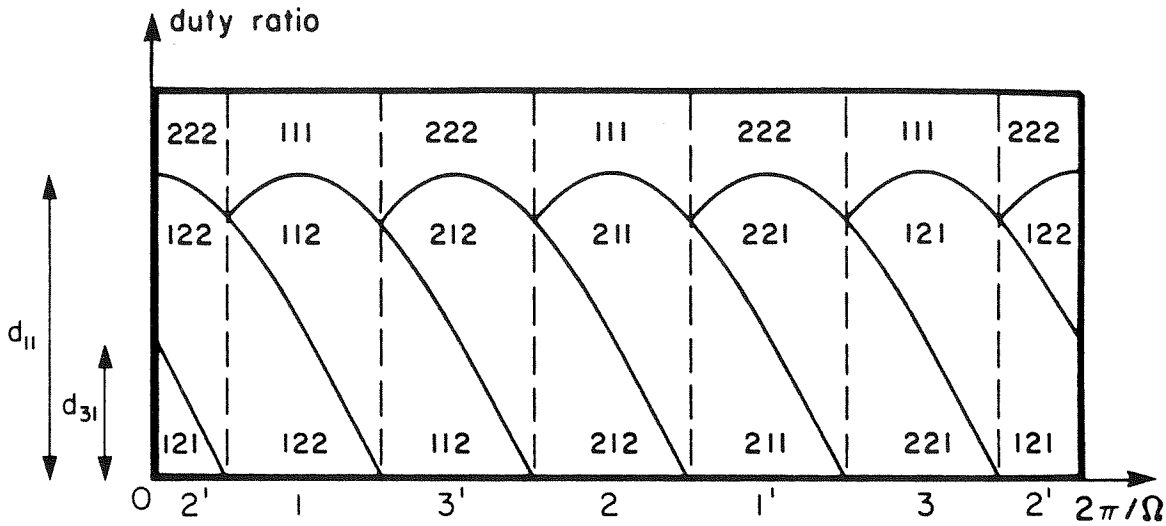


Fig. 4.6 Switching diagram for six-stepped PWM of a buck inverter showing two sinusoidal segments used to modulate all throws.

Each digit is either 1, for the positive end of the source, or 2, for the negative end.

Again, every modulation cycle consists of six 60° intervals. In each interval, one switch is permanently attached to either end of the supply while the other two are switched back and forth between the source terminals. In interval 2, for instance, switch 2 is stationary at the positive end of V_g while switches 3 and 1 start the switching period at end 2 of the supply and terminate at end 1. The roles of the throws are permutated throughout six intervals according to *six-stepped* sequence.

In interval n or n', where $1 \le n \le 3$, the throw wk that is connected without modulation to one source terminal is the one with

$$w = n \quad \text{and} \quad k = \begin{cases} 1 & \text{in interval } n \\ 2 & \text{in interval } n' \end{cases} \tag{4.8a,b}$$

The throw w_1k_1 that is modulated by

$$d_{w_1k_1} = d_m \cos\theta \quad , \qquad 30° \le \theta < 90° \tag{4.9}$$

is the one with

$$w_1 = \begin{cases} w+1 & \text{if } w=1,2 \\ 1 & \text{if } w=3 \end{cases} \quad \text{and} \quad k_1 = \begin{cases} 2 & \text{in interval } n \\ 1 & \text{in interval } n' \end{cases} \tag{4.10a,b}$$

The throw w_2k_1 that is modulated by

$$d_{w_2k_1} = d_m \cos(\theta - 60°) \quad , \qquad 30° \le \theta < 90° \tag{4.11}$$

is the one with

$$w_2 = \begin{cases} w_1+1 & \text{if } w_1=1,2 \\ 1 & \text{if } w_1=3 \end{cases} \tag{4.12}$$

These *same* two functions are used for all six intervals, the two throws receiving them being picked by six-stepped rotation.

From the above duty ratio specification, the *effective duty ratio* in *any* interval is

$$d_w = d_{w1} - \frac{1}{3}\sum_{z=1}^{3} d_{z1} = \frac{d_m}{\sqrt{3}} \cos\left[\theta - (w-1)\frac{2\pi}{3}\right] \tag{4.13}$$

$$\text{for} \qquad 1 \le w \le 3$$

The effective modulation amplitude is thus $\frac{d_m}{\sqrt{3}}$, better than the $\frac{d_m}{2}$

offered by continuous PWM. Although this improvement seems small, it must be reminded that even the voltage-source inverter, with square wave output, can give only $\frac{2}{\pi}$ ($\approx$.64) V_g in its fundamental component.

Six-stepped PWM uses duty ratio efficiently: it eliminates any idling intervals and allows the modulation amplitude to go all the way to *one*. The resulting higher effective duty ratio *reduces stress level* on all circuit components; for instance, the inductor can be designed smaller and current rating of semiconductor devices lower because inductor current is decreased by a factor of $\frac{2}{3}$ for the same output current. The switching loss is *less* than that in continuous PWM because one throw is always inactive in the buck, and two in the boost inverter. The switching noise spectrum should improve because the drive is highly balanced and symmetrical, the symmetry periodicity being at six times the inversion frequency; this symmetry is absent from the switching diagram of Fig. 4.3.

In summary, *six-stepped PWM* combines the strength of six-stepped drive and continuous PWM to synthesize *sinusoidal* outputs with *improved effective duty ratio*. The higher effective modulation amplitude allows the three-phase buck inverter to invert V_g to an output amplitude as high as $\frac{V_g}{\sqrt{3}}$ (continuous PWM yields only $\frac{V_g}{2}$); likewise, the three-phase boost inverter can invert I to an output amplitude as high as I (continuous PWM provides only $\frac{2}{3} I$).

4.1.3 Bidirectionality of Power Flow

The reversal of power at input and output ports requires a change in polarity of either voltage or current at these ports. This change can be done *electronically* if the port is already conditioned for four-quadrant operation, as is the input of a buck or output of a boost inverter. It, however, may require *additional switches* if the port is only one- or two-quadrant, as is the input of a buck-boost inverter.

First, consider the case of a buck topology during regeneration. If the polarity of load voltage is the *same* during both forward and reverse energy transfers, the *currents* through the inductors have to *reverse* direction for power to flow backward. The only requirement for this current reversal is the adjustment of modulation amplitude such that the inverted potential at the source end of the inductors is *lower* than the load potential. If the polarity of load voltage *changes* for regeneration, the current direction needs not do so. In this case, not only modulation amplitude is altered, but modulation phase needs be delayed by 180° so that rectified ac currents flow *into* the dc supply *and* volt-second is still balanced across the inductors.

The *voltage-fed* buck inverter in the above examples demands no topological modification because it is already fed by a *voltage* source whose current polarity changes freely. The *current-fed* buck-boost topology, however, does not share this convenience because it is still fed by a *voltage* source whose polarity is *fixed* instead of variable as that of a current source. Therefore, the dc supply in the buck-boost inverter has to be encased in a bridge as shown in Fig. 4.7 so that it can swing freely to match the polarity at the other end of the inductor. In normal mode of operation,

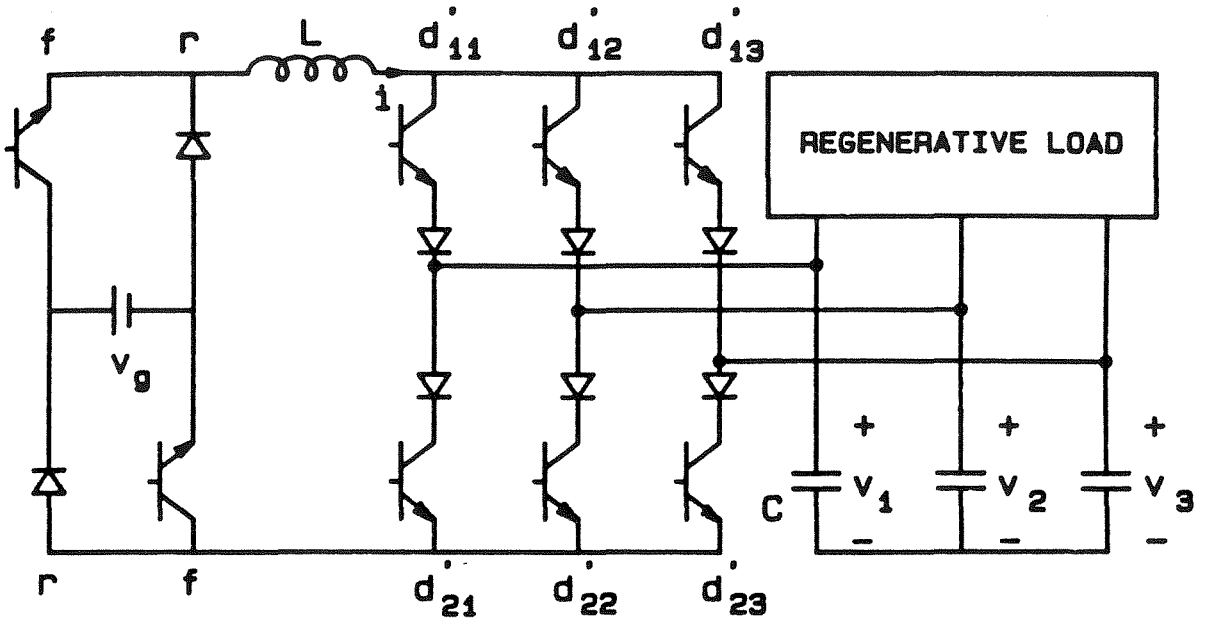


Fig. 4.7 Buck-boost inverter with input bridge for regeneration.

both transistors are on during dT_s and one is off during $d'T_s$. In reverse mode of operation, both transistors are off during dT_s and one is on during $d'T_s$.

In boost-type topology, the inductor current always flows in *one* way regardless of the direction of power. Therefore, current polarities at both input and output ports are completely controlled *electronically*, and the mechanism of power reversal is speedy. If the sign of load voltage is the *same* during regeneration, the phase of duty ratio modulation needs be reversed, and vice versa, so that power flows away from the load. At the same time, the diodes of the bridge must take over the transistors, and all duty ratios should be adjusted so that the average potential across the

inductor just overcomes the small parasitic drop; feedback is necessary to tune the duty ratio.

In review, power bidirectionality is achieved *electronically* with or without topological modification. Electronic control involves the adjustment of dc duty ratios as well as modulation amplitude and phase of ac duty ratios. A bridge is cast around the dc supply in boost-type, current-fed inverters so that the unidirectional inductor current can both charge and discharge the source.

4.2 Isolation

The feasibility of high-frequency isolation motivates the determination of suitable means to insert an isolation transformer in some of the basic topologies discussed in Chapter 3. Examples are given below for few voltage-fed and current-fed inverters.

The flyback topology is *inherently isolable* because the energy-storage inductor stays completely at either the source or load during each switching cycle. Isolation is thus implemented by splitting the inductor winding in Fig. 3.7 into two *coupled* windings sharing a common magnetic path, as is portrayed in Fig. 4.8. The input throw d is functionally related to the output throws although they are physically separated. Drive strategies for the switches are analogous to those explained in Subsection 4.1.2 for the buck-boost inverter; in particular, six-stepped PWM is highly recommended as it reduces the size and stress of circuit elements and introduces less switching noise.

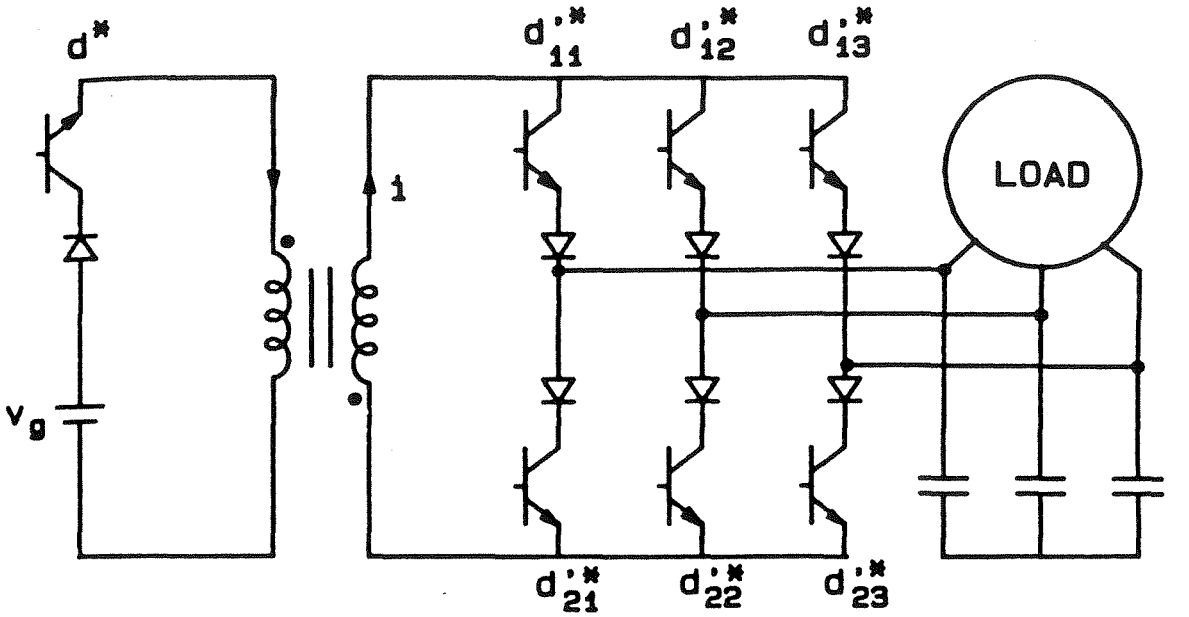


Fig. 4.8 Isolated flyback inverter.

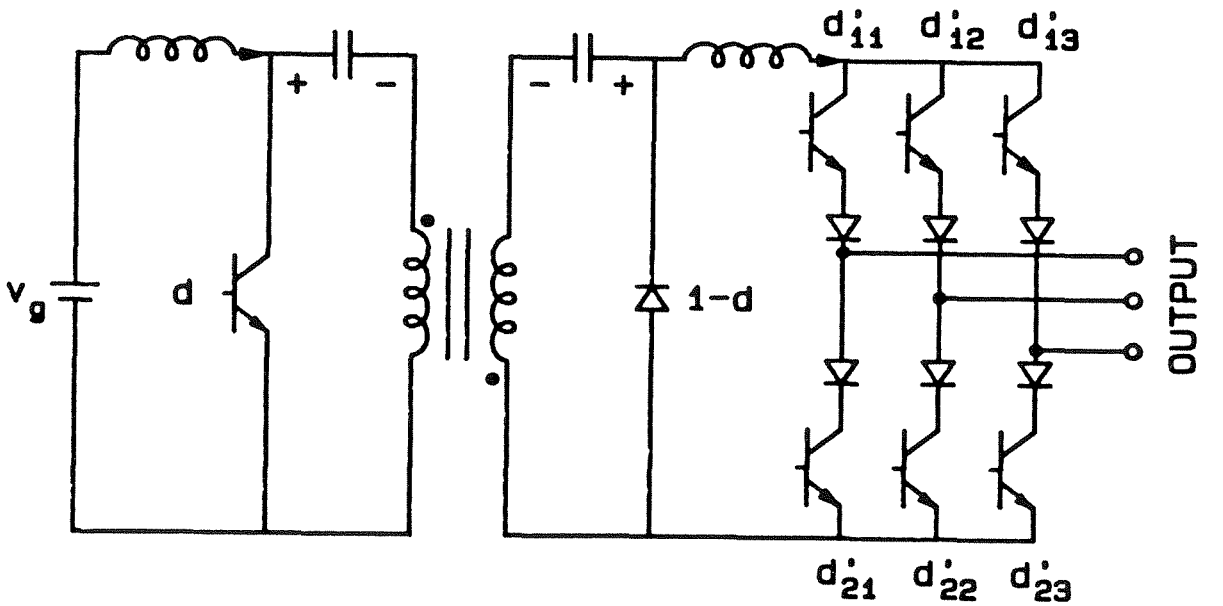


Fig. 4.9 Boost-boost inverter, cascade of a boost dc converter and a boost inverter, with isolation as in the Ćuk dc converter.

The application of the isolation principle used in the Ćuk dc converter to a boost-boost inverter results in the *isolated boost-boost inverter* in Fig. 4.9. Under steady-state condition, the duty ratio of the input switch, whose transistor and diode are split across the transformer, is *dc* to establish *dc* voltages on the capacitors and *dc* currents through the inductors. The dc current in the output inductor is then inverted into sinusoidal three-phase currents by two sinusoidally modulated switches at the output. The topology is inherently isolable because the energy-transfer capacitors, effectively in series, are completely at either the input or output. The capacitors ensure only ac magnetizing flux circulates in the transformer.

Isolation can also be inserted in buck-type inverters, although not as naturally as in the previous examples. As there are forward, push-pull, half-bridge, and full-bridge dc converters, the isolated buck dc converters, there are also *forward, push-pull, half-bridge, and full-bridge inverters*, the *isolated* buck inverters. A push-pull inverter with a four-winding isolation transformer and two double-throw switches in the input section is depicted in Fig. 4.10. Volt-second balance for the transformer is attained by application of V_g for equal durations to two primary windings. The secondary windings are switched synchronously with their primary counterparts so that regardless of what happens on the primary side, the secondary bus *always* delivers V_g to the output bridge. After the transformer, then, everything is identical to a non-isolated buck inverter.

In retrospect, examples of high-frequency isolation have been demonstrated for some inherently isolable inverters, such as the flyback, isolated boost-buck, isolated boost-boost, and so on topologies. Isolated buck dc converters can also be extended into forward, push-pull, full-bridge, and

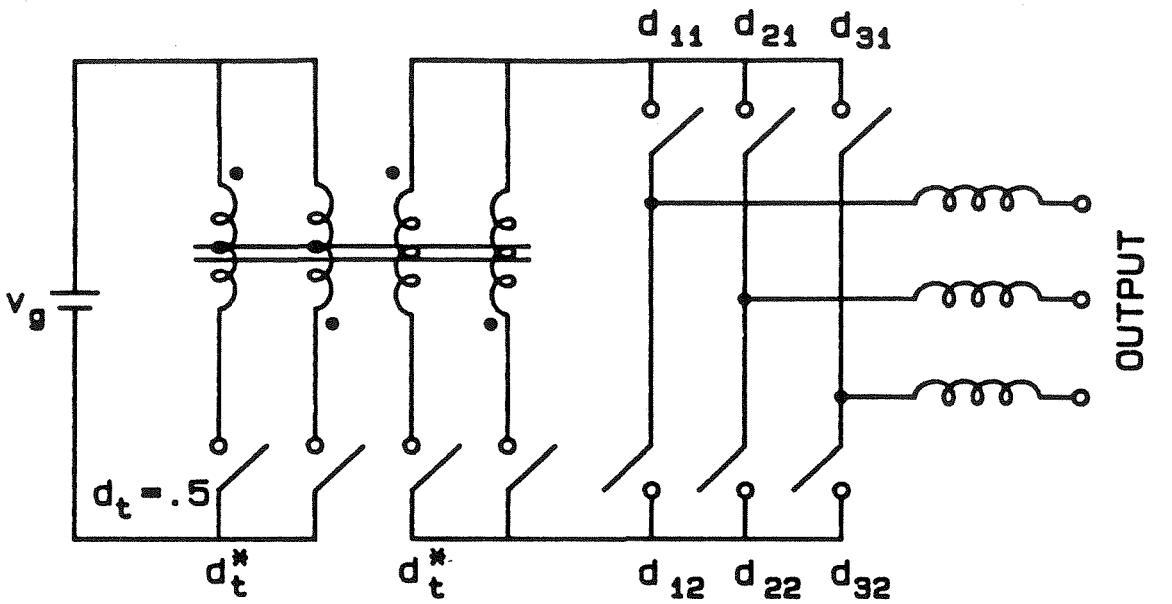


Fig. 4.10 Push-pull inverter, buck inverter with isolation as in the push-pull dc converter.

half-bridge inverters. Needless to say, more topologies can be synthesized by union of a dc converter and an inverter.

4.3 Measurement Principle

The measurement of switched-mode converters is more difficult than that of linear circuits because of the interference of switching harmonics with the desired signal. Fortunately, this difficulty has been overcome satisfactorily for dc converters thanks to standardized techniques introduced in [5] and other contributions. In view of the considerable amount of efforts and results already developed, it is advisable not to start from ground zero to create another measurement method for ac converters.

This section thus deals with the conditioning of signals in inverters so that they become meaningful to a dc measurement system.

It has been proved that the *ofb variables* are the equivalent *dc* description of balanced polyphase sinusoids; therefore, the interface between the inverter and the measurement circuit is the *implementation of the abc-ofb transformation*. In particular, this conditioning link should generate the real part v_r, imaginary part v_i, and magnitude v_m of the backward phasor $\tilde{v}_b$ characterizing a set of sinusoidal states. It is also desirable to have the phase of the rotating axes *adjustable* relative to that of duty ratio modulation, chosen as reference.

From the definition of backward phasor in Appendix B, $\tilde{v}_b$'s of two ofb reference frames of angles Φ_{T1} and Φ_{T2} are related by

$$\tilde{v}_b(\Phi_{T2}) = e^{j(\Phi_{T2}-\Phi_{T1})}\tilde{v}_b(\Phi_{T1}) \tag{4.14}$$

The corresponding real and imaginary parts thus satisfy

$$v_r(\Phi_{T2}) = \cos(\Phi_{T2}-\Phi_{T1})v_r(\Phi_{T1}) - \sin(\Phi_{T2}-\Phi_{T1})v_i(\Phi_{T1}) \tag{4.15}$$

$$v_i(\Phi_{T2}) = \sin(\Phi_{T2}-\Phi_{T1})v_r(\Phi_{T1}) + \cos(\Phi_{T2}-\Phi_{T1})v_i(\Phi_{T1}) \tag{4.16}$$

In other words, v_r and v_i, or any combination thereof, of one ofb coordinate system are expressible as *linear combinations* of v_r and v_i of any other ofb coordinate system, the phases of the two sets of coordinates differing by an arbitrary, constant angle. This observation simplifies not only the measurement hardware, but also the derivation of analytical results for $\Phi_{T2} \neq 0$ from those already computed for $\Phi_{T1} = 0$.

If $\Phi_{T2} = \Phi_{T1}+90°$ in Eq. (4.16),

$$v_i(\Phi_{T1}+90°) = v_r(\Phi_{T1}) \tag{4.17}$$

In other words, the *imaginary* part in any coordinate system is obtained by measurement of the *real* part in another one 90° behind. If Φ_T is set to the phase Φ_v of $\tilde{v}_b$ so that the real axis aligns with $\tilde{v}_b$,

$$v_m = v_r(\Phi_v) \tag{4.18}$$

Therefore, the ***phasor amplitude*** can also be measured by reading the ***real*** part in an ofb system in phase with the phasor itself. As a result of Eqs. (4.17) and (4.18), only *one* circuit to measure the ***real component*** in rotating coordinates of ***arbitrary phase*** needs be built to completely characterize the amplitude or all real and imaginary parts for any Φ_T.

It is important to recognize that poles of the inverter are ***invariant*** to Φ_T because transfer functions of all coordinate angles are linearly dependent. Likewise, zeros of $\hat{v}_m$- frequency responses are independent of Φ_T since the length of a phasor is the same wherever it is measured. Zeros of v_r and v_i, however, may be varied as functions of Φ_T according to Eqs. (4.15) and (4.16). Therefore, if dynamics of these functions are not satisfactory with $\Phi_T = 0$, an improvement is possible with some other values of Φ_T.

For a three-phase system, the real component as a function of Φ_T can be expressed as

$$v_r(\Phi_T) = \frac{1}{\sqrt{3}} \sum_{w=1}^{3} v_w \cos\left[\theta_T - (w-1)\frac{2\pi}{3}\right] \tag{4.19}$$

where θ_T is related to the angle θ of the duty ratio modulation according to

$$\theta_T = \theta - \Phi_T = \int_0^t \omega(\tau)\, d\tau - \Phi_T \tag{4.20}$$

Three multipliers and one summer are thus required to calculate v_r from v_1, v_2, and v_3 at a given Φ_T. The phase shifting of Φ_T is accomplished through a digital adder. The whole circuit is simple yet efficient, as is verified in the next section.

4.4 Experimental Verification

This section consists of five parts. The first two describe the signal-processing circuitry and power stage associated with an experimental *three-phase flyback inverter*. The last two tabulate steady-state and dynamic data.

The block diagram in Fig. 4.11 highlights the relationship among the input signal-processing circuit, power stage, and output signal-processing circuit. The left portion of the picture synthesizes switching functions with the required duty ratios for the switches in the power stage. The one following the inverter conditions time-varying outputs so that they can be measured by instruments developed for dc converters.

Observe that even though steady-state inputs and outputs of the inverter itself may contain sinusoidally time-varying components, *all quiescent inputs and outputs of the overall system are purely dc*. The box labeled "Three-Phase Flyback Inverter" thus corresponds to the abc reference frame while the surrounding ones reflect the abc-ofb transformation acting on converter parameters. Variables passed to the measurement setup are then real representations of the ofb coordinate system.

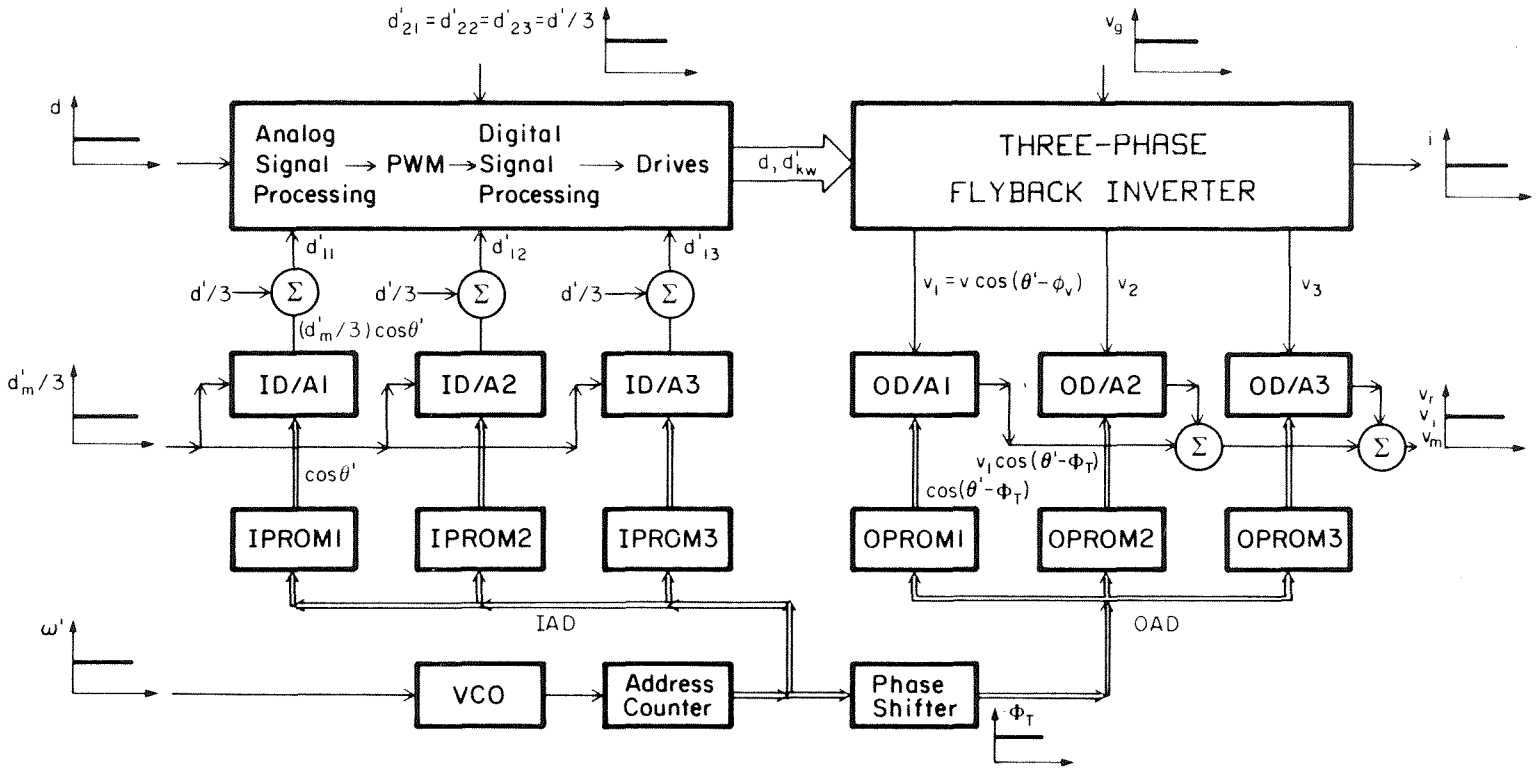


Fig. 4.11 Block diagram of the experimental flyback inverter showing the power stage and the circuitry to transform the ac system into a dc equivalent.

4.4.1 Input Signal-Processing Circuitry

The input half of Fig. 4.11 is expanded in Fig. 4.12 to exemplify the steps to synthesize the switching functions for a multiple-throw switch. The expansion consists of duty ratio generators, *multiple-output pulse-width modulator*, and isolated drives. The duty ratio section includes a VCO (voltage-controlled oscillator), an address counter, PROM's (IPROM1 and IPROM2 - IPROM3 is redundant), D/A converters (ID/A1 and ID/A2), and summers. Outputs of the D/A converters are sinusoidal modulations displaced by 120°. The instantaneous modulation frequency ω' is proportional to the voltage ω' input to the VCO, and the instantaneous modulation amplitude $\frac{d_m'}{3}$ the voltage $\frac{d_m'}{3}$ input to the D/A converters. Dc offsets $\frac{d'}{3}$, derived from the voltage of the input duty ratio d, are then added to the synthesized sinusoids such that the final results are proper for the pulse-width modulator.

To demonstrate the drive flexibility that results from fast switching and the independency of the two switches in the flyback topology, modulation is applied only to the output throws of the first switch. Thus,

$$d_{1w}' = \frac{d'}{3} + \frac{d_m'}{3}\cos\left[\theta' - (w-1)\frac{2\pi}{3}\right] \qquad (4.21a)$$

and

$$d_{2w}' = \frac{d'}{3} \quad , \qquad 1 \le w \le 3 \qquad (4.21b)$$

where

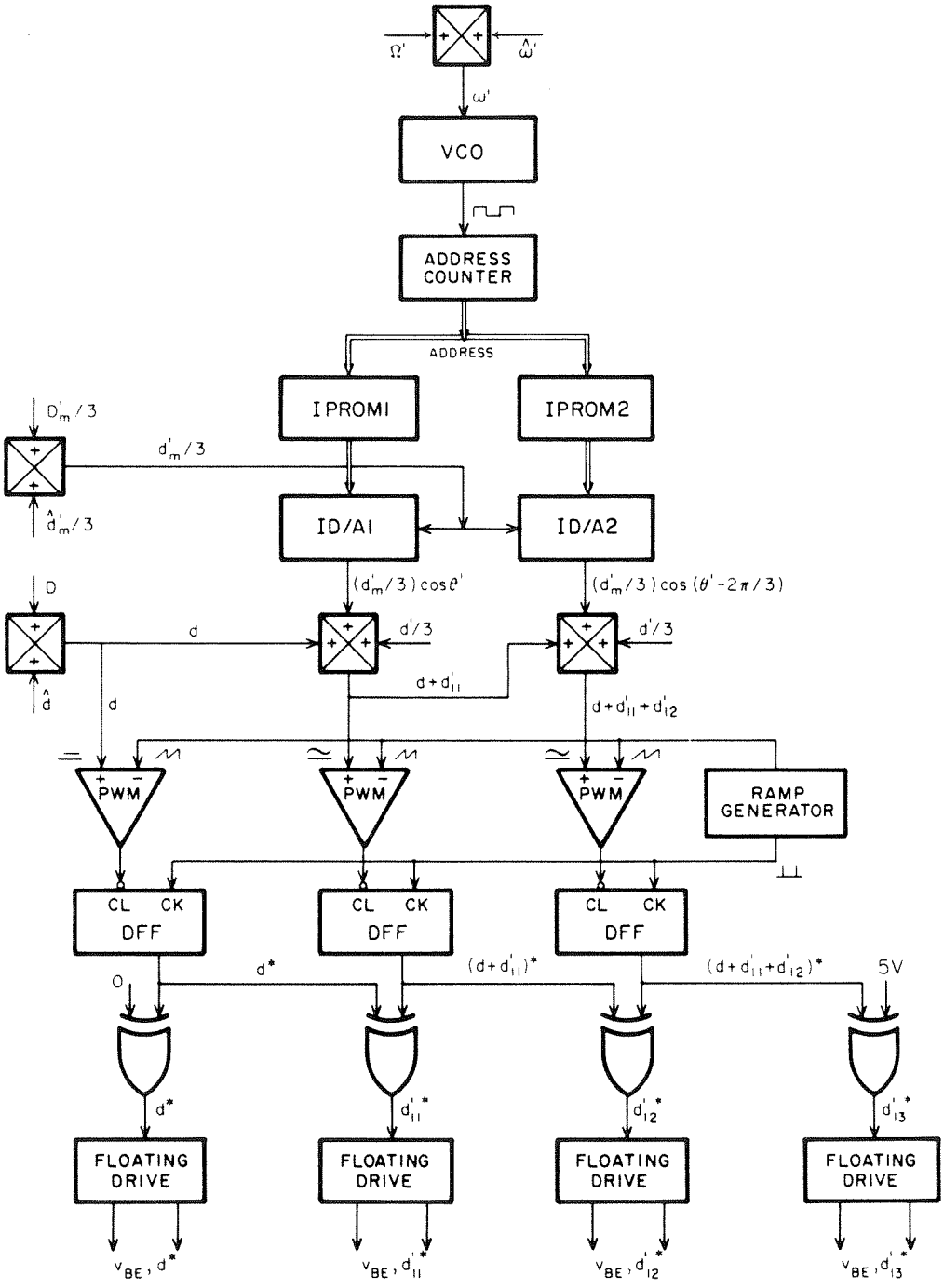


Fig. 4.12 Block diagram to synthesize the switching functions of a sinusoidally modulated triple-throw switch.

$$d' = 1-d \quad , \quad d_m' \le d' \quad \text{and} \quad \theta' = \int_0^t \omega'(\tau)\, d\tau \qquad (4.22a,b,c)$$

The above functions are detailed in the switching diagram of Fig. 4.13.

Drive waveforms for, say, the modulated switch (d_{1w}') are achieved by the multiple-output pulse-width modulator in Fig. 4.12. The modulator consists of three comparators and exclusive-or gates. The comparators invert the analog signals d, $(d + d_{11}')$, and $(d + d_{11}' + d_{12}')$ into the respective digital signals d^*, $(d + d_{11}')^*$, and $(d + d_{11}' + d_{12}')^*$ demonstrated by the first, third, and fifth square waves in Fig. 4.14. These waveforms next pass through the flip-flops where their rising edges are synchronized and multiple-pulse problem eliminated. The cleaned-up signals are then subtracted digitally at the exclusive-or gates to retrieve the desired switching functions d^*, $d_{11}'^*$, $d_{12}'^*$, and $d_{13}'^*$ shown in thick trace in Fig. 4.14. Drive waveforms for the other switch are obtained in an analogous manner.

4.4.2 Power Stage

The power stage consists of the base drive circuitry and the flyback inverter itself. As is described in Fig. 4.15, the base drive first amplifies the switching function through a DS0026 buffer to the power level required by the base of the transistor. The amplified square wave then drives an isolation transformer through some resistors, a capacitor, and a diode. This drive has favorable transient response and is safeguarded against spurious turn-on of the transistor when the throw is supposed to be off.

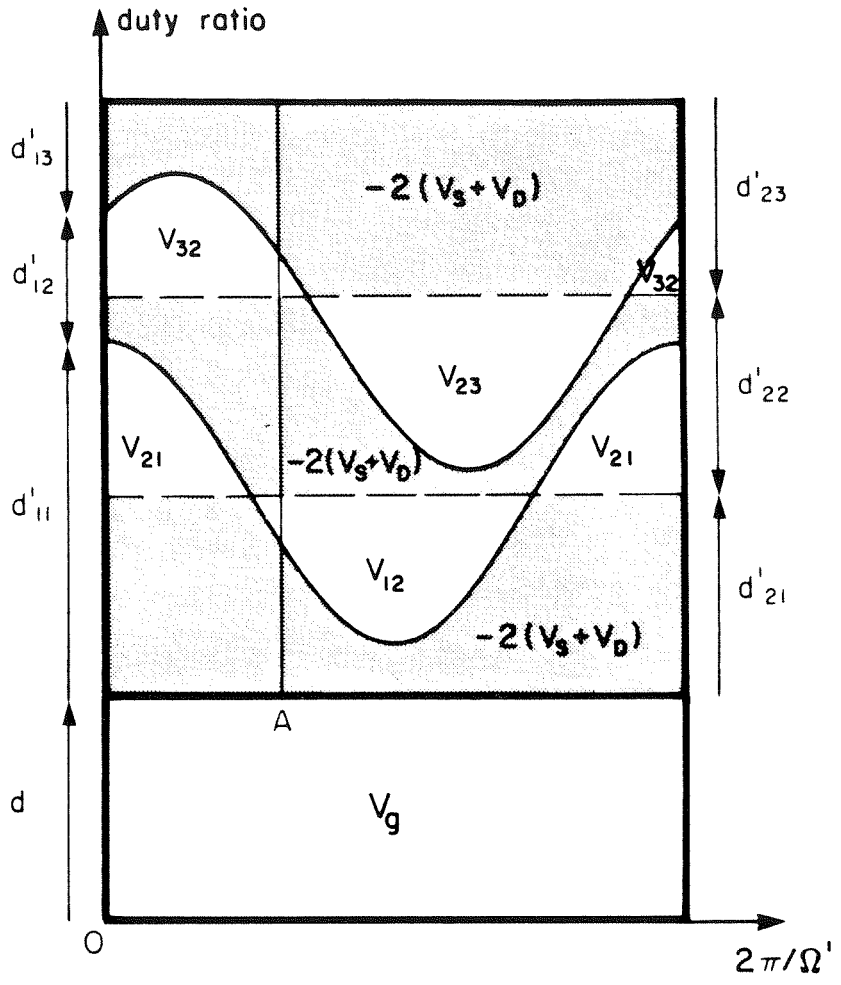


Fig. 4.13 Switching diagram of the experimental flyback inverter showing inductor voltages for modulation of only one switch.

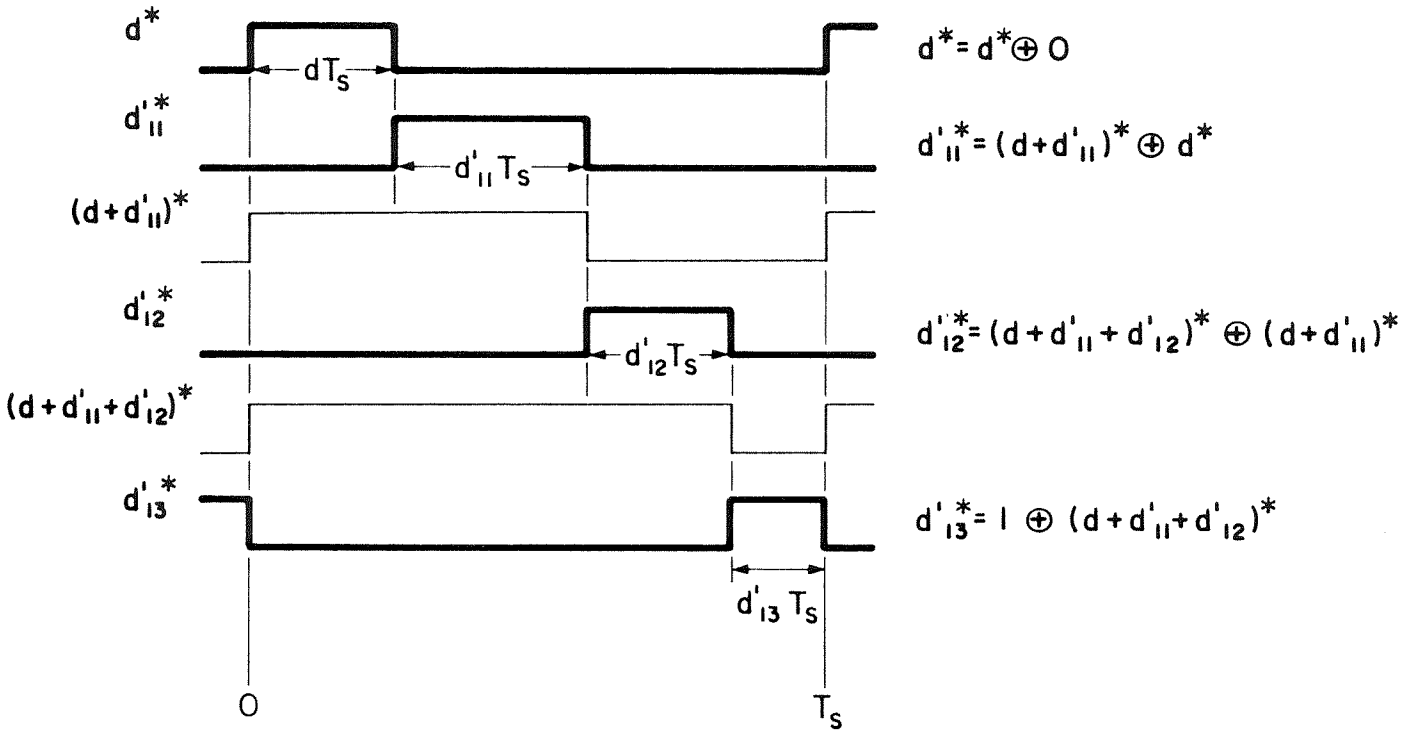


Fig. 4.14 Output (thick) and intermediate (thin) waveforms in the multiple-output pulse-width modulator.

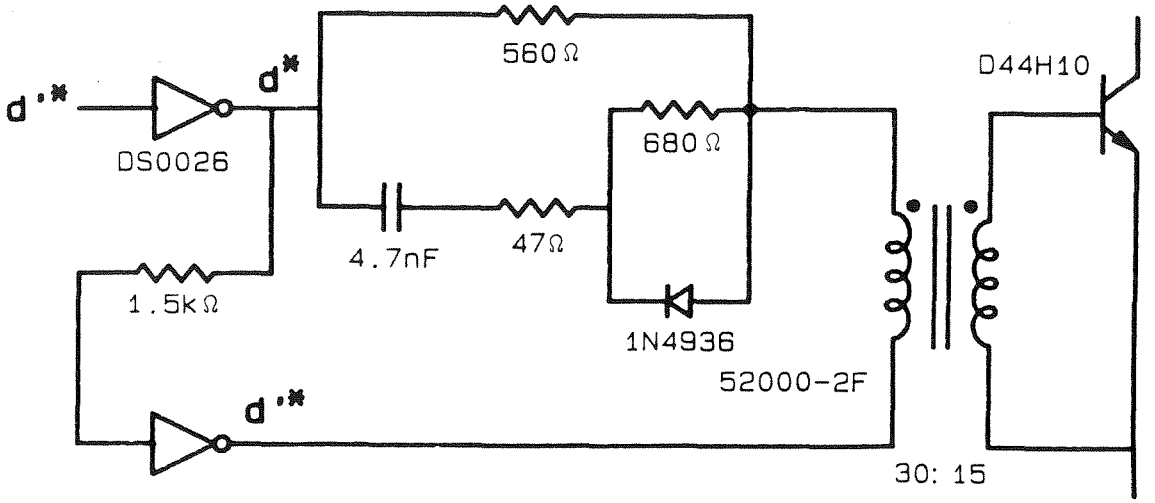


Fig. 4.15 Isolated base drive for one transistor.

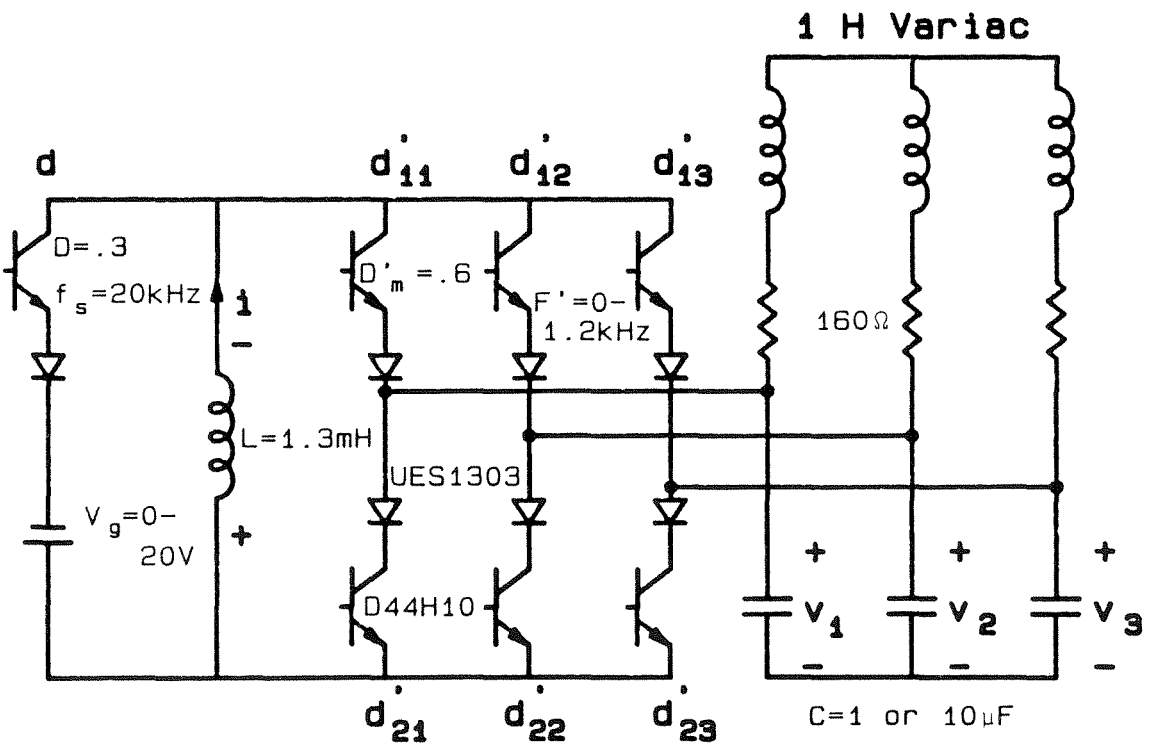


Fig. 4.16 Principal components of the experimental flyback inverter, driving a highly inductive load.

After the isolated drive come the power transistors and the rest of the inverter. Essential components of the circuit are shown along with their values in Fig. 4.16. *Not* shown are *low-power* diodes anti-parallel to the transistors to absorb inadvertent negative spikes during switching transients; a transient absorber, e.g., zener diode, should also shunt the inductor for the same reason just in case the transistors do not commutate smoothly. Fast switching devices with low on-drop or on-resistance is essential in minimization of unwanted harmonics that already exist owing to the finiteness of switching frequency.

4.4.3 Output Signal-Processing Circuitry

The inductor current is a direct output as it is already dc. The capacitor voltages, however, need to go through the abc-ofb transformation before they can be measured by dc instruments. As is depicted in the lower right of Fig. 4.11, the output conditioning circuit is composed of D/A converters (OD/A1, OD/A2, and OD/A3), PROM's (OPROM1, OPROM2, and OPROM3), and a phase shifter. The phase shifter is merely an eight-bit TTL adder that shifts the address of the output PROM's from that of the input PROM's by a constant amount $-\Phi_T$. This arrangement guarantees that the *instantaneous rotation frequency of the ofb coordinates is identical to that of the duty ratio modulation*; the phase of the rotating axes, however, lags that of the modulation by the *adjustable* Φ_T.

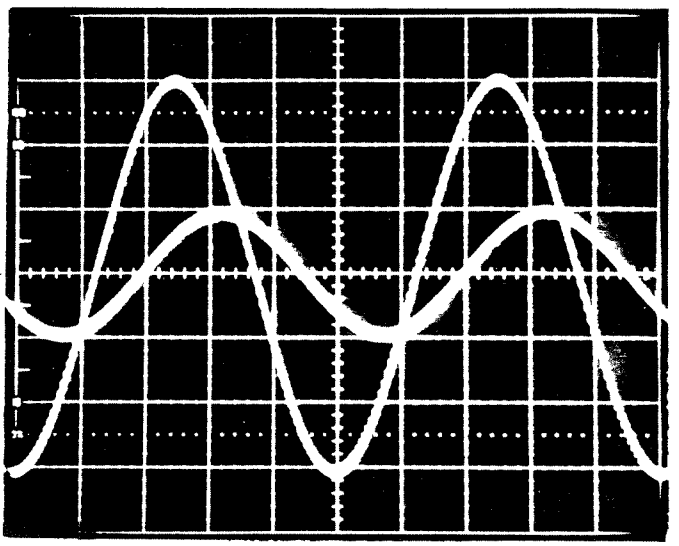
The output D/A converters ***multiply*** the sinusoids in the output PROM's with the corresponding attenuated capacitor voltages. The sum of these products is either v_r, v_i, or v_m, depending on the set value of Φ_T.

To summarize, the experimental circuit consists mainly of a VCO, PROM's, D/A converters, and a phase shifter to synthesize the sinusoidally modulated duty ratios and the *abc-ofb transformation*; a *multiple-output pulse-width modulator* to convert duty ratios into switching functions; and a three-phase flyback inverter with associated base drive hardware. Inputs to the system are the modulation frequency ω', modulation amplitude $\frac{d_m'}{3}$, input duty ratio d, and source v_g. Outputs are the inductor current and the real part, imaginary part, and amplitude of the capacitor voltage phasor, measured in an ofb reference frame of *arbitrary* angle. The resulting *dc-in, dc-out* overall system has the right format for standard *dc* measurement setups.

4.4.4 Steady-State Results

The large magnetizing *inductance* of a three-phase autotransformer has been connected as part of the load to convince that a flyback topology is as good for motor drive applications as a current-source inverter. The load voltage (thin trace) and current of phase 1 are illustrated in Fig. 4.17a for $V_g = 6.5\,V$ and $F' = \frac{2\pi}{\Omega'} = 200\ Hz$; the power factor is clearly $\approx .5$ *lagging*, very poor. The circuit performs as expected even under this highly inductive load: the three-phase outputs v_1, v_2, and v_3 in the second, third, and fourth trace, respectively, of Fig. 4.17b looks almost as sinusoidal as the duty ratio modulation d_1' (top trace) of the first phase, confirming the trifle contribution of harmonics at the power level of the experiment. *Absent* from the picture is the *cross-over distortion* often found in voltage-fed switched-mode amplifiers [20]; the flyback topology circumvents this

a)



b)

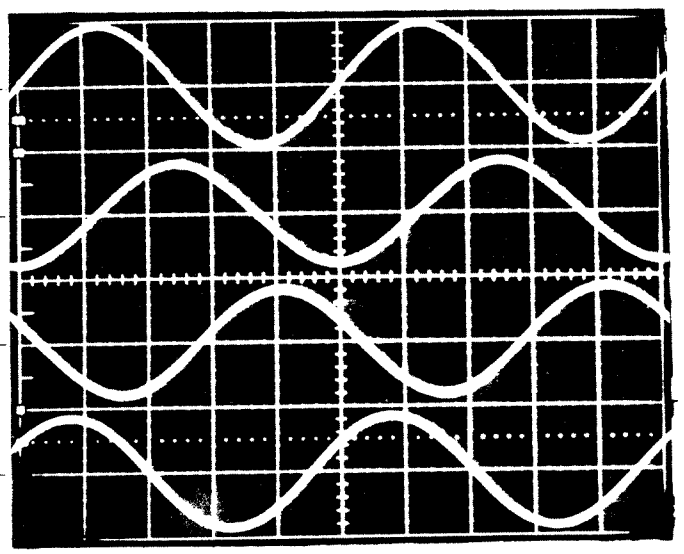


Fig. 4.17 (a) Voltage (thin trace; 5 V/div) and load current (thick trace; 10 mA/div) of phase 1 showing highly inductive load; (b) three phase voltages (lower traces; 20 V/div) and duty ratio modulation of phase 1 (top trace; 2 V/div). Horizontal scale: 1 ms/div.

shortcoming because its switch current, being dc, *never* "crosses-over" even though the output currents do.

For ease of discussion, the load is set to purely 160 ohms in the remaining pictures. In Fig. 4.18, the modulation frequency is swept from dc to 200 *Hz* to detect the peculiar steady-state rhp zero in the voltage phasor (V_g is adjusted to 10 *V* in anticipation of the rapid increase in amplitude at high frequency). Although the measurement is restricted to a narrow frequency range because of power limitation, the overall drop of 60° in phase in conjunction with a rising trend in amplitude is evident. Prediction and data go hand-in-hand over the output range of interest.

Switching waveforms at the ends of the inductor with respect to the capacitor junction are photographed in Fig. 4.19a for *zero* modulation frequency and Fig. 4.19b for modulation frequency of 60 *Hz*. As is clearer

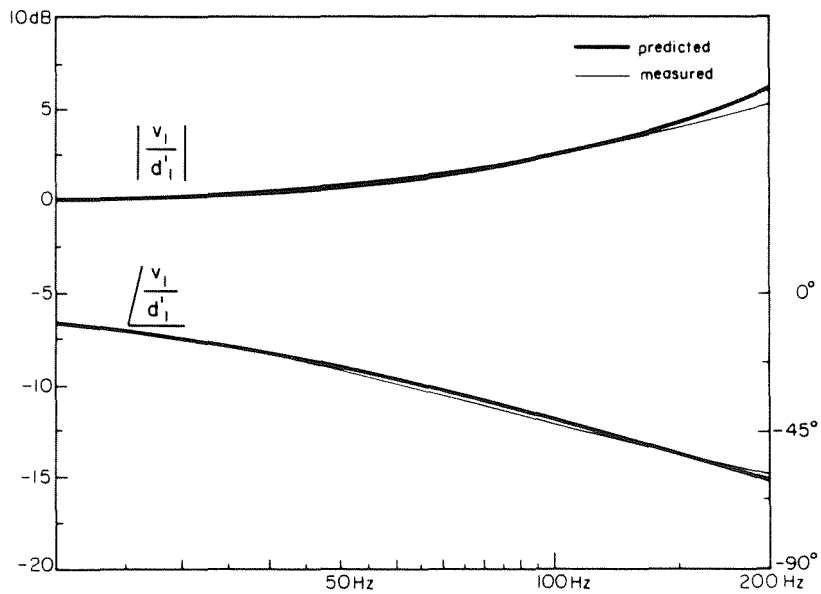
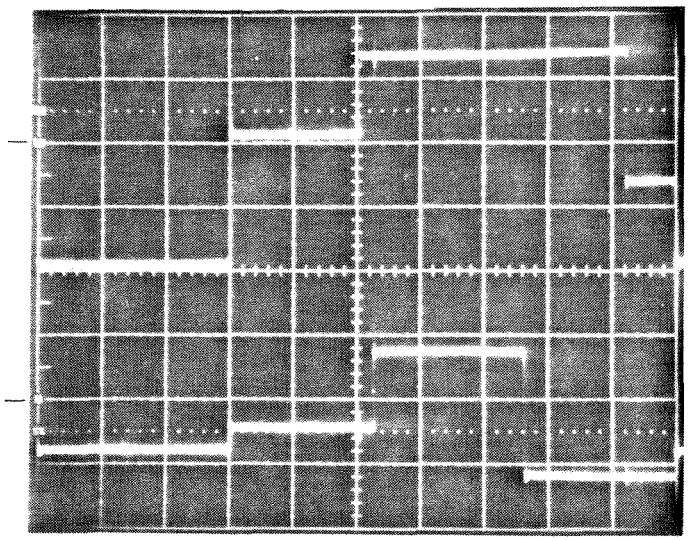


Fig. 4.18 Steady-state frequency response proving the existence of right-half-plane zero.

a)



b)

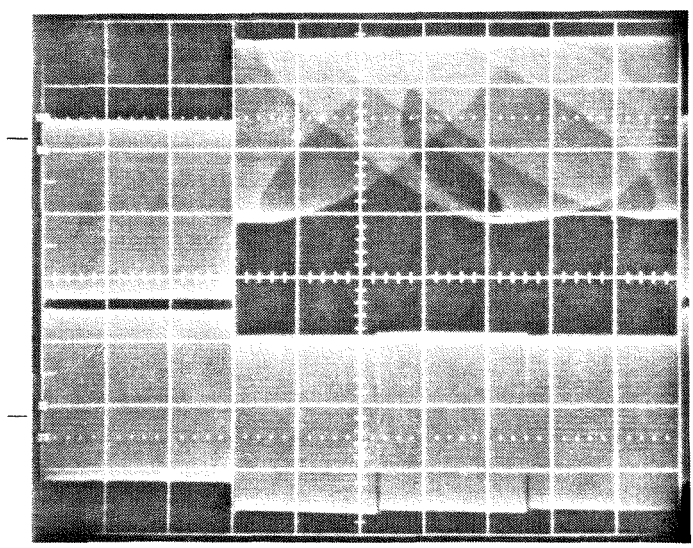


Fig. 4.19 Switching voltages at negative (top traces) and positive (bottom traces) ends of the inductor relative to capacitor common for (a) F' = 0 Hz and (b) F' = 60 Hz. Vertical scale: 10 V/div; horizontal scale: 5 μs/div.

in Fig. 4.19a, the four horizontal distances in the top trace (negative end of the inductor) record, from left to right, the duty ratios d, d_{11}', d_{12}', and d_{13}'; those in the bottom trace (positive end of the inductor), d, d_{21}', d_{22}', and d_{23}'. The vertical distance in the first interval is not meaningful, but those in the last three are samples of the capacitor voltages v_1, v_2, and v_3. Except for the duty ratios of the lower trace that are "normal" dc, all other duty ratios and phase voltages are *balanced sinusoidal dc*.

As the inversion frequency increases to 60 Hz in Fig. 4.19b, four transition points within $d'T_s$ of the top waveform trace out four ellipses to characterize simultaneous sinusoidal motions in both vertical (voltage) and horizontal (duty ratio) directions. The corresponding points in the lower trace simply draw vertical lines because the duty ratios are dc and only vertical motions exist.

A host of information is available from Fig. 4.19b. The height of any ellipse measures the peak-to-peak phase voltage; the width indicates the peak-to-peak duty ratio modulation; and the inclination translates into the phase difference between the output voltage and input duty ratio. The shape of the ellipse provides a rough estimate of waveform ideality. Dc duty ratios can be interpreted directly from either trace.

The switched voltage across the whole inductor at 20 Hz is captured in Fig. 4.20. The voltage segment at 15 V represents V_g, and the one slightly below zero arises from the finite switch drop. Each "heart" actually consists of two rectified halves of the same ellipse; the rectification occurs at the dc duty ratio lines of the unmodulated throws. The voltages and duty ratios involved can be deduced by comparison of Figs. 4.20 and 4.13.

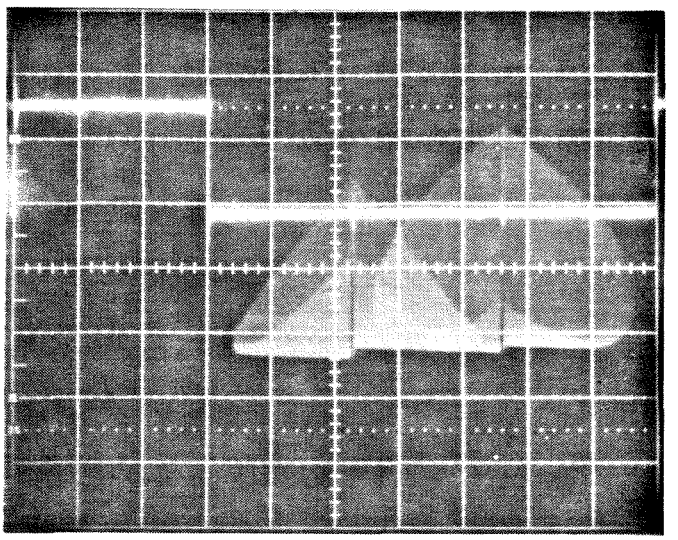


Fig. 4.20 Switching voltage across the inductor at F' = 20 Hz. Vertical scale: 10 V/div; horizontal scale: 5 μs/div.

Overall, describing equations predict well the steady-state amplitude and phase responses of capacitor voltages and the dc value of inductor current. Distortion is inevitable because the switching frequency is finite and volt-second sampling sequential. The switching diagram is a helpful aid in recognition of unusual switching details in steady-state waveforms.

4.4.5 Small-Signal Dynamic Results

Since all inputs and outputs of the flyback inverter are steady-state dc in the ofb reference frame, their dynamic frequency responses can be obtained by well-known measurement techniques developed for dc converters. In this experiment the Automatic Measurement System (AMS) [5] takes all

data and plots them in the familiar Bode format; results are then overlaid on theoretical curves predicted by the Switching Converter Analysis Program (SCAP) [5]. Proper modifications, however, need be entered in the measurement program to condition it for noisy data. "Noise" used here refers to the harmonics that always exist in practical inverters because of nonidealities in components, finite switching frequency, and sequential application of volt-seconds or amp-seconds to the states. It dominates small-signal responses, especially during high-frequency roll-off, although it is barely discernible at the power level of the test circuit.

All data are taken for $D = .3$ and $D_m' = .6$. The source, which influences only the dc gain, is adjusted so that the inductor does not saturate when F' or C changes. Figure 4.21 displays the *amplitude-to-amplitude* transfer function for $C = 1\ \mu F$ and $F' = 200\ Hz$. The circuit

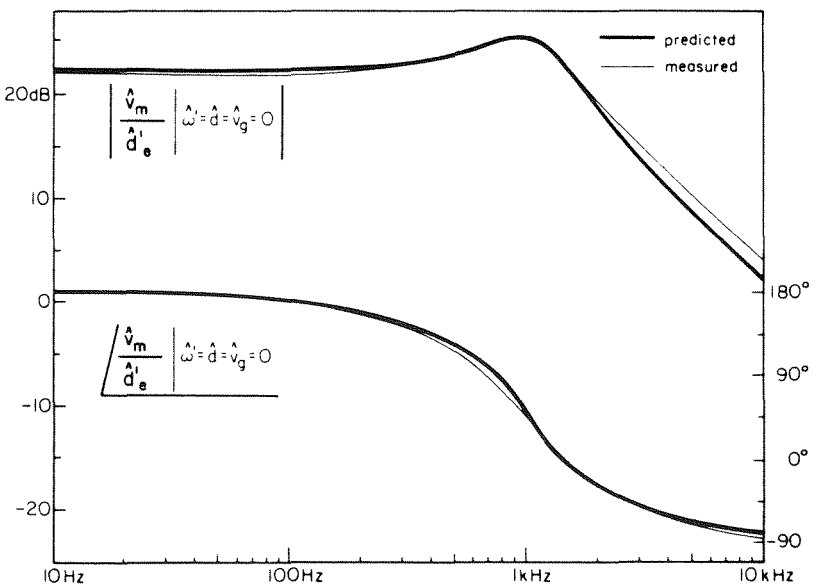


Fig. 4.21 $\frac{\hat{v}_m}{\hat{d}_e'}$ *transfer function for* $C = 1\ \mu F$ *and* $F' = 200\ Hz$.

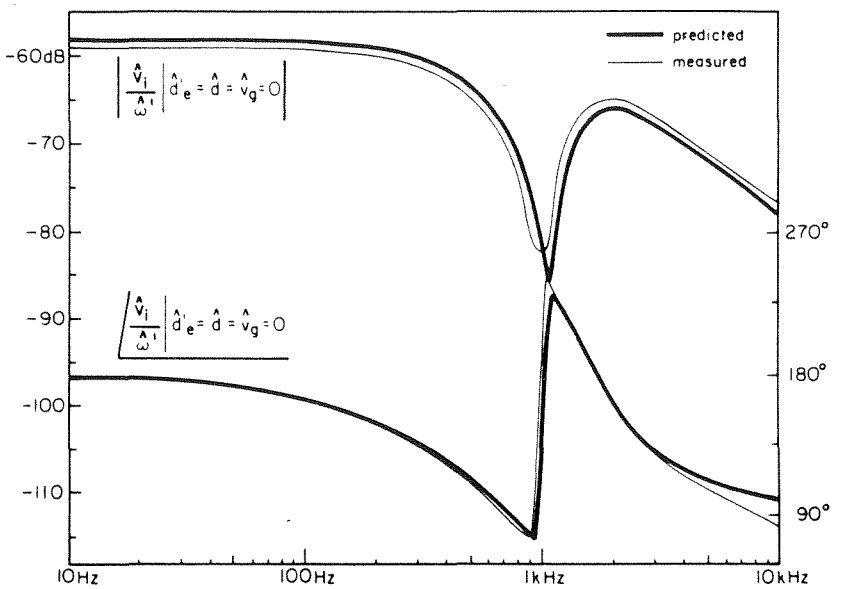
value places the real pole slightly below 1 kHz and the complex poles around 1.1 kHz. The net change of 270° in phase and single-slope asymptote indicate the presence of both lhp and rhp zeros.

Figures 4.22a and b have been devised to track the zeros in $\frac{\hat{v}_i}{\hat{\omega}'}$. Again, $C = 1\mu F$ to place the RC corner at about 1 kHz, and measurements are made for F' slightly below (Fig. 4.22a) and above (Fig. 4.22b) this corner. The amplitude plots in both figures confirm the zeros are complex and have very high Q. The phase for $F' < 1$ kHz, however, drops only 90° to indicate the zeros are in the left half-plane while that for $F' > 1$ kHz plunges down 450° to warn that they have migrated into the right half-plane!

Among the simple transfer functions is $\frac{\hat{i}}{\hat{d}}$ with a dominantly single-pole behavior (Table 3.2). Prediction and measurement both substantiate this fact in Fig. 4.23 for $C = 10$ μF. The zeros arrive at 220 Hz and dominate the earlier pole at 70 Hz only to be overcome by the complex poles at 400 Hz.

All results reported up to here have been taken with Φ_T in Fig. 4.11 set at zero. Favorable dynamics, however, may exist in ofb frames with proper nonzero Φ_T. This claim is verified for $\frac{\hat{v}_r}{\hat{\omega}'}$ at $-\Phi_T = 55°$ in Fig. 4.24. Accentuating the graph are sharp glitches due to complex *lhp zeros*. The ensuing single-pole roll-off is the advantage of proper selection of frame of reference.

a)



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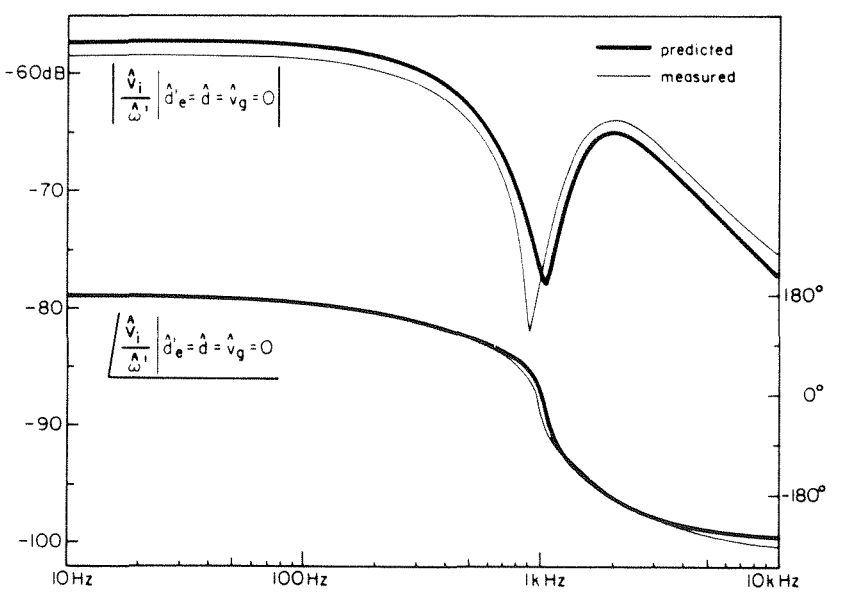


Fig. 4.22 $\frac{\hat{v}_i}{\hat{\omega}'}$ *transfer function with complex zeros in (a) the left half-plane when F' < 1 kHz moving into (b) the right half-plane when F' > 1 kHz; C = 1 μF.*

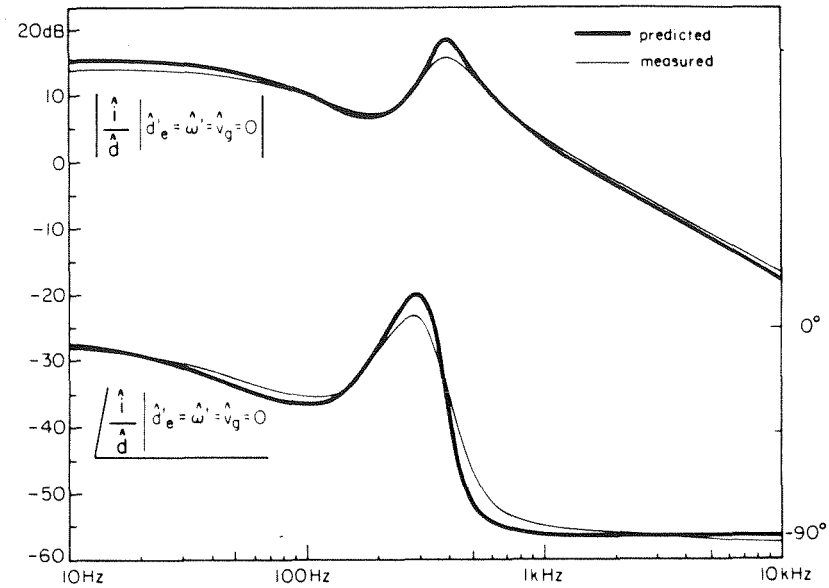


Fig. 4.23 $\dfrac{\hat{i}}{\hat{d}}$ *transfer function for* $C = 10\ \mu F$.

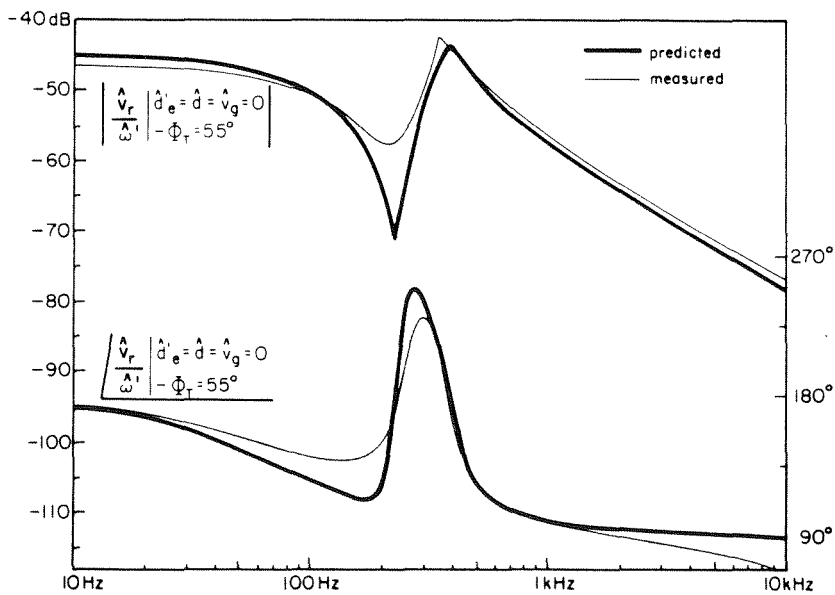


Fig. 4.24 $\dfrac{\hat{v}_r}{\hat{\omega}'}$ *with left-half-plane zeros owing to* $-\Phi_T = 55°$.

In general, small-signal bandwidth is a function of circuit components and quiescent operating condition. There is no rule saying that it is bounded by the inversion frequency, and the results recorded here have proved it can be *much higher than the inversion frequency*. Such a wide bandwidth, furthermore, can be predicted and measured with a high degree of accuracy if the switching frequency is sufficiently higher than the bandwidth itself. Thus, this experiment has confirmed prediction by measurement up to 10 *kHz*, way above the 1 *kHz dynamic* and *inversion* ranges - the switching frequency is 20 *kHz*.

In closing, this chapter has substituted anti-parallel transistor and diode for the voltage-fed throw in a buck inverter and series transistor and diode for the current-fed throw in a boost inverter. The *switching diagram* is introduced to explain the modulation strategies for these devices; attention is called to the *six-stepped PWM* that not only synthesizes *ideal* waveforms, but also *maximizes the effective duty ratio*. Drive policies for forward power transfer need be modified *electronically* for *regeneration*; in some cases, *topological* modification is also required to change a one-quadrant into four-quadrant port. With additional components, *isolation* can be incorporated into a host of topologies. Examples include the flyback, isolable boost-boost, push-pull, forward, and so on inverters.

An experimental *three-phase flyback inverter* has been constructed to test the theory. Signal-processing circuitry is built around the power stage to realize the *abc-ofb transformation* that conditions time-varying inputs and outputs into *dc* values acceptable to *instruments developed for dc converters*. Results are satisfactory: observed waveforms are practically clean, and empirical steady-state and dynamic frequency responses agree

well with the prediction. Fast switching thus permits a *wide inversion range*, an even *wider dynamic bandwidth*, and a still *wider frequency range of analytical and empirical validity*.

PART II

SWITCHED-MODE RECTIFICATION

CHAPTER 5

REVIEW OF EXISTING RECTIFIERS

Many industrial applications, such as dc motor drive, dc power supply, battery charger, high-voltage dc transmission, and so on, require the conversion of ac into dc power. This ac-to-dc conversion process is called rectification, and the corresponding power processor is named the *rectifier*. Although such a rectifier can accept either single-phase or polyphase ac at its input, only the later type is considered in the following work. Thus, there can be N, from two to infinity, sinusoidal input voltages whose amplitudes are equal and whose adjacent phases are displaced by $\pm 90°$ in a two-phase system or by $\pm \frac{360°}{N}$ in a more-than-two-phase system.

The simplest and most popular rectifier topology has been the three-phase *diode bridge rectifier* shown in Fig. 5.1. Although this circuit is economical and rugged, it does have several drawbacks. It injects a fair amount of high-frequency harmonics into the line through "spikes" in its line current waveforms. It generates unwanted harmonics, in addition to the desired dc component, at the output. Both input and output harmonics are difficult to filter because they occur at line frequency. The topology lacks control of its output, which has only one amplitude and one polarity. Post regulation is thus generally required to bring the voltage to a well-regulated level. The use of merely unidirectional diodes in Fig. 5.1 prevents energy from flowing backward, and so the circuit is unsuitable for power

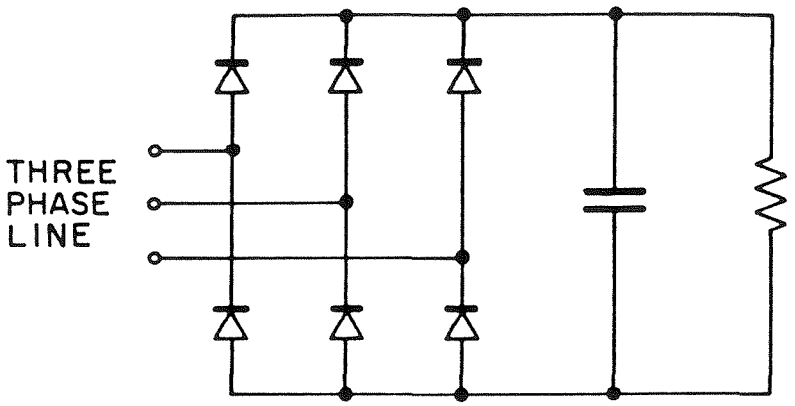


Fig. 5.1 Three-phase diode bridge rectifier.

regeneration.

Active switches, instead of diodes, can be employed in rectifiers to acquire more control of terminal properties. The *speed* at which these devices switch and their *switching functions* then indicate the *type* of topology. In general, existing ac-to-dc converters can be grouped into *slow-switching* and *fast-switching* categories.

The first section of this chapter studies characteristics of slow-switching rectifiers. Although there are a variety of circuits belonging to this family, space permits an investigation of only the more popular *phase-controlled rectifier*, identical in topology to the bridge rectifier mentioned earlier. Because of the low-frequency limitation, however, this circuit can

eliminate only part of the handicaps experienced by the uncontrolled configuration.

The following section then focuses on fast-switching rectifiers, which have evolved recently as semiconductor technology pushes forward both the frequency and the power handling capability of bipolar and field-effect transistors. Two different energy processing principles are presently governing the topologies in the high switching frequency end, namely, *pulse-width modulation* and *resonance*. Their operations are reviewed and their merits compared. The survey suggests that very few circuits fully utilize the benefits of fast switching. More importantly, there has been little effort to unify the theory of switched-mode rectification that describes basic rectifier topologies and demonstrates their continuous evolution into other useful configurations. These observations motivate the more fundamental investigation into rectifier topologies and analyses in the upcoming chapter.

5.1 Rectifiers Switched at Low Frequency

The classification of rectifiers according to their switching frequency bases on the comparison of switching and input (or line) frequencies. When these two frequencies are compatible or, to be exact, equal, then the circuit operates at "low" frequency. A familiar example of this category is the *phase-controlled rectifier* frequently found at the front end of many motor drive systems that require a variable dc input [24, 25, and 26].

As is illustrated in Fig. 5.2(a), the phase-controlled rectifier consists of two triple-throw switches that apply both ends of the load to various input lines. The throws in the circuit switch at Ω_g, same as line frequency, under steady-state condition. According to Fig. 5.2(c), their timing follows

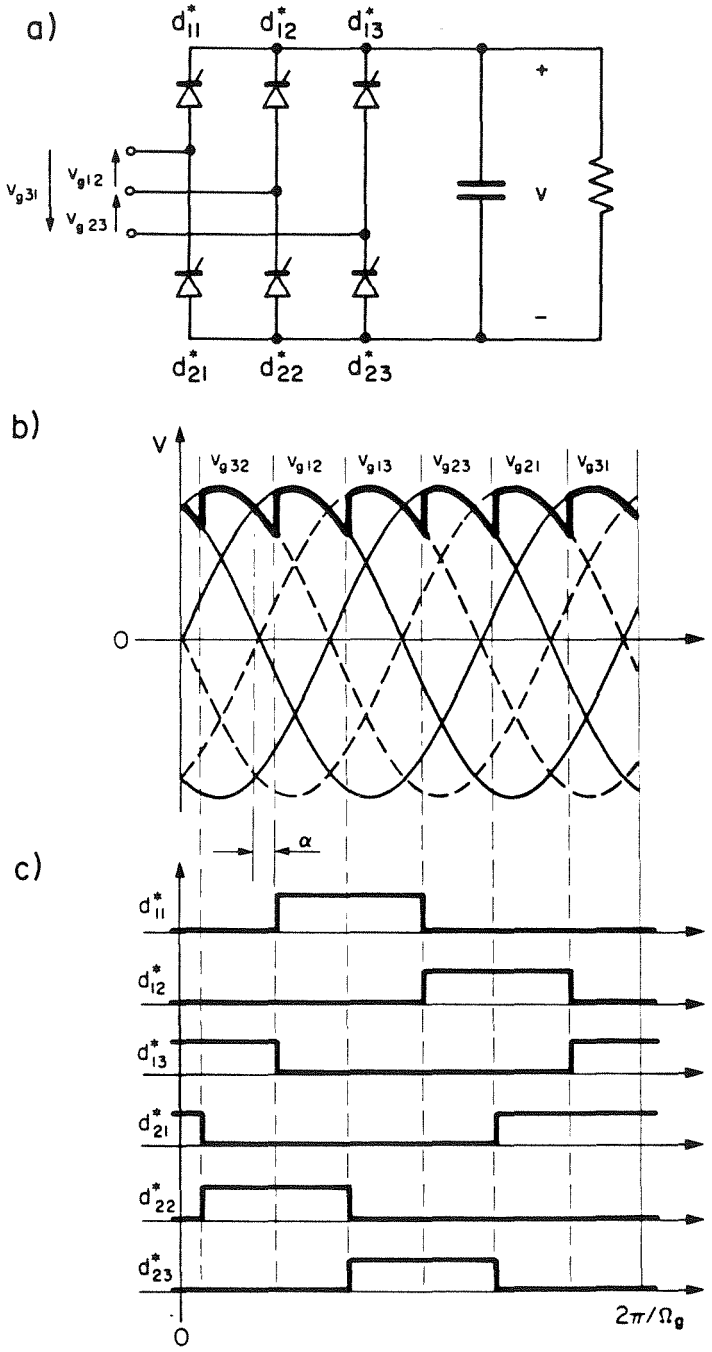


Fig. 5.2 (a) Phase-controlled rectifier, (b) its output (thick) voltage in relation to input (thin and dotted) line voltages, and (c) six-stepped switching functions.

the familiar six-stepped sequence. Thus, each of the three throws in one switch is activated for 120°, with the falling edge of one trailed by the rising edge of the next. Two corresponding throws in the two switches are 180° out-of-phase. Each line cycle then consists of six distinct switched networks corresponding to six different line voltages, as is obvious from Fig. 5.2(b).

Control of the output is achieved via the *firing angle* α defined according to Figs. 5.2(b) and (c). It can be shown that the output voltage v is proportional to $\cos\alpha$, with the peak value approximately equal to the line amplitude [24]. The topology thus steps the source amplitude *down* with a *nonlinear* dc gain function. Two-quadrant operation is available with proper implementation of the switches.

The use of firing angle to influence the output voltage, however, forces the fundamental component of line current to be out-of-phase with the input phase voltage. Since the angle α alone determines both the output level *and* input displacement angle (the angle between phase voltage and fundamental component of line current), the second quantity has to be sacrificed to gain tight control of the first. Therefore, the input displacement factor (cosine of the displacement angle) of the phase-controlled rectifier is always poorer than that of the bridge rectifier. It is always inductive and becomes worse at lower firing angle or output voltage.

Another drawback of the circuit arises from the low switching frequency itself, and it is the *large ripple* in the output waveform, as is evident from Fig. 5.2(b). This ripple contains $6n^{th}$ harmonics whose patterns vary with firing angle. To filter out these harmonics requires large reactive elements which not only are bulky and costly, but also impede the speed of the system.

Harmonics are also found in input line currents because of six-stepped operation of the switches. They are difficult to eliminate because they exist at low frequencies and change as a function of firing angle. In general, they can be found at $(6n+1)$ times the source frequency and become more objectionable at lower output. When coupled with finite line impedances, they generate distortion in the line voltage which then propagates to other customers of the power company. They, together with low power factor, increase the volt-ampere rating of generation and distribution facilities.

In view of later extension of the phase-controlled rectifier into a slow-switching cycloconverter, it is beneficial to preview the bidirectional implementation of the circuit in Fig. 5.2(a). There, the switches are two-quadrant-in-voltage if the converter has to carry only "positive" current. To extend the "positive" converter of Fig. 5.2(a) into four-quadrant operation, it is logical to *anti-parallel* it with a "negative" converter to create the "dual" converter in Fig. 5.3. Recall that an analogous practice has been observed earlier in the *switched-mode power amplifier* where two *two-quadrant-in-current* dc-to-dc converters are oriented in a "push-pull" fashion so that the amplifier can interface with both polarities of current *and* voltage.

It is important to differentiate each pair $d_{wkp}{}^*$ and $d_{wkn}{}^*$ ($w \equiv 1$ or 2 and $k \equiv 1$, 2, or 3) as *two two-quadrant throws* instead of *one four-quadrant throw* even though they appear anti-parallel in the structure. In fact, since they are anti-parallel, only one of them can undergo *natural commutation* at any given instant. Hence, they cannot commutate *simultaneously* as in a four-quadrant realization. The true four-quadrant

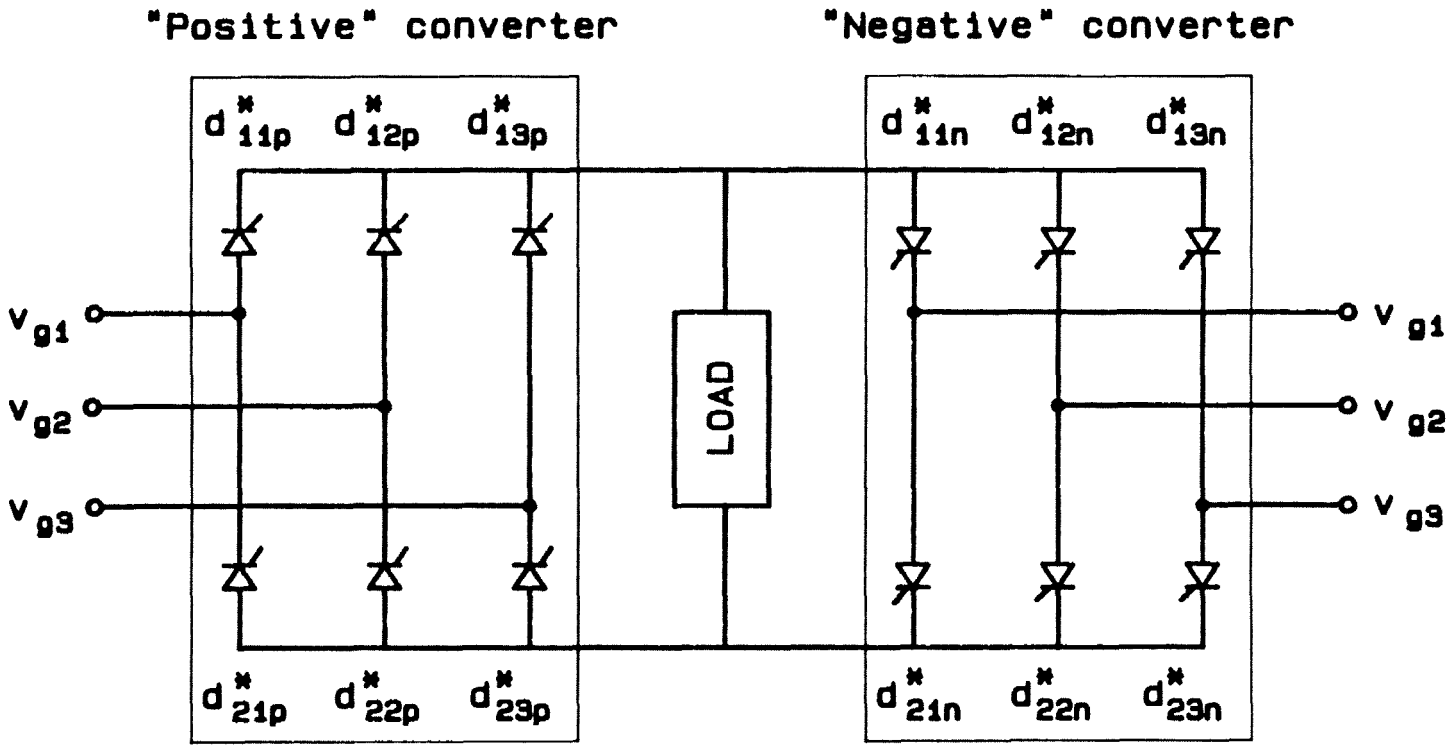


Fig. 5.3 The "dual" phase-controlled rectifier capable of four-quadrant operation.

switch is introduced later in conjunction with fast-switching cycloconverters.

Two different modes of operation associate with the dual converter of Fig. 5.3. In the "circulating current-free" mode, only either the positive or negative half conducts at any time, depending on the direction of load current. This mode necessitates circuitry to detect the cross-over point for transition from one set of thyristors to the other. In the "circulating current" mode, the d_{wkp}^{*} and d_{wkn}^{*} throws are fired at opposite angles so that the two half-converters synthesize the same *average* voltage to the load. These throws inevitably short out the line because they are not completely synchronized in commutation. Therefore, a "circulating-current reactor" is always inserted between the positive and negative converters to limit circulating current between them.

Besides the dual converter arrangement, a variety of other versions of the phase-controlled rectifier also exist. These configurations employ transformers connected to synthesize more than three balanced polyphase voltages from a three-phase line. More thyristors are then added to allow the load to communicate with the new phases. This "multiphasing" technique increases the power handling capability and improves the input and output harmonic situation of the basic phase-controlled rectifier.

To summarize, slow-switching rectifiers typically use the bridge topology switched in a six-stepped manner. Control of the output is achieved by changing the "firing angle" of the switches. Because of low switching frequency, the phase-controlled rectifier exhibits a fair amount of harmonics at both ports, poor input power factor, and other undesirable characteristics. These disadvantages have motivated the study of other

alternatives to switched-mode rectification. The following section examines the most recent approach, which relies on *faster* switching frequency to circumvent the aforementioned drawbacks.

5.2 Rectifiers Switched at High Frequency

Few examples of rectifiers switched above two decades of the line frequency are reviewed below. The first assembles three *nonlinear* PWM dc-to-dc converters and closes three separate loops to build a rectifier with high-quality input currents [28]. The second implements multiloop control of the conventional bridge rectifier switched at high frequency [29]. The last processes three-phase into dc power via a resonant link [35].

5.2.1 Rectifier Using Dc-to-Dc Regulators

As is proposed in [28], this circuit is an example of the *integration* principle in which many dc-to-dc blocks constitute the phases of a multiphase system. Each phase uses a one-quadrant flyback converter whose input is the rectified line voltage, as is illustrated in Fig. 5.4. The rectification is achieved by four *uncontrolled* diodes connected across one of the three lines. Control is possible through the single output transistor.

Because of the nonlinearity of the flyback stage, simple sinusoidal duty ratio modulation generates distortion at the output. Therefore, multiple feedback loops are closed around the circuit to ensure that the line current is sinusoidal; once the input current is ideal, the output voltage is expected to be clean. All states as well as the line voltage are involved in the design of control circuit.

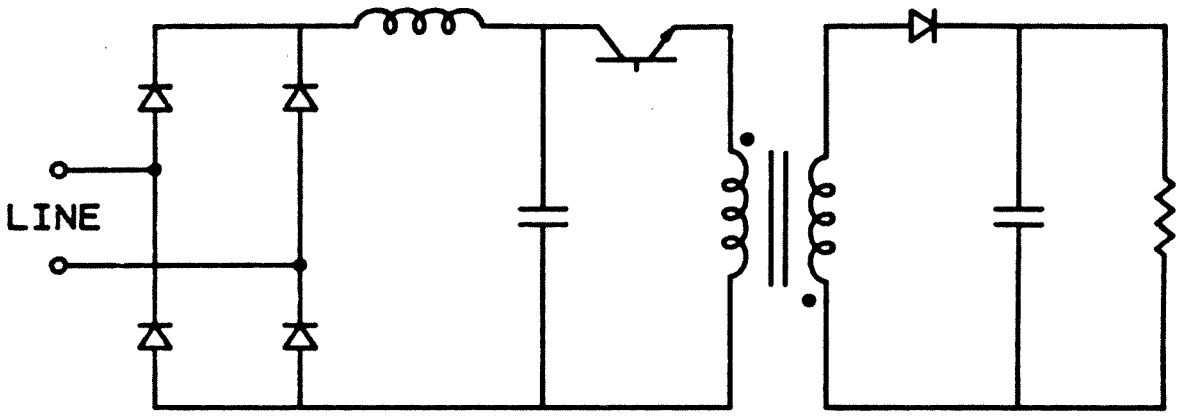


Fig. 5.4 Flyback dc converter used as one phase of a polyphase rectifier.

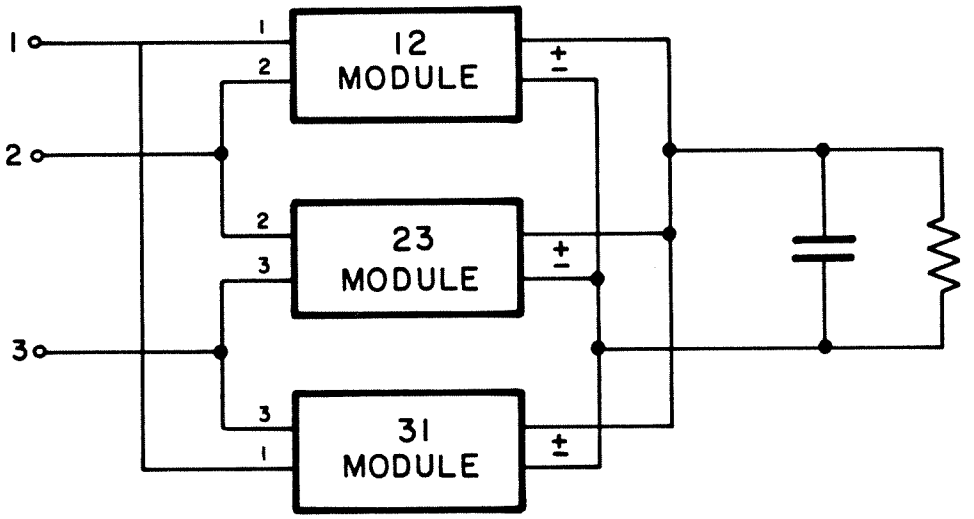


Fig. 5.5 Ac-to-dc converter using three flyback dc regulators.

The integration of the three resulting *dc-to-dc regulators* into a three-phase rectifier is pictured in Fig. 5.5. The inputs of the blocks are configured in a "delta" on the line. The output diodes and the dotted ends of transformer secondaries are then tied together to feed one common load.

Ease of isolation is one of the first characteristics enumerated in [28] owing to high switching frequency. Fast switching also allows low values of reactive elements and, consequently, quick transient response and broad small-signal bandwidth. The input phase current tracks the reference very closely, forcing the input power factor to be very close to unity. The amplitude of the reference is used to control the dc voltage level. Third harmonics can be introduced into the module current, without degradation of the line current, to alleviate current stress on all devices. The transformer secondaries can be staggered to optimize the current ripple seen by the load.

In spite of the above achievements, the proposed approach has not yet fully utilized all benifits of fast switching. The very integration of many dc-to-dc converters instead of searching for a genuine *three-phase* topology forfeits the advantage of *balanced polyphase synergy*. As a result, the circuit employs three separate inductors which may be merged into *one* in some "right" topology yet to be conceived. These inductors also have to carry harmonics that increase the overall rating of the design. A truly polyphase converter should process no harmonics both externally and *internally*.

The circuit in Fig. 5.4 is certainly economical because it requires only three transistors and interfaces with ac input through simple diode bridge. The diodes, however, do not allow power to flow *backward* or

generate *reactive* power for the utility company. If the topology were to incorporate these two desirable attributes, it would indeed require a large number of active switches.

It is important to recognize that only a limited number of dc-to-dc topologies can be used in the integration plan. The flyback has been chosen in this case since its *ideal* dc gain can approach *infinity*. This high gain is essential to boost the line voltage in zero-crossing region to the regulated dc output. However, the dc gain of a physical power processor cannot be made arbitrarily large because losses are always present. Therefore, it is not surprising that [28] observes "abnormal" behavior, which may come from discontinuous conduction mode or instability, at cross-over.

Dc-to-dc converters with boosting capability generally have nonlinear gain characteristics. Therefore, they always rely on feedback loops to ensure no low-frequency distortion at the output. The design of such a loop, however, is not trivial because the system is time-varying. It has been shown in [20] that even the steady-state vector, which participates in perturbed dynamic equations, is not described accurately by the "quasi-dc" assumption. By the same token, this assumption should only be invoked cautiously for small-signal analysis, especially when the system bandwidth is comparable with the line frequency.

To summarize, integration of many dc converters to synthesize a polyphase rectifier is a simplistic concept suitable for some practical applications. It both exemplifies some potentials of fast-switching rectification and opens way to more refinements in the future.

5.2.2 Fast Switching Bridge Rectifier with Multiloop Control

The phase-controlled rectifier reviewed in the first section cannot generate clean power because it switches at the frequency of the main. Its *topology*, however, is a genuinely three-phase one that, as is explained in the subsequent chapter, has *ideal* characteristics. The authors of [29] exploit these characteristics by switching the topology with fast PWM, instead of slow six-stepped, drives.

The basic topology discussed in [29] is the familiar three-phase bridge with two triple-throw switches at the input and a generalized load at the output, as is shown in Fig. 5.6. The LC filters between the line and switches are there to smooth out current pulses and not essential to the operation of the circuit. Feedback and feedforward are used in a multiloop control scheme to regulate the output power and maintain unity power

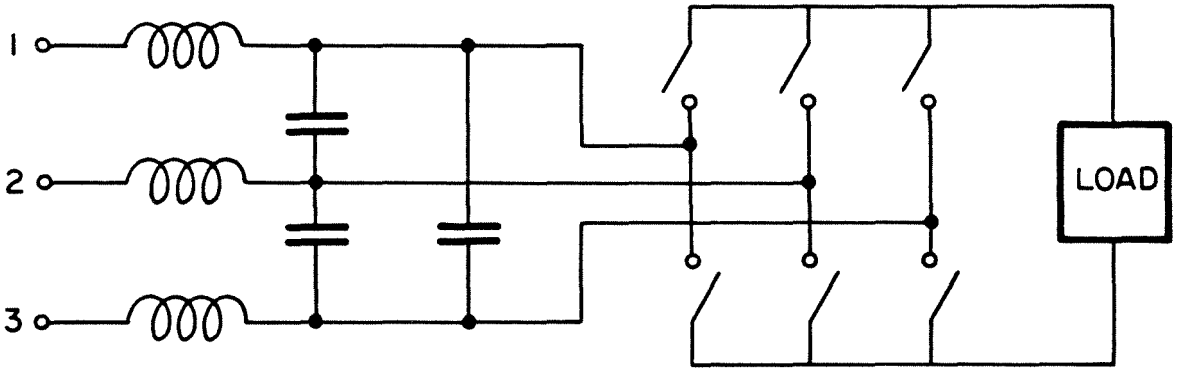


Fig. 5.6 Multiloop ac-to-dc converter with unity power factor.

factor at the input.

The control algorithm recognizes seven distinct switched networks associated with all possible combinations of switch positions. Out of the seven, one is the "zero" state, in which two switches short together, and six are the "transfer" states, in which two switches apply line voltages of both polarities to the load. A complex "transfer vector," which takes on seven discrete values corresponding to seven switched topologies, can then be defined as control parameter and is used to characterize the system equations. The value of this vector that produces the correct amount of output power for known input conditions is next computed by the control loops. The result decides which two switched networks are to be activated in a switching cycle and how long each should exist. When the two transfer states are over, the system rests in the zero state till the beginning of next switching period.

Results simulated on computer have proved good transient responses, a benefit of fast switching. The output current contains mostly switching ripples and no nonlinear harmonics. The input power factor is satisfactorily close to unity.

Although the proposed ac-to-dc conversion strategy is a step in the right direction, it signifies that a great deal of studies still need to be devoted toward the understanding and modeling of rectifiers. For instance, its operation can be explained in terms of more general concepts, such as switching function and *duty ratio*, instead of the topological variable "transfer vector." In particular, duty ratio facilitates both the modeling and design of switched-mode converters because it is *continuous*. Characterization of the rectifier by a "transfer vector," on the contrary,

leads to complicated control algorithm and cumbersome switching waveform synthesis.

In requesting all seven switched networks, [29] does not acknowledge a multitude of other switching alternatives. Recall that at high switching frequency, *independent* switches can be driven *independently*. Therefore, there are many switching policies that require only a couple of switched circuits and, hence, much simpler hardware. Nevertheless, more involved drives do possess their own merits. The one used in [29], which can be implemented more properly, is shown later to output a significantly higher dc level than the more straightforward drives.

In summary, the bridge rectifier promises superior performances when switched in the PWM mode. Although satisfactory results have been obtained, they pertain only to a closed-loop system. More fundamental analysis thus needs to be carried out to extract all open-loop properties. This requires the identification of more appropriate control variables and more rigorous steady-state and dynamic modeling.

5.2.3 Resonant Rectifiers

Resonant conversion has attracted more and more attention in the past few years. In contrast to the PWM principle, the resonance principle puts prime importance on reactive elements. These elements realize a "resonant tank" that serves as an intermediate energy storage and transfer link. The natural time constant of the tank is comparable to the switching time. Consequently, the energy in the tank or the whole system can be controlled via the switching frequency [35].

A block diagram of the resonant rectifier is described in Fig. 5.7. The heart of the system is the "resonant block," which usually contains a series LC combination. It taps power from the source through "modulation switches" and simultaneously delivers power to the load through "demodulation switches."

There are two triple-throw switches oriented in a fashion similar to that of the bridge rectifier in Fig. 5.6. They are driven by "pulsed six-stepped" switching functions that combine the six-stepped switching of a phase-controlled rectifier with the high-frequency switching of a dc-to-dc resonant converter. A line cycle is thus divided into six equal intervals during each of which the line voltage with maximum amplitude acts as the dc input to the resonant circuit. Each six-stepped interval is decomposed further into many short switching periods. In each switching period, four of

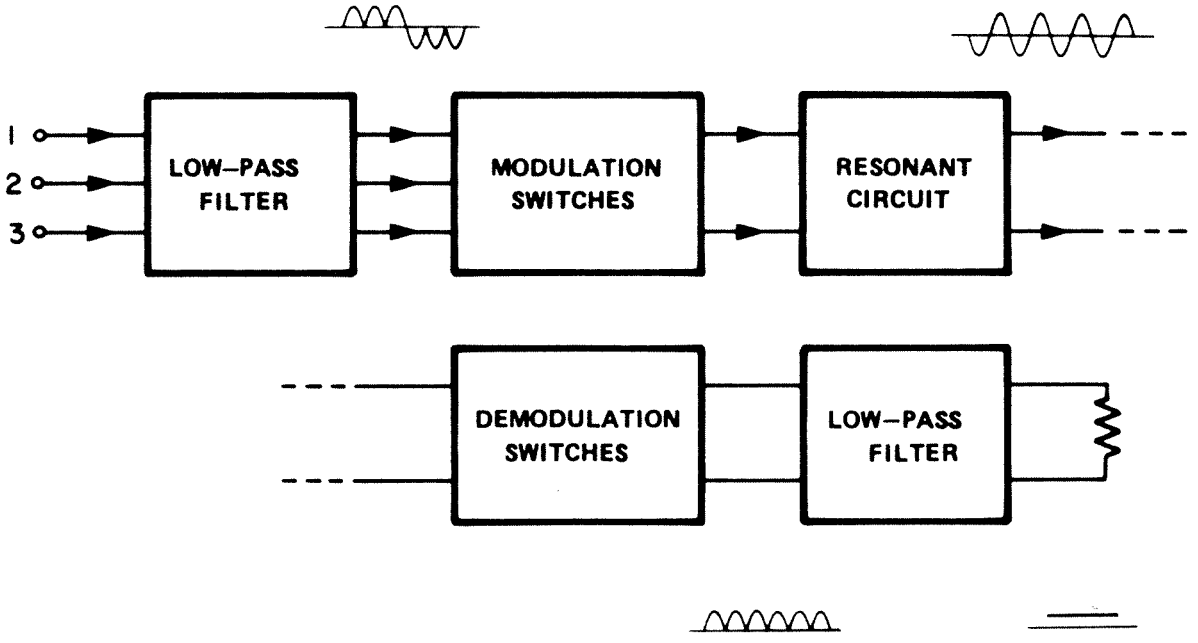


Fig. 5.7 Functional block diagram of a resonant rectifier showing a resonant link surrounded by modulation and demodulation switches.

the six input throws invert the line into an *ac* voltage that then excites the resonant tank.

The resonant current consists of both positive and negative pulses made from sinusoidal segments. The area of each pulse can be coded with the desired amount of energy by selection of the proper switching frequency. The energy pulses are rectified and then passed to the load by the demodulation switches.

Under proper conditions of switching frequency, load, and other circuit parameters, the current through the active switch falls to zero before the turn-off signal arrives [36]. In other words, the circuit can be load-commutated. This feature makes the resonant rectifier very attractive for multikilowatt applications for which switching devices with very short turn-off time are unavailable. Even if fast transistors were available at this high power level, it is still much more preferable to turn off the switch when it carries very little or no current.

According to [35], the rectifier provides the freedom of control of input power factor and direction of power flow. Its current waveform, however, exhibits a fair amount of line harmonics typical of six-stepped switching. Its output voltage also contains harmonics at multiples of six times the main frequency. Fortunately, the ripple at the output diminishes with an increasing number of resonant pulses per source cycle.

In general, the implementation of a resonant rectifier requires more hardware than that of a PWM circuit. For instance, the one in [35] contains ten inductors and one capacitor to realize just the resonant tank. Its modulation switches are composed of six throws; and its demodulation switches, four. The input throws have to be four-quadrant to carry the ac

resonant current and block the ac main. They necessitate sensing circuitry that samples conditions of voltages and currents in the rectifier and logic blocks that decide which throw is to be turned on or off next.

Circuit complexity is worthwhile only if it is outweighed by the advantages offered by the circuit. At present, all positive attributes of resonant rectification have not yet been brought to light because not much analysis has been done on this class of converters. The analysis itself is difficult since time constants of the circuit is at the same order of magnitude as the switching period. Even in the simpler case of dc-to-dc conversion, it is not until recently that [36] proposes more proper ways to define and study the resonant conversion principle. Hopefully, the techniques presented there can be generalized to model resonant rectification in the same way that describing equations are modified to treat PWM rectification. Only then, it is possible to answer such question as whether a resonant rectifier can have truly dc output voltage and sinusoidal input currents when controlled by simple (e.g., sinusoidal) frequency modulation functions in an open-loop manner. If feedback is the only way to attain ideal terminal behaviors, then it is necessary to know more about dynamics of the converter. Only when these issues are fully understood can the resonant rectifier gain its full momentum.

In summary, this chapter has reviewed ac-to-dc converters that switch at low or high frequency. The phase-controlled rectifier has been cited as an example of the low-frequency category. It is then switched at high frequency and controlled by multiple loops to acquire clean power flow. Besides the bridge topology, many dc regulators can be integrated to form a polyphase rectifier. The use of high-frequency resonant link is also a

promising alternative to switched-mode rectification.

As a result of this review, it is evident that fast switching cures many problems created by slow switching. The high-frequency circuits presently available, however, have not yet reaped all benefits of fast switching. There is thus a strong urge to reconsider the rectification theory, first, from a topological viewpoint. A unified analysis and modeling technique then needs be proposed so that fast-switching rectifiers can be understood thoroughly and used confidently.

CHAPTER 6

FAST-SWITCHING SINUSOIDAL PWM RECTIFIERS

This chapter studies *fast-switching* polyphase-to-dc converters that use *sinusoidal* pulse-width modulation to rectify sinusoidal inputs into clean dc output in an *open-loop* fashion. The number of input phases can be any integer larger than one. If there are *two* inputs, the second one is delayed from the first by $\pm 90°$. If there are N (greater than two) phases, any two adjacent ones are displaced by $\pm \frac{360°}{N}$. The phase sequence is assumed to be positive, and the input frequency can be any positive or negative real number.

Four issues are investigated in this chapter. The *buck*, *boost*, *buck-boost*, and *flyback rectifiers* are characterized in the first section. The *describing equation* of the boost topology in both stationary and rotating reference frames is exemplified in the second section. *Steady-state*, *dynamic*, and *canonical models* are then solved in the remainder of the chapter.

6.1 Description of Topologies

The buck, boost, buck-boost, and flyback topologies are presented in the following three subsections. Their switch distributions are analyzed in conjunction with their filter arrangements. Since only *duty ratios*, not exact timing waveforms, of the switches influence circuit behavior, explanations are

directed toward duty ratio assignments, not switching functions. Furthermore, duty ratios are assumed to be *continuous* in this chapter to facilitate the qualitative understanding of rectifiers.

6.1.1 Buck Rectifier

The *buck rectifier* is the extension of the fast-switching buck dc converter or slow-switching phase-controlled rectifier into fast-switching rectification. An N-phase topology, where $N>2$, is illustrated in Fig. 6.1; voltage-fed characteristic is evident. The N input sources here, as well as throughout the thesis, satisfy

$$v_{gk} = v_g \cos[\theta_g - (k-1)\frac{2\pi}{N}], \qquad (1 \le k \le N) \tag{6.1}$$

where

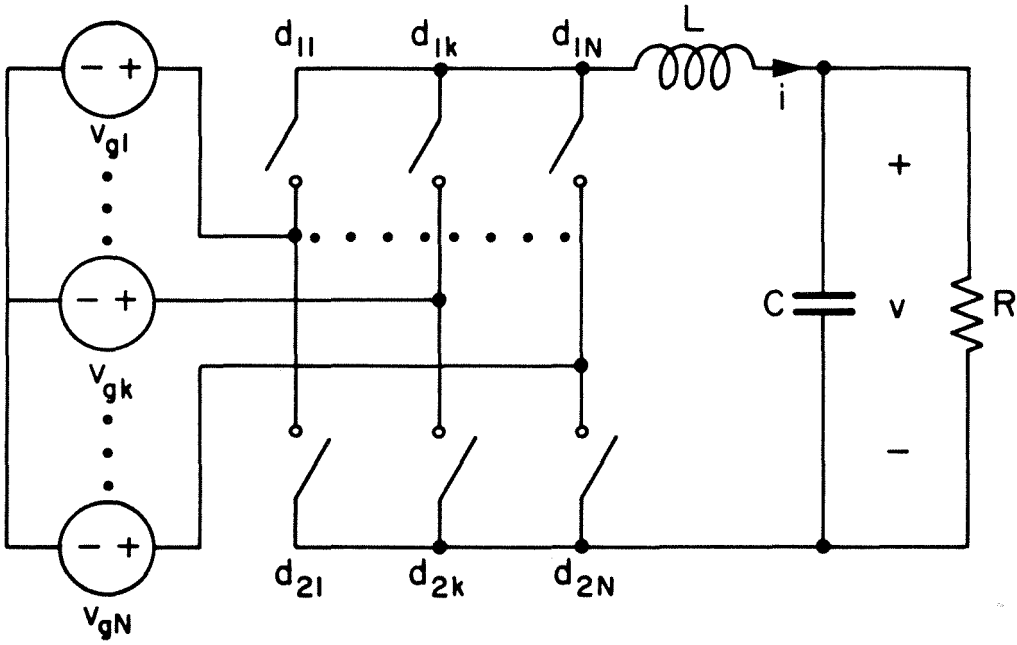


Fig. 6.1 N-phase buck rectifier with two N-throw switches pulse-width-modulated by sinusoidal functions.

$$\theta_g = \int_0^t \omega_g(\tau)d\tau + \varphi_g \tag{6.2}$$

where the lower case v_g and ω_g denote the *instantaneous source amplitude* and *frequency*, respectively. The frequency can be any real number, where a negative value means a reversal of phase sequence.

Although the buck and phase-controlled rectifiers share the same topology, their *switching principles* differ. While the latter is switched at low frequency in six-stepped sequence, the former is *pulse-width-modulated sinusoidally* at high frequency by

$$d_{wk} = \frac{1}{N} + \frac{d_{mw}}{N}\cos\left[\theta_w - (k-1)\frac{2\pi}{N}\right],\ (1\le w\le 2 \text{ and } 1\le k\le N) \tag{6.3}$$

where

$$d_{mw} \le 1 \qquad \text{and} \qquad \theta_w = \int_0^t \omega_g(\tau)d\tau + \varphi_w \tag{6.4a,b}$$

Note that dc components in the duty ratios of the two throws connected to the same phase (k) ought to be equal. Modulation amplitudes and phases, on the other hand, are independent as the two switches are so. The modulation frequency has been assumed *locked* to the line frequency; this assumption serves most general applications and can always be relaxed if necessary.

The duty ratios d_{1k} and d_{2k} do not affect the network directly; rather, it is the *effective duty ratio*

$$d_k = d_{1k} - d_{2k} = \frac{2d_m}{N} \cos\left[\theta - (k-1)\frac{2\pi}{N}\right] \tag{6.5}$$

where

$$d_m \leq 1 \qquad \text{and} \qquad \theta = \int_0^t \omega_g(\tau)\, d\tau \tag{6.6a,b}$$

that influences circuit performance. Therefore, the modulations of the switches should have equal amplitudes and opposite phases to maximize the *effective modulation amplitude* $\frac{2d_m}{N}$ defined in Eq. (6.5). The resulting peak value of this amplitude is $\frac{2}{N}$.

PWM action inadvertently generates switching noise. Therefore, an LC filter follows the switches to attenuate high-frequency harmonics; filters may also precede the switches to smooth out line currents. Filter components, of course, can be made small by increase of switching frequency.

Specifications for the two-phase (or semi-four-phase) buck rectifier are analogous to the above. The circuit itself is described in Fig. 6.2, which includes two triple-throw switches feeding the line into the filter, load combination. The third pair of throws has been added to return current back to the source neutral.

The main is defined according to

$$v_{gk} = v_g \cos\left[\theta_g - (k-1)\frac{\pi}{2}\right], \qquad (1 \leq k \leq 2) \tag{6.7}$$

where θ_g is as given in Eq. (6.2). Correspondingly, the duty ratios satisfy

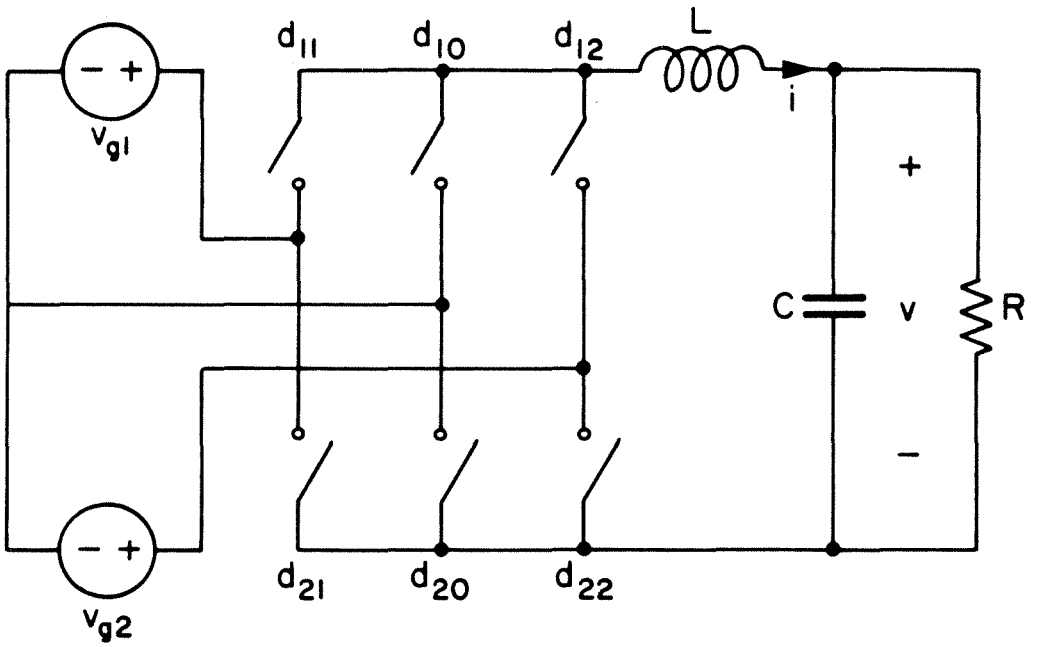


Fig. 6.2 Two-phase buck rectifier.

$$d_{wk} = \frac{1}{2+\sqrt{2}} + \frac{d_{mw}}{2}\cos\left[\theta_w - (k-1)\frac{\pi}{2}\right],\ (1 \le w,k \le 2) \tag{6.8}$$

where

$$d_{mw} \le \frac{2}{2+\sqrt{2}} \tag{6.9}$$

and θ_w is as given in Eq. (6.4b). The definition of effective duty ratio modulation d_k given in Eq. (6.5) also applies to the two-phase case.

In summary, this subsection has proposed the ***buck rectifier*** that is composed of two multiple-throw switches and an LC filter connecting the switches to the load. The switches operate at ***high frequency*** according to the *PWM* principle. Their performances are characterized in terms of duty

ratios that require only easy-to-synthesize *sinusoidal* modulations. The specifications presented here are used later with describing equations to model the *open-loop* behavior of the rectifier.

6.1.2 Boost Rectifier

Natural extension of the boost dc-to-dc converter or reverse operation of the buck inverter (Fig. 3.1) results in the *boost rectifier*. This topology belongs to the *current-fed* family, as is pictured in Fig. 6.3 for the N-phase case, where $N > 2$. It consists of N small inductors, which can be integrated into a *single* magnetic piece, that transform the source voltages into a set of balanced polyphase currents. The N double-throw switches at the output end then rectify these ac currents into a dc current for the resistive load. This configuration guarantees smooth input currents although

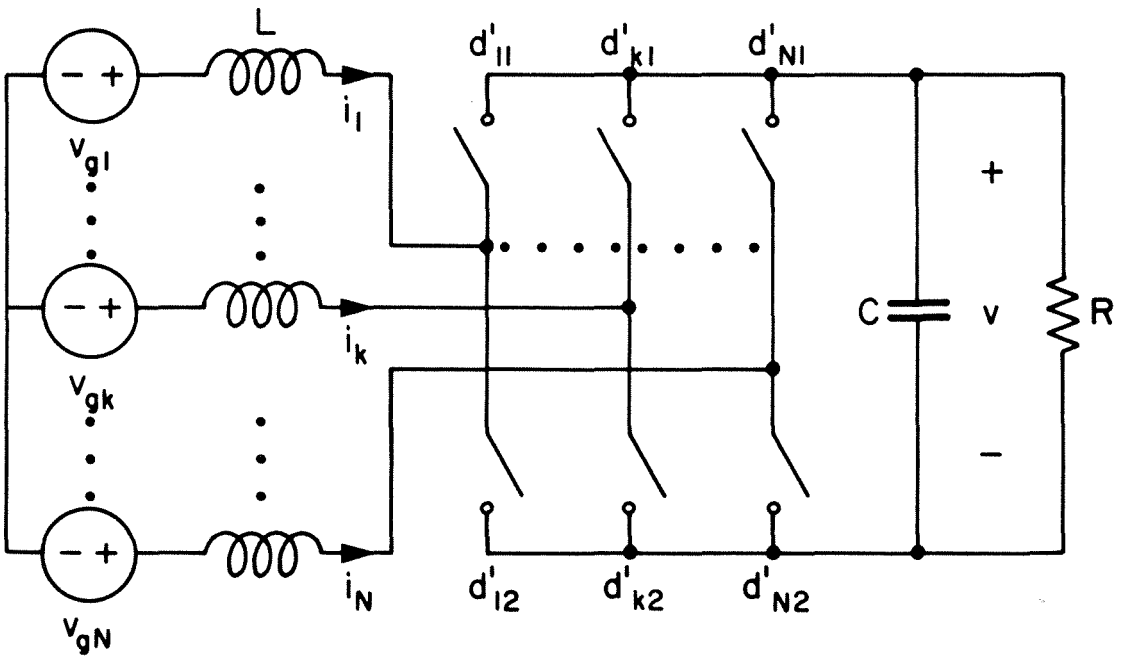


Fig. 6.3 N-phase boost rectifier with N double-throw switches pulse-width-modulated by sinusoidal functions.

its output ripple is higher than that in the buck topology.

The line voltages here are as specified earlier in Eq. (6.1). Duty ratios of the upper throws satisfy

$$d'_{k1} = \frac{1}{2} + d'_k, \qquad (1 \le k \le N) \tag{6.10}$$

where "prime" (') signifies that the switches lie at the load side, and

$$d'_k = \frac{d'_m}{2} \cos\left[\theta - (k-1)\frac{2\pi}{N}\right] \tag{6.11}$$

where θ is as provided by Eq. (6.6), and

$$d'_m \le 1 \tag{6.12}$$

The duty ratios consist of dc components and *sinusoidal* modulations. Although any dc value may be chosen, $\frac{1}{2}$ is selected because it optimizes the *effective modulation amplitude* $\frac{d'_m}{2}$ of the *effective duty ratio* defined according to Eq. (6.11). Continuous PWM thus offers a peak modulation amplitude of $\frac{1}{2}$ for the boost rectifier. The modulation frequency has been locked to the line frequency although it does not have to be so in few applications.

The reduction of Fig. 6.3 to the semi-four-phase case is shown in Fig. 6.4. The three independent throws there are driven by

$$d'_{01} = \frac{1}{2} - \frac{d'_{m0}}{2} \cos\theta_0 \tag{6.13a}$$

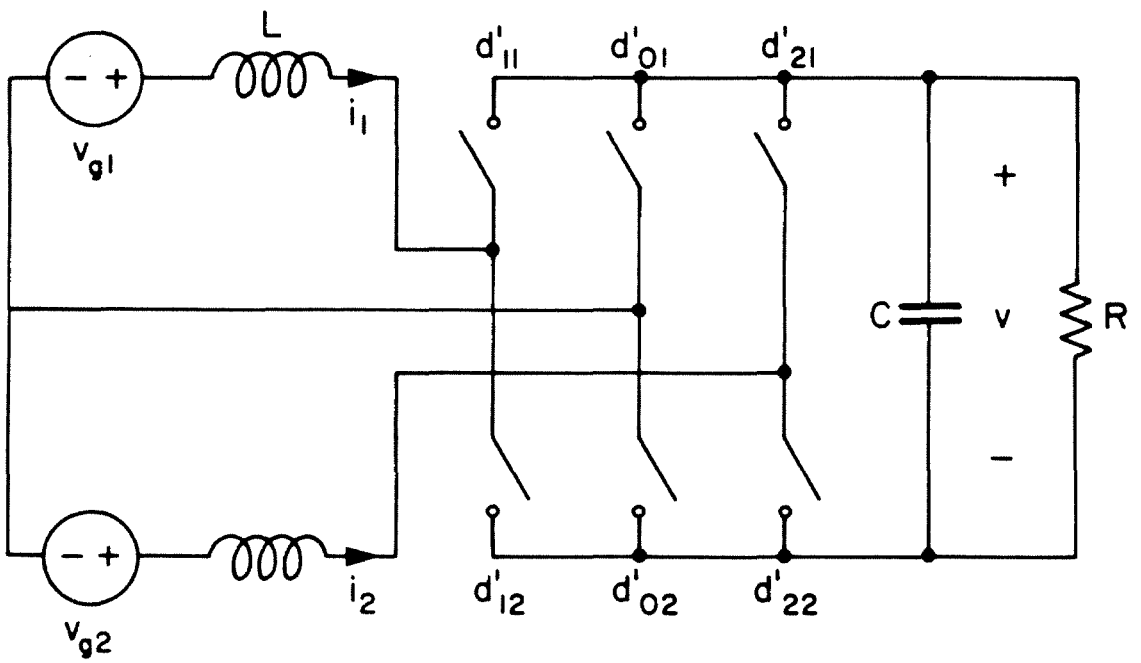


Fig. 6.4 Two-phase boost rectifier.

$$d'_{11} = \frac{1}{2} + \frac{d'_{m0}}{2}\cos\left(\theta_0 + \frac{\pi}{2}\right) \tag{6.13b}$$

$$d'_{21} = \frac{1}{2} + \frac{d'_{m0}}{2}\cos\left(\theta_0 - \frac{\pi}{2}\right) \tag{6.13c}$$

where

$$d'_{m0} \leq 1 \qquad \text{and} \qquad \theta_0 = \int_0^t \omega_g(\tau)d\tau - \varphi_0 \tag{6.14a,b}$$

The preceding equations can be proved to yield the maximum amplitude for the effective duty ratio

$$d_k' = d_{k1}' - d_{01}' = \frac{d_m'}{2} \cos\left[\theta - (k-1)\frac{\pi}{2}\right], \quad (1 \le k \le 2) \tag{6.15}$$

This value turns out to be $\frac{\sqrt{2}}{2}$, much larger than $\frac{1}{2}$ owing to the presence of the neutral switch.

In summary, this subsection has introduced the *boost rectifier* that converts sinusoidal voltages into sinusoidal currents by small input inductors and rectifies these currents into the load via output switches. The switches are *pulse-width-modulated at high frequency*; their duty ratios consist of simple *sinusoidal* functions. These specifications are shown later to synthesize very *clean* dc output and draw *sinusoidal* currents even when the circuit operates *open-loop*.

6.1.3 Buck-Boost and Flyback Rectifiers

The buck-boost and flyback rectifiers are considered together because their characteristics are very similar. The buck-boost topology is simply a buck rectifier with a "boosting" switch added to the output end of the inductor, as is illustrated in Fig. 6.5. Note that the *three* switches shown are *independent*. The two input ones rectify the ac line into a dc voltage, converted next into a dc current by the high-frequency inductor. The output switch then feeds this current into the load.

Under steady-state condition, the output duty ratio is *dc*. The input duty ratios are modulated according to the sinusoidal functions in Eq. (6.3). The definition of effective duty ratio and optimization of effective modulation amplitude for the buck-boost rectifier follow those established earlier for the buck rectifier.

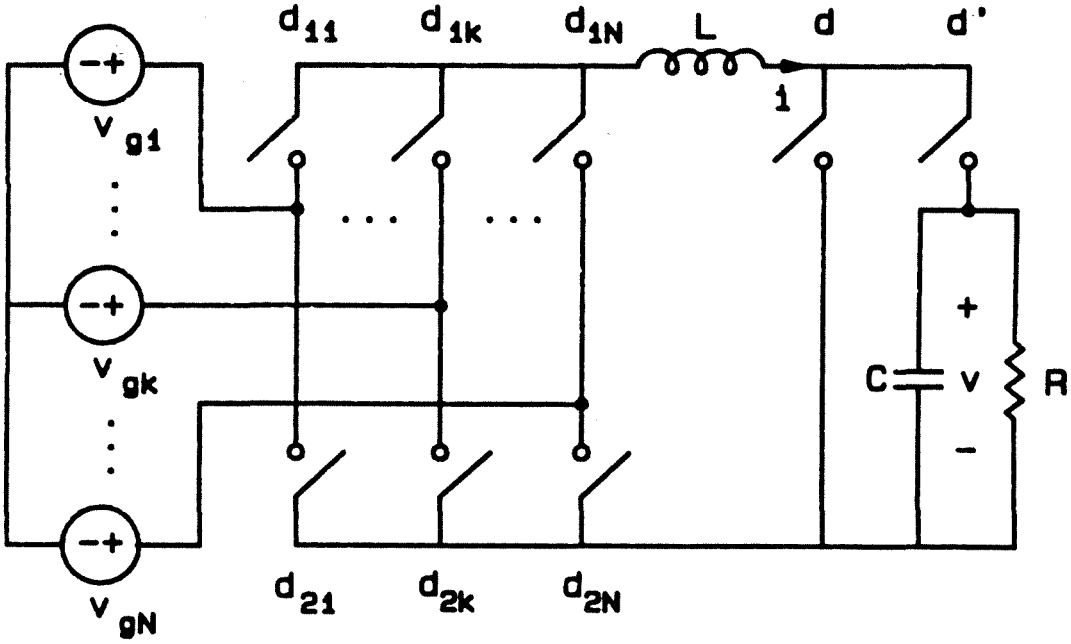


Fig. 6.5 N-phase buck-boost rectifier, cascade of an N-phase buck rectifier and a boost dc converter.

The two-phase version of Fig. 6.5 also exists. It is simply the two-phase buck rectifier of Fig. 6.2 with an extra switch at the load side of the inductor.

The buck-boost circuit cannot provide isolation because the inductor connects the source to the load during some part of the modulation cycle. However, its topology can be rearranged into that of the flyback rectifier described in Fig. 6.6 (for more than two phases) that allows isolation by separation of energy storage and transfer intervals. The flyback structure consists of *two* independent switches, instead of three as in the buck-boost. Each switch has three input throws and one output throw. The two output throws, however, can be merged into one since they are always in

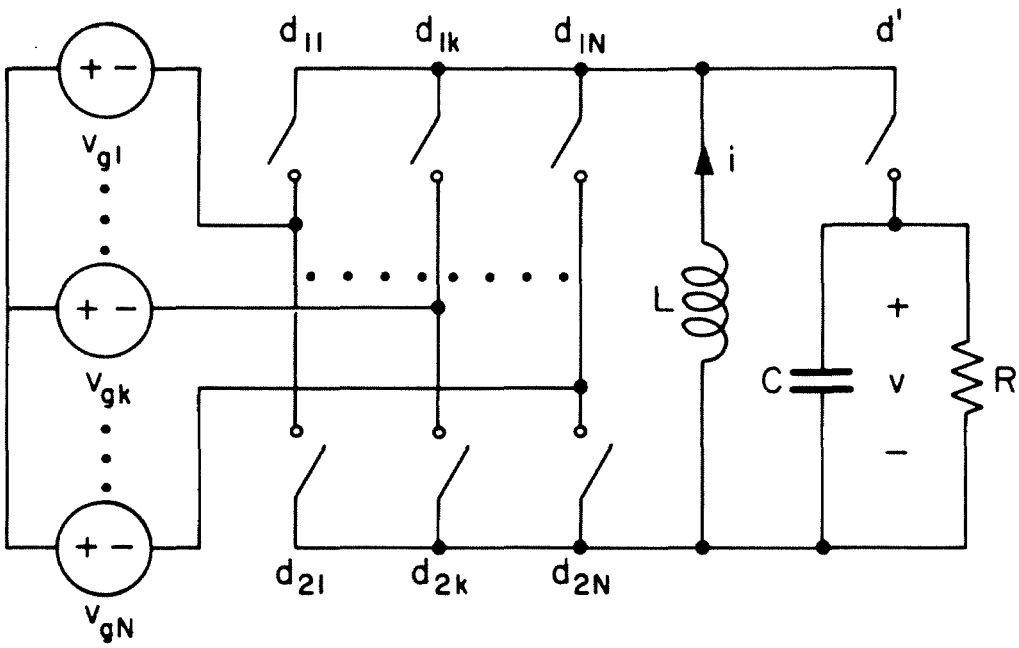


Fig. 6.6 N-phase flyback rectifier with one (N+1)-throw and one N-throw switch pulse-width-modulated by sinusoidal functions.

series.

Every switching cycle is divided into a charging period dT_s and a discharging period $d'T_s$. In the former, the input throws are activated according to

$$d_{wk} = \frac{d}{N} + \frac{d_{mw}}{N} \cos\left[\theta_w - (k-1)\frac{2\pi}{N}\right] \tag{6.16}$$

where

$$1 \le w \le 2\ , \quad 1 \le k \le N\ , \quad \text{and} \quad d_{mw} \le d \tag{6.17a,b,c}$$

and d_{mw} and θ_w obey Eq. (6.4). The ***sinusoidal*** modulations in these duty ratios rectify the source into a dc voltage, which establishes a dc current in

the inductor. The output throw then switches the inductor current into the load with the duty ratio

$$d' = 1 - d \tag{6.18}$$

The effective duty ratio d_k and optimal modulation strategy are as suggested by Eqs. (6.5) and (6.6).

The two-phase flyback rectifier is illustrated in Fig. 6.7. Its operating principle is similar to that of the N-phase case. Its input duty ratios are chosen as

$$d_{wk} = \frac{d}{2+\sqrt{2}} + \frac{d_{mw}}{2} \cos\left[\theta_w - (k-1)\frac{\pi}{2}\right], \quad (1 \le w, k \le 2) \tag{6.19}$$

where

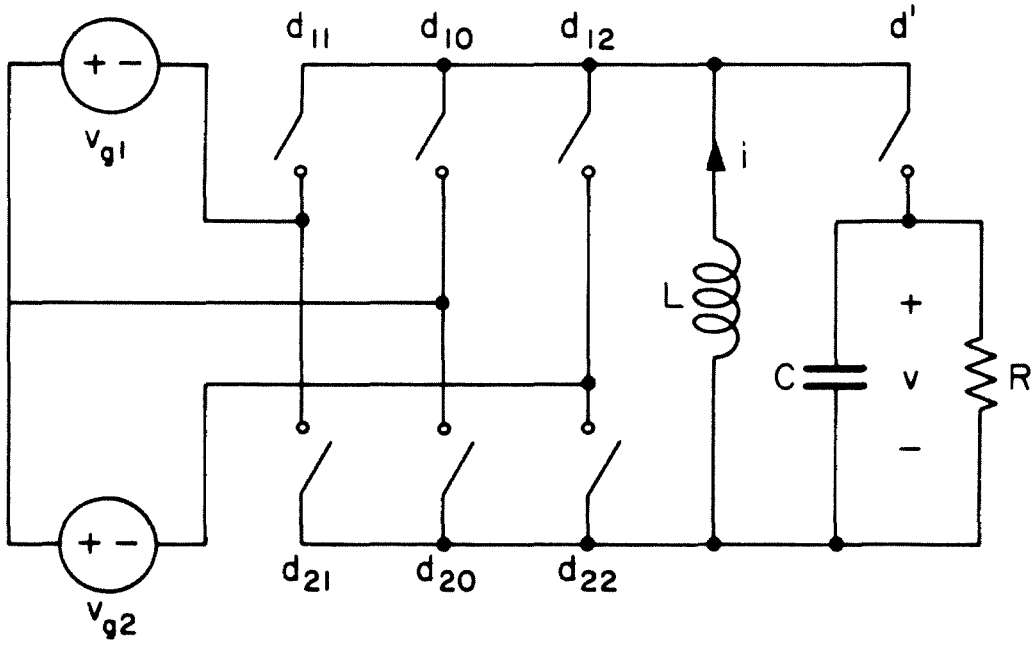


Fig. 6.7 Two-phase flyback rectifier.

$$d_{mw} \leq \frac{2}{2+\sqrt{2}}\, d \tag{6.20}$$

The topologies proposed in Figs. 6.5 through 6.7 employ only one inductor as intermediate energy link. They are actually the practical degenerates of more generalized buck-boost and flyback rectifier configurations which may contain an *arbitrary* number of inductors between the line and load. These inductors generally carry *ac*, as well as dc, currents as their associated switches are modulated at a frequency *different* from the main frequency. Such generalized topologies, however, are only of theoretical interest since their implementations require an excessive amount of hardware.

To recap, this subsection has suggested the *buck-boost* and *flyback rectifiers* pulse-width-modulated at much higher than the source frequency. Their input throws use easy-to-generate *sinusoidal* modulation functions to rectify the ac input; the rectified voltage is transformed into a dc current, which subsequently supplies the load via the dc duty ratio of the output throw. The next section shows that these simple *open-loop* specifications synthesize clean power at both input and output terminals.

6.2 Steady-State Performance

This section applies the describing equation technique presented in Chapter 1 to analyze the rectifiers introduced in the previous section. Equations are written first in the *stationary* (or *abc*) frame of reference and then transformed to the *rotating* (or *ofb*) coordinates where the system description is more meaningful and well-defined.

Procedures for the buck, buck-boost, and flyback topologies are straightforward because rectification takes place right at the input switches *before* the involvement of any reactive elements. Thus, the buck rectifier can be modeled as a buck dc-to-dc converter whose input voltage is $v_g \cos\varphi_g$ and duty ratio is d_m. Likewise, the buck-boost (or flyback) rectifier is equivalent to a boost dc-to-dc converter whose dc input is $d_m v_g \cos\varphi_g$ and duty ratio is d.

The analysis of the boost topology is more instructive because the ac switches of this circuit lie at the output side. Switching function descriptions of Figs. 6.3 and 6.4 in the abc coordinate system lead to the following matrix equation for boost rectifiers with two or more phases

$$\mathbf{P}\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{6.21}$$

where bold uppercase and lowercase letters signify a matrix and a vector, respectively; "$\dot{\mathbf{x}}$" abbreviates "the first derivative of $\mathbf{x}$";

$$\mathbf{P} = \begin{bmatrix} L\mathbf{I}_N & \mathbf{o}_N \\ \mathbf{o}_N^T & C \end{bmatrix}, \quad \mathbf{x} = \begin{bmatrix} [i_k] \\ v \end{bmatrix} \tag{6.22a,b}$$

where $\mathbf{I}_N$ is the $N \times N$ unity matrix, $\mathbf{o}_N$ is the $N \times 1$ zero vector, and $1 \le k \le N$;

$$\mathbf{A} = \begin{bmatrix} \mathbf{O}_N & -[d_k'] \\ [d_k']^T & -1/R \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \mathbf{I}_N \\ \mathbf{o}_N^T \end{bmatrix} \tag{6.22c,d}$$

where $\mathbf{O}_N$ is the $N \times N$ zero matrix and d_k' is given by Eq. (6.11) for $N > 2$ or Eq. (6.15) for $N = 2$; and

$$\mathbf{u} = [v_{gk}] \tag{6.22e}$$

where v_{gk} is defined by Eq. (6.1) for $N>2$ or Eq. (6.7) for $N=2$. The term d_k' in matrix $\mathbf{A}$ indicates that the circuit is inherently *nonlinear*. Nevertheless, the following analysis proves that this nonlinearity does *not* imply low frequency harmonics in output voltage and input current waveforms.

Equations (6.21) and (6.22) are difficult to manipulate as they are time-varying. Therefore, they are transformed to the ofb coordinates by

$$\tilde{\mathbf{T}} = \begin{bmatrix} \tilde{\mathbf{T}}_i & \mathbf{o}_N \\ \mathbf{o}_N^T & 1 \end{bmatrix} \tag{6.23}$$

where "tilde" ($\tilde{}$) implies a complex or transformed quantity. This transformation invokes $\tilde{\mathbf{T}}_i$ described in Eq. (B.3b) ($N>2$) or Eq. (B.3a) ($N=2$) to act on i_k, balanced polyphase, while passing v, dc single-phase, intact to the new frame. It is selected to be in-phase with the effective duty ratio d_k'.

Under $\tilde{\mathbf{T}}$, Eq. (6.21) becomes

$$\mathbf{P}'\dot{\tilde{\mathbf{x}}} = (\mathbf{A}_r + \mathbf{A}_d d_e' + \mathbf{A}_\omega j\omega_g)\tilde{\mathbf{x}} + \mathbf{B}'\tilde{\mathbf{u}} \tag{6.24}$$

where

$$d_e' = \frac{\sqrt{N}}{2}\frac{d_m'}{2} \tag{6.25}$$

is the *transformed duty ratio*, the transformation of the effective duty ratio d_k' by $\tilde{\mathbf{T}}_i$;

$$\mathbf{P}' = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & C \end{bmatrix}, \quad \tilde{\mathbf{x}} = \begin{bmatrix} \tilde{i}_f \\ \tilde{i}_b \\ v \end{bmatrix}, \quad \mathbf{A}_r = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -1/R \end{bmatrix} \tag{6.26a,b,c}$$

$$\mathbf{A}_d = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & 0 \end{bmatrix}, \quad \mathbf{A}_\omega = \begin{bmatrix} L & 0 & 0 \\ 0 & -L & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{6.26d,e}$$

$$\mathbf{B}' = \begin{bmatrix} \mathbf{I}_2 \\ \mathbf{o}_2^T \end{bmatrix}, \text{ and } \quad \tilde{\mathbf{u}} = \begin{bmatrix} \tilde{v}_{gf} \\ \tilde{v}_{gb} \end{bmatrix} = \begin{bmatrix} \dfrac{\sqrt{N}}{2} v_g e^{-j\varphi_g} \\ \dfrac{\sqrt{N}}{2} v_g e^{+j\varphi_g} \end{bmatrix} \tag{6.26f,g}$$

where $\tilde{\imath}_b$ and $\tilde{\imath}_f$ stand respectively for "backward" and "forward" current phasors, the ofb equivalents of the abc inductor current i_k, and so on for $\tilde{v}_{gb}$ and $\tilde{v}_{gf}$. Although these phasors are complex conjugates, they are both retained to preserve mathematical symmetry.

Note first that the system matrices in the rotating coordinates all have *constant* coefficients under steady-state condition. Therefore, quiescent solutions should also be constant. Constant, *real* v translates into *purely dc* capacitor voltage while constant, *complex* $\tilde{\imath}_b$ signifies *purely sinusoidal* inductor currents. The boost rectifier topology suggested is indeed ideal.

According to Eq. (6.24), the control parameters are d_e', ω_g, v_g, and φ_g. Under steady-state condition, they are dc and symbolized by D_e', Ω_g, V_g, and Φ_g. The derivative in Eq. (6.24) is then zero, and the resulting algebraic equation provides steady-state solutions of the rectifier. Results obtained this way are listed in Table 6.1 for the buck, boost, buck-boost, and flyback rectifiers.

As the phase-controlled rectifier, the buck rectifier has its dc gain dependent on $\cos\Phi_g$. Its dc voltage can thus have both polarities with proper switch implementation. A sinusoidal output is also possible if Φ_g varies linearly with time instead of being a constant as in the rectifier mode

Rectifier	Capacitor Voltage V	Inductor Current $I\,e^{j\Phi_i}$
Buck	$D_m\,V_g\cos\Phi_g$	$\frac{V}{R}$
Boost	$\frac{N}{4}\frac{R}{\Omega_g L}D_m'\,V_g\sin\Phi_g$	$\frac{1}{j\Omega_g L}(V_g e^{j\Phi_g}-\frac{D_m'}{2}V)$
Flyback	$\frac{D_m}{D'}V_g\cos\Phi_g$	$\frac{V}{D'R}$

TABLE 6.1 Steady-state capacitor voltages and inductor currents in the buck, boost, and flyback (or buck-boost) rectifiers.

of operation. This is equivalent to modulation of duty ratio at a frequency different from the line frequency.

Besides Φ_g, the dc gain of the buck converter also depends on the modulation amplitude D_m, a new control parameter not available in the phase-controlled case. Since this control enters *linearly*, it should be preferred to Φ_g in regulation of the output amplitude. The angle Φ_g can then be reserved for *independent* adjustment of the input *power factor*.

As its name implies, the buck topology always steps the input voltage down. Its maximum output for *continuous* sinusoidal modulation is V_g, significantly lower than the $\sqrt{3}\,V_g$ provided by the phase-controlled rectifier. In the next chapter, the "six-stepped PWM" drive is introduced to

improve the peak gain factor from 1 to $\frac{3}{2}$.

The buck-boost and flyback rectifiers possess all the properties mentioned above. In addition, the output duty ratio allows the dc voltage to be stepped above the source by $\frac{1}{D'}$. Since the input and output throws are independent, *linear* control via D_m does not have to be sacrificed in acquisition of *boosting* function via D'.

Note that the dc gains for the three converters just considered are independent of the number of phases. This happens because any change in N is compensated by an inverse variation of the modulation amplitude $\frac{D_m}{N}$.

While the buck, buck-boost, and flyback topologies stand closely together in terms of steady-state performance, the boost rectifier creates its own class. As is displayed in Table 6.1, the dc gain of the boost structure depends on the impedances R and $\Omega_g L$ to reflect the nonzero impedances the *ac* inductor currents insert between the sources and load. It also increases as more supplies power the load because the modulation amplitude does not decrease to offset the higher number of phases.

More interesting is the appearance of $\sin\Phi_g$, instead of $\cos\Phi_g$, in the gain formula. To appreciate this dependence, consider when the duty ratio modulation is in-phase with the source and the output is predicted to be zero. Since the output switches work as an inverter in the backward direction, they apply to the output ends of the inductors a set of sinusoidal voltages in-phase with the sinusoidal source voltages. Consequently, the current in each inductor is *orthogonal* to the respective input voltage.

Therefore, the circuit absorbs no power, and the output ought to be zero. Owing to the sine term, both polarities of output are available with proper switch implementation.

The modulation amplitude D_m' influences the gain even more peculiarly than the phase angle does. It comes in *linearly*, instead of inversely as in the boost dc-to-dc converter. Again, this behavior can be justified at least for the trivial case of $D_m' = 0$ and the output is expected to be zero. When $D_m' = 0$, the output ends of the inductors are *always* shorted together. Since the currents in the inductors add up to zero, no power is delivered to the load, and so the capacitor voltage is forced to zero as predicted. The output voltage does not "blow up" as in the dc-to-dc case to maintain volt-second balance for the inductors because volt-second balance is already provided *totally* by the *ac* input.

When the modulation amplitude is away from zero, the volt-second mechanism is shared simultaneously by both the ac source and the dc capacitor voltage, as is dictated by Eqs. (6.21) and (6.22). It is the contribution of volt-second balance from the ac main that takes away the boost-like behavior of the topology. Therefore, the boost appearance can be retrieved if this contribution is somehow deactivated.

One way to avoid the ac input is to set the impedance $\Omega_g L$ in the circuit to zero. According to Table 6.1, Φ_g also has to be 0° or 180° to avoid an infinite output. Substitution of these values into Eqs. (6.24) through (6.26) then yields

$$V = \pm \frac{V_g}{D_m'/2} \tag{6.27}$$

which is exactly the boosting function expected. The topology thus deserves its name at least when the input is dc ($\Omega_g = 0$) or when the switching frequency is infinite ($L = 0$). Unfortunately, neither of these two conditions is realistic because the line frequency is often nonzero and the switching speed is always finite.

A more practical mean to block the volt-second contribution from the ac main is to *minimize the inductor currents*, which may peak excessively high if the whole line is applied across the small impedance $\Omega_g L$. It is equivalent to selection of Φ_g to make the input power factor unity or input admittance seen by the source real.

The input admittance is the ratio of the inductor current phasor (Table 6.1) to the source voltage phasor:

$$\tilde{Y} = \frac{I e^{j\Phi_i}}{V_g e^{j\Phi_g}} \tag{6.28a}$$

or

$$\tilde{Y} = \frac{1}{j\Omega_g L}\left[1 - \frac{D_e'^2 R}{\Omega_g L}\sin 2\Phi_g + j\,2\frac{D_e'^2 R}{\Omega_g L}\sin^2\Phi_g\right] \tag{6.28b}$$

where

$$D_e'^2 = \frac{N D_m'^2}{16} \tag{6.28c}$$

For $\tilde{Y}$ to be real, Φ_g should be such that

$$\sin 2\Phi_g = \frac{\Omega_g L}{D_e'^2 R} \tag{6.29}$$

Use of $\sin \Phi_g$ provided by this formula under the practical constraint

$$\frac{\Omega_g L}{D_e'^2 R} \ll 1 \tag{6.30}$$

results in the boost dc gain of Eq. (6.27). Therefore, in practical circumstances in which the inductive impedance $\Omega_g L$ is much smaller than the effective load resistance $D_e'^2 R$, the boost rectifier indeed steps the input up with the correct function provided the line angle Φ_g is adjusted to maintain unity input power factor.

To summarize, this section has modeled fast-switching sinusoidal PWM rectifiers and discussed their *steady-state solutions. Describing equation* is used to obtain the dynamic equations of the circuits in the abc reference frame. The results are transformed to the ofb coordinates where the equations are characterized by *constant* coefficients that greatly simplify the analysis.

Steady-state waveforms in all converters have been shown to be ideal, i.e., *dc* output voltages and *sinusoidal* input currents. Gain functions of the buck, buck-boost, and flyback rectifiers depend on cosine of the angle between the supply and duty ratio modulation, just as in the phase-controlled rectifier. In addition, they introduce the *modulation amplitude of the duty ratio* as a new control parameter, which allows *independent* adjustments of the output voltage and *input power factor.*

In general, the boost rectifier does not perform exactly as its dc-to-dc equivalent. Its gain varies linearly with the modulation amplitude and sine of the line angle. If these control parameters are adjusted to maintain unity input power factor, the gain formula of the practical boost topology indeed reduces to the familiar boost function.

6.3 Small-Signal Dynamics

The ofb matrix equation, although it is stationary, is generally nonlinear because it contains products between the controls and state vector (Eq. (6.24)). Hence, dynamic study is restricted to the small-signal sense in which perturbations are sufficiently small so that their responses behave linearly. The derivation of the *perturbed equation* relating these small-signal excitations and outputs is illustrated below for the boost rectifier.

Each control parameter in Eq. (6.24) can be expressed as the sum of a steady-state component and a *perturbed* component, designated by the "caret" (^) symbol:

$$d_e' = D_e' + \hat{d}_e', \quad \omega_g = \Omega_g + \hat{\omega}_g, \text{ and } \tilde{\mathbf{u}} = \tilde{\mathbf{U}} + \hat{\tilde{\mathbf{u}}} \tag{6.31a,b,c}$$

Correspondingly, the state vector can be decomposed as

$$\tilde{\mathbf{x}} = \tilde{\mathbf{X}} + \hat{\tilde{\mathbf{x}}} \tag{6.32}$$

Substitution of these definitions into Eq. (6.24), omission of second-order terms, and Laplace-transformation of the resulting equation then culminate in the following perturbed equation

$$(s\mathbf{P}' - \tilde{\mathbf{A}}_0)\hat{\tilde{\mathbf{x}}}(s) = \mathbf{A}_d\tilde{\mathbf{X}}\hat{d}_e'(s) + \mathbf{A}_\omega\tilde{\mathbf{X}}j\hat{\omega}_g(s) + \mathbf{B}'\hat{\tilde{\mathbf{u}}}(s) \tag{6.33}$$

where

$$\tilde{\mathbf{A}}_o = \mathbf{A}_r + \mathbf{A}_d D_e' + \mathbf{A}_\omega j\Omega_g \tag{6.34}$$

and the other quantities are as specified in Eqs. (6.24) through (6.26).

All control-to-state transfer functions are derivable from Eq. (6.33). These functions, however, are generally unmeasurable because they may be complex. Therefore, a *real* output vector $\hat{\mathbf{y}}$, which includes the real part $\hat{\imath}_r$ and imaginary part $\hat{\imath}_i$ of the current phasor $\hat{\tilde{\imath}}_b$, as well as the capacitor voltage $\hat{v}$, needs be related to the complex state vector $\hat{\tilde{\mathbf{x}}}$ as follows

$$\hat{\mathbf{y}}(s) = \tilde{\mathbf{C}}\hat{\tilde{\mathbf{x}}}(s) \tag{6.35}$$

where

$$\hat{\mathbf{y}}(s) = \begin{bmatrix} \hat{\imath}_r(s) \\ \hat{\imath}_i(s) \\ \hat{v}(s) \end{bmatrix} \quad \text{and} \quad \tilde{\mathbf{C}} = \begin{bmatrix} 1/2 & 1/2 & 0 \\ j/2 & -j/2 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{6.36a,b}$$

The small-signal frequency responses of the preceding outputs all contain the characteristic polynomial or the determinant

$$|s\mathbf{P}' - \tilde{\mathbf{A}}_o| = \frac{\Omega_g{}^2 L^2}{R}\left[1 + (RC + \frac{2D_e'{}^2 R}{\Omega_g{}^2 L})s + \frac{s^2}{\Omega_g{}^2} + \frac{RC}{\Omega_g{}^2}s^3\right] \tag{6.37}$$

in their denominators. This polynomial is real since it represents a realizable circuit. It does not depend on the line angle Φ_g because a short replaces each source in determining the eigenvalues of the topology. It can be factorized approximately into

$$|s\mathbf{P}' - \tilde{\mathbf{A}}_o| \approx \frac{\Omega_g{}^2 L^2}{R}(1 + \frac{s}{\omega_p})\left[1 + \frac{1}{Q}\frac{s}{\omega_o} + (\frac{s}{\omega_o})^2\right] \tag{6.38}$$

where

$$\omega_p = \frac{\Omega_g L}{2D_e'^2 R}\Omega_g, \quad \omega_o = \sqrt{2}\,\frac{D_e'}{\sqrt{LC}}, \text{ and } Q = \frac{2D_e'^2 R}{\omega_o L} \tag{6.39a,b,c}$$

if the two inequalities

$$(\Omega_g L)^2 \ll (2D_e'^2 R)^2 \quad \text{and} \quad \Omega_g^2 \ll \omega_o^2 \tag{6.40a,b}$$

are satisfied.

Both requirements in Eq. (6.40) are realistic. The first one demands that the inductive impedance is sufficiently smaller than the effective load resistance. It is fulfilled easily in high voltage, low current applications that employ boost rectifiers switched at much higher than the source frequency. The second inequality requires that the line frequency is sufficiently below the effective LC corner. It, too, can be satisfied with proper choice of switching frequency, inductance, and capacitance.

The complex pole pair and real pole resulted from the above assumptions are well-separated. The real pole represents the slow mode of response since it is well below Ω_g; the capacitor is effectively open in this lower frequency range. The complex poles portray the fast mode of response because they stay well above Ω_g; the steady-state impedance $\Omega_g L$ is insignificant compared to the dynamic impedance sL in this upper frequency domain.

Out of the many transfer functions, those involving the perturbation of modulation amplitude are encountered more often. Their dc gains and zeros are tabulated in Table 6.2 for reference purpose. Observe that the capacitor voltage possesses a pair of complex rhp zeros; fortunately, the zeros exhibit low Q-factor and stationary position in practical circumstances. The inductors have simpler dynamics, which include a lhp zero at twice the

Function	Dc Gain	Zeros	where
$\frac{\hat{i}_r}{\hat{d}_e'}$	$-\frac{2V}{\Omega_g L}$	$\frac{s}{\Omega_g}(1+\frac{s}{\omega_{z1}})$	$\omega_{z1}=\frac{2}{RC}$
$\frac{\hat{i}_i}{\hat{d}_e'}$	$\frac{2V}{\Omega_g L}$	$(1+\frac{s}{\omega_{z1}})$	$\omega_z=\Omega_g$
$\frac{\hat{v}}{\hat{d}_e'}$	$\frac{V}{D_e'}$	$1-\frac{1}{Q_z}\frac{s}{\omega_z}+(\frac{s}{\omega_z})^2$	$Q_z=\frac{\Omega_g L}{2D_e'^2 R}$

TABLE 6.2 $\hat{d}_e'$-transfer functions of the boost rectifier.

RC corner in both $\hat{i}_r$- and $\hat{i}_i$- responses. Transfer functions associated with $\hat{\omega}_g$ and $\hat{\tilde{\mathbf{u}}}$ also indicate that the inductor currents tend to have minimal phase while the capacitor voltage does not.

Small-signal dynamics of the buck, buck-boost, and flyback rectifiers are similar to those of their corresponding dc-to-dc converters. Thus, the results reviewed in Table A.2 can be modified to describe the frequency responses of these rectifiers. For instance, since the buck rectifier is equivalent to a buck dc converter whose input is $v_g \cos\varphi_g$ and duty ratio d_m, its output responds to the $\hat{d}_m$-excitation with a double-pole roll-off starting at the LC corner. Likewise, since the buck-boost (or flyback) rectifier can be modeled as a boost dc converter whose input is $d_m v_g \cos\varphi_g$

and duty ratio d, its output contains an LC pole pair whose location changes with D'. There is a rhp zero in $\frac{\hat{v}}{\hat{d}}$, and there is no zero in $\frac{\hat{v}}{\hat{d}_m}$ of these topologies.

To recap, this section has detailed the *small-signal analysis technique* and discussed the transfer functions of some ideal fast-switching rectifiers. The key points are the expression of the ac system in terms of *dc* inputs and outputs and the subsequent derivation of the perturbed equations by superposition of small-signal perturbations on dc quiescent values. In contrast to the "quasi-dc" method frequently used in the past, the approach adopted here does not sacrifice any accuracy or impose any assumptions beyond the describing equation step.

Responses of the outputs to small-signal excitations in the source amplitude, transformed duty ratio, and modulation frequency have been calculated. The buck, buck-boost, and flyback rectifiers behave very much like their dc counterparts. The boost rectifier displays third-order poles which may be decomposed into an LC complex pair and an LR real one. Its inductor currents generally exhibit more favorable dynamics than its capacitor voltage. Dynamic poles and zeros of the nonlinear topologies are sensitive to operating conditions.

6.4 Canonical Model

The mathematical description of the canonical model is the *linearized* ofb describing equation, which combines the steady-state and perturbed equations. For the boost example, this combination takes the form

$$(s\mathbf{P}' - \tilde{\mathbf{A}}_0)\tilde{\mathbf{x}}(s) = \mathbf{A}_d\tilde{\mathbf{X}}\hat{d}'_e(s) + \mathbf{A}_\omega\tilde{\mathbf{X}}j\hat{\omega}_g(s) + \mathbf{B}'\tilde{\mathbf{u}}(s) \qquad (6.41)$$

where $\tilde{\mathbf{u}}$ and $\tilde{\mathbf{x}}$ consist of steady-state and perturbed components as defined in Eqs. (6.31) and (6.32), respectively. Steady-state solutions are retrieved by suppression of s and the careted terms; small-signal transfer functions are derived by replacement of $\tilde{\mathbf{x}}$ and $\tilde{\mathbf{u}}$ by $\hat{\tilde{\mathbf{x}}}$ and $\hat{\tilde{\mathbf{u}}}$, respectively. The linearized equation can be manipulated, by the procedure outlined in Section 1.6, into the canonical model for the boost rectifier illustrated in Fig. 6.8.

The model is composed of two complex-conjugate halves, as is evident from the subscripts b and f. In the "backward" half, the polyphase ac source is represented by the independent voltage supply $\tilde{v}_{gb}$. The control parameters are captured in the dependent voltage generator $\tilde{e}'_b\hat{d}'_e + \tilde{\lambda}'_b\hat{\omega}_g$ and dependent current generator $j'\hat{d}'_e$, where

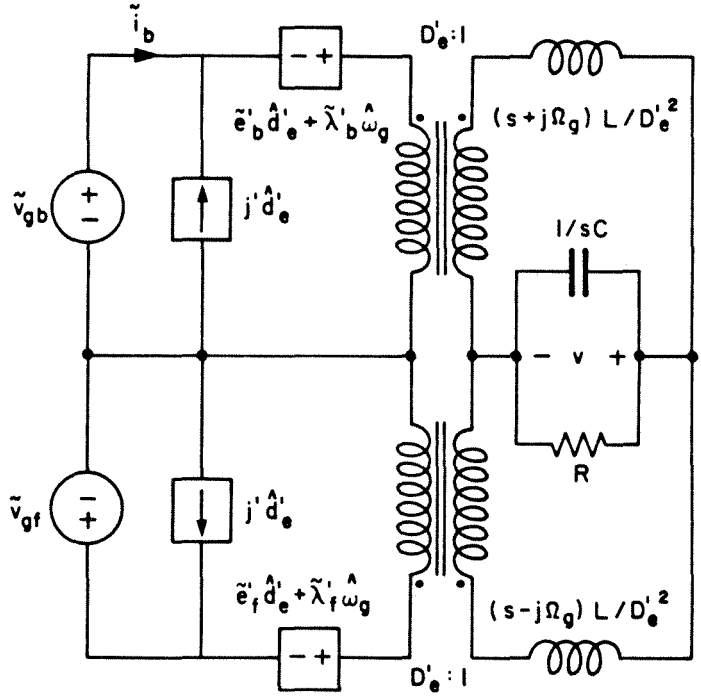


Fig. 6.8 Linearized, continuous, and time-invariant model of the boost rectifier showing excitation and control generators, rectification transformers, and a complex low-pass filter.

$$\tilde{e}_b' = -V\left[1 - \frac{(s+j\Omega_g)L}{2D_e'^2R}\right] \tag{6.42a}$$

$$\tilde{\lambda}_b' = -jL\tilde{I}_b, \quad \text{and} \quad j' = \frac{V}{2D_e'^2R} \tag{6.42b,c}$$

The coefficients of the controlled sources, together with the output filter, determine the zeros of the frequency responses.

After the control and excitation generators comes the ideal transformer whose *rectification ratio* signifies the *dc gain* provided by the modulation amplitude D_e' of the switches. The output of the transformer is next converted into a current via the *complex* inductor, also a part of the low-pass filter. The *real* component of the inductor is responsible for *dynamics* across the filter while the *imaginary* component sets *steady-state* values. Note that since the inductor is in a *reflected* position, its current is *not* the same as the current supplied by the main.

The backward inductor alone can supply only complex current to the load. Therefore, it is paralleled by the forward inductor that furnishes the complex-conjugate current and, hence, helps confining reactive power to the input side of the switches. This parallel orientation thus realizes effectively the *current-rectification* function of the switches.

The common canonical model for the buck, buck-boost, and flyback rectifiers is delineated in Fig. 6.9; the particular one for the buck has $D' = 1$ and $\hat{d}' = 0$. It is straightforward because all rectification takes place right after the input sources. The series connection of $\tilde{v}_{gf}$ and $\tilde{v}_{gb}$ thus portrays the *voltage-rectification* function of the input throws as well as restricts reactive power to the line side of the switches.

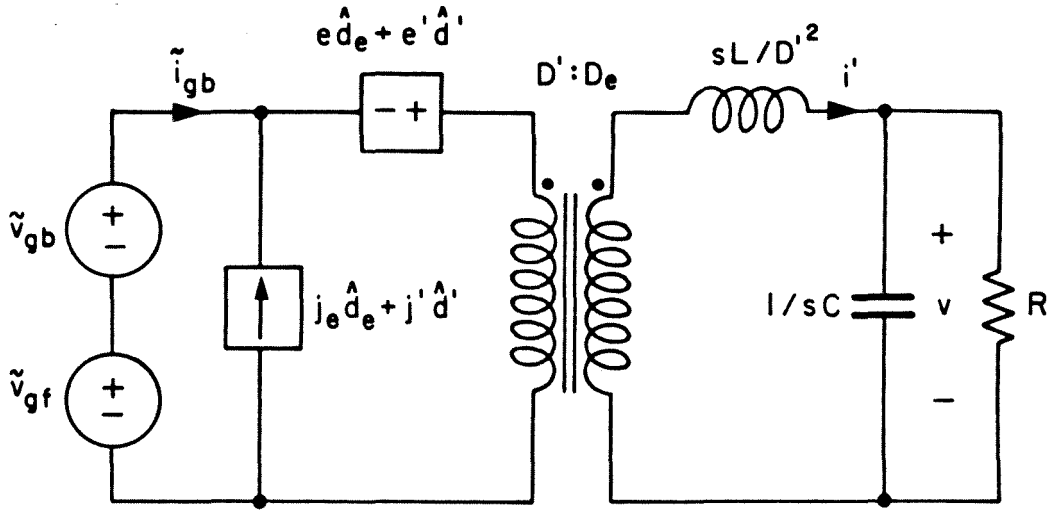


Fig. 6.9 Linearized, continuous, and time-invariant model of the buck, buck-boost, and flyback rectifiers showing excitation and control generators, a rectification transformer, and a low-pass filter.

Because the effective voltage beyond the ac throws is purely dc, there is no need for any complex modeling as in the boost topology. In fact, the controlled generators, rectifying transformer, and LC filter in Fig. 6.9 are similar to those of a buck-boost dc converter. The coefficients of the dependent sources satisfy

$$e = \frac{\tilde{V}_{gb} + \tilde{V}_{gf}}{D_e}, \quad e' = -\frac{V}{D_e}\left(1 - \frac{sL}{D'^2R}\right) \qquad (6.43a,b)$$

$$j_e = -I, \quad \text{and} \quad j' = \frac{D_e}{D'} I \qquad (6.43c,d)$$

The *transformed duty ratio* d_e contained in the rectification ratio of the

ideal transformer is related to the d_m in Eq. (6.5) by

$$d_s = \frac{d_m}{\sqrt{N}} \tag{6.44}$$

The current i' flowing in the inductor of the model is defined according to

$$i' = D'i + I\hat{d}' \tag{6.45}$$

In conclusion, this chapter has described the *buck*, *boost*, *buck-boost*, and *flyback rectifiers* and studied their performances. They are switched above two decades of the input frequency and pulse-width-modulated by only *sinusoidal* functions. Balanced polyphase circuits with number of phases ranging from two to infinity have been presented.

After the specifications, *state-space describing equations* have been obtained. Equations of the buck, buck-boost, and flyback rectifiers are solved directly in the abc reference frame because they are dc. Their *steady-state results* resemble those of the corresponding dc converters although they have new control variables, such as the *amplitude of duty ratio modulation* and the *angle between phase voltage and duty ratio modulation*. The equation of the boost rectifier is first transformed to the ofb coordinates so that it, too, has *constant* coefficients. The analysis there shows that this circuit behaves as its dc kin in practical environments if its input power factor is maintained at unity. Steady-state results confirm that all topologies have *dc* output voltages and *sinusoidal* input currents.

The time-invariant equations of the rectifiers have been perturbed to derive *small-signal transfer functions*. Excitations include the perturbations of input voltage, modulation amplitude and frequency of ac duty ratios, and dc duty ratio. Responses of the buck-type topologies are,

again, repetitions of those of their dc-to-dc equivalents. The inductor currents in the boost rectifier prove to be easier to regulate than the output voltage. Small-signal bandwidths of all transfer functions are *broad* owing to fast switching frequency and can be predicted with a high degree of accuracy below half the switching frequency.

Finally, steady-state and dynamic descriptions are consolidated in the *linearized, time-invariant, and continuous canonical model.* The model consists of voltage and current generators representing the sources and duty ratio controls; an ideal transformer specifying the *rectification ratio*; and a low-pass filter affecting the overall dynamics. *Voltage rectification* in the buck, buck-boost, and flyback circuits is modeled by *series* connection of the sources whose voltages are rectified. *Current rectification* in the boost rectifier is reduced to *parallel* connection of the inductors whose currents are rectified.

CHAPTER 7

PRACTICAL ASPECTS OF FAST-SWITCHING SINUSOIDAL PWM RECTIFIERS

This chapter deals with practical aspects of the fast-switching rectifiers described in Section 6.1. It is divided into three sections. The first section realizes the switches in three-phase topologies using the steady-state results developed earlier. The second section introduces high-frequency *isolation* into the basic converters and other derived topologies. The last section evaluates the performance of rectifiers operated as *fast-switching impedance converters*.

7.1 Three-Phase Implementation

This section discusses three different issues. The first one concerns the connection of transistors and diodes and the stress on these devices in practical rectifiers. The second involves the selection of drive strategies that optimize both the output voltage and size of circuit elements. The last one suggests some modifications that allow the original rectifiers to accept the backward flow of power.

7.1.1 Switch Realization and Stress

The implementation of ideal rectifier circuits centers around the switches. These switches ought to be built from fast semiconductor devices, presently the bipolar and field-effect transistors. In the following examples, the bipolar transistor is used just for convenience although the field-effect

device is much more preferred in terms of drive, ruggedness, and speed.

The input throws in the buck (Fig. 6.1), buck-boost (Fig. 6.5), and flyback (Fig. 6.6) rectifiers all carry *dc* current from the inductor and block *ac* voltage from the main. They are thus *two-quadrant-in-voltage* and are realized by cascade connection of a transistor and a diode. The transistor withstands the positive off-voltage, and the diode absorbs the negative excursion. Figure 7.1 illustrates how this is done for a buck-boost rectifier. Note that this switch realization eliminates "shoot-through faults," i.e., any number of input throws at any positions may be activated simultaneously without detrimental outcomes. In fact, both switches must be on all the time to guarantee a path for the inductor current.

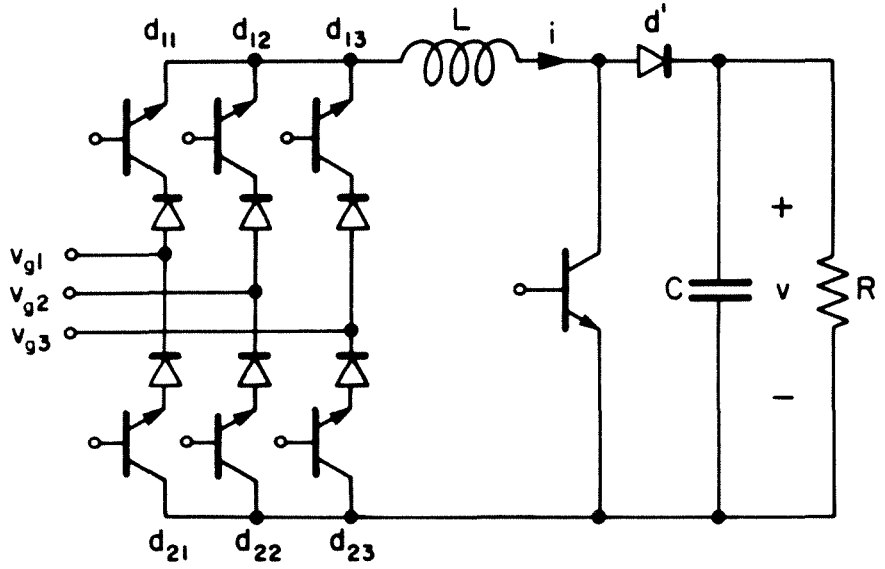


Fig. 7.1 Three-phase buck-boost rectifier with each voltage-two-quadrant throw implemented by a transistor and a diode in series.

The output throw in the flyback topology is topologically related to the input ones and, hence, is constructed in a similar manner. The output switch in the buck-boost case, on the other hand, is topologically independent from the input ones and is decoupled from the ac line by the inductor. It has to block only the dc capacitor voltage and is constructed as indicated in Fig. 7.1.

Switches in the boost rectifier carry *ac* currents and block *dc* voltage. Therefore, they are *two-quadrant-in-current* and can be implemented by anti-paralleling a transistor and a diode. Figure 7.2 shows a practical boost circuit with semiconductor switches. Note that "dead time" must be inserted between the falling edge of one throw and rising edge of the other (of the same switch) to insure that the transistors do not destroy themselves by shorting out the output capacitor.

Current stresses for the devices are the peak steady-state inductor currents, tabulated in Table 6.1, with adequate allowance for current ripple. Voltage stresses are either the line voltage, the output voltage, or a combination of both, as are listed in Table 7.1 for the four topologies under investigation. Note that although the off-voltage across the output transistor of the flyback rectifier appears very low if V is comparable to $\sqrt{3}V_g$, rating specification should take into account the fact that V has to start from zero when the circuit is first turned on.

In summary, this subsection has shown that switches in all rectifiers are two-quadrant in either voltage or current and can be realized by either anti-parallel or series connection of a transistor and a diode. Peak currents through these devices are determined primarily by inductor currents. Voltage stresses across them depend on line and output voltages

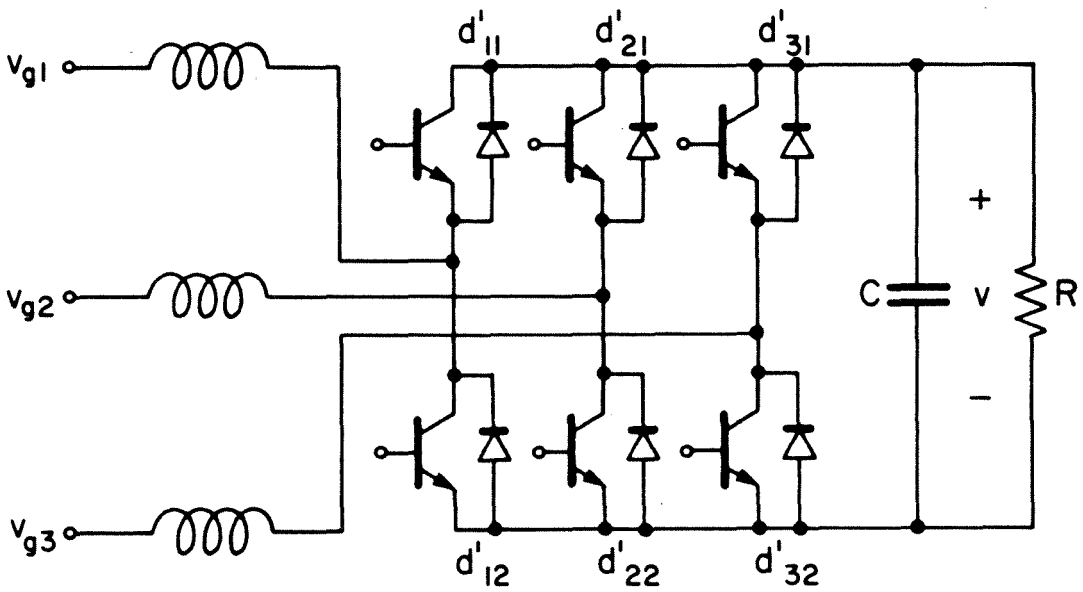


Fig. 7.2 Three-phase boost rectifier with each current-two-quadrant throw implemented by a transistor and a diode in antiparallel.

and are summarized in Table 7.1.

7.1.2 Modulation Strategies

According to the describing equation modeling technique presented in the first chapter, first-order performance of fast-switching rectifiers depends on only the *duty ratios* of the switches. Since any given duty ratio may correspond to an infinite number of *switching functions*, a variety of drive schemes exist for any given set of duty ratios. Out of these schemes, however, only some are "optimal" in the sense that they maximize the transformed duty ratio and, hence, minimize the size of circuit elements. *Continuous* and *six-stepped (sinusoidal) PWM's* are reconsidered below as

Rectifier	Input		Output	
	Transistor	Diode	Transistor	Diode
Buck	$\sqrt{3}\,V_g$	$\sqrt{3}\,V_g$		
Boost			V	V
Buck-boost	$\sqrt{3}\,V_g$	$\sqrt{3}\,V_g$	V	V
Flyback	$\sqrt{3}\,V_g$	$\sqrt{3}\,V_g$	$\max\,(\sqrt{3}\,V_g - V,\, 0)$	$\sqrt{3}\,V_g + V$

TABLE 7.1 Voltage stresses across the transistors and diodes of the buck, boost, buck-boost, and flyback rectifiers.

examples of efficient drive policies.

Consider first the buck-boost topology shown in Fig. 7.1, which is also representative of the buck and flyback rectifiers. *Continuous PWM* for the input throws employs a switching function diagram analogous to that plotted in Fig. 4.11 for the three-phase boost inverter. According to Table 6.1, the highest output voltage is then V_g obtained when the duty ratio functions are

$$d_{1k} = \frac{1}{3} + \frac{d_m}{3} \cos[\ \theta - (k-1)\frac{2\pi}{3}\ ] \tag{7.1a}$$

and

$$d_{2k} = \frac{1}{3} - \frac{d_m}{3} \cos[\ \theta - (k-1)\frac{2\pi}{3}\ ]\ , \qquad (1 \le k \le 3) \tag{7.1b}$$

A better result can be attained by employment of *six-stepped PWM* whose switching function diagram is similar to that delineated in Fig. 4.13 for the boost inverter. The transformed duty ratio of this more efficient modulation strategy can be proved to be $\frac{3}{2}$ times higher than that offered by continuous PWM. The corresponding peak output voltage is $\frac{3}{2} V_g$, which compares very favorably with the $\sqrt{3} V_g$ provided by the familiar phase-controlled rectifier.

Continuous and six-stepped PWM can also be extended to the boost rectifier. The continuous function

$$d'_{k1} = \frac{1}{2} + \frac{d'_m}{2} \cos[\ \theta - (k-1)\frac{2\pi}{3}\ ]\ , \qquad (1 \le k \le 3) \tag{7.2}$$

allows a maximum modulation amplitude of $\frac{1}{2}$. The six-stepped PWM of

Fig. 4.14 for the buck inverter can be adapted to the boost rectifier to bring the peak modulation amplitude up to $\frac{1}{\sqrt{3}}$.

To summarize, many flexible drive policies are available for fast-switching rectifiers, some of which are superior to the others. Examples considered in this subsection are *continuous* and *six-stepped PWM's*, which both generate a purely dc output voltage and sinusoidal input currents. Six-stepped PWM, although it requires slightly more complicated circuitry, offers higher transformed duty ratio than continuous PWM does.

7.1.3 Bidirectionality of Power Flow

Many kinds of "load" return power back to the source during the course of operation. This reversal of power flow requires a change in polarity of either voltage or current at the input and output ports. The change can be executed electronically if the port is already conditioned for four-quadrant operation, as is the input of the buck rectifier. However, it may necessitate additional switches if the terminal can operate in only one- or two-quadrant mode, as can the output of the buck-boost rectifier. Thus, the output switch in Fig. 7.1 ought to be voltage-two-quadrant if the load voltage is anticipated to swing negatively; an analogous caution applies to the output of Fig. 7.2.

Consider first the buck-boost topology of Fig. 7.1, which can be used to understand the buck and flyback rectifiers as well. For this structure, minimal alteration is guaranteed when the inductor current is maintained in the *same* direction regardless of mode of operation. Energy is then delivered from the load whenever the output voltage flips sign. Volt-second

balance for the inductor requires that the phase of input modulations is advanced by 180°. Consequently, input currents flow backward so that the sources accept power from the load. If the sources are stiff, the modulation amplitude needs to be properly adjusted, probably by a feedback loop, to ensure zero average voltage across the inductor.

If the load is a battery that cannot reverse its polarity during the discharging mode, it has to be enclosed in a bridge, as is drawn in Fig. 7.3. During $d'T_s$, either of the output transistors can be on. During dT_s, both of them are either on to discharge the battery or off so that the diodes can charge the battery. With the bridge installed, a negative voltage is applied to the output end of the inductor for reversal of power flow; therefore, the remaining adjustments are the same as those specified in the preceding paragraph.

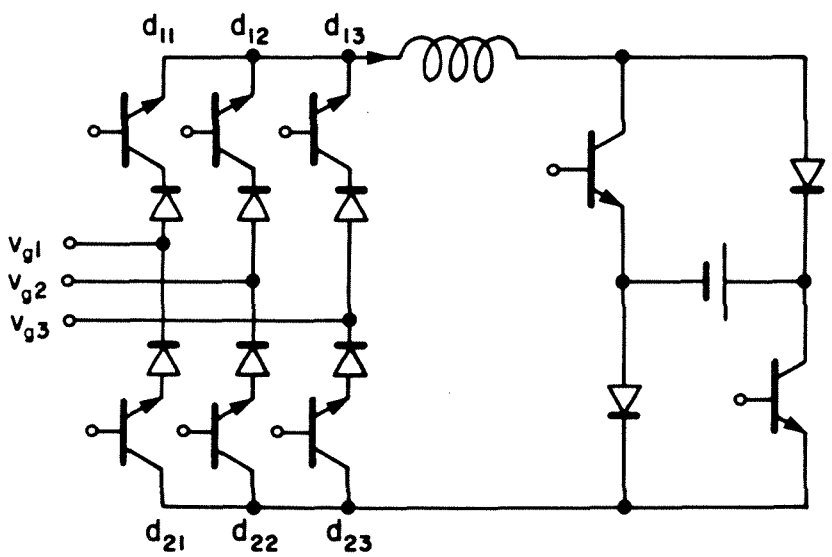


Fig. 7.3 Bidirectional buck-boost rectifier.

If the boost rectifier replaces the buck-boost circuit to discharge the above battery, no bridge is required since the direction of the average current into the load can be controlled electronically. The modulation phase should be preserved, and only the modulation amplitude is varied such that the inverted battery voltage is strong enough to push currents back into the sources. If the load voltage goes negative, the bridge should be inserted back to avoid application of this negative potential to the throws of the original topology.

To recast, the reversal of power flow necessitates a change in polarity of either voltage or current at the input and output ports. This change requires switch modification and electronic adjustment of the modulation amplitude and phase.

7.2 Isolation

One advantage of fast switching is the ease of *isolation*, which requires transformers whose size diminishes with switching frequency. This section examines how isolation may be incorporated in some of the rectifiers proposed earlier in Chapter 6, especially the flyback and isolable boost-buck rectifiers.

The flyback topology is inherently isolable because the energy storage inductor stays at either the input or output side within each switching cycle. Isolation can thus be implemented by splitting the inductor winding into two coupled windings sharing a common magnetic path, as is pictured in Fig. 7.4. Note that the output throw d' actually belongs to the upper switch although it is physically attached to the secondary, instead of primary, winding of the inductor.

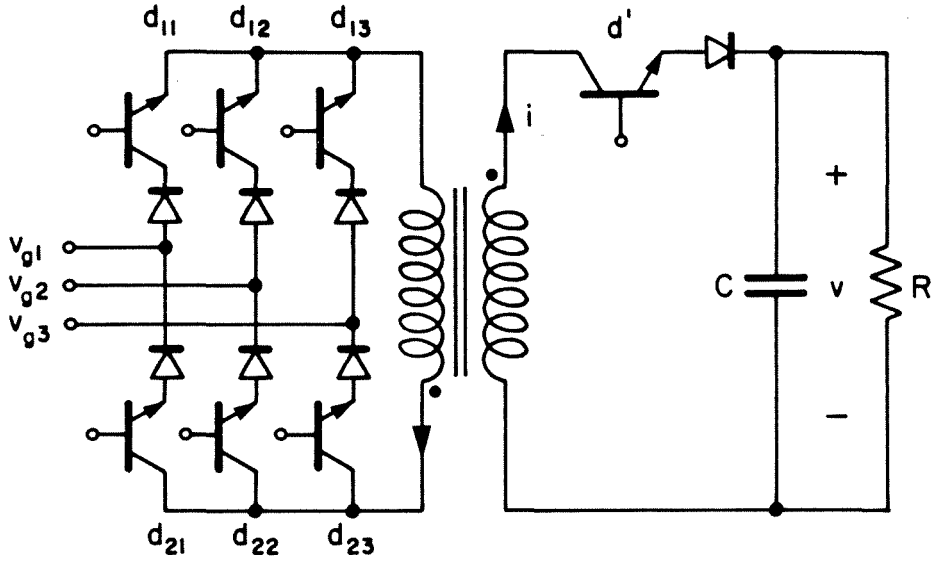


Fig. 7.4 Isolated flyback rectifier.

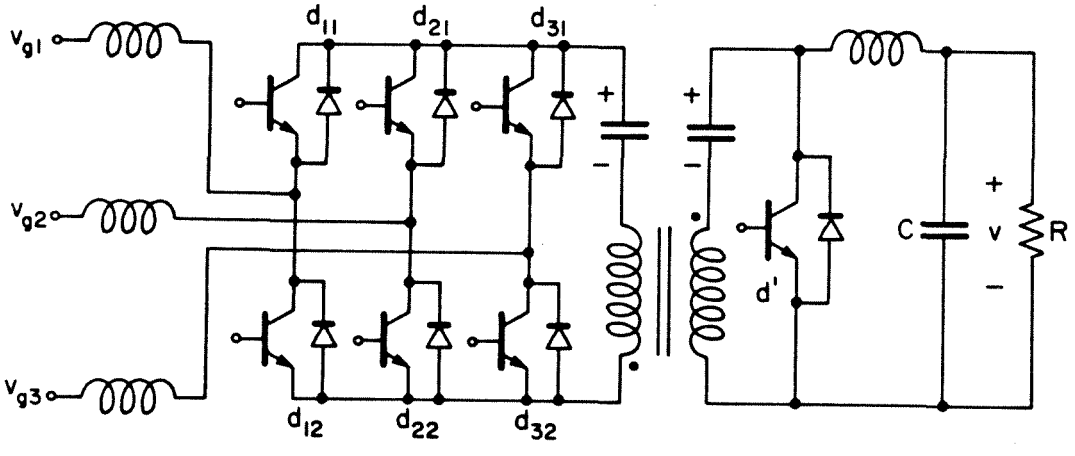


Fig. 7.5 Boost-buck rectifier, cascade of a boost rectifier and a buck dc converter, with isolation as in the Ćuk dc converter.

Another rectifier that is inherently isolable is the isolated boost-buck of Fig. 7.5. As in the flyback circuit, each switching period is decomposed into a charging interval dT_s and a discharging interval $d'T_s$. During dT_s, all six input transistors are on and the output transistor is off so that the input inductors absorb energy from the source while the two intermediate capacitors, effectively in series, supply the load through the output LC filter. Then during $d'T_s$, the output transistor is activated and the input switches recharge the capacitors, again in series, according to the duty ratio functions

$$d_{k1} = \frac{d'}{2} + \frac{d_m}{2} \cos\left[\theta - (k-1)\frac{2\pi}{3}\right], \quad (1 \le k \le 3) \tag{7.3}$$

Under steady-state condition, the capacitors sustain only dc voltages. They also prevent any dc flux from flowing through the isolation transformer.

Although the buck and buck-boost rectifiers are not inherently isolable, isolation can still be incorporated by extension of the techniques used in the push-pull and full-bridge dc-to-dc converters. It is recommended that the transformer be inserted between the input switches and the inductor and that six-stepped PWM be used to minimize the number of extra switches.

In review, fast switching reduces the size of magnetic components and allows isolation transformers to be built in the rectifiers more freely. Some circuits, such as the flyback and isolable boost-buck topologies, can readily accept an isolation transformer without demanding any more semiconductor devices. Some others, such as the push-pull and full-bridge rectifiers, do need additional switches besides the isolation transformer.

7.3 Fast-Switching Impedance Converters

Concerns about poor, usually inductive, power factors created by many industrial loads have led to a variety of schemes to supply reactive power to the main [31]. In the early days, synchronous condensers, capacitors, and inductors have been paralleled with the load so that the overall phase angle looks more presentable to the line. Switched-mode circuits, such as the phase-controlled rectifier and the six-pulsed cycloconverter, have then been used in conjunction with reactive components to build "VAR (volt-ampere reactive) generators," which furnish part of the reactive power for utility companies.

The VAR generators, however, face many drawbacks of slow switching mentioned before. For instance, their energy-storage elements are bulky and expensive and impede their response speed. They introduce the harmonic problem while correcting the power factor one. Their control is very limited because the only control parameter is the firing angle of the switches. Therefore, they hardly qualify as *impedance converters* that synthesize impedances whose amplitude and phase can be adjusted *independently*.

This section shows that the fast-switching rectifiers encountered earlier are perfect candidates for impedance conversion without the aforementioned problems. Once the general impedance conversion function is realized, application of the topologies as power-factor controllers is straightforward.

The *input impedance* $\tilde{Z}_i$ of a rectifier is defined as the ratio of the input phase voltage phasor to the input phase current phasor, which may be evaluated in either stationary or rotating reference frame:

$$\tilde{Z}_i = \frac{\tilde{V}_{gb}}{\tilde{I}_{gb}} \tag{7.4}$$

Its value for the buck-boost and flyback rectifiers can be determined from either the canonical model (Fig. 6.9) or steady-state formulas (Table 6.1):

$$\tilde{Z}_i = \frac{N}{2} \frac{D'^2}{D_m^2} \frac{e^{j\Phi_g}}{\cos\Phi_g} R \tag{7.5}$$

The circuit thus converts a real resistance R into a *polyphase impedance* $\tilde{Z}_i$ whose phase is first set by Φ_g and amplitude is then adjusted independently via D', D_m, and R. Since the synthesized phase and amplitude can take on *any* values, the conversion function is perfect.

Unity power factor operation is achieved when Φ_g is set to zero. A "switched-mode capacitor (or inductor)" is simulated by operation with Φ_g in the vicinity of $-90°$ (or $90°$) and shorting out the load. Note that even when a straight wire is placed across the output of the rectifier, a small amount of power still needs be delivered to overcome parasitic losses. This is why Φ_g has to deviate slightly from $\pm 90°$ and the power factor cannot be precisely zero.

For the boost rectifier, the input impedance becomes

$$\tilde{Z}_i = \frac{j\Omega_g L}{1 - \frac{N}{8} \frac{R}{\Omega_g L} D_m'^2 e^{-j\Phi_g} \sin\Phi_g} \tag{7.6}$$

A comparison of Eqs. (7.6) and (7.5) reveals that the boost topology allows less control flexibility for $\tilde{Z}_i$ than the buck-boost or flyback circuit does. For instance, the phase of Eq. (7.6) is a function of not only Φ_g, but also all other parameters. If R is fixed, there is no way that D_m' and Φ_g can produce all desired amplitudes; therefore, the load must be controlled in conjunction with the switches to achieve the full range of amplitude.

For fixed D_m' and R, the qualitative change of power factor as a function of Φ_g is as depicted in Fig. 7.6. There are four values of Φ_g at which the power factor is unity; they satisfy:

$$\sin 2\Phi_g = \frac{16}{N D_m'^2} \frac{\Omega_g L}{R} \tag{7.7}$$

They are the boundaries between alternate regions of leading and lagging power factors on the trigonometric plane. The capacitive areas can be enlarged by reducing the right-hand side of Eq. (7.7) toward zero.

By selection of sufficiently small Φ_g and large R, it is possible to approximate the denominator of Eq. (7.6) to a positive or negative ***real*** number. The positive case corresponds to a highly inductive $\tilde{Z}_i$, and the negative one a highly capacitive $\tilde{Z}_i$. Therefore, the configuration is capable of delivering a large amount of reactive power comfortably. The power factor can be adjusted very close to zero by bringing Φ_g toward zero and R toward infinity. A precisely zero power factor is difficult to achieve because of finite parasitic losses in the circuit.

In general , almost any complex values may be assigned to the denominator of Eq. (7.6) by proper selection of R, D_m', and Φ_g. Hence, the impedance converted by the boost rectifier should cover a wide enough range

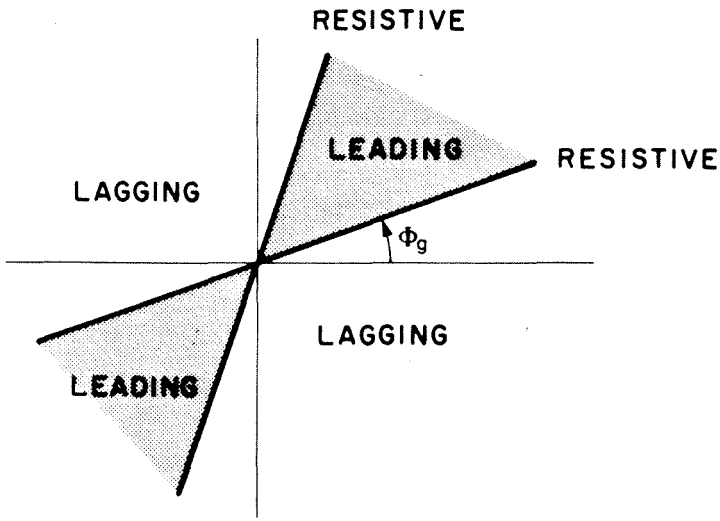


Fig. 7.6 Regions of leading, unity, and lagging power factors of the boost impedance converter.

of amplitude and phase for most applications.

In conclusion, the ideal rectifier topologies introduced in Chapter 6 are realizable and have many useful features. Each throw in these circuits can be implemented by either series or anti-parallel connection of a transistor and a diode, depending on whether it is two-quadrant in voltage or current, respectively. Switches can be modulated sinusoidally by a variety of ways, the best one being the *six-stepped PWM*, which offers maximum effective duty ratio while preserving ideal waveforms at all points in the circuit. The modulation strategy can be modified to reverse direction of power flow electronically.

Fast switching allows *isolation* to be incorporated with ease in most rectifiers. Examples have been given for the flyback and isolable boost-buck topologies, which accept an isolation transformer naturally. The full-bridge and push-pull structures, the isolated versions of the buck rectifier, are straightforward extensions of the respective full-bridge and push-pull buck dc-to-dc converters.

Any of the fast-switching rectifiers can be used as a *switched-mode impedance converter*, which transforms a dc load at the output into a polyphase impedance at the input. Discussions have been centered around the buck-boost topology, which can synthesize an impedance of any amplitude and phase, and boost topology, which exhibits a very broad range of impedance values. These circuits inherit all merits of fast switching, namely, small reactive elements, ideal waveforms, quick responses, flexible controls, and so on.

PART III

SWITCHED-MODE CYCLOCONVERSION

CHAPTER 8

REVIEW OF EXISTING CYCLOCONVERTERS

A *cycloconverter* converts N (>1) balanced sinusoids of one amplitude and frequency into M (>1) balanced sinusoids of another amplitude and frequency; the numbers of phases at the input and output can differ, and so can the phase sequences. Cycloconverters are found in such applications as motor drive, in which variable voltage and frequency are to be produced from constant line condition, or variable-speed, constant-frequency generator, in which a fixed frequency for the supply bus is to be derived from an unsteady shaft speed.

Cycloconverters can be divided into slow- and fast-switching groups according to the ratio of switching to input or output frequency. *Slow-switching* cycloconverters switch at a frequency comparable to input or output frequency; they are reviewed in the first section. *Fast-switching* cycloconverters operate at two decades above the input or output frequency; they are examined in the last section.

8.1 Cycloconverters Switched at Low Frequency

This section is composed of two parts. The first one discusses the *phase-controlled cycloconverter*, a direct extension of the phase-controlled rectifier into polyphase application. The second one focuses on the *unrestricted frequency changer (UFC)*, which involves regular sampling,

instead of phase-control, of input voltages.

8.1.1 Phase-Controlled Cycloconverter

Integration of three *dual converters* illustrated in Fig. 5.3 results in the *six-pulse (phase-controlled) cycloconverter* [24] of Fig. 8.1. The circuit thus consists of six triple-throw switches whose realization by thyristors is exemplified for the second phase. Note that although each pair of anti-parallel "positive" (darkened) and "negative" (not darkened) thyristors appears as a four-quadrant throw, it actually works as *two voltage-two-quadrant throws* since the converter is under the circulating current-free mode of operation. Only one of the back-to-back devices is activated at any time, depending on the polarity of load current.

Since each phase is to synthesize an *ac* waveform, the firing angle is modulated such that the low-frequency component of the output has the desired amplitude and phase. One of the most elementary firing laws has been the *cosinusoidal control* that involves natural sampling of a sinusoidal reference by a carrier comprising cosinusoidal segments at the input frequency; firing instants thus coincide with the intersections of reference and carrier signals. The resulting waveform resembles that sketched in Fig. 8.2 for v_1 of Fig. 8.1. In this waveform, the amplitude of the component at the reference frequency is directly proportional to the reference amplitude.

The piecewise synthesized output of Fig. 8.2 is inevitably rich in harmonics. Both sub- and super-harmonics exist, and these are not necessary at multiples of input or output frequency or some common periodicity thereof (if there is one) - "Fourier series" simply does not apply

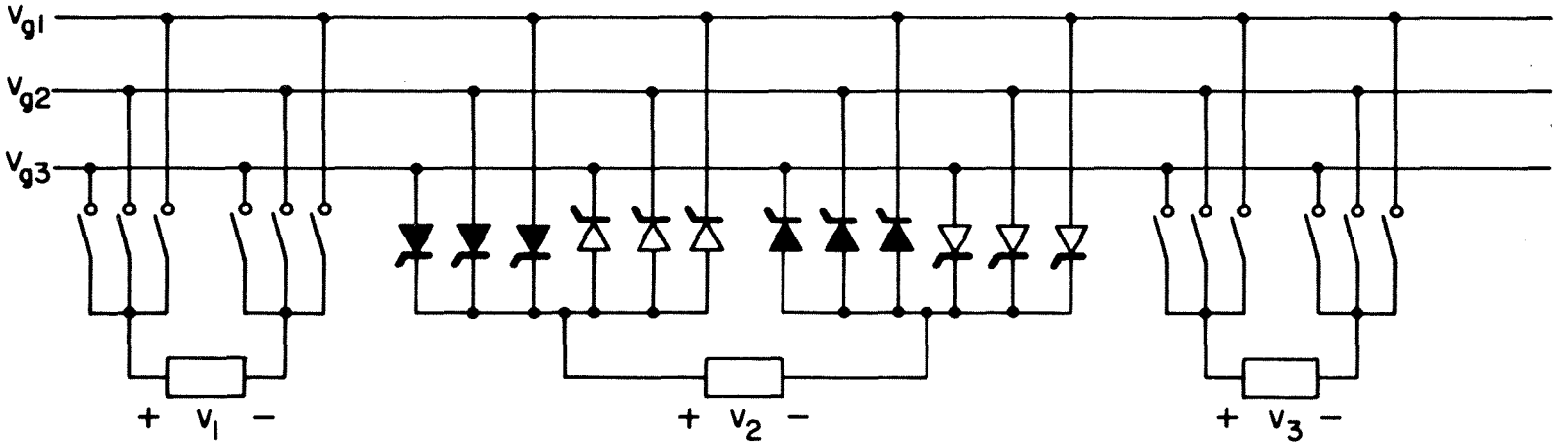


Fig. 8.1 Six-pulse cycloconverter (circulating current-free mode).

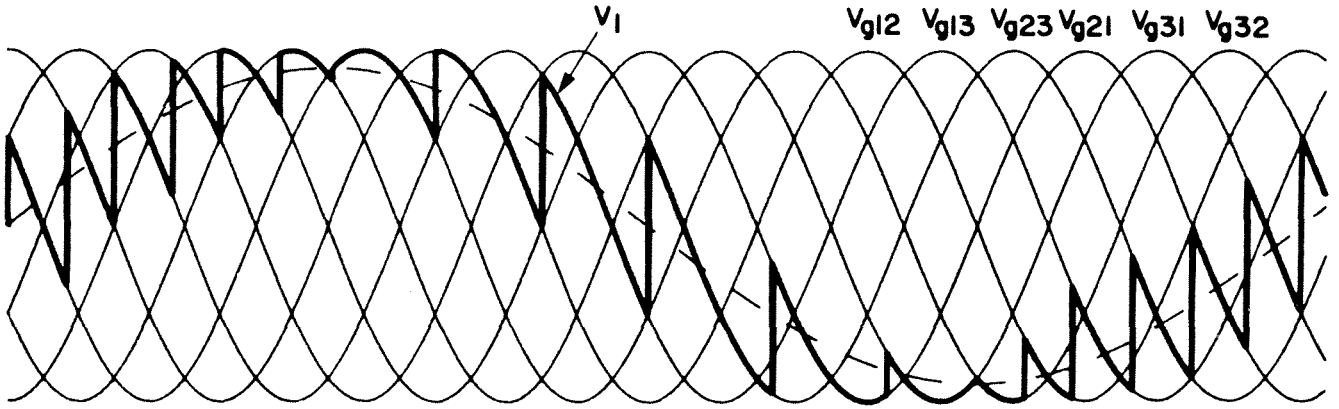


Fig. 8.2 Output (thick) voltage of a six-pulse cycloconverter in relation to input (thin) line voltages.

here. The harmonic figure deteriorates quickly at high modulation frequency, and this degradation limits the useful output frequency below two-thirds of the input frequency.

Input currents also suffer from the harmonic problem. Current harmonics arise from voltage harmonics and phase-control itself. Even a large filter is not very effective in attenuation of harmonics since they are so close to the fundamental component and their pattern varies with operating condition.

Besides the harmonics, beat power and poor input power factor are some other concerns. The beating effect is eminent whenever input and output frequencies are not synchronized. The input power factor is generally lagging because of phase-control and cannot be controlled arbitrarily because that freedom is reserved for adjustment of voltage amplitude.

In addition to the six-pulse cycloconverter, a variety of similar topologies with different pulse numbers are also described in [24] and [25]. All of these share the same *buck-type* configuration and differ in the number of switches, which may be as small as three or as large as twelve. As another example, consider the *three-pulse cycloconverter* in Fig. 8.3 whose switches are as realized in Fig. 8.1. This converter does not require isolated load as the six-pulse one. Because of the reduced number of switches, however, its maximum voltage gain is only $\frac{3\sqrt{3}}{2\pi}$, half of that of the six-pulse cycloconverter.

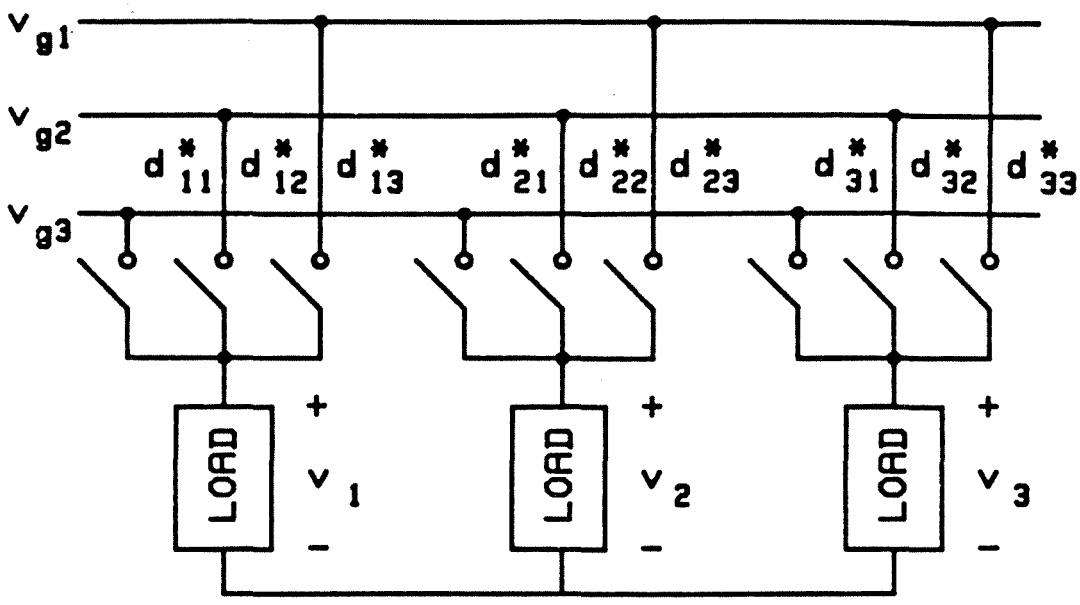


Fig. 8.3 Three-pulse cycloconverter (circulating current-free mode).

8.1.2 Unrestricted Frequency Changer

The *unrestricted frequency ranger (UFC)* uses the *same buck-type topology* as the phase-controlled cycloconverter; examples of UFC thus include the six-pulse circuit in Fig. 8.1, the three-pulse one in Fig. 8.3, and so on [33]. The operating principle of the switches, however, is no longer phase-control, in which the firing angle is modulated at the output frequency. Instead, the switching frequency f_s is related to the input frequency f_g and output frequency f according to

$$f = f_g \pm f_s = f_g \pm \frac{f_c}{P} \tag{8.1}$$

where f_c is the clock frequency, and P is the pulse number. For the six-pulse converter in Fig. 8.1, each switching period is divided into $P = 6$ *equal* clock intervals corresponding to six combinations of line voltages. The arrival of each clock pulse turns off one throw and initiates another, the pair of commutated throws being permutated by six-stepped symmetry. This switching sequence applies all six polarities of line voltage to the load, as can be seen from Fig. 8.4 for the first phase of a six-pulse UFC.

Owing to Eq. (8.1), the output frequency of an UFC can be any value and is not restricted below some small fraction of line frequency as in the phase-controlled cycloconverter. The output phase sequence can be reversed by choice of f_s such that $f_s < f_g$. Reactive power can be inverted, i.e., an inductive load appears capacitive to the source, and vice versa, if $f_s > f_g$.

Although a UFC provides more freedom to control the output frequency than a phase-controlled rectifier does, it lacks a mechanism to vary the output amplitude, at least in the six-pulse case. Its harmonic content, better than that of the phase-controlled rectifier, is still not satisfactory because of the low-frequency steps in Fig. 8.4. Sub- and super-harmonics in its output voltages and input currents are difficult to filter effectively since the switching frequency specified in Eq. (8.1) is still too close to the source or load frequency.

In summary, slow-switching cycloconverters generally employ the buck-type, voltage-fed topology; their number of switches is selected to improve the voltage amplitude or reduce the switching noise. Two different

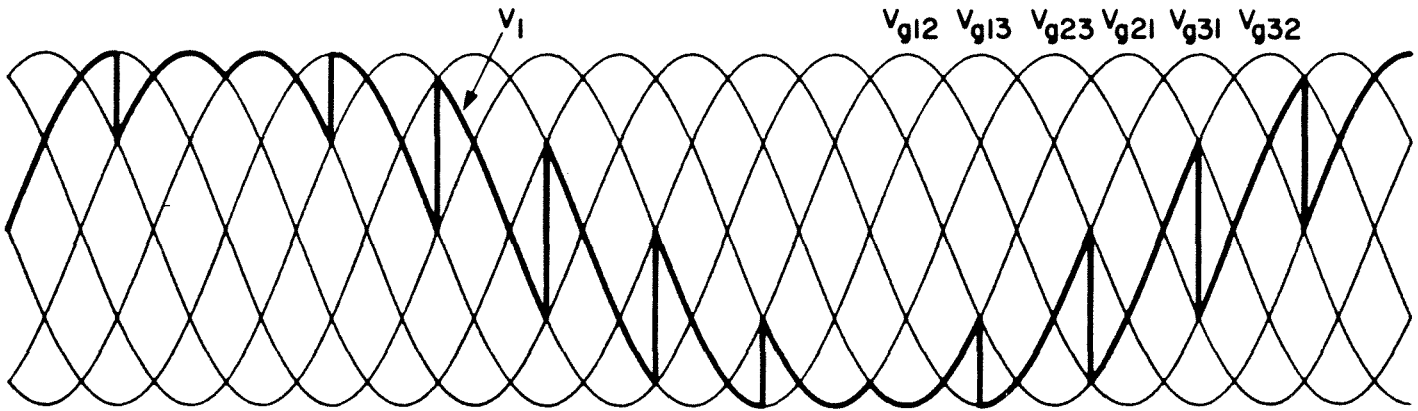


Fig. 8.4 Output (thick) voltage of an unrestricted frequency changer in relation to input (thin) line voltages.

switching strategies have been discussed. In the *phase-controlled cycloconverter*, the firing angle is *modulated at the output frequency* to synthesize a stepped voltage whose desired component is proportional to the reference signal. In the *unrestricted frequency changer*, switches commutate at the sum or difference of line and load frequencies; on-times of all throws are *equal* and *constant* throughout every switching cycle.

8.2 Cycloconverters Switched at High Frequency

Two classes of fast-switching cycloconverters are studied in this section. The *high-frequency-synthesis cycloconverter* is considered first as an example of ac-to-ac energy processing by PWM principle. The *resonant cycloconverter* is considered next as an example of frequency conversion by resonant principle.

8.2.1 High-Frequency-Synthesis Cycloconverter

The *high-frequency-synthesis cycloconverter (HFSC)* [37] is topologically *identical* to the three-pulse converter illustrated in Fig. 8.3. Its throws, however, are switched at high frequency and controlled by the following PWM functions:

$$d_{11} = d_{23} = d_{32} = \frac{1}{3} + \frac{D_m}{3}\cos\Omega t \tag{8.2a}$$

$$d_{12} = d_{21} = d_{33} = \frac{1}{3} + \frac{D_m}{3}\cos(\Omega t - \frac{2\pi}{3}) \tag{8.2b}$$

$$d_{13} = d_{22} = d_{31} = \frac{1}{3} + \frac{D_m}{3}\cos(\Omega t + \frac{2\pi}{3}) \tag{8.2c}$$

Phase voltages after the switches then consist of sinusoidal components

superimposed by high-frequency harmonics. The amplitude and frequency of the desired sinusoids are controlled via the amplitude and frequency of the duty ratio modulations in Eq. (8.2). Switching noise is absorbed at low-pass LC filters inserted between the switches and load.

The useful output of a high-frequency-synthesis cycloconverter is at either the sum or difference of input and modulation frequencies. A wide cycloconversion range is thus available, the upper limit being imposed by the switching frequency and amount of ripples tolerated. Fast-switching PWM also permits the phase sequence at the input to be reversed, and the power factor inverted, from those at the output by proper sizing of line and modulation frequencies.

In spite of the above advantages, the high-frequency-synthesis cycloconverter has several drawbacks. Its maximum voltage gain is only $\frac{1}{2}$, and this low value necessitates some modification of the basic topology if the circuit is to drive a variable-speed motor from the main. Its switches are four-quadrant and, hence, difficult to drive: overlapping must be avoided to prevent shorting out the line, but no dead time is allowed because of the absence of free-wheeling diodes. With the drive functions defined in Eq. (8.2), power factor control is impossible as the input power factor is fixed for a given load. In [37], two modulation frequencies symmetrical about the main frequency are injected into the duty ratios to create some correction of power factor. This complicated algorithm, however, still restricts the angle of the impedance seen by the source to be always smaller than the load impedance; if the load is highly resistive, the opportunity to redistribute reactive power is lost.

Reactive elements have been assigned only secondary importance in [37] and ignored in the modeling process. As is proved in next chapter, this neglect of L and C is hardly justified, especially at the low switching frequency exemplified. Reactive elements influence not only small-signal transfer functions, but also steady-state frequency responses unless the filter is designed in suitable proportion to the load. Furthermore, inductors and capacitors serve more than just filters: they are also *topological elements*; for instance, boost-type topologies with finite switching frequency simply do not exist if they are deprived of inductors. Therefore, failure to acknowledge the *topological role* of energy-storage components means rejection of a host of useful, ideal cycloconverter topologies. More on the significance of filter elements is examined in next chapter.

8.2.2 Resonant Cycloconverters

A typical *resonant cycloconverter*, such as the "parallel" one in [34] or "series" one in [35], can be cast in the block diagram of Fig. 8.5. The circuit consists mainly of a set of *modulation switches*, a *resonant tank*, and a set of *demodulation switches*. The modulation switches convert three-phase, low-frequency line energy into single-phase, high-frequency resonant power. The resonant power is then redistributed into a three-phase load under another amplitude and frequency by the demodulation switches.

Two frequencies govern the operation of each set of switches: a slow one to select which two input lines to deliver or two output lines to consume power, and a fast one to excite or extract energy from the resonant tank. Input line selection is done at line frequency by the input switches, and output load selection at load frequency by the output switches.

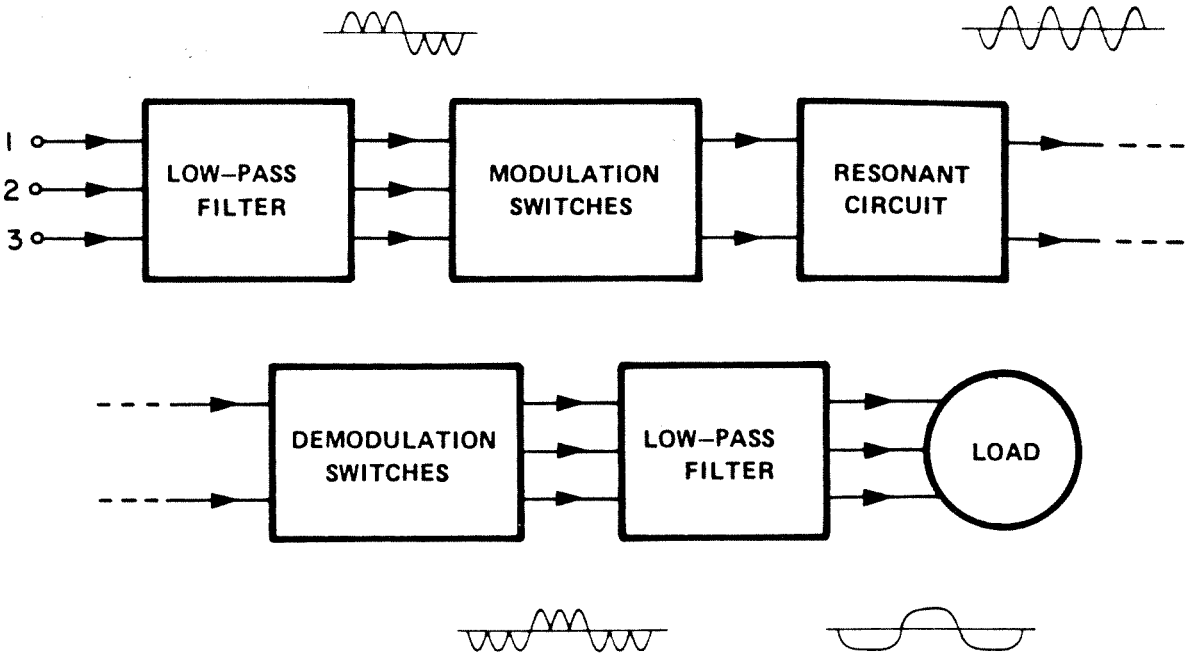


Fig. 8.5 Functional block diagram of a resonant cycloconverter showing a resonant link surrounded by modulation and demodulation switches.

As far as the slow action is concerned, the modulation switches in [35] follow the six-stepped sequence of a phase-controlled rectifier, and the demodulation switches that of a current-source inverter.

Within each sixth of a line period, the input throws are switched at high frequency, usually at .5 duty ratio, to excite the resonant link. The area of a resonant pulse can be coded with the desired amount of energy by modulation of this high switching frequency; therefore, variation of the switching frequency is the principal means to regulate the amount of power into the load. Within each sixth of an output cycle, the demodulation throws are locked to the resonant frequency to transfer tank energy into the output. Polarities of the load and tank currents are required to determine

which throws steer the resonant pulses.

If operated in the proper frequency range, the resonant cycloconverter turns its switches off at zero or low current; this low current stress renders the circuit attractive for high-power applications. Owing to its high-frequency link, the topology permits a wide range of output frequency. Power factors at both input and output ports can be adjusted independently. Power flow can be reversed electronically, and regeneration is thus speedy.

Resonant cycloconverters usually require more components than PWM ones. For instance, the example in [35] needs four-quadrant switches because the voltages and link current are all ac. Control hardware is complicated because most voltages and currents have to be sensed just for switching purposes. At the present, this circuit complexity is not very well traded off for waveform quality: a fair amount of low-frequency harmonics is still present owing to six-stepped influence. More study needs be carried out to see whether clean power is obtainable from simple (e.g., sinusoidal) frequency modulation functions.

One major obstacle to the widespread use of resonant cycloconverters is the lack of basic understanding and analytical techniques for these networks. Standard tools for PWM converters are not applicable here since switching and resonant frequencies are generally comparable. Fortunately, methods have been proposed in [36] to contribute more insight to steady-state and dynamic behavior of dc resonant converters. Similar efforts are undoubtedly valuable to the promotion of resonant cycloconversion.

In conclusion, existing cycloconverters can be classified either as slow- or fast-switching according to the ratio of switching to input or output frequency. Members of the slow-switching group share the buck-type topology with a varying number of switches. Examples are the *phase-controlled cycloconverter*, whose throws are fired at angles *modulated* at the output frequency, and *unrestricted frequency changer*, whose throws are fired *uniformly* at the sum or difference of input and output frequencies. Fast-switching cycloconverters operate on either PWM or resonant principle. Reviewed are the buck-type *PWM high-frequency-synthesis cycloconverter* and series and parallel *resonant cycloconverters*. The theory in fast-switching cycloconversion is still at an elementary stage, especially when reactive elements are considered integrally as topological components. The following chapters augment this theory with more ideal PWM topologies and modeling techniques.

CHAPTER 9

FAST-SWITCHING SINUSOIDAL PWM CYCLOCONVERTERS

This chapter presents *fast-switching PWM* cycloconverters that synthesize *sinusoidal* waveforms from *sinusoidal* control functions. The numbers of input and output phases may differ and are generally greater than one. If there are two phases, they are displaced by $\pm 90°$; if there are N phases, any two adjacent ones are displaced by $\pm \frac{360°}{N}$. Although a two-phase cycloconverter and an $N(>2)-M(>2)-$phase one differ slightly in topology, they share identical mathematical and functional characteristics.

Four topics are discussed in this chapter. The *topologies* are described and their *inputs* specified in the first section. *Steady-state* performance is next analyzed, by the describing equation technique, in the second section. Dynamics is bypassed here since it is just another straightforward repetition of the procedure outlined in Chapter 1 and exemplified in Chapters 3 and 6. *Canonical models* of the topologies are then compared in the third section. Finally, the cycloconverter is related topologically to the dc converter, inverter, and rectifier and endorsed as the *generalized converter* for all four fields of power electronics.

9.1 Description of Topologies

The *buck*, *boost*, *buck-boost*, and *flyback cycloconverters* are presented in this section. Each is elaborated in terms of the positions of its switches and reactive components relative to the sources and load. The switches are characterized by their continuous *duty ratios*, and the sources their sinusoidal voltages. The load is assumed to be resistive for simplicity sake although it can be any other balanced polyphase impedances, e.g., ac machines, utility bus, and so on.

9.1.1 Buck Cycloconverter

The *buck cycloconverter* is the extension of the fast-switching buck dc converter or slow-switching phase-controlled cycloconverter (or UFC) into high-frequency cycloconversion. As is delineated in Fig. 9.1, an $N\,(>2)-M\,(>2)-$phase buck cycloconverter retains the familiar traits of a voltage-fed topology: M N-throw switches feeding the load through a polyphase LC filter. Although the switch arrangement here is identical to that in the three-pulse network in Fig. 8.3, the drive strategy is completely different. The throws are switched at high frequency and pulse-width-modulated according to

$$d_{wk} = \frac{1}{N} + d_{wke} \tag{9.1}$$

where the *effective duty ratio* d_{wke} satisfies

$$d_{wke} = \frac{d_m}{N}\cos\left[\theta + (k-1)\frac{2\pi}{N} \pm (w-1)\frac{2\pi}{M}\right] = d_{wk} - \frac{1}{M}\sum_{z=1}^{M} d_{zk} \tag{9.2}$$

where

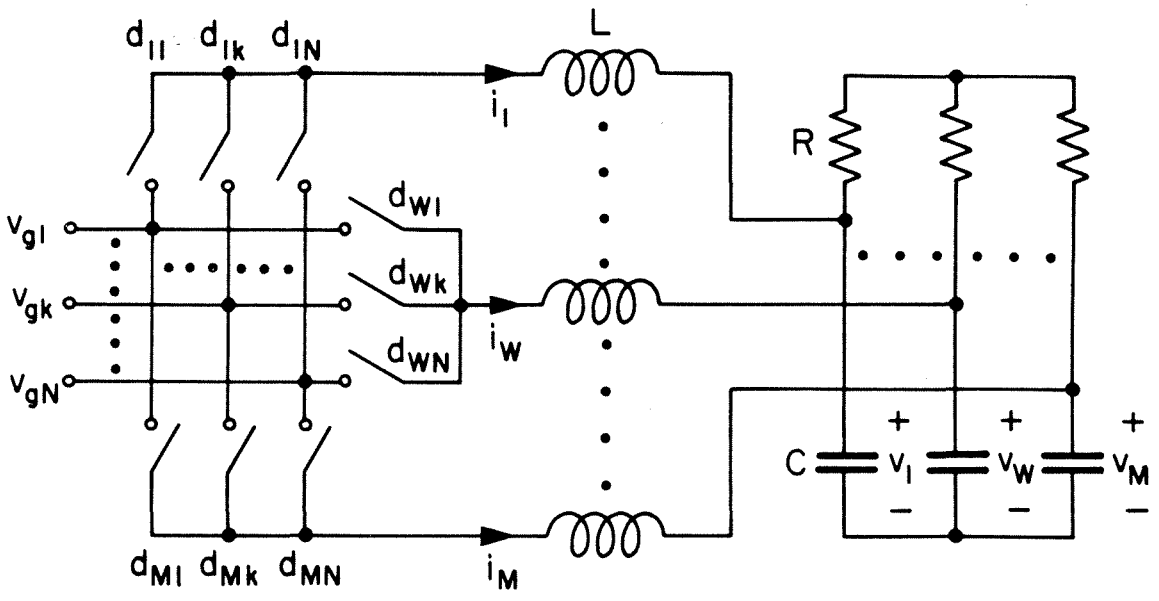


Fig. 9.1 N-M-phase buck cycloconverter with M N-throw switches pulse-width-modulated by sinusoidal functions.

$$1 \le k \le N \quad , \qquad 1 \le w \le M \tag{9.3a,b}$$

$$d_m \le 1 \text{ , and} \qquad \theta = \int_0^t \omega(\tau) d\tau \tag{9.3c,d}$$

In the above, $\frac{d_m}{N}$ is the *instantaneous modulation amplitude* and ω the *instantaneous modulation frequency*; negative ω is possible and means a reversal of phase sequence. The signs of phase sequence as specified in Eq. (9.2), together with the arbitrary sign of ω, account for all possible combinations of modulation phase sequences.

Besides the balanced polyphase duty ratios, the other inputs are the sources of excitation, also balanced polyphase:

$$v_{gk} = v_g \cos\left[\theta_g - (k-1)\frac{2\pi}{N}\right], \qquad (1 \le k \le N) \tag{9.4}$$

where

$$\theta_g = \int_0^t \omega_g(\tau)d\tau + \varphi_g \tag{9.5}$$

where v_g is the *instantaneous input amplitude* and ω_g the *instantaneous input frequency*, which takes on both polarities.

The switches governed by Eq. (9.1) convert the N voltages defined by Eq. (9.4) into M balanced *sinusoidal* voltages at frequency $\omega_v = \omega + \omega_g$, which can be any real number, superimposed by switching noise. These pulsating waveforms are then passed to the load through *small* LC low-pass filters designed to attenuate the high-frequency noise without significantly affecting the desired sinusoids. The inductors can be integrated to save magnetic material since their *instantaneous* fluxes sum up to zero. The capacitors can be connected in a delta although they are illustrated in a wye configuration. The load may be more than a trivial resistor bank: if an impedance can be driven by a slow-switching cycloconverter, it should perform smoother if supplied by a fast-switching PWM cycloconverter.

Modified reduction of the generalized topology in Fig. 9.1 results in the two-phase buck cycloconverter captured in Fig. 9.2. The circuit consists of three poles, the third one for the load neutral; each pole has three throws, the third one for the source neutral. The main now satisfies

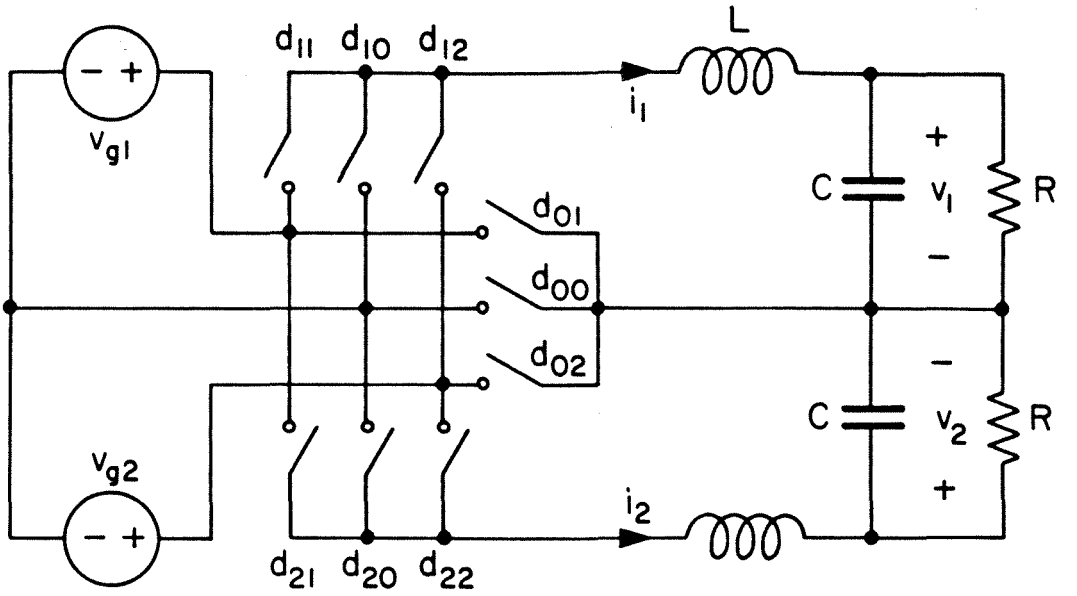


Fig. 9.2 Two-phase buck cycloconverter.

$$v_{gk} = v_g \cos\left[\theta_g - (k-1)\frac{\pi}{2}\right], \quad k = 1,2 \tag{9.6}$$

The duty ratios for the switches are

$$d_{0k} = \frac{1}{2+\sqrt{2}} - \frac{d_{mo}}{2+\sqrt{2}} \cos\left[\theta_o + (k-1)\frac{\pi}{2}\right] \tag{9.7a}$$

$$d_{1k} = \frac{1}{2+\sqrt{2}} + \frac{d_{mo}}{2+\sqrt{2}} \cos\left[\theta_o + (k-1)\frac{\pi}{2} \pm \frac{\pi}{2}\right] \tag{9.7b}$$

$$d_{2k} = \frac{1}{2+\sqrt{2}} - \frac{d_{mo}}{2+\sqrt{2}} \cos\left[\theta_o + (k-1)\frac{\pi}{2} \pm \frac{\pi}{2}\right] \tag{9.7c}$$

where

$$1 \le k \le 2 \ , \quad d_{mo} \le 1 \ , \quad \text{and} \quad \theta_o = \int_0^t \omega(\tau)\, d\tau + \varphi_o \qquad (9.8a,b,c)$$

This selection of duty ratio optimizes the effective duty ratio d_{wke}:

$$d_{wke} = d_{wk} - d_{0k} = \frac{d_m}{2} \cos\left[\, \theta + (k-1)\,\frac{\pi}{2} \pm (w-1)\,\frac{\pi}{2}\,\right] \qquad (9.9)$$

where

$$1 \le w \le 2 \ , \quad 1 \le k \le 2 \ , \quad \text{and} \quad d_m \le \frac{2\sqrt{2}}{2+\sqrt{2}} \qquad (9.10a,b,c)$$

With the above controls and inputs, the two-phase cycloconverter performs as the generalized one.

In summary, an $N-M$ *-phase buck cycloconverter* consists mainly of M N-throw switches *pulse-width-modulated* by continuous balanced *sinusoids* at frequency ω much lower than the switching frequency. These switches cycloconvert N sinusoidal input voltages at frequency ω_g into M desired components at frequency $\omega_g + \omega$ and switching harmonics. Small LC filters are inserted after the switch matrix so that the load receives smooth, *sinusoidal* waveforms.

9.1.2 Boost Cycloconverter

The boost *cycloconverter* results from reverse operation of the buck cycloconverter or extension of the boost dc converter into cycloconversion. As is depicted in Fig. 9.3, an $N-M$ -phase boost topology exhibits the familiar constituents of a current-fed structure: inductors in series with the sources to transform voltages into currents and switches to feed these currents into the load. External inductors may be saved if line inductance is available; they can be integrated onto one magnetic piece since their

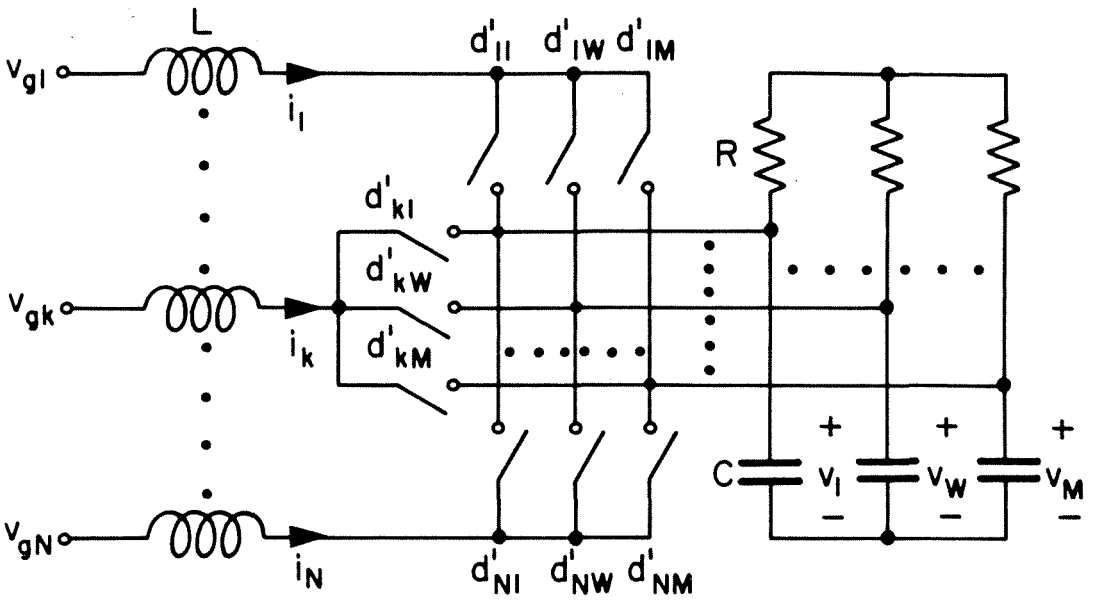


Fig. 9.3 N-M-phase boost cycloconverter with N M-throw switches pulse-width-modulated by sinusoidal functions.

instantaneous fluxes sum up to zero. The N M-throw switches are operated at high frequency and modulated according to

$$d'_{kw} = \frac{1}{M} + d'_{kwe} \tag{9.11}$$

where the *effective duty ratio* d'_{kwe} satisfies

$$d'_{kwe} = \frac{d'_m}{M} \cos\left[\theta' + (k-1)\frac{2\pi}{N} \pm (w-1)\frac{2\pi}{M}\right] = d'_{kw} - \frac{1}{N}\sum_{l=1}^{N} d'_{lw} \tag{9.12}$$

where

$$1 \le k \le N \quad , \qquad 1 \le w \le M \tag{9.13a,b}$$

$$d_m' \leq 1 \text{ , and} \qquad \theta' = \int_0^t \omega'(\tau) d\tau \tag{9.13c,d}$$

where prime (') has been used with duty ratios associated with the output side of the circuit. The above duty ratios interact with the voltages specified in Eq. 9.4 to generate N *sinusoidal* inductor currents at the *same* frequency and phase sequence as those of the main and to convert these currents into M *sinusoidal* load currents at frequency $\omega_v = \omega_g + \omega'$ (each frequency can be any real number). Of course, there are also current harmonics at high frequency, and they are shunted away from the load by the capacitors.

The two-phase boost cycloconverter is shown in Fig. 9.4. A third pole has been added to switch the source neutral, and a third throw is present in each pole to return current for the load neutral. The duty ratios of the switches are

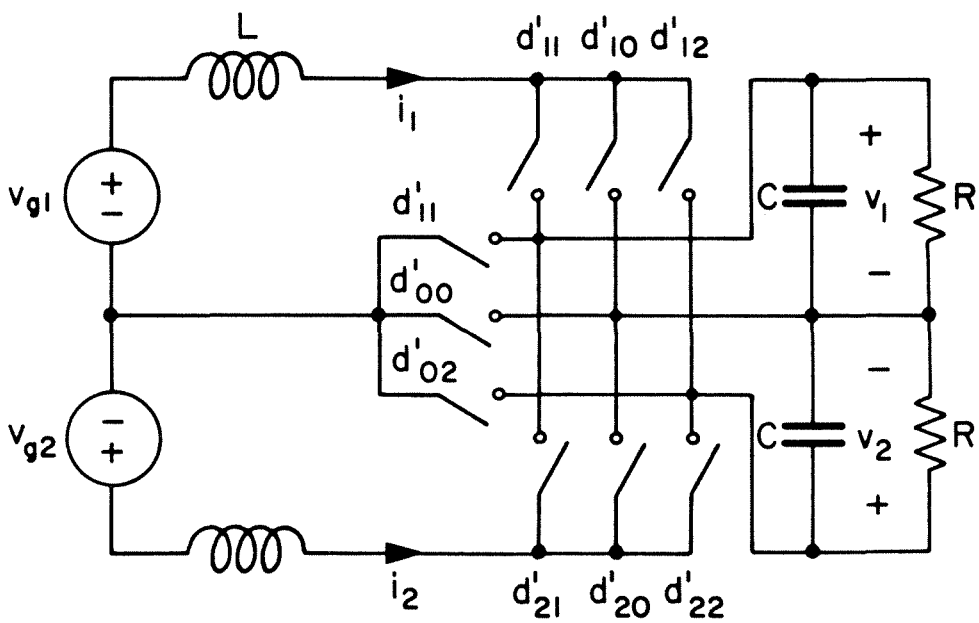


Fig. 9.4 Two-phase boost cycloconverter.

$$d'_{0w} = \frac{1}{2+\sqrt{2}} - \frac{d'_{mo}}{2+\sqrt{2}} \cos[\theta'_o \pm (w-1)\frac{\pi}{2}] \qquad (9.14a)$$

$$d'_{1w} = \frac{1}{2+\sqrt{2}} + \frac{d'_{mo}}{2+\sqrt{2}} \cos[\theta'_o \pm (w-1)\frac{\pi}{2} + \frac{\pi}{2}] \qquad (9.14b)$$

$$d'_{2w} = \frac{1}{2+\sqrt{2}} + \frac{d'_{mo}}{2+\sqrt{2}} \cos[\theta'_o \pm (w-1)\frac{\pi}{2} - \frac{\pi}{2}] \qquad (9.14c)$$

where

$$1 \le w \le 2 \ , \quad d'_{mo} \le 1 \ , \quad \text{and} \quad \theta'_o = \int_0^t \omega'(\tau)\, d\tau + \varphi'_o \qquad (9.15a,b,c)$$

This selection of duty ratio optimizes the effective duty ratio d'_{kwe}:

$$d'_{kwe} = d'_{kw} - d'_{0w} = \frac{d'_m}{2} \cos[\theta' + (k-1)\frac{\pi}{2} \pm (w-1)\frac{\pi}{2}] \qquad (9.16)$$

where

$$1 \le w \le 2 \ , \quad 1 \le k \le 2 \ , \quad \text{and} \quad d'_m \le \frac{2\sqrt{2}}{2+\sqrt{2}} \qquad (9.17a,b,c)$$

With the above duty ratio assignment, the two-phase boost cycloconverter behaves as the $N-M$ −phase one.

In review, an $N-M$ *−phase boost cycloconverter* places N inductors between the sources and switches to transform source voltages into *sinusoidal currents* at the source frequency. The switches then pulse-width-modulate these currents, by *sinusoidal* duty ratios at frequency ω', into M *sinusoidal* currents at frequency $\omega_g + \omega'$. The cycloconverted currents generate smooth, sinusoidal voltages on the output impedance.

9.1.3 Buck-Boost and Flyback Cycloconverters

The *buck-boost cycloconverter* is the polyphase-to-polyphase version of the buck-boost dc converter. As is described in Fig. 9.5, an $N\,(>2)-M\,(>2)-$phase topology looks similar to an overall slow-switching current-source inverter system, composed of a phase-controlled rectifier at the input, a 60 Hz choke as intermediate dc link, and a current-source inverter at the output. Despite this similarity, the *four independent* switches in the buck-boost cycloconverter operate on an entirely different principle. The two independent N-throw switches right after the source are not phase-controlled: they are pulse-width-modulated at high frequency with the continuous duty ratios

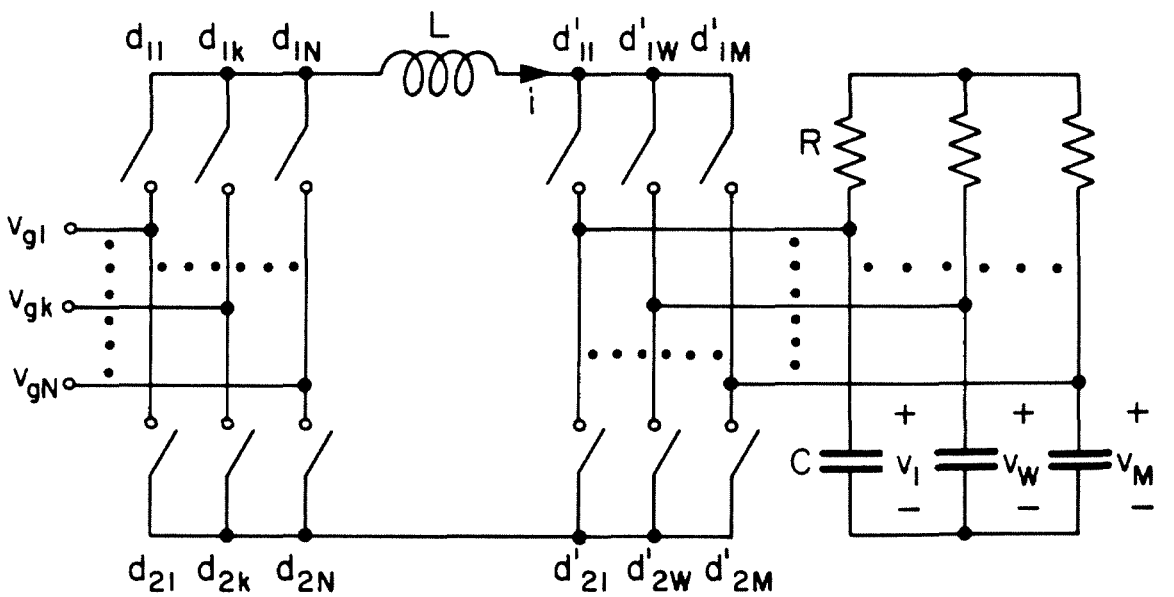


Fig. 9.5 N-M-phase buck-boost cycloconverter, cascade of an N-phase buck rectifier and an M-phase boost inverter.

$$d_{rk} = \frac{1}{N} + \frac{d_{mr}}{N} \cos[\,\theta_r - (k-1)\,\frac{2\pi}{N}\,] \tag{9.18}$$

where

$$1 \le r \le 2 \quad , \quad 1 \le k \le N \tag{9.19a,b}$$

$$d_{mr} \le 1 \qquad \text{and} \qquad \theta_r = \int_0^t \omega_g(\tau)d\tau + \varphi_r \tag{9.19c,d}$$

According to the above, the modulation amplitudes and phases of two input switches are generally independent. The optimal *effective duty ratio* is attained when the amplitudes equal and phases oppose:

$$d_k = d_{1k} - d_{2k} = \frac{2d_m}{N} \cos[\,\theta - (k-1)\,\frac{2\pi}{N}\,] \tag{9.20}$$

where

$$d_m \le 1 \qquad \text{and} \qquad \theta = \int_0^t \omega_g(\tau)d\tau \tag{9.21a,b}$$

This optimality, however, is only with respect to *continuous* PWM and is still inferior to some piecewise continuous strategy, such as six-stepped PWM (Subsection 4.1.2).

Once the instantaneous frequency and phase sequence of duty ratio modulation are locked to those of the line, an effective *dc* voltage is generated at the input end of the inductor. The inductor then transforms this voltage into a *dc* current, just as in a boost inverter. In contrast to that in a current-source inverter, the inductor in a buck-boost cycloconverter is *small* owing to fast switching; therefore, the dynamic response here is very *fast* and can be improved further by increase of the switching frequency. In general, more than one inductor may store the

intermediate energy, and their currents may be balanced polyphase dc or ac. This generic topology, however, is only of theoretical interest.

The two *independent* M-throw switches at the output invert the inductor current into M *sinusoidal* currents at frequency ω'. Again, this inversion is not six-stepped, but is fast-switching PWM with

$$d'_{rw} = \frac{1}{M} + \frac{d'_{mr}}{M} \cos\left[\theta'_r - (w-1)\frac{2\pi}{M}\right] \tag{9.22}$$

where

$$1 \le r \le 2 \quad , \quad 1 \le w \le M \tag{9.23a,b}$$

$$d'_{mr} \le 1 \quad \text{and} \quad \theta'_r = \int_0^t \omega'(\tau)\, d\tau + \varphi'_r \tag{9.23c,d}$$

In analogy with Eq. (9.20), the maximum effective duty ratio at the output can be chosen to be

$$d'_w = d'_{1w} - d'_{2w} = \frac{2d'_m}{M} \cos\left[\theta' - (w-1)\frac{2\pi}{M}\right] \tag{9.24}$$

where

$$d'_m \le 1 \quad \text{and} \quad \theta' = \int_0^t \omega'(\tau)\, d\tau \tag{9.25a,b}$$

Six-stepped PWM is certainly applicable to the output switches also.

The two-phase buck-boost cycloconverter is portrayed in Fig. 9.6. The input switches are modulated according to

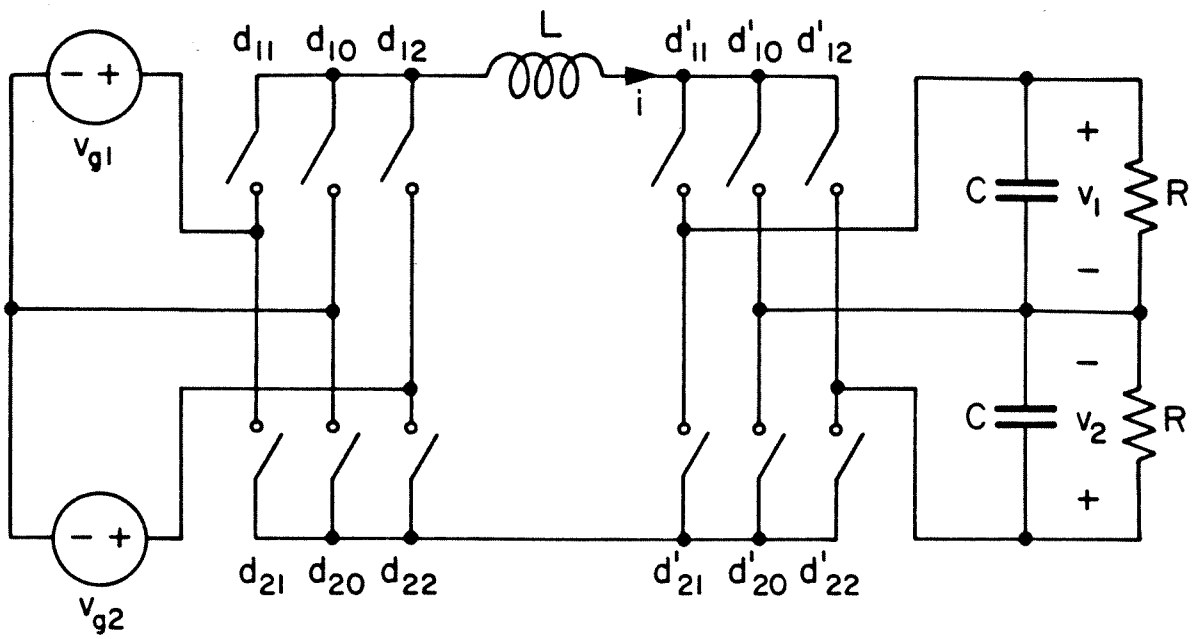


Fig. 9.6 Two-phase buck-boost cycloconverter.

$$d_{1k} = \frac{1}{2+\sqrt{2}} + \frac{d_m}{2}\cos\left[\theta-(k-1)\frac{\pi}{2}\right] \tag{9.26a}$$

$$d_{2k} = \frac{1}{2+\sqrt{2}} - \frac{d_m}{2}\cos\left[\theta-(k-1)\frac{\pi}{2}\right] \tag{9.26b}$$

where

$$k = 1,2\ , \qquad d_m \le \frac{2}{2+\sqrt{2}}\ , \qquad \text{and} \qquad \theta = \int_0^t \omega_g(\tau)\,d\tau \tag{9.27a,b,c}$$

This modulation provides the highest effective duty ratio defined in Eq. (9.20). The output duty ratios satisfy similar equations:

$$d'_{1w} = \frac{1}{2+\sqrt{2}} + \frac{d'_m}{2}\cos\left[\theta' - (w-1)\frac{\pi}{2}\right] \tag{9.28a}$$

$$d'_{2w} = \frac{1}{2+\sqrt{2}} - \frac{d'_m}{2}\cos\left[\theta' - (w-1)\frac{\pi}{2}\right] \tag{9.28b}$$

where

$$w = 1,2\ , \qquad d'_m \le \frac{2}{2+\sqrt{2}}\ , \qquad \text{and} \qquad \theta' = \int_0^t \omega'(\tau)\,d\tau \tag{9.29a,b,c}$$

These functions maximize the effective duty ratio specified in Eq. (9.24). Apart from the preceding modifications, the two-phase and $N-M-$phase buck-boost cycloconverters are alike in performance.

Topological manipulation of the buck-boost cycloconverter yields the $N\,(>2)-M\,(>2)-$*phase flyback cycloconverter* presented in Fig. 9.7. The topology consists of only *two* independent switches, instead of four as in the buck-boost converter; each switch has $(N+M)$ throws. In interval $d\,T_s$ of each switching period T_s, the input throws charge up the inductor by

$$d_{rk} = \frac{d}{N} + \frac{d_{mr}}{N}\cos\left[\theta_r - (k-1)\frac{2\pi}{N}\right] \tag{9.30}$$

where

$$1 \le r \le 2 \qquad , \qquad 1 \le k \le N \tag{9.31a,b}$$

$$d_{mr} \le d \qquad \text{and} \qquad \theta_r = \int_0^t \omega_g(\tau)d\tau + \varphi_r \tag{9.31c,d}$$

According to the above, the modulation amplitudes and phases of two input switches are generally independent. The optimal *effective duty ratio* is attained when the amplitudes equal and phases oppose:

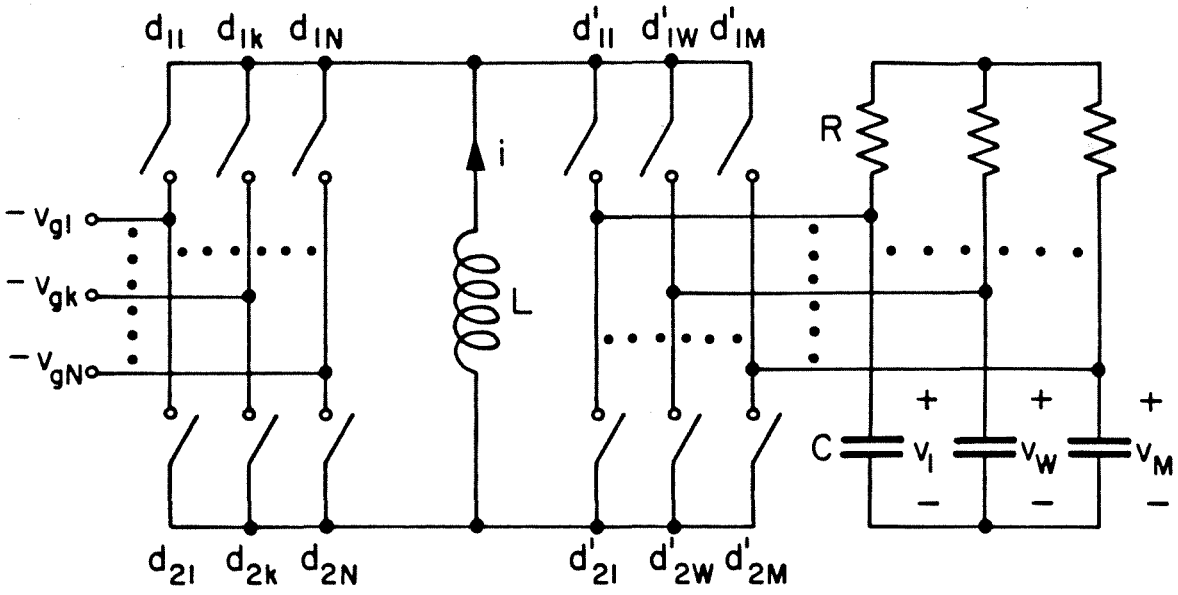


Fig. 9.7 N-M-phase flyback cycloconverter with two (N+M)-throw switches pulse-width-modulated by sinusoidal functions.

$$d_k = d_{1k} - d_{2k} = \frac{2d_m}{N} \cos\left[\theta - (k-1)\frac{2\pi}{N}\right] \tag{9.32}$$

where

$$d_m \leq 1 \qquad \text{and} \qquad \theta = \int_0^t \omega_g(\tau)\, d\tau \tag{9.33a,b}$$

After the charging time, the inductor discharges its current into the load during $d'\ T_s$ with

$$d'_{rw} = \frac{d'}{M} + \frac{d'_{mr}}{M} \cos\left[\theta'_r - (w-1)\frac{2\pi}{M}\right] \tag{9.34}$$

where

$$1 \le r \le 2 \quad , \quad 1 \le w \le M \tag{9.35a,b}$$

$$d'_{mr} \le d' \qquad \text{and} \qquad \theta'_r = \int_0^t \omega'(\tau)\, d\tau + \varphi'_r \tag{9.35c,d}$$

In analogy with Eq. (9.32), the maximum effective duty ratio at the output can be chosen to be

$$d'_w = d'_{1w} - d'_{2w} = \frac{2d'_m}{M} \cos\left[\theta' - (w-1)\frac{2\pi}{M}\right] \tag{9.36}$$

where

$$d'_m \le d' \qquad \text{and} \qquad \theta' = \int_0^t \omega'(\tau)\, d\tau \tag{9.37a,b}$$

Six-stepped PWM is a beneficial alternative to the above modulation policy.

As in the buck-boost converter, sinusoidal input voltages and duty ratio modulations establish a dc current in the inductor. This dc current is then inverted into M *sinusoidal* currents and voltages at any frequency ω' for the load. Operating principles of the flyback and buck-boost cycloconverters are thus similar; their mathematical descriptions can be proved to be also identical.

The two-phase flyback cycloconverter is illustrated in Fig. 9.8. Its duty ratios are assigned as follows:

$$d_{1k} = \frac{d}{2+\sqrt{2}} + \frac{d_m}{2} \cos\left[\theta - (k-1)\frac{\pi}{2}\right] \tag{9.38a}$$

$$d_{2k} = \frac{d}{2+\sqrt{2}} - \frac{d_m}{2} \cos\left[\theta - (k-1)\frac{\pi}{2}\right] \tag{9.38b}$$

where

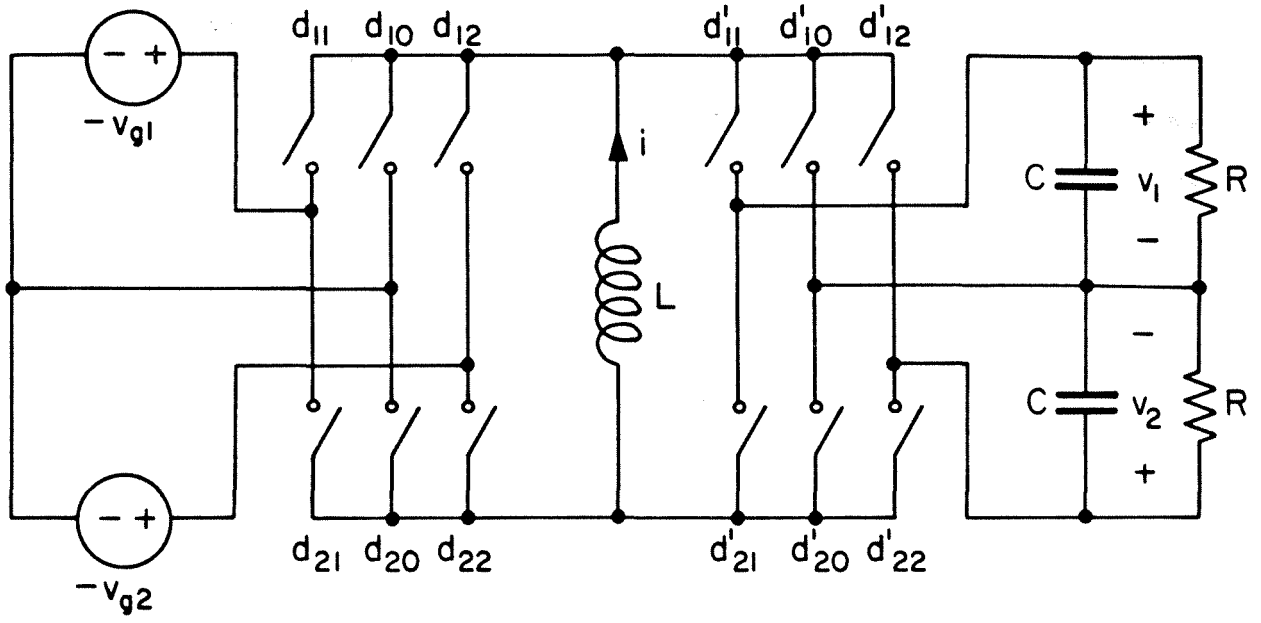


Fig. 9.8 Two-phase flyback cycloconverter.

$$k = 1,2\ , \qquad d_m \le \frac{2}{2+\sqrt{2}}\, d\ , \qquad \text{and} \qquad \theta = \int_0^t \omega_g(\tau)\, d\tau \tag{9.39a,b,c}$$

$$d'_{1w} = \frac{d'}{2+\sqrt{2}} + \frac{d'_m}{2} \cos\left[\, \theta' - (w-1)\,\frac{\pi}{2}\,\right] \tag{9.40a}$$

$$d'_{2w} = \frac{d'}{2+\sqrt{2}} - \frac{d'_m}{2} \cos\left[\, \theta' - (w-1)\,\frac{\pi}{2}\,\right] \tag{9.40b}$$

where

$$w = 1,2\ , \qquad d'_m \le \frac{2}{2+\sqrt{2}}\, d'\ , \qquad \text{and} \qquad \theta' = \int_0^t \omega'(\tau)\, d\tau \tag{9.41a,b,c}$$

In retrospect, the *buck-boost* and *flyback cycloconverters* are examples of *current-fed, indirect* cycloconversion: they rely on intermediate dc current link. They use a set of input throws pulse-width-modulated *sinusoidally* at line frequency to build up a *dc* current in the energy storage/transfer inductor. Another set of output throws then invert this current into balanced *sinusoidal* currents at *any* frequency for the load.

9.2 Steady-State Performance

Describing equations of the cycloconverters introduced in the previous section can be derived by following the method developed in Chapter 1. Steady-state solutions of these equations are then solved in either stationary (abc) or *rotating (ofb)* frame of reference; the later one has been adopted in view of its applicability to dynamic and canonical models. The ofb equations are obtained from the abc ones via coordinate transformation. Since there are usually more than one frequency involved, the transformation actually comprises many sub-transformations, each for one frequency. If a state is single-phase (e.g., the inductor current in a flyback converter), it needs be passed simply through a *unity* sub-transformation. If many states constitute a balanced polyphase set (e.g., the capacitor voltages), they require the *abc-ofb* sub-transformation reviewed in Appendix B. The sub-transformation of M states at *instantaneous frequency* ω_v also has *order* M and *instantaneous frequency* ω_v.

After the transformation, $M-2$ of the M balanced polyphase quantities are discarded as they are either identically zero or indeterminate but fixed to zero in practice. The remaining two states are the *backward component*, directly proportional to the phasor describing the stationary

sinusoidal waveforms, and *forward component*, the complex conjugate of the former. *All balanced systems with more than two input or output phases are thus equivalent and reducible a two-phase system.*

For the topologies described earlier, the reduced equations have *time-invariant* coefficients under steady-state condition; therefore, steady-state ofb solutions are *constant*. A *constant ofb scalar* corresponds to a *dc* abc value, and a *constant ofb phasor* translates to *sinusoidal* abc waveforms. Thus, the buck, boost, buck-boost, and flyback cycloconverters are *ideal* as expected. Steady-state capacitor voltages and inductor currents for optimal continuous modulation and resistive load are tabulated in Table 9.1; these results can be used directly in design since they describe actual waveforms.

The phase angle φ_g in Eq. (9.5) has been set to zero for steady-state evaluation of the buck and boost cycloconverters. In the buck case, both inductor current and capacitor voltage are sinusoids at frequency $\Omega_v = \Omega + \Omega_g$. If the switching frequency is infinite, Ω_v may be *any* real value; otherwise, the upper bound for Ω_v is limited only by the amount of ripple the load is willing to tolerate. *Negative* Ω_v is equivalent to *positive* Ω_v with opposite phase angle: the modulation frequency and phase sequence can always be chosen to reverse the phase sequence and sign of reactive power across the switches.

At low filter reactances, the voltage gain of the buck cycloconverter is $\frac{D_m}{2}$; the topology thus deserves its name. Unfortunately, this gain is too low: the output is at most half of the input amplitude. The basic circuit thus needs modification if it is to drive a load rated at line condition. Note that the low-reactance output is independent of the number of input

Type	Capacitor Voltage $V e^{-j\Phi_v}$	Inductor Current $I e^{-j\Phi_i}$
Buck	$\frac{D_m V_g}{2} \frac{1}{1+j\Omega_v \frac{L}{R}+(j\Omega_v)^2 LC}$	$\frac{D_m V_g}{2R} \frac{1+j\Omega_v LC}{1+j\Omega_v \frac{L}{R}+(j\Omega_v)^2 LC}$
Boost	$\frac{2V_g}{D_m'} \frac{1}{1+j\Omega_g \frac{L_e}{R}-\Omega_g\Omega_v L_e C}$	$\frac{4MV_g}{ND_m'^2 R} \frac{1+j\Omega_v RC}{1+j\Omega_g \frac{L_e}{R}-\Omega_g\Omega_v L_e C}$
Flyback	$\frac{D_m}{D_m'} V_g \cos\Phi_g \ (1-j\Omega' RC)$	$\frac{M}{2} \frac{D_m}{D_m'^2 R} V_g \cos\Phi_g \ (1+\Omega'^2 R^2 C^2)$
where $\Omega_v = \Omega+\Omega_g$ or $\Omega'+\Omega_g$; $L_e = \frac{4M}{ND_m'^2} L$		

TABLE 9.1 Steady-state capacitor voltages and inductor currents in the buck, boost, and flyback (or buck-boost) cycloconverters.

and output phases because the duty ratio is not a function of M and any change in N is offset by an opposite change in modulation amplitude. All phases of the network are thus completely decoupled, each being excited and filtered separately.

Since filter reactances are nonzero, their effects become pronounced as the output frequency increases. For the buck cycloconverter feeding a resistive load, the *steady-state frequency response* for the capacitor voltage is simply a second-order roll-off whose poles are the LC corner. In general, the response depends on the interaction between filter and load impedances. It may shape the amplitude gain to be completely different from a flat $\frac{D_m}{2}$ and present the main with something other than the load impedance unless the filter is intentionally designed to locate steady-state corners beyond the output frequency range of interest.

The inductor current and capacitor voltage in the boost cycloconverter are also *sinusoidal*. The frequency and phase sequence of the currents are obviously identical to those of the source. The frequency of the voltages is $\Omega_v = \Omega_g + \Omega'$ and may be adjusted to *any real* number via the modulation frequency Ω'; the sign of Ω_v can be used to control those of reactive power and phase sequence *across the switches*.

As filter reactances approach zero, the dc voltage gain approaches $\frac{2}{D_m'}$: the circuit steps up as expected . As in the buck case, the low effective modulation amplitude here prevents the voltage amplitude to go *below* $2V_g$; therefore, modification of the original topology is essential to recover the voltage range below $2V_g$. The boosting property, however, does

not hold when Ω_g and Ω_v are large: the voltage tends toward *zero*, instead of infinity, as D'_m approaches zero. Recall that boosting action prevails in a boost *dc* converter because the output voltage always has to be higher than input voltage to maintain volt-second balance for the inductor. In a boost *cycloconverter*, the output voltages are not the sole mechanism for volt-second balance: the *input* voltages also contribute volt-second balance since they are already *ac*. As the modulation amplitude approaches zero, the inductors are effectively connected in a star configuration, whose center is the shorted switched ends of the inductors, and are completely volt-second balanced by the *ac* inputs. Sinusoidal currents are established in the inductors, but they only circulate reactive power in the star, and do not deliver any real power to the load.

In the presence of *nonzero filter reactances*, then, *buck*-type property in one direction does *not* imply *boost*-type property in the other.

Filter reactances also modify the magnitude and phase of steady-state phasors at high input and output frequencies. The voltage *steady-state frequency response* for a boost cycloconverter driving a resistive load looks "second-order" but is actually not. This type of response is rarely encountered in linear circuits as it involves two different frequencies: one in the inductive reactance $\Omega_g L$ and the other in the capacitive susceptance $\Omega_v C$, and these two frequencies do not change together. In motor drives, for instance, Ω_g is constant while Ω_v is adjusted; in variable-speed, constant frequency generators, the opposite situation holds; and in variable-frequency, variable-speed applications, both Ω_g and Ω_v fluctuate independently. The phase response as a function of only Ω_v starts out at $-\arctan\frac{\Omega_g L_e}{R}$ and

drops toward -180°, the first 90° from the inductor and the second from the capacitor. Interestingly, this second-order phase trend is accompanied by a magnitude roll-off of only first order because only the capacitive, not inductive, reactance changes with Ω_v. Unusual steady-state transfer functions undoubtedly exist for other frequency and loading situations.

In the analysis of the buck-boost and flyback cycloconverters, the source phase angle φ_g is preserved. This angle controls not only the output amplitude, but also the input power factor. Since the inductor current is *dc*, the input power angle is also φ_g; therefore, any angle between $-180°$ and $+180°$ is possible. This freedom is a definite advantage over the buck and boost converters, in which the magnitude of input power angle is fixed by the load and only the sign can be changed.

The capacitor voltages are sinusoidal as expected. Their frequency is the modulation frequency Ω' and can be any real number. The sign of Ω' controls the phase sequence into the load. At low capacitive susceptance, the dc voltage gain is $\frac{D_m}{D_m'}\cos\Phi_g$; stepping down is thus possible through the input modulation amplitude, and stepping up the output one; Φ_g should be saved for power factor control. At high Ω', a rhp zero shapes the steady-state frequency response; this phenomenon has been found in the boost inverter and attributed to the volt-second balance requirement for the inductor.

To summarize, the buck, boost, buck-boost, and flyback cycloconverters are indeed *ideal*, namely, they all generate *sinusoidal* output voltages and input currents from *sinusoidal* duty ratio modulations. *Any output frequency* or *phase sequence* is possible, the frequency limit being

determined by the switching frequency. *Complete control of input power factor* is possible only with the buck-boost and flyback topologies owing to their dc link. When filter reactances are low, the buck cycloconverter steps down; the boost, up; and the buck-boost or flyback, up and down. Filter reactances generally affect even *steady-state frequency responses* and can be neglected *only by design*.

9.3 Canonical Models

As inverters and rectifiers, cycloconverters are modeled in the ofb reference frame where they are *time-invariant*. To put the buck cycloconverter in the ofb coordinates, the following phase can be used for current and voltage transformations:

$$\theta_{Ti} = \theta_{Tv} = \int_0^t [\,\omega(\tau) + \omega_g(\tau)\,]\, d\tau \tag{9.42}$$

Since there is neither rectification nor inversion in the topology, backward and forward components do not have to interact to convert complex into real power; therefore, backward and forward circuits are decoupled. The canonical model relating backward voltage and current is depicted in Fig. 9.9.

The model includes excitation and control generators, a cycloconversion transformer, and a complex low-pass filter. The *excitation generator* is the backward phasor of input phase voltage (note that φ_g has been set to zero without loss of generality). The *control generators* are dependent voltage and current sources controlled by the frequency and amplitude of duty ratio modulations as well as the line frequency; their

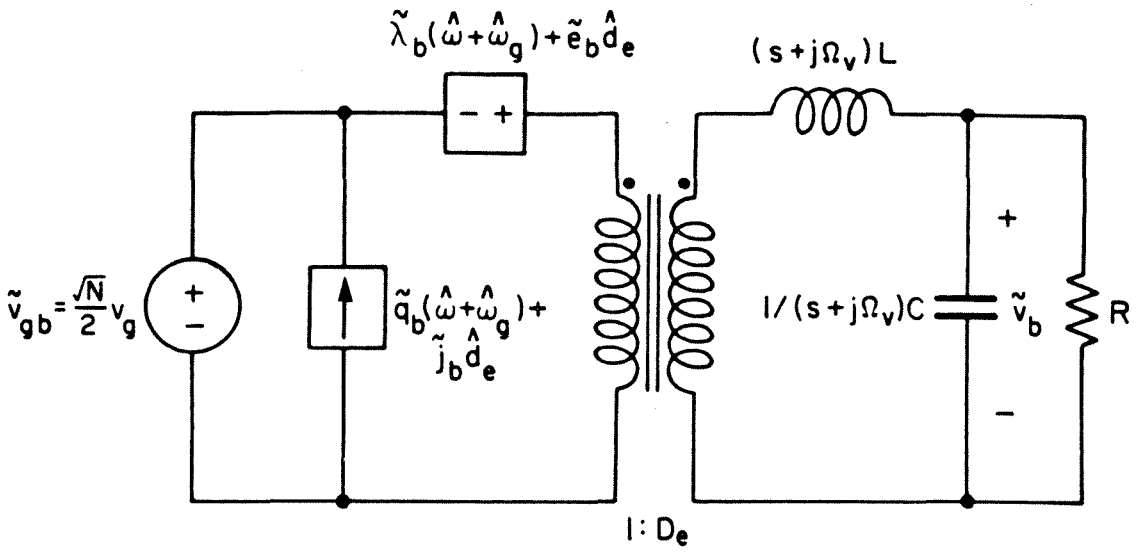


Fig. 9.9 Linearized, continuous, and time-invariant model of the buck cycloconverter showing excitation and control generators, a cycloconversion transformer, and a complex low-pass filter.

coefficients are

$$\tilde{e}_b = \frac{\tilde{V}_b}{D_e}, \quad \tilde{j}_b = -\tilde{I}_b, \quad \tilde{q}_b = -jD_e C\tilde{V}_b \tag{9.43a,b,c}$$

$$\tilde{\lambda}_b = -j\frac{L}{D_e}[\tilde{I}_b + (s+j\Omega_v)C\tilde{V}_b] \tag{9.43d}$$

The above coefficients help determining the zeros of control-to-output transfer functions.

The input signals are processed by an ideal transformer that parallels the switching process in the actual circuit. The *cycloconversion ratio* of the transformer is the *transformed duty ratio* D_e defined as

$$D_e = \frac{\sqrt{MN}}{2}\frac{D_m}{N} = \sqrt{\frac{M}{N}}\frac{D_m}{2} \tag{9.44}$$

This ratio emphasizes the *modulation amplitude* as the prime influence over steady-state and dynamic gains.

The secondary of the cycloconversion transformer drives a *complex filter* that represents the low-pass filter in the real converter. The real part of each complex reactance is the dynamic reactance while the imaginary part, the steady-state reactance. Note that the system is fourth-order even though only one L and one C appear in the model.

The canonical model for the boost cycloconverter can be derived by use of a current transformation of phase

$$\theta_{\mathcal{N}} = \int_0^t \omega_g(\tau)\, d\tau \tag{9.45a}$$

and a voltage transformation of phase

$$\theta_{\mathcal{V}} = \int_0^t [\, \omega_g(\tau) + \omega'(\tau)\,]\, d\tau \tag{9.45b}$$

The resulting circuit comprises a forward and a backward half decoupled from each other thanks to the absence of rectification or inversion. The backward model is portrayed in Fig. 9.10 for $\varphi_g = 0$. It demonstrates the familiar input, cycloconversion, and filter functions. Control variables are still amplitudes and frequencies of the main and duty ratio modulations; coefficients of the dependent generators are

$$\tilde{e}'_b = (s + j\Omega_g)\frac{L}{D'_e}\tilde{I}_b - \tilde{V}_b \tag{9.46a}$$

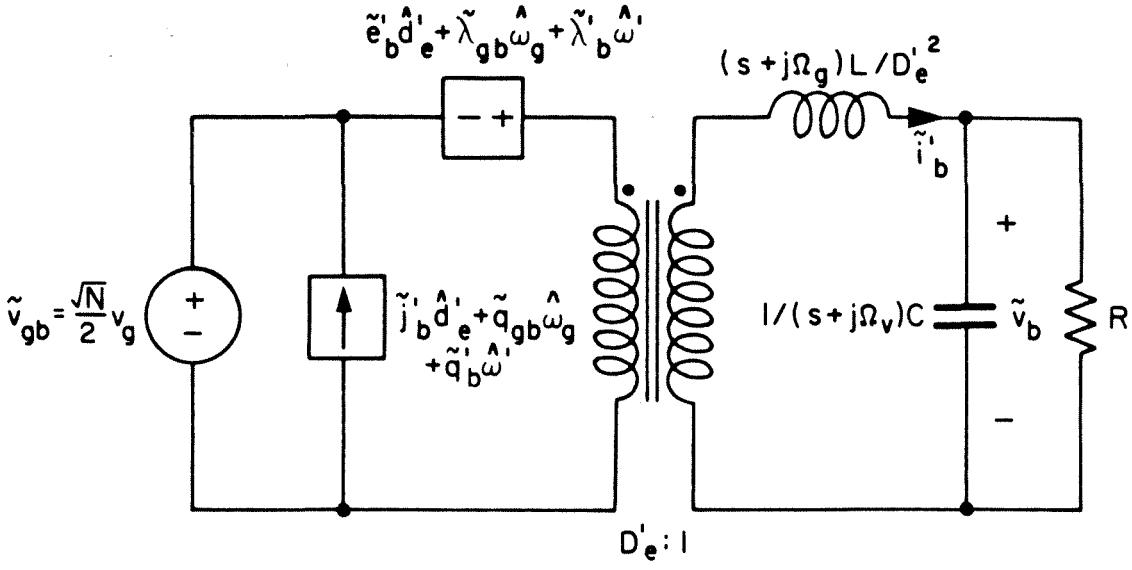


Fig. 9.10 Linearized, continuous, and time-invariant model of the boost cycloconverter showing excitation and control generators, a cycloconversion transformer, and a complex low-pass filter.

$$\tilde{\lambda}'_b = -j\frac{L}{D'_e}(s+j\Omega_g)C\tilde{V}_b \tag{9.46b}$$

$$\tilde{\lambda}_{gb} = -j\frac{L}{D'_e}[(s+j\Omega_g)C\tilde{V}_b + D'_e\tilde{I}_b] \tag{9.46c}$$

$$\tilde{j}'_b = \frac{\tilde{I}_b}{D'_e}, \quad \tilde{q}'_b = \tilde{q}_{gb} = -j\frac{C\tilde{V}_b}{D'_e} \tag{9.46d,e}$$

The *cycloconversion ratio* the switches impose upon the inputs is inversely proportional to the *transformed duty ratio* D'_e defined as

$$D'_e = \frac{\sqrt{MN}}{2}\frac{D'_m}{M} = \sqrt{\frac{N}{M}}\frac{D'_m}{2} \tag{9.47}$$

Boosting function is transparent.

Fourth-order low-pass filtering is embodied in the complex LC filter following the cycloconversion transformer. Note that while the real frequency is s for both reactances, the imaginary one is Ω_g for L and Ω_v for C. The inductor current in the model is related to that in the actual circuit by

$$\tilde{\imath}_b' = D_e'\tilde{\imath}_b + \tilde{I}_b\hat{d}_e' - jC\tilde{V}_b(\hat{\omega}_g + \hat{\omega}') \tag{9.48}$$

Note that $\frac{L}{D_e'^2}$ is also the *steady-state* inductance, not just the dynamic one as in a boost dc converter. At low modulation amplitude, this inductance opens up as $D_e'^2$ while the cycloconversion gain increases only as D_e'; therefore, the output tends toward zero instead of infinity as the modulation depth vanishes. The loss of boosting property, as well as poor steady-state and dynamic bandwidths, discourages operation at small d_m'.

For the flyback and buck-boost cycloconverters, only one sub-transformation is required for the capacitor voltages; this transformation tracks the phase of the output duty ratio modulation:

$$\theta_{TV} = \int_0^t \omega'(\tau)\, d\tau \tag{9.49}$$

The resulting model is delineated in Fig. 9.11. Now backward and forward phasors interact at the input port to rectify complex into real voltage and at the output port to invert real into complex currents. The forces behind the control generators are the line amplitude and modulation amplitude and frequency. Coefficients of the dependent generators can be proved to be

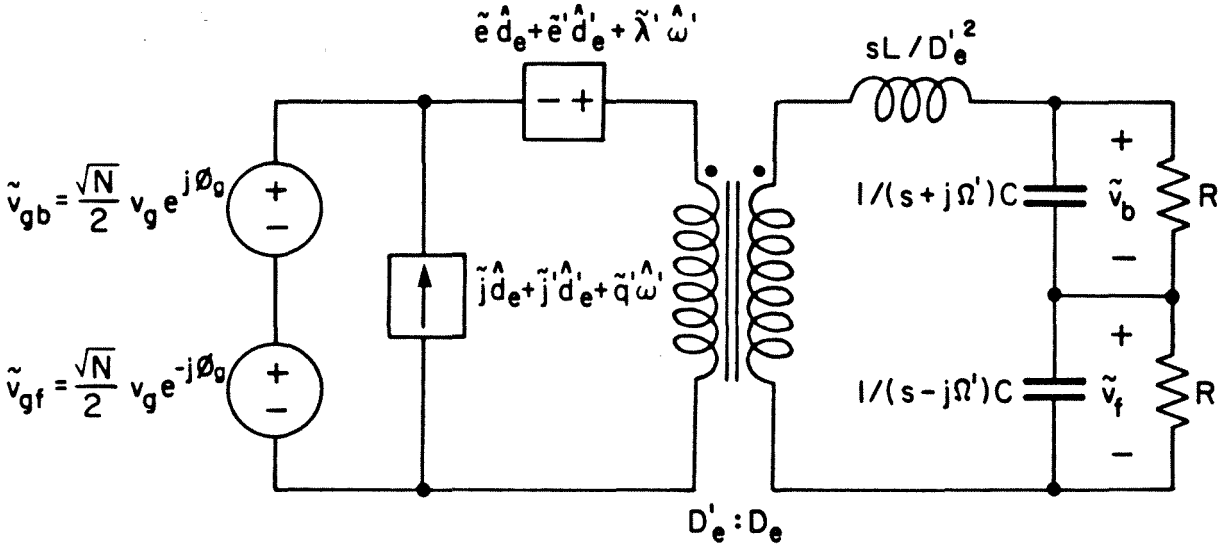


Fig. 9.11 Linearized, continuous, and time-invariant model of the buck-boost and flyback cycloconverters showing excitation and control generators, a cycloconversion transformer, and a complex low-pass filter.

$$\tilde{e} = \frac{\sqrt{N}V_g\cos\Phi_g}{D_e}, \qquad \tilde{e}' = \frac{D'_e}{D_e}sL_e I - \frac{\sqrt{N}V_g\cos\Phi_g}{D'_e} \tag{9.50a,b}$$

$$L_e = \frac{L}{D'^2_e}, \quad \tilde{\lambda}' = -jRC\left[\frac{\sqrt{N}V_g\cos\Phi_g}{1+(s-j\Omega')RC} + \frac{D'_e}{D_e}\tilde{V}_b\frac{sL_e}{R}\right] \tag{9.50c,d}$$

$$\tilde{j} = -I, \quad \tilde{j}' = \frac{D_e}{D'_e}I, \quad \text{and} \quad \tilde{q}' = -j\frac{D_e}{D'_e}C\tilde{V}_b \tag{9.50e}$$

Input and output *transformed duty ratios* are defined according to

$$D_e = \frac{\sqrt{N}}{2}\frac{2D_m}{N} = \frac{D_m}{\sqrt{N}} \quad \text{and} \quad D'_e = \frac{D'_m}{\sqrt{M}} \tag{9.51a,b}$$

Their ratio is the *cycloconversion ratio*, which provides the steady-state and

small-signal gain across the switches.

The low-pass LC network in the physical circuit is encompassed in the *third-order complex filter* in the model. Model states are related to actual ones by

$$\tilde{i} = D_e' i + I \hat{d}_e' - jC\tilde{V}_b \hat{\omega}' \tag{9.52a}$$

$$\tilde{v}_f' = \tilde{v}_f - j \frac{D_e}{D_e'} \sqrt{N} V_g \cos\Phi_g \frac{RC\hat{\omega}'}{1 + (s - j\Omega')RC} \tag{9.52b}$$

Since $\frac{L}{D_e'^2}$ does not affect the steady-state inductive reactance, which is zero, the converter still boosts at low modulation amplitude. Dynamic bandwidths, however, are degraded at high gain.

To review, *continuous, time-invariant* circuits have been developed in the ofb reference frame to model switched, time-varying cycloconverters. The models are *canonical* in the sense they all contain *control* and *excitation generators*, a *cycloconversion transformer*, and a *complex low-pass filter*. Backward and forward components are *decoupled* in the buck and boost cycloconverters, in which energy conversion is *direct*; they *interact* in the buck-boost and flyback topologies, in which power is converted *indirectly* through a dc link.

9.4 Reduction of Cycloconverters to Dc Converters, Inverters, and Rectifiers

Reflection upon the extensions of fast-switching PWM dc converters (Appendix A) into inverters (Chapter 3), rectifiers (Chapter 6), and cycloconverters (Chapter 9) reveals many common characteristics among

these four kinds of converters. For one thing, the topologies are *ideal*: all their waveforms are either *dc* or *sinusoidal*. Thanks to this ideality, the circuits can be represented by *similar* continuous, time-invariant *canonical models* in the *same ofb frame of reference*.

Three common groups of elements are shared by all models: *excitation* and *control generators*, *conversion transformer*, and *low-pass filters*. True inputs, amid all time variations, are the dc source and duty ratios and the amplitudes and frequencies of ac sources and duty ratio modulations. The conversion ratio is related to duty ratio controls of the switches and is descriptive of converter type, e.g., all buck converters step down, boost converters step up, and so on. Steady-state and small-signal bandwidths are determined by complex reactances that have analogous meanings for all areas of switched-mode conversion.

The above similarities inevitably suggest that dc converter, inverter, rectifier, and cycloconverter topologies of the same type (e.g., flyback) may be consolidated. Since dc is just a special case of balanced polyphase ac, it is logical to expect dc converter, inverter, and rectifier are just special cases of cycloconverter. That the cycloconverter is the most generalized structure is proved below for the buck-boost topology.

A buck-boost dc converter is derived from the four-phase buck-boost cycloconverter in Fig. 9.12. The input v_g to the dc converter is equivalent to the following set of four-phase, dc excitations:

$$v_{g1} = -v_{g3} = \frac{v_g}{2} \quad \text{and} \quad v_{g2} = v_{g4} = 0 \qquad (9.53a,b)$$

The above assignment effectively removes v_{g2} and v_{g4} from the picture and

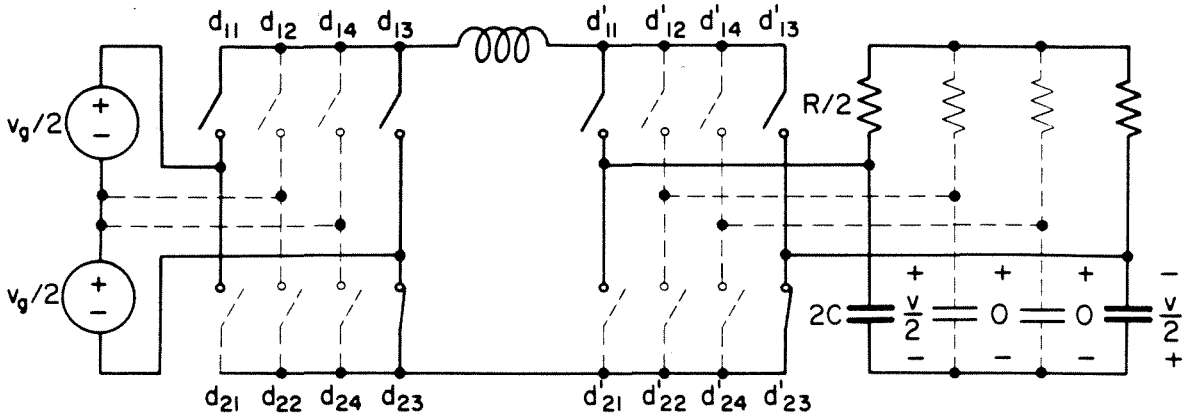


Fig. 9.12 Reduction of a four-phase buck-boost cycloconverter with dc inputs and outputs to a buck-boost dc converter.

places v_{g1} and v_{g3} in series. The four throws related to v_{g2} and v_{g4} are then redundant; hence, the input duty ratios are distributed as

$$d_{11} = 1 - d_{13} = d \quad \text{and} \quad d_{23} = 1 \tag{9.54a,b}$$

The upper switch thus retains only two throws that feed v_{g1}, the positive end of v_g, and v_{g3}, the negative end of v_g; the lower switch is eliminated by being permanently connected to v_{g3}. The overall result is the *input end of a buck-boost dc converter*, as is emphasized by the thick trace. It is important to realize that Eq. (9.54) still creates a set of four-phase, dc *effective duty ratios* $d_k = d_{1k} - d_{2k}$:

$$d_1 = -d_3 = d \quad \text{and} \quad d_2 = d_4 = 0 \tag{9.55a,b}$$

Therefore, the reduced switch arrangement and duty ratio assignment in the dc converter still "cycloconvert" implicitly.

By the same token, the top output switch is simplified into a double-throw one, and the bottom output switch discarded by

$$d'_{11} = 1 - d'_{13} = d' \quad \text{and} \quad d'_{23} = 1 \tag{9.56a,b}$$

Again, these functions still generate four-phase, dc effective duty ratios although the thick line in Fig. 9.12 shows that the output end is exactly that of a boost dc converter. Therefore, the output voltages are also four-phase dc:

$$v_1 = -v_3 = \frac{v}{2} \quad \text{and} \quad v_2 = v_4 = 0 \tag{9.57a,b}$$

Two phases of the load carry no current while the other two are effectively in series. The four-phase, dc output obviously has become a single-phase, dc one with effective load R and capacitance C supported by v. The buck-boost cycloconverter has thus been reduced to a buck-boost dc converter.

An M-phase buck-boost inverter can be developed from a four-M-phase buck-boost cycloconverter by use of the switch topology at the input of Fig. 9.12 and the corresponding specifications in Eqs. (9.53) and (9.54). Likewise, an N-phase buck-boost rectifier can be obtained from an N-four-phase buck-boost cycloconverter by following the output arrangement in Fig. 9.12 and functions in Eqs. (9.56) and (9.57). In general, the procedure applies to the buck, boost, flyback, and other topological types as well.

In conclusion, the *buck*, *boost*, *buck-boost*, and flyback cycloconverters have been described as examples of topologies capable of generating *sinusoidal* waveforms from fast-switching, *sinusoidal pulse-width*

modulation. *Steady-state* and *canonical models* are analyzed with particular emphasis on the *cycloconversion function* of switches and the *frequency responses* of nonzero filter reactances. Steady-state output frequency starts from dc and can go *very high* if the converter switches fast enough; both phase sequences are possible. Dynamic bandwidth is *wide* since fast switching implies small energy-storage elements.

In view of the *similarities in performance and models* of dc converters, inverters, rectifiers, and cycloconverters, it has been stated that four areas of switched-mode energy processing are also *topologically related*. In particular, a dc converter, inverter, or rectifier of a given type (e.g., buck-boost) is demonstrated to be just a special case of the corresponding cycloconverter. Therefore, the *cycloconverter* is established as the *generalized converter* whose topology and model are representative of all fields of dc and ac power conversion.

CHAPTER 10

PRACTICAL ASPECTS OF FAST-SWITCHING SINUSOIDAL PWM CYCLOCONVERTERS

This chapter comprises four sections. *Switches* of the topologies considered in the previous chapter are implemented and their drives discussed in the first section. *Isolation* is incorporated by insertion of transformer and, possibly, additional switches in the second section. *Input impedances* of cycloconverters are calculated and *switched-mode impedance converters* promoted in the third section. An *experimental flyback cycloconverter* is built and tested in the final section.

10.1 Three-Phase Implementation

Three topics are examined in this section. The first is the connection of *transistors and diodes* in place of ideal switches and the specification of *stress* for these devices in practical designs. Some *modulation principles* for the switches are discussed next for forward power conversion. Issues in *bidirectional power flow* are studied in the last part.

10.1.1 Switch Realization and Stress

The switches in a buck (Fig. 9.1) or boost (Fig. 9.3) cycloconverter are *four-quadrant*: they carry *ac currents* and block *ac voltages*. One way to implement each throw of such a switch encases one transistor in a bridge made from four diodes, as is illustrated in Fig. 10.1a. The transistor

provides active control, i.e., determines when the throw is on or off. The diodes rectify the ac current or voltage before passing it to the transistor. A three-phase buck or boost cycloconverter requires nine transistors and thirty six diodes if bridged-transistors are used.

The configuration in Fig. 10.1b realizes a four-quadrant throw by anti-paralleling two voltage-two-quadrant throws, each being realized by a transistor and diode in series, or anti-cascading two current-two-quadrant throws, each being realized by a transistor and diode in anti-parallel. During the on state, both transistors are activated; the one that conducts, together with the series diode, is picked by current polarity. During the off state, the diode protects its anti-parallel transistor from negative bias. A three-phase buck or boost cycloconverter requires eighteen transistors and eighteen diodes if blocks like Fig. 10.1b are used.

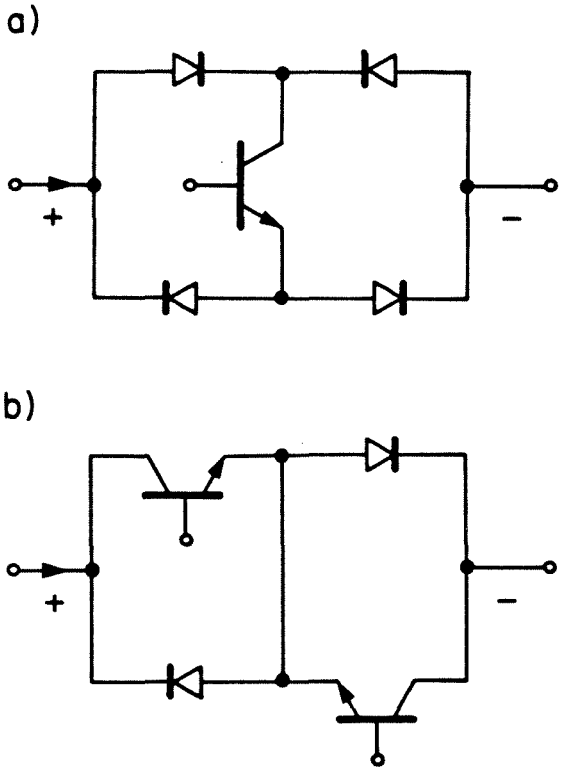


Fig. 10.1 Realization of a four-quadrant throw with (a) one transistor and four diodes and (b) two transistors and two diodes.

Neither circuit in Fig. 10.1 satisfies the requirement of *perfect* commutation in four-quadrant switching. As is obvious from Fig. 10.2 for two throws in a buck cycloconverter, the transistors cannot be simultaneously on to avoid shorting out the line. This non-overlapping restriction is fulfilled with current-two-quadrant throws by allowance of some dead time sufficiently longer than the storage time of active devices. This dead time, however, is not permitted in Fig. 10.2 since no diode free-wheels the inductor current while both transistors are off. More elaborate switch realization is thus essential for the buck or boost cycloconverter to be useful.

Current stress in the transistor or diode in a buck or boost topology is evidently at least the amplitude of the inductor current (Table 9.1). Voltage stress is the peak line voltage of either the input line, for the

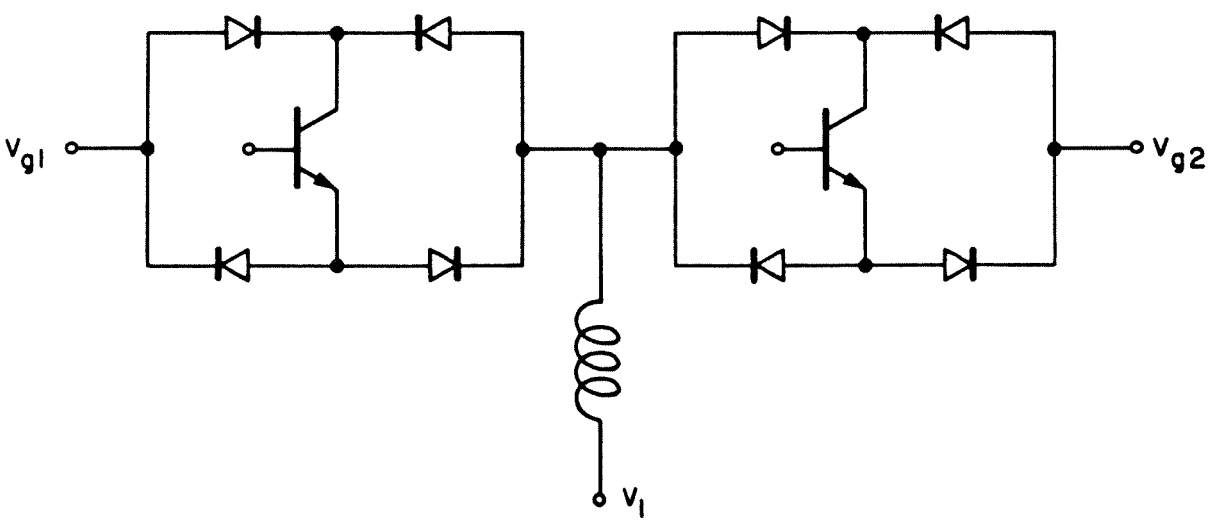


Fig. 10.2 Two bidirectional throws in a buck cycloconverter.

buck, or output line, for the boost converter. Voltage stress is tabulated in Table 10.1, where the output phase voltage is specified in Table 9.1.

The dc link in a buck-boost or flyback cycloconverter makes the current through the switches *dc*. Therefore, the throw is voltage-two-quadrant and built by connection of a transistor and diode in series; a three-phase buck-boost converter with real switches is portrayed in Fig. 10.3. The switch topology here is famous for its ruggedness and protection simplicity. Although no dead time is permitted, any number of throws belonging to one switch may overlap without any destruction. The flyback cycloconverter shares a similar switch arrangement.

The current flowing through a transistor or diode in a buck-boost or flyback cycloconverter is at least the inductor current. The voltage stress is the peak line voltage, as is summarized in Table 10.1.

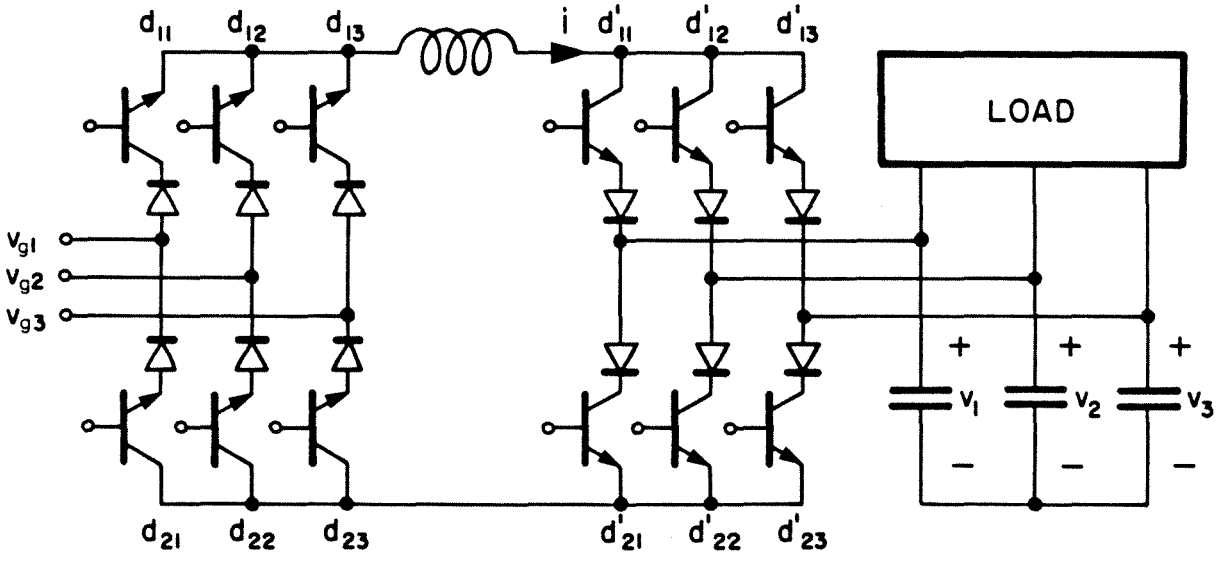


Fig. 10.3 Three-phase, four-quadrant realization of a buck-boost cycloconverter.

Cycloconverter	Input transistor/diode	Output transistor/diode
Buck	$\sqrt{3}\,V_g$	
Boost		$\sqrt{3}\,V$
Flyback	$\sqrt{3}\,V_g$	$\sqrt{3}\,V$

TABLE 10.1 Voltage stresses across the transistors and diodes of the buck, boost, and flyback (or buck-boost) cycloconverters.

In summary, the throw in a buck or boost cycloconverter is four-quadrant and realized by a bridged-transistor or two pairs of anti-parallel transistor and diode in anti-series. Drives for both configurations are difficult because neither dead nor overlapping time is allowed. The throw in a buck-boost or flyback topology is voltage-two-quadrant and implemented by cascade of a transistor and diode. The resulting switch arrangement is easy to drive and rugged. Current stress of the device is the peak inductor current, and voltage stress the peak line voltage.

10.1.2 Modulation Strategies

It has been proved that low-frequency components in the outputs of fast-switching cycloconverters with slow PWM depend on only *duty ratios*. Since a given duty ratio may be synthesized by a variety of switching functions, modulation strategies are numerous and flexible. For the buck or boost topology, a policy that simplifies signal-processing circuitry has been proposed in [37]. Only three switching functions are used for all nine throws:

$$d_{11}^{*} = d_{23}^{*} = d_{32}^{*} \tag{10.1a}$$

$$d_{12}^{*} = d_{21}^{*} = d_{33}^{*} \tag{10.1b}$$

$$d_{13}^{*} = d_{22}^{*} = d_{31}^{*} \tag{10.1c}$$

Their duty ratios are

$$d_{11} = d_{23} = d_{32} = \frac{1}{3} + \frac{d_m}{3}\cos\theta \tag{10.2a}$$

$$d_{12} = d_{21} = d_{33} = \frac{1}{3} + \frac{d_m}{3}\cos\left(\theta - \frac{2\pi}{3}\right) \tag{10.2b}$$

$$d_{13} = d_{22} = d_{31} = \frac{1}{3} + \frac{d_m}{3}\cos\left(\theta + \frac{2\pi}{3}\right) \tag{10.2c}$$

The switching diagram for such a drive scheme is delineated in Fig. 10.4. Note that the switching functions specified by Eqs. (10.1a) and (10.2a) are referenced to the bottom horizontal axis while those specified by Eqs. (10.1c) and (10.2c) the top one; the distance between the two sine waves is related to Eqs. (10.1b) and (10.2b). Three digits are used to designate a switched

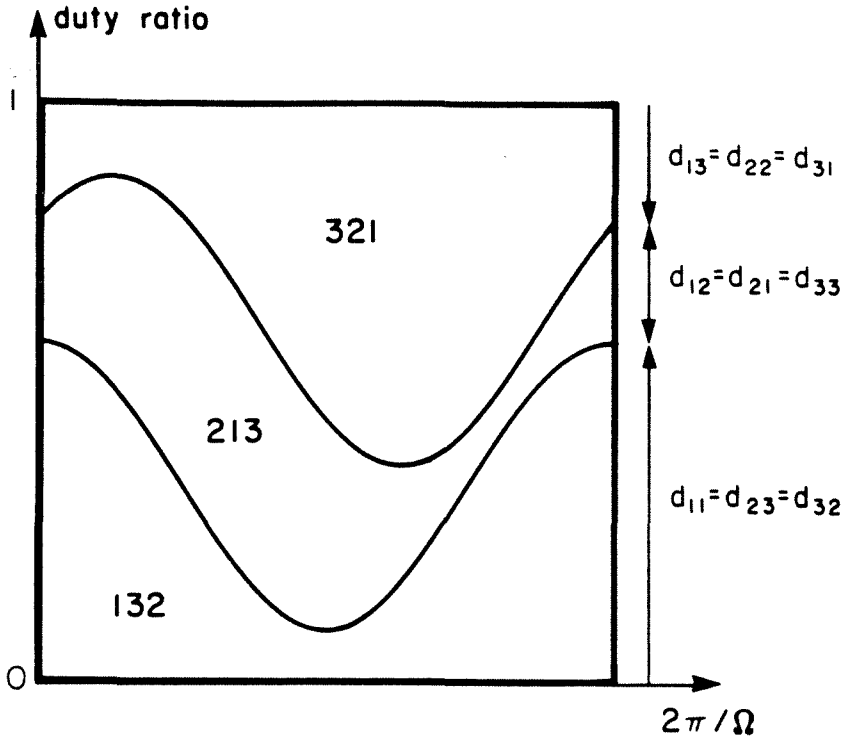


Fig. 10.4 Switching diagram for the buck cycloconverter.

topology since there are three switches. Each takes on three values as there are three throws or input sources. Thus, only three switched topologies exist over the entire modulation cycle. In the one below the lower sine curve, for instance, inductor 1 is at v_{g1}; inductor 2, v_{g3}; and inductor 3, v_{g2}.

If the phase sequence of the sources is also positive as that of the duty ratio modulations in Eq. (10.2), the output is at frequency $\omega_v = \omega_g - \omega$ with negative phase sequence if $\omega_g > \omega$, and at $\omega_v = \omega - \omega_g$ with positive phase sequence if $\omega > \omega_g$. Any $\omega_v > 0$ with positive phase sequence or $0 < \omega_v < \omega_g$ with negative phase sequence is thus possible from $\omega > 0$. The $\omega_v > \omega_g$ with negative phase sequence is available if $\omega < 0$ or $\omega > 0$ with negative phase

sequence. Reversal of phase sequence at any frequency can thus be achieved smoothly by straightforward electronics.

The input switches of a buck-boost or flyback cycloconverter are driven as those of the corresponding rectifier, and the output switches those of the inverter. Modulation can be either continuous or six-stepped PWM. If continuous PWM is used, amplitudes and phases of the four switches are completely independent. In any case, the frequency and phase sequence of the input switches must lock to those of the source. The frequency and phase sequence of the output switches then determine those of the load. Reversal of phase sequence here is even simpler than that of the buck and boost cycloconverters.

10.1.3 Bidirectionality of Power Flow

Since switches in all topologies are already *four-quadrant*, reversal of power flow can be executed *electronically* without topological modification. If the output voltage of a buck cycloconverter keeps the same polarity, the inductor current has to change direction during regeneration. The modulation amplitude needs be adjusted, usually by a feedback loop if both sources are stiff, so that the effective voltage across the inductor drives current backward. If the output voltage flips sign, the current does not have to. The phase of duty ratio modulation then needs be delayed by 180° so that the source current reverses. The transition time in this case depends on the capacitors while that in the other the inductors.

The foregoing consideration applies to a boost cycloconverter as well. The only difference is that the inductor currents always reverse no matter what happens at the output.

In the buck-boost or flyback topology, the inductor current maintains the *same* direction for both forward and backward energy transfers. Therefore, the duty ratio modulation of the input switches always changes sign in going from one mode to the other. The output duty ratio has to do the same unless the phases of output voltages are already delayed by 180°. Regeneration can be accomplished in one switching period since only control signal is involved.

In review, reversal of power flow is natural in cycloconverters as their switch implementations are *four-quadrant*. Only the *phase* or *amplitude* of duty ratio modulation needs be adjusted *electronically*. The phase variation delays the phase of *either* voltage *or* current by 180° during regeneration. Amplitude control is essential if voltage sources are connected to both input and output terminals.

10.2 Isolation

As is depicted in Fig. 10.5, splitting the inductor into two coupled windings on one magnetic path isolates the flyback cycloconverter. Note that the top six transistors, as well as the bottom six, actually belong to *one* switch although they are physically separated. In dT_s of each switching cycle, six transistors on the primary side charge up the inductor by Eq. (9.30). The other six then discharge the stored energy into the load by Eq. (9.34) during the remainder of the cycle.

The dual of the flyback topology is the *isolated boost-buck cycloconverter* described in Fig. 10.6. Its inductors function both as filters, to smooth out the input and output currents, and topological elements, to charge and discharge the intermediate capacitors. The capacitors prevent dc

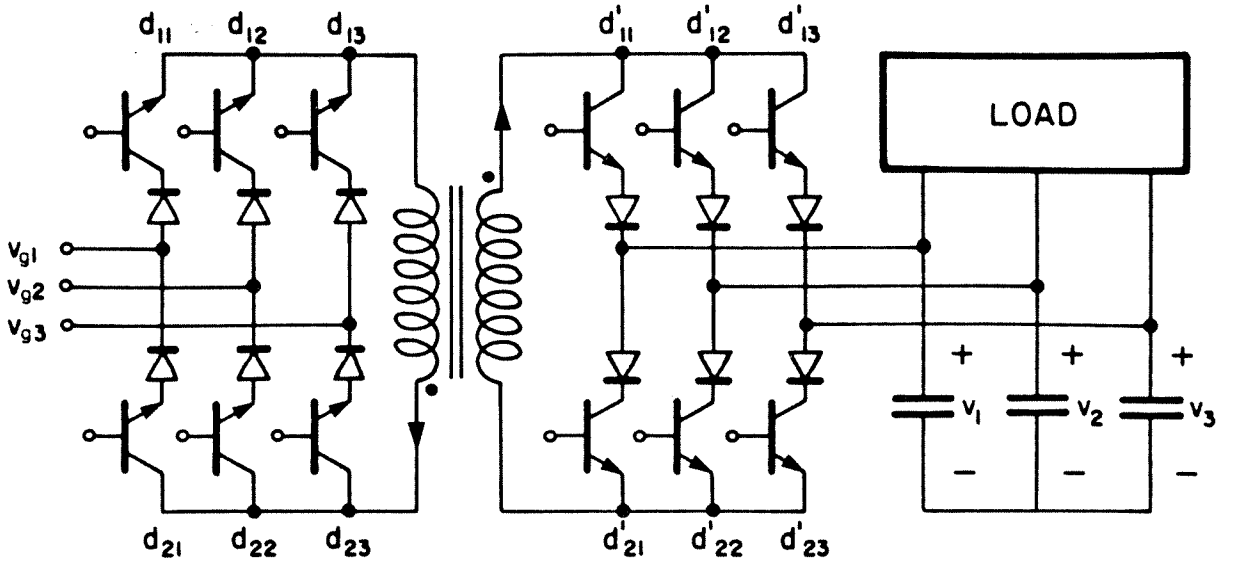


Fig. 10.5 Three-phase, four-quadrant flyback cycloconverter with isolation.

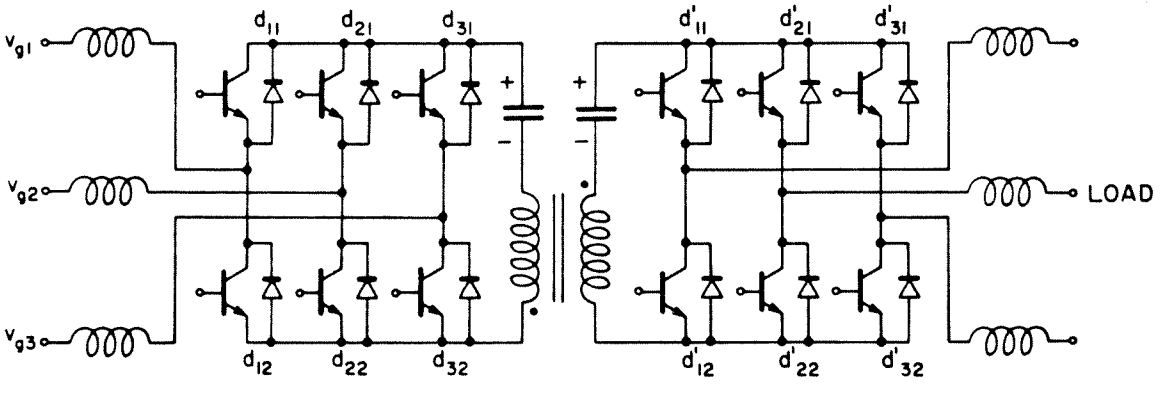


Fig. 10.6 Boost-buck cycloconverter, cascade of a boost rectifier and a buck inverter, with isolation as in the Ćuk dc converter.

current from saturating the isolation transformer.

Operations of the switches in Figs. 10.5 and 10.6 are analogous. In dT_s, all input throws are activated to charge up the input inductors and place the capacitors in series. The output throws transfer the capacitive energy into the load by

$$d'_{w1} = \frac{d}{2} + \frac{d'_m}{2} \cos\left[\theta' - (w-1)\frac{2\pi}{3}\right] \qquad (10.3)$$

where

$$1 \le w \le 3 \ , \quad d'_m \le d \ , \quad \text{and} \quad \theta' = \int_0^t \omega'(\tau)\, d\tau \qquad (10.4a,b,c)$$

During the rest of the period, the output switches are all on to put the capacitors in series again. The input switches now replenish the capacitors by

$$d_{k1} = \frac{d'}{2} + \frac{d_m}{2} \cos\left[\theta - (k-1)\frac{2\pi}{3}\right] \qquad (10.5)$$

where

$$1 \le k \le 3 \ , \quad d_m \le d' \ , \quad \text{and} \quad \theta = \int_0^t \omega_g(\tau)\, d\tau \qquad (10.6a,b,c)$$

As in the flyback case, the input modulation frequency and phase sequence follow those of the sources; the output ones determine those of the load.

It is important to realize that a *three-phase* source is isolated from a *three-phase* load in Figs. 10.5 and 10.6 with only *two* windings and *no* additional switches. This simplification is possible because a *dc link* is present and isolation is inserted *at this link*, which is *single-phase*. A three-

phase transformer, with more than three windings, and many extra switches would be required if isolation were done right after the sources. Therefore, the component count is significantly reduced in the isolated *direct*, such as buck or boost, cycloconverters by *integration of the isolation transformer into a dc link*.

10.3 Fast-Switching Impedance Converters

The *input impedance* of a cycloconverter is the ratio of the input voltage phasor to the input current phasor; it can be computed in either abc or ofb frame of reference:

$$\tilde{Z}_i = \frac{\tilde{V}_{gb}}{\tilde{I}_{gb}} \tag{10.7}$$

This impedance is generally a function of not only the load, but also the *duty ratio controls*. Therefore, the load can be presented differently to the source, and a cycloconverter is a *switched-mode impedance converter*, although some topologies are better candidates than others.

From the canonical model in Fig. 9.9, $\tilde{Z}_i$ for a buck cycloconverter driving a *general* impedance $\tilde{Z}_l$, per-phase impedance of some arbitrary load, is

$$\tilde{Z}_i = \frac{1}{D_e{}^2}\left(j\Omega_v L + \frac{1}{j\Omega_v C} // \tilde{Z}_l\right) \tag{10.8}$$

which reduces to the following for a resistive load:

$$\tilde{Z}_i = \frac{N}{M}\frac{4}{D_m{}^2}\frac{1 + j\Omega_v L/R + (j\Omega_v)^2 LC}{1 + j\Omega_v RC} R \tag{10.9}$$

If $-\Omega_v$ substitutes Ω_v in the above, $\tilde{Z}_i$ becomes its complex conjugate. Therefore, the sign of reactive power may be changed at will via the sign of Ω_v, controlled ultimately by the frequency and phase sequence of duty ratio modulation. An *inductive* load then may appear *capacitive* to the main, and vice versa.

Unfortunately, the buck topology pulse-width-modulated by Eq. (9.1) leaves no freedom for *power factor* control, as is transparent from Eq. (10.8). The authors in [37] have modulated the duty ratios by two sinusoids at different frequencies and opposite phase sequences to regain some power factor correction; one frequency is $\omega_g + \omega_v$ and the other $\omega_g - \omega_v$. The input power angle can then be varied between plus and minus of that determined by Eq. (10.8), essentially the load angle if filter impedances are negligible. The demand for two frequencies locked symmetrically around the line frequency, however, requires complex circuitry and is justified only when the load power factor is poor. If the load is highly resistive, only a small range of power factor close to unity is presented to the line, even with this involved strategy.

From the model in Fig. 9.10, the input impedance of a boost cycloconverter feeding an impedance $\tilde{Z}_l$ is

$$\tilde{Z}_i = j\,\Omega_g\,L + D_e'^2\,\frac{1}{j\,\Omega_v\,C}\,//\,\tilde{Z}_l(\Omega_v) \tag{10.10}$$

where $\tilde{Z}_l$ is evaluated at Ω_v. It is the sum of the inductive reactance and the output impedance reflected to the input side. As the modulation amplitude approaches zero, the line sees only L as expected; this is in contrast to the buck case, in which no modulation implies infinite $\tilde{Z}_i$. If

$\tilde{Z}_l = R$, Eq. (10.10) reduces to

$$\tilde{Z}_i = D_e'^2 R \frac{1 + j\Omega_g L/(D_e'^2 R) - \Omega_v \Omega_g LC/D_e'^2}{1 + j\Omega_v RC} \tag{10.11}$$

As in a buck cycloconverter, power factor control is limited. The sign of reactive power responds to that of Ω_v only when $j\Omega_g L$ in Eq. (10.10) is negligible compared to the reflected Ω_v-impedance.

The $\tilde{Z}_i$ for a buck-boost or flyback cycloconverter driving a general load can be obtained from Fig. 9.11 as

$$\tilde{Z}_i = \frac{N}{M}\left[\frac{D_m'}{D_m}\right]^2 \frac{Z_m \cos\Phi_z}{\cos\Phi_g} e^{j\Phi_g} \tag{10.12}$$

where Φ_g is the angle by which the duty ratio modulation lags the input phase voltage; Z_m and Φ_z satisfy

$$Z_m e^{j\Phi_z} = \frac{1}{j\Omega_v C} // \tilde{Z}_l(\Omega_v) \tag{10.13}$$

For a resistive load, the above becomes

$$\tilde{Z}_i = \frac{N}{M}\left[\frac{D_m'}{D_m}\right]^2 \frac{R}{1 + (\Omega_v RC)^2} \frac{e^{j\Phi_g}}{\cos\Phi_g} \tag{10.14}$$

Clearly, the power angle is identical to the phase Φ_g between the line and duty ratio modulation. Since Φ_g is freely adjustable between 0° and 360°, *any* lagging or leading power factor is possible for *any* load. The amplitude of $\tilde{Z}_i$ can be assigned any value through D_m' and D_m; this flexibility is not offered by the buck and boost cycloconverters. A switched-mode resistor is synthesized, regardless of the actual load, by letting Φ_g be zero; a capacitor, Φ_g slightly above $-90°$; and an inductor, Φ_g slightly

below 90°. Energy-storage elements are slightly lossy because of parasitics in practical circuits.

In retrospect, an inductive can be switched into a capacitive load, and vice versa, by fast-switching cycloconverters. Only the *flyback* and *buck-boost* topologies offer a *complete range of power factor*, from zero to one, leading or lagging, thanks to their dc link. Useful synthesized elements include a resistor, for unity power factor requirement, a capacitor, and an inductor, for reactive power generation, of any amplitude.

10.4 Experimental Flyback Cycloconverter

A low-power flyback cycloconverter has been built to check the steady-state waveforms. The essential elements of the circuit are described in Fig. 10.7, Fig. 4.16 and its mirror image about the inductor. The signal-processing circuitry to drive the transistors is similar to that explained earlier for the experimental flyback inverter (Subsection 4.4.1).

The output throws are controlled by a block diagram like Fig. 4.12 without the input switching function d^*. The same hardware is then duplicated to drive *six* input throws. The whole system permits independent adjustment of input and output modulation frequencies, both ranging from dc to 250 Hz, and amplitudes.

Although the switching frequency is stated as 20 kHz, the *ramp* to the pulse-width modulator actually runs at 40 kHz. Every two ramp cycles thus make up one switching cycle; the input and output drives are then strobed on during alternate ramp period. This scheme simplifies circuitry by fixing d and d' at $\frac{1}{2}$. To reduce design complexity further, only duty

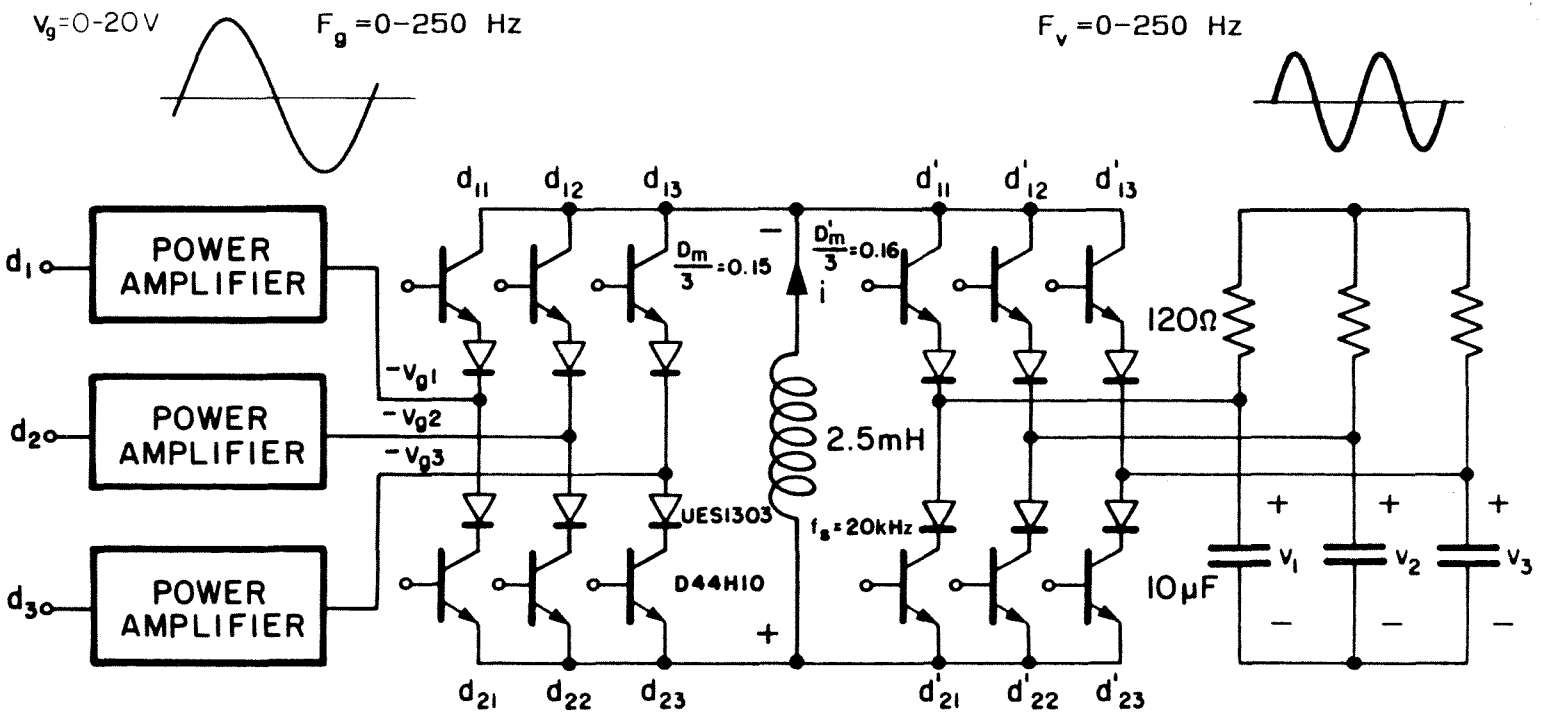


Fig. 10.7 Principal components of the experimental flyback cycloconverter.

ratios of the upper switch are modulated, and those of the other are purely dc. The resulting modulation strategy is certainly far from optimality; nevertheless, it demonstrates the drive flexibility in fast switching. The switching diagram for the transistors is depicted in Fig. 10.8 for $\Omega_v = \Omega' = 2\Omega_g$. According to the convention used before, "23" is the topology with pole 1 at source 2 and pole 2 at source 3; "1'2'", the one with pole 1 at output 1 and pole 2 at output 2.

Recall that to establish a dc current in the inductor, the input modulation frequency and phase must be those of the source voltages. This requirement is satisfied by simulation of the main by three-phase power amplifiers whose inputs are the duty ratio modulations themselves. The output frequency and phase sequence are determined, of course, by those of output duty ratio modulation.

Steady-state and switching waveforms are shown in Figs. 10.9 through 10.11. Capacitor voltages are displayed in Fig. 10.9 for $F_g = 100\,Hz$ and $F' = 200\,Hz$ to prove that stepping up of frequency is as natural and simple as stepping down. The waveforms look quite sinusoidal at the low power level considered.

Switching voltages at two ends of the inductor for different combinations of input and output frequencies are illustrated in Fig. 10.10. The cycloconverter performs as a *dc converter* in Fig. 10.10a where both input and output are dc. The duty ratios in the upper trace all equal $\frac{1}{6}$ as their modulation amplitude is zero. Those in the lower trace, although they are also dc, contain *dc sinusoidal* components. The cycloconverter functions as an *inverter* in Fig. 10.10b where the line is dc but the load is ac (at

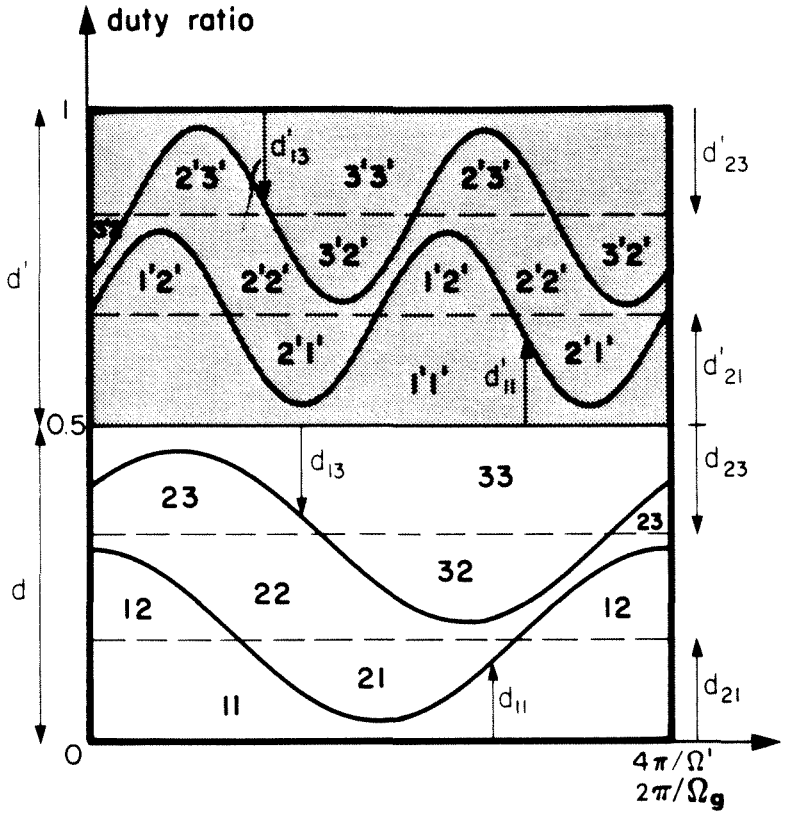


Fig. 10.8 Switching diagram of the flyback cycloconverter when $\Omega' = 2\Omega_g$.

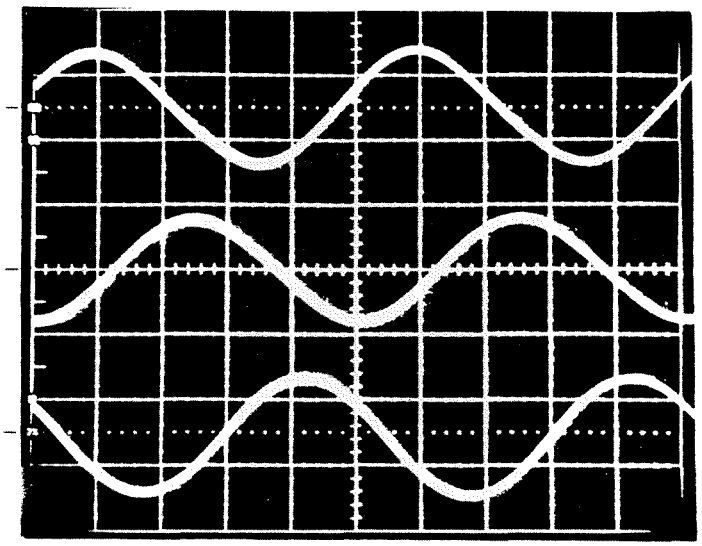
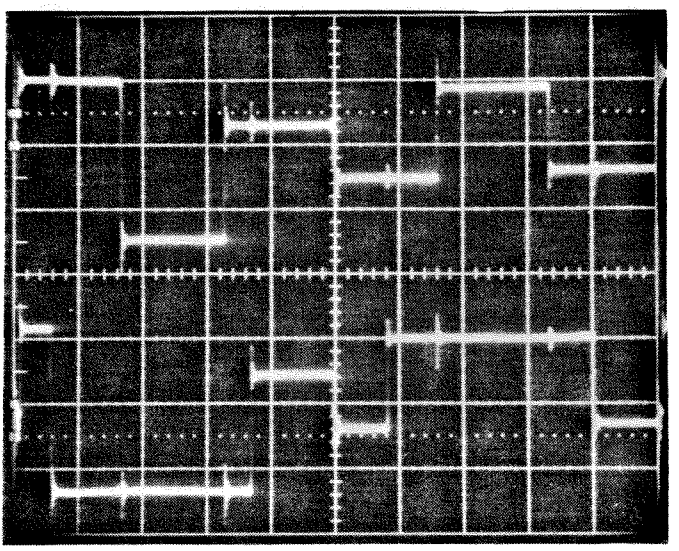


Fig. 10.9 v_1, v_2, *and* v_3 *(top to bottom) when* $F_g = 100\,Hz$, $V_g = 12.5\,V$, and $F' = 200\,Hz$. *Vertical scale: 10 V/div; horizontal scale: 1 ms/div.*

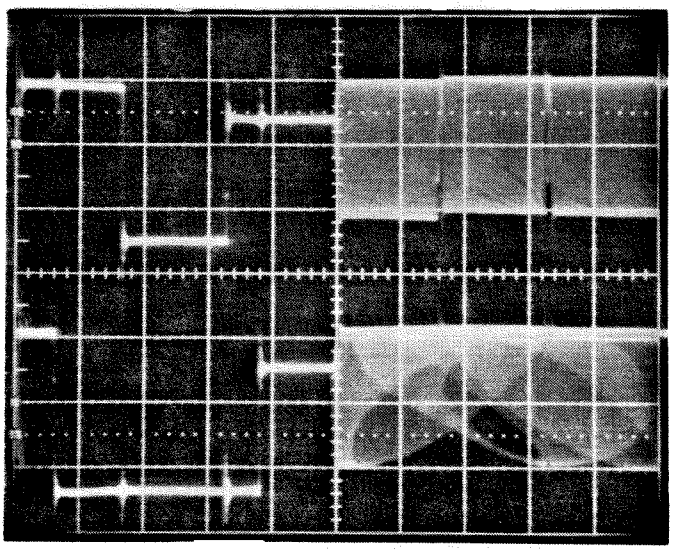
$100\,Hz$). In the absence of modulation, the transition points in the first trace simply move as functions of voltage during $d'T_s$ and plot out two vertical lines. Those in the second trace travel in both directions under influence of sinusoidal voltages (vertical) and duty ratios (horizontal) and generate four ellipses.

The cycloconverter operates as a *rectifier* in Fig. 10.10c where the input is at $200\,Hz$ while the output is dc. Vertical segments now appear in dT_s of the top waveform, and ellipses the bottom one. Finally, ac-to-ac is demonstrated in Fig. 10.10d for line frequency of $200\,Hz$ and load frequency of $100\,Hz$. Significance of the trajectories is obvious.

a)



b)



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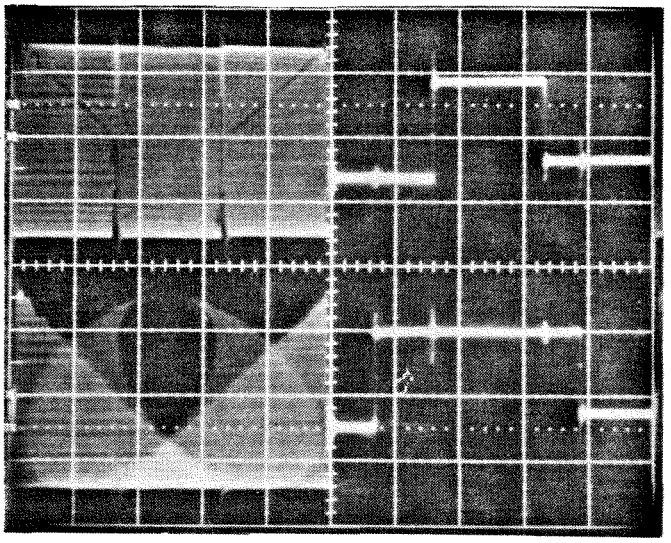


d)

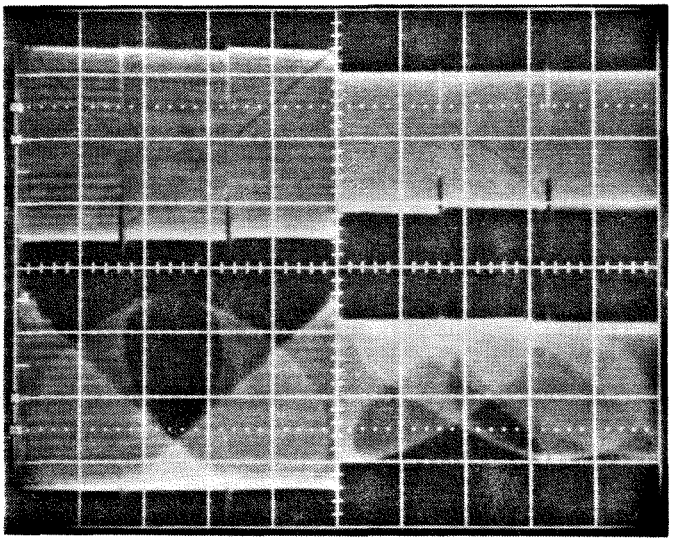


Fig. 10.10 Switching voltages at unmodulated (top) and modulated (bottom) ends of the inductor for V_g = 15 V when (a) F_g = F' = 0 Hz, (b) F_g = 0 Hz, F' = 100 Hz, (c) F_g = 200 Hz, F' = 0 Hz, and (d) F_g = 200 Hz, F' = 100 Hz. Vertical scale: 10 V/div; horizontal scale: 5 μs/div.

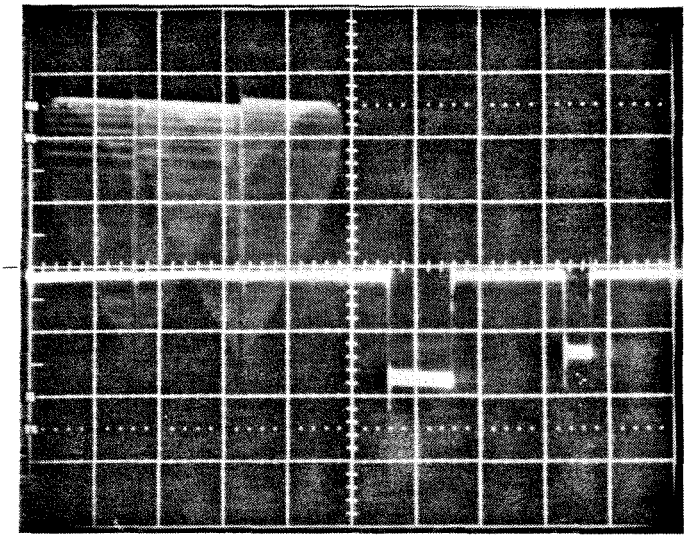
Switching voltages across the whole inductor are photographed in Fig. 10.11 for rectifier and cycloconverter operations. The dc voltage slightly above $-2\,V$ in Fig. 10.11a represents two transistor-diode drops during idling intervals. The dc voltage at $\approx -17\,V$ and $\approx -13\,V$ within $d'T_s$ are line voltages v_{12} and v_{32} (see Fig. 10.8). Each heart shape in dT_s is actually two halves of an ellipsoid, the second one being rectified at the transition line of the unmodulated switch by reversal of polarity of line voltage (refer to Fig. 10.8). The curves in Fig. 10.11b for cycloconversion are interpreted analogously.

Steady-state and dynamic frequency responses here are as reported in Figs. 4.18 and 4.21 through 4.24 for the flyback inverter.

In conclusion, this chapter has studied the implementation, isolation, input impedance, and verification of fast-switching sinusoidal PWM cycloconverters. It has been learnt that switches in direct, such as buck and boost, converters are *four-quadrant* and, hence, not only require a large amount of semiconductor devices, but also are difficult to drive. Switches in *indirect*, such as buck-boost and flyback, topologies, on the other hand, are only *two-quadrant*, implemented with fewer components, and controlled with ease. In both cases, *regeneration* is executed *electronically* without topological modification since the switch realization is already four-quadrant. Only the phase and amplitude of duty ratio modulation need be adjusted to reverse the flow of power.

Isolation demands fewer transformer windings and switching devices in *indirect* cycloconverters because it can be done right at the dc link, which is single-phase. The dc link also makes the buck-boost or flyback topologies ideal for *switched-mode impedance conversion*; an impedance of *any*

a)



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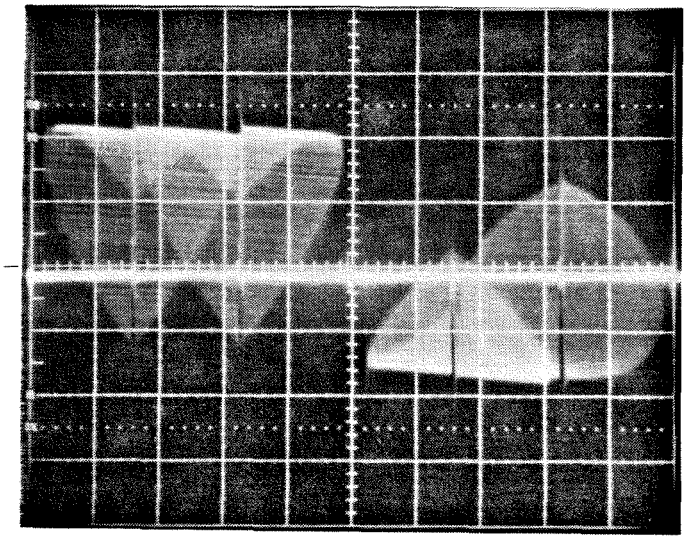

Fig. 10.11 Switching voltage across the inductor when (a) F_g = 250 Hz, F' = 0 Hz, V_g = 15 V and (b) F_g = 100 Hz, F' = 150 Hz, V_g = 13 V. Vertical scale: 10 V/div; horizontal scale: 5 μs/div.

amplitude and phase can be synthesized from any load.

Because of its interesting properties, a flyback cycloconverter has been built. The circuit generates *sinusoidal* outputs from sinusoidal inputs as expected. Stepping up line frequency is as easy as stepping it down; in fact, any combination of input and output frequencies between dc and 250 *Hz* (or higher for a switching frequency of 20 *kHz*) is possible. Dc conversion, inversion, and rectification have been demonstrated to be just special cases of cycloconversion.

CONCLUSION

Topologies and *analysis techniques* for fast-switching *inversion (dc-to-ac)*, *rectification (ac-to-dc)*, and *cycloconversion (ac-to-ac)* have been developed in this thesis. They are the generalization of those for fast-switching dc and slow-switching dc or ac conversions. As a result, switched-mode dc conversion, inversion, rectification, and cycloconversion theories are now unified.

To draw a universal picture, the restriction of *constant instantaneous power flow*, satisfied naturally by dc converters, has been imposed upon ac switchers. This restriction implies *ideal*, i.e., *dc single-phase* or *balanced sinusoidal polyphase*, waveforms. To identify ideal topologies, the switching frequency is pushed sufficiently beyond the input and output frequencies so that switching harmonics are attenuated adequately by low-pass filters and negligible relative to the desired components. *Sinusoidal PWM* is chosen because under *fast switching*, the steady-state *low-frequency* performance of many open-loop or closed-loop control schemes is essentially one form of PWM or another. In short, *ideal topologies with fast-switching sinusoidal PWM* have been realized.

Each familiar *dc converter* has been extended, under the previous constraints, into its *inverter*, *rectifier*, or *cycloconverter equivalent*. Thus, there now exist the flyback inverter, flyback rectifier, and flyback cycloconverter, all being ideal and exhibiting characteristics similar to those

of their dc kin. The same conclusion holds for the buck, boost, buck-boost, boost-buck, forward, push-pull, full-bridge, etc., topologies as well. Ac converters are named after their dc roots to emphasize that *four fields of switched-mode conversion are topologically related*. After all topologies have been enumerated and examined, the *cycloconverter* is endorsed as the *generalized converter* that degenerates into the other three converters under special input or output frequencies.

Topology serves as the unifying factor not only over all classes of converters, but also *within each class* itself. To consolidate the ramifications in any of the four areas, it is important to differentiate a *topology* from the *drive strategy* for its switches. Any topology may be driven open-loop or closed-loop, slow-switching or fast-switching, six-stepped or PWM, and so on. These many drive schemes have given birth to different names and, frequently, the false impression of distinct topologies. For instance, the "three-pulse cycloconverter" [24] and "generalized transformer" [37] are two names for the *same* buck-type circuit in Fig. 8.3; the first one is pulsed at low frequency, and the second pulse-width-modulated at high frequency. Likewise, a question frequently raised for the boost inverter is whether it can drive a motor; the answer is *yes* because the boost inverter (Fig. 3.3) is *topologically identical* to the current-source inverter (Fig. 2.2), and the current-source inverter, for sure, can drive a motor. Therefore, switching strategy does *not* define topology; and distinct drive schemes can give *similar* qualitative results that are determined by the *topology* itself.

Once the universal relationship among all topologies has been established, a *generalized analysis method* necessarily follows. The *describing equation technique* has thus been revitalized in this thesis to

treat dc converters, inverters, rectifiers, and cycloconverters. It uses *switching functions* and basic network principles to derive the *state-space switching equations* of a switching converter. These equations are exact and, hence, applicable to a variety of control algorithms. For *pulse-width modulation* at much lower than the switching frequency, it suffices to retain only the *duty ratios* of the switching functions to describe the *low-frequency inputs and outputs*. The resulting *continuous* differential equations are the *describing equations* of the converter.

Except for dc converters, describing equations written in the *stationary*, or *abc*, frame of reference are generally *time-varying*. Ease of analysis of time-invariant systems, such as dc switchers, suggests the transformation of the abc describing equations to the *rotating*, in this case *ofb*, coordinates where the converter, if ideal, is described by its *dc equivalent*. The ofb coordinates are also a convenient ground for comparison and unification of topologies.

Buck, *boost*, *buck-boost*, and *flyback inverters*, *rectifiers*, and *cycloconverters* with more than one phase have been described and analyzed. Description is in terms of the arrangement of switches and filter elements relative to the source and load. Switches are specified by their *duty ratios*, either purely *dc* or dc with polyphase *sinusoidal* modulation. Analysis by *describing equations* and *coordinate transformation* reveals that *all converters with any number of phases* (>1) *are equivalent and reducible to the two-phase converter*; therefore, it suffices to study only the two-phase case. The four types of topology examined pass the *ideality test*: their ofb describing equations all have *constant* coefficients under steady-state condition. True *excitations* are *dc sources* and the *amplitude* and *frequency*

of ac sources; true *controls* are *dc duty ratios* and the *amplitude* and *frequency* of ac duty ratios; outputs are then *dc states* or the *amplitude* and *phase* of ac states.

Steady-state results are thus also *constant* and are solutions of a set of algebraic equations. A *constant scalar* in the ofb reference frame represents a *dc* waveform in the abc coordinates, and *constant phasors* balanced *sinusoidal* states. The *frequency* of sinusoidal outputs ranges from *dc* to a *very high upper bound* determined by the switching frequency and amount of ripple tolerated; both phase sequences can be chosen electronically. *Dc gains* at zero filter reactances are consistent with names of the topologies: the buck converters step down; the boost, up; and the buck-boost and flyback, up and down. At *high filter reactances*, *steady-state frequency responses* are no longer flat because they have poles and zeros. These corners move with quiescent operating points, and their interpretations usually go beyond linear circuit theory. For instance, responses of boost-type inverters blow up at frequencies where the load impedance has poor power factor; this singularity happens to maintain volt-balance for the inductor. Therefore, filter reactances should generally be included even in the steady-state picture unless they are designed properly; of course, "properly" is guaranteed by *analysis* of steady-state behavior in the presence of filters.

Since switched-mode structures are generally nonlinear, large-signal dynamics are formidable; therefore, *dynamic study* has been restricted to the *small-signal sense*. Dynamic analysis then involves perturbation of the describing equations in the ofb coordinates and solution of various input-to-output transfer functions. The small-signal bandwidth of the converter itself

is wide and can be further broadened by increase of switching frequency or, correspondingly, decrease of filter reactances. Eventually, the load imposes its own dynamics over the entire converter/load system.

Both steady-state and dynamic results can be illustrated and performances of different topologies compared by way of *canonical models*. The model is the circuital form of the *linearized describing equations*, again in the rotating reference frame. Three groups of elements always exist, namely, *input excitation and control generators*, *conversion transformers*, and *low-pass filters*. Excitation generators are phasors representing the supplies; control generators are driven by dc duty ratios or amplitudes and phases of sinusoidal duty ratio modulations. Conversion transformers partly model the switching process; their *conversion ratio* depends on the steady-state amplitude of duty ratio modulation and affects both steady-state and dynamic gains. Low-pass filters account for the energy-storage elements in the actual circuit; their *topology* also reflects the conversion process across the switches. The filter frequency is in general *complex*; its real part s is responsible for *dynamic reactance*, and imaginary part $j\,\Omega$ *steady-state* reactance - this imaginary frequency introduces corners into steady-state frequency responses. Filter components vary as functions of quiescent condition and are similar for dc converter, inverter, rectifier, and cycloconverter of the same topology.

Analytical results have been used to realize the connection of transistors and diodes in place of ideal switches. Throws in inverters and rectifiers are either voltage-two-quadrant, implemented by transistor and diode in series, or current-two-quadrant, implemented by transistor and diode in anti-parallel. Throws in direct cycloconverters are four-quadrant

and in indirect ones two-quadrant. Owing to fast switching, a *multitude of flexible modulation strategies* can drive the switches for a given gain function. Examples are *continuous* and *six-stepped PWM*; the latter retains the sinusoidal quality of the former and the high effective duty ratio of six-stepped switching. The *phase* and *amplitude* of duty ratio modulations determine the *direction of power flow*; the particular combination of phase and amplitude adjustments depends on how power reversal is initiated. In some converters, more switches need be added to condition the ports for four-quadrant operation.

Isolation is affordable with fast switching since the transformer is small. The flyback and isolable boost-buck topologies accept an isolation transformer naturally since they contain a dc link that stays completely at either the input or output. Other topologies less inherently isolable, such as the buck, can still be isolated by extension of the techniques employed in dc conversion. Thus, there exist forward, push-pull, full-bridge, etc., inverters, rectifiers, and cycloconverters. Isolation in polyphase circuits is greatly simplified if it can be integrated into the dc link.

Rectifiers and cycloconverters have been operated as *switched-mode impedance converters*. In this application, they change the sign of reactive power to make a capacitive load appear inductive to the source, and vice versa. Some topologies, such as the buck rectifier and buck-boost or flyback cycloconverter, can convert an arbitrary load to an impedance of any amplitude and phase for the source. The synthesized impedance is controlled by dc duty ratios and amplitude, frequency, or phase sequence of sinusoidally modulated duty ratios. The input can thus be presented with any power factor, e.g., unity, leading, and lagging, in an *open-loop* fashion.

Experimental flyback inverter and cycloconverter have been built to verify the theory. Interesting waveforms have been observed at both low- and high-frequency scales; their explanations are facilitated by *switching function diagrams*. The abc-ofb transformation has been implemented to condition ac waveforms for standard *dc measurement setups*. Steady-state and small-signal corners arrive where predicted by describing equations. Therefore, there are not only topologies with wide steady-state and dynamic bandwidths, but also analysis and measurement techniques to explain circuit behavior within and beyond these bandwidths.

This thesis is just a small step in a journey still long and challenging. The search for novel topologies, a topic of frequent interest to innovative minds, will undoubtedly continue in not only dc conversion, but also inversion, rectification, and cycloconversion. The thrust should be even stronger in the ac fields to take full advantage of new fast-switching devices, versatile integrated circuits and microprocessors, and modern control theories. The analysis techniques described here apply to PWM drives and classical, continuous control. The problem certainly needs be reformulated for other discrete control strategies more suitable for certain applications. In carrying out the analysis, it should be remembered that the *topology still remains the same*, and only the switching or control policy is changed.

Space and time have limited consideration of practical applications here, and a great deal of works still lie ahead in this direction. Motor drive, uninterruptible power supply, utility interface, and reactive power generation are just a few examples. The vast amount of loads, topologies, switching strategies, and control techniques inevitably generate an unmeasurable number of interesting problems only few of which have been partially solved.

APPENDICES

APPENDIX A

TOPOLOGY AND ANALYSIS IN DC CONVERSION

This appendix consists of five sections. The first summarizes familiar *dc converter topologies*; the second their *steady-state* voltage gains; the third their *small-signal dynamics*; the fourth their *canonical models*. The final section reviews *state-space averaging* and explains how this approach fits into the more general describing equation technique.

A.1 Description of Topologies

The *buck*, *boost*, *buck-boost*, and *boost-buck dc converters* are illustrated in Fig. A.1. The buck topology consists of a double-throw switch, which chops the input into a dc component and switching harmonics, and an LC filter, which attenuates the switching noise while passing the dc part to the load. The boost circuit places an inductor in series with the source to convert voltage into current; the current is then fed into the load by a double-throw switch.

The buck-boost converter is the cascade of a buck and a boost topology; the capacitor of the buck stage is discarded as it is redundant. The boost-buck circuit, on the other hand, is the series connection of a boost and a buck converter; the capacitor is retained to absorb the mismatch in inductor currents. The composite topologies are not frequently used in dc conversion since they require two transistors - two independent

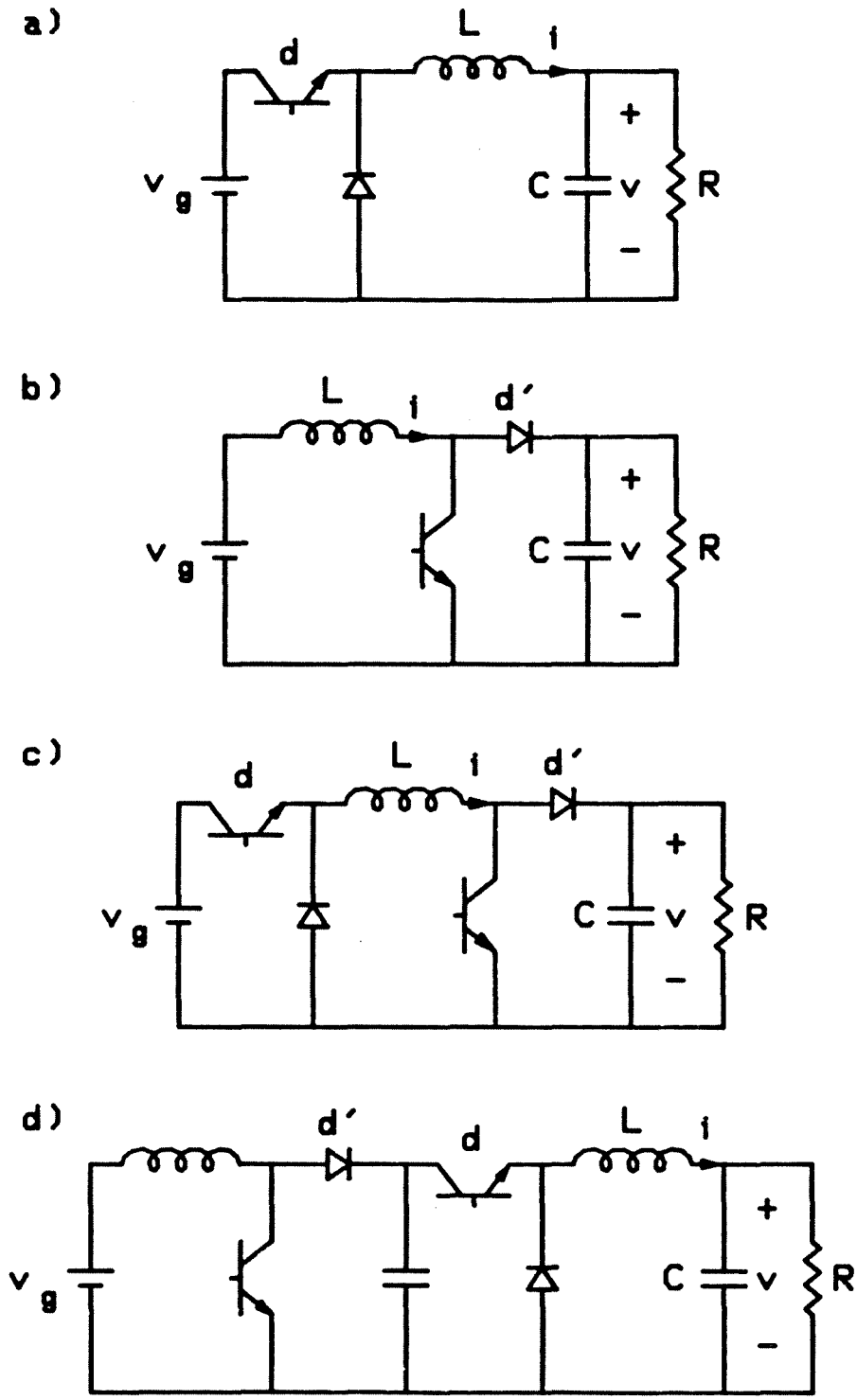

Fig. A.1 (a) Buck, (b) boost, (c) buck-boost, and (d) boost-buck dc converters.

controls are available, though. Nevertheless, they find useful applications in ac conversion fields.

Topological manipulation of the buck-boost results in the *flyback* and of the boost-buck the *Ćuk* converter described in Figs. A.2a and c, respectively. As their predecessors, the flyback and Ćuk topologies are *indirect* converters, i.e., they process energy through an intermediate link. The link in the former is current and in the latter voltage. Owing to their energy storage/transfer inductor or capacitor, which stays completely at either the source or the load, they incorporate isolation naturally. The isolated versions are delineated in Figs. A.2b and d.

A.2 Steady-State Performance

Steady-state voltage gains for the buck, boost, and flyback dc converters are tabulated in Table A.1. Those for the buck-boost, boost-buck, and Ćuk stages are equal to that of the flyback topology. The significance of the names is apparent: "buck" means *step down*, "boost" *step up*, and "buck-boost" (or boost-buck, flyback, Ćuk) *step up and down*. Steady-state frequency responses are flat, i.e., no steady-state pole or zero exists, because steady-state filter reactances are always zero.

A.3 Small-Signal Dynamics

Duty-ratio-to-output and line-to-output transfer functions are compared in Table A.2 for the buck, boost, and flyback topologies. Only the buck responses are linear with second-order roll-off at the LC corner independent of quiescent operating point. The other two are nonlinear with poles and right-half-plane zeros moving as functions of steady-state duty

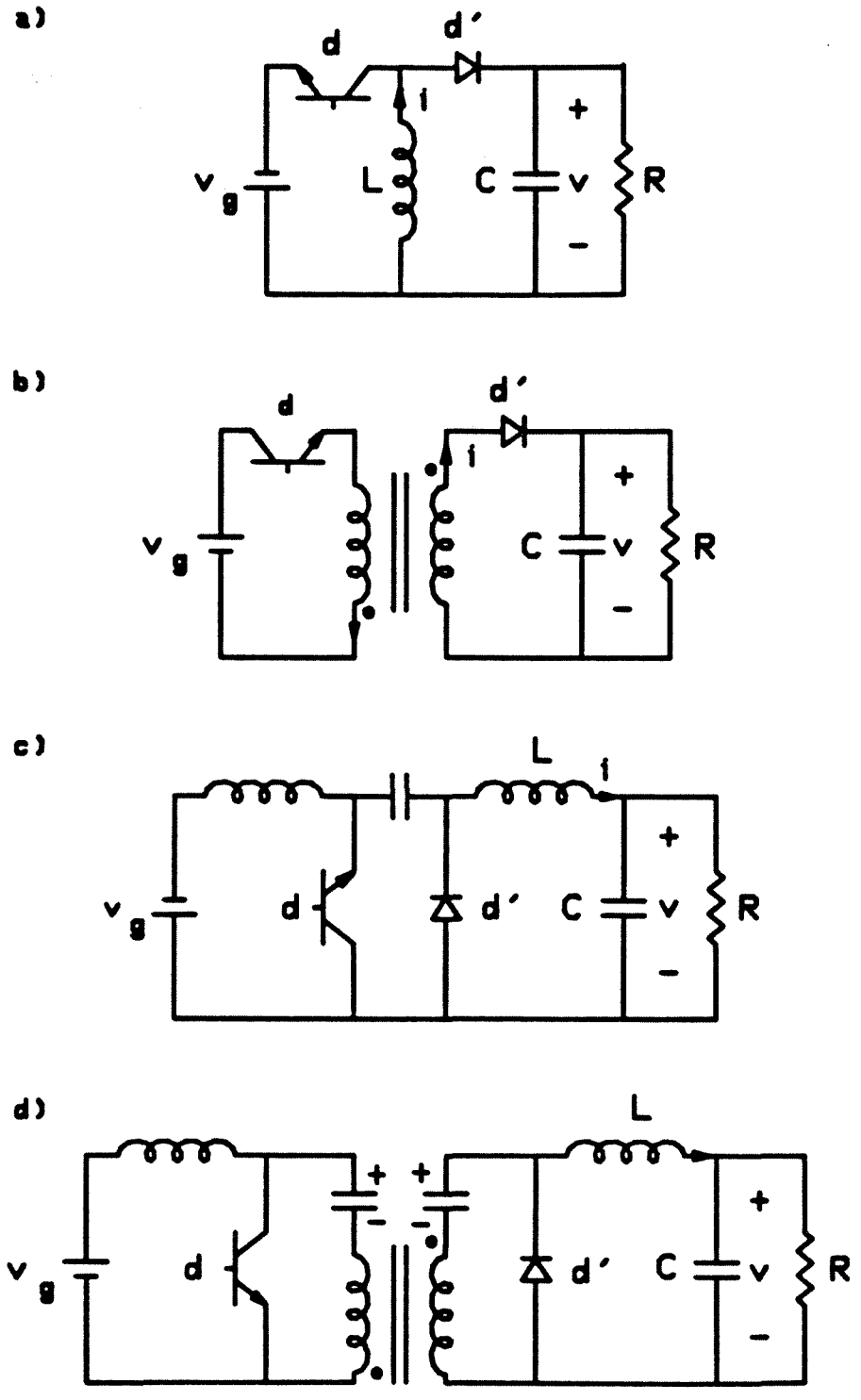

Fig. A.2 (a) Non-isolated and (b) isolated flyback dc converters; (c) non-isolated and (d) isolated Cuk dc converters.

Dc Converter	Capacitor Voltage V	Inductor Current I
Buck	$D\ V_g$	$\frac{D\ V_g}{R}$
Boost	$\frac{V_g}{D'}$	$\frac{V_g}{D'^2 R}$
Flyback	$\frac{D}{D'} V_g$	$\frac{DV_g}{D'^2 R}$

TABLE A.1 Steady-state capacitor voltages and inductor currents in the buck, boost, and flyback (or buck-boost) dc converters.

ratio.

A.4 Canonical Models

Since the buck, boost, and flyback dc converters are all of second-order, they share the canonical model shown in Fig. A.3 whose elements are as specified in Table A.3. The model has three sections, namely, *input generators*, *a conversion transformer*, and a *low-pass filter*. The excitation generator is driven by the dc supply, and control generators the duty ratio of the switch. The dependent current source is inserted to correct the input current and account for nonzero line impedance.

Parameter	Buck	Boost	Flyback
G_{vg}	D	$\frac{1}{D'}$	$\frac{D}{D'}$
G_{vd}	V_g	$\frac{V_g}{D'^2}$	$\frac{V_g}{D'^2}$
ω_o	$\frac{1}{\sqrt{LC}}$	$\frac{D'}{\sqrt{LC}}$	$\frac{D'}{\sqrt{LC}}$
Q	$\frac{R}{\omega_o L}$	$\frac{D'^2 R}{\omega_o L}$	$\frac{D'^2 R}{\omega_o L}$
ω_z	∞	$\frac{D'^2 R}{L}$	$\frac{D'^2 R}{DL}$
where $\frac{\hat{v}}{\hat{v}_g} = G_{vg} \frac{1}{1 + \frac{1}{Q}\frac{s}{\omega_o} + (\frac{s}{\omega_o})^2}$			
and $\frac{\hat{v}}{\hat{d}} = G_{vd} \frac{1 - \frac{s}{\omega_z}}{1 + \frac{1}{Q}\frac{s}{\omega_o} + (\frac{s}{\omega_o})^2}$			

TABLE A.2 Line- and duty-ratio- to-output transfer functions of the buck, boost, and flyback dc converters.

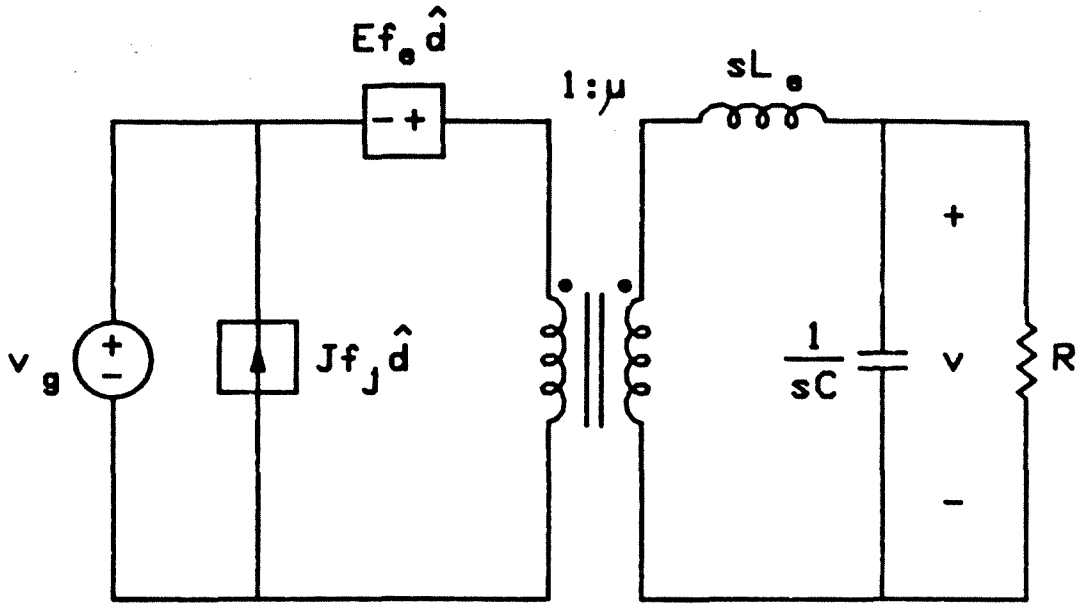

Fig. A.3 Canonical model of the buck, boost, and flyback converters.

The inputs excite a conversion transformer whose *conversion ratio*, related to the duty ratio, provides the steady-state and dynamic gain across the switch. The transformer then drives an LC section that models the low-pass filter in the actual circuit. The filter frequency is real since the steady-state frequency is zero. The effective inductance varies with $\frac{1}{D'^2}$ to reflect switching nonlinearity; this form of effective inductance is found in ac converters as well.

Parameter	Buck	Boost	Flyback
μ	D	$\frac{1}{D'}$	$\frac{D}{D'}$
E	$\frac{V}{D^2}$	V	$\frac{V}{D^2}$
f_e	1	$1 - s\frac{L_e}{R}$	$1 - s\frac{DL_e}{R}$
J	$-\frac{V}{R}$	$-\frac{V}{D'^2R}$	$-\frac{V}{D'^2R}$
f_j	1	1	1
L_e	L	$\frac{L}{D'^2}$	$\frac{L}{D'^2}$

TABLE A.3 Parameters of the canonical model of the buck, boost, and flyback dc converters.

A.5 Relation of State-Space-Averaging to Describing Equation Technique

After the describing equation technique was developed for slow-switching ac conversion, and could have been applied to fast-switching dc conversion as well had it been more popularized, *state-space averaging* has been introduced as an analysis tool for switched-mode dc power supplies. As is detailed on the left side of Fig. A.4, the method first enumerates *all* $\overline{T}$ *switched networks* in *each switching cycle*; this step is straightforward in simple dc structures whose $\overline{T}$ is always small and constant, but is involved in multiple-pole, multiple-throw circuits whose $\overline{T}$ is large and varying. The linear state-space equation of the switched topology during $\overline{d}_m T_s$, where $\overline{d}_m$ is the *topological duty ratio* of switching interval m within some period T_s, is then expressed as

$$\mathbf{P}\dot{\mathbf{x}} = \overline{\mathbf{A}}_m \mathbf{x} + \overline{\mathbf{B}}_m \mathbf{u} , \qquad 1 \le m \le \overline{T} \tag{A.1}$$

The *averaged state-space equation* for *one* switching period is the average of $\overline{T}$ equations like Eq. (A.1):

$$\mathbf{P}\dot{\mathbf{x}} = \sum_{m=1}^{\overline{T}} \overline{d}_m (\overline{\mathbf{A}}_m \mathbf{x} + \overline{\mathbf{B}}_m \mathbf{u}) \tag{A.2}$$

In dc converters, the averaged equations for all periods are identical; therefore, the average description is certainly *unique*. In ac converters, the averaged equations of different periods have different $\overline{T}$, $\overline{d}_m$, and so on; therefore, questions of *uniqueness* and *correct control parameters* arise.

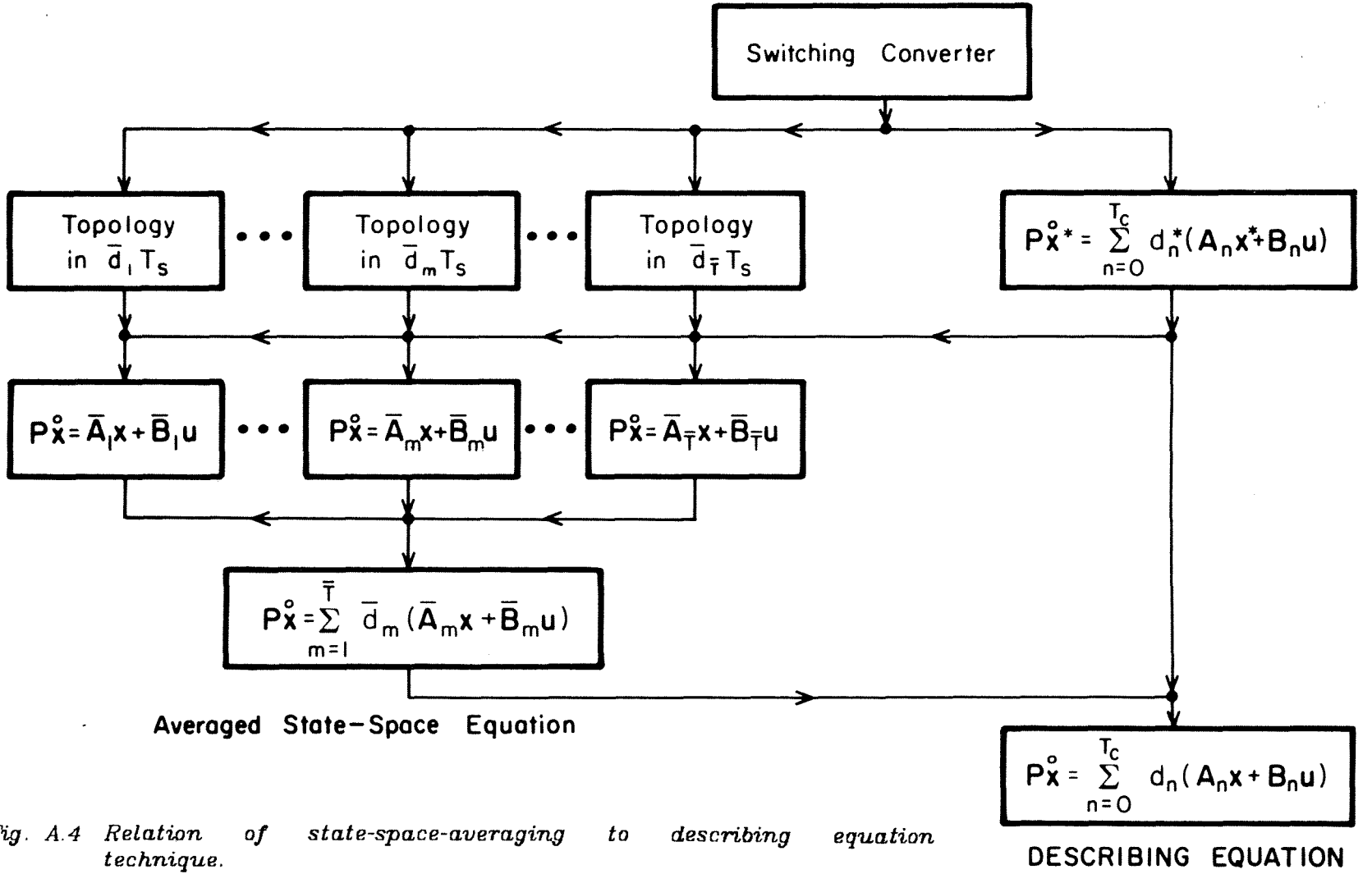

Fig. A.4 Relation of state-space-averaging to describing equation technique.

It is known that the *describing equation technique* avoids the aforementioned ambiguities. Therefore, these ambiguities may be superficial if state-space-averaging is proved to be a special case of describing equation. Fortunately, as is shown in Fig. A.4, topological duty ratios and equations of state-space averaging are just *decompositions* of the *state-space switching equation*

$$\mathbf{P}\dot{\mathbf{x}}^* = \sum_{n=0}^{T_c} d_n{}^* (\mathbf{A}_n \mathbf{x}^* + \mathbf{B}_n \mathbf{u}) \tag{A.3}$$

(this equation is obtained by inspection of the original switching network and use of switching functions $d_n{}^*$ of T_c independent throws; its derivation never resorts to meticulous switching and topological details). Reversely, the averaged state-space equations of all switching periods can be manipulated back to the *describing state-space equation*

$$\mathbf{P}\dot{\mathbf{x}} = \sum_{n=0}^{T_c} d_n (\mathbf{A}_n \mathbf{x} + \mathbf{B}_n \mathbf{u}) \tag{A.4}$$

where d_n is the *duty ratio of the switching function* $d_n{}^*$. Thus, the average description is still unique although there are not as many as $\overline{T}$ control parameters. There are only T_c control parameters, where T_c is always less than $\overline{T}$; true control parameters are *duty ratios* d_n *of the switching functions*, not topological duty ratios $\overline{d}_m$.

APPENDIX B

THE ABC-OFB TRANSFORMATION

A vector $\mathbf{v}$ in the stationary (abc) frame of reference can be transformed into a vector $\tilde{\mathbf{v}}$ in the rotating (ofb) coordinates [23] by

$$\mathbf{v} = \tilde{\mathbf{T}}\tilde{\mathbf{v}} \qquad \text{or} \qquad \tilde{\mathbf{v}} = \tilde{\mathbf{T}}^{-1}\mathbf{v} \tag{B.1a,b}$$

If the order of the system is M and the phase sequence positive,

$$\tilde{\mathbf{T}}^{-1} = \frac{1}{\sqrt{2}} \begin{bmatrix} e^{j\theta_T} & e^{-j\theta_T} \\ e^{j(\theta_T - \frac{\pi}{2})} & e^{-j(\theta_T - \frac{\pi}{2})} \end{bmatrix}, \qquad M = 2 \tag{B.2a}$$

$$\tilde{\mathbf{T}}^{-1} = [\, T_{lm} \,] = \left[\frac{1}{\sqrt{M}} e^{-j(l-1)(m-1)\frac{2\pi}{M}} e^{j\theta_T \delta_{l2}} e^{-j\theta_T \delta_{lM}} \right], \qquad M > 2 \tag{B.2b}$$

and

$$\tilde{\mathbf{T}} = \frac{1}{\sqrt{2}} \begin{bmatrix} e^{-j\theta_T} & e^{-j(\theta_T - \frac{\pi}{2})} \\ e^{j\theta_T} & e^{j(\theta_T - \frac{\pi}{2})} \end{bmatrix}, \qquad M = 2 \tag{B.3a}$$

$$\tilde{\mathbf{T}} = [\, T_{pq} \,] = \left[\frac{1}{\sqrt{M}} e^{j(p-1)(q-1)\frac{2\pi}{M}} e^{-j\theta_T \delta_{q2}} e^{j\theta_T \delta_{qM}} \right], \qquad M > 2 \tag{B.3b}$$

where the phase θ_T of the transformation satisfies

$$\theta_T = \int_0^t \omega(\tau)\, d\tau - \varphi_T \tag{B.4}$$

and

$$\delta_{ij} = \begin{cases} 1 & \text{if } i=j \\ 0 & \text{if } i\neq j \end{cases} \tag{B.5}$$

The above transformation converts a *balanced sinusoidal* vector

$$\mathbf{v} = \left[v\cos[\,\theta_v - (w-1)\frac{\pi}{2}\,] \right], \qquad M=2 \tag{B.6a}$$

$$\mathbf{v} = \left[v\cos[\,\theta_v - (w-1)\frac{2\pi}{M}\,] \right], \qquad M>2 \tag{B.6b}$$

into

$$\tilde{\mathbf{v}} = [\,\tilde{v}_f \quad \tilde{v}_b\,], \qquad M=2 \tag{B.7a}$$

$$\tilde{\mathbf{v}} = [\,0 \quad \tilde{v}_f \quad 0 \quad \cdots \quad 0 \quad \tilde{v}_b\,], \qquad M>2 \tag{B.7b}$$

where

$$\theta_v = \int_0^t \omega(\tau)\,d\tau - \varphi_v \quad \text{and} \quad 1\le w\le M \tag{B.8a,b}$$

and the *backward phasor* $\tilde{v}_b$ and *forward phasor* $\tilde{v}_f$ are defined as

$$\tilde{v}_b = \frac{\sqrt{M}}{2} v\, e^{-j(\varphi_v-\varphi_T)} \quad \text{and} \quad \tilde{v}_f = \frac{\sqrt{M}}{2} v\, e^{j(\varphi_v-\varphi_T)} \tag{B.9a,b}$$

The amplitude of the backward phasor is directly proportional to that of the stationary sine waves; its phase is the difference between those of the sine waves and the transformation. An ideal polyphase *ac* converter appears *time-invariant* in the ofb coordinates because $\tilde{v}_b$ and $\tilde{v}_f$ are constant under steady-state condition. Any M^{th} order is always reduced to second order owing to Eqs. (B.7a) and (B.7b).

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