

Charge Transfer in Charge Coupled Devices

Thesis by

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ABSTRACT

Theoretical analysis of the dynamics of charge transfer in charge coupled devices is central to the intelligent design and proper estimation of the usefulness of this new device concept. In this report, a detailed study of the electrostatics and dynamics of buried channel charge coupled devices (BCCDs) is presented. Both theoretical and experimental study of BCCD has been very difficult due to the additional complexity in the BCCD structure in contrast to the original simpler structure of surface charge coupled devices (SCCDs). And up to present, no comprehensive study of BCCD which includes the complete electrostatic and dynamic analysis of BCCD operations has been reported. It is the purpose of this thesis to assist physicists, device engineers, and applications engineers interested in BCCD by presenting all essential information on the buried channel CCDs in one place and in a comprehensive form so that the background laid on BCCD can be applied immediately to the case of the SCCD studies achieved in the past and also to the investigation of a future CCD structure.

The work reported in this thesis consists of three major contributions to the rapidly progressing CCD research and is described in the main text, Chapter 1, 4, and 5 of this thesis.

In Chapter 1 the relations between the electrostatic potential and the charge distribution in one dimensional structure for BCCD are analyzed in detail. An expression for the channel potential in terms of salient physical parameters is obtained by depletion approximation. And its implications on doping levels, and profiles; charge storage capa-

city; geometrical structure and gate voltages are discussed in detail to provide a useful reference and guide-work in design and analysis of buried channel CCDs. The results obtained numerically for the case of Gaussian doping profile are also presented and correlated with the uniform doping model. In Chapter 4 a detailed two dimensional electrostatic analysis of buried channel CCDs is presented. By a simple capacitance network model the two dimensional Poisson equation appropriate for the structure is reduced into a second order differential equation in a single spatial dimension. The resulting equation relates the signal charge and the minimum channel potential under all the relevant electrodes and interelectrode regions. A diffusion equation describing the charge transfer is coupled to this equation in order to incorporate the static model in dynamic charge transfer description. The results of a detailed numerical simulation of the charge transfer process in the resulting realistic model of a high density buried channel CCD remain to be studied in Chapter 5. It is shown that the limitations on the device performance due to incomplete free charge transfer are reduced considerably by powerful field-aided charge transfer. The procedure to estimate the significance of this reduction in terms of the charge remaining as a function of time is formulated analytically.

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Chapter 1

ELECTROSTATIC ANALYSIS OF BASIC ONE
DIMENSIONAL MOS STRUCTURE FOR BURIED CHANNEL CCDs1.0 Introduction to Charge Coupled Devices

In 1970, Boyle and Smith* in Bell Labs showed that a signal charge packet in a metal-oxide-semiconductor (MOS) structure could be stored in a potential well under a depletion-biased metal electrode and moved from under one electrode to the next by appropriate pulsing of the electrode potentials. For the structure to be used as a signal processing device, the electrodes must be placed close enough to make the potential wells couple and the signal charge packets move smoothly from one well to the next. The resulting structure is commonly known as the charge coupled device (CCD).

In the past few years there have been tremendous advances in the fabrication of this new class of semiconductor devices. These advances, occurring in an already sophisticated technology, were made possible by earlier parallel developments in the parent field of large scale integrated circuits.

Analog-signal-processing developments in CCDs have been very significant, for the first time bringing the full impact of monolithic integrated-circuit technology to bear on sophisticated analog communi-

* Boyle, W. S., and Smith, G. E. "Charge Coupled Semiconductor Devices," B.S.T.J., 49, No.4 (April 1970), pp.587-593

cation systems. CCD delay-line, multiplexing and filtering components are by now operating in developmental systems, where they provide such complex and vital signal-processing operations as matched filtering in spread-spectrum communication, bandpass and low-pass filtering, Hilbert and Fourier transforms for single-side band modulation and complex coding for military communications. However, most significant of all their commercial implications are CCD memory systems. Here progress has been slow, mostly due to the already high level of bipolar and MOS memory technology and the fact that CCD memories, owing to their charge-transfer process, are basically serial. Nevertheless, CCD memories have been gaining momentum. The first to arrive is 16,000- to 32,000-bit serial CCD memory element capable of operating at respectable 1- to 5-megahertz kilobits on a chip in the next two years, at last ushering in the age of mass-memory chip technology.

A typical two dimensional CCD structure is illustrated in Fig.1.1 as one unit cell of the overlapping gate structure using the standard silicon technology. The device is a series of simple metal-oxide-semiconductor (MOS) capacitors coupled in such a way that the signal charge on the capacitors can move from under one storage to the next. The storage site is actually a potential well created under the electrodes at the semiconductor insulator interface. In Fig. 1.2a and Fig. 1.2b the band diagram of a metal-insulator-n semiconductor is shown to illustrate the creation of potential wells at the interface when a voltage pulse is applied to the metal electrode. Minority carriers, injected in response to a digital or analog signal or generated by

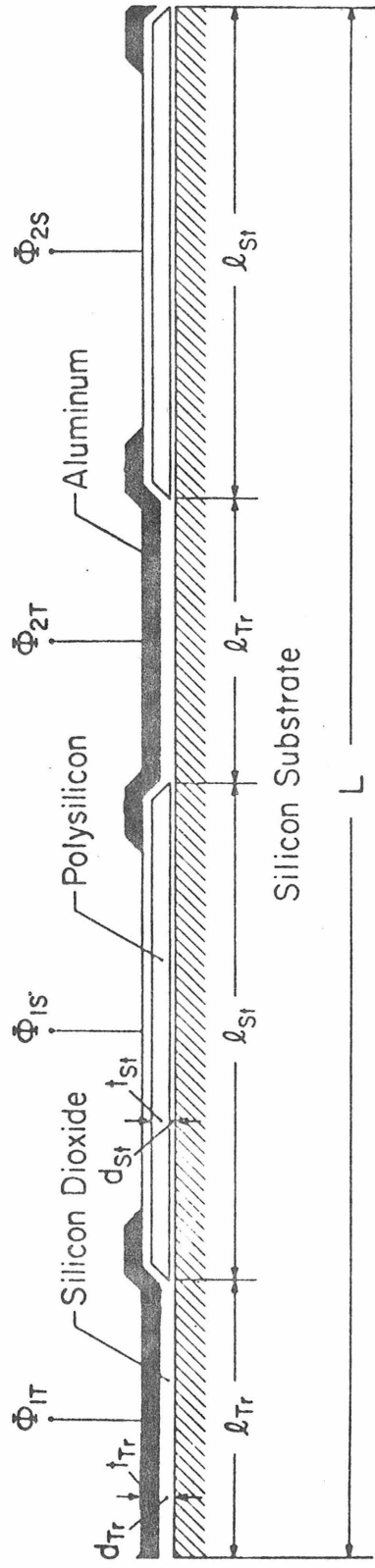


Figure 1.1 One unit cell of the overlapping gate structure using the standard silicon gate technology.

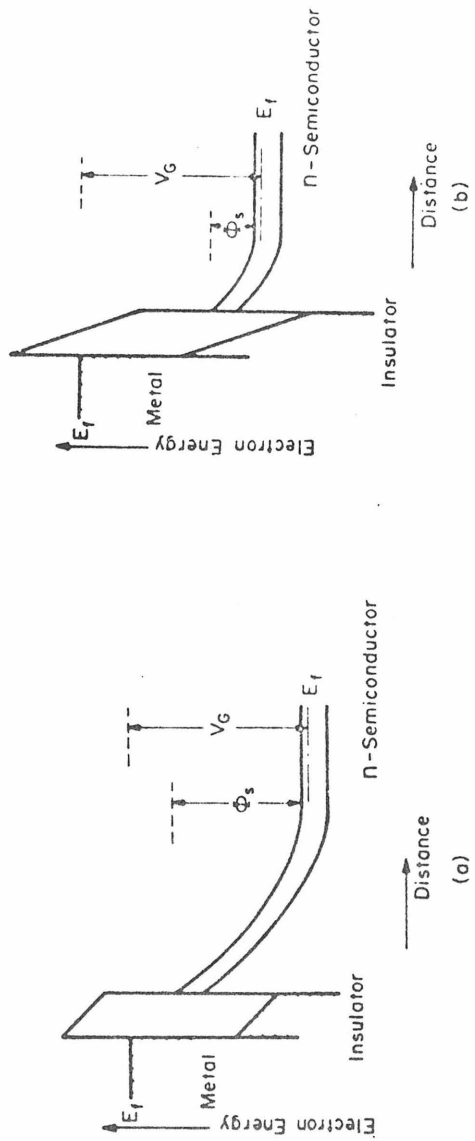


Figure 1.2 Energy level diagram of a metal-insulator-n semiconductor
 (a) when a voltage pulse has just been applied to the metal
 electrode
 (b) after the accumulation of some minority carrier at the
 insulator-semiconductor interface

photons, are stored as charge packets in these potential wells resulting in a decrease in depth of the potential well.

The storage and transfer of the charge packets are controlled by the clocking pulses driving the closely spaced electrodes as shown in Fig. 1.3 where a three phase clocking scheme is used. In the three phase operation three electrodes are needed to store one bit of information and obtain a directionality in the signal flow. The figures illustrate how the 4-bits information in a 1-0-1-0 pattern is transferred to the right.

The original charge coupled device, as introduced in 1970, operates by moving minority carriers along the surface of a semiconductor with voltage pulses applied to metal electrodes which are separated from the semiconductor by an insulating layer (SiO_2). Today, this type of charge coupled devices is referred to as surface charge coupled devices (SCCD). The analysis of charge-transfer characteristics of SCCD in terms of free-charge losses, (see Appendix I) and losses due to the trapping by fast interface states (see Appendix II) has been central to the intelligent design and proper estimation of the usefulness of this new device concept. In these detailed studies in Appendix I and II it is shown that the transit characteristics of SCCD from one electrode to the next is determined by the minority carrier transport under the influence of thermal diffusion and electric fields due to the external electrode voltages and the self-induced carrier repulsions. It is now known that the transport limitations are largely determined by device geometry; for long electrodes, thermal diffusion is predominantly responsible for transferring the last

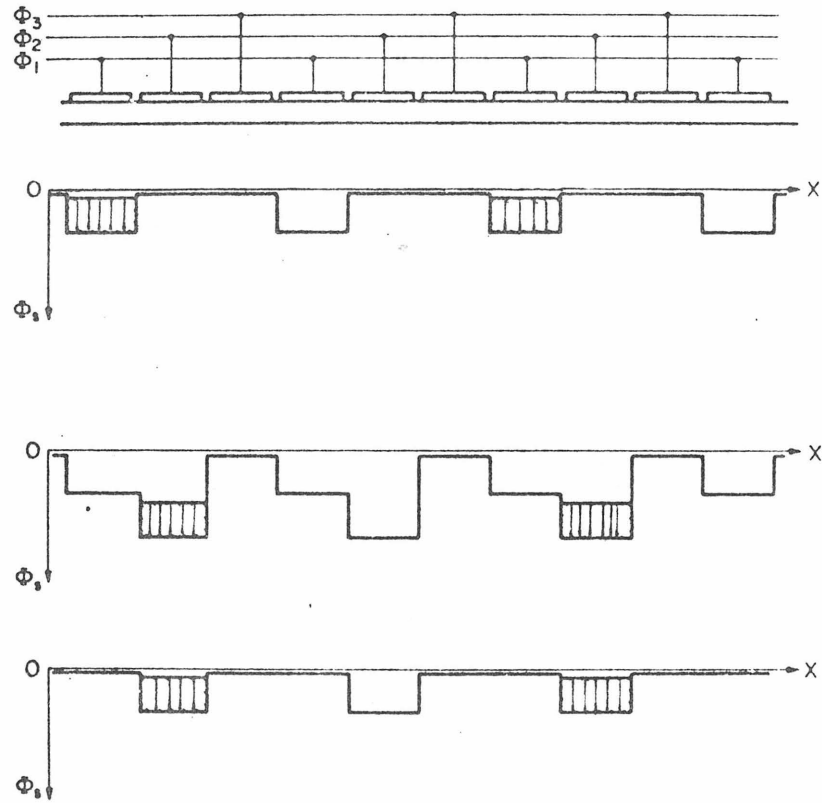


Figure 1.3

Schematic cross section of a three-phase charge coupled device structure. The electrodes are pulsed in the sequence $\phi_1\phi_2\phi_3$.

small amount of charge forward and limits efficient operation to clock frequencies below 10 MHz. Surface state trapping is much less dispersive, and even at low frequencies 10^{11} states/cm²-eV can impose the requirement for regeneration after as few as 100 transfers.

To overcome these problems in 1972, a modified CCD structure was introduced by a group of scientists* in Bell Labs. However, due to the additional complexity in structure, the first-fabricated devices did not work at all. And further detailed experimental and theoretical investigations remained to be carried out. This new type of CCD is today referred to as buried channel charge coupled devices (BCCDs) in contrast to the original surface charge coupled devices (SCCDs). The new buried channel CCD is the subject of investigation in this thesis. The cross-sectional view of this BCCD is illustrated in Fig. 1.4. In this modified BCCD structure, the charge does not flow at the semiconductor surface; instead it is confined to a channel in the p-layer which lies beneath the surface. The buried channel device has the potential of eliminating surface trapping because the signal charge packets now move away from the interface. And it is also expected that this modification in structure will give rise to increased fringing fields under the electrodes and that the diffusion will be replaced by the more powerful field-aided

* Walden, R.H., Krambeck, R.H., Strain, R.J., McKenna, J., Schryer, N.L., and Smith, G.E. "The Buried Channel Charge Coupled Devices" B.S.T.J. BRIEF, 51, No.7 (September 1972), pp.1635-1640

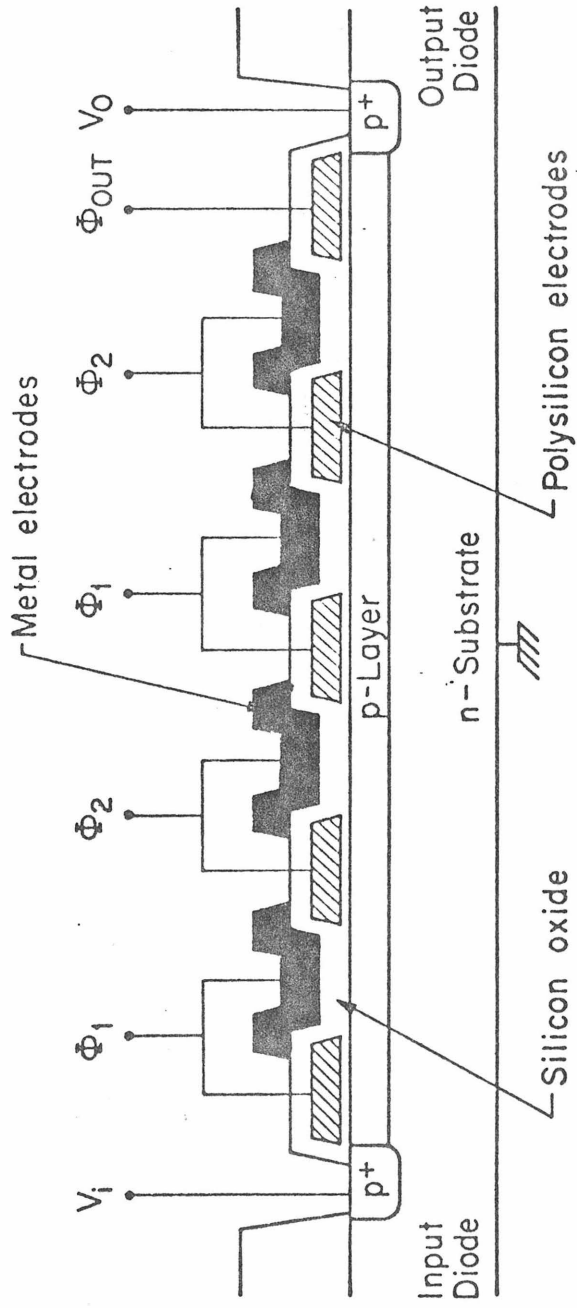


Figure 1.4 Cross-sectional view of two phase overlapping gate buried channel charge coupled devices.

transfer as an important factor in the final charge transfer process. This should lead to fast, efficient transport even when little charge remains to be transferred.

However, both the theoretical and the experimental study of BCCD devices has been very difficult due to the additional complexity in structure. Up to present, no comprehensive study of BCCD which includes the complete electrostatic and dynamic analysis of BCCD operations has been reported. It is the purpose of this thesis to assist physicists, device engineers, and applications engineers interested in BCCD. By presenting all essential information on the buried channel CCDs in one place and in a comprehensive form they can immediately apply this analysis of BCCD to the case of the SCCD studies in the past (see Appendix I and II) and also to the investigation of a future CCD structure discussed in Appendix III. With these motivations, a detailed study of the electrostatics and dynamics of this new BCCD is presented in the main text, Chapter 1, 4, and 5 of this thesis.

1.1 Introduction

Electrostatics play an important role in the design of a functioning buried channel device. The connection between geometrical structure; doping levels, and profiles; charge storage capacity; gate voltages are all determined by simple electrostatic analysis. This analysis must be carried out before any consideration of the actual charge transfer process is made. In principle the electrostatic analysis could be made by solving the Poisson equation with all the relevant charge distributions and applied potentials for the correct three dimensional geometry. However, in general this would require numerical solutions which would be

both expensive to generate and difficult to use in considering the impact of varying some of the physical parameters on the performance of the device. Hence, it is desirable to idealize the actual device structure so that one can obtain an accurate but approximate analytic solution to the electrostatic problem which will indicate how all the device parameters interact.

In this chapter I take just such an approach. The charge distributions and potential under a CCD gate are assumed to be one dimensional. As we will see this approximation makes it possible to obtain interesting and very useful results for the electrostatics of the buried channel device. While these results are very useful, they are not accurate enough for our considerations of the charge transfer and we will present a numerical solution of the electrostatic problem in two dimensions in the **chapter 4**.

To be specific we will consider only a p-channel device. However, n-channel could be done in exactly the same way.

This chapter is organized according to the following format. In 1.2 the problem is set up with the definition of charge densities and relevant geometrical parameters assuming a uniform doping profile. The solution to this problem in terms of charge stored Q , gate voltage ϕ_G , and the potential of the buried channel ϕ_m are presented in 1.3 within the depletion approximation. The implication of these results in the design of buried channel CCD's is given in the following three sections 1.4, 1.5, and 1.6. The changes in these parameters brought about changing the doping profile from uniform to Gaussian in the

region near the oxide is discussed in section 1.7. Section 1.8 contains the conclusion.

1.2 Electrostatic Potential and Charge Distribution

The one dimensional geometric structure for a buried p-channel charge coupled device is illustrated in Fig. 1.5a. The structure consists of a metal gate followed by a layer of silicon dioxide which rests on silicon that has been doped p-type near the surface on a n-type substrate. The potential energy versus position is shown in Fig. 1.5b. Throughout this discussion we will reference all potentials to the Fermi level in the n-type substrate. Since we will be dealing with holes throughout this problem, we will take the electrostatic potential to be positive in the standard sense, that is, the potential will increase downward on the figure. As a consequence of this definition, the position of the conduction edge in eV is given by ΔE such that

$$\Delta E = \phi - E_C > 0$$

E_V and E_C are the respective values of the band edges referenced to the potential zero, $\phi = 0$, far into the substrate. We note that $E_C = -\Delta E$ deep in the substrate since $\phi = 0$. The electrostatic problem is further specified by giving various contributions to the charge density. The free carrier densities for electrons and holes are given by

$$n = N_C \exp \left[\frac{E_C - \phi_n}{kT} \right], \quad (1-1a)$$

and

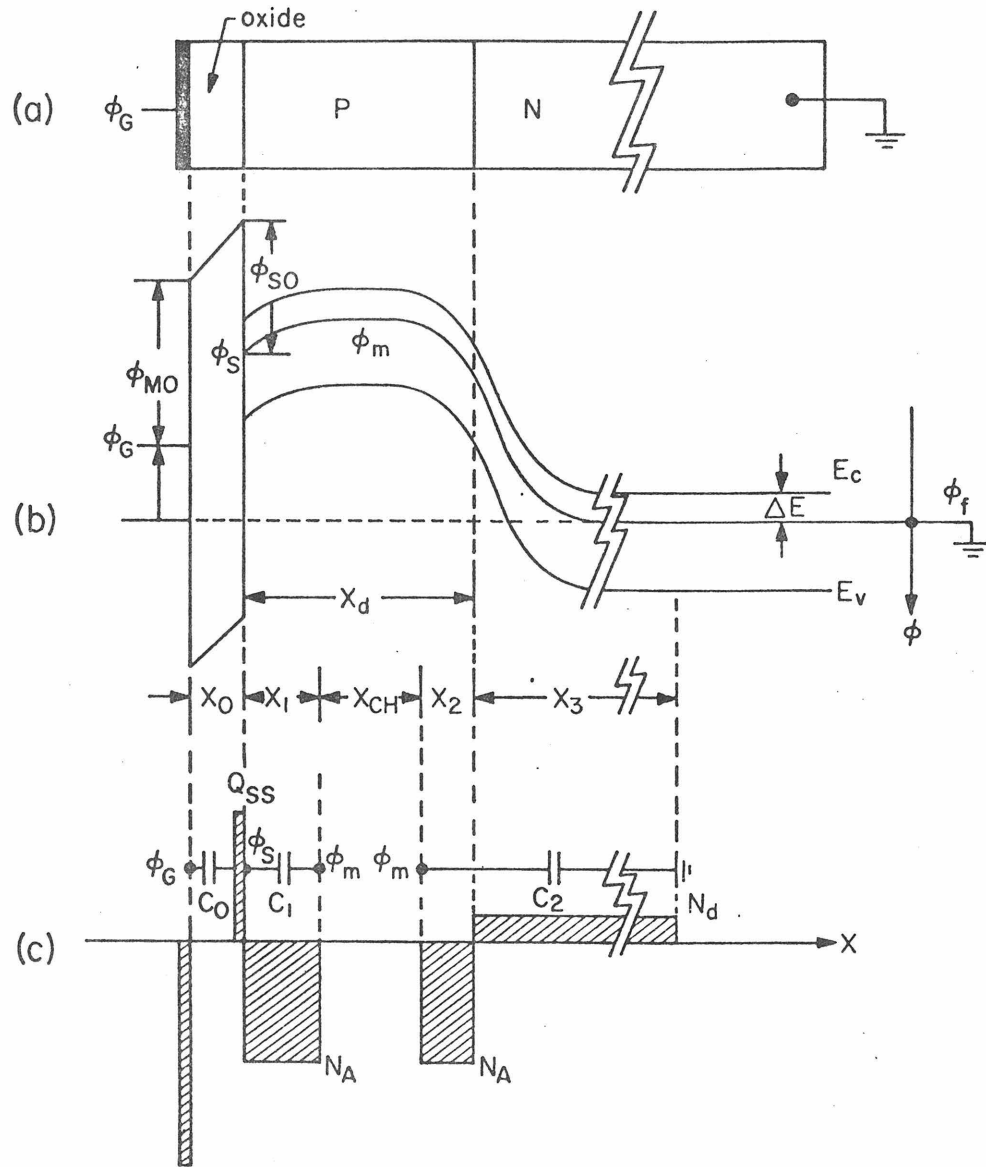


Fig. 1.5 (a) MOS Structure for buried channel CCD, (b) the band and electrostatic potential profiles, and (c) the charge distribution.

$$p = N_V \exp \left[\frac{\phi_p - E_V}{kT} \right], \quad (1-1b)$$

where N_C and N_V are the effective densities of states in the conduction and valence bands, respectively; and ϕ_n and ϕ_p are the quasi-Fermi levels within the semiconductor.

Further we need to specify the position of the zero of potential (the Fermi level) with respect to the band edges. Using the standard results for a semiconductor doped to a level N_D , we have the deviation of the conduction band edge ΔE .

To accomplish this, we note that $E_C = -\Delta E$ deep in the substrate, and we define the intrinsic electron or hole density n_i deep in the substrate by

$$n_i^2 = np = N_C N_V \exp \left(\frac{E_C - E_V}{kT} \right) \quad (1-2a)$$

Then, after a little algebra, using the relation $N_D = p-n$, with Eqs. (1-1a) and (1-1b) we obtain the difference ΔE in term of the substrate doping N_d as seen by

$$\Delta E = \phi_0 + kT \ln \left(\frac{N_C}{n_i} \right), \quad (1-3a)$$

where ϕ_0 is defined by

$$\phi_0 = kT \ln \left[\frac{N_d}{2n_i} + \sqrt{1 + \left(\frac{N_d}{2n_i} \right)^2} \right] \quad (1-3b)$$

The derivation is as following:

We observe in Fig. 1.5b that the curves for the conduction band, E_C , and the electrostatic potential, ϕ , run parallel to each other, and that

the displacement, ΔE , is a constant quantity everywhere in the semiconductor. We calculate the value of ΔE deep in the substrate therefore, where we observe that $\phi_n = \phi_p = \phi = 0$. Hence, using the relation $N_d = p - n$, with Eqs. (1-1a) and (1-1b) we obtain an equation which relates the conduction band E_C and valence band E_V deep in the substrate as seen by

$$N_d = p - n = N_V \exp\left(\frac{-E_V}{kT}\right) - N_C \exp\left(\frac{E_C}{kT}\right)$$

Eliminating E_V from this equation by Eq. (1-2a), we obtain an equation for E_C as seen by

$$\frac{N_C N_d}{n_i^2} = \exp\left(\frac{-E_C}{kT}\right) - \left(\frac{N_C}{n_i}\right)^2 \exp\left(\frac{E_C}{kT}\right)$$

Then, noting that deep in the substrate $\Delta E = -E_C$, this equation gives ΔE in terms of the substrate doping N_d and the intrinsic semiconductor parameters N_C and n_i as seen in Eq. (1-3a) with ϕ_0 defined by Eq. (1-3b).

END OF DERIVATION

This quantity ϕ_0 can be used to write the electron and hole densities in a symmetric form and we obtain, after some manipulation, by using Eqs. (1-1) and (1-2),

$$n = n_i \exp\left[\frac{(\phi - \phi_0) - \phi_n}{kT}\right], \quad (1-4a)$$

and

$$p = n_i \exp\left[\frac{\phi_p - (\phi - \phi_0)}{kT}\right]. \quad (1-4b)$$

The derivation is as following:

From Eq. (1-3a) with $\Delta E = \phi - E_C$ we obtain

$$kT \ln \left(\frac{N_C}{n_i} \right) = \phi - E_C - \phi_0 \quad .$$

That is,

$$N_C \exp(E_C/kT) = n_i \exp \left(\frac{\phi - \phi_0}{kT} \right)$$

Including ϕ_n in both sides we obtain Eq. (1-4a) from Eq. (1-1a).

If we apply Eq. (1-2a) to the above equation we obtain

$$\left(\frac{n_i^2}{N_V} \right) \exp(E_V/kT) = n_i \exp \left(\frac{\phi - \phi_0}{kT} \right) \quad .$$

This gives

$$N_V \exp(-E_V/kT) = n_i \exp \left(\frac{\phi_0 - \phi}{kT} \right) \quad .$$

Including ϕ_p in both sides we obtain Eq. (1-4b) from Eq. (1-1b).

END OF DERIVATION

With these equations (1-4a) and (1-4b) for the electron and hole densities we can write the one dimensional Poisson equation as

$$\frac{d^2 \phi}{dx^2} = - \frac{1}{\epsilon_{Si}} \left[p(\phi, \phi_p) - n(\phi, \phi_n) + d(x) \right] \quad , \quad (1-5)$$

where we denote the impurity doping concentration in the semiconductor by $d(x)$, and the dependence of the hole and electron densities upon

the potential ϕ and the quasi-fermi levels ϕ_p and ϕ_n is indicated explicitly by means of Eq. (1-4), and we note that the impurity doping concentration $d(x)$ is a positive quantity in the n-type substrate and negative in the p-diffusion region. Specifically, $d(x) = N_d$ deep in the substrate, but we consider the doping to be not necessarily uniform in the vicinity of the p-diffusion layer. It can be a Gaussian in particular.

When the minority carriers are neglected, the Poisson equation in the n-type substrate can be approximated by

$$\frac{d^2\phi}{dx^2} = -\frac{1}{\epsilon_{Si}} \left[d(x) - n(\phi, \phi_n) \right] \quad (1-6a)$$

Correspondingly, when the electron concentration is neglected in the p-diffusion layer, we obtain

$$\frac{d^2\phi}{dx^2} = -\frac{1}{\epsilon_{Si}} \left[d(x) + p(\phi, \phi_p) \right] \quad (1-6b)$$

where ϵ_{Si} is the semiconductor dielectric constant.

We have now set up the problem with the definition of charge densities and relevant geometrical parameters. One more point, however, remains to be made clear before considering the implications of this problem. It is about the relation between the built-in voltage ϕ_B of the p-n junction and the minimum potential ϕ_m of the potential well.

For the uniformly doped abrupt p-n junction shown in Fig. 3.1c at the thermal equilibrium, the minimum potential ϕ_m in the p-diffusion layer is equal to the built-in voltage of the p-n junction which is given by depletion approximation as

$$\phi_B = kT \ln \left(\frac{N_A N_d}{n_i^2} \right) \quad (1-7)$$

However, the presence of the signal charge Q and the gate voltage ϕ_G control the actual value of the minimum potential ϕ_m . We will study this effect by applying depletion approximation to the one dimensional MOS structure for the uniformly doped abrupt p-n junction doping profile. That is, $d(x) = N_d$ in the substrate and $d(x) = -N_A$ in the p-diffusion layer. The expression for ϕ_m will be obtained accordingly.

1.3 Depletion Approximation

We define x-coordinate along the depth of the semiconductor as indicated in Fig. 1.5c by the horizontal line. The origin of x-coordinate is taken to be at the oxide-semiconductor interface. That is, the p-diffusion region is defined as $0 < X < X_d$. The problem is to obtain an expression for the minimum potential ϕ_m in terms of the gate voltage ϕ_G and the signal charge Q which is defined as

$$Q = N_A X_{CH} = N_A (X_d - X_1 - X_2) \quad (1-8a)$$

where N_A is the p-channel doping density, X_{CH} is the width of the channel, X_d the p-layer depth. X_1 and X_2 are the surface field and metallurgical junction depletion widths respectively. These parameters are seen in Fig. 1.5c.

Corresponding to X_1 and X_2 , we define the respective depletion capacitance as $C_1 = \epsilon_{Si}/X_1$ and $C_2 = \epsilon_{Si}/X_2$ where ϵ_{Si} is the silicon dielectric constant.

The gate voltage ϕ_G controls the surface electric field E_s at the oxide-semiconductor interface, which is related to the oxide electric field by Gauss's law. The oxide electric field is given by the potential drop across the oxide divided by the oxide thickness X_0 . And the potential drop is given by the difference of the gate voltage ϕ_G and the surface potential ϕ_s adjusted by the metal-oxide work function ϕ_{MO} and the oxide-semiconductor barrier height ϕ_{SO} as illustrated in Fig. 1.5b. These simple facts lead to a relation between E_s and ϕ_s .

Assuming the presence of positive interface charge Q_{SS} , we obtain

$$\phi_s = \phi_{sF} - \frac{\epsilon_{Si} E_s}{C_0} \quad , \quad (1-8b)$$

where C_0 is the oxide capacitance per unit area, ϕ_s the surface potential. ϕ_{sF} is defined by

$$\phi_{sF} \equiv \phi_G - \phi_{MO} + \phi_{SO} + \frac{Q_{SS}}{C_0} \quad . \quad (1-8c)$$

We note ϕ_{sF} is the surface potential when the band is flat at the interface, that is when $E_s = 0$. Equation (1-8b) gives one boundary condition for the Poisson equation (1-6b) in the p-diffusion layer.

Integrating Poisson equation from $X = 0$ to $X = X_1$, that is, in the surface field induced depletion region, we obtain

$$E_s = \left(\frac{N_A}{\epsilon_{Si}} \right) X_1 \quad , \quad (1-8d)$$

and

$$\phi_m = \phi_s - \left(\frac{\epsilon_{Si}}{2N_A} \right) E_s^2 \quad , \quad (1-8e)$$

where X_1 is the surface field induced depletion width. The p-side and n-side junction depletion width must be connected by the relation

$X_2 N_A = X_3 N_d$ because of charge neutrality deep in the substrate. The p-side junction depletion width X_2 can be written in terms of the minimum potential ϕ_m as seen by

$$\frac{X_2}{X_d} = \sqrt{\frac{-\phi_m}{\phi_q}} \quad , \quad (1-8f)$$

where

$$\phi_q = \frac{N_A X_d^2}{2\epsilon_{Si}} \left[1 + \frac{N_A}{N_d} \right] \quad . \quad (1-8g)$$

If the value of the minimum potential ϕ_m is known, we first obtain the p-n junction depletion width ($X_2 + X_3$) from Eq. (1-8f) and then Eq. (1-8g). If the amount of the signal charge Q is prescribed, Eq. (1-8a) gives the surface field induced depletion width X_1 . Then the surface electric field E_s , and then the surface potential ϕ_s , can be calculated from Eq. (1-8d) and (1-8e) respectively. The corresponding gate voltage ϕ_G can be evaluated from Eq. (1-8b) knowing the relation between the gate voltage ϕ_G and ϕ_{SF} as seen in Eq. (1-8c).

In those equations there are four fixed parameters, X_0 , X_d , N_A , and N_d that can be controlled in the fabrication of device, and three more variables, Q , ϕ_m , and ϕ_{SF} among which there is only one constraint during the device operations. The associated constraint among the three variables can be written as an expression of the minimum potential ϕ_m in terms of the gate voltage ϕ_{SF} and the signal charge Q . In the following, the procedure to calculate the expression is described.

To write the analytic expression for the minimum potential as simple as possible, we introduce three parameters, ϕ_t , ϕ_d and R defined by

$$\phi_t = \frac{N_A \epsilon_{Si}}{2 C_o^2} \quad , \quad (1-9a)$$

$$\frac{\phi_d}{\phi_t} = \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d}\right) \left[2 + \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d}\right)\right] \quad , \quad (1-9b)$$

and

$$R = \frac{N_A \phi_d - \phi_{sF}}{2N_d \phi_d + \phi_t} \quad , \quad (1-9c)$$

with $Q_d \equiv N_A X_d$ and $C_d = \epsilon_{Si}/X_d$. ϕ_t is just a geometrical constant (in volt) determined by the p-channel doping density N_A and the oxide capacitance C_o . ϕ_d is proportional to ϕ_t and the proportionality constant given in Eq. (1-9b) is actually a quadratic function of the single charge Q . The dimensionless constant R is of the order of 10 to 20 in normal device configurations because N_A is 10 to 20 times larger than the substrate doping N_d . The physical significance of these parameters, ϕ_t , ϕ_d and R are explained more in detail as we go further in interpretation and results of depletion approximation in next section.

In terms of these parameters, the minimum potential ϕ_m can be expressed as

$$\phi_m(Q, \phi_{sF}) = - \left(1 + \frac{N_d}{N_A}\right) \left[\phi_d - \phi_{sF}\right] f(R) \quad , \quad (1-10a)$$

where $f(R)$ is a slowly varying function of R and defined by

$$f(R) = \frac{R}{1 + R + \sqrt{1 + 2R}} \quad . \quad (1-10b)$$

The derivation is as following:

Eq. (1-8a) with $Q_d = N_A X_d$ gives

$$\frac{Q}{Q_d} = 1 - \left(\frac{X_1}{X_d}\right) - \left(\frac{X_2}{X_d}\right)$$

With Eq. (1-8f) for X_2/X_d we obtain

$$-\frac{\phi_m}{\phi_q} = \left[\left(1 - \frac{Q}{Q_d}\right) - \left(\frac{X_1}{X_d}\right) \right]^2 \quad (*)$$

Also from Eq. (1-8e) substituting ϕ_s by Eq. (1-8b) and X_1 by Eq. (1-8d) we obtain

$$\phi_m = \phi_{sF} - \left(\frac{N_A X_d}{C_o}\right) \left(\frac{X_1}{X_d}\right) - \frac{N_A X_d^2}{2 \epsilon_{si}} \left(\frac{X_1}{X_d}\right)^2$$

Using Eq. (1-9a) for ϕ_t and $C_d = \epsilon_{si}/X_d$ we obtain

$$\phi_m = \phi_{sF} - 2\phi_t \left(\frac{C_o}{C_d}\right) \left(\frac{X_1}{X_d}\right) - \phi_t \left(\frac{C_o}{C_d}\right)^2 \left(\frac{X_1}{X_d}\right)^2$$

This equation and Eq. (*) above give

$$\begin{aligned} \left(\frac{X_1}{X_d}\right)^2 &= -\frac{\phi_m}{\phi_q} + 2\left(1 - \frac{Q}{Q_d}\right) \left(\frac{X_1}{X_d}\right) - \left(1 - \frac{Q}{Q_d}\right)^2 \\ &= \left(\frac{C_d}{C_o}\right)^2 \left\{ \frac{\phi_{sF} - \phi_m}{\phi_t} \right\} - 2\left(\frac{C_d}{C_o}\right) \left(\frac{X_1}{X_d}\right) \end{aligned}$$

Solving for X_1/X_d we obtain

$$2 \left[\left(1 - \frac{Q}{Q_d} \right) + \frac{C_d}{C_o} \right] \left(\frac{X_1}{X_d} \right) = \left(1 - \frac{Q}{Q_d} \right)^2 + \left(\frac{C_d}{C_o} \right)^2 \left[\frac{\phi_s F^{-\phi_m}}{\phi_t} \right] + \left(\frac{\phi_m}{\phi_q} \right)$$

Substituting X_1/X_d of the above equation to Eq. (*) we obtain

$$- \frac{\phi_m}{\phi_q} = \left\{ \left(1 - \frac{Q}{Q_d} \right) - \frac{\left(1 - \frac{Q}{Q_d} \right)^2 + \left(\frac{C_d}{C_o} \right)^2 \left[\frac{\phi_s F^{-\phi_m}}{\phi_t} \right] + \left(\frac{\phi_m}{\phi_q} \right)}{2 \left[\left(1 - \frac{Q}{Q_d} \right) + \frac{C_d}{C_o} \right]} \right\}^2$$

This equation can be rearranged to give

$$- 4 \left[\left(1 - \frac{Q}{Q_d} \right) + \frac{C_d}{C_o} \right]^2 \left(\frac{\phi_m}{\phi_q} \right) = \left\{ \left(1 - \frac{Q}{Q_d} \right) \left[\left(1 - \frac{Q}{Q_d} \right) + \frac{2C_d}{C_o} \right] - \left(\frac{C_d}{C_o} \right)^2 \left[\frac{\phi_s F^{-\phi_m}}{\phi_t} \right] - \left(\frac{\phi_m}{\phi_q} \right) \right\} \quad .(**)$$

Knowing from Eq. (1-9b) that

$$\left(1 + \frac{\phi_d}{\phi_t} \right) = \left[1 + \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d} \right) \right]^2$$

the LHS of the above equation (**) becomes

$$- 4 \left(\frac{C_d}{C_o} \right)^2 \left(1 + \frac{\phi_d}{\phi_t} \right) \left(\frac{\phi_m}{\phi_q} \right)$$

Also substituting ϕ_d of Eq. (1-9b) into the RHS of Eq. (**), we can write the RHS of Eq. (**) as seen by

$$\left\{ \left(\frac{C_d}{C_o} \right)^2 \frac{\phi_d}{\phi_t} - \left(\frac{C_d}{C_o} \right)^2 \left(\frac{\phi_{SF} - \phi_m}{\phi_t} \right) - \left(\frac{\phi_m}{\phi_q} \right) \right\}^2$$

Consequently the Eq. (**) above becomes

$$\begin{aligned} & - 4 \left(1 + \frac{\phi_d}{\phi_t} \right) \left(\frac{\phi_m}{\phi_q} \right) \\ & = \left\{ \left(\frac{C_d}{C_o} \right) \left(\frac{\phi_d - \phi_{SF}}{\phi_t} \right) + \left\{ \frac{C_d}{C_o \phi_t} - \frac{C_o}{C_d \phi_q} \right\} \phi_m \right\}^2 \quad (****) \end{aligned}$$

Furthermore noting by Eq. (1-8g) and Eq. (1-9a) that

$$\left(\frac{C_d}{C_o \phi_t} \right) - \left(\frac{C_o}{C_d \phi_q} \right) = \left(\frac{C_d}{C_o \phi_t} \right) \frac{1}{(1 + N_d/N_A)}$$

the RHS of this equation (***) becomes

$$\left(\frac{\phi_d - \phi_{SF}}{\phi_t} \right)^2 \left(\frac{C_d}{C_o} \right)^2 \left[1 + \frac{\phi_m}{(1 + N_d/N_A) (\phi_d - \phi_{SF})} \right]^2$$

Knowing from Eq. (1-8g) and (1-9a) that

$$\left(\frac{\phi_t}{\phi_q}\right)\left(\frac{C_o}{C_d}\right)^2 = \left(\frac{N_d}{N_A}\right) \frac{1}{(1 + N_d/N_A)}$$

and defining the parameter f by the equation as seen by

$$f = \frac{-\phi_{fil}}{(1 + N_d/N_A)(\phi_d - \phi_{SF})} \quad (****)$$

the above equation (***) can be written as

$$\frac{2f}{R} = (1 - f)^2 \quad (*****)$$

where R is given by Eq. (1-9c).

Solving this equation for $f(R)$ in terms of R we obtain the Eq. (1-10b). Since $f(R)$ is originally defined by the Eq. (****) above, we immediately obtain the analytic expression for the minimum potential ϕ_m as seen by Eq. (1-10a). In the above derivations, the four equations (*), (**), (***) and (*****) are all the same relation expressed in terms of different physical parameters, and the parameters R and $f(R)$ seem to play very important roles in studying the mutual interactions among the important device parameters such as the oxide thickness X_o , the p-layer diffusion depth X_d , the p-layer doping N_A , and the substrate doping N_d ; and the three more variables, Q , ϕ_{SF} , and ϕ_m .

END OF DERIVATION

For large values of R , $f(R)$ approaches unity very slowly. If we want to know a rough value of the minimum potential without going through the calculation procedure defined by Eqs. (I-9) and (I-10), we can estimate the value by computing ϕ_d from Eq. (I-9b) and setting $\phi_m \approx -(\phi_d - \phi_{SF})$, where we note the gate voltage ϕ_G is related to ϕ_{SF} by Eq. (I-8c).

The general characteristics of the physical parameters implied in the analytic expression for the minimum potential can be seen by the relationships implied in the above equations. It is clear from Eq. (I-10a) that the dependence of the minimum potential ϕ_m upon the gate voltage is quite linear. On the other hand because ϕ_d defined by Eq. (I-9b) depends quadratically upon the signal charge, we expect that the minimum potential will also show a quadratic dependence on the signal charge. We also note that a thicker oxide produces a deeper minimum potential. This effect can be calculated quantitatively by Eq. (I-9a) in which we see the value of ϕ_t is proportional to the square of the oxide thickness. For a given gate voltage, the minimum potential is different for different oxide thicknesses, because the value of ϕ_d will be different. But ϕ_d does not depend on ϕ_{SF} or on the gate voltage. Hence we observe, when two MOS structures with different oxide thickness are given, the difference of the minimum potentials will not depend appreciably upon the gate voltage applied on both structures. These observations are important in designing a working buried channel CCD and clocking schemes, and so we will discuss these points more clearly in detail in the next section.

1.4 Interpretation and Results of Depletion Approximation

We first describe qualitatively how the parameters ϕ_t and ϕ_d depend on the oxide thickness X_o and the signal charge Q . This consideration is important to describe qualitatively how the minimum potential ϕ_m depends on the salient physical parameters.

ϕ_d for two different values of oxide thickness is plotted in Fig. 1.6 as a function of the signal charge normalized by the maximum depletion charge $Q_d = N_A X_d$. In this case study, the p-channel depth X_d is taken to be 1μ and the p-channel doping density to be $20,000 \text{ e}/\mu^3$ which is equal to $2 \times 10^{16} \text{ e}/\text{cm}^3$. The silicon dielectric constant ϵ_{Si} is taken to be $11.7 \epsilon_0$ which is equal to $648 \text{ e}/\text{volt}\cdot\mu$ and the silicon oxide dielectric constant ϵ_{SiO_2} to be $3.9 \epsilon_0$ or $216 \text{ e}/\text{volt}\cdot\mu$.

Observe in Fig. 1.6 that the nonlinear dependence of ϕ_d prevails when more signal charge Q is present in the channel.

Knowing the value of ϕ_d , the difference $(\phi_{SF} - \phi_d)$ can be calculated for a given value of ϕ_{SF} . This difference is of the order of the minimum potential ϕ_m . Hence ϕ_d gives a rough estimate of the voltage drop of the minimum potential ϕ_m relative to the gate voltage (ϕ_{SF}) . Specifically, Fig. 1.6 shows for zero gate voltage $(\phi_{SF} = 0)$ and the zero signal charge $(Q = 0)$, the channel potential is rough -45 volt for $X_o = 0.32\mu$ and -25 volt for $X_o = 0.12\mu$. Hence the thicker the oxide, the lower the channel potential for the charge carriers.

In Fig. 1.7, ϕ_t and ϕ_d are plotted against the oxide thickness for zero-signal charge. As seen in the figure, and as one can easily see from Eq. (1-9b) when ϕ_d is expressed in terms of X_o , ϕ_d is a linear

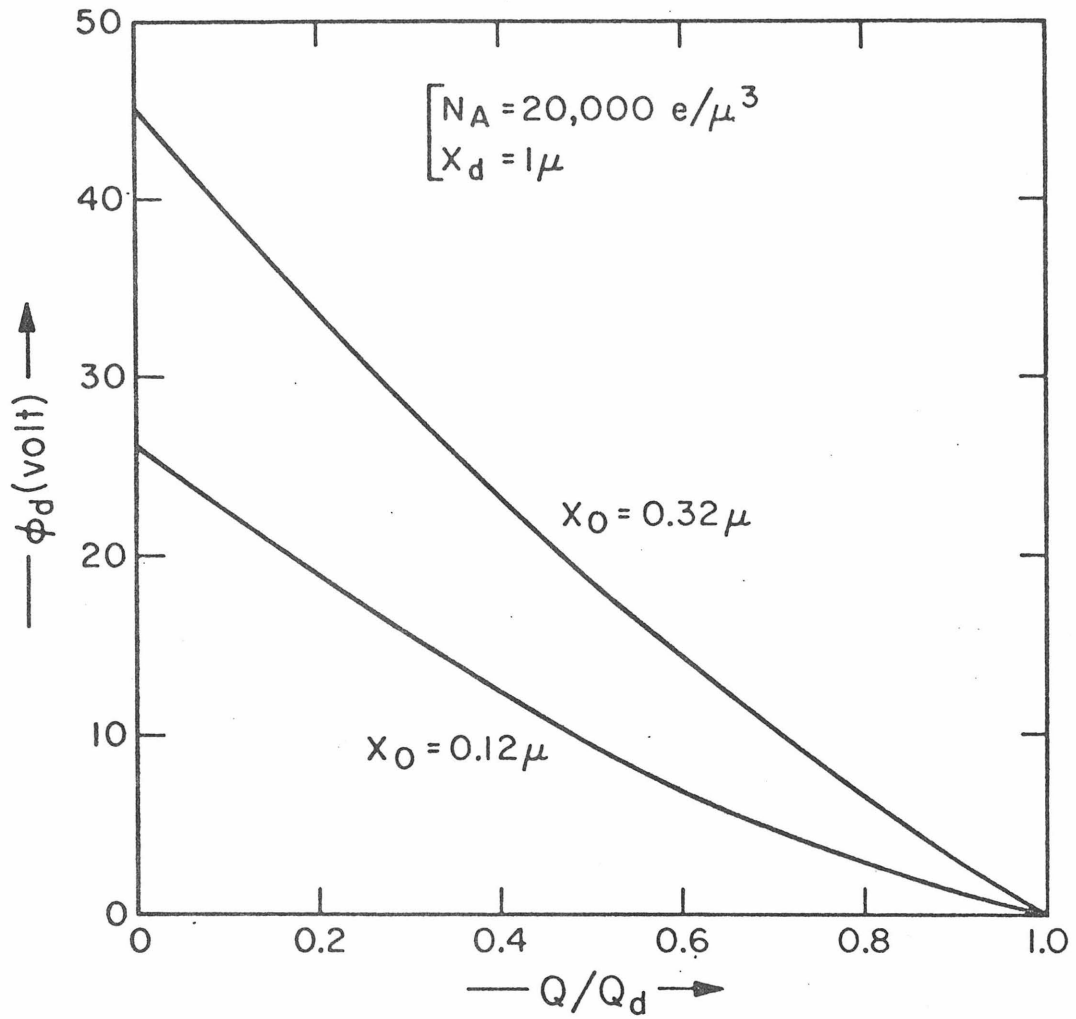


Fig. 1.6 ϕ_d defined by Eq. (1-9b) plotted against the signal charge Q normalized by the sheet doping density Q_d in the p-layer for the oxide thickness X_0 of 0.12μ and 0.32μ .

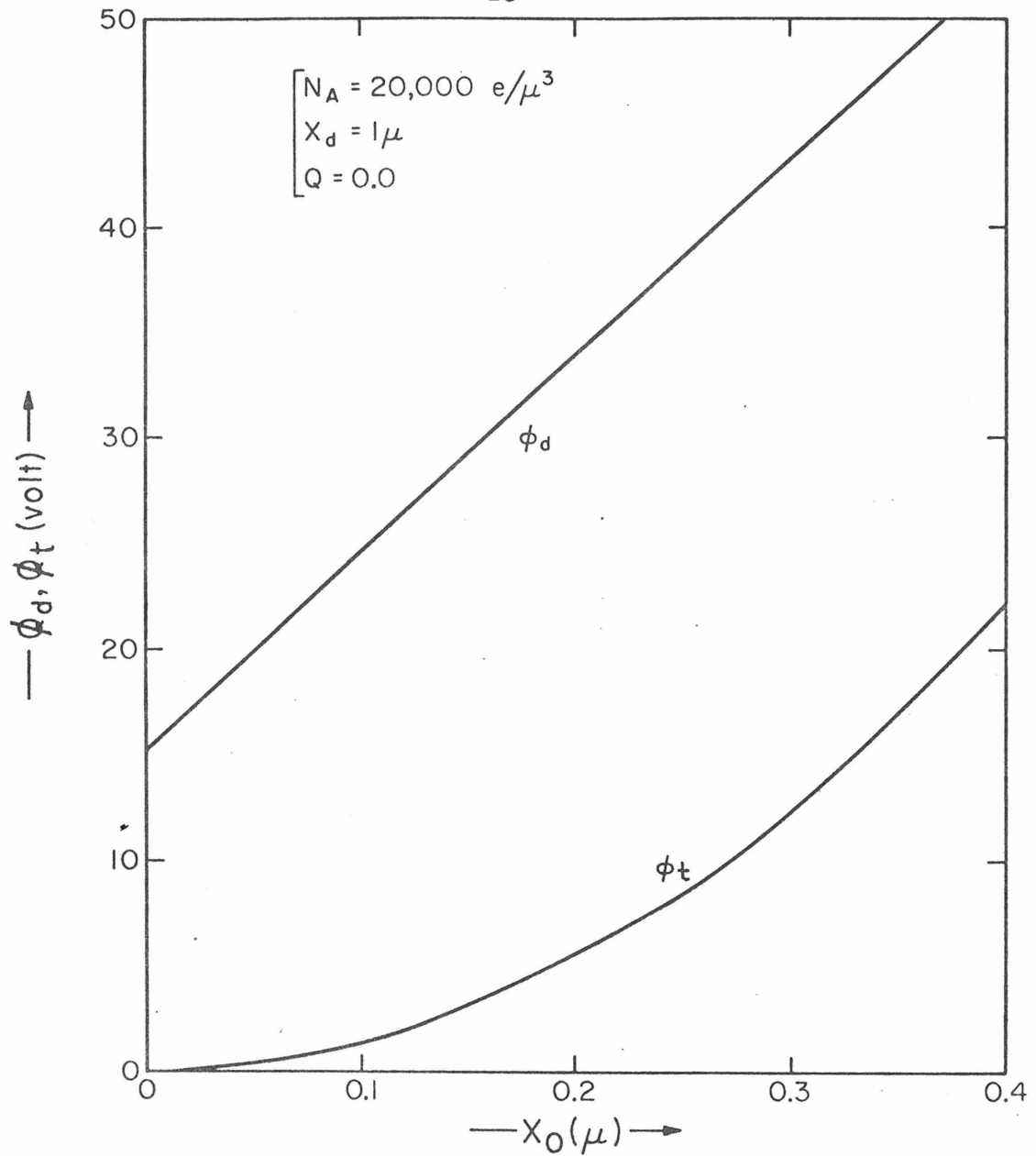


Fig. 1.7 The dependence of the parameters ϕ_d and ϕ_t defined by Eq. (1-9a) and Eq. (1-9b) upon the oxide thickness X_0 is illustrated in the figure.

function of the oxide thickness when no signal charge is present. As a matter of clarity, for $Q = 0$ from Eq. (1-9b), we obtain

$$\frac{\phi_d}{\phi_t} = \frac{1}{C_o} + \frac{1}{2C_d} \quad (1-10c)$$

The linear dependence of ϕ_d upon the oxide thickness X_o also implies qualitatively the linear dependence of the minimum potential ϕ_m , upon X_o . The quadratic dependence of ϕ_t upon the oxide thickness X_o is clear from Fig. 1.7 and also from Eq. (1-9a).

We have shown how the parameters ϕ_t and ϕ_d depend quantitatively on the oxide thickness and the signal charge, and also described qualitatively how the minimum potential ϕ_m depends on these parameters. As for Eq. (1-10a) we have considered only for the factor $(\phi_{SF} - \phi_d)$ and if we wish to have a more accurate value, we can calculate the value of R from Eq. (1-9c) to obtain the correction factor $f(R)$ for the minimum potential. But this correction is only about 10 ~ 20% of the first rough estimate. This point can be made clear as we consider the actual values of R and $f(R)$ as follows.

For the range of interest, the values of R will be between 5.0 and 50.0 as shown in Fig. 1.8a. In this figure, R is plotted against the normalized signal charge Q/Q_d for a pair of typical values of oxide thickness X_o and of ϕ_{SF} . Observe that the values of R may vary in a wide range but the corresponding factor $f(R)$ will be fairly constant as clearly seen in Fig. 1.8b when one compares Figs. 1.8a and 1.8b.

For a special case of interest with no signal charge present, the minimum potential is plotted against ϕ_{SF} for different oxide thickness

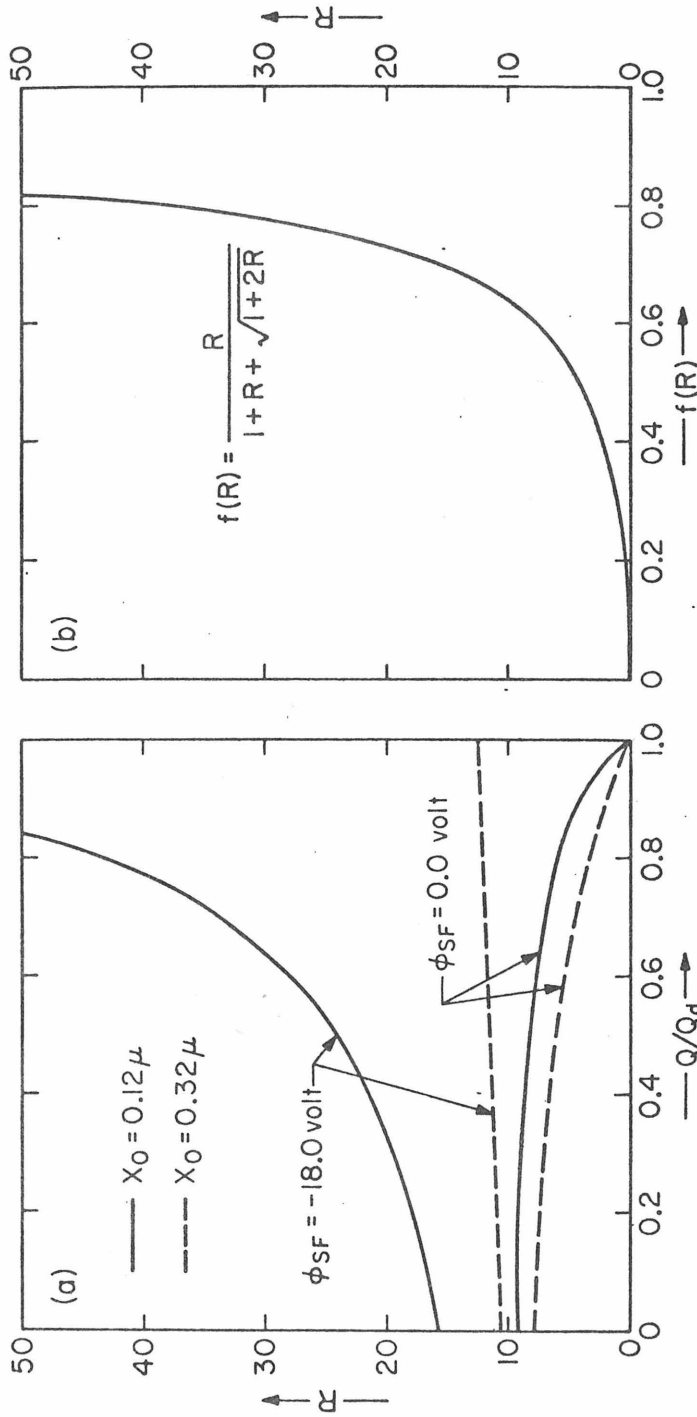


Fig. 1.8a The values of R defined by Eq. (1-9c) are plotted against Q/Q_d for typical values of oxide thickness X_0 and surface flat band voltage ϕ_{SF} corresponding to the gate voltage ϕ_G and the oxide thickness X_0 .

Fig. 1.8b The values of R and the function $f(R)$ defined by Eq. (1-10b) are plotted for a quick estimate of $f(R)$ for a given signal level Q/Q_d .

in Fig. 1.9. As we claimed earlier, note that the dependence of the minimum potential upon ϕ_{SF} (hence, upon the gate voltage) is quite linear. We also observe the lines are for practical purposes parallel. That is, the difference of the minimum potentials will not depend on the gate voltage applied on a pair of MOS structures with different oxide thickness.

In Fig. 1.10a, the dependence of the minimum potential upon the signal charge is illustrated for typical values of oxide thickness and gate voltages (actually ϕ_{SF}). The top two solid curves are for $\phi_{SF} = 0.0$ volt, and the bottom two for $\phi_{SF} = -18.0$ volt. These four curves define the minimum potential levels, that is, the four points at $Q = 0$ in the figure, which may be applied for two phase buried channel CCD operations. This point is discussed further in the next section and the full treatment of two phase buried channel CCD operations is given in the next chapter.

We are now in the position to discuss one of the most important aspects in the metal oxide semiconductor system for our one dimensional buried channel CCD structure, that is, the condition for zero surface electric field, or flat band.

The dashed curve in Fig. 10.a was obtained by calculating the values of the minimum potential as a function of the signal charge with the constraint that the surface electric field E_s is zero. That is, for the case of zero-depletion width X_1 by Eq. (3-8d), we obtain from Eqs. (1-8a) and (1-8f) after some manipulation for $E_s = 0$, that is, for $X_1 = 0$,

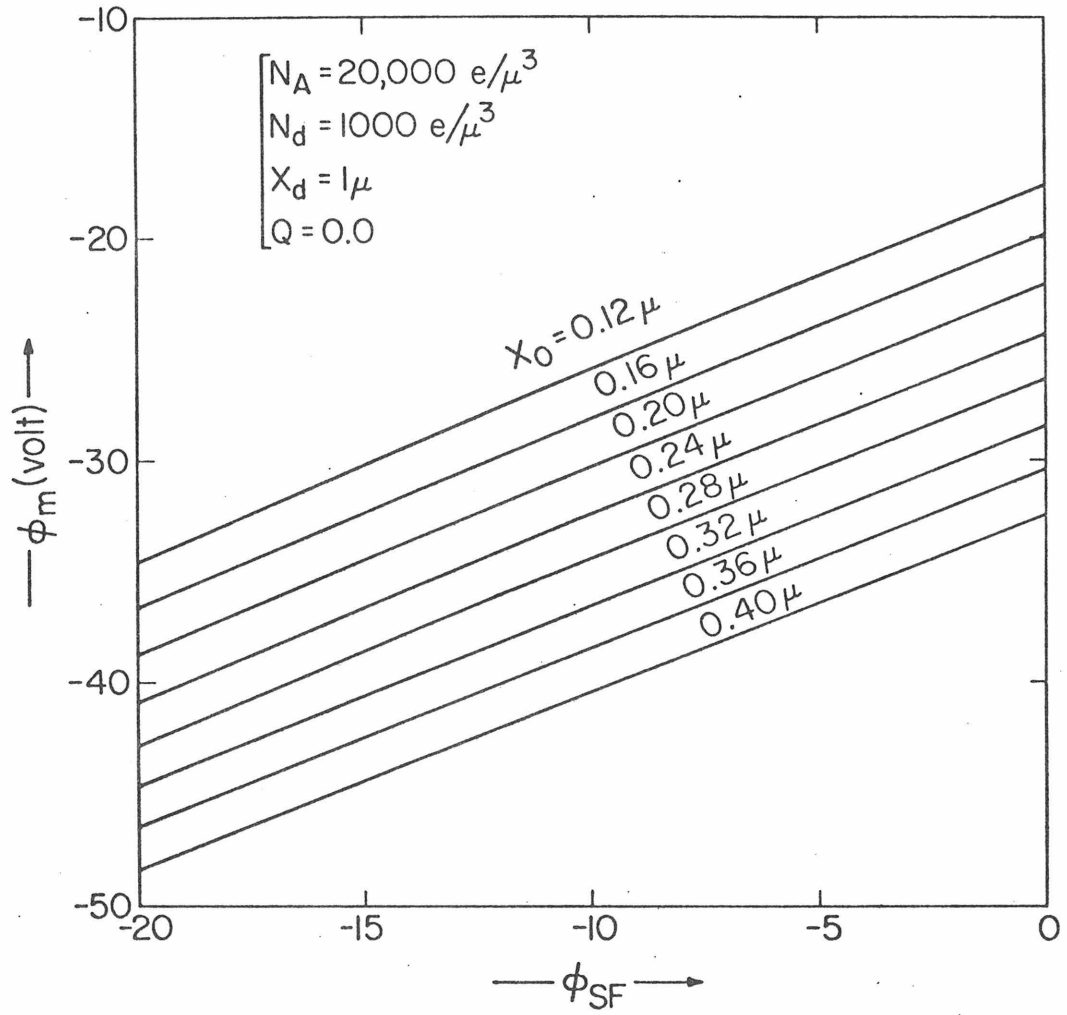


Fig. 1.9 The minimum potential ϕ_m plotted against ϕ_{SF} for various oxide thickness X_0 .

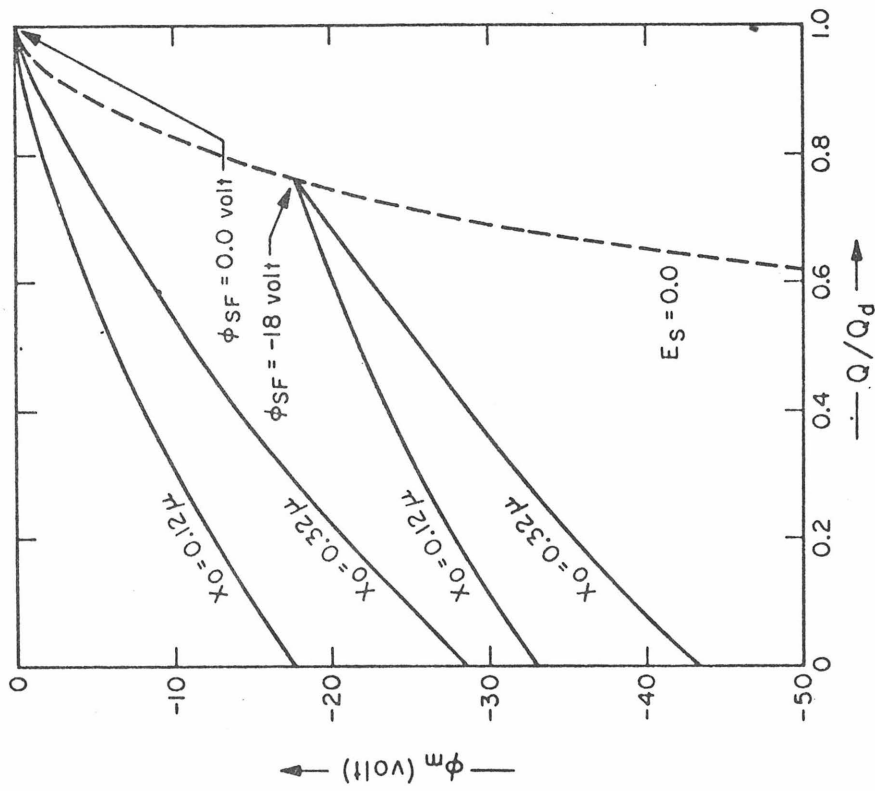
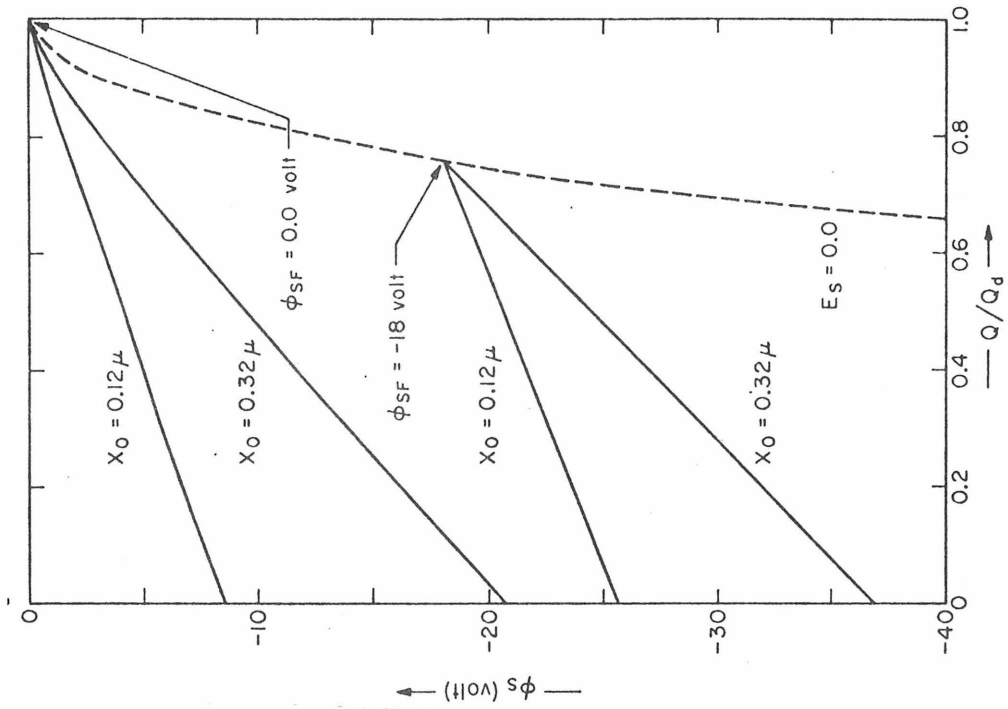


Fig. 1-10 The minimum potential ϕ_m plotted against the signal level Q/Q_d in (a), and ϕ_s in (b).

$$\phi_{sF} = \phi_m \Big|_{E_s=0} = - \left(1 - \frac{Q}{Q_d}\right)^2 \phi_q \quad (1-11a)$$

Recall that the parameter ϕ_q was originally introduced in Eq. (1-8f) to relate the *p*-side depletion width X_2 to the minimum potential ϕ_m . Here, we also note the band is flat at the semiconductor-oxide interface. Hence, we have $\phi_m = \phi_{sF}$. When the signal charge increases beyond the dashed curve, the signal charge will "touch" the oxide-semiconductor interface.

The surface electric field is zero and the band is flat when, for given gate voltage (ϕ_{sF}), the amount of the signal charge becomes, from the Eq. (1-11a) above,

$$Q \Big|_{E_s=0} = Q_d \left[1 - \sqrt{-\frac{\phi_{sF}}{\phi_q}} \right] \quad (1-11b)$$

When no signal charge is present ($Q = 0$), then from Eq. (3-11a) we note that the magnitude of the gate voltage ϕ_{sF} must be set equal to ϕ_q given by Eq. (1-11b). For the values used in the case study, this gives $\phi_{sF} = -\phi_q = -324$ volt for $E_s = 0$ and $Q = 0$. For this value of ϕ_{sF} , Eq. (1-11a) gives $Q = 0$. The dashed curve in Fig. 1.10a is given by Eq. (1-11a) and the values of the signal charge Q for $E_s = 0$ (calculated by Eq. (1-11b) for $\phi_{sF} = 0.0$ volt and -18 volt) give the two points that are arrowed in Fig. 1.10a.

The surface potential ϕ_s is plotted against signal level in Fig. 1.10b. Note the dependence of the surface potential upon the signal charge is quite linear as compared to the minimum potential. The slope is proportional to the oxide thickness X_0 and given by the

reciprocal of the oxide capacitance C_o . Note the pairs of lines for $X_o = 0.12$ and $X_o = 0.32$ are parallel to each other respectively. As we observe in the relation given by Eq. (1-8b), the surface potential depends on the surface electric field in a linear fashion. Hence we observe that the surface electric field is also a linear function of the signal charge Q in a good accuracy.

The surface electric field E_s is plotted in Fig.1.11. The slope is roughly the reciprocal of the silicon dielectric constant ϵ_{Si} . The analytic expression for the surface electric field is as messy as the one for the minimum potential ϕ_m . To complete the discussion, we present the expression anyway.

Define two parameters $A(Q)$ and $B(Q)$ as seen by

$$A(Q) = \left(1 + \frac{N_d}{N_A}\right) \left(1 - \frac{Q}{Q_d}\right) + \frac{N_d}{N_A} \frac{C_d}{C_o} \quad , \quad (1-11c)$$

and

$$B(Q) = \left(1 + \frac{N_d}{N_A}\right) \left[\left(1 - \frac{Q}{Q_d}\right)^2 + \frac{\phi_{sF}}{\phi_q} \right] \quad . \quad (1-11d)$$

Both $A(Q)$ and $B(Q)$ are functions of the signal charge Q . Then the surface electric field E_s can be calculated from the expression

$$E_s = \frac{AQ_d}{\epsilon_{Si}} \left[1 - \sqrt{1 - B/A^2} \right] \quad . \quad (1-11e)$$

The condition for zero surface electric field is $B(Q) = 0$. Then from Eq. (1-11d) we have the relation as seen in Eq. (1-11c). For the range of interest, the right factor in RHS of (1-11e) is fairly constant with values between 0.6 and 0.8 and the surface electric field is proportional to A , which is a linear function of the signal charge Q .

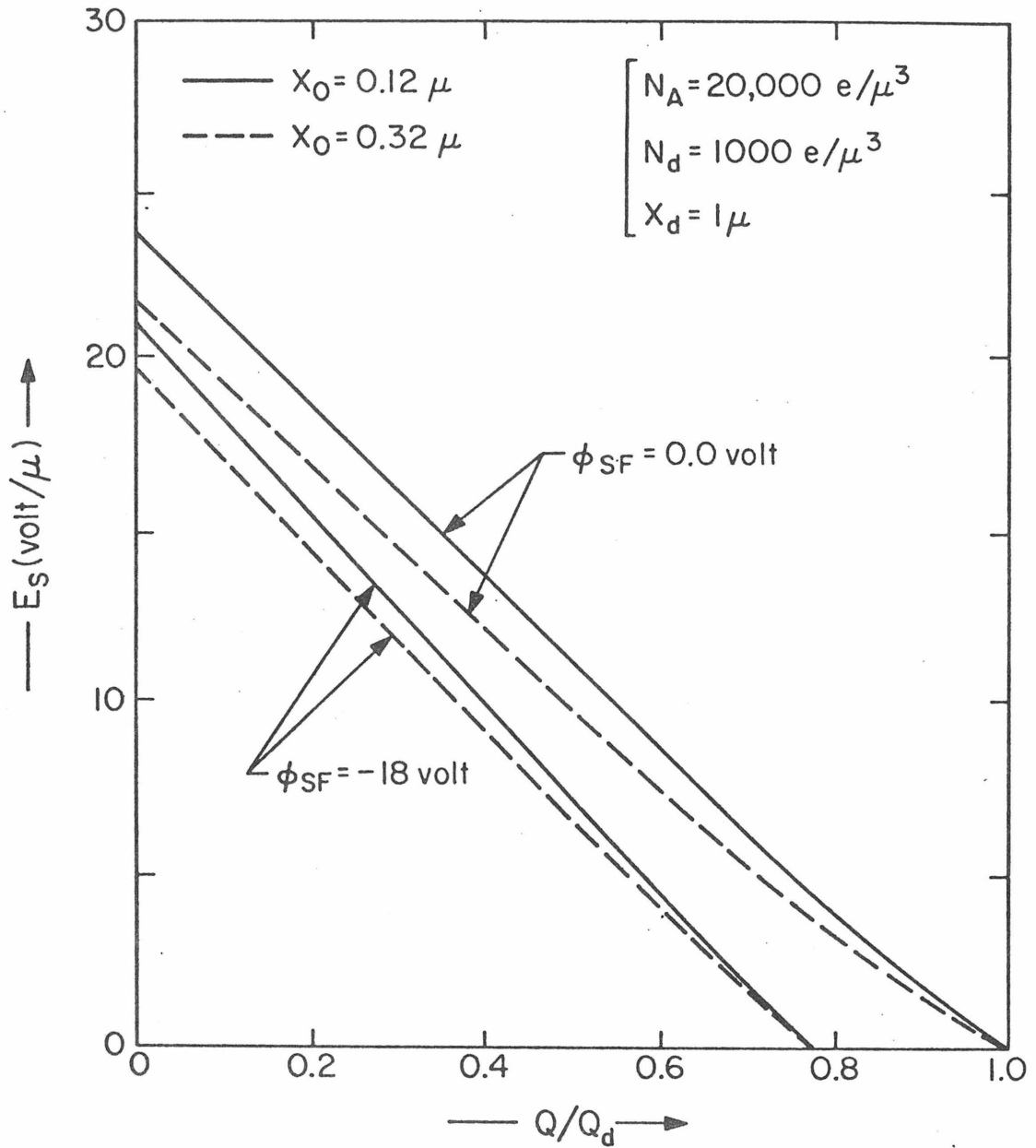


Fig. 1.11 The strength of the surface electric field E_s is plotted against the signal level Q/Q_d for typical values of the oxide thickness X_0 and the flat band voltage ϕ_{SF} corresponding to the gate voltage ϕ_G as related by Eq. (1-8c).

1.5 Constraints on Gate Voltage and Signal Charge

We are now in the position to describe the upper and lower bounds imposed on the minimum potential for normal device operations. Without this consideration, the device operation is practically impossible and the important results are summarized as a graphic illustration in Fig. 1.12.

We will first give the physical background for the upper and lower bounds and then derive the equations which represent the constraints between the gate voltage (ϕ_{SF}) and the signal charge Q for normal device operations. The conditions outside the normal device operations, that is, the accumulation and inversion conditions will then be discussed.

Returning to Fig.1.10a for $\phi_{SF} = 0.0$ volt, we observe the minimum potential approaches to zero as the amount of signal charge approaches the maximum possible capacity Q_d . However, we note the minimum potential must be always lower than the ground reference at least by the amount of the p-n junction built-in voltage ϕ_B given by Eq. (1-7). For our case study, $N_A = 20,000 \text{ e}/\mu^3$ and $N_D = 1000 \text{ e}/\mu^3$ and ϕ_B is about 0.63 volt. If the minimum potential is raised beyond this point by the excess signal charge, the p-n junction will be forward-biased momentarily and the signal charge will be dumped to the substrate as a current through the p-n junction.

To prevent the p-n junction from becoming forward-biased, the gate voltage and the signal charge must be controlled so that the minimum potential ϕ_m is always lower than the ground reference potential at least by ϕ_B . That is,

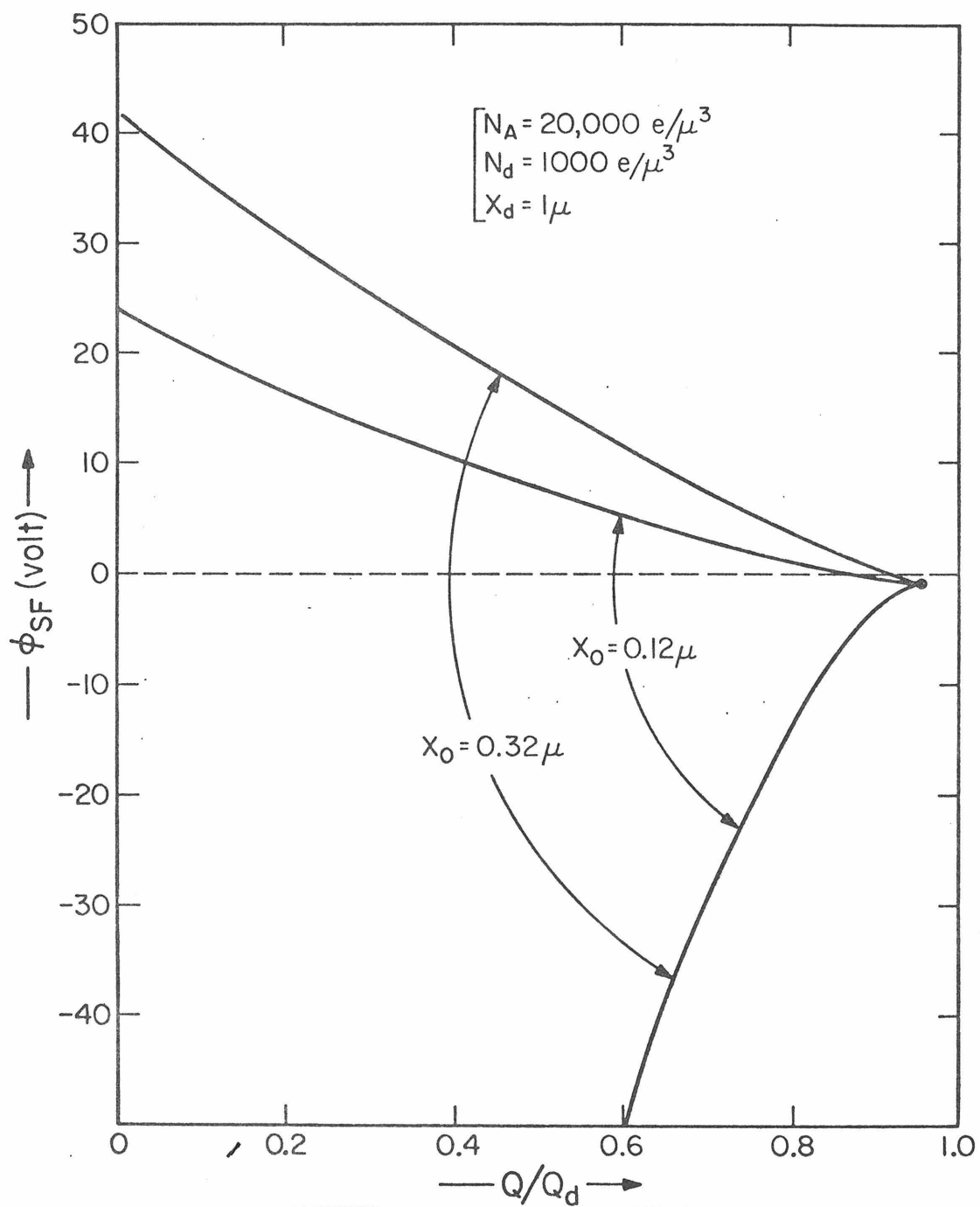


Fig. 1.12 The range of the permissible values of the gate voltage ϕ_G is implied by the flat band voltage ϕ_{SF} plotted against the signal level Q/Q_d for typical oxide thickness of 0.12μ and 0.32μ .

$$\phi_m(\phi_{SF}, Q) \leq -\phi_B \quad (1-12a)$$

On the other hand, when the surface electric field E_s becomes zero, the signal charge starts accumulating at the interface. Then, the trapping in interface states at the semiconductor oxide interface imposes limitations on the performance of CCD operations. To prevent the signal charge from "touching" the interface, we must have, referring to Eq. (1-11a) or Fig.1.10a and Fig.1.10b

$$\phi_m(\phi_{SF}, Q) \geq -\left(1 - \frac{Q}{Q_d}\right)^2 \phi_q \quad (1-12b)$$

From the above two equations, it is clear that we cannot have the signal charge Q equal to Q_d in any circumstances during CCD transfer operations.

Combining the constraints (1-12a) and (1-12b) we obtain

$$-\left(1 - \frac{Q}{Q_d}\right)^2 \phi_q \leq \phi_m \leq -\phi_B \quad (1-12c)$$

This inequality imposes a smaller upper bound than the previous one (Q_d) upon the signal charge Q . That is, we must always have $Q \leq Q_{MAX}$ where Q_{MAX} is defined as

$$Q_{MAX} \equiv Q_d \left[1 - \sqrt{\frac{\phi_B}{\phi_q}} \right] \quad (1-12d)$$

This condition, $Q \leq Q_{MAX}$, must be satisfied regardless of the gate voltage ϕ_{SF} . The signal charge must be always smaller than this value at least. (The gate voltage actually restricts the value of Q further into a narrow range.) For the case study in this presentation, Q_{MAX} is smaller than Q_d by 4.5% for $\phi_q = 308$ volt and $\phi_B = 0.63$ volt.

The problem is to rewrite Eqs. (1-12a) and (1-12b) in terms of the gate voltage ϕ_{SF} and the signal charge Q explicitly. When $\phi_m = -\phi_B$, we have a functional dependence between the signal charge Q and the gate voltage ϕ_{SF} . This functional relation gives the boundary for the range of Q and ϕ_{SF} constrained by Eq. (1-12a). The calculation is tedious but the result can be obtained by solving Eq. (1-8) for $\phi_m = -\phi_B$. And we obtain the constraint corresponding to Eq. (1-12a) as seen by

$$\phi_{SF} \leq \left[\frac{Q_{MAX} - Q}{C_o} \right] \left[1 + \left(\frac{C_o}{2C_d} \right) \frac{Q_{MAX} - Q}{Q_d} \right] - \phi_B \quad (1-13a)$$

This is the constraint to keep the signal charge from being washed away to the substrate. Note for the maximum signal charge $Q = Q_{MAX}$.

$$\phi_{SF} \leq -\phi_B.$$

The other constraint (1-12b) can be written simply as

$$\phi_{SF} \geq - \left(1 - \frac{Q}{Q_d} \right)^2 \phi_q \quad (1-13b)$$

because $\phi_{SF} = \phi_m$ for $E_s = 0$ as seen in Eq. (1-11a).

These **formulations** are very important when one is involved in designing a working buried channel CCD structure. Figure 1.12 shows the range of the permissible values of ϕ_{SF} and Q . The boundary lines can be obtained from Eqs. (1-13a) and (1-13b). Observe the oxide capacitance C_o appears in the expression (1-13a) but the lower bound for ϕ_{SF} which is given by Eq. (1-13b) does not depend on the oxide thickness. These characteristics are clearly observed in Fig. 1.12.

The conditions under normal device operations are clear from the

above discussion. The conditions outside the normal device operations, that is, the accumulation and inversion conditions can be described more intuitively with the aid of Fig. 1.13a and 1.13b. We now first consider the condition depicted in Fig. 1.13a, that is, the accumulation.

Suppose a certain amount of signal charge is present in the p-diffusion layer and we would like to consider how the gate voltage influences the band structure. When a large negative voltage is applied to the gate, the resulting interface electric field becomes attractive to the signal charge. That is, $E_s < 0$ and the constraint given by Eq. (1-13b) and shown in Fig. 1.12 will not be satisfied. In this case, as depicted in Fig. 1.13a, an accumulation layer will be formed at the interface whose thickness is small compared to the insulator thickness X_0 . Consequently, under accumulation the capacitance measured will be essentially that of the insulator C_0 . The mobile charge and fixed charge distributions are illustrated in the lower figure.

Now suppose we raise the gate voltage suddenly to a very large positive value. Then, the constraint defined by Eq. (1-13a) suddenly becomes not satisfied and all of the signal charge will be washed away into the substrate suddenly. If the gate voltage is in a reasonable range, some of the signal charge can be "saved" in the p-diffusion region. As we increase the gate voltage, the signal charge will be repelled from the surface, then also from the p-diffusion region, partially by the positive surface state charge Q_{ss} and the positive image charge at the gate, resulting in the growth of a depletion layer which extends deeper into the p-diffusion layer. A

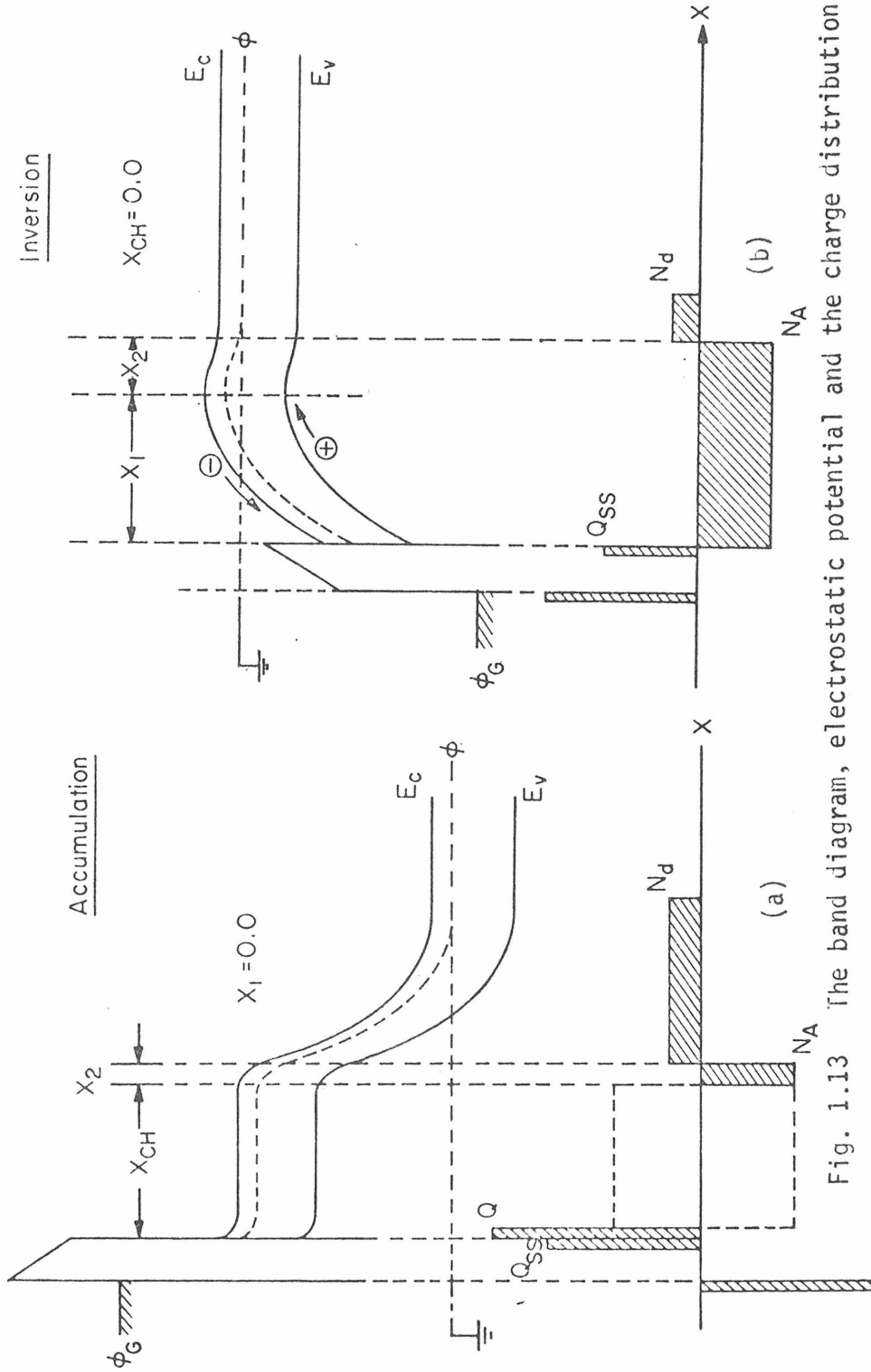


Fig. 1.13 The band diagram, electrostatic potential and the charge distribution

are illustrated for the case of signal charge Q accumulating at the oxide-semiconductor interface (a), and for the case of inversion (b) in which the thermally generated electrons are attracted to the inversion layer at the interface.

further increase of the voltage causes the p-layer near the interface to collect thermally generated minority carriers (electrons) forming an inversion layer. The situation is illustrated in Fig.1.13b. The time required for this process is called the storage time. For a good device, the storage time is of the order of one second. Since the storage time is much greater than the typical operation time of CCD, the effect of the formation of an inversion layer is not so serious and indeed in this way we can refresh the CCD, that is, we can delete all the signal charges.

1.6 Device Capacitance

The gate capacitance C_g is the most important parameter when one is concerned with the clock load and the actual speed of the device operation. In this section we first consider the gate capacitance and describe how it changes under the condition of inversion. Then the relevant relations among the gate capacitance and other capacitance, such as oxide capacitance and depletion capacitance, are presented in terms of the physical parameters discussed in the previous sections.

The gate capacitance C_g may be defined as the change of the image charge on the metal gate with respect to the gate voltage. The charge on the metal gate is by definition the image charge of the total charge at the interface and inside the semiconductor. We now describe how it changes under the condition of inversion depicted in Fig. 1.13b

When the device is static, the large positive gate voltage causes thermally generated minority carriers to shield effectively the depletion region from any increase in field so that the capacitance

becomes dominated by the inversion layer and approaches that of the insulator C_0 . However, during dynamic operations of the device the positive voltage results in the growth of a depletion layer which extends deeper into the p-diffusion layer, and the increasing distance between it and the charge on the metal causes the capacitance to fall further with increasing gate voltage.

We now approach the problem more quantitatively to obtain the relevant expressions among the gate, oxide and depletion capacitances and other physical parameters.

In normal device operations, using the relations given by Eqs. (1-8) it can be shown that the gate capacitance is proportional to the change of the surface electric field with respect to the gate voltage ϕ_G (or ϕ_{SF}). Specifically, we have

$$C_g = \epsilon_{Si} \frac{\partial E_s}{\partial \phi_{SF}} \quad , \quad (1-14a)$$

and this can be also rewritten as

$$\frac{1}{C_g} = \frac{1}{C_0} + \frac{1}{C_1} + \frac{1}{C_2} \quad , \quad (1-14b)$$

where $C_1 = \epsilon_{Si}/X_1$ is the surface depletion capacitance and $C_2 = \epsilon_{Si}/(1 + \frac{N_d}{N_A})X_2$ is the p-n junction capacitance.

In principle, it is possible to obtain the change $\Delta\phi_m$ of the minimum potential in terms of the changes, $\Delta\phi_{SF}$ and ΔQ , of the surface flatband voltage and the signal charge. After a diligent work of symbol manipulations, one would find

$$\Delta\phi_m = \frac{\left(\frac{1}{C_0} + \frac{1}{C_1}\right) \Delta Q + \Delta\phi_{SF}}{1 + C_2 \left[\frac{1}{C_0} + \frac{1}{C_1}\right]}, \quad (1-15a)$$

This expression can be easily obtained by considering the differential capacitor network shown in Fig. 1.5 c. The change of the minimum potential with respect to the surface flatband voltage ϕ_{SF} is fairly constant. As we observe from Fig. 1.9 its value is about 0.8. The influence of the gate voltage upon the minimum potential is attenuated by the presence of the capacitors, that is, from Eq. (1-15a) we have

$$\frac{\partial\phi_m}{\partial\phi_{SF}} = \frac{1}{1 + C_2 \left[\frac{1}{C_0} + \frac{1}{C_1}\right]} < 1 \quad (1-15b)$$

With the introduction of the p-n junction capacitance C_2 , we can express the gate capacitance C_g in a neat form as seen by

$$C_g = C_2 \frac{\partial\phi_m}{\partial\phi_{SF}} \quad (1-15c)$$

The change of the minimum potential upon the change in the signal charges can be expressed as

$$\frac{\partial\phi_m}{\partial Q} = \left[\frac{1}{C_0} + \frac{1}{C_1}\right] \frac{\partial\phi_m}{\partial\phi_{SF}} \quad (1-15d)$$

We have given all the important analytic formulas for the gate capacitance and other important physical parameters. And from these equations above, we can obtain quantitatively how the capacitances C_1 , C_2 and C_g depend on the salient physical parameters. The relevant calculations have been performed and the surface depletion capacitance C_1 , the p-n junction capacitance C_2 , and the gate capacitance C_g are plotted in Fig. 1.14a, 1.14b, and 1.14c respectively.

In practice during the operations of CCD, the amount of the signal charge Q would not be more than 50% of Q_d . Hence as seen in Eq. (1-15b) the change of the minimum potential upon the gate voltage is fairly constant, and its value is always around 0.8. This is because of the small p-n junction and capacitance C_2 compared to the oxide and surface depletion capacitance, C_0 and C_1 . Figure 1.14c is useful when one wishes to estimate the load upon the clock-drive. For small signal level, we note the gate capacitance C_g is always about $100 \text{ e/volt} \cdot \mu^2$. If one drives the clock with 1 MHz with the voltage swing of 20 volts, the current to be supplied to the gate is $2 \times 10^9 \text{ e/sec} \cdot \mu^2$. If the gate dimension is 10μ by 100μ , the current is $2 \times 10^{12} \text{ e/sec}$ or about $0.32 \mu\text{A}$ per gate. If one unit cell of the device consists of four gates, we must supply $1.28 \mu\text{A}$ per bit. For a thousand bit shift-register, the current would be 1.28 mA .

It should be noted at this stage that the gate capacitance C_g so defined above is actually a function of the gate voltage ϕ_{SF} and the signal charge Q . In a specific device operation, one more constraint

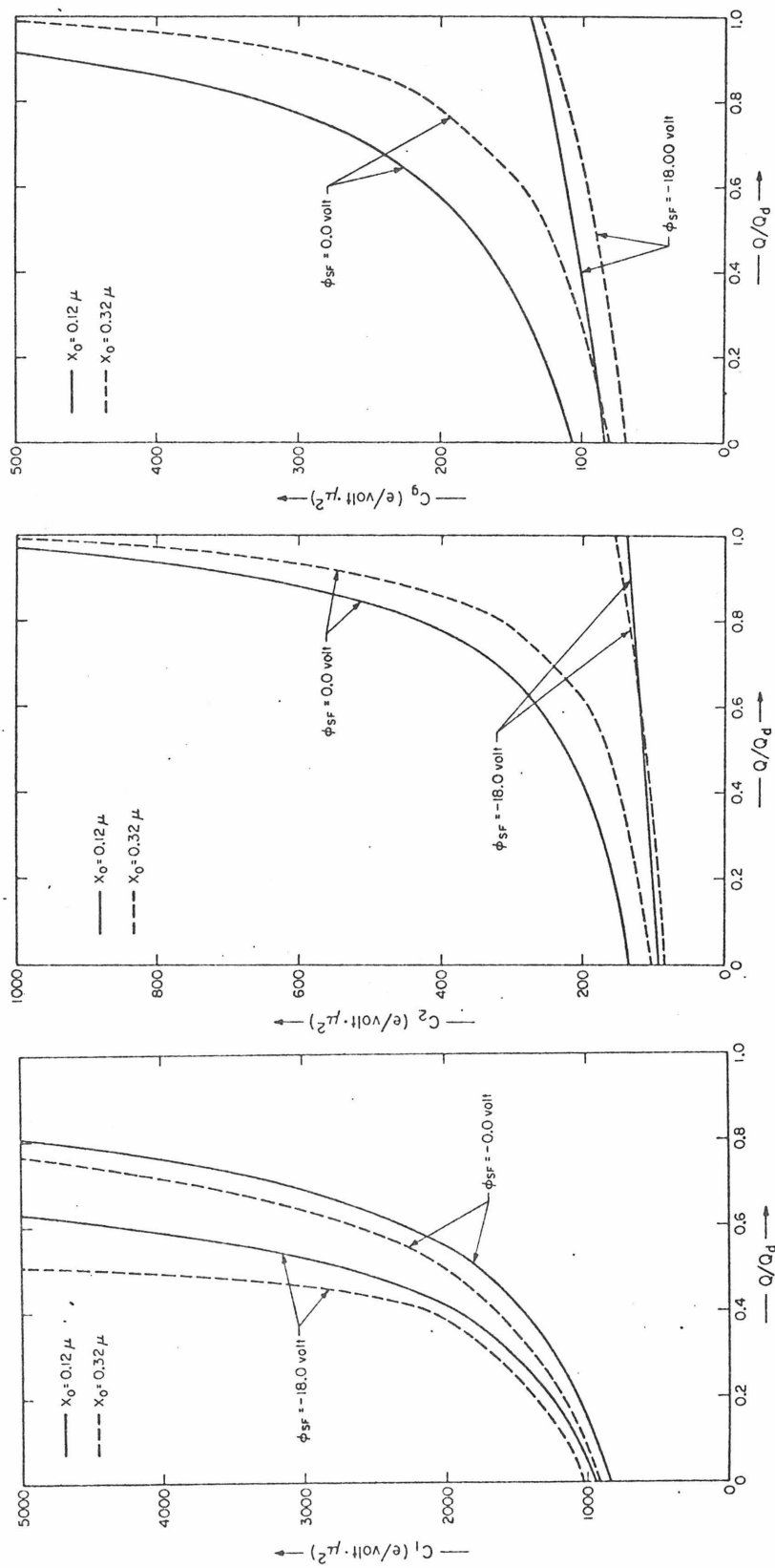


Fig. 1.14 The surface depletion capacitance C_1 (a), the p-n junction capacitance C_2 (b), and the gate capacitance C_g (c) are plotted against the signal level Q/Q_d for X_0 of 0.12μ and 0.32μ ; and for ϕ_{SF} of 0.0 volt and -18 volt. Note $100e/volt\text{-}\mu^2$ is equal to 1.6×10^{-5} pF/ μ .

among the gate voltage ϕ_{SF} , the signal charge Q and the minimum potential ϕ_m must be specified.

For example, in actual CCD operations, the signal charge Q is to move relatively slowly with respect to the gate voltage swing and the gate capacitance corresponds to the value with fixed signal charge while the gate voltage is changing. On the other hand, in the case of surface field-effect transistors with metallurgical p-diffusion channel, the signal (channel) charge Q can be supplied or extracted readily through the source and drain metallurgical contacts. The charge Q responds quickly to the gate voltage but the channel potential is fixed by the source and drain voltages while the gate voltage is changing rapidly.

An analytic expression for the gate capacitance C_g in terms of the gate potential ϕ_{SF} and the signal charge Q can be obtained by tedious symbolic manipulations from Eq. (1-8). But the result can be expressed quite compactly by using the two parameters A and B defined by Eqs. (1-11c) and (1-11d). The gate capacitance is found to be

$$C_g = C_g(\phi_{SF}, Q) = \frac{N_d C_d}{N_A \sqrt{A^2 - B}} \quad (1-15e)$$

The gate capacitance is a very useful measure in estimating the clock load and the operation frequency. But when the dynamic charge transfer process in CCD is under consideration, the information regarding the channel potential ϕ_m and the amount of the signal charge Q is essential

in the calculation of charge transfer efficiency. Specifically we must know how the channel potential ϕ_m depends on the signal charge Q . In Fig.1.15 we have plotted the gradient of the minimum potential against the signal charge. Observe the dependence is quite linear upon the signal charge. That is, the actual dependence of the minimum potential upon the signal charge is quadratic as we have claimed earlier referring to Fig1.10a. The slope of the curves we see in Fig. 3.15 will be steeper for lighter p-diffusion doping level N_A . This point can be understood clearly from the relation given by Eq. (1-15d) if one notes that the p-n junction capacitance C_2 is small compared to the oxide and surface depletion capacitance. In this case, we find, taking $\partial\phi_m/\partial\phi_{SF} \approx 1.0$,

$$\frac{\partial^2\phi_m}{\partial Q^2} \approx \frac{\partial}{\partial Q} \left[\frac{1}{C_0} + \frac{1}{C_1} \right] = \frac{\partial}{\partial Q} \left[\frac{1}{C_1} \right] \approx -\frac{1}{\epsilon_{Si} N_A} \quad (1-16a)$$

Or differentiating Eq. (1-10a) twice with respect to the signal charge Q , we obtain in a better approximation

$$\frac{\partial^2\phi_m}{\partial Q^2} \approx -\frac{1}{\epsilon_{Si} N_A} \left[1 + \frac{N_d}{N_A} \right] f(R) \quad (1-16b)$$

where the factor $f(R)$ is taken to be a constant with respect to the signal charge Q . The values of $f(R)$ for $Q = 0.0$ are seen from Fig. 1.10 and are around 0.7. For $\phi_{SF} = 0.0$, Fig.1.15 shows $\partial\phi_m/\partial Q = 0.0$. This fact can be explained using Eq. (1-11b). For $\phi_{SF} = 0.0$, $Q = Q_d$ at $E_s = 0.0$. $E_s = 0.0$ gives $X_1 = 0.0$. Also $Q = Q_d$

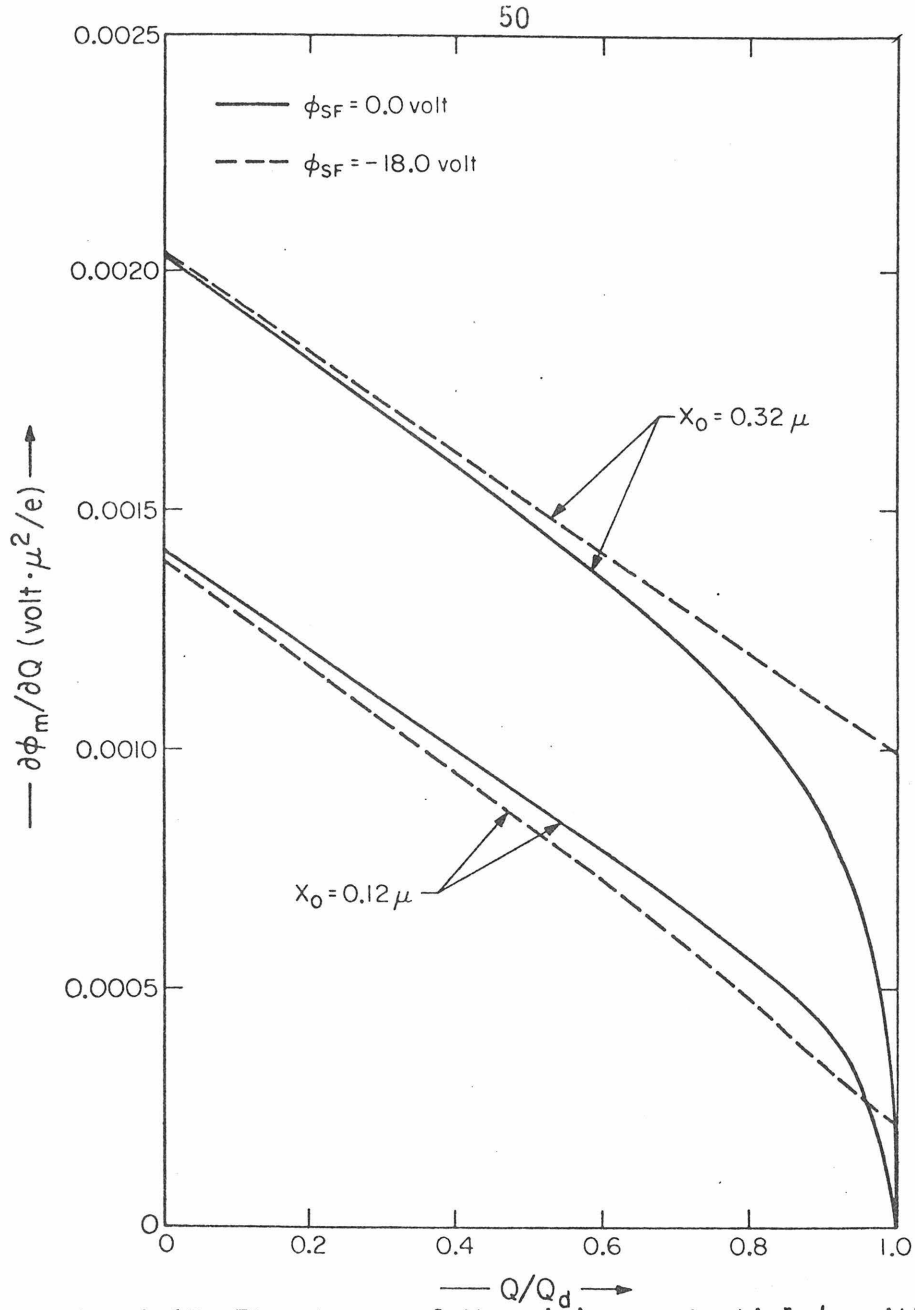


Fig. 1.15 The change of the minimum potential ϕ_m with respect to the change in the signal Q is plotted against the signal level. The fact that the slope is practically constant for small values of Q/Q_d allows us to approximate ϕ_m by a quadratic function of the signal charge Q as seen in Eq. (1-17)

gives $X_1 + X_2 = 0$. Hence X_2 is also zero. That is, C_1 and C_2 in Eqs. (1-15d) and (1-15b) must be infinite, resulting in $\partial\phi_m/\partial Q = 0.0$. Of course, this condition is outside of the normal device operations, and never realized in practice.

The fact that the slope is fairly constant for low signal level in Fig. 1.15 suggests a quadratic approximation of the minimum potential with respect to the signal charge Q . That is, we expand ϕ_m about $Q = 0.0$ as a second order polynomial of Q as seen by

$$\phi_m(\phi_{SF}, Q) \approx \phi_m(\phi_{SF}, 0) + \left. \frac{\partial\phi_m}{\partial Q} \right|_{Q=0.0} Q + \frac{1}{2} \left. \frac{\partial^2\phi_m}{\partial Q^2} \right|_{Q=0.0} Q^2 \quad (1-17)$$

The values of $\phi_m(\phi_{SF}, 0)$ have been plotted in Fig. 1.9. The values of the coefficients of the second and third terms have been calculated exactly. And the values of the potential calculated by Eq. (1-17) agree with the exact values by Eq. (1-10) within the errors of 0.1% for the range of interest. If we had plotted these values on Fig. 1.10a the corresponding points would fall on the lines, and there is no way to see the differences in the figure.

When one analyzes the dynamic charge transfer process in CCD, it is very important to express the minimum potential in the form given by Eq. (1-17). In the analysis, one is interested in the signal charge Q and the minimum potential ϕ_m . The simpler the relation between these two quantities ϕ_m and Q is expressed, the better for the charge transfer analysis in multi-gate structures.

1.7 Gaussian Doping Profile

For uniformly doped abrupt p-n junction, the depletion approximation gives excellent agreements with the exact solution which is solved numerically using Eq. (1-6). For many realistic devices the doping in the p-diffusion layer is typically introduced by ion-implantation followed by drive in diffusion. The resulting fixed charge distribution is a Gaussian doping profile characterized by the two parameters, the surface charge density N_s and the p-n junction depth X_g . To apply the results of the previous sections we first describe the procedure to obtain the effective p-diffusion density N_A and the effective diffusion depth X_d from N_s and X_g . This correlation allows us to estimate the general dependence of the minimum potential ϕ_m and the gate capacitance C_g on other salient physical parameters.

In this case, the fixed charge distribution $d(x)$ can be given quite accurately by a Gaussian profile as seen by

$$d(x) = N_d - (N_s + N_d) \exp \left[-\alpha^2 \left(\frac{x}{X_g} \right)^2 \right] \quad , \quad (1-18a)$$

and

$$\alpha^2 = \ln \left(1 + \frac{N_s}{N_d} \right) \quad , \quad (1-18b)$$

where N_s is the surface density of the p-diffusion layer and X_g is the position of the p-n junction of the semiconductor. The total sheet charge density Q_d in the p-diffusion layer is then given by

$$Q_d = - \int_0^{x_g} d(x) dx > 0 \quad . \quad (1-19a)$$

This quantity may be thought of as the product of the effective average doping density N_A and the effective depth x_d of the p-diffusion layer. That is, as before

$$Q_d = N_A x_d \quad . \quad (1-19b)$$

If we take the effective depth of the p-diffusion layer to be equal to the p-n junction depth, that is, $x_d = x_g$, then the relation (1-19b) determines the value of the effective doping N_A . However, the exact numerical calculation of the electrostatic potential gives a better agreement to the solution of the depletion approximation if we choose the effective depth to be at the reflection point of the Gaussian doping profile. By differentiating Eq. (1-18a) twice with respect to x and setting it to be zero, we obtain

$$x_d = \frac{x_g}{\alpha} \quad . \quad (1-20)$$

That is, for a Gaussian doping profile, the effective depth is actually shallower and the position of the minimum potential is closer to the oxide-semiconductor interface. Consequently, the signal charge will be transferred along the potential valley closer to the interface.

The effective p-diffusion density N_A can be obtained by Eq. (1-19b) if the actual value of Q_d is computed from Eq. (1-19a) for the doping profile $d(x)$ given by Eq. (1-18a). The result is given as seen by

$$Q_d = -N_d X_g \left[1 - \frac{\sqrt{\pi} \exp(\alpha^2)}{2\alpha} \operatorname{erf}(\alpha) \right] \quad (1-20b)$$

This quantity Q_d is by definition equal to $N_A X_d$ by Eq. (1-19b). Hence from Eq. (1-20a) $X_d/X_g = 1/\alpha$. Hence we have

$$N_A = \frac{Q_d}{X_d} = N_d \left[\frac{1}{\alpha} - \frac{\sqrt{\pi} \exp(\alpha^2)}{2\alpha^2} \operatorname{erf}(\alpha) \right] \quad (1-20c)$$

Therefore, we observe X_d/X_g , N_A/N_d and $Q_d/N_d X_g$ are all functions of α , hence, N_s/N_d only.

In Fig. 1.16a the effective average doping N_A and the sheet charge density Q_d are plotted against the surface doping N_s . The units are normalized by the substrate doping N_d for N_A and N_s , and $N_d X_g$ for Q_d . In Fig. 1.16b the effective diffusion layer depth X_d is plotted also against N_s/N_d .

We have now established a procedure to correlate the results of the uniform doping case to that of the Gaussian doping case. And the general characteristics of the potential profile and charge distribution can be easily compared for both cases.

In Fig. 1.17 the approximate potential profile is compared with the exact numerical solution. Observe that in the p-diffusion layer, the charge distribution is such that the entire signal charge packet is a neutral zone. The signal charge packet arranges itself according to the doping concentration so that the electrostatic potential is at its minimum value in the entire neutral signal charge packet.

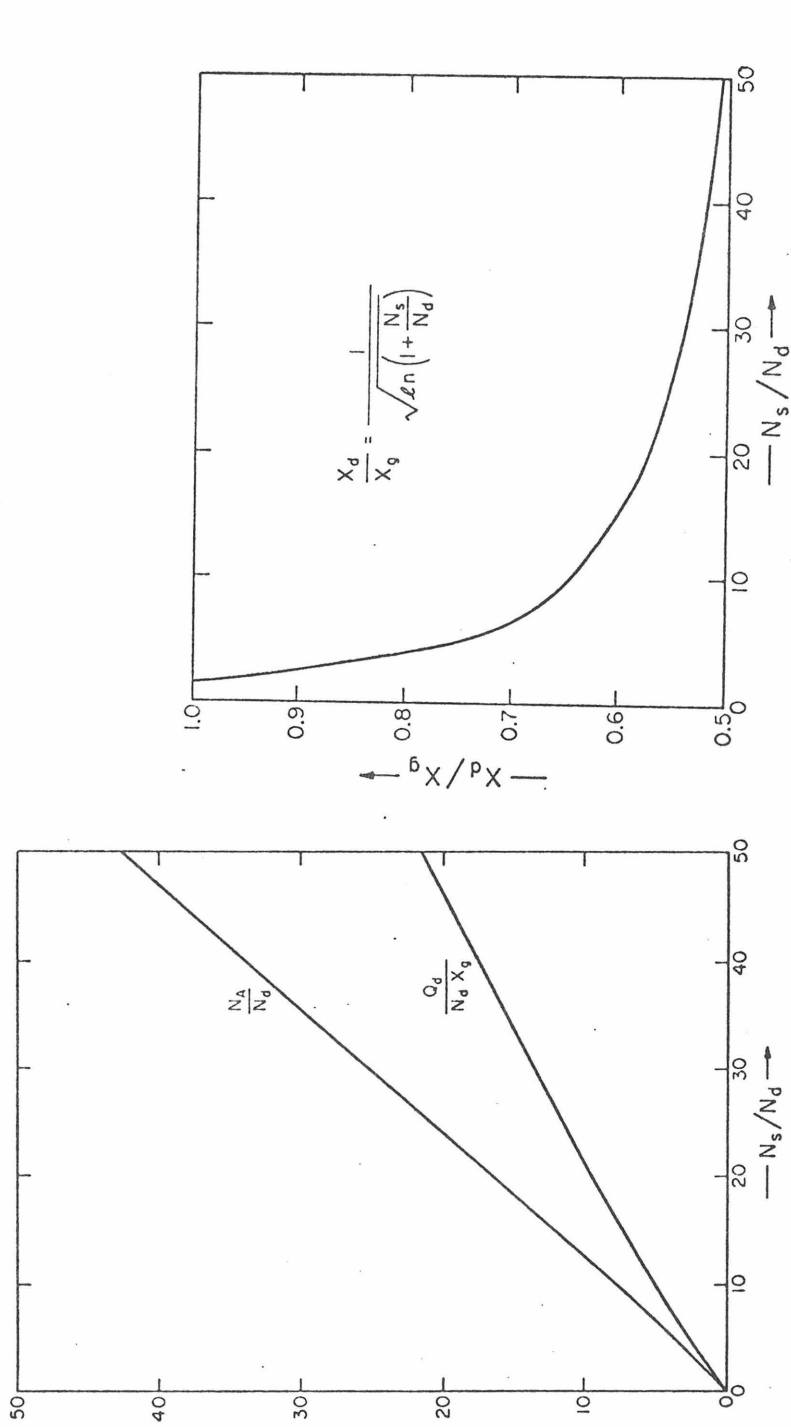


Fig. 1.16 (a) The effective p-diffusion layer doping density N_A/N_D and the sheet charge density $Q_D/N_D X_G$ are plotted against the surface density N_s/N_D .
 (b) The effective diffusion layer depth X_D/X_G is plotted against the surface density N_s/N_D . Here, all quantities are normalized.

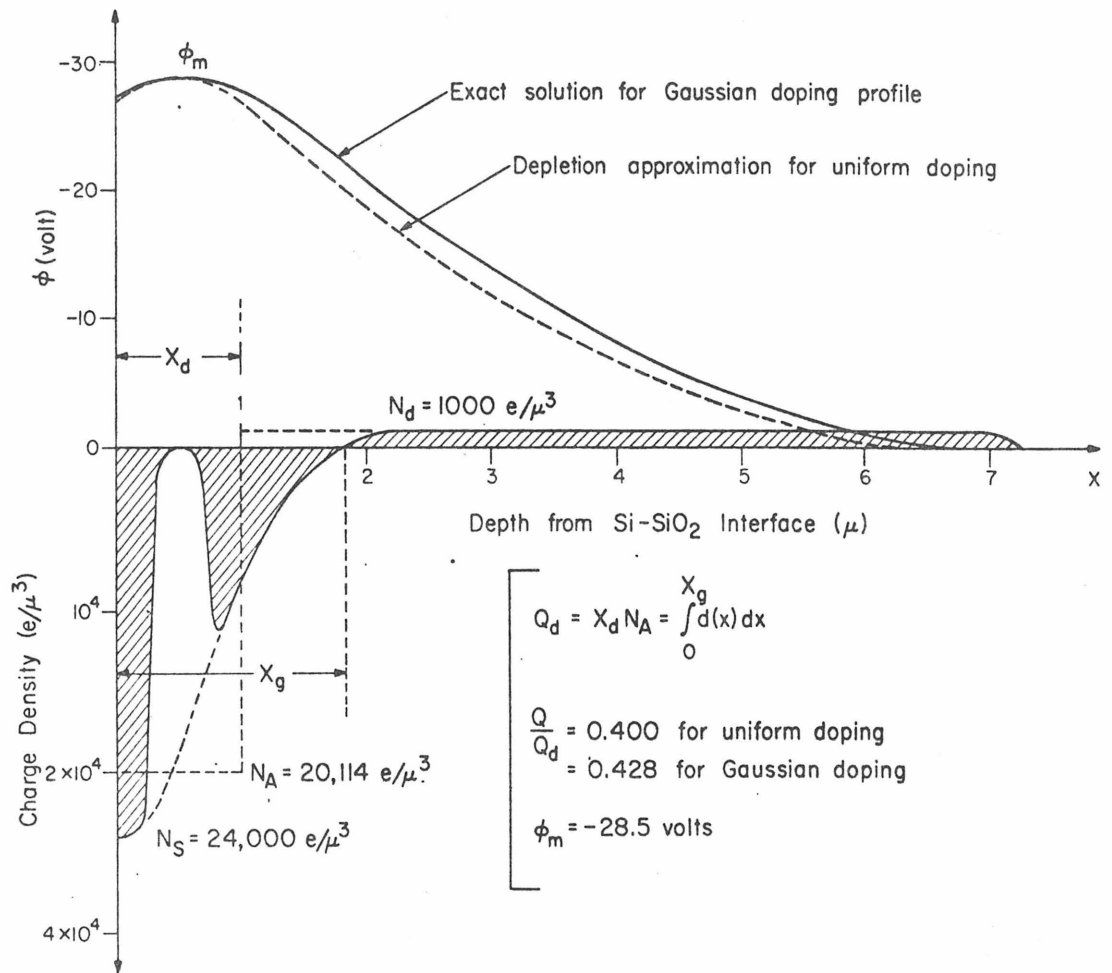


Fig. 1.17 The potential profiles ϕ by the depletion approximation and the exact numerical solution of the Gaussian doping profile are compared. $X_d = 1.0 \mu$ and the p-layer doping N_A of $20,000 \text{ e}/\mu^3$.

The oxide thickness X_0 is taken 0.32 and the gate voltage ϕ_{SF} equal to -18.0 volt. Since the gate voltage is fixed, the minimum potential ϕ_m and the signal charge Q are not independent of each other. Demanding the minimum voltage ϕ_m to be -28.5 volts, the corresponding signal charge Q/Q_d is 0.400 for uniform doping and 0.428 for Gaussian doping. In principle, it is possible to fix the signal charge Q/Q_d to be 0.400 and obtain the corresponding minimum potential ϕ_m for the uniform doping (which is -28.5 volt as before) and for the Gaussian theory case (which will be slightly lower than -28.5 volt) respectively. But the actual numerical computation for the Gaussian Profile case turns out easier if the minimum potential ϕ_m is fixed at the start rather than Q . This fact can be understood easily if one recalls the form of the Poisson's equation (1-6b) in the p-channel region, which includes the minimum potential ϕ_m in the expression. Then after computing the potential $\phi(x)$ as a function of the spatial coordinate X , we obtain the amount of the signal charge from the relation given by

$$Q = - \int_0^{X_g} d(x) \exp\left(\frac{\phi_m - \phi}{kT}\right) dx = Q_d - \epsilon_{Si} \left. \frac{\partial \phi}{\partial x} \right|_{x=0} + \epsilon_{Si} \left. \frac{\partial \phi}{\partial x} \right|_{x=X_g}, \quad (1-20d)$$

which gives the total signal charge from the minimum potential ϕ_m and the electrostatic potential profile ϕ .

We are now in the position to describe the general dependence of the minimum potential ϕ_m and the gate capacitance C_g for the case of the Gaussian doping profile and compare with the approximation made by the depletion approximation.

For our case study, the surface doping density N_s is taken to be $24,000 \text{ e}/\mu^3$ and the effective p-diffusion layer depth χ_d to be 1μ . Then, from Fig. 1.12a or Eq. 1-20c, the effective p-layer density N_A is found to be $20,114 \text{ e}/\mu^3$. The corresponding actual p-n junction depth χ_g for the Gaussian doping profile is found from Fig. 1.16b or Eq. (1-20a) to be 1.82μ . The substrate doping is fixed and taken to be $1000 \text{ e}/\mu^3$. The dependence of the minimum potential ϕ_m upon the gate voltage (ϕ_{SF}) for zero signal charge $Q = 0.0$ is illustrated in Fig. 1.18 for comparison with the results of the depletion approximation.

Figure 1.19 shows the dependence of the minimum potential ϕ_m upon the signal charge. The illustration format is similar to Fig. 1.10a. The slope of the minimum potential shown in Fig. 1.19 is plotted in Fig. 1.20. The gate capacitance C_g for the Gaussian doping case is also plotted in Fig. 1.21. The solutions of the exact numerical calculation for the Gaussian profile follows the general characteristics of the solutions obtained by the depletion approximation with surprising accuracy.

There may be several ways to compute the minimum potential and other salient physical parameters in the exact numerical calculations. We outline below one possible procedure to obtain the gate capacitance C_g and other relevant physical parameters.

By numerical calculations, we can obtain the electrostatic potential everywhere inside the semiconductor. The equation to be solved numerically is given by Eq. (1-6) and identified to be the form of a nonlinear differential equation seen by

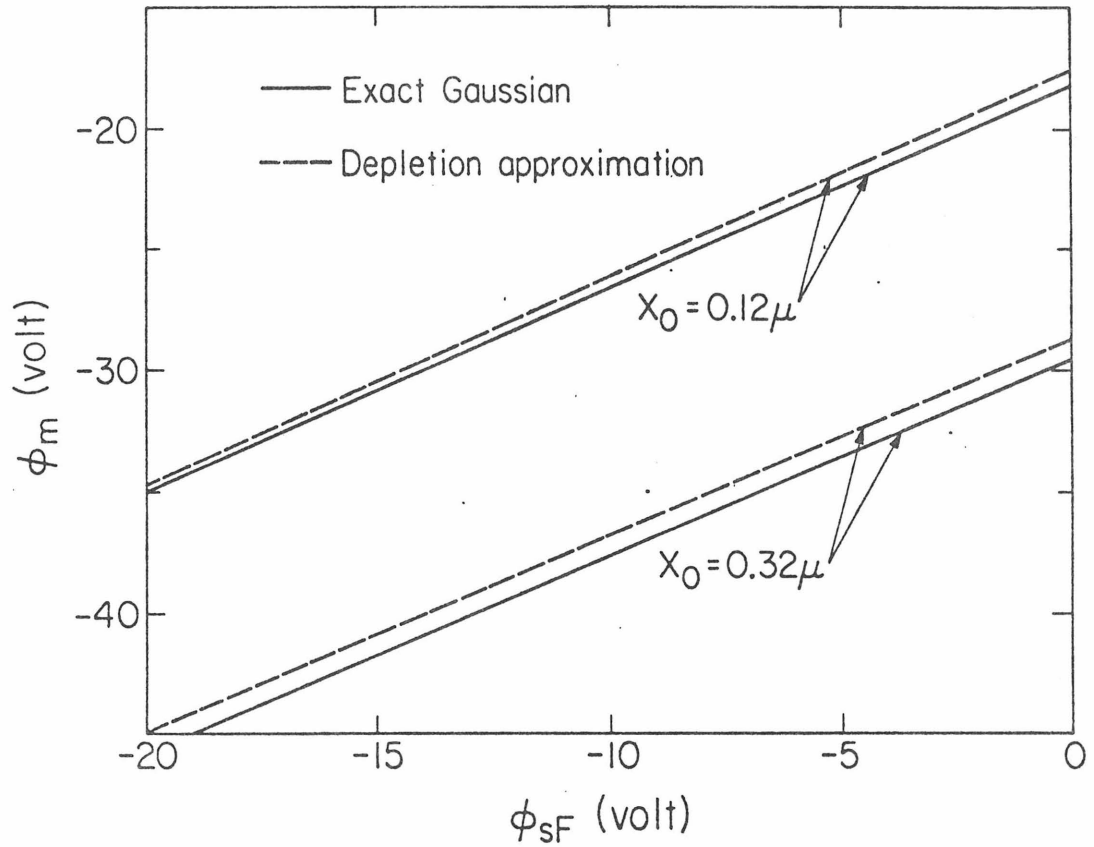


Fig. 1.18 The dependence of the minimum potential upon the flat band surface potential ϕ_{SF} defined by Eq. (1-7c) is illustrated for different oxide thickness X_0 for the Gaussian doping profile .

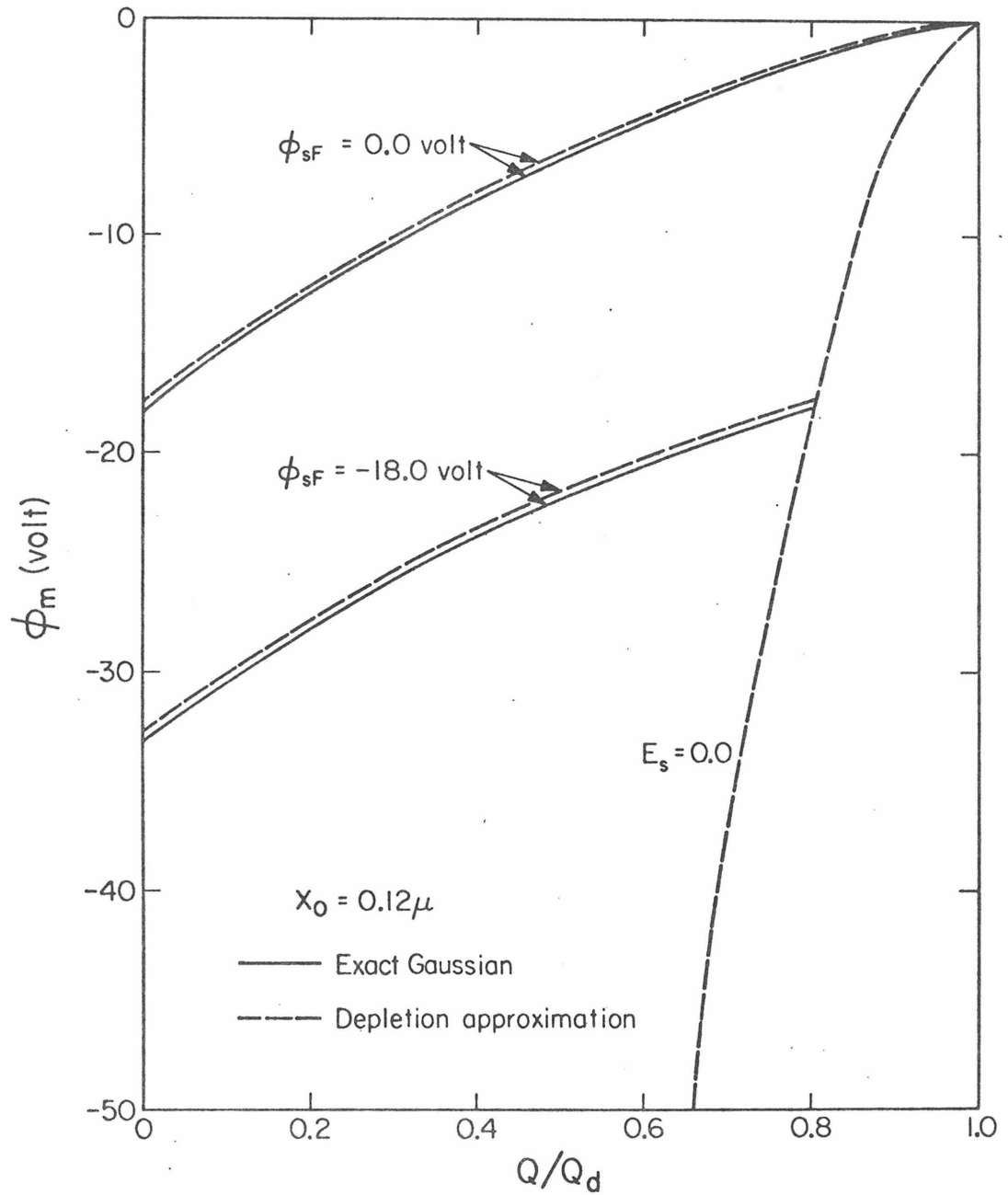


Fig. 1.19 The dependence of the minimum potential upon the signal charge is illustrated for the case of the Gaussian doping profile. Observe the similar characteristics between Fig. 1.10a and this figure.

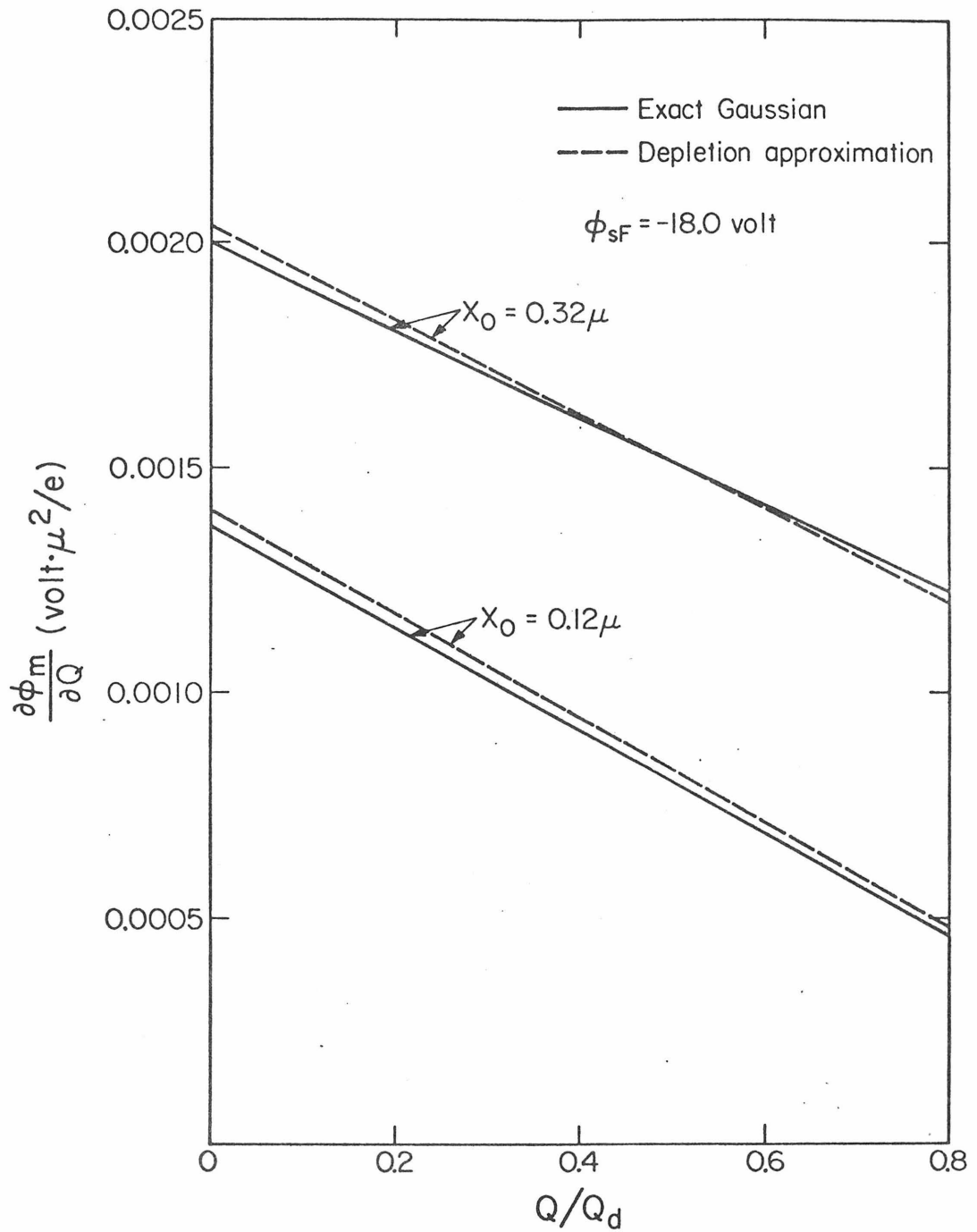


Fig. 1.20 The change of the minimum potential with respect to the change in the signal charge is illustrated for a Gaussian doping profile. Observe for the range of interest, the slope is fairly constant.

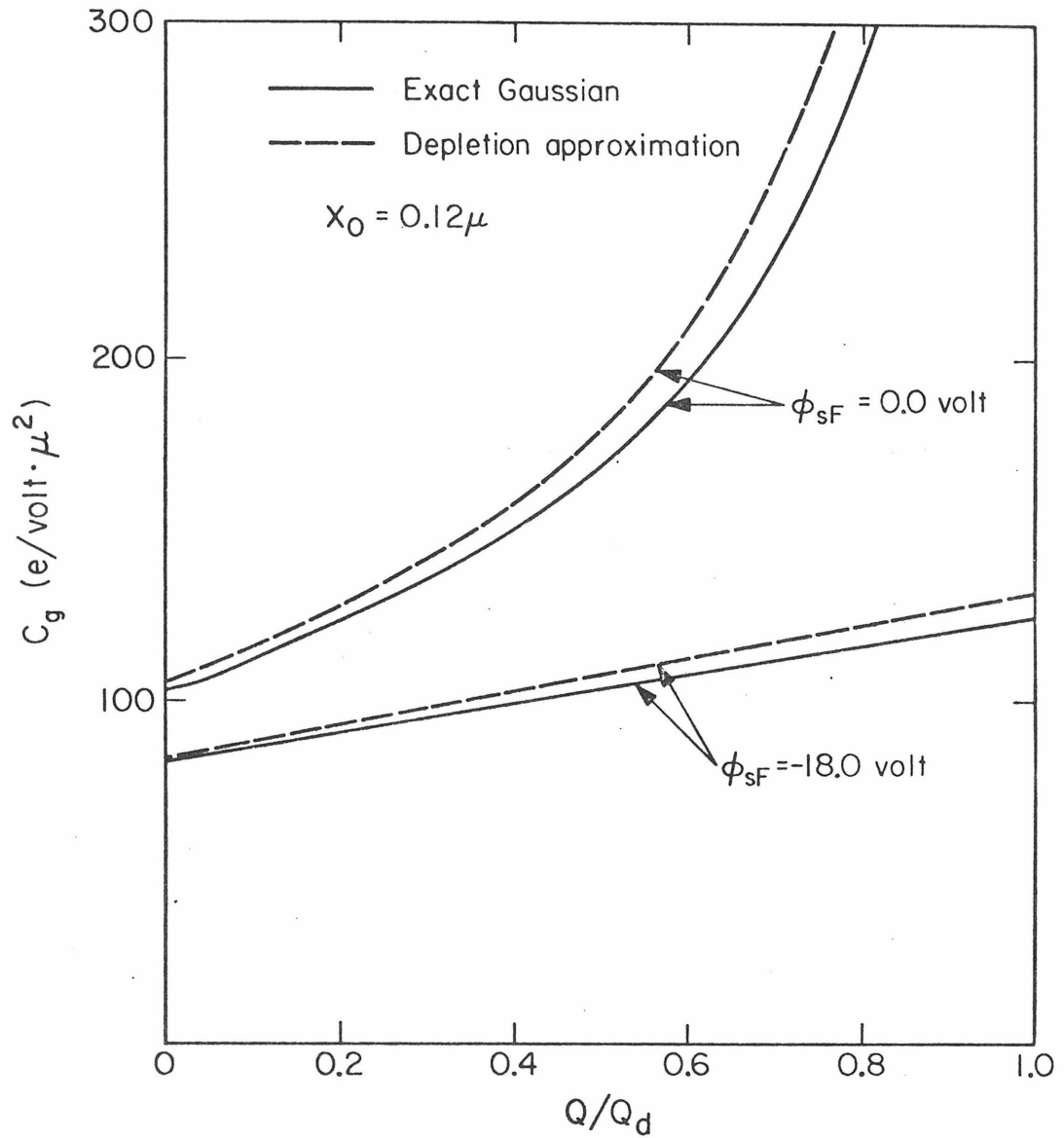


Fig. 1.21 The format is similar to Fig. 1.14c. The gate capacitance C_g for the Gaussian doping case is plotted against the signal charge Q . Observe the similar characteristics between Fig. 14c and this figure. The values are computed by Eq. (-14a) numerically.

$$\frac{\partial^2 \phi}{\partial x^2} = f(\phi, x) \quad \text{for} \quad 0 < x < \infty \quad . \quad (1-20a)$$

The boundary condition at the Si-SiO₂ interface is given by Eq. (1-8b) and can be written as

$$\phi = \phi_{SF} + \frac{\epsilon_{Si}}{C_0} \frac{\partial \phi}{\partial x} \quad \text{at} \quad x = 0 \quad . \quad (1-20b)$$

At $x = \infty$, that is, deep in the substrate, the potential is grounded, hence we have the remaining boundary condition:

$$\phi = 0.0 \quad \text{at} \quad x = + \infty \quad . \quad (1-20c)$$

Solving Eq. (1-20) we obtain the potential $\phi(x)$ as a function of the spatial coordinate everywhere for $0 \leq x \leq \infty$. In order to calculate the derivatives of the salient physical parameters, we introduce a parameter ψ defined by

$$\psi = \frac{\partial \phi}{\partial \phi_{SF}} \quad . \quad (1-21a)$$

Then, corresponding to Eq. (1-20) by differentiating them with respect to ϕ_{SF} we obtain an ordinary linear differential equation with respect to ψ given as

$$\frac{\partial^2 \psi}{\partial x^2} = g(x)\psi(x) \quad \text{for} \quad 0 < x < \infty \quad , \quad (1-21b)$$

where the boundary conditions for this corresponding case are given by

$$\psi = 1 + \frac{\epsilon_{Si}}{C_0} \frac{\partial \psi}{\partial x} \quad \text{at} \quad x = 0.0 \quad , \quad (1-21c)$$

and

$$\psi = 0.0 \quad \text{at} \quad x = \infty \quad , \quad (1-21d)$$

where

$$g(x) = \frac{\partial f(\phi, x)}{\partial \phi(x)} = g(\phi(x), x) \quad (1-21e)$$

Solving Eq. (3-21) we obtain $\psi(x)$ everywhere for $0 < x < \infty$. Hence from Eq. (3-14a) we obtain the gate capacitance C_g by the relation

$$C_g = - \epsilon_{Si} \left. \frac{\partial \psi}{\partial x} \right|_{x=0} \quad (1-22a)$$

From the solution $\phi(x)$ of the Eq. (1-21), we obtain the minimum potential ϕ_m and its location X_m . Then we can identify $\partial \phi_m / \partial \phi_{SF}$ to be the value of ψ at $X = X_m$. That is,

$$\frac{\partial \phi_m}{\partial \phi_{SF}} = \psi(X_m) \quad (1-22b)$$

Then from Eq. (1-15c) we can compute the p-n junction capacitance C_2 . Then from the relation (1-14b) we have the surface depletion capacitance C_1 . The change of the minimum potential with respect to the signal charge can be computed from Eq. (1-15d).

1.8 Conclusion

Since buried channel CCD operates in the reverse biased p-n junction depletion region, which is under thermal nonequilibrium, care must be taken in specifying the form of the Poisson's equation applicable for the structure. Unlike the surface CCD, the signal is to be transferred as a neutral packet away from the semiconductor-oxide interface and the concept of quasi-fermi levels has to be specified in

order to obtain the electrostatic potential and the signal level. By linear depletion approximation the relations among the minimum potential and other physical parameters are studied in detail. The procedure for the Gaussian profile to obtain the effective p-diffusion density N_A and effective depth X_d from the surface density N_s and the p-n junction depth X_g is presented. The agreement between the exact numerical calculation and the analytic approximation presented in this paper has been shown to be excellent. The actual numerical computation is outlined and we believe the detailed results presented in this presentation will serve as a useful reference and guide-work for those people who are designing the device and studying the transfer mechanism in details. This work is a stepping stone to the two dimensional analysis of buried channel CCD structures which begins with the analysis given herein as basis.

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IMPORTANT FORMULAS

1. Minimum Potential ϕ_m

$$\phi_m = - \left(1 + \frac{N_d}{N_A}\right) (\phi_d - \phi_{sF}) f(R)$$

$$\phi_t = \frac{N_A \epsilon_{Si}}{2C_o^2}$$

$$\frac{\phi_d}{\phi_t} = \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d}\right) \left[2 + \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d}\right)\right]$$

$$R = \frac{N_A}{2N_d} \frac{\phi_d - \phi_{sF}}{\phi_d + \phi_t}$$

$$f(R) = \frac{R}{1 + R + \sqrt{1 + 2R}}$$

2. Surface Flat Band Condition

$$\frac{\phi_{sF}}{\phi_q} = - \left(1 + \frac{Q}{Q_d}\right)^2$$

$$\phi_q = \frac{N_A X_d^2}{2\epsilon_{Si}} \left[1 + \frac{N_A}{N_d}\right]$$

3. Surface Electric Field E_s

$$E_s = \frac{AQ_d}{\epsilon_{Si}} \left[1 - \sqrt{1 - B/A^2}\right]$$

$$A = \left(1 + \frac{N_d}{N_A}\right) \left(1 - \frac{Q}{Q_d}\right) + \frac{N_d}{N_A} \frac{C_d}{C_o}$$

$$B = \left(1 + \frac{N_d}{N_A}\right) \left[\left(1 - \frac{Q}{Q_d}\right)^2 + \frac{\phi_{sF}}{\phi_q}\right]$$

4. Constraints on Gate Voltage ϕ_{sF}

$$\phi_{sF} \leq \left[\frac{Q_{MAX} - Q}{C_o}\right] \left[1 + \frac{C_o}{2C_d} \frac{Q_{MAX} - Q}{Q_d}\right] - \phi_B$$

$$\phi_{sF} > - \left(1 - \frac{Q}{Q_d}\right)^2 \phi_q$$

5. Device Capacitance

$$\frac{1}{C_g} = \frac{1}{C_o} + \frac{1}{C_1} + \frac{1}{C_2}$$

$$\Delta\phi_m = \frac{\left(\frac{1}{C_o} + \frac{1}{C_1}\right) \Delta Q + \Delta\phi_{sF}}{1 + C_2 \left[\frac{1}{C_o} + \frac{1}{C_1}\right]}$$

$$C_g = \frac{N_d C_d}{N_A \sqrt{A^2 - B}}$$

6. Gaussian Doping Profile

$$X_d = \frac{X_g}{\alpha}$$

$$N_A = N_d \left[\frac{1}{\alpha} - \frac{\sqrt{\pi} \exp(-\alpha^2)}{2\alpha^2} \operatorname{erf}(\alpha) \right]$$

$$\alpha^2 = \ln \left(1 + \frac{N_s}{N_d}\right)$$

Chapter 2

APPENDIX II : Final Stage of the Charge Transfer
Process in Charge Coupled Devices

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Final Stage of the Charge-Transfer Process in Charge-Coupled Devices

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Abstract—The final stages of transfer of charge from under a storage gate is formulated analytically including both fringing-field induced drift and diffusion. Analytic solutions to these equations are presented for constant fringing fields, and a system of equations for spatially varying fields is developed. Approximate solutions for spatially varying fringing fields, when combined with a lumped-parameter model of the self-induced field effects, are shown to give a reasonably accurate representation of the free-charge transfer process.

I. INTRODUCTION

EARLY descriptions [1], [2] of the charge transfer in charge-coupled devices (CCD) assumed that during the final stage of the charge transfer, the mechanism of transfer would be diffusion from under the storage gate. However, subsequent studies of the surface-potential profiles under the gates [3] indicated that fringing-field induced drift could act as an additional charge-transfer mechanism. In certain designs of CCD, this second mechanism can actually act as the dominant mechanism for transfer and enhance the rate of transfer during the final stage of charge transfer [4], [5].

These 2 mechanisms of transfer are characterized by 2 time constants, the thermal-diffusion time constant, τ_{th} , and the single-carrier transit time constant, τ_{tr} . In the case when the fringing fields are 0, the final stages of the diffusion processes are characterized by a profile which is a cosine function in shape and which decays exponentially with a time constant given by

$$\tau_{th} = \frac{4L^2}{\pi^2 D} \quad (1)$$

where L is the length of the storage electrode, and D is the diffusion constant.

On the other hand, if we neglect diffusion phenomenon, the charge remaining under the storage gate will be swept out in a single-carrier transit time

$$\tau_{tr} = \int_0^L \frac{dx}{\mu E(x)} \quad (2)$$

In this paper, we study these results analytically. We show that it is possible to obtain an analytic solution of

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the continuity equation in which the combined effects of diffusion and a uniform fringing field are included. A set of equations for spatially varying fringing fields are developed to show that the analytic solution for spatially varying fields can also be written in a form analogous to that for constant fringing fields.

The standard variational method is applied to obtain an approximate analytic expression for the characteristic time constants for spatially varying fringing fields. Self-induced drift terms are included by using an approximate lumped-circuit model.

II. TRANSPORT DYNAMICS

The transport dynamics along the insulator-semiconductor interface are described by the continuity equation

$$\frac{\partial q}{\partial t} + \frac{\partial J_x}{\partial x} = 0 \quad (3a)$$

and the diffusion equation

$$J_x = -D \frac{\partial q}{\partial x} + \mu q \left(-\frac{\partial \phi_s}{\partial x} \right) \quad (3b)$$

where q is the surface-charge density, ϕ_s is the surface potential, and x is the distance along the interface in the direction of charge transfer. J_x is the sheet-current density.

In this paper, we want to consider the solution to (3) for boundary conditions and approximations appropriate to the case where the storage gate contains a small amount of charge. This condition will arise in the final stage of the charge transfer, in the complete charge-transfer mode [5], or when the CCD is operated in a low-level injection application, such as low light-level imaging. In these cases, we can to the first approximation neglect the self-induced field terms.

When a CCD is operated in the complete charge-transfer mode, detailed numerical simulation of the transport dynamics under all the relevant gate electrodes and interelectrodes regions show that the charge transfer in the last stages of the transfer process can be approximately described by the discharge of the storage gate with an almost perfect sink at one end [5]. Therefore, we have considered the solution of (3) for the discharge of the storage gate using the boundary conditions

$$q(t, L) = 0, \quad \text{for } t > 0 \quad (4a)$$

$$J_x(t, 0) = 0, \quad \text{for } t > 0. \quad (4b)$$

Condition (4a) corresponds to assuming a perfect sink at

the right-hand end of the storage gate $x = L$; (4b) corresponds to assuming that no current flows out of the bucket under the storage gate through the edge at $x = 0$.

III. CONSTANT FRINGING FIELD

Assuming a constant fringing field E under the storage gate and neglecting the self-induced field term, the residual surface-charge profile under the storage gate is given by solving (3) to obtain

$$q(t,x) = \sum_{n=1}^{\infty} A_n \exp\left(\frac{Ex}{2kT}\right) \cdot \sin\left[\frac{\pi}{2} C_n \left(1 - \frac{x}{L}\right)\right] \exp\left(-\frac{t}{\tau_n}\right) \quad (5)$$

where kT is the thermal voltage and n is a summing index. The solution is given by a Fourier expansion multiplied by a common function, $\exp(Ex/2kT)$, with constants C_n , τ_n , and A_n to be determined as follows.

C_n is determined by the boundary condition at $x = 0$ and is given by solving the transcendental equation (see Fig. 1)

$$\tan\left(\frac{\pi}{2} C_n\right) + \left(\frac{kT}{LE}\right) \pi C_n = 0 \quad (6a)$$

where C_n is in the range given by

$$2n - 1 \leq C_n < 2n, \quad \text{for } n = 1, 2, \dots \quad (6b)$$

τ_n is given by substituting (5) into (3) to obtain

$$\frac{1}{\tau_n} = C_n^2 \frac{\pi^2 D}{4L^2} + \frac{(\mu E)^2}{4D} \quad (7)$$

Noting that the exponential term, $\exp(Ex/2kT)$ in (5) can be taken outside of the summation, we then obtain

$$A_n = \frac{2}{L[1 - (\sin \pi C_n)/\pi C_n]} \int_0^L q(0,x) \exp\left(\frac{-Ex}{2kT}\right) \cdot \sin\left[\frac{\pi}{2} C_n \left(1 - \frac{x}{L}\right)\right] dx \quad (8)$$

where use of the boundary condition (6a) has been made.

Detailed numerical simulations [4], [5] of charge transfer, including the effects of fringing fields, show that the profile of charge changes for a single-carrier transit time and then becomes stationary with an exponential time decay of the amplitude. This result is easily understood in light of the solution presented in the previous discussion. From (7) and (6b), one can see that τ_n is a decreasing function of n . Hence, for reasonably smooth initial charge distributions which produce finite values of A_n which either remain relatively constant or decrease with increasing n , we expect that eventually the first term in the series in (5) dominates the series, and $q(t,x)$ can be approximated by

$$q(t,x) \approx A_1 \exp\left(\frac{Ex}{2kT}\right) \sin\left[\frac{\pi}{2} C_1 \left(1 - \frac{x}{L}\right)\right] \exp\left(-\frac{t}{\tau_f}\right) \quad (9)$$

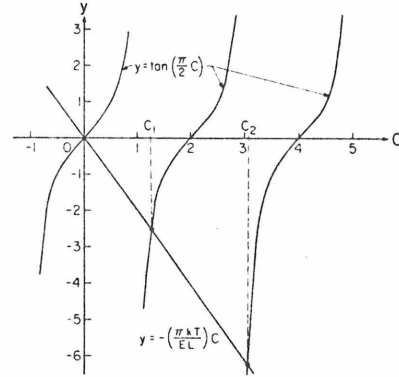


Fig. 1. The graph illustrates how to obtain C_1 and C_2 defined by (6a). Note $1 < C_1 < 2$ and $3 < C_2 < 4$ for any value of LE/kT . This is the condition given by (6b) for numbering the root C_n (the intersection) of the straight line with each branch of the tangent function.

where we have replaced τ_1 by τ_f to indicate that it is the time constant characterizing the final decay of the charge. Using (7), we find that

$$\frac{1}{\tau_f} = C_1^2 \frac{\pi^2 D}{4L^2} + \frac{(\mu E)^2}{4D} \quad (10)$$

Hence, we find for times which are greater than some as yet to be determined time (see Section IV), the charge profile remains constant, and the amplitude decays exponentially with time. The charge profiles at several different times are shown in Figs. 2 and 3 to illustrate the details of the charge transfer.

Determination of the value of τ_f depends upon the value of C_1 . The results of a numerical solution of (6a) for C_1 , as a function of the dimensionless parameter LE/kT , are plotted in Fig. 4. From this plot, we see that C_1 ranges from 1 for $LE/kT = 0$ to a value of 2 as LE/kT approaches infinity. (Note the first term in (6a) is negative.)

To compare this final decay constant with the 2 characteristic times defined in Section I, we have computed the value of the ratio of τ_f to τ_{th} to be

$$\frac{\tau_f}{\tau_{th}} = \frac{1}{C_1^2 + (LE/\pi kT)^2} \quad (11a)$$

and the value of the ratio of τ_f to τ_{tr} to be

$$\frac{\tau_f}{\tau_{tr}} = \frac{ALE/\pi^2 kT}{C_1^2 + (LE/\pi kT)^2} \quad (11b)$$

These ratios as a function of LE/kT are plotted in Fig. 5.

IV. STATIONARY PROFILE WITH CONSTANT FRINGING FIELD

According to the detailed numerical simulation [4], [5] of charge transfer under the influence of fringing fields, the charge profile under the storage gate drifts for a

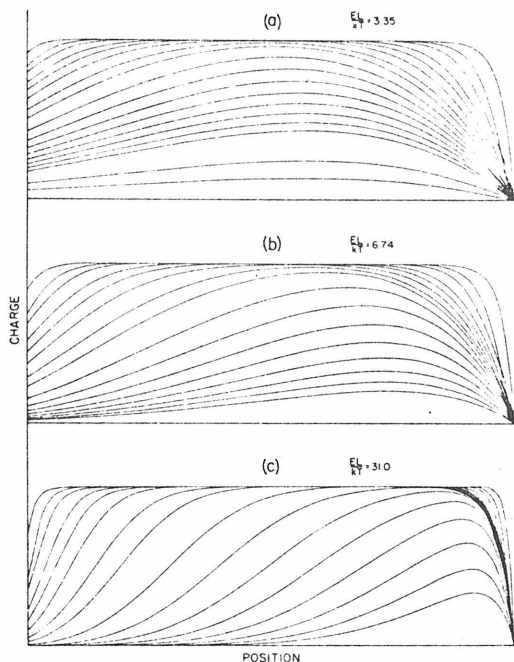


Fig. 2. The details of the charge decay at different instances are illustrated for three different values EL/kT of constant fringing-field strength. The initial charge profile is taken to be uniform. The total initial charge is 70 percent of the full bucket charge ($14.6 \text{ C}/\mu^2$). Note in all three cases, the relative charge profile becomes stationary within a single-carrier transit time. The position of the peak of the final charge profile is given exactly by (14). (a) $EL/kT = 3.35$. The total number of profiles shown is 18. The corresponding times are 0.01, 0.02, 0.03, 0.05, 0.07, 0.10, 0.15, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.5, and 2.0 of a single-carrier transit time. (b) $EL/kT = 6.74$. The total number of profiles shown is 16. The corresponding times are similar to Fig. 2(a). The profiles at $t = 1.5$ and 2.0 are deleted. (c) $EL/kT = 31.0$. The total number of profiles shown is 16. The corresponding times are the same as Fig. 2(b).

single-carrier transit time and then becomes stationary. No matter how strong the fringing fields are for reasonable initial charge distributions, such as uniform or a cosine shape, in the final stage of charge transfer, the stationary profile results eventually because of the thermal-diffusion mechanism. This is to say that the first term in the infinite series in (5) becomes the dominant one within an elapsed time, t , of the order of a single-carrier transit time.

We now return to the question of what is the value of the lower time limit for the validity of approximation of keeping only the first term in the series in (5). To gauge this time, we consider the ratio r_{12} of the first two terms in the series in (5). Assuming that A_1 is the same as A_2 and neglecting spatial variation, this ratio is given by

$$r_{12} = \exp \left[\frac{t}{\tau_{th}} (C_2^2 - C_1^2) \right]$$

where use of (7) has been made. In terms of the single-

carrier transit time, this ratio can be written as

$$r_{12} = \exp \left[\frac{t}{\tau_{tr}} \frac{\pi^2 kT}{4LE} (C_2^2 - C_1^2) \right].$$

Taking as our criterion the fact that the value of the exponent in this expression is greater than one, we find that (9) is valid for

$$t > \tau_{tr} \left[\frac{4LE/\pi^2 kT}{C_2^2 - C_1^2} \right]. \quad (12)$$

The right-hand side of this inequality is a multiple of the τ_{th} , with the constant multiplying the transit time depending on the value of the parameter EL/kT . The value of this multiplier can be approximated as follows.

The value of $C_2^2 - C_1^2$ varies monotonically between 8 when EL/kT is 0 to 12 when EL/kT approaches infinity. Thus we can replace the inequality by

$$t > \tau_{tr} \left(\frac{EL}{kT} \right) / 2\pi^2. \quad (13)$$

This inequality shows that for EL/kT between 0 and about 30 (the values normally encountered in devices), the approximation is valid for times greater than a single-carrier transit time. Hence, the results of the numerical simulations are in good agreement with the analytical results obtained here, and we can describe the final charge profile by (9).

The peak position of the charge packet, x_{peak} , after it becomes stationary under the storage gate, is given by differentiating (9) with respect to x and setting the resulting equation to be 0. Then using the condition (6a), we obtain

$$x_{peak} = 2L \left(1 - \frac{1}{C_1} \right). \quad (14)$$

This expression shows the peak-position varies with the strength of the fringing field. For 0 field, C_1 is unity. The surface-charge profile is a cosine function with a maximum at $x = 0$, and it decays exponentially with the time constant equal to the thermal-diffusion time constant.

For large fringing fields, the value of C_1 approaches 2 as shown in Fig. 4, but never becomes larger than 2. For extremely large fringing fields, $C_1 \approx 2$ and $x_{peak} \approx L$, implying that the peak position approaches the sink edge at $x = L$. At times, the exponential decay is observed satisfying the inequality in (12), and the characteristic decay time is a factor approximately $\frac{1}{2}$ of the single-carrier transit time, as we observe in Fig. 5. Figs. 2 and 3 illustrate the details of the charge decay as we have discussed so far.

V. SPATIALLY VARYING FRINGING FIELDS

We now note that the constant and spatially varying fringing fields both give similar charge-decay characteristics. This is to say that the analytic solutions of both spatially varying and constant fringing fields can be written in similar forms. Both solutions can be expressed by infinite series, and as time elapses, the term with the

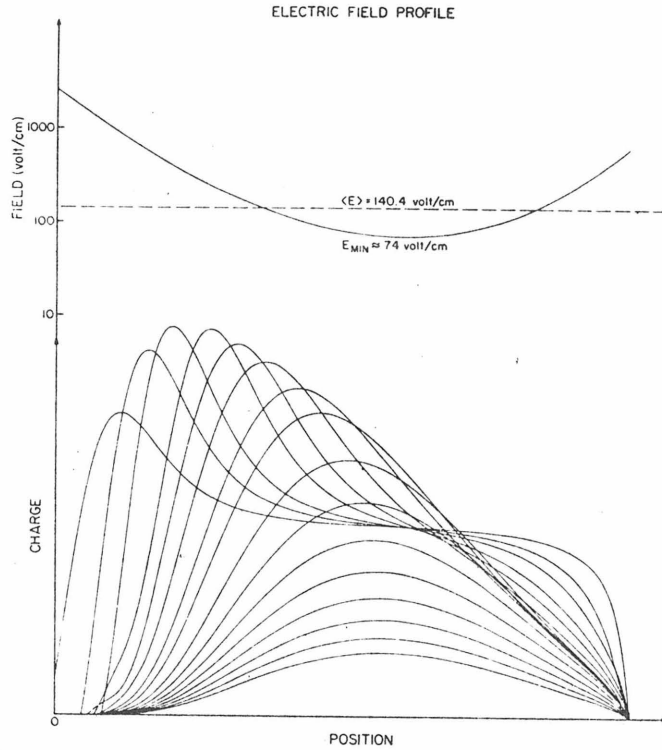


Fig. 3. The details of the charge decay at different stages. The condition is similar to the results of Fig. 2 except the fringing field is spatially varying in this case. An average fringing field computed by (2) is 140 V/cm. The minimum field is 74 V/cm. The total number of profiles shown is 16. The corresponding times are the same as Fig. 2(b) and (c).

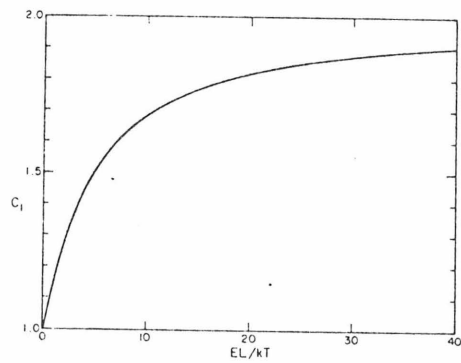


Fig. 4. Values of C_1 defined by (6), plotted against the normalized fringing-field strength EL/kT .

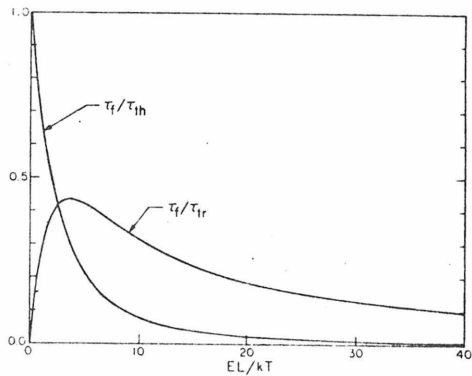


Fig. 5. The final decay time constant, τ_f , normalized by the single-carrier transit time τ_s , and by the thermal-diffusion time constant τ_{th} , plotted against the normalized fringing-field strength EL/kT .

largest time constant τ_1 becomes dominant, resulting in the exponential decay characteristics and the constant charge profile. In this case, it is convenient to work with

$Q(t, x)$, as seen by

$$Q(t, x) = \int_0^x q(t, x') dx'. \quad (15)$$

Using the definition for Q and the fact that current flows only out of one end of the gate (see (4b)), we can write (3) as

$$\frac{\partial Q}{\partial t} = D \frac{\partial^2 Q}{\partial x^2} - \mu E(x) \frac{\partial Q}{\partial x} \quad (16)$$

$$\frac{1}{\tau_1} = \left[D \int_0^L [d\gamma_1/dx]^2 dx + (\mu/2) \int_0^L [E^2(x)/2kT - dE/dx] \gamma_1^2(x) dx \right] / \int_0^L \gamma_1^2(x) dx. \quad (23)$$

where the boundary condition equivalent to (4a) is given by

$$\left. \frac{\partial Q(t,x)}{\partial x} \right|_{x=L} = 0. \quad (17a)$$

The boundary condition (4b) is used to derive (16). We now have instead, a different boundary condition at $x = 0$, which follows directly by the definition of $Q(t,x)$ given by (15) and is seen as

$$Q(t,0) = 0, \quad \text{for all } t. \quad (17b)$$

To eliminate the first derivative from (16), we introduce the following transformation:

$$Q(t,x) = \exp\left(\frac{1}{2kT} \int_0^x E(x) dx\right) R(t,x). \quad (18)$$

Then, (16) becomes

$$\frac{\partial R}{\partial t} = D \frac{\partial^2 R}{\partial x^2} - \frac{\mu}{2} \left[\frac{E^2(x)}{2kT} - \frac{dE}{dx} \right] R \quad (19)$$

with the new boundary conditions given by

$$\frac{\partial R}{\partial x} + \frac{E(x)}{2kT} R = 0, \quad \text{at } X = L \quad (20a)$$

and

$$R(t,0) = 0, \quad \text{for all } t. \quad (20b)$$

The solution of (19) together with the boundary conditions is given by an infinite series of the form

$$R(t,x) = \sum_{n=1}^{\infty} B_n \gamma_n(x) \exp(-t/\tau_n) \quad (21)$$

where B_n is to be determined by the initial values of $R(0,x)$. $\gamma_n(x)$ and τ_n are the eigenfunctions and eigenvalues, respectively, of the eigenvalue problem given in (19) and (20).

The results in the case of constant fringing fields combined with the results of detailed numerical simulations suggest strongly that for times which are a few times the single-carrier transit time, we can approximate the series in (21) by the first term and write

$$Q(t,x) = B_1 \exp\left(\frac{1}{2kT} \int_0^x E(x) dx\right) \gamma_1(x) \exp(-t/\tau_f) \quad (22)$$

where again, we have replaced τ_1 by τ_f .

The largest time constant τ_f could, in general, be obtained by solving (19) and (20). However, a good estimate can be obtained from the standard variational procedure for lowest eigenvalues [8]. According to this procedure, the exact value of τ_f is obtained by minimizing

The solution of (19) with $E(x)$ constant suggests the trial function for the first eigenfunction

$$\gamma_1(x) = \sin\left[\frac{\pi C_1 x}{2L}\right]. \quad (24)$$

This trial function must satisfy the boundary conditions of (20). That is, the value of C_1 is to be determined by the strength of the fringing field $E(L)$ at the sink edge of the gate (see (20a)). Since the fringing fields at the ends of storage gates are very large [3], [5], we have

$$E(L) \gg kT/L. \quad (25)$$

Hence, substituting $\gamma_1(x)$ of (24) into R of (20a), we obtain

$$-\tan\left(\frac{\pi C_1}{2}\right) = \pi C_1 \frac{kT}{LE(L)} \ll 1 \quad (26a)$$

and hence,

$$C_1 \approx 2. \quad (26b)$$

With this value of C_1 , substituting the trial function given by (24) into (23), we obtain

$$\frac{1}{\tau_1} = \frac{4}{\tau_{th}} + \frac{\mu^2 E_{eq}^2}{4D}. \quad (27a)$$

E_{eq} is an equivalent constant fringing field for the spatially varying fringing field $E(x)$ and is given by

$$E_{eq}^2 = \frac{2}{L} \int_0^L \left[E^2(x) - 2kT \frac{dE}{dx} \right] \sin^2\left[\frac{\pi x}{L}\right] dx. \quad (27b)$$

Note that, due to the weighting function $\sin^2(\pi x/L)$, the integral vanishes at both ends of the gate; $x = 0$ and L . The contribution of the integrand at the ends of the storage gate is relatively small, but the fringing fields at the positions of high-charge concentration are weighted heavily in the integral. If the fringing field is slowly varying and is at its minimum value E_{min} under most of the storage gate (except at the ends), then we obtain $E(x) \approx E_{min}$ and $dE/dx \approx 0$. Hence, from (27b), we have $E_{eq} \approx E_{min}$. Finally, we obtain an approximate analytic formula of the time constant for spatially varying fringing fields, which is

$$\frac{1}{\tau_f} = \frac{1}{\tau_1} \approx \frac{4}{\tau_{th}} + \frac{\mu^2 E_{min}^2}{4D}. \quad (28)$$

Care must be taken in applying this formula. This formula

was obtained for slowly varying fringing fields under most of the storage gate, and other configurations may give different fringing-field profiles leading to different results.

For example, in CCD structures with short storage-gate length L , E_{sq} may be a few times larger than E_{min} . In this case, (27b) could be used to obtain E_{sq} if the fringing-field profile is known. For short storage-gate length L , the spatial dependence of the fringing fields can be approximated by [3]

$$E(x) = \frac{E_{min}L}{2X}, \quad \text{for } 0 \leq X \leq L/2 \quad (29a)$$

$$= \frac{E_{min}L}{2(L-X)}, \quad \text{for } L/2 \leq X \leq L. \quad (29b)$$

Substituting (29) into (27b), we obtain $E_{sq} = 1.95E_{min}$ for the same trial function $\psi_1(x)$ given by (24). In either case, as seen in (28), we note that the reduction of the final decay time constant by the fringing-field strength is quadratic rather than linear.

If we include the nonlinear self-induced field drift, exact analytic solutions of (3) become difficult. However, using a lumped-circuit model,¹ the charge-transfer characteristics can be obtained by solving the discharge equation [5], [6]

$$J_x = -\frac{dQ(t,L)}{dt} \quad (30a)$$

where J_x is the steady-state discharge current density assumed constant across the gate, and $Q(t,L)$ is the total charge under the gate.

The relation between the surface potential ϕ_s and surface-charge density q , under the transfer gate, is given according to the gradual channel approximation [4], [5]

$$\phi_s = \phi_{s0} + \frac{q}{C} \quad (30b)$$

where ϕ_{s0} is the surface potential with no charge, and C is the effective oxide- and depletion-layer capacitance per unit area. When the fringing fields are negligible compared to the self-induced field, we have

$$\frac{\partial \phi_s}{\partial x} \approx \frac{1}{C} \frac{\partial q}{\partial x}. \quad (30c)$$

Then, if the difference in the surface potential between the beginning and end of the gate is V , by integrating the diffusion equation (3b) over space, we obtain [5], [7]

$$J_x = \frac{\mu C}{2L} [V^2 + 2kTV] \quad (31a)$$

where, we note

$$q(0) = CV. \quad (31b)$$

Since J_x in (3b) is assumed constant for $0 \leq x \leq L$, we

¹ According to this model, the storage gate is considered, in this case, as a capacitor discharged through a transfer channel which is the same storage gate.

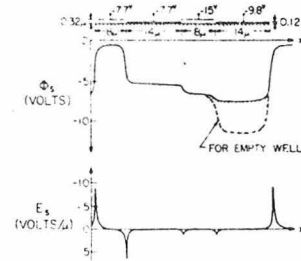


Fig. 6. The surface potential and electric field along the Si-SiO₂ interface obtained from the solution of the two-dimensional Poisson's equation. The electrode voltages correspond to the latter stages of the charge transfer,² with a signal charge in the receiving storage gate. The substrate doping is 10^{17} donors/cm³. The fixed surface-state charge is 3.6×10^{11} cm⁻², in this calculation.

obtain $q(x)$ for $0 \leq x \leq L$. Then, by integrating $q(x)$, we obtain

$$Q(t,L) = \frac{2}{3}LCV \frac{V + 3kT/2}{V + 2kT}. \quad (31c)$$

Then, the solution of (30a) is of the form

$$\frac{Q(t,L)}{Q(0,L)} = \frac{\exp(-t/\tau_f)}{1 + Q(0,L)/\frac{2}{3}LCV(1/2kT)(\tau_f/\tau_{ch})[1 - \exp(-t/\tau_f)]} \quad (32)$$

where $Q(0,L)$ is the initial total charge under the storage gate, and τ_f is given by (28).

VI. NUMERICAL RESULTS

The exact fringing-field profile can be obtained by solving the two-dimensional Poisson equation for the CCD structure with the applied gate voltages. In Fig. 6, we have plotted the surface potential and surface-potential gradient along the semiconductor-insulator interface. The voltages on the gate electrodes (see Fig. 6) are those corresponding to the last stage of the charge transfer. Most of the signal charge was taken to be in the receiving storage electrode.² Periodic boundary conditions were used. The minimum fringing field E_{min} , in this case, is equal to 74 V/cm.

To check the accuracy of the approximate solution for τ_f given by (28), we have solved (3) numerically for the fringing-field profile given in Fig. 6 [2]. The full-line curve in Fig. 7 represents the numerically calculated residual charge under the storage gate versus transfer time with the self-induced fields. The dashed-line curve in Fig. 7 is the residual charge calculated using (32). The value

² For two-phase push-clock scheme, the actual receiving gate voltage is -15.0 V instead of -9.8 V in Fig. 3, and the difference of 5.2 V corresponds to the amount of the signal charge present under the receiving gate.

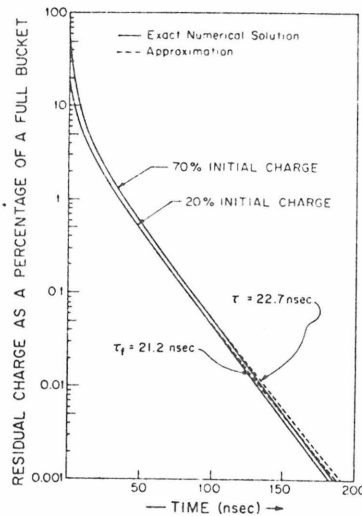


Fig. 7. Total residual charge under the left Si-source gate as a function of time. The effective oxide capacitance is $3.22 \text{ F}/\mu^2$, and the full bucket charge is $14.6 \text{ C}/\mu^2$. The solid curve represents exact numerical solution of (3), and the dashed curve is an approximation by (32). τ_f is for the slope of the two parallel solid lines and τ for the dashed lines. The final slope (hence, also the final time constant) does not depend on the total amount of the initial charge under the storage gate.

of the final decay time constant τ_f calculated from (28) is 22.7 ns compared to 21.2 ns obtained from the numerical solution.

VIII. CONCLUSION

Incomplete transfer of free charge in CCD with small amounts of charge to be transferred was characterized analytically, including the effects of diffusion and fringing fields. We have found that, independent of the fringing-field profile, the exponential decay characteristic is solely due to diffusion. However, the characteristic time constant τ_f for the decay depends on diffusion and fringing

fields and is found to be always a fraction of the single-carrier transit time τ_{tr} (see Fig. 5).

The standard variational procedure was applied to obtain an approximate analytic expression for the characteristic time constant (See (23)), and the expression was evaluated for spatially varying fringing fields (see (26)) which vary relatively slowly over most of the storage gate length but increase considerably at the edges of the gates. Such fringing-field profiles are typical for most minimum geometry CCD structures (minimum gate dimension of about 10μ) and substrate doping greater than $10^{14}/\text{cm}^3$. The constant and spatially varying fringing fields both were found to give exponential charge-decay characteristics. When the magnitude of the field becomes greater than a few times kT/L , the discharge is considerably enhanced by the fringing-field drift.

If the self-induced field terms are introduced, then, using a lumped-circuit model, the free-charge transfer process is given quite accurately by the formula given.

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Chapter 3

APPENDIX II : Influence of Interface States on
Incomplete Charge Transfer in Overlapping Gate CCDs

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The Influence of Interface States on Incomplete Charge Transfer in Overlapping Gate Charge-Coupled Devices

AMR M. MOHSEN, T. C. MCGILL, YOSHIAKI DAIMON, AND CARVER A. MEAD

Abstract—A simple and accurate model is used to estimate the incomplete charge transfer due to interface states trapping in the overlapping gate charge-coupled devices. It is concluded that trapping in the interface states under the edges of the gates parallel to the active channel limits the performance of the devices at moderate and low frequencies. The influence of the device parameters, dimensions, and clocking waveforms on the signal degradation is discussed. It is shown that increasing the clock voltages, increasing the signal charge, or using push clocks reduces the incomplete charge transfer due to interface state trapping.

I. INTRODUCTION

THE incomplete charge transfer due to trapping in interface states at the semiconductor-oxide interface imposes limitations on the performance of charge-coupled devices at moderate and low frequencies, where the incomplete free charge transfer is very small [1]–[5]. Several authors [6]–[8] have studied the effects of interface state trapping. Carnes and Kosonocky [7] have measured the large signal losses due to the interface states trapping in charge-coupled devices. Tompsett [8] has also calculated the transfer inefficiency and the reduction in the signal-to-noise ratio (SNR) of the output signal due to interface states for three-phase charge-coupled devices.

This paper presents a study of the incomplete charge transfer due to trapping in interface states in overlapping gate charge-coupled devices¹ operated with a background

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¹We have considered the overlapping gate structure as it seems presently to be the most technically promising CCD structure for the potential large scale applications of these devices [2], [4]. However, most of the analysis, discussion, and conclusions given in this paper apply also to the other CCD structures.

charge and its dependence on frequency, device parameters, dimensions, and clocking waveforms, to establish guiding design rules for the operation of these devices with optimum performance. Section II describes how trapping in interface states results in incomplete transfer. Section III presents the theoretical model and the basis of our approximations. Sections IV–VII derive expressions for the net charge trapped in the interface states under the storage gates, the transfer gates, and the edges of the gates. Section VIII calculates the signal degradation due to trapping in interface states for a two-phase overlapping gate charge-coupled device. A discussion of the results and conclusions is presented in Sections IX and X.

II. INCOMPLETE CHARGE TRANSFER DUE TO TRAPPING IN INTERFACE STATES

In Fig. 1, one unit cell of an overlapping gate charge-coupled device using silicon gate technology is shown [9]. If a voltage is applied to one of the storage electrodes, a potential well is created at the interface where signal charge can be stored. Some of this charge will be trapped in interface states. During the first stages of the transfer of charge to the next storage site, some carriers will also be trapped in interface states under the transfer gates. In the latter stages of the transfer process, the relatively large fringing fields under the transfer gates sweep out the mobile carriers very rapidly and the interface states then start to emit the captured carriers. According to the Shockley–Read–Hall rate equations [10] the emission time constant τ_e of the interface states varies exponentially with their energy level relative to the band edge. If the emission time constant of the interface states in a given energy range is smaller than the transfer time, then most of the trapped carriers in these

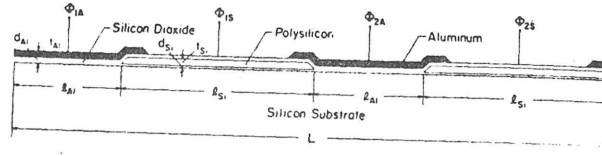


Fig. 1. One unit cell of the overlapping gate structure using the silicon gate technology.

states are emitted and can join the main packet. Interface states with an emission time constant equal or larger than the transfer time will emit only a fraction of the trapped carriers. Since the storage gate is longer and has a thinner oxide than the transfer gate, the fringing fields under it are much smaller than under the transfer gate. The residual charge under the storage gate, in the latter stages of the charge transfer process, decreases exponentially with a time constant that depends on thermal diffusion and the small fringing fields [1]-[3], [14]. Interface states continue to capture carriers from the residual signal charge until the residual charge becomes so small that emission from the traps becomes dominant. The nonemitted trapped carriers under the storage gate and the transfer gate are thus lost from the signal charge and will be emitted in the succeeding packets. If the next signal samples do not contain any charge, the interface states continue to emit the captured carriers until a signal sample containing charge passes. Then the empty interface state fill by capturing carriers from that signal sample. After its transfer, the trapped carriers are emitted and so on.

The charge captured by interface states from a large charge packet passing through the device is larger than the charge emitted into that packet, unless it has been preceded by an equal or larger charge packet. But the charge captured by interface states from a small charge packet passing through the device is smaller than the charge emitted into that packet, unless it has been preceded by an equal or smaller charge packet. Thus the interaction of the signal charge with the interface states results in incomplete transfer of charge from one storage site to another and imposes limitations on the performance of the overlapping gates charge-coupled devices.

The signal degradation due to the trapping of carriers in the interface states can be considerably reduced by using the fat zero scheme. In this scheme the zero signal is represented by a small background charge or "fat zero," so that charge packets are always flowing across the device [6]. Hence the interface states under the storage and transfer electrodes are filled every cycle. The net charge trapped from a signal charge packet will then be the difference between the captured charge it lost at each transfer and the charge emitted into that packet, by the interface states under the storage and transfer gates, which was trapped from the preceding charge packets. Since for a sufficiently large fat zero charge the capture time constant of the interface state

is very small (as discussed later), the interface states will be almost completely filled during each cycle and similar net trapping occurs during every cycle. The incomplete transfer due to trapping in interface states is consequently reduced by orders of magnitude.

III. MODEL AND APPROXIMATIONS

The interface states at the semiconductor-oxide interface are characterized by their density $N_{ss}(E)$ and capture cross section $\sigma_h(E)$. The capture and release of charge from these states is described by the Shockley-Read-Hall equation [10]. Assuming a p-channel² device and assuming that the interface is always kept under depletion to exclude the majority carrier and suppress any recombination between the trapped holes and electrons, the rate equation describing the occupation of the interface states at any energy E above the valence band is given by

$$\frac{dn_{ss}}{dt} = K_1(N_{ss} - n_{ss})p - K_2n_{ss} \exp(-E/KT) \quad (1a)$$

$$K_1 = \sigma_h V_{th}/d \quad (1b)$$

$$K_2 = \sigma_h V_{th} N_v \quad (1c)$$

where N_{ss} is the interface state density (states/cm² · eV), n_{ss} the density of filled interface (states/cm² · eV), and p the density per unit area of the mobile holes in the valence band at the interface. σ_h is the trap capture cross section for holes and V_{th} the average thermal velocity of the mobile carriers. d is the average thickness of the inversion layer at the interface, N_v the density of states in the valence band, and KT the electron-volt equivalent of temperature.

The first term describes the rate of capture of the mobile carrier and is proportional to the density p of the available mobile carriers and the density of the empty traps ($N_{ss} - n_{ss}$). The second term describes the rate of emission of the trapped carrier. This term is proportional to the density of the filled interface states and decreases exponentially as the trap energy increases.

The total rate of capture of the mobile carrier is then given by

$$\text{rate of capture} = -\left. \frac{dp}{dt} \right|_{\text{capture}} = \int_0^{E_f} \frac{dn_{ss}}{dt} dE, \quad (2)$$

² The same discussion and analysis given below holds for n-channel devices. In this case the mobile electrons interact mostly with interface states near the conduction band edge.

where E_g is the energy gap. The mobile carrier continuity equation that describes the performance of the device must be modified to include this capture rate [2] (neglecting thermal generation currents):

$$\frac{\partial q}{\partial t} = -\nabla_x \cdot (J) - e \left. \frac{dp}{dt} \right|_{\text{capture}} \quad (3)$$

where q is the surface charge density of the mobile carrier, e the electronic charge, J the sheet current density, and x the distance along the interface.

Thus, from the rigorous standpoint, the continuity equation (3) should be solved simultaneously with the nonequilibrium rate equations (1a) and (2) in the regions under the source and receiving storage gates and transfer gate. While a rigorous treatment is conceptually possible, the uncertainty in the parameters characterizing the interface states makes such an elaborate calculation unwarranted. However, with suitable approximations one can make calculations that give qualitatively reliable and quantitatively suggestive estimates of the incomplete transfer due to interface state trapping.

When charge-coupled devices are operated with the circulating background charge, interface states having an emission time constant larger than the cycle time remain almost completely filled all the time. These states capture carriers every cycle and do not get a chance to reemit an appreciable fraction of the captured carriers during the cycle time. Interface states with an emission time constant much less than the cycle time will be emptying and filling every cycle. These interface states have an energy of a few KT above the valence band edge (as shown later). Hence the interface states that make a substantial contribution to the incomplete transfer will be those with a time constant of the order of the clock cycle period and will lie within an energy range of the order of the thermal voltage. For the low interface state density obtainable with the present thermally grown oxide [11]–[13] the rate of capture or emission is quite small compared to the other terms in (3). Thus, one can obtain an accurate solution by the following procedure. First, the term in (3) due to trapping is neglected, and the continuity equation is solved to obtain the free charge transfer characteristics. The surface charge density profiles $q(x, t)$ are then used with the rate equations (1) and (2) to calculate the incomplete charge transfer due to trapping in interface states.

The precise values of the interface state density N_{ss} and capture cross section σ_h of the interface states; their distribution in energy over the bandgap; and their dependence on temperature, normal and tangential surface fields are not well known, and vary strongly with the type and preparation of the oxide over the active channel of the device [11]–[13]. For our purposes here, we will take N_{ss} and σ_h independent of all the previously mentioned parameters. However, if the exact energy dependence of N_{ss} and σ_h in the relevant part of the bandgap is accurately known, it can be easily incorporated

in this model. Consistent with the same order of accuracy of the previous assumptions, we can also use average values of the mobile carrier concentration and neglect the effect of their spatial distribution under the electrodes, to further simplify the numerical calculation.

IV. TRAP OCCUPATION IN STEADY STATE AND TRANSIENT

In steady state, the trap occupation can be obtained from (1a) and is given by

$$n_{ss} = \frac{N_{ss}}{\left(1 + \frac{K_2 \exp(-E/KT)}{K_1 p}\right)} \quad (4)$$

The interface states are in equilibrium with the mobile carriers. Their occupation is described by the same quasi-Fermi level as the mobile carriers.

$$E_f = KT \ln \frac{K_2}{K_1 p} = KT \ln \frac{N_{ss} \cdot d}{p} \quad (5)$$

Following a sudden abrupt change in the mobile carrier concentration, say p_0 to p_1 , the trap occupation changes to the new steady-state value corresponding to the new mobile carrier concentration p_1 with an effective time constant given by

$$\tau_{eff} = \frac{1}{K_1 p_1 + K_2 \exp(-E/KT)} \quad (6)$$

If the effective time constant of the interface states τ_{eff} is smaller than the time constant τ measuring the variation of the mobile carrier density, then the trap occupation reaches steady state very rapidly and effectively equilibrates with the varying carrier density. That is, if $\tau > \tau_{eff}$, then

$$n_{ss}(t) = N_{ss} / \left[1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t)}\right] \quad (7)$$

Thus, the quasi-Fermi levels of the traps follows the quasi-Fermi level of the mobile carriers

$$E_f(t) = KT \ln \frac{N_{ss} \cdot d}{p(t)} \quad (8)$$

On the other hand, if $\tau < \tau_{eff}$, then the trap occupation fails to follow the variation of the mobile carrier. If we let $K_1 p(t) \gg K_2 \exp(-E/KT)$, then this occurs when the mobile carrier density falls to a level such that

$$K_1 \tau p(t) < 1. \quad (9)$$

For charge transfer from under a gate, we can define two regimes. First, when $K_1 p(t) \tau > 1$, the mobile carrier is in effective equilibrium with the trapped charge. The total number of trapped carriers p_{tr} is given by

$$p_{tr}(t) = N_{ss} \left[E_g - KT \ln \frac{K_2}{K_1 p(t)} \right] \quad (10)$$

Second, when $K_1 p(t) \tau < 1$, the mobile charge is no longer in equilibrium with the trapped charge. If we let t_4 be the time the emission mechanism becomes dominant,

then for $t > t_4$ the trap occupation is given by

$$n_{..}(t) = \frac{N_{..}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t_4)}} \cdot \exp[-(t - t_4)K_2 \exp(-E/KT)]; \quad (11)$$

and the interface states start to empty with a time constant that increases exponentially with the trap energy. The total number of trapped carriers is given by

$$p_{..}(t) = N_{..} \left[E_0 - KT \ln K_2(t - t_4) - \frac{KT}{(t - t_4)K_1 p(t_4)} \right], \quad t > t_4. \quad (12)$$

So in this case the interface states above $E_f = KT \ln K_2(t - t_4)$ are almost full and those below it are nearly empty. The last terms in (10) and (12) show the dependence of the interface state occupation on the mobile carrier density.

V. TRAPPING IN INTERFACE STATES UNDER THE STORAGE GATES

When a signal charge packet is stored under the storage gate, all the interface states trap carriers and are filled very rapidly down to a quasi-Fermi level given by (5). As the charge transfers to the next storage site, the residual charge decreases. In the complete charge transfer mode³ the transfer of charge at the end of the charge transfer process (say after a time t_3) becomes limited by thermal diffusion and fringing fields. The residual charge under the storage gate is then given by

$$p(t) = p(t_3) \exp[-(t - t_3)/\tau], \quad t > t_3, \quad (13)$$

where the characteristic time constant τ depends on diffusion and fringing fields [2], [14].

Since the fringing fields under the storage gate are relatively small giving a rather large value of τ and the charge $p(t_3)$ is relatively large, the inequality

$$\tau K_1 p(t_3) > 1 \quad (14)$$

is satisfied at the beginning of this time interval. Hence, the mobile charge is in equilibrium with the trapped charge. However, at later times the free carrier density may fall to such a value that the interface states are no longer in equilibrium with the free carriers and the interface states begin to simply emit the charge trapped in them. This state prevails for times t such that

$$t > t_4 = t_3 + \tau \ln(K_1 p(t_3) \tau). \quad (15)$$

If the clock frequency f_0 is such that the charge transfer ends at a time t less than t_4 , then the interface states will remain filled down to an energy defined by (8). When the next charge packet arrives, it fills all the interface states, and after it transfers the total number

³ In the complete charge transfer mode all the charge under the storage gate is transferred to the following gates: none is deliberately retained. (See [2] and [5].)

of trapped carriers is given by (10) with the proper value of $p(t)$. So, when the device is operated with a circulating background charge, or fat zero, the net charge trapped from a signal charge packet is maximum when it is preceded by a fat zero and is given by

$$\Delta q_{..} = eA_{..}N_{..}KT \ln \frac{p_s(t)}{p_0(t)}, \quad (16)$$

where $\Delta q_{..}$ is the net charge trapped per transfer, $A_{..}$ the area of the storage gate, $p_0(t)$ and $p_s(t)$ are the residual charge under the storage gate at the end of the transfer time t for the fat zero charge and the signal charge, respectively. When the difference between $p_s(t)$ and $p_0(t)$, is relatively small, then

$$\Delta q_{..} = eA_{..}N_{..}KT \frac{(p_s(t) - p_0(t))}{p_0(t)}. \quad (17)$$

It follows from (13) and (17) that the net charge trapped is almost independent of frequency. In addition all the interface states above an energy E_1 where

$$E_1 = KT \ln \frac{K_2}{K_1 p(1/2f_0)} \quad (18)$$

will always be filled with captured holes. If the charge transfer ends after a time $t > t_4$, then in the complete charge transfer the interface states under the original storage gate continue to emit the trapped charge for one whole transfer (or $(m - 1)$ transfer times for m transfers/cycle). This released charge is added to the next packet transferred into this storage bucket. When the next charge packet comes along, all the interface states are filled again. After this charge packet transfers, the interface states start to emit and so on. So when the device is operated with a circulating background charge, the net charge trapped from a signal charge packet at each transfer, for transfer time $t > t_4 + \tau$, is also maximum when preceded by a fat zero and can be obtained directly from (12).

$$\Delta q_{..} = eRA_{..}N_{..}KT \frac{1}{(t - t_4)K_1} \left[\frac{1}{p_0(t_4)} - \frac{1}{p_s(t_4)} \right] \quad (19)$$

where $p_0(t_4)$ and $p_s(t_4)$ are the residual charge under the storage gate after a time t_4 [as defined in (15)] for the fat zero charge and the signal charge, respectively, and R is a fraction given by

$$R = \frac{(m - 1)t}{mt - t_4} = \frac{m - 1}{m} \cdot \frac{1}{1 - f_0 t_4}, \quad (20)$$

where m is the number of transfers/bit. If t_4 is smaller than the cycle time, then $t_4 f_0 < 1$ and for $m = 2$, $R \approx \frac{1}{2}$. If the difference between $p_s(t_4)$ and $p_0(t_4)$ is relatively small, then

$$\Delta q_{..} = \frac{1}{2} eA_{..}N_{..}KT \frac{\tau}{(t - t_4)} \frac{[p_s(t_4) - p_0(t_4)]}{p_0(t_4)}. \quad (21)$$

Thus, for transfer times $t > t_4 + \tau$, the net charge trapped/transfer decreases almost directly with the clock

frequency. Also, all the interface states above an energy E_1 are filled with captured holes. E_1 is almost independent of the signal charge and is given by

$$E_1 = KT \ln K_2(mt - t_i). \quad (22)$$

VI. TRAPPING IN INTERFACE STATES UNDER THE TRANSFER GATES

The surface potential and the surface potential gradient under the gates of an overlapping gate charge-coupled device along the silicon-silicon oxide interface are plotted in Fig. 2. These plots are obtained from a solution of the two-dimensional Poisson equation for substrate doping of $8 \times 10^{14}/\text{cm}^3$ and $10^{14}/\text{cm}^3$ [14]. The electrode voltages correspond to the latter stages of the charge transfer with a signal charge in the receiving storage gate. Since the transfer gate is shorter and has a thicker oxide than the storage gate, the fringing fields under it are much larger than under the storage gate. Typical values of single carriers transit time under the transfer gate are of the order of a few nanoseconds.

When a signal charge packet transfers from one storage site to the next, interface states under the transfer gate trap some of the charge during the first stages of the transfer process. Since fringing fields under the transfer gates are relatively large, the mobile carriers are swept out very rapidly and the emptying of the interface states begins earlier in the transfer process. Thus for all transfer times t of interest

$$t > t_{itr}. \quad (23)$$

The trapped carriers emitted before the transfer ends will join the main packet. During the latter times of the cycle, a larger fraction γ of the emitted carrier will drift backwards to join the succeeding packet of charge, and a smaller fraction $(1 - \gamma)$ will drift forward to join the original packet of charge. Because of the asymmetrical surface potential distribution γ is greater than one half. Then in the next cycle, during the transfer of the next packet of charge, the interface states under the transfer gate capture some charge, and so on. From the plots of the average mobile carrier concentration under the transfer gates for a two-phase overlapping gate CCD in Figs. 3 and 5, it is clear that the interface states will capture carriers for a time interval Δt . During that time interval an average carrier concentration p_{av} may be defined. The traps fill with an effective time constant τ_{eff} given by

$$\tau_{eff} = \frac{1}{K_1 p_{av} + K_2 \exp(-E/KT)} \approx \frac{1}{K_1 p_{av}}. \quad (24)$$

The filling probability or the fill factor F of the traps is given by

$$F = [1 - \exp(-\Delta t/\tau_{eff})]. \quad (25)$$

For transfer times $t > t_{itr}$, the interface states empty according to (11) and the total trapped carriers is given

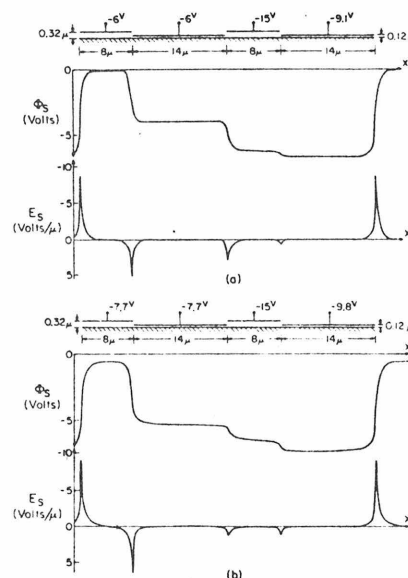


Fig. 2. Plots of the surface potential and surface potential gradient along the silicon-silicon oxide interface obtained from the solution of the two-dimensional Poisson equation of the structure in Fig. 1 with minimum geometry dimensions. $l_{s1} = 8 \mu$, $l_{s2} = 14 \mu$, $d_{s1} = 1200 \text{ \AA}$, $d_{s2} = 3200 \text{ \AA}$, $t_{s1} = 0.5 \mu$, and $t_{s2} = 0.5 \mu$. The electrode voltages correspond to the latter stages of the charge transfer, with a signal charge in the receiving storage gate. The substrate doping is 0.8×10^{15} donors/cm³ in Fig. 2(a) and 10^{14} donors/cm³ in Fig. 2(b).

by (12). When the device is operated with a circulating background charge or fat zero, the net charge trapped from the signal charge in interface states under the transfer gates is maximum when it is preceded by a fat zero and is given by

$$\Delta q_{tr} = \gamma e A_{tr} N_{it} K T \left\{ F_s \ln \left(\frac{\frac{1}{f_0} - t_{itr}}{\frac{1}{mf_0} - t_{itr}} \right) - F_0 \ln \left(\frac{\frac{1}{f_0} - t_{itr}}{\frac{1}{mf_0} - t_{itr}} \right) \right\} + \frac{R}{\left(\frac{1}{mf_0} - t_{itr} \right)} \left(\frac{F_0}{K_1 p_{av0}} - \frac{F_s}{K_1 p_{av}} \right), \quad (26)$$

where R is a fraction given by (20). p_{av0} , p_{av} are the average mobile carrier concentration under the transfer gate during the interval Δt for a background charge and a signal charge, respectively. F_0 , F_s are the filling probability as defined by (25) for a background charge and a signal charge, respectively. A_{tr} is the area under the transfer electrodes and t_{itr} , t_{itr} are the times at which the emptying of the interface states start for the background charge and the signal charge.

Two special cases are of interest. First, if the fill factors F_s and F_0 are less than one and unequal, then the first two

terms dominate. For $\gamma = 1$ and $t_{4,s} \approx t_{4,r}$, (26) reduces to

$$\Delta q_{tr} = eA_{tr}N_{tr}KT(F_s - F_0) \ln m \frac{(1 - f_0 t_{4,tr})}{(1 - m f_0 t_{4,tr})}$$

For $f_0 t_{4,tr} \ll 1$ and $m = 2$,

$$\Delta q_{tr} = eA_{tr}N_{tr}KT(F_s - F_0) \ln 2. \quad (27)$$

Second, if the fill factors are equal to one ($\Delta t/\tau_{ct} \gg 1$), then (26) reduces to

$$\Delta q_{tr} = eA_{tr}N_{tr}KT$$

$$\left\{ \frac{\delta(t_i)}{(t - t_{4,tr})} R + \frac{R}{(t - t_{4,tr})} \left(\frac{1}{K_1 p_{av0}} - \frac{1}{K_1 p_{av1}} \right) \right\}$$

For $f_0 t_i \ll 1$, $m = 2$, $R \approx \frac{1}{2}$

$$\Delta q_{tr} = eA_{tr}N_{tr}KT \left\{ f_0 \delta(t_i) + f_0 \left(\frac{1}{K_1 p_{av0}} - \frac{1}{K_1 p_{av1}} \right) \right\}, \quad (28)$$

where $\delta(t_i)$ is the difference in the time t_i at which the emptying of the interface states start for the signal charge and the background charge.

In the first case, the net charge trapped is almost frequency independent. While in the second case it increases almost linearly with frequency.

All the interface states under the transfer gate above an energy E_1 are filled with captured holes. E_1 is almost independent of the signal charge but depends on the clock frequency and is given by

$$E_1 = KT \ln K_2 \left(\frac{1}{f_0} - t_i \right) \cong KT \ln \frac{K_2}{f_0}. \quad (29)$$

VII. TRAPPING IN THE INTERFACE STATES UNDER THE EDGES OF THE GATES

Trapping in the interface states under the edges of the storage and transfer gates also add to the incomplete charge transfer [8]. Since the precise area covered by the charge being transferred at the interface depends upon the surface potential profiles under the gates which in turn depends on the surface charge density, the number of interface states at the edges that come in contact with the charge is dependent upon the amount of surface charge. The surface potential profile for a given surface charge density and sequence of potentials applied to the gate electrodes is obtained by solving the two dimensional Poisson equation for the CCD structure. Solutions [2], [9], [14] to this equation along and perpendicular to the active channel show that fringing fields penetrate under the edges of the gates for a distance of approximately a depletion layer thickness. The onset of these fringing fields define the spatial extent of the mobile charge. For fixed voltages applied to the gates, the depletion layer thickness and the penetration of fringing fields increase with decreasing surface charge. Hence a small surface charge is confined to a smaller area at the interface than a larger charge.

In the treatment of trapping and release of charge by these interface states, we must distinguish between the interface states at the gate edges parallel to the channel from those at the gate edges perpendicular to the channel.

In the case of the interface states at the edges perpendicular to the channel, the signal charge or the background charge flows over the interface states during every cycle. Thus the interface state can capture carrier from both the signal charge and background charge. Hence, the filling and emptying of these interface states is similar to that under the transfer gates.⁴

The net charge trapped from a signal charge in the interface state under the perpendicular edges when the device is operated with fat zeros is maximum when it is preceded by a fat zero. If the probability of filling of the interface states by the background charge is less than unity, then from (27)

$$\Delta q_{\perp} = eA_{\perp}N_{tr}KT(1 - F_0) \ln 2, \quad (30)$$

where A_{\perp} is the area under the perpendicular edges and F_0 is the fill factor for the background charge defined by (25). In the case F_0 is almost equal to unity, then from (28)

$$\Delta q_{\perp} = eA_{\perp}N_{tr}KT \left\{ f_0 \delta(t_i) + f_0 \left(\frac{1}{K_1 p_{av0}} - \frac{1}{K_1 p_{av,edge}} \right) \right\}. \quad (31)$$

In the case of the interface states parallel to the edges we must distinguish between two clocking schemes, the drop clock and the push clock. With drop clocks the signal charge is stored below a gate at a holding voltage V_1 which is a fraction of the largest clock voltage V_m that the MOS structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates, and the charge flows to the potential minimum thus created. With push clocks the charge is stored under a gate held at V_m , and transferred to a nearby gate, also at V_m , by raising the potential of the gate where the charge has been residing and thus "pushing" the charge to the next gate. Charge-coupled devices can be operated with two-phase, three-phase, or four-phase clocking schemes by push clocks, drop clocks, or a combination of push and drop clocks [2], [5], [15].

So with drop clocks, the charge transfer is effected by creating deeper potential wells under the next gates; and the background charge does not flow over the edges of the gates parallel to the channel. Thus the interface states under the parallel edges capture carriers from the signal charge but do not trap any carriers from the background charge; and the parallel edges are residual areas of the

⁴ Note that in this case, since the signal charge remains under the storage electrode for one whole transfer time, the probability of filling the interface states by the signal charge F_s is equal to unity. As discussed in Section VI, we may also obtain the average mobile charge density under the edges $p_{av,edge}$ and p_{av0} and the time interval Δt_s for which the background charge is in contact with the edges from the charge transfer dynamics and the surface charge density profile of the signal charge under the electrodes.

active channel that the background charge cannot reach. For example, after a signal charge is transferred from under the storage gate, the interface states under the parallel edges of this gate continue to emit the trapped carriers until the next signal charge passes, then the interface states fill again. The net charge trapped from the signal charge in the interface states under the parallel edges of the storage and transfer gates increases with increasing the number of fat zeros preceding it. This is unlike the net trapped charge in interface states under the storage gates, transfer gates, and the perpendicular edges that is almost independent of the number of fat zeros preceding the signal charge.

The net charge trapped in the interface states under the parallel edges increases logarithmically with the clock frequency (similar to the charge trapped when no fat zeros are used) [7]. For digital signals, the net trapped charge per transfer in the interface states under the parallel edges from the first "one bit" preceded by n_{zero} "zero bits" can be easily obtained from (12).

$$\Delta q_{e1} = eKT(N_{st}A_{st,e1} + N_{st}F_sA_{tr,e1}) \cdot \ln \left[\frac{(n_{zero} + 1/M) - t_{e1}}{f_0} \right] / \left(\frac{1}{mf_0} - t_{e1} \right) \quad (32)$$

where A_{st} and A_{tr} are the area of the edges parallel to the channel under the storage and transfer gates respectively. t_{e1} is the time at which the emptying of the interface states under the parallel edges start. For $f_0 t_{e1} \ll 1$ and $m = 2$ (32) reduces to

$$\Delta q_{e1} = eKT(N_{st}A_{st,e1} + N_{st}F_sA_{tr,e1}) \ln(2n_{zero} + 1). \quad (33)$$

In this case, all the interface states under the parallel edges above an energy E_1 , where for $n_{zero} \gg 1$

$$E_1 \cong KT \ln K_2 \left((n_{zero} + 1) \frac{1}{f_0} - t_{e1} \right), \quad (34)$$

are filled with the captured holes.

But with push clocks, the trapping effects under the parallel edges are reduced. The charge transfer characteristics and the charge profiles under the gates for the signal charge and the fat zero charge tend to be more similar with push clocks, [2], [5], [15]; hence the interaction of the traps with the mobile carriers of both charges is almost the same. For example, with the two-phase push clock, the charge transfer does not start until the surface potential under the storage gate is larger than that under the next transfer gate for both the fat zero charge and the signal charge. Hence the fat zero charge covers almost the same area covered by the signal charge at the interface under the storage gates before the charge transfer begins. Thus with push clocks, the behavior of most of the parallel edge area of the storage gates is similar to the behavior of the perpendicular edges and hence is described by (30) and (31). So the effective area of the parallel edges under the gates that interact with

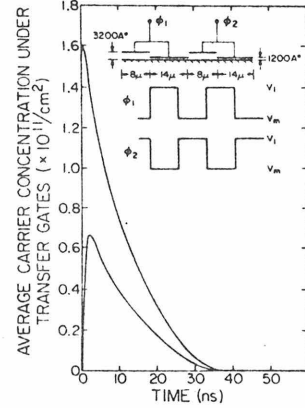


Fig. 3. Average carrier concentration under the transfer gates versus transfer time for the fat zero and signal charge. A two-phase drop clock with zero fall and rise time is used. $V_m = -15$ V, $V_1 = -7$ V.

the mobile carriers according to (32) and (33) is much smaller with push clocks than with drop clocks.

VIII. NUMERICAL RESULTS

When the device is operated with a circulating background charge the total net charge trapped from a large charge packet in interface states at each transfer is obtained by summing the different contributions obtained above:

$$\Delta q = \Delta q_{st} + \Delta q_{tr} + \Delta q_{\perp} + \Delta q_{\parallel}. \quad (35)$$

The same net charge Δq is emitted to the background charge by the interface states when it is preceded by a large signal charge. The influence of this incomplete charge transfer due to trapping in interface states on the signal degradation is best described by the signal degradation factor ϵ , defined by Berglund [16]:

$$\epsilon = \frac{\Delta q}{q_s - q_0} = \epsilon_{st} + \epsilon_{tr} + \epsilon_{\perp} + \epsilon_{\parallel}, \quad (36)$$

where q_s is the signal charge and q_0 is the background charge, so $q_s = eA_{st}p_s$ and $q_0 = eA_{st}p_0$. ϵ_{st} , ϵ_{tr} , ϵ_{\perp} , ϵ_{\parallel} are the signal degradation factors due to trapping in interface states under the storage gate, transfer gate, and the perpendicular and parallel edges of the gates, respectively. p_s and p_0 are the mobile carrier densities for the signal charge and the background charge, respectively.

We have evaluated the relative magnitudes of the signal degradation factors for an overlapping gate charge-coupled device with dimensions consistent with typical layout tolerances of silicon gate technology. The storage polysilicon gates are 14μ long and 8μ apart. The channel width is 8μ . The results in Figs. 3-6 are taken from a detailed numerical solution of the transport dynamics in p-channel devices with a substrate doping of $0.8 \times$

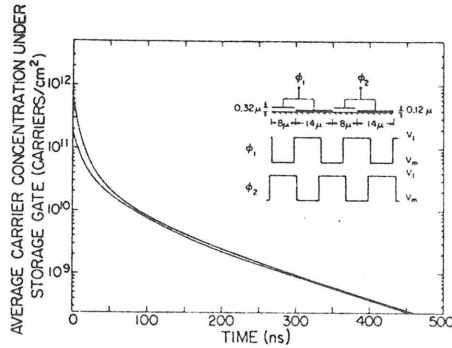


Fig. 4. Average carrier concentration under the storage gates versus transfer time for the fat zero and signal charge. A two-phase drop clock with zero fall and rise times is used. $V_m = -15$ V, $V_s = -7$ V.

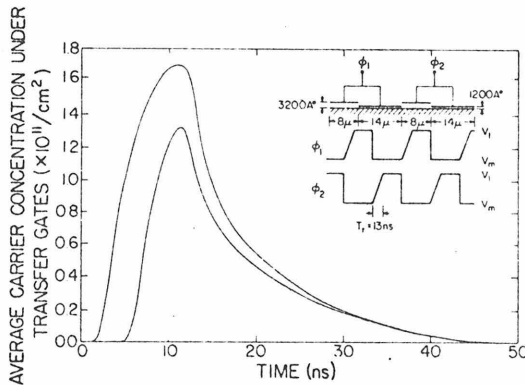


Fig. 5. Average carrier concentration under the transfer gates versus transfer time for the fat zero and signal charge. A two-phase push clock with zero fall time and 13-ns rise time is used. $V_m = -15$ V, $V_s = -6$ V.

$10^{15}/\text{cm}^3$ and minimum geometry dimensions operated in the complete charge transfer modes [2]. In Figs. 3 and 4 the average mobile carrier concentration under the storage and transfer gates is plotted versus time when a two-phase drop clock is used. The same plots for a two-phase push clock are shown in Figs. 5 and 6.

In Table I we have listed the values of the quantities used to evaluate the signal degradation from the previous equations. An average value of N_{ss} and σ_n was taken in agreement with the published values in the literature [11]–[13]. With a substrate doping of $0.8 \times 10^{15}/\text{cm}^3$ and for the minimum geometry dimensions, fringing fields under the storage electrodes are negligible [1], [2], [14]. Hence the time constant of the exponential decrease of the residual carrier under the storage gate is the thermal diffusion time constant $\tau_d = l_{si}^2/2.5D$. The time intervals Δt (which are the times the carriers spend under the transfer gates and the perpendicular edges) are taken from Figs. 3 and 5.

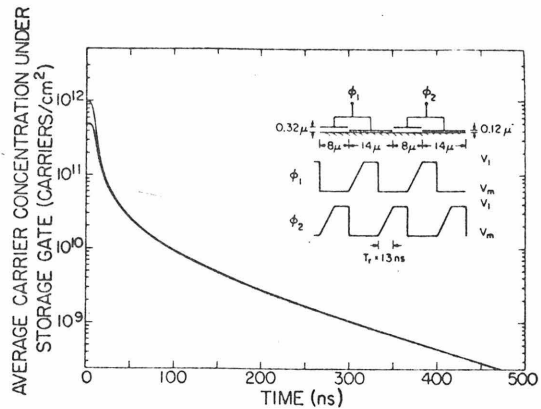


Fig. 6. Average carrier concentration under the storage gates versus transfer time for the fat zero and signal charge. A two-phase push clock is used. $T_r = 13$ ns, $V_m = -15$ V, and $V_s = -6$ V.

Zero fall and rise time for the two-phase drop clock and zero fall time and 13-ns rise time for the two-phase push clock were used in the numerical simulation of the charge transfer characteristics shown in Figs. 3–6. For larger rise and fall times, the values of Δt are larger. The fill factors F_0 and F_s are then calculated using an average carrier density under the transfer gates during the time intervals Δt from Figs. 3 and 5. They are almost unity for the drop and push clocks. Hence 28 and 31 should be used to estimate Δq_{tr} and Δq_{eL} . The value of $n_{s,ss}$ in (33) was taken as unity to give the minimum value of ϵ_{eL} . The ratio of the area of the edges to the storage gate area depends on the width of the channel W , the lengths of the storage and transfer gates, and the substrate doping concentration. The values of $A_{s,er}/A_{sL}$, $A_{t,er}/A_{sL}$, and A_{eL}/A_{tL} are taken from surface potential plots of the solutions of the two-dimensional Poisson equation of the device similar to those in Fig. 2. With push clocks, the effective area of the parallel edges under the storage gates that interacts with the mobile carriers according to (32) and (33) was taken as one-tenth of the total parallel edge area under the storage gates. Actually a smaller value is expected because of the neutralization effect mentioned previously during the pushing of the charge.

In Table II we have listed the values of ϵ_{sL} , ϵ_{tr} , ϵ_{eL} , ϵ_{eS} , and ϵ for the drop and push two-phase clock at a frequency of 1 Mc for the minimum geometry device. In our calculations, we chose a suitable background charge to represent a fat zero ep_0 and a large charge to represent the signal charge ep_s , as would be used, for example, to represent the zero and the one bit in a digital serial memory. In Figs. 7 and 8 we have plotted the signal degradation factor due to incomplete free charge transfer and due to trapping in interface state versus frequency. Several conclusions become apparent for this particular

TABLE I

Values of Parameters and Constants Used in the Calculation		
$N_{ss} = 2 \times 10^{10}/\text{cm}^2 \cdot \text{eV}$	$V_{th} = 10^7 \text{ cm/s}$	$t_s \sim 150 \text{ ns}$
$\sigma_A = 10^{-15} \text{ cm}^2$	$d = 25 \text{ \AA}$	$t_{st} \sim 500 \text{ ns}$
$K_1 = 1/25 \text{ cm}^2/\text{s}$	$C_0 = 2.86 \times 10^{-8} \text{ F/cm}^2$	$\tau = 117 \text{ ns}$
$K_2 = 10^{11} \text{ s}^{-1}$	$p(t_s) = 4.5 \times 10^9/\text{cm}^2$	$A_{tr}/A_{st} = 0.58$
	$A_{s1}/A_{st} = 0.156$	
	<i>Static Drop Clock</i>	
$p_s = 6.25 \times 10^{11}/\text{cm}^2$	$p_{av \text{ edge}} = 1.57 \times 10^{11}/\text{cm}^2$	$t_{str} \cong 35 \text{ ns}$
$p_o = 1.79 \times 10^{11}/\text{cm}^2$	$\frac{p_s(t_s) - p_o(t_s)}{p_o(t_s)} = 1.75 \times 10^{-2}$	$F_s = 1 - e^{-76} = 1$
$p_{avs} = 0.5 \times 10^{11}/\text{cm}^2$	$\delta(t_s) = 6 \text{ ns}$	$F_o = 1 - e^{-41} = 1$
$p_{avo} = 0.27 \times 10^{11}/\text{cm}^2$	$\Delta t_{tr} \cong 35 \text{ ns}$	$\frac{A_{trst} + A_{stst}}{A_{st}} \Big _{W=8 \mu} = \frac{1}{10}$
	$\Delta t_{so} \cong 7 \text{ ns}$	
	<i>Dynamic Push Clock</i>	
$p_s = 9.8 \times 10^{11}/\text{cm}^2$	$p_{av \text{ edge}} = 2.45 \times 10^{11}/\text{cm}^2$	$\Delta t_{tr0} \cong 40 \text{ ns}$
$p_o = 4.6 \times 10^{11}/\text{cm}^2$	$\frac{p_s(t_s) - p_o(t_s)}{p_o(t_s)} = 1.75 \times 10^{-2}$	$t_{str} \cong 45 \text{ ns}$
$p_{ars} = 0.6 \times 10^{11}/\text{cm}^2$	$\delta(t_s) = 1.5 \text{ ns}$	$F_s = 1 - e^{-118} = 1$
$p_{avo} = 0.4 \times 10^{11}/\text{cm}^2$	$\Delta t_{tr} \cong 44 \text{ ns}$	$F_o = 1 - e^{-72} = 1$
	$\Delta t_{so} \cong 13 \text{ ns}$	
	$\frac{A_{trst} + A_{stst} \text{effective} }{A_{st}} \Big _{W=8 \mu} = \frac{1}{200}$	

device. Trapping effects due to the interface states under the storage gate are larger than those under the transfer gate and under the perpendicular edges of the storage gate.⁵ Trapping in interface states under the parallel edges of the gates is dominant at low frequencies. Also the incomplete charge transfer due to trapping in interface states when the device is operated with push clock is much less than when it is operated with drop clock. At low clock frequencies the signal degradation due to trapping interface states is larger than that due to incomplete free charge transfer. But at high frequency, the device performance is limited by the free charge transfer process.

It should be emphasized that the results shown in Figs. 7 and 8 are for a minimum geometry overlapping gate charge-coupled devices under a specific set of operation conditions. The specific values of the signal degradation due to trapping in interface states depend on the device geometry and the operating conditions. So care should be taken in extrapolating the specific values of the signal

degradation factors in Figs. 7 and 8 to other CCD structures with other dimensions under other operating conditions. The equations derived in the previous sections should be used with the device and model parameters appropriate to each case.

IX. DISCUSSION

The analysis and results given in the previous sections reveal some important and general features of the incomplete charge transfer due to trapping in interface states in charge-coupled devices. In this section we discuss some of these important features, such as the relative contribution to the signal degradation of the interface states under the storage and transfer gates and their edges; the influence of clocking waveforms and voltages, device dimensions, and parameters on the incomplete charge transfer due to trapping in interface states, and design features of CCD structures to reduce it.

When charge-coupled devices are operated with fat zeros, trapping in interface states under the edges of the gates parallel to the channel is the dominant effect at low frequencies. The parallel edges are the areas parallel to the channel at the interface under the storage and transfer gates that are covered by the signal charge and are not covered by the background charge. The interface states under the parallel edges capture charge from the signal charge only. The resulting signal degradation is almost frequency independent, varies inversely with the channel width, and depends on the information content of the signal. At low frequency the signal degradation due to trapping in the interface states under the storage gates, the transfer gates, and the perpendicular edges is relatively smaller. These interface states capture charge from both the signal charge and the background charge.

⁵ This is actually due to the following reasons. First, for a sufficiently large background charge, the mobile carriers during the first stages of the charge transfer process effectively equilibrate with the interface states under the transfer gates and the perpendicular edges. Second the area under the transfer gates and the perpendicular edges in the overlapping gate structure is usually smaller than the area under the storage gates. Third, because of the larger fringing fields under the transfer gates and the perpendicular edges, the mobile carriers are swept out very rapidly and the emptying of the interface state begin earlier in the transfer process. But under the storage gate the residual charge decreases with a relatively large time constant. The interface states under it continue to capture carriers from the residual charge and the quasi-Fermi level follows the quasi-Fermi level of the residual charge. When the residual charge becomes small enough, emission from the traps becomes dominant. This results in a change of the slope of the signal degradation due to trapping in interface states under the storage gates versus clock frequency as shown in Figs. 7 and 8.

TABLE II
NUMERICAL VALUES OF SIGNAL DEGRADATION FACTORS FOR A
P-CHANNEL MINIMUM GEOMETRY TWO-PHASE CCD AT 1-Mc
CLOCK FREQUENCY

Signal Degradation Factor Due to Trapping in Interface States Under:	Equation	Value for Drop Clock	Value for Push Clock
Storage gate ϵ_{s1}	(16)	8.4×10^{-5}	1.7×10^{-5}
Transfer gate ϵ_{t1}	(28)	3.62×10^{-6}	0.975×10^{-6}
Perpendicular edges ϵ_{p1}	(31)	1.33×10^{-6}	0.464×10^{-6}
Parallel edges ϵ_{p2}	(33)	1.64×10^{-6}	7.0×10^{-6}
Total ϵ	(36)	2.53×10^{-4}	2.54×10^{-4}

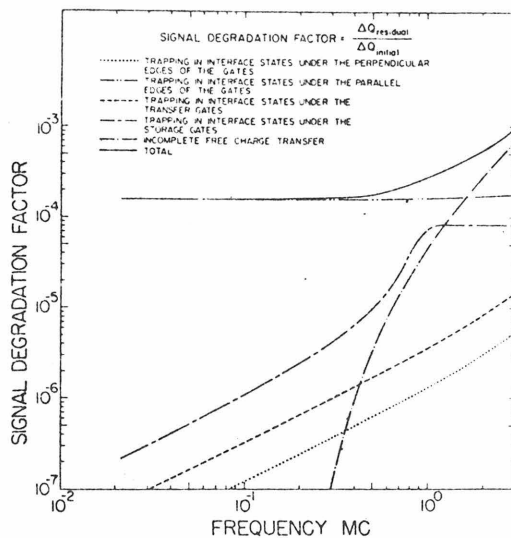


Fig. 7. Signal degradation factors versus clock frequency for the minimum geometry device operated with a two-phase drop clock.

Hence the background charge is effective in reducing the effect of trapping in these interface states on the incomplete charge transfer. For a sufficiently large background charge the effective time constant of the interface states is typically a fraction of a nanosecond. With the finite rise and fall times obtained with the practical clock drivers, and for the minimum geometry CCD devices we have considered, these interface states can equilibrate with both the signal charge and background charge. This leads to a small signal degradation that is directly proportional to frequency.

From the equations derived in Sections V-VII, and [2], [5], [15], we may conclude that increasing the clock voltage amplitude and the signal charge reduces the incomplete transfer due to trapping in interface states and the incomplete free charge transfer. Clocking waveforms that tend to reduce the incomplete free charge transfer by making the charge transfer for large and small charge similar will also reduce the incomplete charge

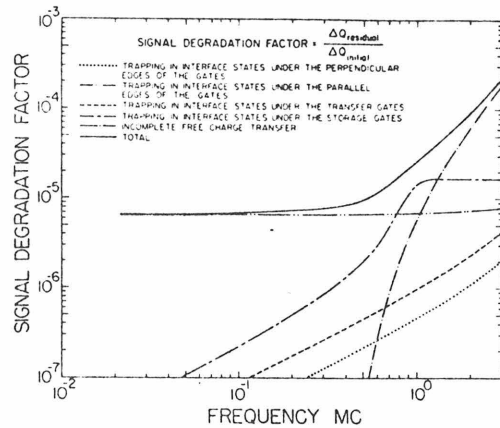


Fig. 8. Signal degradation factors versus clock frequency for the minimum geometry device operated with a two-phase push clock.

transfer due to trapping in interface states because the effective parallel edge area is reduced and the charges under the storage and transfer gates, and the time at which emptying of the interface states begins tend to be less dependent on the initial charge. For example, when the device is operated with a two-phase push clock, the incomplete charge transfer due to the interface state is reduced by over an order of magnitude over that when it is operated with a drop clock. If the device is operated in the complete charge transfer mode the other details of the clocking waveforms such as its rise time and wave-shape affect mainly the time interval Δt the charge spends under the transfer gate and the time t_4 at which the interface states starts to empty. For example, if the rise time increases, Δt and t_4 increase and the signal degradation ϵ_{s1} due to the interface states under the storage gates increases slightly. The signal degradation due to interface states under the transfer gates and the perpendicular edges ϵ_{t1} and ϵ_{p1} also increase very slightly if $\Delta t/\tau_{eff} \gg 1$, but decrease if the fill factor F_s and F_o are less than unity.

Certain design features of CCD structures may reduce the incomplete charge transfer due to the interface states. A wide active channel increases the signal charge relative to the net charge trapped in the parallel edges and hence reduces the signal degradation factor at low frequencies.⁶ Thinner oxide over the active channel increases the oxide capacity and the signal charge density. Thus, the net charge trapped under the storage gates, transfer gates,

⁶ Increasing the active channel width increases also the SNR and dynamic range of the CCD. The noise introduced to the signal charge in the storage process through the leakage and thermal generation current is proportional to the square root of the gates' area. The noise introduced during the transfer process through the fluctuations of the carriers trapped in the interface states and through suppressed transfer loss fluctuations is also proportional to the square root of the gates' area [17], [18]. But the signal charge is directly proportional to the gate area. Hence the dynamic range and SNR can be increased by increasing the active channel width of the device without degrading its high-frequency performance.

and the perpendicular edges decreases, and the area of the edges is reduced. A higher substrate doping reduces the edges' area, but also reduces the fringing fields under the storage gates and hence decreases the rate of free charge transfer. A structure with a high substrate doping (or channel stop diffusion) and a low doping under the active channel reduces the parallel edge area and increases the fringing fields at the same time. The large fringing fields reduce the incomplete free charge transfer at high frequency. The net charge trapped under the transfer and storage gates is also reduced as the interface states start to empty earlier in the transfer process. The perpendicular edge area is increased in this structure, but since in the overlapping gate CCD the effect of the perpendicular edges is relatively small, the overall effect of interface states on incomplete transfer is reduced at low frequencies. Such a structure can be easily achieved with ion implantation or otherwise. Reduction of the signal degradation due to trapping in interface states also can be achieved by decreasing the interface state density N_{ss} , for example, by using the (100) instead of the (111) substrate. Moving the charge pockets in potential wells in the bulk rather than at the interface as in buried channel CCD [19] eliminates the incomplete charge transfer and fluctuation noise due to trapping of the signal charge in the interface states. Since trapping in the defect states of the buried channel is expected to be much smaller than interface state trapping, the signal degradation in buried channel charge-coupled devices is much smaller than in surface channel CCD.

The signal degradation due to trapping in interface states limits the performance of CCD devices at low frequency, but at high frequency the signal degradation due to incomplete free charge transfer is dominant. According to the simple model we have considered, the capture cross section σ_h and the interface state density N_{ss} were taken constant for simplicity. Actually the variation of N_{ss} and σ_h with energy will change the frequency dependence of the signal degradation due to trapping in interface states from that plotted in Figs. 7 and 8. However, the frequency dependence of the signal degradation factor due to the interface states will still be weaker than that due to incomplete free charge transfer. The latter changes very rapidly with frequency, for example, in Fig. 8 it changes by more than four orders of magnitude over only one decade of frequency.

So far, we have assumed that the background charge and the signal charge are sufficiently large so that the interface states under the transfer gates and the perpendicular edges can effectively equilibrate with the mobile carriers. However, if the background charge, or the capture cross section σ_h , or the time interval Δt the carriers spend under the transfer gates and the perpendicular edges is too small, then these interface states cannot equilibrate with the mobile carriers in transit. The fill factors F_s and F_0 are thus less than unity, and the first two terms in (26) dominate at sufficiently low frequency. In this case

the contribution to the signal degradation from the interface states under the perpendicular edges and the transfer gates tends to a constant value at low frequency given by (27) and (30). This contribution is due to the difference in the filling probabilities of the interface states for the background charge and the signal charge. The contribution to the signal degradation from the interface states under the parallel edges and the storage gates increase also by decreasing the background charge. However, the trapping in the interface states under the parallel edges still remains the dominant effect especially from minimum geometry devices.

If the storage and transfer gate lengths are reduced, the time interval Δt that the charge spends under the transfer gate decreases and the relative area of the perpendicular edges increases. Also the time t_4 at which the emptying of the interface states starts decreases. Thus ϵ_{s1} slightly decreases but ϵ_{s1} increases, ϵ_{tr} decreases very slightly in the case $\Delta t/\tau_{eff} \gg 1$, but increases considerably if the filling probabilities F_s and F_0 are less than unity. The signal degradation due to the parallel edges ϵ_{s1} , which is the dominant effect, also decreases very slightly.

The interface states under the storage gates, the transfer gates, and the perpendicular edges can capture carriers every cycle from the signal charge and the fat zero charge. Hence the interface states with energy levels above E_1 [given by (18), (22), (29), and (34)] do not get a chance to reemit the captured carriers and are filled all the time. The interface states with energy between the valence band edge and the energy E_1 will be emptying and filling every cycle.⁷ For example, for digital signals, the net trapped charge from the first "one bit" in the interface states under the storage and transfer gates and the perpendicular edges is almost independent of the number of preceding "zero bits." But the net trapped charge from the first one bit in the interface states under the parallel edges increases logarithmically with the number of preceding zero bits. If a two-phase device is operated with no fat zeros, then the net trapped charge per transfer from the first one bit preceded by n_{zero} zero bits can be easily obtained from (12).

$$\begin{aligned} \Delta q = & eA_s KTN_{ss} \ln \left(\frac{n_{zero} + 1/2}{f_0} - t_{4s1} \right) / \left(\frac{1}{2f_0} - t_{4s1} \right) \\ & + eA_{tr} KTN_{ss} P_s \ln \left(\frac{n_{zero} + 1/2}{f_0} - t_{4tr} \right) / \left(\frac{1}{2f_0} - t_{4tr} \right) \\ & + eA_s KTN_{ss} \ln \left(\frac{n_{zero} + 1/2}{f_0} - t_{4s1} \right) / \left(\frac{1}{2f_0} - t_{4s1} \right) \end{aligned}$$

and for $t_{4s1} < 1/2f_0$ and $t_{4tr} \ll 1/2f_0$

$$\Delta q = eKTN_{ss}(A_{tr} + A_{s1}F_s + A_s) \ln(2n_{zero} + 1). \quad (37)$$

⁷ Thus the incomplete charge transfer due to trapping in interface states under the storage and transfer gates and the perpendicular edges is due to the variable mean occupation of the state with energy close to E_1 . Therefore the values of N_{ss} and σ_h at the energy E_1 should be used to estimate the trapping effects in these states.

The above result was used by Carnes and Kosonocky [7] to measure N_{ss} by measuring the slope of the charge loss versus $\ln n_{zero}$. However, (37) shows that the so measured value of N_{ss} is some average value of N_{ss} under the transfer and storage gate. A typical value of the signal degradation factor ϵ at each transfer in this case is about 10^{-3} , if n_{zero} is equal to unity.

Measurements of the signal degradation factor in charge-coupled devices are difficult and require long register strings for a good accuracy. The signal degradation factor due to incomplete free charge transfer at high frequencies was measured by Carnes and Kosonocky [20] using a 64-bit two-phase overlapping gate shift register. They measured a signal degradation factor of 10^{-4} at 1 Mc. Using feedback to increase the effective number of transfers, Levine [21] measured a signal degradation of 3×10^{-5} at 200 kc and 9×10^{-6} at 10 kc. Presently, the experimental data of the signal degradation factor in the overlapping gate charge-coupled devices are relatively sparse. So experimentally, the precise values of the signal degradation due to trapping in the interface states at low frequencies and its frequency dependence are not presently well known.

X. CONCLUSIONS

Using a simple model we have estimated the signal degradation due to interface states trapping in overlapping gates charge-coupled devices operated with a background charge taking into account the refilling of the in-

terface states during transfer. Our results show that the incomplete transfer due to interface states limit the performance of these devices at low frequencies. The most dominant effect is trapping in the interface states under the parallel edges (the areas parallel to the active channel at the interface under the storage and transfer gates that are covered by the signal charge and are not covered by the background charge).

For a sufficiently large background charge the interface states under the storage gates, transfer gates, and the perpendicular edges of the gates can effectively equilibrate with both the signal and background charge. Hence the incomplete charge transfer due to trapping in these interface states varies almost directly with frequency and becomes very small at sufficiently low frequency.

Some design features of CCD structures were shown to reduce the incomplete charge transfer due to interface state trapping. We have shown also that increasing the clock voltages or increasing the signal charge or using push clock instead of drop clocks reduces the incomplete charge transfer due to interface states trapping.

APPENDIX

If the mobile carrier concentration $p(t)$ is varying with time, then the transient average occupation of the interface states at an energy E above the valence band is obtained by integrating the rate equation (1). Assuming $p(t) \gg KT \cdot N_{ss}$ then we get

$$n_{ss} = K_1 N_{ss} \exp \left[- \int_0^t (K_1 p(t') + K_2 \exp(-E/KT)) dt' \right] \\ \cdot \int_0^t p(t') \exp \left[\int_0^{t'} (K_1 p(v) + K_2 \exp(-E/KT)) dv \right] dt' \\ + \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(0)}} \exp \left[- \int_0^t (K_1 p(t') + K_2 \exp(-E/KT)) dt' \right] \quad \text{for } t > 0. \quad (A1)$$

If $p(t) = p(t_3) \exp(-(t - t_3)/\tau)$ for $t > t_3$, then

$$n_{ss}(t) = K_1 N_{ss} \exp [-K_1 p(t_3) \tau (1 - \exp(-(t - t_3)/\tau)) - K_2 (t - t_3) \exp(-E/KT)] \\ \cdot \int_{t_3}^t p(t') \exp [K_1 p(t_3) \tau (1 - \exp(-(t' - t_3)/\tau)) + K_2 (t' - t_3) \exp(-E/KT)] dt' \\ + \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t_3)}} \exp [-K_1 p(t_3) \tau (1 - \exp(-(t - t_3)/\tau)) - K_2 (t - t_3) \exp(-E/KT)] \quad \text{for } t > t_3. \quad (A2)$$

This can be easily reduced to

$$n_{ss}(t) = N_{ss} K_1 \tau \exp [K_1 \tau p(t) - K_2 (t - t_3) \exp(-E/KT)] \\ \cdot [p(t) \exp (K_2 \exp(-E/KT)) E_c (K_1 \tau p(t)) - p(t_3) E_c (K_1 \tau p(t_3))] \\ + \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t_3)}} \exp [-K_1 p(t_3) \tau (1 - \exp(-(t - t_3)/\tau)) + K_2 (t - t_3) \exp(-E/KT)] \quad \text{for } t \geq t_3 \quad (A3)$$

where $E_c(x)$ is the exponential integral of order c defined by

$$E_c = \int_1^{\infty} \frac{\exp(-xv)}{x+c} dv \quad (A4)$$

and

$$p_{tr} = N_{ss}KT[E_1(K_2(t-t_4) \exp(-E_g/KT)) - E_1[K_2(t-t_4)] - E_1(K_2(t-t_4) \exp(-E_g/KT) + K_1(t-t_4)p(t_4)) + E_1(K_2(t-t_4) + K_1(t-t_4)p(t_4))].$$

$$c = \tau K_2 \exp(-E/KT). \quad (A5)$$

If $K_1\tau p(t) > 1$, then the asymptotic expansion of $E_c(x)$ can be used:

$$E_c(x) = \frac{e^{-x}}{x+c}. \quad (A6)$$

For $t > t_3 + [1/K_1p(t_3)]$, (A3) reduces to

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1p(t)}} + \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1p(t_3)}} \cdot \exp[-K_1p(t_3)\tau(1 - \exp(-(t-t_3)/\tau)) - K_2(t-t_3) \exp(-E/KT)]. \quad (A7)$$

Two special cases are of interest. First, if $K_1p(t_3)\tau > 1$, then the second term is negligible for $t > t_3 + \tau$, and (A7) reduces to

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1p(t)}}. \quad (A8)$$

Thus the interface states have a small effective time constant τ_{eff} and can equilibrate very rapidly with the mobile carrier. Assuming a constant interface state density N_{ss} states/cm²·eV and a constant capture cross section σ_h cm², the total density of trapped carriers p_{tr} is given by

$$p_{tr} = \int_0^{E_g} n_{ss}(t) dE = N_{ss}KT \ln \left[\frac{\exp(E_g/KT) + \frac{K_2}{K_1p(t)}}{1 + \frac{K_2}{K_1p(t)}} \right].$$

If $1/K_2 < [1/K_1p(t)] < 1/K_2 \exp(E_g/KT)$, then

$$p_{tr} = N_{ss} \left(E_g - KT \ln \frac{K_2}{K_1p(t)} \right). \quad (A9)$$

Second, if $K_1p(t)\tau \leq 1$, (A7) reduces to

$$n_{ss} = \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1p(t_4)}} \cdot \exp[-K_2(t-t_4) \exp(-E/KT)] \quad t > t_4, \quad (A10)$$

where t_4 is the time the emission of carriers becomes dominant and the refilling of the traps becomes negligible. It is given by

$$K_1p(t_4)\tau = 1. \quad (A11)$$

Similarly integrating (A10), we get

If $1/K_2 < t - t_4 < 1/K_2 \exp(E_g/KT)$ and $t - t_4 > [1/K_1p(t_4)]$, then we may use the asymptotic expansion of the exponential integral for small and large arguments to get

$$p_{tr} = N_{ss} \left[E_g - KT \ln K_2(t-t_4) - \frac{KT}{(t-t_4)K_1p(t_4)} \right]. \quad (A12)$$

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Chapter 4

TWO DIMENSIONAL ELECTROSTATIC ANALYSIS OF
BURIED CHANNEL CHARGE COUPLED DEVICES4.1 Introduction

Although one dimensional electrostatic calculations give a fairly good understanding of the device characteristics, it is not enough to describe the complete electrostatic characteristics of the device structure. The reason is as following: In the case of surface CCD's the minimum potential is directly controlled by the gate voltage through the thin silicon dioxide, and the resulting fringing field is relatively small. However, in the buried channel CCD the minimum potential is in the buried layer deep in the bulk and the influence of the gate voltage upon the minimum potential is smoothed out more effectively, by the neighboring electrodes resulting in high fringing fields along the direction of the charge transfer. This fact makes it necessary to consider variation of the potential not only normal to the insulator semiconductor interface but also along the direction of charge transfer. Thus, the two dimensional electrostatic analysis of buried channel CCD becomes essential to the understanding and estimation of the usefulness of this device.

In this chapter, a detailed two dimensional electrostatic analysis of buried channel CCD is presented. In the next section the results of the electrostatic analysis of the basic one dimensional MOS structure for buried channel CCD are reviewed and summarized in order to

establish a basis to the two dimensional electrostatic analysis. The simplest standard two dimensional electrostatic analysis is first described in Section 4.3 for a surface field effect transistor with p-type, epitaxially grown, metallurgical channel. This transistor structure is simple but complex enough to have many of the characteristics that are found in buried channel CCD. The gradual channel approximation for the transistor is first presented and compared with the exact two dimensional numerical calculation. Furthermore the analysis is extended to the case in which there is no mobile charge in the channel, that is, in the completely depleted channel. And it is shown that the correction in the channel potential to the gradual channel approximation is proportional to the curvature of the potential with a fairly good accuracy. In Section 4.4, the results of the two dimensional numerical calculation of the minimum potential profile in buried channel CCD are presented and it is shown in Section 4.5 that the speculation given in Section 4.3 about the relation between the minimum potential and its curvature is also valid in the more complicated structure of buried channel CCD. This physical interpretation leads to a simple capacitance model which is also discussed in Section 4.5. This simple electrostatic model replaces the two dimensional nonlinear Poisson equation by a linear second order differential equation with a single spatial coordinate. In Section 4.6, the complete dynamic charge transfer model compatible with actual numerical calculations is established with this simple capacitance model. The consequence of this dynamic charge transfer model remains to

be studied in the next chapter.

4.2 Basic One Dimensional MOS Structure

In this section we first present the channel potential ϕ_m and the gate capacitance C_g in terms of the signal charge Q and the gate voltage ϕ_{SF} . Furthermore, for a Gaussian doping profile we describe the procedure to obtain the effective p-diffusion density N_A and the effective diffusion depth X_d from the surface charge density N_s and the p-n junction depth X_g .

The expressions appearing in this section are essential in developing the later sections and are frequently quoted. To make this chapter as independent as possible from the other chapters, the review and summary of the one dimensional analysis are given here.

The salient physical parameters which appear in the basic one dimensional MOS structure consists of four fixed parameters that can be controlled in the fabrication of device, and three more variables, among which there is only one constraint during the device operations. The four fixed parameters are the oxide thickness X_o , the p-diffusion depth X_d , the p-diffusion doping concentration N_A , and the substrate doping N_d . The other three parameters are the equivalent gate voltage ϕ_{SF} , the signal charge Q and the channel potential ϕ_m . The associated constraint among the three variables can be written as an expression of the potential ϕ_m in terms of the gate voltage and the signal charge Q .

This expression establishes a procedure for calculating the minimum potential ϕ_m if the gate voltage ϕ_{SF} and the signal

charge Q are pre-specified. The procedure is outlined below.

First calculate the three parameters ϕ_t , ϕ_d and R defined by the following three equations

$$\phi_t = \frac{N_A \epsilon_{Si}}{2C_o^2} \quad , \quad (4-1a)$$

$$\frac{\phi_d}{\phi_t} = \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d}\right) \left[2 + \frac{C_o}{C_d} \left(1 - \frac{Q}{Q_d}\right)\right] \quad , \quad (4-1b)$$

and

$$R = \frac{N_A}{2N_d} \frac{\phi_t - \phi_{sF}}{\phi_d + \phi_t} \quad , \quad (4-1c)$$

where $Q_d \equiv N_d X_d$ and $C_d \equiv \epsilon_{Si}/X_d$. ϵ_{Si} is the silicon dielectric constant (648 e/volt· μ). C_o is the oxide capacitance.

Then the channel potential ϕ_m can be expressed as

$$\phi_m = - \left(1 + \frac{N_d}{N_A}\right) f(R) \left[\phi_d - \phi_{sF}\right] \quad , \quad (4-1d)$$

where $f(R)$ is a slowly varying function of R and defined by

$$f(R) = \frac{R}{1 + R + \sqrt{1 + 2R}} \quad . \quad (4-1e)$$

From these equations given above, it is also possible to express the signal charge Q in terms of the gate voltage and the minimum potential ϕ_m . The result is presented below for future use:

$$\frac{Q}{Q_d} = \left(1 + \frac{C_d}{C_o}\right) - \sqrt{\frac{-\phi_m}{\phi_q}} - \sqrt{\left(\frac{C_d}{C_o}\right)^2 + \left(\frac{\phi_{sF} - \phi_m}{\phi_p}\right)} \quad , \quad (4-2a)$$

where ϕ_p and ϕ_q are defined by

$$\phi_p = \frac{N_A X_d^2}{2 S_i} \quad , \quad (4-2b)$$

and

$$\phi_q = \left(1 + \frac{N_A}{N_d}\right) \phi_p \quad . \quad (4-2c)$$

The gate capacitance C_g can be written in general as a series combination of the oxide capacitance C_o , the surface depletion capacitance C_1 and the metallurgical junction capacitance C_2 as seen by

$$\frac{1}{C_g} = \frac{1}{C_o} + \frac{1}{C_1} + \frac{1}{C_2} \quad . \quad (4-3a)$$

If we define the two parameters A and B as seen by

$$A = \left(1 + \frac{N_d}{N_A}\right) \left(1 - \frac{Q}{Q_d}\right) + \frac{N_d}{N_A} \frac{C_d}{C_o} \quad , \quad (4-3b)$$

and

$$B = \left(1 + \frac{N_d}{N_A}\right) \left[\left(1 - \frac{Q}{Q_d}\right)^2 + \frac{\phi_{sF}}{\phi_q} \right] \quad , \quad (4-3c)$$

Then the gate capacitance C_g can be calculated from A and B by the expression given below:

$$C_g = \frac{N_d C_d}{N_A \sqrt{A^2 - B}} \quad . \quad (4-3d)$$

Observe that the parameter ϕ_q is of the order of 324 volts but the range of the gate voltage ϕ_{sF} is of the order of 20 volts. Hence, the parameter

B does not change much during the gate voltage swing. Hence the gate capacitance C_g is fairly constant with respect to gate voltage.

We are now in a position to describe the procedure to obtain the effective p-diffusion density N_A and the effective diffusion depth X_d from the surface density N_s and the p-n junction depth X_g .

The total sheet charge density Q_d in the p-diffusion layer is then given as before by $Q_d = N_A X_d$. This quantity is equal to the spatial integration of the charge density from the Si-SiO₂ interface to the p-n junction depth X_g . The charge density is described by the Gaussian charge distribution function $d(x)$ given by

$$d(x) = N_d - (N_s + N_d) \exp \left[-\alpha^2 \left(\frac{x}{X_g} \right)^2 \right] \quad , \quad (4-4a)$$

where

$$\alpha^2 \equiv \ln \left(1 + \frac{N_s}{N_d} \right) \quad . \quad (4-4b)$$

We choose the effective depth X_d to be at the reflection point of the Gaussian doping profile and obtain the expression as seen by

$$X_d = \frac{X_g}{\sqrt{\ln \left(1 + \frac{N_s}{N_d} \right)}} \quad . \quad (4-4c)$$

Since the total sheet charge density Q_d is given by

$$Q_d = \int_0^{X_g} d(x) dx = N_d X_g \left[1 - \frac{\sqrt{\pi} \exp(-\alpha^2)}{2\alpha} \operatorname{erf}(\alpha) \right] \quad , \quad (4-4d)$$

where erf is the error function, we then obtain the effective p-diffusion density N_A from the relation given by

$$N_A = \frac{Q_d}{X_d} = N_d \left[\frac{1}{\alpha} - \frac{\sqrt{\pi} \exp(\alpha^2) \operatorname{erf}(\alpha)}{2\alpha^2} \right] \quad (4-4e)$$

4.3 Surface Field Effect Transistor with Metallurgical Channel

The structure of a surface field effect transistor with p-type, epitaxial grown, metallurgical channel is depicted in Fig. 4.1a. We analyze this simple structure first in order to understand the basic underlying principles applicable also in the more complicated buried channel charge coupled device structure shown in Fig. 4.1b. Specifically we consider first the current-voltage characteristics, the turn-off voltage, the saturation current, the transconductance and the response time of the transistor. These characteristics are essential in defining the functional capabilities of the transistor and in return give a good guide line in design and estimation of the usefulness of the more complicated structure of buried channel CCD. Furthermore, the channel potential at the onset of saturation is analyzed in gradual channel approximation and compared with the exact numerical solutions. This analysis is extended to the case of the completely depleted channel, that is, no mobile charge in the channel. This study leads to a very interesting result about the channel potential profile. The channel potential seems to decay exponentially, as we go farther from the source to drain, to the final value of the drain saturation voltage. This speculation leads to the simple capacitance model to be discussed in the subsequent sections.

Returning to Fig. 4.1a, we begin the analysis with the qualitative description of the surface field effect transistor. In the following calculations, we consider only that portion of the channel which can be

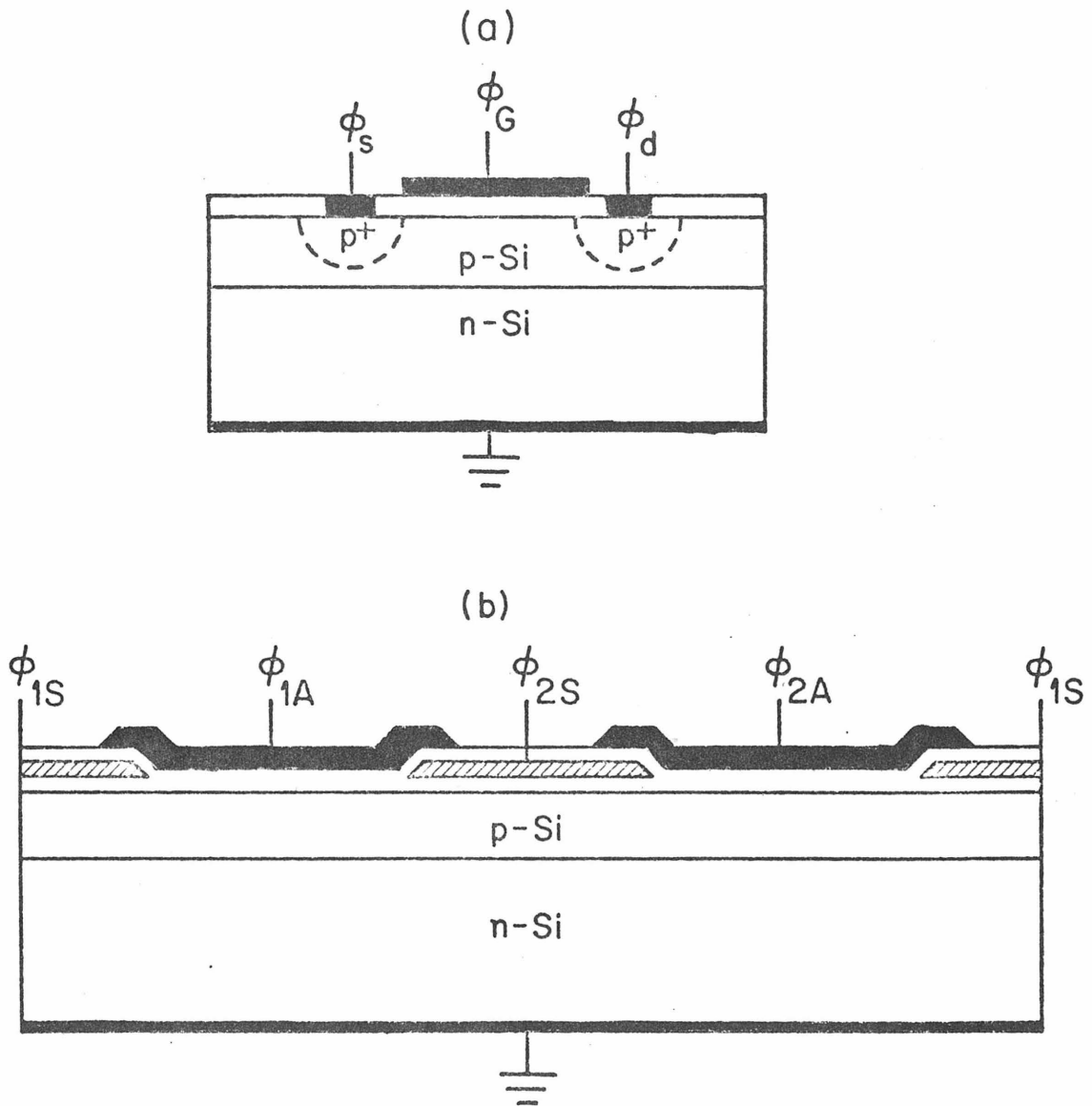


Fig. 4.1a The structure of a surface field effect transistor with a metalurgical channel. The channel is p-type, epitaxially grown.

Fig. 4.1b One unit cell of overlapping gate buried channel CCD.

modulated by the application of the gate voltage. In reality, there are series resistances present, both near the source and near the drain, which impose an IR drop between the source and drain contacts and the channel.

In normal operations, the source and drain voltages will be biased negative with respect to the substrate to maintain the p-n junction reverse biased. If the drain voltage ϕ_D is further biased negative with respect to the source voltage ϕ_S , the mobile signal charges (holes in this p-channel device) will flow from source to drain through the p-type region enclosed between the two depletion regions. The p-diffusion layer doping N_A is normally made 20 ~ 30 times larger than the substrate doping N_d . And the corresponding p-n junction depletion layer will not modulate the channel width significantly. However, the gate voltage will influence the channel width significantly through the surface electric field. The actual channel width X_{CH} can be calculated from Eq. (4-2a), knowing that the signal charge Q is simply given by the product $N_A X_{CH}$. In the relation (4-2a) we note the value of ϕ_q is much larger than ϕ_p . The last term in RHS of Eq. (4-2a) presents the modulation of the channel by the surface electric field which in turn is controlled by the effective gate voltage ϕ_{SF} . On the other hand, the p-n junction depletion width will be influenced by the channel potential ϕ_m . But because of the large value of ϕ_q , the middle term in Eq. (4-2a) is very small and the corresponding p-n junction depletion layer does not have a significant effect upon the total channel width X_{CH} .

The most important characteristic of any type of transistor is

the current-voltage relationship, and we now formulate our analysis to this goal. The calculations of the turn-off voltage, the saturation current and the transconductance are the natural extension of this following analysis.

The resistance dR of the elemental section dy of the channel is given according to gradual channel approximation by

$$dR = \frac{dy}{Z \mu_p Q(\phi_m, \phi_{SF})} \quad , \quad (4-5a)$$

where Z designates the width of the p-diffusion layer. (Recall the depth of the p-diffusion layer is denoted by I_d). The hole mobility μ_p in the bulk silicon is taken to be $480 \text{ cm}^2/\text{volt}\cdot\text{sec}$ in the later calculation. The amount of the mobile signal charge Q depends on the gate voltage ϕ_{SF} and the local channel potential ϕ_m which is also a function of the spatial coordinate y , taken along the direction of the charge transfer. The source and drain ends are defined to be located at $y = 0$ and $y = L$ respectively.

The voltage drop across the elemental section of the channel is then given by

$$dV = -I_d dR = \frac{-I_d dy}{Z \mu_p Q(\phi_m, \phi_{SF})} \quad , \quad (4-5b)$$

where I_d is the drain current which we would like to calculate in terms of the gate, source, and drain voltages. The integration of Eq. (4-5b) with the expression $Q(\phi_m, \phi_{SF})$ substituted from Eq. (4-2a)

yields the drain current I_d as seen by

$$I_d(\phi_{SF}, \phi_s, \phi_d) = G_0 \left[F(\phi_{SF}, \phi_s) - F(\phi_{SF}, \phi_d) \right] \quad , \quad (4-5c)$$

where $F(\phi_{SF}, \phi)$ is defined by

$$F(\phi_{SF}, \phi) = \left(1 + \frac{C_d}{C_0} \right) \phi + \frac{2}{3} \frac{(-\phi)^{3/2}}{\sqrt{\phi_q}} + \frac{2}{3} \phi_p \left[\left(\frac{C_d}{C_0} \right)^2 + \frac{\phi_{SF} - \phi}{\phi_p} \right]^{3/2} \quad , \quad (4-5d)$$

and G_0 is the conduction of the p-type diffusion layer, discounting the presence of the two depletion regions altogether, and given by $Z\mu_p Q_d / L$.

The channel conductance g in the linear region can be calculated by expanding the drain current at the source and taking $(\phi_d - \phi_s)$ very small. That is, in the linear region, the drain current will be given as

$$I_d(\phi_{SF}, \phi_s, \phi_d) = G_0 \frac{Q(\phi_{SF}, \phi_s)}{Q_d} \cdot (\phi_s - \phi_d) \quad , \quad (4-5e)$$

and the corresponding channel conductance g is given by taking the gate voltage ϕ_{SF} constant and as seen by

$$g(\phi_{SF}, \phi_s) = \frac{\partial I_d}{\partial (\phi_s - \phi_d)} \Bigg|_{\phi_{SF} = \text{constant}} = G_0 \frac{Q(\phi_{SF}, \phi_s)}{Q_d} \quad . \quad (4-5f)$$

We note that $Q(\phi_{SF}, \phi_s)$ is given by Eq. (4-2a), replacing the channel potential ϕ_m by the source voltage ϕ_s . The channel potential g in the

linear region is independent of the relative voltage difference ($\phi_d - \phi_s$) between the source and drain, but depends on the source ϕ_s and the gate voltage ϕ_{SF} . (Of course, in the range of validity of linear expansion, $\phi_d \approx \phi_s$).

We are now in the position to extend the above analysis to obtain the expressions for the turn-off voltage, the saturation current and the transconductance. These physical parameters are important not only in characterizing the surface field effect transistor but also in understanding the qualitative aspects of dynamic charge transfer process in buried channel CCD's

For a fixed source voltage ϕ_s , as we increase the gate voltage ϕ_{SF} , the channel conductance decreases because the surface depletion width increases as seen in the last term in RHS of Eq. (4-2a). At a certain gate voltage, the conductance vanishes altogether. This turn-off voltage can be calculated from the condition $q = 0.0$ or $Q(\phi_{SF}, \phi_s) = 0.0$ of Eq. (4-2a) to be the value $\phi_{SF} = V_T$ with V_T given by

$$V_T = \phi_s + \phi_p \left(1 - \sqrt{\frac{-\phi_s}{\phi_q}} \right) \left(1 + \frac{2C_d}{C_o} - \sqrt{\frac{-\phi_s}{\phi_q}} \right) \quad (4-6a)$$

In the linear region ($\phi_d \approx \phi_s$) with the fixed source voltage ϕ_s the condition of the zero channel width χ_{CH} is given by the gate voltage ϕ_G to the turn-off voltage V_T as seen above.

On the other hand, for a fixed gate voltage ϕ_G , the drain saturation voltage ϕ_{dsat} (or the pinch-off voltage) is defined to be the

value of the drain voltage at the zero channel width, $X_{CH} = 0.0$, at the drain terminal. This implies that the relation between the gate voltage and the drain saturation voltage $\phi_{d \text{ sat}}$ can be written exactly in the form given by Eq. (4-6a) and we obtain

$$\phi_{sF} = \phi_{d \text{ sat}} + \phi_p \left(1 - \sqrt{\frac{-\phi_{d \text{ sat}}}{\phi_q}} \right) \left(1 + \frac{2C_d}{C_o} \sqrt{\frac{-\phi_{d \text{ sat}}}{\phi_q}} \right). \quad (4-6b)$$

We must solve Eq. (4-6b) to obtain the drain saturation voltage $\phi_{d \text{ sat}}$ in terms of the fixed gate voltage ϕ_G . But this has been done. And the result is simply given by Eq. (4-1d) with the zero signal charge $Q = 0.0$. Substitution of the so-obtained drain saturation voltage $\phi_{d \text{ sat}}$ into the current-voltage relationship Eq. (4-5c) gives the magnitude of the drain saturation current, $I_{d \text{ sat}}$.

Another important property of the transistor is the transconductance defined as the change of drain current at a given drain voltage upon a change in gate voltage. This quantity is negative for p-channel devices because the channel resistance increases as we increase the gate voltage resulting the decrease in the drain voltage. The magnitude of the transconductance can be calculated from (4-5c) to be

$$g_m = \left. \frac{\partial I_D}{\partial \phi_{sF}} \right|_{\phi_d = \text{const}} = G_o \left[\sqrt{\left(\frac{C_d}{C_o} \right)^2 + \left(\frac{\phi_{sF} - \phi_d}{\phi_p} \right)} - \sqrt{\left(\frac{C_d}{C_o} \right)^2 + \left(\frac{\phi_{sF} - \phi_s}{\phi_f} \right)} \right] \quad (4-6c)$$

The transconductance in the linear region can be obtained by expanding the bracketed terms in Eq. (4-6c) above. Conversely, the transconductance in the saturation region can be calculated by inserting $\phi_d = \phi_{d \text{ sat}}$ into Eq. (4-6c). This yields, applying the relation (4-6b), the same expression (4-5f). This shows that the transconductance in the saturation region is exactly equal to the channel conductance in the linear region.

One more aspect of the transistor characterization remains to be studied. This is the response time of the transistor. When the gate voltage ϕ_{SF} changes by an amount $\Delta\phi_{SF}$, the channel width X_{CH} will be modulated because there is also the corresponding change in charge contained within the depletion regions surrounding the channel. This additional charge in the depletion region is equal to the amount of the induced charge ΔQ_G on the gate. The response time of the system can then be defined as that time in which the change in the drain current makes up the change in the total charge on the gate, that is, $t\Delta I_D = \Delta Q_G$. Thus it follows that this response time is given by

$$t = \frac{\Delta Q_G}{\Delta\phi_{SF}} \frac{\Delta\phi_{SF}}{\Delta I_D} = C_G / g_m \quad , \quad (4-7a)$$

where g_m is the transconductance given by Eq. (4-6c) and C_G is the total gate capacitance we must integrate $C_g(\phi_{SF}, Q)$ over the area of the gate. That is,

$$C_G(\phi_{SF}, \phi_d, \phi_s) = Z \int_0^L C_g(\phi_{SF}, Q) dy \quad . \quad (4-7b)$$

The use of the relation (4-5b) and regarding the signal charge Q to be a function of the local channel potential ϕ_m as given by Eq. (4-2a) results in a simple procedure to calculate the total gate capacitance C_G in terms of the gate, source and drain voltages.

$$C_G = \frac{Z^2 \mu_p}{I_d} \int_{\phi_d}^{\phi_s} Q(\phi, \phi_{SF}) C_g(\phi_{SF}, Q) d\phi \quad (4-7c)$$

The instantaneous current on the gate (or the clock load) is simply given by

$$j = C_G \frac{d\phi_{SF}}{dt} \quad (4-7d)$$

We have now come to the stage of the most important discussion in this section. This is about the channel potential at the onset of saturation. The validity of the gradual channel approximation fails in this transit condition. And we have to rely on the exact two dimensional numerical calculation.

Figure 4.2a illustrates the conditions that prevail under the onset of saturation. The values of the salient parameters in this calculation are $N_A = 20,000 \text{ e}/\mu^3$, $N_d = 1,000 \text{ e}/\mu^3$, $X_d = 1\mu$, $X_o = 0.12\mu$, $\phi_s = -20.0$ volt, $\phi_{SF} = -18.0$ volt, and $L = 12\mu$. The drain voltage ϕ_d is computed by Eq. (4-1d) with $Q = 0.0$ (the condition of the drain saturation voltage) and is found to be -32.8 volt. The solid curve in Fig. 4.2b represents the channel potential along the direction of the charge transfer computed by the gradual channel approximation. The validity

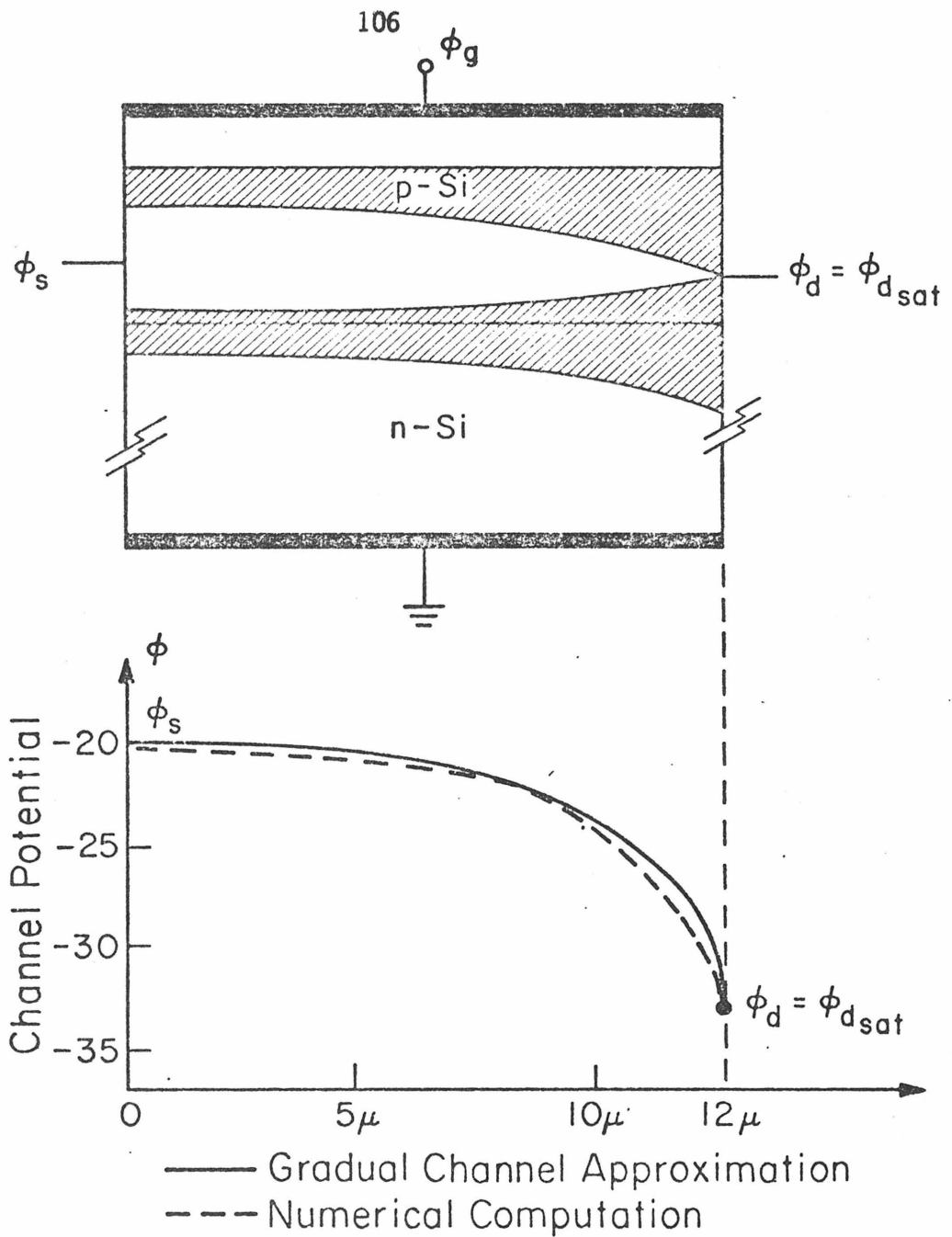


Fig. 4.2a The ideal condition at the onset of saturation is illustrated. $\phi_d = \phi_{d\text{sat}} = -32.8$ volt and $\phi_s = -20$ volt.

Fig. 4.2b The channel potentials computed by the gradual channel approximation and the numerical computation are compared. The gate length L is 12μ . $\phi_{SF} = -13$ volt.

of this approximation is confirmed by the actual two dimensional numerical calculation shown as a dashed curve in Fig. 4.2b.

This calculation is done under the condition of steady state and the channel potential depends strongly upon the charge profile. If there is no mobile charge at the onset of saturation, that is, when the source voltage is raised from $\phi_{d \text{ sat}}$ to the present value of -20 volt very suddenly, there is still some time to go for the system to reach the steady state illustrated in Fig. 4.2a. The channel will be opened from the source to the drain gradually. And the corresponding channel potential changes as illustrated qualitatively in Fig. 4.3. The validity of the gradual channel approximation fails in this transit condition. And we have to rely on the exact two dimensional numerical calculation for the channel potential. Moreover, to obtain the exact transit curves 1, 2, 3 and 4 depicted in Fig. 4.3, we must couple the two dimensional continuity equation to the Poisson's equation. We have not done this. We simply showed the qualitative channel boundary and potential profile in the transit conditions. However the actual channel potential at $t = 0.0$ can be computed by the two dimensional Poisson's equation above. And the curve shown in Fig. 4.3a is the result of the exact numerical calculation. The channel potential seems to decay exponentially, as we go further from the source to drain, to the final value of the drain saturation voltage $\phi_{d \text{ sat}}$. This speculation is verified when the curvature $\partial^2\phi/\partial y^2$ is plotted against the difference $(\phi - \phi_{d \text{ sat}})$ as shown in Fig. 4.3c. Indeed the channel potential

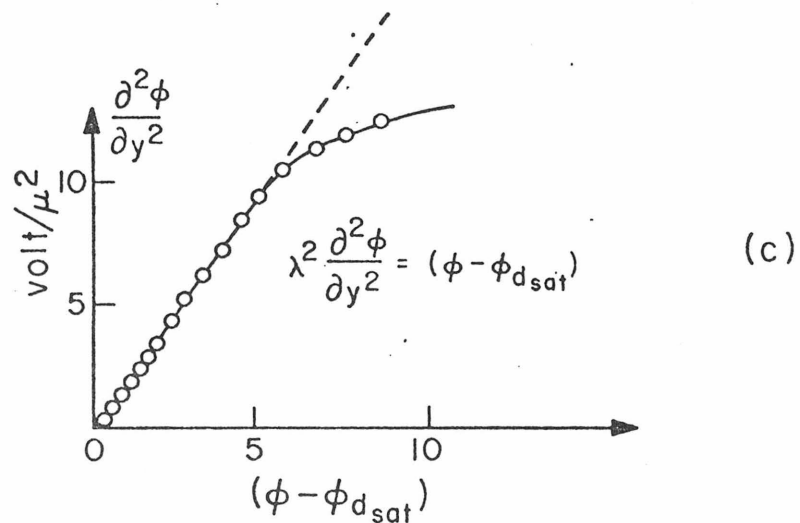
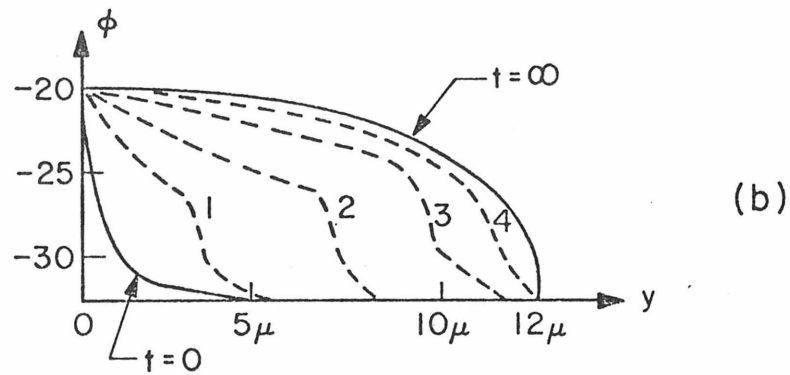
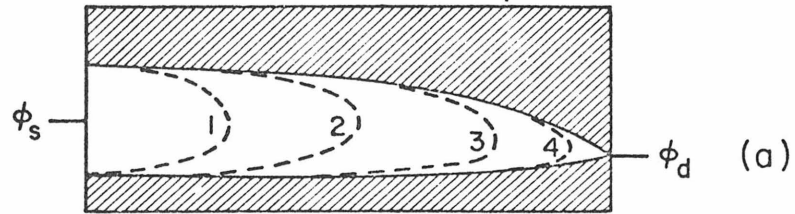


Fig. 4.3a The boundary of the channel at the transition period when the drain voltage changes suddenly from ϕ_s to $\phi_{d_{sat}}$.

Fig. 4.3b The channel potential at transit times. The profiles at $t = 0$ and $t = \infty$ are calculated exactly.

Fig. 4.3c The curvature of the channel potential.

follows the simple relation given by

$$\lambda^2 \frac{\partial^2 \phi_d}{\partial y^2} = (\phi - \phi_{d \text{ sat}}) \quad , \quad (4-8)$$

with $\lambda = 0.67$. The deviation $(\phi - \phi_{d \text{ sat}})$ from the gradual channel approximation is proportional to the curvature of the potential with a fairly good accuracy. This characteristic can also be observed in the more complicated structure of Fig. 4.1b. The physical interpretation of Eq. (4-8a) leads to the simple capacitance model to be discussed in the later section.

This concludes the review of the basic underlying principles of the field effect transistor with the metallurgical p-type channel. With this amount of knowledge, it is now a straightforward procedure to extend the above analysis to the electrostatic problem of two dimensional Buried Channel Charge Coupled Devices.

4.4 Minimum Potential Profile in Buried Channel Charge Coupled Devices

In this section we will describe the general characteristics of the channel potential profile and the resulting fringing field in buried channel charge coupled devices. The detail of the solution of the two dimensional Poisson equation is further studied and the results are compared with the relations implied in one dimensional depletion approximation. In order to clarify the computational procedure, the nature of two dimensional Poisson's equation for the buried channel charge coupled devices is also discussed. The interpretation of the detailed results presented in this section remains to be studied in the next

section.

One of the major factors causing the buried channel device to differ from the surface channel device, can be illustrated by the relationship of the gate oxide capacitance to the depth of the potential well produced by that gate. Given two identical gate electrodes at the same potential, in a surface channel device the gate with the larger oxide capacitance will produce the deeper well at the interface. In a buried channel device, the gate with the smaller oxide capacitance will produce the deeper well in the depleted channel. Hence the aluminum and silicon gate should be used as storage and transfer gates, respectively in buried channel charge coupled devices. In the structure illustrated in Fig. 4.1b, the oxide thickness is 0.12μ under polysilicon electrodes and 0.32μ under the aluminum electrodes.

For two-phase operation the one dimensional analysis shows that the values of 0.0 volt for the source gates and -18.0 volt for the receiving gates should give the optimum minimum potential profile along the direction of the signal charge transport. Two dimensional Poisson's equation corresponding to the structure shown in Fig. (4.1b) is solved numerically for zero signal charge. The result is shown in Fig. 4.4. The minimum fringing fields are found to be 824 volt/cm under the silicon transfer gate and 1796 volt/cm under the aluminum gate. These values are one order of magnitude bigger than the surface CCD fringing fields strength.

Under these physical conditions present, it is of interest to consider how the mobile signal charge profile would affect the overall

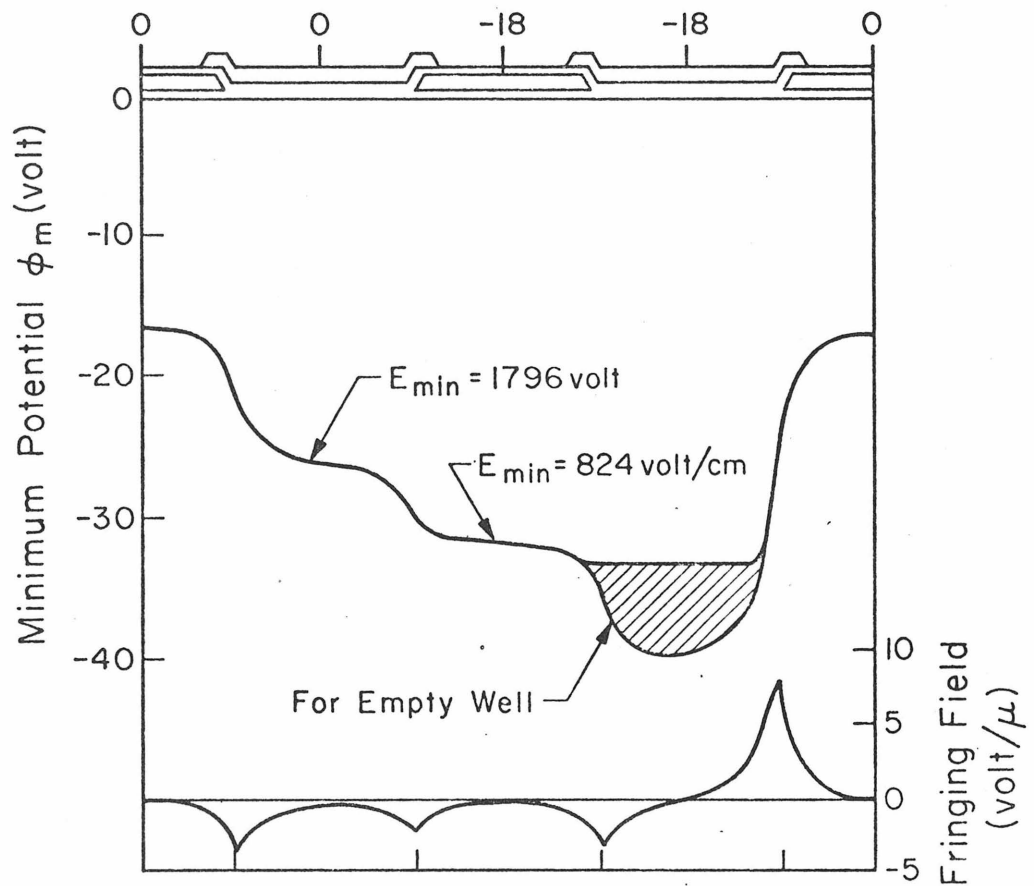


Fig. 4.4 The minimum potential and the potential gradient along the direction of charge transfer. $N_A = 20,000 e/\mu^3$, $N_d = 1000 e/\mu^3$, and $X_d = 1.0 \mu$. The shaded region is the potential lift due to the signal charge in the well.

view of the minimum potential profile. As the signal charge is being transferred into the storage well under the aluminum drain gate, the signal charge should raise the minimum potential from the zero-signal level (-39.9 volts). But as seen in Fig. 4.4, the minimum potential under the aluminum drain gate should not be raised higher than the level (-31.6 volt) of the minimum potential under the silicon transfer gate. This condition limits the maximum signal capacity down to 30% of $Q_d = N_A X_{CH}$, i.e., $6000 e/\mu^2$. If the gate dimension is 100μ by 12μ , then the maximum signal charge that can be processed is 7.2 million electron charges.

However, for three or four phase clocking schemes, the maximum signal charge processing capacity will be quite possibly larger.

In Fig. 4.5, we have plotted the fringing field profiles under the aluminum source gate and silicon transfer gate in an expanding scale.

The above result is the most important one in the two dimensional electrostatic analysis of buried channel CCD's, and needs to be studied in order to obtain the important correlations between the one dimensional and two dimensional analysis. Specifically, we expect the solution of one dimensional depletion approximation to give fairly good agreements with the solution of the two dimensional Poisson's equation in the most of the area except at the interelectrode regions. In Fig. 4.6, we have plotted the following three quantities which represent errors involved in the linear depletion approximation

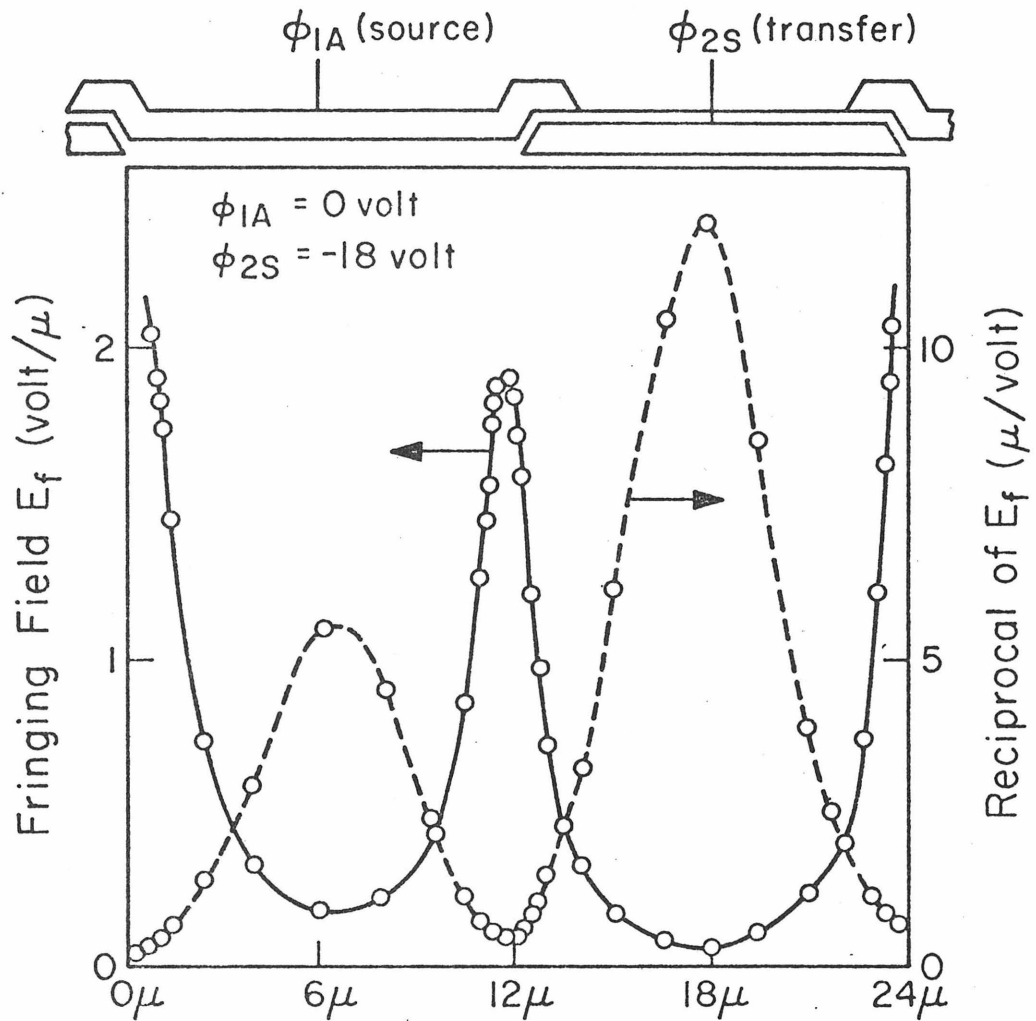


Fig. 4.5 The fringing field profile in an exponential scale under the source aluminum electrode and the silicon transfer electrode.

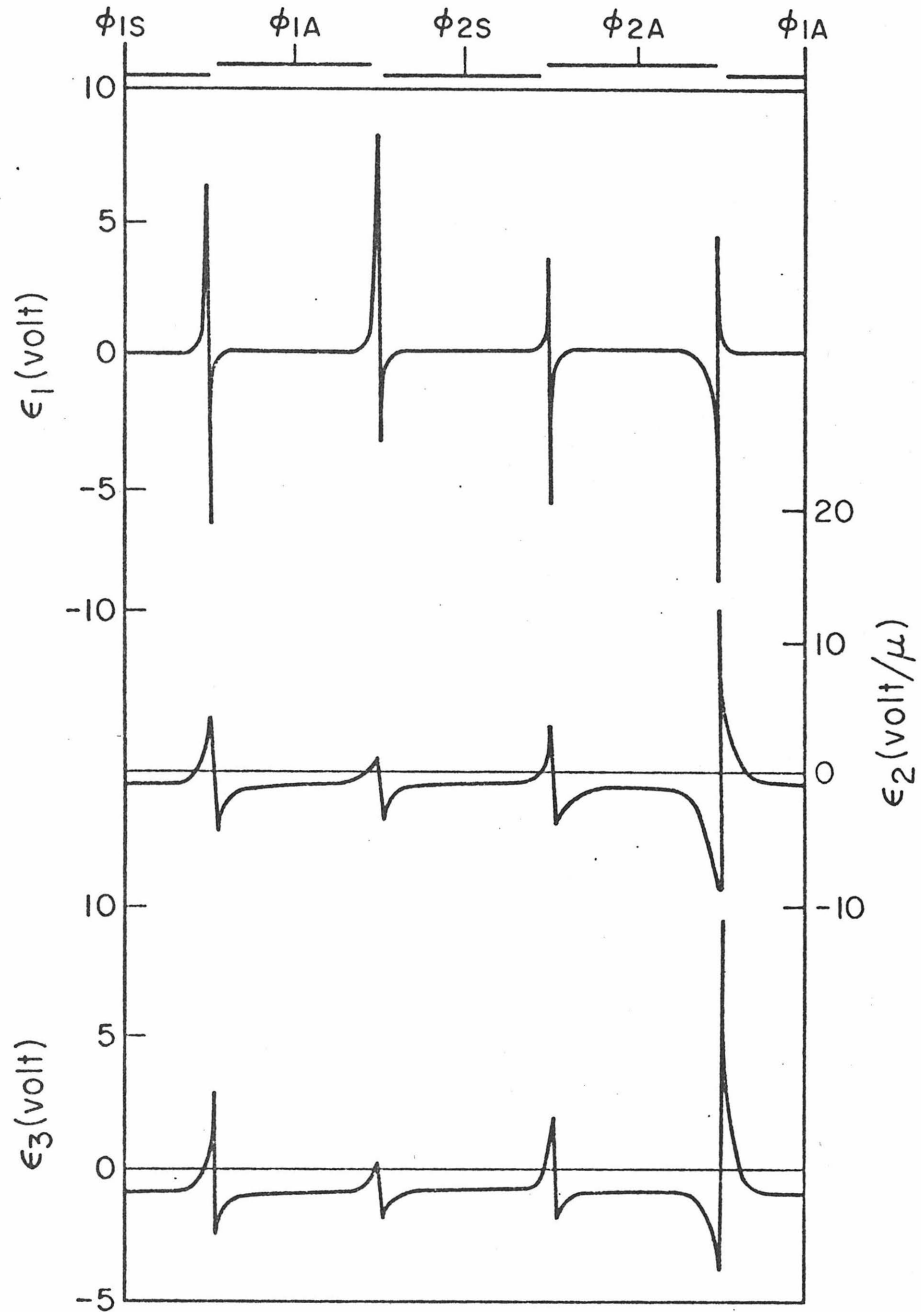


Fig. 4.6 Plots of errors ϵ_1 , ϵ_2 , and ϵ_3 defined by Eqs. 4.9.

$$\epsilon_1 = \phi_{SF} - \phi_s - \frac{\epsilon_{Si} E_s}{C_0} = \int_0^{x_0} \int_0^x \frac{d^2 \phi}{dy^2} dx' dx \quad , \quad (4-9a)$$

$$\epsilon_2 = E_s - \frac{N_A x_1}{Si} = \int_0^{x_1} \frac{\partial^2 \phi}{\partial y^2} dx \quad , \quad (4-9b)$$

$$\epsilon_3 = \phi_m - \phi_s + \frac{\epsilon_{Si} E_s^2}{2N_A} = \int_{\phi_m}^{\phi_s} \frac{\partial^2 \phi}{\partial y^2} d\phi \quad . \quad (4-9c)$$

In one dimensional structure these three quantities ϵ_1 , ϵ_2 and ϵ_3 are theoretically all zero. This error estimate indicates that our results are in good agreement in all but the small interelectrode regions.

To complete our discussion we have plotted in Fig. 4.7 the surface electric field E_s perpendicular to the interface and the depth x_1 of the surface field induced space charge region. Note x_1 denotes the position of the minimum potential from the interface. The surface potential ϕ_s and the minimum potential ϕ_m are compared in Fig. 4.8.

It is very important at this stage to describe the nature of the two dimensional Poisson equation appropriate for the structure of buried channel CCD's. The detailed results presented above can be reproduced with the aid of the discussions given below.

Poisson's equation for two dimensional buried channel charge coupled

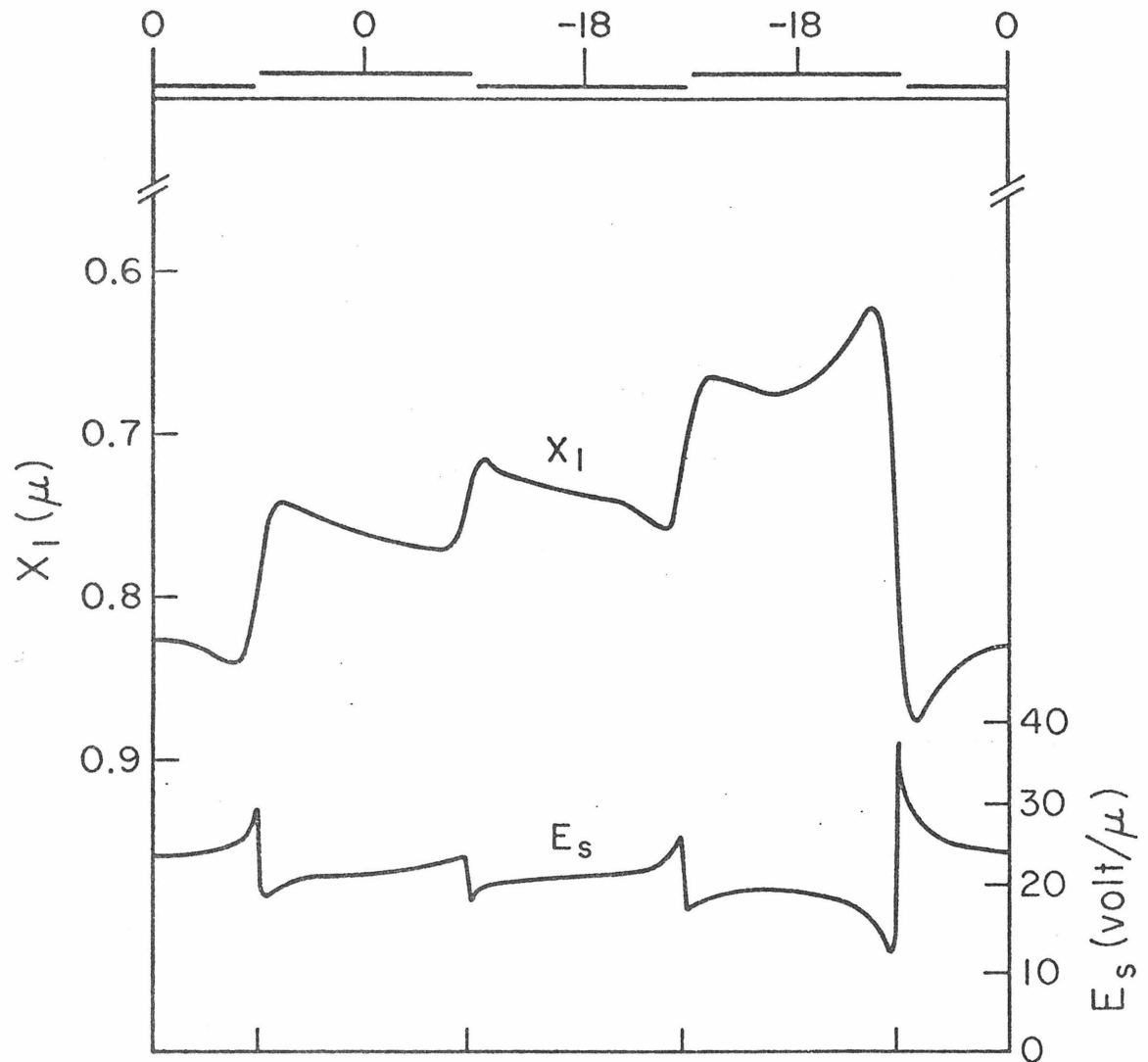


Fig. 4.7 The surface electric field E_s normal to the interface and the depth X_1 of the surface field induced depletion region are plotted along the direction of charge transfer. Note that X_1 is the distance of the minimum potential ϕ_m from the oxide-semiconductor interface.

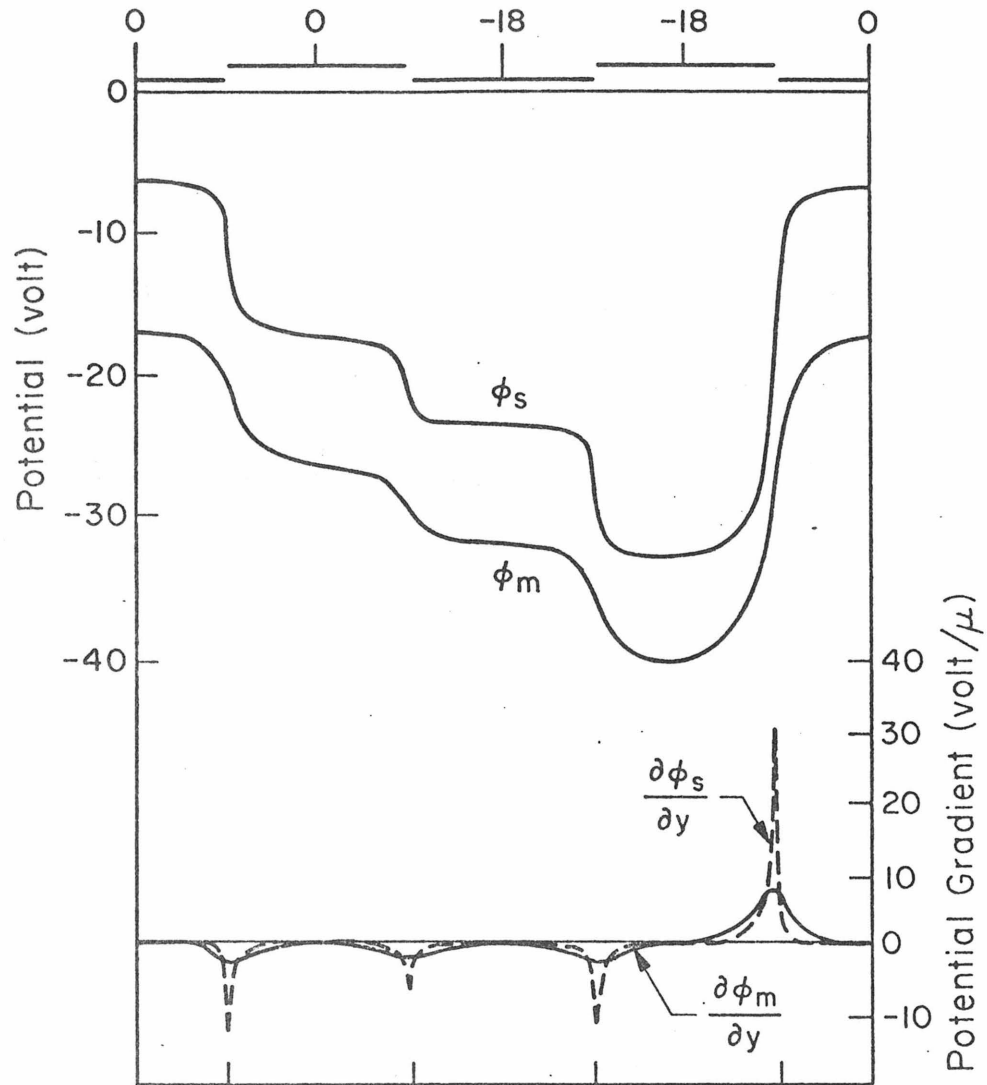


Fig. 4.8 The surface potential ϕ_s , and the minimum potential ϕ_m are compared. The corresponding potential gradients are also shown in the lower figures.

devices has a similar form to that of one dimensional form in which the quasi-fermi level ϕ_n of electrons is approximated to be a constant throughout in the semiconductor whose value is equal to the fermi level ϕ_f deep in the substrate. The presence of signal charge determines the form of the quasi-fermi level ϕ_p of holes in the p-diffusion region. But in the n-type Si-substrates, its value can be approximated by the fermi level ϕ_f . In the operation of buried channel charge coupled devices, the quasi-fermi level ϕ_p of holes in the p-diffusion region can be assumed to be a function of the y-coordinate only, which is defined parallel to the direction of charge transfer. From Boltzmann statistics (which is a good approximation for Fermi-Dirac statistics for energies at least several kT away from quasi-fermi levels), we have the concentration of holes in the form as seen by

$$p = n_i \exp \left[\frac{\phi_p - (\phi + \phi_0)}{kT} \right] \quad , \quad (4-10a)$$

where n_i is the intrinsic electron or hole density and ϕ_0 is determined by the definition of the reference potential deep in the substrate to be

$$\phi_0 = kT \ln \left[\frac{N_d}{2n_i} + \sqrt{1 + \left(\frac{N_d}{2n_i} \right)^2} \right] \quad . \quad (4-10b)$$

Note n_i , ϕ_0 and ϕ_p are all constant along the depth of the semiconductor, that is, along x-axis.

Hence we observe that the condition of no x-coordinate dependence of the quasi-fermi level ϕ_p of holes is equivalent to no signal charge motion along x-coordinate (perpendicular to semiconductor surface)

$$J_x = -D \frac{\partial p}{\partial x} - \mu p \frac{\partial \phi}{\partial x} = 0 \quad (4-10c)$$

This assumption is essential in the description of the dynamic signal charge transfer which will be discussed later in this thesis. The Poisson's equation in the p-diffusion region is given by

$$\frac{d^2 \phi}{dx^2} + \frac{d^2 \phi}{dy^2} = - \frac{[d(x) + p(\phi, \phi_p)]}{\epsilon_{Si}} \quad (4-10d)$$

where ϕ_p is assumed to be a function of y-coordinate only. In the n-type Si substrate, the Poisson's equation is given by

$$\frac{d^2 \phi}{dx^2} + \frac{d^2 \phi}{dy^2} = - \frac{[d(x) - N_d \exp(\phi/kT)]}{\epsilon_{Si}} \quad (4-10e)$$

After solving the Poisson's equation, we obtain the potential $\phi(x,y)$ everywhere. And if we obtain the position $\chi_m(y)$ of the minimum potential along the direction of charge transfer. We can write the mobile signal charge density $p(x,y)$ as

$$p(x,y) = -d(\chi_n) \exp\left(\frac{\phi_q - \phi}{kT}\right) \quad (4-10f)$$

where the quantity ϕ_q is related to the quasi-fermi level of holes in the p-diffusion region by

$$\phi_q = \phi_p - \phi_o - kT \ln \left| \frac{d(x_m)}{n_i} \right| \quad (4-10g)$$

When the doping $d(x)$ is considered uniform and given by $(-N_A)$ in the p-diffusion layer, Eq. (4-10g) becomes

$$\phi_q = \phi_p - kT \ln \left(\frac{N_A N_d}{n_i^2} \right) \quad (4-10h)$$

And the mobile signal charge is written as

$$p(x,y) = N_A \exp \left(\frac{\phi_q - \phi}{kT} \right) \quad (4-10i)$$

ϕ_q is the minimum potential for this case along the direction of the signal charge transfer. $\phi_q = \phi_m(y)$.

The condition of zero signal charge everywhere corresponds to the case in which the quasi-fermi level ϕ_p for holes is such that the quantity $(\phi_q - \phi)/kT$ in Eq. (4-10g) is a very large negative value everywhere. In this case, in p-diffusion layer, we can write the Poisson's equation as

$$\frac{d^2 \phi}{dx^2} + \frac{d^2 \phi}{dy^2} = - \frac{d(x)}{\epsilon_{Si}} \quad (4-10j)$$

We assume that the doping profile $d(x)$ does not vary along the

direction of charge transfer (y-axis).

4.5 Capacitor Network Model for Buried Channel Charge Coupled Devices

In the previous sections we have shown that the exact numerical calculation of the two dimension Poisson's equation results in the channel potential which differs from the one dimensional gradual channel approximation by an amount which is proportional to the second spatial derivative of the exact channel potential (Ref. Eq. (4-8)). Numerically we have found the decay length λ to be 0.67μ for the particular values of the physical parameters. We now give a simple physical system which may explain this result better. The following is the derivation of the simple capacitance network model for buried channel CCD's.

For two dimensional BCCD structure, we consider the differential capacitor network shown in Fig. 4.9b, which is obtained by inter-connecting the one dimensional series capacitance structure shown in Fig. 4.9a by another capacitance C . Note that C_0 , C_1 and C_2 are in capacitance per unit area while C has a dimension of capacitance. And physically we expect the value of the capacitance C to be of the order of $\epsilon_{Si} \lambda_d$. From Fig. 4.9b the differential signal charge per unit length is given by

$$\partial Q_j \cdot dy = (\partial \phi_{m_j} - \partial \phi_{S_j}) C_1 dy + \partial \phi_{m_j} C_2 dy + (\partial \phi_{m_j} - \partial \phi_{m_{j-1}}) C/dy + (\partial \phi_{m_j} - \partial \phi_{m_{j+1}}) C/dy \quad (4-11a)$$

Note ∂Q_j has a dimension of charge per unit area. The differential, $\partial \phi_m$, of the minimum potential is related to the differential gate

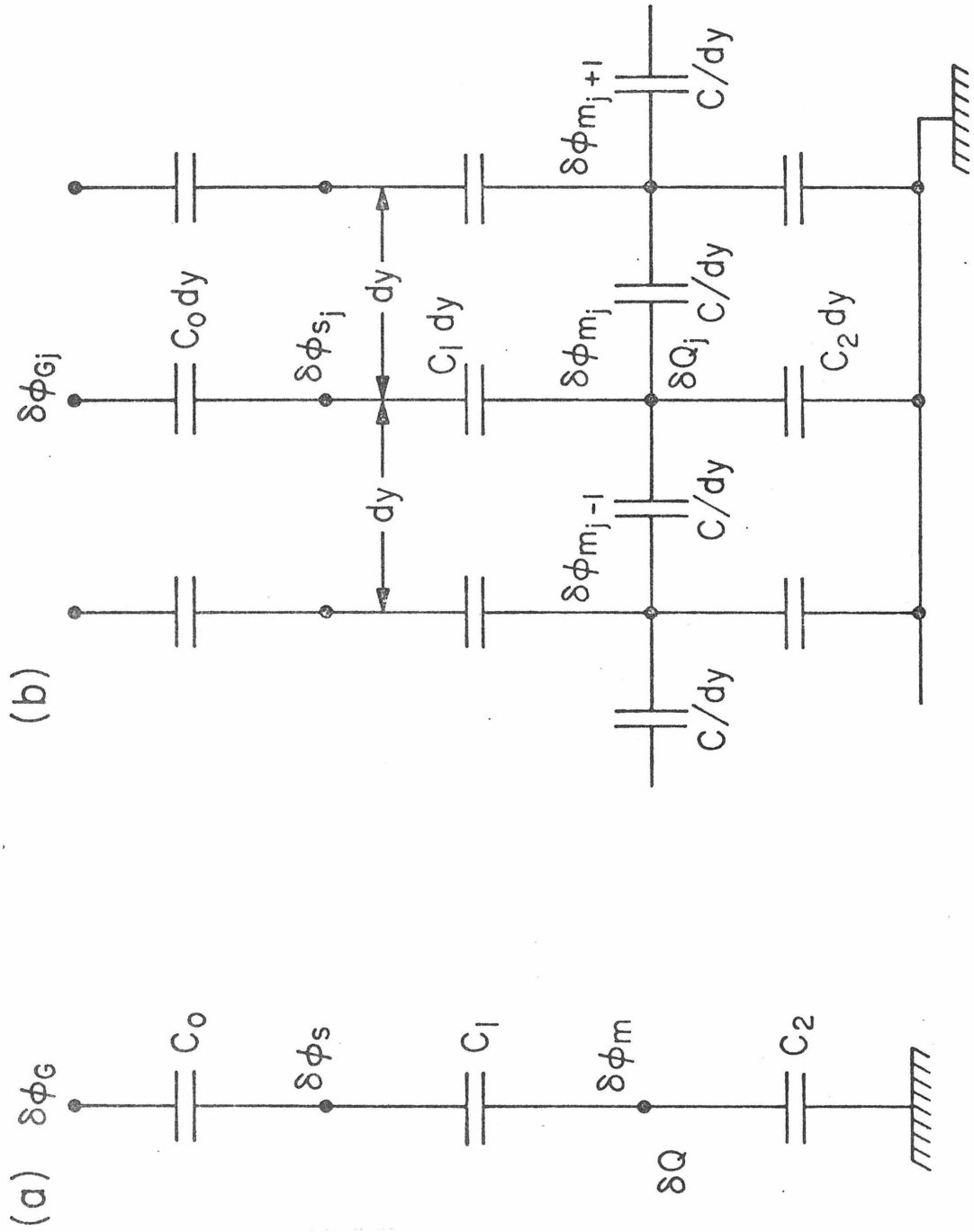


Fig. 4.9 The capacitance network for one dimensional MOS structure (a) and two dimensional structure (b)

voltage $\partial\phi_G$ by

$$\left(\partial\phi_{S_j} - \partial\phi_{G_j}\right) C_0 dy + \left(\partial\phi_{S_j} - \partial\phi_{m_j}\right) C_1 dy = 0 \quad (4-11b)$$

Hence the differential surface potential is given by

$$\partial\phi_{S_j} = \frac{C_0 \partial\phi_{G_j} + C_1 \partial\phi_{m_j}}{C_0 + C_1} \quad (4-11c)$$

Substitution of Eq. (4-11c) into Eq. (4-11a) results in a differential equation for the differential minimum potential $\partial\phi_m$

$$C \frac{d^2}{dy^2} [\partial\phi_m] = \frac{\partial\phi_m - \partial\phi_{m_0}}{\frac{\partial\phi_m}{\partial Q}_0} \quad (4-11d)$$

where $(\partial\phi_m/\partial Q)_0$ and $\partial\phi_{m_0}$ are the solutions when we take one dimensional case depicted in Fig. 4.9a. Finally by adding constants, we obtain

$$C \frac{d^2\phi_m}{dy^2} = \frac{\phi_m - \phi_{m_0}}{(\partial\phi_m/\partial Q)_0} \quad (4-12)$$

This simple equation implies that the minimum potential profile ϕ_m is linearly dependent upon its second derivative wherever $\partial\phi_{m_0}$ and $(\partial\phi_m/\partial Q)_0$ are constant. In two dimensional BCCD structure, these two quantities are indeed constant except at the interelectrode regions where the effective oxide thickness and gate voltage are changing abruptly. But these interelectrode regions are extremely narrow and their field effect on the overall minimum potential profile is quite

negligible. Hence we can approximate ϕ_{m_0} and $(\partial\phi_m/\partial Q)_0$ by step functions whose values are to be obtained by solving the linear MOS capacitance by standard depletion approximation.

The linkage capacitance C is an adjustable parameter in this model which depends only on the geometrical device parameters and its value must be computed from the solution of two dimensional Poisson's equation to give the best fit in Eq. (4-12). The solution of Eq. (4-12) is compared with the exact numerical solution in Fig. 4.10 for no signal charge present in the channel. In Fig. 4.11 we present the phase diagram of the minimum potential which strongly confirms the validity of this linkage model for BCCD structure. Notice that the second derivative, $\partial^2\phi_m/\partial y^2$, is indeed a piecewise linear function of the minimum potential ϕ_m as implied by Eq. (4-12)

However as seen in Fig. (4-12) the surface potential ϕ_s is not quite piecewise linear. This linear dependence of the potential upon its derivative is a valid assumption only for the minimum potential.

This capacitance model is successfully applied in actual dynamic charge transfer calculation in buried channel CCD's.

In the actual charge transfer description, the minimum fringing field is the most important parameter to be considered. In Fig. 4.13, we show how the values of the linkage capacitance C influence the estimated minimum potential calculated by Eq. (4-12).

When the signal charge is present in the channel and given as a function of y -coordinate, we can still compute the minimum potential ϕ_{m_0} and its signal-charge derivative $(\partial\phi_m/\partial Q)_0$ by the linear depletion

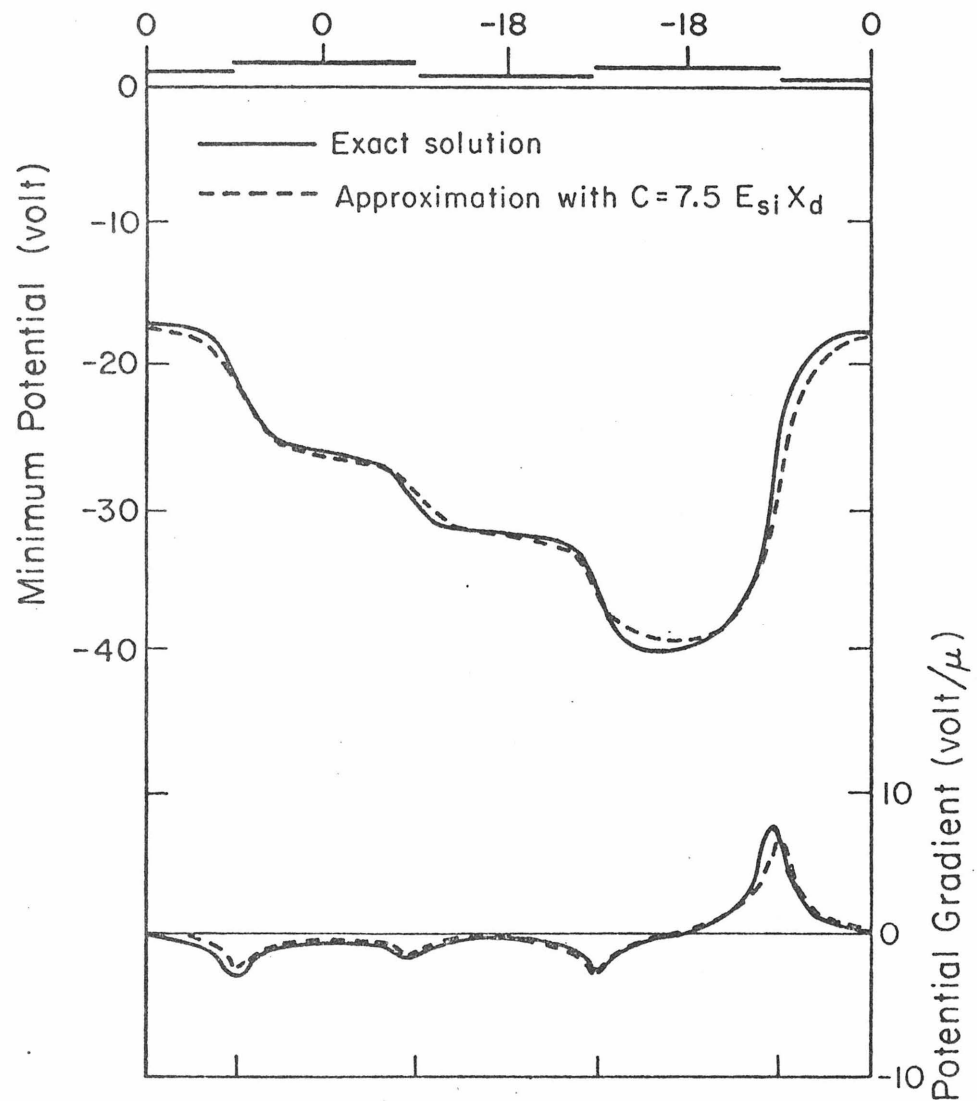


Fig. 4.10 The potential profile (dashed curve) obtained by the capacitance model (Eq. 4-6) is compared with the numerical solution. The value of the linkage capacitance C that gives the best fit is found to be $7.5 \epsilon_{si} X_d$.

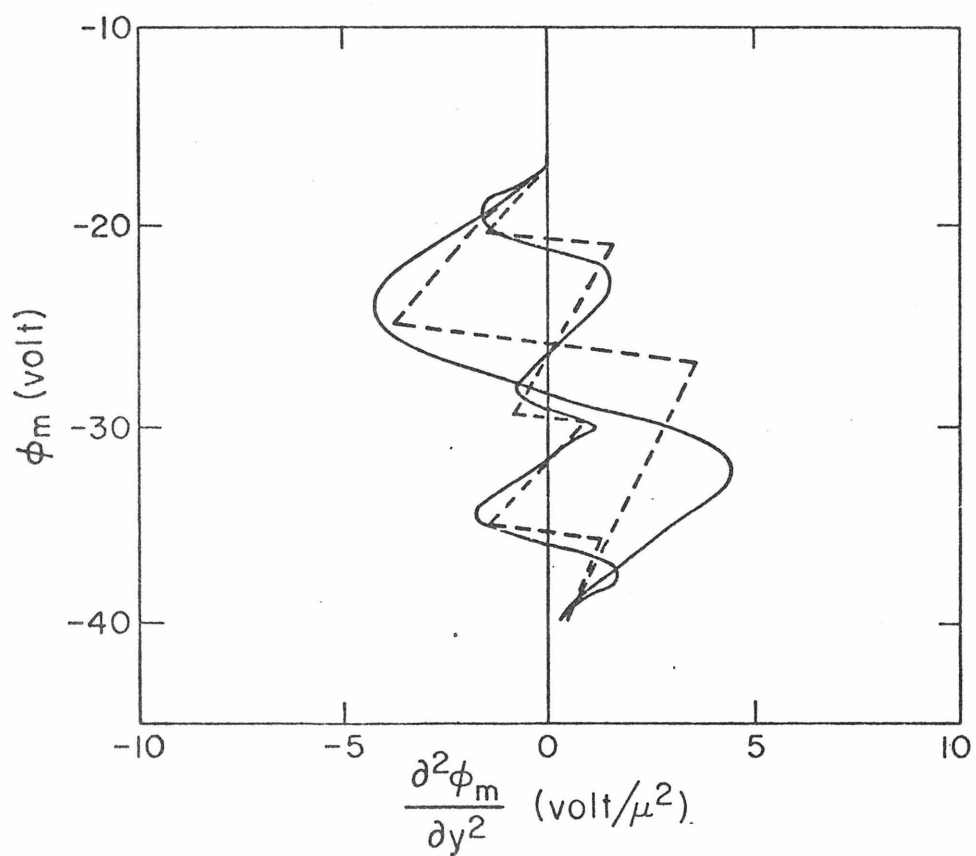


Fig. 4.11 The minimum potential ϕ_m plotted against the second derivative $\partial^2 \phi_m / \partial y^2$. Note that the second derivative is indeed a piecewise linear function of the minimum potential ϕ_m .

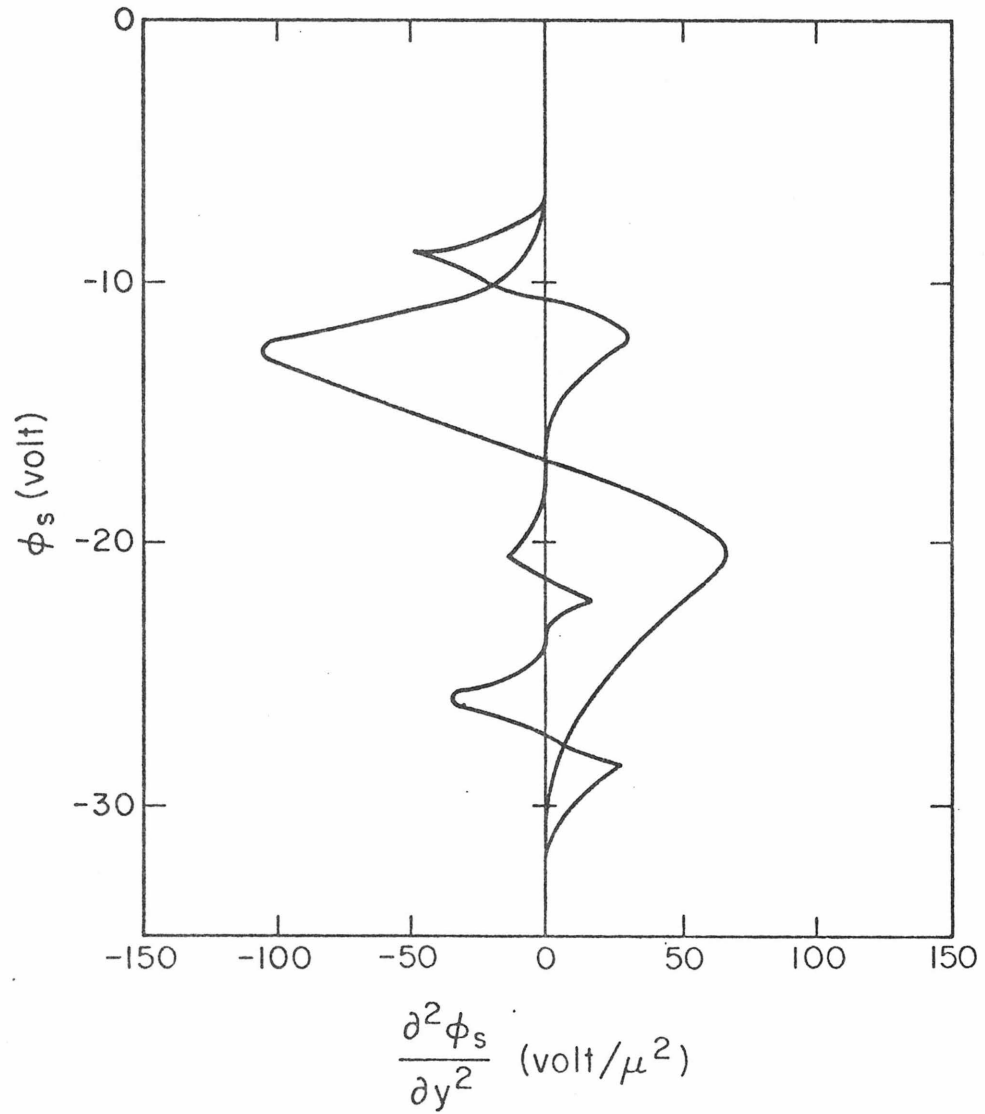


Fig.4.12 The surface potential plotted against its second derivative. The curve is not quite as linear as it was for the minimum potential in Fig.4.11.

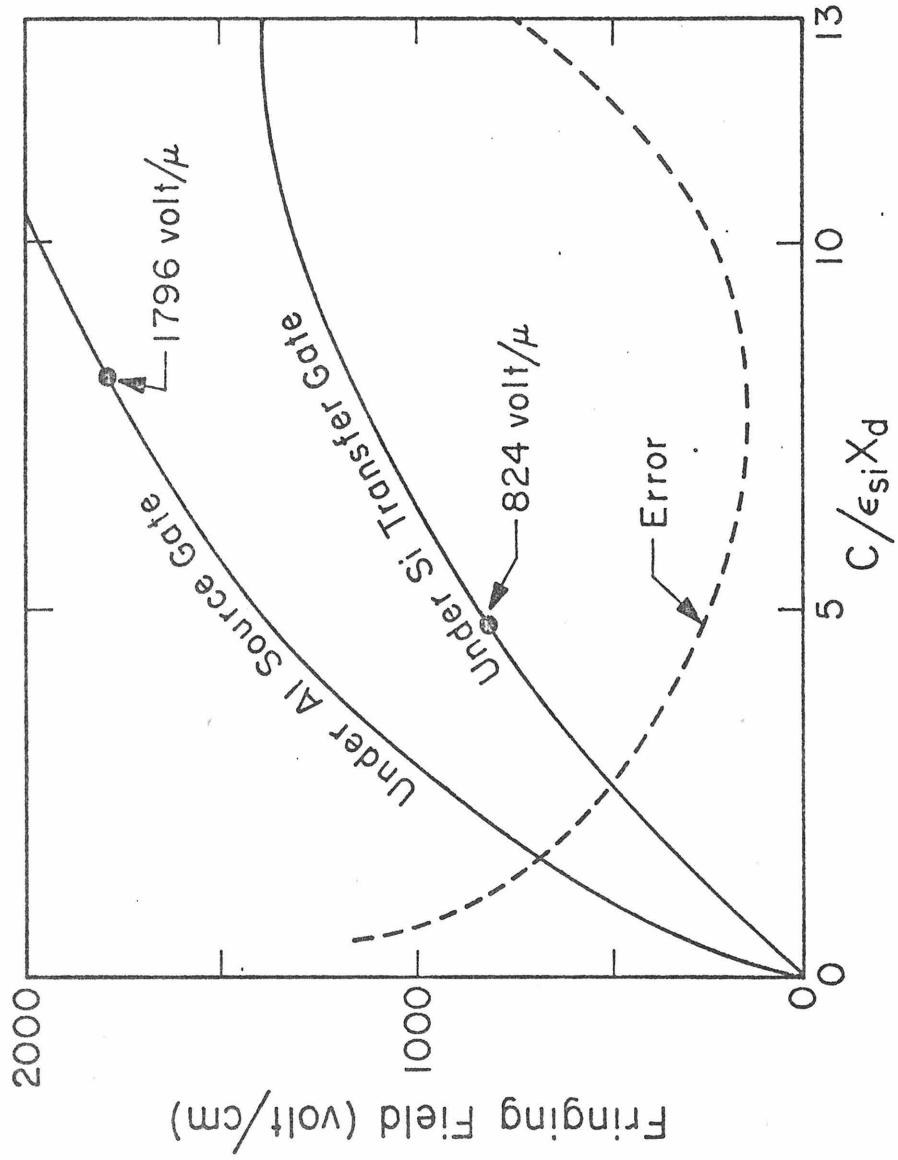


Fig. 4.13 The estimated minimum potential gradients under the Al source and the Si transfer gates (Eq.4.12) computed for different values of C .

approximation. Then the use of Eq. (4-12) results in Fig. 4.14 which shows the actual minimum potential profile in the two dimensional BCCCD with signal charge present, whereby we use the same linkage capacitance value C obtained previously.

When the gradual channel approximation is used, the minimum potential profile is not as smooth as the one solved by the linkage capacitance model. Physically we expect the electrostatic potential to change smoothly as seen in Fig. 4.14. Rewriting Eq. (4-12) as

$$\phi_m(Q) = \phi_{m_0}(Q) + C \left(\frac{\partial \phi_m}{\partial Q} \right)_0 \frac{d^2 \phi_m}{dy^2}, \quad (4-13)$$

we observe that the standard gradual channel approximation is equivalent to assuming $C = 0.0$. Indeed, the second term in RHS of Eq. (4-13) gives a very small correction to the actual channel potential. Whenever there is appreciable signal charge present in the channel, the potential is more or less given by the first term of RHS with a good accuracy. However, at the final stage of the charge transfer, there is very little residual charge in the channel and the charge decay will be influenced strongly by the fringing field. This fringing field actually originates from the second term of Eq. (4-13) and it is important to adjust the value of the capacitance C from the actual numerical data of the potential profile with no signal present.

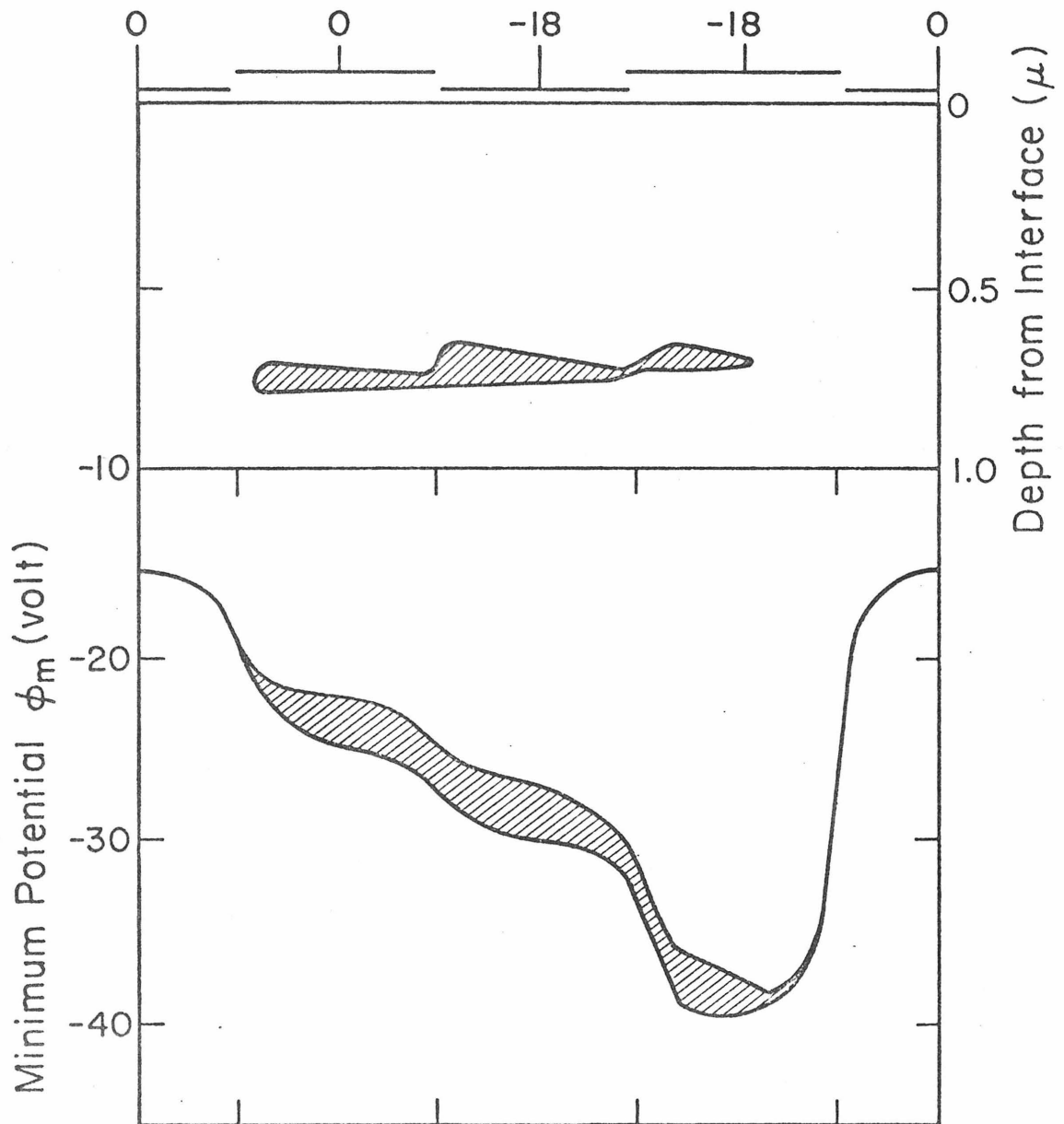


Fig. 4.14 The physical location of the charge packet in the p-layer is shown in the upper figure. The lower figure is the minimum potential with signal charge present.

4.6 Dynamic Charge Transfer Model

The transport dynamics in the p-diffusion channel in BCCD are described by the two dimensional continuity equation.

$$\frac{\partial P}{\partial t} = - \frac{\partial J_x}{\partial x} - \frac{\partial J_y}{\partial y} \quad , \quad (4-14a)$$

where p is the signal charge concentration per unit volume. Integrating over the p-diffusion depth and assuming no signal charge leakage at the interface and p-n junction boundaries, that is, $J_x = 0$ at $x = 0$ and $x = X_d$, we obtain

$$\frac{\partial Q}{\partial t} = - \frac{\partial}{\partial y} \left[\int_0^{X_d} J_y dx \right] \quad , \quad (4-14b)$$

where we note

$$\int_0^{X_d} J_y dx = -D \frac{\partial Q}{\partial y} - \mu \int_0^{X_d} P \frac{\partial \phi}{\partial y} dx \quad . \quad (4-14c)$$

Also we note from Eq. (4-10a)

$$\frac{\partial \phi}{\partial y} = \frac{\partial \phi_p}{\partial y} - \frac{kT}{p} \frac{dP}{dy} \quad . \quad (4-14d)$$

We have assumed the quasi fermi level of holes ϕ_p is independent of the x-axis. Hence the first term of RHS of Eq. (4-14d) is independent of the X-axis. We also assume that whenever there is appreciable hole density, the density along the transverse direction with respect to the

signal charge transfer will smooth out and be uniform. If we assume this, the potential gradient $\partial\phi/\partial y$ becomes a constant value along the x-axis in the region where the signal charge is appreciable.

Therefore we can take the potential gradient $\partial\phi/\partial y$ outside of the integral of Eq. (4-14c). And finally the continuity equation describing the charge transfer dynamics becomes

$$\frac{\partial Q}{\partial t} = D \frac{\partial^2 Q}{\partial y^2} + \mu \frac{\partial}{\partial y} \left[Q \frac{\partial \phi_m}{\partial y} \right] \quad (4-15)$$

Intuitively this result might have been expected but what was not clear is what physical assumptions lead to this result. First we assumed the quasi-fermi level ϕ_p does not depend on x-coordinate in the p-diffusion layer. This assumption immediately gives the current density along the x-axis to be zero. $J_x = -\mu p \frac{\partial \phi_p}{\partial x} = 0.0$. But this condition was not enough to derive Eq. (4-15). We must speculate that the mobile signal charge p also does not have the x-coordinate dependence wherever there is appreciable signal charge. That is, the mobile signal charge density is not graded along the transverse direction with respect to the signal charge transfer.

We have now established the complete dynamic charge transfer model compatible to actual numerical calculations. The simultaneous computation of the signal charge $Q(y)$ and the channel potential $\phi_m(y)$ from the two final equations (4-13) and (4-15) gives the actual time dependent solutions of $Q(y)$ and $\phi_m(y)$. The initial condition is the signal

charge profile $Q(y)$ at $t = 0.0$. Using Eq. (4-13) alone, we compute the channel potential $\phi_m(y)$ at $t = 0.0$. Before specifying the initial charge profile $Q(y)$, the constant C must be adjusted from the actual two dimensional calculation of the Poisson's equation relevant to the dynamic system.

4.7 Conclusion

Choosing adequate values for the device parameters two dimensional Poisson's equation was solved numerically. The resulting minimum potential and its fringing field profiles were presented and compared with the linkage capacitance model developed in the content. The continuity equation for the charge transfer in BCCD was discussed. The fundamentals of the computational procedure for the charge transfer dynamics of BCCD have been established herein.

FREE CHARGE TRANSFER IN BURIED CHANNEL CHARGE COUPLED DEVICES

1.1 Introduction

Previous theoretical work on the operation of charge transfer devices has focused upon surface charge coupled devices and integrated circuit versions of the bucket brigade shift registers. Another type of charge transfer device, namely buried channel charge coupled device, is known to have several advantages over the former two devices. However, up to the present, only a static two dimensional model of buried channel charge coupled devices has been considered. The static model has not been incorporated in dynamic charge transfer description; and, consequently, our understanding of the device operation has been quite qualitative.

In this chapter we present the results of a detailed numerical simulation of the charge transfer process in a realistic model of a high density buried channel CCD. The general set of partial differential equations describing charge transfer and the electrostatic potential has been reduced to a set of two partial differential equations involving a single spatial dimension and the time. To accomplish this we have used a simple capacitance network model to reduce the appropriate two dimensional Poisson's equation into a second order differential equation in a single spatial dimension. The resulting equation relates the signal charge and the minimum channel potential under all the relevant electrodes and interelectrode regions. A diffusion

equation describing the charge transfer is coupled to this equation. The resulting coupled differential equations were solved and the results are presented in this presentation.

In Section 5.2 the general set of partial differential equations describing charge transfer and electrostatic potential is presented. The equations are further simplified to obtain approximate but valid analytic solutions in the subsequent sections. It is shown that the charge transfer process in buried channel CCDs divides into three distinct stages. In the first stage, the charge is confined under the source storage gate and spreads itself according to the rapidly changing clock voltages. This process is shown to take less than a nanosecond in Section 5.3. During the second stage discussed in Section 5.4, the charge transfer occurs in a manner analogous to the operation of a buried channel IGFET (see Section 4.3). The storage electrodes act as source and drain, and the transfer electrode acts as the control gate. This process is shown to take a few nanoseconds. In the final stage described in Section 5.5, the charge transfer is characterized by transfer induced by the relatively large fringing fields. It is shown in Section 5.6 that the residual charge decays exponentially with a final characteristic time constant of the order of a nanosecond. This process is shown to require a time of the order of ten nanoseconds.

The entire charge transfer characteristics can be summarized in the two illustrations shown in Fig. 5.1 and 5.2: in Fig. 5.1a the minimum potential, charge profile and current density at $t=0.221$ nanosecond are illustrated. At $t = 0$, the transfer and drain gate voltages

start dropping to the final value (-10 volt) from the initial value (10 volt). The plot is shown at the gate voltages of -8 volt. The barrier and source gate voltages are set to be 10 volt throughout the transfer process. Charge is normalized by 935 electron charges/ μ^2 . Current density is normalized by 23.4 electron charges/ μ -nanosec. The length L of one unit cell of the device is 48μ consisting of two polysilicon gates and two aluminum gates. Fig. 5.1b depicts the charge transfer at $t = 0.443$ nanosecond. Note the current density under the transfer gate is almost constant. The charge transfer in this stage can be described quite accurately by buried channel IGFET. Fig. 5.1c depicts the charge transfer at $t = 1.05$. Note the slope of the current density indicates that the net charge under the transfer gate is decreasing.

In the top of Fig. 2, the net charging, charging and discharging of the transfer gate are shown by the curves (a), (b) and (c). Current density is normalized by $Q_{\text{total}}D/L^2 = 23.4$ electron charges/ μ -nanosec. Time is normalized by $t = (0.001)L^2/D = 1.92$ nanoseconds with $L = 48$ and $D = 12$ cm^2/sec . In the lower figure, the charge is shown as a percentage of the total signal charge of 45,000 electron charges/ μ . The lines (a), (b), and (c) represent the total residual charge under the source and transfer gates, the charge under the source gate only, and the charge under the transfer gate respectively. Note that the curves eventually become straight, implying the exponential decay characteristics of the powerful field-aided transfer. The final slope (hence, the characteristic time constant) is 0.765 nanosecond for, lines (a) and (c), and 0.165 nanosecond for line (b).

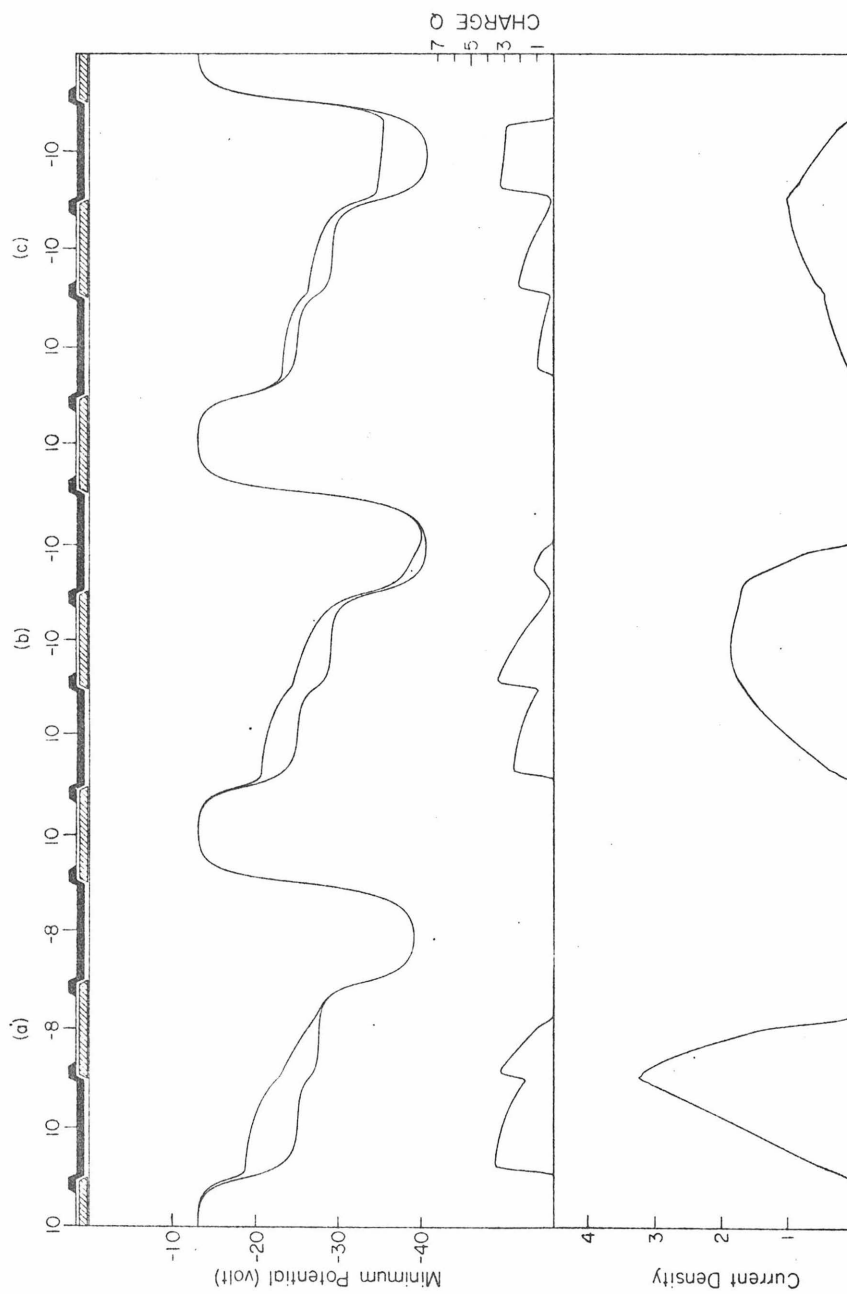


Fig. 5.1 The three stages (a), (b), and (c) of the charge transfer in buried channel CCDs are illustrated by the minimum potential, charge and current density plots. Charge and current density are normalized.

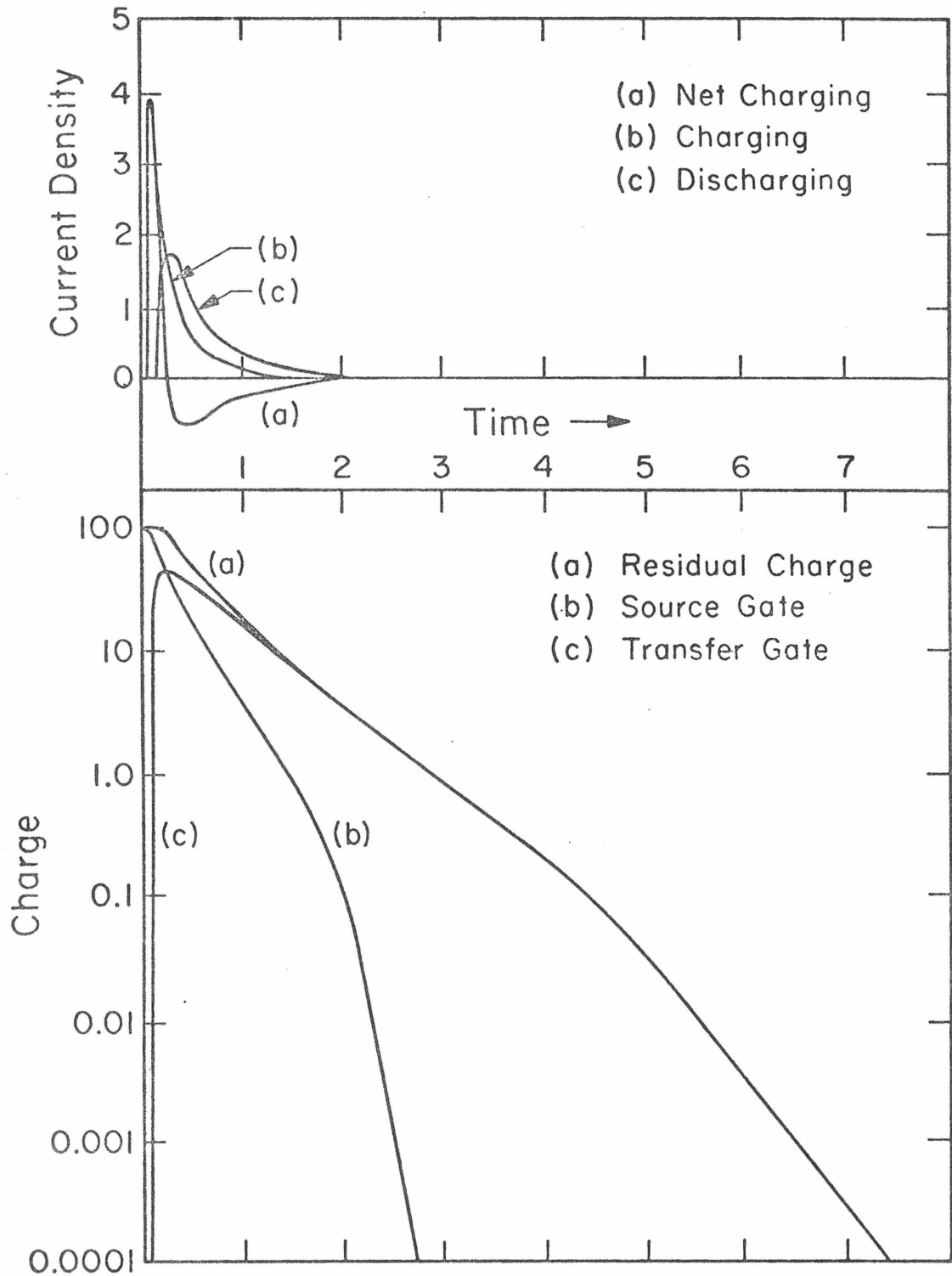


Fig. 5.2 The charge and the current density plotted against the transfer time normalized by $(0.001)L^2/D = 1.92$ nsec.

5.2 Transport Equations

Due to the two dimensional nature of the buried channel CCD structure, the storage and transfer of charge along the buried channel should be described by the two dimensional continuity equation together with the two dimensional Poisson's equation. While this rigorous approach is conceptually possible, the cost of such analysis leads us to seek some valid approximation to simplify the solution. To accomplish this, in Chapter 4 we have developed a set of two partial differential equations involving a single spatial dimension and the time. According to this model, the storage and transfer of charge along the buried channel is described by the continuity equation

$$\frac{\partial q}{\partial t} = - \frac{\partial J}{\partial x} \quad , \quad (5-1a)$$

where the diffusion equation is given by

$$J = -D \frac{\partial q}{\partial x} - \mu q \frac{\partial \phi_m}{\partial x} \quad , \quad (5-1b)$$

q is the sheet charge density of the free mobile carriers in the buried channel, J is the sheet current density and ϕ_m is the minimum channel potential. D and μ are the carrier diffusion constant ($12 \text{ cm}^2/\text{sec}$) and mobility ($480 \text{ cm}^2/\text{volt sec}$) in silicon.

The minimum channel potential gradient, $\partial \phi_m / \partial x$, is due to the variable channel charge density and the two dimensional nature of the buried channel CCD structure. According to the simple capacitance model

developed in Chapter 4 the minimum channel potential profile can be approximated by solving the second order differential equation in a single spatial dimension

$$\phi_m = V_m(q, x) + C \left(\frac{\partial V_m}{\partial q} \right) \frac{\partial^2 \phi_m}{\partial x^2} \quad , \quad (5-2)$$

where $V_m(q, x)$ is the solution of the one-dimensional Poisson's equation with the parameters of the solutions chosen to correspond to the one dimensional cut through the structure. In the standard gradual channel approximation, ϕ_m is determined uniquely by the local sheet charge density q and is given by V_m alone. (That is, in Eq. (5-2) above $C = 0.0$). In this case, we note that, at the interelectrode regions where the charge density q changes abruptly, the electrostatic potential ϕ_m also changes abruptly. However, physically the electrostatic potential must be continuous even though the charge density is discontinuous. The electric field is the one that becomes discontinuous in this case. Hence, the gradual channel approximation is valid only under the electrode plates where the charge density is (spatially) changing gradually. In Chapter 4 we have developed this differential equation (5-2) to obtain an accurate minimum channel potential profile under all the relevant electrodes and interelectrode regions.

The capacitance C was found to be of the order of $X_d \epsilon_{Si}$ where X_d is the depth of the p-diffusion buried layer and ϵ_{Si} is the silicon dielectric constant. In the calculations presented below we have considered p-channel device with dimensions consistent with typical

layout tolerance of present silicon gate technology: Oxide thickness is 0.12μ under the silicon gates and 0.32μ under the aluminum gates. X_d is taken to be 1.00μ with the diffusion layer doping N_A 25000 donors/ μ^3 , the substrate doping N_d of 1000 donors/ μ^3 , and $C = 7.5 X_d \epsilon_{Si}$.

5.3 Self-Induced Drift Effect in the First Stage

In this section we study the charge transfer process in the first stage. Specifically we will first show that the charge profile under the source gate is of elliptic shape. This result is derived from the fact that the current density under the source gate is a linear function in spatial coordinate. The spatial integration of this charge profile is the total charge $Q(t)$ under the source gate, and the analytic expression for the total charge $Q(t)$ will be derived. This expression implies the hyperbolic charge decay characteristics. And the further considerations lead to the fact that this hyperbolic charge decay characteristic is not the consequence of the constant current assumption but rather of much a general nature. It is concluded that the lumped circuit model gives excellent agreement with numerical results even though the current density at the beginning of discharge is not really uniform in the spatial coordinate.

We now begin the analysis, returning to the situation depicted in the Fig. 5.1a in which the charge profile under the source gate is under consideration.

As the gate voltages on the transfer gate and drain gate start dropping from +10 volt to -8 volt, the charge under the source gate spreads itself according to the rapidly changing channel potential. The

response time is of the order of silicon relaxation time constant $t_{\text{relax}} = \epsilon_{\text{Si}} / \mu N_A = 0.054$ picosecond which is much smaller than values of interest. The charge takes about 0.2 nanoseconds propagating under the transfer gate to reach its end. Figure 5.1a illustrates the details of the charge transfer at this stage. Note that the gradient of the current density indicates the charge under the transfer gate is still increasing. The linear dependence of the gradient upon the spatial coordinate implies that the time rate of change in the charge density ($\partial q / \partial t$) is the same everywhere under the source gate. In this case, the current density $J(t, x)$ can be approximated by a linear function in spatial coordinate and is given by

$$J(t, x) = \left(\frac{x}{\ell} \right) J(t, \ell) \quad , \quad (5-3a)$$

where ℓ is the length of the aluminum source gate (12μ). Since at the beginning of discharge the charge density under the source gate is very high, the field drift is predominantly due to the self-induced field effect. Hence, neglecting also the thermal diffusion effect we obtain

$$J \approx -q \frac{\partial \phi_m}{\partial x} \approx -\frac{\mu}{C_0} q \frac{\partial q}{\partial x} \quad , \quad (5-3b)$$

where C_0 is the effective oxide capacitance. Solving Eqs. (5-3) we obtain

$$q(t, x) = \sqrt{q^2(t, 0) - x^2 \left(\frac{C_0}{\mu \ell} \right) J(t, \ell)} \quad . \quad (5-4)$$

That is, the charge profile is of elliptic shape. We indeed observe this shape both in the charge and potential profiles under the source gate in Fig. 5.1a

To obtain the total charge $Q(t)$ under the source gate as an unique function of time, we need one more condition. In general treatment of charge transfer in surface CCD, this condition has been imposed on the charge density $q(t, \ell)$ at the end of the source gate and set to be zero. This condition is based on the fact that the fringing field at the interelectrode is so large that we can assume a perfect sink at the end of the transfer gate. However, as we observe in Fig. 5.1a, the charge density at the interelectrode region is relatively small but does not diminish to zero. Inspecting Fig. 5.1a and 5.1b, we note that, at the end of the source gate, the charge density decreases to about one-half of the peak charge density $q(t, 0)$. Assuming $q(t, \ell) = q(t, 0)/2$ for the time of interest, then by integrating Eq. (5-3b) for the current density assumed in the form given by Eq. (5-3a), we obtain

$$J(t, \ell) = \frac{3\mu}{4\ell C_0} q^2(t, 0) \quad , \quad (5-5a)$$

$$q(t, x) = q(t, 0) \sqrt{1 - \frac{3}{4} \left(\frac{x}{\ell}\right)^2} \quad , \quad (5-5b)$$

and

$$Q(t) = \int_0^{\ell} q(t, x) dx \approx \frac{3\ell}{4} q(t, 0) \quad . \quad (5-5c)$$

Solving the continuity equation,

$$\frac{dQ}{dt} = -J(t, \ell) \quad (5-6a)$$

We obtain

$$Q(t) = \frac{Q(o)}{1 + \frac{Q(o)}{\epsilon C_o kT} \frac{t}{(\ell^2/D)}} \quad (5-6b)$$

and

$$J(t, \ell) = \frac{J(t, o)}{\left[1 + \frac{Q(o)}{\epsilon C_o kT} \frac{t}{(\ell^2/D)} \right]^2} \quad (5-6c)$$

with

$$J(t, o) = \frac{4}{3} \frac{Q(o)}{(\ell^2/D)} \frac{Q(o)}{\epsilon C_o kT} \quad (5-6d)$$

The form of the expression (5-6b) is a familiar form appearing in the standard lumped circuit model in which the current density has been assumed to be constant. In our case, however, as we can see in Fig. 5.1a, the current density is not constant at all. But we have obtained the similar expression (5-6b) in our discharge model.

We will now show that the hyperbolic charge decay characteristic as seen in Eq. (5.6b) above is not the consequence of the constant-current assumption but rather is due to the nonlinear self-induced drift effect alone. That is, independent of the assumption made on the current

density profile, if we solve the nonlinear diffusion equation

$$\frac{\partial q}{\partial t} = - \frac{\partial}{\partial x} \left[- \frac{\mu q}{C_0} \frac{\partial q}{\partial x} \right] \quad , \quad (5-7)$$

with appropriate boundary conditions we should obtain a similar expression to Eq. (5-6b). To make this point clear, we solve this Eq. (5-7) in Appendix A by separation of variables with the following boundary conditions

$$J(t,0) = - \frac{\mu q}{C_0} \frac{\partial q}{\partial x} \Big|_{x=0} = 0 \quad , \quad (5-8a)$$

and

$$q(t,\ell) = \alpha q(t,0) \quad , \quad (5-8b)$$

with α being a fraction of unity. The solution is indeed given by a similar form to Eq. (5-6b):

$$Q(t) = \frac{Q(0)}{1 + f(\alpha) \frac{Q(0)}{\ell C_0 kT} \frac{t}{(\ell^2/D)}} \quad , \quad (5-9)$$

where $f(\alpha)$ is defined in the Appendix I and has been computed numerically.

In Appendix B, the same problem is treated for the case of uniform current density in space. $Q(t)$ is again given as in Eq. (5-9) above but in this case with $f(\alpha)$ being a rational function of α . The function $f(\alpha)$ is plotted in Fig. 5.3 and compared for the both cases. Note that

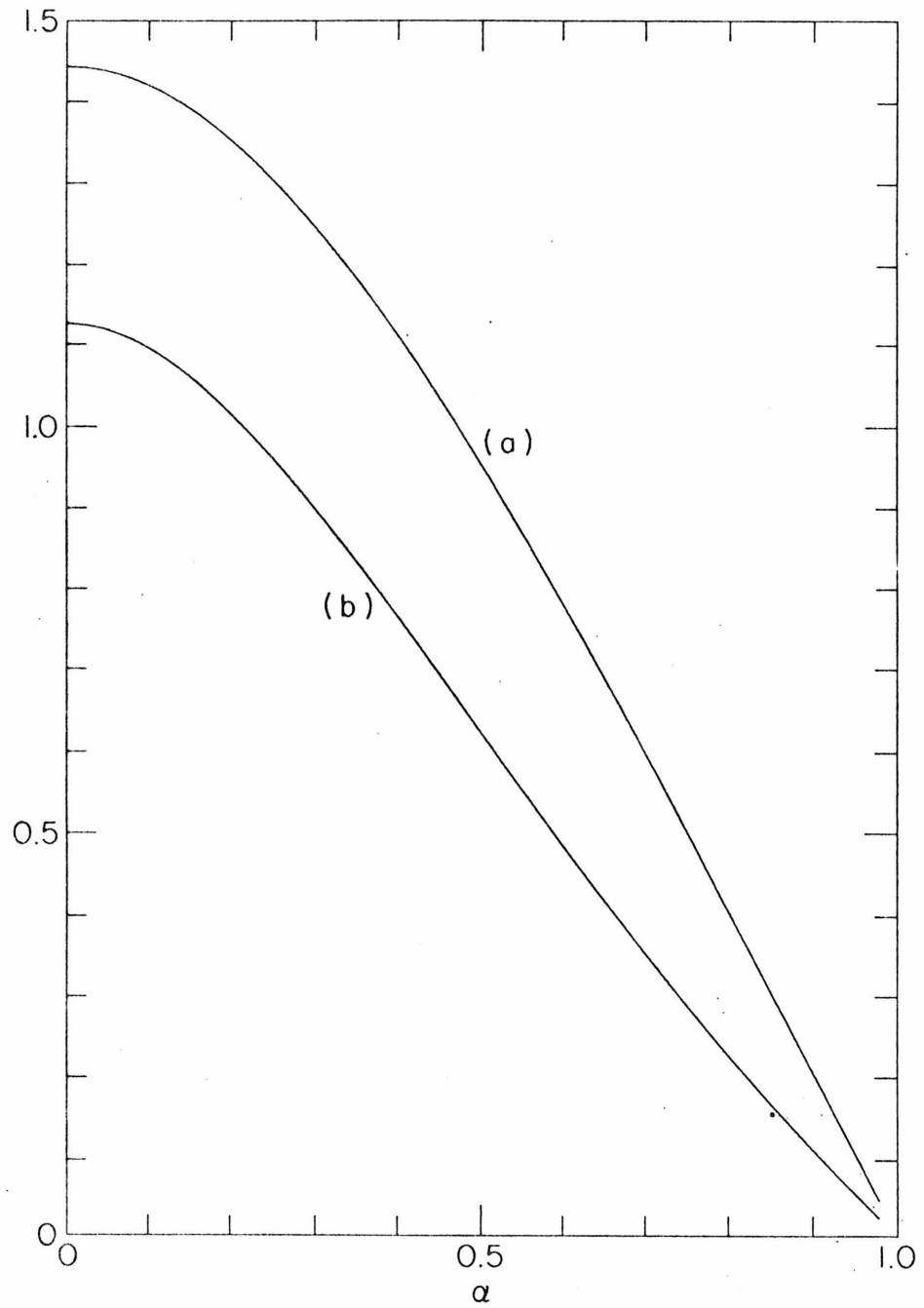


Fig. 5.3 $f(\alpha)$ defined by Eq. (A.6b) in Appendix A and by Eq. (b.5) in Appendix B are shown in curve (a) and (b) respectively.

the characteristic difference between the two cases is quite negligible. This observation supports the fact that the lumped circuit model gives excellent agreement with numerical results even though the current density at the beginning of discharge is not really uniform in the spatial coordinate.

5.4 Buried Channel IGFET in the Beginning of the Second Stage

In this section we first describe the characteristics of the potential profile under the transfer gate at the beginning of the second stage. It is shown that the potential profile which we observe under the transfer gate in Fig. 5.1b is a logarithmic function in space. Assuming the charge density at the beginning of the transfer gate to be a constant in time, the charge propagation time τ_p for the charge to reach the end of the transfer gate from the beginning of the transfer gate is estimated. The duration of the steady state after this propagation time is also considered in this section.

In the lumped circuit model, the current density under the transfer gate is assumed to be uniform. Figure 5.1b illustrates the details of the charge transfer at this stage. We observe in the figure that the charge profile under the transfer gate is very much a linear function of the spatial coordinate. Hence we write the charge density as

$$q(t,x) = q(t,0) + \left(\frac{x}{\ell}\right)[q(t,\ell) - q(t,0)] \quad . \quad (5-10a)$$

Then, solving the expression (5-1b) for the potential profile in the case of uniform current density, we obtain

$$\phi_m(x) = \phi_m(0) + \left[\frac{\ell J}{(1-\alpha)\mu q(0)} - kT \right] \ln \left[1 - (1-\alpha) \left(\frac{x}{\ell} \right) \right], \quad (5-11)$$

where α is defined by Eq. (5-8b) as before. Hence, the potential profile which we observe under the transfer gate in Fig. 5.1b is a logarithmic function in space. Since the current density under the source gate in Fig. 5.1b is still quite linear in space, the charge and potential profiles under the source gates must be of elliptic shape as we have discussed in the previous section. This stage should last as long as the source storage gate supplies the signal charge to flow through the transfer gate. And the charge transfer in this stage is quite adequately described by Buried Channel IGFET.

We are now in the position to consider the propagation time and the duration of the steady state in the beginning of this second stage of the charge transfer.

We assume the charge density $q(t,0)$ at the beginning of the transfer gate to be a constant q_0 in time. In this stage, the charge propagation time τ_p for the charge to reach the end of the transfer gate from the beginning of the transfer gate is estimated in Appendix C, and is given by

$$\tau_p = (0.38) \left(\frac{C_0 kT}{q_0} \right) \left(\frac{\ell^2}{D} \right) \quad (5-11)$$

During the transient period illustrated in Fig. 5.1a and 5.1b, we observe the peak charge density at the beginning of the transfer gate is fairly constant. This observation is supported by the fact that the gradient of the current density goes through zero in the interelectrode region because the source gate is discharging and the transfer gate is being charged in this period. (See the current density profiles in Fig. 5.1a and 5.1b). Hence as a consequence of conservation of charge, the total charge under the transfer gate must not change in time. That is, from the results illustrated in Fig. 5.2, we conclude this stage lasts only for a very short period. Note that Fig. 5.1b illustrates the details of the charge transfer at the instant when the net charging of the transfer gate is zero. That is, in Fig. 5.2 (top), this is the time when the line (a) passes through the zero. At the same time, in Fig. 5.2 (bottom), the curve (c) is at its peak value and the curve (a) starts decreasing.

5.5 Lumped Circuit Model in the Second Stage

In this section we first give the general description of the charge transfer in the second stage, leading to the calculation of the total charge under the source gate as a function of time. In this calculation we assume an appropriate shape for the charge profile. Furthermore, we will discuss the time it takes for the fringing field effect to become compatible to the self-induced field drift, and then the time it takes more to observe the final exponential decay characteristics. The analysis is extended to the calculation of the total charge under the transfer gate as a function of time. And the time when the

residual charge under the source gate becomes less than the charge under the transfer gate is estimated.

In this second stage with minor modifications, the charge transfer under the source gate is described quite adequately in the manner presented in the Section 5.3. Since the charge density under the source gate is diminishing to the amount that the thermal diffusion and fringing field drift may soon become compatible to the self-induced field drift effect, we include in the following analysis all of the three effects.

The presence of charge q raises the local channel potential ϕ_m by q/C_0 whose gradient is the self-induced field. The difference of the potential we observe in Fig. 5.1 is plotted as a function of the local charge density q in Fig. 5.4. The potential difference is indeed proportional to q and its proportionality constant is $1/C_0$. Hence formally we can write the minimum channel potential as

$$\phi_m(x) = \phi_{m_0}(x) + \frac{q(x)}{C_0} \quad (5-12a)$$

where $\phi_{m_0}(x)$ is the channel potential without any charge. Substitution of Eq. (5-12a) into Eq. (5-16) results in

$$J = -D \frac{\partial q}{\partial x} - \frac{\mu}{C_0} q \frac{\partial q}{\partial x} - \mu q \frac{\partial \phi_{m_0}}{\partial x} \quad (5-12b)$$

The total current density is given as a sum of thermal diffusion, self-induced field drift and fringing field drift terms. This equation can be solved in two different approaches. One way is to assume the current

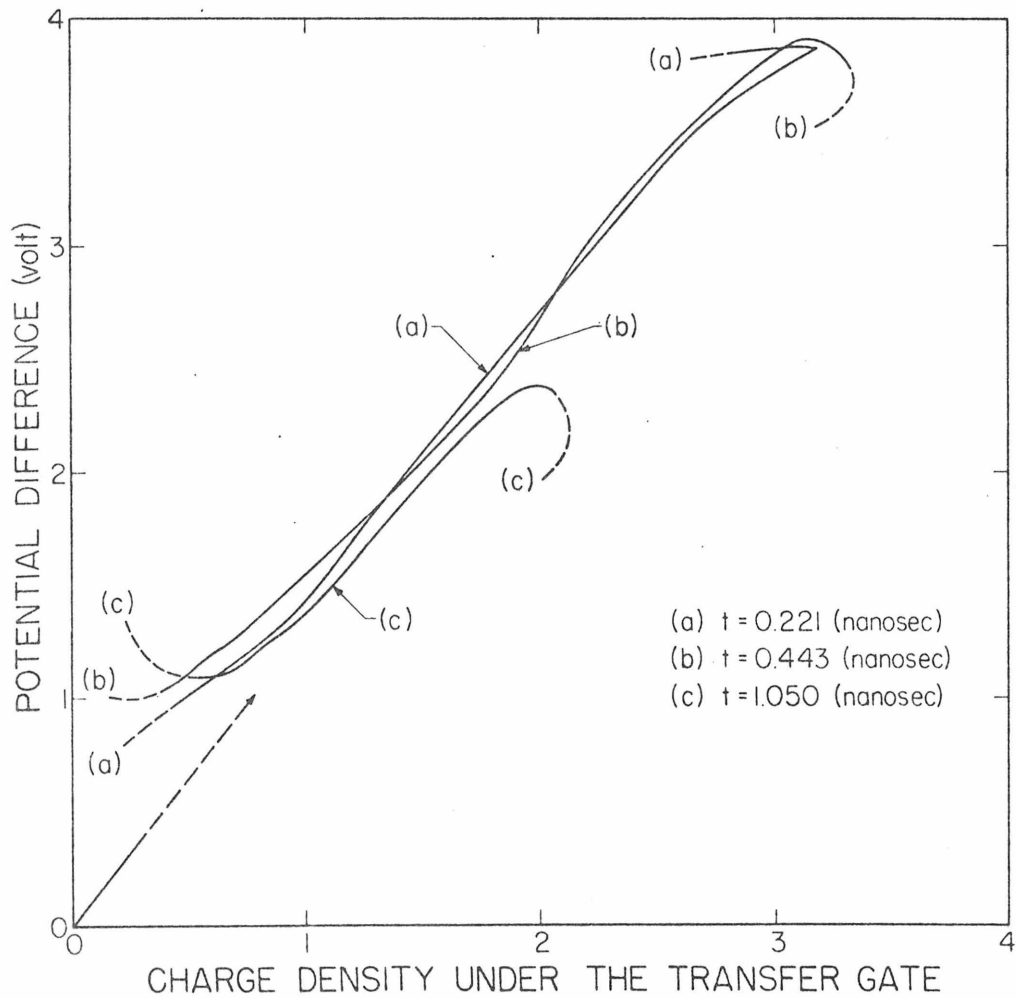


Fig. 5.4 Plot of the potential difference due to the charge under the transfer gate. The curves (a), (b), and (c) correspond to the three stages shown in Fig. 5.1. Note the potential difference is roughly proportional to the charge density. The effective capacitance (slope) is $C_0 \approx \Delta q / \Delta V = 0.75$ normalized charge density per volt.

density to be constant, and obtain the charge profile by solving Eq. (5-12b) for q . The other way is to assume a form for the charge profile and evaluate the current density by Eq. (5-12b). We now give a simple argument to obtain a solution of Eq. (5-12b) following the latter approach.

From the plot of the charge profile in Fig. 5.1c, we simply note that the charge profile can be roughly approximated by a linear function:

$$q(t,x) = q(t,0) \left[1 + (\alpha-1) \left(\frac{x}{\ell} \right) \right] \quad (5-13a)$$

Hence the total charge under the source gate is given by

$$Q(t) = \int_0^{\ell} q(t,x) dx = \frac{\ell(1+\alpha)}{2} q(t,0) \quad (5-13b)$$

We note from Fig. 5.1c, the charge density under the source gate can be approximated by a linear function of space as was given by Eq. (5-3a). The integration of Eq. (5-12b) over space results in the discharge current density $J(t,\ell)$ at the end of the source gate in terms of the total charge under the source gate $Q(t)$:

$$J(t,\ell) = \frac{Q(t)}{\tau_0} + \frac{\beta}{\tau_{th}} \frac{Q^2(t)}{C_0 kT} \quad (5-14a)$$

where τ_0 is the exponential decay time constant when the second term in RHS of Eq. (5-14a) above becomes small compared to the first term and given by

$$\tau_0 = \frac{\tau_{tr}}{2} \frac{1}{1 + \beta \frac{\tau_{tr}}{\tau_{th}}} \quad (5-14b)$$

β is a constant (whose value is around unity) and given by

$$\beta = \frac{16}{\pi^2} \left(\frac{1 - \alpha}{1 + \alpha} \right) \quad (5-14c)$$

The thermal diffusion and single carrier transit time constants, τ_{th} and τ_{tr} , are defined as

$$\tau_{th} = \frac{4l^2}{\pi^2 D} \quad (5-15a)$$

and

$$\tau_{tr} = \frac{l}{\mu E} \quad (5-15b)$$

In this formalization the fringing field is assumed to be constant for simplicity and given by E . The effective strength E may be estimated by evaluating

$$\frac{l}{E} = \int_0^l \frac{dx}{\left(\frac{\partial \phi_{m0}}{\partial x} \right)} \quad (5-15c)$$

where $\partial \phi_{m0} / \partial x$ is the gradient of the channel potential without any charge shown in Fig. 5.5 (bottom) with solid line. Solving the continuity equation (5-6a) we obtain the total charge under the source gate as a function of time.

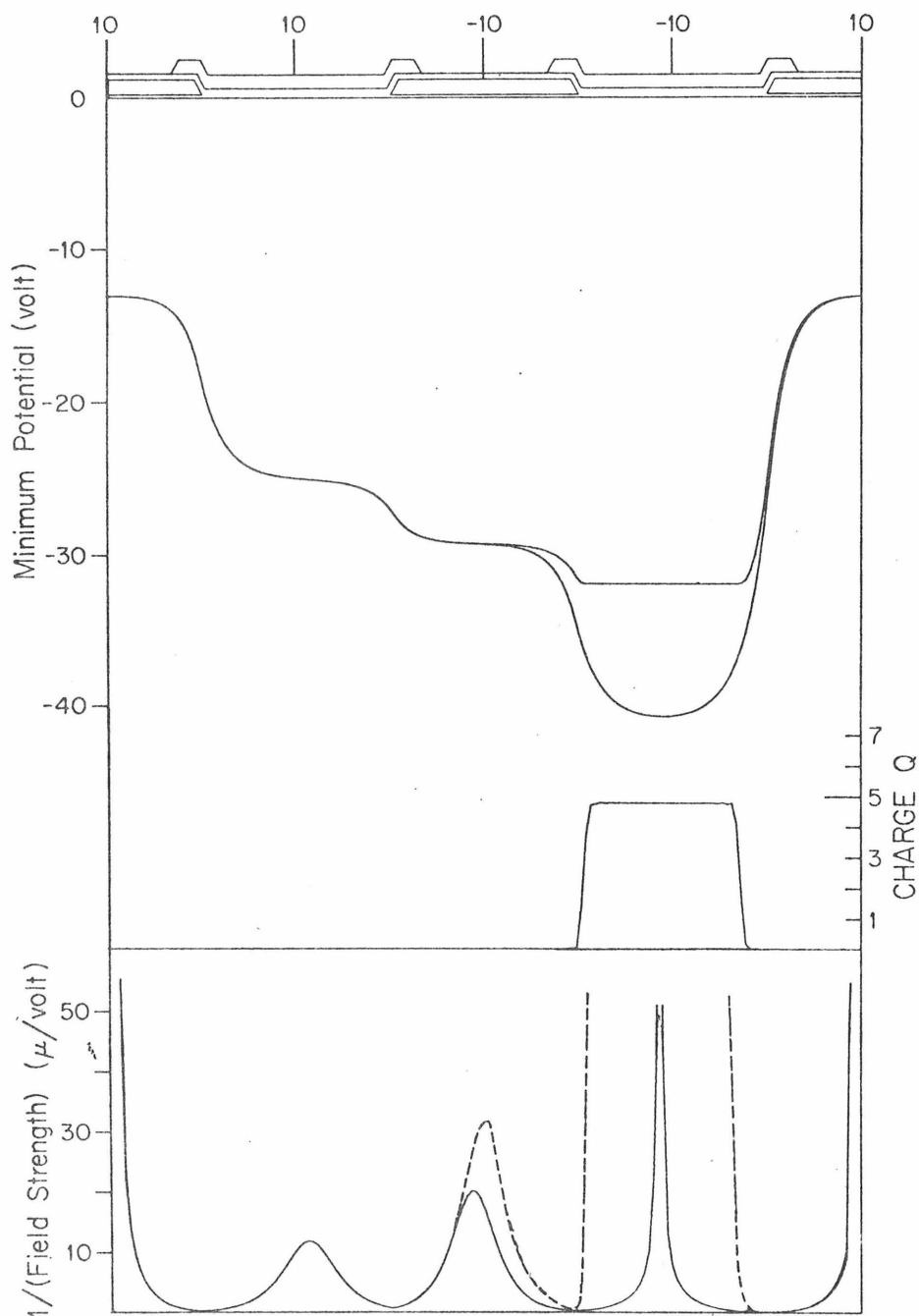


Fig. 5.5 Plots of the minimum potential, charge density and the reciprocal of the fringing field strength. The dashed curve in the bottom is with the charge under the drain gate.

$$Q(t) = \frac{Q(o) \exp(-t/\tau_o)}{1 + \beta \frac{\tau_o}{\tau_{th}} \frac{Q(o)}{\ell C_o kT} [1 - \exp(-t/\tau_o)]} \quad (5-16)$$

This equation has been derived under the assumption that the charge profile is given by a linear function of the form given by Eq. (5-13a). Hence, the peak of the charge profile is assumed to be always at the beginning of the source gate.

We are now in the position to calculate the time it takes for the fringing field effect to become compatible to the self-induced field drift and then, the time it takes more to observe the final exponential decay characteristics.

According to Eq. (5-16) above, after the time yet to be determined, the charge will decay exponentially in time. This time τ_o can be estimated as following. We equate the magnitude of the first term of RHS of the expression (5-14a) for the current density to the second term. Then, we obtain the minimum charge Q_m for which the self-induced field effect is compatible to the fringing field drift and thermal diffusion effects:

$$Q_m = \frac{1}{\beta} \left(\frac{\tau_{th}}{\tau_o} \right) (\ell C_o kT) \quad (5-17a)$$

Solving Eq. (5-16) for $Q(t) = Q_m$, we obtain the time t_o at which the charge transfer begins to be influenced by the fringing field and thermal diffusion mechanism:

$$t_0 = \tau_0 \ln \left[\frac{2}{1 + Q_m/Q(0)} \right] \approx (0.69) \tau_0 \quad . \quad (5-17b)$$

According to the detailed numerical simulation of the charge transfer illustrated in Fig. 5.1, the peak of the charge profile indeed stays at the beginning of the source gate for a while. And during this period, the charge decays in the manner characterized in this section. And for $t > t_0$ the total charge $Q(t)$ given by Eq. (5-16) can be described quite accurately by

$$Q(t) = Q_m \exp \left(- \frac{(t - t_0)}{\tau_0} \right) \quad . \quad (5-17c)$$

After this time t_0 , the fringing field influences the charge transfer as the main mechanism. Then as have analyzed in detail in Ref. [4], at some time later the peak of the charge profile starts moving towards the end of the gate. Figure 5.6 illustrates the details of the charge transfer under the transfer gate at this stage. After this transition time, the relative shape of the charge becomes stationary and the charge decays exponentially in time. The transition time Δt in this process has been estimated in Chapter 2 and is given by

$$\Delta t = \left(\frac{\tau_{tr}}{2\pi^2} \right) \left(\frac{E\ell}{kT} \right) \quad . \quad (5-18a)$$

At the time $t_1 = t_0 + \Delta t$, the charge will start decaying exponentially with the final decay time τ_f . In this stage, the self-induced field

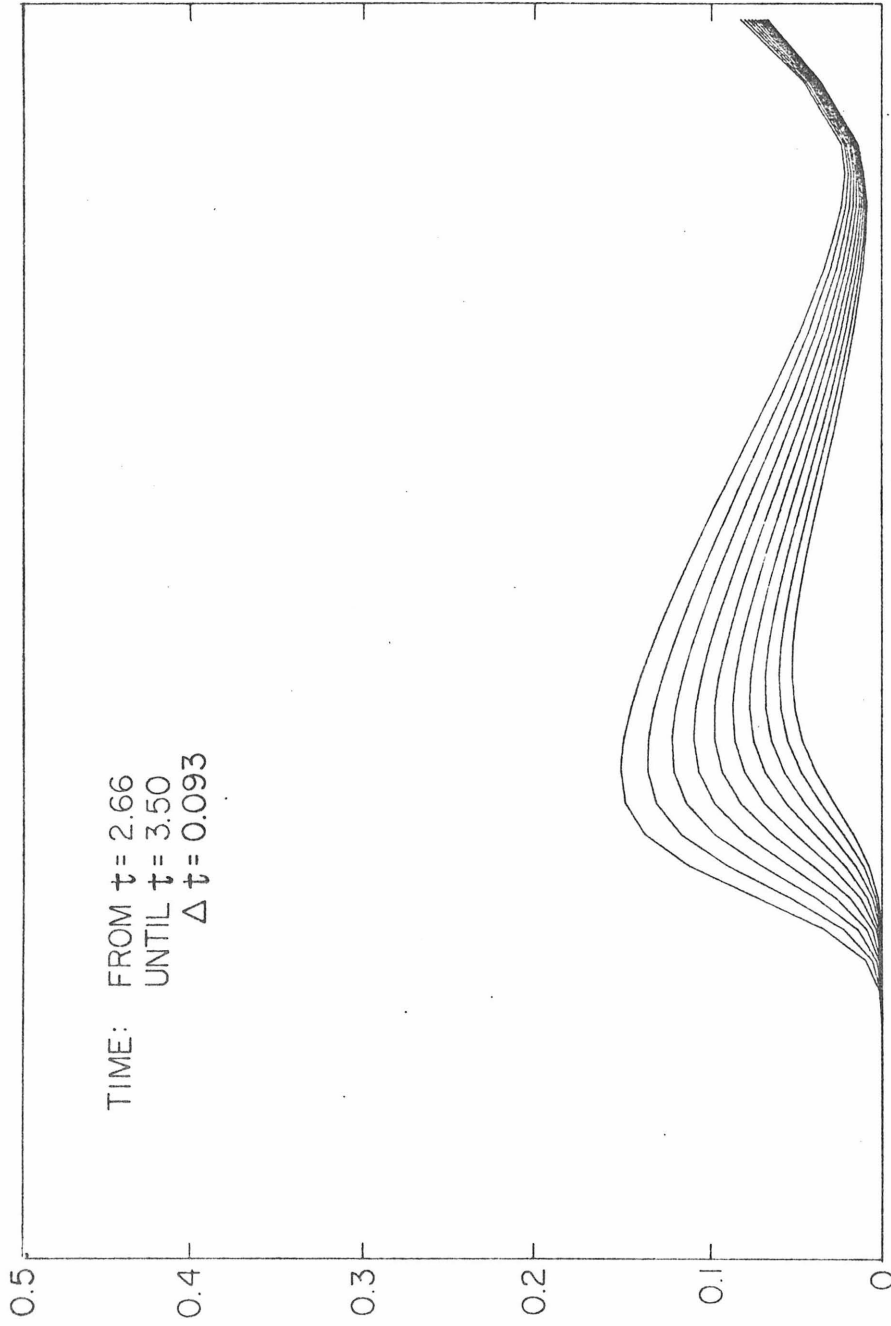


Fig. 5.6 Charge profiles under the transfer gate at several instances. Note the peak of the charge profile is drifting. The time is in the normalized unit of $(0.001) L^2/D = 1.92$ nanosec. The charge density is also normalized by $935e/\mu^2$.

drift effect has become completely negligible compared to the thermal diffusion and fringing field drifts. (See. Fig. 5.7). In this final stage of the charge transfer, the total charge is approximately given by

$$Q(t) = Q_E \exp \left[- \frac{(t-t_1)}{\tau_f} \right] \quad , \quad (5-18b)$$

where

$$Q_E = Q_m \exp \left(- \frac{\Delta t}{\tau_0} \right) \quad . \quad (5-18c)$$

We now focus our attention upon the charge under the transfer gate. Specifically we will calculate the total charge under the transfer gate as a function of time. The time rate of the change in the total charge under the transfer gate is given by the difference of the current density $J(t,0)$ at the beginning of the transfer gate from the current density $J(t,\ell)$ at the end of the transfer gate:

$$\frac{\partial Q}{\partial t} = J(t,0) - J(t,\ell) \quad . \quad (5-19)$$

The readers should not be confused by the dual usage of the symbols Q , J and space coordinate x under the source gate and transfer gate. When we are discussing the charge transfer under one particular gate, we define the beginning of the gate to be a $x = 0$ and the end of the gate to be at $x = \ell$. The symbol Q in Eq. (5-19) is meant to be the total charge under the transfer gate whereas in Eq. (5-14a) and (5-16) the same symbol is used for the total charge under the source gate.

We note the current density $J(t,0)$ is given as an independent

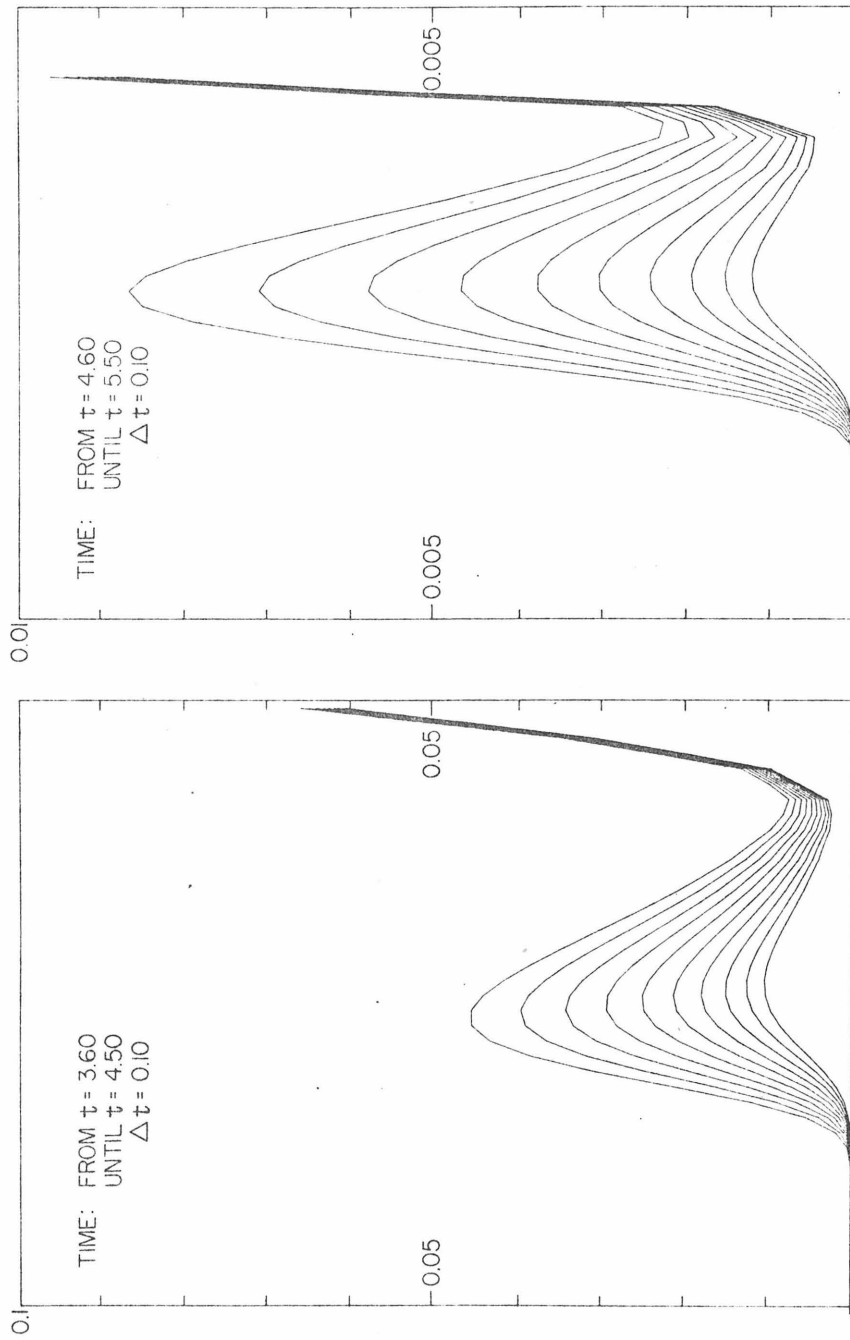


Fig. 5.7 The charge profiles under the transfer gate at the final stage of the charge transfer process. Note the relative shape of the charge profile is not changing in time, implying the exponential decay characteristics.

quantity which is a function of time only. This function can be obtained from Eq. (5-14a) with use of Eq. (5-16). Care must be taken in applying these equations in Eq. (5-19).

As we see in Fig. 5.1c, the current density under the transfer gate can be quite adequately approximated by a linear function:

$$J(t,x) = J(t,o) + \left(\frac{x}{\ell}\right) \left[J(t,\ell) - J(t,o) \right] \quad (5-20a)$$

The charge profile under the transfer gate can be approximated again by Eq. (5-13a) as in the case of the source gate. Then, integrating with Eq. (5-12b) the charge density given by Eq. (5-20), we obtain the discharge density $J(t,\ell)$ at the end of the transfer gate in terms of the total charge under the transfer gate $Q(t)$:

$$J(t,\ell) + J(t,o) = \frac{Q(t)}{\tau_o} + \frac{\beta}{\tau_{th}} \frac{Q^2(t)}{\ell C_o kT} \quad (5-20b)$$

where τ_o , τ_{th} , and β are defined as before. Then, eliminating the charge density $J(t,\ell)$ at the end of the transfer by using Eqs. (5-19) and (5-21), we obtain

$$\frac{\partial Q}{\partial t} = 2J(t,o) - \left[\frac{Q(t)}{\tau_o} + \frac{\beta}{\tau_{th}} \frac{Q^2(t)}{\ell C_o kT} \right] \quad (5-20c)$$

The total charge under the transfer gate $Q(t)$ can be obtained as a function of time by solving this equation (5-20c) above. As we observe in Fig. 5.2 (top), the charging current $J(t,o)$ becomes negligible compared to the discharge current $J(t,\ell)$ at the time, t_o , given by Eq. (5-17b). This is approximately the time when the total charge under the source gate becomes quite negligible compared to the total charge under the

transfer gate. At this time, the lines (a) and (c) in Fig. 5.2 (bottom) start joining together, and the line (b) starts to exhibit the final exponential charge decay characteristics. Hence after this time, the charging current term $J(t,0)$ in Eq. (5-20c) above can be ignored. And we obtain the solution of $Q(t)$ in the same form as was given previously in Eq. (5-16).

The entire charge transfer analysis in this second stage will now be complete with the estimation of the time when the residual charge under the source gate becomes less than the charge under the transfer gate.

We note in Fig. 5.2 (bottom), when the lines (b) and (c) coincide, the total charge under the source gate is equal to the total charge under the transfer gate. Since the sum of the two quantities are the total initial charge under the source gate, we observe that at this time the charge under the source gate decreased to 50% of what was there originally. This time, τ_p , can be estimated by setting $Q(t) = Q(0)/2$ in Eq. (5-16). And we obtain for $Q(0) \gg Q_m$,

$$\tau_p = \left(\frac{4}{\pi^2 \beta} \right) \left(\frac{C_o kT}{Q(0)/\ell} \right) \left(\frac{\ell^2}{D} \right) \quad (5-21)$$

At this time ($t \approx \tau_p$), as we observe in Fig. 5.2, the head of the charge packet reaches at the end of the transfer gate and the discharge current starts rising as seen in line (c) of Fig. 5.2 (top). We recall this time has been estimated by a different method in Appendix C, and is given by Eq. (5-11). Note the similarity in Eqs. (5-11) and (5-21)

5.6 The Exponential Decay Characteristics in the Final Stage

In this section we first describe qualitatively the channel potential profile and the charge distribution at the completion of the second stage of the charge transfer. We will then describe and outline how to estimate the final decay time constant in the final stage of the charge transfer. The actual analytic formula for the final decay time constant with appropriate fringing field profile and the charge distribution is also presented.

In Fig. 5.5, we have plotted the minimum channel potential, charge density, and reciprocal of the potential gradient at the completion of charge transfer. The solid curve in the bottom figure is the plot for the potential gradient with no charge everywhere. The dashed curve is the one with all the signal charge resting finally under the drain gate. The presence of the charge under the source gate lowers the minimum field strength under the transfer gate by 158 volt/cm. That is, the minimum field strength is 318 volt/cm with charge and 493 volt/cm with no charge. The minimum field strength under the source gate remains almost the same value of 844 volt/cm.

Note the charge and potential profile under the drain gate is everywhere flat. This is expected because the charge is at rest and the current density J in Eq. (5-1b) is zero. Hence the charge density is given as an exponential function of the potential:

$$q = q_0 \exp \left[- \frac{\phi_m - \phi_{m0}}{kT} \right] \quad (5-22)$$

where ϕ_{m_0} is the local minimum channel potential under the drain gate and q_0 is the peak charge density. A small increase in the potential ϕ_m results in a drastic reduction in the charge density q . And only way to pack the total charge under the drain gate is to have ϕ_m near ϕ_{m_0} wherever the charge is present: Inside the charge packet, there is no field.

We will now describe and outline how to estimate the final decay time constant in the final stage of the charge transfer.

In Chapter 2 we have analyzed the charge transfer process in this final stage. According to the detailed analysis of the charge transfer under the influence of fringing fields, the profile of charge under the source and transfer gates changes for approximately a single carrier transit time and then becomes stationary with an exponential time decay of the amplitude. The exponential time constant t_f is estimated by the standard variational procedure and given by

$$\frac{1}{\tau_f} = \frac{s}{\tau_{th}} + \frac{(\mu E_{eq})^2}{4D}, \quad (5-23a)$$

where s is a dimensionless quantity determined by the final charge profile $q(x)$ under the transfer gate.

$$s = \frac{4\ell^2}{2\pi} \frac{\int_0^\ell \left[\frac{dq}{dx}\right]^2 dx}{\int_0^\ell q^2(x) dx} \quad (5-23b)$$

E_{eq} is an equivalent constant fringing field for the spatially varying fringing field $E(x)$ and is given by

$$E_{\text{eq}}^2 = \frac{\int_0^l \left[E^2(x) - 2kT \frac{dE}{dx} \right] q^2(x) dx}{\int_0^l q^2(x) dx} \quad (5-23c)$$

To estimate the value of the final decay time constant, the knowledge of the fringing field profile and the final charge density profile is required. In Fig. 5.6 and 5.7 we presented the charge profiles at several instances till the profile reaches the final form and decays with an exponential time constant, τ_f .

If we use the final charge profile shown in Fig. 5.7 and the fringing field profile shown in Fig. 5.5 (bottom) in evaluating the final exponential decay time constant τ_f from Eqs. (5-23), the calculated value is exactly the same value we obtained from the results of the detailed numerical simulation of the charge transfer process. This is expected from the consequence of the variational calculus. The variational procedure is a powerful tool to estimate the eigenvalues of a physical system when the eigenfunctions (or states) are not known exactly. When they are known, the calculated eigenvalues are the exact eigenvalues of the system. Hence the true usefulness of the procedure described in Eqs. (5-23) lies upon the fact that we can obtain a good estimate of the value of the final decay time constant without knowing the values of the fringing field and the charge density at every point in space. That is, the knowledge of general characteristics of these profiles should be enough to obtain a good estimate of the final decay time constant.

The results we presented in Fig. 5.5 suggests that the fringing field can be approximated roughly by

$$E(x) = \frac{E_{\min} \ell}{2x} \quad \text{for} \quad 0 < x < \frac{\ell}{2},$$

$$E(x) = \frac{E_{\min} \ell}{2(\ell - x)} \quad \text{for} \quad \frac{\ell}{2} < x < \ell. \quad (5-24a)$$

From Fig. 5.6, accordingly we approximate the charge profile by

$$q(x) = \left(\frac{2x}{\ell}\right)^n q_0 \quad \text{for} \quad 0 < x < \frac{\ell}{2},$$

$$q(x) = 2^n \left(1 - \frac{x}{\ell}\right)^n q_0 \quad \text{for} \quad \frac{\ell}{2} < x < \ell, \quad (5-24b)$$

where we have introduced one parameter n whose value is to be determined by minimizing $\tau_f(n)$ of Eq. (5-23a), according to the standard variational procedure. The calculation is somewhat involved but the results are very useful in estimating the final decay time constant and are presented in Fig. 5.8a for our case study. The same procedure may be applied for different gate length and other physical parameters. Hence we have plotted in Fig. 5.8b the ratio of the final decay time constant to the thermal diffusion time constant as a function of the normalized fringing field strength $\ell E_{\text{eq}}/kT$:

$$\frac{\tau_f}{\tau_{\text{th}}} = \frac{1}{s + (\ell E_{\text{eq}}/kT)^2} \quad (5-25a)$$

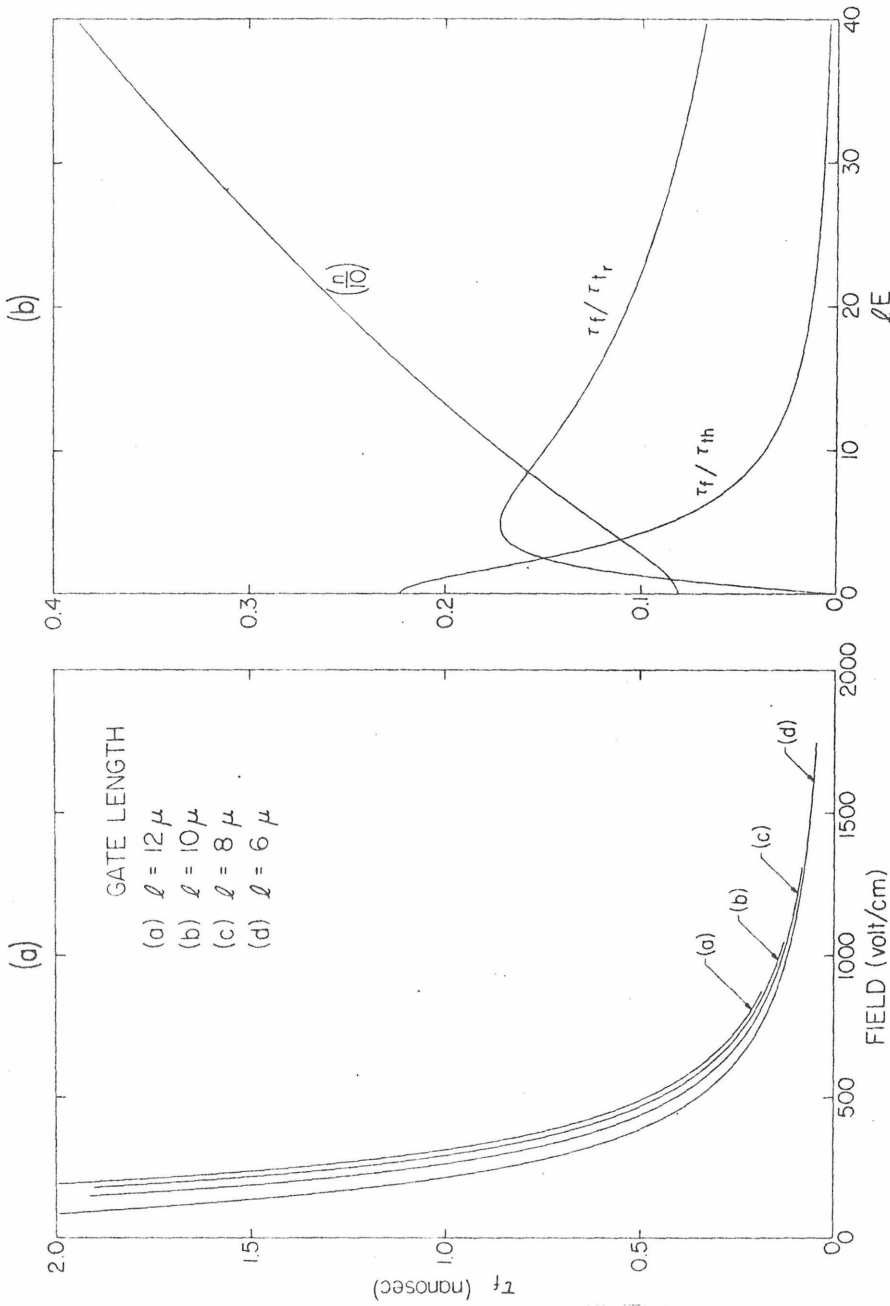


Fig. 5.8 (a) The final decay time constant estimated for the charge and fringing field profiles given by Eq. (5.24). $D = 12 \text{ cm}^2/\text{sec}$.

(b) The parameter n appearing in Eq. (5.24) is scaled down by factor 10 to match the scale with the plots of τ_f/τ_{th} and τ_f/τ_{tr} .

The computational procedure to compute τ_f is described briefly in Appendix D. Since from Eqs. (5-15)

$$\frac{\tau_{th}}{\tau_{tr}} = \frac{4\ell E_{eq}}{\pi^2 kT} \quad , \quad (5-25b)$$

we obtain the ratio of the final decay time constant to carrier transit time:

$$\frac{\tau_f}{\tau_{tr}} = \frac{4\ell E_{eq}/\pi^2 kT}{s + (\ell E_{eq}/kT)^2} \quad . \quad (5-25c)$$

This quantity is also plotted in Fig. 5.8b.

5.7 Numerical Results

In this section we will first give the values of relevant physical parameters in our case study and describe the normalization units for the illustrations. Then we will describe in general how to estimate the quantities τ_0 , Q_m , t_0 , and τ_f in the final stage of charge transfer. The outline and results of the detailed calculation procedure of the related physical parameters such as τ_0 , t_0 , Δt , t_1 , Q_m , and Q_t are also presented.

The analysis we have done so far is intended to characterize the entire charge transfer quantitatively with reasonable accuracy. For our case study, the diffusion layer depth is $X_d = 1\mu$ and the channel doping is set to be $N_A = 25,000$ electron charges/ μ^3 . The average width of the charge packet is $X_{CH} = 0.15\mu$. Hence the total charge is $Q_{total} = N_A X_{CH} \ell = 45,000$ electron charges/ μ where the aluminum or silicon

gate length ℓ is taken to be 12μ . The charge density shown in the figures are normalized by $Q_{\text{total}}/L = 935$ electron charges/ μ^2 where the length L of one unit cell of the device is 48μ in our case study. Accordingly, the time is normalized by $(0.001) L^2/D = 1.92$ nanoseconds and the current density by $Q_{\text{total}} D/L^2 = 23.4$ electron charges/ $\mu \cdot \text{nanosec}$. The effective oxide capacitance C_0 under the transfer gate is (as seen in Fig. 5.4) 0.75 normalized charge density per volt. Hence $\ell C_0 kT = 21$ electron charges/ μ . For the gate length $\ell = 12\mu$, the thermal diffusion time constant τ_{th} is equal to 48.6 nanosecond by Eq. (5-15a).

We will now describe in general how to estimate the quantities τ_0 , Q_m , t_0 , and τ_f in the final stage of charge transfer. If the effective fringing field strength E at this final stage is known, we can compute τ_0 from Eq. (5-14b). Then the minimum charge Q_m and the time t_0 can be estimated by Eqs. (5-17a) and (5-17b). From the numerical results shown in Fig. (5.2) we can read off the values of Q_m and t_0 and compare them with the values predicted by Eqs. (5-17a) and (5-17b). The final decay time constant τ_f appearing in Eq. (5-18) can also be read off from Fig. 5.2 (bottom) and compared with the calculations done in the previous section which is summarized in Fig. 5.8a and 5.8b.

We have now reached to the final part of this section. In this last part we will first outline and then give results of the detailed calculation procedure of the related physical parameters such as τ_0 , t_0 , Δt , Q_m and Q_E .

The minimum fringing field as shown in Fig. 5.5 in the final stage of charge transfer is 315 volt/cm under the transfer gate and 844 volt/cm

under the source gate. Then with these values of the field strength, the plots of Fig. 5.8a predict the final decay time constants of 0.640 nanoseconds under the transfer gate and 0.155 nanoseconds under the source gate. The actual observed values in Fig. 5.2 (bottom) are 0.765 nanoseconds and 0.165 nanoseconds.

The effective fringing field E can be estimated by Eq. (5-15c) for the fringing field profile shown with the solid line in Fig. 5.5 (bottom), and is found to be 1250 volt/cm. The corresponding single carrier transit time τ_{tr} is 2 nanoseconds by Eq. (5-15b) where the hole mobility μ in silicon is taken to be $480 \text{ cm}^2/\text{volt-sec}$. Then since the ratio of τ_{tr} divided by τ_{th} (48.6 nanoseconds) is very small, we note from Eq. (5-14), τ_0 is about one-half of the single carrier transit time. That is, $\tau_0 \approx 1$ nanosecond. Hence from Eq. (5-17b), $t_0 \approx 0.5$ nanosecond. That is, the charge under the transfer gate should start decaying exponentially at $t = t_0 \approx 0.5$ nanosecond with the exponential decay time constant $\tau_0 \approx 1$ nanosecond. This period should last till $t_1 = t_0 + \Delta t$ where Δt is given by Eq. (5-18a). Since $E\ell/kT = 60$, we obtain $\Delta t = 6$ nanoseconds. Hence we expect $t_1 \approx 6.5$ nanoseconds. The actual value t_1 observed in lines (a) and (c) in Fig. 5.2 (bottom) is about 8 nanoseconds.

Q_m computed from Eq. (5-17a) for $\beta = 1$ is 1000 electron charges/ μ which is about 23% of the initial total charge $Q_{total} = Q(o) = 45,000$ electron charges/ μ . Then from Eq. (5-18c), since $\Delta t/\tau_0 \approx 6$, we obtain $Q_E \approx 2.5$ electron charges/ μ , which is about 0.055% of the initial charge. The actual value Q_E observed in Fig. 5.2 (bottom) is

about 0.07%.

5.9 Conclusion

The results of a detailed numerical simulation of free charge transfer in buried channel Charge Coupled Devices have been presented. Our analysis shows that except for a very short time the current density is not quite uniform. However the time dependence of the charge decay (see Section 5.3) is quite independent of the form assumed for the current density profile. The dominant effect was shown to be the fringing field effect and there are two time constants (τ_0 and τ_f) associated with the entire charge transfer process. The approximate analytic expressions for the two time constants and other important physical parameters (Q_m , Q_E , t_0 , t and Δt) are derived and the corresponding charge transfer characteristics are explained in detail. The most important quantity in this analysis is the residual charge $Q(t)$ as a function of time and we have obtained an explicit analytic expression of this quantity $Q(t)$. For 12μ gate structure, we have shown that the charge transfer efficiency can be achieved as high as 99.99% at 100MHz (see Fig. 5.2) and that this efficiency can be improved much further for compact CCD structures (shorter gate length, etc.) as discussed in Section 5.6 and summarized in Fig. 5.8.

Appendix A

SPATIALLY VARYING CURRENT DENSITY

We assume the solution of Eq. (5-7) to be the form given by

$$q(t,x) = q(o,o) A(t) \sqrt{B(x)} \quad , \quad (A-1a)$$

with

$$A(o) = 1 \quad . \quad (A-1b)$$

Hence from Eqs. (A-1a) above at $t = 0$ we obtain

$$B(o) = 1 \quad , \quad (A-1c)$$

and

$$Q(o) = \int_0^l q(o,x) dx = q(o,o) \int_0^l \sqrt{B(x)} dx \quad . \quad (A-1d)$$

Then, the boundary conditions for $B(x)$ corresponding to Eqs. (5-8a) and (5-8b) are given by

$$\frac{dB}{dx} = 0 \quad \text{at} \quad x = 0 \quad , \quad (A-2a)$$

and

$$B(\ell) = \alpha^2 \quad . \quad (A-2b)$$

Substituting Eq. (A-1a) into Eq. (5-7) we obtain

$$\beta = - \frac{1}{A^2(t)} \frac{dA}{dt} = - \frac{\mu}{2C_0} \frac{q(o,o)}{\sqrt{B(x)}} \frac{d^2B}{dx^2} \quad . \quad (A-3)$$

where β is a constant to be determined from the shape of the function $B(x)$ to be solved. Solving Eq. (A-3) further, we obtain

$$A(t) = \frac{1}{1 + \beta t} \quad , \quad (A-4a)$$

$$\left(\frac{dB}{dx}\right)^2 = \frac{8 C_0 \beta}{3\mu q(o,o)} \left[1 - B^{\frac{3}{2}}(x) \right] \quad . \quad (A-4b)$$

Hence the function $B(x)$ can be expressed implicitly by the integral

$$\int_{B(x)}^1 \frac{dB}{\sqrt{1 - B^{3/2}}} = \left(\frac{x}{\ell}\right) g(\alpha) \quad , \quad (A-5a)$$

where

$$g(\alpha) = \int_{\alpha}^1 \frac{dB}{\sqrt{1 - B^{3/2}}} \quad , \quad (A-5b)$$

and

$$\beta = \frac{3 q(o,o)}{8C_0 \ell^2} g^2(\alpha) \quad . \quad (A-5c)$$

Use of Eq. (A-1d) allows us to write the constant β in the form:

$$\beta = \frac{f(\alpha)}{(\ell^2/D)} \frac{Q(o)}{\ell C_0 kT} \quad , \quad (A-6a)$$

where

$$f(\alpha) = \frac{3}{8} \frac{\ell g^2(\alpha)}{\int_0^{\ell} \sqrt{B(x)} dx} \quad (A-6b)$$

Now from Eq. (A-5a) we note

$$dx = \left[\frac{\ell}{g(\alpha)} \right] \frac{(-dB)}{\sqrt{1 - B^{3/2}}} \quad (A-7a)$$

Hence

$$\int_0^{\ell} \sqrt{B(x)} dx = \frac{\ell}{g(\alpha)} \int_{B(\ell)}^{B(0)} \frac{\sqrt{B} dB}{\sqrt{1 - B^{3/2}}} \quad (A-7b)$$

This integral can be calculated analytically. The limits of the integration are given by Eq. (A-1c) and (A-2b). Hence

$$\int_0^{\ell} \sqrt{B(x)} dx = \frac{4\ell}{3g(\alpha)} \sqrt{1 - \alpha^3} \quad (A-7c)$$

Hence from Eq. (A-6b) above we obtain

$$f(\alpha) = \frac{9}{32} \frac{g^2(\alpha)}{\sqrt{1 - \alpha^3}} \quad (A-7d)$$

When $\alpha = 0$, from Eq. (A-5b) we obtain

$$g(0) = \int_0^1 \frac{dB}{\sqrt{1 - B^{3/2}}} = \frac{4}{3} \int_0^{\pi/2} \sin^{1/3} \theta d\theta = 1.73 \quad (A-8a)$$

Hence from Eq. (A-7d) we obtain

$$f(0) = 1.44 \quad (A-8b)$$

To compute $f(\alpha)$ numerically for $0 < \alpha < 1$, we note from Eq. (A-5b) by transforming the variable in the integral we can write

$$g(\alpha) = \frac{4}{3} \int_{\arcsin(\alpha^{2/3})}^{\pi/2} \sin^{1/3} \theta \, d\theta \quad (\text{A-9})$$

Hence we evaluate $g(\alpha)$ from this Eq. (A-9) above to obtain $f(\alpha)$ from Eq. (A-7d).

Appendix B

UNIFORM CURRENT DENSITY

If we assume the current density J to be uniform in space, then from Eq. (5-3b) we obtain

$$J(t) = \frac{(1-\alpha^2)\mu}{2 C_0 \ell} q^2(t,0) \quad , \quad (B-1)$$

where we assume $q(t,\ell) = \alpha q(t,0)$ as before. The charge profile is given by

$$q(t,x) = q(t,0) \sqrt{1 - (1-\alpha^2)\left(\frac{x}{\ell}\right)} \quad . \quad (B-2)$$

The total charge under the source gate is then given by integrating Eq. (B-2) above to obtain

$$Q(t) = \left(\frac{2}{3}\right) \left(\frac{1 + \alpha + \alpha^2}{1 + \alpha}\right) \ell q(t,0) \quad . \quad (B-3)$$

Hence the current density in terms of the total charge is given by

$$- \frac{dQ}{dt} = J(t) = \left(\frac{9}{8}\right) \frac{(1-\alpha^2)(1+\alpha^2)}{(1 + \alpha + \alpha^2)^2} \frac{\mu}{C_0 \ell^3} Q^2(t) \quad . \quad (B-4)$$

Solving for $Q(t)$, we obtain the same formula (Eq. 5-9) with

$$f(\alpha) = \left(\frac{9}{8}\right) \frac{(1-\alpha^2)(1+\alpha)^2}{(1 + \alpha + \alpha^2)^2} \quad . \quad (B-5)$$

This function is plotted in Fig. 5.3 and compared with the results of the spatially-varying current-density case of Appendix A

Appendix C

PROPAGATION TIME UNDER TRANSFER GATE

The propagation time under the transfer gate can be calculated by solving the continuity Eq. (5-1a) with the self-induced field drift of Eq. (5-3b). We assume the current density at the beginning of the transfer gate is always a constant q_0 , and no charge is present under the transfer gate at $t = 0$. Therefore, we have

$$q(t,0) = q_0 \quad \text{for} \quad t \geq 0 \quad , \quad (\text{C-1a})$$

and

$$q(0,x) = 0 \quad \text{for} \quad 0 < x \leq \ell \quad . \quad (\text{C-1b})$$

Introducing the Boltzmann's transformation,

$$y = \frac{x}{2} \sqrt{\frac{C_0}{\mu q_0 t}} \quad , \quad (\text{C-2a})$$

and normalizing the charge density by

$$p = \left(\frac{q}{q_0}\right)^2 \quad , \quad (\text{C-2b})$$

the continuity equation becomes

$$\frac{d^2 p}{dy^2} = -\frac{2y}{\sqrt{p}} \frac{dp}{dy} \quad , \quad (\text{C-3a})$$

with boundary conditions

$$p = 1 \quad \text{at} \quad y = 0 \quad , \quad (\text{C-3b})$$

and

$$p = 0 \quad \text{at} \quad y = \infty \quad . \quad (C-3c)$$

Numerical integration is required to obtain a solution of Eq. (C-3a) above. The solution $p(y)$ decreases [5] monotonically from 1 at $y = 0$ to zero at $y = 0.81$. Hence by using Eq. (C-2a) we observe the head of the charge profile reaches the end of the transfer gate at $t = \tau_p$ such that

$$0.81 = \frac{\ell}{2} \sqrt{\frac{C_o}{\mu q_o \tau_p}} \quad . \quad (C-4)$$

Solving the Eq. (C-4) for τ_p , we obtain Eq. (5-1.).

Appendix D

EVALUATION OF τ_f

Substitution of Eqs. (5-24b) into Eq. (5-23b) results in an expression for the parameters in terms of n :

$$s = \frac{16 n^2 (2n + 1)}{\pi^2 (2n - 1)} \quad (D-1)$$

The equivalent constant fringing field can be evaluated by Eq. (5-23c) from Eq. (5-24a) together with Eq. (5-24b):

$$E_{eq}^2 = \frac{(2n + 1)}{(2n - 1)} E_{min}^2 \quad (D-2)$$

Hence from Eq. (5-23a) we obtain

$$\frac{1}{\tau_f} = \left(\frac{2n + 1}{2n - 1} \right) \left[\frac{1}{\tau_{th}} - \frac{16}{\pi^2} + \frac{(\mu E_{min})^2}{4D} \right] \quad (D-3)$$

or from Eq. (5-25) we obtain

$$\frac{\tau_f}{\tau_{th}} = \pi^2 / f \left(\frac{\mu E_{min}}{kT} \right) \quad (D-4a)$$

where

$$f(x) = \left(\frac{2n + 1}{2n - 1} \right) (16 n^2 + x^2) \quad (D-4b)$$

For a given value of $x = \mu E/kT$, we compute n such that

$$\frac{\partial f}{\partial n} = 4 \left[8n + 4 - \frac{(x^2 + 4)}{(2n - 1)^2} \right] = 0 \quad (D-5)$$

Then with this value of n , we compute $f(x)$ from Eq. (D-4b). Figure 5.7 results immediately from Eqs. (D-3) and (D-4a). For practical purposes, we first compute the value of n for $x = 0$ from Eq. (D-5). That is, rewriting Eq. (D-5) we obtain

$$x^2 = 32n \left[n^2 - \frac{n}{2} - \frac{1}{4} \right] \quad (D-6)$$

Hence for $x = 0$,

$$n_0 = \frac{1 + \sqrt{5}}{4} \approx 0.809 \quad (D-7)$$

For a larger n greater than $n_0 = 0.809$, we first calculate x from Eq. (D-6), then evaluate $f(x)$ from Eq. (D-4b) to obtain τ_f/τ_{th} from Eq. (D-4a). If the effective gate length ℓ is known, we can calculate τ_{th} by Eq. (5-15a) and obtain τ_f from Eq. (D-4a) or (D-3).

Chapter 6

APPENDIX III

SCHOTTKY BARRIER BURIED CHANNEL CHARGE COUPLED DEVICES

I. INTRODUCTION

In this chapter we discuss a new active semiconductor device. The device is analogous to the buried channel device discussed in previous chapters except that channel potential is controlled through Schottky barriers formed by metal electrodes deposited directly on the semiconductor. In contrast the standard buried channel device consists of conducting gates deposited on an insulator which rests upon the semiconductor.

This device has one principal advantage which may make it useful when the CCD concept is extended to materials other than silicon. The metal-oxide-semiconductor technology is exceedingly successful when based on silicon. However, when attempts have been made to extend this technology to other semiconductors there has been little success. The primary reason for this lack of success is the poor behavior of the semiconductor insulator interface. The new device described and analyzed in this chapter has the benefit of doing away with the semiconductor insulator interface under the control electrodes and going directly to a metal semiconductor interface which is well defined on semiconductors such as GaAs.

In this chapter we present an electrostatic analysis of the Schottky Barrier Buried Channel Charge Coupled Devices (SBBCCCD), which could be constructed with presently available technology on GaAs. Special attention was focused on making the electrostatic

potential in the channel such that one would expect smooth ~~transfer~~ of the charge and, hence, not encounter the difficulties which were found in the first buried channel charge coupled devices [1].

It was found that, if the structure was fabricated by simply putting metal pads on GaAs surface and leaving gaps between the pads, then the electrostatic potential had very undesirable wells in this gap region. These electrostatic wells would act as traps for the signal charge and, hence, prevent the satisfactory operation of the device. This important problem was solved by adding a high dielectric constant material (Si_3N_4) to the region between the metal electrodes. This solution is found to virtually eliminate the potential traps and make possible the operation of the device.

This chapter is organized in the following fashion. Section II contains a detailed description of the physical structure of the device. Section III contains a one dimensional electrostatic analysis of the device. Section IV contains a two-dimensional electrostatic analysis, and Section V contains conclusion and a discussion of the results.

II. DEVICE STRUCTURE

An obvious extension of the well-known buried channel charge coupled device [1] is a Schottky Barrier buried channel CCD which operates by moving majority carriers along the buried channel. This channel can be controlled by the gate voltages applied on the metal electrodes which form Schottky barriers with respect to the semiconductor in contact.

The proposed Schottky barrier buried channel structure is shown in Fig. 1 as a unit cell of three-phase n-channel CCD. It consists

of an n-type layer of GaAs on a p-type GaAs substrate with metal electrodes forming Schottky contacts at the semiconductor surface. The structure is completed with an Si_3N_4 film which can be deposited by a radio frequency glow discharge reaction [2] of silane and ammonia at a fixed substrate temperature of 300°C . The silicon nitride was chosen in this calculation because of its relative high dielectric constant of the order of 8. The thickness, X_d , is 20 times the acceptor density, N_A , of the substrate, which is $1000e/\mu^3$.

In order to form a buried channel, it is necessary to completely drain the n-type layer and part of the adjacent regions at the Schottky barrier and the metallurgical n-p junction. This can be accomplished by reverse-biasing the n-layer and p-type substrate, with respect to the Schottky electrodes, strongly enough to drain all of the electrons out of the n-layer. The signal charge is to be transported along the buried channel in this depleted condition.

III. ONE DIMENSIONAL STRUCTURE

The band diagram of the one dimensional Schottky barrier buried channel structure is shown in Fig. 1. We define the x-coordinate along the depth of the semiconductor as indicated by a horizontal line in the figure. The n-layer is defined by the condition $0 \leq x \leq X_d$.

The most important expression of interest is the analytic expression of the channel potential ϕ_m in terms of the gate voltage ϕ_G and the signal charge Q . This expression can be derived by the standard depletion approximation for the rectangular charge distribution and is given as

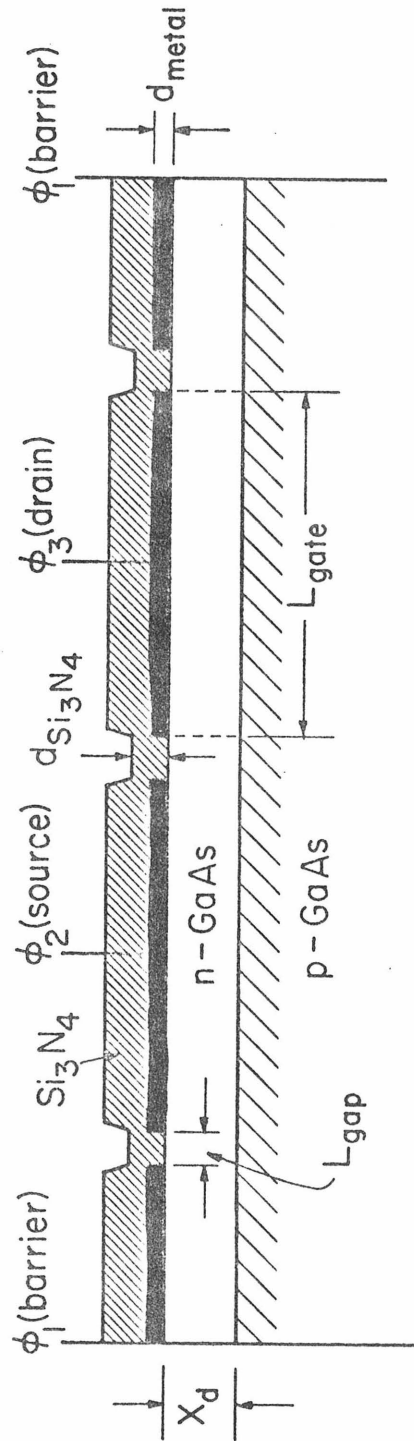


Figure 1 One unit cell of three-phase n-channel Schottky Barrier CCD Structure.

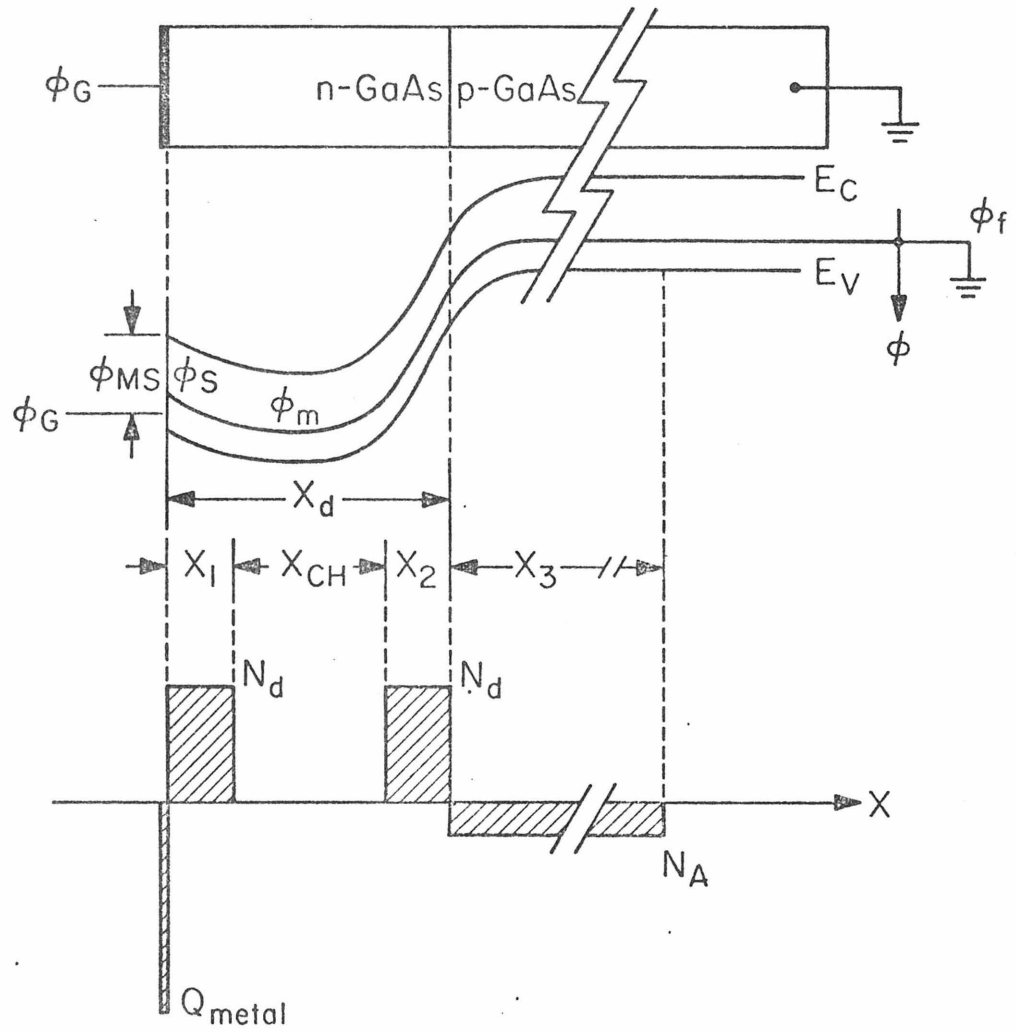


Figure 2 One Dimensional Band Diagram and Charge Distribution for Schottky Barrier p-n junction structure.

$$\phi_m = \left(1 + \frac{N_A}{N_d}\right) (\phi_G - \phi_{MS} + \phi_d) f(R) \quad , \quad (1)$$

where $f(R)$ is a factor of order unity and defined as

$$f(R) = \frac{1}{1 + R + \sqrt{1 + 2R}} \quad , \quad (2a)$$

and the dimensionless parameter is defined by

$$R = \frac{N_d}{2N_A} \left(1 + \frac{\phi_G + \phi_{MS}}{\phi_d}\right) \quad , \quad (2b)$$

with

$$\phi_d = \frac{X_d^2 N_d}{2\epsilon_{\text{GaAs}}} \left(1 - \frac{Q}{Q_d}\right)^2 \quad , \quad (2c)$$

and

$$Q_d = X_d N_d \quad , \quad (2d)$$

The general characteristics of the dependence of the channel potential ϕ_m upon the pertinent device parameters are clear from above relationships. The factor $f(R)$ is a slow varying parameter. Hence one would note from Eq. 6 that the channel potential changes quite linearly with respect to gate voltage ϕ_G but not with the signal charge Q .

IV. TWO DIMENSIONAL ELECTROSTATIC CALCULATION

A solution of two dimensional Poisson equation for this three-phase CCD structure has been solved numerically by over-relaxation method and the computed channel potential is shown in Fig. 3. The solid curve is with silicon nitride deposited by a radio frequency glow

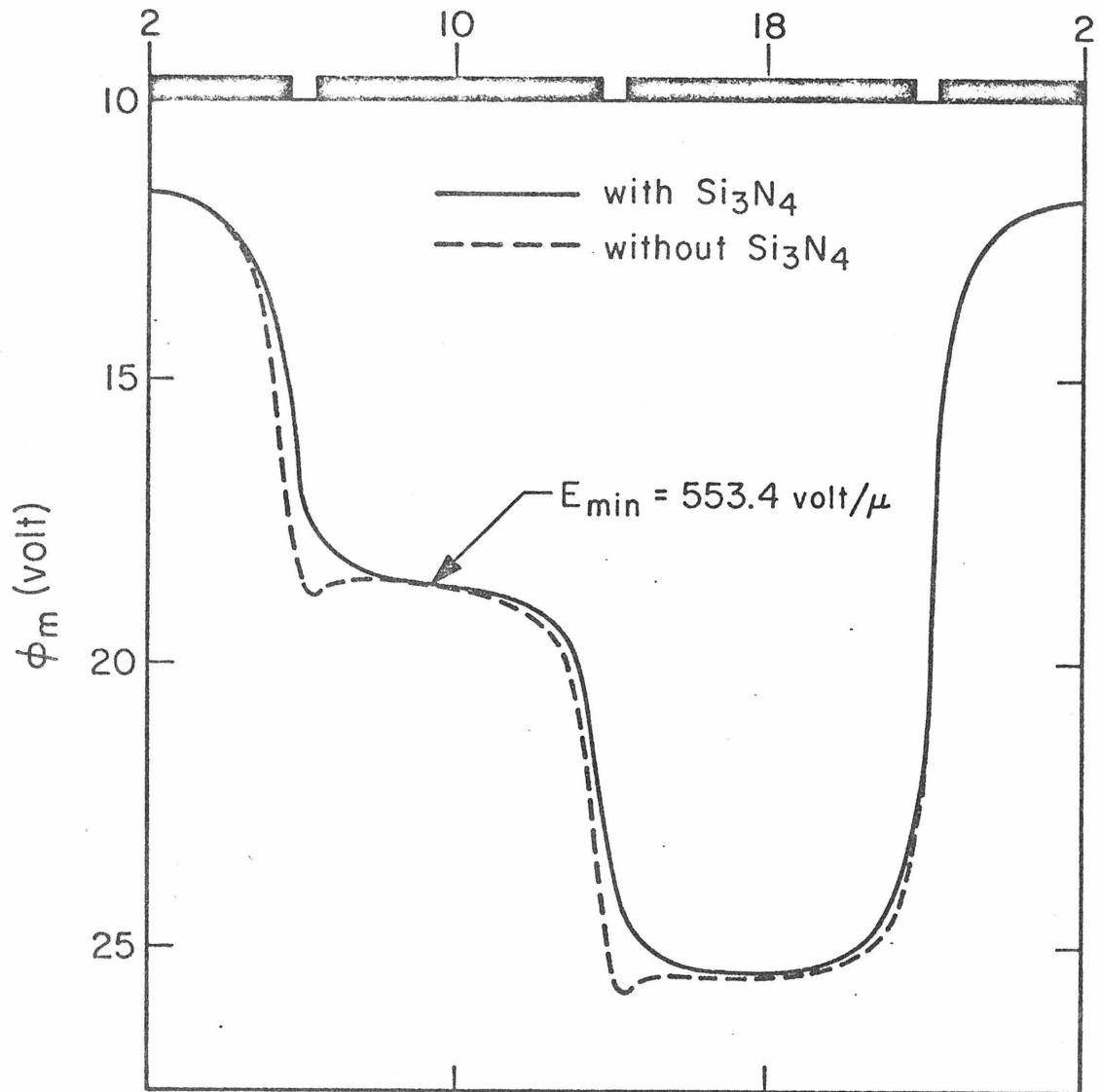


Figure 3 The channel potential profile along the direction of charge transfer. The solid curve is with silicon nitride deposited by a radio frequency glow discharge reaction. The dashed curve is without silicon nitride layer.

discharge reaction. This method is ideal since the resulting dielectric layer has a relatively high dielectric constant of 8. The dashed curve is obtained with no dielectric filling in the interelectrode gaps. The finite interelectrode gaps give rise to the potential minima similar to the results reported for the insulated gate buried channel CCD. The minimum fringing field for the case of silicon nitride deposition was found to be $553.4 \text{ volt}/\mu$. The details of the potential gradient for this situation is illustrated in Fig. 4

The undesirable gap effect can be understood with the aid of Fig. 5 in which we show the electrostatic potential along the distance from the interface to the substrate at the midgap of the source and drain gates. By Gauss's law, the electric field becomes discontinuous at the interface due to the abrupt change in the value of the dielectric constant. Since GaAs has the d-c dielectric constant 12 times larger than that of the vacuum, the surface electric field perpendicular to the interface must be very small inside the semiconductor. This situation is illustrated in the Fig. 5. Note the dashed curve increases its slope abruptly at the interface.

When the silicon nitride is present, the abrupt increase in the potential gradient is negligible at the interface as seen by the silicon nitride to the vacuum. In this calculation the thickness of silicon nitride is taken to be 0.9μ .

In Fig. 6, we have plotted the surface potential along the direction of the charge transfer. The abrupt change in the potential at the interelectrode gaps is obvious from the figure. It would be

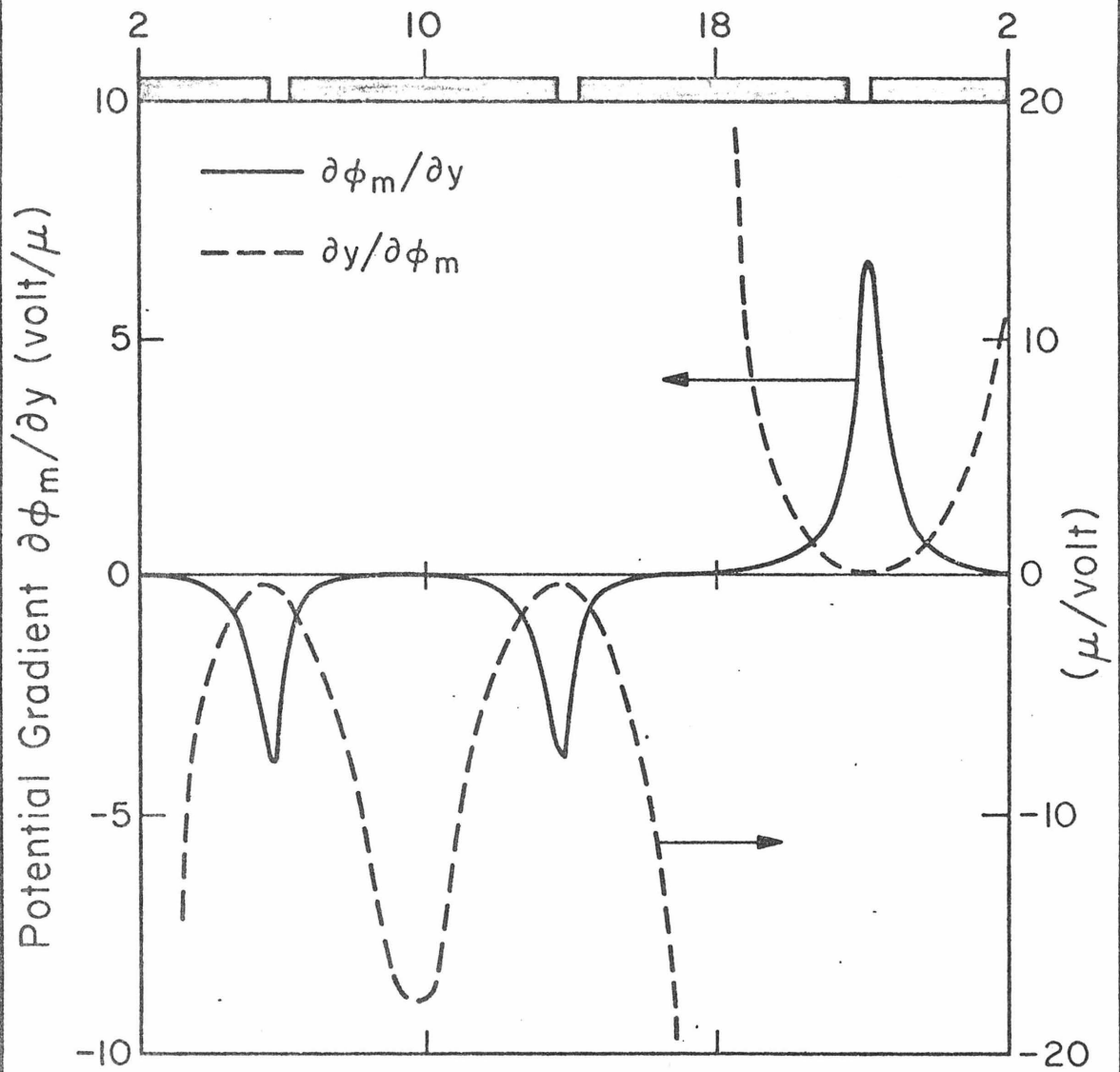


Figure 4 The potential gradient $\partial\phi_m/\partial y$ and its reciprocal $\partial y/\partial\phi_m$ plotted along the direction of charge transfer.

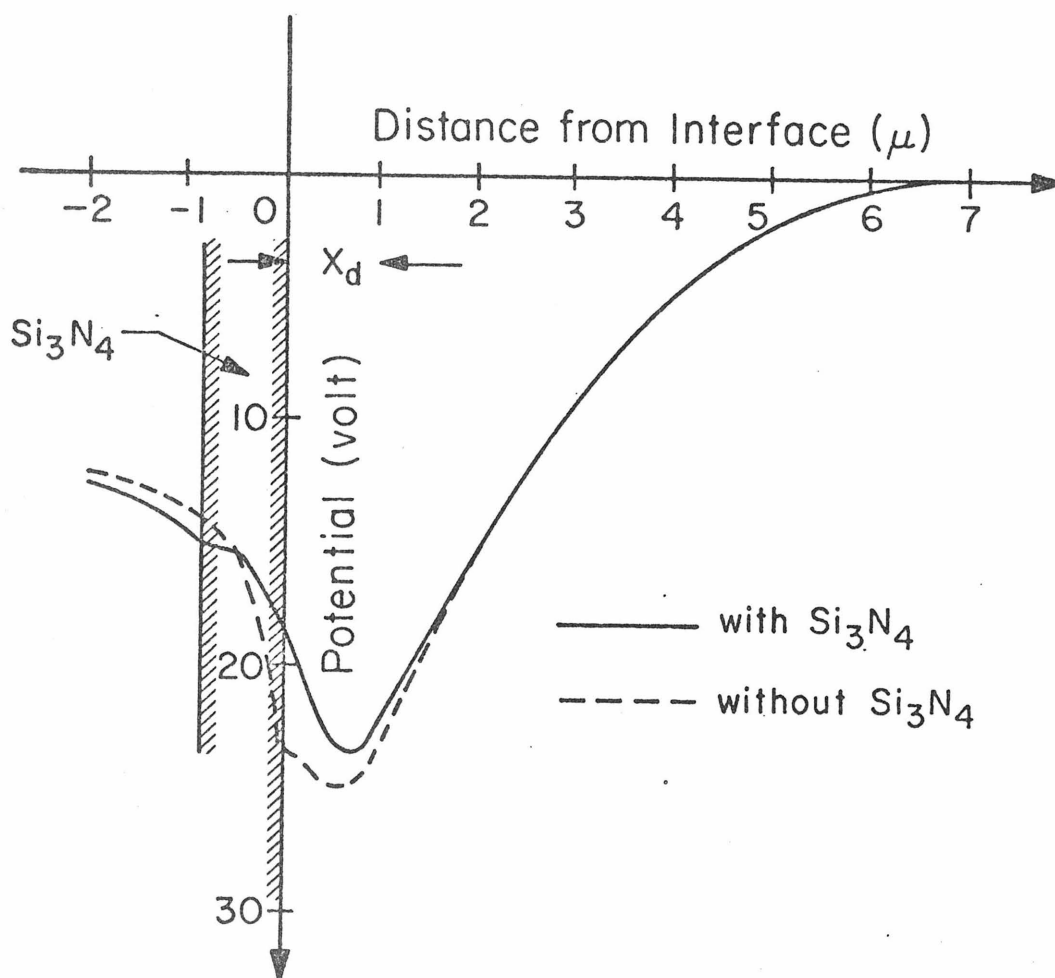


Figure 5 The electrostatic potential profile along the distance from the interface to the substrate is shown at the midgap of the source and drain gates.

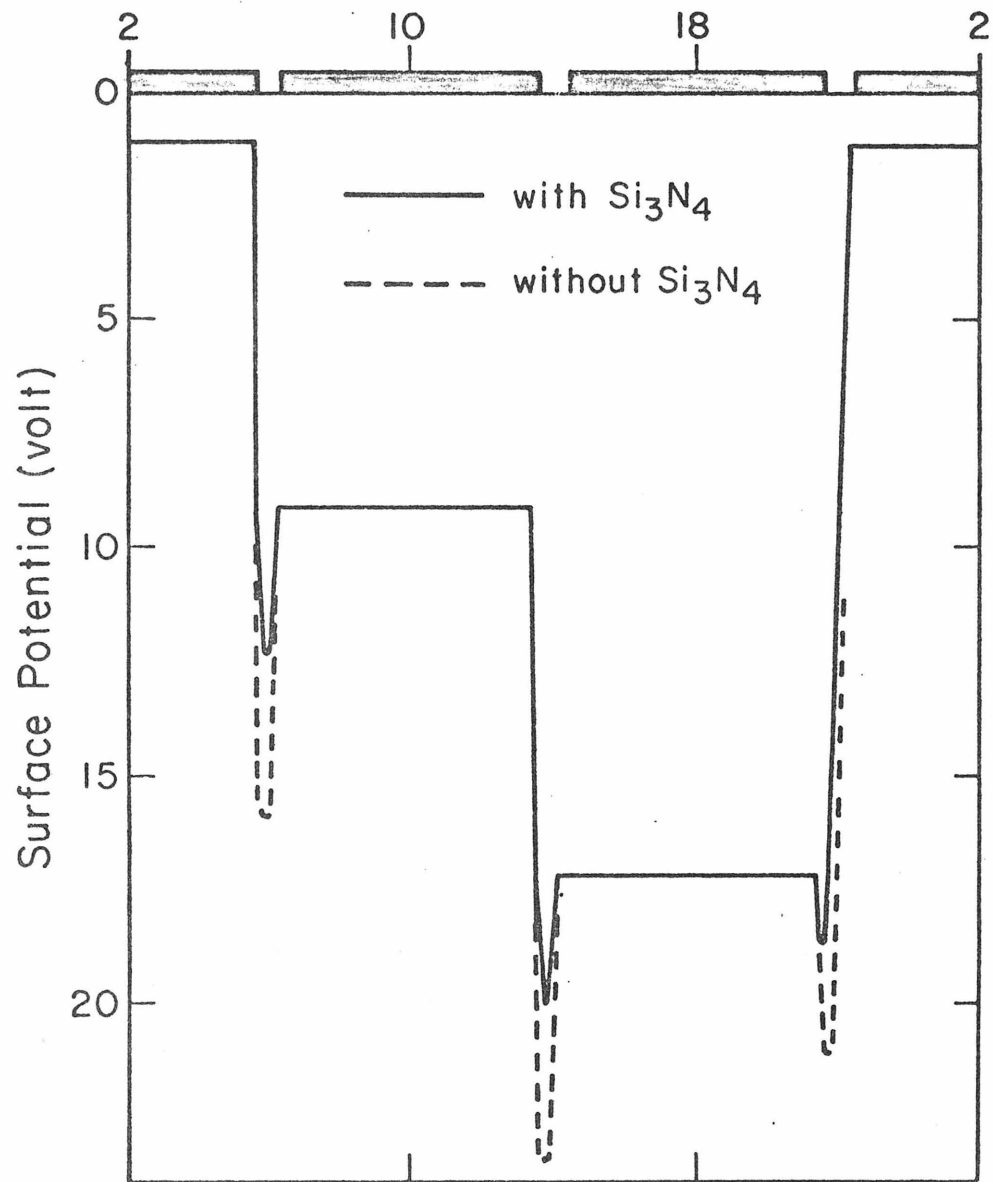


Figure 6 The surface potential profile along the direction of charge transfer. The solid curve is with silicon nitride deposition. The dashed curve is without silicon nitride layer.

desirable, to have the interelectrode potential vary monotonically across the gap; one way to do this would be to let the spacing go to zero. However, in the actual device fabrication, 1μ gap is the narrowest gap one can realize in the present state of art. Fig. 6 shows that the gap effects can be reduced by filling the gap with high dielectric materials for a finite-gap structure.

The device can still be operated if the gap minimum is higher than the channel potential. Fig. 7 shows that this is indeed the case for the conditions we have applied in the calculation. In this figure, we have plotted the surface potential and channel potential in the same graph to illustrate their relative positions.

V. CONCLUSION

A new active semiconductor device, namely Schottky Barrier buried channel CCD is described and some pertinent design considerations are discussed on the basis of the one dimensional electrostatic analysis (depletion approximation) for the minimum channel potential. The two dimensional Poisson equation, appropriate for the structure, has been solved numerically with special attention focussed upon the final gap effect in the three phase structure. And it is concluded that the monotonic channel potential can be achieved by filling the gap with a high dielectric material.

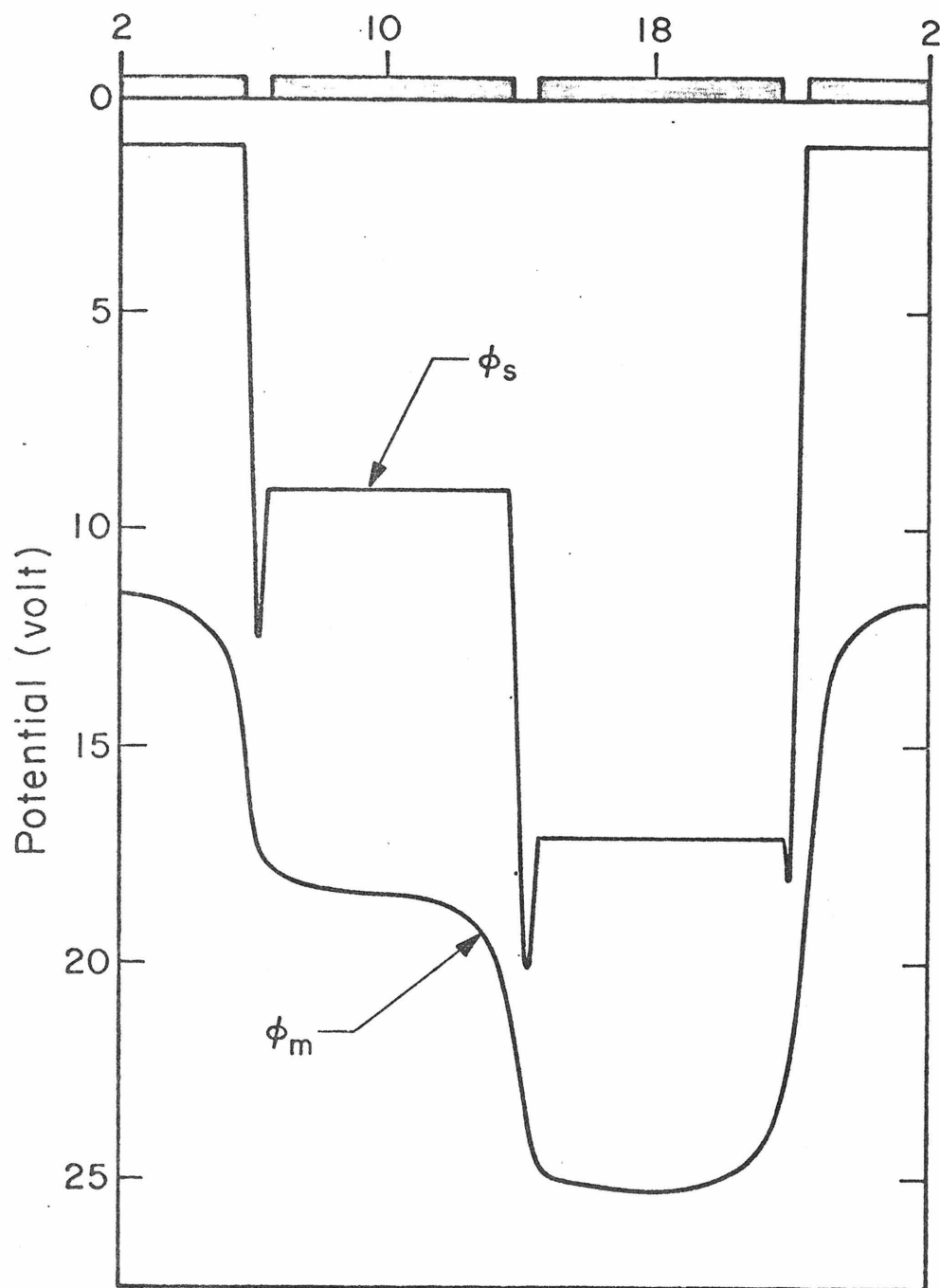


Figure 7 The surface potential and the channel potential along the direction of charge transfer. Both curves were calculated for the case of Si_3N_4 deposition.

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