ELECTRICAL PROPERTIES OF ION IMPLANTED LAYERS IN SILICON AND GALLIUM ARSENIDE

Thesis by

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To my parents

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ABSTRACT

Part I

With the advent of ion implantation, it has become possible to introduce many new dopant species into silicon. The electrical behavior of implanted species displaying deep energy levels was investigated in this work. Hall effect and sheet resistivity measurements were taken as a function of temperature to determine the carrier concentration, mobility, compensation, and impurity ionization energy in the implanted layers. However, since these electrical parameters varied with depth in the samples, conventional Hall effect methods were inadequate. Special differential Hall techniques were developed to characterize the inhomogeneous samples.

The validity of this differential technique was demonstrated by investigating the doping effects of indium in silicon. Differential measurements were first made on samples shallow diffused with indium. Then the results were compared with bulk values that had been obtained in a uniformly doped sample by standard methods. In addition, studies were made on indium implanted silicon to determine the influence of radiation effects. In all three cases an indium acceptor level of 160 meV was observed. Mobility plots versus temperature were also consistent with bulk measurements. However, significant compensation effects were noticed in the implanted layers.

With the analysis technique experimentally confirmed, the electrical behavior of tellurium implanted silicon was investigated.

Samples were implanted with several doses to study the electrical activity as a function of impurity concentration. Isothermal anneal cycles were performed to determine the anneal temperature necessary to attain peak electrical activity. After anneal, differential Hall measurements were made from 100° to 278°K to characterize the implanted layers. Tellurium was found to behave as a donor with an energy level of 140 meV in ion implanted silicon. For room temperature electron densities above 10^{17} carriers/cm^3, the ionization energy was observed to decrease. In conjunction with this decrease, the doping efficiency of ion implanted tellurium was also observed to decrease for concentrations in excess of $10^{17}/cm^3$. Both of these effects were attributed to the influence of energy level broadening.

Part II

Ion implantation was investigated as a doping process for the fabrication of submicron n-type layers in GaAs. Tellurium implantation was performed as a function of dose (3×10^{13} - 1×10^{15} Te/cm^2) and substrate temperature (23°C - 350°C). After implantation, a protective dielectric coating was sputtered on the samples to prevent the GaAs from disassociating during the anneal. The protective qualities of three dielectrics (SiO_2, Si_3N_4, AlN) were compared. Anneal temperatures ranged from 750°C to 950°C. The residual radiation damage and defects in the implanted layers

were studied by photoluminescence and Rutherford backscattering measurements. The electrical characteristics were analyzed by Schottky barrier capacitance-voltage and Hall effect measurements. Sequential Hall measurements in conjunction with layer removal were used to determine the carrier concentration and mobility profiles in the implanted layers. In addition, junction capacitance-voltage and current-voltage measurements were performed to evaluate the quality of implanted diodes.

The samples implanted at room temperature and subsequently annealed with a SiO_2 protective coating displayed almost no electrical activity and had intrinsic regions extending several microns into the GaAs. In contrast, high electrical activity was observed in samples implanted at elevated temperatures followed by anneal with a Si_3N_4 coating. A doping efficiency of 50% was achieved with a carrier density approaching the maximum attainable in tellurium doped GaAs (7×10^{18} electrons/cm^3). However, the electrical activity varied over a wide range for samples with identical implant conditions. This scatter in the electrical measurements was attributed to the poor adherence of the Si_3N_4 layers to the GaAs surface during the anneal.

The maximum electrical activity achieved using an AlN encapsulent was comparable to the value attained using a Si_3N_4 coating. However, the electrical activity was consistently high for the AlN protected samples and the AlN displayed better adherence to the GaAs during anneal than Si_3N_4.

The contents of this thesis have been published under the following titles:

"Lattice Location and Dopant Behavior of Group II and VI Elements Implanted into Silicon," J. Gyulai, O. Meyer, R. D. Pashley and J. W. Mayer, Proc. of 1st Int. Ion Implantation Conf., Rad. Effects 7, 17 (1971).

"Ionization Energy Determination in Indium Implanted Silicon," R. D. Pashley, Proc. 2nd Int. Ion Implantation Conf., Springer-Verlag, New York (1971).

"Electrical Properties of Indium Implanted Silicon," R. D. Pashley, Rad. Effects 11, 1 (1971).

"Investigation of Tellurium Implanted Silicon," F. T. Lee, R. D. Pashley, T. C. McGill and J. W. Mayer, to be published.

"Influence of Implantation Temperature and Surface Protection on Tellurium Implantation in GaAs," J. S. Harris, F. H. Eisen, B. Welch, J. D. Haskell, R. D. Pashley and J. W. Mayer, Appl. Phys. Lett. 21, 601 (1972).

"Properties of Tellurium Implanted Gallium Arsenide," F. H. Eisen,J. S. Harris, B. Welch, R. D. Pashley, D. Sigurd, and J. W. Mayer, Proc. 3rd Int. Ion Implantation Conf., Plenum Press, New York (1973).

"The Fabrication of N-type Layers in GaAs by the Ion Implantation of Tellurium," R. D. Pashley and B. M. Welch, submitted to Solid-St. Electron.

Other publications not associated with this work are listed below:

"128-Bit Multicomparator," C. A. Mead, R. D. Pashley, L. D. Britton, Y. T. Daimon and S. F. Sando, to be published.

"Magnetoelectric Properties of Magnetite Thin Films," J. S.-Y. Feng, R. D. Pashley and M.-A. Nicolet, to be published.

TABLE OF CONTENTS

PART I

ENERGY LEVEL DETERMINATION IN ION IMPLANTED SILICON

Chapter 1

INTRODUCTION

There is considerable interest in understanding the electrical behavior of deep energy levels in silicon.[1] Devices such as photodetectors and thermistors rely on the impurity effects of deep levels. A wide variety of space-charge-limited current phenomena are attributed to the presence of deep levels. Also several undesirable effects (trapping, oscillation, and negative-resistance) have been associated with the presence of these levels.

In the past, investigations have been limited to dopants that could be introduced into silicon by equilibrium techniques. With the development of ion implantation, it has become possible to introduce many new species.

To characterize the doping effect of these new species the carrier concentration, mobility, compensation, and impurity ionization energy should be determined for samples implanted with these dopants. For bulk-doped semiconductors, these quantities can be obtained from simple Hall effect and resistivity measurements taken as a function of temperature. Many investigators have performed similar measurements on implanted samples.[2-9] However, this technique can only be used to give a qualitative picture for implanted layers as the electrical parameters vary as a function of depth in such specimens.

On the other hand, if the measurements are taken in combination with sequential layer removal, bulk values of these parameters can be

determined as a function of depth in the samples. The analysis procedure has been described by Johansson et al.[10] However, the experimental validity of this technique has not been confirmed.

For this reason, we have investigated the doping effects of indium in silicon. The electrical behavior of indium has been well characterized[11-16] in silicon (see Table I). It has a deep acceptor level of approximately 160 meV. Since indium can be added to silicon by equilibrium techniques, a test can be made of the analysis procedure proposed by Johansson et al. Using the proposed technique, energy level determinations were made on samples shallow diffused with indium. For comparison, standard methods were used to measure the ionization energy in silicon bulk-doped with indium.

Once the analysis technique was verified, studies were made on indium implanted silicon to see if the implanted ionization energy was also 160 meV. The mobility and the presence of compensation were also measured in the implanted layers. Comparison was made with the shallow diffused results to see if radiation damage affected the implanted values.

However, to study the dopant behavior in implanted samples, it is necessary to have a large fraction of the implanted species on regular lattice sites and to eliminate compensating effects caused by radiation damage. In the thermal annealing sequences used to reduce the influence of radiation damage, one must consider the possibility that precipitation and outdiffusion effects might occur.[4]

Several of the group II and VI elements have been implanted into silicon.[4] Backscattering measurements were used to study the

TABLE I

Indium in Silicon

Reference	Measured Ionization Energy (meV)	Method
Pokrovskii, et al.[11]	160	Hall
H. Preier [12]	156	Hall
Morin, et al.[13]	160	Hall
Messenger, et al.[14]	153	Hall
R. Newman [15]	160	Optical
Holland, et al.[16]	160	Hall

lattice location of the implanted species as a function of anneal temperature. Most of the implanted species displayed a low substitutional level and outdiffused during the anneal. However, tellurium and selenium maintained high substitutional components (~60% and ~40% respectively) and did not significantly outdiffuse below 800°C.

Initial studies on the electrical behavior of implanted selenium were difficult and led to confusing results. As expected, Se behaved as a donor in silicon. But only low electron densities ($\leq 10^{17}$ electrons/cm^3) could be attained independent of ion dose. Ionization energy measurements were contradictory and may have been influenced by the large amount of electrically inactive selenium present in the implanted layers.

On the other hand, tellurium displayed relatively high doping efficiencies and appeared to have a deep level in silicon. Hence, tellurium was chosen to be the subject of the second energy level investigation in silicon.

The introduction of tellurium into silicon by equilibrium techniques is difficult. Only by careful vapor growth techniques can tellurium doped silicon be prepared.[17] Electrical measurements on such samples indicate tellurium to be donor with an ionization energy of approximately 140 meV.[17]

Ion implantation was used to prepare the tellurium doped specimens for this work. Samples were implanted with doses ranging from 4×10^{12} Te/cm^2 to 1.4×10^{15} Te/cm^2 to study the dose dependence of the electrical activity. Isothermal anneal cycles were performed

to determine the anneal temperatures necessary to attain high doping efficiency. After anneal, the surface carrier concentration and mobility were measured as a function of temperature. Since only qualitative conclusions could be drawn from such data, the tellurium ionization energy was computed from Hall measurements taken as a function of temperature in conjunction with layer removal.

Chapter 2

HALL EFFECT TECHNIQUES

In order for implantation to become useful in device application, the electrical characteristics of implanted layers must be understood. Hall effect and sheet resistivity measurements can be used to determine the number of electrically active centers and carrier mobility. In addition, the impurity ionization energy and the amount of compensation present can be determined by performing these measurements as a function of temperature.

For bulk-doped semiconductors these measurements are simple. However, the fact that implanted layers are thin (often less than 1000Å) with dopant concentrations varying as a function of depth, requires special techniques in making the Hall effect and sheet resistivity measurements. The purpose of this chapter is to describe the special techniques that have been developed for the analysis of implanted layers.

2.1 Surface Hall Effect and Sheet Resistivity Measurements

2.1.1 General Principles

Hall effect and sheet resistivity measurements can be performed using several different techniques and sample configurations.[18] The standard Hall sample is bar shaped and requires a minimum of five electrical contacts. Also, the measurement technique for this configuration requires knowledge of the contact spacing on the sample surface. The most versatile method was introduced by van der Pauw[19] and necessitates only four contacts be made on the periphery of a

sample with uniform thickness. No knowledge is needed of the contact spacing and the sample may take any shape as long as it is singly connected.

The van der Pauw configuration can be conveniently used for measurements on diffused or ion implanted samples. However, care must be taken to isolate the Hall pattern from the bulk of the semiconductor. The necessary electrical isolation can be accomplished either by using a substrate material of very high resistivity or by planar or mesa processing such that a p-n junction isolates the layer of interest.

Planar techniques involving ion implantation through a mask, often result in junctions with a low breakdown voltage. For this reason, mesa processing was chosen to isolate the Hall structures from the substrate material.

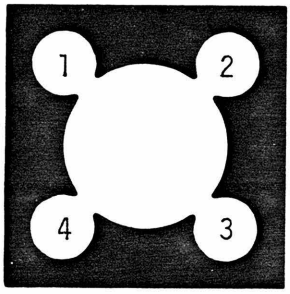


Fig. 1 The van der Pauw pattern used to measure sheet resistivity and Hall effect in this work. The contact regions are numbered clockwise 1 to 4.

Figure 1 shows the van der Pauw pattern used in measuring Hall effect and sheet resistivity in this work. The contact pads are numbered clockwise 1 through 4. To determine the number of carriers, N_s, per cm^2 in a sample, a current I_{13} is passed between two

opposite contacts and a measurement is made of the voltage change ΔV_{24} (the Hall voltage) between the other contacts when a magnetic field B is applied normal to the sample surface.

$$N_s = \frac{B \cdot I_{13}}{\Delta V_{24}} (6.25 \times 10^{10}) \quad , \tag{1}$$

in units of volts, gauss, and amperes.[†] Correspondingly, the sheet resistivity ρ_s is obtained from the potential difference V_{12} between two adjacent contacts generated by passing a current I_{34} between the two remaining contacts.

$$\rho_s = \frac{\pi}{\ell n\ 2} \frac{V_{12}}{I_{34}} \tag{2}$$

Combination of the surface carrier concentration N_s and the sheet resistivity ρ_s yields the effective mobility μ_e.

$$\mu_e = \frac{1}{q\ N_s \rho_s} \quad , \tag{3}$$

where q is the charge on an electron.

If the pattern is not symmetrical, a geometrical correction factor f[19] enters into the relation for the sheet resistivity.

$$\rho_s = \frac{\pi}{2\ \ell n\ 2} (R_1 + R_2) f(R_1/R_2) \quad , \tag{4}$$

[†]The Hall factor $r = \mu_H/\mu_D$, where μ_D is the drift mobility, was assumed to be unity in the absence of more precise data.

where $R_1 = V_{12}/I_{34}$ and $R_2 = V_{14}/I_{23}$. Since a symmetrical pattern was utilized in this work, large deviations in the R values are indicative of a non-uniform layer thickness across the Hall pattern. Hence, to avoid misinterpreting the data, measurements should be performed for all configurations of current path and B-field direction. Averaging of values can be used to reduce the measurement error.

2.1.2 Differential Analysis Procedure

The interpretation of surface Hall effect and sheet resistivity measurements made on diffused or ion implanted samples is complicated because both the carrier density n and the mobility μ vary with depth in the samples. Thus, the surface carrier concentration and the effective mobility are weighted averages.[20]

$$N_s = \frac{\left[\int n(x)\mu(x)dx\right]^2}{\int n(x)\mu(x)^2dx} \tag{5}$$

$$\mu_e = \frac{\int n(x)\mu(x)^2dx}{\int n(x)\mu(x)dx} \tag{6}$$

In a typical sample there is a heavily doped region with low mobility near the surface followed by a tail region with low doping and high mobility. The surface carrier concentration can be twice as large as the actual number of carriers/cm^2 due to the weighting of the higher mobility in tail region. Similarly, the effective

mobility can be much larger than the actual mobility in the heavily doped region.

Hence, if meaningful interpretations are to be made, a method of extracting the carrier density and mobility from surface measurements should be developed. This can be accomplished by combining layer removal techniques with Hall and sheet resistivity measurements. The necessary theoretical relations can be derived from the weighted averages of N_s and μ_e. Equations (5) and (6) involve two integrals. These may be solved for and then differentiated to give

$$n(x)\mu(x)^2 = \frac{d}{dx}\left[N_s\mu_e^2\right] \tag{7}$$

$$n(x)\mu(x) = \frac{d}{dx}\left[N_s\mu_e\right] \tag{8}$$

Solving for $n(x)$ and $\mu(x)$, we get

$$n(x) = \frac{\frac{d}{dx}\left[N_s\mu_e\right]^2}{\frac{d}{dx}\left[N_s\mu_e^2\right]} \tag{9}$$

$$\mu(x) = \frac{\frac{d}{dx}\left[N_s\mu_e^2\right]}{\frac{d}{dx}\left[N_s\mu_e\right]} \tag{10}$$

Experimentally the carrier density and mobility are determined by measuring N_s and μ_e, stripping off a thin layer of material, and repeating the measurement. By repeating this differential measurement many times the carrier density and mobility profiles can be determined in the sample. This procedure for computing bulk values from surface

measurements will be referred to as the differential analysis method.

2.2 Measurements as a Function of Temperature

In studies of implanted dopants, one would like to determine ionization energies and the presence of compensating centers. This information can be obtained by performing differential Hall effect measurements as a function of temperature. This section will describe the analysis procedure for such measurements.

2.2.1 Uniform Doping

Shockley describes the usual procedure for deriving energy levels from Arrhenius plots of carrier concentration versus 1/T for a bulk doped sample.[21] As an example, we will discuss the case of p-type doping with the presence of donor compensation (Fig. 2).

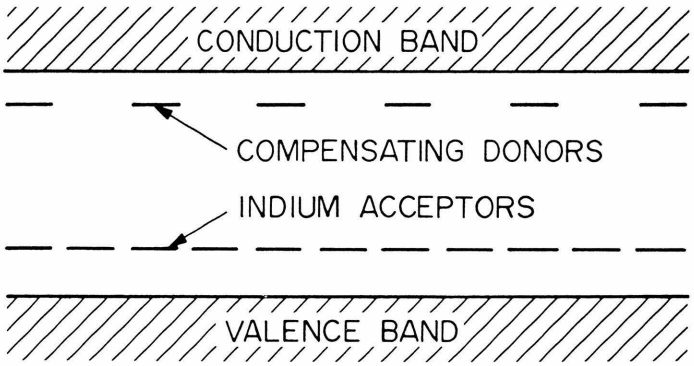


Fig. 2 Energy band diagram for p-type silicon with donor compensation.

For a non-degenerate system, there are two straight line regimes of an Arrhenius plot (considering the 'freeze-out' domains only, see Fig. 3). The upper portion is defined by the charge balance between the free charge carriers p and the ionized acceptors. This non-compensated line has a slope† of

$$\frac{\partial \log p}{\partial (1/T)} = - (2.52)E_A - (.39)T \quad , \tag{11}$$

where E_A is the acceptor ionization energy in meV. The lower portion, commonly referred to as the compensated regime, is determined by the charge balance between the ionized acceptors and the ionized compensating donor centers. Its slope† is given by

$$\frac{\partial \log p}{\partial (1/T)} = - (5.04)E_A - (.78)T \tag{12}$$

The 'knee' in the Arrhenius plot determines the doping level of the compensation (see Fig. 3).

For n-type doping with acceptor compensation the corresponding slope equations are

$$\frac{\partial \log n}{\partial (1/T)} = - (2.52)E_A - (.37)T \quad , \tag{13}$$

for the non-compensated line, and

---

†The correction for the $T^{1.7}$ dependence of N_V, the effective density of states for the valance band, has been included in these relations $N_V \sim m_h^* T^{1.5}$ where $m_h^* \sim T^{0.2}$.

Fig. 3 Theoretical temperature dependence of the carrier concentration for a p-type silicon sample with donor compensation (considering "freeze-out' domains only). Slope analysis of such an Arrhenius plot yields the acceptor ionization energy E_A and the presence of compensating donors ($4 \times 10^{14}/cm^3$ in this case). Numerical values on the axes are for qualitative understanding only.

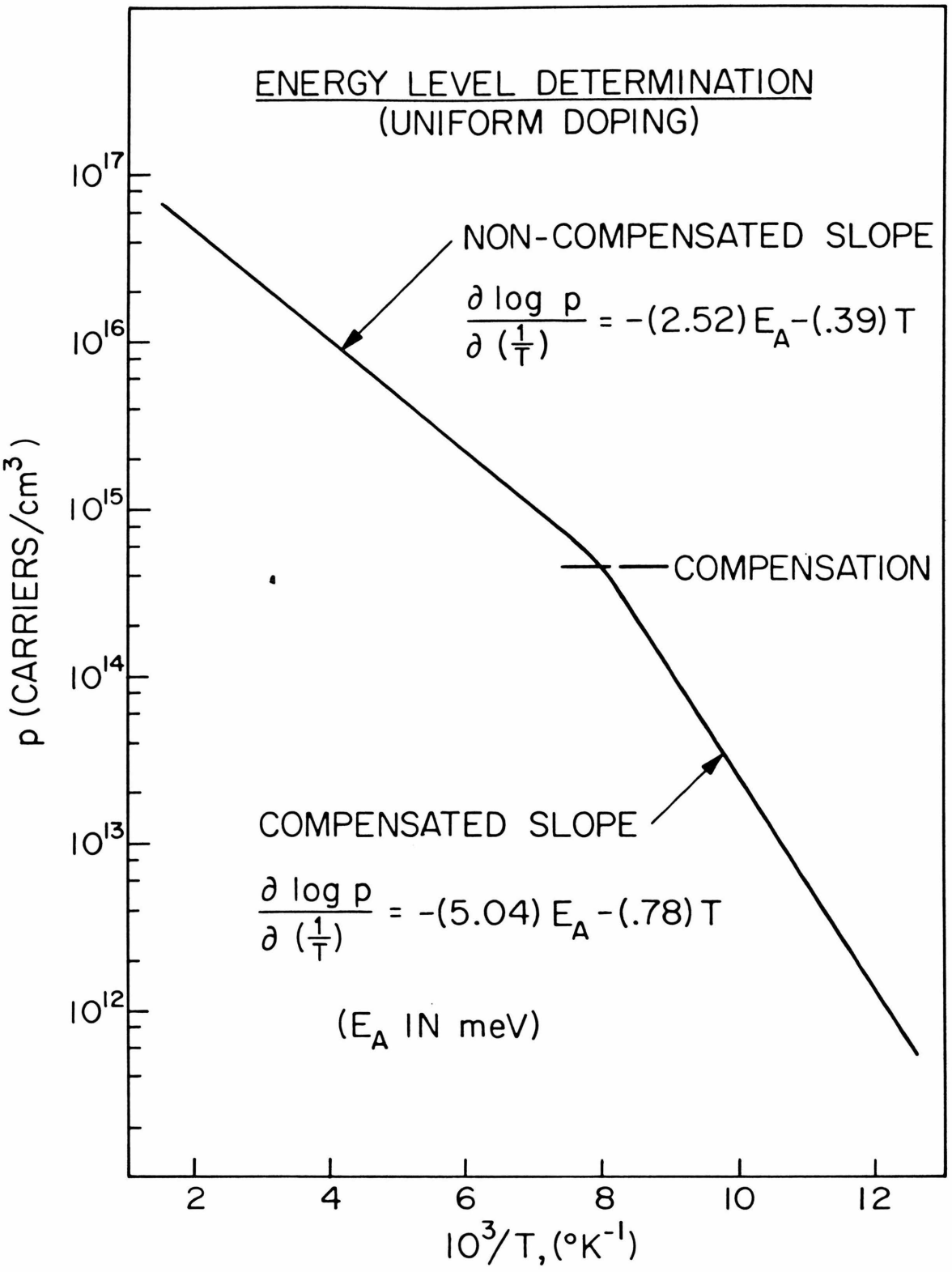

ENERGY LEVEL DETERMINATION
(UNIFORM DOPING)
NON-COMPENSATED SLOPE
$\frac{\partial \log p}{\partial (\frac{1}{T})} = -(2.52) E_A - (.39) T$
COMPENSATION
COMPENSATED SLOPE
$\frac{\partial \log p}{\partial (\frac{1}{T})} = -(5.04) E_A - (.78) T$
(E_A IN meV)
p (CARRIERS/cm^3)
10^{17}
10^{16}
10^{15}
10^{14}
10^{13}
10^{12}
2
4
6
8
10
12
$10^3/T, (°K^{-1})$

Figure 3

$$\frac{\partial \log n}{\partial (1/T)} = - (5.04)E_A - (.73)T \quad , \tag{14}$$

for the compensated line.

2.2.2 Nonuniform Doping

The effect of nonuniform doping and the presence of a compensation profile will be illustrated with the following simple model. First, let us assume that a nonuniform sample can be treated as two layers[5], one containing P_p acceptors/cm^2 with C_p compensating donors/cm^2 and the other P_t acceptors/cm^2 with C_t compensating donors/cm^2 (Fig. 4). Then we may apply the uniform analysis technique to each layer. The Arrhenius plot for the first layer is derived from the temperature dependence of the number of carriers/cm^2, P_{s_p} in the layer. Similarly, the Arrhenius plot for the second layer is produced from the temperature behavior of P_{s_t}. Note that the 'knee' in both curves is determined by the corresponding compensation in each layer (see Fig. 4). Since the layers cannot be physically separated, we are unable to directly measure P_{s_p} and P_{s_t}. As a result, we must interpret surface measurements made on the sample as a whole. Such measurements yield an effective surface carrier concentration P_s which is related to P_{s_p} and P_{s_t} by

$$P_s = \frac{\left[P_{s_p}\mu_p + P_{s_t}\mu_t\right]^2}{\left[P_{s_p}\mu_p^{\,2} + P_{s_t}\mu_t^{\,2}\right]} \quad , \tag{15}$$

where μ_p and μ_t are the carrier mobilities in each layer. However,

Fig. 4 The effect of nonuniform doping and the presence of a compensation profile in a semiconductor is illustrated by a two layer model. The first layer is assumed to contain P_p acceptors/cm^2 with C_p compensating donors/cm^2, while the second P_t acceptors/cm^2 with C_t compensating donors/cm^2 as shown in the insert. The figure shows the temperature dependence of the surface carrier concentration (solid lines) for each layer. Note the sharp compensation 'knee' in each curve. The dashed line represents the temperature dependence of the effective surface carrier concentration P_s obtained from measurements on the combined structure. Obviously, interpretation of an experimental P_s curve is impossible unless the doping and compensation profiles are determined. Numerical values on the axes are for qualitative understanding only.

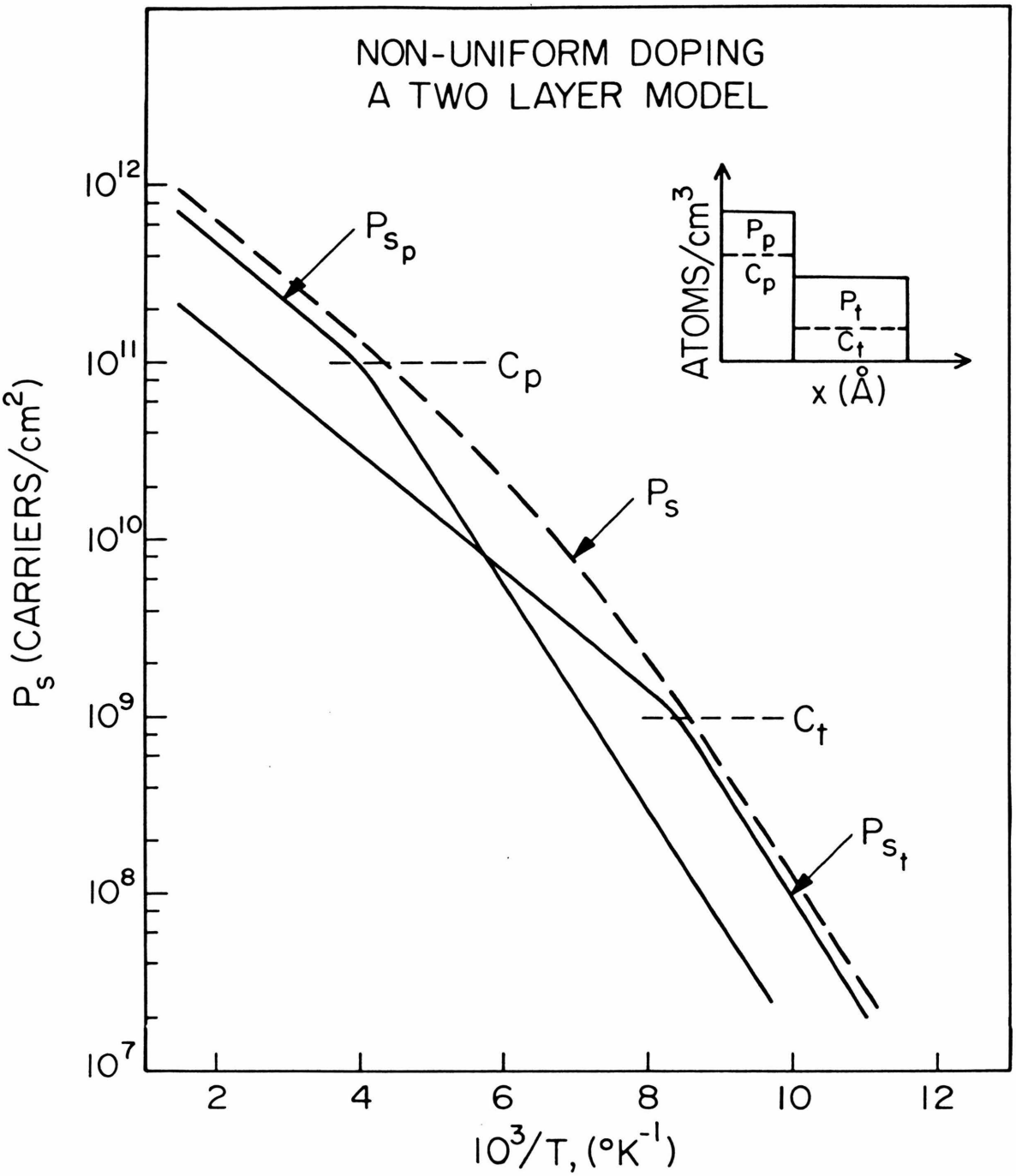

NON-UNIFORM DOPING
A TWO LAYER MODEL
P_s (CARRIERS/cm^2)
10^{12}
10^{11}
10^{10}
10^9
10^8
10^7
P_{s_p}
C_p
P_s
C_t
P_{s_t}
ATOMS/cm^3
P_p
C_p
P_t
C_t
x (Å)
2
4
6
8
10
12
$10^3/T$, ($^\circ K^{-1}$)

Figure 4

we cannot analyze the Arrhenius plot of P_s versus 1/T unless several assumptions are made about the nonuniform sample. For example, models (like this one) must be made of the carrier concentration and mobility profiles.

In order to avoid the difficulties of interpreting plots of effective quantities it is necessary to determine the actual density and mobility distributions for each sample. In the last section, a differential analysis procedure was described for measuring these profiles by performing Hall effect and sheet resistivity measurements as a function of layer removal (stripping). The strips must be made thin enough so that each layer removed can be assumed to have a uniform acceptor concentration and compensation profile (Fig. 5). Knowing the thickness d of a stripped layer, we can determine the number of carriers/cm^3, p, and the carrier mobility μ in the layer.

$$p = \left(\frac{1}{d}\right) \frac{\left[P_{s_1}\mu_1 - P_{s_2}\mu_2\right]^2}{\left[P_{s_1}\mu_1^2 - P_{s_2}\mu_2^2\right]} \tag{16}$$

$$\mu = \frac{\left[P_{s_1}\mu_1^2 - P_{s_2}\mu_2^2\right]}{\left[P_{s_1}\mu_1 - P_{s_2}\mu_2\right]} \tag{17}$$

Here P_{s_1} and μ_1 are the effective surface carrier concentration and mobility measured before layer removal, while P_{s_2} and μ_2 are the corresponding quantities observed after layer removal. However, it is apparent that since the effective quantities will change very

Fig. 5 The differential analysis method for analyzing Hall measurements on nonuniform doped specimens. A typical nonuniform acceptor and compensation profile is shown in the insert. Measurement of the effective surface carrier concentration (dashed lines with values on left axis) and mobility as a function of layer removal allows one to compute the number, p, of carriers/cm^3 and the carrier mobility μ in the stripped layer (see relations given). Slope analysis of the Arrhenius plot of p versus 1/T (solid line with values on right axis) yields the acceptor ionization energy and the number of compensating donors/cm^3 in the removed layer. Numerical values on the axes are for qualitative understanding only.

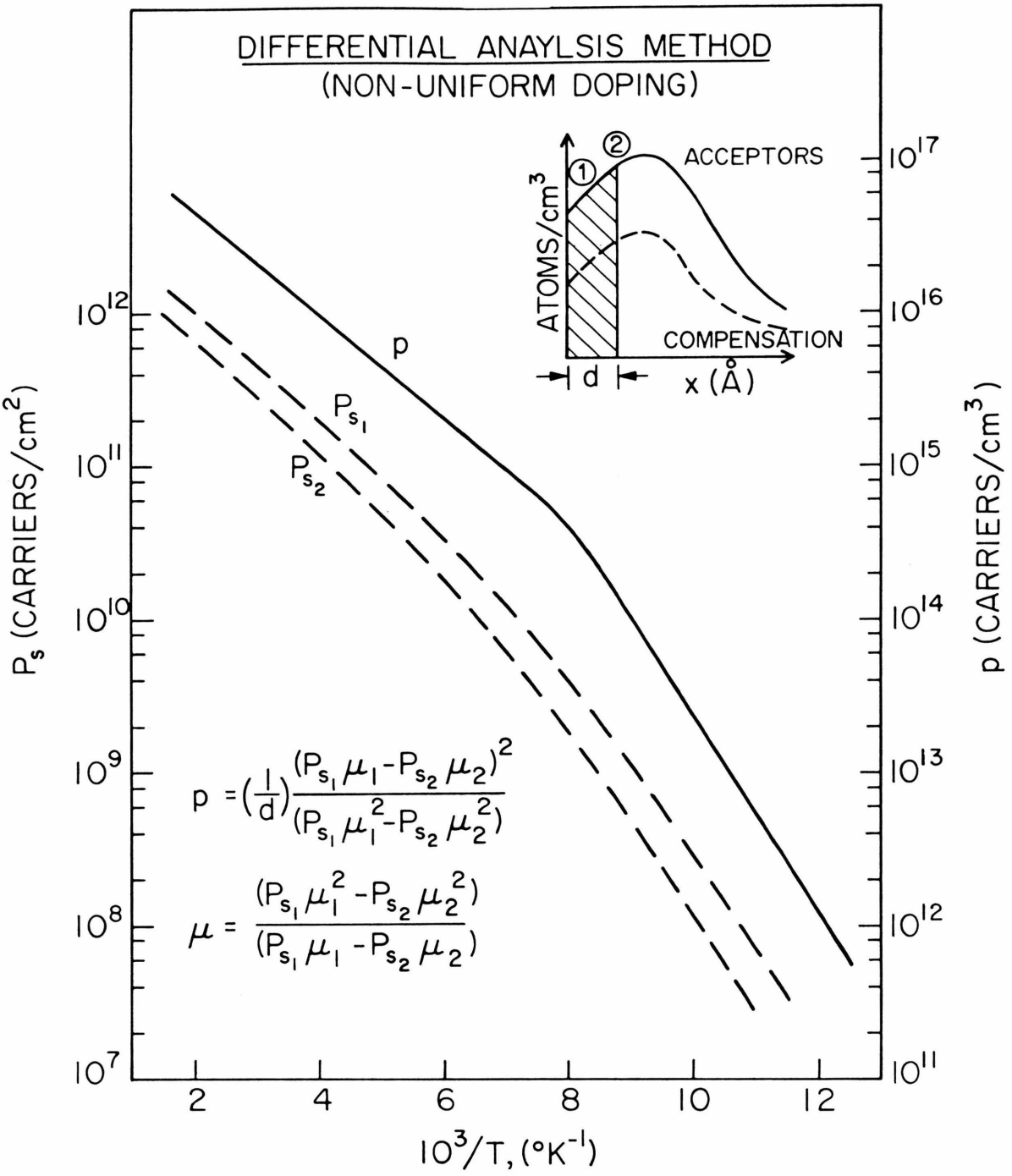

DIFFERENTIAL ANAYLSIS METHOD
(NON-UNIFORM DOPING)
ACCEPTORS
ATOMS/cm3
COMPENSATION
x (Å)
d
p
Ps1
Ps2
Ps (CARRIERS/cm2)
p (CARRIERS/cm3)
10^12
10^11
10^10
10^9
10^8
10^7
10^17
10^16
10^15
10^14
10^13
10^12
10^11
2
4
6
8
10
12
10^3/T, (°K^-1)
p = (1/d) (Ps1 μ1 - Ps2 μ2)^2 / (Ps1 μ1^2 - Ps2 μ2^2)
μ = (Ps1 μ1^2 - Ps2 μ2^2) / (Ps1 μ1 - Ps2 μ2)

Figure 5

little after a given layer removal, small errors in these quantities will result in large errors in the computed layer carrier density and mobility. Hence accuracy is imperative.

If surface measurements are performed as a function of temperature after each layer removal, the above analysis can be used to derive Arrhenius plots of carrier concentration versus 1/T for each layer (see Fig. 5). Thus, we can determine the dopant ionization energy and the number of compensating donors/cm^3 in each layer.

2.3 Experimental Procedure

2.3.1 Implantation and Sample Preparation

The semiconductor substrates used in ion implantation studies should be of high quality with low defect concentration. The presence of electrically inactive impurities and crystallographic defects may influence the behavior of the implanted layer. During sample preparation, it is necessary to heat the implants to high temperatures. As a result, the originally inactive impurities or defects might become electrically active.

The sample preparation prior to ion implantation is vital for the fabrication of uniform implanted layers. Before implantation, the substrate should be thoroughly cleaned (organic scrub followed by a hydrofluoric acid etch) to remove surface impurities. A thin residue left on the sample surface could result in a non-homogeneous implanted region.

The implantation process is discussed in detail by Mayer, et al.[22] In brief, it consists of scanning a narrow beam of high energy ions

across a sample surface. By such methods, ions are implanted into the substrate producing a doped layer that is uniform over a large area.

There are several parameters that can be varied during implantation: implant energy, ion dose, substrate temperature and substrate crystallographic orientation. The implant energy determines the penetration depth of the implanted ions in the substrate. Theory developed by Lindhard, Scharff, and Schiøtt[23] describes the profile of the implanted ions. The profiles are Gaussian with the peak depth and width dependent upon implant energy, ion mass, and substrate mass. Implant energies generally range from 40 to 400 keV producing ion penetration depths from .05μ to 1μ.

The ion dose is a critical parameter in the evaluation of implanted layers. For most investigations, the implant dose is in the region of 10^{12} to 10^{15} ions/cm^2. However, for ionization energy studies, the dose should be low enough so as not to result in energy level broadening. To avoid a reduction in the ionization energy, the maximum doping concentration should be kept below 10^{17} atoms/cm^3 in the implanted layers.

Substrate temperature can strongly influence the electrical activity of the implanted layer. In silicon, hot implantation generally results in lower electrical activity.[22] However, as we will see in Part II of this thesis, hot implantation in GaAs produces much higher electrical activity than room temperature implantation.

The crystallographic orientation of the substrate to the incident ion beam can drastically affect the implant profile. If the beam is aligned with a major crystallographic axis, ions may penetrate 10 times the depth observed in samples with a random orientation.[22] The resulting ion distribution is called a channeled profile. In some cases, the profile almost resembles a step function: a profile much different from the Gaussian observed for implants not aligned (random orientation).

During implantation lattice disorder is created as the implanted ions come to rest in the crystal. In order to characterize the electrical behavior of implanted layers, the crystallinity must be restored. High temperature anneal has been successful at reducing the radiation damage and producing conductive layers. Samples are generally annealed in a quartz tube furnace with a flowing inert gas such as Ar or N_2. However, precautions should be taken to be sure the furnace is not contaminated. Typical implant doses represent less than a monolayer, and hence, contaminants could easily influence the electrical behavior. Samples are usually annealed in the range of 600 to 1000°C for less than 15 minutes.

After anneal, the Hall pattern is defined on the implanted surface. Conventional photoresist and etching techniques were used in this work to fabricate the van der Pauw mesa (see Fig. 1).

2.3.2 Layer Removal Technique

Anodic stripping operations[10] were utilized to remove uniform silicon layers, i.e. silicon dioxide was anodically grown

and then removed by etching. The anodizing was performed in a teflon beaker containing the anodic solution (97% N-methylacetamide, 2% deionized water, and 1% potassium nitrate by weight). The area of the anodic oxide was defined on the sample with a vinyl mask. Care was taken to not etch the contact pads or the channels connecting them with central Hall disk.

The masked sample was then secured below a hole in the bottom of the teflon beaker. The anodization was carried out with a constant current density of 9 ma/cm^2 in the presence of high intensity light. Ellipsometry measurements were used to determine the thickness-voltage dependence. Oxide thicknesses were found to be reproducible to within $\pm$ 5%. The oxide layer was stripped with concentrated hydrofluoric acid (HF). The amount of silicon removed was assumed to be 43% of the anodic oxide thickness. This was verified for thick anodic layers (1550Å) by performing interferometry measurements on the silicon step after oxide removal.[24]

2.3.3 Electrical Measurements

Hall effect and sheet resistivity were measured as a function of temperature using a heat exchange, gas flow liquid nitrogen cryostat. The controller and platinum sensor maintained set temperatures to within $\pm$ .2°K. The Hall electronics has been described in a previous publication.[10] Essentially it contains a constant current generator, an electrometer, and a simple means for choosing contact combinations. To generate the Hall voltage, a 4000G regulated

field electromagnet was employed. Measurements were performed using pressure contacts to the implanted layers. Before each measurement, the pressure contacts were adjusted to achieve ohmic behavior for currents passing through the implanted layer.

2.4 Experimental Considerations

There are several sources for measurement error associated with differential Hall effect analysis. They should all be recognized and attempts made to minimize their effects.

The Hall effect is not the only source of an induced voltage resulting from the application of a magnetic field. Other galvanomagnetic and thermomagnetic effects (Nernst, Righi-Leduc, magnetoresistance, and Ettinghausen effects) exist.[25] However, by using a symmetric van der Pauw pattern and performing Hall measurements for all configurations of current and B-field, these effects can be eliminated.

In general, the Hall voltage is linear in applied magnetic field, but for very small or large B fields, the voltage becomes field independent.[25] The nature of this variation is influenced by the dopant species and its concentration in the sample. As a precaution, the Hall voltage should be measured for several current and B-field values.

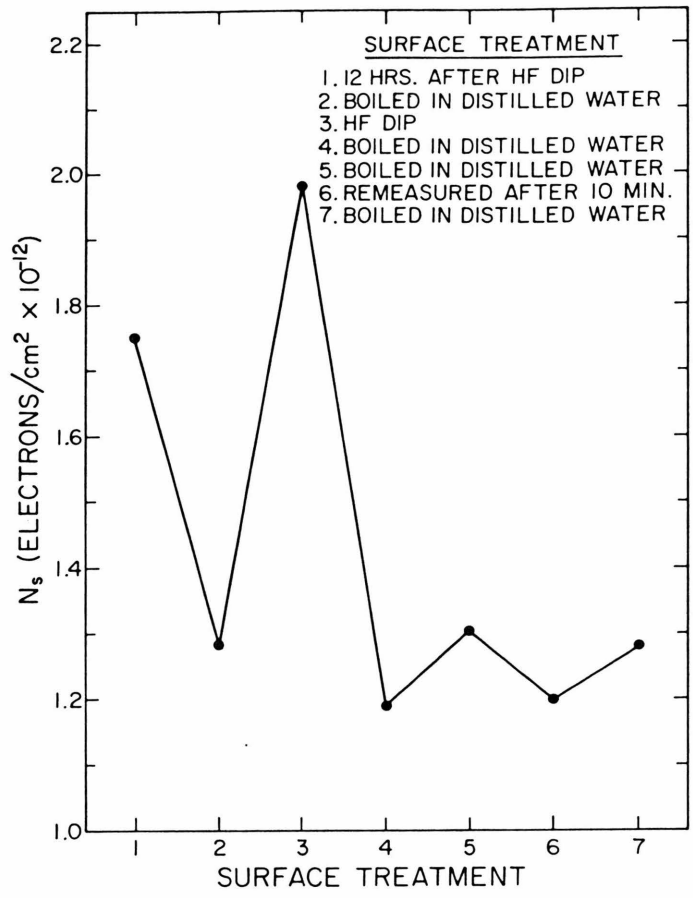
The condition of the sample surface may strongly influence the measurements. Silicon has a surface state concentration of $1 - 5 \times 10^{11}$ states/cm^2.[26] Different surface treatments on implants with low values of N_s can result in large changes in the electrical activity. For

example, a silicon sample implanted with 10^{13} Te/cm^2 and annealed to 800°C had N_s values ranging from 1.2×10^{12} to 2.0×10^{12} electrons/cm^2 depending on surface treatment (See Fig. 6a). The electrical activity was also observed to vary as a function time for this sample (Fig. 6b). Variations like these can be disastrous for differential Hall effect measurements. High energy implants may offer a solution to this problem in that larger doses may be implanted while keeping the volume concentration in the layer below impurity banding values. In cases where low electrical activity is encountered, care should be taken to passivate the sample surface before each measurement. (For example, by leaving the anodic oxide on the sample surface during measurement).

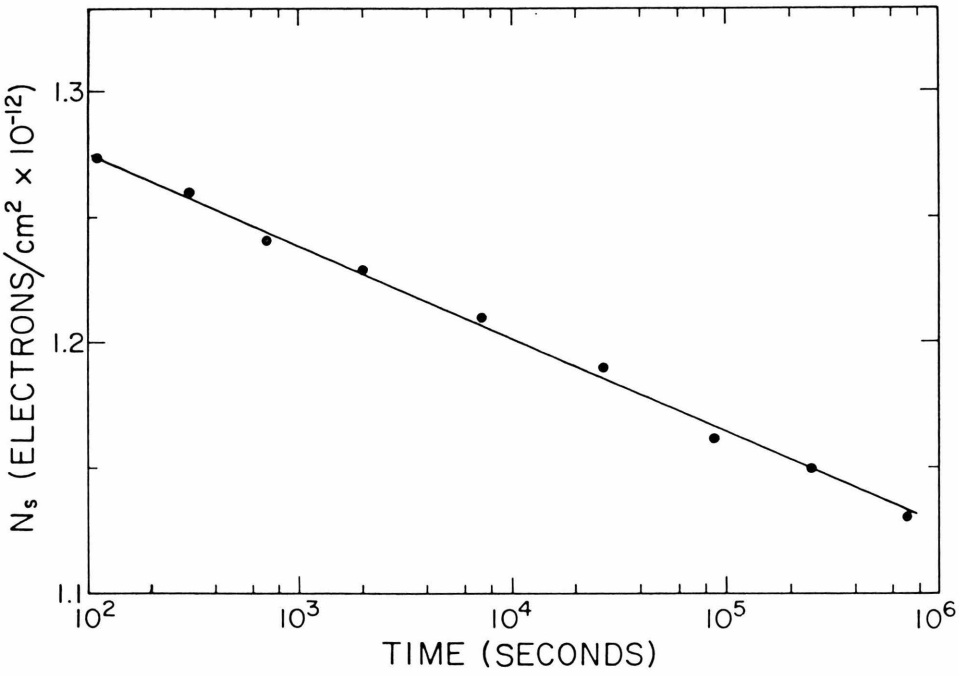
Accurate measurements depend upon having good isolation between the implanted layer and the substrate. Poor etching procedures, mechanical damage, or surface contamination can result in high leakage currents on the periphery of the mesa structure. Physical punch-through of the junction can occur if too much pressure is applied to the contact probes. Also, if alloyed metal films are used for contacts, the isolating junction can be shorted by the penetration of the metal during alloy. Consequently, the isolating junction should always be examined prior to measurement.

Uniform layer removal is essential for the determination of ionization energies in implanted samples. Anodic stripping techniques can be employed to remove uniform layers from a silicon substrate. However, if large anodic sections (> 600Å) are taken, the silicon surface becomes rough and pitted. Figure 7 shows the surface of a

Fig. 6 (a) Influence of surface treatment on the surface carrier concentration for a silicon sample implanted with 10^{13} Te/cm^2; (b) Variation of the surface carrier concentration in this sample as a function of time.


SURFACE TREATMENT
1. 12 HRS. AFTER HF DIP
2. BOILED IN DISTILLED WATER
3. HF DIP
4. BOILED IN DISTILLED WATER
5. BOILED IN DISTILLED WATER
6. REMEASURED AFTER 10 MIN.
7. BOILED IN DISTILLED WATER
N_s (ELECTRONS/cm^2 x 10^{-12})
2.2
2.0
1.8
1.6
1.4
1.2
1.0
1
2
3
4
5
6
7
SURFACE TREATMENT

(a)


N_s (ELECTRONS/cm^2 x 10^{-12})
1.3
1.2
1.1
10^2
10^3
10^4
10^5
10^6
TIME (SECONDS)

(b)

Figure 6

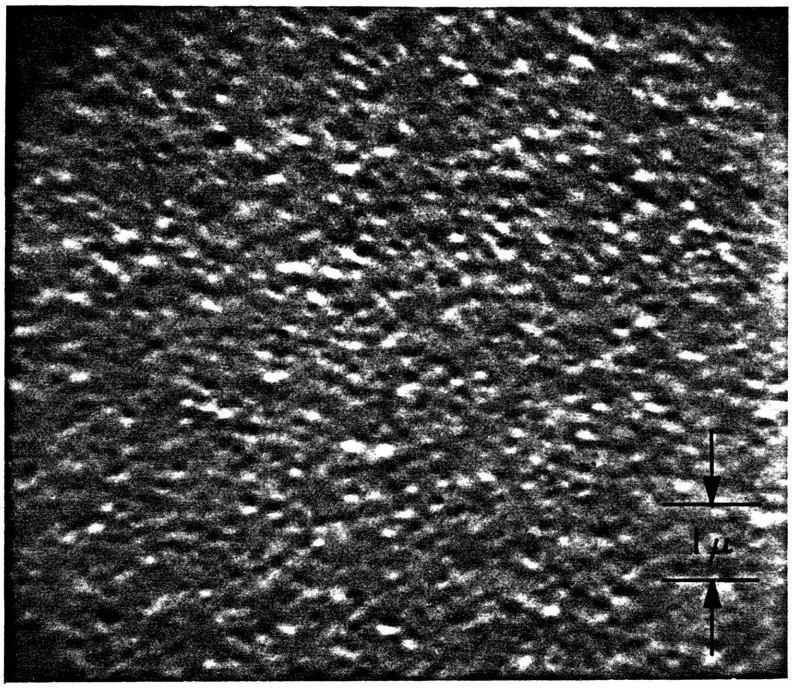


Fig. 7 Scanning electron microscope photograph of the silicon surface after 4500 Å of silicon have been removed by anodic stripping.

sample after 4500Å of silicon have been removed with anodic sections of 600Å or more. Originally, the silicon surface was smooth and featureless. Differential Hall measurements were performed as a function of temperature on this sample. The resulting Arrhenius plots of carrier concentration versus 1/T actually displayed a carrier-type change after several layers had been removed. To avoid such complications, differential Hall measurements should only be performed with anodic sections of 300Å or less.

Chapter 3

INDIUM IMPLANTED SILICON

This chapter deals with the determination of the indium ionization energy and the presence of compensating centers resulting from the implantation of indium into silicon. Care was taken to avoid impurity banding effects by keeping the implant doses low. Also, the samples were fully annealed to reduce the influence of radiation damage. Electrical conductivity and Hall effect were measured from 100° to 278°K as a function of layer removal. For comparison, similar measurements were performed on silicon shallow diffused with indium. This was done to verify the analysis technique proposed by Johansson, et al. In addition, bulk silicon uniformly doped with indium was measured by the conventional Hall method.

Other investigators have studied indium implants. Recently, Gamo et al. verified that the atomic concentration profile of indium implanted into silicon at room temperature obeys the Lindhard-Scharff-Schiøtt (LSS) theory.[27] The anneal behavior of the effective surface carrier concentration was studied by Bergamini et al.[6] A preliminary discussion of the ionization energy of indium implanted into silicon was presented by Johansson et al.[10] Backscattering measurements by Eriksson et al. were used to determine the lattice location of implanted indium as a function of anneal and implant dose.[28] The results and discussions presented in these papers were used to guide the experimental technique of this work.

3.1 Sample Preparation

Implantations of indium were made at energies between 50 and 80 keV into 2000 and 20,000 Ω-cm n-type etch-polished slices of float-zoned silicon. Ion doses ranged from 5×10^{12} to 5×10^{14} ions/cm^2 with the substrates at room temperature (R.T.). (Implantations were performed at the Research Institute for Physics, Stockholm, and the Nuclear Research Center, Karlsruhe.) No deliberate attempt was made to orient the crystal with the incident beam.

The shallow diffused samples were prepared following the technique of Fuller and Ditzenberger.[29] The indium diffusion was conducted at 1100°C for a duration of two hours. The base material was 100 Ω-cm n-type etch-polished, float-zoned silicon.

After the Hall pattern was placed on the implanted specimens, they were annealed at 850°C in a quartz tube furnace with flowing argon. Anneal times were thirty minutes for all implants except the high dose implant (5×10^{14}/cm^2), which was annealed for one hour. Annealing studies have shown that high temperatures ($\sim$850°C) are necessary to obtain the maximum surface carrier concentration P_s for implanted indium.[6,10] Since the supersaturation of indium in silicon can occur during diffusion,[29] the diffused samples were annealed at 900°C for one hour.

The indium doped Si was obtained from High Performance Technology, Inc. The indium concentration was 9×10^{16} atoms/cm^3 as determined by Hall measurements. The base material was high purity float-zoned silicon with less than 10^{12} compensating donors/cm^3.

3.2 Results

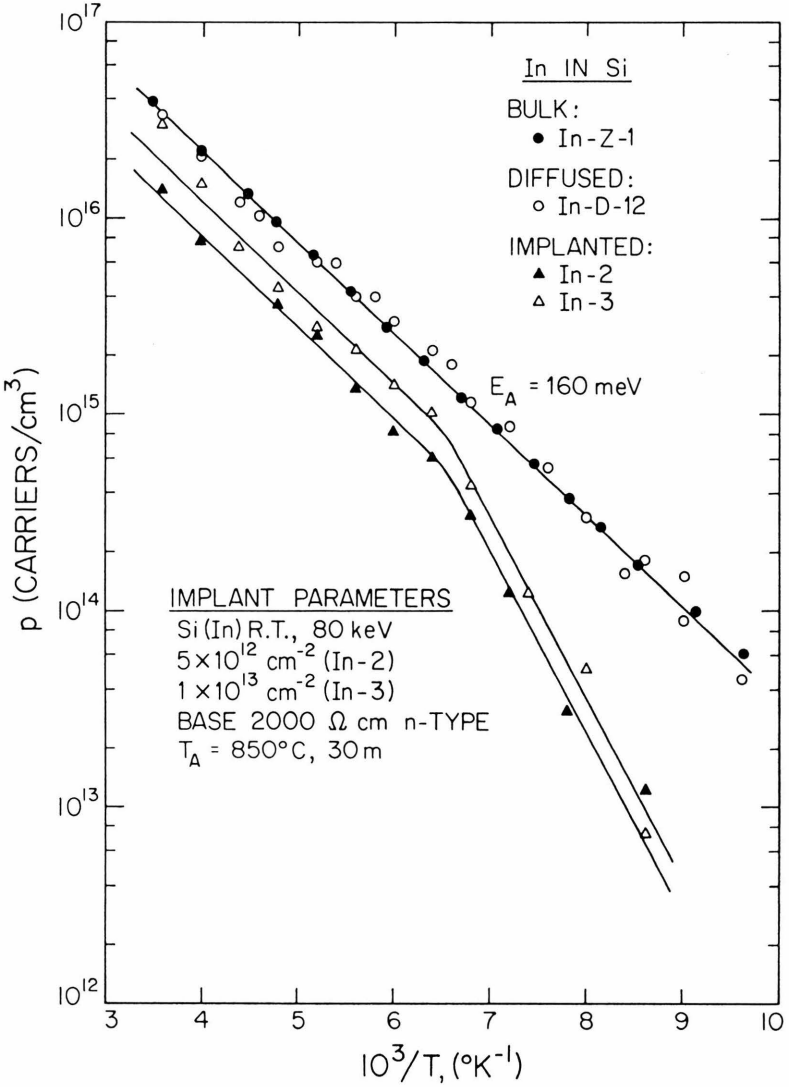
3.2.1 Bulk Doped

The carrier concentration of the bulk doped sample is shown as a function of reciprocal temperature in Fig. 8. The straight line behavior of this Arrhenius plot indicates the presence of a single energy level with no compensating effects. Upon slope analysis, the impurity ionization energy is found to be 160 meV. The sign of the Hall effect implies the impurity is an acceptor. These results are in agreement with those reported elsewhere for indium doped silicon (Table I).

Figure 8 shows the hole mobility as a function temperature. At high temperatures, where lattice scattering predominates, the mobility is measured to be proportional to $T^{-2.4}$. This agrees closely with the measured temperature dependence of the Hall mobility in p-type silicon with similar doping concentrations.[30]

3.2.2 Shallow Diffused

The effective surface carrier concentration P_s for the diffused specimen is presented as a function of temperature in Fig. 9 . The curves correspond to surface measurements taken after successive layer removal steps. It is apparent that no meaningful energy level determinations may be inferred from these Arrhenius plots. This was predicted, as the doping is no longer uniform. However, using the analysis technique discussed in the last chapter , the carrier concentration/cm^3 and mobility can be found in a stripped layer by combining surface measurements before and after layer



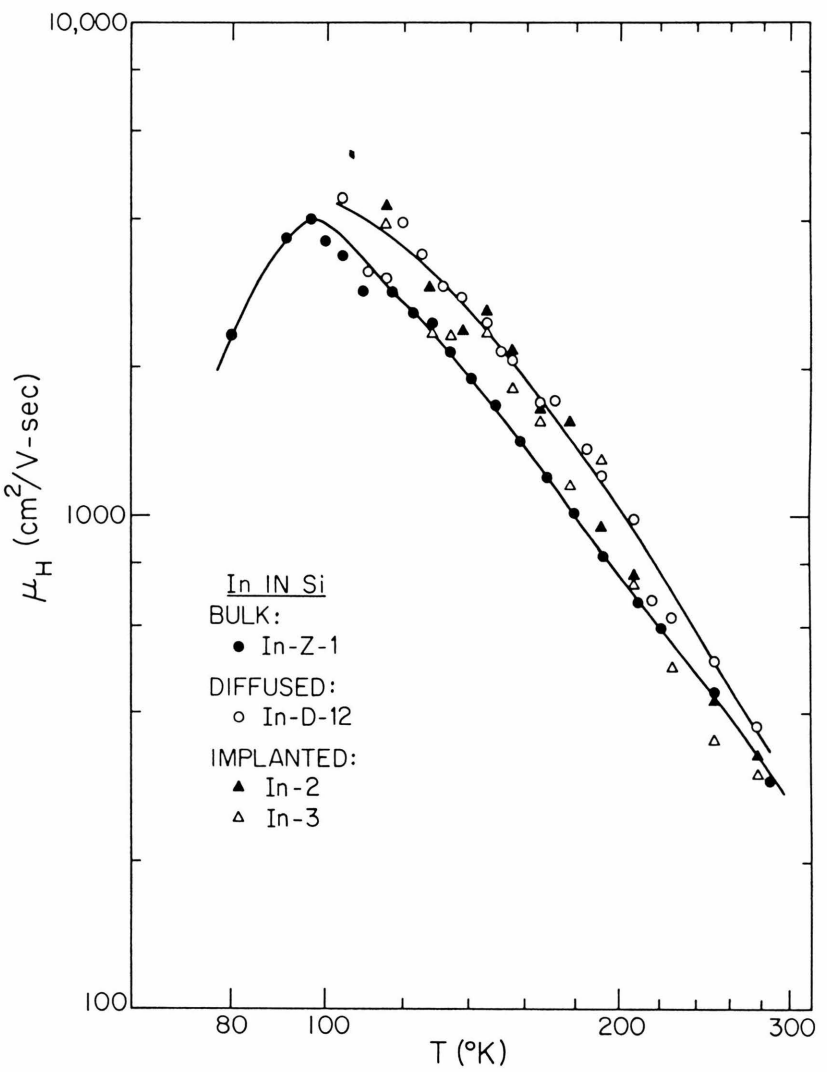


Fig. 8 The temperature dependence of the carrier density and Hall mobility for silicon samples implanted, diffused, and bulk doped with indium.

removal. Figure 9 shows the Arrhenius plots of the carrier concentration /cm^3, p, versus 1/T for the stripped layers. Energy level computations on these curves yield an impurity ionization energy of 160 meV. In addition, the Hall sign is that of an acceptor. These results are consistent with the bulk doping results. Also, the hole mobility in the diffused layers is observed to be in accordance with bulk values (Fig. 8). Hence, the differential analysis technique is an accurate method for analyzing nonuniform samples.

It is interesting to note that the carrier concentration /cm^3 in the second layer is larger than that of the first layer (Fig. 9). In fact, the number† of substitutional indium atoms/cm^3 present in the second layer is $5 \times 10^{18}/cm^3$ compared to $9 \times 10^{16}/cm^3$ for the first layer. Such behavior is not characteristic of diffusion. However, after the sample had been diffused with indium it was annealed. Possibly indium outdiffusion occurred during the anneal. Backenstoss has reported that the solid solubility limit for substitutional indium in silicon is 4×10^{17} atoms/cm^3.(31) Since the indium concentration in the second layer obviously exceeds this limit, solubility driven outdiffusion is indeed very plausible.

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†These values were computed by extending the Arrhenius plot to the high temperature regime where all of the substitutional indium atoms are fully ionized. Only the impurity ionization energy E_A, the valence band effective density of states N_V, and the carrier concentration p, for a given temperature are necessary to determine the impurity's substitutional concentration p°.

$$E_A = \frac{T}{5} (\log N_V - 2 \log p + \log p^\circ)$$

Fig. 9 The temperature dependence of the effective surface carrier concentration P_S is shown as a function of layer removal for the shallow diffused sample In-D-12. The carrier concentration p in the removed layers was computed by differential analysis and is presented as a function of temperature above the P_S plots.

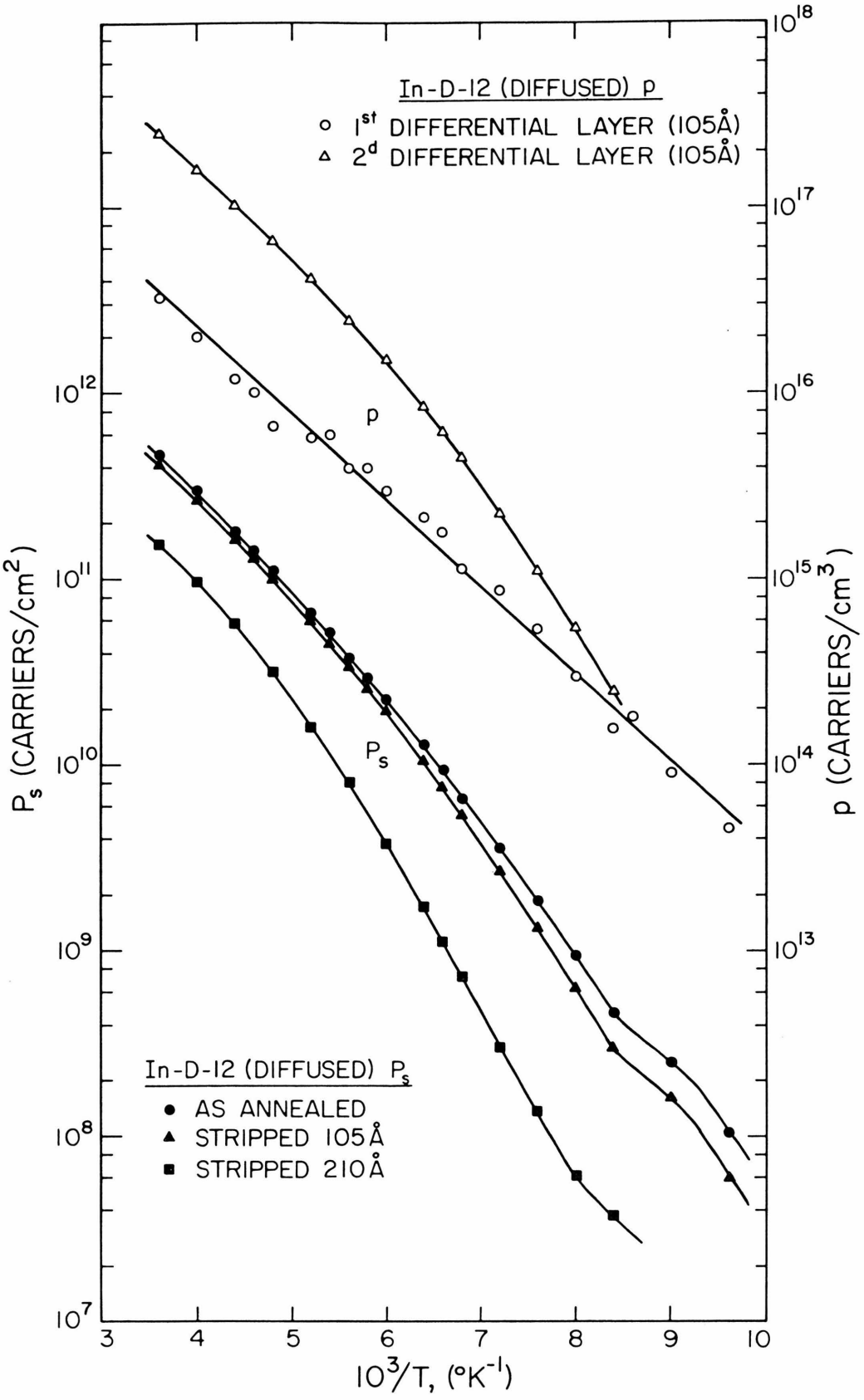

In-D-12 (DIFFUSED) p
1st DIFFERENTIAL LAYER (105Å)
2d DIFFERENTIAL LAYER (105Å)
p
Ps
In-D-12 (DIFFUSED) Ps
AS ANNEALED
STRIPPED 105Å
STRIPPED 210Å
Ps (CARRIERS/cm2)
p (CARRIERS/cm3)
10³/T, (°K⁻¹)
10⁷
10⁸
10⁹
10¹⁰
10¹¹
10¹²
10¹³
10¹⁴
10¹⁵
10¹⁶
10¹⁷
10¹⁸
3
4
5
6
7
8
9
10

Figure 9

Additional evidence for indium supersaturation in the second layer is the high compensation ($\sim 10^{16}$ donors/cm^3) exhibited by the layer's Arrhenius plot. The n-type silicon base material used for the diffusion had a resistivity of 100 Ω-cm. Thus, compensation should be observed at 5×10^{13} donors/cm^3 unless a sizable fraction of the indium atoms are acting as donors. Kaus[32] has proposed that substitutional acceptors behave as donors when they are located interstitially in silicon. One can speculate that the high interstitial indium concentration arises from the motion of indium atoms from substitutional sites to relieve the supersaturated condition of the second layer.

3.2.3 Implanted

In Fig. 10 the directly obtained quantities of effective surface carrier concentration P_s and sheet resistivity ρ_s are plotted as a function of reciprocal temperature for a sample implanted with 1×10^{13} ions/cm^2. The curves correspond to surface measurements taken after successive layer removal steps. As layers are removed, the values of P_s decrease while those of ρ_s increase. These curves are typical for the indium implants that were studied.

To obtain bulk values for the stripped layers, the differential analysis method was used to combine successive sets of surface quantities. Figure 8 shows the Arrhenius plots of the carrier concentration /cm^3 versus 1/T for the initial stripped layer of two implants. For both specimens, the high temperature portion of the Arrhenius plot is parallel to the bulk sample Arrhenius plot. Furthermore,

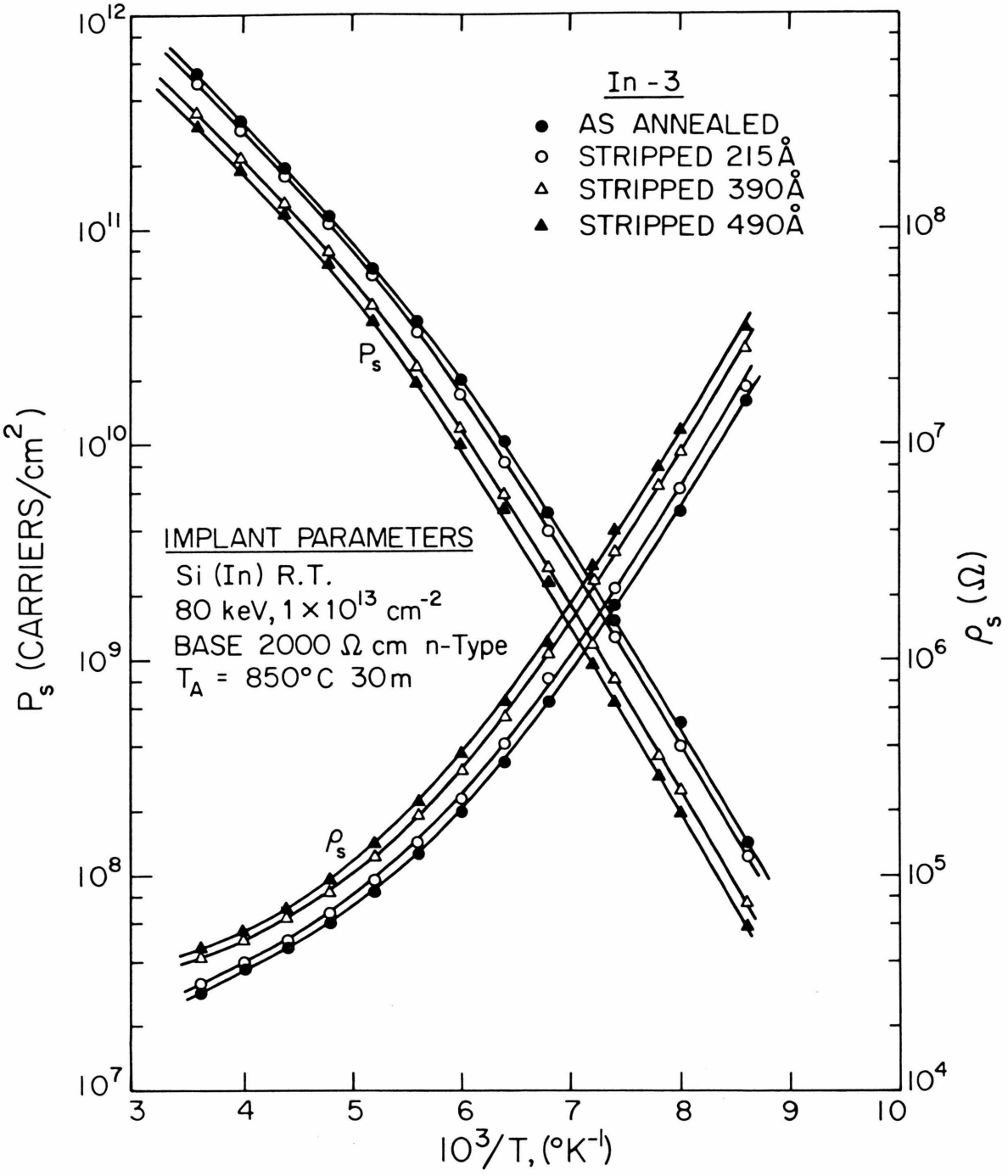


Fig. 10 The temperature dependence of the effective surface carrier concentration P_S and sheet resistivity ρ_S is shown as a function of layer removal for a typical indium implant.

the slope of the low temperature regime is almost double that of the high temperature regime. Such behavior is predicted by slope theory when compensation is present in indium doped silicon. Thus indium implanted in silicon has the same ionization energy as indium doped by equilibrium methods into silicon. However, the implantation of indium seems to introduce significant compensation which does not anneal out of the samples. The temperature dependence of the mobility in these implanted layers is also consistent with the bulk mobility behavior (Fig. 8).

Table II summarizes the electrical properties observed for indium implanted silicon. It is significant that there is a marked difference between implanted indium concentration and the electrically active indium concentration in the stripped layers. It was first thought that the low electrical concentrations were a result of outdiffusion during the annealing. However, Gamo et al. have measured the atomic concentration profiles of implanted indium by means of radioactivation analysis and found that no outdiffusion occurs during annealing.[27] Precipitation must then take place during the annealing. This is supported by the indium solubility work of Backenstoss.[31] At indium concentrations higher than $4 \times 10^{17}/cm^3$, he was able to detect the precipitation of indium by autoradiography and also found that the resistivity became independent of indium concentration in this range. The presence of compensation in the implanted layers is possibly a result of interstitial indium or residual implant damage effects.

TABLE II

Summary of the Electrical Properties of Indium Implanted Silicon

Sample No.[a]	Differential Layer Thickness[b] (Å)	Indium Ionization Energy (meV)	Implanted Indium Concentration[c] (cm^{-3})	Electrically Active Indium Concentration[d] (cm^{-3})	Compensation (cm^{-3})
In-2,(1)	193	160	4×10^{16}	1.5×10^{16}	5×10^{14}
In-2,(2)	135	160[e]	7×10^{17}	4.5×10^{17}	5×10^{15}
In-2,(3)	105	160[e]	1×10^{18}	5.5×10^{17}	5×10^{15}
In-3,(1)	215	160	2×10^{17}	3×10^{16}	8×10^{14}
In-3,(2)	175	160[e]	2×10^{18}	8×10^{17}	1×10^{16}
In-3,(3)	100	160[e]	1×10^{18}	2×10^{17}	4×10^{15}
In-5,(1)	215	156	3×10^{19}	8×10^{16}	2×10^{16}

[a] The number in parenthesis refers to the differential layer analyzed (they are numbered sequentially from the surface).

[b] Thickness of stripped layers. Note the mean projected range R_p is 390Å for In-2 and In-3, and 273Å for the In-5.

[c] Based on Gamo, et al.[27] using the implant energy and dose (In-2: 80 keV, $5 \times 10^{12}/cm^2$; In-3: 80 keV, $1 \times 10^{13}/cm^2$; In-5: 50 keV, $5 \times 10^{14}/cm^2$).

[d] Computed by extending the Arrhenius plot to the fully ionized regime (see the section on the diffused sample results).

[e] Energy level determination was complicated as a result of the broad compensation 'knee' in the Arrhenius plot.

3.3 Summary of Results

The validity of the differential analysis technique was experimentally confirmed. Determinations of impurity ionization energy were made in samples with nonuniform doping profiles by performing differential Hall effect measurements as a function of temperature.

Using such a procedure, it was shown that indium has the same ionization energy in silicon independent of doping technique. An energy level of 160 meV was observed for indium implanted, diffused, and bulk doped into silicon. In addition, the hole mobility was found to be proportional to $T^{-2.4}$ in all three cases. Significant compensation was measured in the implanted layers. It was speculated that solubility effects were responsible for the creation of the compensating centers.

CHAPTER 4

TELLURIUM IMPLANTED SILICON

In this chapter the electrical behavior of tellurium implanted silicon is investigated. Samples were implanted over a wide dose range to study the electrical activity as a function of impurity concentration. Isothermal anneal cycles were performed to determine the anneal temperatures necessary to attain peak electrical activity. After anneal, electrical resistivity and Hall effect were measured from 100° to 278°K as a function of layer removal. Arrhenius plots produced by these measurements were used to determine the ionization energy of the implanted tellurium.

4.1 Sample Preparation

Implantations of tellurium were made at energies between 100 and 220 keV into etch-polished slices of p-type float-zone silicon; resistivities varied from 10 to 2000 Ω-cm. Ion doses were between 4×10^{12} and 1.4×10^{15} Te/cm^2 with the substrates kept at room temperature. (Implantations were performed at Rockwell International Science Center.) No deliberate attempt was made to orient the crystal with the incident ion beam.

After the van der Pauw patterns were put on the implanted specimens, they were annealed in a quartz furnace with flowing nitrogen. Anneal temperatures ranged from 600 to 1000°C with anneal times of 15 to 30 min.

4.2 Results

4.2.1 Anneal Behavior

Figure 11 shows the anneal behavior of the surface carrier concentration N_s and effective mobility μ_e for samples implanted with varying doses of tellurium. An amorphous layer was formed in the high dose implants and as a result high electrical activity is observed for low anneal temperatures. For the low dose implants, an anneal temperature of 750°C is required before peak values of electrical activity were observed. In both cases, the N_s and μ_e values are fairly constant over the anneal range from 750°C to 900°C. Consequently, samples were annealed between 800 and 900°C for energy level studies. Above 900°C a drop in the electrical activity occurs which may be attributed to tellurium outdiffusion or precipitation.

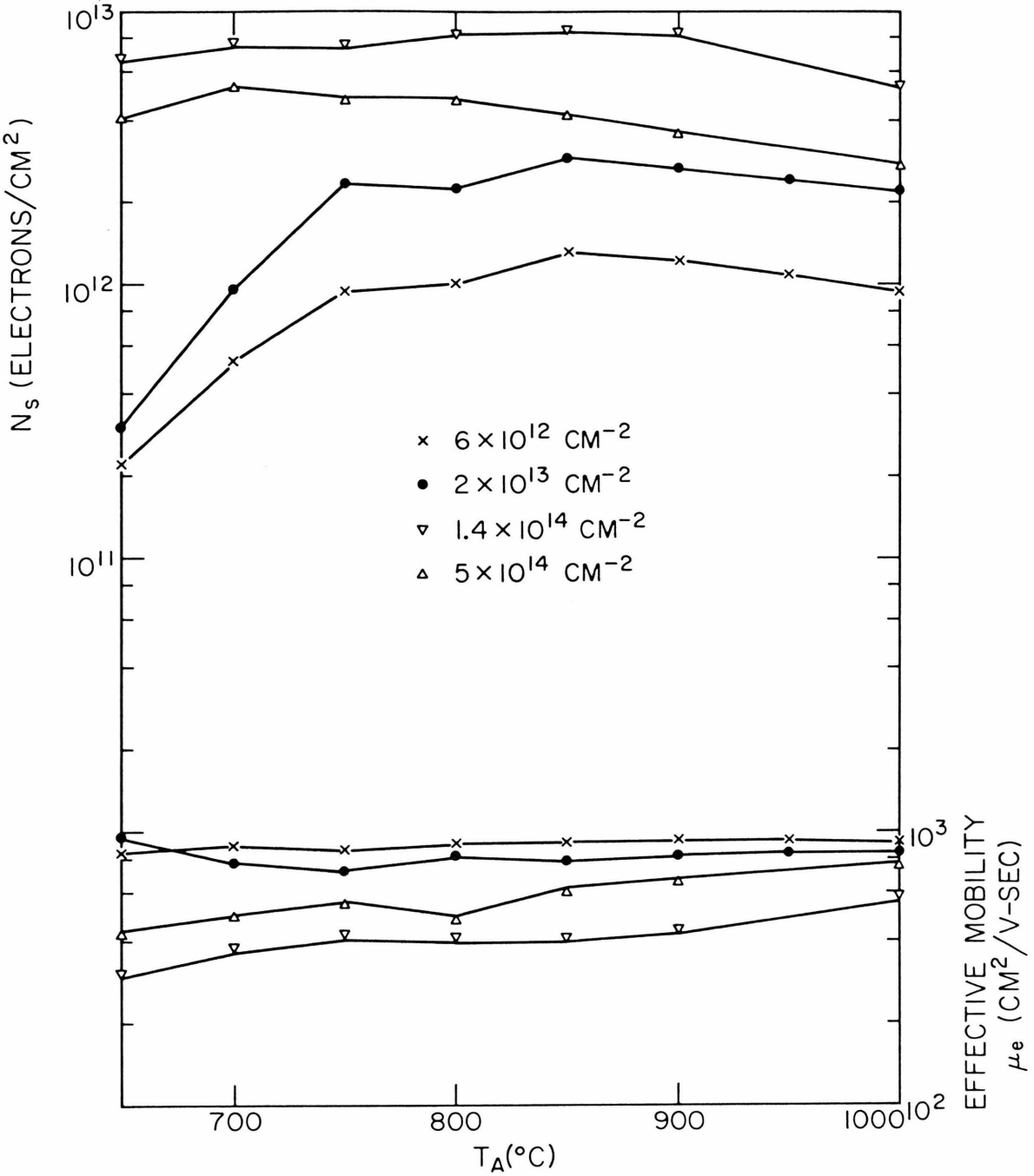


Fig. 11 Anneal behavior of the surface carrier concentration N_s and the effective mobility μ_e for silicon implanted at room temperature with 220 keV Te ions.

4.2.2 Electrical Characteristics

The directly obtained quantities of effective surface concentration and effective mobility are plotted as a function of reciprocal temperature in Fig. 12. As expected, the low dose implants have Arrhenius plots that have steep slopes indicating the presence of a deep level. However, as the dose increases the Arrhenius slope becomes smaller. In fact for the sample implanted with $1.4 \times 10^{15} Te/cm^2$, the electrical activity is almost independent of temperature. This decrease in the Arrhenius slope as a function of ion dose suggests the formation of an impurity band[33].

The effective mobilities behave as one would expect. For the low dose implants the mobility is proportional to $T^{-1.5}$ while for high doses the mobility is much lower and almost independent of temperature.

Since only qualitative observations can be made from these data, differential analysis measurements were performed as a function of temperature to determine the tellurium ionization energy. Figure 13 shows the Arrhenius plots of the carrier density n versus $1/T$ for specimens implanted at several different doses. For the low dose sample (4×10^{12} Te/cm^2), energy level calculations yield an impurity ionization energy of 140 meV. In addition, the Hall sign was that of a donor. These results are consistent with the bulk doping results reported by Fischler.[17]

As the ion dose increases, the ionization energy is observed to decrease. Simple theoretical models cannot explain this decrease. Impurity banding should not occur until much higher electron densities

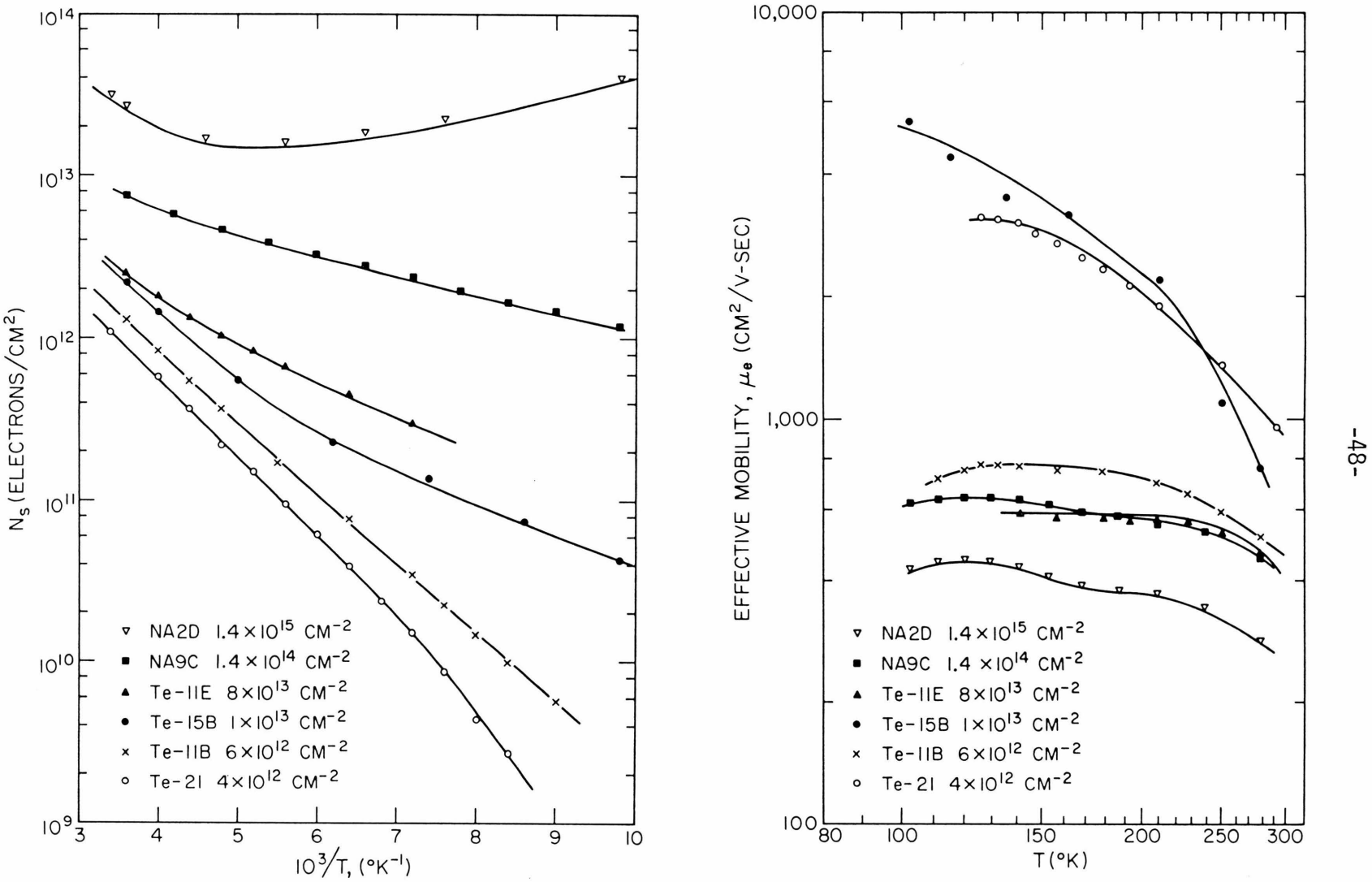


Fig. 12 The temperature dependence of the surface carrier concentration and effective mobility in tellurium implanted silicon.

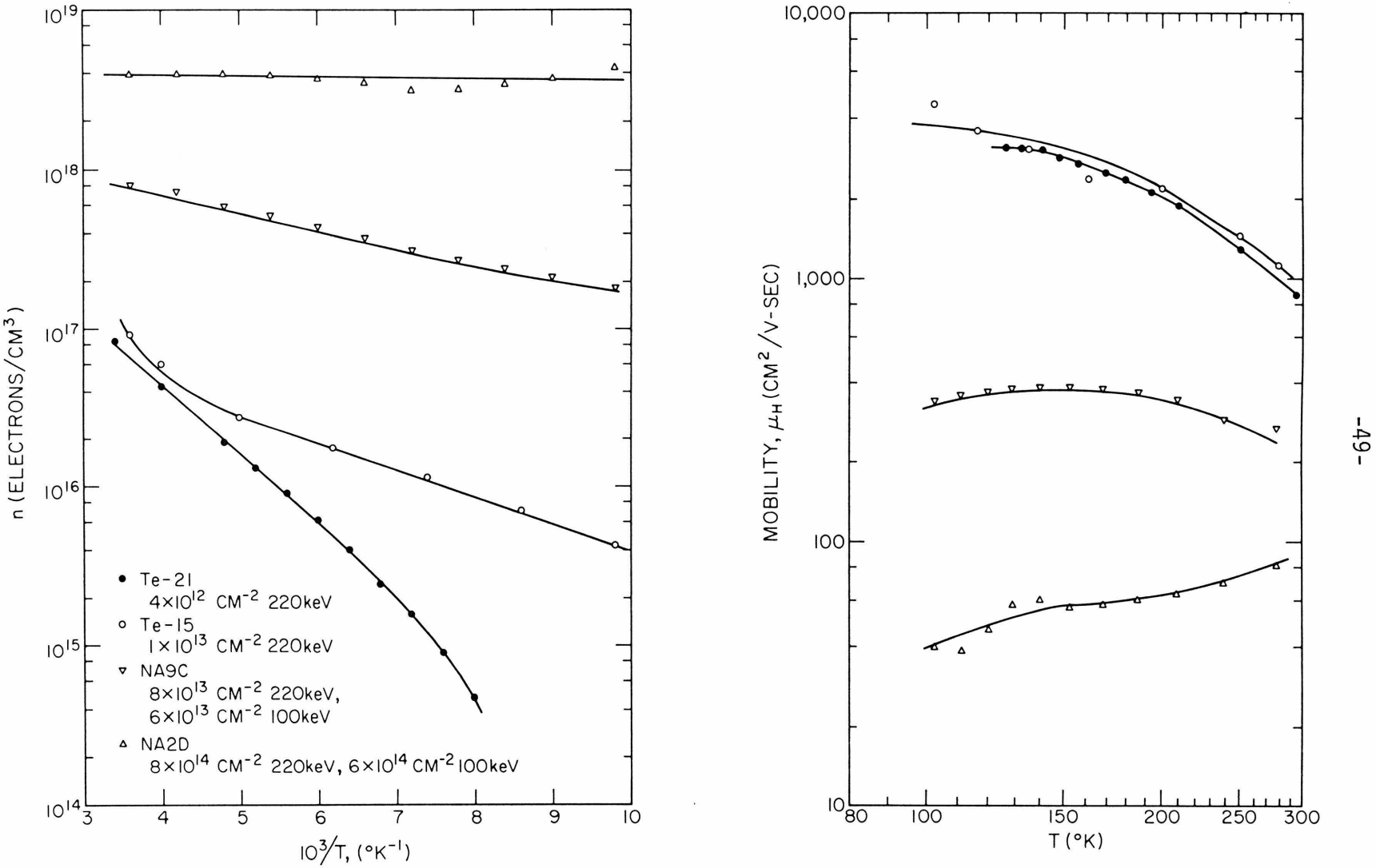


Fig. 13 The temperature dependence of the carrier density and the Hall mobility in tellurium implanted silicon.

for deep levels. Recently, however, F. Lee[34] proposed a theoretical model involving energy level broadening that explains this effect. At impurity concentrations above $5 \times 10^{17}/cm^3$, the impurity level broadens due to the overlap of neighboring impurity potential wells. Fluctuations in these potentials also contribute to this broadening effect and produce a tail on the conduction band density of states. At relatively low impurity concentrations the potential overlapping is small, and therefore band tail formation and impurity level broadening are negligible, i.e. the ionization energy is representative of tellurium energy level. If the impurity concentration is high, the smear of the band edge and the broadening of the impurity level combine to create an apparent reduction in the ionization energy.

The temperature dependence of the mobility in implanted samples is presented in Fig. 13. These curves agree closely with mobility plots for bulk doped silicon[30] of similar carrier concentration (arsenic doping). For samples with a carrier concentration above 1×10^{18} electrons/cm^3 the mobility is low with almost no temperature dependence. The lower doped samples exhibit a temperature dependence characteristic of lattice scattering.

The differential values of electron density at room temperature are plotted as a function of tellurium concentration in Fig. 14. The values of the tellurium concentration were calculated by LSS theory using the implant dose and energy. At concentrations below 10^{17} Te/cm^3 there is a one to one correspondence between the electrical activity and the impurity concentration. However above

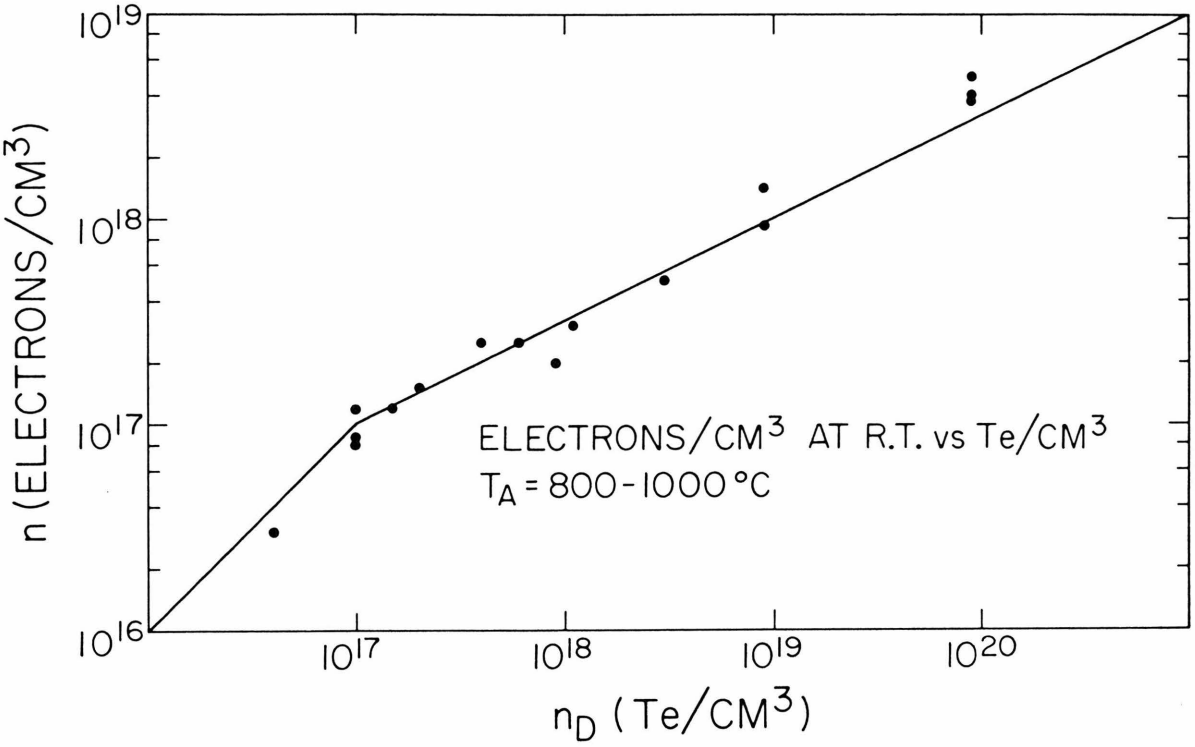


Fig. 14 Electron density at room temperature versus the tellurium concentration in tellurium implanted silicon. The tellurium concentration values were calculated by LSS theory using the implant dose and ion energy.

this tellurium density, the electron concentration only increases as the square root of the impurity concentration. Originally this behavior was thought to be the result of solubility effects. However, the energy level broadening theory also explains this behavior.

4.3 Summary of Results

Tellurium was found to behave as a donor with an energy level of 140 meV in ion implanted silicon. For room temperature electron densities above 10^{17} carriers/cm^3, the ionization energy was observed to decrease. In fact, at a concentration of 4×10^{18} electrons/cm^3 the carrier density became independent of temperature. In conjunction with this decrease in the ionization energy, the doping efficiency of the ion implanted tellurium was observed to fall off for concentrations in excess of 10^{17} Te/cm^3. Both the decrease in the ionization energy and the doping efficiency may be attributed to energy level broadening effects.

The temperature dependence of the mobility was consistent with bulk doped silicon of similar carrier concentration.

Chapter 5

CONCLUSION

The validity of the differential analysis procedure was experimentally established. The indium ionization energy was determined in samples with nonuniform doping profiles by performing differential Hall effect measurements as a function of temperature. An energy level of 160 meV was observed for indium implanted, diffused, and bulk doped into silicon.

By using the differential analysis technique tellurium was found to behave as a donor with an energy level of 140 meV in ion implanted silicon. However, a decrease in both the ionization energy and the doping efficiency was noted for samples with impurity densities above 10^{17} Te/cm^3. These effects were attributed to energy level broadening effects (theory by F. Lee[34]).

The differential layer procedure facilitates the investigation of the electrical properties of dopants that can only be introduced into silicon through implantation. Hence, the properties of several new dopants may be studied. However, care must be taken to avoid impurity banding effects by keeping the implant doses low. For n-type implants, it has been found that surface states tend to influence the electrical measurements when the implanted dose is less than 10^{13} ions/cm^2. High energy implants offer a solution to this problem in that larger doses may be implanted while keeping the volume concentration in the layer below impurity banding values.

In addition, anodic stripping has been found to create pits in

the silicon surface if sections larger than 600Å are taken. The differential analysis procedure relies on the ability to remove uniform layers from a sample surface. Hence, if meaningful measurements are to be taken, layer removal should be performed with anodic sections of 300Å or less.

In light of these difficulties, the differential Hall analysis technique may not be the most ideal method to determine energy levels of ion implanted species. Recently, Fahrner and Goetzberger[35] demonstrated the feasibility of a metal-oxide-silicon (MOS) capacitance technique which greatly simplifies the investigation of deep levels in silicon. It is based on the transformation of bulk levels into surface states which then can be measured by conventional MOS capacitance techniques. The species to be investigated is ion implanted into the Si-SiO_2 interface so that the peak of ion distribution coincides with the interface. The bulk energy level of the species is then reflected as a surface state energy. Using this technique, the energy levels of several impurities were correctly determined.

PART II

THE FABRICATION OF N-TYPE LAYERS IN GaAs BY THE ION IMPLANTATION OF TELLURIUM

Chapter 1

INTRODUCTION

After its initial success in silicon, ion implantation has been considered as a doping process for gallium arsenide. Diffusion of impurities, particularly n-type dopants, in GaAs is difficult to control due to surface deterioration and other problems which arise at diffusion temperatures. Epitaxial methods, while successful, are also hard to control and cannot produce uniform layers less than a few microns in thickness. Ion implantation, on the other hand, promises the accurate control of the doping process and lends itself well to mass production.

Over the past several years, there has been considerable effort devoted to the fabrication of microwave transistors in gallium arsenide. Because of the high electron mobility, GaAs microwave transistors should have cut-off frequencies equal to seven times those of their silicon counterparts. Not long ago, the fabrication of a 50 GHz GaAs Schottky barrier field effect transistor (MESFET) was announced.[36] The device was constructed by epitaxial methods; the channel was 1500Å thick with a carrier concentration of 10^{17} electrons/cm^3. Even though the operation of this device was not optimal, it demonstrated the feasibility of GaAs as a material for the production of microwave transistors. However, unless another method is found to create submicron n-type layers of GaAs, the production costs of GaAs MESFETs may be prohibitive.

The doping of GaAs by ion implantation has been investigated

by several workers.[37-46] The results of the implantation of p-type dopants into GaAs are summarized in Table I. Some of the initial efforts were performed without encapsulating the samples during anneal. The resulting doping efficiency was quite low with 10% efficiency obtained for zinc implants and 2% for cadmium implantation. Coating the samples with a protective layer of SiO_2 before anneal produced almost 100% doping efficiency for Zn, Cd, Mg, and Be implants. Peak carrier concentrations were consistent with those which can be achieved by the introduction of these dopants during the growth process.

However, the carrier concentration profiles were much broader than predicted by LSS theory suggesting the occurrence of enhanced diffusion during the anneal.[42] In addition, for Zn and Cd implantation in n-type substrates, a semi-insulating layer extending several microns in the samples remained after high temperature anneal.[46] The formation of this intrinsic region was attributed to a deep diffusion of compensating defects during implantation or subsequent anneal.

In contrast to p-type implantation, the electron concentrations achieved by implanting n-type dopants have generally been at least an order of magnitude lower than those which can be obtained by doping during growth (see Table II). Most of the investigations were performed by room temperature implantation followed by anneal with a SiO_2 protective coating on the samples. The doping efficiencies were usually less than 10% and the dopant profiles exhibited deep diffusion characteristics. However, in a few instances,

TABLE I

IMPLANTATION IN GaAs

Behavior of p-type Dopants

Dopant	Implant Temperature (°C)	Protective Coating	Anneal Temperature (°C)	Doping Efficiency	Peak Carrier Concentration (cm^{-3})	Reference
Zn	23	Bare	600	~1%	----	37
Zn	23	SiO_2	800	100%	5×10^{19}	38
Cd	500	Base	650	10%	$\sim 10^{19}$	39
Cd	23	SiO_2	800-900	100%	2×10^{19}	40
Mg	23	SiO_2	800-900	100%	2×10^{19}	41
Be	23	SiO_2	600-900	100%	$\sim 10^{19}$	41

TABLE II

IMPLANTATION IN GaAs

Behavior of n-type Dopants

Dopant	Implant Temperature (°C)	Protective Coating	Anneal Temperature (°C)	Doping Efficiency	Peak Carrier Concentration (cm^{-3})	Reference
S	23	SiO_2	700	6%	2×10^{17}	42
Si	23	SiO_2	700	11%	8×10^{17}	42
Ge	23	SiO_2	700	4%	3×10^{18}	43
Ge	500	SiO_2	700	4%	3×10^{18}	43
Se	23	SiO_2	800	15%	$\sim 10^{18}$	44
Se	500	SiO_2	800	50%	$\sim 10^{19}$	44
Te	23	SiO_2	600	--	------	45
Te	100	SiO_2	600	<1%	6×10^{16}	45
Te	180	SiO_2	600	3%	4×10^{18}	45

the implantation temperature was elevated. Zelevinskaya and Kachurin[43] reported no difference could be detected between germanium room temperature implants and 500°C implants, while Foyt, et al.[44] observed an increase in selenium doping efficiency from 15% to 50% for the same implant temperatures. Bicknell, et al.[45] also observed an increase in doping efficiency as a function of implantation temperature for tellurium implanted GaAs. Furthermore the peak carrier concentrations approached those which can be achieved by doping during growth.

The initial efforts at implanting GaAs indicated that it was necessary to encapsulate the implants during anneal to ensure high doping efficiency. The surface of unprotected samples suffered deterioration as a result of GaAs disassociation at elevated temperatures. In fact, it has been shown that there is a pronounced release of arsenic from implanted surfaces at temperatures as low as 300°C.[47]

For n-type implantation, it was noted that by elevating the implant temperature increased doping efficiencies could be attained. Implant damage studies have shown there is a corresponding decrease in the amount of disorder produced during implantation.[48]

In an effort to obtain better results from the implantation of n-type dopants into GaAs, we have examined the effects of increasing the implant temperature and changing the protective layer used during anneal. We decided to study the effect of varying the implant temperature since initial work[44] indicated that room temperature implantation results in lower electrical activity than hot substrate implantation. Channeling measurements were used to

determine the lattice damage as a function of implant temperature. After implantation, a protective dielectric coating was sputtered on the samples to prevent the GaAs from disassociating during the anneal. In view of the fact that gallium readily diffuses through SiO_2 at typical GaAs anneal temperatures,[49] it became imperative to change the protective coating. The protective qualities of three dielectrics (SiO_2, Si_3N_4, and AlN) were compared. Anneal temperatures ranged from 750°C to 950°C. Since backscattering techniques are not sensitive enough to detect defect concentrations less than $10^{19}/cm^3$ (using double alignment techniques),[50] photoluminescence spectra were taken to indicate relative defect densities in the annealed specimens. The electrical characteristics of the implants were analyzed by Schottky barrier capacitance-voltage and Hall effect measurements. Sequential Hall measurements in conjunction with layer removal (differential Hall measurements) were used to determine the carrier concentration and mobility profiles in the implanted layers. In addition, junction capacitance-voltage and current-voltage measurements were performed to evaluate the quality of implanted diodes. Tellurium was chosen as the implanted dopant so as to facilitate the study of the lattice location and depth distribution of the dopant atoms using helium backscattering techniques.

Chapter 2

EXPERIMENTAL METHOD

2.1 Sample Preparation

Different GaAs substrates were used: boat grown Cr-doped semi-insulating material for measurements by backscattering or Hall effect methods, p-type GaAs for Hall and junction measurements, and n-type epitaxial layers for capacitance-voltage and photoluminescence measurements. The p-type GaAs was cadmium doped and had a measured carrier concentration of 2.3×10^{17} holes/cm^3 with a mobility of 196 cm^2/v-sec. Substrates were first lapped, mechanically polished with an 0.3μ alumina, and then chemi-mechanically polished in a solution consisting of Cabosil, H_2O, and H_2O_2 on a vibratory polisher. Following this, the samples were organically cleaned and etched for one minute in a 3 part H_2SO_4, 1 part H_2O_2 and H_2O solution to remove work damage.

The implant procedure is illustrated in Fig. 1. Implantations* of 220 keV tellurium were performed with the incident beam at least 10° from any low index axis. Ion doses ranged from 3×10^{13} to 1×10^{15} Te/cm^2 with the substrates at temperatures varying from room temperature to 350°C. In some cases, an additional implant was made at 60 keV with a dose one-third the 220 keV dose.

After implantation, 2000-4000 Å of dielectric (SiO_2, Si_3N_4, or AlN) was deposited* on the samples by sputtering or plasma vapor

*Implantation and dielectric deposition were performed at the Rockwell International Science Center.

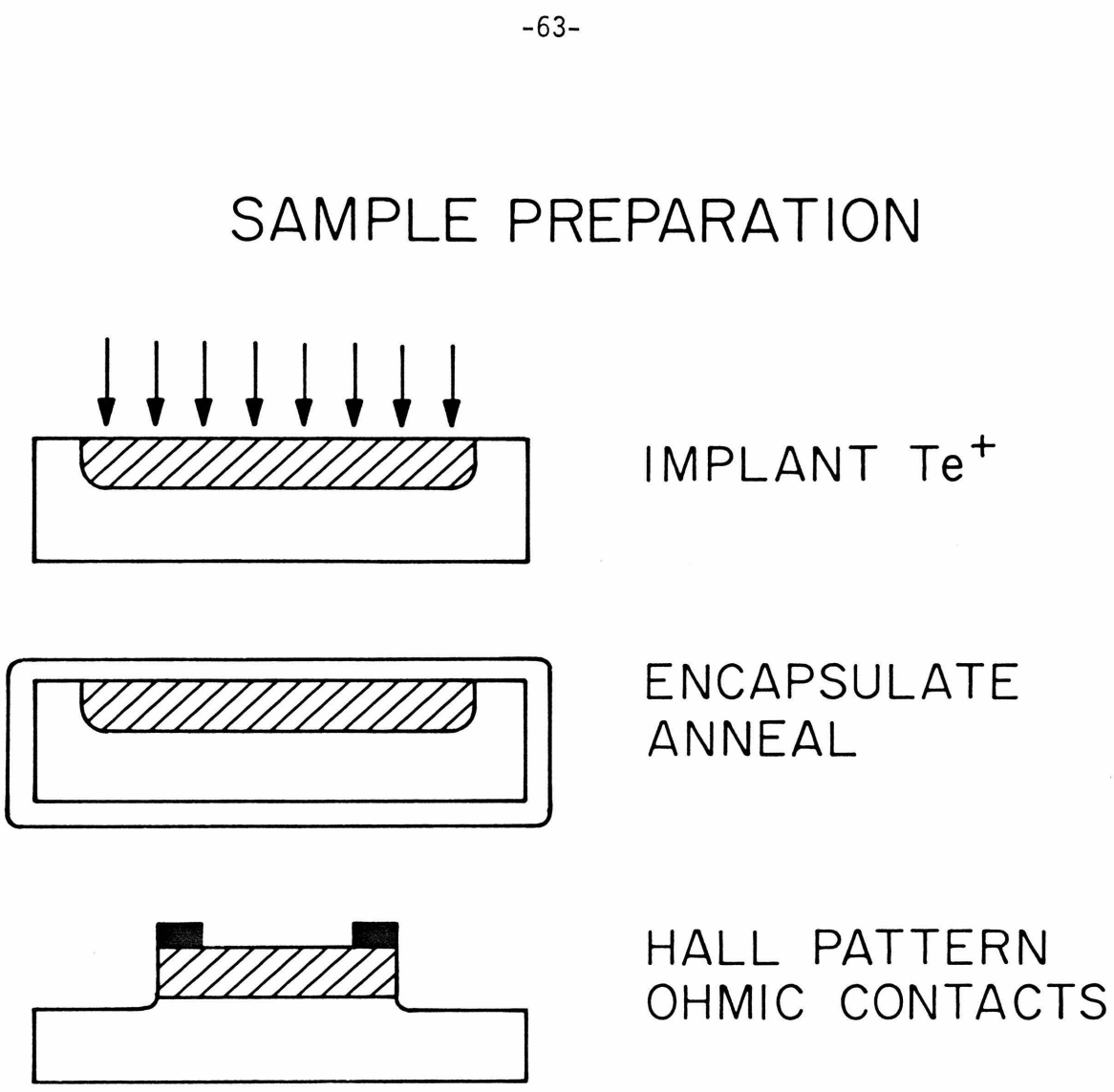


Fig. 1 The three basic steps of the sample preparation procedure are illustrated.

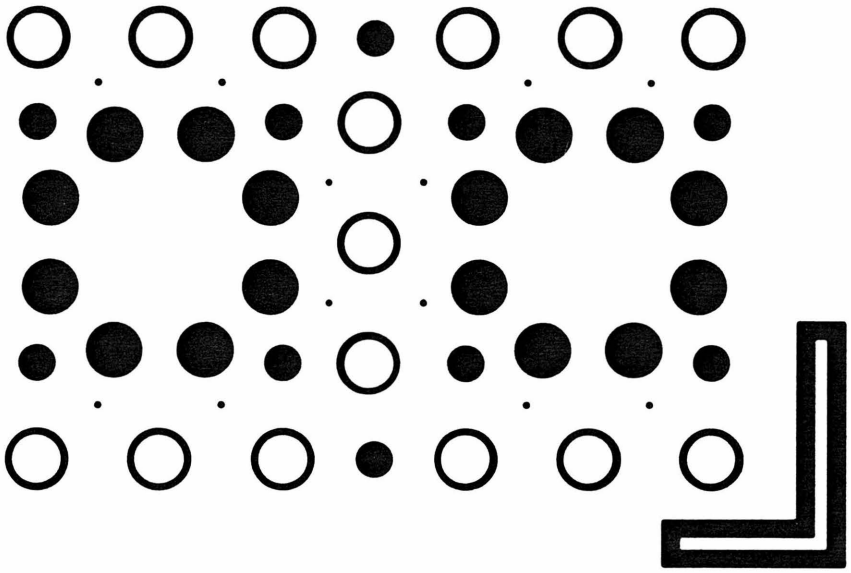
deposition techniques. The samples were then annealed to 750-950°C for 15 minutes in either vacuum ampoules (Chapter 3) or a flowing hydrogen ambient (Chapter 4). Hydrofluoric acid was used to remove the dielectric layer after the anneal. Photoresist lifting techniques were employed to make Ohmic contacts to the implanted layers. A 400 Å layer of Au-Ge (12 weight percent Ge), followed by a 500 Å layer of Ni was evaporated on the resist coated implants. Thin films of Au-Ge were chosen to avoid shorting theimplanted junction as Au-Ge is known to penetrate deep into GaAs during alloy.[51] The contacts were alloyed at 450°C for 2 minutes in a hydrogen atmosphere.

Mesa etching was used to define the Hall effect structure on the GaAs surface. The mesa mask used in Chapter 3 was the van der Pauw pattern presented in Part I of this thesis. In Chapter 4, a more complicated set of masks was utilized to fabricate various size diode structures in addition to the Hall structure (see Fig. 2). Additional contact pads were provided on the van der Pauw pattern to insure the existence of four Ohmic contacts for Hall measurements. Back contact to the implanted diodes was made with In-Ga.

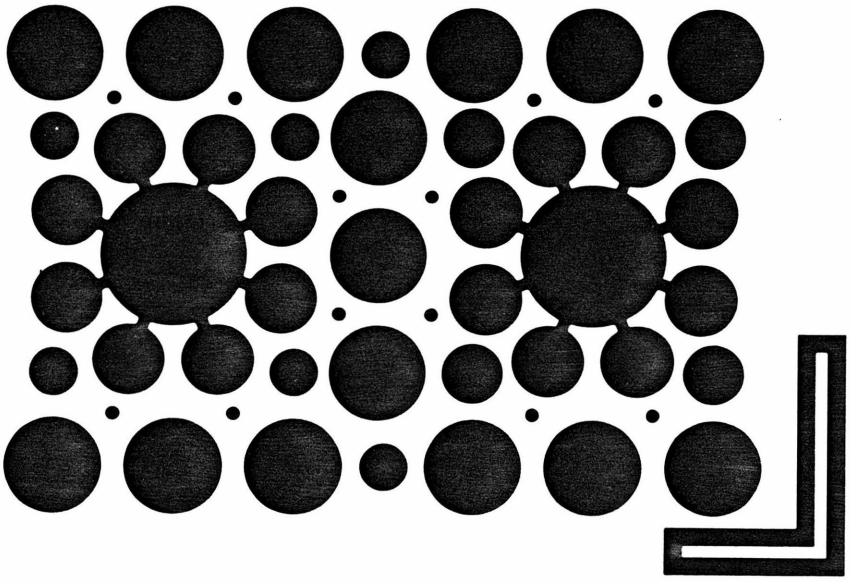
2.2 Analysis Techniques

2.2.1 Backscattering Techniques

The physical properties of the implanted layers and the various dielectric coatings used during annealing were investigated by backscattering of high energy He^+ ions, combined with channeling



(a)



(b)

Fig. 2 Photographs of the contact mask (a) and the mesa mask (b) used in Chapter 4 to fabricate Hall patterns and various size implanted diodes.

effect measurements.[†](52,53) The energy distribution of the backscattered particles was recorded with a surface barrier detector of 16 keV resolution. Standard electronics, including a pulse pile-up rejection system, fed pulses to a 512-channel pulse-height analyzer. The energy-to-channel-number conversion, typically 3.5 keV per channel, was calibrated by scattering from Si, V and Au targets.

The energy spectrum of backscattered He^+ ions provides mass, depth, and composition information on the sample studied(52,53). The atomic masses of elements present in a thin target are reflected by the energy positions of their respective backscattering peaks (scattering kinetics). For a sample thicker than a few hundred Ångstroms, the signal produced by a given element is broadened toward lower energies by an amount proportional to the sample thickness. The height of an elemental peak is directly related to the concentration of that element in the sample. If the concentration of an element varies as a function of depth in a sample, the backscattering signal height will vary proportionally.

Channeling techniques can be used to study the lattice location and the resulting lattice damage of ion implanted species.(50) In brief, the technique involves determining the scattering yield from an implanted layer when the incident beam is aligned with a major crystallographic axis, and comparing it with the random yield (beam

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[†]Measurements performed using the 3 MV accelerator at the Kellogg Radiation Laboratory (Caltech) and the Rockwell International Science Center accelerator.

enters along a non-aligned direction). The fraction of impurity atoms located off lattice sites is given by the ratio of the aligned impurity signal area to the random impurity signal area. The relative amount of disorder present in a sample is proportional to the same ratio for the substrate disorder peak.

2.2.2 Hall Effect Techniques

Hall effect and sheet resistivity were measured at room temperature using the van der Pauw configuration (see Part I, 2.1). In some cases, differential Hall effect measurements (Part I, 2.1) were performed in conjunction with layer removal to determine the carrier concentration and mobility profiles in the implanted layers. Since the anodic oxidation technique used in silicon cannot be applied to GaAs, chemical etching procedures were utilized. Thin layers were stripped from the implanted surface by etching the sample in a solution of equal parts H_2SO_4 and H_2O_2 to 100 parts H_2O. The etch rate was approximately 300 Å/min. During the etch, the contact pads and channels to the Hall pattern were protected by black wax. The thickness of the removed layers was calculated by performing interferometry measurements on the GaAs step after the final strip had been completed.

Chapter 3

INFLUENCE OF IMPLANTATION TEMPERATURE AND SURFACE PROTECTION ON TELLURIUM IMPLANTATION IN GaAs

In this chapter the effect of elevating the implant temperature and changing the protective coating used during annealing is analyzed for tellurium implanted gallium arsenide.

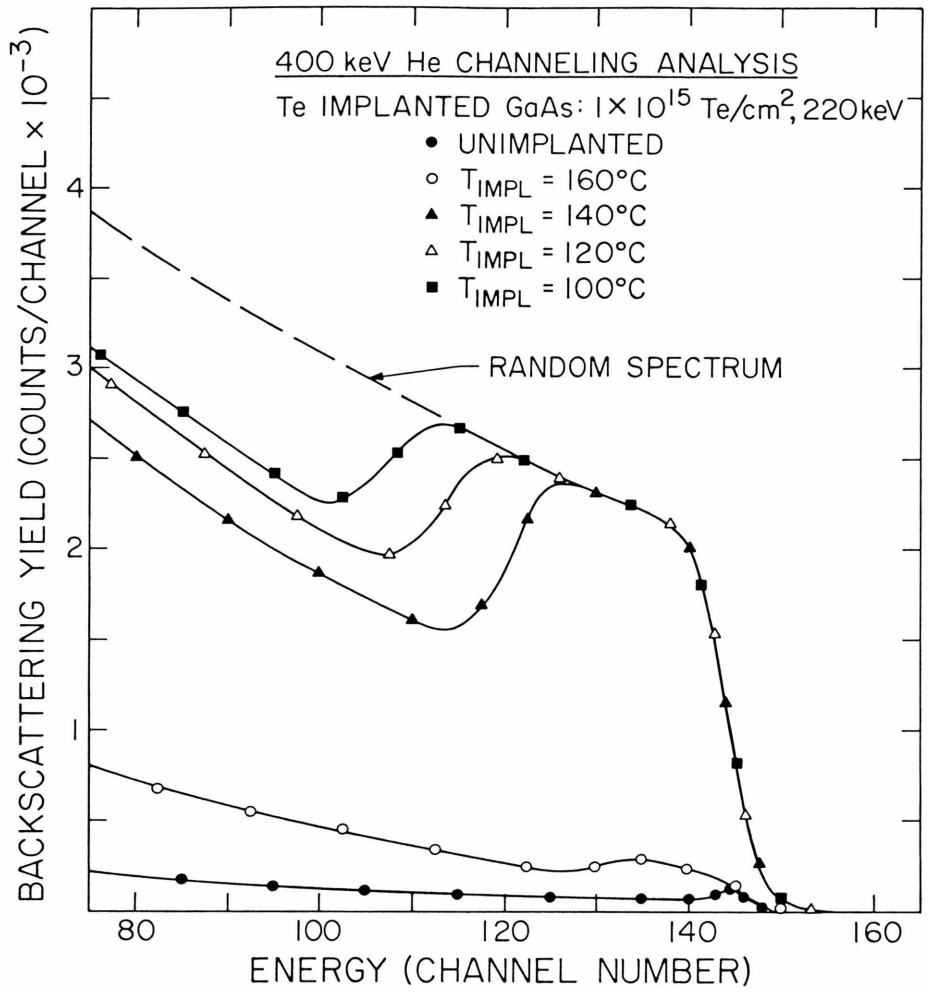
Channeling measurements are used to determine the lattice damage as a function of implant temperature. The protective qualities of SiO_2 and Si_3N_4 are compared by backscattering and photoluminescence techniques. The electrical properties of the implanted layers are analyzed by Hall effect and Schottky barrier capacitance-voltage measurements.

3.1 Physical Properties

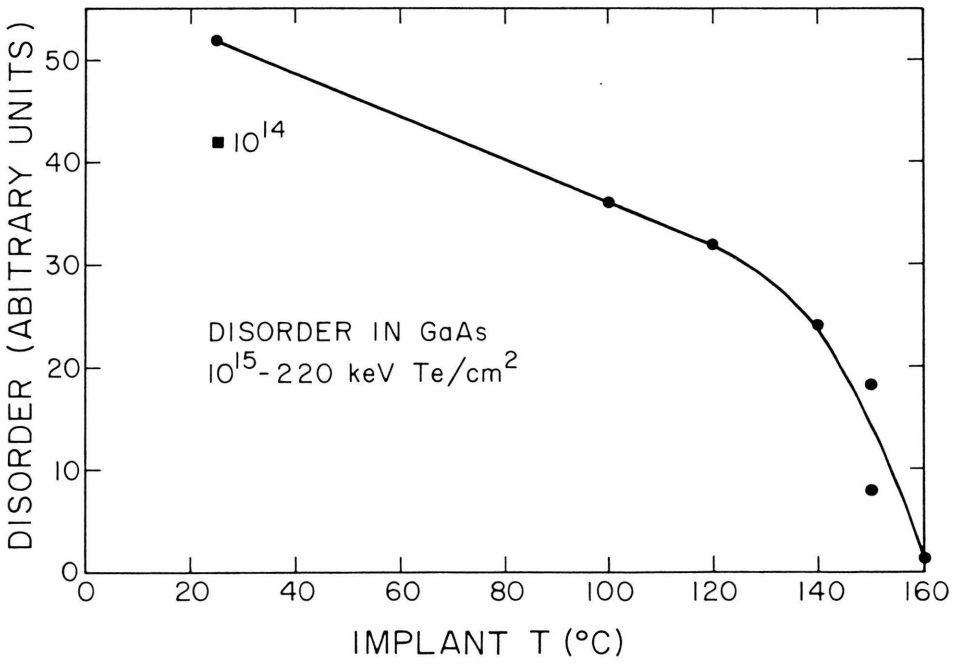
3.1.1 Lattice Disorder vs. Implant Temperature

In Fig. 3a, 400 keV channeling spectra are shown for tellurium implanted GaAs as a function of implant temperature. The samples were not annealed before the channeling measurements were performed. The GaAs substrates were implanted with a flux of about 1 $\mu A/cm^2$ of 220 keV Te to an integrated dose of 10^{15} Te/cm^2. The dashed line in Fig. 3 indicates the random yield. The damage peak is found in the aligned GaAs spectrum close to the GaAs edge. At implant temperatures of 140°C and below, the implant damage is so large that the aligned spectrum merges with the random spectrum. In contrast, the aligned spectrum for the 160°C implant is almost identical to that of

Fig. 3 Study of lattice disorder produced in tellurium implanted GaAs as a function of implant temperature. (a) Random and <110> aligned spectra of 400 keV He ions backscattered from GaAs samples that have been implanted at various temperatures. (b) The relative amount of disorder plotted as a function of implant temperature for these unannealed specimens.


400 keV He CHANNELING ANALYSIS
Te IMPLANTED GaAs: 1×10^15 Te/cm^2, 220keV
UNIMPLANTED
T_IMPL = 160°C
T_IMPL = 140°C
T_IMPL = 120°C
T_IMPL = 100°C
RANDOM SPECTRUM
BACKSCATTERING YIELD (COUNTS/CHANNEL × 10^-3)
ENERGY (CHANNEL NUMBER)
80
100
120
140
160
1
2
3
4

(a)


DISORDER (ABITRARY UNITS)
IMPLANT T (°C)
■ 10^14
DISORDER IN GaAs
10^15 - 220 keV Te/cm^2
0
10
20
30
40
50
0
20
40
60
80
100
120
140
160

(b)

Figure 3

the unimplanted sample.

The relative amount of disorder in each sample was computed from the area under the damage peaks and is presented as a function of implant temperature in Fig. 3b. Up to an implant temperature of 140°C, the channeling measurements indicate that an amorphous layer had been formed. Around 150°C, there is a large decrease in the amount of disorder and at a temperature of 160°C the disorder has almost vanished. Similar results have been noted by Whitton and Bellavance[48] for sulfur implantation in GaAs.

Figure 4 compares the 2 MeV channeling spectra for two samples implanted at elevated temperatures. In both cases the damage peak is almost nonexistent. Most important, however, is the low aligned yield in the tellurium peak. This indicates that most of the tellurium in the unannealed samples is located along <110> rows, and therefore, is probably substitutional.

3.2.2 Diffusion Problems During Anneal

The gallium masking qualities of SiO_2 and Si_3N_4 are compared in Fig. 5. Two silicon samples, one coated with SiO_2 and the other Si_3N_4, were placed in a vacuum ampoule with a small amount of gallium and heated to 800°C for 30 minutes. After heating, backscattering measurements were performed to determine the gallium profiles in the dielectrics. As expected, gallium readily diffused through the SiO_2 layer. However, there was little, if any, diffusion of gallium into the Si_3N_4 layer.

Additional measurements by Chu, et al.[54] have indicated that

Fig. 4 Random and <110> aligned spectra of 2 MeV He ions back-scattered from two GaAs samples implanted at elevated temperatures with Te.

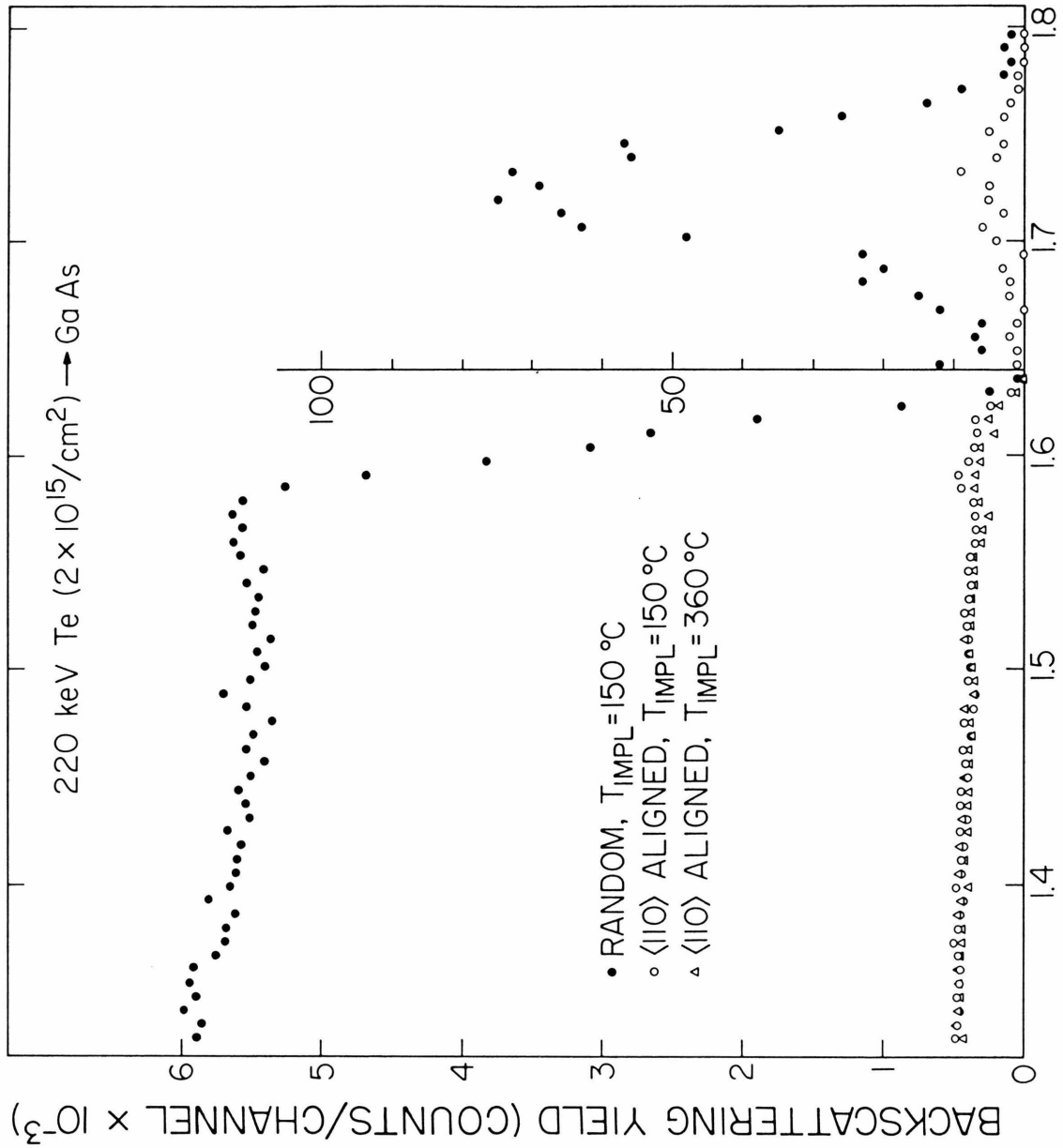

220 keV Te (2 × 10^15/cm^2) → Ga As
• RANDOM, T_IMPL=150 °C
○ ⟨110⟩ ALIGNED, T_IMPL=150 °C
△ ⟨110⟩ ALIGNED, T_IMPL=360 °C
BACKSCATTERING YIELD (COUNTS/CHANNEL × 10^-3)
ENERGY [MeV]
0
1
2
3
4
5
6
100
50
1.4
1.5
1.6
1.7
1.8

Figure 4

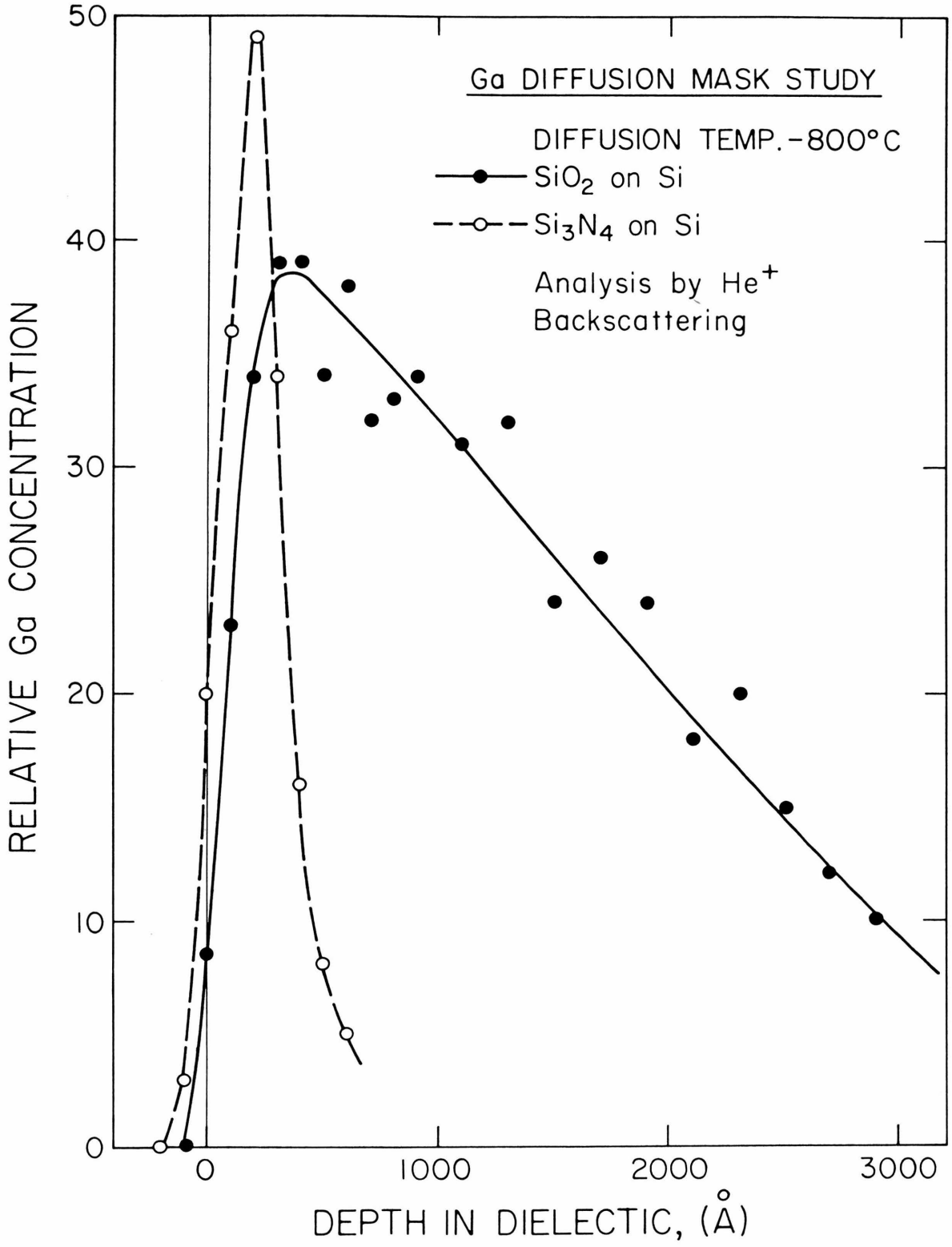


Fig. 5 Gallium diffusion through SiO_2 and Si_3N_4. Analysis by 2 MeV He ion backscattering.

arsenic does not diffuse through either SiO_2 or Si_3N_4.

The out-diffusion of implanted tellurium in GaAs is shown in Fig. 6. The GaAs substrate was implanted at room temperature with a dose of 10^{15} Te/cm^2. SiO_2 was used as the protective coating during the 15 minute anneal at 800°C. Again, backscattering techniques were used to determine the impurity profile. The as-implanted profile has a peak depth that agrees closely with the value of 550 Å predicted by LSS theory[55] for 220 keV tellurium implanted GaAs. During the anneal, some tellurium clearly out-diffuses and collects on the sample surface.

On the other hand, no motion is noted in the tellurium profile of a 350°C implant coated with Si_3N_4 during a 900°C anneal. The backscattering spectra of three different samples is presented in Fig. 7 as a function of heat treatment during and after implantation. The Te dose in the 900°C anneal sample was appreciably smaller than in the other two implants. Because of this low dose, the peak to background ratio is small. However, when this fact is taken into account, the width of the Te distribution is approximately equal to those of the other two implants.

3.1.3 Defects in Annealed Implants

Figure 8 shows photoluminescence spectra obtained at 77°K with the use of illumination from a He-Ne laser. The peak at 8200 Å is due to band-to-band recombination. Samples implanted at 150°C and annealed at 750°C had a band-gap intensity about the same as for an unimplanted sample, and approximately 100 times that for room-

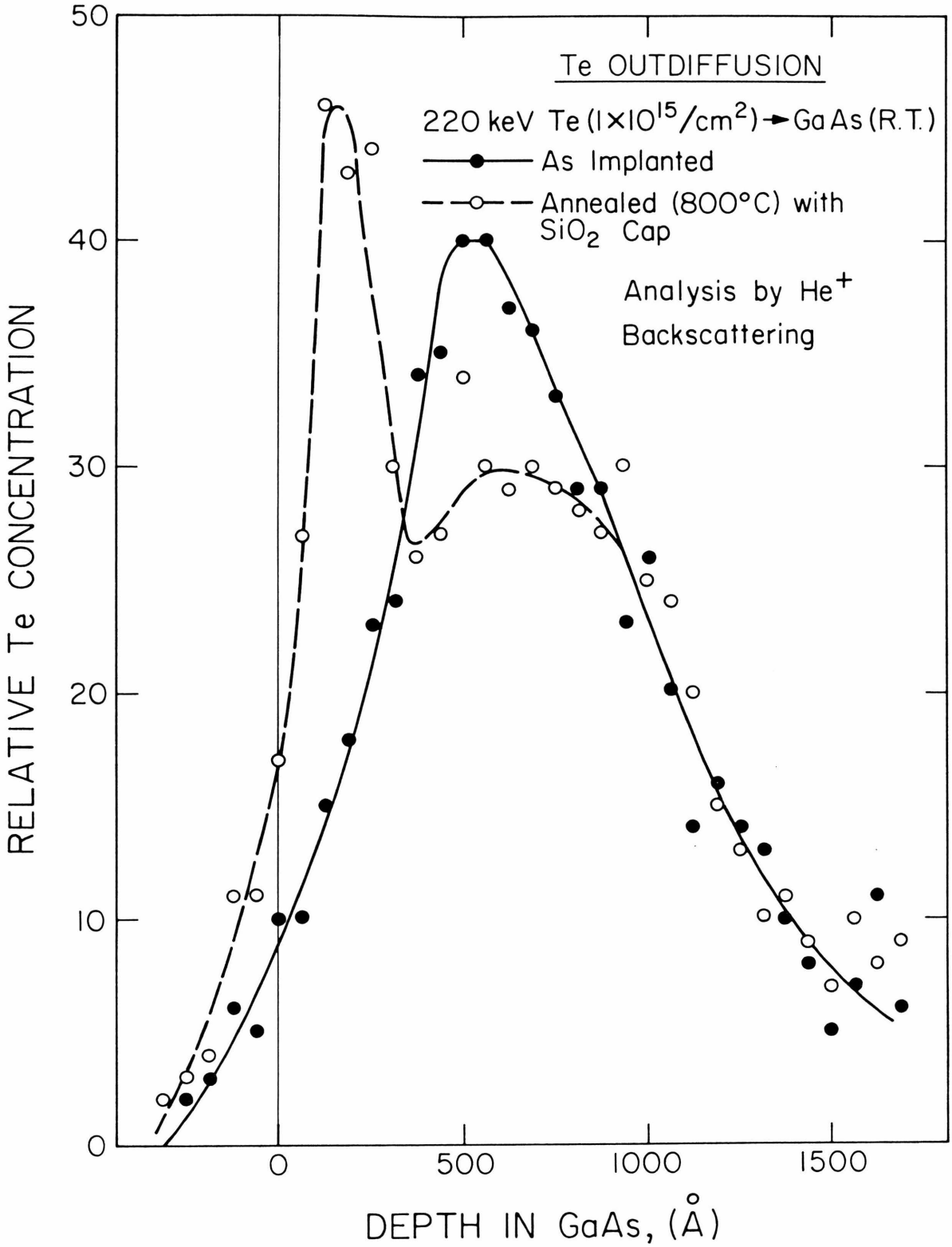


Fig. 6 Tellurium out-diffusion during anneal in a room temperature implant coated with SiO_2. Analysis by backscattering.

Fig. 7 Random and <110> aligned spectra of 2 MeV He ions backscattered from Te atoms implanted in GaAs. Three spectra are presented as a function of sample heat treatment during and after implantation.

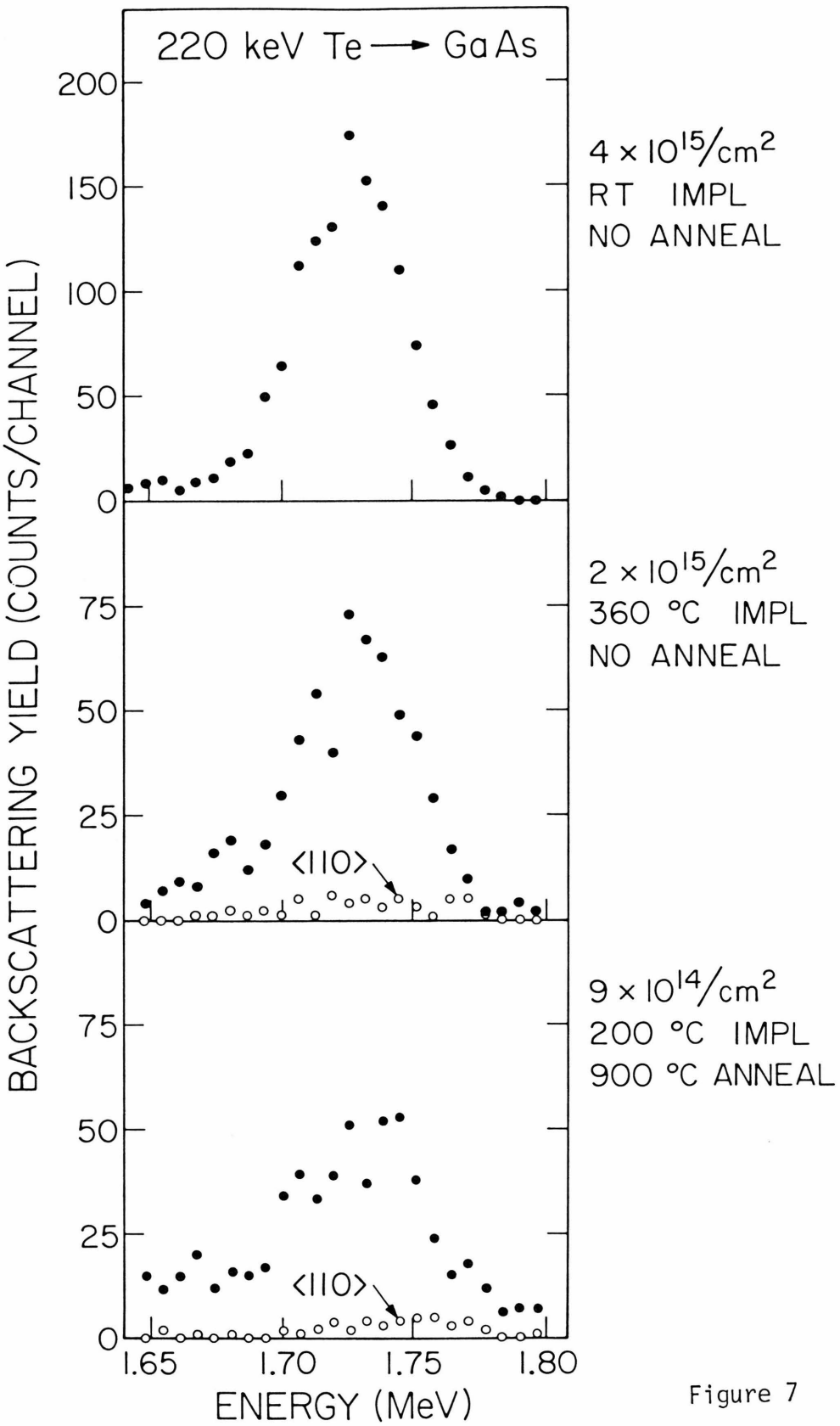

220 keV Te → GaAs
4 × 10^15/cm^2
RT IMPL
NO ANNEAL
2 × 10^15/cm^2
360 °C IMPL
NO ANNEAL
9 × 10^14/cm^2
200 °C IMPL
900 °C ANNEAL
<110>
<110>
BACKSCATTERING YIELD (COUNTS/CHANNEL)
ENERGY (MeV)
200
150
100
50
0
75
50
25
0
75
50
25
0
1.65
1.70
1.75
1.80

Figure 7

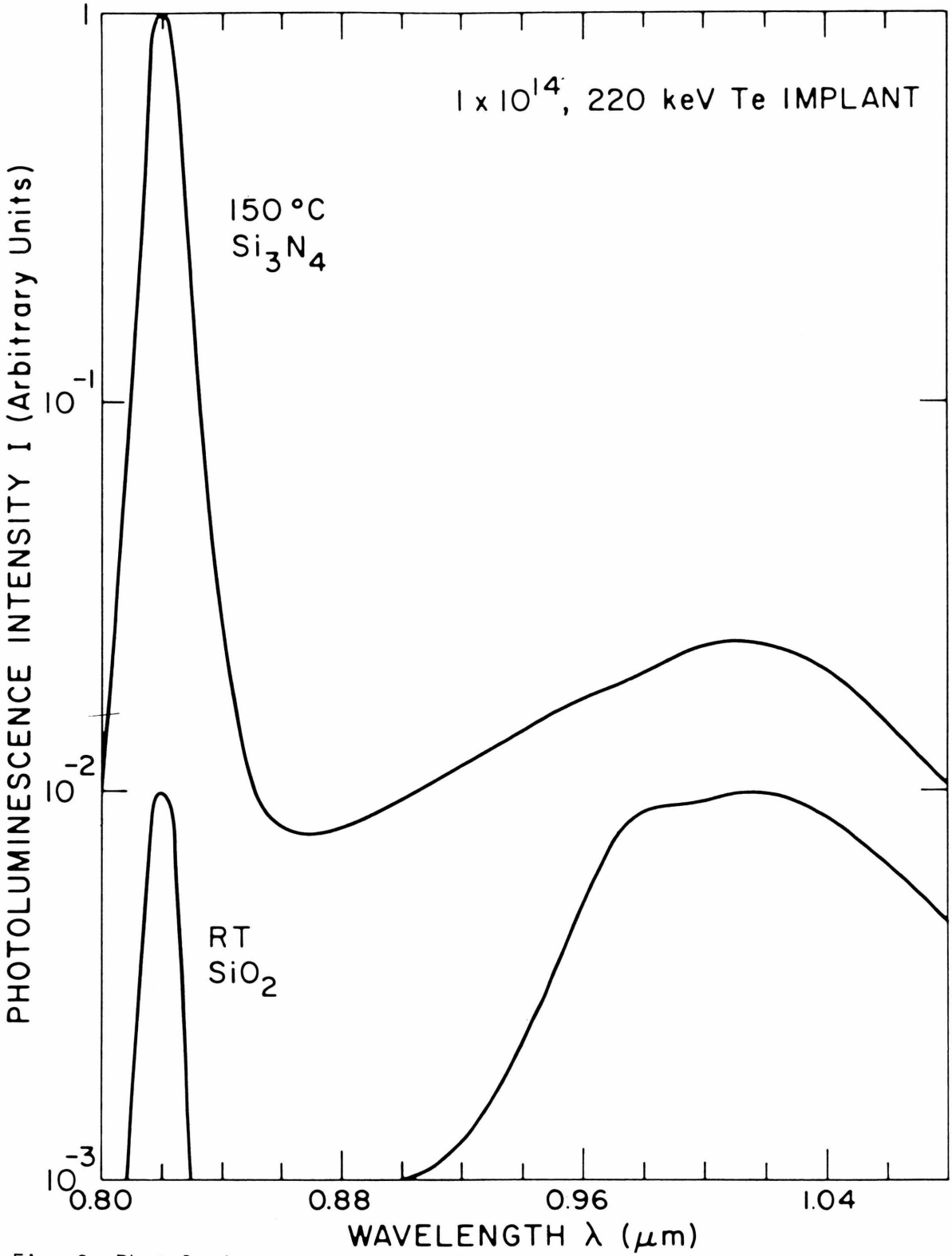


Fig. 8 Photoluminescence spectra for Te implanted GaAs annealed at 750°C. Two spectra are presented as a function of implant temperature and dielectric coating.

temperature implants annealed at the same temperature (see Table III). This indicates that the annealing to 750°C of samples implanted at 150°C is sufficient to remove most of the defects which quench the photoluminescence, whereas this is not the case for room-temperature implants.

The broad peak observed at 1μ is a frequently observed peak attributed to a gallium-vacancy-Te complex (V_{Ga} Te_{As}).[56] The intensity of this peak is much higher relative to the band-gap peak for all samples annealed with SiO_2 on the surface compared to those with Si_3N_4. In a sample implanted at 150°C and annealed with a SiO_2 coating, this peak was approximately 20 times as intense as in the sample implanted at 150°C and annealed with a Si_3N_4 protective coating (Fig. 8). The observation of enhanced gallium vacancy formation with SiO_2 on the surface during annealing is consistent with our backscattering results on the diffusion of Ga in SiO_2.

3.1.4 Summary of Results

The implantation of tellurium into a hot GaAs substrate has been shown to result in reduced lattice disorder compared to room temperature implantation. During anneal, the out-diffusion of tellurium was observed in a room temperature implant coated with SiO_2. No motion was detected in the tellurium profile of a 350°C implant coated with Si_3N_4 during anneal.

Silicon nitride was shown to be an excellent mask against Ga out-diffusion during anneal. In contrast, Ga readily diffused through SiO_2 and as a result gallium-vacancy-tellurium (V_{Ga}-Te) complexes

TABLE III

Photoluminescence of Tellurium Implanted GaAs

Implant Temperature[a]	Anneal Coating[c]	Band Gap Intensity	1.0μ Peak Intensity	Ratio (BG/1.0μ)
23°C	Bare	.01	.003	3.3
23°C	SiO_2	.01	.004	2.5
23°C	Si_3N_4	.01	.0004	25
23°C(b)	Si_3N_4	.01	.0007	15
150°C	Bare	1.0	.02	50
150°C	SiO_2	1.0	.50	2
150°C	Si_3N_4	1.0	.017	60
150°C(b)	Si_3N_4	1.0	.02	50

(a) Implant dose: 1×10^{14} Te/cm^2 at 220 keV

(b) For these samples, 200Å of Si_3N_4 were sputtered on surface before implantation.

(c) Implants were annealed at 750°C for 15 min.

were found in the implanted layers annealed with a SiO_2 protective coating.

This suggests that higher electrical activity should be observed in hot implants annealed with a Si_3N_4 protective layer compared to room temperature implants annealed with a SiO_2 coating.

3.2 Electrical Measurements

Schottky barrier capacitance-voltage measurements[57] have been made to determine the electron concentration profile in the samples used for the photoluminescence measurements. For all samples implanted at room temperature, the electron concentration was substantially lower than the original concentration to depths of $\sim 3\mu$. In contrast, no high-resistance layers were observed for 150°C implants, and the doped region merged smoothly into the epitaxial layer background doping.

In Table IV, the electrical activity of the implanted layers is presented as a function of implant temperature and protective coating. Hall effect techniques were used to measure the surface carrier concentration in the implants. The samples were implanted with a dose of 10^{14} Te/cm^2 and annealed at 750°C for 15 minutes. No electrical activity was detected in the room temperature implants, and very little detected in the 150°C implants coated with SiO_2. Only the 150°C implants which were annealed with a Si_3N_4 protective layer exhibited any sizable electrical activity. The maximum doping efficiency observed was 7%.

TABLE IV

Electrical Activity of Tellurium Implanted GaAs

Implant[a] Temperature (°C)	Protective Coating[b]	Surface Carrier Concentration, N_s (cm^{-2})
23	SiO_2	(c)
23	Si_3N_4	(c)
150	SiO_2	6×10^{11}
150	SiO_2	7×10^{11}
150	Si_3N_4	6×10^{12}
150	Si_3N_4	7×10^{12}
150	Si_3N_4	3×10^{12}

(a) Implant dose: 1×10^{14} Te/cm^2.

(b) Implants were annealed at 750°C for 15 min.

(c) Capacitance-voltage measurements indicated that the carrier density was below 10^{16} electrons/cm^3 (the electron density of the substrate).

In an effort to improve the doping efficiency, the implantation temperature was increased to 350°C and the anneal temperature raised to 900°C with a Si_3N_4 coating on the implants. For comparison, electrical measurements were also performed on samples annealed to 750°C. The dependence of the surface carrier concentration on ion dose is shown in Fig. 9. The lower dashed line represents the 750°C anneal results and the upper dashed line, the 900°C results (the low points were obtained on samples with poor nitride adhesion). Clearly, the higher anneal temperature gave more electrical activity. In one sample implanted with a dose of 3×10^{13} Te/cm^2 and subsequently annealed to 900°C, a 50% doping efficiency was attained.

For the 900°C results, one notices that for doses larger than 1×10^{14} Te/cm^2, there is no increase in electrical activity above 3×10^{13} Te/cm^2. Similar behavior has been observed for p-type implantation in GaAs and is usually indicative of solubility effects.[38]

Sequential Hall effect measurements in conjunction with layer removal were used to determine the carrier concentration profile in a sample implanted with 1×10^{14} Te/cm^2 at 350°C (Fig. 10). The sample was coated with 300Å of Si_3N_4 during implantation to avoid disassociation effects and subsequently annealed to 950°C with a 2000Å coating of Si_3N_4. As expected, the peak in the carrier concentration was shallow due to the 300Å pre-implant nitride. The peak carrier concentration was 8×10^{18} electrons/cm^3; a value approximately equal to the maximum electron concentration which has been attained by doping GaAs with tellurium during growth.[58] However, the mobility in the layer was somewhat low compared to bulk values.

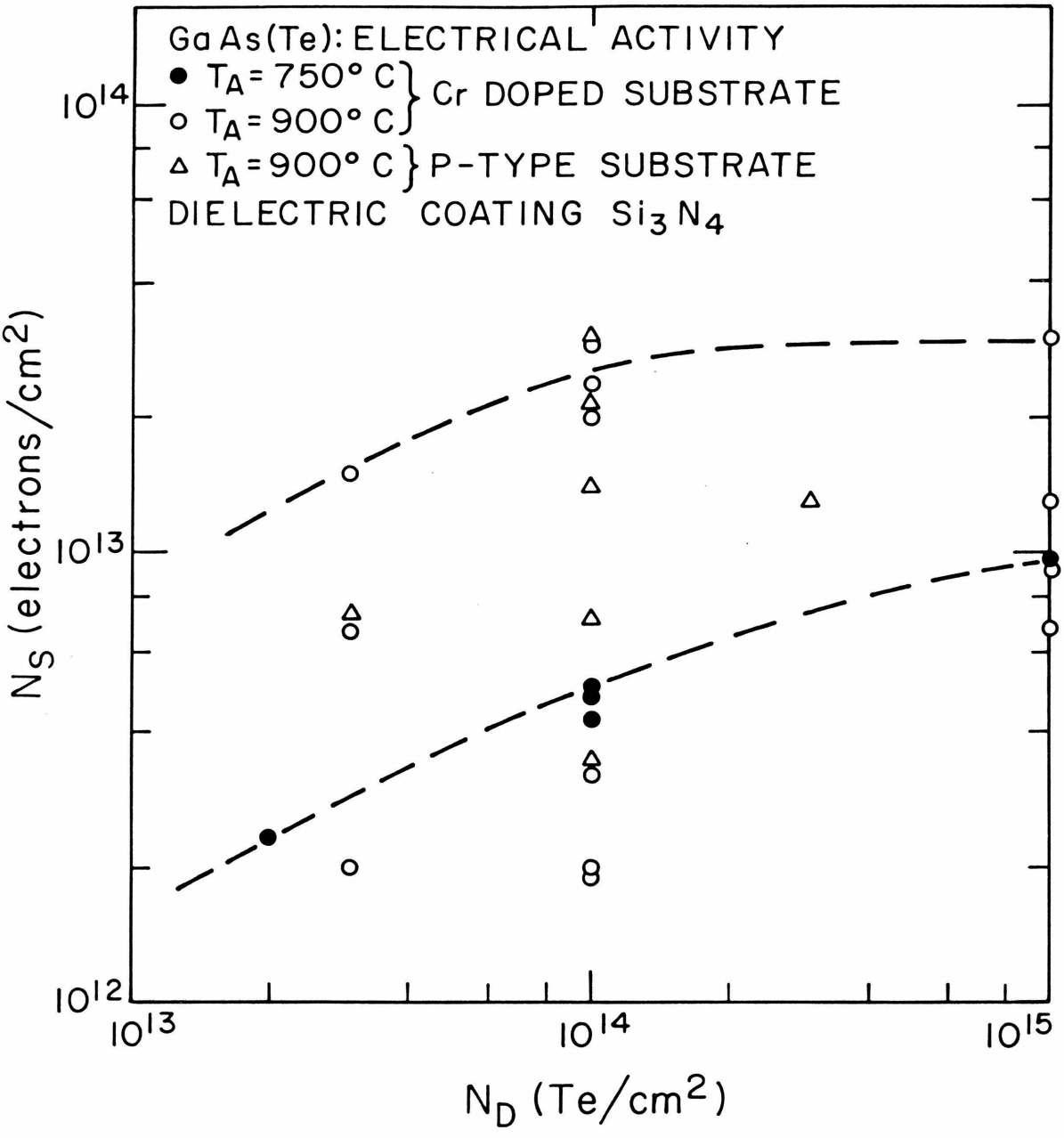


Fig. 9 The measured number of electrons/cm^2 in Te implanted GaAs after anneal as a function of the number of implanted ions/cm^2.

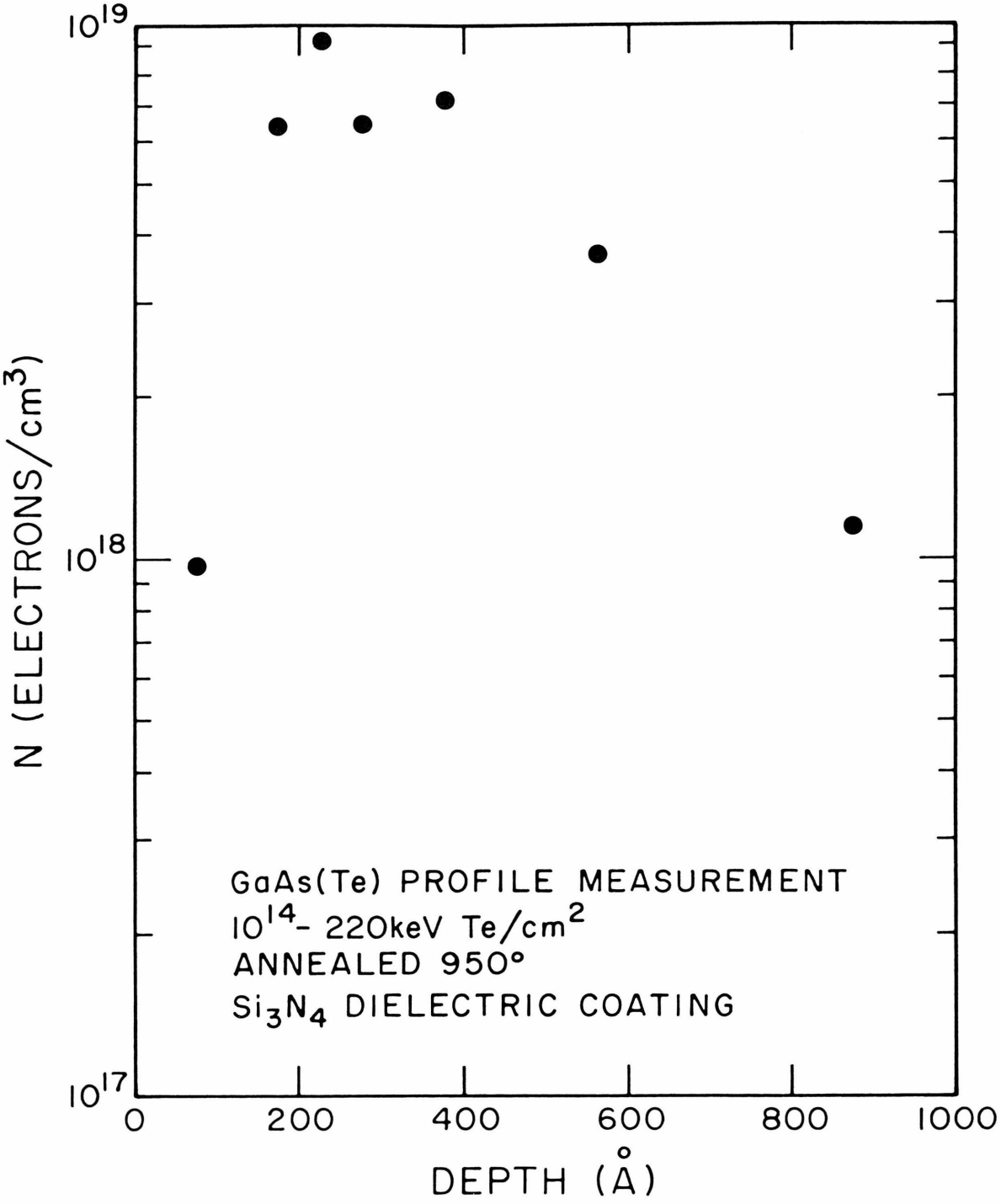


Fig. 10 The electron concentration profile for a GaAs sample implanted with 1 x 10^{14} Te/cm^2 at 350°C through a 200Å Si_3N_4 layer. The sample was annealed at 950°C for 15 min. prior to differential Hall measurements.

3.3 Silicon Nitride Adherence

Some difficulty was observed in the course of this work with the adherence of the Si_3N_4 layers to the GaAs surface during the anneal. As was mentioned, we attribute the scatter in the electrical measurements to this problem. Figure 11a is a scanning electron microscope photograph of a tellurium implanted GaAs specimen coated with Si_3N_4. Only the upper right portion of the field of view was exposed to the tellurium beam. After the implant was covered with Si_3N_4, it was annealed to 750°C for 15 minutes. The Si_3N_4 has bubbled (dark patches) and in one case ruptured (the white area) in the implanted region. Inside the ruptured area several thermal etch pits can be seen on the GaAs surface (Fig. 11b). Even in the non-implanted area (Fig. 11c), the Si_3N_4 bubbled. However, the bubble size was much smaller than in the implanted region. Evidence of the large amount of GaAs disassociation occurring during the anneal, is witnessed by the regrowth patterns seen in Fig. 11d.

Backscattering measurements indicated that the sputtered Si_3N_4 layers contained a significant amount of oxygen. The presence of oxygen in Si_3N_4 could lead to gallium out-diffusion during anneal for samples coated with this dielectric.

3.4 Summary

The electrical measurements were consistent with the predictions made in section 3.1. High electrical activity was observed in samples implanted at elevated temperatures and subsequently annealed with a Si_3N_4 coating. In contrast, room temperature implants coated with

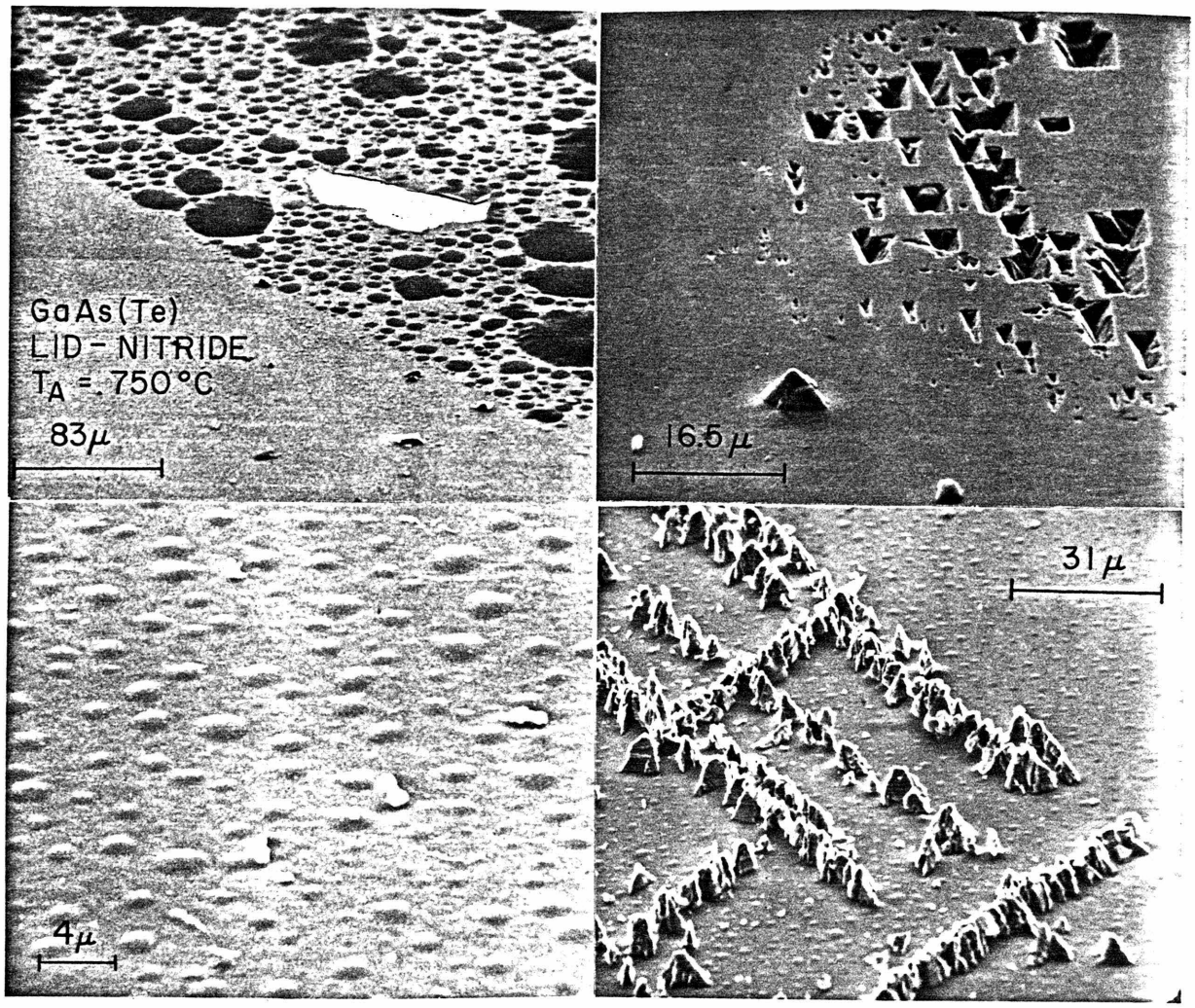


Fig. 11 Scanning electron microscope photographs of a Te implanted GaAs specimen coated with Si_3N_4, after a 750°C anneal. The sample was implanted at room temperature with a dose of 5×10^{14} Te/cm^2. (a) Si_3N_4 coating on the GaAs where only the upper right portion of the field view was exposed to the Te beam; (b) Thermal etch pits on the GaAs surface inside the ruptured area of the Si_3N_4 shown in (a); (c) Bubbles in the Si_3N_4 over the unimplanted area in (a); (d) GaAs regrowth patterns in one of the thermally etched areas of the GaAs surface.

SiO_2 during anneal displayed almost no electrical activity.

A maximum doping efficiency of 50% was achieved for 350°C implants annealed to 900°C with a Si_3N_4 encapsulent. The peak electron concentration was approximately equal to the maximum attainable in tellurium doped GaAs (7×10^{18} electrons/cm^3).

However, the electrical activity of implants overcoated with Si_3N_4 varied over a wide range for samples with identical implant conditions. The scatter in the electrical measurements was attributed with the poor adherence of the Si_3N_4 layers to the GaAs surface during anneal.

Chapter 4

THE USE OF AlN AS AN ENCAPSULATING LAYER

In the previous chapter, it was shown that by implanting tellurium into substrates held at 350°C and using Si_3N_4 as an encapsulating layer during anneal, a peak electron concentration approximately equal to the maximum attainable in tellurium doped GaAs could be achieved. However, there were two problems encountered in use of Si_3N_4 as the encapsulating layer. First, it was difficult to sputter oxygen-free thin films of Si_3N_4. Further it was hard to maintain the adherence of these films to the GaAs surface during anneal. As a result, the observed electrical activity varied over a wide range for samples with identical implant conditions. The poor adherence of the Si_3N_4 is attributed to an expansion coefficient mismatch. Si_3N_4 has an expansion coefficient of 3.2×10^{-6}/°C compared to 6.8×10^{-6}/°C for GaAs.

In an effort to obtain more uniform results, we have examined the effect of changing the encapsulating layer. The objective was to find a dielectric layer with improved adherence and masking qualities that would result in consistently high electrical activity. AlN was chosen as the protective layer for this work since it has an expansion coefficient of 6.1×10^{-6}/°C which closely matches the GaAs value. In addition, any oxygen incorporated in the AlN film would be in the form of Al_2O_3, not SiO_2 as in the case of Si_3N_4. Previous work by Chu, et al.[54], indicated that Al_2O_3 is a good mask against gallium and arsenic diffusion.

The integrity of the AlN film was analyzed before and after anneal by Rutherford backscattering measurements and scanning electron microscopy. The electrical properties of the annealed implants was investigated with junction I-V measurements, C-V measurements, and Hall effect measurements. As a basis of comparison, electrical measurements were also performed on samples overcoated with Si_3N_4.

4.1 Aluminum Nitride Properties

The backscattering spectrum of an AlN layer sputtered on a vitreous carbon substrate is shown in Fig. 12. The energy positions marked on the figure refer to the presence of a given element on the sample surface (scattering kinetics). Depth effects are reflected in energy loss: the width of the aluminum peak is proportional to the AlN film thickness. The nitrogen peak is complicated by overlap from an oxygen peak. The inset in Fig. 12 shows a schematic decomposition of the data into step spectra. It is apparent that the addition of the nitrogen and oxygen signals creates the step structure observed in the backscattering spectrum. Analysis shows that there are nearly equal amounts of oxygen and nitrogen in the sputtered film. Assuming the film to be composed of AlN and Al_2O_3, composition calculations yield that the film is 3 parts AlN and 1 part Al_2O_3 with a slight excess of aluminum.

Ellipsometry measurements were used to determine the film thickness and index of refraction. The refraction index of a dielectric film is a good judge of film quality. The reported value for the refraction index of AlN is 2.16.[59] Our films had an index of

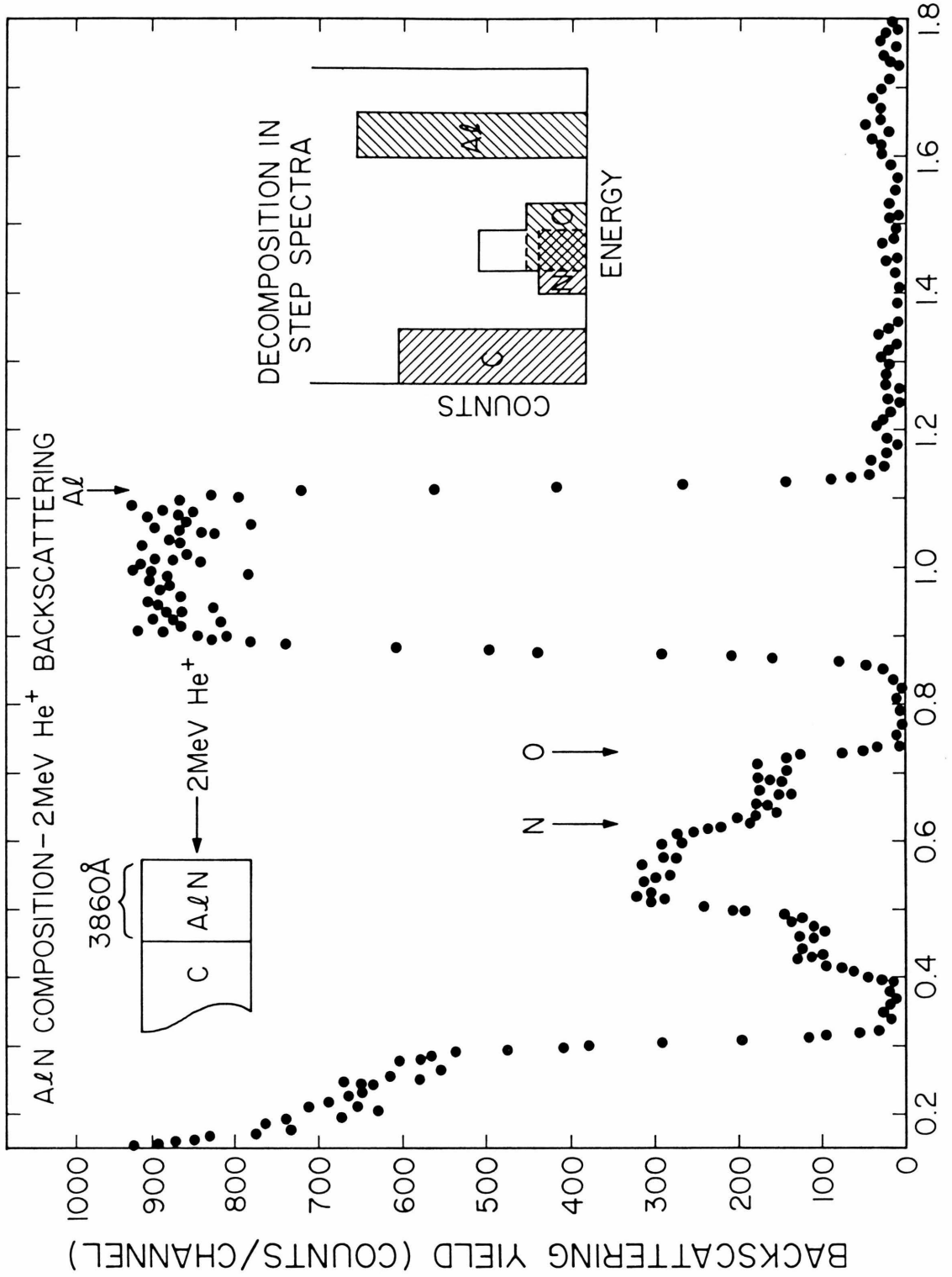


Fig. 12 Energy spectrum of 2 MeV He ions backscattered from a sputtered AlN film on carbon.

2.46. The discrepancy is assumed to be a result of the excess aluminum in the AlN films since Al_2O_3 has an index of refraction smaller than that of AlN.

In the past, there have been problems with gallium or arsenic out-diffusing through the dielectric overcoat during anneal. Figure 13 compares backscattering spectra taken before and after anneal of an AlN coated GaAs sample. The counts beyond 1.4 MeV indicate there are trace impurities in the AlN film. However, since there is no change in the spectrum after anneal, we conclude that there was no pronounced gallium or arsenic out-diffusion during the anneal. If gallium or arsenic were present in the film, they were in concentrations less than 2%.

Electron microscopy verified that the AlN adhered to GaAs during anneal. The surface of an AlN overcoated GaAs sample was smooth and featureless after annealing at 850°C for 15 minutes. In contrast, the scanning electron microscope photograph of Si_3N_4 coated GaAs in the last chapter showed definite evidence of bubbling after a 750°C anneal.

4.2 Electrical Measurements

The current-voltage characteristics of several implanted diodes were measured in the range of 10^{-11} to 10^{-2} amps. The forward characteristic of an ideal GaAs diode generally follows the relation $I = I_o \exp(qV/nkT)$ where $n = 2$.[60] Only in one case (see Fig. 14) was such an ideal behavior approximated. Most of the implanted diodes had a forward characteristic n value equal to 1.15 (see Table V).

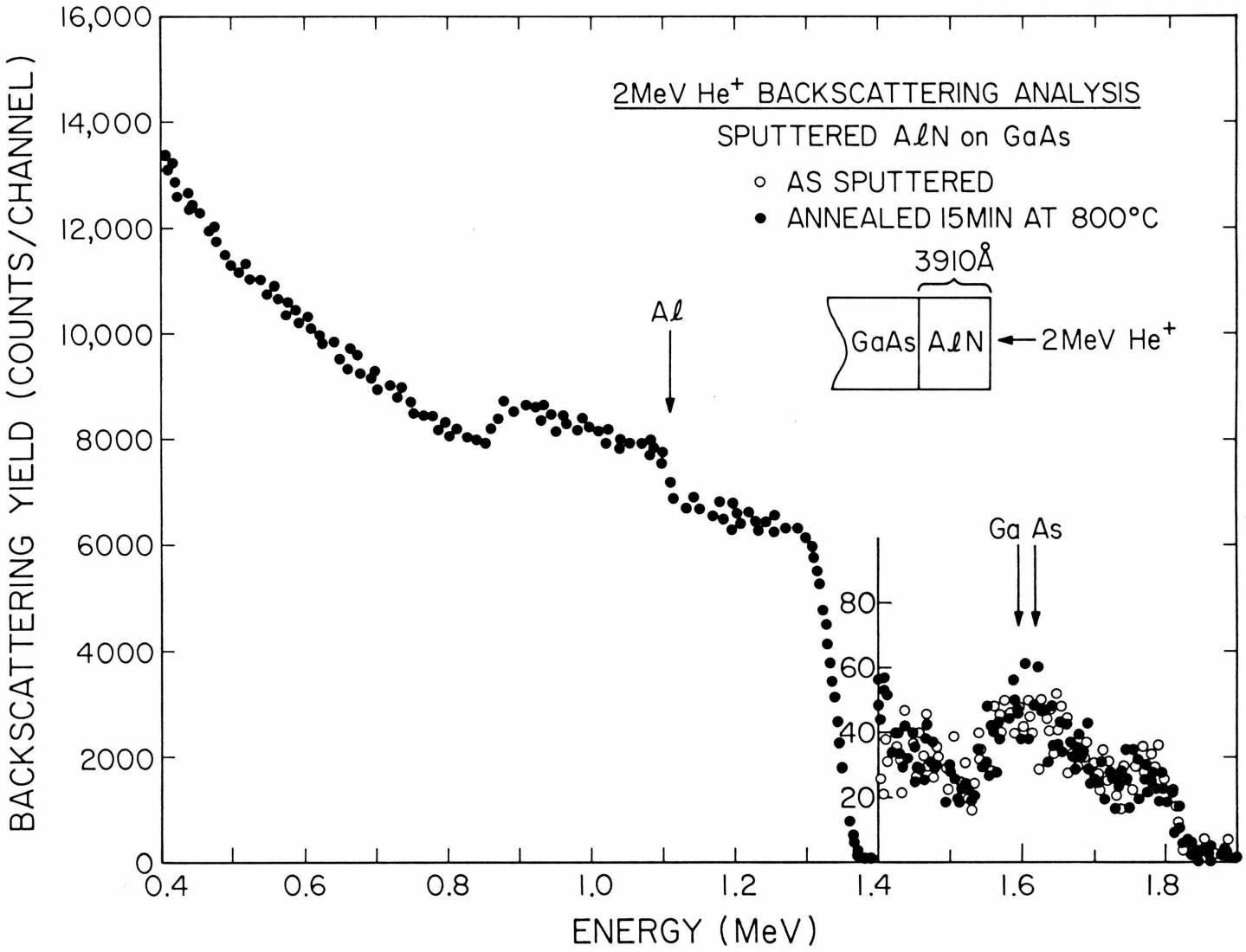


Fig. 13 Energy spectrum of 2 MeV He ions backscattered from an AlN coated GaAs sample. Measurements were taken on the AlN film as sputtered (open circles) and after annealing at 800°C (filled circles). The integrated beam current was equal for both measurements.

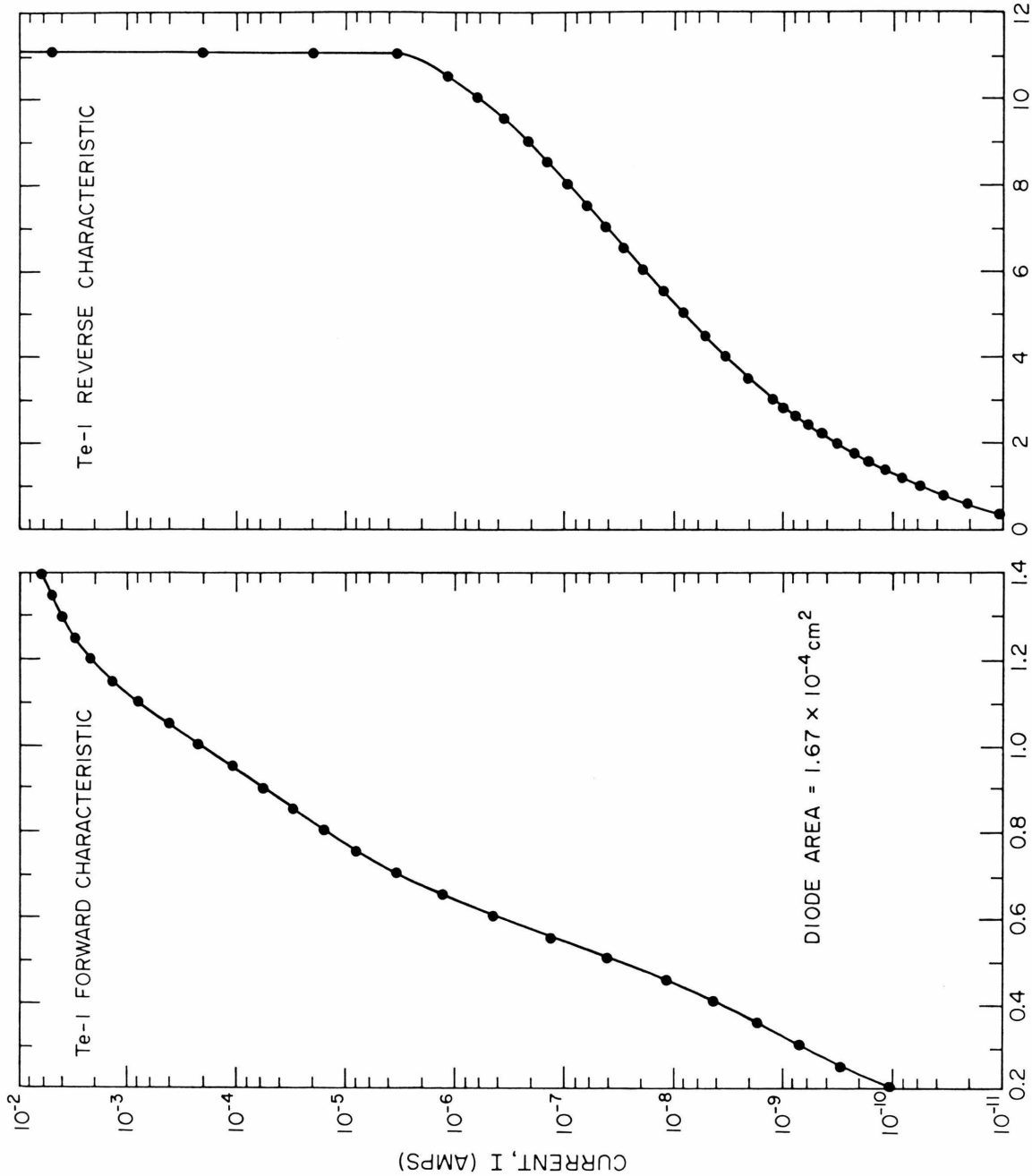


Fig. 14 Current-voltage characteristics of an ion implanted diode (Te-1).

Table V

Summary of the Electrical Properties of Tellurium Implanted GaAs

Sample No.	Implant Dose (cm^{-2})	Anneal Overcoat	Surface Carrier Concentration (cm^{-2})	Effective Mobility (cm^2/V-sec)	Junction Grading (cm^{-4})	Forward I-V Slope[b] (n)
Te-4	$3x10^{13}$(a)	Si_3N_4	$6.6x10^{12}$	1984	$2.3x10^{22}$	1.16
Te-2	$1x10^{14}$(a)	Si_3N_4	$7.2x10^{12}$	1389	----	----
G-74	$1x10^{14}$	Si_3N_4	$2.0x10^{13}$	1498	$3.1x10^{22}$	1.15
G-80	$1x10^{14}$	Si_3N_4	$1.3x10^{13}$	1350	----	----
Te-1	$3x10^{14}$	Si_3N_4	$1.2x10^{13}$	1538	$4.5x10^{22}$	2.0
Te-3	$3x10^{13}$(a)	AlN	$1.8x10^{13}$	1664	$2.7x10^{22}$	1.18
Te-5	$1x10^{14}$(a)	AlN	$3.1x10^{13}$	1371	$2.9x10^{22}$	1.21
Te-19	$1x10^{14}$(a)	AlN	$2.6x10^{13}$	1158	----	----
Te-6	$3x10^{14}$	AlN	$4.0x10^{13}$	1166	$2.5x10^{22}$	1.16

(a) For these samples, an additional implant was made at 60 keV with a dose one-third of the 220 keV dose given.

(b) $I = I_o \exp(qV/nkT)$.

The excess current cannot be attributed to periphery leakage since in all cases the forward current scaled as a function of junction area. The reverse characteristics were of varied quality. Some had better reverse characteristics (for example, Te-1 in Fig. 14) than diffused structures of similar substrate doping.[60] Others, however, had high leakage currents and low breakdown voltages. Since the leakage was mostly junction area dependent, the deep penetration of the Au-Ge contacts may have been the cause of these poor characteristics.

Figure 15 shows a scanning electron microscope photograph of the cleaved edge of one of the ion implanted diodes. The upper right portion of the field of view is the Au-Ge contact on the top surface of the diode. On the cleaved edge, several fingers of alloyed Au-Ge can be seen to penetrate to depths of 1200Å or more. The junction does not show up clearly in Fig. 15, but it is located 2200Å ± 200Å deep in the GaAs. If the junction region were not heavily doped, a low voltage breakdown would occur as the depletion layer approached the alloyed Au-Ge.

The photoresponse of a reversed biased implanted diode is shown in Fig. 16. Measurements were performed using a Cary spectrometer modified to generate a uniform photon flux as a function of wavelength. The sharp response at 9000Å is typical for a GaAs photodiode, however the peak is usually quite narrow.[61] At wavelengths lower than 9000Å GaAs becomes highly absorbent. As a result, the electron-hole pairs generated by light absorption are located near the detector surface and usually recombine before reaching the junction region.

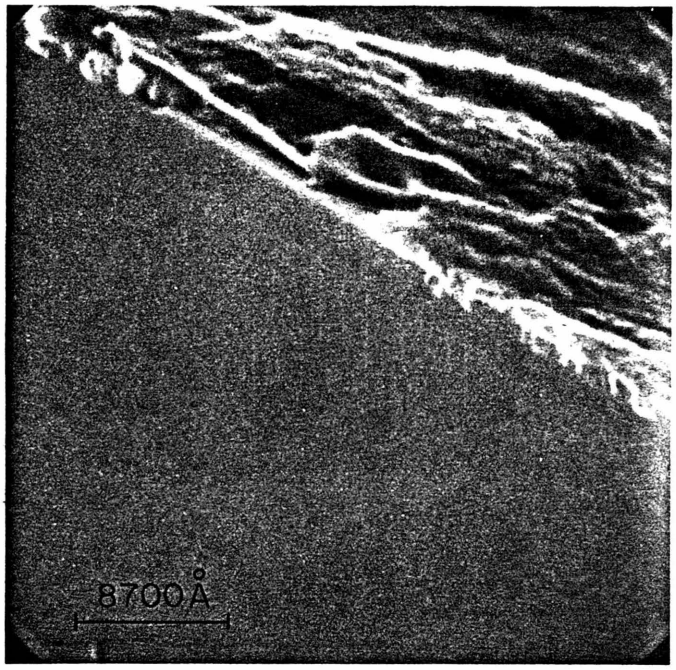


Fig. 15 Scanning electron microscope photograph of the cleaved edge of an ion implanted diode (Te-1).

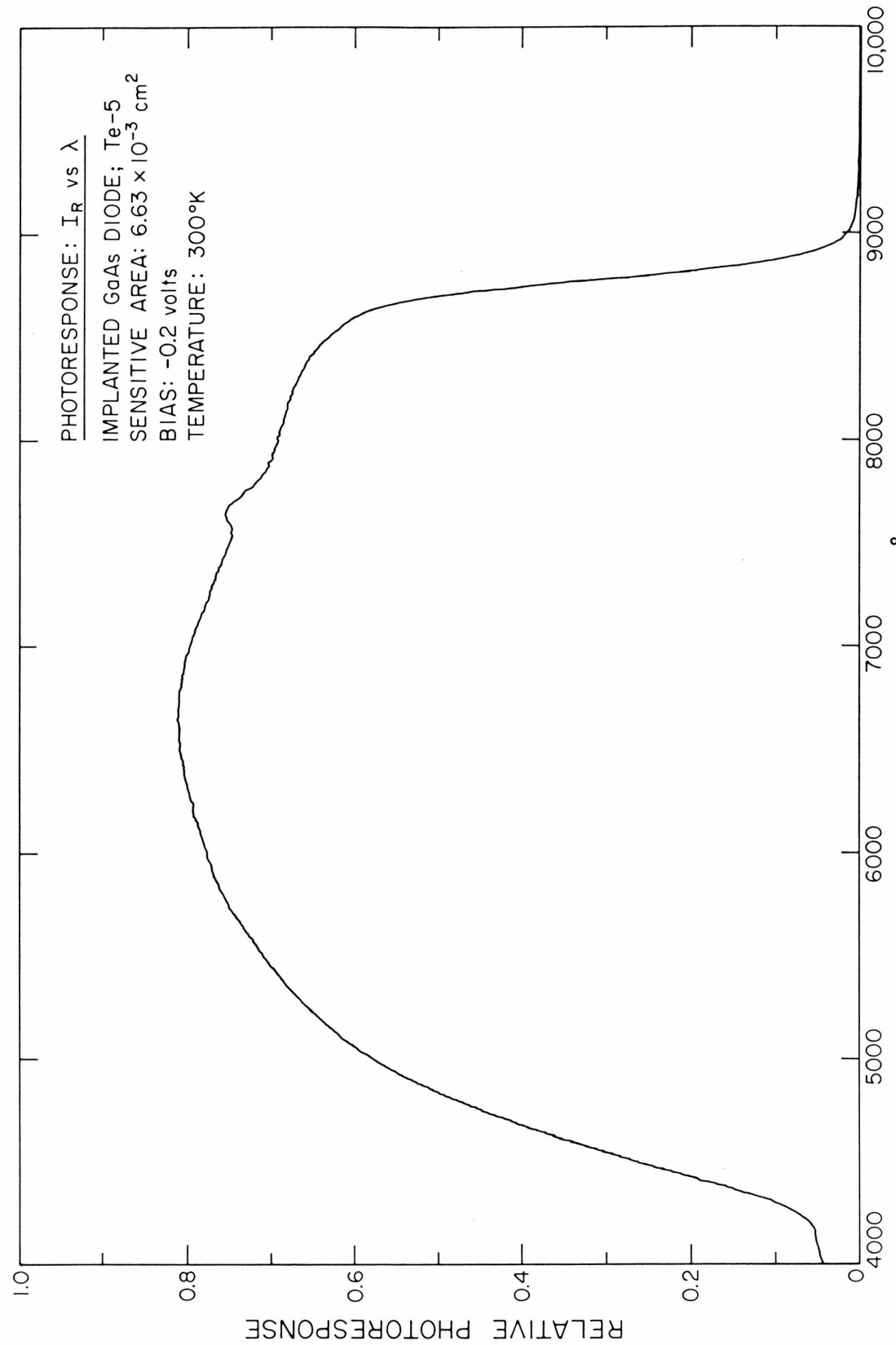


Fig. 16 Photoresponse of a reversed biased ion implanted diode (Te-5).

In contrast, the implanted diode has a broad photoresponse peak extending from 9000Å to 4000Å which is attributed to its shallow junction depth.

Capacitance-voltage measurements indicated that all the junctions were linearly graded with no evidence of intrinsic layers. The C-V characteristics of two implanted diodes are presented in Fig. 17. The diodes were prepared identically except one was overcoated with AlN before anneal and the other Si_3N_4. In both cases the $1/C^3$ vs. V curves are linear, characteristic of linear graded junctions. Slope calculations[62] yield a grading of $2.5 \times 10^{22}/cm^4$ for the AlN sample (Te-6) and $4.5 \times 10^{22}/cm^4$ for the Si_3N_4 specimen (Te-1). The results for other samples are summarized in Table V. It is interesting to note that there is no large discrepancy in the grading values between the AlN overcoated samples and the Si_3N_4 covered samples.

The surface carrier concentration and effective mobility in the implanted layers are listed in Table V. The doping efficiency ranges from a few percent up to 45% with the AlN overcoated samples generally having higher efficiencies than the Si_3N_4 coated samples. In addition, the AlN overcoated samples have surface carrier concentration values that increase with increasing dose, while the Si_3N_4 values show some scatter.

The carrier concentration and mobility profiles for an implanted sample overcoated with Si_3N_4 are shown in Fig. 18. Sequential Hall measurements in conjunction with layer removal were used to determine the carrier profile to a depth within a 1000Å of the implanted

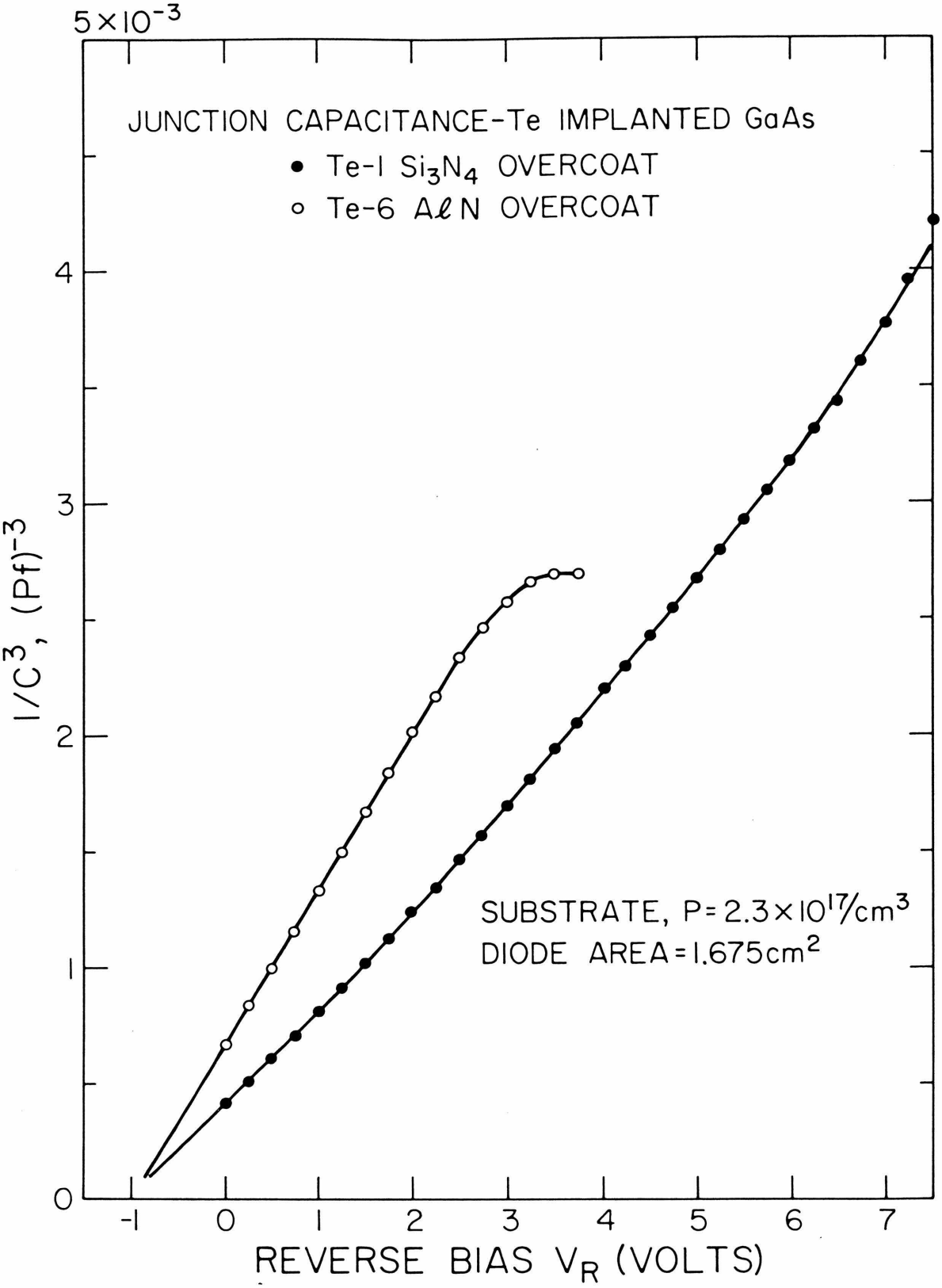


Fig. 17 Capacitance-voltage characteristics of two ion implanted diodes.

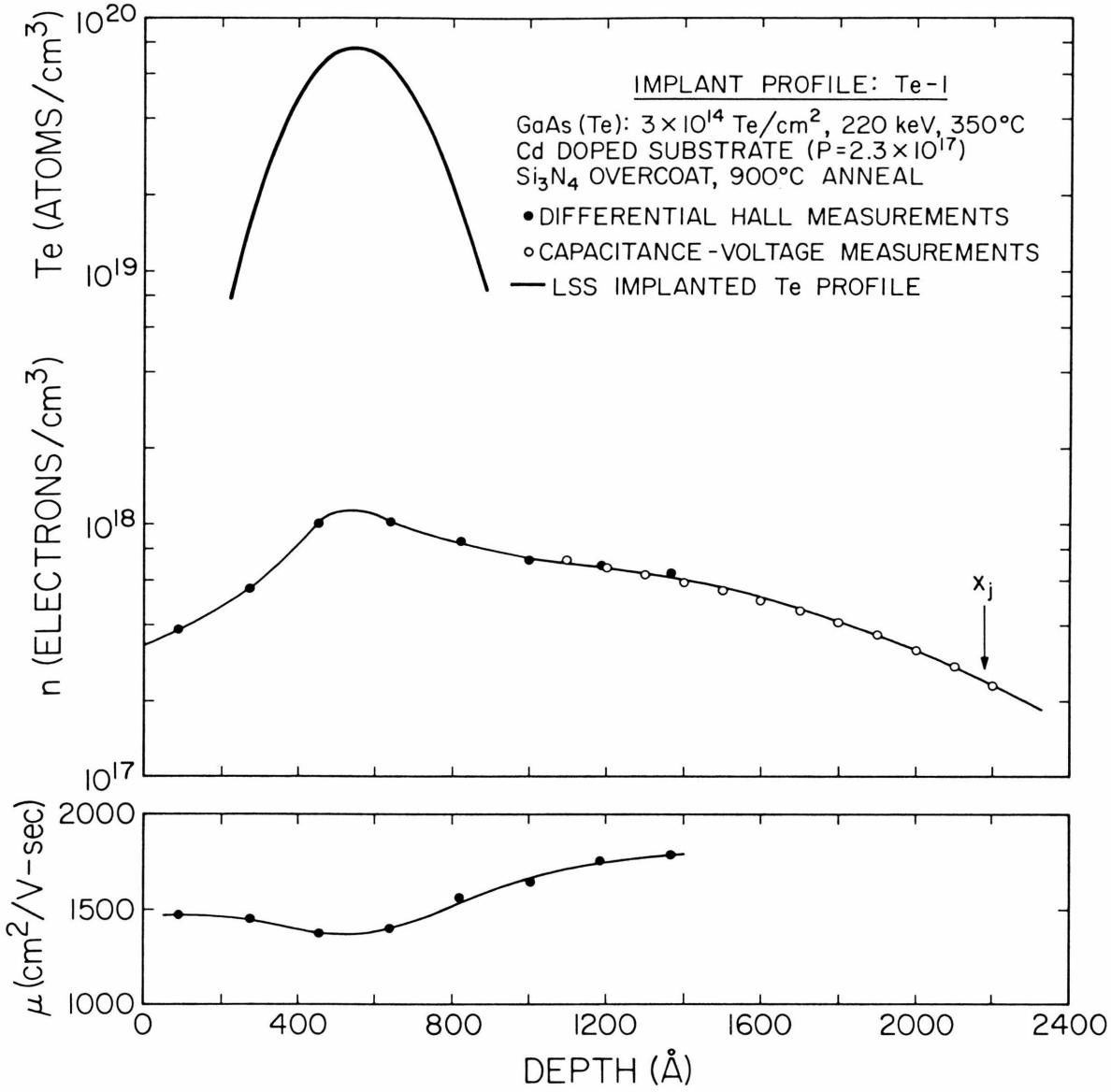


Fig. 18 Electron concentration and mobility profiles for a tellurium implanted sample processed with a Si_3N_4 coating during anneal.

junction. Slope analysis of the capacitance-voltage data (Fig. 17) produced a carrier concentration profile referenced to the junction depth and the substrate doping level. By using the SEM value of 2200Å as the junction depth and a substrate doping of 2.3×10^{17} holes/cm^3, the C-V data were coupled with the differential Hall effect data to generate a carrier concentration profile extending from the surface to the junction depth. The match of C-V carrier profile (open circles) to the Hall effect carrier profile (filled circles) is additional evidence that no intrinsic region exists in the implanted layer.

The depth of the implanted carrier peak agrees closely with the value of 550Å predicted by Lindhard, Scharff, and Schiøtt (LSS) theory[55] for 220 keV tellurium implanted GaAs. However, the peak carrier concentration is markedly lower than the LSS value (solid line in Fig. 18) and the carrier profile exhibits a tail extending deep into the sample. This tail is an order of magnitude greater than that predicted by simple diffusion of tellurium during the anneal.[63] Similar tails were observed in GaAs implants by Sansbury et al.,[42] and attributed to radiation enhanced diffusion.

The mobility in the implanted layer is significantly lower than that expected for epitaxial GaAs layers of equal carrier concentration.[64] The low mobility may be a result of carrier scattering from residual radiation effects such as dislocations and atomic defects.

Figure 19 presents the profile of an identical implant processed with AlN encapsulent. In this case, the Hall effect

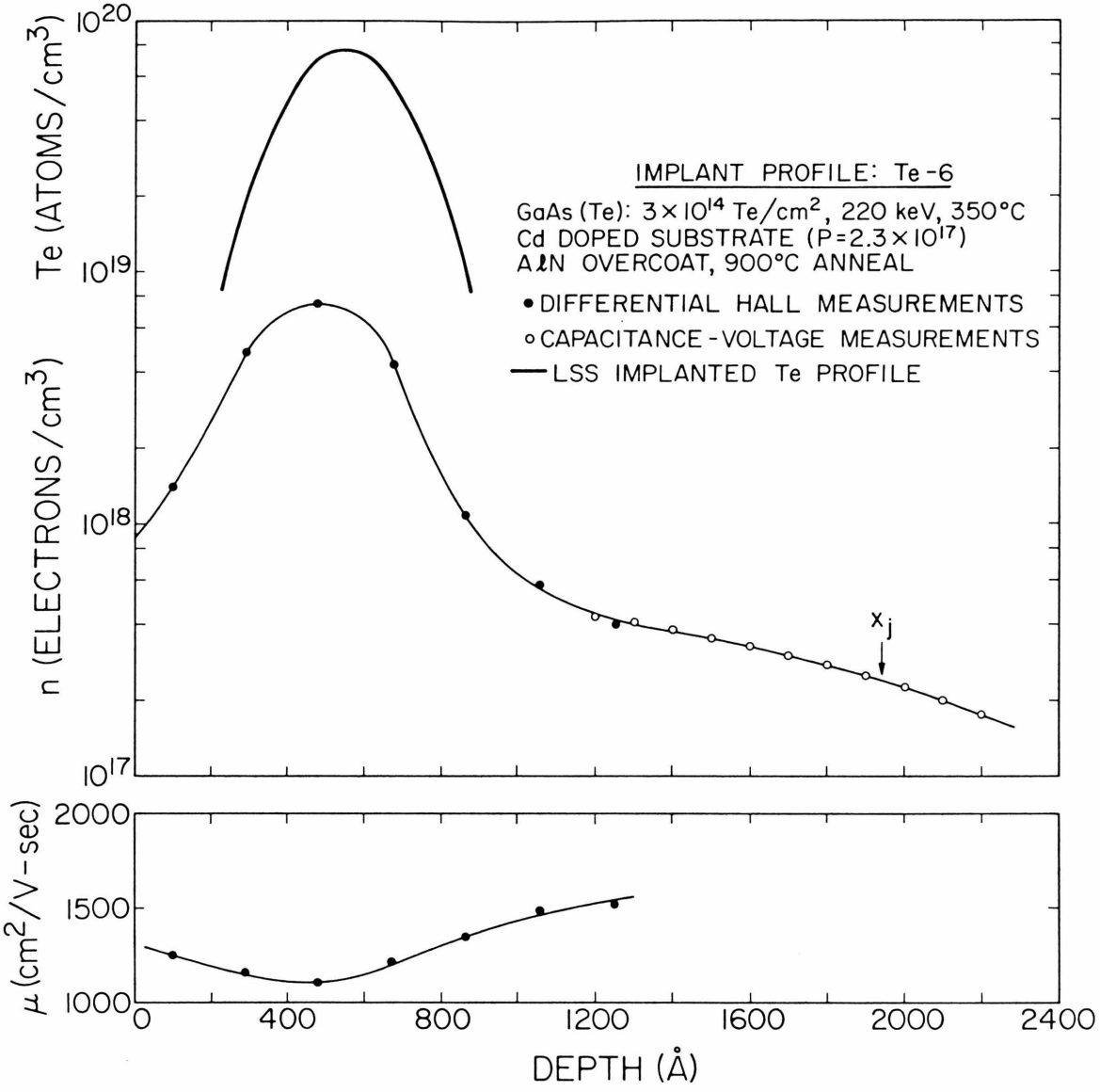


Fig. 19 Electron concentration and mobility profiles for a tellurium implanted sample processed with an AlN coating during anneal.

profile and C-V profile were matched by slope without the aid of a junction depth measurement. The carrier profile exhibits a significantly higher peak electron concentration than that of the previous sample. The peak value of 7×10^{18} electrons/cm^3 is equal to the maximum electron concentration which has been attained by doping GaAs with tellurium during growth.[58] In addition, the penetrating component of the carrier concentration is not as pronounced as that of the Si_3N_4 overcoated sample.

Chapter 5

CONCLUSIONS

5.1 Summary of Results

The implantation of tellurium has been shown to create submicron n-type layers in GaAs with electron concentrations approximately equal to the maximum attainable in tellurium doped GaAs (7×10^{18} electrons/cm^3). Furthermore, a doping efficiency of 50% was achieved with the promise of higher efficiency for lower dose implantation. Implanted junctions showed no evidence of an intrinsic region which had plagued initial implantation efforts.

The implant procedure used by previous investigators (namely, room temperature implantation followed by anneal with a SiO_2 encapsulating layer) was shown to be inferior to hot substrate implantation with a subsequent anneal using a Si_3N_4 protective layer. By elevating the implant temperature we avoided the production of an amorphorous layer which seems to lead to lower electrical activity. Silicon nitride was chosen as the encapsulent since neither Ga or As diffuses through it at typical anneal temperatures. In contrast, Ga readily diffuses through SiO_2 and as a result gallium-vacancy-tellurium (V_{Ga}-Te) complexes were found in implanted layers annealed with a SiO_2 protective coating.

In an effort to improve the doping efficiency, the implant temperature was raised to 350° and the samples were annealed to 900°C with a Si_3N_4 coating. A doping efficiency of 50% was achieved with a carrier concentration approaching the maximum attainable in Te doped

GaAs. However, the electrical activity varied over a wide range for samples with identical implant conditions. The scatter in the electrical measurements was attributed to the poor adherence of the Si_3N_4 layers to the GaAs surface during the anneal.

In Chapter 4 the protective qualities of AlN were investigated. The maximum electrical activity achieved using an AlN encapsulent was comparable to the value attained using a Si_3N_4 coating. However, the electrical activity was consistently high for the AlN protected samples, in contrast to the scattered values observed for Si_3N_4 coated samples. Also, AlN displayed better adherence to the GaAs surface and superior protection against gallium out-diffusion during anneal than Si_3N_4.

In conclusion, it has been clearly demonstrated that by proper choice of the implant temperature and dielectric coating, electron concentrations close to those observed for bulk doped samples can be obtained.

5.2 Suggestions for Future Work

In light of these results, the implantation of other n-type dopants (S, Si, and Se) should be re-examined. The lighter atomic weight of these elements compared to Te would allow the production of much thicker n-type layers by implantation.

Further improvements in doping efficiency could be attained by changing the implantation procedure. Over the dose range studied in this work, the electrical activity remained fairly constant as a

function of dose. The highest doping efficiency (50%) was observed in the lowest dose implant (3×10^{13} Te/cm^2). To improve doping efficiency, the implantation of lower doses (10^{12} - 10^{13} Te/cm^2) should be investigated.

To optimize the implantation procedure, a study of electrical activity vs. implant temperature and anneal temperature should be performed as a function of dose. As a result of low dose implantation, samples will have reduced radiation damage and high temperature anneal may no longer be required.

Work should continue on investigating the protective qualities of dielectric encapsulents. To avoid the complications of implanted layers, experiments should be performed on GaAs substrates with a thin n-type epitaxial layer on the surface. Samples should be coated with the dielectric, annealed, and then analyzed. Measurements taken before and after anneal could be compared to evaluate the protective quality of the dielectric. Hall effect techniques could be used to measure the change in the surface carrier concentration and mobility in the epitaxial layer. Defects introduced during anneal could be detected by photoluminescence measurements. Scanning electron microscopy could be used to verify the adherence of the dielectric during anneal and ellipsometry measurements used to evaluate the dielectric index of refraction.

Also, it would be interesting to perform differential Hall effect measurements as a function of temperature on implanted GaAs samples. The Arrhenius plot of the carrier concentration would indicate the dopant ionization level and the amount of compensation present in the implanted layer. The corresponding curve of mobility would reveal information on the carrier scattering mechanism in the layer.

5.3 Applications

As mentioned previously, the industrial production of GaAs microwave transistors depends on the ability to create submicron n-type layers of GaAs. The maximum frequency of oscillation for a GaAs Schottky barrier field effect transistor (MESFET) depends critically on the uniformity of the channel layer thickness. Vapor phase epitaxial techniques, while successful in producing thin layers, are hard to control. On the other hand, ion implantation has been shown to be an accurate method of producing uniform layers of n-type GaAs and can easily be implemented for mass production. The natural extension of this application would be to integrate several MESFETs on the same substrate to form a microwave amplifier. Previously, this has been impractical because of low yield problems associated with the use of epitaxial layers.

In addition to the doping of active regions, ion implantation can be utilized to reduce GaAs contact resistance. For most devices it is essential to have the lowest resistance Ohmic contacts possible. The generation of excessive Ohmic heating limits the output power of such devices as laser diodes and Gunn oscillators. In

microwave devices like Schottky barrier field effect transistors (MESFETs), the cut-off frequency is limited by the device series resistance of which contact resistance is usually the dominant factor. The placing of n^+ contact regions on an epitaxial MESFET with channel doping of 10^{17} donors/cm^3 would reduce contact resistance by a factor of 100 over direct contact to the epitaxial layer.[65]

In closing, ion implantation may find application in the production of GaAs optoelectric devices. The fabrication of GaAs laser diodes is presently a very complicated process involving several epitaxial layers. Ion implantation would simplify the fabrication procedure and could result in better device characteristics. In addition, ion implantation could make a major impact on the light emitting diode (LED) industry. Diffusion techniques are currently being used to create the p-n junctions necessary for LED devices. However, ion implantation allows the fabrication of junctions with the n-type layer on the surface. Since the absorption coefficient for the characteristic radiation is 10 times less in n-type material than p-type GaAs,[66] the most efficient devices result from p-n junctions constructed with the n-type layer on the surface. High efficiency photovoltaic devices could also be fabricated by implantation in GaAs. The feasibility of such a device was demonstrated in section 4.2.

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