Precision at Scale:
System Design from Tiny Biosensors to Giant Arrays

Thesis by
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In Partial Fulfillment of the Requirements for the
Degree of
Doctor of Philosophy

CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California

2020
Defended July 24, 2020

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To Kim, my love,
to our beloved children,
and to our loving extended family.

ACKNOWLEDGEMENTS

There is a popular saying that it takes about 10,000 hours of deliberate practice to master a field. The average Caltech graduate student who works 60-80 hours a week throughout the year and graduates in an average of 5.6 years, completes about *twice* as much hours of training. Besides the impressive result of graduating as a master expert, undertaking such an endeavour is nearly impossible without a supporting circle of family, management, colleagues and friends who deserve special thanks.

First and foremost I would like to thank my loving wife Kim. In truth, this thesis would probably not have been written if she hadn't encouraged me to apply to Caltech's graduate program. She stood by my side through the transition to a foreign country and through exams, deadlines, and sleepless tapout nights, while making sure that our family and house remain functioning. She is an equal partner to this achievement; I couldn't have done this without her. Our beloved sons Ivri and Uri also deserve my thanks for being a part of this journey. I hope that one day they will remember with a smile the time that they spent with their father in lab, probably more time than the average undergraduate student does.

I am grateful to my advisor, Prof. Ali Hajimiri for the opportunity to work in his research group. It is not trivial to admit an older student with a family, who might turn out to be less productive due to additional commitments. Ali is, of course, an expert in his field, but he holds several other qualities that are less commonly found in academic advisors. It is his saying that in his lab he trains leaders. Indeed, from him I learned that it is not always enough to be technically capable of executing a task: it is the *purpose* behind an idea, the justification, and foresight of potential expansions that matter. From him I learned that by doing so, I can harness people and resources to achieve meaningful goals. While other electrical engineering groups research contemporary problems, Ali is always looking into the future, and this made the experience of working for him unique. His view and advice on personal and professional matters were always insightful, and have taught me an important lesson in decision-making. I am proud to have him as my mentor.

I would also like to thank my thesis committee, Prof. Azita Emami, Sander (Sandy) Weinreb and Alireza Marandi for taking the time and patience to participate in my candidacy and defense presentations. The latter was scheduled amidst the COVID-19 pandemic and I greatly appreciate their willingness to attend despite the many

disturbances to their research, family, and life routines.

I was fortunate to be a part of Caltech's Space Solar-Power Program, and to see the innards of a truly ambitious project to send huge power-transmitter satellites into space. I would like to thank all the participating groups and our collaborators for the insightful interaction. I had the pleasure of working closely with Drs. Florian Bohn, Behrooz Abiri, and Amir Safaripour, as well as Austin Fikes and Mohith Manohara. I wish to thank them for the fruitful technical discussions, help, and guidance which were invaluable to completing my Ph.D. work.

I also wish to thank my colleagues from our lab who were a significant part of my social and academic life here: Prof. Constantine Sideris, Dr. Alex Pai and Dr. Brian Hong, Aroutin Khachaturian, Reza Fatemi, Parham Khial, and Elliott Williams. Some of the funniest and most fun moments happened with them in and out of the lab, in between our work assignments. I had the pleasure of collaborating with Craig Ives and Armina Khakpour and I would like to wish them the best of luck in their future work. I want to thank all the other lab member in the past and present that I had the honor to meet and work with: Dr. Kaushik Dasgupta, Dr. Reza Hashemi, Dr. Fatemeh Akbar (Noyan), Oren Mizrahi, Samir Nooshabadi, Ailec Wu, Alex White, Garret Sullivan and Stephan Turkowski. Dave Hodge deserves special thanks for keeping our equipment and lab running in an orderly manner despite the students elaborate attempts to destroy them.

My work here wouldn't have been possible without a broader circle of social support. Our Israeli scholars and faculty friends helped us to feel a little bit closer to home. We also formed friendships with several of our children's families and I would like to thank them all. I would also like to dedicate special thanks to the Children's Center at Caltech which was a pillar of stability and security through these years. If not for them, I probably wouldn't have been able to complete my academic duties during the COVID-19 pandemic.

Last, but not least I would like to thank our extended family who were a part of this journey. To our parents Ishay and Ayala Katziri and Soli Banaji, and my grandmother Tzvia, who supported us form near and afar. To my late biological father Yaakov Gal who never had the opportunity to see me earn my Ph.D., and to Kim's mother Marian Eichorn. To our loving brothers and sisters Omer, Alona, Einav, Yael, Lilach and their families. To our family in Pasadena Amy, Dave, Jeff and Allie, and to our cousins from LA Hedy, Jerry, Marge, Richard and Lois, who did everything they could to make us feel at home here in the US.

ABSTRACT

In order to change the world, technological advancements must be made affordable and available for the general public to use. In other words, we must be able to *scale* our inventions effectively. Silicon integrated circuits are crucial components in scaling electronic systems because they are mass producible and offer a phenomenal cost-to-complexity ratio. This thesis summarizes the author's work on highly scalable sensor and array systems. It presents three high precision systems, that demonstrate how the use of highly functional radio-frequency integrated circuits enables the realization of previously unfeasible architectures.

PUBLISHED CONTENT AND CONTRIBUTIONS

[1] B. Abiri *et al.*, "A lightweight space-based solar power satellite," *Proceedings of IEEE, **In Review***, 2020.
M.G. was a part of the RF electronics team that developed the RFIC and flexible tile structure.

[2] M. Gal-Katziri, A. C. Fikes, F. Bohn, B. Abiri, M. Hashemi, and A. Hajimiri, "Scalable, deployable, flexible phased array sheets," in *2020 IEEE MTT-S International Microwave Symposium (IMS)*, 2020.
M.G. designed parts of the RFIC, was a partner in the system integration, assembled the flexible array, and carried its measurements.

[3] A. Hajimiri *et al.*, "Dynamic focusing of large arrays for wireless power transfer and beyond," *IEEE Journal of Solid-State Circuits, **In Review***, 2020.
M.G. designed parts of the RFIC, worked on the programming interface between the unit cells to a central controller, and wrote an FPGA hardware interface from the main controller to the array sub-units.

[4] M. Gal-Katziri and A. Hajimiri, "Analysis and design of coupled inductive bridges for magnetic sensing applications," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 1883–1894, 2019. DOI: https://doi.org/10.1109/JSSC.2019.2907196.
M.G. developed the generalized concept of energy storage shift, carried analysis, designed and measured a magnetic bridge sensor IC.

[5] M. R. M. Hashemi *et al.*, "A flexible phased array system with low areal mass density," *Nature Electronics*, vol. 2, no. 5, pp. 195–205, May 2019, ISSN: 2520-1131. [Online]. Available: https://doi.org/10.1038/s41928-019-0247-9.
M.G. designed parts of the RFIC and was a partner in the tile design and integration.

[6] M. Gal-Katziri and A. Hajimiri, "A coupled inductive bridge for magnetic sensing applications," in *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, Sep. 2018, pp. 342–345. DOI: https://doi.org/10.1109/ESSCIRC.2018.8494313.
M.G. developed the sensor concept, designed the chip, carried out measurements, and presented the material.

[7] E. Gdoutos *et al.*, "A lightweight tile structure integrating photovoltaic conversion and rf power transfer for space solar power applications," in *2018 AIAA Spacecraft Structures Conference*. 2018. [Online]. Available: https://arc.aiaa.org/doi/abs/10.2514/6.2018-2202.
M.G. was a part of the RF electronics team that developed the RFIC and flexible tile structure.

[8] M. D. Kelzenberg *et al.*, "Ultralight energy converter tile for the space solar power initiative," in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)*, 2018, pp. 3357–3359. DOI: https://doi.org/10.1109/PVSC.2018.8547403.
M.G. was a part of the RF electronics team that developed the RFIC and flexible tile structure.

[9] M. Gal-Katziri and A. Hajimiri, "A sub-picosecond hybrid DLL for large-scale phased array synchronization," in *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2018, pp. 231–234. DOI: https://doi.org/10.1109/ASSCC.2018.8579340.
M.G. developed the hybrid loop concept, and fabricated and measured the DLL IC.

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NOMENCLATURE

CMOS. silicon complementary metal-oxide semiconductor.

EIF/EOF. "Operation Iraqi/Enduring Freedom" - An acronym that refers to the U.S.-led conflict in Afghanistan and Iraq.

EM. Electromagnetic.

GEO. Geosynchronous equatorial orbit at an altitude of 35,000 km (22,000 miles) above earth.

IC. Integrated Circuit.

ILFD. Injection-Locked Frequency Divider.

JP8. Jet propulsion fuel, specified and used widely by the US military.

LCOE. Levelized Cost of Electricity.

LEO. Low earth orbit at an altitude between 160 to 2,000 km (99 to 1,200 miles) above earth.

LNA. Low Noise Amplifier.

PA. Power Amplifier.

PD. Photo Diode.

PLL. Phase-Locked Loop.

PPF. Poly Phase Filter.

PS. Phase Shifter.

PSD. Power Spectral Density.

PV. Photovoltaic.

RFIC. Radio Frequency Integrated Circuit.

SBP. Space Based Power.

SSP. Space Based Solar Power.

TIA. Transimpedance Amplifier.

VCO. Voltage Controlled Oscillator.

Chapter 1

INTRODUCTION

Had we told a mid-19th century scholar that within a hundred years our life expectancy would more than double, that a man would walk on the moon, and that we would be able to light entire cities by the flip of a switch, he would have laughed in our face, called us madmen, or at least asked for some of that recreational substance we had been consuming after the siesta. Yet within a century, humankind achieved all those and more: Our food production has increased by an order of magnitude, we drive cars that are faster than a cheetah and can go over a longer distance, and we are able to respond and combat new diseases at an admirable speed through a truly global collaborative effort. This last achievement is one that we are currently experiencing as the COVID-19 pandemic threatens to hurt millions around the globe and paralyze economy and society alike. All of these remarkable achievements have one thing in common: they have been enabled by the technological breakthroughs of mathematicians, physicists, chemists, biologists, engineers, and other highly skilled professionals.

Technology, however, is necessary but insufficient for a discovery to change the world. A key ingredient in the process is its democratization - or *scaling*, in the scientific jargon - which is the process by which it is made accessible for the general public's use. We light our homes and operate our household items because the cost of a light-bulb is around one dollar and electricity is cheaper than a quarter for a kWh. We are not starving because a pound of rice can be produced and sold for a few dozen cents, and we can battle viral infections because we can manufacture and disseminate hundreds of millions of vaccines globally.

In this regard, it appears that there has never been an enabler of scaling in the history of electronics quite like the integrated circuit, which allows to reliably mass-produce complex, miniaturized systems. Of these, silicon complementary metal-oxide semiconductor (CMOS) fabrication processes deserve a place of honor. While they do not offer the highest performance, the low cost of fabrication and rapid shrinking of technology nodes deliver an astounding value in cost-to-complexity ratio. Not only can complete systems and networks (SoCs, NoCs) be implemented on a single chip, but also CMOS ICs enable the realization of previously unfeasible

and uneconomical architectures.

This thesis summarizes my work at Caltech on two such types of systems: magnetic biosensors and flexible, very large-scale phased arrays. Though seemingly disconnect, they are both fantastic examples of the way that CMOS integrated circuits enable the scaling of electronic systems in several contexts to create paradigm-shifting architectures. Integrated biosensors can be fabricated at low cost to offer multi-modal, multi-channel building blocks for on-site diagnostics and mass producible analysis instruments. One great advantage is that their signal conditioning and processing circuitry can be integrated on-chip not only to reduce their size, cost and power consumption, but also to allow modalities that are impractical otherwise, such as very high frequencies of operation. Very large-scale phased arrays, on the other hand, *must* utilize highly mass-producible technologies in order to be rendered suitable for most consumer applications. In particular, phased arrays implemented on flexible substrates are arguably unfeasible without taking advantage of highly functional parts, capable of self synchronization, calibration and regulation. This, to account for vibrations and deformation with a small component count to maintain the system's physical flexibility.

While a large part of the thesis body deals with the design of radio-frequency integrated circuits, it is important to note that substantial attention is given to the fundamental justification of the concepts and to quantitative system-level considerations. This is done for two reasons. First, as an engineer, I believe that systems should be designed to be both sound and useful. Second, both biosensors and large phased arrays require a high level of precision, for example in the sensitivity of a sensor or in the quality of a clock synchronizing numerous array elements. These can only be achieved with a deep understanding of *quantitative* considerations which should not be oversighted. For these reasons, each of the thesis chapters start with a substantial theoretical background, putting it in the context of the field to which it pertains.

The thesis organization is as follows: the first chapter studies the underlying physics of inductance shift sensors as a special case of the broader family of magnetic energy deviation sensors. The result is a quantitative definition of performance metrics with all assumptions and approximations explicitly stated. The analysis is then used to design a modified ac Wheatstone bridge that uses two inductor pairs in a cross-coupled configuration, to half its size and double its transducer gain while maintaining a fully differential structure with a matched frequency response. Finally,

the measurements of a proof-of-concept sensor are presented and discussed. The second chapter presents my work on very-large scale arrays as a part of Caltech's solar-space power program (SSPP). First, an analysis of the economics of solar-space power is presented and its implications discussed. Then, an overview of the proposed SSPP architecture is given. Later, three levels of the work of the SSPP RF-electronics group - with my contribution as a part of it - are presented: First, a phased array driver RFIC is presented, which is at the heart of the energy conversion system to perform most of the system's task in a cost-effective and modular fashion. Second, the RFIC is used to design a scalable and modular RF-photovoltaic power conversion phased array unit-cell on a flexible PCB substrate. And lastly, sixteen of these unit cells patterns are combined to build a single-sheet, flexible, 256-elements phased array. The third and final chapter presents a novel approach to synchronize RF phased arrays with a laser. It discusses the theoretical background and the quantitative trade-offs of several clock synchronization schemes. A novel mm-wave phased RFIC with an integrated photodiode for clock synchronization purposes is then presented. Notably, this section discusses only the RFIC simulated expected performance, since the chips were just recently fabricated and were not yet measured.

I wish the readers to enjoy reading through this thesis, and I hope that they will find it interesting and inspiring.

Chapter 2

ANALYSIS AND DESIGN OF MAGNETIC ENERGY-DEVIATION SENSORS

Magnetic sensors are often proposed as a miniaturized, low-cost alternative to fluorescence for cell-sorting and on-site diagnostics applications [1][2]. Many of these systems sense changes in relative permeability to detect biological material bound to magnetic particles (beads) within the sensing area. The integration of susceptibility sensors on a single chip is appealing since it offers mass-producibility and allows the addition of significantly more complex functionality in comparison to discrete solutions. A major challenge with on-chip implementations, however, is the required sensitivity. For instance, cytometers need to be able to detect single cells[3], and hand-held diagnostics devices might have to sense concentrations as small as a few parts per million of material in a sample [4]. So far, the most sensitive devices demonstrated have used inductors as a magnetic sensor, with different trade-offs. Frequency shift oscillators [5] are compact and have the highest sensitivity, but suffer from oscillator long-term drift [6][7]. Integrated transformers on the other hand [8][9] are more suitable for cell sorting applications, but use additional tuning inductors to achieve their required single bead sensitivity. In addition, the physical implementations of these systems rely on an intuitive approach, often with only qualitative prediction of performance metrics. This chapter presents a more quantitative method. First, a deeper understanding of the underlying physics of susceptibility sensors is developed, which provides a systematic design technique and allows to discuss the special case of inductive shift sensing with all assumptions and approximations explicitly stated. Then, several types of inductive shift sensors will be presented, including a novel sensor based on a compact differential coupled inductive bridge. Later, the new sensor topology will be presented, and it will be shown how it offers a response time similar to transformer-based sensors and a sensitivity comparable to frequency shift oscillators. Finally, an on-chip coupled bridge integrated sensor will be demonstrated alongside a quantitative discussion of measurement results.

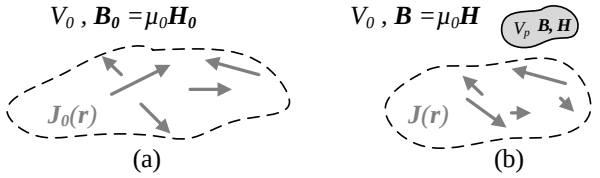


Figure 2.1: Arbitrary current density in volume V_0 (a) with, and (b) without a magnetic particle V_p in the volume.

2.1 Magnetic Susceptibility Sensors

Magnetic susceptibility sensors are designed to sense changes in the relative permeability in space. Traditionally, they are regarded as inductors with an inductance that shifts in the presence of magnetic material. While useful for practical circuit design, this viewpoint obscures the true nature of those devices and might limit designers to a specific subset of physical implementations. Fundamentally, susceptibility sensors are *magnetic energy storage elements* and the sensed quantity is the change in stored magnetic energy due to a magnetic perturbation.

Magnetic energy deviation sensors

A magnetic sensor can be thought of as an arrangement of current densities $\boldsymbol{J_0}(\boldsymbol{r})$, as in Fig. 2.1a (bold variables are ***vectors***). These currents induce a magnetic field $\boldsymbol{B_0}(\boldsymbol{r})$ in the volume V_0, which stores magnetic energy, U_{B0}, of

$$U_{B0} = \frac{1}{2} \int_{V_0} \boldsymbol{H_0} \cdot \boldsymbol{B_0} dv. \tag{2.1}$$

If the medium is isotropic and $\boldsymbol{B_0}$ is linear with respect to $\boldsymbol{H_0}$, the two can be related by

$$\boldsymbol{B_0} = \mu_0 \boldsymbol{H_0}. \tag{2.2}$$

We now introduce a magnetic particle, with volume V_p into V_0 (Fig. 2.1b). In general, the original currents and fields will change their value to $\boldsymbol{J}(\boldsymbol{r})$, $\boldsymbol{B}(\boldsymbol{r})$, and $\boldsymbol{H}(\boldsymbol{r})$ in order to fulfill Maxwell's equations in its presence. The modified stored magnetic energy U_B can then be found from solving Maxwell's equations again and applying the new fields to (2.1). However, if we assume that the current distribution $\boldsymbol{J_0}(\boldsymbol{r})$ is far away enough such that it does not change significantly in the presence of the added particle, and that the particle was unmagnetized before it was entered to V_0, an approximate solution is given in [10]. Suppose that before V_p was introduced

into V_0, the currents $\boldsymbol{J_0}(\boldsymbol{r})$ in Fig. (2.1a) were reduced to 0. Then, with V_p in V_0, those currents are increased back until $\boldsymbol{J}(\boldsymbol{r}) = \boldsymbol{J_0}(\boldsymbol{r})$. The work W done to recreate $\boldsymbol{J_0}(\boldsymbol{r})$ is

$$W = \int_{V_0} dv \int_0^{\boldsymbol{B}} \boldsymbol{H} \cdot d\boldsymbol{B}, \tag{2.3}$$

and the excess energy stored by the particle is

$$\Delta U_B = W - U_{B0}. \tag{2.4}$$

Substituting (2.1) and (2.3) into (2.4) and separating integrals leads to

$$\begin{aligned} \Delta U_B = \frac{1}{2} \int_{V_0 - V_p} (\boldsymbol{H} \cdot \boldsymbol{B} - \boldsymbol{H_0} \cdot \boldsymbol{B_0}) dv \\ + \int_{V_p} dv \left(\int_0^{\boldsymbol{B}} \boldsymbol{H} \cdot d\boldsymbol{B} - \frac{1}{2} \boldsymbol{H_0} \cdot \boldsymbol{B_0} \right). \end{aligned} \tag{2.5}$$

Assuming that (2.2) holds and using boundary conditions [10] shows that the integration over $(V_0 - V_p)$, outside the particle, is proportional to an integral over V_p. Furthermore, by neglecting hysteresis effects and assuming that inside V_p, $\boldsymbol{B} = \mu \boldsymbol{H}$, the change in stored magnetic energy can be written as

$$\Delta U_B = \frac{1}{2} \int_{V_p} \boldsymbol{M} \cdot \boldsymbol{B_0} dv. \tag{2.6}$$

It is noteworthy that the stored magnetic energy due to a magnetic particle in space depends only on $\boldsymbol{M}(\boldsymbol{r})$, the magnetic polarization, and $\boldsymbol{B_0}(\boldsymbol{r})$ inside V_p. This sets the theoretical foundation to analyze magnetic susceptibility sensors.

Energy deviation induced by magnetic nanoparticles

Magnetic beads are made of ferromagnetic nano-scale particles embedded in a non-conductive matrix. Even though their internal structure can be complex and vary between manufacturers, they are commonly modeled and characterized as paramagnetic material[11][12], where, for weak magnetic fields,

$$\boldsymbol{B_p} = \mu_p \boldsymbol{H_p} = \mu_0 (1 + \chi) \boldsymbol{H_p}. \tag{2.7}$$

Here μ_0 is the vacuum permeability, χ is the bead effective (unit-less) susceptibility, and subscript p refers to the region inside the particle. Since the magnetic properties

stem from ferrites, χ is typically $\sim 10^{-1}$, orders of magnitude larger than regular paramagnetic materials. The phenomenon is referred to as superparamagnetism. A magnetic bead will be magnetized if placed in a static, constant magnetic field $\boldsymbol{B_0}(\boldsymbol{r})$, and $\boldsymbol{M}(\boldsymbol{r})$ is calculated in [13] to be

$$\boldsymbol{M} = \frac{3}{\mu_0}\left(\frac{\mu_p - \mu_0}{\mu_p + 2\mu_0}\right)\boldsymbol{B_0}. \tag{2.8}$$

It is noteworthy that integrated magnetic sensors usually operate at radio frequencies where the electromagnetic fields are not static. However, their inductors are usually designed with dimensions much smaller than wavelength so they can be modeled as lumped elements and treated with a quasi-static approximation [14]. Even though integrated inductors store electric energy, manifested as parasitic capacitance, the phenomenon occurs mostly between the inductor surface and the bulk, whereas magnetic particles interact with the sensor above the chip surface. Therefore, the validity of (2.8) will be assumed for the following treatment.

If placed in an energy storage deviation sensor as defined in 2.1, the energy shift due to a magnetic bead can easily be calculated by substituting (2.8) into (2.6). If the bead is small enough such that the unperturbed magnetic field in its proximity is roughly constant, the integral can be simplified to

$$\Delta U_B \approx \frac{1}{2}\frac{3}{\mu_0}\left(\frac{\mu_p - \mu_0}{\mu_p + 2\mu_0}\right)|B_0|^2 V_p \tag{2.9}$$

with $|B_0|^2$ due to the vector dot product in (2.6). This result can be written in terms of χ and the magnetic energy density of the un-perturbed system, $u_{B0} = |B_0|^2/2\mu_0$, as

$$\Delta U_B \approx \left(\frac{3\chi}{\chi + 3}\right)u_{B0}V_p. \tag{2.10}$$

It is important to note that even though u_{B0} is considered constant in the proximity of the bead, it might still vary in space, as will become clear in 2.1.

Inductance shift sensors

As a special case, we can define the current densities $\boldsymbol{J_0}(\boldsymbol{r})$ as an assortment of current-carrying wires, I_k (Fig. 2.2) and define ΔU_B in terms of the change in L and M, the self- and mutual- inductances associated with each wire-pair. Under harmonic excitation in the quasi-static approximation, K wires store magnetic energy

of

$$U_{B0} = \frac{1}{2}\sum_{k=1}^{K} L_{k0} I_k^2 + \sum_{k=1}^{K}\sum_{l=k+1}^{K} M_{k0,l0} I_k I_l, \tag{2.11}$$

where L_{k0}, $M_{k0,l0}$ are their unperturbed self-, and mutual-inductances. The deviation in the stored magnetic energy is then proportional to the sum of all of the partial deviations ΔL_k, $\Delta M_{k,l}$, the change in L_{k0}, $M_{k0,l0}$, respectively, scaled by the current intensities, I_k:

$$(\frac{3\chi}{\chi+3}) u_{B0} V_p \approx \frac{1}{2}\sum_{k=1}^{K} \Delta L_k I_k^2 + \sum_{k=1}^{K}\sum_{l=k+1}^{K} \Delta M_{k,l} I_k I_l. \tag{2.12}$$

This result suggests that the spatial response profile of a magnetic energy deviation sensor may be engineered by appropriately arranging the generating current configuration. Exemplary synthesis objectives are maximizing the total deviation for a given power input, or producing a spatial uniform response, either on a surface or *vertically* along a microfluidic channel. A special case of (2.12) is when the arbitrary wire configuration in Fig. 2.2 consists of a single wire. Then, $I_1 = I$ and $I_2 ... I_k ... I_K = 0$, and the inductance shift is calculated to be

$$\Delta L \approx \frac{2}{I^2}(\frac{3\chi}{\chi+3}) V_p u_{B0}. \tag{2.13}$$

Interestingly, for typical superparamagnetic materials, $\chi \ll 3$, so

$$\Delta L \approx \frac{2}{I^2}\chi V_p u_{B0}. \tag{2.14}$$

A similar result was previously presented in [15] assuming only that the magnetic field, $\boldsymbol{H_0}(\boldsymbol{r})$, does not change in the presence of a small magnetic perturbation. Here we have shown how the latter holds only for small values of χ and only if the fundamental assumptions of 2.1 are fulfilled.

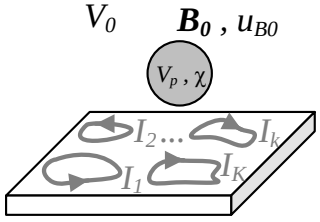


Figure 2.2: Magnetic bead with volume V_p and susceptibility χ in a space V_0 with an unperturbed magnetic energy density of $u_{B0} = B_0^2/2\mu_0$.

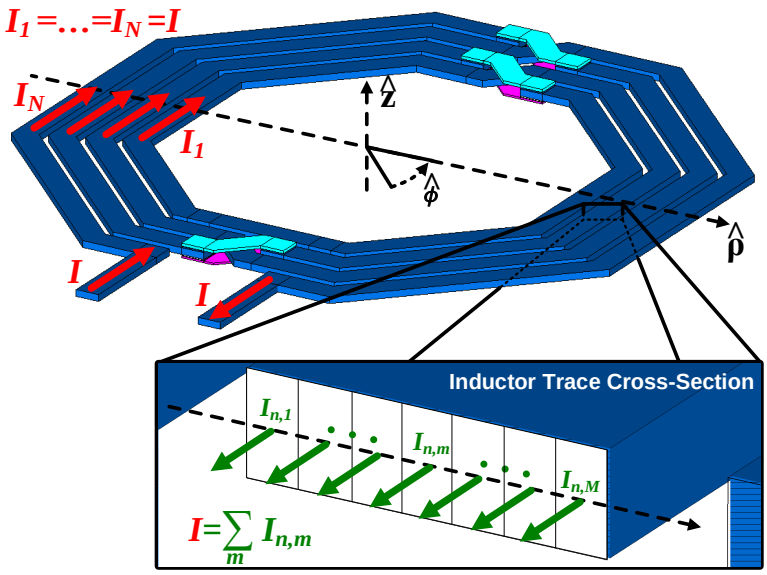


Figure 2.3: Planar inductor segmentation as one-dimensional current-loops.

Magnetic field of a planar spiral inductor

Since V_p and χ are known physical properties, the only information needed to define an inductor based magnetic-sensor response is its unperturbed energy density profile. Without loss of generality, we consider an N-turn *octagonal* inductor, and approximate it as an assortment of concentric circular loops, as shown in Fig 2.3. Each turn is modeled as M parallel one-dimensional loops, carrying currents of $I_{n,m} = I \cdot f_{n,m}, (1 \leq m \leq M, 1 \leq n \leq N)$. Although the currents in all the turns are equal ($I_1 ... I_N = I$) for inductors modeled as lumped components, the current distributions inside each of the turns generally are not, due to the skin effect, current crowding, or such. $f_{n,m}$ is an arbitrary scaling factor that was added in order to capture these secondary interactions. The magnetic field, $\boldsymbol{B}_{n,m}$, generated by each loop can be derived analytically from [13][16], and is most easily described in cylindrical coordinates. Due to the structural symmetry in ϕ, it depends only on the vertical and radial coordinates z and ρ, respectively, and has the following vector components:

$$\boldsymbol{B}_{n,m}(\rho, z) \approx \frac{\mu_0}{2\pi} \cdot \frac{I_{n,m}(\lambda_\rho \hat{\boldsymbol{\rho}} + \lambda_z \hat{\boldsymbol{z}})}{[z^2 + (\rho - a_{n,m})^2]\sqrt{z^2 + (a_{n,m} + \rho)^2}}, \tag{2.15}$$

with

$$\lambda_\rho = \frac{z}{\rho}[(a_{n,m}^2 + z^2 + \rho^2)E_2(k) - E_1(k)], \tag{2.16}$$

$$\lambda_z = [(a_{n,m}^2 - z^2 - \rho^2)E_2(k) + E_1(k)], \tag{2.17}$$

and

$$k^2 = 4\frac{\rho \cdot a_{n,m}}{z^2 + (a_{n,m} + \rho)^2}, \tag{2.18}$$

where $a_{n,m}$ is the loop radius, $E_1(k)$, $E_2(k)$ are elliptic functions of the first and second kinds, respectively, and $\hat{\boldsymbol{z}}$, $\hat{\boldsymbol{\rho}}$ are the vertical and radial field orientations, respectively. The total field of the inductor is the sum of all the fields that are generated by all the loops in all the traces:

$$\boldsymbol{B}(\rho, z) \approx \frac{\mu_0 I}{2\pi} \sum_{n,m} \frac{f_{n,m}(\lambda_\rho \hat{\boldsymbol{\rho}} + \lambda_z \hat{\boldsymbol{z}})}{[z^2 + (\rho - a_{n,m})^2]\sqrt{z^2 + (a_{n,m} + \rho)^2}}. \tag{2.19}$$

An important result of this calculation is that the magnetic field $\boldsymbol{B}$ is proportional to the inductor current, I. Hence, $u_B \propto I^2$, and the inductance shift in (2.13) is to the first order *independent of the excitation current*. In practice, setting $f_{n,m} = 1/M$ leads to a very good estimate of the field components and the calculated magnetic fields are remarkably similar to full-3D EM simulations, even when octagonal inductors are approximated as circular, as shown in 2.4. This allows for a rapid *a priori* quantitative estimate of an inductance-shift sensor sensitivity.

2.2 A Survey of Integrated Magnetic Biosensors

To date, three types of integrated inductance shift sensors were demonstrated: frequency shift sensors, transformer-based sensors, and bridge sensors. The first type detects the change in the frequency of a free-running oscillator, while the other two detect voltage offsets induced by magnetic perturbations above the sensor surface. As such, the first type is a time varying system while the other two are LTI for analysis purposes. It is noteworthy that the most of the systems surveyed here were designed intuitively, with a limited physical background to estimate their performance. Therefore some of their issues, which will be discussed, are not fundamental flaws but stem from uninformed design choices.

Frequency shift sensors

A frequency shift oscillator senses changes in the permeability of the environment by monitoring its self-oscillating frequency. These sensors are usually modeled as an LC tank in which L is the sense inductor and C is the effective parallel tank capacitance. In this model, the positive feedback mechanism of the oscillator is lumped into a negative resistance block as shown in Fig. 2.4 to obtain the oscillation frequency

$$f_0 = \frac{1}{\sqrt{L_0 C_0}}. \tag{2.20}$$

This architecture is advantageous due to its simplicity. Practical implementation of LC oscillators is well-studied and resolving the frequency shift requires nothing but a digital counter if the signal amplitude is large enough. The digital output of the system eliminates the need for additional interface circuitry to a processing unit. The relation between the shift in the oscillation frequency and environment permeability (modeled as additional inductance) is resolved to the first order from (2.20) and is conveniently independent of the oscillation amplitude

$$f = f_0 \left(1 - \frac{\Delta L}{2L}\right). \tag{2.21}$$

The two main drawbacks of these systems are their limited noise performance and relatively slow response time. Measuring the frequency shift with a digital counter requires by definition a gating clock to trigger the counter, effectively imposing a lower-bound on the system accuracy. Typical magnetic nano-particles are responsive in the low-GHz range and therefore sensing particle-related sub-ppm frequency shifts requires by definition gating times in the order of milliseconds. Worse still, since these are free running oscillators, the timing accuracy is limited by their phase noise [17], and hence averaging is only useful to a certain extent. Several variations were proposed to overcome these issues: Differential structures and correlated double counting schemes [15][18] employ dummy devices to cancel out local drifts in integrated sensors. While they show a significant improvement in sensitivity both theoretically and practically, they still require several seconds of averaging to achieve these performance. Long-term drifts due to temperature gradients and signal coupling far degrade the stated performance in measurements lasting more that 90 seconds. Recently a dual-mode oscillator sensor topology was proposed [7]. By using the same inductor core at two different frequencies, namely where the magnetic particles are responsive and where they are not, temperature drifts are cancelled to a significant extent for very long time periods. This sensor is however

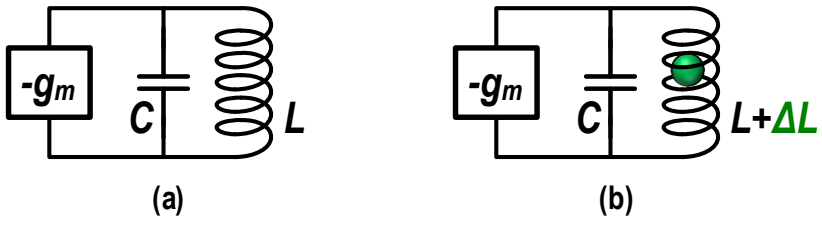


Figure 2.4: An oscillator circuit (a) with and (b) without a magnetic perturbation in the inductor core.

targeting by design a single type of magnetic nanoparticles and relies on accurate knowledge of their frequency response, which might vary between manufacturers or different batches [15]. Frequency shift sensors demonstrate the highest reported sensitivity do date, but their relatively slow response time makes them unsuitable for dynamic applications such as cell-cytometry.

Transformer based sensors

Transformer-based permeability sensors are linear transducers. They sense changes in the magnetic flux coupled from the primary ("excitation") coil of a transformer to its secondary ("pickup") coil. A simplified implementation is shown in Fig. 2.5. The excitation coil is wound around the core in a "figure-8" shape so in the absence of perturbation the total flux change in the secondary is zero. Magnetic particles placed around the excitation coil interfere with the flux coupling between the primary and secondary, and thus induce either a positive or a negative signal in the output amplifier.

This topology is fundamentally different than the frequency shift scheme. Its main advantage is that the transducer can be described as an LTI system and the front-end consists of driven amplifiers. At a low GHz range, these sensors work far above the $/1f$ noise corner and the transducer noise contribution is only the thermal noise of the equivalent series resistors of the transformer's inductors. The lack of self-oscillating noise components $1/f^n$ allows to integrate it for longer time periods and trade bandwidth with SNR. The drawback of this architecture is its complexity. The coupled signals can be small (in the orders of microvolts) and therefore require substantial amplification which itself adds noise and is subject to drift. The sensed RF signal needs to be down-converted and digitized for further processing. Practically, the added noise and interference are far greater than the fundamental sensitivity limit of the linear transducer. While this is a technology-dependent issue, it is the reason

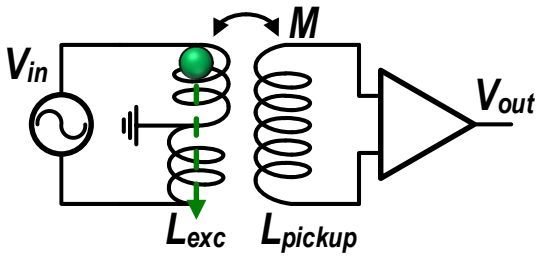


Figure 2.5: An example of a magnetic perturbation travelling in the vicinity of a transformer-based inductance-shift sensor.

why transformer-based sensors have so far demonstrated slightly lower sensitivity than their frequency counting counterparts.

Bridge sensors

Bridge sensors are another type of linear transducers. Unlike transformers, their excitation is not coupled to the output, but drives a balanced impedance at the input of a receiver amplifier. A perturbation of the balance generates a deviation from the amplifier quiescent point and thus can be detected. Bridge circuits are well-studied. They usually employ a differential architecture to null common-mode perturbation that might overshadow the sensed quantity. AC bridges are commonly used for precision measurements [19], and therefore are natural candidates for biomedical magnetic sensing systems. Moreover, capacitive and resistive bridges were demonstrated with complementary sensing elements [20][21] in which both bridge branches respond to a perturbation with inverse polarity to double the differential output voltage. Inductive bridges are more challenging, however, and the problem is exacerbated in integrated implementations. An all-inductor bridge requires four inductors, is large, and suffers from unwanted coupling effects. Reducing its size by changing one of its branches with capacitors is also problematic as it leads to an unmatched frequency response and to a narrow-band nulling. The next section will describe a novel bridge architecture which takes advantage of the mutual coupling of two coupled inductors to reduce its size while maintaining a matched frequency response. As a result, its differential-output voltage also increases compared to a standard structure.

2.3 Coupled Inductive Bridge Sensors

Transducer gain

The sensor in Fig. 2.6a is based on a differentially driven, differential AC bridge, but is composed of two pairs of coupled inductors. A perturbation of the effective permeability in core A, for example, (Fig. 2.6b) incurs shifts of ΔL_1, ΔL_2, and ΔM in its self- and mutual-inductances, $L_{A,1}$, $L_{A,2}$, and M_A, respectively. We require $L_{A,1} = L_{B,1} = L_{A,2} = L_{B,2} = L$ and $M_A = M_B = M$ to ensure a matched frequency response of the two branches. As a result, all of the inductors equivalent series resistances are also similar with $R_{A,1} = R_{B,1} = R_{A,2} = R_{B,2} = R$. It can be shown that under a sinusoidal drive signal with differential and common mode components

of magnitudes V_d and V_c, the voltage at each of the bridge outputs is

$$V_{out,p} \approx \frac{V_d}{2} \cdot \frac{s(\Delta L_2 + \Delta M)}{s(2L + 2M) + 2R} + V_c \cdot \frac{s(2L + 2M + \Delta L_2 + \Delta M) + 2R}{s(2L + 2M) + 2R}, \tag{2.22}$$

$$V_{out,n} \approx \frac{V_d}{2} \cdot \frac{-s(\Delta L_1 + \Delta M)}{s(2L + 2M) + 2R} + V_c \cdot \frac{s(2L + 2M + \Delta L_1 + \Delta M) + 2R}{s(2L + 2M) + 2R}. \tag{2.23}$$

It is important to note that unlike the approximation in [22], $\Delta L1$ and $\Delta L2$ are not assumed to be equal. The differential output voltage, $V_{out,diff} = V_{out,p} - V_{out,n}$, can be approximated as

$$V_{out,diff} \approx \frac{V_d}{2} \cdot \frac{s(\Delta L_1 + \Delta L_2 + 2\Delta M)}{s(2L + 2M) + 2R} + V_c \cdot \frac{s(\Delta L_2 - \Delta L_1)}{s(2L + 2M) + 2R}. \tag{2.24}$$

If the bridge is excited with a differential input and drives a matched load, the V_c-dependent part of the output can be neglected, because it is multiplied by perturbation terms only. The inductor series resistance can be expressed in terms of the quality

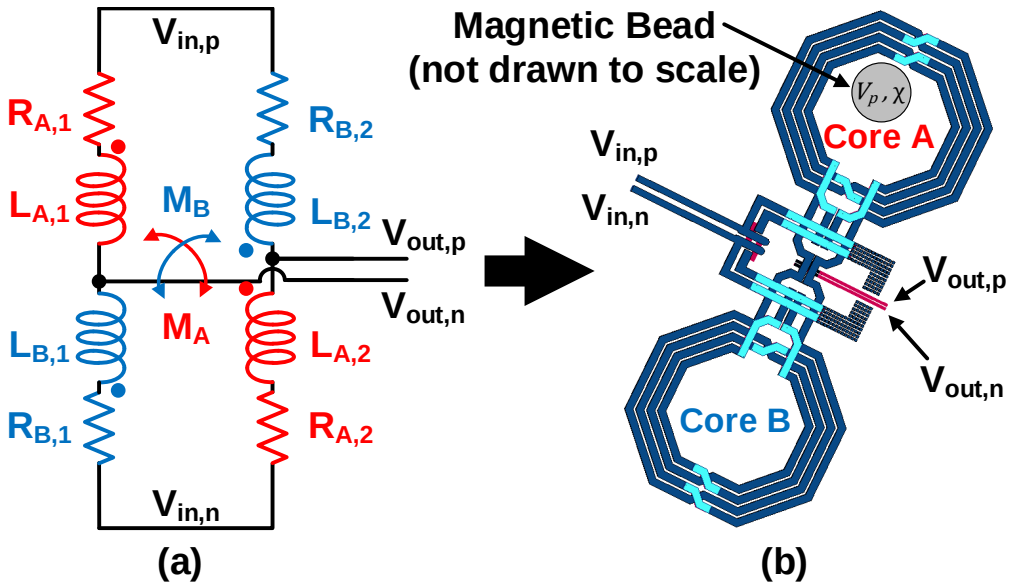


Figure 2.6: A coupled inductive bridge. (a) Circuit schematics. Inductors with the same color share a core. (b) Physical implementation with a magnetic perturbation near one of the cores (not drawn to scale).

factor $Q_{eq} = \omega(L + M)/R$ to give

$$V_{out,diff} \approx \frac{V_d}{4} \cdot \frac{\Delta L_1 + \Delta L_2 + 2\Delta M}{L + M} \cdot \frac{1}{1 - j/Q_{eq}}. \tag{2.25}$$

The result of (2.25) highlights three important characteristics of this topology. First, a perturbation of the coupled core produces a differential inductance shift equal to the shift that the same perturbation would have produced, had it been placed on the surface of a single inductor, composed of the *series-connected core inductors* $L_{ser} = 2(L + M)$. Hence, the amount of inductance shift as a function of bead-parameters can be predicted using (2.13). Second, the denominator is composed of only *half the series connected inductance*. This leads to effectively twice the gain of a standard bridge. It is noteworthy that a similar voltage output could be achieved by using a four-inductor bridge with inductances of $0.5L_{ser}$. However, such a structure will be about 1.5 times larger (excluding keep-out zones), would suffer from unwanted and unaccounted coupling effects, and would have a smaller effective sensing area compared to the coupled case. Third, since the sensed quantity is in quadrature with the series resistance, even moderately low values of Q_{eq} hardly affect the output. For example, in a core with a coupling factor $M/L = 0.8$ and $Q_L = \omega L/R = 6$, the differential output voltage degradation is less than 0.5%. Combining (2.14) and (2.25) gives the bridge *transducer gain*

$$G_t \triangleq \frac{V_d}{4} \cdot \frac{1}{L + M} \cdot \frac{1}{1 - j/Q_{eq}} \cdot \frac{2}{I^2} \chi V_p u_{B0} \cdot 10^6 \tag{2.26}$$

in units of [μV/bead] where u_{B0} is the unperturbed magnetic energy density of the series connected core inductors and χ and V_p are the susceptibility and volume of the bead, respectively.

Input and output impedances

Input and output impedances are important for the design of the bridge excitation and receiver circuits and are estimated by approximating the bridge outputs as open-circuits. The input impedance test circuit is shown in Fig. 2.7a. Due to symmetry, the test current I_t is equally divided between the bridge branches so each inductor induces a voltage with magnitude $sMI_t/2$ in its coupled counterpart. The result is equivalent to four inductors sized $(L+M)$, connected in series/parallel with an input impedance of

$$Z_{in} \approx s(L + M) + R. \tag{2.27}$$

The output impedance test-current in Fig. 2.7b is equally divided between the excited-branch inductors, resulting zero current at the other branch. The mutual inductance has no effect and the differential output impedance is

$$Z_{out} \approx sL + R + R_s \tag{2.28}$$

assuming an excitation source with an output impedance R_s. The result in (2.28) is a worst-case scenario, since if the bridge input is tuned, then a parallel capacitor is added to it. At the tuning frequency, usually $Z_{c,tune} < R_s$ and the output impedance becomes $Z_{out} \approx sL + R + Z_{c,tune}$.

Noise considerations

The coupled bridge is passive, so it only adds to the circuit the thermal noise associated with its inductor series-resistance. The other fundamental noise source is the excitation signal which propagates to the output and is not necessarily ideal. The noise associated with the source, $e_{n,S}$, in Fig. 2.8a can be treated as correlated differential and common-mode components with identical amplitudes. These propagate to the output identically to (2.24), so the output noise due to each excitation source,

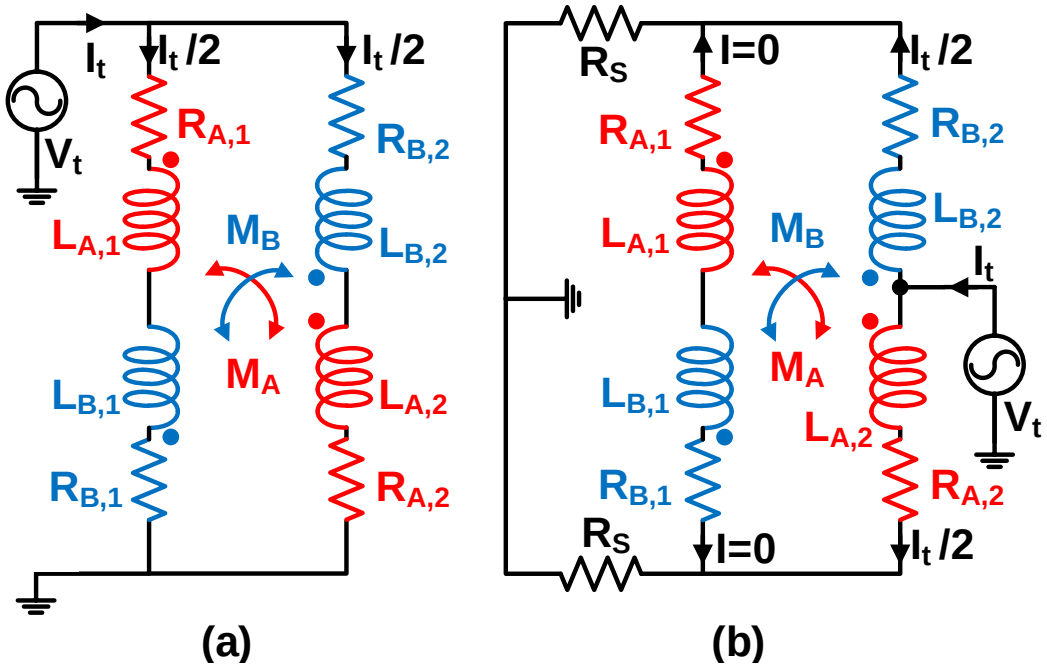


Figure 2.7: Schematic circuits of the sensor's (a) input impedance test circuit and (b) output impedance test circuit.

$e_{n,out}|_S$, is

$$< e_{n,out} > |_S \approx \frac{\sqrt{< e_{n,S} >^2}}{2} \left[\frac{\pm s(\Delta L_1 + \Delta L_2 + 2\Delta M)}{s(2L + 2M) + 2R} + \frac{s(\Delta L_2 - \Delta L_1)}{s(2L + 2M) + 2R} \right], \tag{2.29}$$

where $\pm$ is added to determine if we applied the source noise at the positive or negative input. The total noise at the output, due to two uncorrelated differential excitation sources, $e_{n,out}|_{S,tot}$, is then

$$< e_{n,out} >^2 |_{S,tot} \approx < e_{n,S} >^2 \left[\omega^2 \frac{(\Delta L_1 + \Delta M)^2 + (\Delta L_2 + \Delta M)^2}{|j\omega(2L + 2M) + 2R|^2} \right]. \tag{2.30}$$

This noise is attenuated similarly to the excitation signal, and therefore is not of a major importance.

The noise source associated with a single inductor series-resistance is shown in Fig. 2.8b. Since the unexcited bridge branch is grounded, its output voltage is 0V and the excited branch behaves like an impedance divider. Then, the output noise due to a single core inductor, $e_{n,out}|_L$, is

$$< e_{n,out} >^2 |_L \approx \frac{< e_{n,L} >^2}{4}. \tag{2.31}$$

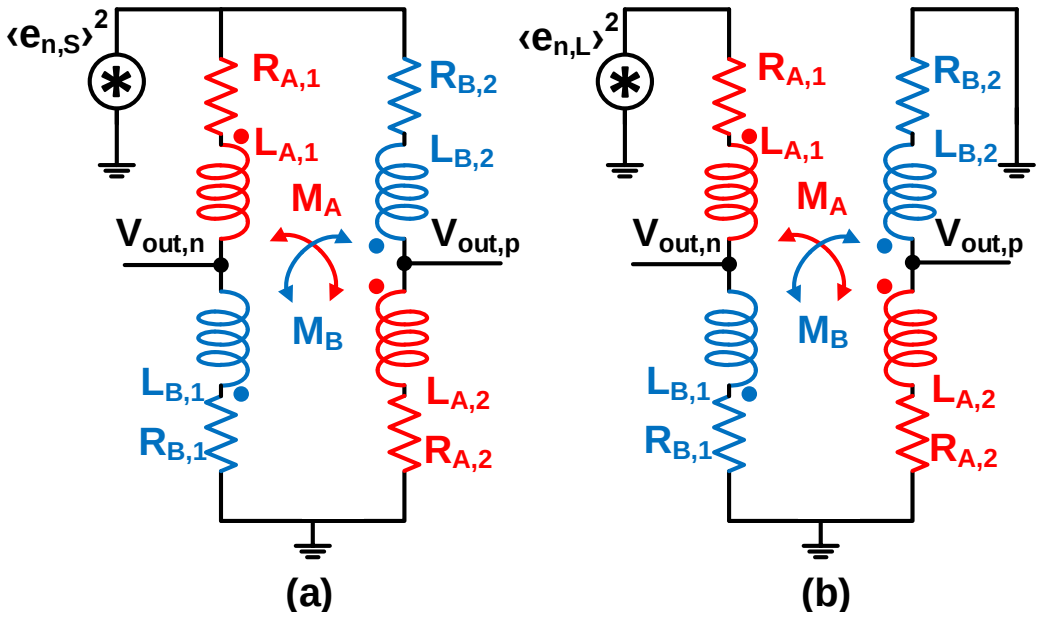


Figure 2.8: Schematic circuits of the sensor's (a) excitation noise and (b) single inductor equivalent thermal noise.

Assuming that the thermal noises of all the inductors are uncorrelated, the total output noise due to the bridge inductors, $e_{n,out}|_{L,tot}$, is

$$< e_{n,out} >^2 |_{L,tot} \approx < e_{n,L} >^2 . \tag{2.32}$$

Integrated RF inductors are usually implemented in a thick metal layer where their equivalent series resistance is ~0.5-10Ω [23]. This results in associated thermal noise densities up to $\sim 0.4 nV/\sqrt{Hz}$ [24]. Since the input-referred noise density of a typical bulk-CMOS amplifier is on the order of several $nV/\sqrt{Hz}$, the thermal noise of the sensor is in most cases insignificant compared to the receiver's input-referred noise.

Parasitic effects

In reality, the useful frequency of operation of an inductor is limited by its parasitic capacitance. Here, we lump the parasitic components into a few discrete devices as shown in Fig. 2.9.

C_p and C_m are the equivalent ground- and mutual-capacitances, respectively. Each inductor's parasitic shunt capacitance is usually much smaller than those quantities and therefore neglected. For inductors with turns number $N > 1$, C_m pins are more naturally modeled between one inductor dot and the other non-dot ports, as shown in Fig. 2.9b. While more complex models could be used to describe the high frequency behavior, ours leads to an insightful result when embedded in the sensor cell with acceptable errors when compared to simulations as shown in 2.4. The complete model in Fig. 2.10a reduces to Fig. 2.10b, highlighting two independent resonance

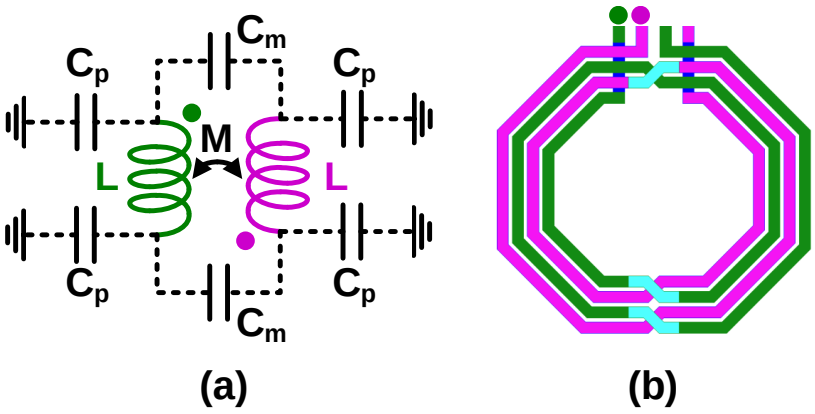


Figure 2.9: A high frequency (a) coupled inductor model and (b) exemplary 2-turn layout.

frequencies: the input impedance is now frequency-dependent with resonance at

$$f_{Z,in} \approx \frac{1}{2\pi\sqrt{(L+M)(C_p+2C_m)}}. \tag{2.33}$$

Interestingly, the frequency-dependent excitation-to-output transfer function exhibits the same resonance frequency of

$$f_{out} \approx \frac{1}{2\pi\sqrt{\frac{(L+M)}{2}(2C_p+4C_m)}} = f_{Z,in}. \tag{2.34}$$

In reality, $f_{Z,in}$ and f_{out} slightly differ due to the distributed nature of the parasitic elements, but the approximation is very reasonable for design purposes. In this work, we define the self-resonance frequency as

$$SRF \triangleq f_{out}, \tag{2.35}$$

and require $f_{nominal} \ll SRF$ so as to maintain the accuracy of our low-frequency model. Nevertheless, additional analysis could be performed to investigate the potential in tuning the sensor output to boost its voltage gain.

2.4 A Coupled Inductive Bridge - Proof-of-Concept Design

Based on the analysis in 2.3, the five main parameters affecting a coupled bridge design are the *maximum* and *flatness* of the location-dependent transducer gain, the

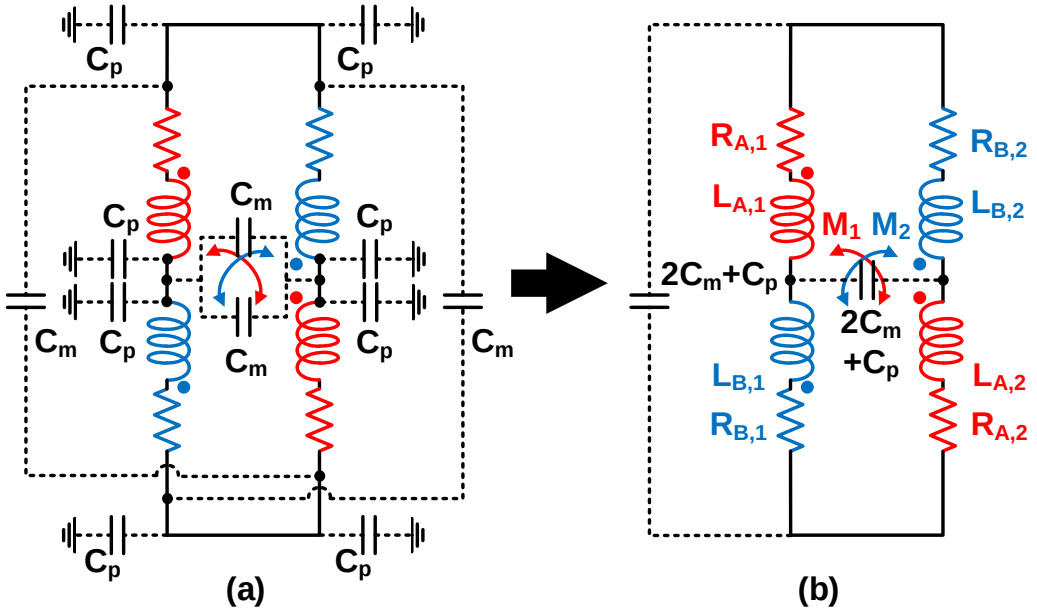


Figure 2.10: A high frequency (a) coupled bridge model and (b) equivalent circuit.

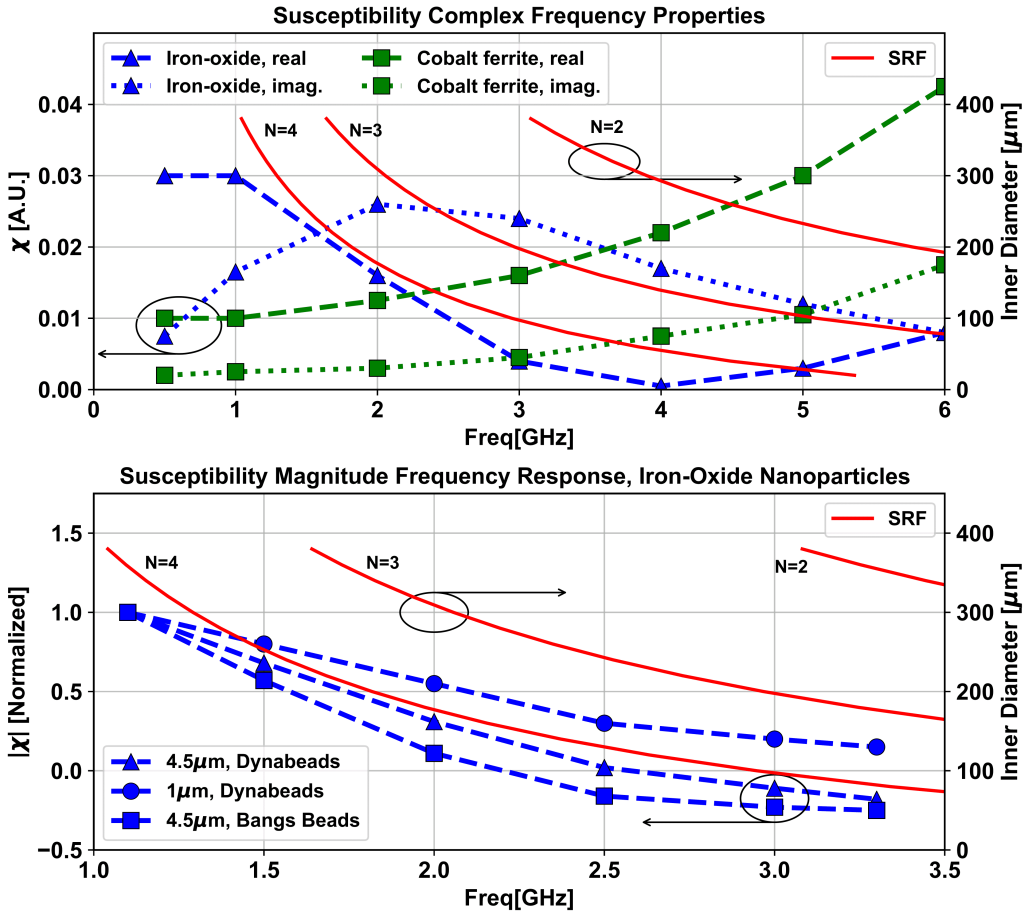


Figure 2.11: Top: complex frequency response of two types of magnetic bead [9]. Bottom: change in magnitude of χ vs. frequency [15] for three bead types.

self and *mutual* inductances which affect the excitation and receiver design, and the *SRF* which limits the frequency of operation. These must be tailored to fit the physical parameters of the sensed material.

Choosing the frequency of operation

Magnetic beads have been demonstrated to show rich frequency behavior [25], which can be exploited for various sensing schemes. This requires the use of a sensor with a suitable SRF. Fig. 2.11 overlays two previously measured datasets of the spectral properties of different beads [9][15] on top of the expected SRF of our coupled sensor, for a different number of turns, N, and different diameters of the core inductors. The desired frequency of operation dictates the sensor size; for example, in order to measure the real part (or magnitude) of χ of iron-oxide nanoparticles up to 1GHz, we require $SRF > 5$GHz. Hence, cores with 2-, 3-, or

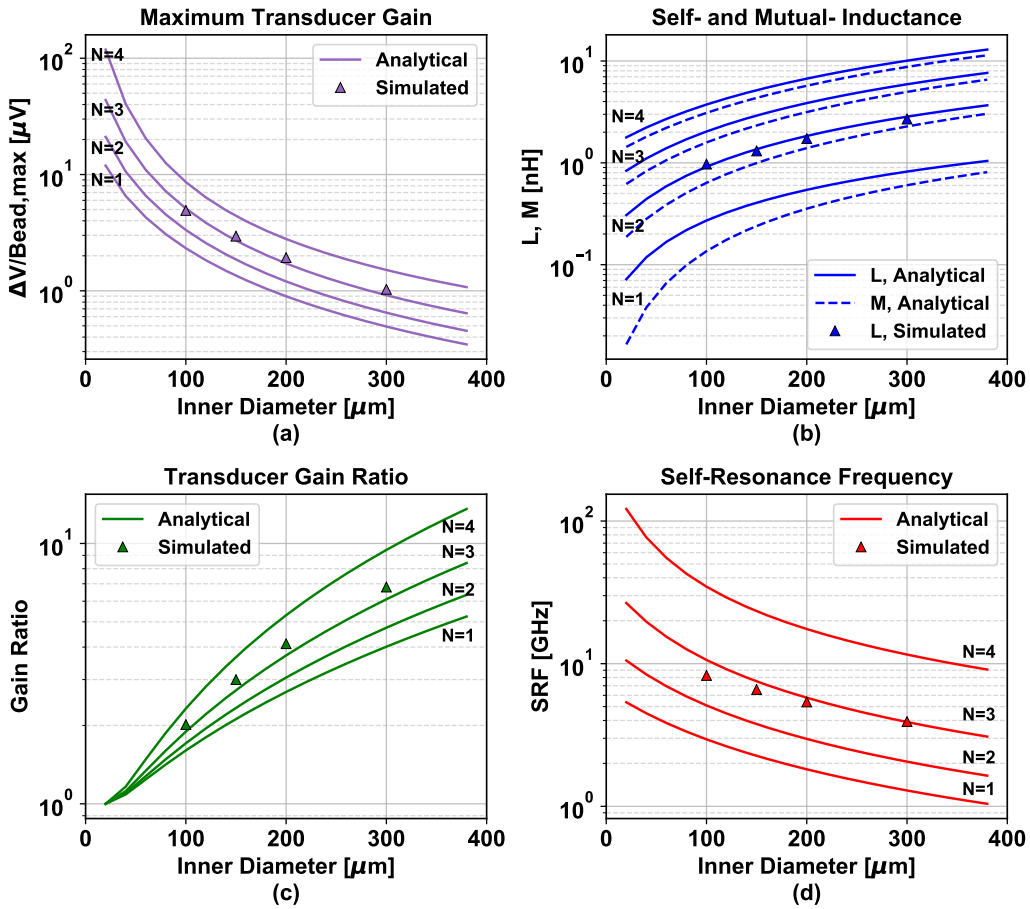


Figure 2.12: Coupled bridge design parameters as a function of the inner core diameter and the number of the single-inductor turns. (a) maximum transducer gain, (b) self and mutual inductance, (c) gain ratio, (d) SRF.

4-turn inductors can be used with inner diameters smaller than 234μm, 103μm, or 30μm, respectively.

Fig. 2.12 shows how sensor performance metrics vary with the inner core diameter and N when used to detect 4.5μm Dynabead-Epoxy® beads. The bead susceptibility is assumed to be χ=0.17 [26], but it is noteworthy that values up to 0.25 have also been reported [27][28]. These beads will be used throughout the paper as a baseline to verify our sensor performance. The transducer gain is calculated from (2.26) with u_{B_0} either simulated or calculated from B_0, which can be approximated by (2.19). The maximum (Fig. 2.12a) and minimum transducer gains are defined on the sensor surface as shown in Appendix-2.4. Their quotient is the gain ratio in Fig. 2.12c which is a measure for the sensor's *gain flatness*. The core inductances (Fig. 2.12b) and SRF (Fig. 2.12d) are calculated using equations (2.36)-(2.39).

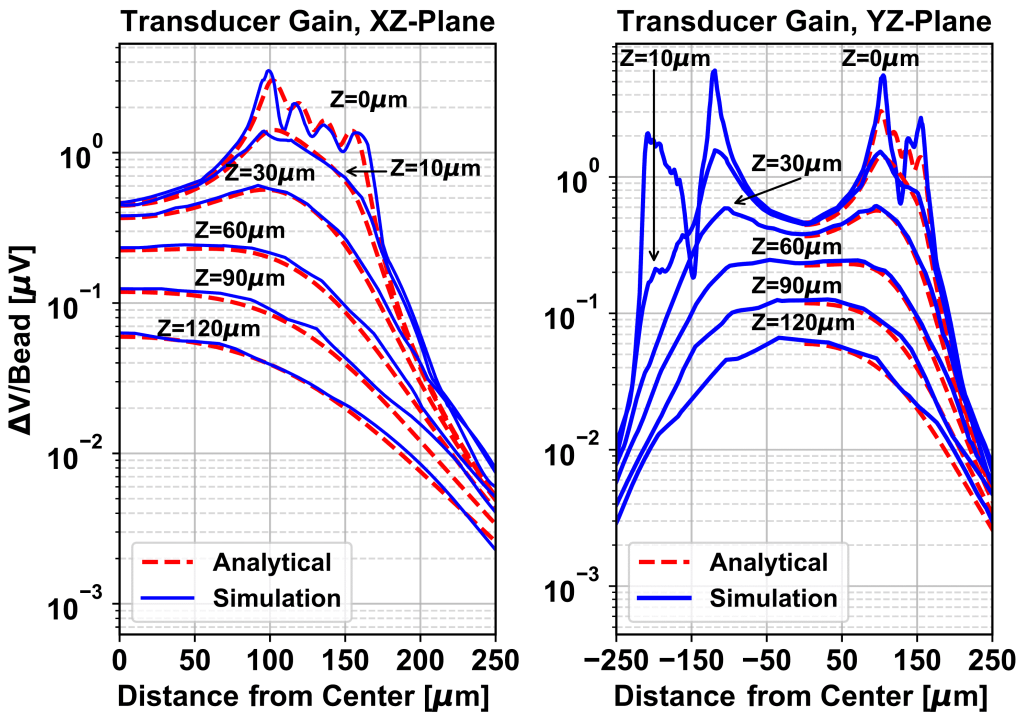


Figure 2.13: Comparison between the calculated and simulated transducer gain as a function of location above the sensor, (left) on xz-plane, (right) on yz-plane.

Transducer gain and flatness.

Fig. 2.14 shows the locations where the maximum and minimum transducer gains are defined. The location with the highest sensor gain is predicted to be near its traces. However, placing a bead there will affect the trace current and will violate the assumption in (2.3). Hence, we measure the maximum transducer gain at about twice the bead diameter inward from the traces–approximately 10μm. The minimum transducer gain is defined on the sensor surface in the center of the core. Therefore, the ratio of the largest gain to the smallest gain is a measure for the gain flatness *at a given height*. The bead's center is assumed to be 5.7μm above the surface to account for its diameter of 4.5μm, for the IC metal traces (3.4μm thick), and for the chip oxide passivation (1.8μm thick).

Inductor model equations.

The circuit parameters of Fig. 2.9a are determined as follows: each inductor inductance, L, is calculated using the modified wheeler equation [29] which for

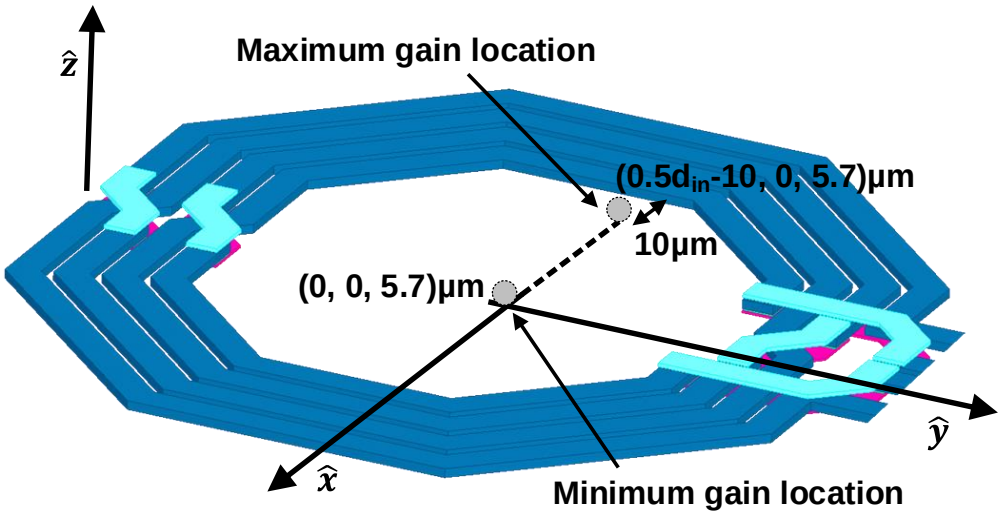


Figure 2.14: Bead location for the calculation of maximum and minimum gain parameters.

octagonal inductors gives

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}, \tag{2.36}$$

where $K_1 = 2.25$, $K_2 = 3.55$ are shape constants for octagonal spiral, $d_{avg} = 0.5(d_{out} - d_{in})$ is the average diameter, and $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$ is the fill factor. d_{out}, d_{in} are the spiral inner- and outer-most diameters, respectively.

The ground capacitance, C_p, is calculated by considering the plate and fringe ground-capacitances of each inductor trace as in [30]:

$$C_p = \frac{l_{tot}\epsilon}{2}\left[\frac{w - t/2}{h} + \frac{2\pi}{\log\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)}\right]. \tag{2.37}$$

Here l_{tot} is the total trace length, ϵ is the dielectric constant, and w, t, and h, are the trace width, thickness, and height above substrate, respectively.

The mutual capacitance, C_m, is calculated from the total length of parallel coupled inductor traces, similarly to [31],

$$C_m = \frac{g_{tot}\epsilon}{2}\left(0.03\frac{w}{h} + 0.83\frac{t}{h} - 0.07\left(\frac{t}{h}\right)^{0.222}\right)\left(\frac{s_t}{h}\right)^{-1.34}, \tag{2.38}$$

with the addition of s_t, the trace spacing, and g_{tot}, the total length of the traces gap.

Finally, the mutual inductance, M, is found from simply using (2.36) to find the inductance of the series-connected coupled inductors, and solving for M in $L_{ser} =$

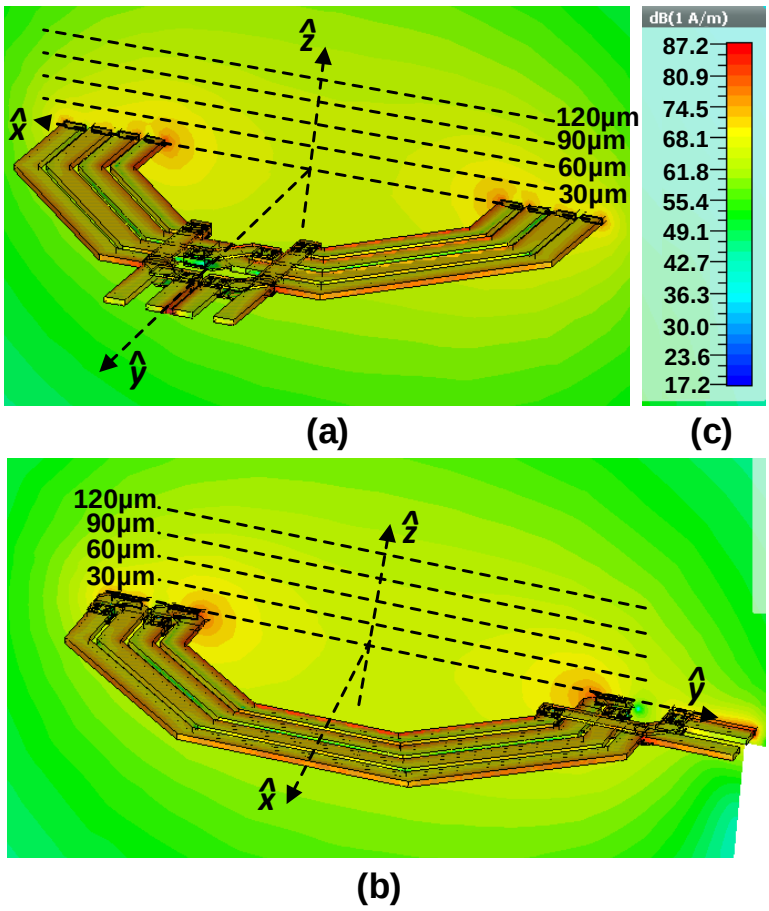


Figure 2.15: Simulated magnetic field intensity with core inductors shorted in series. (a) On xz-plane, (b) on yz-plane, with (c) recorded values in $dB(A \cdot m^{-1})$ (to increase contrast).

$2(L+M)$:

$$M = \frac{L_{ser}}{2} - L. \tag{2.39}$$

The series resistance does not play a major role in this sensor design, but can be calculated from [23] if needed.

Magnetic field profile

One implication of (2.25) and (2.26) is that the sensor gain is proportional to the energy density profile of the series-connected core inductors. Fig. 2.13 draws comparison between the transducer gain that was calculated from the magnetic field predicted in (2.19) and the gain that was derived from the simulated fields of a similarly-sized sensor core. One comparison was done using the field values on the xz-plane (Fig. 2.15a) at several heights above the sensor surface. A second

comparison was done on the yz-plane (Fig. 2.15b) to illustrate the difference in results due to the core leads and trace cross-overs, which are not included in the analytical model.

Core sizing

For a prototype design, we chose a 2-turn, 200μm inner-diameter sensor core. It has SRF ≈6GHz with maximum gain and gain-ratio of 2μV/bead and 4, respectively. The self- and mutual-inductances are L ≈1.7nH and M ≈1.3nH. This choice of parameters allows to easily sense a single 4.5μm bead at the sensor surface as well as to conveniently tune its input at the low-GHz range. To finalize the design, the chosen core was simulated with a commercial 3D-EM software [32]. A comparison between the gain-profile from calculated and simulated magnetic energy density is shown in Fig. 2.13, demonstrating the accuracy of the model presented in 2.1. The only differences are on the yz-plane near the leads and trace cross-overs which are not considered in the analytical calculation as discussed in Appendix 2.4.

Excitation and receiver

A sensor cell based on the core dimensions chosen in 2.4 was integrated with excitation and receiver circuitry in a 65nm bulk CMOS process (Fig. 2.16). The input driver stage is designed to have sufficient gain such that the excitation voltage is amplitude-limited at 1.6V differential peak-to-peak using a 1V supply. In addition, it includes a six-capacitor bank for frequency tuning. The receiver includes a summing amplifier for the offset-cancellation (OC) scheme detailed in 2.4. Both receiver and OC paths were designed with CMRR>60dB to decrease common mode offsets. Their simulated gains are 24dB and 19dB, respectively, to buffer and sufficiently amplify the bridge output. The receiver's simulated input-referred noise is lower than 10nV/$\sqrt{Hz}$, theoretically allowing a measurement of 500nV at the sensor output with an SNR=10dB at a 250Hz bandwidth or, equivalently, with a detection time of ∼3ms[33]–fast enough for cell-sorting applications [9]. Additional peripheral circuitry include an RF-to-DC amplitude detector for driver swing estimation and four thermometers for temperature gradient monitoring.

Offset cancellation

Our bridge sensor features matching characteristics which cancel most of its output offsets. Despite that, small residual offsets might result from branch mismatch, signal feedthrough, and temperature gradients. These can be canceled by subtracting

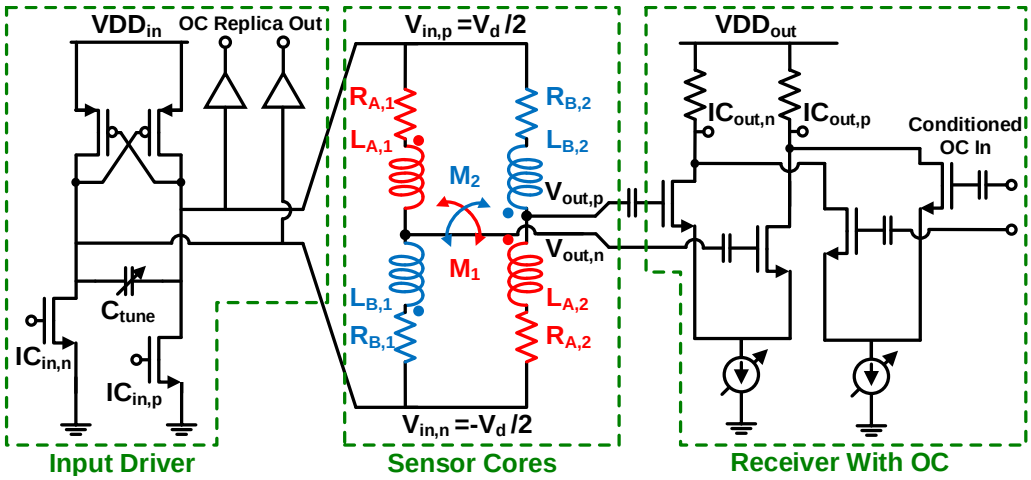


Figure 2.16: Simplified schematics of the fabricated IC.

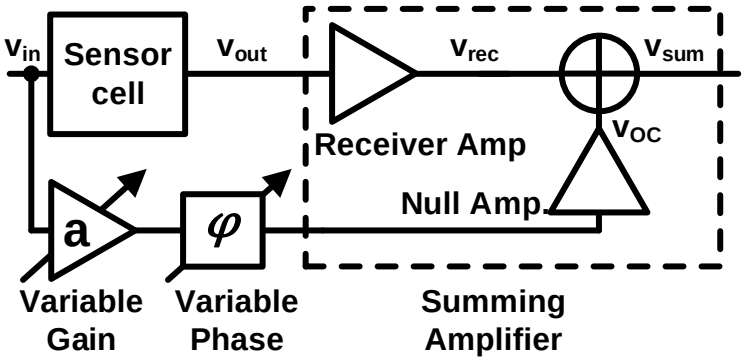


Figure 2.17: General structure of offset cancellation scheme.

a phase-shifted and attenuated replica of the excitation voltage from the received signal. Offset Cancellation (OC) can be done at the frequency of operation (RF) or in a down-converted signal. While high-resolution OC at RF is more difficult to implement, it relaxes the demands on the receiver input dynamic range. Fig. 2.17 shows a general OC scheme for the fundamental tone of harmonic signal with an amplitude A and a radial frequency ω

$$v_{rec} = A \cdot \cos \omega t. \tag{2.40}$$

The subtraction of a phase shifted and attenuated replica of the excitation signal

$$v_{OC} = Aa \cdot \cos (\omega t + \varphi) \tag{2.41}$$

from v_{rec} results in an output, v_{sum}, with a frequency ω and an amplitude of

$$A_{sum} = A\sqrt{a^2 - 2a\cos\varphi + 1}, \tag{2.42}$$

which should be nulled in order to cancel offsets prior to taking actual measurements. Clearly, the relative phase shift, φ, required to perfectly null the output is, to the first order, independent of the amplitude scaling factor a. Hence, an iterative binary search algorithm can be utilized to calibrate the sensor with a logarithmic complexity. If a and φ in (2.42) are both set digitally by N- and M-bit DACs, respectively, then the worst-case attainable OC is

$$\frac{A_{sum}}{A} = \sqrt{\left(1 - \frac{1}{2^N}\right)^2 - 2\left(1 - \frac{1}{2^N}\right)\cos\frac{\pi}{2^M} + 1}. \tag{2.43}$$

One subtlety in (2.43) is that the amplitude DAC is assumed to only cover the range up to the (unknown) output offset. If the replica OC signal is much larger than the offset in the received signal, additional bits are required for initial adjustments– approximately 3.5 bits for every 20dB of initial output uncertainty. Fig. 2.18 shows the achievable OC as a function of the number of phase and amplitude control bits.

Our sensor IC is designed for evaluation purposes and does not include down-conversion circuitry. Therefore, OC currently is done only at RF. For the same reason, offset signal conditioning is implemented off-chip with 12- and 16-bit phase and amplitude controls, respectively.

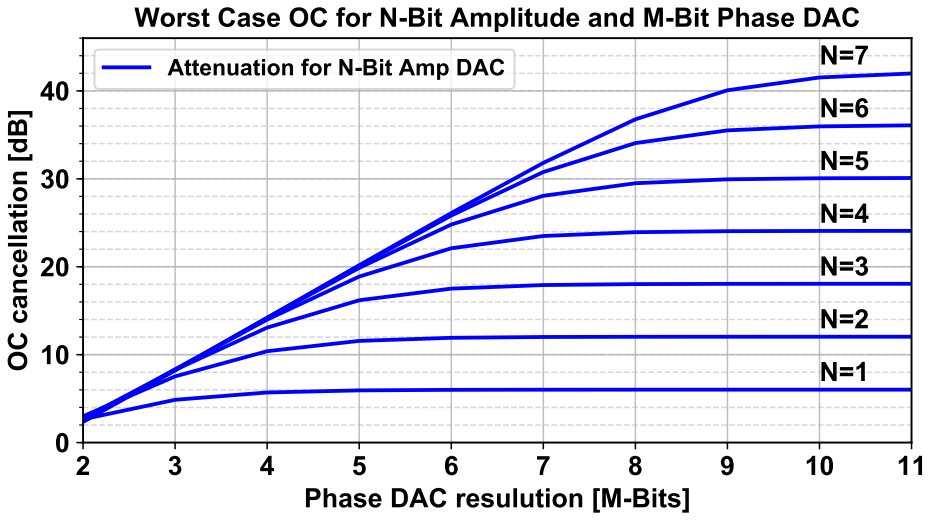


Figure 2.18: Attainable offset cancellation as a function of amplitude and phase control number of DAC bits.

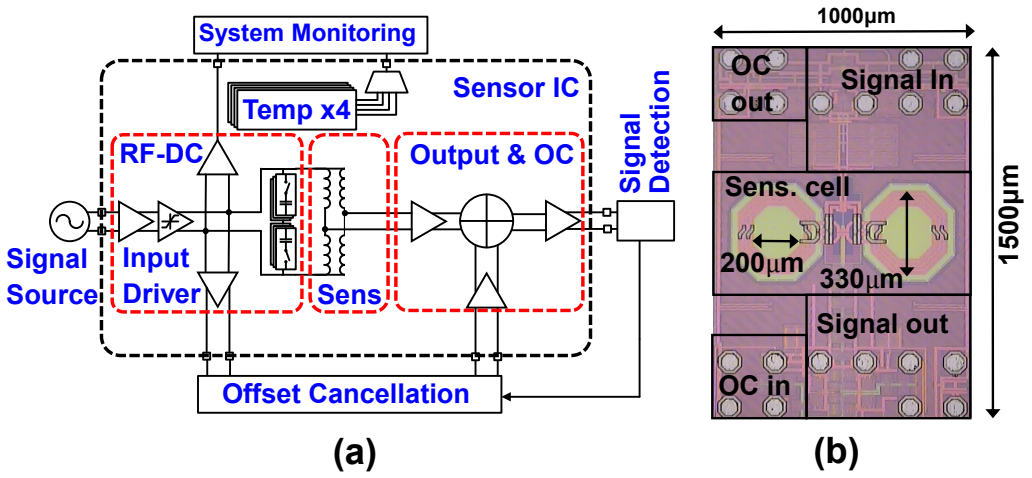


Figure 2.19: Top level view: (a) simplified measurement system schematics and (b) the chip die photo.

Sensor system characterization

The IC die photo and system schematics are shown in Fig. 2.19. No additional processing is done besides a back-lapping of the chip to a standard thickness of 300μm. For evaluation purposes, the output amplitude is recorded with a spectrum analyzer. Prior to detecting magnetic beads, additional performance characterization was carried out.

Input swing and receiver gain estimation

The sensor transducer gain (in μV/bead) is proportional to the bridge excitation swing (2.26), which is not directly accessible. To estimate it, we have integrated an RF-to-DC detector at the bridge input. The detector output was measured with variable input power (Fig. 2.20a) and at different tuning frequencies (Fig. 2.20b). Its close match with the simulation results leads to an estimated differential input swing of 1.6V peak-to-peak. In addition, it is necessary to know the bridge output voltage. However, its output is buffered by the receiver signal path, which is not directly measurable. Here, we use the OC path as a surrogate for the receiver path gain estimate. For that purpose, both paths are designed as cascades of identical amplifiers–six for the receiver and four for the OC. The OC path gain was measured (Fig. 2.21) and compared against simulation. The good agreement between the two results leads to an estimate of a 5dB difference between the receiver and OC path gains. The input driver and receiver consume 8.7mW and 11mW (including the OC amplifiers) at 100% duty cycle, respectively.

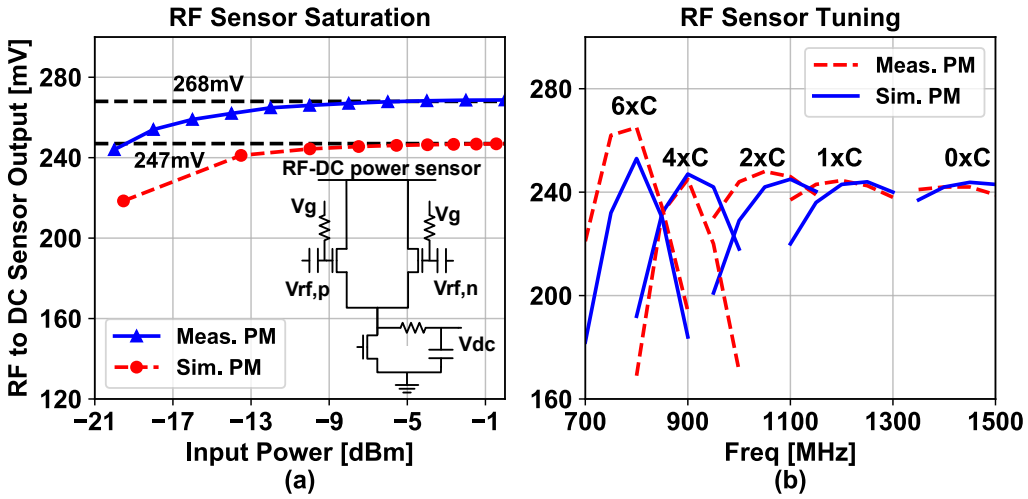


Figure 2.20: Measurement vs. simulation of (a) input power saturation, and of (b) input matching.

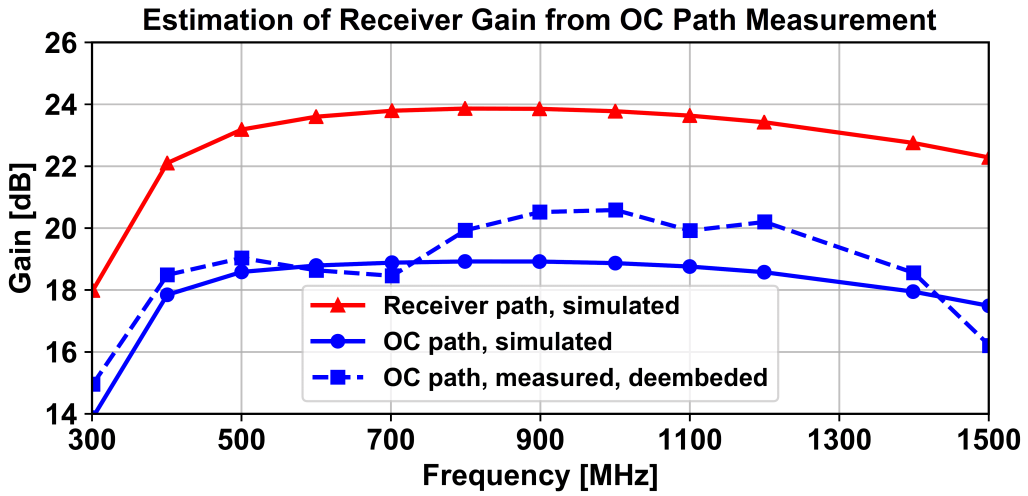


Figure 2.21: Comparison between the simulated and measured OC path gain to the simulated receiver gain.

Spatial transducer gain profile

Next, the spatial transducer gain profile of the inductively-coupled sensor was characterized (Fig. 2.22). This was done with a solid 15μm-diameter iron oxide bead which is small enough to obtain localization information, but generates a large enough signal such that offset errors are negligible. Gain reduction vs. height was measured at several sites above the sensor surface and compared to simulations (Fig. 2.23). The measured attenuation rate is about 0.23dB/μm and agrees well with the simulated results of 0.27dB/μm, especially given the uncertainty in height measurement and location on the sensor surface. These results are important for cytometry applications, where a microfluidic channel can be tens of micrometers high [9] with implications on the choice of the sensor inductor size; smaller inductances may be required in order to increase the sensitivity, as shown in (2.26). The gain is lower at the sensor leads (Fig. 2.23-right) and at its center, where the magnetic field intensity is lower. This is a common feature of all inductor-based sensors. If necessary, the optimization proposed in (2.12) or the method discussed in [34] can be adopted to achieve a horizontally uniform gain profile.

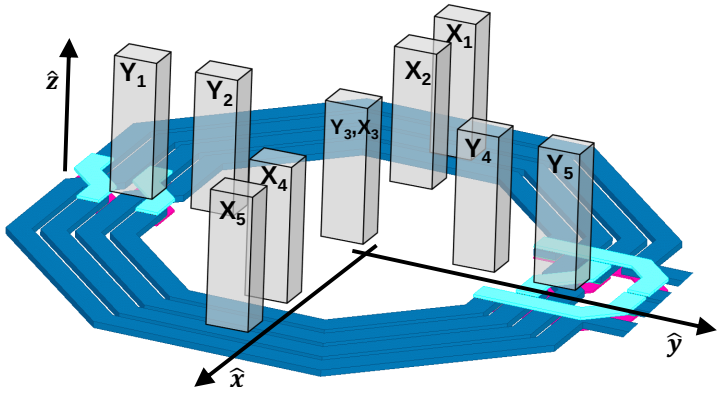


Figure 2.22: Probe locations for gain profile characterization.

Magnetic particle detection

Finally, the sensor performance was quantified by measuring several groups of 4.5μm Dynabead-Epoxy® magnetic beads bonded to non-magnetic probes. Measurements are taken in dry media as shown in Fig. 2.24. Each measurement includes an OC calibration followed by 30 minutes of application/removal of the probe using a micro-positioner. OC reduces the measured offset from 0.4mV to less than 3μV at the output of the sensor cell within less than 20 steps. Even though small temperature fluctuations, on the order of single degrees, were observed during the

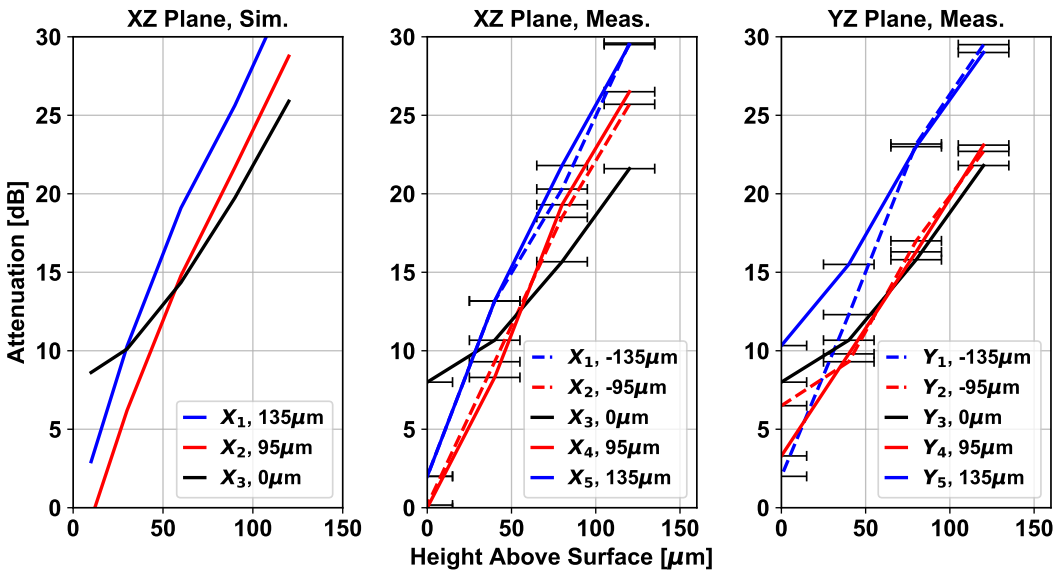


Figure 2.23: Gain profile degradation vs. height on yz-plane (right) and xz-plane (middle) compared to simulation prediction (left).

measurements, no in-depth investigation of the temperature-dependent behavior was carried at this time. All measurements were done at 770MHz to minimize spectral interferences from cellular bands and other laboratory equipment. The output signal is currently recorded using an additional off-chip receiver in order to verify the sensor cell performance, with the intention to integrate an on-chip baseband in the future. Fig. 2.25 shows a typical response of our coupled bridge sensor to several discrete quantities of magnetic beads. These are raw measurements that were averaged using a 16-point sliding-window for presentation purposes. The mean (dotted lines) and $\pm 1\sigma$ standard deviation (grey) are overlaid on the output readings, demonstrating a clear distinction between "high" and "low" output values over the whole measurement interval. These results show a stable, continuous detection over significantly longer time periods compared to previously reported similar works. The measurements of Fig. 2.25 were repeated several times at several locations on the sensor surface and demonstrated similar, continuously stable responses over periods at least half an hour long. The average sensor output voltage as a function of the number of applied beads is summarized in Fig. 2.26.

Qualitatively, these results match the measured gain profile of Fig. 2.23. Quantitatively, the measured transducer gain is up to 1.15μV/bead at the sensor edge and 0.38μV/bead in its center, compared to the predicted values of 2.1μV/bead

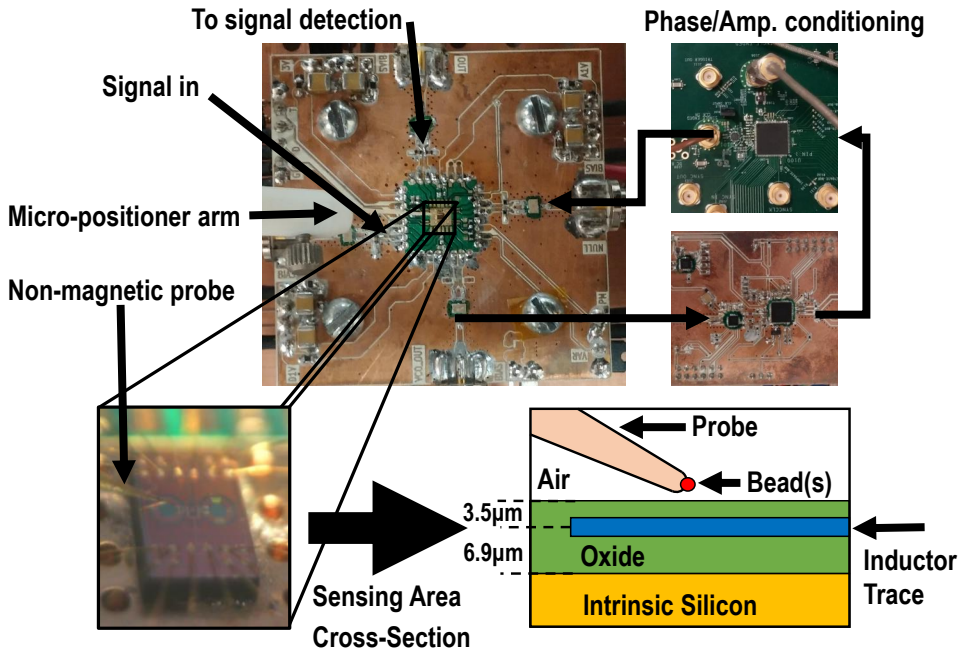


Figure 2.24: Measurement system, including OC circuitry.

and 0.46μV/bead, respectively. The lower measured gain can be attributed to three factors. First, beads near a sensor trace might affect the current distribution in it, violating the assumption in (2.3). Second, the transducer gain was already shown to decrease by about 0.25dB/μm with height (Fig. 2.23) above it, so if the beads are not flush at the chip surface, significant loss is expected. Finally, measurements are done at RF, where $|\chi|$ may be lower than its DC values (Fig. 2.11). Considering these facts, the measurements agree well with our predictions. The good agreement both verifies that the coupled bridge works as intended and supports the theoretical background that was developed in 2.1.

2.5 Conclusions

This work presents a systematic approach to the design of magnetic susceptibility sensors. A novel, all-inductor, fully symmetrical bridge sensor is demonstrated as a proof-of-concept of the design approach. By fabricating the bridge sensor along with integrated excitation and receiver circuitry, as well as carefully characterizing its performance and employing an efficient offset cancellation scheme, we show how our physical model and sensory system can be designed to the desired specifications. Though only a prototype, the coupled bridge was demonstrated to reliably detect 4.5μm magnetic beads with significantly improved long-term stability in comparison to state-of-the-art, as shown in Table 2.1.

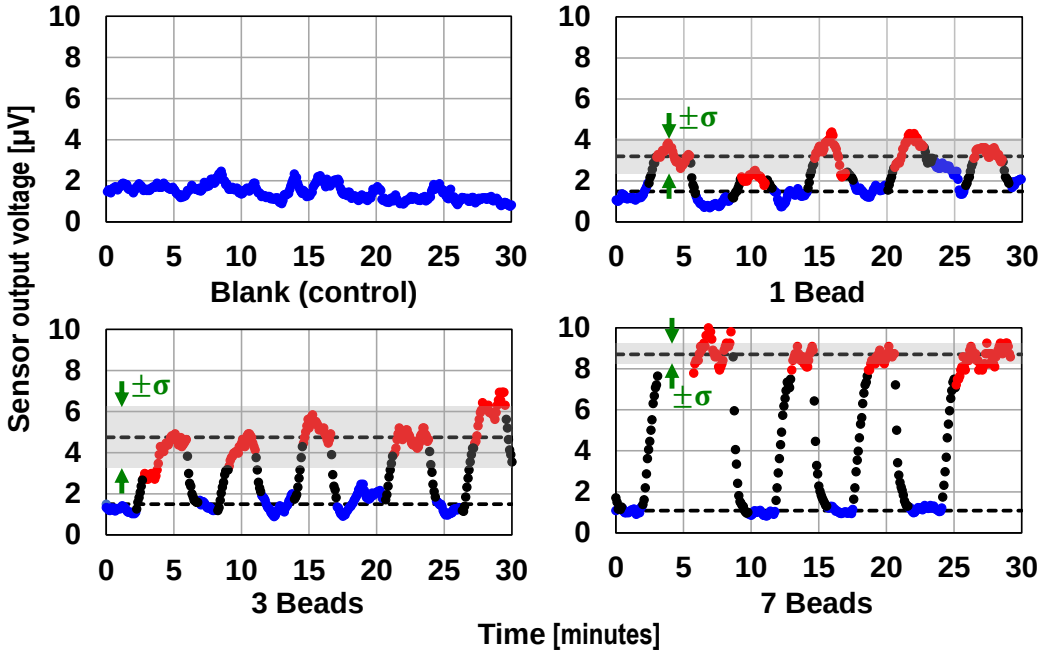


Figure 2.25: Exemplary system response to different amounts of 4.5μm iron-oxide beads.

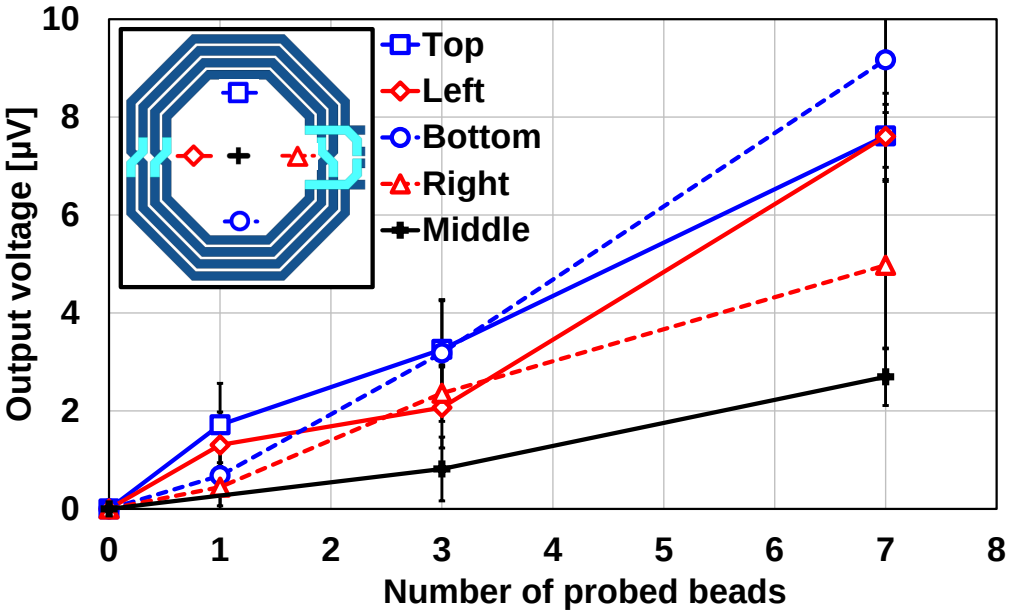


Figure 2.26: Sensor cell response for 4.5μm beads at various locations on the core surface.

Table 2.1: Comparison table

	ISSCC 09'[5]	ISSCC 14'[8]	JSSC 17'[9]	**This work**
Sensor Type	LC tank	Transformer	Transformer	**Bridge**
Target App.	Immunoassay	Cytometry	Cytometry	**Immunoassay/ Cytometry**
Min. Bead Size (iron-oxide)	1μm	4.5μm	4.5μm	**4.5μm**
Long Term Stability	90 seconds	3 seconds	20 seconds	**30 minutes**
Additional Inductors	No	Dummy	Tank	**No**
Effective Sensing Area	N/A	15x15μm	30x30μm	**200x200μm**

Chapter 3

CALTECH'S SPACE SOLAR POWER PROJECT [1]

3.1 Introduction

The idea to collect solar power in space and send it down to earth is over half a century old. It was presented in both fiction [35] and technical [36] literature, and is appealing because it overcomes major issues of terrestrial photovoltaic conversion. Space-based solar power is not affected by weather, avoids atmospheric attenuation and reflection, and is potentially continuously available throughout the day. Physically delivering the collected power with cables or elevators is not currently feasible due to the associated distance and assembly weight. Hence, the vast majority of published work aims to convert the solar power and send it down to earth in the form of an electromagnetic beam. Though this method is presumably inefficient due to the energy conversion and focusing losses, its practical advantages in terms of cost, mass, and manufacturability seem to overcome the drawbacks. Additionally, an EM beam may be electrically steered to provide dynamic power delivery and splitting, which makes the concept very appealing for commercial, emergency, and defense uses. Such a radiating array launched into space can presumably include EM receivers to perform remote sensing and measurement missions to further increase its functionality and therefore its economic and scientific value. Surprisingly, the main challenge is not solar-to-EM power conversion efficiency *per se*. A quick look at Glaser's original proposal in Fig. 3.1 for a power-converting satellite highlights the main difficulties with this design. The solar power density is given at about 1.36kW/m^2 in space and the radiated beam width of an antenna is inversely proportional to both its aperture size and frequency of operation. Therefore, transmitting and focusing a reasonable amount of power from a single power satellite require a large solar panel and a sizable aperture antenna on the same structure. Operating at high frequencies can only ease the problem to a limit, above which the loss associated with the conductors and active components is unacceptable. It will be quantitatively shown that with the current cost of launching mass into space, previously proposed solar power architecture make little economic sense in terms of the expected income versus the cost of space segment fabrication/ deployment.

[1] This work was done in collaboration with Dr. F. Bohn, Dr. B. Abiri, Dr. M.R. Hashemi, and A. Fikes.

The system's design challenges are therefore to maximize the specific power in W/kg radiated by the array, to improve its longevity, and to expand its functional capabilities.

Caltech has identified solar space power research as an important frontier in science and sustainability. A collaboration of researchers in the field of electronics, photovoltaics, and lightweight space structures has been working since 2015 on the development of novel architectures, structures, and circuits to enable feasible space-based power transfer. The main approach is to take advantage of technology advances and custom designed integrated circuits to significantly reduce space-based radiator weight and therefore launch cost, as will be shown in the following chapters. During my time at Caltech, I had the privilege to be part of the RF electronics team in this collaboration. Our main achievement to date is a first demonstration of a lightweight, modular, and fully integrated solar-to-RF power conversion unit (tile) with an exceptional power-to-mass ratio meant to be the basic building block of a future space power delivery system. The next sections will describe the space-solar power system with an emphasis on the electrical functionality. I will further detail my contributions to the project from the aspects of timing synchronization, system level integration, and thermal reliability.

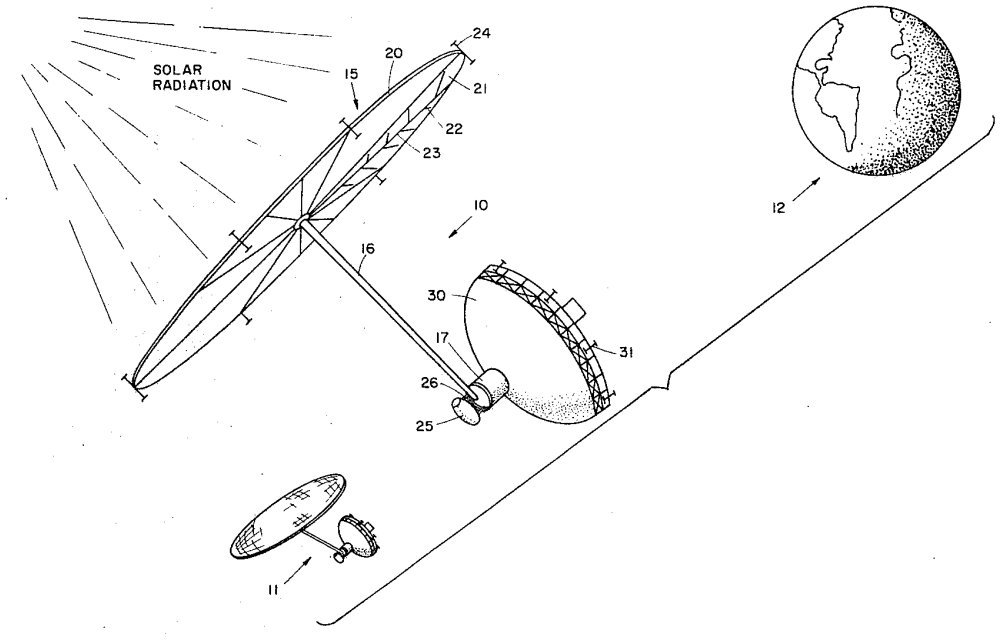


Figure 3.1: Glaser's original patent drawing of a solar power satellite.

3.2 System Overview

Cost Perspective

The main challenge with space-based power delivery is to design an economically viable system. Even though some benefits of space-based power like dynamic beam steering are hard to quantify and monetize, an approximate estimate of space power economics is crucial to evaluate the system viability. This chapter will derive a rough estimate of space-based power levelized cost of electricity (LCOE), compare it to current energy costs, and draw system-level conclusions. Some of the assumptions are technology-dependent or estimated magnitudes and are not fundamental limits to system performance. Nevertheless, this exercise is important to understand the design-space and the variables that determine this concept's feasibility.

The discussion starts with the estimated energy costs in selected countries and in US expeditionary operations, shown in table 3.1 and in Fig. 3.2. While the prices slightly change between different surveyors [37][38], these approximate values are sufficient for the discussion that will follow.

Table 3.1: Average worldwide prices for electrical power*

Country	US Cents/kW·h	Year Updated
Egypt	4	2019
China	8	2019
South Africa	11	2019
United States**	7.7 - 19.36 [Hawaii - 29.18]	2018
Australia	22	2019
Japan	28	2019
Germany	35	2019

∗ Data from [37]
∗∗ Data from [39]

Clearly, the cost of energy in remote operations is orders of magnitude higher than in well established populated areas. For this reason, the solar space power concept might be initially more appealing to defense operations, disaster response, or rural areas.

Derivation of the space segment contribution to SSP LCOE

[2] The expected contribution of the space segment to the LCOE of space-based power is a function of the deployment cost of the space segment C_{ss}, the received power

[2]Based on data and derivation from [41] and [40], with newly developed results and insights.

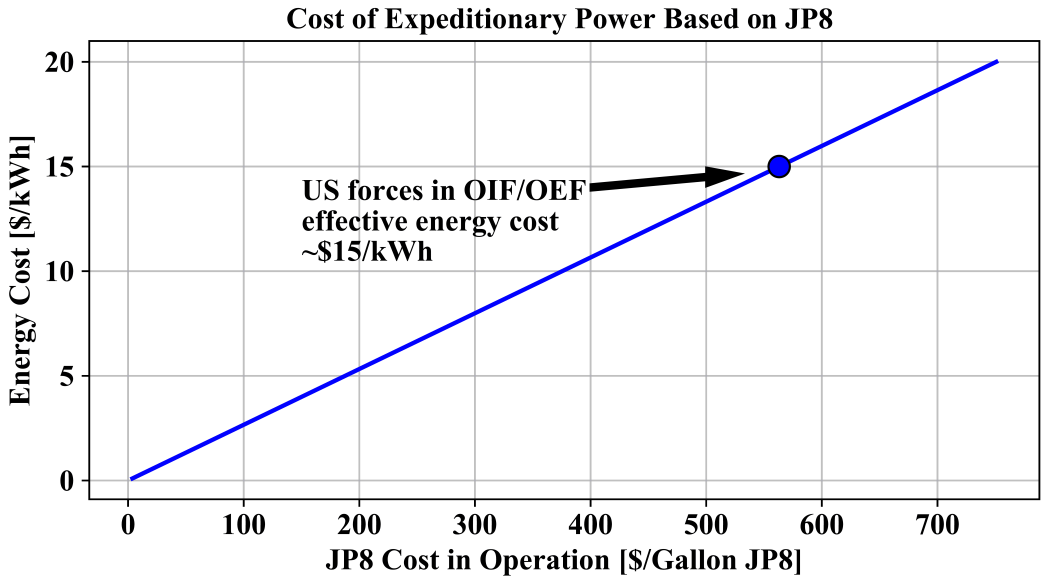


Figure 3.2: Cost of expeditionary power. Both JP8 cost and the JP8 cost of transport to destination affect total cost in operation [40].

on grid P_g, and the total illumination time expressed as $T_{il}[h/yr] \cdot T[yrs]$

$$LCOE_{ss} = \frac{C_{ss}}{P_g T_{il} T}[\$/kW \cdot h]. \tag{3.1}$$

Received power

The received power on ground can be found from the modified Friis formula [42]

$$P_g = \left(\frac{f}{c \cdot r}\right)^2 P_{DC}\eta_t A_t A_r \eta_r, \tag{3.2}$$

where f is the frequency of operation, c is the speed of light, r is the distance between transmitter and receiver, and P_{DC} is the DC power supplied by the photovoltaic cell. This equation can be further expanded as follows: the transmitted power $P_{DC}\eta_t$ can be re-written as

$$P_{DC}\eta_t = I_{AM0} A_{PV} \eta_{ss}, \tag{3.3}$$

where I_{AM0} is the sun power density in space of 1.36kW/m^2, A_{PV} is the photovoltaic receiver area, and η_{ss} is the total space segment conversion efficiency from solar to transmitted RF power. One special assumption that we will use throughout this calculation is that the stringent weight requirements effectively force a uni-body carrier for both the PV and RF modules of the space craft. Then, the most efficient

utilization of area is with $A_{PV} = A_t$ and the received power can be re-written as

$$P_g = \left(\frac{f}{c \cdot r}\right)^2 I_{AM0} {A_t}^2 A_r \eta_{ss} \eta_r. \tag{3.4}$$

The efficiencies associated with the space segment and ground power conversion can be further expanded to

$$\eta_{ss} = \eta_{PV} \cdot \eta_{DCRF} \cdot \eta_{Tx}, \tag{3.5}$$

in which

- η_{PV} = Photovoltaics to DC conversion efficiency
- η_{DCRF} = DC to RF conversion efficiency
- η_{Tx} = Transmitting antenna efficiency,

and

$$\eta_r = \eta_{diff} \cdot \eta_{RFDC} \cdot \eta_{DCAC}, \tag{3.6}$$

with

- η_{diff} = Main lobe power (diffraction efficiency)
- η_{RFDC} = RF to DC conversion efficiency including rectenna
- η_{DCAC} = DC to grid AC conversion efficiency.

Lastly, the ground receiver rectenna array is designed to fill the projected area of the main lobe from the SSP spacecraft(s). Depending on the orbit and the size of the transmitting aperture, the receiving rectennas can be either in the near or far field. Assuming circular apertures, the receiver aperture size A_r can be written as

$$A_r = (r\theta)^2 = r^2 \begin{cases} \frac{A_t}{r^2} + \frac{c^2}{f^2 A_t} & r < 2A_t f/c \\ \frac{c^2}{f^2 A_t} & r > 2A_t f/c \end{cases}. \tag{3.7}$$

Substituting (3.4) into (3.7) gives

$$P_g = \begin{cases} \left[\left(\frac{fA_t}{cr}\right)^2 + 1\right] I_{AM0} A_t \eta_{ss} \eta_r & r < 2A_t f/c \\ I_{AM0} A_t \eta_{ss} \eta_r & r > 2A_t f/c \end{cases}. \tag{3.8}$$

Orbital considerations

One of the primary challenges with space-based solar power is the design and maintenance of a satellite constellation in formation. In the past decade, substantial amount of research has been done on the guidance, navigation, and control of formation flying satellites [43][44]. Formation flight has also been demonstrated in space by missions such as GRACE [45], GRAIL [46], and PRISMA [47]. The detailed design of the formation flying constellation along with the associated sensing and actuation requirements is currently being pursued and will be presented at a later date. A critical decision in the orbital design of the space solar constellation is the choice of the orbit altitude. From a launch cost perspective, low Earth orbits (LEO) are easier to get to and place less stringent requirements on the beamwidth of the antenna array. But a LEO constellation would not be able to generate power 40% of the time on account of being eclipsed by the Earth. While the constellation could be placed in a terminator orbit (polar sun-synchronous 6am-6pm), it leads to a highly inefficient orientation for RF transmission. The LEO constellation would also require a network of ground-based receivers on Earth to continuously relay power from the space-based array. Moreover, in low Earth orbit, one must deal with orbital perturbations due to atmospheric drag, Earth oblateness (J2), and solar radiation pressure, further complicating the guidance, navigation, and control problem. On the other hand, a constellation in GEO can radiate all its power to a single ground-based receiver. The spacecraft is always in view of the sun, except for a few days of the year close to the equinoxes when the Earth eclipses the sun for up to an hour each day. While the electronics in GEO must survive a harsher radiation environment than LEO, maintaining a constellation in formation flight is relatively easier since we only have orbital perturbations from solar radiation pressure. Keeping these factors in mind, the point design presented in this paper assumes that the constellation is in GEO.

Cost of space array deployment

The number of spacecrafts N_{SV} that are needed to generate a total power of P_g is

$$N_{SV} = \left\lceil \frac{A_t}{A_{SV}} \right\rceil \tag{3.9}$$

with A_{SV} being a single spacecraft area. Substituting (3.8) into (3.9) yields

$$N_{SV} = \begin{cases} \left\lceil \frac{P_g}{\left[\left(\frac{fA_t}{cr}\right)^2 + 1\right] I_{AM0} A_{SV} \eta_{ss} \eta_r} \right\rceil & r < 2A_t f/c \\ \left\lceil \frac{p_g}{I_{AM0} A_{SV} \eta_{ss} \eta_r} \right\rceil & r > 2A_t f/c \end{cases}. \tag{3.10}$$

The ceiling operation accounts for the integer amount of spacecrafts in an array. There are a limited number of launchers at present, capable of putting large payloads into GEO. We characterize a given launch system's capability by M_{GEO}, the mass that the launcher can place into GEO, and κ, a de-rating factor for the launcher, acknowledging that some reserve mass is needed to accommodate uncertainty in the mass of the space vehicles and supporting structure for the space vehicles on the launcher [48]. Given κ and M_{GEO}, and the mass of the space vehicle, we can compute the number of space vehicles with mass m_{SV} that a given launcher can place into GEO, n_{SV}

$$n_{SV} = \left\lfloor \frac{\kappa M_{GEO}}{m_{SV}} \right\rfloor \quad 0 < \kappa < 1. \tag{3.11}$$

The number of launches needed to place all spacecrafts in GEO, assuming integer number of vehicles can fit in a launcher, is then

$$N_L = \left\lceil \frac{N_{SV}}{n_{SV}} \right\rceil. \tag{3.12}$$

The specific power S, radiated by each spacecraft in the array, can be defined as

$$S = \frac{I_{AM0} A_{SV} \eta_{ss}}{m_{SV}}. \tag{3.13}$$

Substituting (3.13) into (3.10) expresses N_{SV} in terms of the SSP system specific power independently from its mass. Since S contains all the design-space variables of the Tx/Rx performance and is decoupled from the launch cost parameters, it should be the optimization objective for the space segment design. With knowledge of N_{SV} and N_L, we begin to see how the system cost, and ultimately the levelized cost of electricity scale with P_g and m_{SV}. Fig. 3.3 shows the trends for the number of space vehicles and launches as a function of power to the grid based on a Falcon 9 Heavy launcher capable of placing 3,000 kg (3 MT) to GEO. Since both N_{SV} and N_L are linearly dependent on P_g, the space vehicle's mass and area determine the slopes of the graphs of both quantities as functions of P_g. Based on these relationships, we can estimate the cost of the space portion of an SSP system. To get a reasonable estimate for the space vehicle cost (payload, spacecraft,

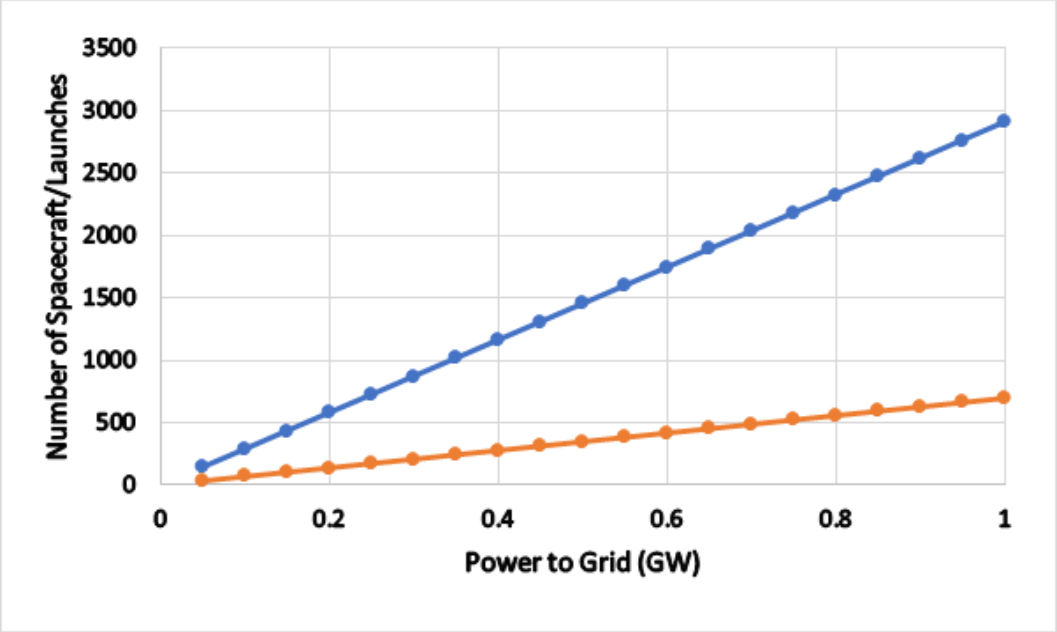


Figure 3.3: N_{SV} and N_L are linearly dependent on P_g. The slopes of the curves depend on the specifics of the space vehicle [41].

integration, testing, etc.), CSV, we employ a rule of thumb that space vehicles cost between \$90,000-\$250,000/kg on-orbit. The variation has to do with the space vehicle complexity, mission requirements, operational lifetime, etc. Another way of looking at the cost spread is the difference between building satellites for Class A, B, C, or D missions [49]. Class A is an operational mission with lowest possible risk, and is usually the most costly of the four classes. We assume that the SSP space vehicles are similar to Class A missions and use \$200,000/kg as a cost scaling figure. The launchers' cost, C_L, is between \$90M for a Falcon 9 Heavy to \$200M for an Ariane 6. A reasonable upper limit for the space portion cost is

$$C_{SS} = C_{SV,kg} \cdot m_{SV} \cdot N_{SV} + C_L \cdot N_L. \tag{3.14}$$

It is noteworthy that (3.15) ignores any cost decrease due to learning curves to produce the satellites and the launchers. Learning curves acknowledge the increase in efficiency of production of an item as the number of items produced is increased [50]. The equation also assumes that every launch is successful and that every satellite works to specification once on orbit. These are optimistic assumptions and therefore (3.15) provides a lower upper bound on cost for the space segment.

Table 3.2: Estimated values for $LCOE_{SS}$ calculation

Variable	Value	Details
I_{AM0}	1366 W/m^2	
r	40,000 km	GEO height plus steering angle
A_{SC}	3600 m^2	Based on structural design
f	10 GHz	See "Selection of operating freq." below
η_{PV}	0.25	Off-the-shelf best in class PV efficiency
η_{DCRF}	0.5	CMOS IC PA efficiency around X-band
η_{Tx}	0.96	High performance RF antenna loss at X-band
η_{diff}	0.84	Center lobe power for circular array
η_{RFDC}	0.82	Rectenna efficiency
η_{DCAC}	0.9	AC grid conversion efficiency
P_g	50 MW	Power to grid design target
$C_{SV,kg}$	200 \$K	Estimated above
M_{GEO}	3000 kg	Falcon 9 Heavy
κ	0.97	3% of M_{GEO}
C_L	90 \$M	Falcon 9 Heavy
T_{il}	8684 hr/yr	24 hr/day illumination except eclipses
T	20 years	Goal mission duration

Expected mission time

Assuming that the satellites operate at GEO, then they can produce energy 365 days a year, 24 hours a day except for twice a year during equinoxes. The total yearly eclipse time is approximately 80 hrs (the maximum daily eclipse time is less than 1 hour 10 minutes), so the total solar illumination time T_{il} is about 8,684 h/yr.

Quantifying the space segment contribution to the LCOE

With all parameters of (3.1) defined, we can now plot the space segment contribution to the LCOE as a function of launch cost and specific power. Table 3.2 shows the design goals and estimated values of $LCOE_{SS}$ equation variables.

Fig. 3.4 and Table 3.3 show the contribution of the space segment to SSP - $LCOE_{SS}$. Three specific data points are highlighted. The first is a fully integrated PV/RF unit cells which was built with available technologies and demonstrated as part of Caltech's SSP program. It measures 165 mm × 100 mm and weights 16.2 g, which scales to a PV/RF weight of 3530 kg for a 60 m × 60 m spacecraft. The

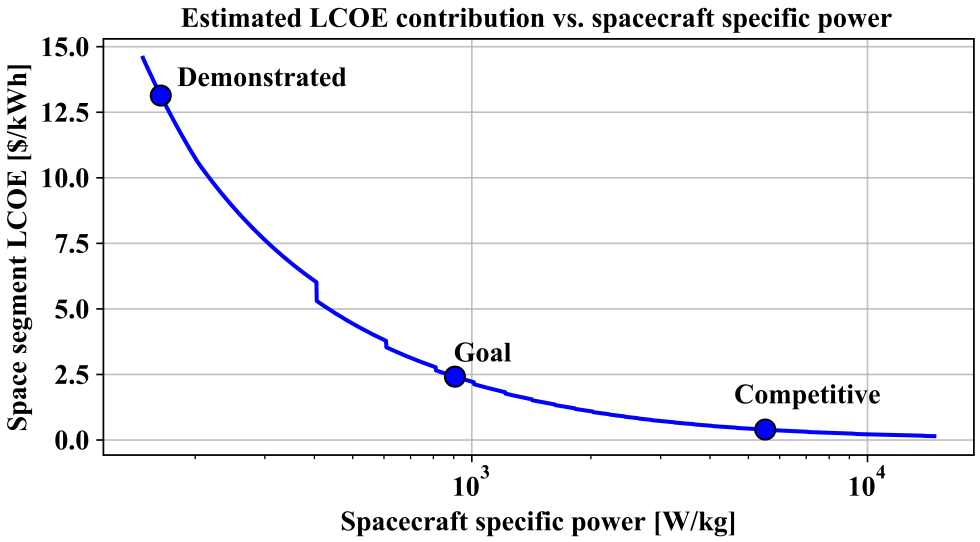


Figure 3.4: Space segment contribution to LCOE vs. spacecraft specific power.

Table 3.3: Estimated values for $LCOE_{SS}$ calculation

Quantity	Demonstrated	Goal	Competitive
m_{SV} [kg]	3605	651	107
S [W/kg]	163	906	5515
N_{SV}	137	137	137
N_L	170	35	6
Spacecraft Cost [$B]	98.8	17.8	2.9
Launch Cost [$B]	15.3	3.2	0.5
$LCOE_{SS}$ [$/kWh]	13.1	2.4	0.4

second is a mid-term design goal with ambitious but realistic build materials, of 1.6 g for a 100 mm × 100 mm unit cell. This translates to an RF/PV weight of 576 kg for a 60 m × 60 m spacecraft. An approximate wight of about 75 kg is assumed for the supporting deployment components: hubs, longerons, booms, etc. The last data point is a calculation of the required array specific power and mass to achieve $LCOE_{SS} = 0.4$. This amount of specific power will position an SSP system LCOE in the ≈ $0.5 range - competitive relative to current energy costs in developed European countries, for example.

In contrast, Fig. 3.5 and Table 3.4 calculate what should be the reduction in spacecraft build and launch costs, to make our demonstrated and goal designs competitive in terms of raw LCOE. This is done by introducing a cost reduction

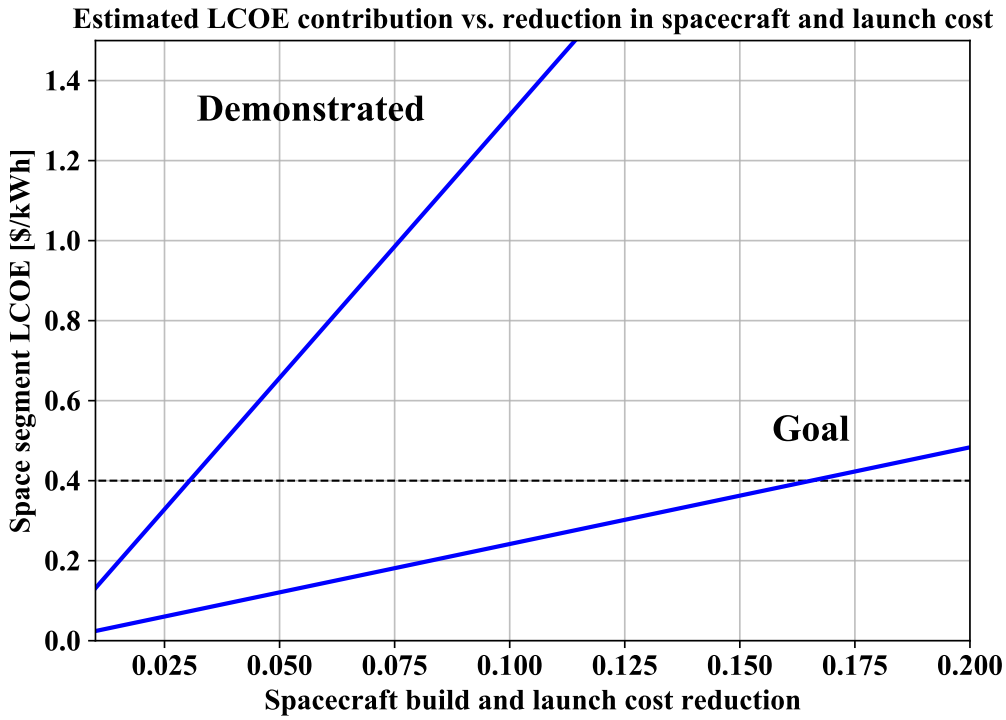


Figure 3.5: Space segment contribution to LCOE vs. reduction in the cost of build and launch of an SSP spacecraft.

Table 3.4: Estimated values for $LCOE_{SS}$ calculation

Quantity	Demonstrated	Goal
m_{SV} [kg]	3605	651
required cost reduction*	0.03	0.166
Total Spacecraft Cost [$B]	2.96	2.96
Total Launch Cost [$B]	0.46	0.52
Spacecraft Build Cost [$K/kg]	6.0	33.2
Single Launch Cost [$M/Launch]	2.7	14.94
Spacecraft Build+launch Cost [$K/kg]	6.93	39.06

∗ Assumed proportional reduction in build and launch costs

factor, α such that

$$C_{SS} = \alpha(C_{SV,kg} \cdot m_{SV} \cdot N_{SV} + C_L \cdot N_L). \tag{3.15}$$

Note that without additional information, we assume a proportional reduction in both build and launch costs over time.

Conclusions

The calculation above is a simplified cost estimate. Several other important factors that might affect the final system LCOE are: RF phased array's array coefficient, angular efficiency of the PV cells, receiving and transmitting energy when earth is between the sun and the array, financing/loan issues of such a high cost project, and more. It does, however, provide very useful information. It is clear that the system viability is highly dependent on its specific power and that with current technologies, with the current costs of similar extraterrestrial missions, SSP is about two orders of magnitude more expensive than terrestrial power. Even if significant technological advancements will result SSP arrays with higher levels (i.e. the "goal" level) of specific power, the space segment's LCOE will still be about an order of magnitude more expensive than power generated on Earth. On the other hand, the system already is, and can more so be in the near future, a competitive energy source for expeditionary operations and as emergency event response. As said before, an SSP system adds the benefit of dynamic power allocation and is able to power extraterrestrial missions as well. Moreover, the spacecraft build and launch costs that will make the system economically competitive can be two to three orders of magnitude higher than predicted two decades ago [51]. In this respect, Caltech's SSP program has made a significant advancement in enabling solar space power as a significant source of sustainable, clean energy.

The following sections will detail some of the design choices which lead to the above results, with emphasis on parts in which I was involved.

3.3 System Level Design

This paragraphs will detail some of the design choices which lead to the above results, with emphasis on the parts in which I had a significant contribution.

Frequency of operation

The selection of the frequency of operation is probably the single most important design choice for the RF part of the SSP system. It affects power conversion and transmission efficiency, antenna density and design complexity, and has significant implication on thermal dissipation and final weight of the integrated module.

From raw efficiency perspective, it can be shown that the frequency of operation should be within the low-gigahertz range. We assume that power is converted to RF using a high-efficiency switching amplifier [52]–[54] where transistors are used as switches and passive devices are used for impedance matching. The passive

efficiency is, fundamentally, frequency dependent. In most cases, the limiting components are inductors, of which size generally decreases and quality factor generally improves with an increase in the frequency of operation. It can be shown [55] that if a PA is matched by n passive sections to the system's output, the matching impact on the total efficiency can be calculated as

$$\eta_{passive} = \left(1 - \frac{\sqrt{\sqrt[n]{PER} - 1}}{Q}\right)^n , \tag{3.16}$$

where Q is the (frequency dependent) matching section quality factor and PER (power enhancement ratio) is the ratio of the required power to the power generated over an easily realizable impedance (e.g. 50 Ω) assuming a peak voltage limited operation. A more intuitive and less quantitative definition of PER is as follows: the optimal impedance shown to a PA depends on the supply voltage and output power - the higher the power, the lower the impedance. If this power should drive a transmission line or an antenna (usually, but not exclusively 50 Ω), then an impedance matching is required. PER is the impedance ratio R_{out}/R_{in} realized by the matching network. The passive efficiency therefore decreases with PER and increases with Q, while different values of n limit the designer to a specific range of realizable PER. Fig. 3.6 illustrates the achievable efficiencies for the required PER, given n and $Q = Q_L$, the quality factor of the matching network inductor. In contrast to the passive components' behavior, the active components' (switches) impact on efficiency deteriorate with frequency. The quantification is architecture and process dependent, but the fundamental reason is the increasing difficulty to prevent temporal overlap between the voltage drop along the transistor and the current flowing through it. The overlap manifests as power dissipation in the switch effectively increasing the loss. Figure 3.7 shows an estimate for the achievable drain efficiency of a 65nm switching PA, given off- and on-chip passives quality factors (50 and 20, respectively), and simulated switch efficiency for a 65 nm bulk CMOS process. Obviously, using high-Q, off-chip passives is favorable for the system performance, but is unacceptable from weight standpoint, where a 1 gr inductor will consume about 60% of the allotted weight of a 10 cm × 10 cm area of the goal system design of 1.6 gr. Keeping with on-chip passives, we see a plateau in the achievable drain efficiencies between 1 GHz - 10 GHz.

With the above efficiency estimates, we can now compare the focusing capability at different frequencies. The first diffraction minimum at a distance R from a circular

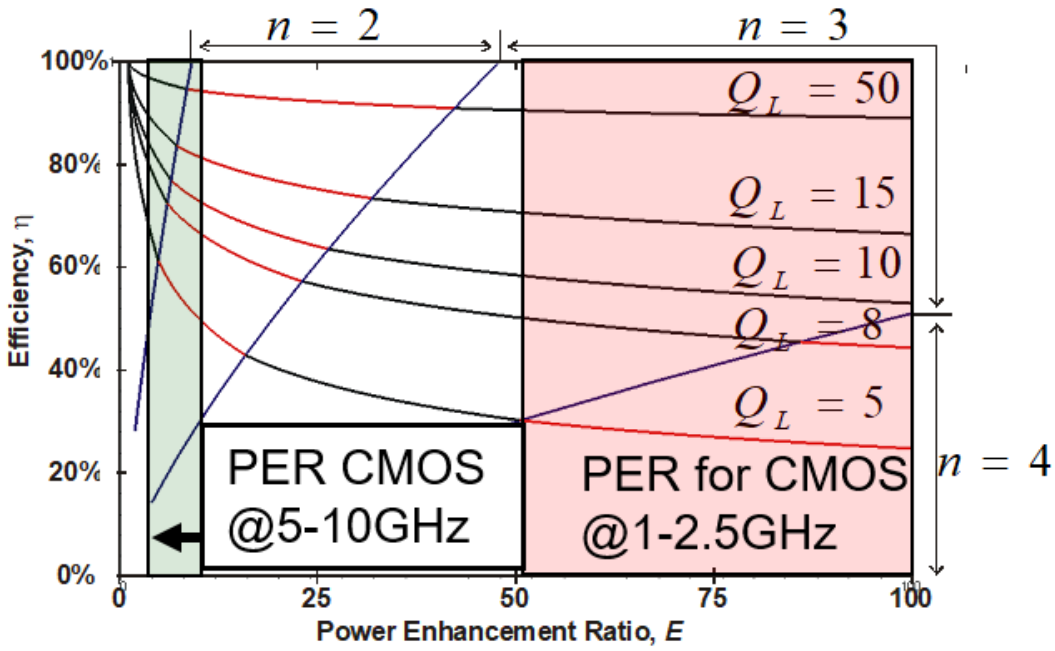


Figure 3.6: Achievable efficiency for given PER, quality factor, and number of output matching stages [55].

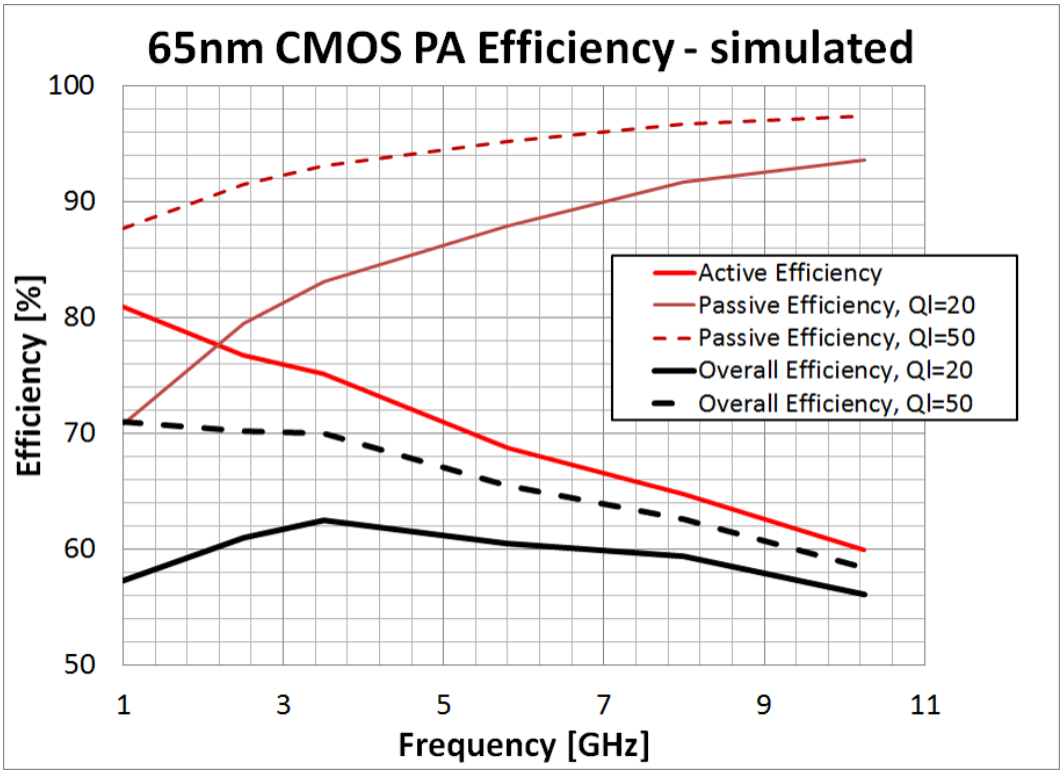


Figure 3.7: Power amplifier efficiency versus frequency as a combination of passive and active component efficiencies (Fig. courtesy of Dr. F. Bohn).

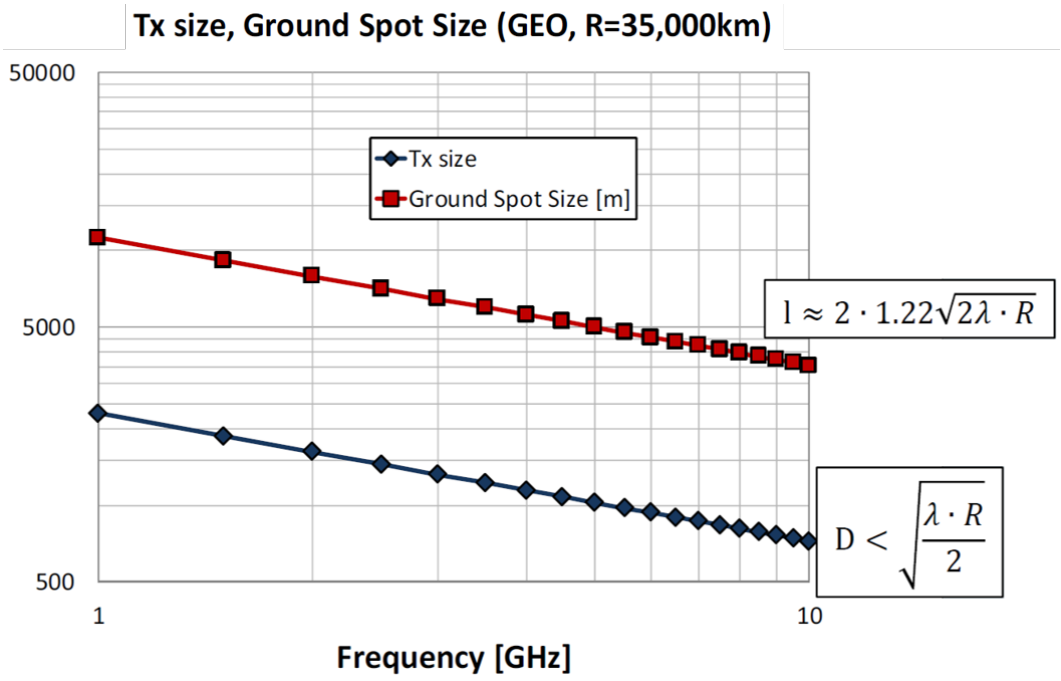


Figure 3.8: SSP array size and its far-field spot size versus frequency of operation (Fig. courtesy of Dr. F. Bohn).

array with diameter d is approximately [56]

$$D_1 = 1.22\frac{R\lambda}{d} \tag{3.17}$$

in the *far-field* of array. Thus, higher frequency of operation results in a smaller collecting area on the ground. Interestingly, due to the square dependence of the far-field (*Fraunhofer*) region on the aperture [42]

$$R_{ff} = 2\frac{d^2}{\lambda}, \tag{3.18}$$

the far-field distance of even a relatively small array at high frequency can be significant. For example, at 10 GHz, a 720 m array's far-field is at approximately 35,000 km, as far away as a GEO orbit. Fig. 3.8 shows the beam size on ground for an array diameter with far-field at GEO versus frequency. One important remark about the far-field approach is that an antenna array does not have to operate at far-field. The beam can also be focused if operating in the near-field (*Fresnel* approximation), and the beam area can be approximated using (3.7). Thus, from focusing standpoint, higher frequency of operation is more desirable.

Fig. 3.9 shows the attenuation of RF waves through the atmosphere. Notably, above

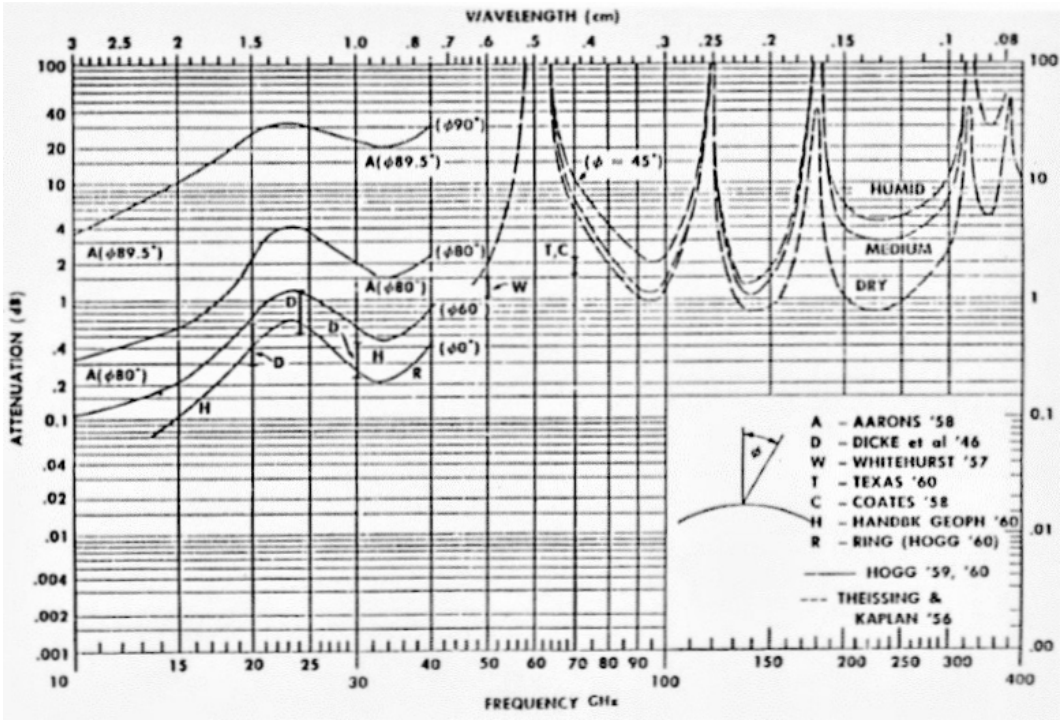


Figure 3.9: FCC's graph of RF attenuation through the atmosphere [57][58]

10-15 GHz, millimeter-waves start suffering from significant attenuation. Therefore the frequency of operation should not be much higher than that.

Lastly, the frequency of operation determines the amount of required antennas per unit area. Assuming a standard 0.5λ spacing in vacuum between antennas, N, the number of antennas per unit area $[Antennas/m^2]$ is calculated as

$$N \approx \frac{f^2}{0.15^2} \tag{3.19}$$

where f is the operating frequency in GHz. Since the power per unit area is determined only by the solar power intensity in space, I_{AM0}, each antenna radiates a power of

$$P_{ant} = \frac{I_{AM0}}{N}. \tag{3.20}$$

Fig. 3.10 shows N and P_{ant} as a function of frequency. While working at low frequency allows for a simpler radiators array design, higher antenna count means that less power is dissipated by each antenna. This has two important implications: first, it requires lower PER and thus allows to achieve higher conversion efficiencies for given on-chip passive quality factors. Second, since each PA dissipates less power, higher antenna count distributes the heat dissipation across the carrier sheet.

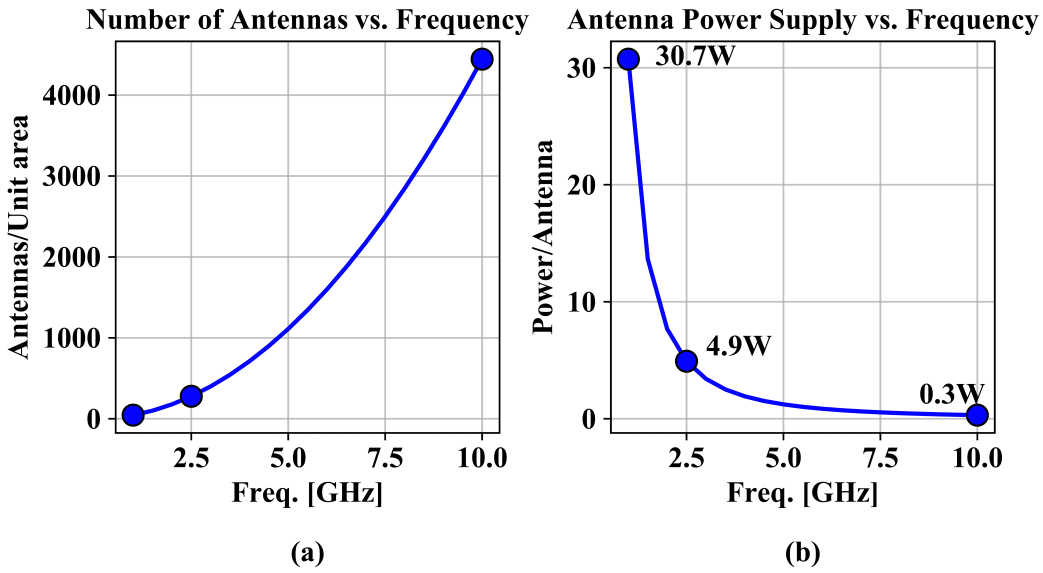


Figure 3.10: Change in (a) number of antennas per unit area and (b) power supply to be radiated by each antenna vs. frequency of operation.

In space, heat dissipation to the environment is radiative (no convection) and thin metallic sheets are poor thermal conductors. Increasing the number of ICs per unit area alleviates much of the thermal dissipation challenge as will be shown later.

Architecture and materials

The architecture and materials for building a lightweight SSP spacecraft are divided into tile- and spacecraft-level. The first is handled by the solar structures and RF electronics teams while the latter is handled by the lightweight solar structures group. This chapter will briefly describe the spacecraft level design, survey the current and asymptotic weight goals, and detail the demonstration structures that were built at Caltech with currently available technologies.

In order to minimize the array weight and ease its deployment, the SSP array is envisioned as a large sheet, assembled from flight-synchronized modules. Following the discussion of cost perspective, the array size is derived from the required power received and beam width on earth. Each module is a separate spacecraft, containing a large number of tiles, held together in groups (panels). Fig. 3.11 illustrates the array's build and function.

The formation of the whole structure in space is yet to be developed, but the deployment of each spacecraft has been discussed, proposed, and implemented as a

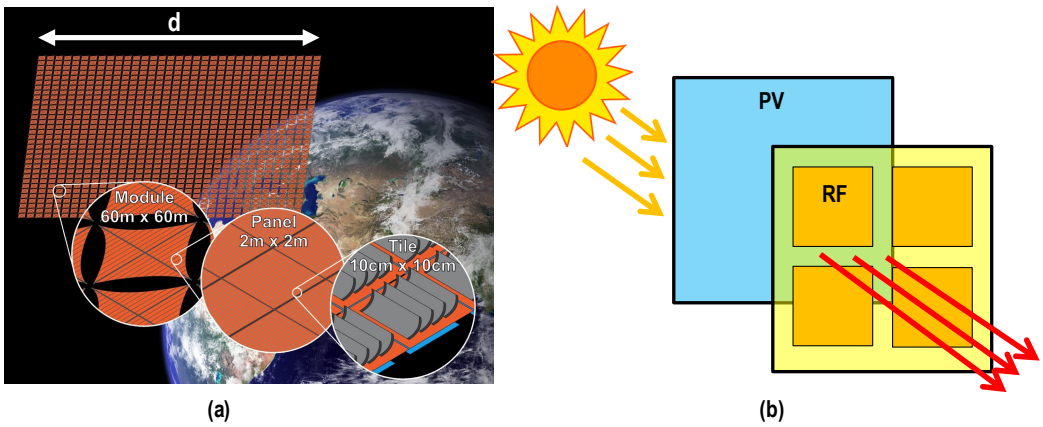


Figure 3.11: Conceptual SSP array: (a) Array, spacecraft, panel and tile levels and (b) concept of operation of an SSP sheet PV-RF power conversion system.

1 m × 1 m prototype, non-functional structure [59] illustrated in figure 3.12.

While this architecture fairly is developed, one drawback is the inconsistent power delivery capability throughout the day. If the RF and PV panels are on opposite sides, the system cannot both receive solar power and transmit it to Earth, when Earth is between the array and the sun (Fig. 3.13a). This effectively halves the power output or doubles the cost of the system's space segment. There are several solutions in development to place RF antennas and PV panels on the same side of a sheet as shown in Fig. 3.13b. Such are low fill-factor antennas (wires), optically transparent ground planes, and flat photovoltaic cells.

The unit cell itself is designed to maximize the specific power of the system in a progressive fashion. The initial design goal aims for the highest achievable specific power with current technologies. The asymptotic goal tries to extrapolate what will be available in the future and the implications on specific power. In parallel to those, a third design was built using available production materials to demonstrate and explore the system's features and design space. The tile's light weight is enabled by a single RFIC that performs most of the tile functions. In the final design stage this RFIC will contain, other than RF chains, a micro-controller on the same or on a separate die, a non-volatile memory, and power regulators, leaving only the antennas and a few capacitors off-chip. It will be mounted on an ultra-thin layer of polyimide and the board's conductors will be made of aluminum, which offers superior mass

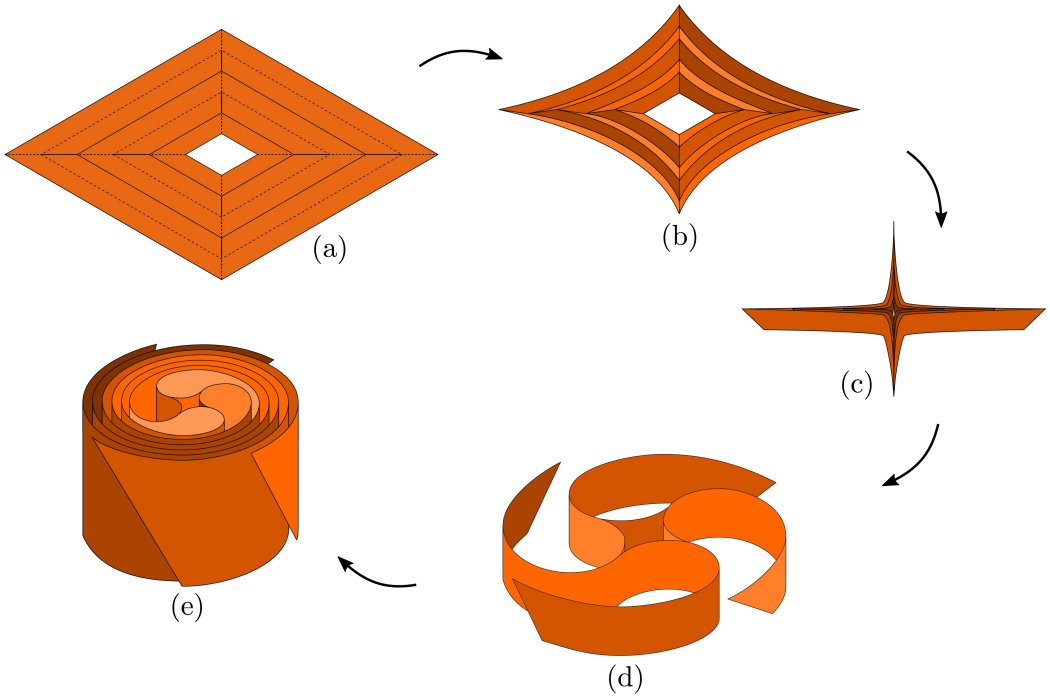


Figure 3.12: SSP spacecraft packaging: (a) Deployed, (b) collapsed plain, (c) folded inwards, (d) collapsed sideways and rolled, and (e) packed [59].

density over copper with negligible hit in conductivity. In order to further reduce weight, the PV cells do not cover the whole back side of the tile, but are made of stripes attached to the back of parabolic reflectors (blinds). The latter are designed such that their focal point is on the PV cells and light that hits them is completely concentrated there. From system-level perspective, attaching the PV and RF parts of an SSP system directly together is a major weight-saving concept. Otherwise, DC cables would be needed to distribute the collected solar power, with a **significant** hit on wither weight, efficiency, or both. The RF antennas, mounted on the other side of the tile, are fabricated on a second ultra-thin polyimide layer and are separated from the main board with an air gap, serving as the cavity or separation (depending on antenna type to be used) enabling the antennas to radiate. To minimize weight, the antenna layer will be suspended in air with a lightweight frame and "s" shaped springs made of fiberglass or other material. Tables 3.5 and 3.6 detail the complete estimate for a 10 m $\times$ 10 m tile materials as well as a spacecraft weight breakdown.

An asymptotic estimate to the expected improvement over time of the tile weight was given in [40]. It is based on the estimate of the involved groups to the reduction in mass possible in the tile and spacecraft components, and is detailed in table 3.7.

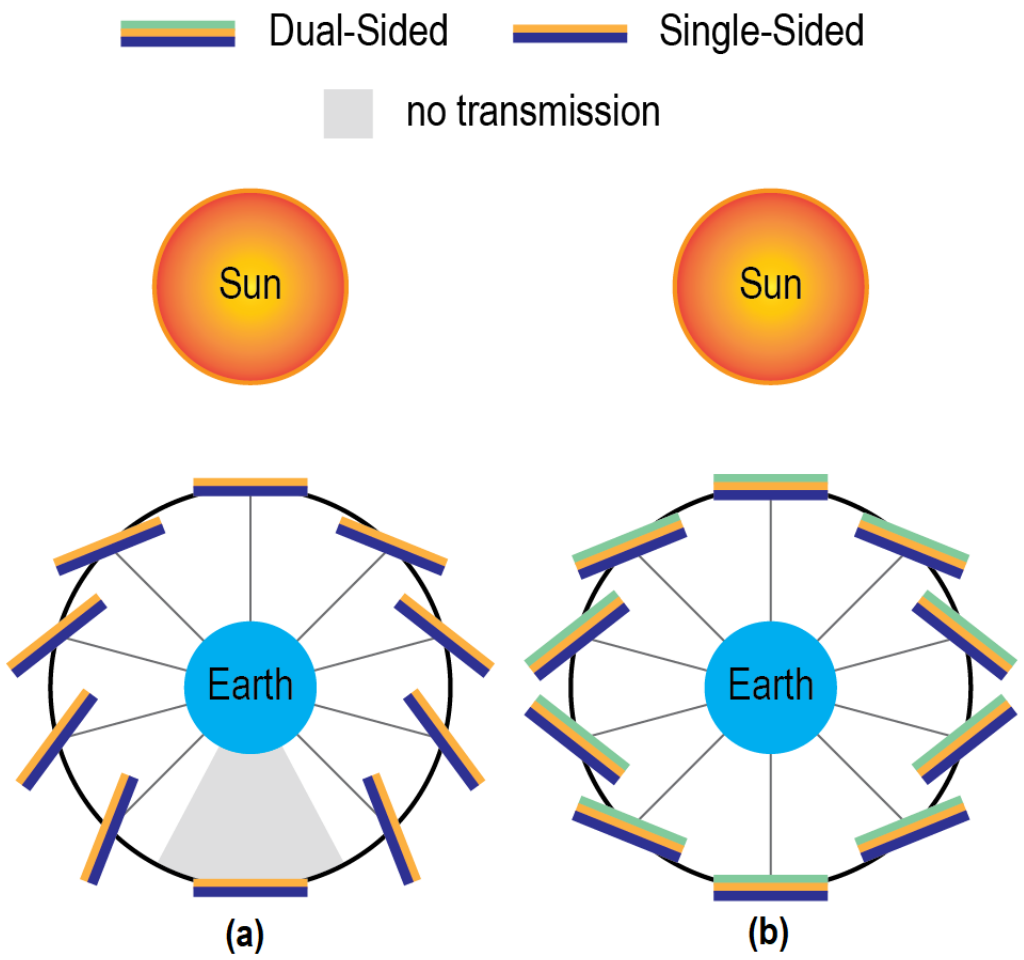


Figure 3.13: Comparison of (a) a single-sided RF/PV vs. (b) a dual-sided RF/PV SSP spacecraft coverage [41].

Table 3.5: Breakdown of mass contributions and total mass of a 10 cm × 10 cm tile

Layer	Material	Thickness [μm]	Mass [gr]
Concentrator Reflective	Al	10	0.324
Concentrator Backing	Kapton	10	0.170
Front Emissive Layer	SiO_2	4	0.122
PV Cell	III-V, Cu	40	0.257
Tile Support	Kapton	10	0.142
Routing Layer	Al	5	0.135
Antenna Backing	Kapton	10	0.142
Antenna Conductive	Al	2	0.054
Si IC and Shield	Si/Al_2O_3	300/1000	0.116
Carbon Fiber Frame	Carbon	Various	0.138
Total			**1.6**

Table 3.6: Mass breakdown of a 60 m × 60 m spacecraft

Component	Mass (kg)
Tiles	576
Hub	50
Strip structure (longerons and battens)	19
Booms	6
Diagonal cords	0.01
Total	**651**

Table 3.7: Expected improvement in areal mass between SSP iterations

Architecture	PV [gr/m^2]	RF [gr/m^2]
Mk 0	790	820
Mk 1	390*	445
Mk 2	36.4*	22
Asymptote	13.4*	11

* These are intended to use Perovskites which will reduce η_{PV} from 28% to 20%

While advancements in the development of materials and technologies are made, an SSP tile prototype, shown in Fig. 3.14, was built using existing technologies. This prototype will be discussed thoroughly in section 3.5. The prototype resembles the proposed final product, but its materials, dimensions, and weight differ in the following aspects:

- The tile is designed for a single 16-output chip. Element spacing is chosen to be 0.6 λ, to minimize antenna coupling while maintaining reasonable grating lobes. Hence RF radiator size on tile is 7 cm × 7 cm.
- The main board is fabricated using off-the-shelf polyimide (kapton) laminates. Fabrication and RF routing constrains its thickness to roughly 300 μm. Metal layer thickness is off-the-shelf 17 μm.
- The PV cell design necessitates some on-board regulators to handle chip required voltage levels.
- The photovoltaics are less efficient than the design goal and cannot supply the required power to the chip to function properly at AM0 solar power intensity. As a result, the finished size of the tile was increased to 16.5 cm × 10 cm.

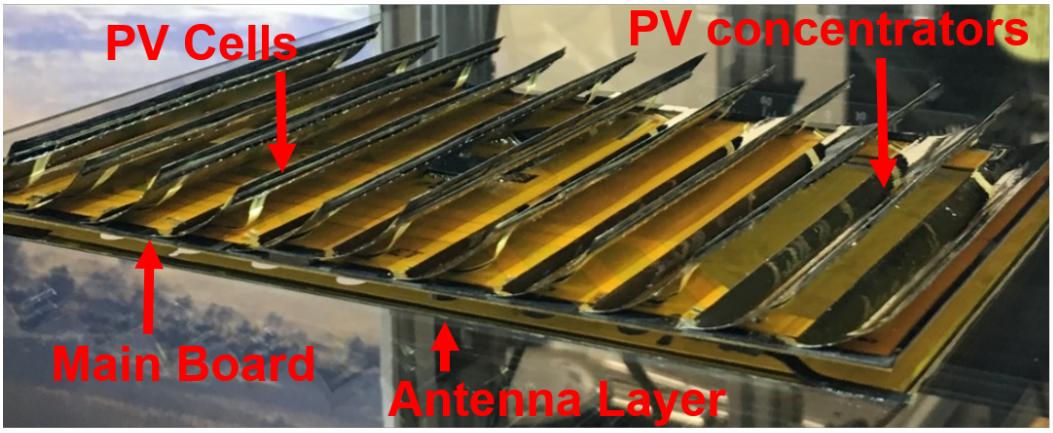


Figure 3.14: A photo of an SSP tile prototype.

– The finished system weight is about 16.2 gr.

While this demonstration board is about 15 times heavier than desired, it is still more than an order of magnitude lighter than similar systems [60]. Later in this thesis, an expansion of the base design of this RF tile is used to build a flexible, fully operating phased array with 256-elements.

RFIC thermal management

There is a loss associated with any power conversion system due to the imperfect nature of electronic components. This loss manifests as heat generated by the power converter and dissipated to the environment through the following mechanisms:

– **Conduction**: Heat interacts with matter and dissipates locally, thus elevating the material temperature.

– **Convection**: Heat transferred by mass motion, where the heated mass moves away from the heat source and thus carries the heat energy away with it. In this context, convection usually accounts for the interaction between the static circuit board and dynamic surrounding air.

– **Radiation**: Transfer of heat energy as electromagnetic waves, due to movement of charged particles in matter. In this context, heat transfer by radiation also accounts for heat transfer between circuit board and the environment.

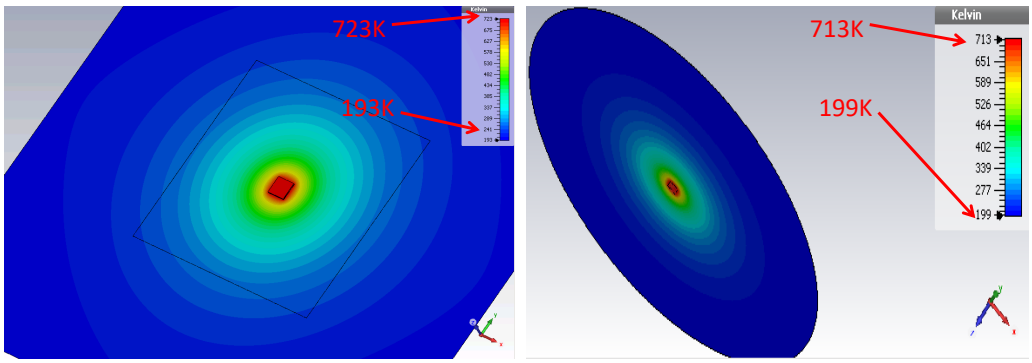


Figure 3.15: IC temperature in space due to heat dissipation on (a) a square tile and (b) a circular tile.

In space, heat conduction is assumed to be similar to Earth, however convection does not occur due to the absence of matter. The background temperature, relevant for radiative heat dissipation, is much lower than on Earth, especially for the spacecraft face that is not facing the sun. The total heat dissipated by RFIC due to DC-RF power conversion is:

$$P_{diss} = I_{AM0} A_t \eta_{PV} (1 - \eta_{DCRF}) \tag{3.21}$$

qith the quantities defined in (3.2)-(3.4). To estimate the tile's IC temperature, we assume that its surface area is 100 cm^2. η_{PV} was assumed 30% and η_{RF} 50%, leading to P_{diss} of roughly 2 W. Thermal simulation was run using CST microwave studio with a 5 μm layer of aluminum ground plane. The aluminum emissivity was assumed to be 0.8 on a single side to account for the fact that its back is blocked by PV structure. Fig. 3.15 shows the simulation results for square and circular tile structures. The circular tile is a simplified version for the thermal design optimization that will be described below. Clearly, this temperature far exceeds silicon ICs' operating temperature range, and requires a more efficient thermal design. The most important observation is that the large temperature gradient is due to the poor thermal conductance of the thin aluminum and does not depend much on the radiative heat dissipation, which is set anyway. The solution is therefore to use a variable thickness ground layer as shown in Fig. 3.16. Thermal conductors can be modeled as equivalent circuit resistors [61]. We try to capture a steady state behaviour, and therefore we are not modeling heat capacitance here. In this case, a metal plane is equivalent to a series of resistors, with values which quadratically reduce with radius. Therefore, an improved thermal design will

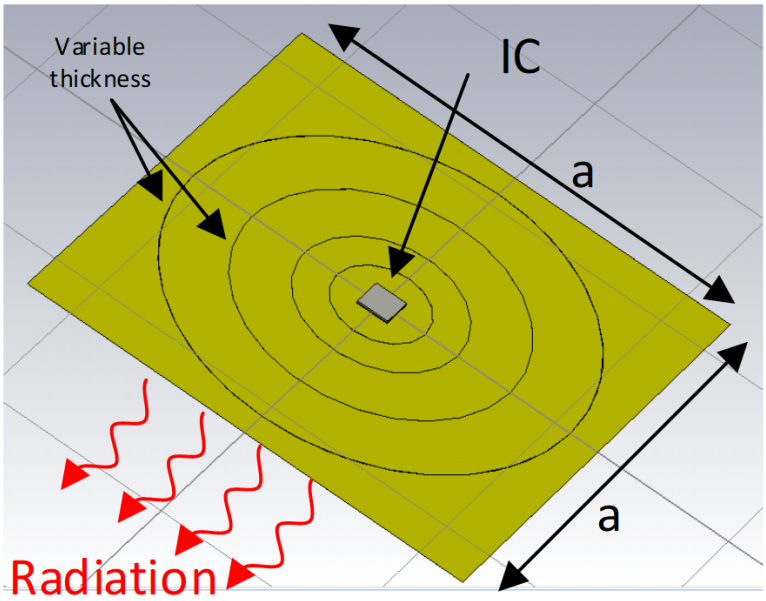


Figure 3.16: Thermal optimization simulation setup.

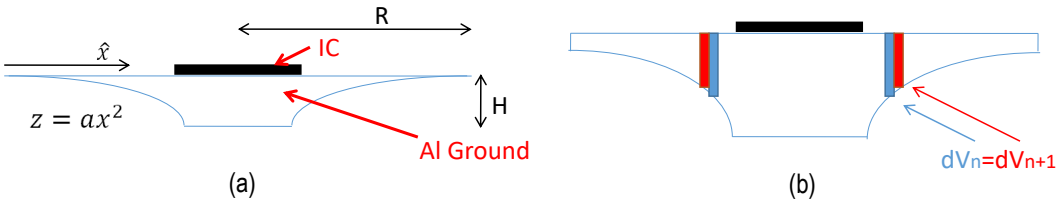


Figure 3.17: Quadratic ground plane profiles. (a) Zero edge thickness. (b) Equal volume.

utilize a varying-thickness ground plane, with a quadratically increasing thickness towards the tile center. Two analytical models are considered as illustrated in Fig. 3.17. The first profile has a quadratically increasing metal thickness from zero at the tile edge ("zero edge thickness"). The second profile keeps the total metal volume constant underneath any constant width annulus around the center ("equal volume"). As a reference, these models were compared to a discrete optimization simulation in which 5 concentric discs with varying height and radius are found to minimize the maximum board temperature. The optimizer uses Nedler-Mead algorithm and is set to preserve the total volume of used metal plane. Fig. 3.18 shows a point optimization and the differences in metal profiles for the three methods described above. After redistributing the metal ground profile, the RFIC temperature significantly drops to 395K or about 120°C, a high, but manageable value. Fig. 3.19

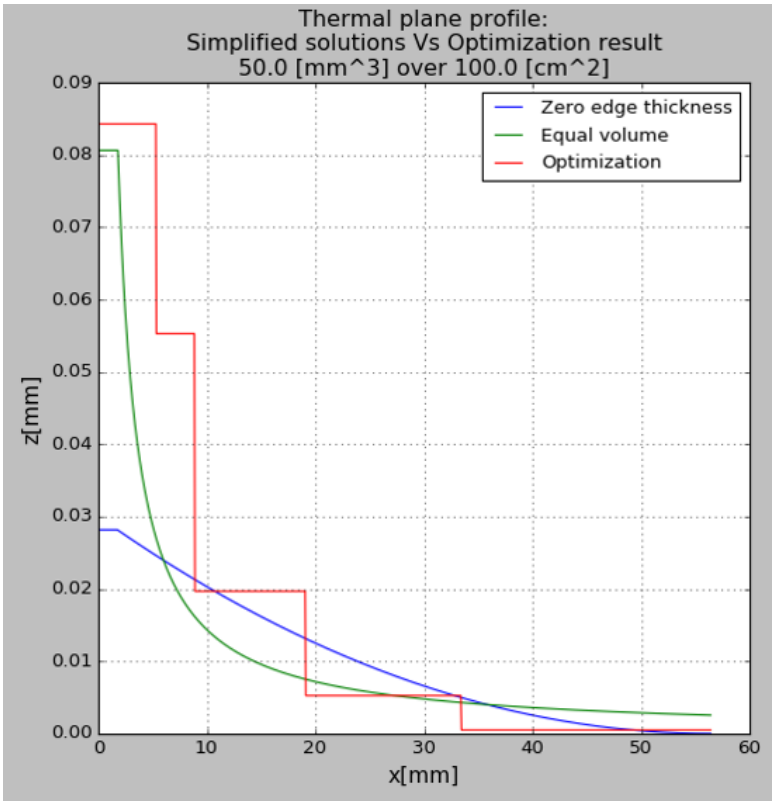


Figure 3.18: Varying ground thickness for each of the thermal conduction improvement schemes.

shows how the maximum board temperature is varying with the amount of heat that each IC dissipates for the three proposed metal profiling methods. This sweep is an equivalent to the frequency of operation, where a higher frequency corresponds to more ICs per unit area and therefore less power dissipated per IC. These results confirm that the "equal volume approximation" is an adequate analytical method to improve IC temperatures by using a gradient ground thickness. The difference from lengthy, brute-force optimization is less than 10% with a much shorter simulation time. Fig. 3.20 shows, using the "equal volume approximation," how the amount (weight) of aluminum used for the ground plane affects the IC temperature. It can be further used as a thermal design guideline when the system performance/cost trade-offs are considered. Lastly, an RF tile with equivalent PV heat sources was simulated. This time the size is set to 6 cm $\times$ 6 cm, according to a frequency of operation of 10 GHz, with 4 $\times$ 4 antennas separated by 0.5 λ, and an RFIC that dissipates 0.72 W. Vertical "fins" with strip heat sources were added to the structure to emulate the PV cells. Each of them was set to dissipate 2 W according to a PV efficiency of $\approx$ 30%. Mock antenna patches were added in front of the IC ground

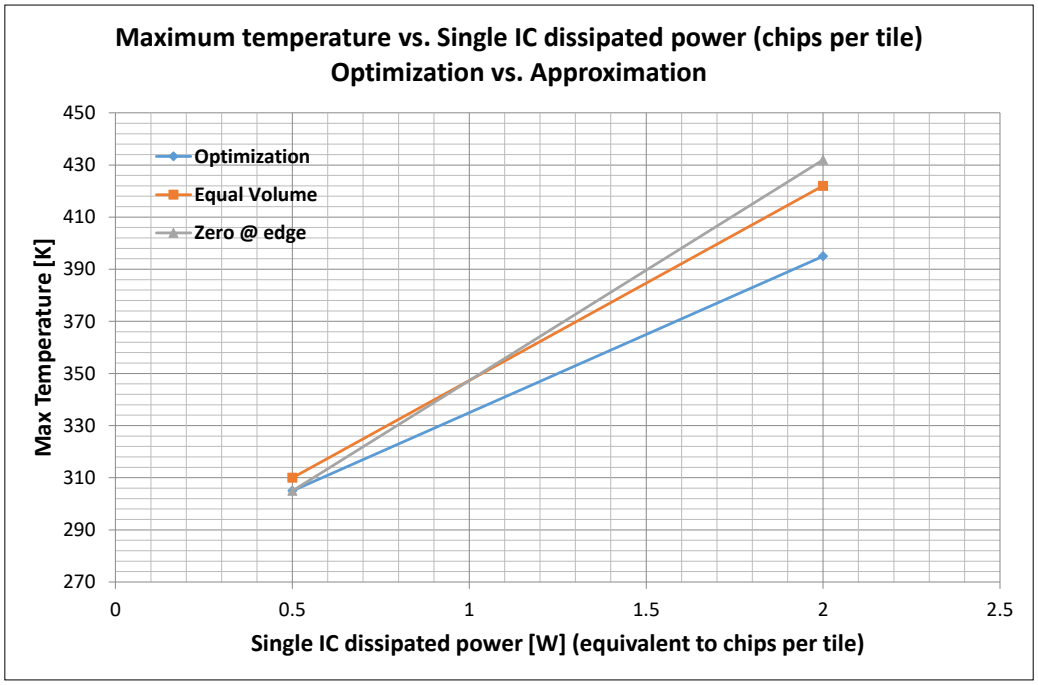


Figure 3.19: Expected temperature as a function of power per chip, all ground leveling schemes.

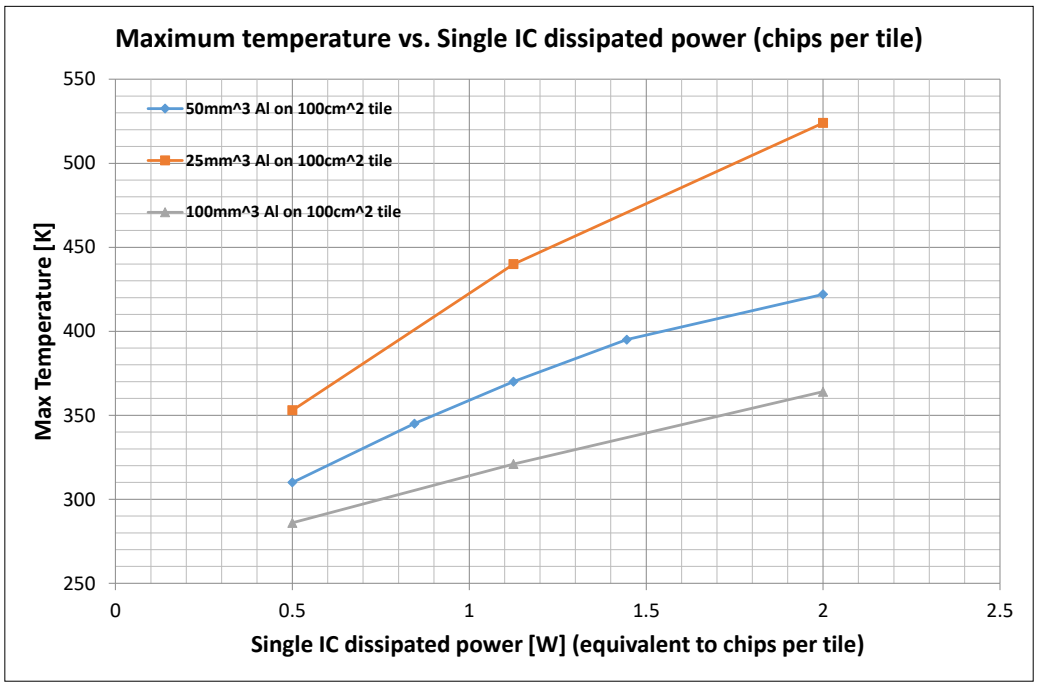


Figure 3.20: IC temperature as a function of power per chip for different ground metal volume, "equal volume" approximation.

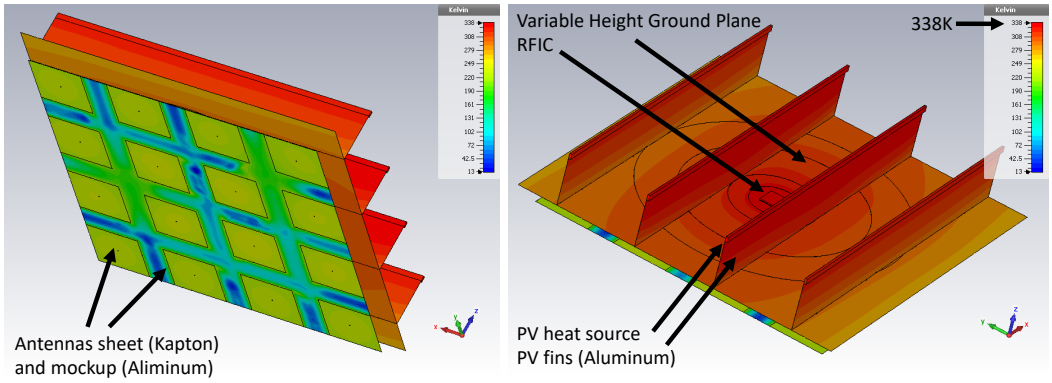


Figure 3.21: Estimated temperature of tile with PV and RFIC heat sources in space.

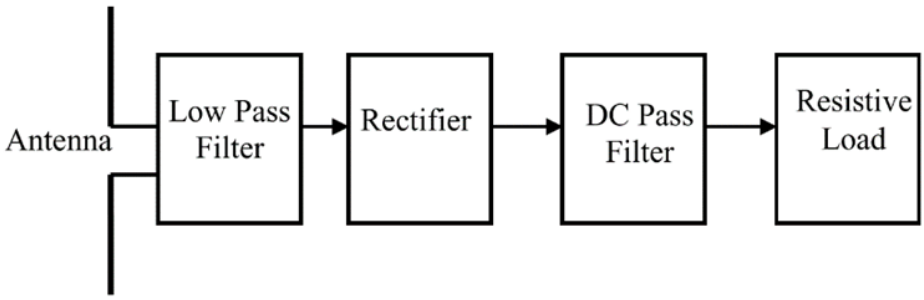


Figure 3.22: A basic rectenna design.

plane and antenna emissivity is again estimated at 0.8 (black paint). The PV side emmisivity is assumed to 0.5. Fig. 3.21 shows the simulated structure and results. A maximum temperature of about 65°C is acceptable and demonstrates the viability of the tile design from the thermal aspect with regard to the cooling mechanism and choice of frequency of operation.

Ground receiver array

So far, the ground receiver part of the system is the least developed. Conceptually, it will be designed as an array of RF to DC converters (rectennas) that will collect and convert the transmitted RF power on Earth. The general structure of a single rectenna includes the receiver antenna, a low pass filter, diodes for RF-DC conversion, and a filtering element to suppress AC components in the rectified waveform, and is illustrated in Fig. 3.22. Even though the basic concept is simple, the design of efficient RF-DC converters is challenging due to the non-idealities of physical components. The diode, which exhibits series resistance, non-zero built-

in voltage, and, at high frequencies, considerable contact inductance and junction capacitance, sets limits for both efficiency and feasible frequency of operation. Passive component losses, which result from the capacitors' dielectric ceramic filling, the inductors' skin effect, and the surface roughness of transmission lines, can also become significant in wavelength-scale RF circuits. Recent studies report efficient rectenna implementations in GHz range, achieving as high as 73%, 83%, and 60% at 2.45GHz [62], 4.5GHz [63], and 10GHz [64], respectively, and similar efficiencies are expected for the SSP ground receivers.

Safety aspects

RF radiation is generally defined as electro-magnetic waves with frequencies of 3 KHz – 300 GHz. RF radiation is non-ionizing, since the photon energy associated with EM waves at those frequencies is not high enough to pull electrons away from atoms and create ions [65]. Non-ionizing radiation has been shown to interact with biological tissue mainly via heat transfer. Studies have also reported other effects of exposure to RF radiation. Several examples are: in 1992, a large study by Chou *et al*. [66] investigated the potential effects of long-term microwave irradiation on rats, by exposing them to 0.4-W/kg SAR at 2450MHz for 13 months. It recorded various parameters, including behavior, blood chemistry/hematology, metabolism, and total body analysis, and found no definitive biological effect in rats chronically exposed to RF radiation at those frequencies. Another study by Lai and Singh [67] showed increased amount of single and double stranded DNA breaks in rats exposed to radiation resulting from whole body SAR of 1.2W/kg. However, an attempt by Malyapa [68] to measure similar results in alkaline comet assay under similar SAR rates while maintaining constant assay temperature, resulted in no significant difference from the control group. In 2010, the *INTERPHONE* study group published the results of a large scale study [69] that investigated a possible connection between cellular phone usage and brain tumors in 13 countries in Europe and Australia. The study observed no increased risk of glioma or meningioma to the average user and is referred here since cellular phones operate in GHz range radio frequencies. Other reported effects on humans include changes in the immune system, behavioral effects, neurological effects, and evidence for a link between microwave exposure and the action of certain drugs and compounds, all under specific exposure conditions [70]. Even though non-thermal biological effects of RF radiation were shown to *exist*, it is still unknown whether or not they impose a biological *hazard*. This fact has led regulators to adopt guidelines for maximum recommended RF powers

density exposure, which are derived from RF thermal effects on human body. For example, the American FCC recommends that professionals be exposed to RF radiation with a density of less than 50 W/m^2 averaged over 30 minutes. In the case of a receiver ground station, the energy density is expected to be 50 W/m^2 – within the FCC recommended limits. If RF radiation power density remains a concern, other measures can be taken, such as protective clothing. Also, since the transmitter is a directional antenna array, the main lobe carries most of the power. Therefore an area out of which the RF power density is negligible can be well defined for the convenience of the general public.

3.4 RFIC Design

An SSP RFIC should perform as many of the system's functions as possible with as few external components as possible. The main performance requirement is doing so accurately and efficiently. The RFIC therefore synthesizes a low noise clock from a low frequency reference, independently controls the phase and amplitude of its output channels, and drives its output antennas. Additional functions such as voltage regulation, biasing, and digital control and communication support the operation of the main system blocks. At a frequency of 10 GHz, the SSP spacecraft will have antennas with spacing of about 15 cm apart. The solar power supplied to the equivalent unit area is about 0.3 W, and about 87 mW (19.4 dBm) for each antenna PA, given a solar conversion efficiency of 25%. A small die on the order of 10 mm^2 is a logical choice for an SSP RFIC. It will not be subject to significant stress when mounted on a flexible substrate and its size can fit about 16 transmit chains without unreasonable design complexity or thermal management. By synchronizing multiple RFICs to a single reference signal, this approach provides a building block to build highly scalable and potentially very large-scale phased-arrays [71].

The RFIC in Fig. 3.23 utilizes 17 on-chip PLLs performing a two-step RF power generation. The on-chip central, programmable PLL in Fig. 3.24 synthesizes a 2.5GHz RF signal from a low frequency, 5 MHz - 200 MHz external reference clock that is distributed to different RFIC units. The chip also utilizes buffers and a delay-locked loop (DLL) circuitry [72] to allow retiming and redistribution of the low frequency reference between chips (Fig. 3.25). This is crucial when large arrays scale to a size where it is impractical to use a single central clock source to directly drive all the system RFICs. The 2.5 GHz frequency generation and distribution will be described in detail in the next chapter.

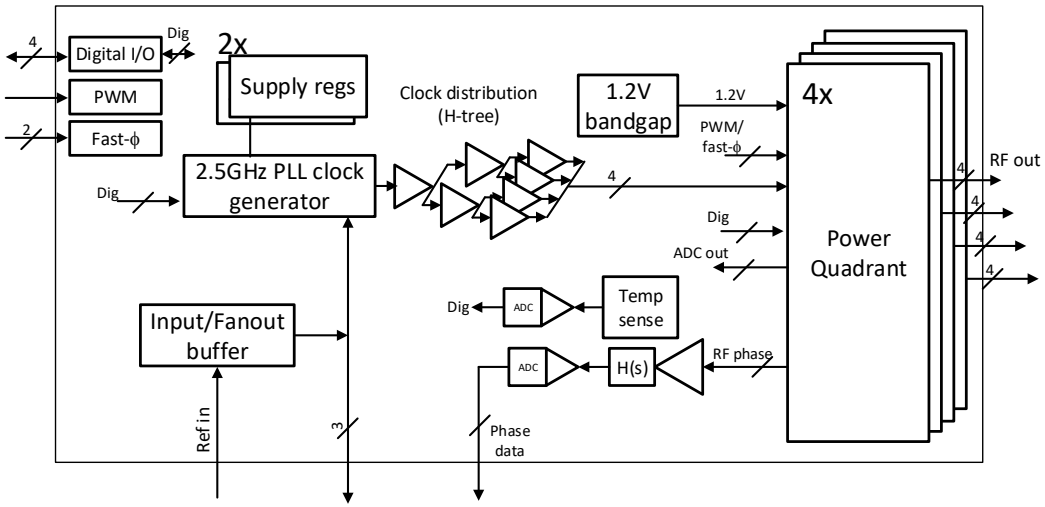


Figure 3.23: A top-level schematic of the SSP RFIC.

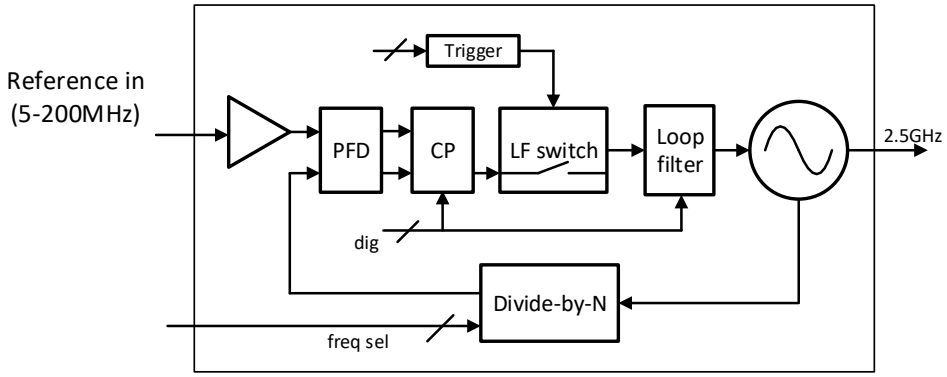


Figure 3.24: An RFIC centralized 2.5GHz output phase locked loop (PLL).

The 2.5 GHz reference is distributed on-chip to four groups (quadrants) of four independently controlled RF chains (Fig. 3.28). Each of the four chains within a quadrant employs a second clock multiplier unit (CMU) to synthesize an output signal around 10 GHz. The CMUs also operate as programmable phase shifters by introducing a digitally controlled current offset to the multiplier charge-pumps, as shown in Figs. 3.26 and 3.27. The introduction of a phase shift through the CMU is simple and efficient. However, it requires a stabilization of the feedback loop and might be too slow for certain applications. Thus, the CMUs are followed by fast vector modulators as shown in Fig. 3.28, which can be programmed and pre-loaded at high speed.

Each chain is completed by a power generation unit, shown in Fig. 3.29 (16 in total).

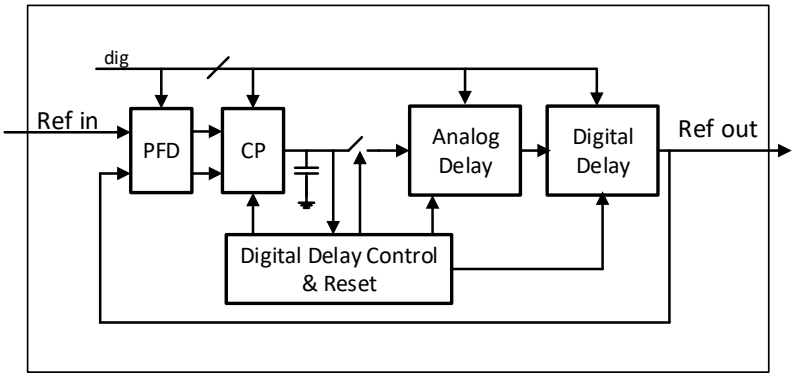


Figure 3.25: An RFIC delay-locked loop (DLL).

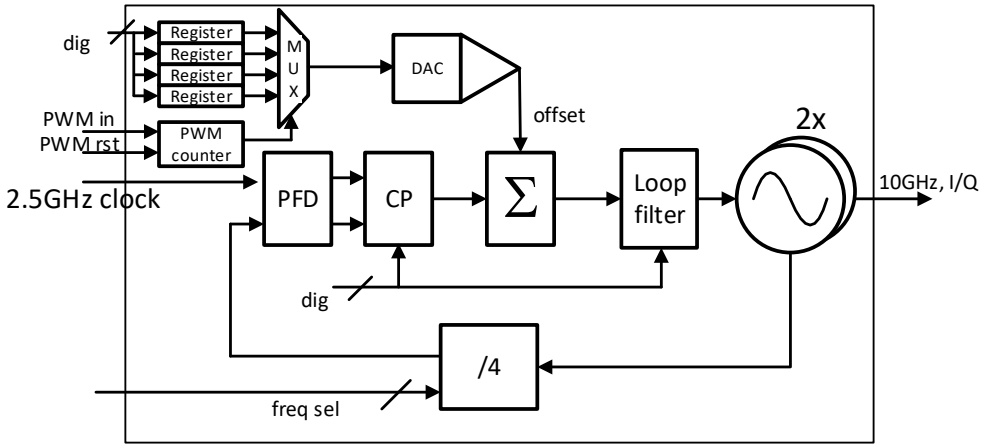


Figure 3.26: Second ×4, 2.5 GHz to 10 GHz clock-multiplier unit (CMU).

Each RF chain PA can be operated and controlled independently, however, within each quadrant they are stacked from a DC perspective as illustrated in Figure 3.30. This allows for reuse of the current that is shared by the four cores, to bias the PAs at almost four times higher voltage and significantly reduce IR drops on the supply lines. Several versions of the RFIC were fabricated and in the latest version only two PAs were stacked on top of each other to improve channel-to-channel isolation and circuit stability, as shown in Fig. 3.31. A control algorithm is used to monitor and adjust the operating voltages of the amplifiers dynamically [73]. The final stage of each amplifier, where most of the DC-to-RF power conversion occurs is realized using a differential-cascode topology to guarantee reliability under load mismatch. The fabricated RFIC along with the physical locations of its blocks is shown in Fig. 3.32

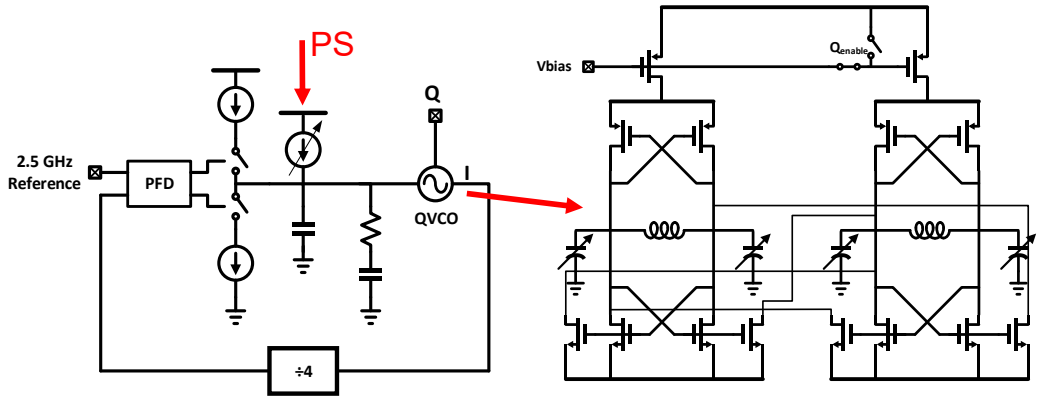


Figure 3.27: CMU phase shift mechanism (Fig. courtesy of Dr. B. Abiri).

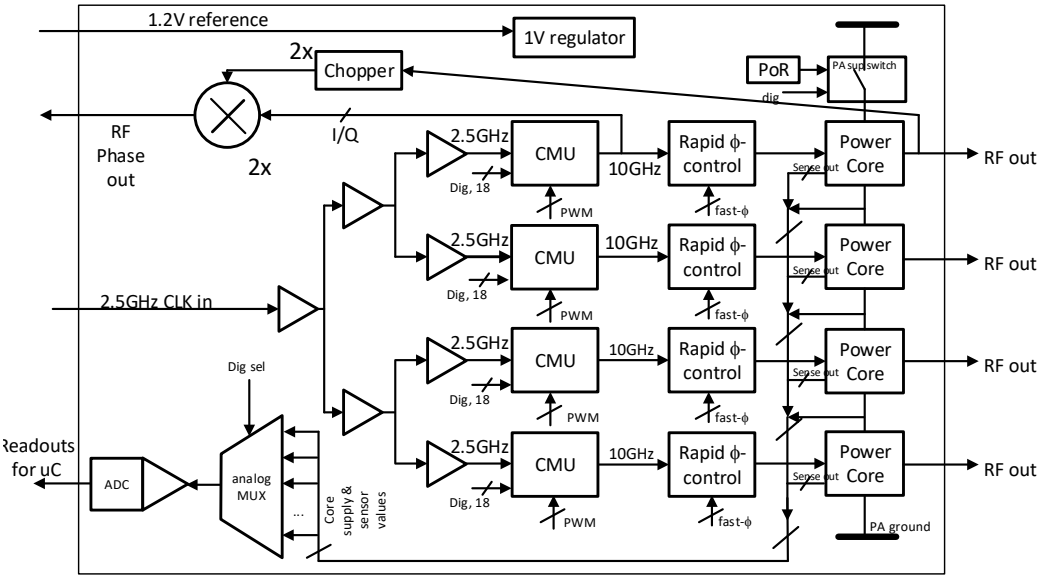


Figure 3.28: Block diagram of the power generation quadrature.

This approach enables very large and highly scalable arrays, using a large number of silicon RFICs. The small component-count, predictable repeatability of manufactured parts, and feature-rich functionality make it economically attractive for a wide range of commercial applications.

An interesting implication of this architecture is that there are broad delay variations in between various daughter cards due to low-frequency reference distribution length variations, as well as different transmission line lengths leading to the individual antennas, as shown in Fig. 3.33. The delay results from manufacturing variation, routing constraints, and board-level RF interference, and manifests as an absolute phase shift between radiating elements. Furthermore, as is the case with other

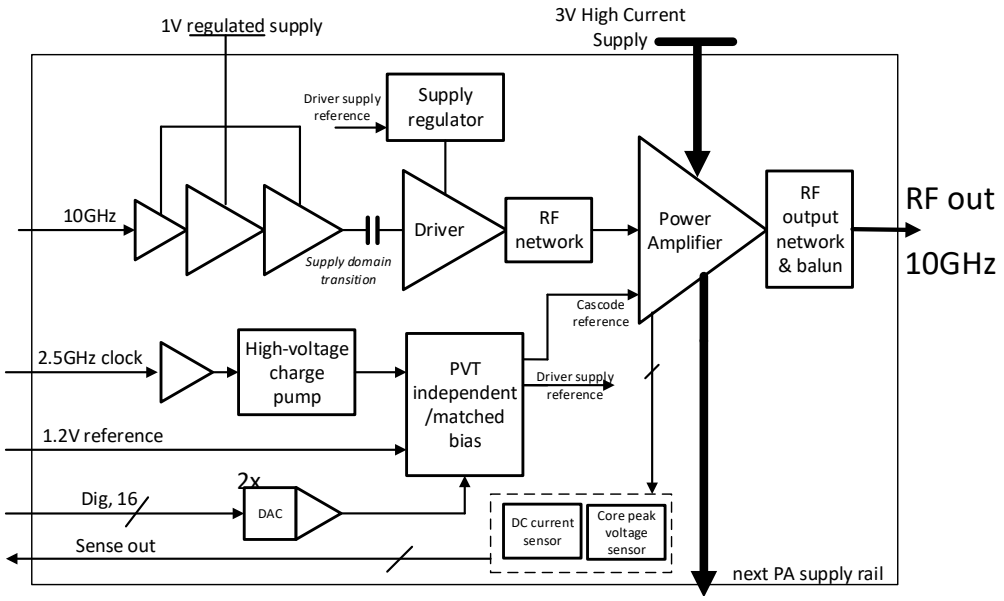


Figure 3.29: Power amplifier block diagram.

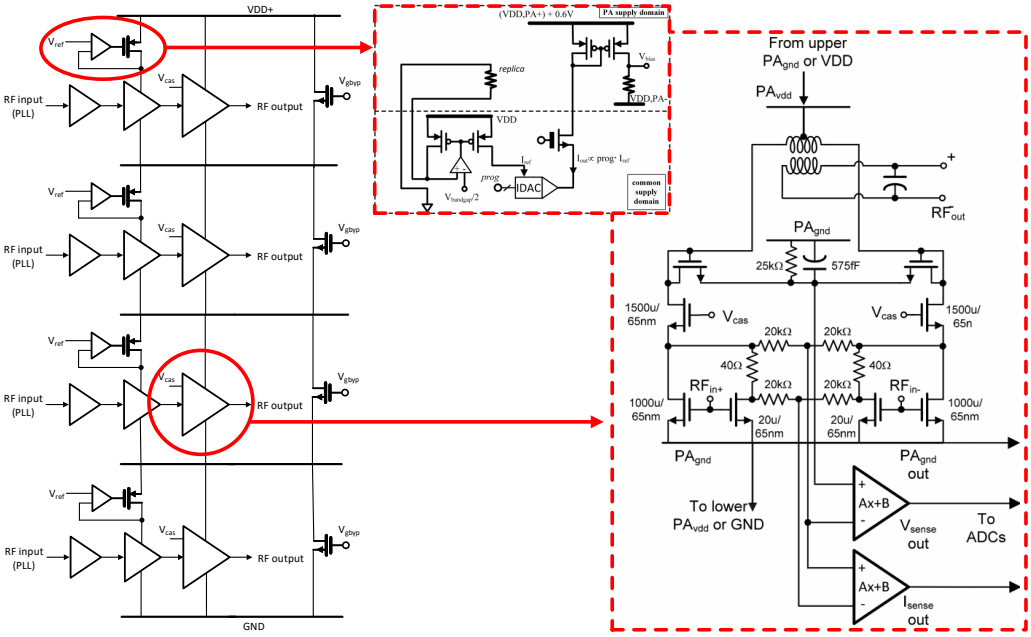


Figure 3.30: Block diagram of four PAs stacked on top of each other from DC perspective [73].

reference distribution techniques, this is also prone to temperature and environmental variations. For example, at 10 GHz, where a typical on-board electrical length is

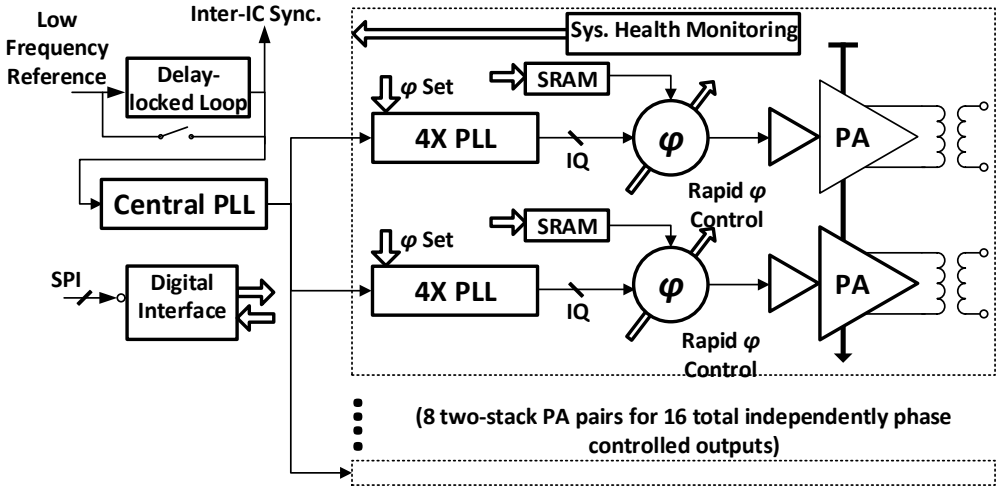


Figure 3.31: Block diagram of an RFIC with two output PAs stacked from a DC perspective [74].

1.5cm, routing differences of 1mm translate into a phase mismatch of more than $\lambda/8$. In a large array, the phase differences between outputs are practically random necessitating a focusing approach that is oblivious to them. A general approach to the focusing of large scale phased arrays will be briefly discussed in the following sections.

On-chip reference-signal synthesis

Using a custom IC to manage the tile's control and communication functions opens a range of possibilities, as well as imposes several challenges when scaling the system size to a larger number of synchronized tiles. Fig. 3.34 shows the conceptual reference and communication bus interconnect between the SSP array tiles. In this scalable array architecture, a single low-frequency reference clock is distributed to the tiles, where the high-frequency signals are synthesized using an integrated PLL and used for the coherent RF signal generation. The reference synchronization is in fact what allows the array tiles to work in concert, as illustrated in Fig. 3.35.

One major challenge with this architecture is maintaining the timing accuracy of the reference signal in the distribution process. A central star or H-tree distribution is impractical in the case of a large scale array as the number of traces and the electrical load of all the driven elements become prohibitively large. On the other hand, sequential buffering of the reference suffers from large accumulated timing

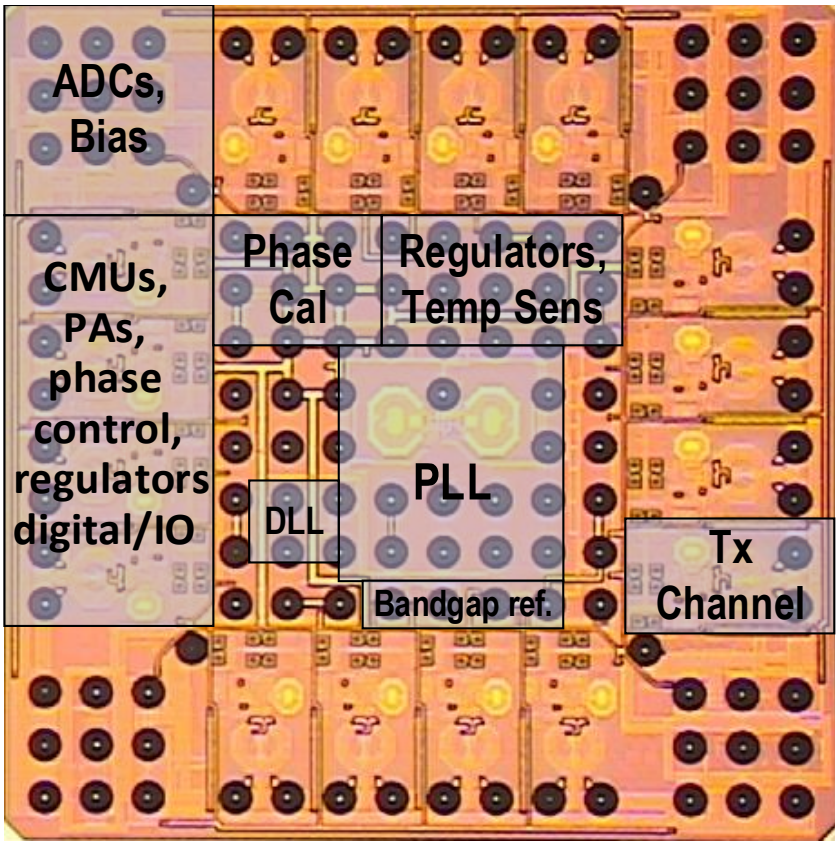


Figure 3.32: Die photo of the phased array transmitter RFIC.

deviations due to variations in the supply, temperature, and the driven load. While the latter is difficult to predict, and is dependent on the conditions of operation, an upper bound for the accumulated timing deviation can be estimated. A simplified physical structure of an inter-tile reference distribution scheme is shown in Fig. 3.36. Assuming that the noise sources of subsequent stages of reference distribution blocks (either on chip or discrete power splitters) are independent, the total noise of a square array with K distribution stages is

$$n_{total} = \sqrt{\frac{1}{4N^2}\sum_{k=1}^{K} 4n \cdot \left[(n_{stage}\sqrt{k})^2 + (n_{stage}\sqrt{2K+1-k})^2\right]}. \tag{3.22}$$

Summing the series gives

$$n_{total} = n_{stage}\sqrt{\frac{(K+1)(2K+1)}{2K}} \approx n_{stage}\sqrt{K+1}. \tag{3.23}$$

This is an upper bound because, in fact, the steering angle of a phased array is dependent on *phase difference* between elements. Therefore, there are correlated noise

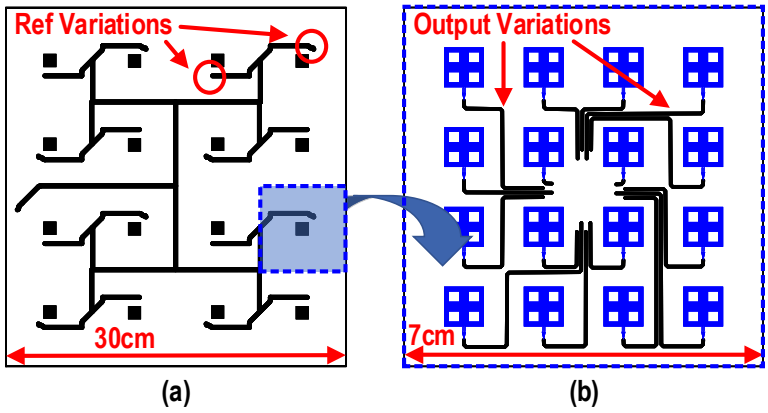


Figure 3.33: Length variations due to (a) reference distribution routing and (b) output antenna traces.

components within the clock distribution paths. The correlation can be significant; an extreme example is a single clock source driving multiple ICs. If the ICs do not add noise of their own, the clock source noise will not translate to any phase error at all. Finding how tight this upper bound is is an interesting and valuable future research problem.

It can be shown [75] that for large arrays ($K \rightarrow \infty$), the theoretical loss of efficiency Φ, due to uniformly, independently distributed random phase errors with a range of δ_{max}, is

$$\Phi(\delta_{max}) = \frac{\sin \delta_{max}}{\delta_{max}}. \tag{3.24}$$

If the phase error is normally distributed, as is in the case of clock phase noise, then

$$\delta_{max} = \sqrt{3} \cdot \sigma. \tag{3.25}$$

Fig. 3.37 shows a plot of (3.26) in percents versus the rms phase noise of an infinite array. By using (3.23) and (3.24), we can estimate the design specifications for a single tile reference distribution noise performance: a maximum of 5% efficiency loss is ≈13 degrees of rms phase noise. At 10GHz, the signal period is 100 ps so the phase error is 3.6 ps. For a 1000 stages of clock distribution then, this requires an integrated phase noise of ≈ 110 fs for each distribution stage.

Another important performance metric is the phase that the on-chip synthesizer adds to the outputs. Assuming that the synthesizers on different chips are independent

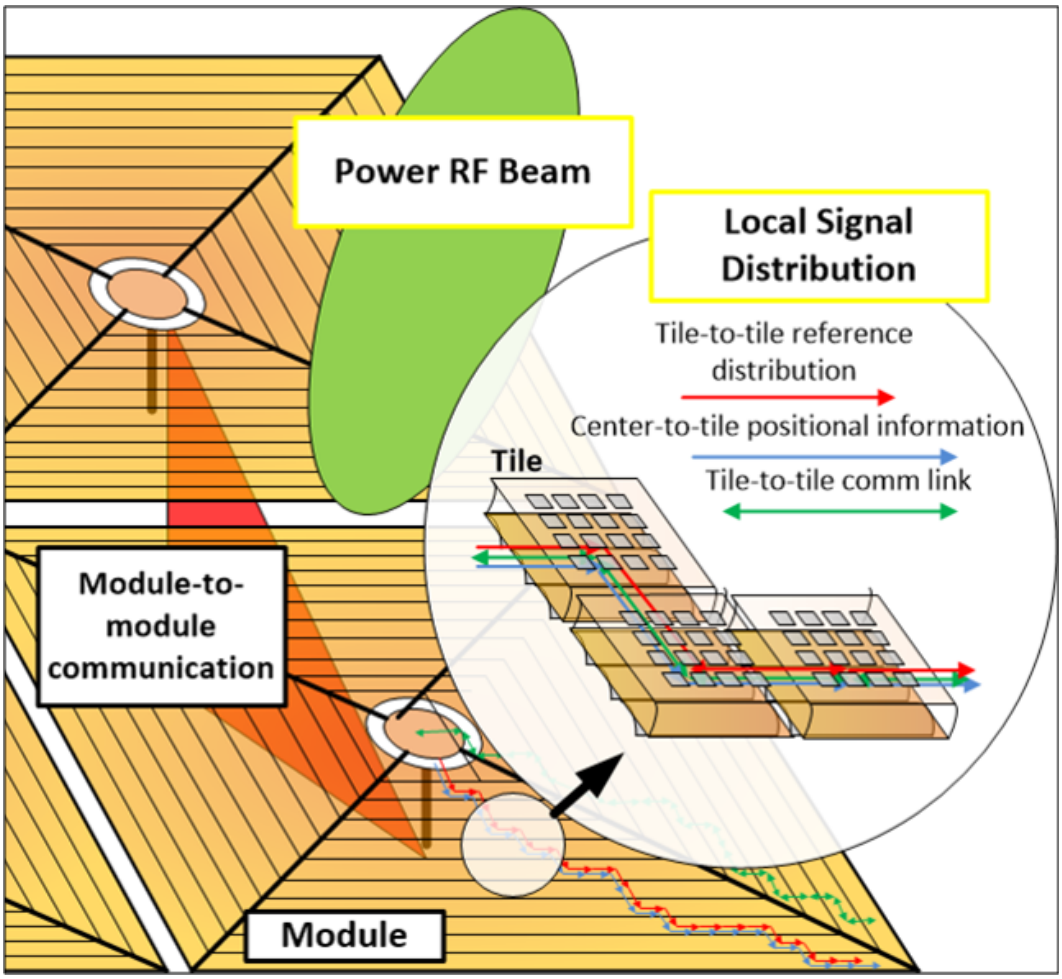


Figure 3.34: Conceptual inter-tile communication and reference distribution (Fig. courtesy of Dr. F. Bohn).

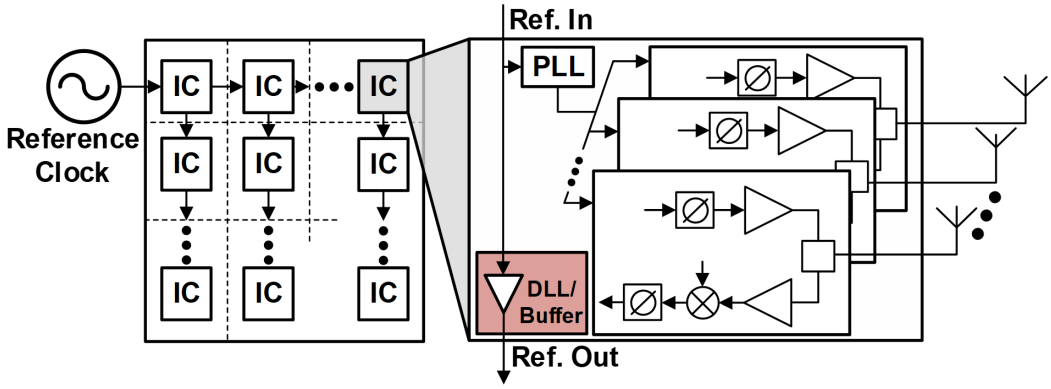


Figure 3.35: Clock distribution to CMOS-driven phased array.

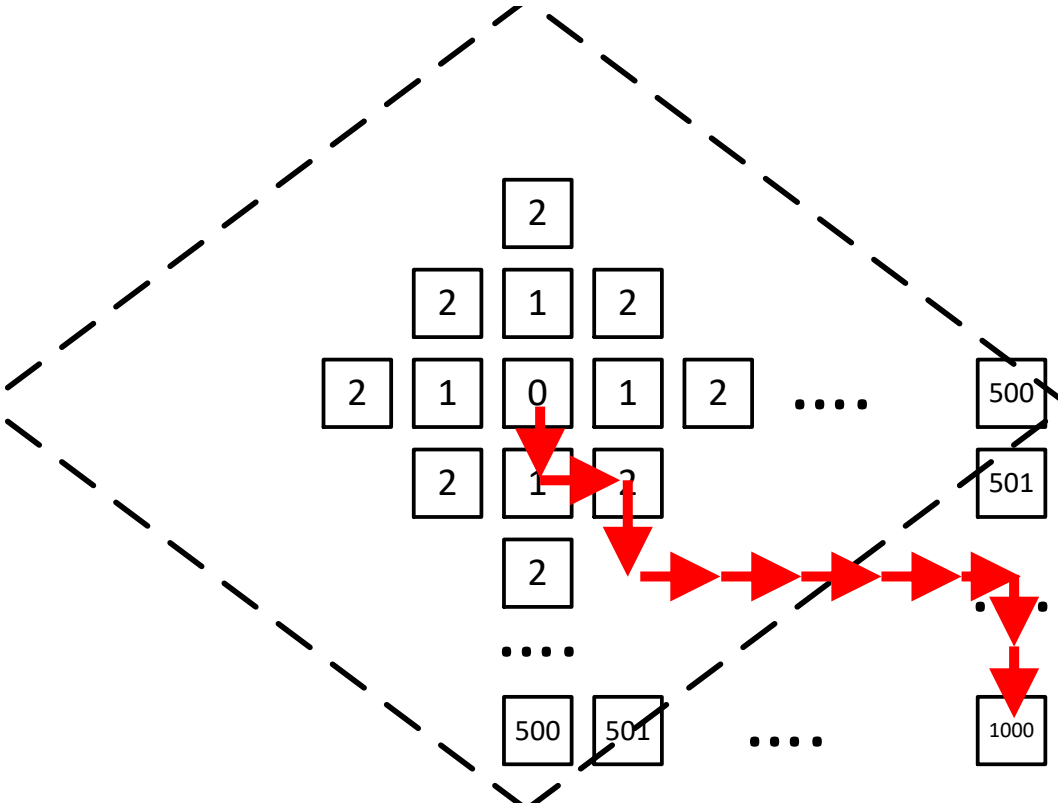


Figure 3.36: On-chip reference generation and distribution (daisy chain option) (Fig. courtesy of Dr. F. Bohn).

from each other, the total phase noise added to the array is

$$n_{tot,chip} = n_{tot,chip}\sqrt{K}. \tag{3.26}$$

For example, for a chip with integrated phase noise of 500 fs only as many as $K = 7.2^2 \approx 50$ chips may be used before the efficiency hit due to phase errors reaches 5%. This is *significantly* more restrictive than the requirement for the clock distribution scheme.

Hybrid DLL

Environmental variations, on the other hand can be mitigated utilizing a delay-locked loop (DLL) in the repeater buffer. While fundamentally sound, this approach presents new challenges since the low reference frequency, usually a few tens of MHz, necessitates a relatively large delay which can lead to unacceptable timing jitter. The SSP RFIC therefore uses a hybrid DLL architecture that utilizes several noise reduction techniques as well as a novel semi-digital loop control scheme with a single phase detection path. Moreover, the co-design of the DLL with the

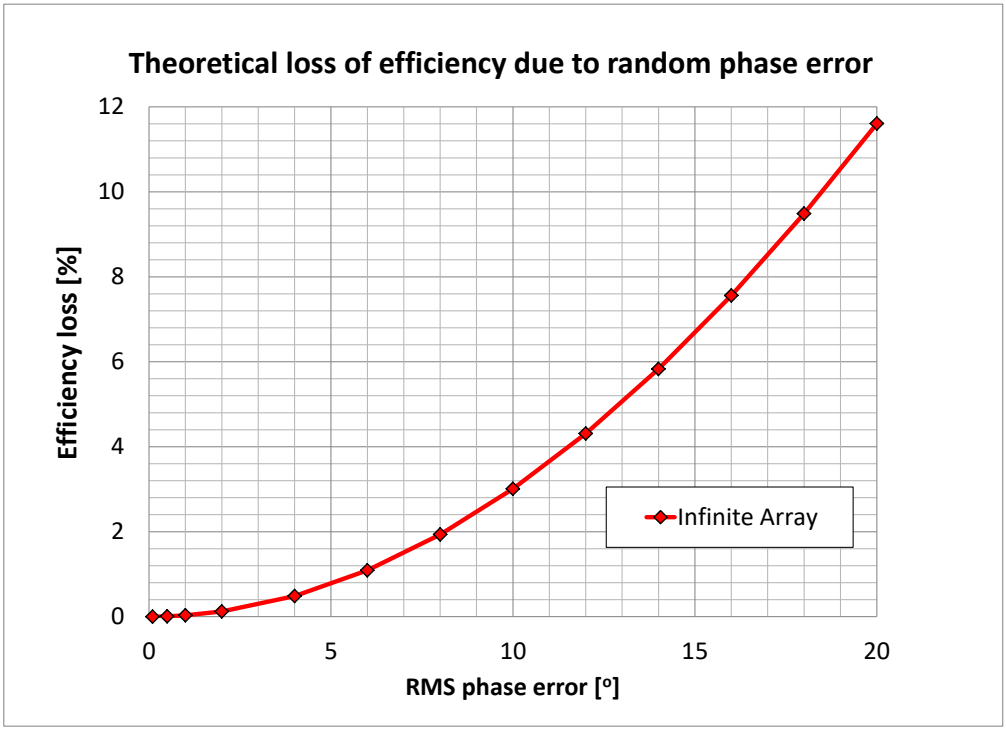


Figure 3.37: Phased array loss of efficiency due to the array's phase noise (infinite array approximation) (Fig. courtesy of Dr. F. Bohn).

subsequent PLL-based synthesizer is exploited to further reduce the overall timing jitter by proper alignment of the two phase noise transfer functions; one loop provides rejection over the frequencies where the other has a large noise contribution. This approach opens the design space, leading to superior overall performance. In a DLL, the output signal must practically be delayed by at least half a clock period compared to the reference in order to correct both negative and positive timing errors. A standard implementation does so with a single continuous delay line, which is usually the main noise contributor due to the large delay range it needs to cover.

A hybrid DLL can solve this problem by using two different sets of delay elements, as shown in Fig. 3.38a,b. A digitally controlled delay line (DCDL) composed of low-noise fixed-delay elements is used for coarse delay tuning, while a short, continuously variable delay line (VDL) is used to fine tune within the digital segments. In order to achieve delay lock, we use an analog DLL architecture and continuously monitor its charge pump (CP) output control voltage (Vc) to adjust the required DCDL value. Initially, the up/down counter of Fig. 3.39b is set to fix the DCDL state, and the DLL loop of Fig. 3.38 continuously controls the VDL. If an unattain-

able VDL tuning value is required, the control voltage Vc will rail, crossing some lower or upper thresholds along the way. This activates the overflow detector of Fig. 3.39a to pause the continuous control loop, initiate a single increase/decrease of a DCDL cell, and restart VDL tracking. Unlike [76], we are not changing the continuous delay range by flipping a state machine to set discrete phase states, but are instead adding or removing a fixed amount of low noise delay as required. This significantly improves the noise performance. In addition, we are tracking the same edge in a monotonous, continuous, and overlapping manner—which, when combined with the fact that the DLL is a first-order control loop, guarantees its stability. The reset circuitry in Fig. 3.39c is crucial to temporarily disable the phase detector and force Vc to mid-supply when a DCDL shift occurs and is synchronized such that the phase detector starts at a consistent state once the VDL tracking restarts. The noise-optimized, pseudo-differential delay elements of Fig. 3.40 also allow tracking of the falling edge of the output clock, which effectively reduces the minimum delay required by T/2 and enables usage of the same delay line at lower reference frequencies. This architecture offers enhanced robustness because (1) it necessitates neither lock detect indication nor dual phase detection circuitry as in [77] [78], (2) the small signal gain is identical for all DCDL values, and (3) the DCDL state changes in single up/down steps. The latter indicates that subsequent VDL tracking starts from a well-defined, nearby position, unlike a digital controller with automatic delay step adjustment. Our implementation favors clock distribution applications where lock time is not a major consideration. If necessary, fast lock is achievable with an a priori estimate of the DCDL delay step values and external programming of the up/down counter state.

Integrated PLL

The hybrid DLL was co-designed with its intended load PLL. In order to minimize the DLL in-band noise, its loop filter bandwidth was optimized to be around 1MHz to sufficiently reject the delay line noise while maintaining a relatively flat noise shape around the PLL loop filter knee frequency. The PLL is the first frequency conversion stage of a building block for large-scale phased arrays and as such, was designed for optimal noise performance, given the chosen design process. The output VCO has a fixed frequency of 2.5GHz and the device size is chosen for minimum noise with the required output amplitude and power consumption. The use of both NMOS and PMOS cross-coupled pairs (Fig. 3.41) has several advantages. The startup gain is almost double because these are two parallel positive feedback blocks (negative-g_m),

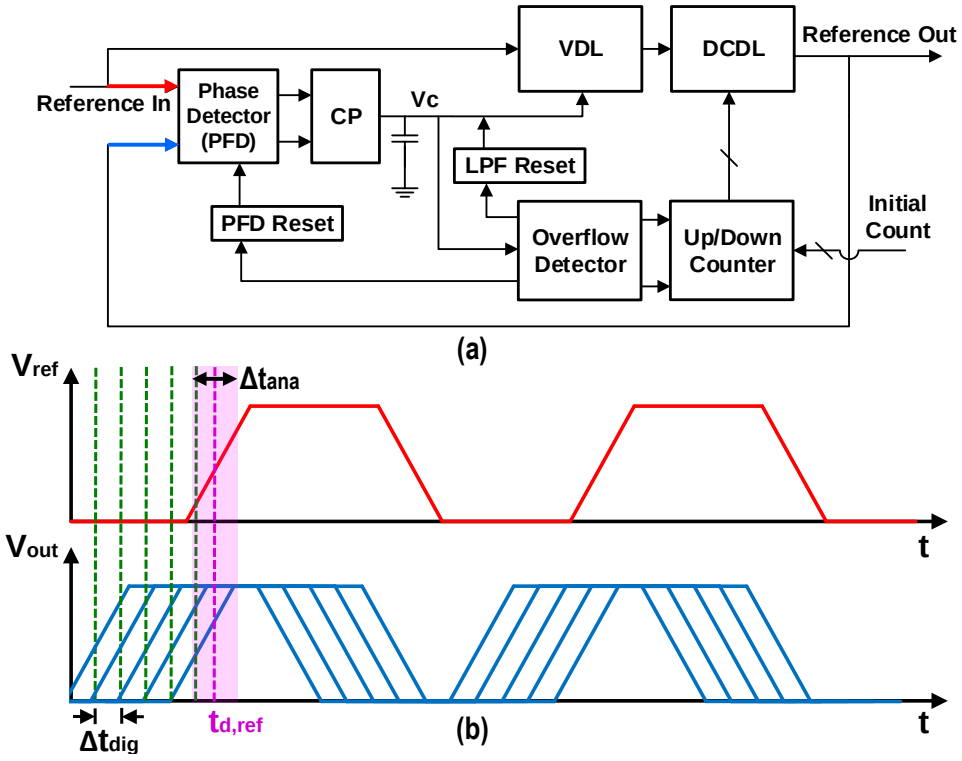


Figure 3.38: Hybrid DLL function. (a) Schematic and (b) hybrid phase tracking.

the swing is almost rail to rail, and since there is no drain inductor, the low-voltage parallel mim-capacitors are not at a risk of voltage breakdown.

The frequency divider is implemented using a standard 2/3 divider topology [79], and the phased-frequency detector is a standard D Flip-Flop state machine [80]. The loop filter and charge-pump current values are digitally variable to set the optimal bandwidth and phase margin depending on the input reference frequency. This was done by using a capacitor bank for the loop filter as illustrated in Fig 3.42. A simulation test-bench was built in Keysight-ADS to optimize the loop filter values and Table 3.8 summarizes the optimization result.

Another important noise source is the PLL reference spurs. These result from periodic variations of the VCO control voltage which exist when the PLL is locked with a net-zero charge injection per-cycle. Integer reference spurs should be minimized because they might become a significant spectral disturbance when present at the output of a large-scale transmitter array. There are two main reference spur sources for an *integer-N* PLL as detailed in Fig. 3.43.

The first source is a mismatch between the charge-pump "up" and "down" current

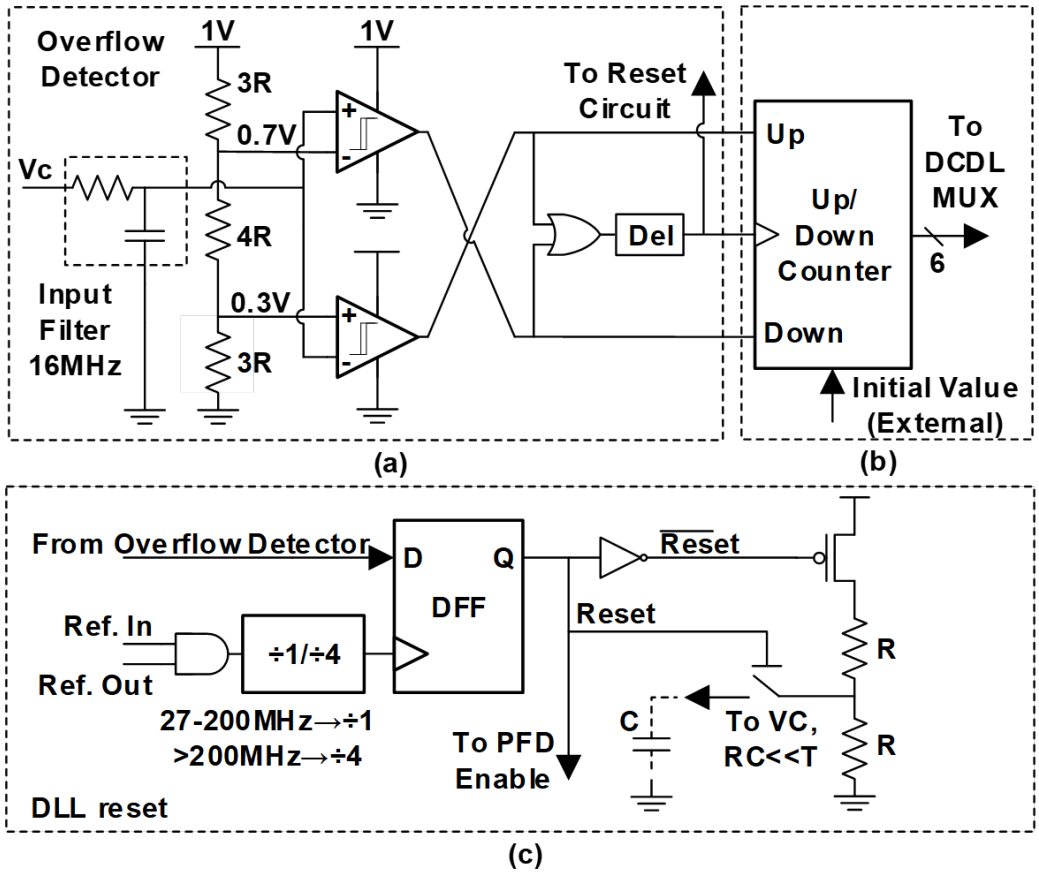


Figure 3.39: Circuit description of the (a) overflow detector/actuator, (b) DCDL MUX set, and (c) reset circuits for a hybrid operation.

Table 3.8: Optimization values of variable PLL loop filter and charge-pump current

Ref. Freq. [MHz]	I_{CP} [mA]	C_{LPF1} [pF]	C_{LPF2} [pF]	C_{LPF3} [pF]	R_{LPF1} [Ω]	R_{LPF2} [Ω]	Loop BW [MHz]	Jitter [fs]
10	0.415	25	600	11	2000	150	0.38	1000
25	0.73	24.5	600	11.2	1450	150	0.8	500
50	1.67	20	600	5.3	650	150	1.63	288
125	1.56	15	580	1	470	150	2.8	183
250	0.83	15	600	1	450	150	2.85	160

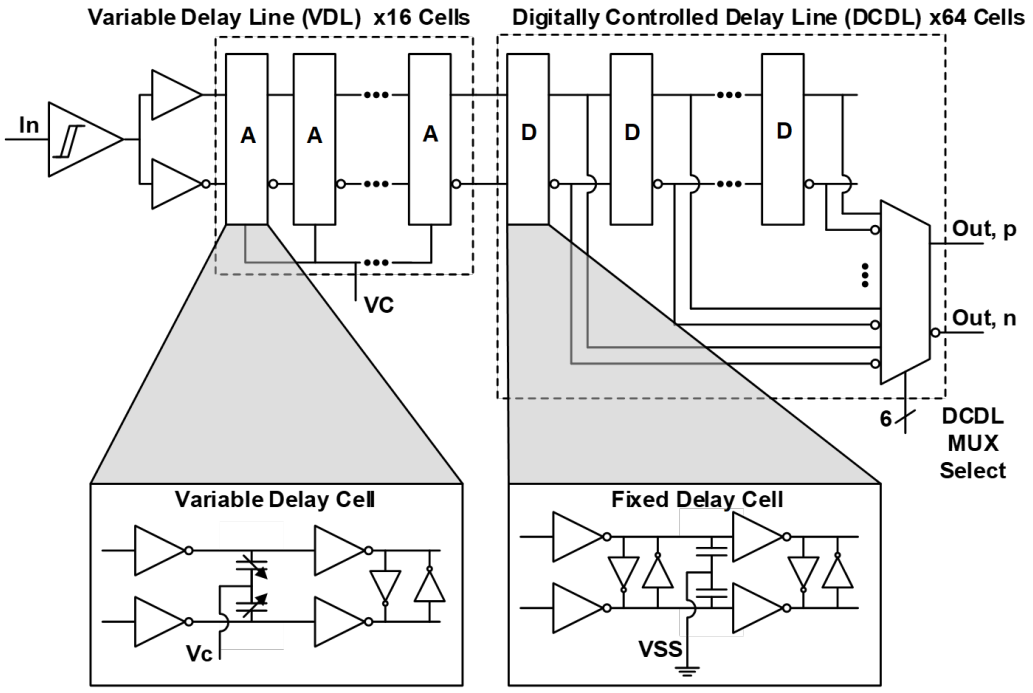


Figure 3.40: Hybrid delay line structure.

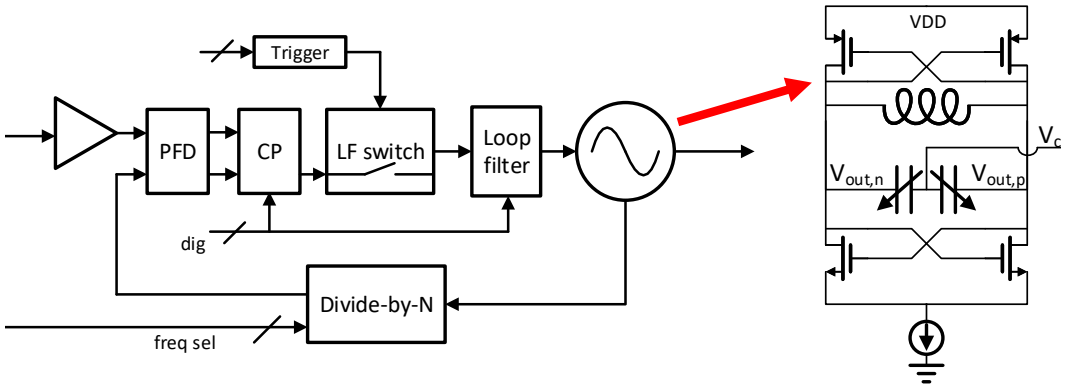


Figure 3.41: PLL VCO.

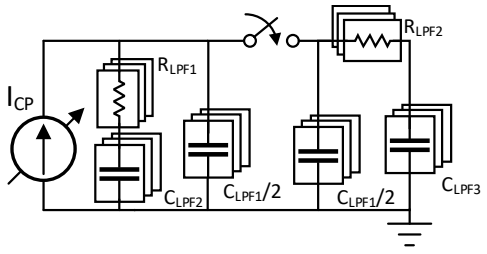


Figure 3.42: A variable loop filter for the optimization of the PLL noise performance at different frequencies.

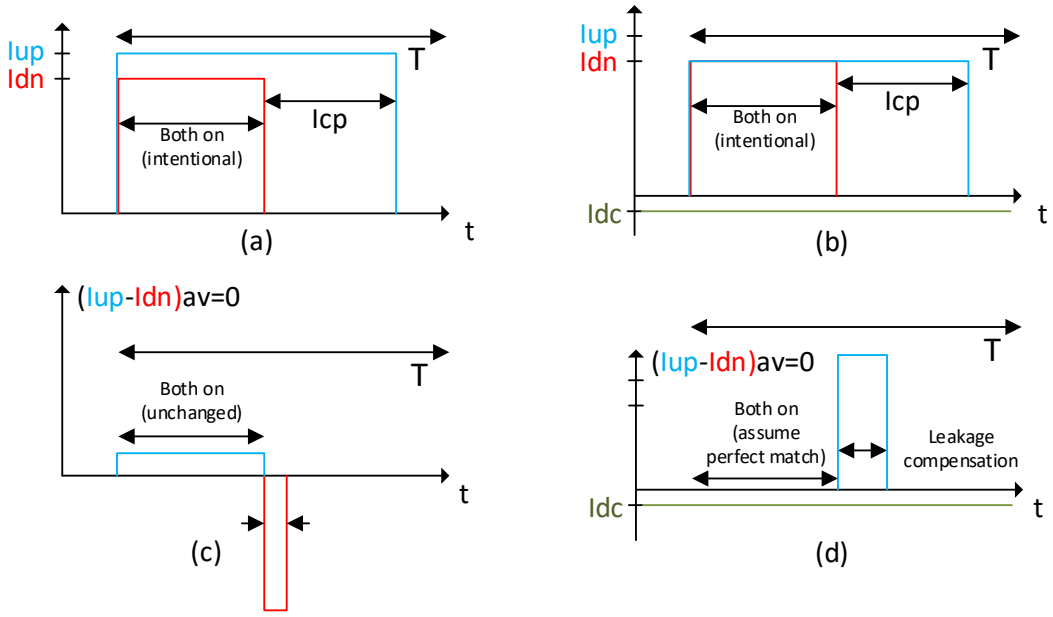


Figure 3.43: Reference spur sources: (a) Charge pump mismatch and (b) DC current leakage. Periodic charge transients on control voltage line (c) due to up/down mismatch and (d) DC leakage.

sources. This is due to the charge-pump dead-zone prevention [80] mechanism that forces "up" and "down" sources to be open simultaneously for a short period of time. The stronger current source injects excess charge which is eliminated in the steady state by the weaker source remaining open for a bit longer. The second spur source results from DC leakage of thin oxide devices due to tunneling effects. Every cycle there is a small leakage current that discharges the loop filter and VCO capacitors, and the loss of charge is prevented in the steady state by excess injection from the charge pump. The ripple that is created by both of the mentioned effects translated into output spurs. To minimize leakage-related spurs, the PLL uses mostly thick-oxide capacitors. This complicates the design and increases its size because the capacitance density is significantly smaller than that of thin oxide devices. The PLL also employs a pass-through switch to negate the effect of the charge-pump current mismatch as shown in Fig. 3.44, similarly to [81]. The switch pass-through start and end time are digitally variable to optimize the spur rejection operation.

The PLL is fabricated in a 65nm bulk CMOS process. It occupies 0.4 mm^2 of active area and consumes about 6mA from a 1V supply. Fig. 3.45 shows the PLL die photo. The PLL is characterized with a reference frequency of 50 MHz. Fig 3.46

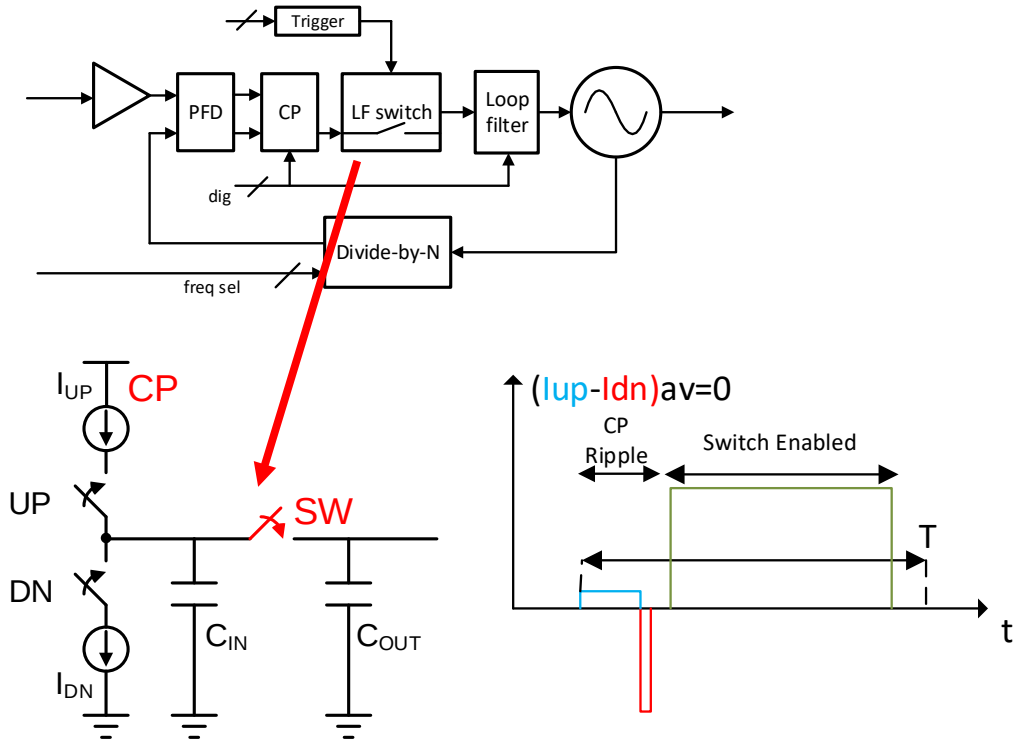


Figure 3.44: Pass-through switch structure for up/down mismatch spur prevention.

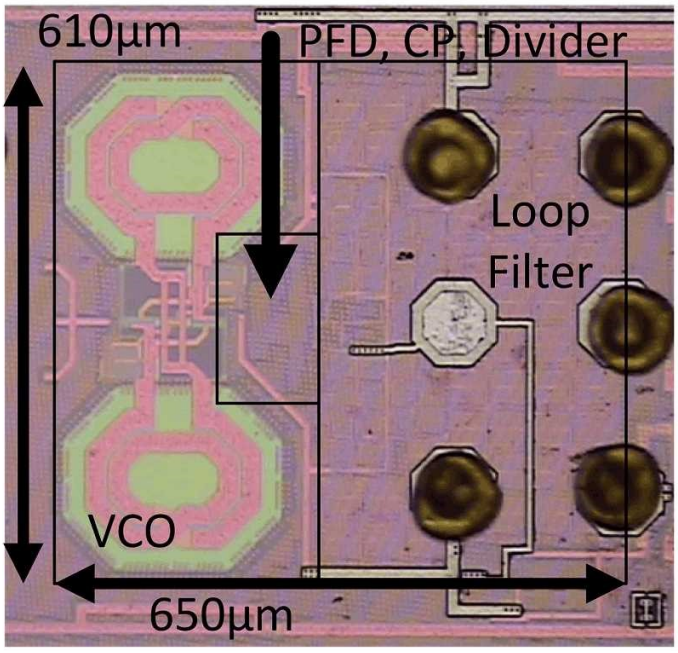
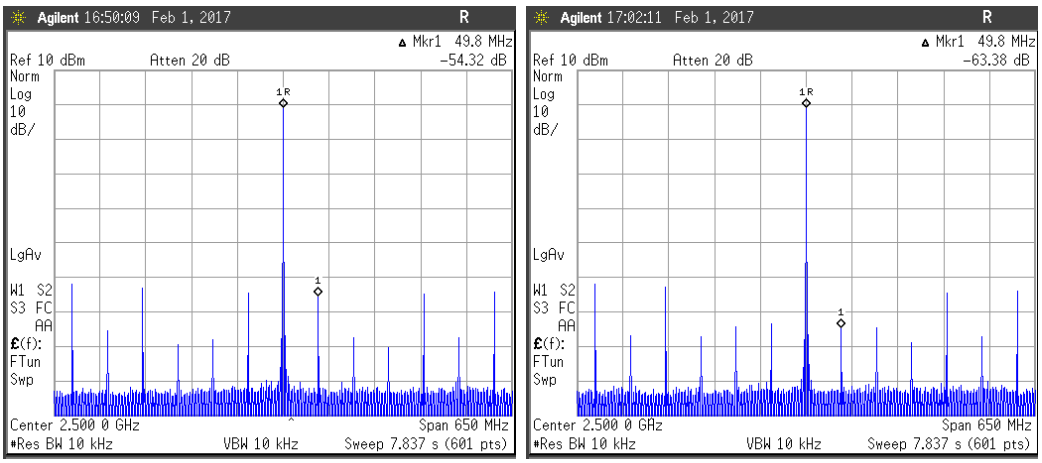


Figure 3.45: PLL die micrograph.



(a) (b)

Figure 3.46: PLL spur reduction switch measurement.

shows the PLL output spectrum and switch operation for phase-noise rejection. The switching operation lowers the output spurs by about 10 dB. Fig. 3.47 shows the harmonic rejection of reference spurs as a function of the switch start and stop times. A heat map of the output reference spur harmonics was plotted versus the digitally-variable start and stop times of the pass-through switch (Fig. 3.47). This is useful in order to understand the timing sensitivities that may change due to production variations. Such sweeps can be used in the future as a basis for digital calibration of the desired reference spur levels. The measured integrated phase noise in Fig. 3.48 is strikingly similar to the simulation. The measurement differs from the simulation in the low-frequency range due to the reference oscillator and charge-pump noise slope that were not taken into account in the simulation. The high range of the noise measurement is limited by the instrument noise floor. Both mismatches from simulation are small enough so as not to be noticeable in the integration.

Reference distribution measurements

The DLL was fabricated in a 65nm bulk CMOS process (Fig. 3.49). It occupies 0.036mm2 of active area, and its joint operation with the PLL was characterized at an output frequency of 2.5GHZ with the input reference ranging from 27MHz-270MHz. Fig. 3.50 shows the delay locking mechanism while the DLL drives either 50Ω or 10pF loads. The control voltage Vc in Fig. 3.50a overflows and resets until it reaches the necessary DCDL value, while fine-tuning persists indefinitely. The delay between the output and reference signals (Fig. 3.50b) was calculated from the

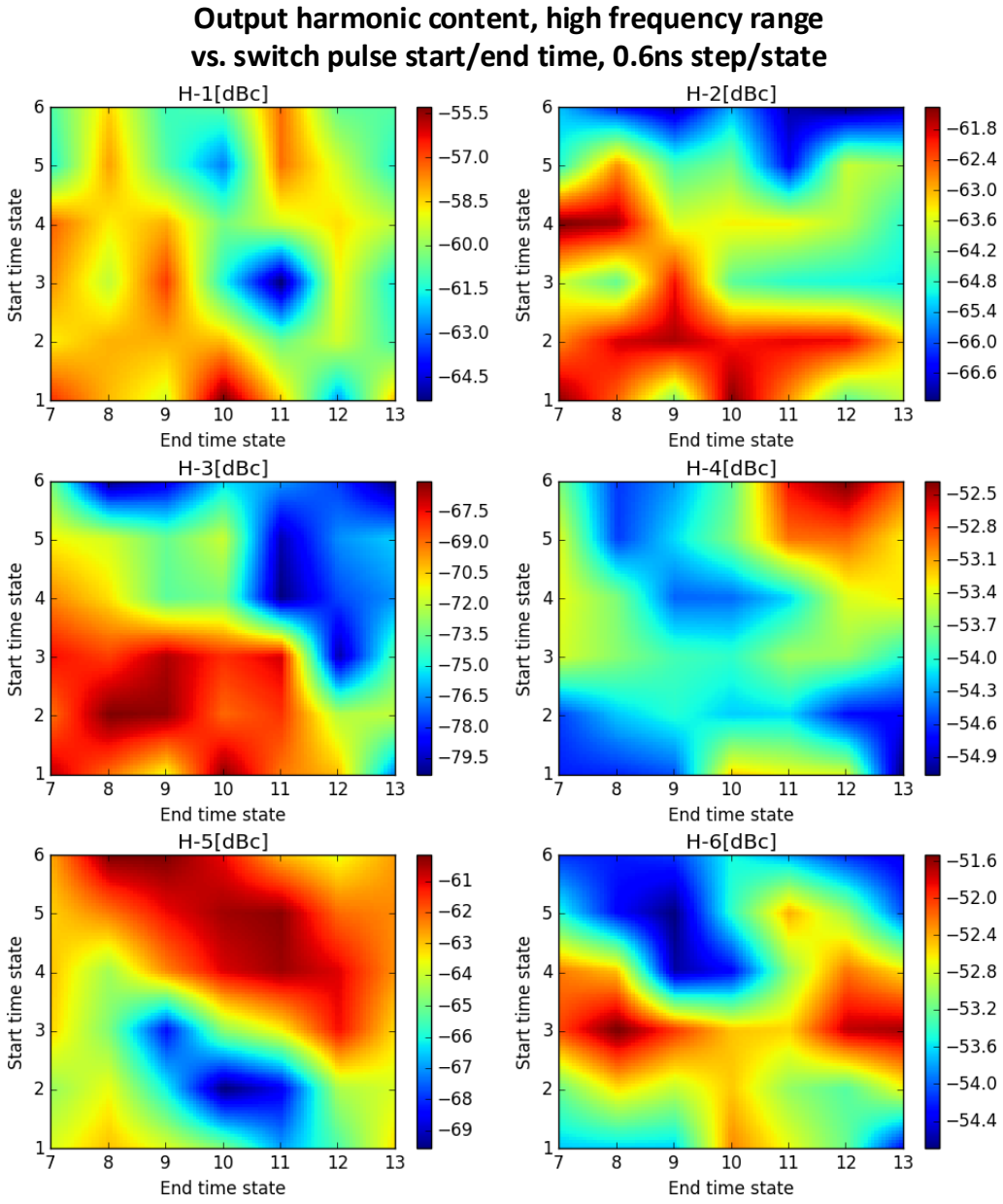


Figure 3.47: PLL reference spur levels for different digital settings of start/stop times of the pulse.

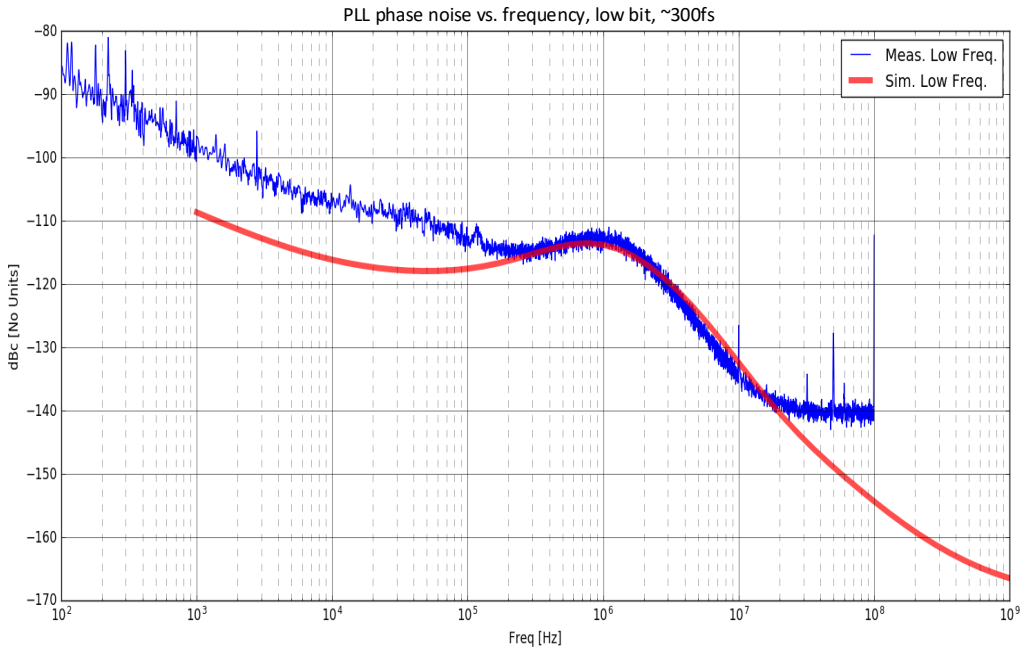


Figure 3.48: PLL phase noise PSD measurement vs. simulation

waveforms' zero-crossing points, emphasizing how proper sizing of the overlapping DCDL step size and VDL range allow for proper operation of the circuit. The SSP is intended to operate in space and phase setting variations are expected to be slow, on the order of minutes, the expected temperature fluctuation is therefore low - less than 10°C in steady state, and the measured closed-loop control voltage tracks the temperature at a rate of 2.4mV/°C. The nominal control voltages for locking are 340mV and 660 mV when counting up and down, respectively, and the overflow detector has a nominal hysteresis of 30 mV. Therefore, temperature variations are not expected to toggle the digital counter and add additional, unaccounted noise. In our clock distribution scheme, static buffer phase offset is programmatically removed when the array is calibrated and therefore not of a major concern. Fig. 3.52 shows how the DLL degrades the noise performance of a reference clock source by examining the phase noise spectral density profile of the cascaded application blocks, measured using a Keysight PXA N9030B signal analyzer (Fig. 3.51). Notably, the frequency band of interest is above 1kHz, where phase errors are presumably correctable by external phased array adjustment algorithms, and below 10MHz, far away from the load PLL loop filter knee frequency. Figs. 3.52a and 3.52b clearly show how the PLL loop filter rejects most of the DLL noise, and thus

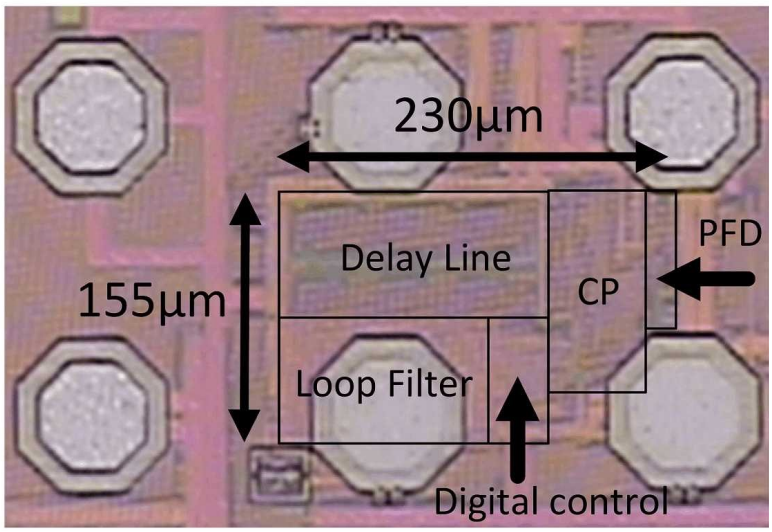


Figure 3.49: Hybrid DLL die photo.

brings it to contribute as little as 323fs rms jitter in the relevant frequency band.

These measurements were repeated at different frequencies between 27MHz and 270MHz, and a summary is shown in Fig. 3.53. The lower and upper frequency ranges are limited by the maximum DCDL delay and overflow actuation timing accuracy, respectively. Fig. 3.53b demonstrates how this DLL is advantageous in that an increase in the frequency of operation decreases the number of DCDL elements that participate in the delay chain, and thus the power consumption remains roughly constant. Fig 3.53c emphasizes how the system is optimized for 50MHz operation. At lower frequencies, the high DCDL count adds more noise to the output, while at higher frequencies the subsequent PLL loop filter has little effect on noise rejection. Because the end goal is the phased array reference distribution scheme of Fig. 3.35, noise performance was characterized for several, cascaded DLLs, as shown in Fig. 3.54, If the noise of each stage is uncorrelated with the others, the total noise measured at the output of an N DLL cascade is expected to be:

$$n_{total}^2 = n_{ref}^2 + n_{meas}^2 + N \cdot n_{DLL}^2 \tag{3.27}$$

where n_{meas} is the measuring instrument noise, n_{ref} is the reference noise, and the single device noise can be estimated from the slope of the linear fit. Fig. 3.55 shows the linear behaviour of the DLL cascade jitter variance at different frequencies and the resulting rms jitter is summarized in Table 3.9, showing good agreement with the single device measurements of Figs. 3.52b and 3.53c.

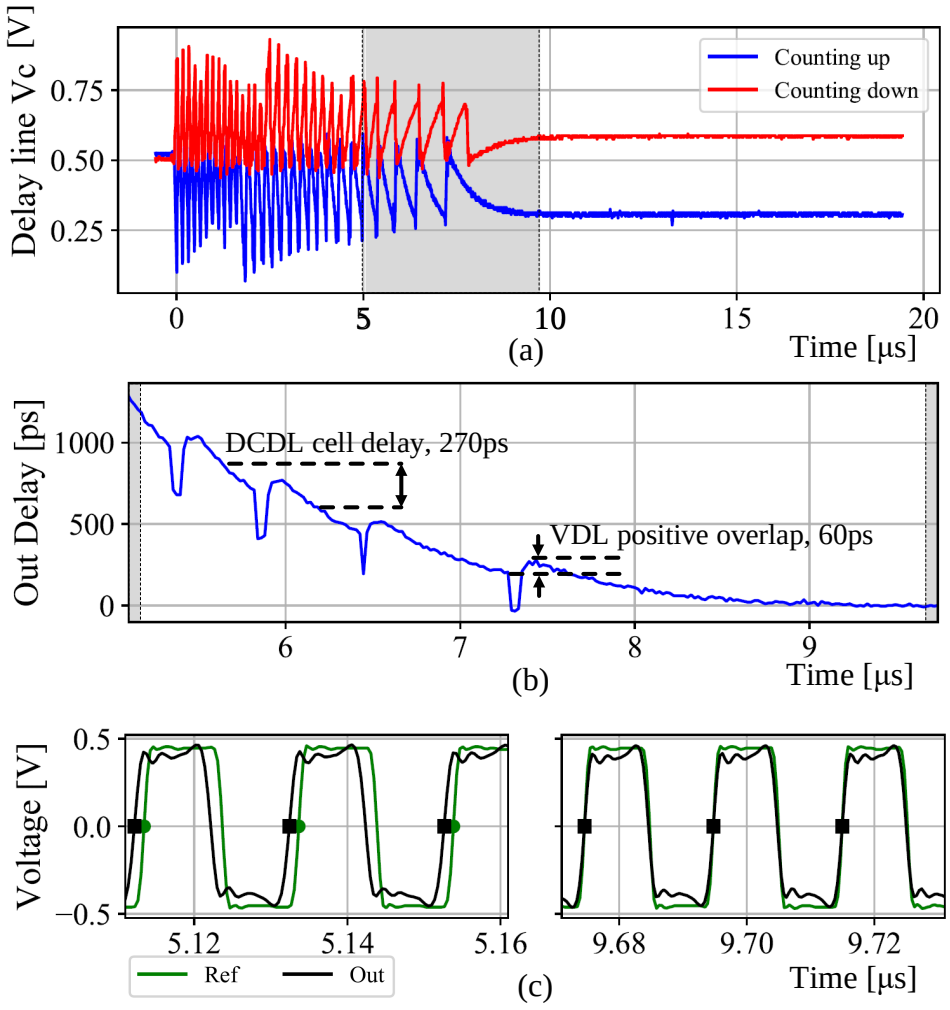


Figure 3.50: Hybrid lock process at different time scales. (a) Loop filter control voltage, (b) time delay between reference and output clocks, and (c) time domain waveforms (adjusted).

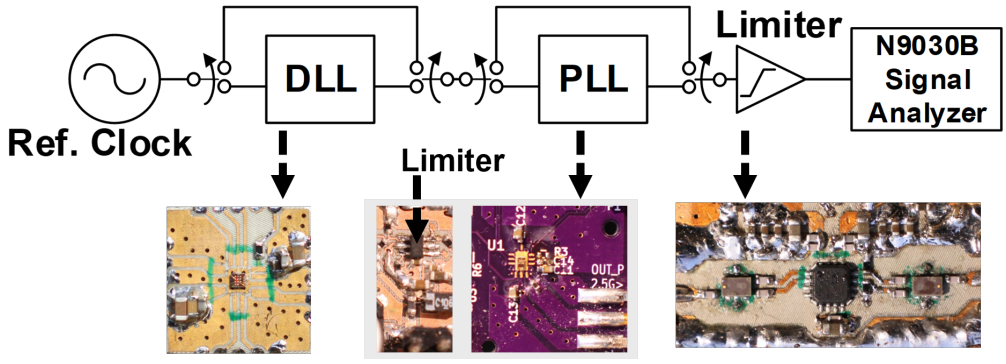


Figure 3.51: Cascaded PLL and DLL measurement setup.

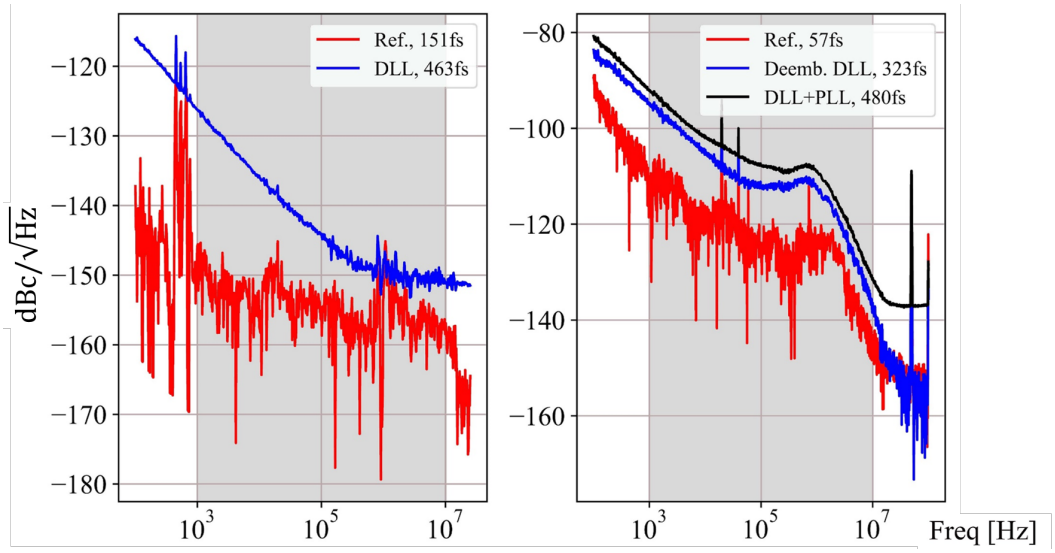


Figure 3.52: Noise performance. (a) 50MHz DLL phase noise and rms jitter, and (b) 2.5GHz post PLL phase noise and rms jitter. The red curves are the rms measurement uncertainty.

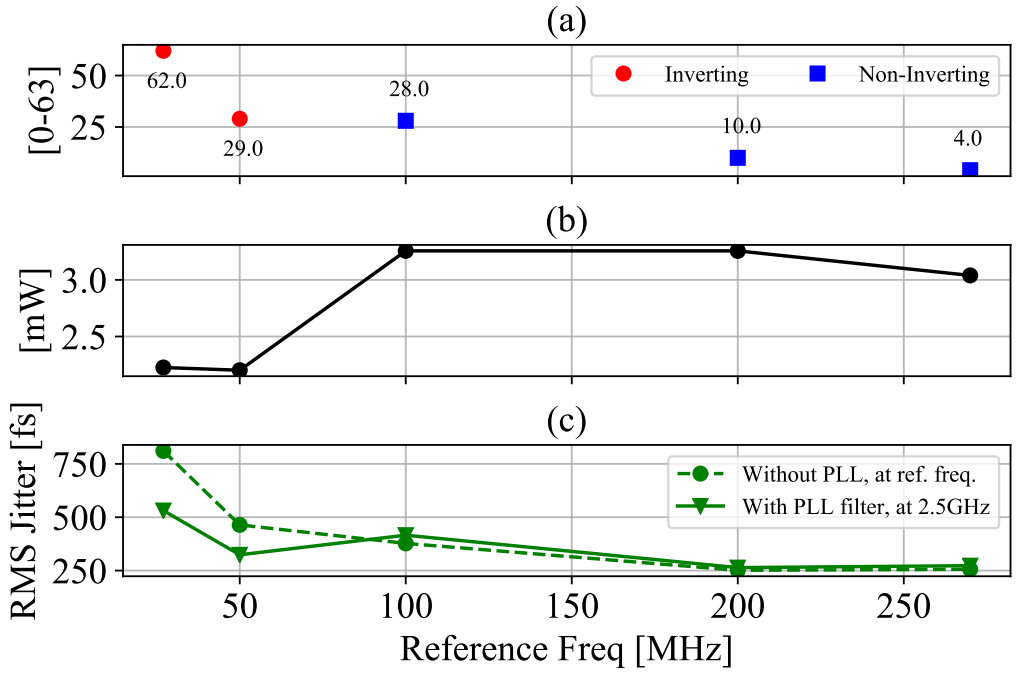


Figure 3.53: Performance vs. frequency. (a) Participating DCDL cell count, (b) power consumption of participating DLL blocks, and (c) rms jitter within the 1kHz - 10MHz band.

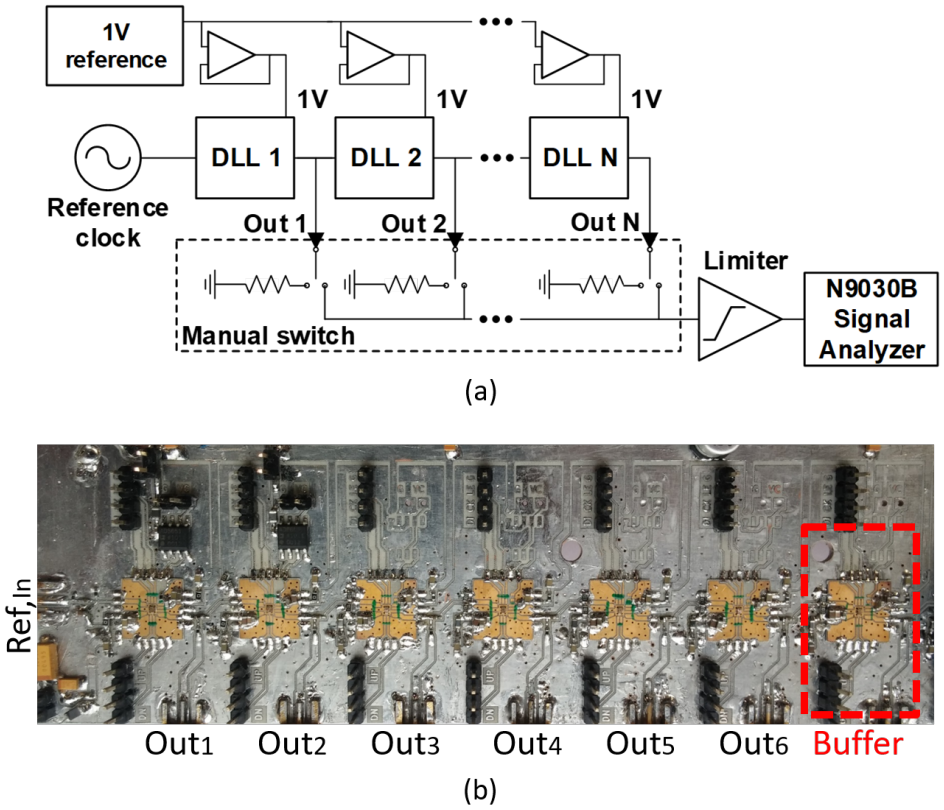


Figure 3.54: Cascaded DLL jitter (a) test setup and (b) photo.

Table 3.9: DLL noise performance, based on Fig. 3.55.

Reference Frequency [MHz]	**27**	**50**	**100**	**200**	**270**
RMS Jitter, 1kHz-10MHz [fs]	733	456	402	268	261
RMS Jitter, 1kHz-f_{ref}/2 [fs]	809	685	698	481	549

Summary

The task of distributing a low noise reference to very large-scale phased arrays is challenging because it does not enjoy the shorter period times of GHz range clocks. Table 3.10 shows a performance comparison of the hybrid DLL/PLL scheme with prior state-of-the-art at similar frequency ranges, and demonstrates how combining new circuit architectures with application-aware design can result in an order-of-magnitude improvement over the state-of-the-art.

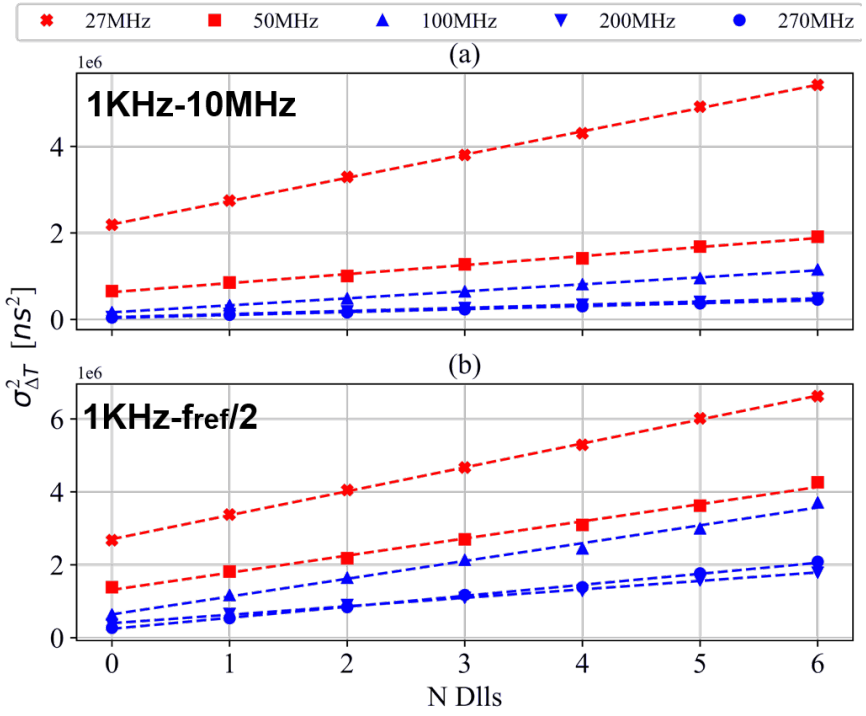


Figure 3.55: Cascaded DLL jitter. (a) 1kHz - 10MHz measurement, and (b) 1kHz-f_{ref}/2 measurement. Red and blue curves indicate locking to inverted/non-inverted output, respectively.

Chip level measurements

Additional measurements were carried out to finalize the RFIC characterization. Fig. 3.56 shows the PA output power and CMU phase shift range, covering more than 360° with a constant amplitude. Fig. 3.57 shows the chip phase noise PSD and integrated phase noise, both of which within the required specifications.

3.5 Tile-Level Integration and SSPP Demo

The self-contained RFIC is the centerpiece of a unit building block tile for the modular system. Each tile incorporates 16 single polarized radiators in a 4×4-grid, where each RFIC output drives a radiator (3.58). The system size can rapidly scale by repeating the tile pattern on a large flexible laminate (Fig. 3.59). The element spacing is 18mm ($0.6\,\lambda$), and the total tile size is 7 cm $\times$ 7 cm. Even though the RFIC could be assembled directly on the flexible board, doing so will introduce significant stress to the soldered bumps which might lead to mechanical failure. In addition, it will require a very tight control of the flexible PCB metal traces, which might be costly for large sheets. For this reason, a thin rigid adapter board (interposer, Fig.

Table 3.10: DLL performance comparison table

	This work		**JSSC 05' [76]**	**TCASII 07' [78]**	**TCASII 09' [82]**	**CICC 13' [83]**
Frequency range	**27-270MHz**		0.25-2GHz	32-320MHz	0.02-3GHz	80-450MHz
Comparison frequency	**50MHz**	**270MHz**	250MHz	200MHz	50MHz	180MHz
RMS jitter [ps]	**0.685**	**0.55**	5.25	4.44	7 (approx.)	2.3
In band RMS jitter	**0.33ps**	**0.26ps**	NA	NA	NA	NA
Power consumption [mW]	**2.25**	**3**	1.2	15 (320MHz)	0.4-3.6	26
Supply voltage [V]	**1**		1.8	2.5	1	1.5
Technology process [CMOS]	**65nm**		180nm	250nm	90nm	130nm
Die area [mm^2]	**0.036**		0.046	0.07	0.005	0.08

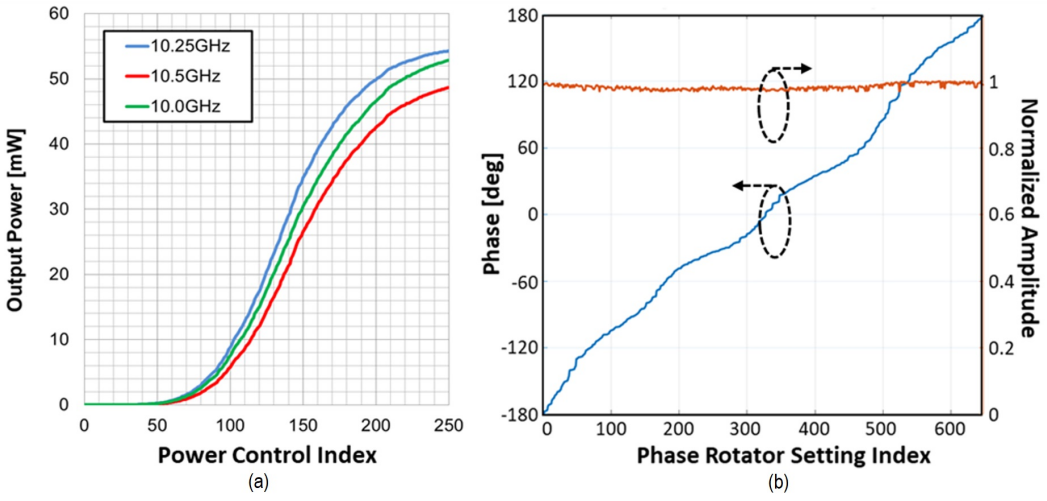


Figure 3.56: RFIC output: (a) power and (b) phase shift range [84].

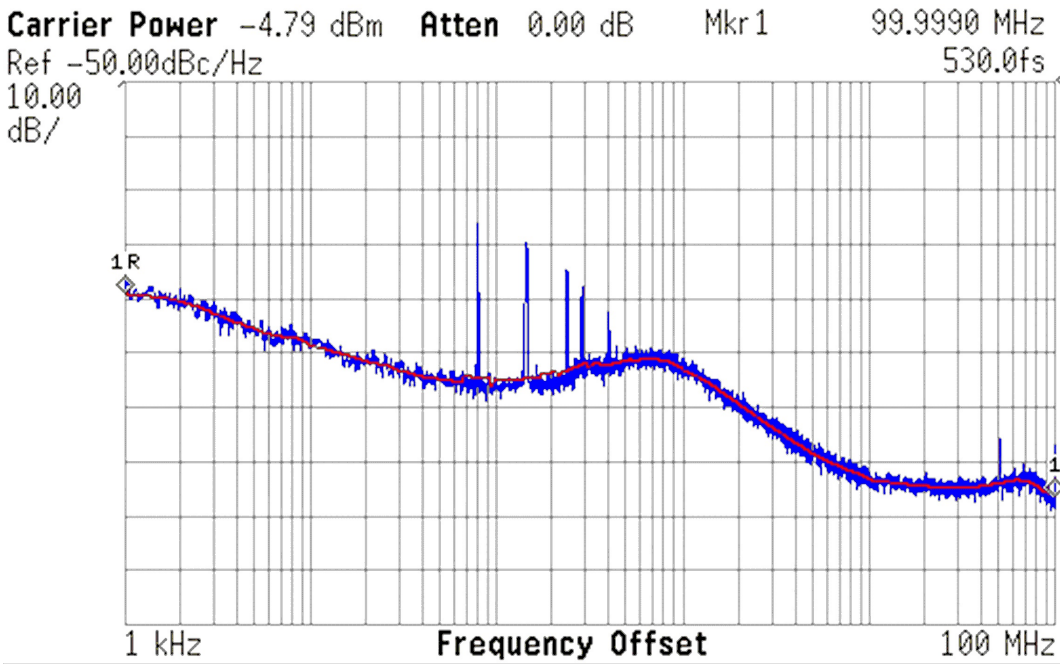


Figure 3.57: RFIC single channel output phase-noise PSD (Fig. courtesy of Dr. F. Bohn).

3.60) is used to mount the integrated circuit on the flexible circuit board. The small interposer only slightly adds stiffness to the flexible circuit board, and is helpful in fanning out the RFIC digital control lines and in converting the radiator 50Ω transmission lines to show an optimal impedance of 75Ω to the PA outputs. The simulated and measured interposer S-parameters in Fig 3.61 agree well with each other and the good matching and inter-channel isolation assist in maintaining the PA stability. This RFIC is designed to work in space, and while it is functional without additional cooling mechanism, a heatsink is needed to reach its performance specs in a terrestrial environment.

Antenna design

The SSP array is supposed to be packed compactly before deployment. This requires the use of either very low profile or collapsible antennas, which must be lightweight as well. The challenge is that in order to function properly, an antenna needs some space from the signal ground plane. For dipole style antennas, this space should be in the order of $\lambda/4$, or 7.5 mm at 10 GHz in vacuum. Patch antennas permit thinner spacing (in the order of $\lambda/10$), but usually exhibit narrower bandwidths. Both types of antennas require a robust feed design at RF frequencies which might collide with the requirement for a lightweight structure. Practically, rigid low profile antennas

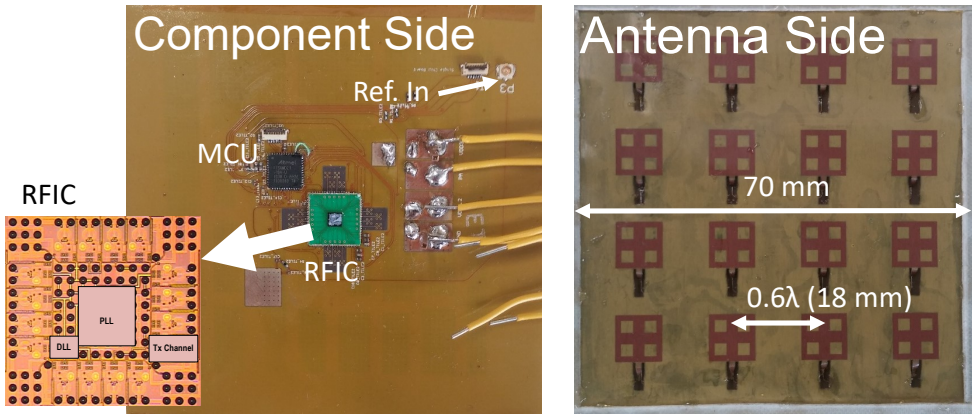


Figure 3.58: A flexible phased-array transmitter unit-cell (tile).

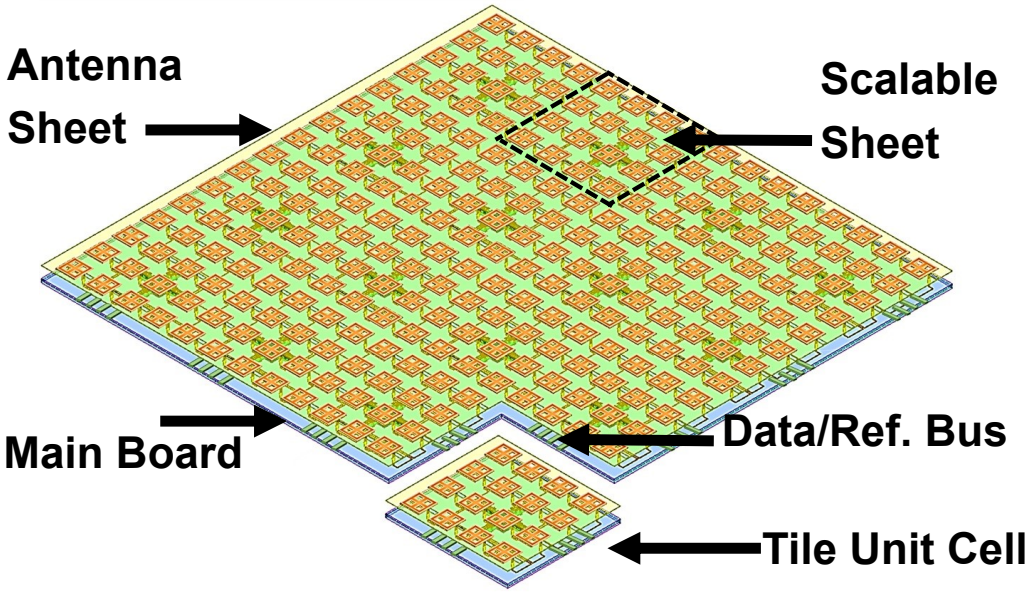


Figure 3.59: Multiple tile unit-cells combined on the same flexible laminate to form a larger array.

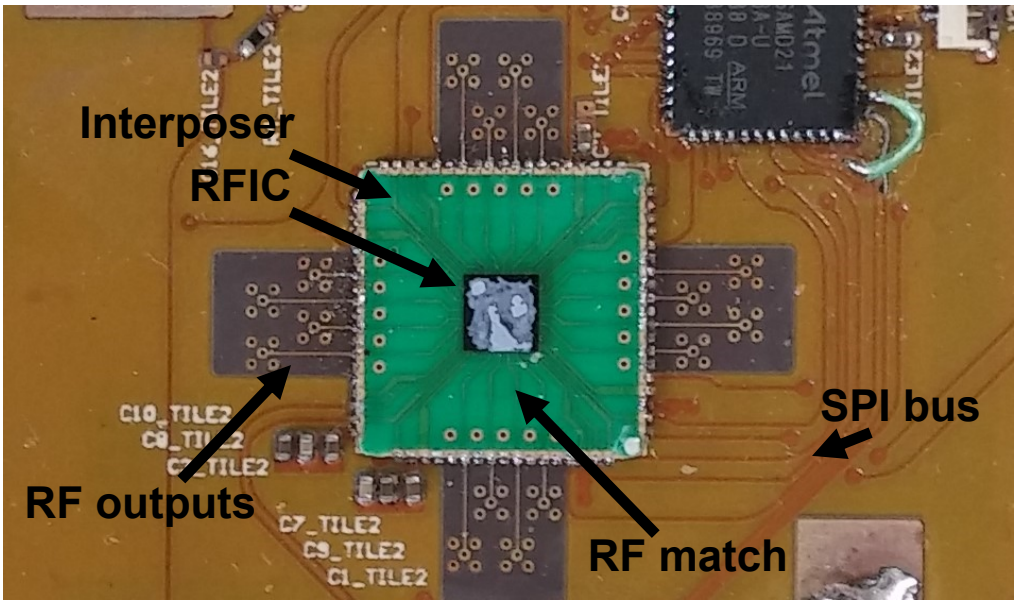


Figure 3.60: Chip-board interface with a small rigid interposer.

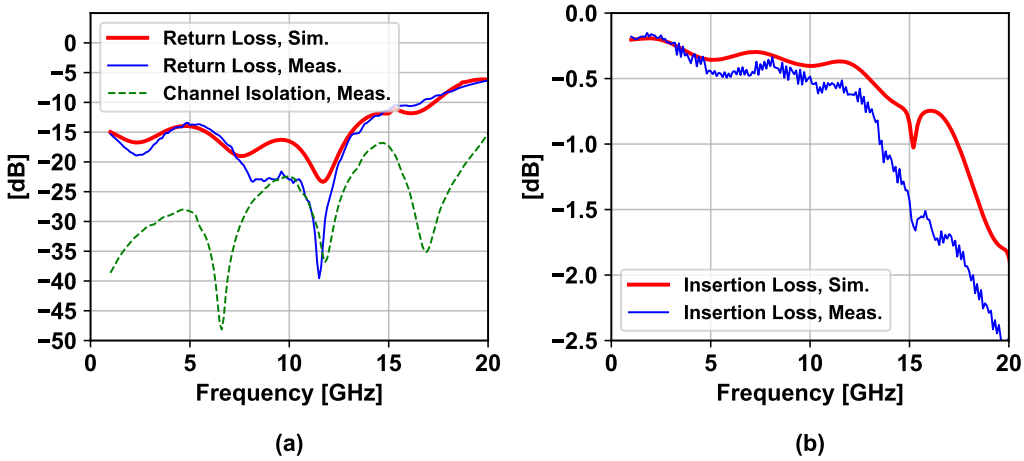


Figure 3.61: Chip interposer measuring (a) return loss and (b) insertion loss.

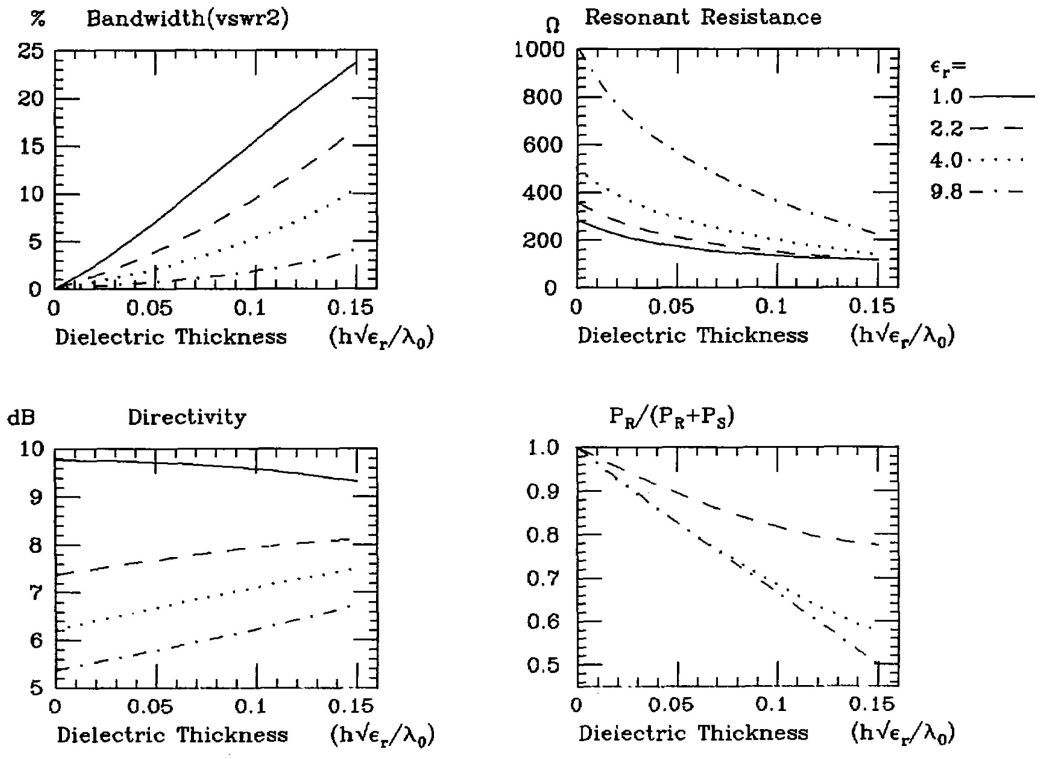


Figure 3.62: Bandwidth, directivity, radiation resistance, and efficiency with respect to surface waves excitation for a resonant square element as a function of dielectric thickness for different ϵ_r [85].

use a dielectric material to decrease their electrical length and reduce their size. Consequently, the EM field in the dielectric increases (for a given radiation power) so their loss increase as well [85]. Bandwidth is also affected. As an example, Fig. 3.62 illustrates the impact of the dielectric material on the performance of a rectangular patch antenna. An SSP spacecraft antenna should also be conducive to scaling of the array's size in terms of performance, manufacturing, and assembly capability. For our design, we use collapsible antennas as shown in Fig. 3.63. They are printed on a thin, 50 μm single-layer polyimide laminate and are designed as patches to reduce the required spacing from the ground plane, in order to improve the structural strength of the assembly. Vacuum is used as separation from the ground plane to reduce loss and increase the bandwitdth. This antenna has four square patches cut away from it to decrease the metal weight and reduce its size, which in turn also improve the isolation between the array's antennas. A series inter-digital capacitor is used to resonate the equivalent series inductance of the antenna lead to match it to the frequency of operation. The single antenna pattern is illustrated in Fig. 3.64. The patch antennas are intended to be used as single sheets, assembled

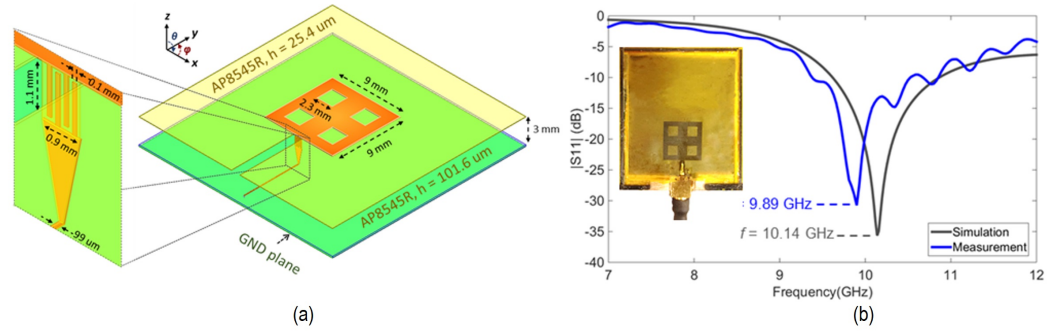


Figure 3.63: Vacuum-suspended patch antenna: (a) designed and (b) fabricated/measured [84].

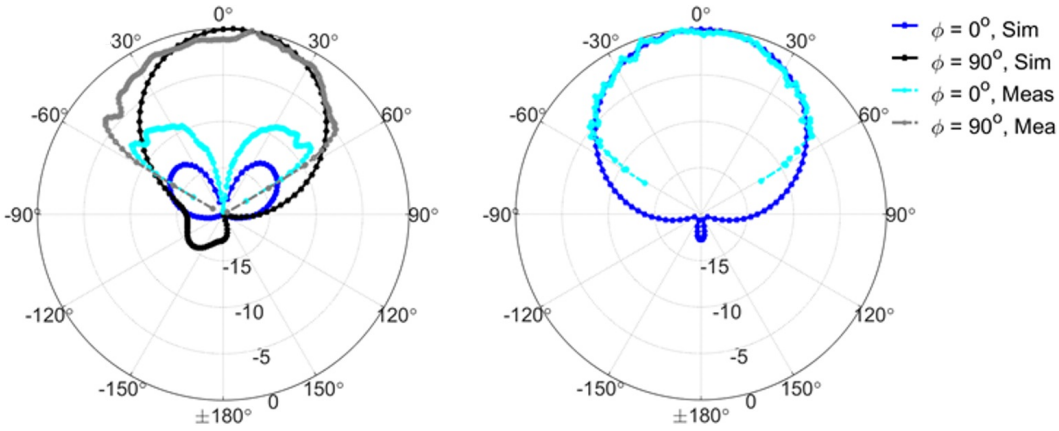


Figure 3.64: Flexible patch antenna pattern [84].

on top of the main board sheet. The antenna structure is placed flat on the main array board, with the leads soldered to the main board's footprint. It is then lifted so a vertical, matched feed excites the antenna, as shown in Fig. 3.65. After lifting, "s" shaped flexible springs are placed between the antennas and ground plane to support the structure. Those "s-springs" are flexible enough to allow for both sheets to be pressed (collapsed) together and rolled into a package. Due to the height difference between the two layers, the structure had some limit on the minimum radius of curvature of the packing as shown in Fig. 3.66.

One challenge with finite antenna arrays is that due to coupling and reflections, the antenna pattern in the array might differ from the standalone pattern. Fig. 3.67 shows such a difference using simple patch antenna designs. The implication is that usually there will be some difference between the expected and measured performance. In addition, this calls for a calibration procedure that will take these

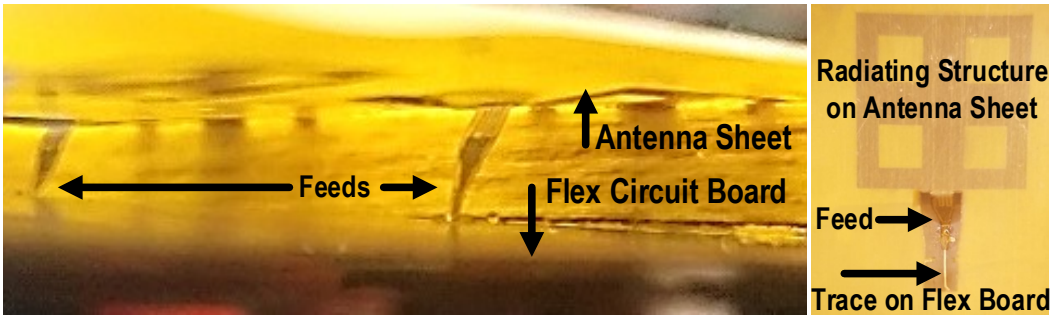


Figure 3.65: Flexible patch antenna sheet and feed above ground.

Figure 3.66: Antenna packing curvature limit due to different radii of the two flexible sheets.

factors into account. Such a calibration and focusing procedure will be described later, when an integration of several tiles to a larger system will be described.

Alternative antenna designs

The patch antenna sheets approach was fabricated and was shown to work. However, it has a few drawbacks: the antenna feed lines are thin and difficult to solder, and the use of two sheets severely limits the flexibility of the assembly. In addition, differences in the rigidity of the main and antenna boards deform the assembled antennas and create uneven locations where the antenna height above ground is significantly different than intended. It is therefore desirable to explore additional antenna design and assembly schemes.

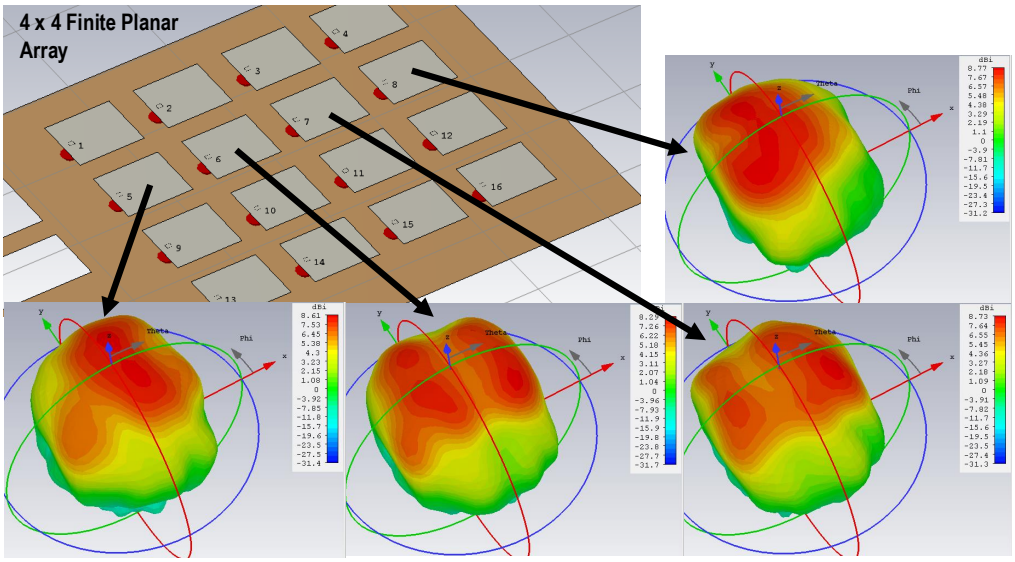


Figure 3.67: Simulated change in element pattern when placed in a finite-size array with a finite ground plane.

Vertical thin sheet

The most promising antenna structure is a vertically attached thin sheet structure as shown in Fig. 3.68. The radiating structure can be designed as a dipole and the $\approx \lambda/4$ distance from ground can be used for impedance matching. Physically, the thin sheet can be supported with a specifically molded fiberglass structure to maintain flexibility without deteriorating the electrical performance. A test antenna was designed and measured (Fig. 3.69). It exhibits a wider band matching and the simulated radiation pattern is wider than the patch pattern. The assembly can be simplified almost to the level of an SMT process (pick and place) with a proper support structure. The drawback of this antenna is its height, which might be unacceptable for some applications. It might also be unsuitable for terrestrial applications where wind might causes the antennas to wobble.

Helical spring

Another tempting option is the use of helical spring antennas. These can be more rigid than vertical thin films with similar performance as shown in Figs. 3.70 and 3.71. This antenna EM field is circularly polarized, and will require a receiver with circularly polarized antennas as well. The main drawback of this design is that the antenna's structural stability trades off with its flexibility. When the antenna is

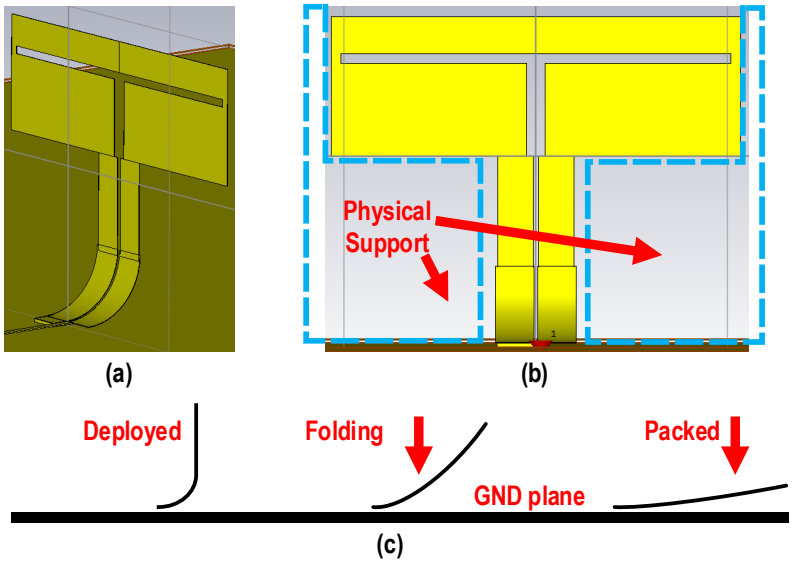


Figure 3.68: Vertical sheet antenna concept.

packed, it is compressed and the stored energy in multiple antennas might lead to unacceptable mechanical stress on the packed spacecraft sheet. Designing a dual polarized equivalent structure is challenging as well.

High dielectric patch

While using high dielectric patches above the ground plane in order to reduce the antenna size might be unsuitable for space-power applications, it can still be useful for communications and sensing, or for applications where structural integrity is more important than performance. The antenna size can be further reduced to $\approx \lambda/4$ on the expanse of efficiency by using a PIFA [86] structure.

Materials selection

In order to reduce the system's weight as much as possible, a thin flexible PCB substrate is used for the main and antenna boards. The planar antennas require only a flexible substrate bonded to a single copper layer. The thinnest commercially available substrate is a 50 μm polyimide layer with a 12 μm copper clad. The main board build is dependant on the level of the integration of the SSP RFIC and on several high-frequency design choices. Currently, a microcontroller is not integrated in the RFIC package. This requires a large number of digital signals to be routed on board. The output RF transmission lines which are routed to the antenna feeds are designed with a specific characteristic impedance and are matched

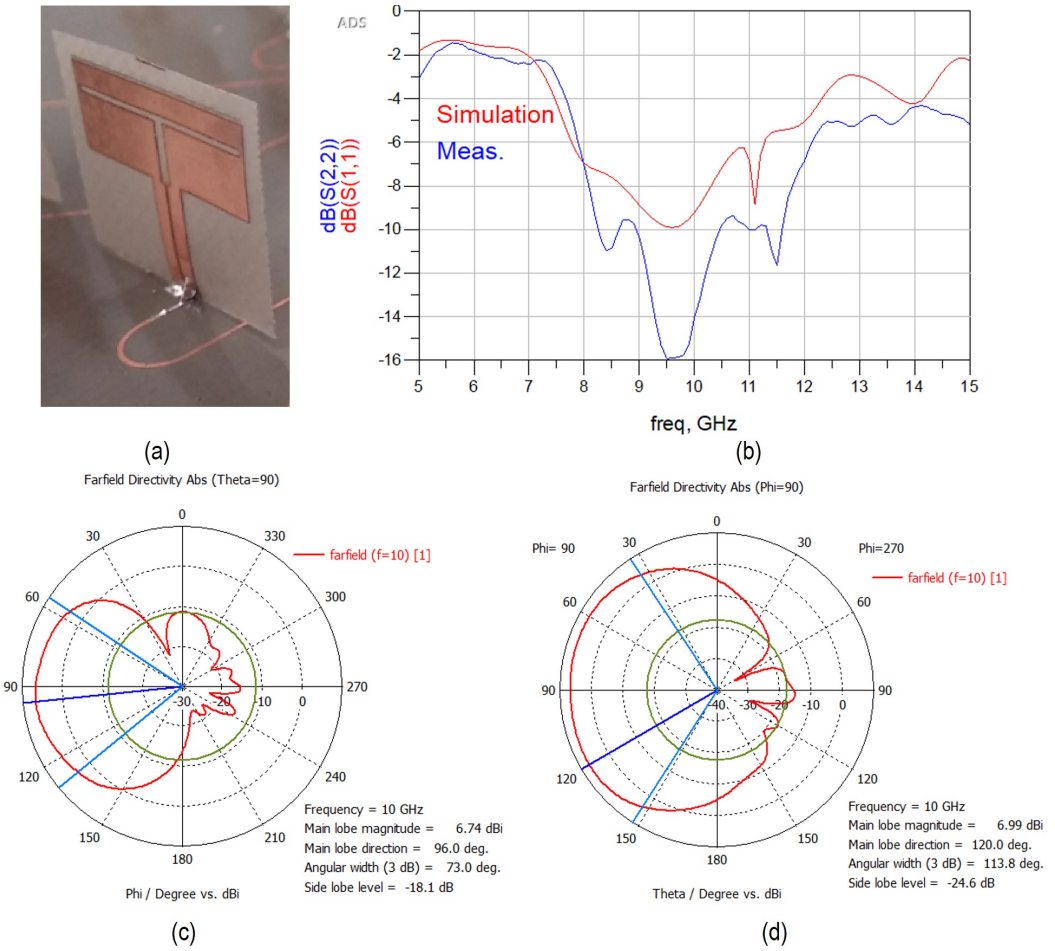


Figure 3.69: Vertical sheet antenna (a) test structure (the plastic support should be removed or changed in the final design), (b) input matching, (c) antenna pattern 0°, (d) antenna pattern 90°.

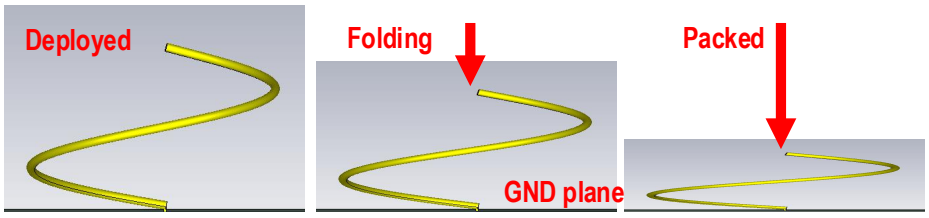


Figure 3.70: Collapsible spiral spring concept.

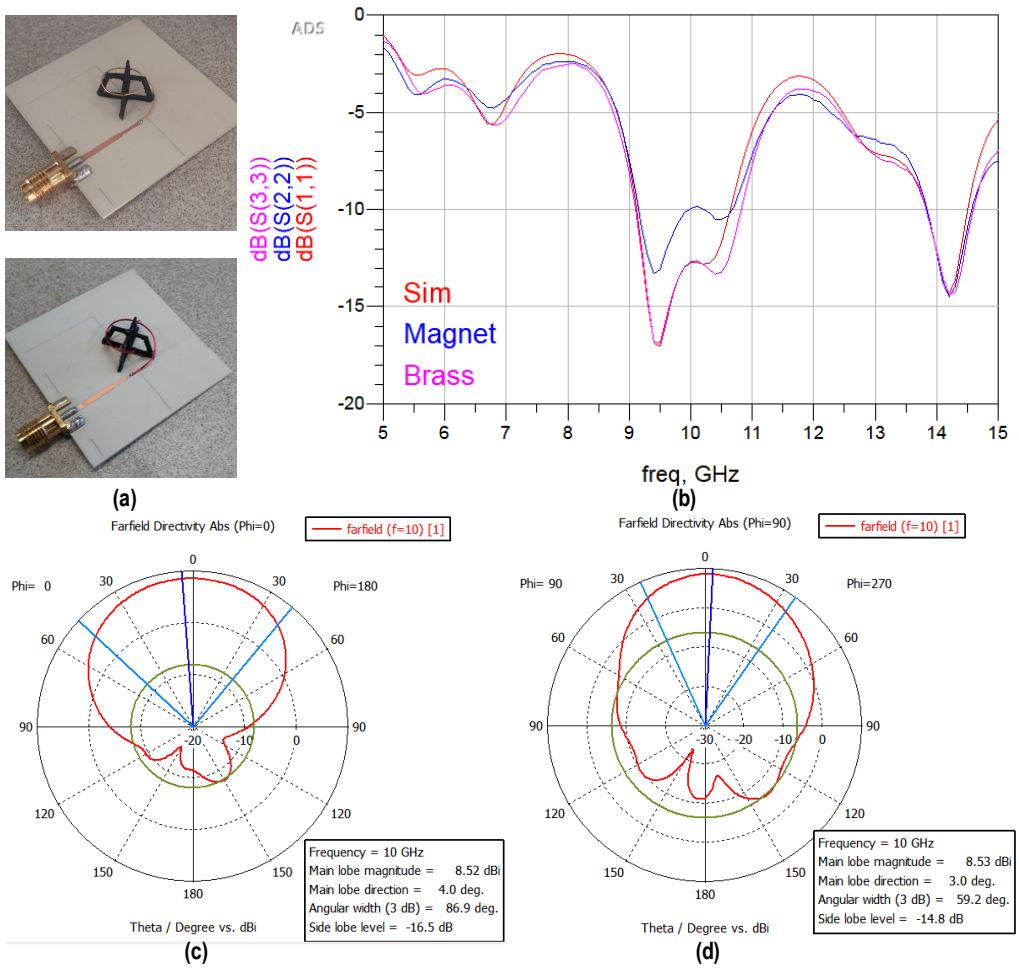


Figure 3.71: Collapsible spring antenna (a) test structure (the plastic support should be removed or changed in the final design), (b) input matching, (c) antenna pattern 0°, (d) antenna pattern 90°.

to the antenna impedance, which is in turn matched to the free-space impedance. Practically, microstrip transmission lines are the only feasible choice because they need a single ground plane, provide almost ideal isolation to the line's backside, and do not require a large number of ground-vias. Three parameters can be modified to allow the use of a thinner dielectric layer effectively lowering the board's aerial mass:

– **Characteristic Impedance**: Lowering this parameter allows the use of a microstrip with a higher width/height ratio. This, however, results in a higher transformation ratio from the set free-space impedance, lowering bandwidth and efficiency.

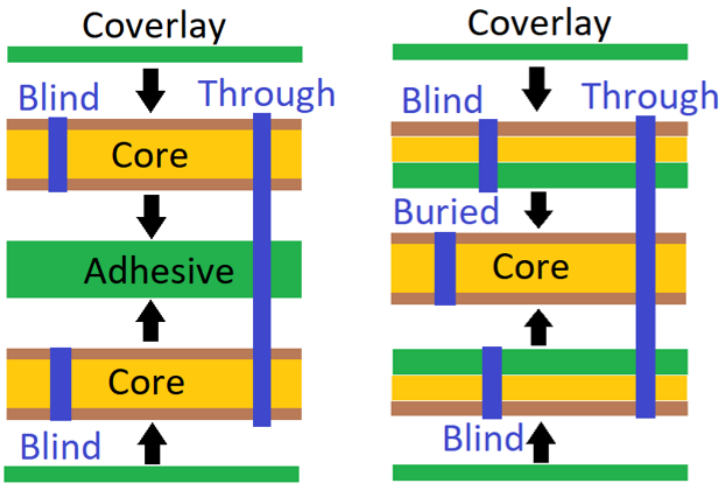


Figure 3.72: Fabrication options for a flexible 4-layers PCB.

- **Line thickness**: Lowering this parameter allows the use of a thinner substrate for a set characteristic impedance, whith some hit in efficiency as well. It is constrained by the fabrication process tolerance.
- **Dielectric constant**: Lowering this parameter increases the vertical electrical length and allows to use thinner substrate for a given transmission line characteristic impedance. The dielectric constant of polyimide is about 3.5 and reducing it further requires the use of specialty materials which are costly and usually weaker mechanically.

While future design iteration may allow to implement the SSP tile on a 2-layer circuit board, currently 4 layers are needed. The board can be fabricated with commercially available single- and double-layer laminates as illustrated in Fig. 3.72. Since the transmission lines function is crucial to the system performance, the fabrication option described in Fig. 3.72 is preferred. The implication though is that buried-vias cannot be used in the design. This is another reason that microstrip lines are used.

The microstrips are designed with a 50 Ω characteristic impedance on a DuPont™ Pyralux® TK which is polyimide infused with teflon. The 2-layer laminate has a dielectric constant ϵ_r =2.5. This allows the use of transmission lines of 100 μm, within fabrication tolerances, with a dielectric thickness of down to 75 μm to separate it from the ground plane. The copper traces were neither plated or covered with isolating laminate (coverlay) to guarantee that they perform as designed. The

finished 4-layer board has an areal density of roughly 0.1 gr/cm^2. A reduction in weight can be achieved by perforating the ground plane to reduce the copper weight of the board. This has minimal implication on the antenna performance if the holes are much small and closer to each other compared to the transmitted wavelength.

RF measurements

The fabricated flexible RF antenna was characterized using a mechanically scanned near-field range [87]. Functionally, a phased array should be able to perform steering of the main lobe in a tangible fashion. In terms of performance, the array output power and EIRP need to be measured.

Measurement Setup

The near-field range uses a vector network analyzer (VNA) to excite an antenna under test, (DUT) and to read the received power in a pre-characterized antenna probe. The probe location can be swept mechanically to measure a 2-D field intensity and phase. The measurement can be either in the near (Fersnel)- or far (Fraunhoffer)-field of the DUT and a far-field pattern can be computed mathematically later in either case. The whole setup is placed in an anechoic chamber to prevent reflections that will degrade accuracy. This allows to obtain a plethora of interesting data regarding the DUT, including complex field components, directivity, polarization, beam steering capability etc. Active antenna arrays that generate the output signal from a low frequency reference require a minor adaptation in order to be measured using this range: since a VNA performs a single-frequency measurement, its output signal must be divided down to the antenna's reference frequency, and the on-chip synthesizers must be set with an equal multiplication ration to avoid erroneous measurement. The measurement setup is illustrated in Fig. 3.73. The flexible phased array was characterized using the near-field range with a near-field probe at 30 cm away from its plane. The probe used is an E-field linearly polarized antenna, which can be rotated 90° around its normal axis to obtain the complex field components. The required phases for the antennas were set using the individually controlled CMUs in each of the RFIC's output channels. The array was measured around 9.8 GHz which is slightly offset from the design frequency of 10 GHz due to small antenna detuning.

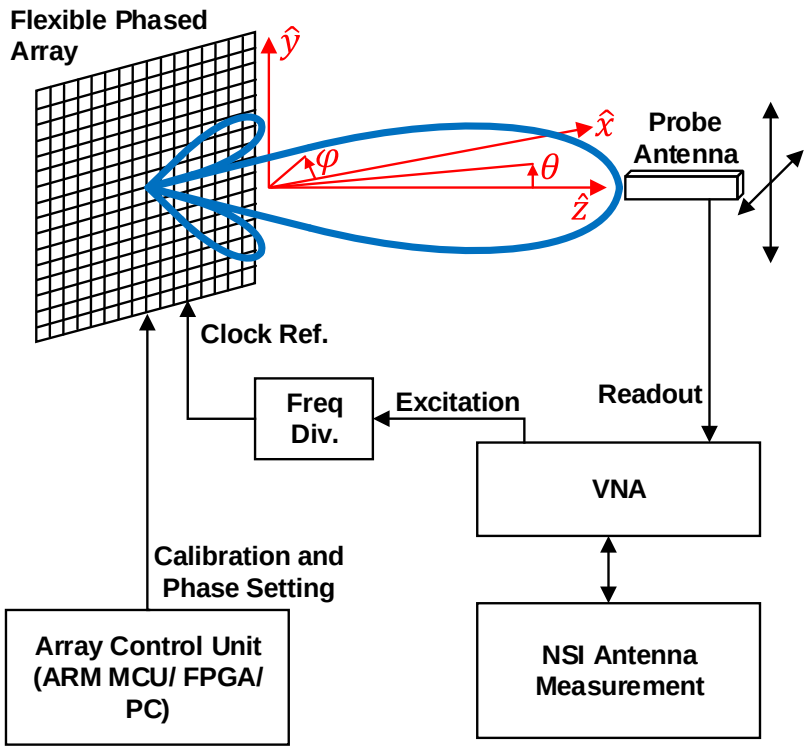


Figure 3.73: Array pattern measurement setup.

Phase Steering

For a *uniform* array, the element phase difference β required to generate a maxima of the array factor at an angle θ_m from the normal to the array plane is

$$\beta = \frac{d}{\lambda} \cdot 2\pi sin(\theta_m) \tag{3.28}$$

where d is the element spacing and λ is the radiated wavelength [42]. For an array operating at 10 GHz with 0.6 λ between elements, this is ≈108° of phase difference. As mentioned before, this should be the phase shift at the antenna output, and there may be large static and dynamic phase offsets between each output channel. In order to overcome the unknown phase offset, the antennas' phases were initially calibrated using a straightforward phase sweep over all of the 16 output channels' digital settings. The required phase for maximum power at broadside were also estimated using a 3-D EM simulator [88] and the result is shown in Fig. 3.74. It is noteworthy that, while this method works, it is inefficient and unpractical for larger arrays. A better approach for focusing and calibration will be described later,

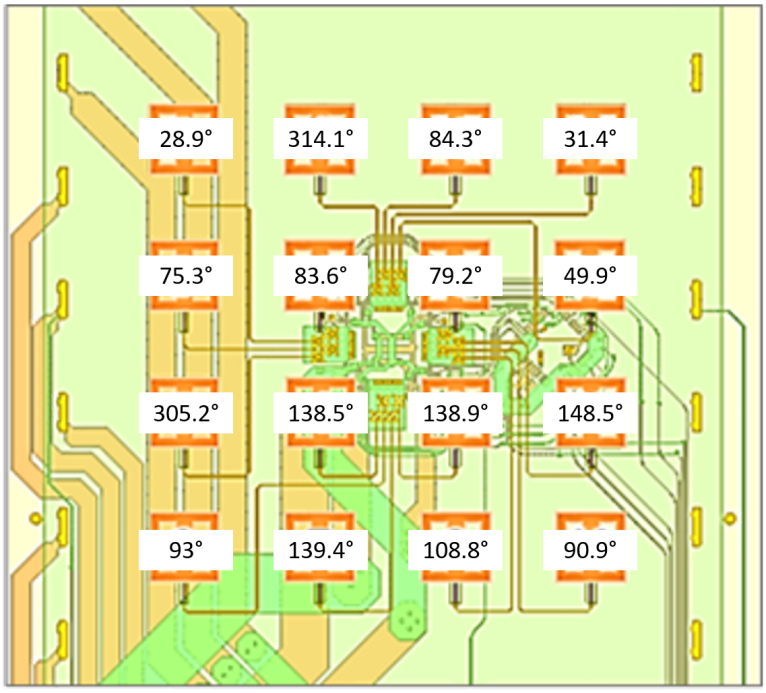


Figure 3.74: Simulated phase of each antenna output for broadside radiation [84].

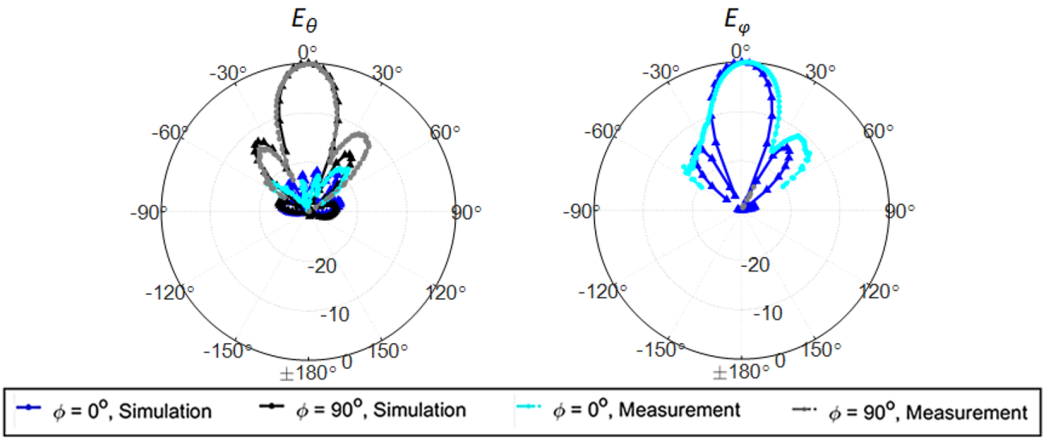


Figure 3.75: Array broadside pattern [84].

where a 256-element array will be presented. The resulting radiation pattern was measured, and is shown in Fig. 3.75. Using the same phase sweep procedure, the array's beam was directed at 30° left (φ = 0°, θ = 30°), and later at 30° up (φ = 90°, θ = 30°) as a demonstration of beam-steering capability (Fig. 3.73 shows the choice of direction). Fig. 3.76 shows the measured x- and y-components of the E-field for those steering angles. The patch antennas are linearly polarized and the measured radiation pattern is mostly an E-field along the y-axis as expected.

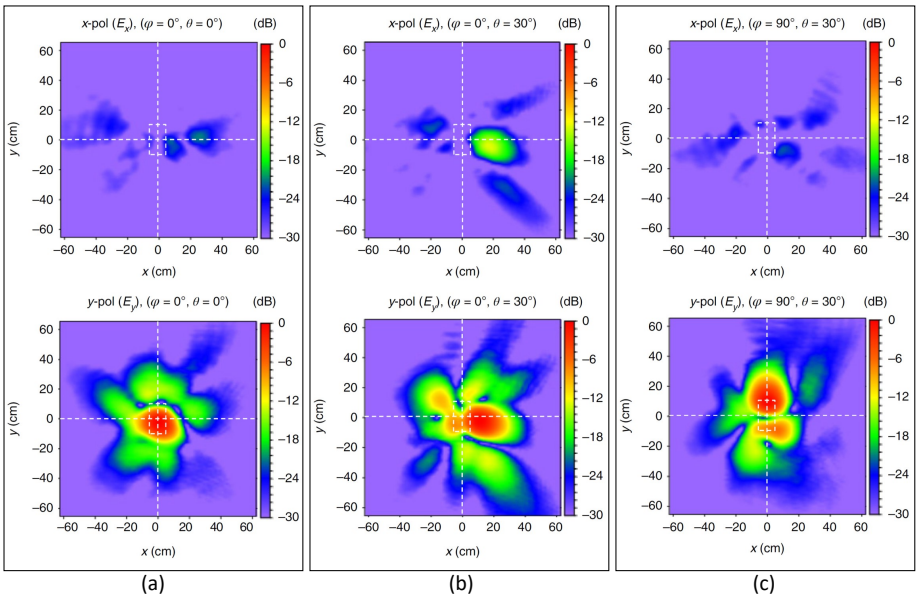


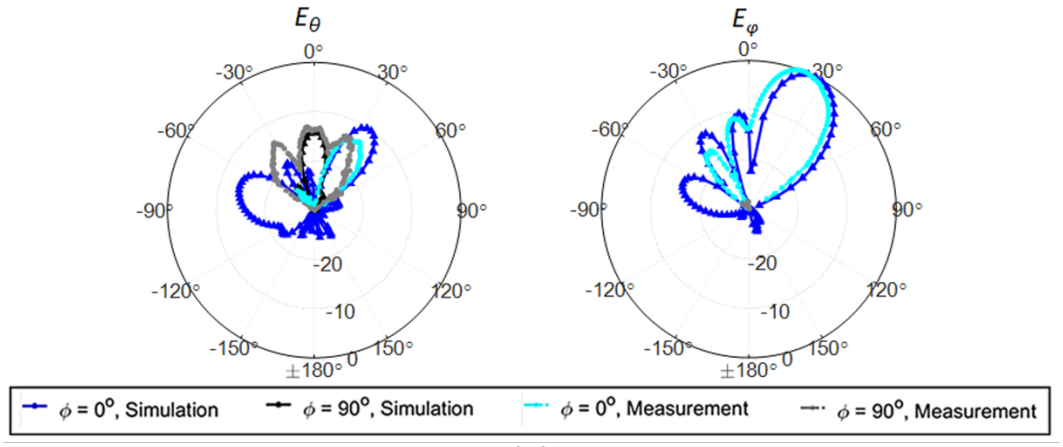
Figure 3.76: Broadside array fields recorded in 2-D [84].

Table 3.11: Measured (simulated) pattern data for broad-side beam ($\varphi = 0°, \theta = 0°$)

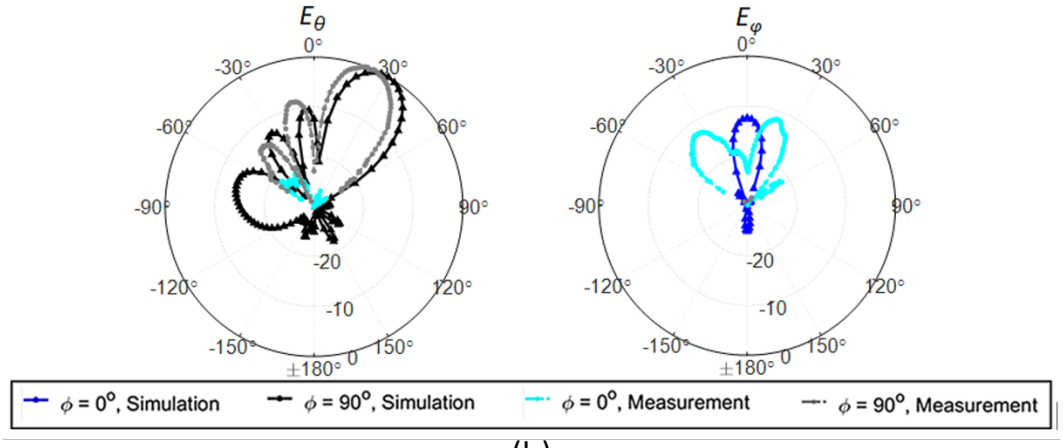
	$E_\theta,\ \varphi = 0°$	$E_\theta,\ \varphi = 90°$	$E_\varphi,\ \varphi = 0°$	$E_\varphi,\ \varphi = 90°$
Normalized intensity [dB]	-18.19 (-20.21)	-0.12 (0)	0 (0)	-24.64 (-36.99)
Largest sidelobe [dB]	-18.19 (-20.21)	-10.92 (-12.54)	-11.09 (-14.31)	-24.64 (-38.04)
Half-power beamwidth [Deg.]	-	23 (22)	20 (21)	-

By performing a near- to far-field transformation, the far-field radiation properties of the tile are obtained. Fig. 3.77 shows a comparison of the measured versus simulated steered antenna patterns. Tables 3.11, 3.12, and 3.13 compare the data of the measured radiation patterns to simulation. The measurement and simulation show good agreement in terms of the radiation patterns, half-power beamwidth, radiation efficiency, and sidelobe levels.

The near-field range can generate 3-D holograms of the radiated fields in space by performing multiple 2-D measurements along the z-axis. This is a valuable capability for near-field applications where a beam is focused in space rather than steered to the far-field (infinity focus). Fig. 3.78 illustrates the field evolution of the three generated beams, which allows a better understanding of the array performance and phase search procedures.



(a)



(b)

Figure 3.77: Steered beam pattern (a) up and (b) left [84].

Table 3.12: Measured (simulated) pattern data for left-steering ($\varphi = 0°$, $\theta = 30°$)

	E_θ, $\varphi = 0°$	E_θ, $\varphi = 90°$	E_φ, $\varphi = 0°$	E_φ, $\varphi = 90°$
Normalized intensity [dB]	-13.33 (10.14)	-13.03 (-14.09)	0 (0)	-28.33 (-29.09)
Largest sidelobe [dB]	-24.7 (-14.11)	-14.04 (-24.38)	-11.55 (-10.58)	-28.36 (-37.08)
Half-power beamwidth [Deg.]	-	-	25 (24)	-

Table 3.13: Measured (simulated) pattern data for up-steering ($\varphi = 90°$, $\theta = 30°$)

	E_θ, $\varphi = 0°$	E_θ, $\varphi = 90°$	E_φ, $\varphi = 0°$	E_φ, $\varphi = 90°$
Normalized intensity [dB]	-21.77 (-31.51)	0 (0)	-12.41 (-26.95)	-29.03 (-39.88)
Largest sidelobe [dB]	-21.77 (-31.51)	-8.57 (-10.6)	-9.25 (-18.65)	-20.48 (-10.28)
Half-power beamwidth [Deg.]	-	23 (24)	-	-

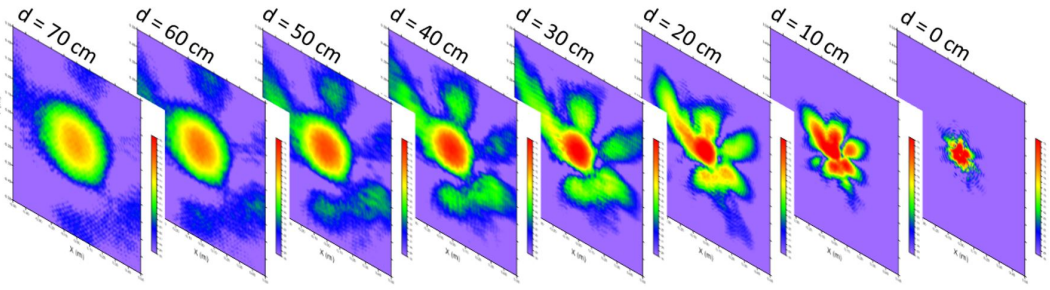


Figure 3.78: Phased array transmitter tile broadside hologram shows the evolution of the radiated field in space [84].

Power Measurement

Even though the tile array has 16 radiating elements, the maximum radiated power was obtained with only 12 elements turned on. This is probably due to thermal sensitivity of the RFIC and maybe some marginal stability resulting from all 17 on-chip PLLs working and pulling each other to some extent. The raw output of each PA measured about 50 mW and the loss associated with the interposer (1-2 dB in the measured version), transmission lines (2-3 dB), and antennas (<1 dB) results in an output power of about 10-20 mW per antenna. The total power in the main lobe is estimated at 19.2 dBm, slightly lower than the expected of 12 output channels maybe due to heating and element-to-element non-uniformity. The tile's EIRP in the frequency range of 9.4 – 10.4 GHz is shown in units of dBW in Fig. 3.79 with the four elements in the corners turned off. A nearly constant maximum EIRP of +38.2 dBm is achieved at 9.56 – 9.72 GHz with an EIRP of +37.1 dBm at 9.8 GHz. Later iterations of this design have improved both the interposer and transmission lines losses, have reduced the output loss, and enabled a stable operation with all 16 elements turned on.

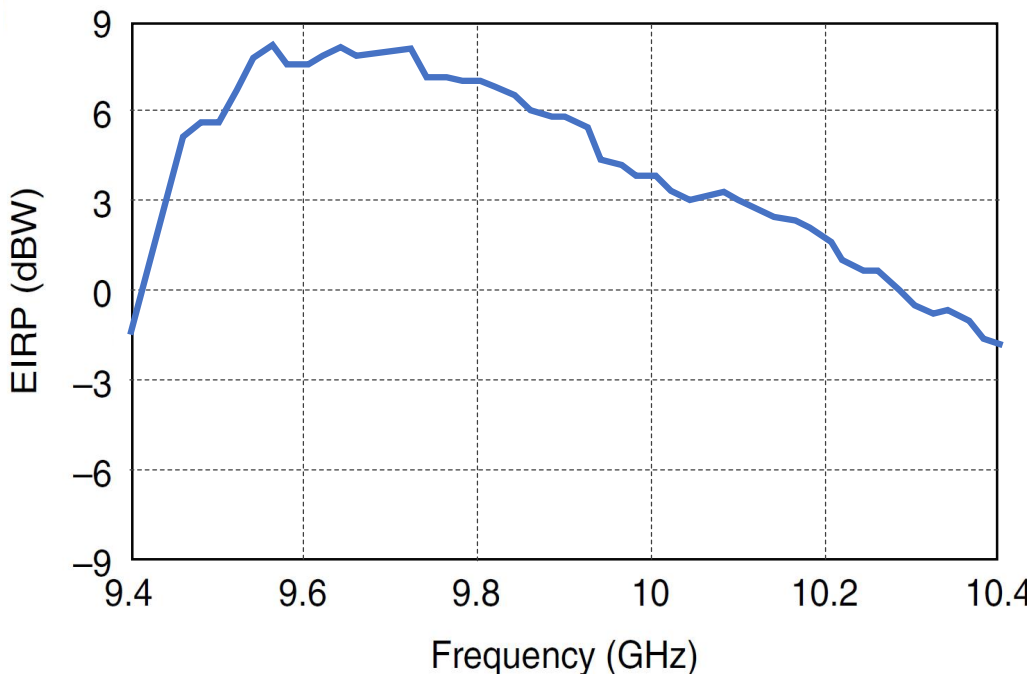


Figure 3.79: Phased array transmitter tile EIRP (image reproduced from [84]).

Solar integration

The flexible phased array tile was integrated with PV cells as a proof-of-concept lightweight SSP spacecraft building block. The structure includes three major parts as illustrated in Fig. 3.80b: an antenna sheet fabricated on a lightweight single copper layer polyimide laminate, a 4-layer carrier board with an SSP RFIC and voltage regulators, and PV concentrators. The latter are parabolic reflectors with a high efficiency solar cell attached onto their back that use lightweight reflective materials to reduce the PV cells' weight and cost, as shown in Fig. 3.80b. The antenna board is attached to the carrier board by flexible carbon-fiber springs that demonstrate its deployability, and is enclosed in a thin frame so it does not collapse.

Unfortunately, the photovoltaic concentration scheme is extremely sensitive to mechanical deformation and manufacturing variations. In order to make certain that sufficient power is supplied to the RFIC to guarantee its functioning the tile area was increased for the demonstration purpose from 7 cm $\times$ 7 cm to 16.5 cm $\times$ 10 cm. It should be stressed, however that this is an integration issue and not a fundamental limitation of the design. Fig. 3.81 shows the finished tile.

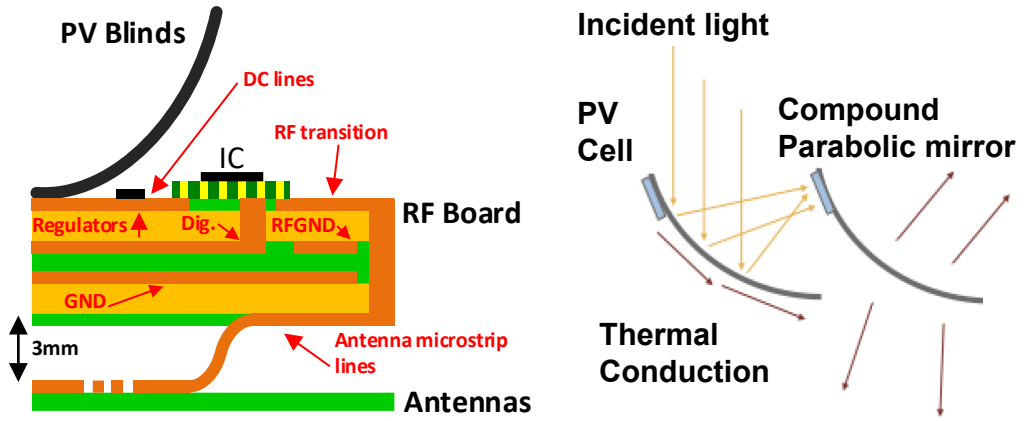


Figure 3.80: Integrated tile: (a) structure and (b) PV reflector concept.

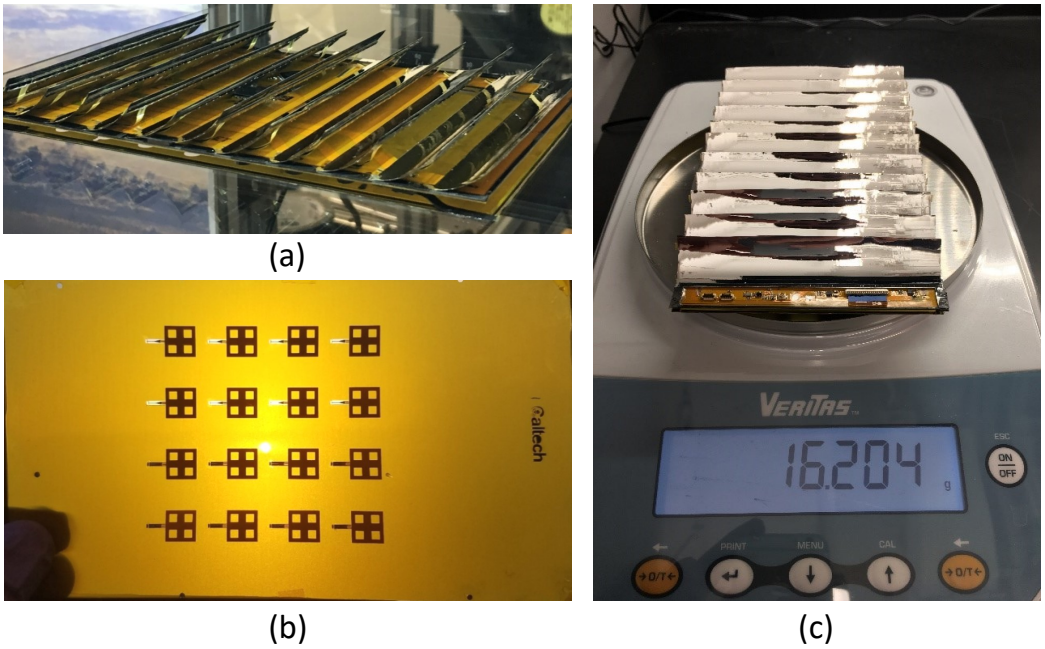


Figure 3.81: Integrated RF-PV tile. (a) Completed demonstration board, (b) antenna sheet, and (c) weight of the assembled board.

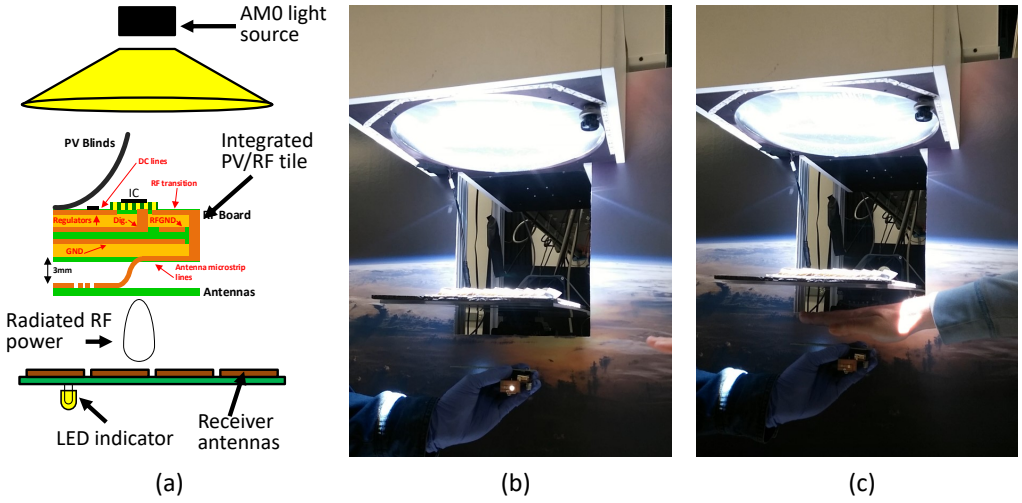


Figure 3.82: Testing an integrated RF-PV tile under AM0 light source. (a) Measurement setup, (b) demonstration of RF lighting an indicator LED. (c) Power is not transferred when line-of-sight is lost.

The RF-PV functionality was tested under a light source with AM0 intensity directed at the solar concentrators. A simple rectenna-array board with an indicator LED is placed on the other side of system and the transmitted RF power is strong enough to light it at a distance of about 20 cm away as shown in Fig. 3.82. This proof of concept demonstration showed that efficient wireless power transfer can be done with structures that are about two orders of magnitude lighter than the ones used in previous works. Thus this is an important step forward to building economically viable space solar power systems.

3.6 System-scale Integration

While the demonstration of a flexible phased-array building block unit is valuable, scaling the system size presents additional significant challenges, notably when compared to similar arrays without beam-steering capabilities [89]–[91]. Distributing a reference signal over large distances results in attenuation and added noise due to the loading of the clock lines, as discussed in section 3.4. Transfer of data to a large number of ICs is either done in parallel, which requires additional on-board real-estate, or serially, which slows down the programming speed or requires an increase in data throughput. The alignment and assembly of a large antenna sheet requires a robust manufacturing process to avoid local deformations in the deployed array. Power distribution might not be a challenge for SSP applications where the

PV unit cells supply the power to each tile locally, but other applications might suffer from significant IR losses if they use long DC lines for power distribution. Additionally, a simple phase sweep procedure is impractical to use for array calibration and focusing due to exponential growth in the possible phase states. The following section will present the design and measurement of a 256-element, 16-RFIC phased array that was built from the SSP tile, and will include details regarding the design challenges and measured performance.

Main board design

The main board is designed using the same 4-layer fabrication process that was used for the single tile demo. As a first step towards a scaled-up system, we use a commercially available flexible-PCB laminate from DuPont™ , Pyralux® AP[92], which is a copper-clad polyimide core. The polyimide has a dielectric constant of 3.4, which requires the use of a 100 μm laminate and slightly increases the system's aerial mass over lower dielectric constant materials. On the other hand the copper adhesion is significantly stronger than Pyralux® TK, for example. this proved better for an initial assembly. This 256-element array is still small enough such that a single low cost CMOS-level pierce-gate oscillator can drive all its RFICs simultaneously at 50 MHz. An EM simulation [93] was run to predict the drive level at the IC input. The reference distribution is designed as an H-tree to provide a matched reference clock to all the ICs. It is noteworthy to remember that, due to production tolerances and PCB design constraints, there might be a residual delay between the ICs that translates to a non-negligible phase difference at 10 GHz. Further increase in the board size might require additional measures as described in section 3.4 to guarantee a low-noise, low-power clock distribution to all the array RFICs. In order to increase the write speed to the array, a field programmable gate array (FPGA) is used as a communication interface to the array with 16 SPI interfaces that are synthesized in hardware for parallel data transfer. It is important to remember that even though an FPGA can output a parallel bitstream, a CPU (or a thread for that matter) that controls it can only process data in series. Therefore this approach makes sense only if the CPU speed is much higher than the SPI interface. Here we are using a xilinx zync® board [94] with an integrated CPU working at 667 MHz to write to a several-MHz SPI module so the previous requirement is fulfilled.

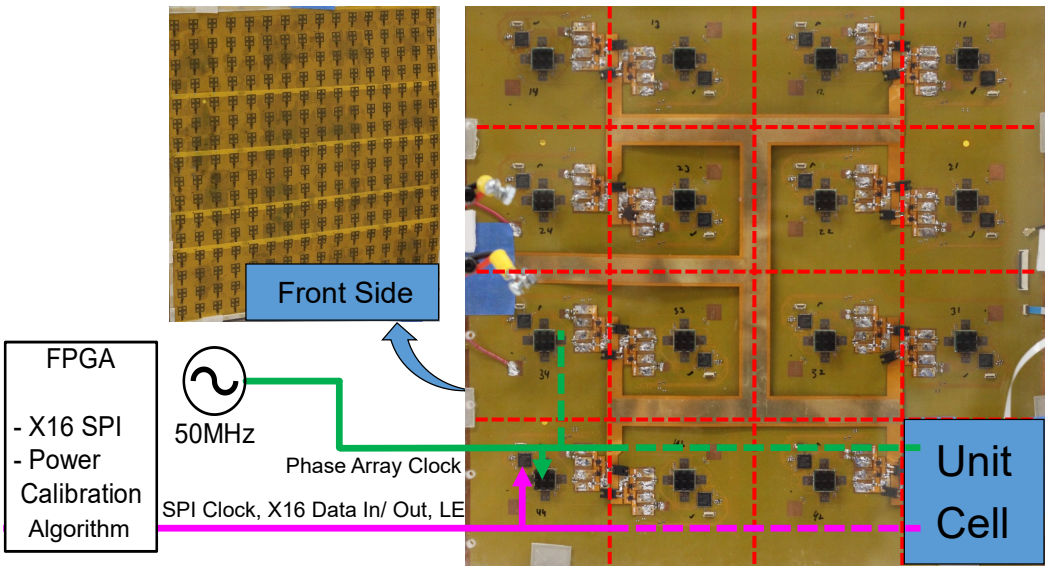


Figure 3.83: An assembled flexible phased array transmitter.

The power strap

DC power is not distributed on the 4-layer flexible circuit board, but instead brought to each sub-unit individually from a 2-layer flexible skeletal structure called the power strap. The mass-saving power strap is made using an inexpensive, non-impedance-controlled substrate with less precise manufacturing standards than the flexible circuit board with 10 GHz transmission lines. The power strap board is shown in Fig. 3.84. The power strap input voltage is 1.8V, which powers the RFIC's stacked PAs directly, and is doubled and regulated to provide other voltage levels needed by the RFIC and local MCU. High-current switches allow the power strap board to power the tiles from a single shared supply or from individual supplies located nearby. The local, individual power option is intended for use in conjunction with photovoltaic cells, which would mount on the opposite side of the planar array, away from the radiators [95]. This capability allows for distributed powering of the array, avoiding heavy, high current carrying wires. Figs. 3.84 and 3.83 illustrate the component-side of the 16-tile phased array and add details about the assembly of the reference clock, data, and power supply to all the array tiles.

Antenna sheet and assembly

The single-chip, 16-antenna design was scaled to a single 30 cm $\times$ 30 cm array of 16 $\times$ 16 radiators. Around the feed of each radiator, there is a cut in the thin

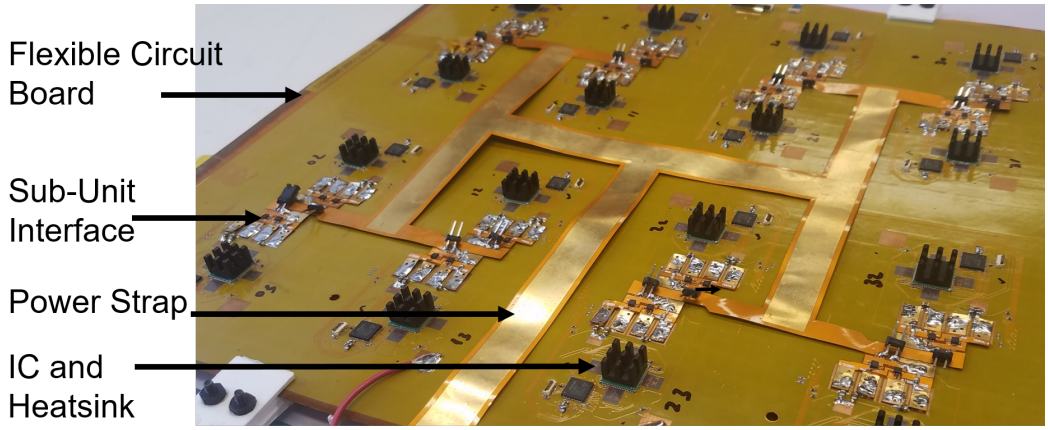


Figure 3.84: Power strap and supply interface for the flexible phased array transmitter.

polyimide layer with small spacers that should be detached after assembly (Fig. 3.85) to enable the lifting of the antenna sheet. Soldering the antennas to the main board requires a special attention. The antenna leads are 100 μm thick lines, that should be aligned and remain in place with a 30 cm $\times$ 30 cm board throughout the assembly process. Clearly, assembly by hand is impractical and will be impossible with larger array sizes. Here we use a "sandwich" concept in which the antenna and the main board are fixed together with solder paste in between, and put with a rigid aluminum fixture in a reflow oven, as shown in Fig. 3.86. This approach can presumably scale with the oven size, or even be implemented using a cylindrical rolling mechanism to process very long sheets. The initial assembly attempt yielded about 85% of the antennas successfully reflown to the main board, and the rest were re-worked manually. While not yet perfect, this made the assembly of the entire array much more manageable.

Focusing

There are several challenges in calibrating large phased arrays to deliver maximum power to a target device [96]. Most notably, the receiver unit must have a dynamic range large enough to sense small phase changes while not saturating when the array is fully optimized as illustrated in Fig. 3.87. Inter-element coupling and system non-linearities (e.g., synthesizer frequency pulling) can present additional challenges. Flexible arrays add another layer of complexity because each element may have a different radiation pattern when the array is deformed and mechanical vibrations can add significant noise to the optimization process [97]. To mitigate these issues, we

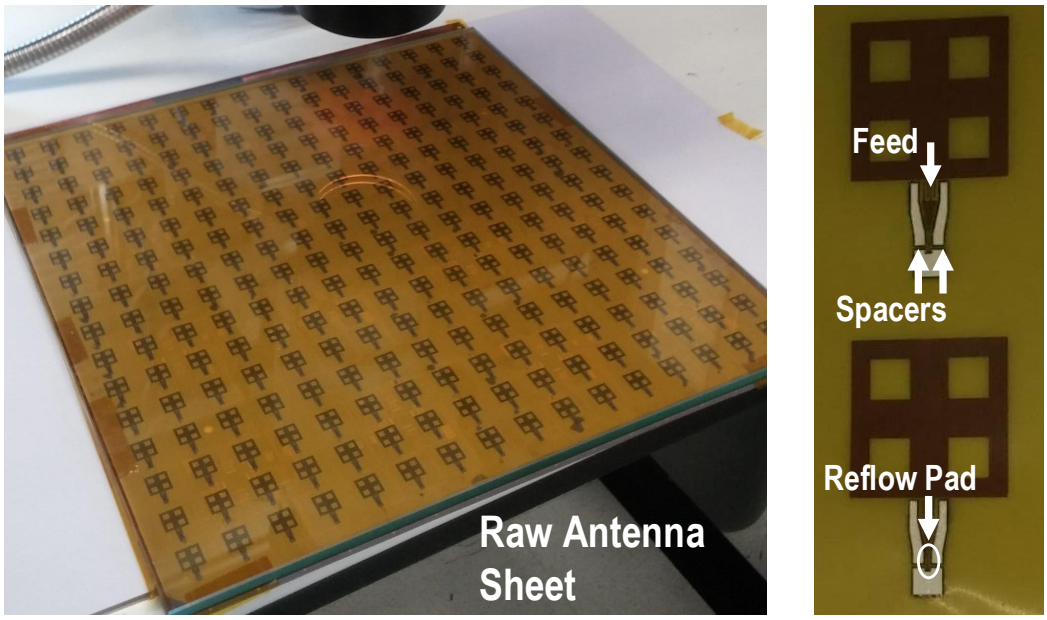


Figure 3.85: Antenna sheets: (a) a raw sheet and (b) a close-up on the board interface.

utilize a novel search algorithm to find the optimum phases of groups of elements – each group is constructed by an appropriate 2-D orthogonal matrix (which, for instance, can be generated from Hadamard matrices) to form an orthogonal basis. Fig. 3.88 shows several examples of how to change the phases of groups of array elements simultaneously to increase the transmitter's output variations and overcome the receiver sensitivity limits. In this manner, in the beginning of the optimization, we search over large variations of small groups of elements (coarse optimization), and in its end, we search over small variations in large groups of the array elements (fine optimization). This approach equalizes the amount of received power changes due to large and small phase sweeps to alleviate the receiver dynamic range requirements with a reasonable optimization time (1000-2000 steps for a 256-element array). Using an N-ary search avoids potential convergence issues associated with other optimization and focusing algorithms in a noisy environment (e.g., gradient decent). To perform a beam optimization, a small rectenna board is placed in front of the phased array and in each iteration, it feeds back a relative power reading to the optimizer. The latter then reprograms the array element phases, takes the next reading, and repeats. It is noteworthy that this method allows to optimize power delivery in the near-field, and that the optimizer can be implemented to work at tens of MHz on an FPGA, for example, to allow real-time power delivery optimization. Fig. 3.89 shows the optimization setup and an exemplary optimization sequence of

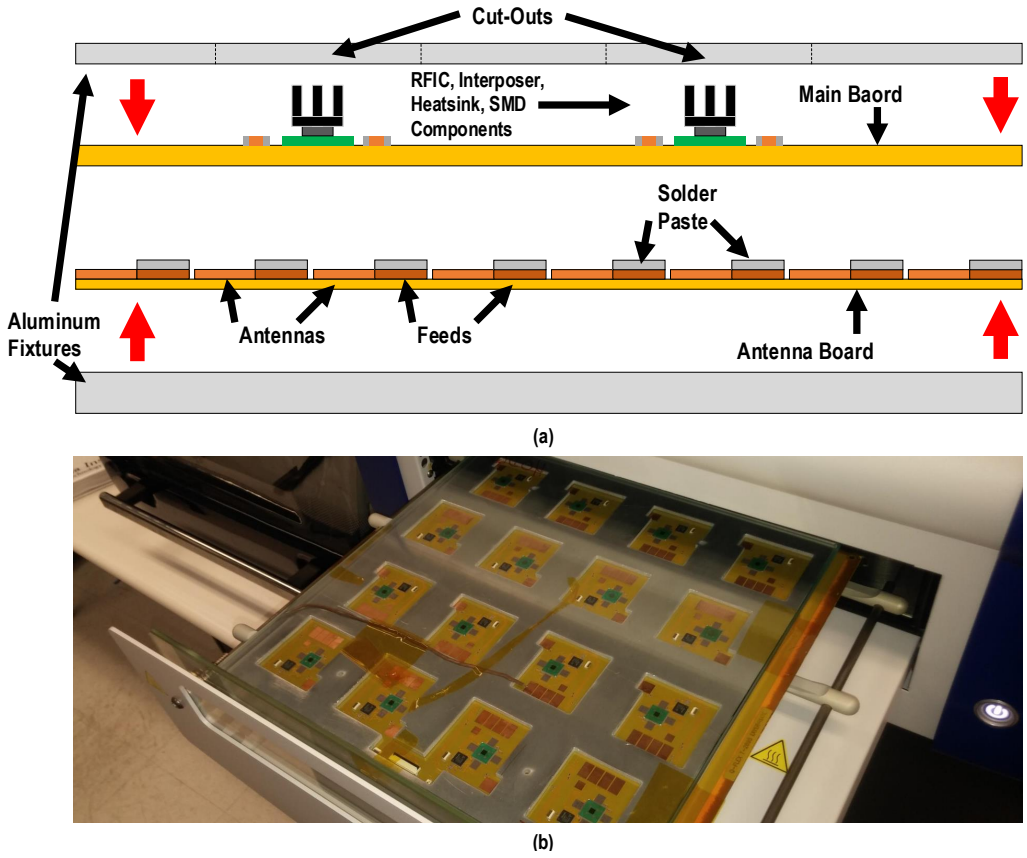


Figure 3.86: Antenna sheet assembly. (a) Schematic description and (b) a demonstration of the assembly process.

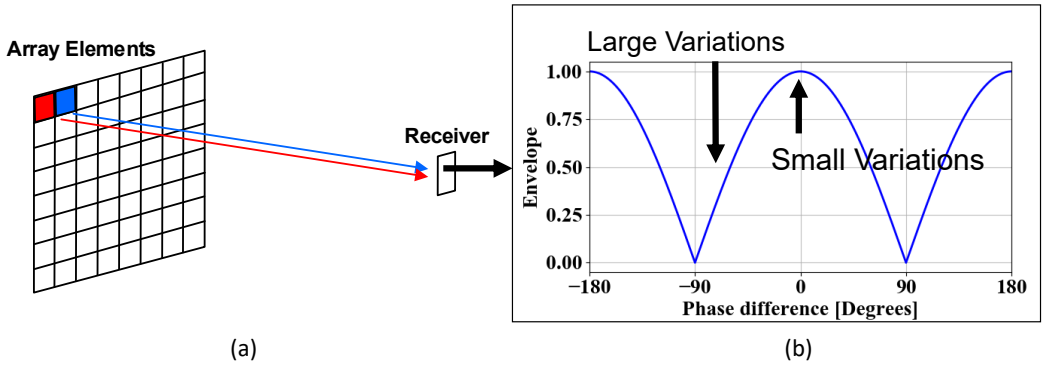


Figure 3.87: The challenges in calibration of large arrays. (a) Physical problem setup and (b) implication on receiver dynamic range.

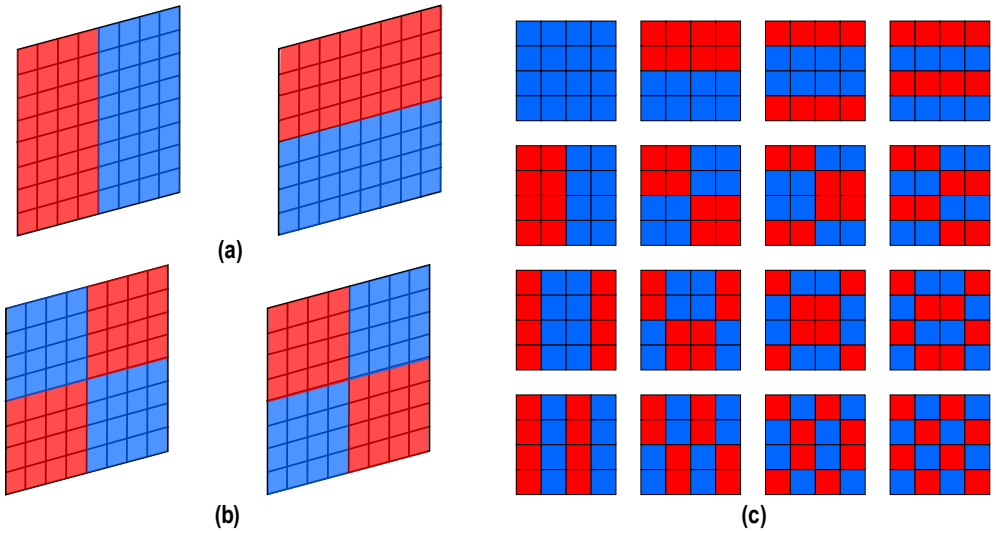


Figure 3.88: Selecting groups of elements for phased array calibration/focusing: (a) half the array elements and (b) fourth of the array elements. (c) An example for a selection of groups of elements in a 16-element array to span an orthogonal phase space.

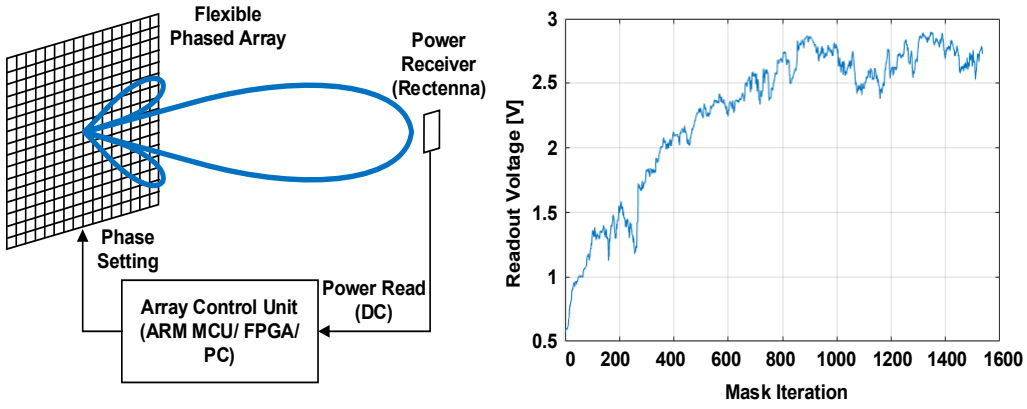


Figure 3.89: Phased array focusing setup (left) and results (right).

the flexible phased array.

Beamforming

To demonstrate the flexible phased array's beam-forming and beam-steering capabilities, the array was calibrated in 5 different steering configurations using the previously described method. The focus point was steered broadside, as well as left/right/up/down to demonstrate 2-D beam-steering. The radiation pattern was measured using the mechanically scanned near-field range in Fig. 3.73, and then

transformed to a far-field pattern. The scan range of the near-field range limits the measurement to 14 degrees of elevation and 40 degrees of azimuth in the far field, with non-physical transform effects occurring at the extremes of the view width. The measured far-field radiation patterns in Fig. 3.90a-e show sidelobe levels below 7 dB and demonstrate a successful beam forming. The sidelobe levels would be reduced if the optimization target distance had not been constrained by available measurement space. The power in the broadside-focused beam main lobe was calculated by integrating the area under it and scaling the result by the maximum measured power density at the range probe. This power estimate is pessimistic because it assumes that the initial probe location was indeed at the maximum of the main lobe, and it neglects the losses due to the non-isotropic probe pattern. Nevertheless, under these constraints, we calculated a main focal-point power of 0.8W at a distance of 2 m.

Deformation correction

For use in deployable and conformal systems, flexible phased arrays must be able to correct their radiation pattern if their mechanical shape is deformed. Here, we deform the array convexly to demonstrate this ability, as shown in Fig. 3.91. Figs. 3.92a and 3.92b clearly show how the original phase settings that were used in the flat array to generate a broadside main lobe result in a scattered pattern when set here. The array is then re-focused to correct the aberrations introduced into the pattern by the shape change, and to find the optimum phases to recreate a broadside main lobe. Fig. 3.92c shows the result of the re-focusing, proving our ability to regenerate the desired pattern for a mechanically deformed array.

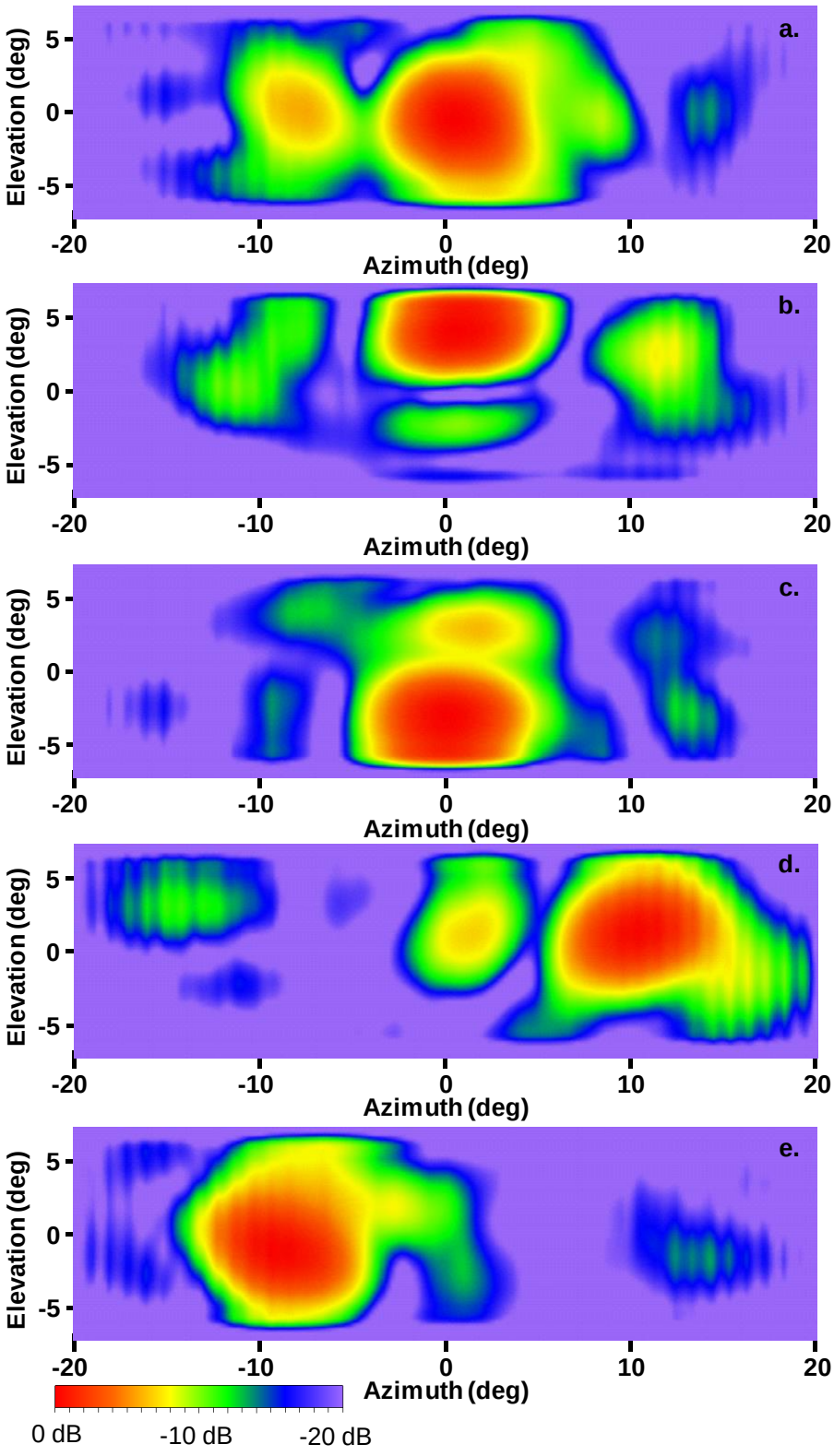


Figure 3.90: Antenna pattern of a steered phased array beam: (a) Broadside, (b) up, (c) down, (d) right, and (e) left.

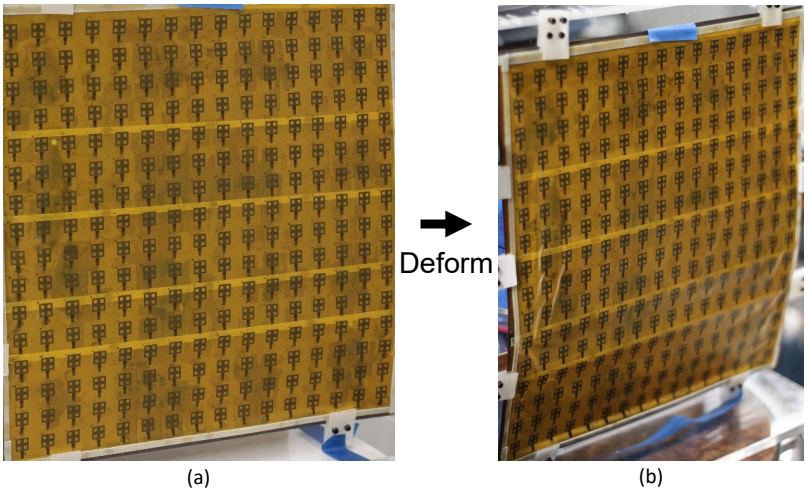


Figure 3.91: A flexible phased array transmitter: (a) flat and (b) deformed.

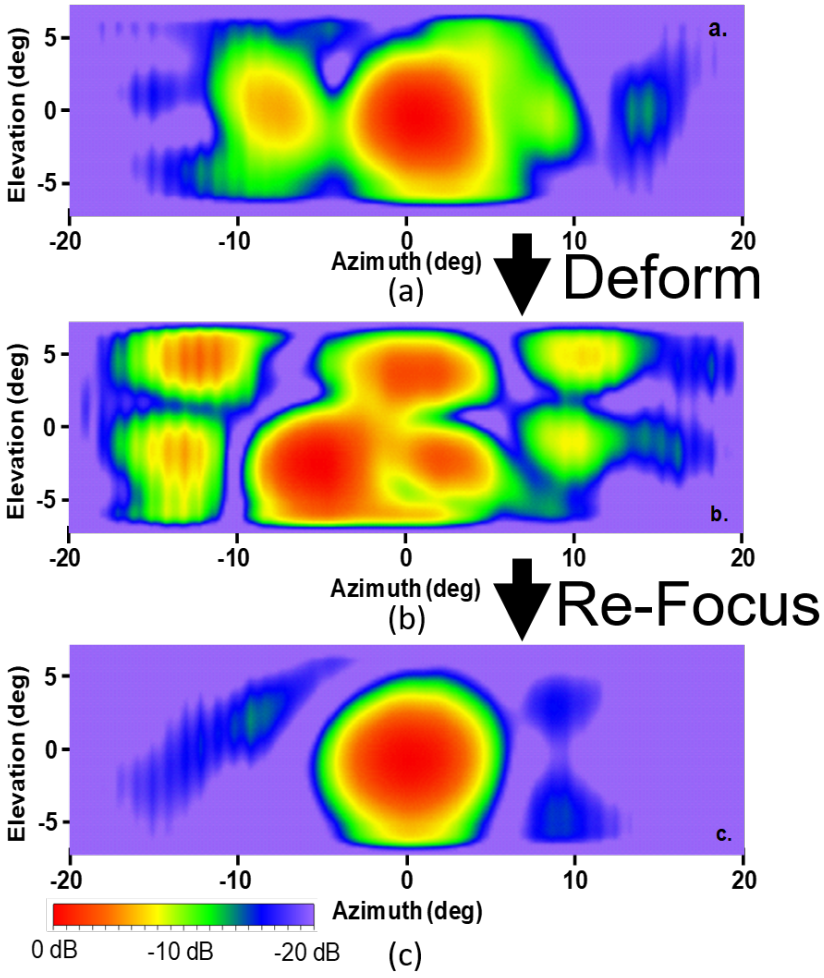


Figure 3.92: Deformation correction. (a) Focusing, (b) deformation, and (c) re-focusing of a deformed flexible phased array transmitter.

Chapter 4

SYNCHRONIZING RF PHASED ARRAYS WITH LIGHT [1]

4.1 Introduction

As active phased arrays become larger, synchronizing the operations of the the array elements becomes more challenging. Synchronization is done either directly with a reference at the output frequency, or indirectly, with a low frequency clock distributed between the RFICs which synthesize the required output signal from it. Each method has its advantages and drawbacks which make is suitable for different applications.

Direct and indirect clock distribution

Direct clock distribution is *in theory* desirable from system complexity and noise perspectives. Since no frequency multiplication is done, all the array's output chains are driven circuits, operating far above $1/f$ noise corner. As such, their noise is set by the thermal noise of the amplifier which is dependent on its bandwidth, and is usually much lower than the noise added by on-chip synthesizers. In addition, the reference phase noise is correlated between all the outputs and therefore does not manifest in the beam-steering, which depends on the phase *difference* between the elements. The array also does not suffer from PLL-related frequency pulling and locking-related instabilities. The theoretical advantages however are hampered by practical difficulties. In the GHz range, generation and distribution of high frequency clock is inefficient and signal loss increases as the array grows in size. The cost of a high frequency material might make it unsuitable for certain applications and cable weight may be prohibitive in the case of large sparse arrays that are distant from each other. In order to enjoy the noise performance of a driven circuit, the driving signal must be large enough compared to the noise floor, which requires a power-hungry clocking scheme. Lastly, implementing a complete multi-output RFIC to reduce complexity means that there may be a significant feedback from the RFICs outputs to its input, which increases the risk for undesired oscillations. For these reasons, direct distribution of clock reference is usually used in classical defense and space applications where lower efficiency, cost, and post fabrication manual tuning are tolerable, and the addition of components (discrete PAs, etc.) is acceptable.

[1] This work is done in collaboration with C. Ives and A. Khakpour.

This architecture is however unacceptable for many commercial applications, in which the economics of the system determine its feasibility. Indirect frequency distribution at a low frequency is simple at the board level and allow to implement large parts of the systems on a low-cost substrate. Frequency generation at those frequencies, usually in the order of 10s of MHz is simple and accurate through the use of quartz-crystals. The clock distribution scheme however becomes difficult with increase of array size, which unacceptably loads the clock source. This issue was thoroughly discussed in section 3.4 and calls for further inspection of additional reference distribution schemes.

4.2 Theoretical Background

Electronic clock distribution schemes

In its simplest form, an on-board trace can be modeled as a capacitive load. This approximation holds if the source is operating at a frequency with a wavelength much longer than the line. The power required to drive the line is determined by the driven voltage swing, V, the frequency of operation, f, and the total capacitance associated with the line length C

$$P_{cap} = CV^2 f. \tag{4.1}$$

Here we assume that long lines are buffered such that the low frequency assumption remains valid when the array grows larger. The capacitance per unit length can be calculated from 2.37 or numerous other sources [98]. Capacitively terminated traces can be driven by a resonant line as well. This is a less-standard design approach and though deserves detailed investigation, it will not be considered for the current comparison. A high frequency signal can drive long lines if the latter are designed as transmission lines and are terminated with a matched load. The power must be split to each element (or an IC controlling several elemenets) and the splitters themselves add some loss that usually increases with frequency. Since all the power is presumably delivered to the load, the power dissipation is determined by the required SNR at the load and the RF lines loss. For an input power of P_{chip} delivered to N RFICs, with a total line length of l to each RFIC, with loss of α_l per unit length, power dissipation associated with the distribution line is

$$P_{RF} = \frac{N \cdot P_{chip}}{l \cdot (1 - \alpha_l)}. \tag{4.2}$$

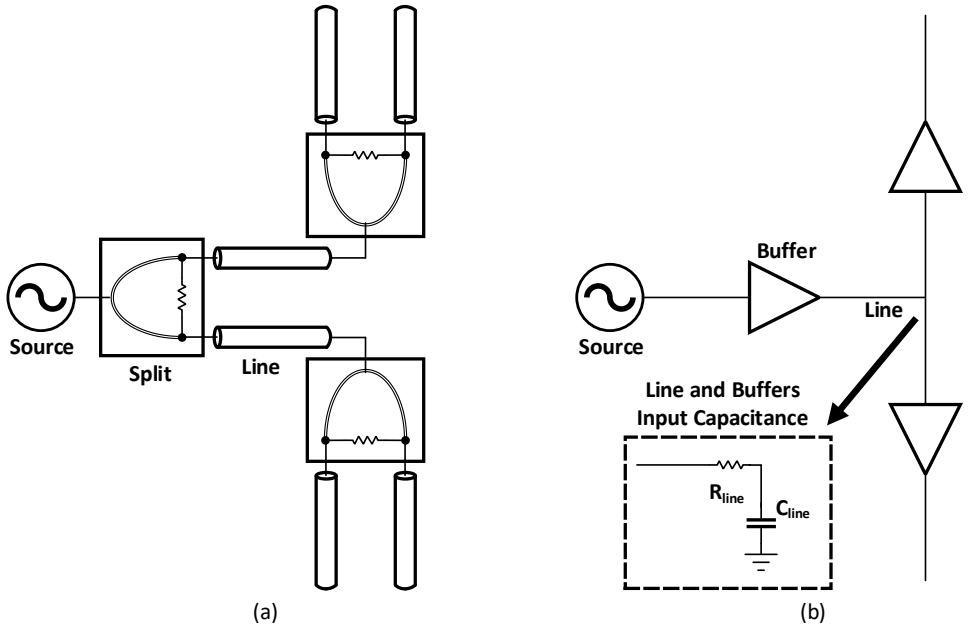


Figure 4.1: High frequency clock distribution schemes: (a) RF based and (b) laser based.

The phase noise PSD in rad^2/Hz of an amplifier with a noise figure F, due to thermal noise is defined by [99]

$$\phi^2_{PSD} = F \cdot \frac{kT}{P_{chip}}, \tag{4.3}$$

with T the environment temperature and k Boltzman's constant. The integrated phase noise in radians in a bandwidth B is

$$\phi_{RMS} = \sqrt{B \cdot \phi^2_{PSD}}, \tag{4.4}$$

or in seconds, given the signal frequency

$$t_{RMS} = \frac{1}{\phi_{RMS} \cdot f_{clock}}. \tag{4.5}$$

Fig. 4.1 illustrates the general configurations of matched and capacitively loaded distribution networks. For simplicity, we assume that both networks use an "H-tree" architecture and that the capacitive network buffers are not constrained to be in the phased array RFICs.

Optical clock distribution

Laser can be used as a clock source by incorporating a photodiode in each RFIC and using a fiber as the distribution line. The required source power in this distri-

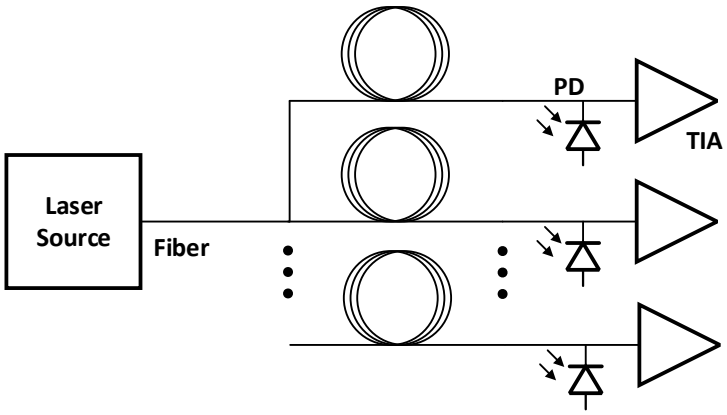


Figure 4.2: Laser clock distribution block diagram.

bution scheme is mainly determined by the power that needs to be absorbed in the photodiode in order to be converted to an electrical signal with sufficient SNR for the phased-array output chain. For an output power of P_{chip} delivered to N RFIC PD with conversion efficiency η_{PD}, the power dissipation associated with the clock distribution is

$$P_{laser} = \frac{N \cdot P_{chip}}{\eta_{PD}}. \tag{4.6}$$

It is important to note that for the same SNR, the required P_{chip} might be significantly higher than an electrical RF signal due to the PD efficiency. However, the loss associated with an optic fiber is negligible over very large distances, so a scaling limit exists where it is beneficial over RF power distribution. In addition, the cost of a high-performance PCB substrate may be prohibitive for the latter in large-scale commercial applications. Fig. 4.2 illustrated the optical reference distribution concept and its loss sources.

Performance comparison

Fig. 4.3 compares the three reference distribution methods in terms of estimated power dissipation versus the number of driven ICs, for a given noise performance. In order to do so, we make several simplifying but realistic assumptions regarding the other design variables. We want to draw conclusions for an SSP system, operated at f_{RF}=10GHz, but also for 5G applications around f_{RF}=28GHz. The low-frequency signal is assumed at a frequency of 50MHz. Each IC is assumed to drive 4 dual polarized antennas $\lambda/2$ apart. Both RF and optical sources will be assumed at a frequency of $f_{RF}/2$. Reasoning for this design choice is given in the conclusions of this section. The distribution line will be assumed as an H-tree for all the

schemes, designed on an FR-4 board with ϵ_r=4.5 or Rogers RO4350B with ϵ_r=3.5 for a capacitive or a matched load, respectively. The requirement for integrated phase noise will be 100fs in order to be competitive with recent state-of-the-art works. Since all those circuits use an indirect reference, they all require an output synthesizer. Recently, numerous PLLs were demonstrated around these frequencies with various reference sources, all achieving roughly 60fs of integrated phase noise [100]–[102]. The Synthesizer contribution is therefore assumed similar and is neglected for comparison purposes. Both a PD with a TIA and an RF LNA will be treated as tuned amplifiers with a noise figure of roughly 6dB and bandwidth of about 5%. Both assumptions are reasonable for a few stages of tuned amplifiers at this frequency. There are two length quantities that need to be calculated to estimate the clock power dissipation for the various methods, as shown in Fig. 4.4: the total length of traces in an H-tree, and the trace length from the clock source to a single chip. For a scale factor $N = 1, 2...$, the number of chips in the array is $N_{RFIC} = 4^N$and the number of chips per array side is $N_{side} = 2^N$. For 2×2 antennas per chip, there is a distance of λ between chips and a total side size of $d = \lambda N_{side}$. The trace length to each RFIC grows with N as

$$l_{RFIC} = \frac{d}{2} + \frac{d}{4} + ... + \frac{d}{2^N} = d \sum_{n=1}^{N} \frac{1}{2^n}. \tag{4.7}$$

Summing and substituting d gives

$$l_{RFIC} = d \cdot \left(1 - \frac{1}{2^N}\right) = (2^N - 1)\lambda. \tag{4.8}$$

The total trace length grows with the array size as

$$l_{tot} = \frac{d}{2} \cdot 3 + \frac{d}{2} \cdot \frac{1}{2} \cdot 3 \cdot 4 + \frac{d}{2} \cdot \frac{1}{2^2} \cdot 3 \cdot 4^2 + ... + \frac{d}{2} \cdot \frac{1}{2^{N-1}} \cdot 3 \cdot 4^{N-1}. \tag{4.9}$$

Summing and substituting d gives

$$l_{tot} = 3d \sum_{n=1}^{N} 2^{n-2} = 2^{N-1}(2^N - 1) \cdot 3\lambda. \tag{4.10}$$

Table 4.1 shows the calculated variables for each of the reference distribution option as well as the size scale for which using an optical reference becomes more efficient than an RF reference.

A few conclusions could be drawn from this power estimate calculation. Notably, with a low frequency reference, the capacitively loaded scheme is by far the most

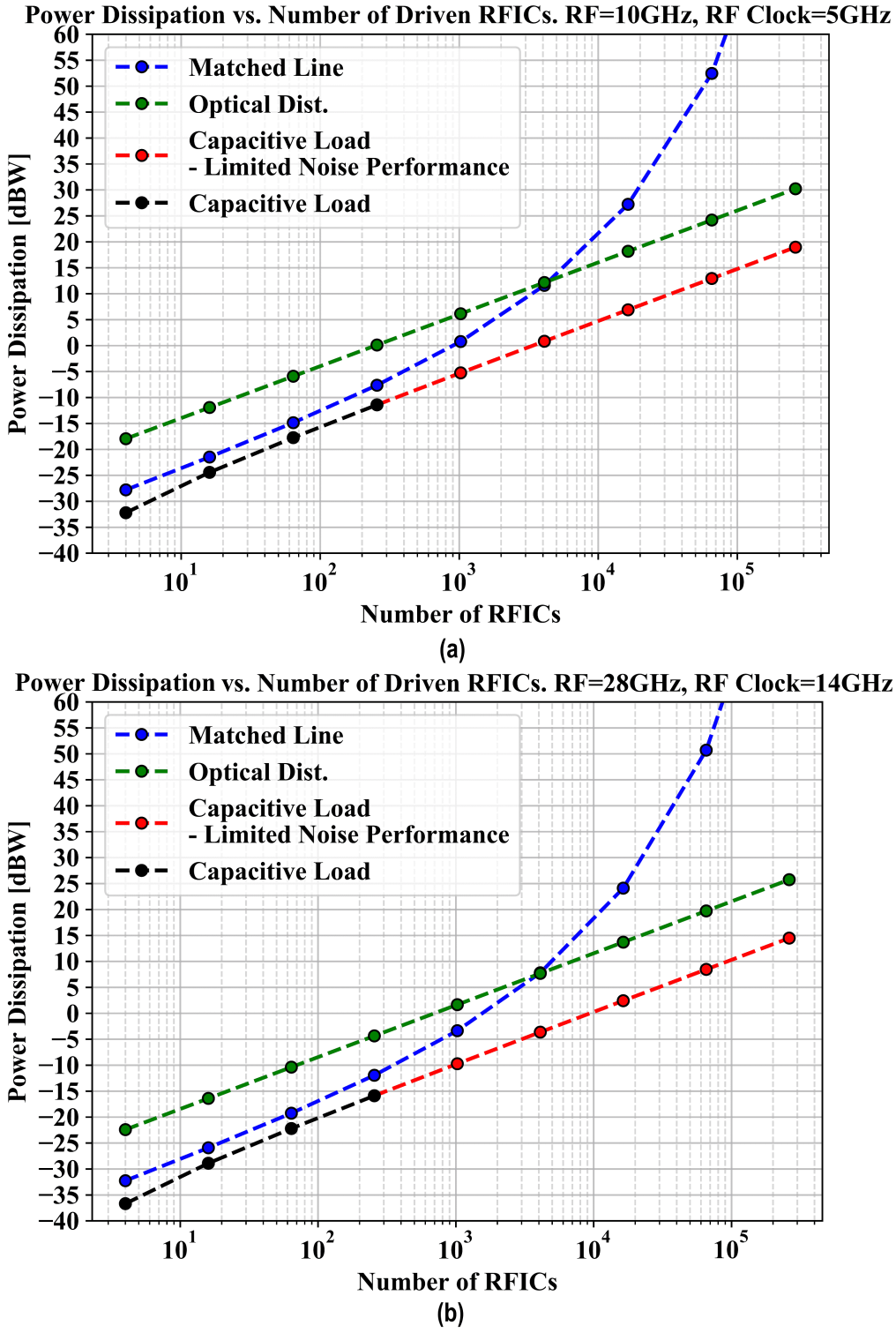


Figure 4.3: Comparison of distribution network power loss for different distribution schemes at (a) 28GHz and (b) 10GHz.

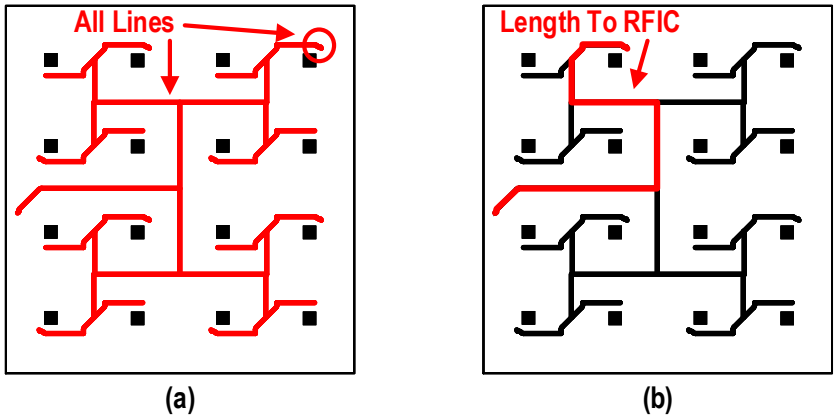


Figure 4.4: Counting the (a) total length of reference distribution lines and (b) distance from centralized source to a single IC.

Table 4.1: Calculated quantities of reference distribution power dissipation.

Quantity	Value 28GHz	Value 10GHz
Reference Frequency [GHz]	14	5
Wavelength [cm]	1.07	3
P_{chip} [dBm]	-8.4	-3.9
Required PN at IC [dBc]	-129.5	-134
RO4350B loss [dB/cm]	0.15	0.05
Antennas @ equal power	16,400	17,600
Side length @ equal power [cm]	68	200

efficient in terms of power dissipation. However, this comes at the expense of added noise, as shown in (3.23). In fact, for very low-noise applications like high throughput 5G communications, the noise added by even 3 stages of low noise buffer with integrated jitter of 50fs can exceed the specifications. RF power distribution is more efficient than its optical counterpart at small scale due to fairly low PD efficiencies on silicon. At a larger scale, optical reference distribution prevails because its power dissipation grows like 2^N, the number of RFICs, while the RF power dissipation grows like 2^{2N} due to the line loss. In terms of cost, high performance RF material is one- to two- orders of magnitude more expensive than low cost FR4 and optic fibers, so it might be unsuitable for high volume commercial applications. There is another subtlety that is crucial to the understanding why an optical reference distribution is desirable. One way to significantly reduce the RFICs' added phase noise is to use low multiplication ratio synthesizers. This allows for a high bandwidth of VCO noise rejection, and the noise of the source is

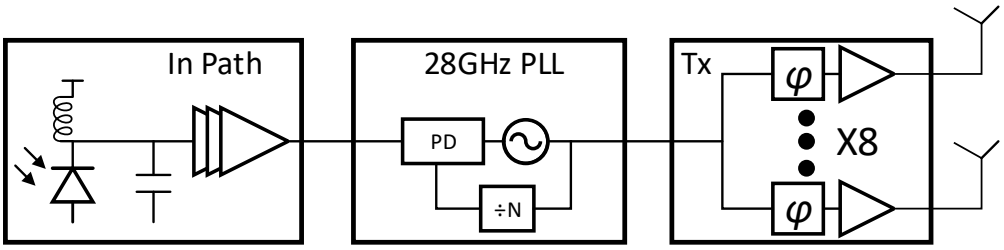


Figure 4.5: Optical reference chip top block diagram.

correlated between all the ICs so it does not contribute to the output phase error. The higher the reference frequency, the higher the loss in the PCB transmission line, and using an optical scheme is more favorable. Another consideration in favor of optical reference distribution is in other architectures where array elements are distant from each other. Examples are sparse arrays with large separations between the array parts, coherent combination of distanced phased arrays, and synchronization between distant parts of large sensor networks, for which cable loss, size, or weight is unfeasible.

4.3 Chip Design

In order to demonstrate an optical reference distribution system, we designed a fully integrated optically driven, 8-channel phased array transmitter RFIC. It is fabricated in a 65nm bulk-CMOS process and has three distinct parts as illustrated in Fig. 4.5. Despite the fact that the smaller the multiplication ratio the better noise performance we get, we chose for demonstration purposes a reference frequency of 3.5GHz with a multiplication ratio of $\times 8$ to 28GHz, to be able to implement a robust PLL that will not risk the complete system.

Input stage design

To take full advantage of CMOS integration, we implemented a photodiode on the fabricated ICs. While this allows to interface a photodetector on-chip without any additional process modification, the silicon band gap forces the system to use (mostly) visible wavelengths. The design of visible-light PDs is popular in home networks [103], vehicular [104], and visible light communications [105], and the design tradeoffs are well-understood [106]. A PD circuit model is illustrated in Fig. 4.6 with the following technology dependent elements:

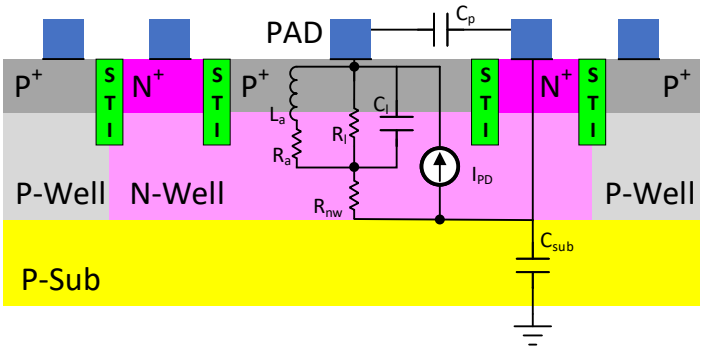


Figure 4.6: Small signal model of a CMOS PD (recreated from [106]).

- C_p, The parasitic capacitance between N^+ and P^+ electrodes
- L_a, Accounts for the phase delay between voltage and current due to ionization
- R_a, Accounts for the finite reverse saturation current and the field dependent velocity
- R_l, C_l, The capacitance and resistance of the depletion region
- R_{nw}, The N-well resistance
- C_{sub}, The N-well/P-sub junction capacitance.

We are using a 3-finger, N^+/P-well, with a shallow trench isolation (STI) guard ring and a deep N-well (DNW) isolation. The design process started with an estimate of the technology layer structure and doping (Fig. 4.7), and was followed by layout construction and simulation in a dedicated software tool [107] to estimate the PD current versus input power, and the parasitic frequency dependent response which expresses mainly as shunt capacitance. Fig. 4.8a,b shows the simulation results and Fig. 4.9 shows the PD final layout. The photodiode size is 45μm $\times$ 45μm with an equivalent capacitance of about 500 fF which can be easily tuned on-chip, and a large enough cross section, to interface with an external fiber. The PD responsivity is estimated from Fig. 4.8b. An initial estimate of input power that will guarantee the proper operation of a 100μm $\times$ 100μm PD was 100 W/cm^2. For the simulation parameters of Fig. 4.8b, this is equivalent to an input power of 169 μW. The output current is 10 μA and therefore the expected output current is 60 mA/W. Contrary to standard serial optical links, a reference clock operates at a single frequency. This opens the design space to the use of narrow-band amplifiers to work with a given PD at higher frequency than dictated by its output capacitance, or a wide-band TIA

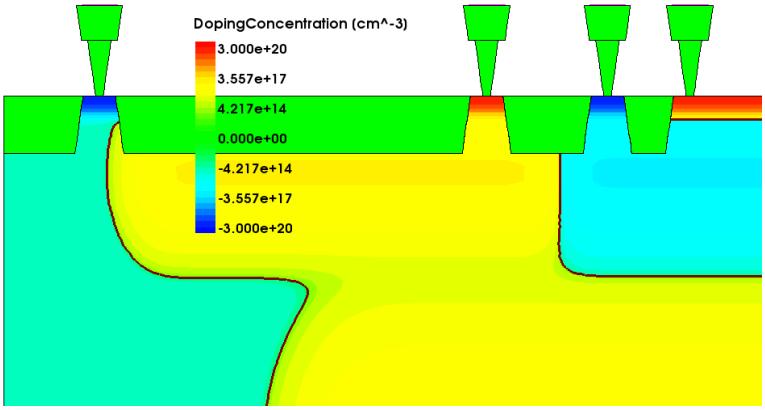


Figure 4.7: A cross section of doping concentrations for PD design (Fig. courtesy of C. Ives).

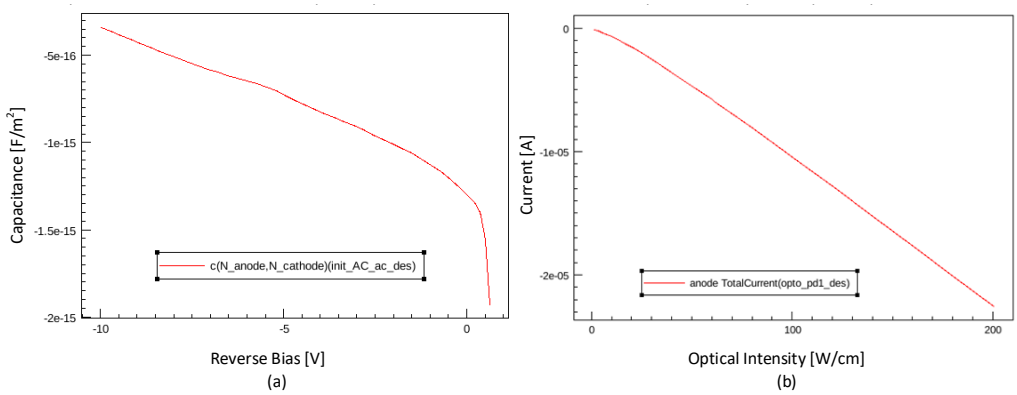


Figure 4.8: Photodiode (a) capacitance density and (a) responsivity simulations (Figs. courtesy of C. Ives).

bandwidth. The input chain is shown in Fig. 4.10. The PD parasitic capacitance is resonated with an inductor at its cathode, and a digitally selectable capacitor bank is used to ensure that the input is tuned to the desired frequency of 7GHz. A common-source differential amplifier is used as the first stage of the TIA-LNA to minimize the integrated noise at the input chain bandwidth. It is followed by two inverter-based amplifiers and a digital divider to bring the input to a rail-to-rail swing with a frequency of 3.5GHz as required by the integrated PLL. The input LNA is employing a negative-g_m cell in parallel with the amplifier tank to artificially boost its gain as shown in Fig. 4.11. The subsequent stages use a common-mode feedback amplifier to ensure the operating point of the inverters (Fig. 4.12). The simulated single-ended output voltage of the chip input chain is illustrated in Fig. 4.13 showing that, with the expected input power, the PLL output is almost at its 1V rail.

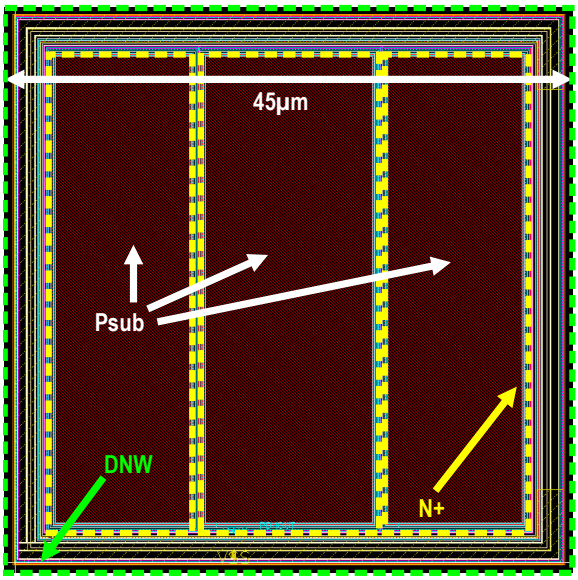


Figure 4.9: Photodiode layout.

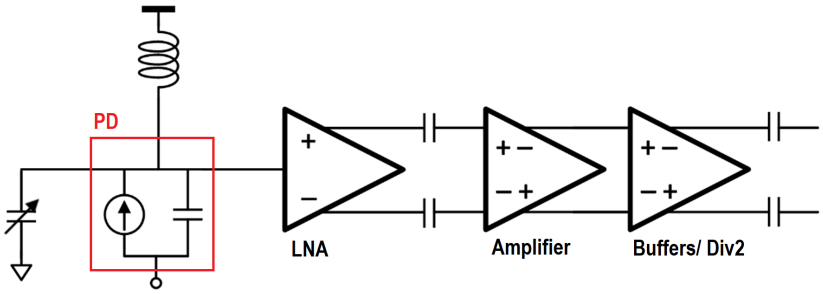


Figure 4.10: Input chain schematics (Fig. courtesy of C. Ives)

PLL design

As mentioned before, a low multiplication ratio PLL allows to synthesize a signal with a large bandwidth and low integrated jitter. The PLL loop filter bandwidth should not be more than 1/10, preferably 1/20 of the reference frequency [108]. In contrast, a small PLL bandwidth will better reject the input reference noise that is introduced by the TIA-LNA. Here we implement a PLL with a loop bandwidth of 50MHz as a tradeoff between the two. The PLL block level is illustrated in Fig. 4.14. Due to the high output frequency, the first division is done with an injection locked frequency divider (ILFD). Subsequent stages are a CML divider and a TSPC divider, as illustrated in Fig. 4.15. The control voltage of the ILFD is connected to the PLL control voltage in order to increase its lock range. It is matched to the VCO's frequency tuning as shown in Fig. 4.17. After that, a current-mode logic

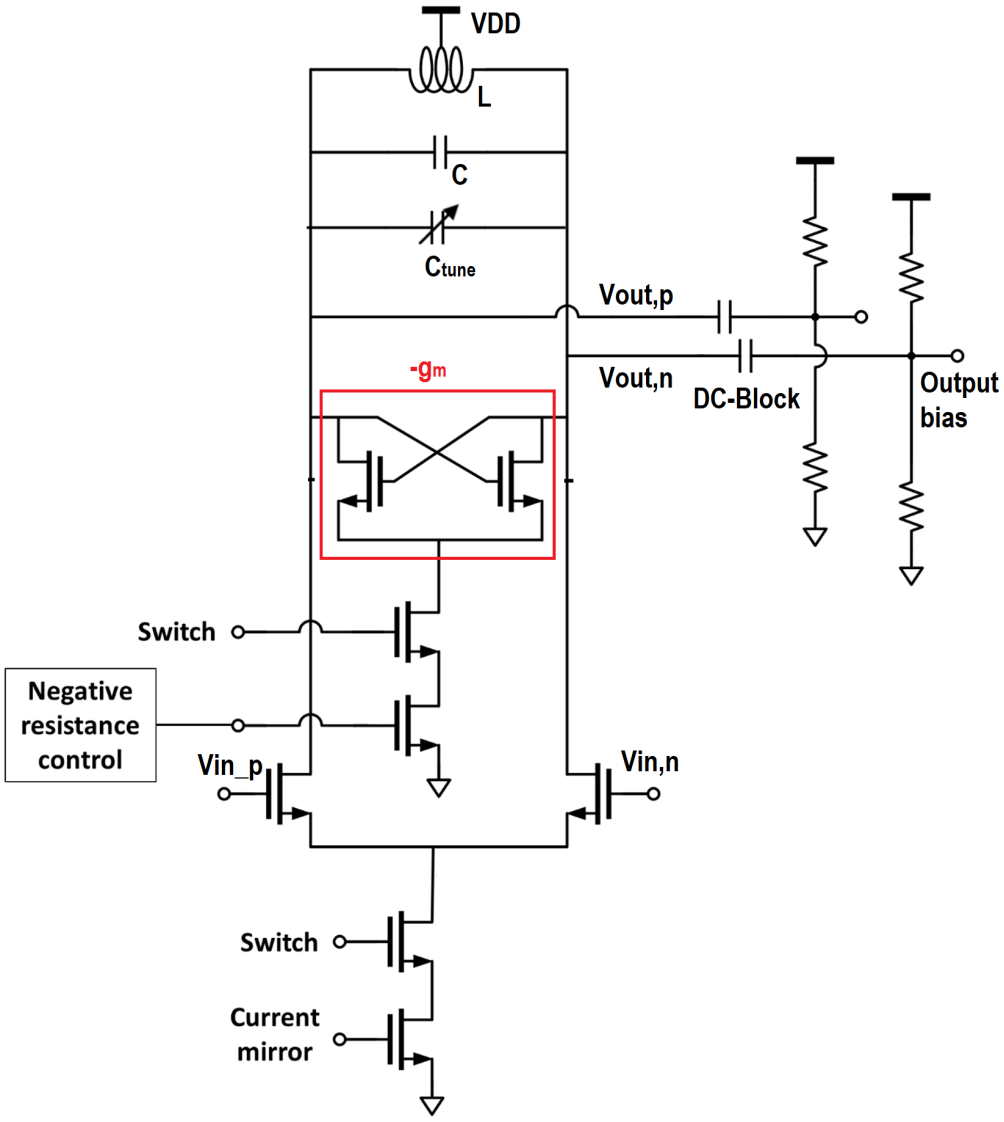


Figure 4.11: PD LNA with a gain-boost $-g_m$ cell (Fig. courtesy of C. Ives).

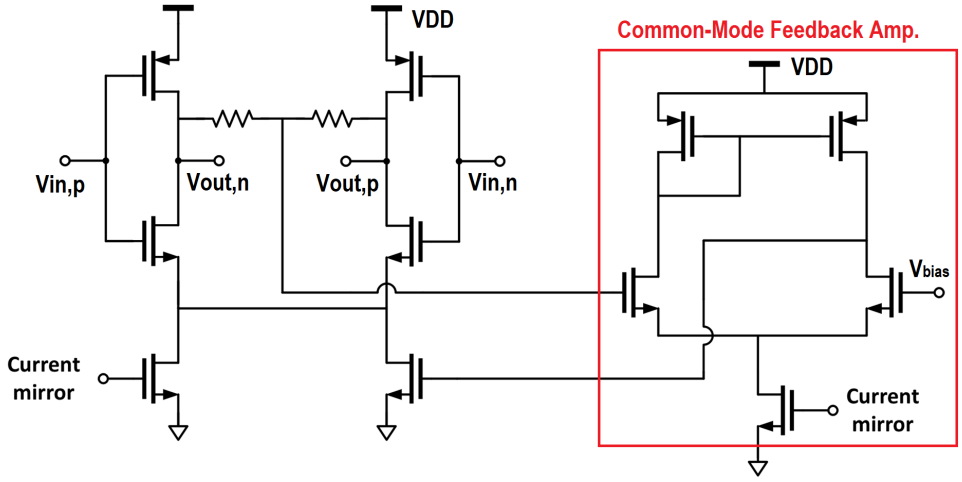


Figure 4.12: A common-mode stabilized inverter amplifier (Fig. courtesy of C. Ives).

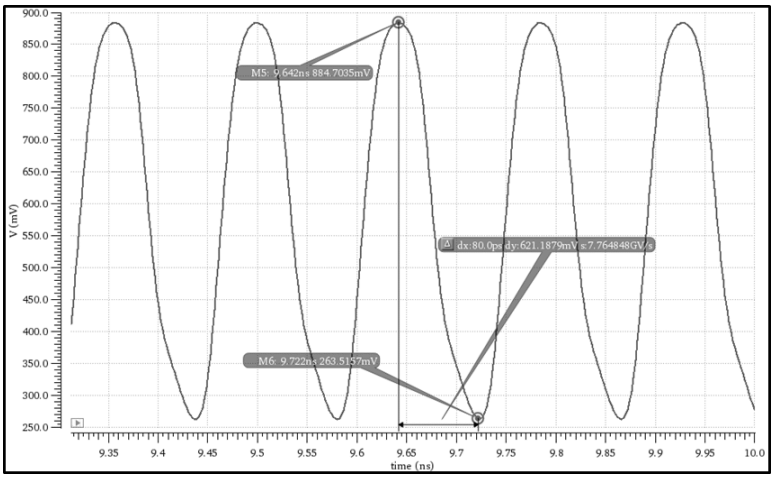


Figure 4.13: Transient simulation of the input chain's output (Fig. courtesy of C. Ives).

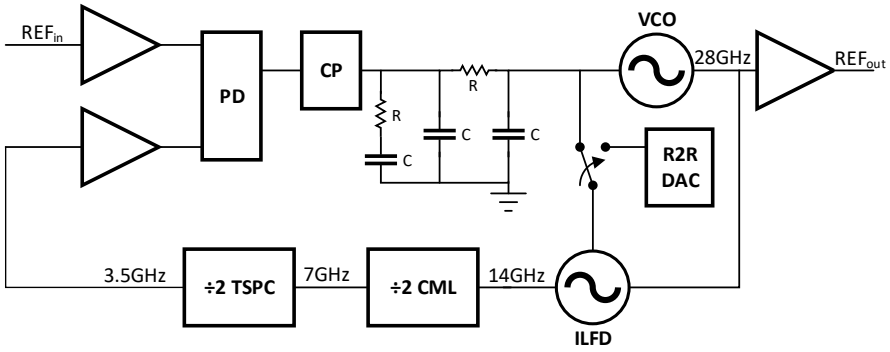


Figure 4.14: An ×8, 3.5 GHz to 28 GHz PLL schematic

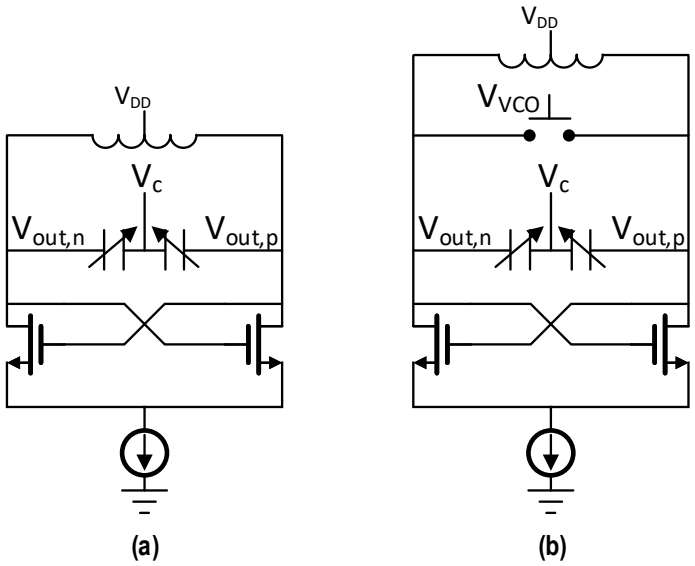


Figure 4.15: VCO and ILFD schematics.

(CML) and a true single-phase clock (TSPC) dividers, as shown in Fig. 4.16 are sufficiently fast. The PLL estimated noise and loop stability are shown in Fig. 4.18, demonstrating estimated performance on-par with current state-of-the-art.

Tx chain design

The Tx output chains consist of a vector modulator phase-shifter and an output PA. Fig. 4.19 shows a simplified vector modulator schematics. The polyphase filter used is single stage RC filter [109] since its loss is sufficiently low and its bandwidth is sufficiently large. The vector modulator provides sufficient gain and output swing to drive the PA and is designed to provide a 6-bit phase steering accuracy. Fig 4.19 shows the achievable phase shift on a constant gain circle. The power amplifier is an overdriven linear amplifier with a series inductance added at the drain of the output stage to better align its voltage and current waveforms. While more sophisticated topologies exist [110], this amplifier is robust with a reasonable output power and drain efficincy (12.5dBm and 28%, respectively), and allows to be operated at backoff should we want to demonstrate a nonuniform phased array operation as well. Fig. 4.21 illustrates the power amplifier schematics and Fig. 4.22 shows the simulated output swing and small signal gain.

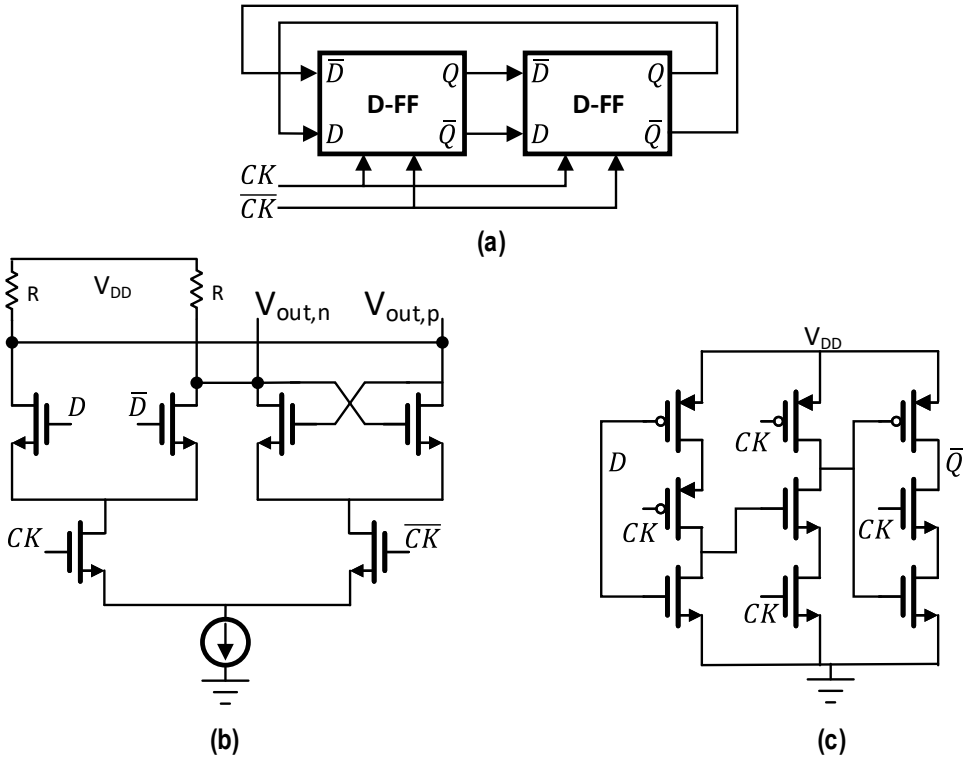


Figure 4.16: PLL intermediate and last stage divide-by-2 circuits. (a) A general structure of a differential frequency divider, (b) CML logic for 14 GHz to 7 GHz division, and (c) TSPC logic for 7 GHz to 3.5 GHz division.

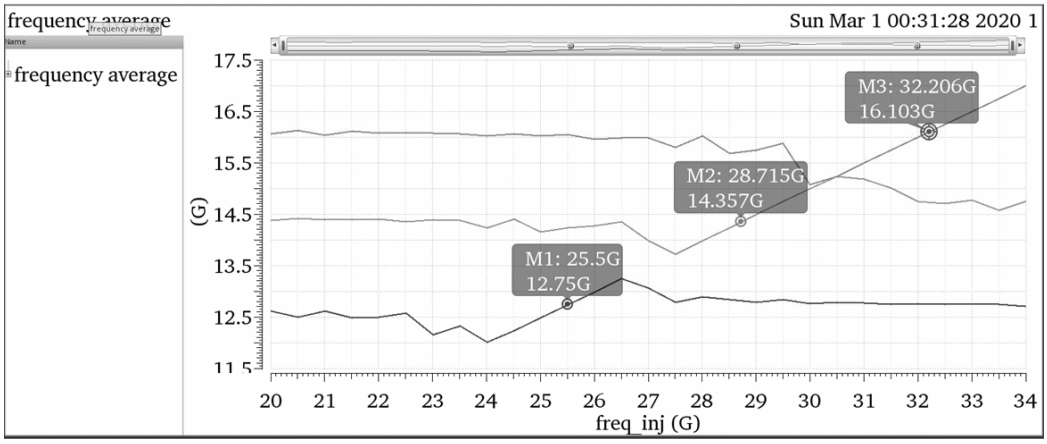


Figure 4.17: PLL ILFD lock range alignment with the VCO control voltage.

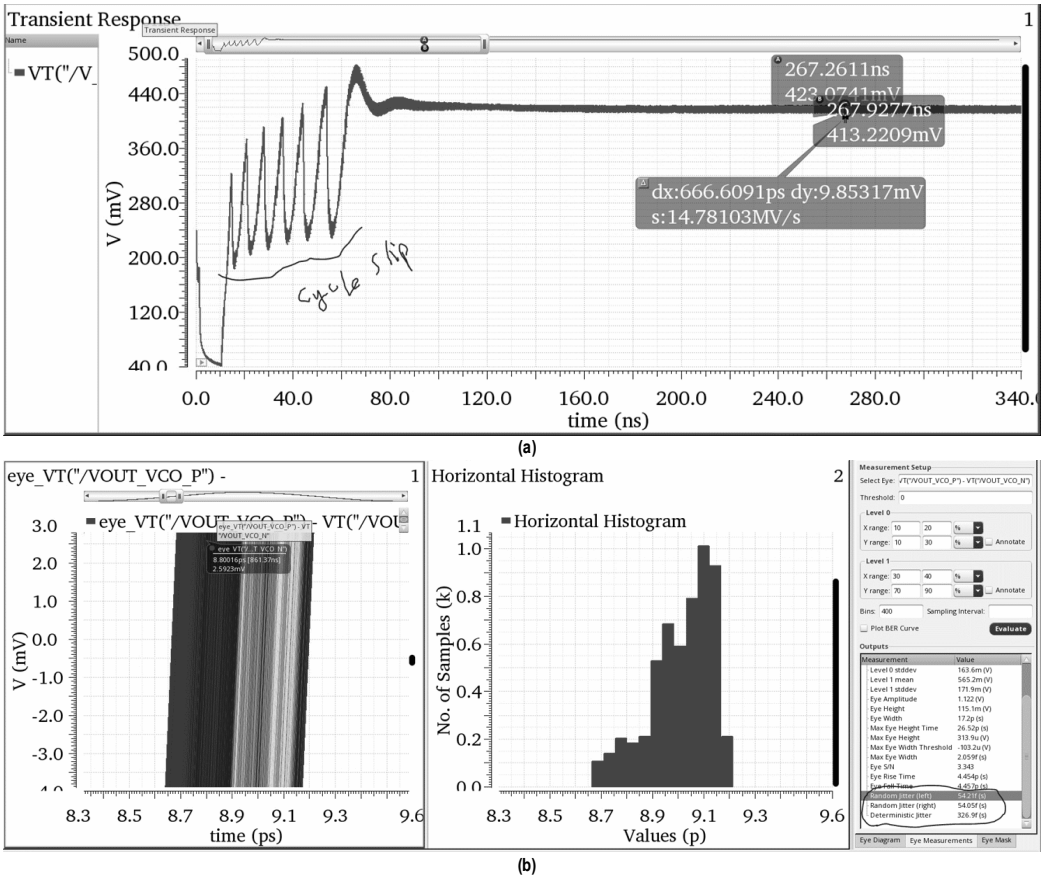


Figure 4.18: 28GHz PLL simulation of (a) transient VCO control voltage and (b) transient jitter. Estimated jitter is ≈ 60 fs.

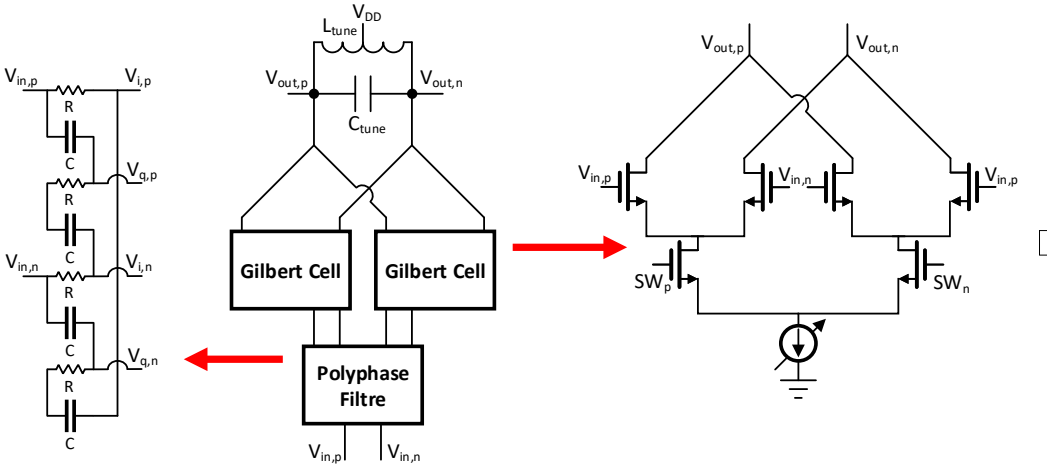


Figure 4.19: Output channel vector modulator phase shifter schematic.

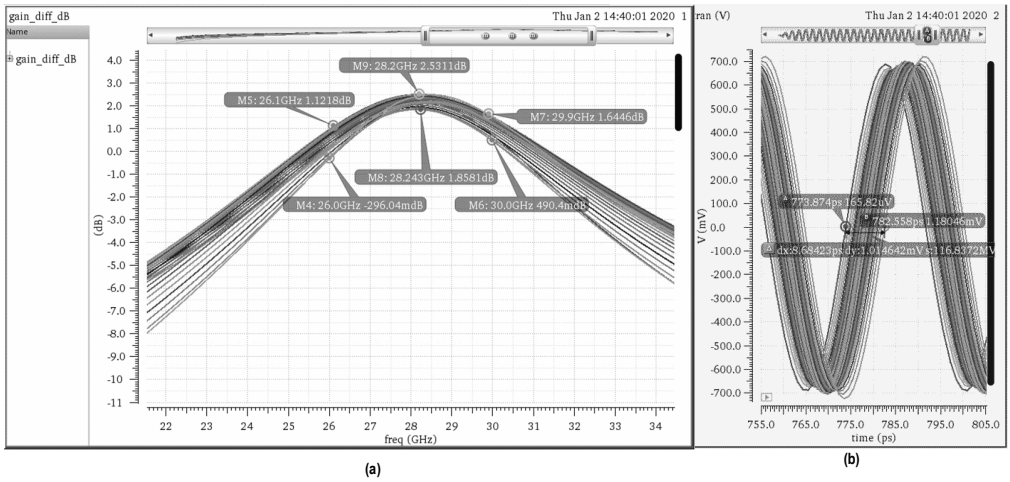


Figure 4.20: Vector modulator phase shifter. (a) Small signal gain and (b) transient phase shift simulations.

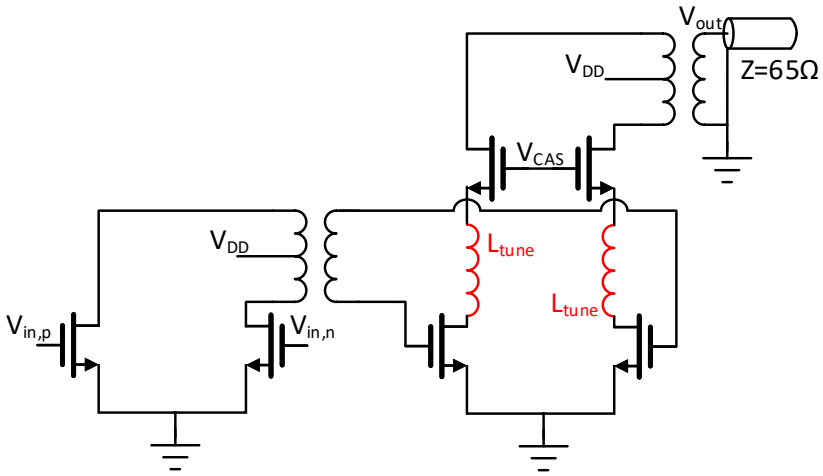
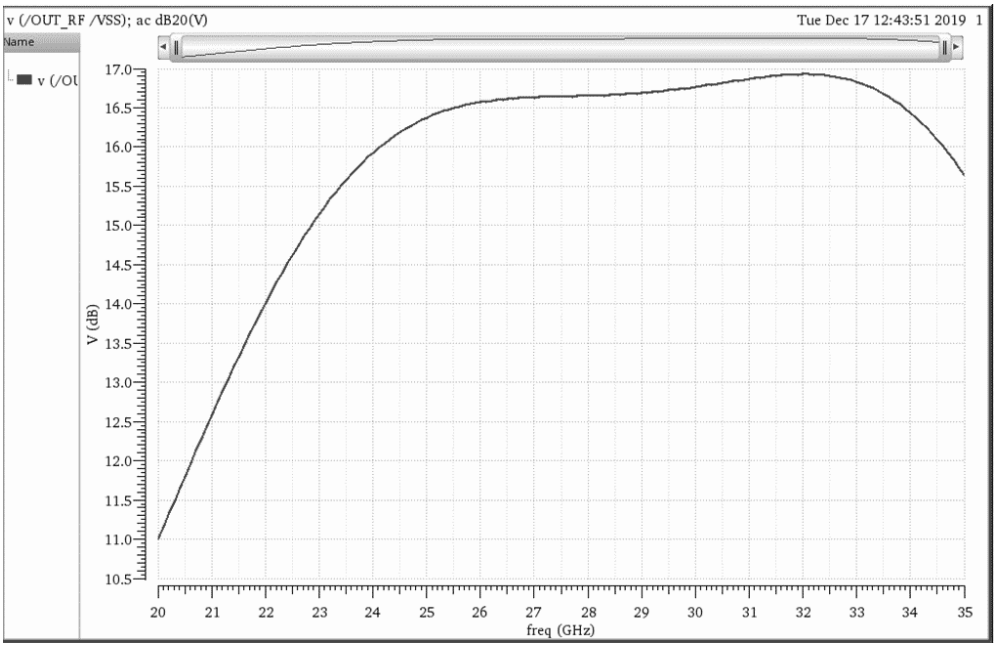
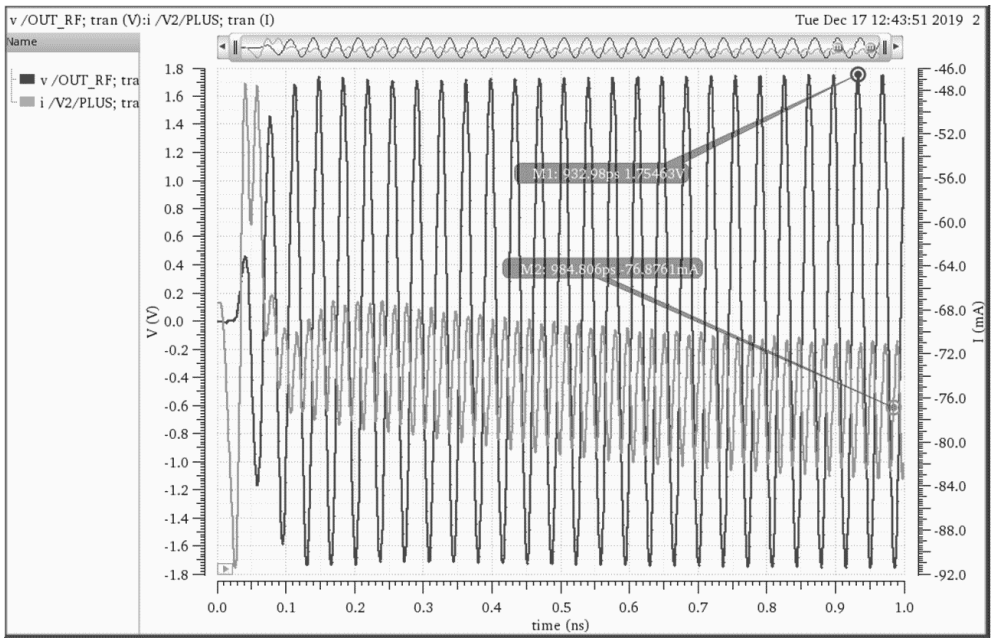


Figure 4.21: Power amplifier output schematic.



(a)



(b)

Figure 4.22: Output power amplifier. (a) Small signal gain simulation and (b) transient supply and RF output swing simulation.

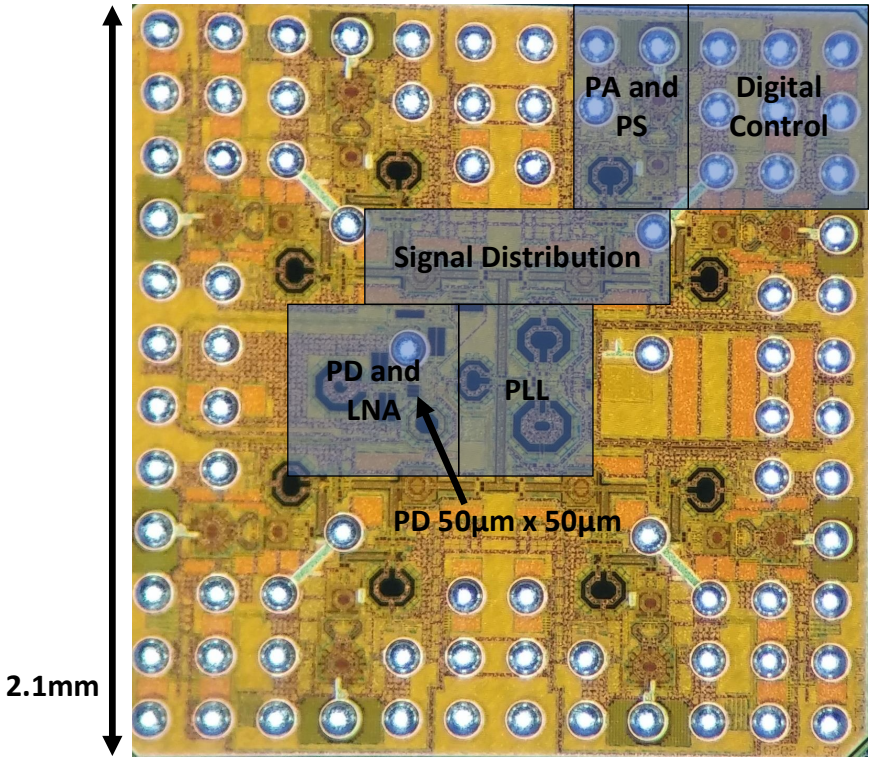


Figure 4.23: Optical reference distribution chip die photo.

Project status

The optically driven phased array chip was fabricated and its die photo is illustrated in Fig. 4.23. It currently awaits to be measured and characterized in the lab.

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