Suspended Trace Air-gap Resonators for Low Loss Superconducting Circuits

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ABSTRACT

Quantum memories and networks for distributed quantum information processing require links between the microwave, mechanical, and optical domains. Coherent integration of long-lived superconducting qubits (SCQs) with optomechanical and photonic devices (OMPDs) remains an outstanding challenge. We present a step towards coherent integration using a suspended trace air-gap resonator (STAR): a superconducting resonator on a silicon-on-insulator (SOI) substrate with the signal trace suspended by silicon tethers above and between galvanically connected ground metal planes. As a result, the electric field energy is closely confined within the microwave structure, yielding lower crosstalk compared to conventional coplanar waveguides (CPW). An order of magnitude improvement in the quality factors for STAR over previous work on SOI is achieved, in a transverse cross-sectional area that is an order of magnitude more compact. Electric field participation in lossy bulk dielectrics, a dominant source of energy leakage in previous measurements of aluminum CPW resonators on SOI, is virtually eliminated in STAR. The loss from the metal-air interface now dominates, but can be reduced by several factors using superconductors with better surface properties. Most importantly, STAR fabrication is compatible with Josephson junction and air-bridge deposition for highly coherent integration of SCQs and OMPDs to realize proposals for quantum information storage and networking.

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[8] https://commons.wikimedia.org/w/index.php?curid=20296340 Schematic by Telemark. Diagram by Jatosado Power Point, CC BY-SA 3.0.

Diagram was taken to be supplemented and annotated in order to describe the deposition process of the tool.

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Chapter 1

INTRODUCTION

1.1 Quantum Computation

For the last century, technological advantage has served as a tool to give nations access to unfathomable resources in weaponry, energy, and computing [4]. In the last decade, technologies for quantum computing and networking have been brought out from academic efforts to the front stage of private research areas of many high tech firms [2]. The quantum technology arms race for processing power will enable unprecedented computational speedup for specific and optimized problem sets [80][35]. Information encoded in the superposition and entanglement of quantum mechanical states scales exponentially with the number of interactable quantum bits (qubits). Fortunately, the exponentially large nature of a quantum computer's parameter space (known as the Hilbert space), if well designed, has a respective logarithmic number of control knobs. We have the potential to perform massive parallel compute on optimized problems using this technology. Possible applications include: machine learning and optimization [34][90][69][108][13], quantum simulation of interacting atom atom molecules [23][95][17][101][57], and other more specific problems such as key generation/verification and prime factorization [78][109][1][91].

At the moment, a general purpose platform for quantum computing does not exist. Trapped ion systems boast extremely long lifetimes and addressability [19], but lack a clear path towards scalability. Photonic systems promise a simpler path to scaling [94], but lack a deterministic photon generator. Other systems are also unproven or in their infancy. Superconducting circuits is a popular platform for many reasons [52], such as commercially available microwave frequency system components, finite element analysis software suites, pattern layout software, and device fabrication tools. Off the shelf 16-bit microwave frequency waveform generators, passive filters, power amplifiers, and signal processing analyzers allow for nanosecond temporal control and measurement of interrogation tones. Material characterization and knowledge of superconducting physics allows electromagnetic solvers to design complex geometries and optimize device performance. Sophisticated modeling of complex

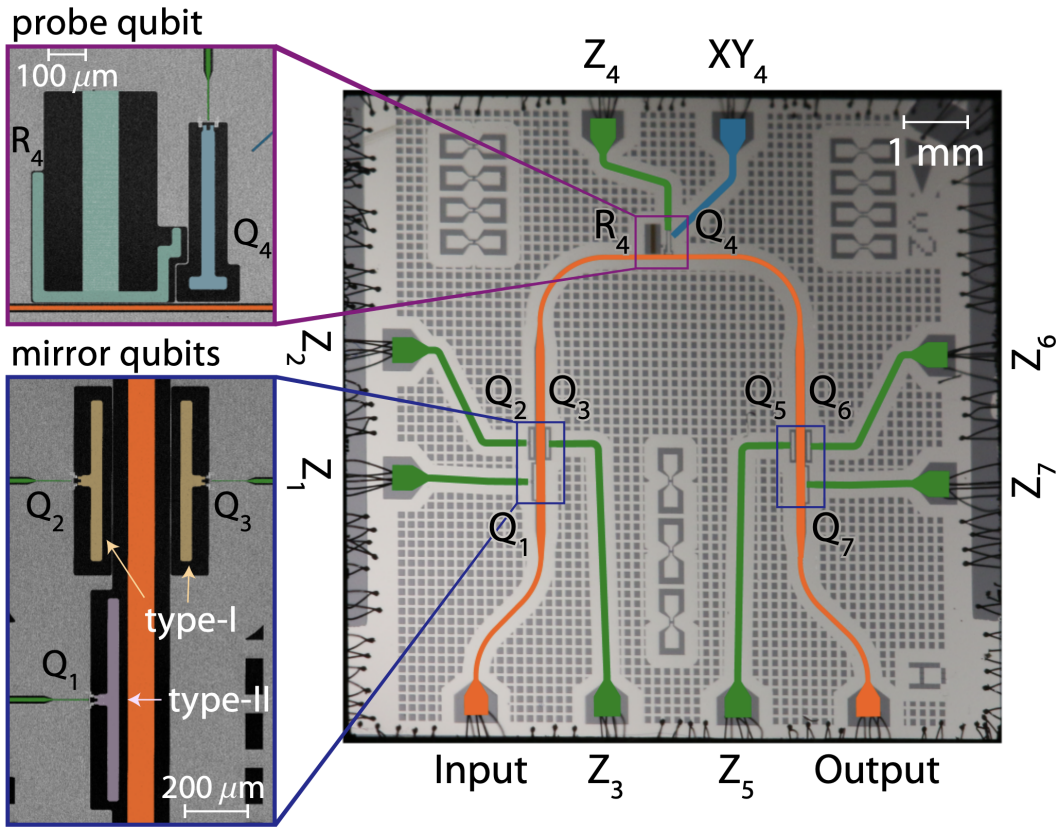

Figure 1.1: An example of a superconducting circuit device used to study interactions of atom-like mirrors along a microwave waveguide. Adapted from [68].

planar geometries allows for precise systems engineering. Automated CAD layout with design rule checking enables error free pattern transfer and CMOS compatible fabrication processing of largely micron scale features. As such, existing technology has enabled the use of microfabrication tools - an example design is shown in Figure 1.1. CMOS compatibility also allows the integration of other technologies such as optomechanical devices, which can provide more degrees of freedom in other domains to better encode quantum information. These features will be leveraged in this work to further improve system performance, but a number of challenges still remain to build a quantum computer scaled for practicality.

1.2 Challenges in Superconducting Circuits

The major outstanding challenges of superconducting circuits can be categorized into three main categories: scaling, connectivity, and loss. Scaling has been, and will continue to be a pressing issue for building a large scale system practical enough to solve generalizable and complex problems more efficiently than classical methods

at a correctable error threshold. Connectivity is a challenge that has not been fully addressed, with many architectures limited to either nearest neighbor coupling [2], or a repeated fully connected subset of some larger graph [82]. Although universal quantum computing is possible in graphs that are not fully connected, the price one must pay is algorithmic overhead through a process that involves a series state swaps across physical qubits. Finally, superconducting circuits are susceptible to energy decay and decoherence through multiple loss mechanisms. Current coherence times best 100 microseconds, but with gate times around tens of nanoseconds, only about 5×10^3 gates can be performed before these loss mechanisms introduce uncorrectable errors in our algorithm. Although many error correction schemes have been proposed, many of them rely on a very large number of qubits with high gate fidelity, a complicated graph with a high level of connectivity, and highly coherent qubits that are long lived.

In the context of superconducting qubits, the scalability of a quantum architecture can be described as the ability to increase the quantity of a critical resource without sacrificing quality. For example, a qubit architecture may claim to be scalable because one could in principle layout millions of physical qubits on a die. However, without control wiring and control electronics integrated into the hardware abstraction layer, this approach is hardly practical or economical [16]. The heat load of the added wiring and the cost of additional control lines using conventional electronics makes scaling infeasible [53]. Increasing the number of qubits on a die also sacrifices the isolation of each unit cell, creating crosstalk and the need for more complicated control and calibration schemes.

Crosstalk is an ever-present issue in very large and complicated integrated systems, and it is no different with superconducting qubits. The binary nature of information processing in semiconductor circuits cannot be extended to superconducting circuits, because the pertinent information of the quantum state is encoded in an analog form. The quantum state becomes binary in nature only when we measure and collapse the wave function of the qubit. Thus, the propagation of errors may not be immediately obvious if there are correlated errors, or errors that are chaotic, i.e. such errors spread through parameter space very quickly despite a small shift in the state vector. The issue of crosstalk could come from many different mechanisms. The most apparent mechanism, due to large planar capacitor geometries in transmon based superconducting qubits, is parasitic capacitive crosstalk. Overlapping electric

field lines in the vicinity of closely packed features mediate cross capacitance, and arises as a qubit-qubit coupling term in the system Hamiltonian. Electrical crosstalk can be easily reduced between neighboring qubits if a geometry can be realized to screen far reaching electric fields. Magnetic crosstalk can also be an issue, if the superconducting qubit relies on magnetic flux for frequency tuning or control. Any control wiring that generates magnetic fields could yield some level of crosstalk across the device, due to wide ranging field lines.

Reducing crosstalk with magnetic fields is much more challenging than electric fields. As a first step, we would want to think about addressing crosstalk with electric fields. The best way to screen electric fields is to surround signal lines or an object of interest with a Faraday cage. The best example of this that we see day to day is a coaxial cable, which has a transverse electromagnetic mode of propagation. The signal carrying lines are at the center geometry of the cylinder, with the outer conductor or the shield of a coaxial cable serving as ground. If this geometry is realized on superconducting devices, we would be able to leverage the coax cable's low crosstalk characteristics and enable high density control wiring. Ultimately, simpler control of what could be hundreds to thousands of physical qubits could be achieved.

Connectivity governs the amount of algorithmic overhead needed to perform computation. Current state of the art techniques use a central bus to mediate coupling or nearest neighbor interactions between qubits. The path for bus mediated coupled qubits is not clear, especially for future proposals for error corrected algorithms. Nearest neighbor tiling aspires to fit the surface code implementation of error correction. By measuring correlated errors, one can infer where the error occurred indestructibly, and feedback corrections needed during computation. For near term applications of quantum circuits, noisy intermediate scale qubits (NISQ) [80] can address a certain class of problems that can be solved using qubits without error correction. Another area of interest for NISQ devices is quantum simulation. Quantum simulation is analogous to the analog approach of computing, whereby operations of infinitesimally small rotations can be performed instead of the rigid gate based circuit implementation. Some applications of analog based computing are molecular systems [98], and very specific quantum problems, such as spins in a lattice [84], or even more exotic physics like circuits that break time reversal symmetry [85].

In these quantum algorithms, the level of connectivity will dictate the complexity of simulations and overhead requirements. For example, when simulating a lattice of spins, the dominant effect is nearest neighbor. On the other hand, there are more exotic and interesting problems in physics involving next nearest neighbor coupling and interactions. Next nearest neighbor coupling will require more connectivity, and some problems may also require very non-local interactions. For algorithms that require a lot of complexity, all-to-all connectivity in a qubit architecture is ideal and desired. However, at the crux of connectivity is again, the issue of crosstalk. In principle, a physical architecture designed for the surface code could have all-to-all connectivity. The connectivity, mediated by crosstalk, would be spatially dependent due to long range parasitic capacitive coupling as the mechanism for non-local interactions. The issue of crosstalk can come into play when algorithms on this architecture utilizes parallelism. Like the quantum bus, one can couple as many qubits as desired, but to individually address and control the level of coupling between each arbitrary pair of qubits requires well controlled or nonexistent crosstalk. For frequency mediated interactions, such as the control-Z gate or the control phase gate, whereby the interactions are turned on and off by a detuning of the qubit frequency, calibrating out crosstalk is a problem that has its own optimization challenges. Detuning the qubits such that they are far apart spectrally, never turns off interactions completely. In such a scheme, there there will always be a background level of interaction or crosstalk between qubits. Thus, all-to-all connectivity must come with a way to turn off parasitic interactions in the ideal state.

In Google's Sycamore processor [2], interactions can be turned completely off by using a qubit as an intermediary coupler. This coupler cancels out an always on capacitive coupling term in the interaction Hamiltonian. The frequency of the coupling qubit mediates the cancellation intensity, and thereby mediates the level of coupling that is desired. However, the Sycamore processor does not enable all-to-all connectivity. All-to-all connectivity might be achieved through a common resonator bus [99]. However, this common bus interaction is also mediated though frequency tuning, where two qubits can be tuned to the same frequency, or away from the bus. A virtual transition or coupling will occur between the two qubits when resonant. One can turn this interaction off between qubits by simply tuning the two qubits off of resonance. However, much like with the old X-Mon architecture with frequency mediated couplings, the bus coupler by itself can never turn interactions perfectly off.

The study of various loss mechanisms for superconductors and superconducting circuits alike, have been an area of research for a couple decades [63] [92]. Early work with kinetic inductance detectors [6] found that a large source of loss comes from substrate materials. With careful analyses of various materials, sapphire and high resistivity silicon have been found to have the lowest loss, due to the crystalline nature of the bulk. Loss through materials is largely considered dielectric loss, but there are other sources of loss that play into effect as well. These other loss channels will be reviewed in this thesis.

Fortunately, there are loss channels which one can engineer around. The crux of making quantum devices useful is the simultaneous need for isolation and control. Qubits should be long lived and free from any decay into the environment. Thus, qubits should be isolated from the environment as well as possible. On the other hand, qubits need to be connected to the environment for us to measure and control them. For example, capacitively exciting the qubit through a microwave line called the XY line will introduce an energy decay channel, due to the resistive elements of the microwave control electronics. Biasing the qubit with a magnetic loop called the flux line or the Z line, will also introduce a loss channel. Coupling each qubit to a readout resonator, which is then coupled to our environment will be a loss mechanism known as the Purcell effect. By isolating each qubit as much as possible, the level of control becomes rather difficult or slow. During the design process, there must be some level of sacrifice in isolation to allow us to control and interface with our qubits one a reasonable time scale. Over-isolating qubits at the expense of slow control might become a zero-sum game if the system is not engineered properly with all dominant loss channels accounted for. Because coupling loss are due to engineered geometries and parameters, we can design qubits that are insensitive to coupling loss relative to the other dominant loss mechanisms in superconducting devices.

1.3 Applications of Hybrid Quantum Systems

Although this thesis is mainly addresses a problem area for superconducting circuits, the ultimate goal of this investigation is to create a platform suitable for both superconducting circuits and optomechanics without sacrificing coherence. The use of multiple quantum technologies requires engineering of a hybrid quantum system [55].

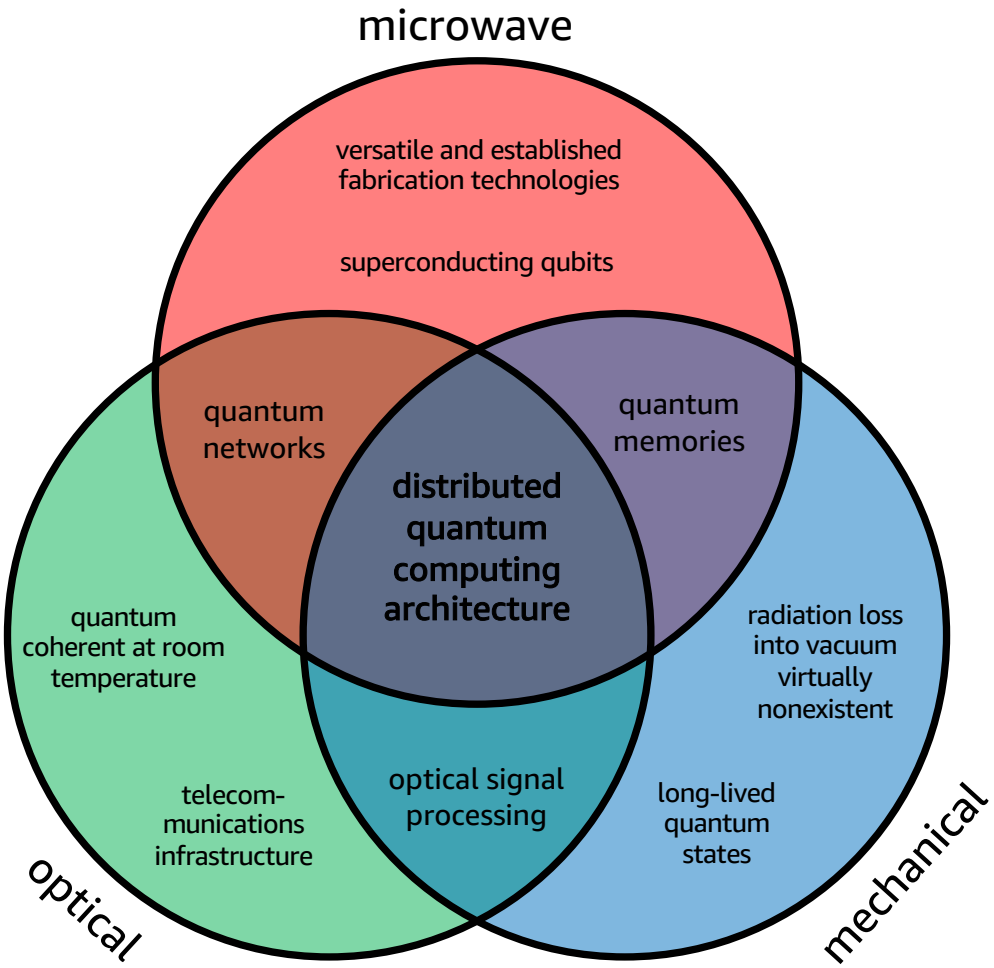

Figure 1.2: Strengths of each platform, with applications of integrating two or more technologies.

In hybrid quantum systems, each subcomponent of the system is used for a feature that is unique to its platform. The hybrid aspect of the system integrates these subcomponent to work together, such that the hybrid system is outperforms the sum of its parts, as illustrated in Figure 1.2. Optical photons (optics) are quantum coherent at room temperature with existing communication infrastructure for long range state transfer. Microwave phonons (mechanics) have virtually non-existent radiation loss into vacuum, and designs that mitigate clamping loss have yielded energy decay time constants five orders of magnitude longer than superconducting qubits (at the same resonance frequency). Microwave photons in superconductors are easy to

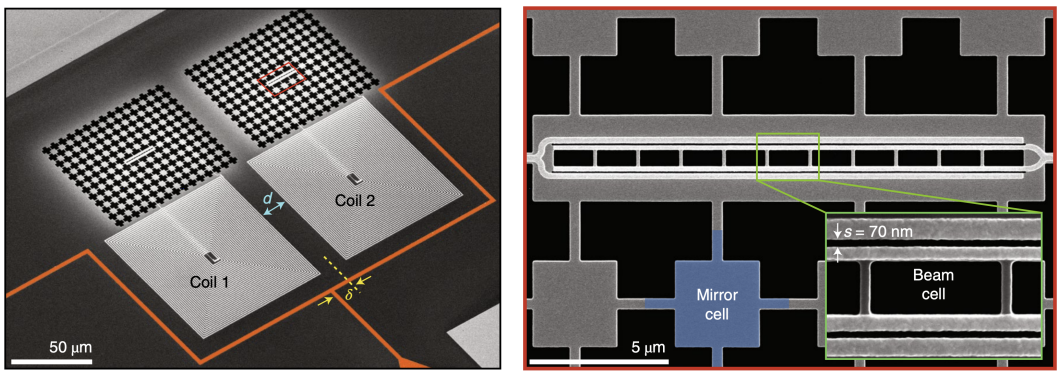

Figure 1.3: Adapted from [46].

fabricate, address, and control (with fast gates) using production fabrication tools and off the shelf microwave equipment. A hybrid platform consisting of a combination of optics or mechanics with superconducting circuits would help address the challenges of scaling, connectivity, and loss.

Transduction from the electrical to optical domain leverages the principle of optomechanics [102][103][67], where a nanofabricated beam has a simultaneous bandgap in both the mechanical (via a breathing mode) and optical (via a defect zone in the silicon) domain. By interfacing with the mechanical mode using a piezoelectric material, the conversion of microwave photons to optical photons could enable distributed computing amongst many computing nodes. Recent work, as shown in Figure 1.3, have taken the first steps to realizing such a hybrid system.

Recently, the mechanical mode of a nanobeam has been shown to have energy leakage rates five orders of magnitude lower than superconducting circuits, using a structure such as one shown in Figure 1.4. This low loss degree of freedom can be used for quantum memories to store quantum information during idle portions of the algorithm.

For integration of multiple technologies onto the same device, these hybrid quantum systems must use the same substrate. Silicon-on-insultaor (SOI) is used extensively in the optomechanics community, so a highly coherent superconducting qubit would make way for the integration of this technology into existing processes. In this thesis, we will review the basics of superconducting circuits and consider various sources of loss. We will then review some basic principle of fabrication, before looking

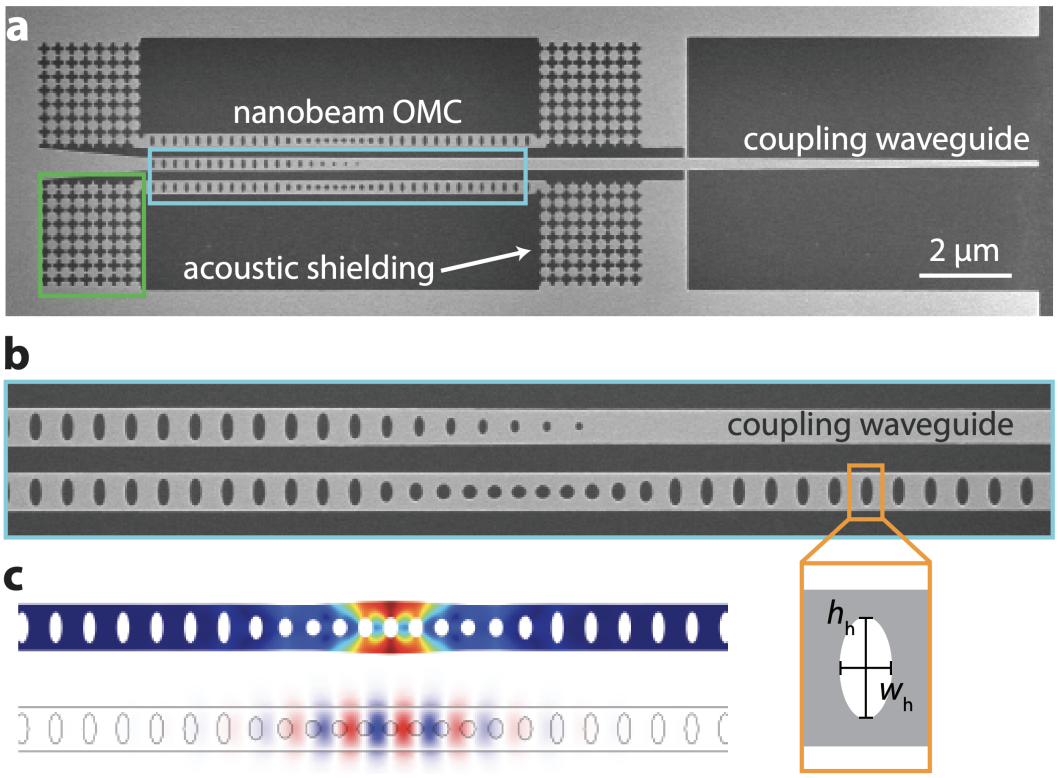

Figure 1.4: Adapted from [60].

at qubit performance on silicon and SOI. Finally, we will address the issues of scalability and loss on SOI by introducing an improved microwave structure and characterizing its performance.

Chapter 2

SUPERCONDUCTING CIRCUITS

2.1 CPW Resonators

Superconducting resonators are the workhorse for superconducting circuits. They can be based on distributed transmission lines or compact lumped elements. The former provides a resonant energy profile found in wave-like systems, such as acoustic or optical cavities where the resonant mode are standing waves that have constructively interfered within the cavity, where the voltage anti-node is at the capacitive end (for quarter wave resonances) and the current anti-node is at the grounded end. The latter emulates the spirit of circuit models, where the energy contained within the resonator follows the capacitive and inductive characteristics of the resonator ($CV^2/2$ and $LI^2/2$). Here, we consider the distributed transmission line model, which can be less lossy and have lower crosstalk depending on the microwave structure chosen.

Transmission Line Model

The transmission line can be modeled by considering an infinitesimal section along two conductors in the transverse direction of propagation (z) as shown in Figure 2.1. We assume that δL is the infinitesimal series inductance of the two conductors, δR is the infinitesimal series resistance of the line (typically considered when the superconductor has a non-zero finite conductivity), δC is the infinitesimal capacitance between the two conductors, and δG is the infinitesimal parallel conductance between the two conductors (typically considered when the dielectric material between the two conductors is lossy). The transmission line is lossless with $R = G = 0$. It follows that the wave equations describing the voltage and currents

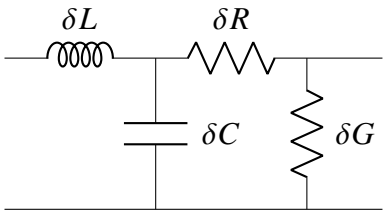

Figure 2.1: Transmission line model for for a microwaves, by considering an infinitesimal piece along the direction of propagation.

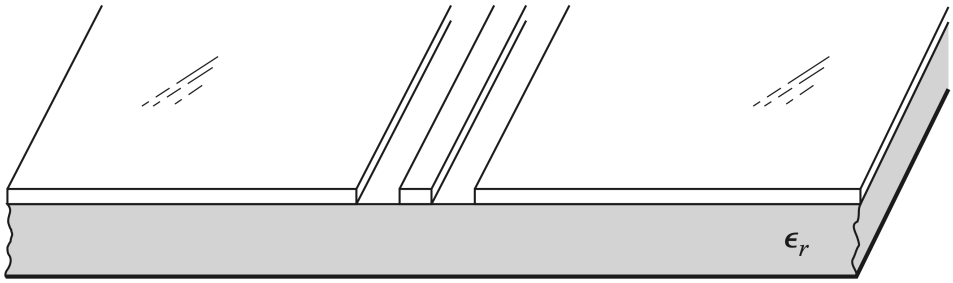

Figure 2.2: Cross sectional view of a coplanar waveguide geometry, commonly used as a transmission line structure on planar substrates [79]. The width W of the center trace and the gap G between the center trace and ground planes set the characteristic impedance Z_0 of the transmission line.

on the transmission line can then be written as [79]

$$0 = \frac{d^2V}{dz^2} - \gamma^2 V \tag{2.1}$$

$$0 = \frac{d^2I}{dz^2} - \gamma^2 I \tag{2.2}$$

$$\gamma = \alpha + i\beta \tag{2.3}$$

with $\alpha \approx \frac{1}{2}\left(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}\right)$ (for $R \ll \omega L$ and $G \ll \omega C$) describing the loss or energy decay in the line and $\beta \approx \omega\sqrt{LC}$ describing the wave propagation in the line. The characteristic impedance is

$$Z_0 = \sqrt{\frac{R + i\omega L}{G + i\omega C}} \tag{2.4}$$

and describes the ratio between currents and voltages during propagation. Like the refractive index in optics, if the characteristic impedance is unmatched along the transmission line, reflections will occur at the mismatched interface.

Transmission Line Structures

Depending on the microwave geometry used in a circuit, a variety of solutions for propagating wave with Maxwell's equations are possible. Some commonly used microwave geometries include: Microstrip (Quasi-TEM), Stripline (TEM), and the Coplanar Waveguide (Quasi-TEM). The mode of interest for a low crosstalk and low radiation signal line is the TEM or transverse electromagnetic condition. A TEM mode will have both its electric and magnetic fields perpendicular to the direction of propagation, which effectively means that the mode does not have any dispersion and allows for a linear phase velocity $v_p = \omega/\beta$. A number of trans-

mission line geometries have the TEM as the main/dominant method of propagation.

Some geometries can be classified to be quasi-TEM due to the fact that the dielectric medium around electrical conductors is slightly non-uniform. Such a discontinuous boundary condition causes the fields to be slightly parallel with the direction of propagation and cause the fields to be more radiative. Such an effect can be seen or accounted for as loss in the transmission line. Loss can be suppressed if the dielectric is very high permitivitty, with most of the energy density in the substrate, making the fields look effectively more TEM. Due to a much larger presence of the field in the substrate, the fields in the vacuum can be considered a minor effect.

For superconducting circuits, the coplanar wave-guide (CPW) is a popular choice due to its simplicity of fabrication and lower radiation properties compared to microstrip. The stripline geometry is a center trace sandwiched between two dielectric later, making it much more difficult to fabricate on a single die or wafer (most likely, die or wafer bonding is required).

Coplanar Waveguides

Currently, most (if not all) superconducting devices, utilize a microwave geometry called a coplanar waveguide (CPW). A CPW is comprised of a metallized characteristic center trace surrounded by two metallized ground planes with a characteristic vacuum gap, all of which lie in-plane on top of the substrate as shown in Figure 2.2. The advantage of such an arrangement is simple device fabrication with microwave properties that result in a quasi-TEM field. Patterning only requires etching away the gap between a center trace and ground planes. The quasi-TEM or TEM-"like" mode of propagation emulates for the most part the TEM mode found in ideal transmission lines, such as a coax cable.

We looked at the basic model of transmission line theory, which assumes some series inductance and some parallel capacitance per unit length. Now let's consider a typical geometry and substrate found in superconducting circuits. For a coplanar

waveguide geometry, these values can be found analytically with [9]

$$L = \frac{\mu_0}{4}\frac{K(k')}{K(k)} \tag{2.5}$$

$$C = 4\epsilon_0\epsilon_{\text{eff}}\frac{K(k)}{K(k')} \tag{2.6}$$

$$k = \frac{W}{W+2G} \tag{2.7}$$

$$1 = k^2 + k'^2 \tag{2.8}$$

where K is the complete elliptic integral of the first kind and ϵ_{eff} is the effective dielectric constant which can often be approximated by $\frac{\epsilon_{\text{sub}}+1}{2}$ when the thickness of the substrate is much larger than the critical dimensions of the waveguide. Generally the effective dielectric constant can be found using numerical methods (see A). The parameter k is a geometric parameter that arises from a complex analysis technique called conformal mapping.

On silicon $\epsilon_{\text{eff}} \approx 6.45$, the design heuristic is $W = 2G$ so $k = 0.5, K(k) = 1.8541$ and $k' = \sqrt{0.75}, K(k') = 2.4413$, which gives $L = 4.1344 \times 10^{-7}$ H/m and $C = 1.7349 \times 10^{-10}$ F/m. It is important to note that the inductance and capacitance per unit length goes along with the full wavelength of a resonator, and does not directly set the resonance frequency like in the case of the lump element resonator. Rather, the resonance is set by the length of the resonator λ and ϵ_{eff}:

$$\frac{\lambda}{n} = \frac{c}{\sqrt{\epsilon_{\text{eff}}} n f_0} \tag{2.9}$$

This makes sense because quarter-wave ($n = 1/4$) and half-wave ($n = 1/2$) resonators have the same resonance frequencies, but different lengths.

Conformal Mapping

To understand solutions for the CPW result, we need to understand conformal mapping techniques, which allow us to map solutions from a parallel plate capacitor (PPC) geometry to the CPW. The basic principle is to apply a transformation to a simpler problem with a known solution, like the PPC, and use the mapping function to obtain a solution for the more complex case. For example, to find the capacitance per unit length of a CPW cross section, we assign the center trace of CPW to map from the bottom electron of the PPC, and the ground planes to the top electrode of

the PPC [28]. By applying a mapping that takes one half of the top electrode to $+\infty$ and the other half to $-\infty$, our solutions for PPC can also be found given that we know the transformation. As shown in Figure 2.3, the elliptic mapping with $S = \mathrm{sn}(z, k)$, where sn is a Jacobi elliptic function, takes values on the complex plane and maps them onto the real axis, and is defined as

$$z = \mathrm{sn}^{-1}(S, k) = \int_0^S \frac{ds}{\sqrt{\left(1 - S^2\right)\left(1 - k^2 S^2\right)}} \tag{2.10}$$

with a periodicity of $4K$ in the real component and $2K'$ in the imaginary component. To evaluate this mapping, we utilize the elliptic sine function

$$K(k) = \int_0^1 \frac{dS}{\sqrt{\left(1 - S^2\right)\left(1 - k^2 S^2\right)}} = \int_0^{\pi/2} \frac{d\theta}{\sqrt{1 - k^2 \sin^2\theta}} \tag{2.11}$$

$$K(k) + iK'(k) = \int_0^{1/k} \frac{dS}{\sqrt{\left(1 - S^2\right)\left(1 - k^2 S^2\right)}} \tag{2.12}$$

$$\approx \int_0^{1/k} \frac{dS}{\sqrt{\left(1 - S^2\right)\left(1 - k^2 S^2\right)}} + i \int_1^{1/k} \frac{dS}{\sqrt{\left(S^2 - 1\right)\left(1 - k^2 S^2\right)}} \tag{2.13}$$

$$= K(k) + iK(k') \tag{2.14}$$

where we have used $S = \sin\theta$, with $k^2(S^2 - 1) = (1 - k^2)\cos^2\theta$, so it follows that $k' = \sqrt{1 - k^2}$. Thus, K is the complete elliptic integral of the first kind. In the PPC geometry, the top electrode is defined from points B to F, and the bottom electrode is defined from points C to E. In the CPW geometry the center trace is defined from points C to E, and the ground planes are defined from B to A and F to G. We also assume that there is some dielectric material with permittivity ϵ_r inside (outside) the PPC box defined by points A - G, which results in the dielectric material being above (below) the metal plane layer on the real axis of S. For the sake of simplicity, we also choose to ignore fringing fields in the PPC problem. We can easily extract the solution for capacitance, and so extract the solution for inductance (by assuming sheets of current) using this method. As a result of how our problem is mapped, our solution thus takes the form of elliptic integrals. This method can be extended to other more complicated geometries, but a mapping needs to be determined first.

Quality Factors

Now that we know how to model CPW geometries analytically, we would like to quantify the performance of these geometries and consider realistic effects such as

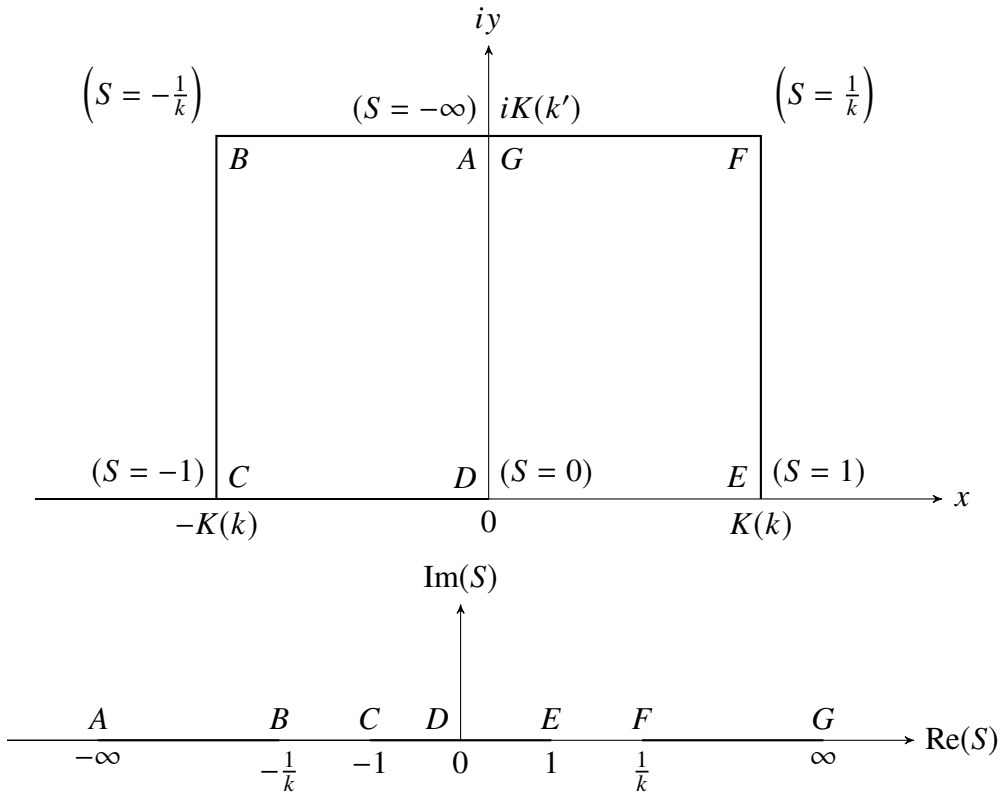

Figure 2.3: The mapping $S = \mathrm{sn}(z, k)$ for a few different values of $z = x + iy$. Such a transformation is useful for mapping parallel plate capacitor solutions to coplanar waveguide or coplanar stripline (by flipping the polarity of metal) geometries.

radiation and material loss. When characterizing superconducting resonators, one important metric that needs to be considered is the quality factor. The quality factor for a resonator at frequency f_0 with resonance peak characterized by full width half max bandwidth of f_{FWHM} is defined as

$$Q = \frac{f_0}{f_{\mathrm{FWHM}}} = \frac{E_{int}}{E_{lost}} \tag{2.15}$$

and describes the decay and energy loss when resonant. E_{int} is the energy stored in the resonator, and E_{lost} is the energy loss per cycle. We have seen in the transmission model in Figure 2.1 that there are resistive and conductive terms which can be modeled as a loss term in the wave equation. The resistive term describes the normal metal state of the SC due to a non-zero temperature or excess Cooper-pair breaking quasiparticles, and the conductive turn describes dielectric loss where the electric field energy is converted into phonons in the dielectric material or radiated away from the transmission line into free space or the microwave packaging. Because there are typically multiple sources of loss, we can look at the individual components

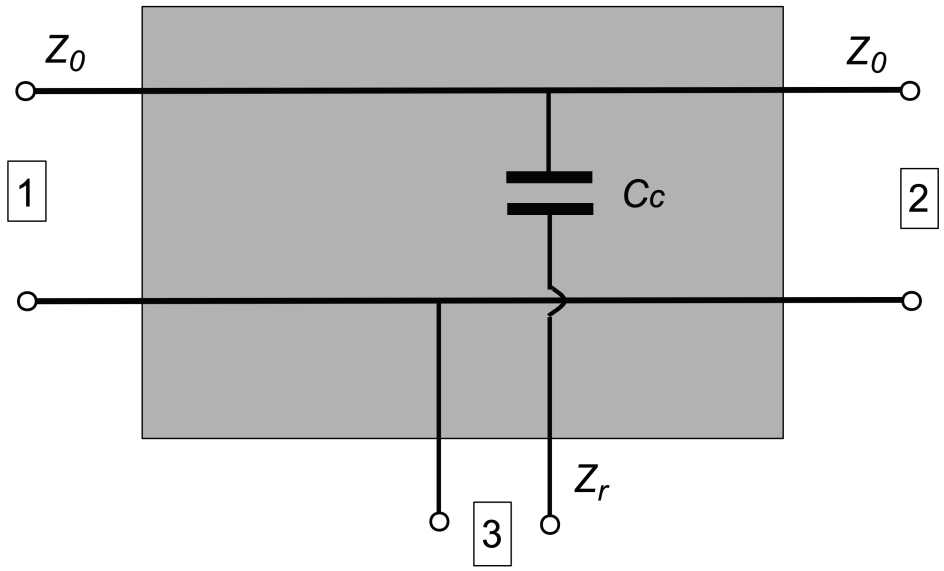

Figure 2.4: Three port model for a capacitively coupled resonator, adapted from [36]

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by prescribing a quality factor to each loss channel and adding up the losses in the following way:

$$\frac{1}{Q_{\text{total}}} = \frac{1}{Q_{\text{radiation}}} + \frac{1}{Q_{\text{dielectric}}} + \frac{1}{Q_{\text{external}}} + \frac{1}{Q_{\text{quasiparticle}}} \tag{2.16}$$

In particular, the external quality factor Q_{external} sets the leakage rate from the resonator out into the measurement environment, whereas the other quality factors are set by the inherent material and device physics and can be combined into one term, Q_{internal}, which can be viewed as the ultimate limit for the quality factor of the resonator, since one can choose the external coupling arbitrarily.

Interrogating Capacitively Coupled Resonators

To excite and measure these resonators, we need to consider a three port model, shown in Figure 2.4, with the two ports serving as the transmission line, and the third port serving as the open capacitive end of a $\lambda/4$ resonator [36]. Alternatively, we can couple the resonator inductively to the transmission line, with the resonator having an open end to ground as shown in Figure 2.5. We find that the scattering parameter into and out of the resonator is

$$|S_{33}| = \sqrt{1 - 2\,|S_{31}|^2} \tag{2.17}$$

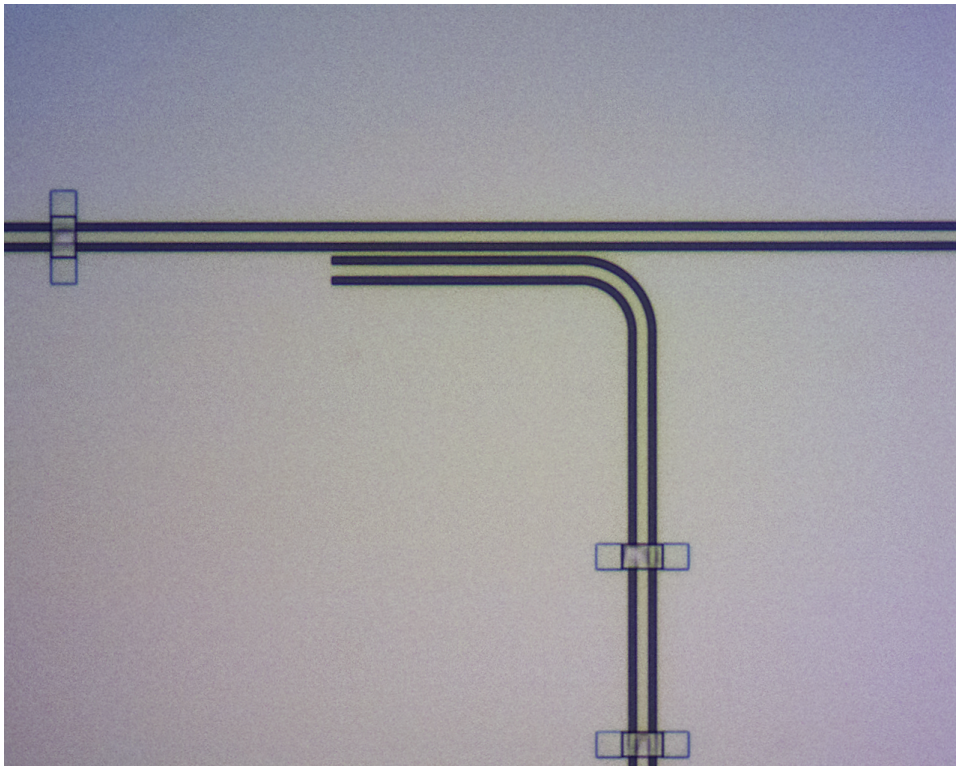

Figure 2.5: Fabricated resonator inductively coupled to a transmission line with the other end open. The center trace width is 10 microns and the gap s 5 microns.

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and that the transmission through the feedline is

$$t_{21} = S_{21} + \frac{S_{31}^2}{e^{2\gamma l}\frac{Z_0+Z_r}{Z_0-Z_r} - S_{33}} \tag{2.18}$$

with l as the length of the resonator, Z_r the characteristic impedance of the resonator, and Z_0 the characteristic impedance of the feedline, with γ given previously by Eq. 2.3. We then define

$$Q_e = \frac{2\pi}{4\,|S_{31}|^2} \tag{2.19}$$

where the factor of 4 comes from equal leakage into port 1 and 2, as well as having two reflections to form a quarter standing wave. It follows that

$$t_{21} = 1 - \frac{Q_r}{Q_e\left(1 + 2iQ_r\frac{\omega-\omega_0}{\omega_0}\right)} \tag{2.20}$$

with $1/Q_r = 1/Q_i + 1/Q_e$. After rearranging, and adding some realistic terms such as a phasor pre-factor $A_0 e^{-i(\omega\tau+\phi)}$ to account for a background transmission spectrum,

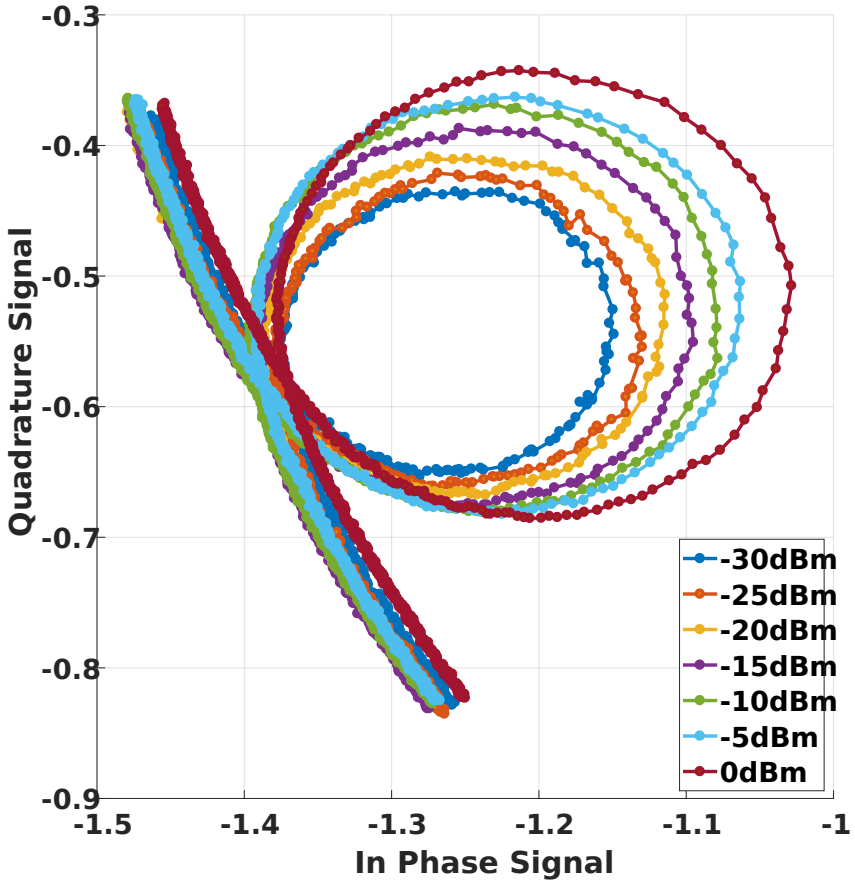


Figure 2.6: Measured resonator signal for various network analyzer output powers in the IQ plane. The shrinking of the resonant circle versus interrogation power represents a decrease in the quality factor, which can be thought of as the full width half max (FWHM) of the resonant dip.

as well as $\delta\omega$ for an asymmetric Fano resonance term, we obtain: [77]

$$t_{21} = A_0 e^{-i(\omega\tau+\phi)}\left(1 - \frac{Q_i - 2iQ_eQ_i\frac{\delta\omega}{\omega_0}}{(Q_e+Q_i) + 2iQ_eQ_i\frac{(\omega-\omega_0)}{\omega_0}}\right) \tag{2.21}$$

If we plot this response in the complex plane with the real axis as the in-phase (I) component and the imaginary axis as the quadrature (Q) component, then we see that the response of the resonator forms a circle that has a diameter set by the magnitude depth of the resonance as shown in Figure 2.6. We also see that the circular shape causes the phase response to be modulated through the resonance.

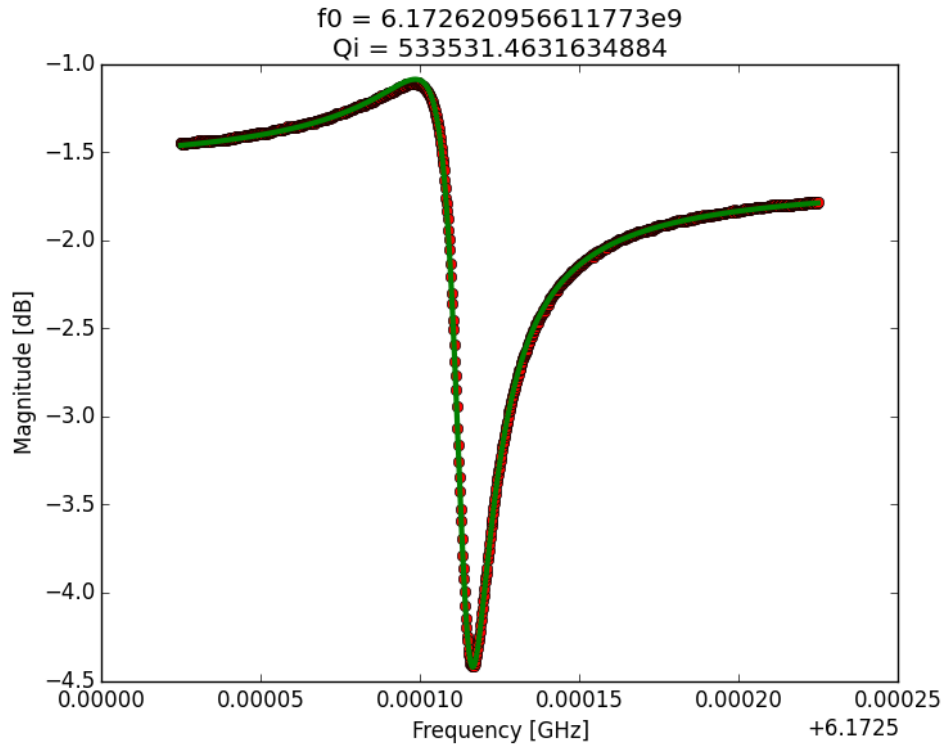


Figure 2.7: Quality factor fit of an aluminum resonator on silicon interrogated at high power, around millions of photons.

The number of photons circulating in the resonator also has an effect on the quality factor. At high circulation powers there are two-level-systems (TLS), which can manifest as an extra tunneling degrees of freedom in some amorphous material on the substrate, that saturate and do not typically have higher energy levels to absorb energy. Thus, the intrinsic quality factors Q_i at high power at not limited to the effects of TLS. An example of a fit to the magnitude response is shown for high interrogation power in Figure 2.7 and low interrogation power in Figure 2.8. In general, we can write the quality factor dependence in terms of the resonator's internal power P_i and some critical power P_c when the TLS start being saturated [15]

$$\frac{1}{Q_i} = \frac{\tan\delta \tanh \frac{\hbar\omega_r}{2k_BT}}{\sqrt{1+(P_i/P_c)^\beta}} + \tan\delta_r \tag{2.22}$$

for some $\tan\delta$ representing the low power TLS loss tangent, β to account geometric variations in the voltage profile of the resonance, and $\tan\delta_r$ representing radiation, quasiparticle or vortex loss. At low power, TLS will have unsaturated transitions near the frequency of the resonator. These TLS will absorb photons from the

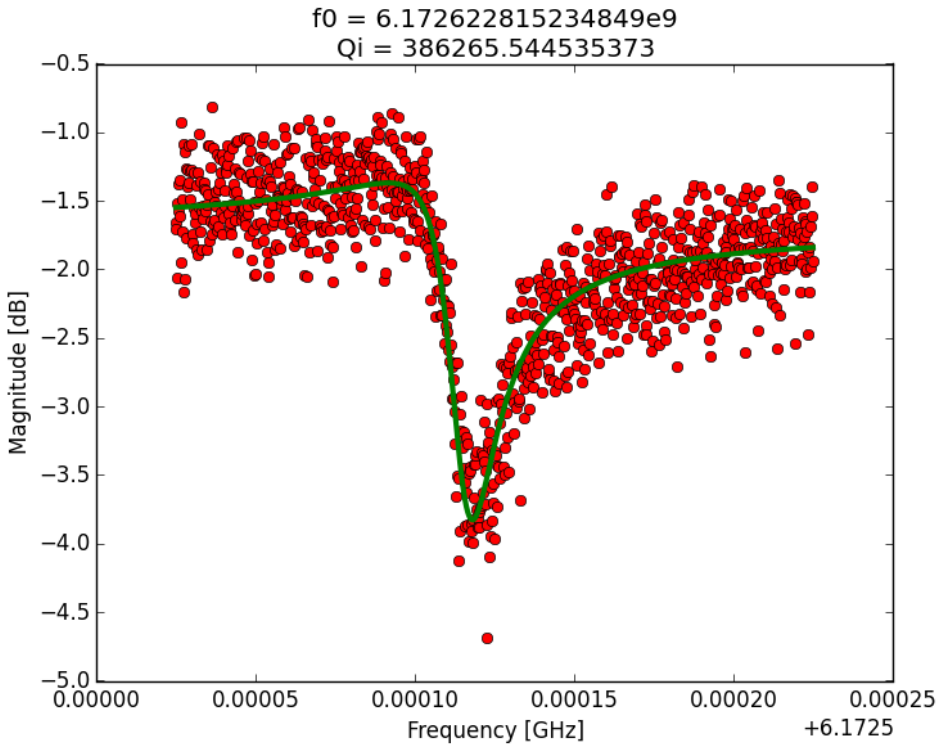


Figure 2.8: Quality factor fit of an aluminum resonator on silicon interrogated at low power, around the 1 - 10 photon level.

resonator and convert the energy a displacement in the molecular bond of the dielectric material (in the amorphous material model for TLS). Thus, the quality factor will typically degrade with lower power in the resonator for aluminum on silicon devices.

To best emulate the environment for the large shunting capacitor of a superconducting qubit, we take advantage of the CPW geometry and probe the quality factor limits due to TLS at single photon levels within the resonator. Superconducting resonators are a convenient proxy for the performance of superconducting qubits, and allow us to understand and study various loss mechanisms that will ultimately inform design decisions on the qubit. To calculate the number of photons circulating within a resonator, we will need to know the circulating power at the feedline of the device, which has been reduced from wiring attenuation and filtering by the time the power reaches the milliKelvin stage. Assuming some capacitance per unit length of

the resonator C' for a resonator of length l, internal circulating power is [9]

$$P_{circ} = \frac{2}{\pi}\frac{Q_r^2}{Q_e}P_{in} \tag{2.23}$$

and with $P_{circ} = \frac{Z_0 V_r^2}{2}$ and $E_{int} = \frac{C'lV_r^2}{2} = \langle n \rangle \hbar\omega_r$, for n phonons on average in the resonator, we have

$$\langle n \rangle = \frac{2P_{in}}{\pi}\frac{Q_r^2}{Q_e}\frac{C'l}{Z_0\hbar\omega_r} \tag{2.24}$$

which we can use to determine the photon number in the resonator when sweeping power measurements.

2.2 Superconducting Qubits

Quantum bits made with superconductors have three primary elements: the superconductor, the tunnel barrier, and the substrate. Typically the superconductor used is aluminum (Al), niobium (Nb), or a niobium titanium (NbTi) disordered alloy is added to a substrate either by electron beam evaporation or sputter deposition in an ultra high vacuum (10^{-9}mbar). The tunnel barrier is often formed from oxidation of an existing Al layer in a controlled oxygen-rich environment, although alternative methods, such as atomic layer deposition (ALD) or etching techniques have been developed [59][73]. The substrate is generally chosen to be low loss: typically sapphire or high-resistivity silicon, such that the quality factor of the superconducting elements is not limited by the bulk substrate.

As we've seen in this chapter, it is possible to pattern superconducting films to form resonant elements, which have some intrinsic quality factor. This resonator has a Hamiltonian described by its circuit values

$$\hat{H} = \frac{\hat{Q}^2}{2C} + \frac{\hat{\Phi}^2}{2L} \tag{2.25}$$

with quantum mechanical energy levels

$$E_n = \left(n + \frac{1}{2}\right)\frac{\hbar}{\sqrt{LC}} \tag{2.26}$$

which have equally space energy levels $\hbar\omega = \frac{\hbar}{\sqrt{LC}}$ apart. However, if we now instead replace the linear inductance with something non-linear, like a Josephson junction, where [61]

$$I_J = I_c \sin\left(\phi_L - \phi_R\right) \tag{2.27}$$

$$V = \frac{\Phi_0}{2\pi}\frac{d\left(\phi_L - \phi_R\right)}{dt} \tag{2.28}$$

with the flux quantum $\Phi_0 = h/2e$ and $\phi_{L/R}$ are the superconducting phases on each side of the junction. It follows that

$$U_J = \int I_J V dt = -\frac{I_c \Phi_0}{2\pi} \cos\left(\hat{\Phi}\right) = -E_J \cos\left(\hat{\Phi}\right) \tag{2.29}$$

where $\hat{\Phi} = \phi_L - \phi_R$. We see that with a modified Hamiltonian with a Josephson junction inductor, an expansion of first few terms around $\phi_L = \phi_R$ yields

$$\hat{H} = \frac{\hat{Q}^2}{2C} - E_J \left[1 - \frac{\hat{\Phi}^2}{2} + \frac{\hat{\Phi}^4}{24} - \cdots\right] \tag{2.30}$$

which introduces a slight perturbation to the quadratic potential from the LC harmonic oscillator. This perturbation slightly shifts the qubit energy levels, such that the energy difference between the $|0\rangle \rightarrow |1\rangle$ and the $|1\rangle \rightarrow |2\rangle$ transition, in other words the anharmonicity α is about $E_C = \frac{e^2}{2C}$ [51]. This anharmonicity allows us to selectively target the $|0\rangle \rightarrow |1\rangle$ without causing transitions from $|1\rangle \rightarrow |2\rangle$, for the purpose of having well defined quantum bits with an addressable frequency as shown in Figure 2.9.

Given current resolution standards, Josephson junctions can be made as small as 100nm by 100nm. With electron beam evaporation tools that allow for in situ oxidation, it is reasonable to fabricate junctions with an inductance of 22nH. Placing a pair of junctions in a superconducting loop to form a superconducting quantum interference device (SQUID), we can tune the effective total inductance of the SQUID by biasing the amounting of flux in the loop. It is also reasonable to fabrication planar capacitors on silicon substrates with self capacitance of 70fF. With these two design values, one can design and fabricate a superconducting qubit with $f_q = \frac{1}{2\pi\sqrt{LC}} \approx 5.7$ GHz. At these frequencies, the corresponding temperature is about 275 milliKelvin (mK), suggesting that we should be far below 100 mK to avoid thermal fluctuations that may cause spurious transitions in our qubit. For this reason, superconducting qubits not only operate at low temperature to allow for superconductivity, but also to allow for the addressing of qubits at microwave frequency using commercial microwave electronics.

The qubit's energy lives between the electric field (either between conductors, or across the tunnel barrier in Josephson junctions) and a superconducting persistent current (either tunneling across the junction barrier or circulating through the SQUID

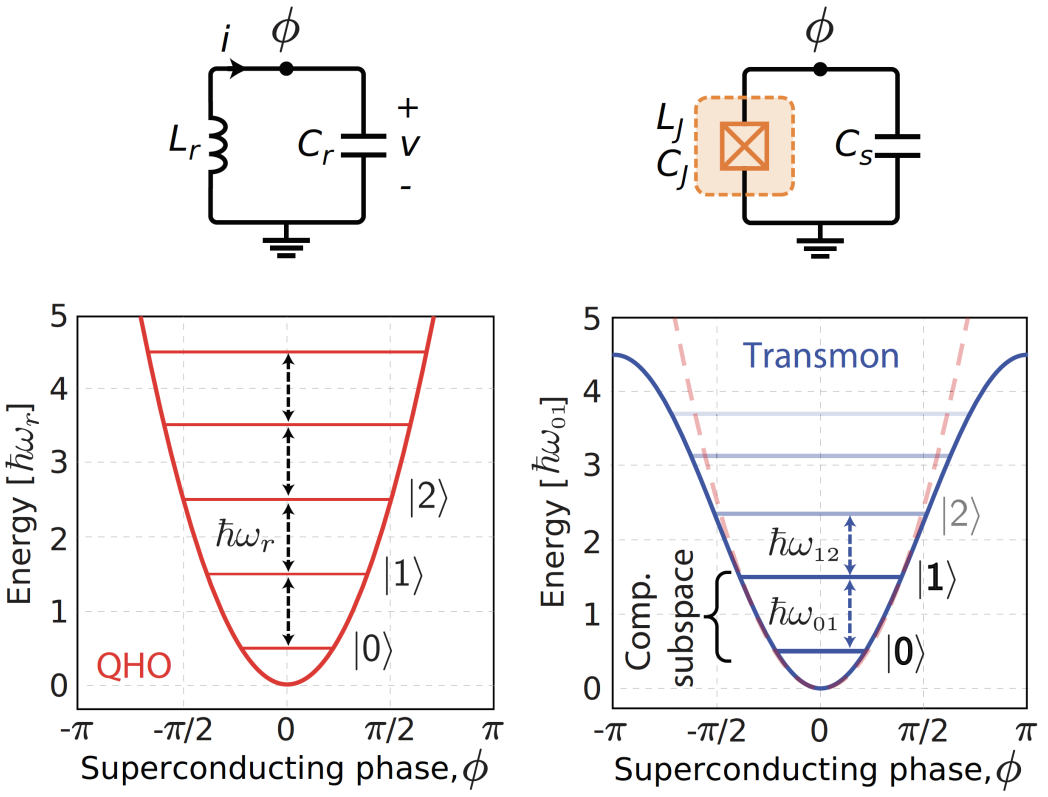


Figure 2.9: Left: Circuit representation and energy levels for a quantum harmonic oscillator (QHO) represented by an LC resonator (L_r, C_r). Right: Circuit representation and energy levels for a quantum bit represented by a Josephson junction (L_J, C_J) shunted by a capacitor C_s. The two lowest levels of the qubit are used for computation. Figure adapted from [52].

loop). Since the dimensions of the qubit capacitor are typically large (up to hundreds of microns across), the extent of electric fields can be quite large. To emulate the extent of these fields, we can use superconducting resonators to characterize how the field energy decays into the substrate or environment. We can also use resonators to study the effect of dissipative vortices, which form when a superconducting film is cooled through its transition temperature with magnetic flux piercing the film. The presence of normal state quasiparticles that drive the superconducting film normal also generates dissipation inducing loss in the superconducting field. More details of the design, layout, and measurement of superconducting qubits will be discussed in Section 3.1 and 5.1.

Chapter 3

LOSS MECHANISMS IN SUPERCONDUCTING QUBITS

Superconducting circuits provide a flexible platform that allows for a high degree of control of the design and layout. However, the limitations due to the lossy properties of materials and nonidealities of the superconducting state remain an outstanding challenge. Figure 3.1 illustrates in a circuit diagram some of the largest contributors to loss, which include loss though the control lines, readout resonator, and radiation. The loss elements of the circuit represent loss that we can control with design. However, there are other losses such as energy adsorption due to substrate material and interface layers left by fabrication and trapped flux in the superconductor when cooling through the transition temperature. These mechanisms are controlled by more systematic processes such as loss from two level system (TLS), dissipative vortices, or paramagnetic surface spins.

The coherence of a qubit is defined as

$$\frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_2^*} \tag{3.1}$$

where T_1 is the pure relaxation (or depolarization) of the qubit and T_2^* is the pure dephasing of the qubit. Because the overall coherence of the qubit will always depend on T_1, we see that $T_2 \leq 2T_1$. Because T_1 will always be a limiting factor when it comes to qubit coherence, studying and understanding how to reduce loss mechanisms related to depolarization is a necessity to design and fabricate more coherent qubits. There are many loss mechanisms that contribute to relaxation of the qubit state, which we can write as:

$$\frac{1}{T_1} = \frac{1}{T_1^{\text{control}}} + \frac{1}{T_1^{\text{purcell}}} + \frac{1}{T_1^{\text{vortex}}} + \frac{1}{T_1^{\text{qp}}} + \frac{1}{T_1^{\text{diel}}} \tag{3.2}$$

The first term $\frac{1}{T_1^{\text{control}}}$ describes the loss due to control wiring, such as the XY drive to perform state transitions or the loss due to the presence of a flux bias line, which is used to tune the qubit frequency. The second term $\frac{1}{T_1^{\text{purcell}}}$ describes the loss through the readout resonator into the environment. The third term $\frac{1}{T_1^{\text{vortex}}}$ describes vorticies that form from trapped flux in the superconductor. The fourth term $\frac{1}{T_1^{\text{qp}}}$

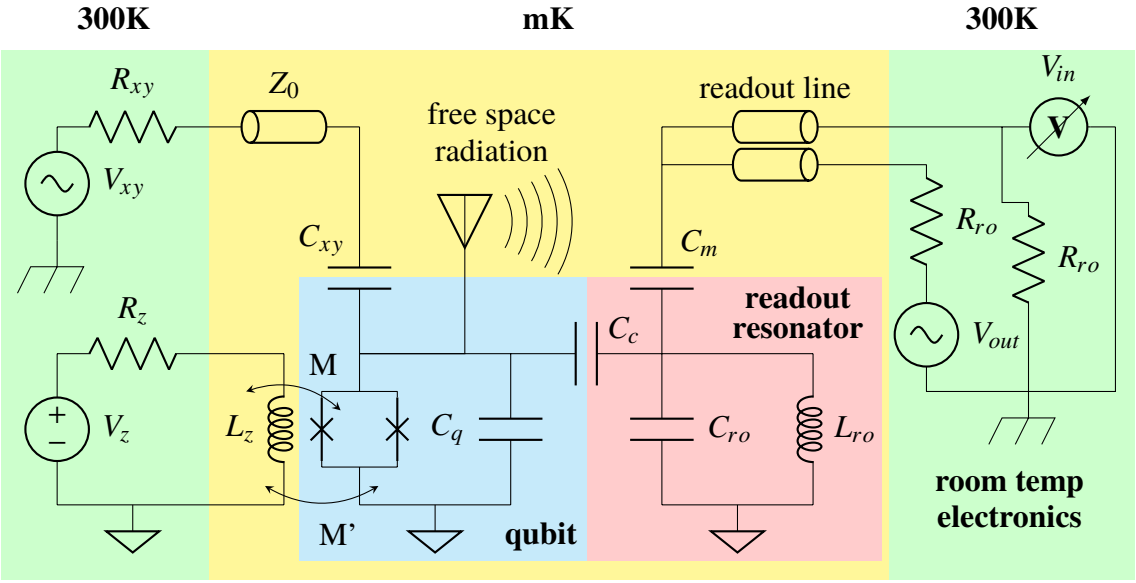


Figure 3.1: Circuit model for various control and readout lines connected to a superconducting qubit. An antenna is included to demonstrate another possibility of a loss channel.

describes excess broken Cooper-pairs in the superconductor, either due to stray infrared radiation or local heating of the superconductor. Finally, the fifth $\frac{1}{T_1^{\text{diel}}}$ term describes loss due to dielectrics and two level systems (TLS) which can absorb energy from electric fields due to dipole coupling between bonds within amorphous material layers.

3.1 Control and Wiring

There many aspects of qubit design to ensure a high level of controllability, while maintaining an adequate level of isolation. In other words, we must connect wiring to allow for qubit control, but not over couple these lines to prevent leakage into the environment. Figure 3.1 shows common loss channels due to the need to do state rotations (XY drive), frequency tuning (Z bias), and readout of the qubit state.

Loss through the XY drive capacitor

The capacitive drive line controls $|0\rangle$ to $|1\rangle$ transitions and requires enough capacitive coupling such we can perform gates quickly (about 10 ns), but not so much coupling that a new loss channel is introduced[51] [8] [87].

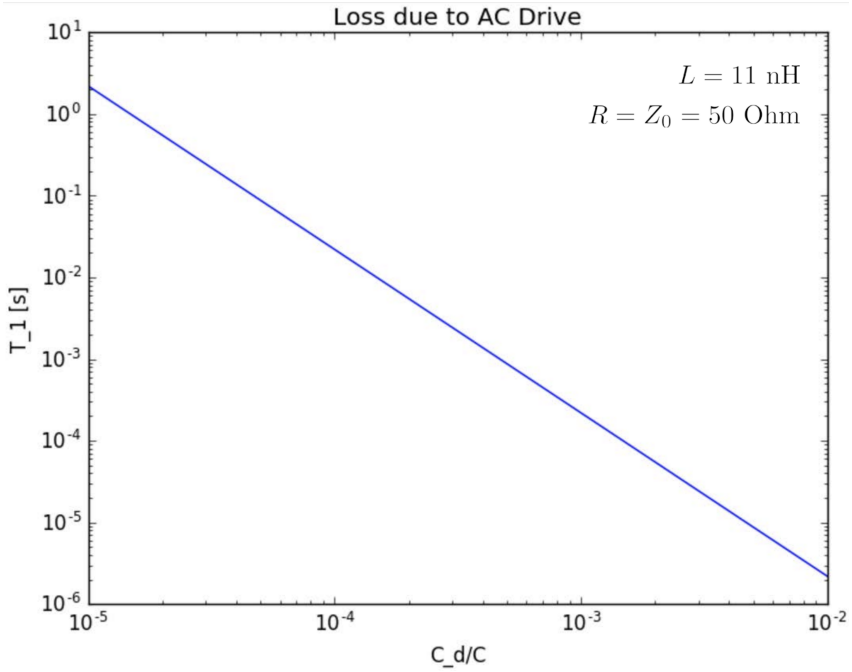


Figure 3.2: Loss due to AC drive for a junction inductance of 11 nH and a driving circuit and transmission line that is 50 Ohm impedance matched.

From the uncertainty principle for the quantum harmonic oscillator, we have

$$\frac{Q_{zp}^2}{2C_q} + \frac{\Phi_{zp}^2}{2L_q} = \frac{\hbar\omega_q}{2} \rightarrow \frac{Q_{zp}^2}{2C_q} = \frac{\Phi_{zp}^2}{2L_q} = \frac{\hbar\omega_q}{4} \tag{3.3}$$

We can related the charge fluctuations to voltage fluctuations of the qubit with $V_0 = \frac{Q_{zp}}{C_q}$ which gives $V_0 = \sqrt{\frac{\hbar\omega_q}{2C_q}}$. The microwave transmission through a capacitor is given by looking at the S-parameter in terms of the Z-parameters of a capacitor between a two port network [79]:

$$S_{21} = \frac{2Z_{21}Z_0}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} \tag{3.4}$$

$$Z_{11} = Z_{22} = 0; \quad Z_{12} = Z_{21} = \frac{1}{i\omega C} \tag{3.5}$$

$$|S_{21}| = \left|\frac{2Z_{21}Z_0}{Z_0^2 - Z_{21}^2}\right| = \frac{2Z_0\omega C}{1 + (Z_0\omega C)^2} \tag{3.6}$$

Thus, the power dissipation from a qubit through capacitive coupling to a resistive load as shown in Figure 3.1 can be found with $Z_0 = R_{xy}$ and $Z_0\omega C \ll 1$. We can approximate $|S_{21}| \approx 2Z_0\omega C$, such that

$$P = \frac{(V_0\,|S_{21}|)^2}{2R_{xy}} \approx 2V_0^2\omega^2 R_{xy}C_{xy}^2 \tag{3.7}$$

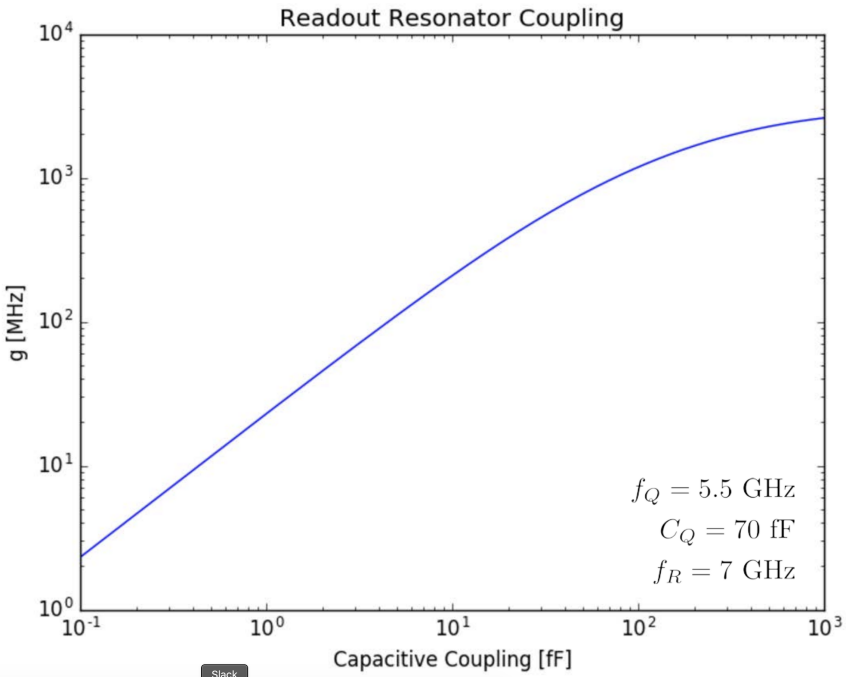


Figure 3.3: Achievable coupling rates between a qubit and a readout resonator that is 1.5 GHz detuned.

It follows that the limited lifetime with $\omega_q = \frac{1}{\sqrt{L_q C_q}}$ is derived as

$$T_1^{xy} = \frac{\hbar\omega_q}{P} = \frac{L_q}{R_{xy}}\left(\frac{C_q}{C_{xy}}\right)^2 \tag{3.8}$$

Purcell decay through the readout resonator

In the traditional transmon design, coupling to the readout resonator is often the dominant source of this type of loss[37]. Possible to engineer a filter that has a frequency dependent decay rate [87]. The spontaneous decay rate of the qubit through the readout resonator is given by

$$\Gamma = \left(\frac{g}{\Delta}\right)^2 \kappa \tag{3.9}$$

where $\Delta = \omega_q - \omega_{ro}$ is the detuning between the qubit and the readout resonator, $\kappa = \omega_{ro}/Q_{ro}(C_m)$ is the decay rate of the readout resonator (which could be frequency dependent if a filter is used) with $Q_{ro}(C_m)$ the quality factor of the resonator which is set by the coupling capacitance C_m to the readout line and is given by [42]:

$$Q_{ro}(C_m) = \frac{\omega_{ro} C_{ro}}{2}\left(\frac{1 + \omega_{ro}^2 C_m^2 R_{ro}^2}{\omega_{ro}^2 C_m^2 R_{ro}}\right) \tag{3.10}$$

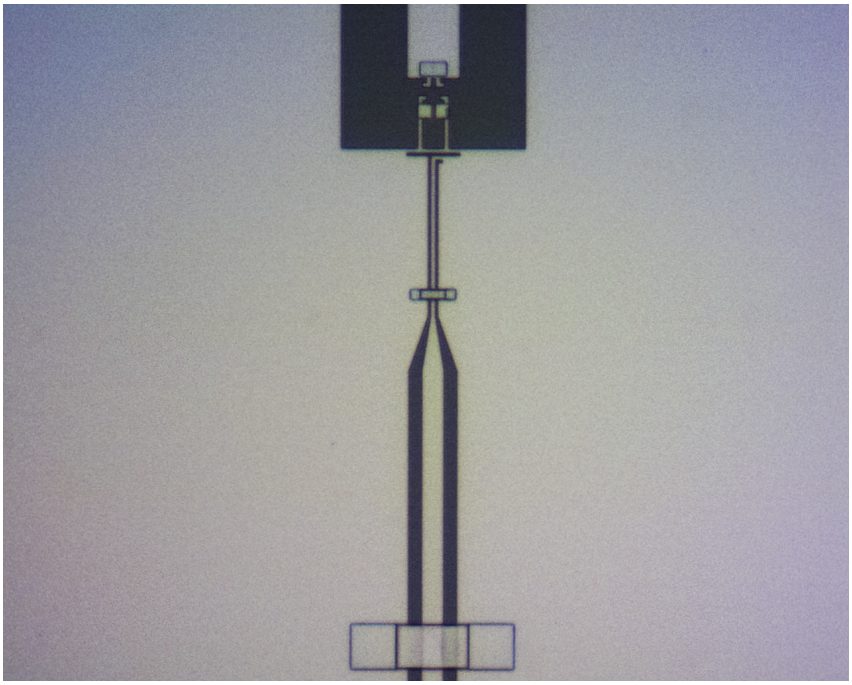


Figure 3.4: A flux bias line design with low parasitic mutual inductance M'. Airbridges are used to control the return currents and minimize long ranging bias fields.

and the coupling g between two resonators is given by (see Appendix B)

$$g = \frac{\sqrt{\omega_q \omega_{ro}}}{2} \frac{C_c}{\sqrt{\left(C_q + C_c\right)\left(C_{ro} + C_c\right)}} \tag{3.11}$$

Thus, the lifetime limit for Purcell decay is

$$T_1^{\text{purcell}} = \frac{1}{\Gamma} = 2C_{ro}\left(\omega_q - \omega_{ro}\right)^2 \frac{\left(C_q + C_c\right)\left(C_{ro} + C_c\right)}{\omega_q \omega_{ro} C_c^2} \left(\frac{1 + \omega_{ro}^2 C_m^2 R_{ro}^2}{\omega_{ro}^2 C_m^2 R_{ro}}\right) \tag{3.12}$$

Inductive loss through the frequency bias line

A perturbative flux noise term Φ_{noise} is added to the frequency bias line such that $\Phi = \Phi_{bias} + \Phi_{noise}$ it follows that [51]:

$$T_1^{z,M} = \frac{\hbar^2}{\left|\left\langle 1|\hat{A}|0\right\rangle\right|^2 S_{\Phi_{noise}}(\omega)} = \frac{\hbar^2}{\left|\left\langle 1|\hat{A}|0\right\rangle\right|^2 M^2 S_{I_{noise}}(\omega_q)} \tag{3.13}$$

where the current quantum noise is $S_{I_{noise}} = \frac{2\hbar\omega_q}{R_z}$ and with some junction asymmetry $d = E_\Delta / E_J = (E_{J1} - E_{J2})/(E_{J1} + E_{J2})$ and $\Phi_B = \pi\Phi_{bias}/\Phi_0$ the operator $\hat{A}$ from this perturbation is

$$\hat{A} = \frac{\pi E_J}{\Phi_0}\left(\sin\Phi_B \cos\hat{\phi} - d\cos\Phi_B \sin\hat{\phi}\right) \tag{3.14}$$

From second quantization,

$$\hat{\phi} = \sqrt{\frac{\hbar}{2m\omega}}(\hat{a} + \hat{a}^\dagger) \tag{3.15}$$

where the effective mass $m = (\Phi_0/2\pi)^2 C_q$. We can approximate around small $\hat{A}$ or in other words we should find the root of this operator, meaning that

$$\sin\Phi_B \cos\phi_0 = d\cos\Phi_B \sin\phi_0 \tag{3.16}$$

$$\phi_0 = \arctan(d\tan\Phi_B) \tag{3.17}$$

Taylor expansion around $\hat{\phi} = \phi_0$ gives

$$\cos(\hat{\phi} = \phi_0) \approx \cos\phi_0 - (\hat{\phi} - \phi_0)\sin\phi_0 - \frac{(\hat{\phi} - \phi_0)^2}{2}\cos\phi_0 + \frac{(\hat{\phi} - \phi_0)^3}{6}\sin\phi_0 \tag{3.18}$$

$$\sin(\hat{\phi} = \phi_0) \approx \sin\phi_0 + (\hat{\phi} - \phi_0)\cos\phi_0 - \frac{(\hat{\phi} - \phi_0)^2}{2}\sin\phi_0 - \frac{(\hat{\phi} - \phi_0)^3}{6}\cos\phi_0 \tag{3.19}$$

to obtain

$$\hat{A} \approx \frac{\pi E_J}{6\Phi_0}\Big(d\cos(\Phi_B)\Big[3\left(\hat{\phi}^2 - 2\hat{\phi}\phi_0 + \phi_0^2 - 2\right)\sin(\phi_0) \tag{3.20}$$

$$+ (\hat{\phi} - \phi_0)\left(\hat{\phi}^2 - 2\hat{\phi}\phi_0 + \phi_0^2 - 6\right)\cos(\phi_0)\Big] \tag{3.21}$$

$$+ \sin(\Phi_B)\Big[(\hat{\phi} - \phi_0)\left(\hat{\phi}^2 - 2\hat{\phi}\phi_0 + \phi_0^2 - 6\right)\sin(\phi_0) \tag{3.22}$$

$$-3\left(\hat{\phi}^2 - 2\hat{\phi}\phi_0 + \phi_0^2 - 2\right)\cos(\phi_0)\Big]\Big) \tag{3.23}$$

We can then use the following expectation values

$$\langle 1|c|0\rangle = 0 \tag{3.24}$$

$$\langle 1|\hat{\phi}|0\rangle = \sqrt{\frac{\hbar}{2m\omega}} \tag{3.25}$$

$$\langle 1|\hat{\phi}^2|0\rangle = 0 \tag{3.26}$$

$$\langle 1|\hat{\phi}^3|0\rangle = 3\left(\frac{\hbar}{2m\omega}\right)^{3/2} \tag{3.27}$$

to compute the value of $\langle 1|\hat{A}|0\rangle$. Given the complexity of evaluating this expression analytically, we can compute numerically with $d = 10\%$, $E_J = 20$GHz, $C_q = 50$fF, $M = 3$pH to obtain

$$\Phi_B = 0 \Rightarrow T_1^{z,M} \approx 8 \text{ ms} \tag{3.28}$$

$$\Phi_B = 0.3\pi \Rightarrow T_1^{z,M} \approx 1 \text{ ms} \tag{3.29}$$

$$\Phi_B = 0.47\pi \Rightarrow T_1^{z,M} \approx 100\ \mu\text{s} \tag{3.30}$$

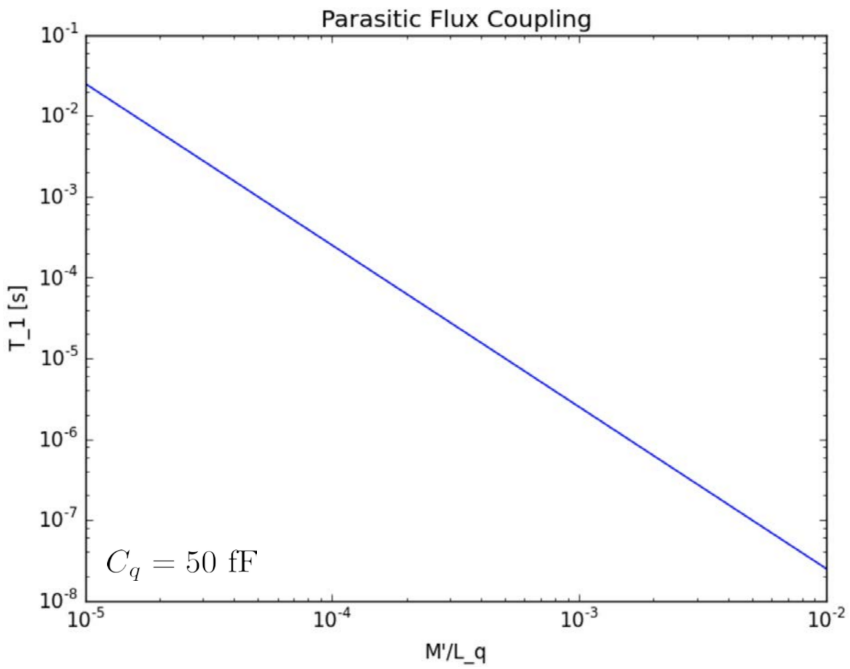


Figure 3.5: T1 loss limit for AC parasitic coupling between the qubit and the flux bias line.

It is important to note that in this analysis, the existence of the junction asymmetry d is what leads to this loss channel. It follows that $d = 0$ gives $\left|\langle 1|\hat{A}|0\rangle\right| = 0$. The parasitic magnetic coupling loss is an AC effect that assumes the induced current due to another mutual inductance M' between the qubit (effectively an LC oscillator) and the resistive load R_z has an associated loss given by [51]:

$$T_1^{z,M'} = \frac{R_z}{M'^2 \omega_q^4 C_q} \tag{3.31}$$

M' is a geometrical property that can be made zero with proper symmetrical design of the flux line (as shown in Figure 3.4) with respect to the qubit capacitor and SQUID loop.

Radiation and packaging loss

Device packaging will also provide a loss channel. The Martinis group has found that floating the device away from the bottom of the box decouples the qubit capacitor from the box and reduces crosstalk between qubits[62]. When the device is not floating, the parasitic coupling is due to a simple parallel plate capacitance $C_b = \epsilon A/d$ that arises when there is a high (11.9) dielectric substrate sandwiched between the qubit capacitor and the box ground. For a 500 μm thick Silicon substrate and a qubit capacitor area of 5000 μm^2, the parasitic capacitance to the device backing

metal is not negligible at around 1fF, which is about 1 - 2% of the shunt capacitance in typical transmon qubit designs. The rate of energy decay from an electric dipole $d = 2eL$ into free space is [51]

$$P_{rad} = \frac{1}{4\pi\epsilon_0}\frac{d^2\omega^4}{3c^2} \tag{3.32}$$

so it follows as before

$$T_1^{rad} = \frac{\hbar\omega_q}{P} = \frac{3\pi\epsilon_0\hbar c}{e^2L^2\omega_q^3} \tag{3.33}$$

The effective electric dipole length L can minimized with designs such as a concentric transmon qubit design [14] or a superconducting backing metal in the packaging [86]. For early iterations of the floating transmon design $L \approx 15\mu$m [89] with the dipole pointing from capacitor island to another. More recent grounded transmon designs (X-mons) have a smaller dipole moment with most of the moment coming from the large potential difference across the Josephson junctions [49].

3.2 Abrikosov vortices

Measurements done on superconducting devices are sensitive to quasiparticle or normal metal states in the superconducting film. One of these normal metal states is a vortex state which appears with pinning or threading of magnetic flux through a thin superconducting type II film. Abrikosov vortices are circulating currents in thin film superconductors caused by the trapping of penetrating magnetic flux when transitioning from a temperature above the critical transition temperature T_C to below T_C. Each vortex is threaded by a flux quantum Φ_0 of magnetic flux and the density of vortices depends on both the coherence length ξ and the London penetration depth λ_l of the of the superconducting film, as well as the external field applied to the superconductor. These circulating currents are not a source of loss on their own, despite having a normal metal region at its core. Rather, the dissipation of energy comes from the displacement and movement of these vortices. The normal metal itself does not lead to loss, but rather the driven dissipative movement of these normal metal cores takes energy out of the system. When vortices appear in superconducting circuits, any current that passes by such formations will couple magnetically to them, and move them across the superconductor. This movement is a dissipative process, which can be modeled as a resistive element. Because of such an effect, vortices will generate loss that depends on both the magnitude of the field penetrating through the skin or the film and the amount of current used to drive these

dissipative mechanisms. The threshold for vortices to form B_{th} is shown in Table 3.1.

Table 3.1: Threshold for vortices to form given various superconducting trace widths.

trace width (μm)	B_{th} (μT)	Field Strength Examples
1	2100	fridge magnet
5	83	Earth's
10	21	field
50	0.83	
100	0.21	

The dissipative mechanisms described have complicated processes, and thus depend on a large number of system parameters. Despite this, attempts have been made to quantify these processes and the dissipation of vortex loss in a superconducting trace can modeled as

$$\frac{1}{T_1^{\text{vortex}}} = H_\theta \left(B - B_{\text{th}}\right) \left(\frac{\frac{J_s^2}{\langle J_s \rangle^2} \left[\frac{\epsilon}{\eta} + \eta \left(\frac{\omega_q}{k_p} \right)^2 \right]}{wtL'} \right) \Phi_0 \left[B - B_{\text{th}}\right] \tag{3.34}$$

$$\approx 0 \text{ if } B < B_{th} \text{ where } B_{th} \approx \Phi_0 / w^2 \tag{3.35}$$

where a large number of geometric, material, and physical properties of the device

need to be taken into account [96] [41] [5] [97]:

$B \equiv$ external field penetrating the superconducting film

$B_{\text{th}} \equiv$ threshold field of vortex formation

$H_\theta \equiv$ Heavyside step function

$J_s \equiv$ current density in the superconductor

$\eta \equiv$ viscous drag coefficient

$k_p \equiv$ pinning constant

$\left(\frac{k_p}{\eta}\right)_{Al} \approx 2\pi \times 4\text{GHz}$ for Aluminum

$\epsilon \approx 0.15$ for Aluminum where:

$\epsilon = 0 \Rightarrow$ dynamics in the flux creep (GR model) regime

$\epsilon = 1 \Rightarrow$ dynamics in the flux-flow resistivity (BS model) regime

$w \equiv$ width of superconducting trace

$t \equiv$ thickness of superconducting film

$L' \equiv$ inductance per unit length of trace

$\Phi_0 \equiv$ flux quantum

The loss is thus non-existent or negligible for fields below the threshold field B_{th}, but linearly contribute to loss based on the properties of the superconductor and geometry of the resonator as represented in Eq. 3.35.

3.3 Quasiparticles

In superconducting aluminum, the gap is equivalent to an energy of a microwave photon at 80 to 120 GHz. Thus, any stray blackbody source of radiation or any stray light that could come in to our sample, could effectively irradiate onto the superconductor and break through Cooper pairs, with energy above the superconducting gap. When these Cooper pairs are broken, superconductivity ceases to exist which leads to normal metal dissipation.

Special filters that block out stray radiation at or above the Cooper pair breaking regime have been made [7][37]. There has also been engineering to essentially trap these quality particles, in a well defined region, such that they do not affect the most critical superconducting parts of your device. These quasiparticle traps are typically just made up of normal metal and are used to quickly dissipate the propagation of

quasiparticles. The choice of metal use is typically copper, because of its high thermal conductivity and it is thought that the long lived quality particles decay slowly because superconductors have not existent thermal conductivity, which allows these quasiparticles to be normally very long lived.

In experiments, parasitic photons can leak into a DR and cause unwanted excitations in the measurement system. From a photon's point of view, a dilution refrigerator (DR) has many available openings such as vacuum pump out ports, cryogenic cables, or telemetry wiring. Unlike phonons, photons will couple with electrons regardless of temperature. Stray light is controlled in three ways in a DR: black absorptive coating, microwave filters, and "light-tight" staging inside the DR. Impedance matched microwave filters will preserve signal integrity while attenuating stray infrared photons.

Increasing the qubit number increases the need for a larger number of control lines in a compact form factor. "Light tight" infrared filters on control lines serve to block out quasiparticle generating infrared light on our superconducting samples [7]. As discussed previously, these quasiparticles act like dissipative metal conductors which negatively affect coherence times. A product line called ECCOSORB act as load absorbers and are able to attenuate across a large frequency range (100 MHz - 100 GHz) depending on application. For qubit control and measurement, filters with a low cutoff frequency are needed for Z control, while filters with a high cutoff frequency are needed for XY control and readout. High frequency filters should have little attenuation and low reflection at our operating point of 4 - 8 GHz. A length for attenuation of 1 cm is chosen so that attenuation is small at these frequencies. ECCOSORB CR-110, the least absorptive epoxy based product, should be used for these filters. Low frequency filters are used on DC lines and attenuate strongly in the microwave range. ECCOSORB CR-124, the strongest epoxy based product, should be used for these filters. A low frequency filter can also be incorporated into the port of the mix plates, saving a considerable amount of space for high density multi-qubit experiments.

The quasiparticle loss limit in a superconducting device can be modeled as:

$$\frac{1}{T_1^{\mathrm{qp}}} = \sqrt{\frac{2\omega_q \Delta}{\pi^2 \hbar}} g \tau_{ss} \tag{3.36}$$

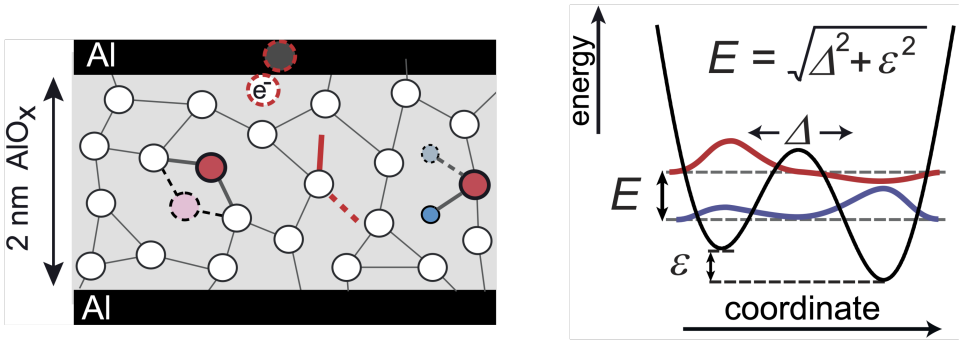


Figure 3.6: Left: Possible mechanisms for two level systems (TLS) in the aluminum oxide layer in Josephson junctions. The red solid/dashed circles indicate tunnelling atoms, the dashed red circles indicates trapped electrons, the blue solid/dashed circles indicate dangling bonds, and the red solid/dashed line indicates hydrogen defects [72]. Right: Tunneling model for TLS, in which the tunneling potential could change depending on defect type. The double well potential is characterized by the energy difference ε and coupling Δ. Adapted from [58].

and is found to be $\frac{1}{500\mu s}$ in typical setups with proper shielding, where τ_{ss} is the quasiparticle relaxation time ($\approx$ 50 ms) and g is the background generation rate ($\approx 10^{-6}$/s).

3.4 Amorphous Dielectrics/TLS

Two level systems (TLS) are the manifestation of material defects in materials or interfaces on superconducting circuit devices. These defects are an outstanding contributor to loss and decoherence in qubits [72]. Because TLS is a catch-all for various fluctuations, the effects of TLS can be seen at low or high frequency, as well as on resonance or off resonance with respect to the qubit. These defects are the result of imperfect or non-crystalline (amorphous) bulk materials such as in silicon or sapphire, as well as interfaces such as the tunnel junction oxide layer, bulk interfaces, and other fabrication residues or surface states as shown in Figure 3.6.

To quantify these defects from a microwave perspective, suppose that we have a thin film of metal ($\sim$ 100 nm) patterned on top of a substrate ($\sim$ 500 μm). There are three possible interfaces where dielectrics (such as oxides, resist, etc.) may appear during the fabrication process: metal-air (ma), metal-substrate (ms), and substrate-air (sa). These interfaces ($\sim$ 5 nm) are shown in Figure 3.7. Each dielectric interface

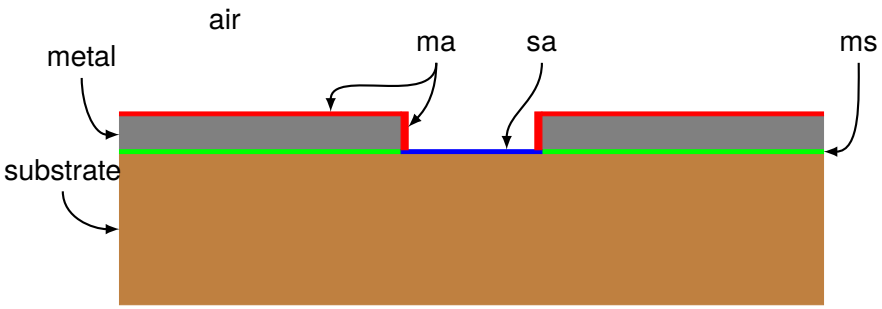


Figure 3.7: Dielectric interfaces on a typical superconducting circuit device. The three possible loss interfaces are shown in red, green, and blue which correspond to the metal-air, metal-substrate, and substrate-air interfaces respectively. Dimensions not to scale.

or bulk mateial layer i will have a characteristic microwave loss tangent $\tan\delta_i$. A weight, known as the participation ratio, p_i for each interface and bulk material helps characterize the total loss tangent for the composite structure [107]

$$\tan\delta = \sum_i p_i \tan\delta_i, \quad Q_0 = \frac{1}{\tan\delta} \tag{3.37}$$

and Q_0, the intrinsic quality factor of a resonator, can be heuristically predicted with the composite loss tangent [63, 79, 105].

$$Q^{\text{diel}} = \omega_q T_1^{\text{diel}} \tag{3.38}$$

$$\frac{1}{T_1^{\text{diel}}} = \omega_q \sum_i p_i \tan\delta_i \tag{3.39}$$

$$p_i = \frac{\iint \frac{|E_i|^2}{2} dA}{\sum_i \iint \frac{|E_i|^2}{2} dA} \tag{3.40}$$

This weight, normalized by the energy per unit length W, is defined as [107]

$$p_i = \frac{t_i \epsilon_i}{W} \int |E|^2 ds = \frac{2 t_i U_i}{W} \tag{3.41}$$

for a thickness t, dielectric constant ϵ of the interface dielectric, and a path ds along the width of the interface. We see that the participation ratio is a ratio of the field energy per unit length contained in the dielectric to the total field energy per unit length. The product $t_i U_i$ gives energy per unit length contained in the cross-sectional area of the interface i, with $U_i = \frac{1}{2}\epsilon_i \int |E|^2 ds$ the energy of the field in the interface per unit area. W is the total energy contained in cross-sectional area of the metal,

substrate, air, and all interfaces.

The 3D transmon takes advantage of this concept by allowing the fields to live in a larger volume. The transmon capacitors are attached to a dipole antenna which radiates these fields into the cavity. Also, designing the transmon capacitor leads to be larger and further away decreases the electric field density U_i and lowers the participation ratio[105][37]. What is the effect of increasing the overall size of the box cavity? The field strength inside the lossy interfaces decreases by the dimension cubed, while the surface area of the lossy dielectrics increases by the dimension squared. This net gain has given 3D transmons an order of magnitude improvement in lifetime over planar devices. Several disadvantages arise from this approach, namely: slower gate times, larger macro-machined device packaging, and scalability/crosstalk issues. One should also note that although the participation ratio of the ma interface for the machined cavity is small, the surface area of the cavity wall is much larger than the device itself, so the cavity needs to be clean and seamless.

It is known that crystalline substrates, such as silicon, contain most of the energy ($p_i \sim 90\%$) and have very small loss tangents ($\tan\delta_{\mathrm{Si}} < 10^{-6}$ at mK temperatures)[62, 105]. However a considerable amount is of energy remains in the air and lossy dielectrics, which may have loss tangents as high as $10^{-3} - 10^{-2}$. In general, we can characterize a qubit's coherence time via the loss from all interfaces:

$$\kappa = \frac{1}{T_1} = \frac{\omega}{Q} = \omega \tan\delta + \Gamma_0 = \omega \sum_i p_i \tan\delta_i + \Gamma_0 \tag{3.42}$$

with an additional loss channel Γ_0 for dissipation of vorticies, quasiparticle excitations, etc. We see that loss tangents on the order of $\sim 10^{-6}$ at 6 GHz or smaller are desirable because we can achieve coherence times on the order of 25 μs or higher.

Studies[105, 107] show that the ms and sa participation ratios are at least an order of magnitude higher than the ma participation ratio. A possible explanation [62] for this discrepancy arises from the larger mismatch of dielectric constants between the air and metal. Thus, surface preparation prior to deposition, careful substrate processing, and optimized capacitance geometries are paramount for improving qubit coherence times.

Chapter 4

PRINCIPLES OF FABRICATION

A highly leveraged feature of the superconducting circuit platform is the ability to fabricate dies using mostly conventional semiconductor processing tools. Such processing tools are readily available in most academic settings, and commonplace in many technology-focused centers around the world. Various fabrication techniques will be discussed in this chapter, including those that allow for the integration of optomechanical and photonic technologies with superconducting circuits.

4.1 Electron Beam Lithography

Electron beam lithography uses high energy beam to cut through long molecular chains on the substrate. Once exposed to this high energy beam, the dissolution rate of these chains in particular solvents increases dramatically, and is removed from the substrate. Because the electron beam can be steered to draw patterns, these selectively removed polymer chains serve as a pattern transfer tool in device fabrication.

Electron Beam Resists

Electron beam resist are comprised of long polymer chains suspended in solvent. The solvent is baked off once the resist is spun on the substrate, and only the polymer chains remain. These polymer chains are sensitive to electron beam exposure, and are selectively soluble in a solution called the developer. There are a few types of beam resist, such as PMMA and ZEP520A. Poly methyl methacrylate (PMMA) are repeating chains of $C_5O_2H_8$. ZEON's ZEP520A is a copolymer - a chain of alternating polymers made of $C_3H_3O_2Cl$ (α-chloromethacrylate) and C_9H_{10} (α-methylstyrene). The α-chloromethacrylate in ZEP520A allows the resist to be highly sensitive, meaning that a lower exposure of electrons will cause the polymer chain to the soluble. The α-methylstyrene gives ZEP520A its high etch resistance in dry etching processes such as ICP-RIE (Inductively Coupled Plasma - Reactive Ion Etching, refer to section 4.4). The long polymer chains are further bound together when baked, and the solvent that suspends these chains dries away. When the electron beam is accelerated towards these interconnected chains, the high energy beam cuts and significantly shortens the length of such polymer chains. This

length shortening process effectively increases the dissolution rate of the polymer in the developer. The amount of electron flux received by the resist can be described as a dose, which has units of $\mu C/cm^2$.

The advantage of using electrons in this patterning process is the ability to use precise magnetic lens to focus the electron beam down to a spot size below 10 nm. However, the electrons accelerated through free-space (vacuum) will eventually encounter the resist and substrate with different scattering processes. The low density resist causes the electron beam to scatter laterally (forward scattering), and cause the beam's energy profile to grow radially as the beam goes deeper into the resist. Once the electrons hit a denser and tighter packed material such as the device substrate, back-scattering becomes an important effect. Back-scattering further spreads the electron beam energy density and starts cutting polymer chains as far as 100 microns away, which will ultimately lower the ultimate resolution of the tool.

Electron beam resists can be comprised of of different polymer chains and in effect, have a different sensitivity too beam energy exposure. The amount of charge dumped into the resist and substrate over a certain area is known as a dose. The "dose to clear" is the dose needed to dissolve away the entirety of a resist using a certain solution and development time. A resist that requires a lower dose to clear is said to be more sensitive than a resist that requires a higher dose to clear. Sensitivity is not only important for process window calibration, but the serial nature of the lithographic process will causes beam write times to depend on the resist sensitivity. For example, a higher sensitivity resist would result in a fast write time compared to a low sensitivity resist. Fortunately, it is possible to make up low sensitivity by developing the resist longer at the risk of the resist cracking due to mechanical stresses. The removal process of the resist is dissolution in a solvent, where the resist erodes away over the course of the development until it is completely removed. Because the electrons exposure cuts long polymer chains, a low dose will leave most polymer chains are intact. As the dose increases, the polymer chains become shorter and thus the rate at which resist is dissolved into the solvent increases.

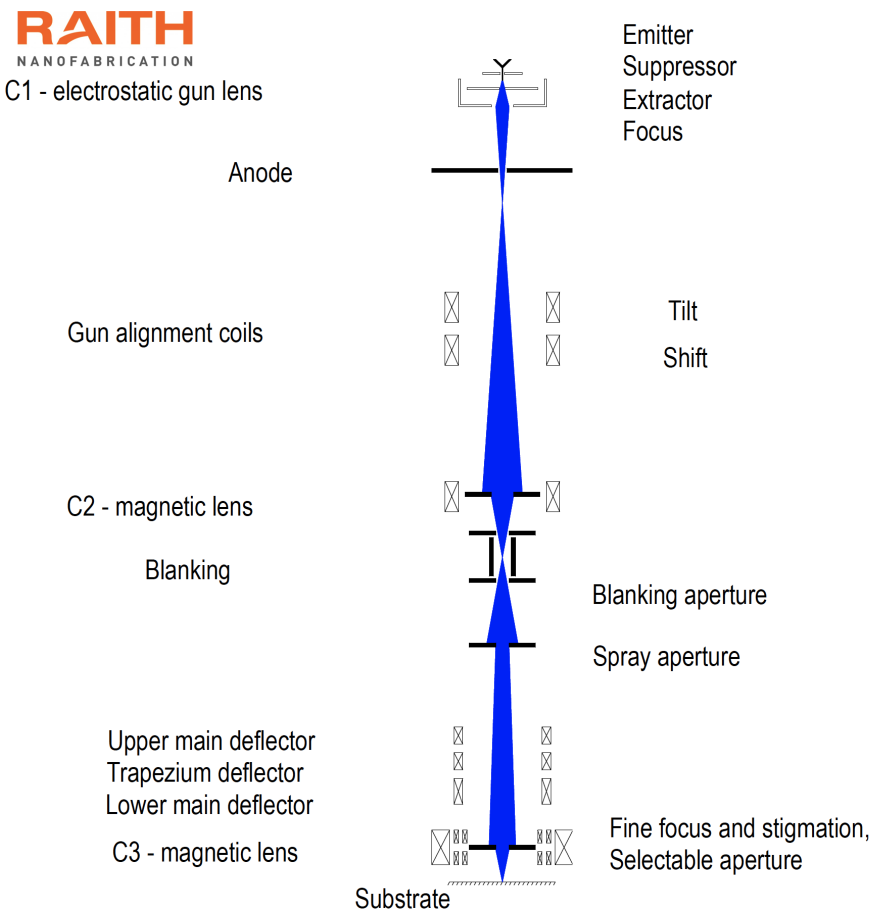


Figure 4.1: Schematic of the electron beam pattern. Adapted from Raith.

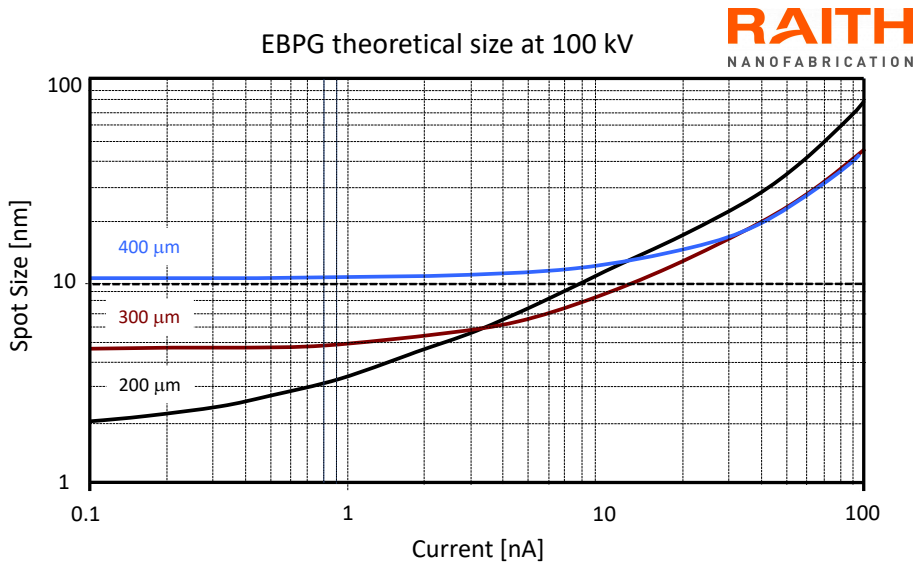


Figure 4.2: Theoretical spot sizes at 100kV in the electron beam system (with no beam deflection from center). Adapted from Raith.

Electron Beam Patterning

During the pattern exposure process, the pattern generator with high frequency digital to analog converters uses magnetic coils to deflect the beam and exposes point by point for a certain dwell time as shown in Figure 4.1. This single dwell time and location is called a shot. By stepping the location from one to another, the resist is exposed "shot to shot." This is where the term “writing on your sample” comes from and such a process can only be considered serial. The maximum frequency of the control electronics is set by:

$$f_{DAC} = \frac{I}{ds^2} \tag{4.1}$$

where f_{DAC} is the required frequency (typically MHz) to expose a shot with dose d (typically in μC/cm^2) and beam current I (typically pA or nA), given a beam step size of s (typically nm). The size of the step taken from shot to shot will depend on the full width half maximum of the beam. Due to the optical aspects (specifically the aperture used) of the beam writer, beam spot size will depend on the current used. Typically the spot size increases with high beam current. For example on the Raith 5200, the 100nA beam at 100keV will have a spot size of 60nm where as the 1nA at 100keV will have a spot size of 5nm, as shown in Figure 4.2. One way to combat this effect if a proximity effect correction, where a decrease in the dose at bulk of a pattern will prevent blow out at the corners.

Proximity effect correction is an important step to achieve ultimate process resolution. When the electrons arrive at the surface of the resist, the polymer chains causes the columnated beam to scatter through the resist. Such a scattering process effectively increases the beam spot size. The scattering energy profile as a function of the distance away from the beam center is characterized by a point spread function. There are two scattering processes. The forward scattering process describes a sight deflection from its original path. This process dominates in a soft material like resist. The back scattering process describes reflected electrons. This process dominates at the resist substrate interface. The substrate is less transparent to electron beam, and the back scattering process results in a wider distribution of energy in the resist layer. Monte Carlo simulations allow these processes to be modeled by tracing the path of each electron over a million times through the resist and substrate stack up. The point spread function is generated by integrating over the energy of these various paths and are parameterized with short range (0.1 - 1 microns), mid range (1 - 100 microns), and long range (100 - 300 microns) parameter. A point spread function can be inverted and applied to the beam dose pattern to account

for parasitic energy spread. This inversion process is the proximity effect correction.

4.2 Optical Lithography

Much like electron beam lithography, optical lithography is based on the principle of irradiating a particular energy flux (called the dose) of ultraviolet light to change the dissolution rate (called the development rate) of a polymer compound (called the resist) in a particular solvent (called the developer).

Compared to electron beam lithography there a some advantages to using optical lithography. Some of these advantages exist because optical remains the industry standard for defining patterns over large areas. With the advent of EUV, critical features can now be made as small as 13.5 nm. Instead of a direct write method as seen in electron beam lithography, the exposure process runs parallel through a mask, meaning that all features are exposed at once. Photoresists can be spun much thicker than their electron beam counterparts, and have good chemical etch resistance for silicon and silicon oxide etching. These two characteristics combined allow for deep (>200 micron) etches in silicon, and long (14 minutes plus) physical etches in silicon oxide. For example, the MEGAPOSIT SPR220 resist can spun 5 - 9 microns thick and used in a DRIE bosch process with a selectivity of up to 100:1, eliminating the need for an Al/Al_2O_3 or silicon oxide based hard mask.

Another useful technique of optical lithography is carried over from microelectromechanical systems (MEMS), where front-to-back alignment is possible with cameras on the underside of the wafer holder. This allows for backside etching (with alignment accuracy of microns, typical in low throughput mask aligners) of specific patterns matched to the front side.

4.3 Electron Beam Evaporation

Much like electron beam lithography, a high voltage power source can also be used to accelerate electrons for material deposition purposes. At a high currents, a filament (typically tungsten) will expel enough electrons towards a cooled and grounded metal crucible to sublimate the material. This sublimated material then evaporates onto the deposition stage.

The filament is out of the line of sight of crucible, so that evaporate contami-

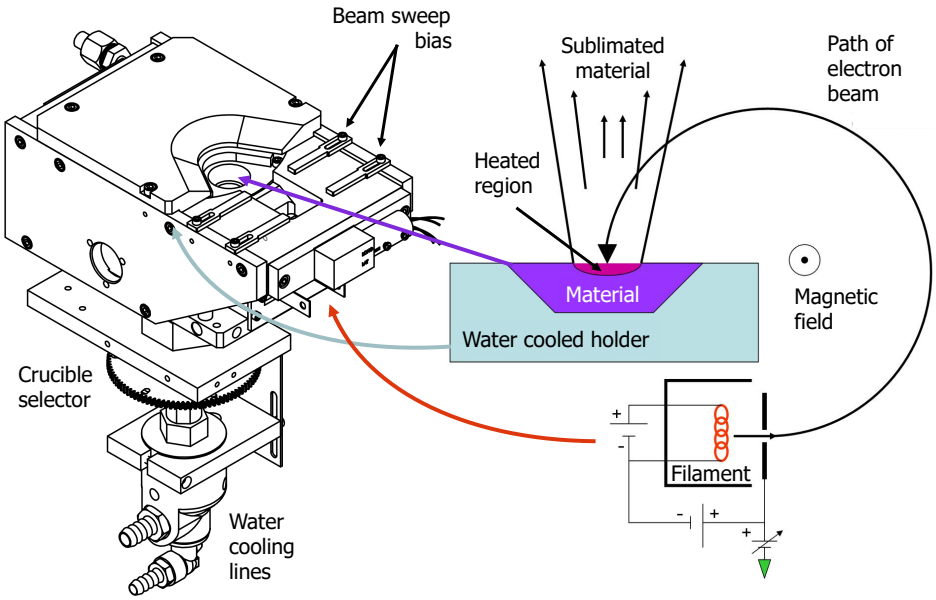


Figure 4.3: Schematic of electron beam deposition. Diagrams adapted [88] for this thesis.

nation onto the filament is minimized. The beam of electrons is steered with a magnetic field to a set the position of the on the material holder. Beam sweeps minimize the dwelling time of a beam at a single point and allows the material to be exposed equally across a larger surface area. Sweeping is important for metals such as titanium or niobium, which have a higher melting temperature (1941K and 2750K) and do not conduct well (11.4W/(m K) and 54W/(m K)) versus Aluminum (933K - 235W/(m K)).

Evaporation is done at low pressure to ensure high purity of deposition and due the long mean free path, the directionality of the deposition is line and sight. The beam of electrons hits the target surface and transfers its energy into thermal energy, which then heats up, melts, and vaporizes the material (also known as sublimation - the reverse process is called deposition), allowing it to precipitate on the surface of the substrate. The high directionality of electron beam deposition can be taken advantage of by installing substrate stages with rotation and tilt capability in the evaporation system. Applications of this capability include conformal depositions and angled evaporation, a key step to forming oxide barrier Josephson junctions for superconducting qubits. The process steps for these junctions are: pattern and

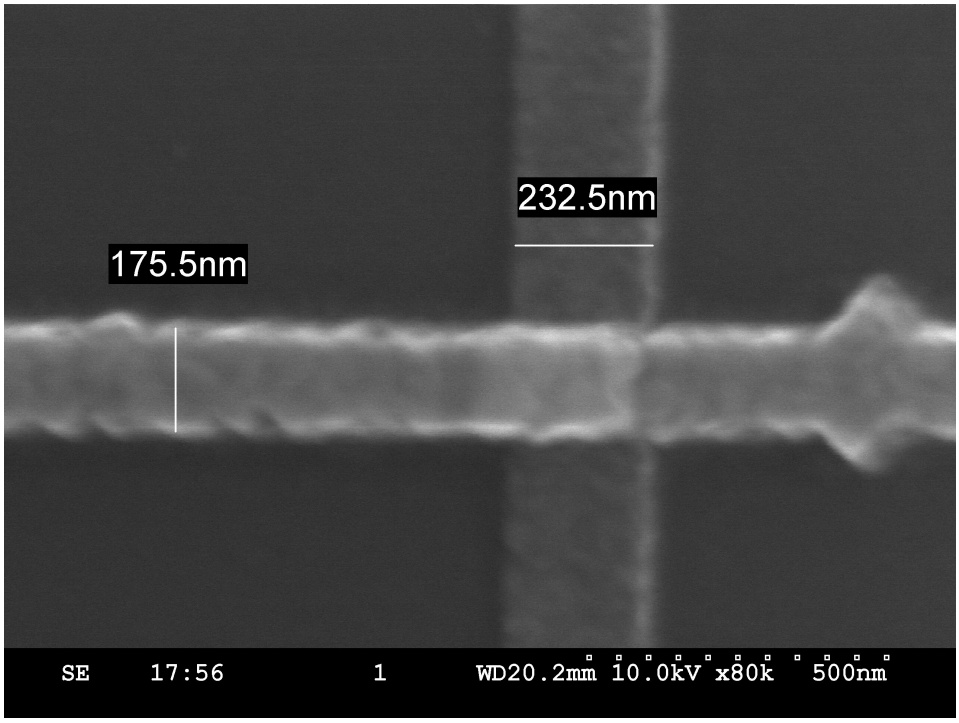


Figure 4.4: Josephson junctions formed by a bi-layer resist stack using the Manhattan method of angled deposition.

develop a resist structure that allows selective shadow deposition of your first and second junction electrodes, evaporate the first electrode layer with some defined stage rotation and/or tilt, flow oxygen into evaporation chamber to form the oxide barrier on top of the metal, evaporate the second electrode layer with a different stage rotation and/or tilt. There are two types of resist structures that can be utilized to allow for the shadowing and masking between the first and second electrode layers. The first type is a Dolan bridge, whereby a resist bi-layer is used with the top resist defining a shadow bridge [31]. This bridge defines areas which can be evaporated onto separately at different rotations and/or tilt. The second method is the Manhattan technique, which utilizes “streets” and “avenues” to allow for masking of each evaporation at steep enough orthogonal rotations, as shown in Figure 4.4. Sometimes, a third evaporation is used to improve the step coverage over the first oxidized evaporation layer. Argon milling, typically found ion based etch system, can also be included. Such milling is required when electrical contact needs to be made between two depositions. When substrate is vented to atmosphere and a native oxide grows on the metal. This oxide needs to be removed to prevent parasitic junctions and ensure good metal contact.

The etching of silicon and silicon oxide is typically done in a reactive ion etching tool. Reactive active etching is a process where ionized gases are accelerated back and forth to a etching surface, whereby these ionized gases can react in one of two ways. The first mechanism is physical, where the ions bombard atoms on the surface and knock them off. The second mechanism is chemical, were ions react and bond with their surface and are then pumped away as a volatile gas. Reactive etching is more commonly seen today with an inductively coupled plasma. Conventional reactive ion etching (RIE), where the ions are accelerated vertically up and down relative to the substrate, is a physical process where an increase in bias power will increase the kinetic energy of each ion. This kinetic energy, through ion bombardment, physically etches away the exposed top layer of substrate.

A higher ion density is achieved with inductively coupled plasma reactive ion etching (ICP-RIE). Inductively coupled plasma (ICP) serves to further ionize and increase the plasma ion density, so that the process etch type can be modified between physical and chemical. The chemical process is governed by the inductive plasma, because the plasma density is well controlled by the amount of power applied to magnetic coils. When process gases are excited with this magnetic coil, production of ions increase and ions move in a helical motion following the geometry of the coils. Increased power delivery (measured in watts) to magnetic coils will cause more ionization, and leads to a higher ion density in the plasma. A higher plasma ion density will react more frequently with atoms on the etching surface. The control of the ionization rate allows for control of the chemical reaction rate, or in other words, the rate at which ions react with the substrate surface. Thus, the ICP component of this etch does not accelerate these ions towards the sample. Rather, ions are generated away from the sample so that the acceleration of ions towards the substrate from the RIE (also known as the forward bias, and is set by the platen power) can control the physical aspect of the etch.

There are other controllable parameters in the ICP-RIE etch process. For example, table can be temperature controlled to control the chemical reaction rate of active species. In certain processes that require extremely low reaction rates, temperatures can be set to as low as -140 degrees C [100]. A helium backing pressure is also set to adhere a wafer to the table and creates a a thermal connection between the wafer and the table. With poor helium backing, the inert helium gas leaks onto the

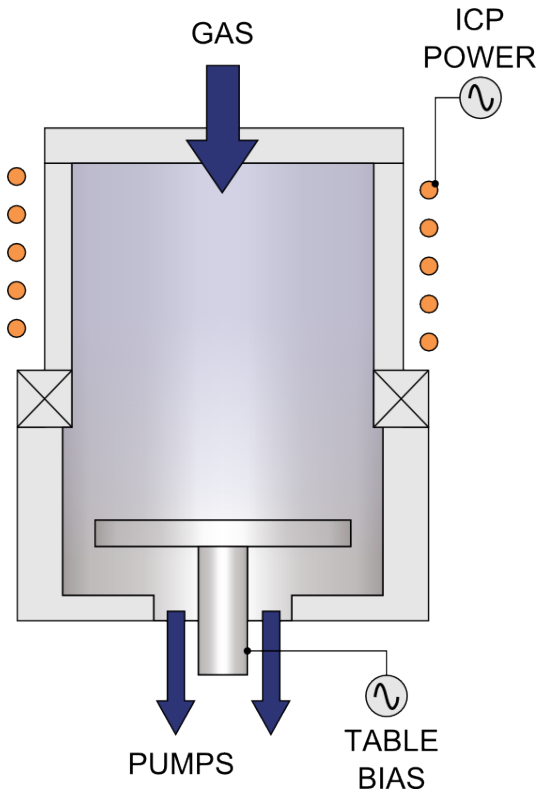


Figure 4.5: Schematic of reactive ion etching with inductive coupled plasma. Diagrams adapted from Oxford Instruments.

edge of the wafer and changes the reaction rate of the etch. Thus, helium backing pressure is an important parameter to monitor. A sufficient helium backing also aids to regulate the wafer temperature. Increasing the wafer temperature increases the rate of the etch. Very high temperatures on the wafer will also melt and deform a photoresist mask.

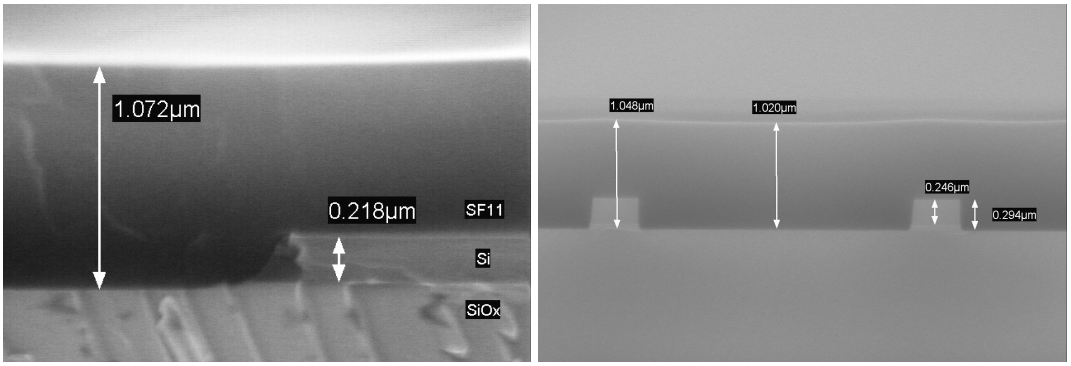
4.4 Plasma Etching

Silicon Etching

Typical silicon etches include etching and passivisation gases such as SF_6 and C_4F_8 respectively. The fluorine atoms in SF_6 chemically bond with silicon atoms to form SiF_4 and are pumped away by a vacuum pump. Isotropic etching, which etches away the material uniformly in all directions, can be achieved with just SF_6. Anisotropy (non-uniformity) is desired when the etch needs to maintain a constant profile relative to the etch plane. The carbon atom in C_4F_8 form a passivation layer and are

harder to etch. Another combination of processes gases include CF4 and O2 for etching and passivation respectively. The combination of an etch and passivation gas allows for two methods types of etching that is anisotropic.

There are two ways to achieve anisotropy. The first type of process is the Bosch process, where SF_6 and C_4F_8 are alternated serially. An isotopic chemical etch with SF_6 is done first, followed by a passivation layer of C_4F_8. Fast etching rates with vertical profiles are possible with high SF_6 gas flows and a strong passivation provided by C_4F_8. The second type is a pseudo-Bosch, whereby the Bosch process is made continuous by flowing in the etching gas and passivation gas simultaneously. In the case of SF_6 and C_4F_8, both gases are let into to the chamber at a specific ratio such that the edge profile is vertical, seamless, and continuous.



(a) Edge of etch front through the silicon device layer.

(b) Isolated islands of silicon etched on SOI.

Figure 4.6: Profile of silicon etches using a pseudo-Bosch process when etching through the ≈ 220 nm silicon device layer on SOI.

Silicon Oxide Etching

Silicon oxide is typically used as an etch mask for other materials. Thus, etching silicon oxide is both a necessity and difficult at the same time. Because of silicon oxide's high etch resistance, a very physical etch is needed. In fact, the combination of C_4F_8, typically a passivation gas, with O_2 works well to etch silicon oxide under very high ICP powers and very high forward bias voltages. The oxygen in this etch serves the burn away any organic residue that may cause micro-masking. Typically, if the oxygen pressure is too low, then any unintended masks such as photoresist will create a grassy texture on the substrate. Residual photoresist may come from

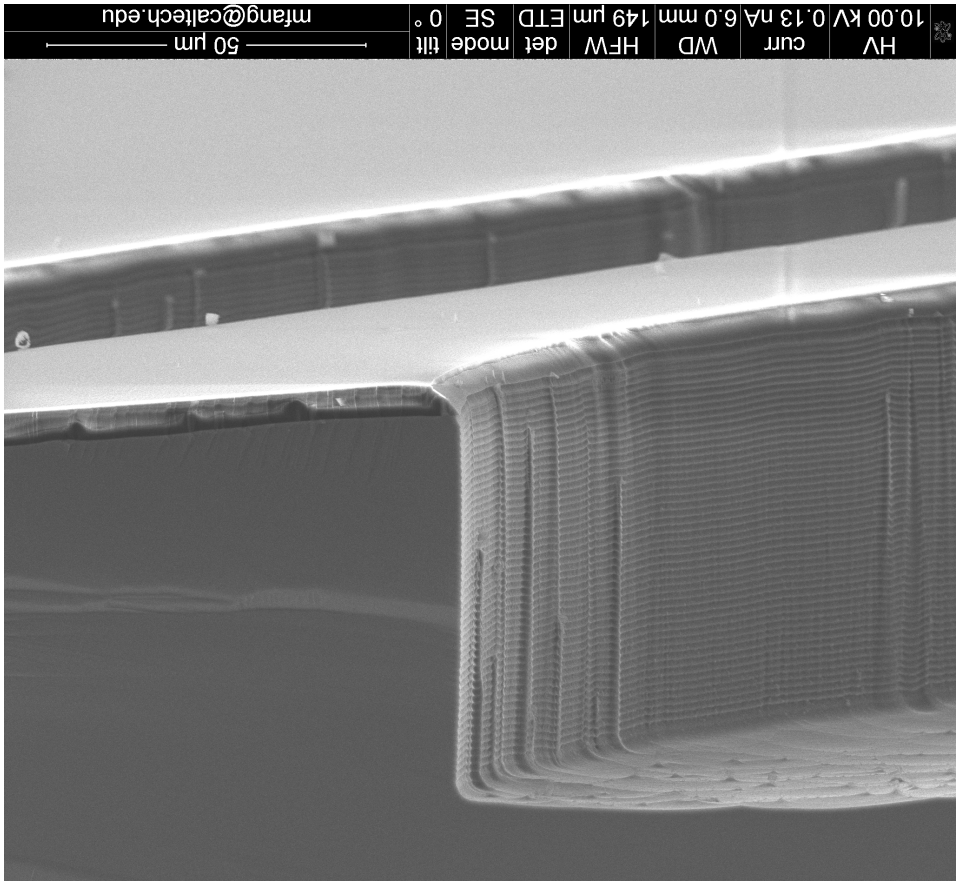
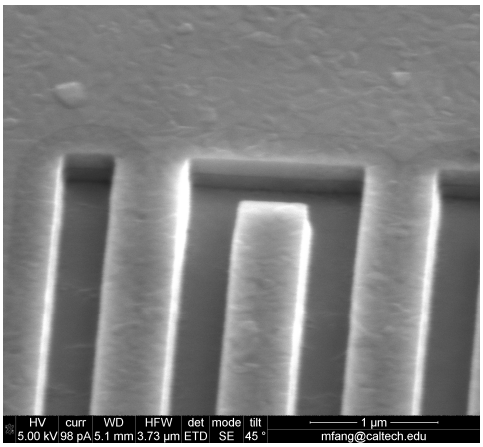


Figure 4.7: Deep reactive ion etching (DRIE) using Bosch process with a MEGAPOSIT SPR220 7.0 resist used as an etch mask. Each horizontal band indicates a cycles in the Bosch process.

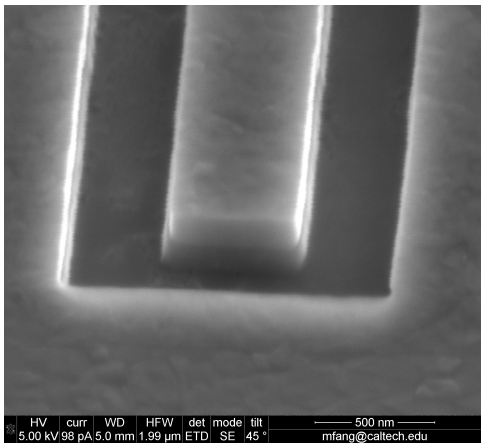
processes where the resist may not have been fully developed. However, if one increases the oxygen content in the plasma, free radicals can burn away any organic residues and prevent micro-masking. One should be careful when increasing oxygen content in this etch. Depending on the selectivity of the resist etch mask, the resist stack will be etched quicker with increasing oxygen flow, and as a result decrease the selectivity of the etch.

Aluminum Etching

The etching of aluminum is possible with a combination of BCl_3 and chlorine gas (Cl_2). The primary purpose of BCl_3 is to break through the native oxide layer of aluminum. In circumstances where BCl_3 is not available, a combination of argon and chlorine can be used. In some cases, the incorporation of methane and hydrogen into the etch can serve as a passivation layer to produce more vertical sidewalls. The reactive etching process with inductive coupled plasma allows for a wide range of



(a) Aluminum fingers etch through into the underlying silicon.



(b) Close up view of the etched aluminum on top of silicon.

Figure 4.8: 3 minute etch of aluminum on silicon using the parameters in table F.1

etches and etch rates using different processes. Because of the largely independent control of the chemical and physical components of the etch, many other materials such as niobium [43], sapphire [47], and germanium [40] can be processed using this technique.

4.5 Anhydrous Hydrofluoric Etching

Another etch technique uses hydrofluoric acid (HF) in its anhydrous vapor phase. Although wet HF has been used frequently in the past to etch silicon through the following chemical reaction,

$$2HF + SiO_2 \rightarrow SiF_4 + 4H_2O \tag{4.2}$$

an issue arises for suspended structures. During the removable of the sacrificial oxide layer in an aqueous solution, the surface tension of water causes the capillary forces to push the suspended structure towards the underlying substrate. Also known as stiction, the once suspended structure sticks to the substrate. Before anhydrous etching, the solution this problem was to keep the release structure submersed in a liquid, typically a solvent like isopropyl alcohol, before dehydrating in a critical point dryer. The critical point dryer bypasses the triple point of water, allowing the liquid to be removed without the effects of stiction.

Alternatively, an anhydrous vapor process lets in a mix of anhydrous (without water) HF, along with ethanol to react with the silicon oxide. As seen from the chemical reaction in Eq 4.2, the reaction is terminated by the presence of water. The role of

ethanol is to act like a catalyst for the reaction by removing the excess water and allowing the reaction to continue. Because this process relies on the lack of water on your device, drying your sample before placing it in a vapor HF tool is critical. The ratio of the ethanol to HF is also important, as the correct balance is needed to satisfy and properly dehydrate the sample to allow the chemical reaction to continue. Another important parameter is the process temperature. The HF needs to stay in its vapor phase, otherwise corrosion of the tool will occur and contaminate samples. The etch rate also depends on the process temperature and pressure. Therefore, we need to operate at a set pressure and temperature, which ensures that all process gases remain in vapor form. The etch rate goes down with temperature and the etch rate goes up with pressure. This process is not a physical process, because it relies on adsorption for the chemical reaction to take place, and thus the ethanol catalyst is critical to removing the local presence of water. The anhydrous nature of the etch also allows selectivity against materially that would typically be etched in a aqueous form of HF, such as aluminum oxide (Al_2O_3), where the reaction goes as

$$Al_2O_3 + 6HF \rightarrow 2AlF_3 + 3H2O \tag{4.3}$$

In anhydrous vapor HF etching, Al_2O_3 [83], along with other materials such as Al, Au, Ni, Pt remain un-etched, allowing more possibilities for processing.

Chapter 5

SUPERCONDUCTING QUBITS ON SILICON AND SILICON ON INSULATOR

5.1 Basic Qubit Design

As discussed in Section 2.2, the qubit is comprised of capacitive and nonlinear inductive components. The corresponding energy associated with these components are

$$E_J = \frac{\Phi_0}{2\pi} I_C = \left(\frac{\Phi_0}{2\pi}\right)^2 \frac{1}{L_q \cos\phi}; \quad \Phi_0 = \frac{\hbar\pi}{e} \tag{5.1}$$

$$E_C = \frac{e^2}{2C_q} \tag{5.2}$$

where E_J and E_C are the Josephson and capacitive energies respectively. The critical current density is set by fabrication parameters, such as oxidation pressure, chamber vacuum pressure, oxidation time, and even possibly the metal evaporation rate (of which can change the surface roughness of the oxidation surface). The junction inductance can be varied across a range of values by changing the junction area. For typical junction processes with a critical current density of $0.344\mu A/\mu m^2$, typical junction inductance values are shown in Figure 5.2. A transmon architecture ensures that the qubit is insensitive to charge noise by adding a large shunt capacitance between the two leads of the superconducting loop, comprising a pair of Josephson junctions. This insensitivity ensures that any charge fluctuations on the qubit capacitor will not induce dephasing through frequency fluctuations. The addition of the shunt capacitance brings the Cooper pair box closer to the flux qubit, where the qubit becomes more sensitive to flux noise. However, due to the large shunt capacitance, we are still able to control and readout the qubit through capacitive means, and take advantage of its insensitivity to charge noise. As a trade off, we no longer have to work in the "sweet spot" of gate charge as seen in the Cooper-pair box. Instead we operate at a different sweet spot called the flux insensitive point. For practical quantum computation, allowing for two qubit gate interactions requires the tunability of transmon. Otherwise, transmons can be made without flux tunability (with just a single junction) which is more protected from flux noise (although magnetic spin fluctuations on the surface near the junction may still affect dephasing). In the

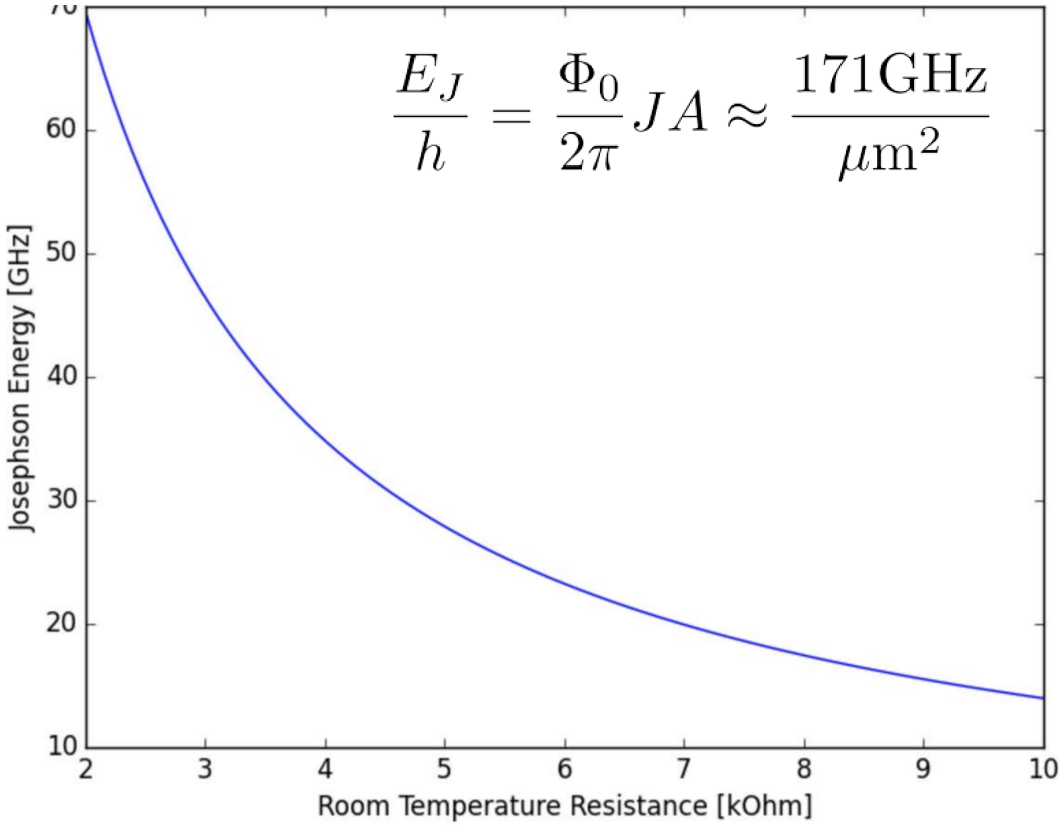


Figure 5.1: The inferred Josephson energy E_J over the resistance measured at room temperature.

transmon regime where $E_J/E_C \gg 1$, we label each energy level E_m [51]:

$$E_m \approx \sqrt{8E_J E_C}\left(m+\frac{1}{2}\right) - E_J - \frac{E_C}{12}\left(6m^2+6m+3\right) \tag{5.3}$$

$$= \frac{\hbar\omega_q}{\sqrt{\cos\phi}}\left(m+\frac{1}{2}\right) - \left(\frac{\hbar}{2e}\right)^2 \frac{1}{L_q\cos\phi} - \frac{e^2}{2C_q}\left(\frac{m^2}{2}+\frac{m}{2}+\frac{1}{4}\right) \tag{5.4}$$

$$\Rightarrow E_{01} \approx \frac{\hbar\omega_q}{\sqrt{\cos\phi}} - E_C \tag{5.5}$$

$$\Rightarrow E_{12} \approx \frac{\hbar\omega_q}{\sqrt{\cos\phi}} - 2E_C \tag{5.6}$$

where the anharmonicity is $\alpha = E_{12} - E_{01} \approx -E_C$. The anharmonicity is an important aspect of qubit design because it ultimately sets the minimum gate speed allowed before exciting higher level states. This is due to the Nyquiest condition that implies a qubit control pulse (typically on the order of ten nanoseconds) has a narrower line width in frequency space relative to the anharmonicity of the qubit. If the line width is too wide, then the probability of an unwanted transition increases substantially, resulting in increased gate errors through leakage into higher states. It

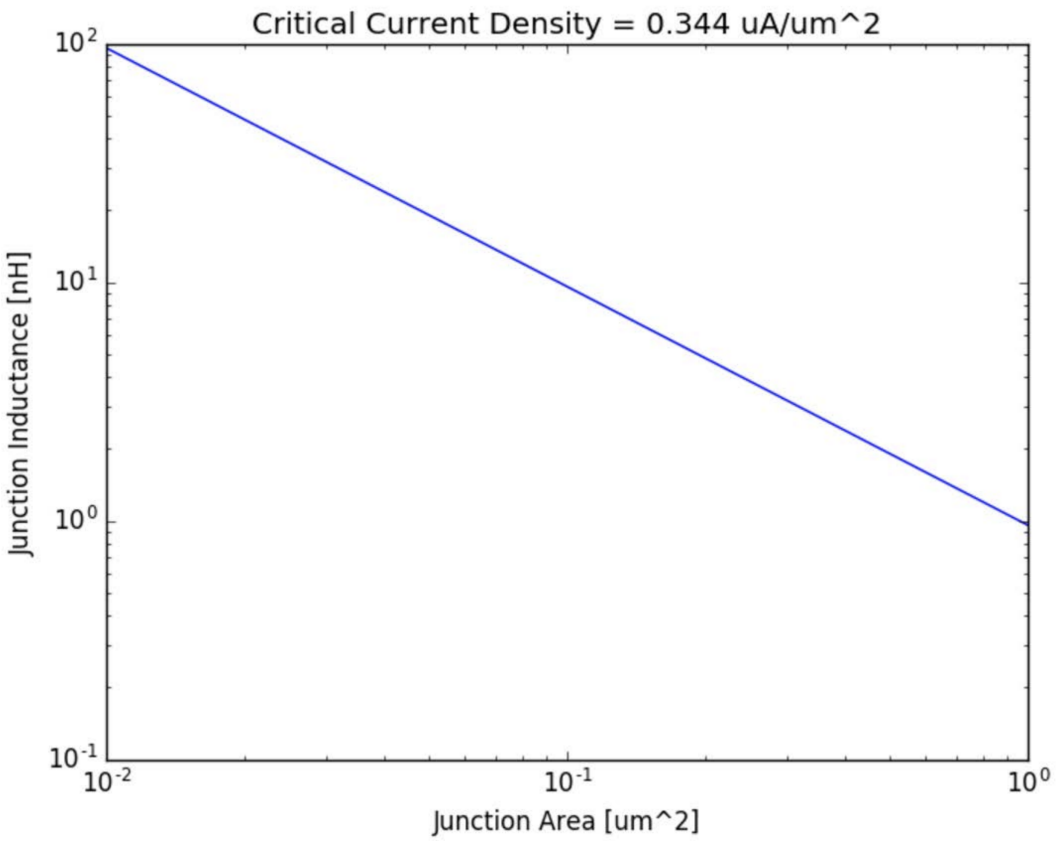


Figure 5.2: The inferred Josephson inductance over the junction area assuming some critical current density of $0.344 \mu A/\mu m^2$.

is however possible to push these gate speeds faster with the use of complex pulse shaping techniques, such as DRAG [71][26] to cancel out high order transitions when performing faster gates.

As discussed in Section 3.1, we must take care to design the right amount of coupling from our control lines to the qubit. Ultimately, the speed of the gate will depend said coupling, the fridge wiring and attenuation, as well as the maximum power output of your digital to analog converters. Designing a highly coherent qubit will limit how well we can couple into the system. Instead, the optimization of output power on control electronics is preffered. A more detailed discussion of qubit gates and drive power is covered in Section E.

Coupling to the readout cavity

In the dispersive limit, where g is small compared to a large cavity detuning Δ, the dispersive shift [87] of the cavity frequency is

$$\chi = -\frac{g^2}{\Delta}\frac{\alpha}{\alpha+\Delta} \approx -\frac{g^2}{\Delta^2}\alpha \text{ for } |\Delta| \gg |\alpha| \tag{5.7}$$

where the coupling g (derived in Section B) between the qubit and the resonator with RLC capacitances C_Q and C_R respectively, is

$$g = \frac{\sqrt{f_Q f_R}}{2}\frac{C_c}{\sqrt{(C_Q+C_c)(C_R+C_c)}} \tag{5.8}$$

where the anharmonicity is α, which for a transmon is $\approx -E_C$. Note that the qubit energy decay due environmental coupling via the readout resonator can be written

$$\Gamma = \frac{g^2}{\Delta^2}\kappa = \frac{g^2}{\Delta^2}\frac{1}{T_1} \tag{5.9}$$

The readout resonator will resonant at one of two frequencies $\omega_{|0\rangle}$ or $\omega_{|1\rangle}$ where $\omega_{|0\rangle} - \omega_{|1\rangle} = 2\chi = \frac{2g^2}{\Delta}$. For a probe tone parked at $\omega_p = (\omega_{|0\rangle} + \omega_{|1\rangle})/2$, halfway between the two frequencies, maximum readout visibility is achieved when[87]

$$\chi = \frac{\omega_r}{2Q_l} \tag{5.10}$$

where Q_l is the loaded quality factor of the readout resonator. We see that a lower resonator quality factor is desirable for a larger dispersive shift. We see now that minimizing the decay rate requires us to increase the non-linearity of the qubit since

$$\Gamma = -\frac{1}{\alpha}\frac{\omega_r\omega_q}{2Q_lQ_q} \tag{5.11}$$

The value for Q_l is chosen to balance visibility from χ and coherence time from $\omega T_1 = 1/\Gamma$ [87].

5.2 Silicon Substrate Design and Fabrication

A layout of qubits on silicon substrate is depicted in Figure 5.3, where a feedline interrogates a readout resonator that is coupled to the qubit capacitor. An XY drive line allows for excitations to excite the qubit between the $|0\rangle$ and $|1\rangle$ state. Keeping in mind the loss limits to maximize the qubit lifetime, the parameters listed in Table 5.1 where chosen for this design.

Table 5.1: Silion qubit design parameters.

Parameter	Design	Simulation/Inferred
Qubit Capacitance	70 fF	67.1 fF
SQUID Inductance	11nH	≈11 nH
Readout Frequency	7.0 GHz	6.9 GHz fF
Readout Capacitance	8.0 fF	8.07 fF
Qubit XY Drive	50 aF	52 aF
Qubit Z Mutual	2.0 pH	1.3 pH
Qubit Z Parasitic	0.1 pH	0.3 pH

5.3 Control Electronics and Measurement Setup

Following the measurement diagram in Figure 5.3, the cryogenic measurement setup involves a combination of microwave electronics, filters, attenuates, mixers, and circulators. A 14 bit arbitrary waveform generator generates in-phase (I) and quadrature (Q) components of a signal at some intermediary frequency of 100 MHz,. This signal is shaped with a cosine envelope for qubit readout and driving. I and Q components are passed into IQ mixers for driving with local oscillator carrier tones provided by separate microwave sources for drivig and readout. IQ mixing allows us to multiple frequencies into a single sideband. The signal is attenuated and filtered at several temperature stages of a dilution refrigerator, to reduce the coupling of Johnson noise from the higher temperature stages (see Appendix D.1).

The flux tuning of the qubit Z control line is provided by a DC source with its output filtered at 4 K with a cryogenic dissipative RC low pass filter and again at the mixing chamber plate with a reflective LC filter. The device is mounted on a gold-plated PCB inside a copper box inside two concentric magnetic shields. A shield on the mixing chamber is painted in an IR absorber mixture [7].

The output is protected from room-temperature noise by two circulators. A high electron mobility transistor amplifies with a noise temperature of 3 Kelvin. Two room temperature power amplifiers were used to further amplify the signal to higher levels. The readout signal is then downconverted with IQ mixers and the resulting demodulated tones are simultaneously digitized using a digitizer. The semi-rigid coaxial cable is made from stainless steel between 300 Kelvin and 4K, with a niobium titanium (NbTi) alloy used between 4 Kelvin and the base temperature plate. Stainless steel is used above 4K for its low thermal conductivity. Below 4K, NbTi outperforms stainless steel with a lower thermal conductivity - preventing the low

temperature stages from heating up from the higher temperature stages. NbTi is also superconducting below 10K, making it also an ideal low loss cable.

5.4 Silicon Qubit Characterization

The first step to qubit characterization is finding the readout resonator. The readout resonator has a power dependent response to when coupled to a qubit, and the resonator's dispersive shift will depend on the qubit's detuning relative to the resonator as seen in Figure 5.4. Thus, the easiest and quickest way to check for the presence of a qubit is to do a power sweep, to check the dispersive shift imparted on the resonator at low powers when the qubit is not saturated from the microwave photons in the readout resonator. Another easy check is to vary the applied flux to the loop of the SQUID, thereby tuning the frequency, which then changes the detuning between the qubit and resonator, and thus effectively changes the dispersive shift of the resonator. The periodicity of the dispersive shift will also inform the mutual coupling between the flux line and the qubit bias loop, as well as the sweet spot where the qubit is most insensitive to flux noise.

Continuous Wave Spectroscopy

We can now choose to park the qubit at a desired location in the tuning period and look for the qubit's excited frequency by sweeping the XY drive frequency and measuring the readout resonator response as shown in Figure 5.5. At high XY drive power, the desired 0 to 1 transition is saturated and higher order transitions can be seen. Since the dispersive shift is linear for higher order transitions, we can fit and back out the anharmonicity of the qubit α and see that it matches well for two photon transitions, such as from the 0 to 2 state. The qubit linewidth at high power is broad, allowing for the qubit to be easily seen. As we lower the drive power, the qubit's line width will become narrower and narrower until the bare linewidth (depending on the lifetime of the qubit) can be seen. At very low drive powers, we can start to precisely map out the frequency tuning curve as a function of current bias on the Z line. However, using a DC source as a bias tool is non-ideal for these frequency sweeps. This is due to the fact that by changing the qubit frequency, the readout resonator frequency also changes. Since doing a three dimensional sweep is costly, the resonator's response to the qubit must be calibrated for as we change the flux bias, so that we only need to interrogate the readout resonator's amplitude or phase response at a single frequency to determine whether or not a dispersive shift has

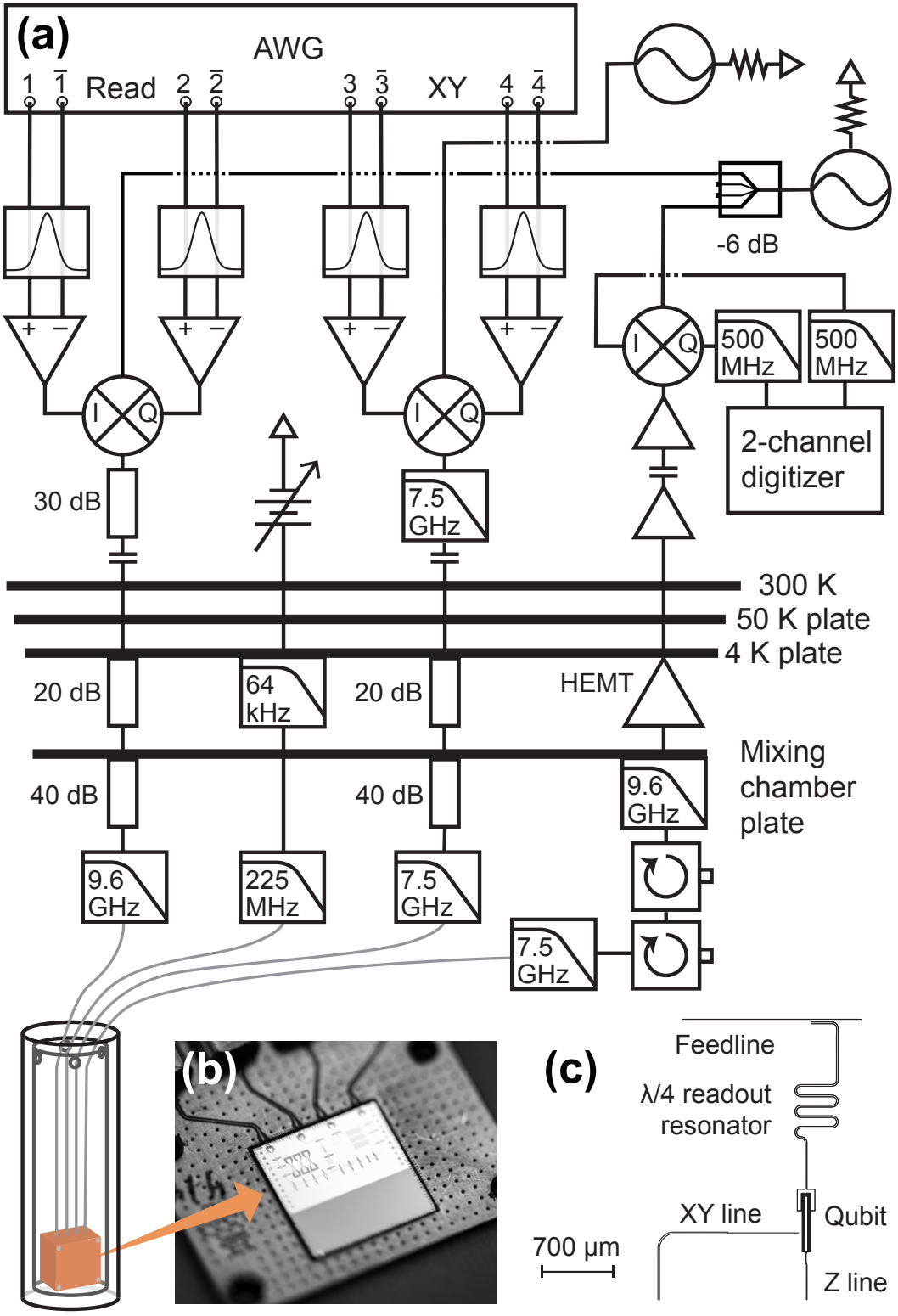


Figure 5.3: Fridge setup and measurement wiring. Adapted from [48].

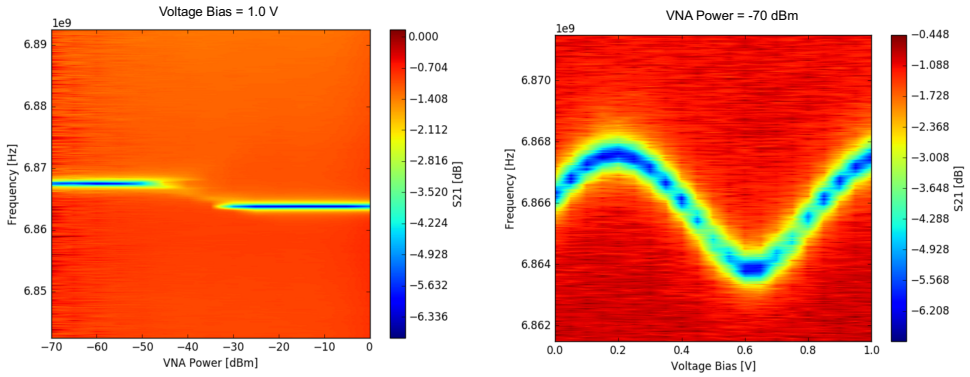


Figure 5.4: Readout resonator frequency shifts due to readout power and qubit frequency detuning.

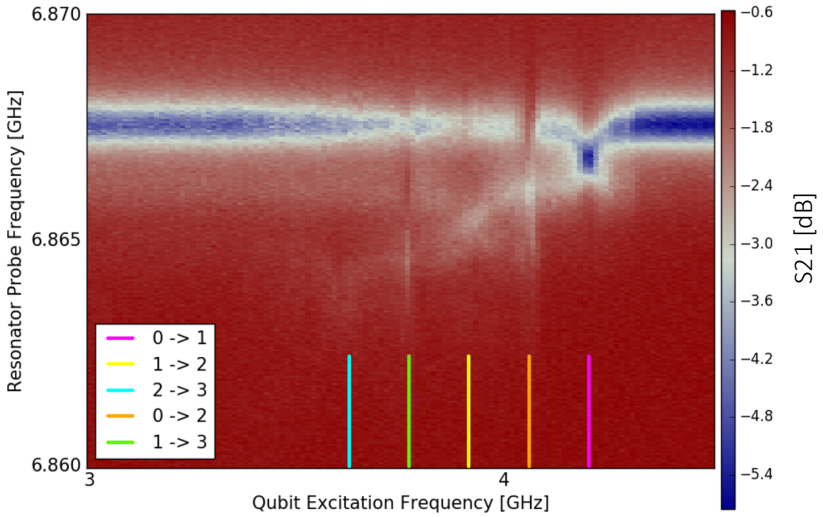


Figure 5.5: Readout resonator response at high qubit drive power. The state transitions are labeled and marked in frequency space.

occurred.

As we start to incorporate more complex characterization methods, the continuous wave approach with a network analyzer with constant excitation of the qubit starts to require not only long acquisition times, but a limit for controlling and measuring the qubit efficiently. Thus, we move to a different spectroscopy technique that relies on gating and quick acquisition times.

Time Domain Pulsed Spectroscopy

The readout resonator response seen on a network analyzer can be measured and interpreted in the same way using pulsed waveform on the arbitrary waveform generator. Internally the network analyzer generates an IF tone (for a duration set by the inverse of the IF bandwidth - i.e. 1μs corresponds to an IF bandwidth or frequency of 1MHz) which is up-converted with mixers to the desired measurement frequency. Then the signal arrives at the other port the signal is down-converted and a demodulation (using integration over the IF bandwidth) to a DC amplitude and phase give the real (in phase) and imaginary (quadrature) components of the signal. In essence, the network analyzer measurement is performed in the same way, expect with the possibility to use a higher IF bandwidth, on the waveform generator and digitizer setup. The real advantage to pulse spectroscopy in the time domain is the ability to have precise control over the excitation of the qubit.

In continuous wave spectroscopy, the constant excitation of the qubit between the 0 and 1 state averages out, and we see the average readout resonator response. In time domain, we can design a pulse that excites the qubit along any probability between the 0 and 1 state, where the readout resonator will display statistics and give probabilities of either being in the 0 or 1 state. For example, in Figure 5.6, the readout resonator response is shown for a qubit excited its excited state (via a pi pulse) or a qubit that has remained in the ground state (where no pi pulse is applied). This pulse is applied immediately before the readout tone, and does not give any time for the qubit to relax. The resonator shifts down in frequency as expected when the qubit is excited. Since we are concerned about acquisition time, we can either park the readout interrogation frequency in the middle of the two resonant dips and look at the phase response, or park the interrogation tone in the dip of the ground state dip, such that any change in the qubit state will be reflected in the amplitude response.

One aspect of the readout resonator measurement that one should keep in mind is that the interrogation must be done at low powers - one cannot simply increase the measurement power to increase signal to noise, or to decrease acquisition time. This is because of two factors: 1) the presence of n photons in the readout resonator

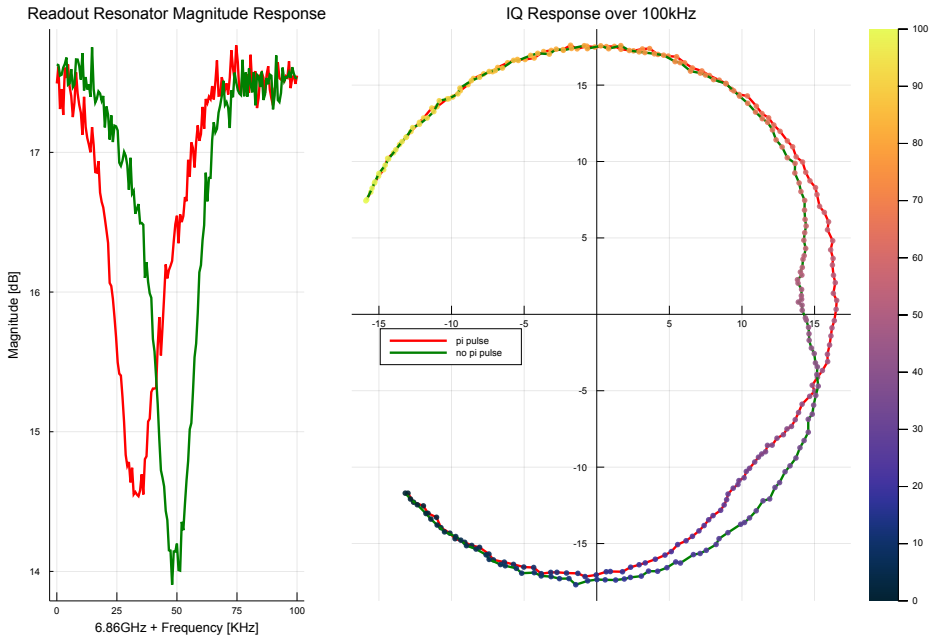


Figure 5.6: Low power readout resonator response for the ground and excited states of the qubit.

will shift the quit frequency as $n\chi$, and 2) the high drive powers will start driving various transitions from one level to another. This effect is seen in Figure 5.7, where a high power readout tone is generating false negatives for the case where we apply pi pulses to excite the qubit. We see that there is a mix of the qubit being the ground state and the excited, due to these high power readout tones driving parasitic transitions between 0 and 1.

When we park the readout tone to obtain the amplitude and phase response and gather statistics over many measurements, we can plot the distribution of our measurement signal in the in phase and quadrature (IQ) plane. For qubits prepared in the ground state, the measurement signal clusters around a cloud, and for qubits prepared in the excited state, the measurement signal clusters around another cloud as shown in Figure 5.8. The variance of these clouds is set by the signal to noise ratio, and if we're limited by quantum noise, the uncertainty principle of quantum mechanics. We find the centroid of these distributions and label them based on the prepared state - blue for a qubit prepared in the ground state and red for a qubit prepared in the excited state. We use the location of the centroids in the IQ plane to generate a perpendicular bisector, in which we use to infer statistics on the qubit

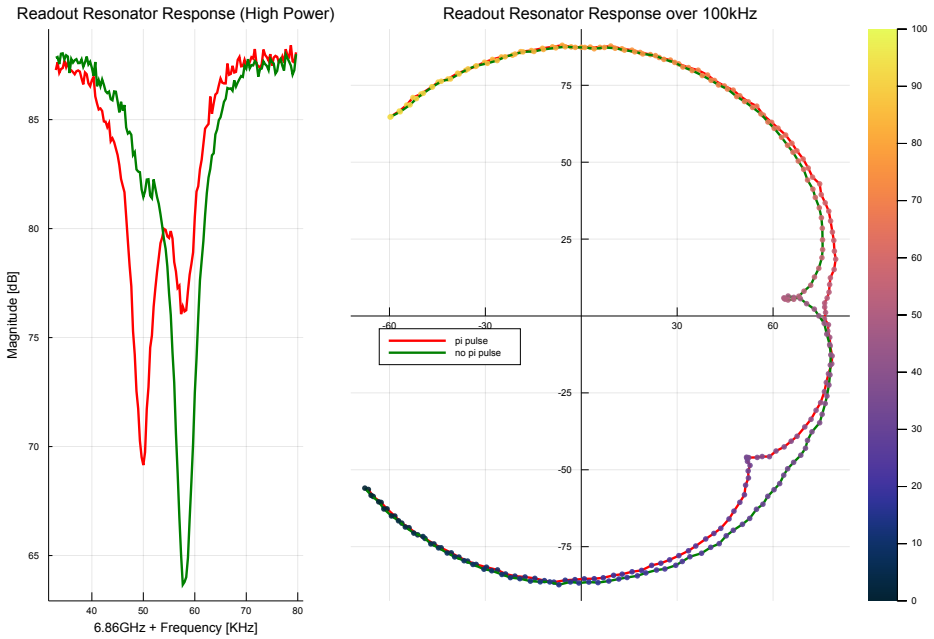


Figure 5.7: High power readout resonator response for the ground and excited states of the qubit.

population. For points that lie on one side of the bisector, we will label these as excited states, and for the others we will label them as ground states. The qubit population is those the fraction of signal that are classified as excited (lying on one side of the bisector) of the total number of signal points. For qubits that were prepared in the excited state, but measured to the be in the ground or vice versa, we can obtain our state preparation and measurement (SPAM) errors, which is used in randomized benchmarking to characterize gate fidelity [50].

In addition to measuring qubit state populations, we can also optimize our qubit excitation pulse using Rabi spectroscopy. For an optimal and fixed readout frequency, as well as a fixed qubit frequency, we can sweep the excitation frequency and pulse length and see swap dynamics on and off resonance with the qubit as shown in Figure 5.9. The IQ data was rotated specifically such that the real part of the readout signal would be "noisy." In fact, this is just a consequence of a change of measurement basis in the IQ plane, and why it is also preferred to gather state population statistics from centroids in the IQ plane. If only one of the two axis in the IQ plane is used to measure, then the state data could be "hidden" along a different axis of measurement as demonstrated. Alternatively, it could also be the case, depending on where the

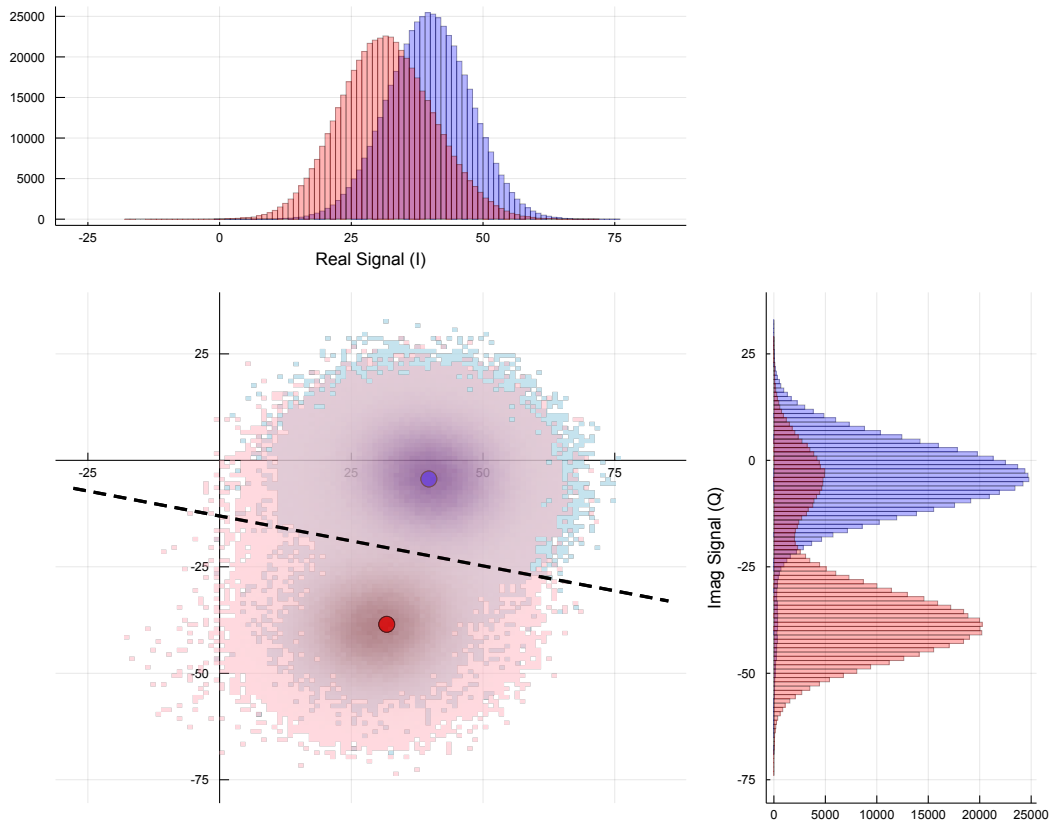


Figure 5.8: Ground (blue) and excited (red) state measurement statistics in the IQ plane from the readout resonator response after demodulation to DC.

readout interrogation tone is parked that the state data could be "hidden" in either the magnitude or phase response of the signal.

To understand the dynamics of the qubit state, we can take line cuts of Rabi spectroscopy measurement. As indicated by the line color at the center, off center, and far away, we can see swapping of the qubit state between the ground and excited centroid in the IQ plane with different various drive frequency detunings in Figure 5.10. For on resonant excitations, the qubit flops fully between the ground and excited states. However, when moving slightly off resonance, the qubit only flops partially to the excited state and decays away slowly over time. For a far off resonant pulse, the qubit remains largely in the ground state.

From the two previous measurements, we can optimize our excitation pulse and readout for characterizing the lifetime and coherence of our qubit. We first use

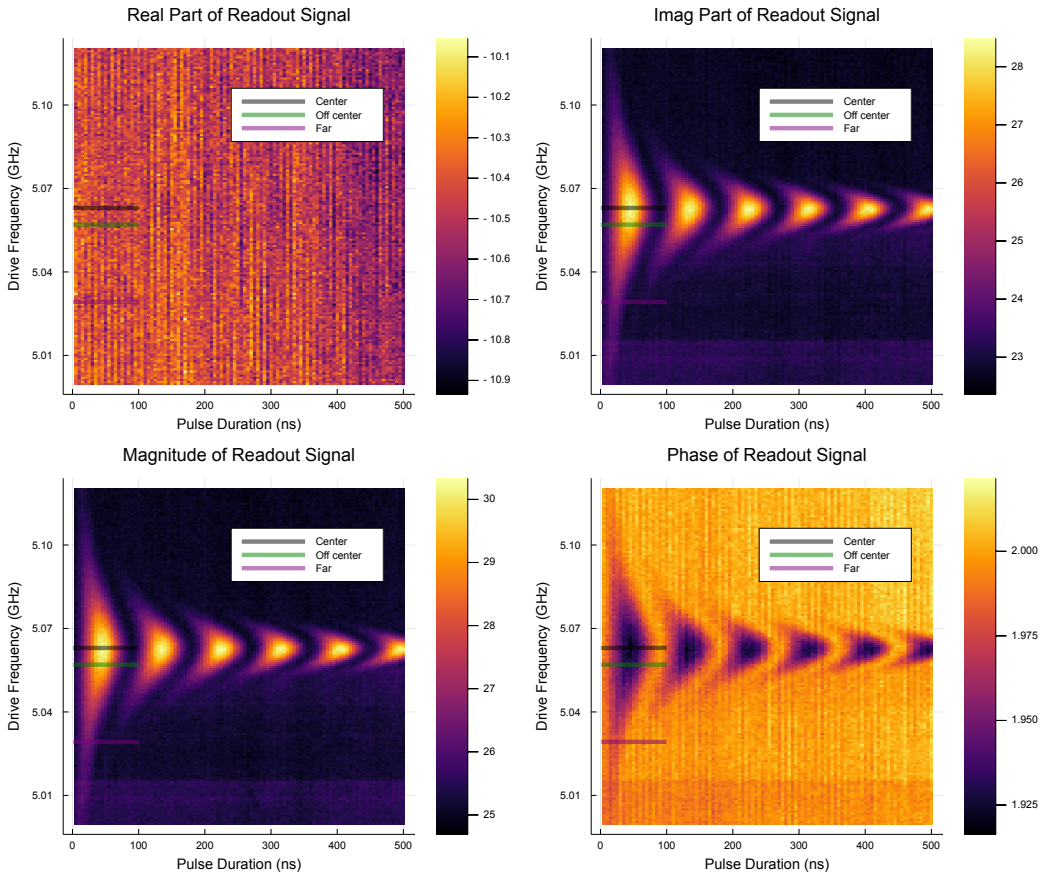


Figure 5.9: Rabi flop response using four different intepretations

Rabi spectroscopy to optimize our excitation pulse, also called a π pulse, since the qubit undergoes a π rotation on the Bloch sphere which represents the transition from the ground to excited state. Next, we can optimize our readout by choosing a readout frequency that maximises the accuracy of the readout, i.e. for any qubit prepared in the ground state, the resonator has the best statistics for being shifted up in frequency, and for any qubit prepared in the excited state, the resonator has the best statistics for being shifted down in frequency.

Now we can perform T1 and T2 measurements, which along with gate times and gate fidelity, can give us metrics for how well a qubits can perform useful computation. The pulse sequence is laid out in Figure 5.11. For a T1 measurement, we wish to measure the qubit's ability to retain its energy in the excited. Thus, we apply a π pulse and sweep a delay parameter τ to measure the probability that the qubit is excited over time. Using a Ramsey pulse sequence, a T2 measurement looks to characterize the qubit's ability to stay phase coherent - that is: how stable qubit's

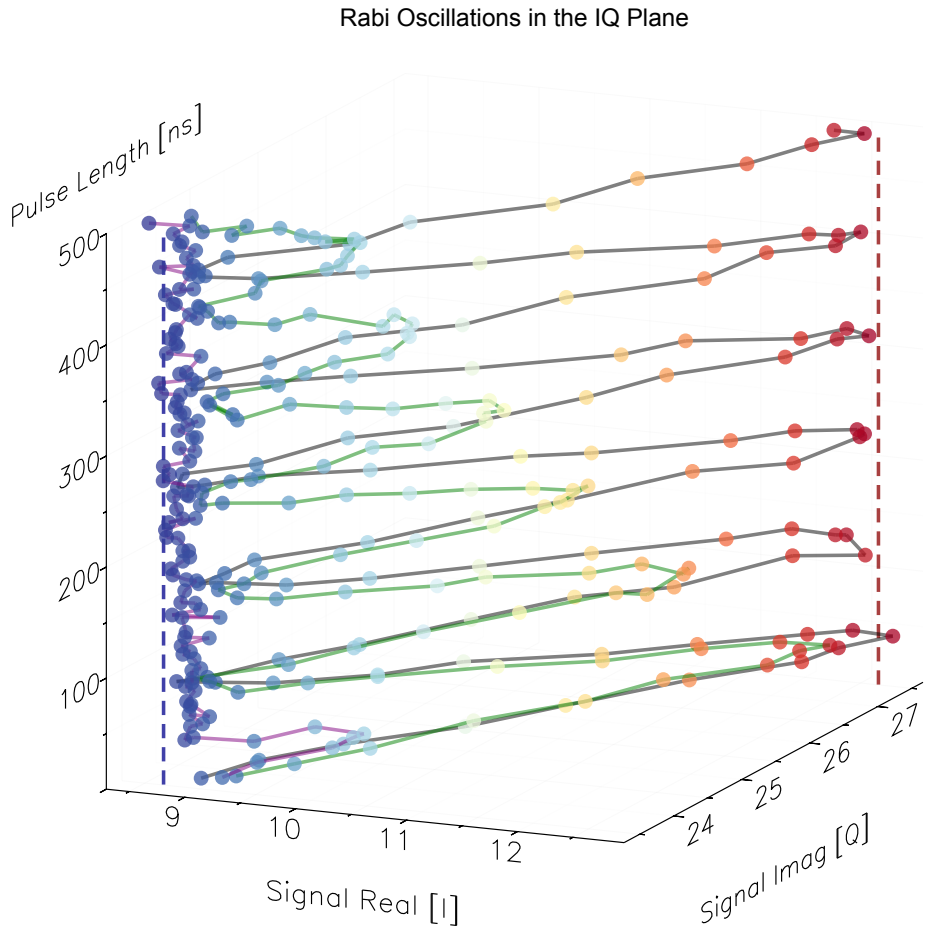


Figure 5.10: IQ trajectories in time (z axes) at a few qubit excitation frequencies. The ground (excited) state centroid is indicated by the blue (red) dashed line.

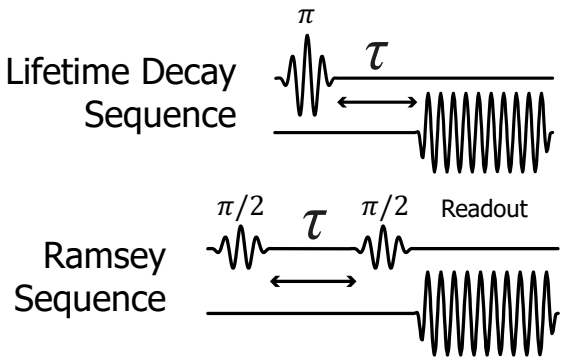


Figure 5.11: Excitation pulse and readout sequence for T1 and T2 characterization measurements.

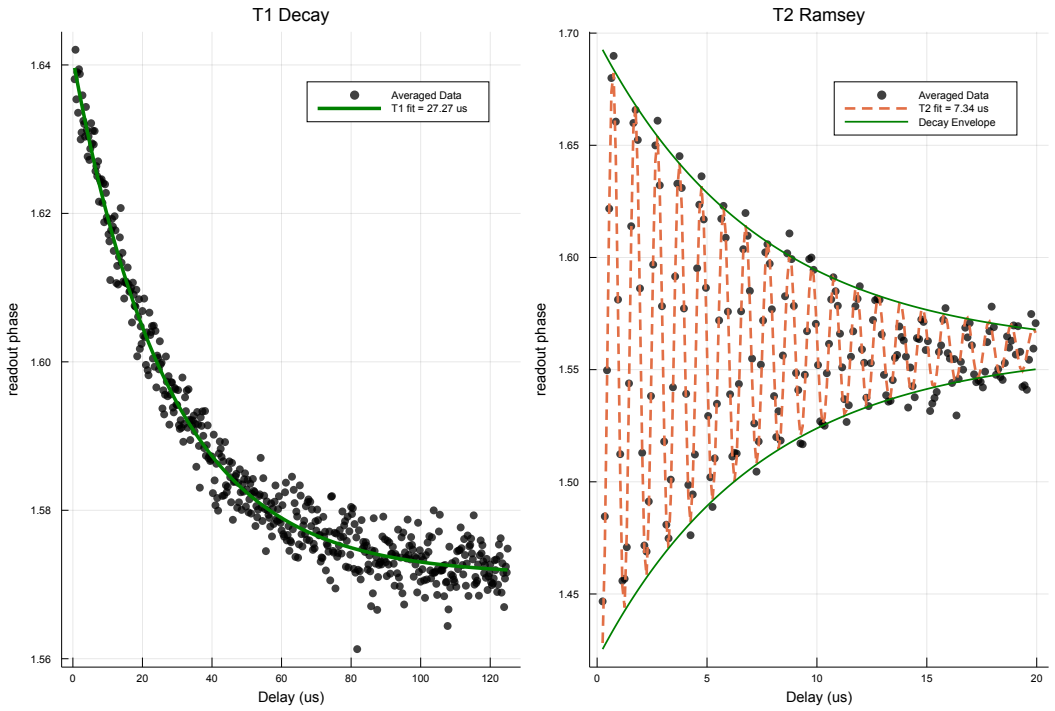


Figure 5.12: T1 and T2 time constants for a qubit fabricated on Silicon.

frequency and how much does the phase fluctuate? To characterize this, we apply half a rotation $\pi/2$ to the qubit to place the state on the equator of the Bloch sphere. At this point we sweep a delay parameter τ before applying another $\pi/2$ rotation to put the state up at the excited state. However, due to the phase noise or frequency jitter in the qubit, the state may not remain phase coherent on the equator, and the second rotation may rotate the qubit away from the excited state. Thus, a qubit's coherence is important for long algorithms that depend on phases to be well matched through the course of computation.

The results of T1 and T2 measurements are shown in Figure 5.12. The qubit shows a long lifetime of over 27μs, and is mostly likely limited to material losses in the substrate based on quality factor measurements on quarter-wave resonators with similar geometries. Based on the readout resonator design, the qubit is not limited by Purcell decay, with a limit at around 60μs. However, T2 might be limited by other reasons, such as flux noise in the measurement setup caused by spurious ground loops, TLS within the junction barrier [21], or para-magnetic surface spins that reside within the SQUID loop [54].

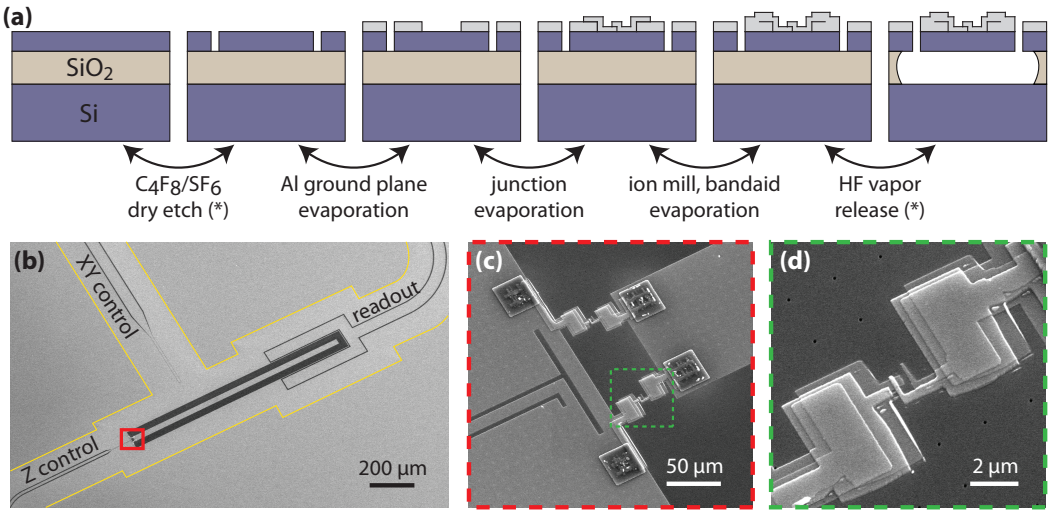


Figure 5.13: SOI fabrication process and layout. Adapted from [48].

5.5 SOI Substrate Design and Fabrication

The process for fabricating qubits on a Silicon-On-Insulator (SOI) substrate requires removing the buried oxide layer underneath the silicon device layer such that the device layer membrane is suspended where the electric field strength is the highest. Locally removing the oxide layer near the edges of transmission lines, by about 100 μm, can greatly help reduce dielectric loss. Releasing a membrane using the top silicon devices requires proliferated access holes. The process for etching through the silicon device layer and releasing a suspended structure with qubit metallization, as well as the area of oxide removed underneath the metallization is shown in 5.13. Due to the SOI substrate, some aspects of the microwave design needed to be changed. ϵ_{eff} now depends on the CPW width W and gap G relative to the thickness of the sacrificial buried oxide layer. This is due to the fact that the electric fields will see more or less of the underlying substrate (which is non-uniform in z) depending on the width and gap, which control the energy distribution and extent of the fields. Due to the fact that much of the local substrate has replaced silicon with vacuum, ϵ_{eff} will also be generally much lower. For a trace width and gap of 23 μm and 2.5μm respectively, we find that $\epsilon_{\text{eff}} \approx 2.5$, which from Eq. 2.9 implies that resonant structures need to be made much longer. A smaller ϵ_{eff} also requires capacitor geometries to be larger, to reach the same levels on a higher ϵ_{eff} substrate. As a result, a qubit structure on SOI needs to be made larger in the planar direction two fold - once with the lower ϵ_{eff} and again with the removal of the buried oxide layer.

Table 5.2: SOI qubit design parameters.

Parameter	Design	Simulation/Inferred
Qubit Capacitance	60 fF	60 fF
SQUID Inductance	11nH	≈11 nH
Readout Frequency	7.2 GHz	7.15 GHz fF
Qubit XY Drive	50 aF	50 aF
Qubit Z Mutual	2.0 pH	1.3 pH
Qubit Z Parasitic	0.1 pH	0.3 pH

Another design consideration is the suspension of a thin membrane. Because a circuit is fabricated on a membrane that can deform in the vertical axis, ϵ_{eff} will vary based on the deformation of the membrane in the vertical direction. This is a direct result of the change in dielectric material seen by the CPW. A larger membrane is also more suspectable to low frequency resonances in the suspended structure. But because a large structure is required for hitting design parameters and reducing loss, a trade off needs to be made with membrane size and qubit requirements.

5.6 SOI Qubit Characterization

Given the extra considerations needed to design an SOI qubit, the parameters for an SOI qubit device are listed in Table 5.2.

Using the characterization techniques described previously, we find as shown in Figure 5.14 that the lifetime and coherence times have been dramatically reduced from the silicon substrate. The largest contributor to under performing metrics on the SOI substrate is likely to be the presence of the buried oxide layer. Although we have removed the oxide as far as 100μm away, the larger capacitor geometries on this substrate will cause the electric fields to have a much large extent. Clearly there is work to be done to improve the lifetime and coherence of qubits on an SOI substrate, if we have realize a viable hybrid architecture. To investigate how we can improve upon this work, we look first look at the sources of dielectric loss and how we can mitigate such effects with a novel geometry.

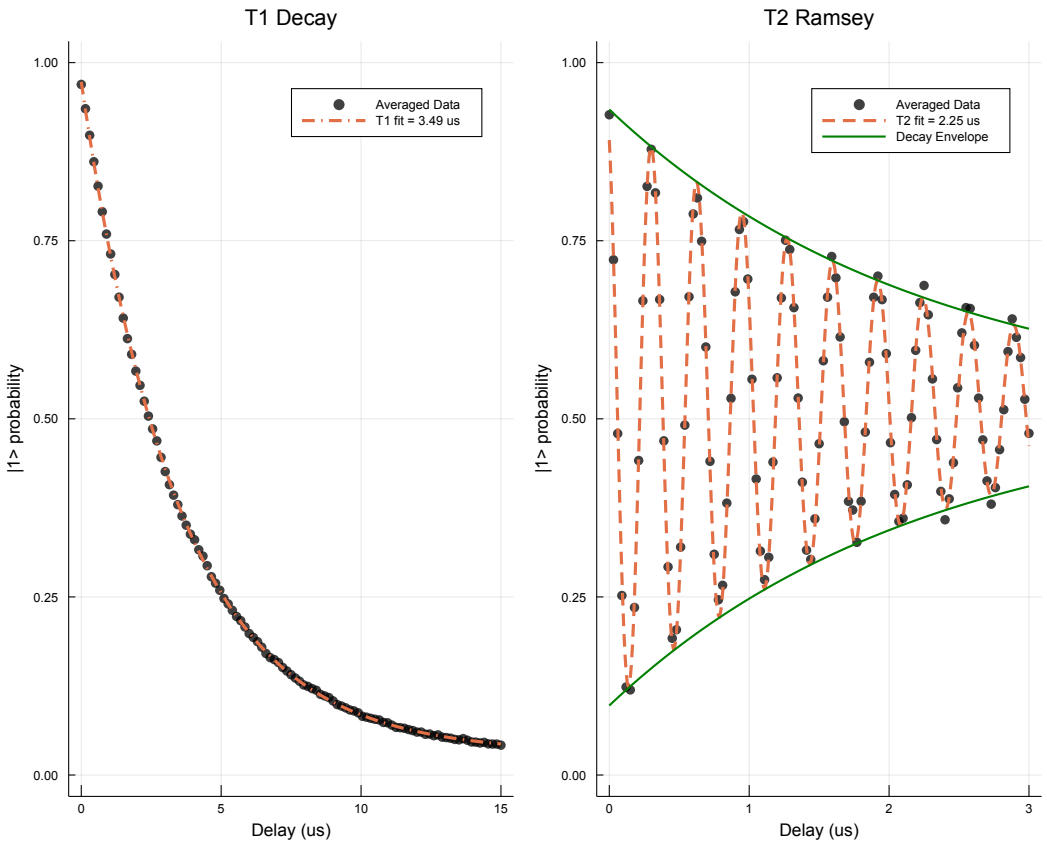


Figure 5.14: T1 and T2 time constants for a qubit fabricated on SOI.

Chapter 6

SUSPENDED TRACE AIR-GAP RESONATORS

The SOI substrate is a vital component to allow for the integration of superconducting circuit technology with the optical and mechanical domains. However, the lossy nature and large suspended microwave membrane that are required make the current platform infeasible for large and more complex technologies. What are some way to mitigate these issues, and make advantage of the multi-layered substrate? Loss in these circuits will always be a limit factor for demonstrating high fidelity quantum operations. Thus, we will first study how our microwave geometry is susceptible to loss.

6.1 Loss simulations

We begin with a 2D cross sectional study of the coplanar waveguide geometry on SOI, as shown in Geometry A of Figure 6.1. We have seen previously in Section 3.4 that lossy interfaces can contribute significantly to the participation of the electric field. Combined with low tangents, these interface ultimately limit the quality factor of superconducting resonators. The first step to investigating these loss interfaces to is start removing them. A sweep of the silicon undercut, or the amount of silicon removed under the metal, will allow us to see the significance of each interface as the fundamental geometry of the structure is changed. Given a center trace width and gap of 15μm, we can sweep the undercut from $+7.5\mu$m, where the silicon device layer is fully removed under the center trace, to -7.5μm, where we entirely recovery the unmodified SOI substrate. The undercut sweep parameter is analogous to trenching the resonators on silicon substrates [22], where an isotropic silicon etch will remove the substrate within the gap region and locally around the edges of your transmission lines. The philosophy of trenching is the remove the silicon-air interface that exists between the signal and ground electrodes where the field is strong, and move that interface futher away to where the fields are weaker.

Other geometries can be considered as well, such as in Geometry B, where vias are added to screen the loss buried oxide layer away from the electric field lines. In Geometry C, we add a backing metal layer, to fully shield the microwave structure from the buried oxide layer, provides a way to protect against crosstalk through

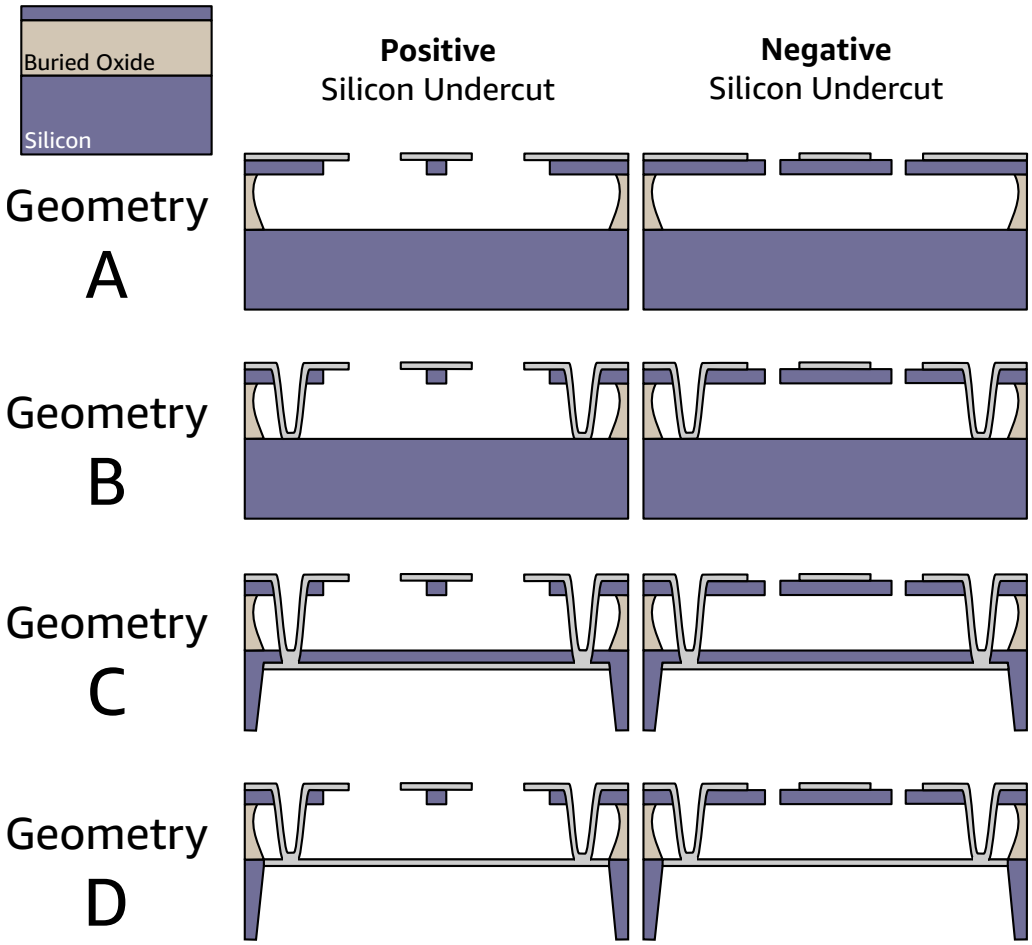


Figure 6.1: Study of loss contributions with four geometries.

the substrate, and uses the via to connect the topside ground planes together. The silicon in the handle layer of the substrate remains, such that the structures metal stress is symmetric vertically. This symmetry allow for smaller deformities due to the mismatches in expansion coefficients and internal materials stresses. Finally, in Geometry D, we remove the silicon between the top and bottom electrodes to minimize the amount of field in any bulk dielectrics.

Numerically simulating the participation ratio requires certain knowledge and assumptions of your substrate. For example, it may not be obvious what your metal-substrate (ms) material may be, and thus you can only guess as to what the loss tangent, dielectric constant, and thickness are. Table 6.1 shows a list of assumptions and parameters used for this simulation. There are a few important assumptions made that may not reflect the actual parameters of the fabricated device. For ex-

Table 6.1: Parameters and assumed material properties for electromagnetic and mechanical FEM simulations.

Material	Thickness	ϵ_r	$\tan\delta$	Residual Stress
Silicon Device Layer	220 nm	11.9	5×10^{-6}	-40 MPa
Silicon Handle	750 μm	11.9	5×10^{-6}	-40 MPa
Buried Oxide	3 μm	3.9	2×10^{-3}	-250 MPa
Aluminum	140 nm	N/A	N/A	450 MPa
Metal-Air Interface	3 nm	10.0	3×10^{-3}	N/A
Metal-Substrate Interface	3 nm	3.9	2×10^{-3}	N/A
Substrate-Air Interface	3 nm	3.9	2×10^{-3}	N/A

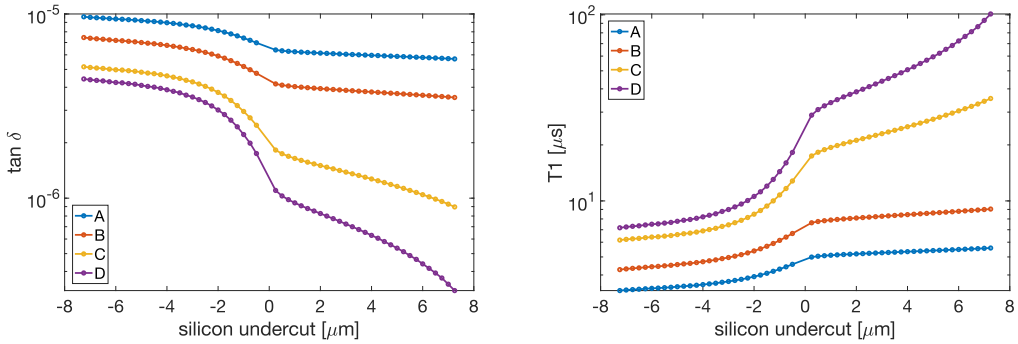
ample, we have assumed that at the metal-substrate interface, a native silicon oxide layer has formed which has the same properties as a thermally grown oxide (found in the buried oxide layer). We also assume that the native oxide formed on the Al superconductor has the same dielectric constant as sapphire, but with a much high loss tangent.

We can extract the total loss tangent from these geometries with

$$\tan\delta = \sum_i p_i \tan\delta_i \tag{6.1}$$

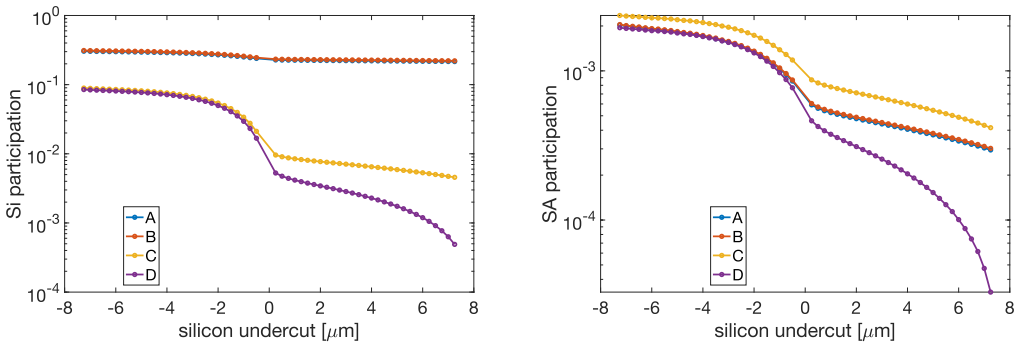
where p_i is the participation ratio and $\tan\delta_i$ is the loss tangent at each material or interface i. The loss tangent for each of the four geometries versus the silicon removed (undercut) is shown in Figure 6.2. We see that the effect of removing the silicon with in the gap (undercut $< 0\mu$m) becomes more dramatic as we approach the edge of the center trace at undercut = 0μm. After the silicon is removed within the gap region, only geometries C and D significantly improve with removal underneath the center. Geometries C and D have a backing metal layer, which pulls the fields through the bottom of the center trace. It thus makes sense that removing silicon directly underneath the trace will result in less loss. We use quality factor $Q = 1/\tan\delta$ as a proxy for the lifetime expected from a qubit with the same capacitor geometry. Thus, this allows us to extract an equivalent limit of $\omega_q T_1 = Q$ for dielectric loss.

Silicon is a major participant in the field energy distribution, only second to the vacuum participation. Fortunately, many studies with superconducting resonators have measured very low loss tangents [62][75][18][112][22], as low as 5×10^{-7}.



(a) Loss tangent estimates (b) T1 at 5 GHz estimates

Figure 6.2: Loss tangent and T1 estimates

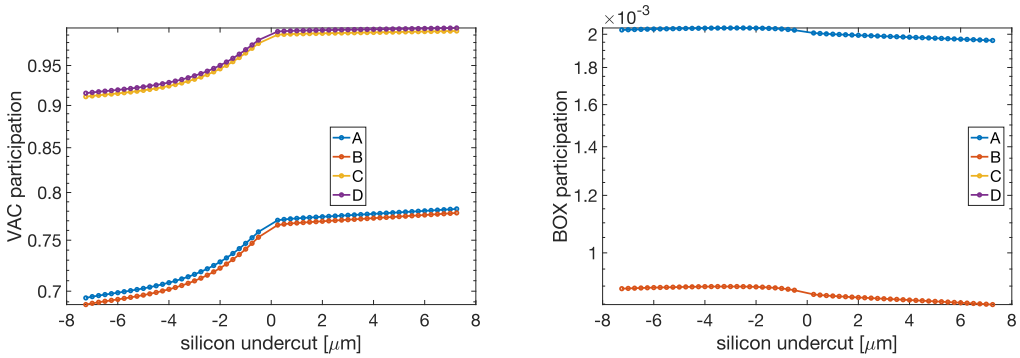


(a) Silicon participation (b) SA interface participation

Figure 6.3: Silicon bulk and interface participation

We see in Figure 6.3a that a considerable amount of field lives in the bulk silicon substrate in Geometries A and B, but considerably less with the backing metal added in Geometries C and D. In fact, Geometry D's sensitivity is the large because we have removed nearly all of the silicon within the structure by this point. The silicon interface with air can be a dominant source of loss. The silicon surface, unless terminated with hydrogen or other hydrophobic coatings, oxidizes readily in ambient air and forms an amorphous layer that eventually self-terminates[70][71]. We see that in Figure 6.3b, that all structures have a large participation on the silicon surface, but Geometry D's sensitivity is drastically reduced as we remove of the underlying silicon.

Vacuum is an ideal space to displace fields due to its lack of loss tangent. Thus, we should aim for as high of a participation as possible. We see in Figure 6.4a that exposing the fields to the silicon substrate causes a large amount of participation



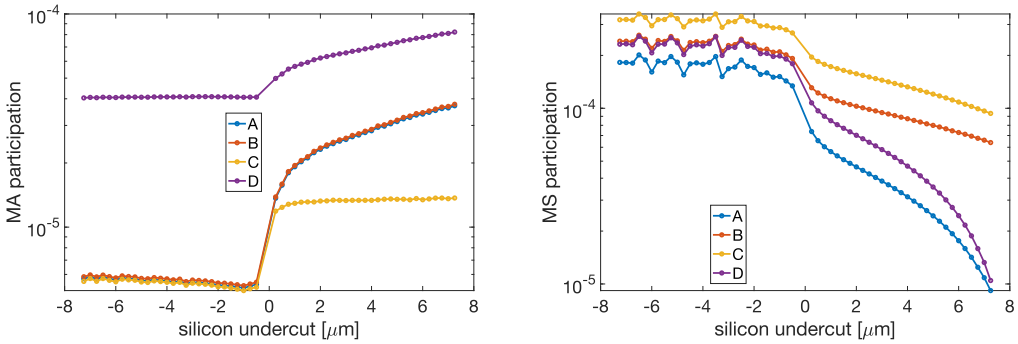
(a) Vacuum participation

(b) Buried oxide participation

Figure 6.4: Vacuum and buried oxide participation

leave the vacuum, due to silicon's high dielectic constant. However, with Geometry C and D, the vacuum participation can be maximized to nearly unity, thanks to the metal backing layer. The buried oxide layer on SOI is typically grown with a thermal oxidation process, and the bulk properties of thermal oxide are well understood [75] [20] [56]. Due to the amorphous nature of the oxide, the mechanism that results in loss can be modeled as a uniform spatial and nonuniform spectral density of TLS coupled to your resonant mode [33]. For simplicity however, we can capture the emergent effect of energy loss into this bath of TLS with an associated loss tangent. The thick and lossy buried silicon oxide layer is the reason for undercutting and suspending a local membrane around the CPW on SOI. Due to the through-oxide via, Geometries and C and D virtually do not participate in the buried oxide layer. Geometry B still participates, because the silicon handle layer beneath allows for fields to go around the via and into the oxide.

The metal-air interface can be highly dependent on fabrication process on material. For example, aluminum quickly self terminates with an amorphous oxide layer upon exposure to atmosphere[81]. Other superconductors [106][24][110] such as rhenium and titanium nitride are found to be less prone to atmospheric oxidation and/or form a less lossy interface layer. Other residues may exist on top of the metal following processing. For example, there may be residual resists that were not fully removed, or other organic residue from wet chemical processing. We for an interface dielectric constant of 10 (associated with aluminum oxide), we see in Figure 6.6a that Geometry D has the highest metal-air participation, which is explained by the nearly the entirety of the electric field lines extending between the



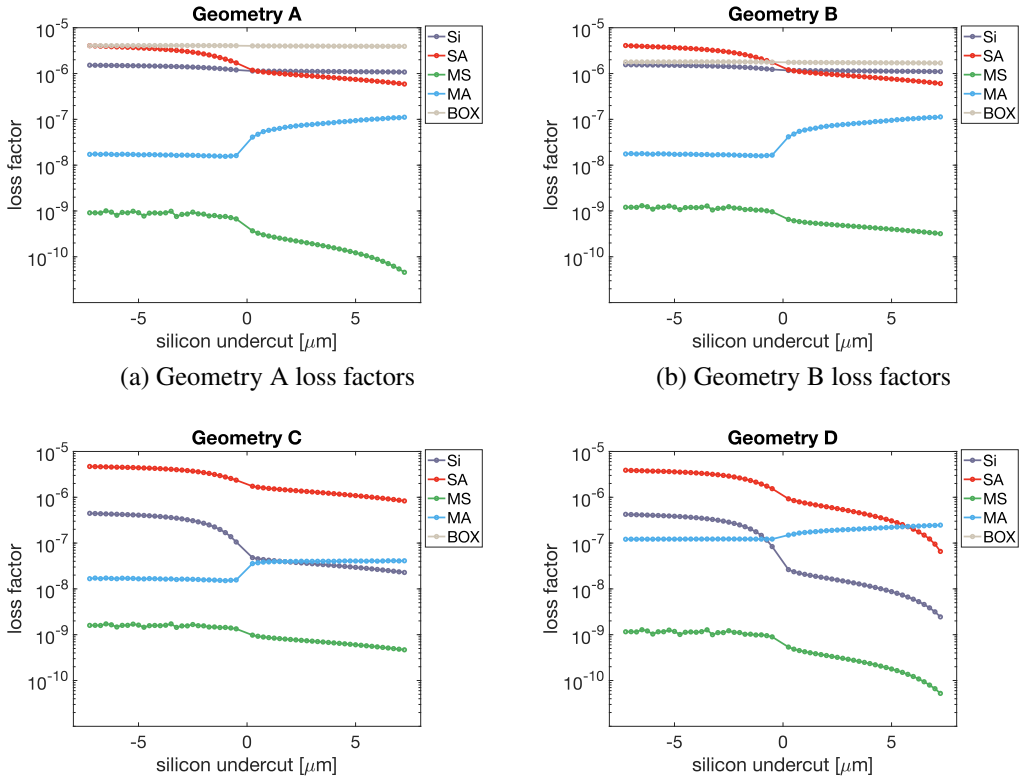
(a) MA interface participation

(b) MS interface participation

Figure 6.5: Metal interface participation

metal and vacuum. Geometry A and B see a moderate amount as we allow more fields to go between the center trace and ground planes. We see that Geometry C sees the least amount of participation due to the presence of silicon next to the metal backing layer, which replaces the metal-air interface with a metal-substrate interface instead. The metal-substrate interface is often set by the pre-metal deposition device preparation. For example, when etching a metal layer the state of the interface is set by the cleaning steps prior to deposition. When lifting off metal features, this interface is set by cleaning steps following the development of resist [81]. We see in Figure 6.6b that removing the silicon in the gap does not affect the ms participation, but when removing silicon in under the metal (where the interface) significantly reduces participation as expected.

To quantify and compare different interface and bulk losses against different geometries, Figure 6.6 shows a quantity that incorporates both the field participation and the loss tangent of the material through the loss factor $x_i = p_i \tan \delta_i$ with loss tangents listed in Table 6.1. These loss factors, assuming the correct material properties, gives a complete picture of how each interface or bulk component contributes to the overall loss tangent. In Geometry A, we recover the traditional SOI structure for an undercut of -7.5 microns. We can see that the buried oxide layer and substrate-air components contribute nearly equally, with silicon being a few times lower. As we increase the silicon undercut, the amount of silicon decreases and as a result, the substrate-air interface and metal-substrate interface participations are reduced. The buried oxide contribution remains dominant, suggesting that the fields should be screened from this bulk somehow. In Geometry B, with the addition of the through



(a) Geometry A loss factors

(b) Geometry B loss factors

(c) Geometry C loss factors

(d) Geometry D loss factors

Figure 6.6: Loss factors ($x_i = p_i \tan \delta_i$) of four geometries.

oxide via, participations are largely unchanged apart from a uniform reduction in the buried oxide participation as intended. A considerable amount loss come from the silicon substrate, buried oxide, and substrate-air interfaces. Geometry C tries to alleviate these issues by removed most of the silicon below the buried oxide, and adding a metal backing layer to completely screen the fields away from the buried oxide. A thin layer of silicon is kept to balance the residual stress along the vertical axis, such that the material stack is symmetric. The perfect screening of the buried oxide layer eliminates its contribution to loss entirely. The substrate-air interface remains a dominant source of loss due to the highly exposed silicon-air interface on the top side of the thinned silicon substrate layer. The silicon loss factor is now dependent on the undercut, due to the overall reduced presence of silicon within the structure. Finally, we see that in Geometry D, without the thinned silicon substrate, that once the silicon is sufficiently undercut, the dominant loss factor becomes the metal-air interface.

To realize a complete undercut of the silicon device layer, we need a way to suspend

the center trace periodically and introduce as little loss as possible. It is clear that the most ideal geometry moves nearly all of the field into the air/vacuum volume. Thus, we should investigate a **suspended trace air-gap resonator** structure (STAR) as explored in Geometry D, to see if we can leverage this geometries low loss properties for superconducting devices.

6.2 Engineered Support Structures

There are two possible methods to suspend the metal center trace. One method is to utilize the existing substrate's device layer to serve as the tethers, which would reduce process complexity overheat. Alternatively, a low loss deposited tether material (such as alumina) could be used as well.

Alumina Topside Tethers

As a first step, we can consider a direct pattern and lift off an alumina structure on the top side of our metal. Alumina is already relatively low loss, with a loss tangent around 2×10^{-3} when deposited with atomic layer deposition (ALD)[76]. With engineered tether structures, we can displace the stress away from the vertical direction and have better control over the deformation of the structure. The concept of engineered tethers were introduced for nanophotonics [44]. Here, I will adapt a structure with multiple narrow lateral beams to support our center trace. For this type of structure, the out-of-plane to in-plane stiffness ratio is $S_{out}/S_{in} = \frac{t^2}{w_m^2}$ where t is the thickness of the material and w_m is the width of the narrow lateral beam. We wish to maximize this ratio, so a thicker and narrower tether is best. Since typical Josephson junction fabrication for superconducting qubits uses an undercut bilayer, reasonable starting parameters to use the 220nm thick device and 350 nm wide lateral beams.

Studies for the ultimate tensile strength of alumina deposited by various methods suggest a strong thickness dependence. An ultimate tensile strength (UTS) of 323 MPa with a thickness of 5.8 um is achieved with electron beam evaporation. Fracture strengths of 3.5 GPa are possible with a 100nm ALD deposition [10], where the alumina shows higher strength as the thickness shrinks. With strength estimates so much higher in thin films, tensile failure due to high stresses in the structure are an unlikely cause for concern. Internal stress of alumina deposited by ALD and electron beam evaporation are in the range of 200 - 550 MPa, depending on

the deposition temperature. Thus, it makes sense to study the deformation of the structure with various internal stresses to check the tendency of the tethers deform due to fabrication uncertainties.

Silicon Underside Tethers

The critical buckling length of a membrane can be found with $l_c = \pi t\sqrt{E/(3\sigma_0)}$, where t is the thickness, E is the Young's modulus, and σ_0 is the internal stress [44]. For a 220 nm thick Si layer, we find that $l_c = 26$ μm. For gaps in the CPW that are reasonably small, these tethers would be feasible. The challenge comes from patterning these structures, which are underneath the metal. An isotropic SF6 etch would work, but the high difficulty of patterning will cause design headaches down the road. As we have seen, complicated tether designs are required to minimize the stress mismatches between aluminum and the tether material.

We wish to design more complicated tethers to redistribute the stress into the lateral direction. A more clever and direct method of making the silicon tethers is to define the tether geometry before depositing the metal. Instead of undercutting the silicon below already existing metal, we can instead pattern the silicon layer first. The only requirements are: the metal must be deposited conformally over the metal, and that the metal can be etched on contoured features so we avoid any remaining unetched metal that may cause shorts. As a consequence, we would require a conformal coating of superconducting metal, which is possible in tools such as an electron beam evaporator with stage tilt and rotation, or a sputter tool with conformal targets and stage rotation. These requirements also require more complex fabrication processing, which can contribute to interface loss. Nevertheless, developing conformal coatings of aluminum is an easier process than developing alumina tethers using ALD, and because silicon is a lower loss material (in the bulk) without the risk of brittle failure or the presence of an additional interface (between the alumina and metal), using silicon for tethers is far more advantageous than alumina.

6.3 Microwave Properties

We are able to compute the microwave properties of the STAR using methods developed for an equivalent microwave structure: the microshield [93]. Previous practical realization of the microshield relied on membrane to support the center

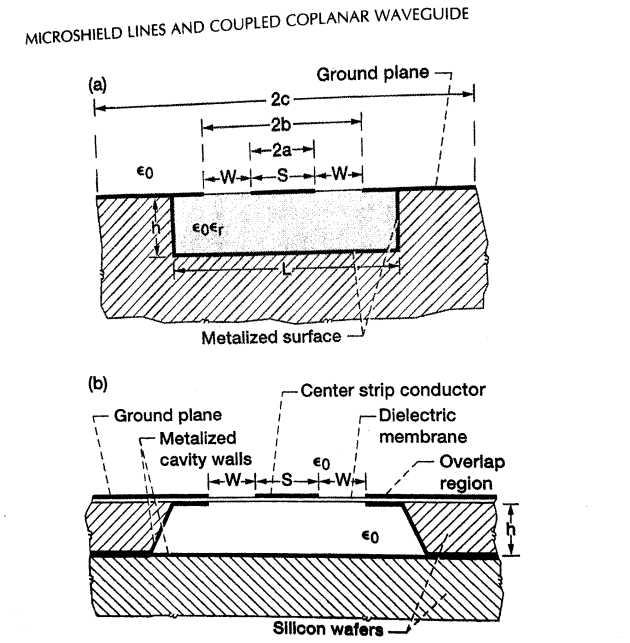


FIGURE 7.1 Rectangular microshield line: (*a*) Analytical model; (*b*) practical realization.

Figure 6.7: Microshield geometry, adapted from [93].

trace, which in the case of superconducting circuits would introduce too much loss. These membrane implementations are equivalent to Geometry D in Figure 6.1 with no silicon removed (undercut of -7.5 microns). The characteristic impedance for this structure is shown in Figure 6.7. There are two microwave regimes for this structure. With large width to gap ratios, the field primarily lives between the top metal electrodes, and resembles a CPW field distribution. For small width to gap ratios, the field is strong between the center trace and backing metal, and resembles a microstrip field distribution. Like CPW's, small width to gap ratios are less radiative and desired for loss loss and low crosstalk microwave transmission lines. Although the microshield geometry assumes that the effective permittivity is 1, we can simulate this per methods discussed in Appendix A to account for the presence of silicon tethers.

From a microwave design and fabrication perspective, STAR is an attractive option due to its low dielectric loss, low crosstalk, and its compact geometry. These metric are shown in comparison to silicon and SOI substrates in Table 6.2. Because the dielectric constant is nearly uniform (with vacuum) above and below the signal plane in STAR, the mode of propagation is a nearly perfect TEM. And because the

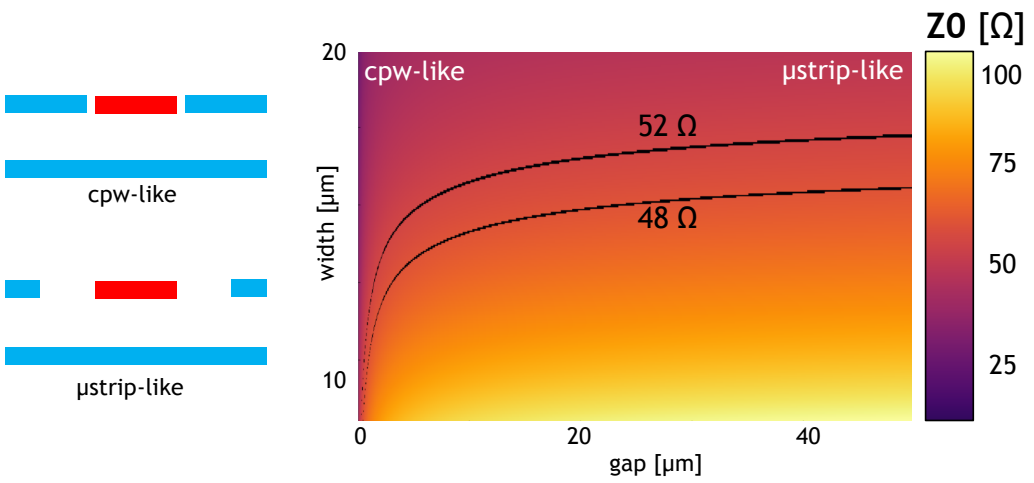


Figure 6.8: Numerical calculation of the characteristic impedance Z_0 using numerical methods (Appendix A.5).

	SOI	Silicon	STAR
Propagation	quasi-TEM	quasi-TEM	TEM
Effective ε_r	geometry dependent	6.45	≈ 1.0
Bulk $\tan\delta$	$< 5\times10^{-6}$/ 2×10^{-3}	$< 5\times10^{-6}$	$< 5\times10^{-6}$
Fab consistency	low	high	moderate
Crosstalk	high	moderate	low

Table 6.2: Comparison between different substrates.

dielectic is vacuum with a small presence of silicon, the effective dielectic constant is close to unity. With SOI, the dielectic constant varies depending on the center trace width because the 3 micron gap, where the buried oxide is removed, causes a non-trivial distribution of energy in the substrate. STAR removes nearly the entire bulk, leaving only the silicon suspension tethers behind. Although the fabrication process for STAR might be complicated, a low deformation of the center trace is key to ensure fabrication repeatability from run to run. SOI on the other hand, does not aim to reduce the deformation of the released membrane, and depending on the release geometry the released membrane may buckle and give a different effective dielectric constant. Finally, the crosstalk is very low in STAR, in part due to the backing metal and vias serving to keep the fields well confined. SOI has the highest crosstalk because the large undercut required to keep the fields away from the buried oxide, along with the low effective dielectric constant (usually around 2) causes any microwave structure to be large. Large microwave structures, are much more radiative and are susceptible to more crosstalk.

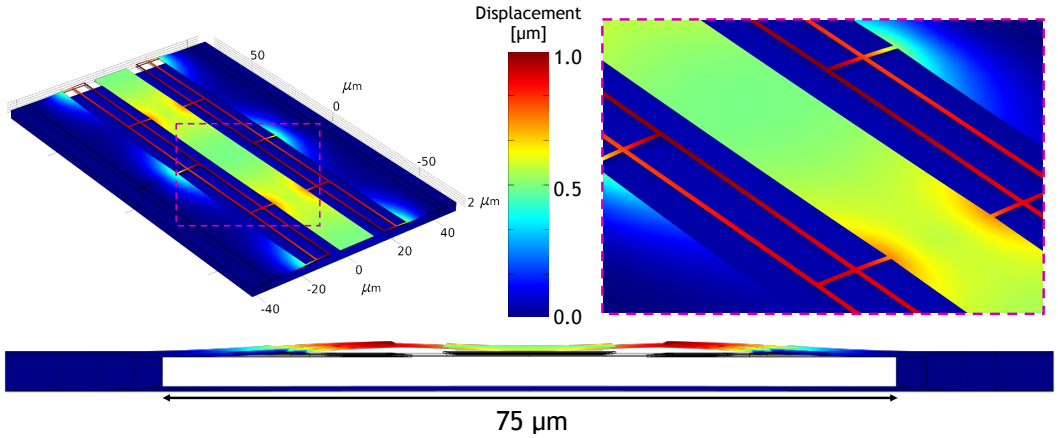


Figure 6.9: Displacement simulation. Parameters: width = 15 μm, gap = 15 μm, tether x-section = 250nm by 220nm, and structure x-section = 75 μm by 3 μm

6.4 Mechanical FEM results

A structural simulation was performed to check that the center trace did not deform significantly. We see in Figure 6.9, due to the engineering of the silicon tethers, that displacement is kept low and the variation in center trace deflection is small with respect to the top to bottom metal separation. The source of these displacements are due to the mismatch in residual stress of each material. For example, silicon and silicon oxide are typically under compressive stress, meaning that these material would prefer to expand when free of any constraints. Conversely, superconductors such as aluminum and niobium prefer to contract and are under tensile stress. The combination of tensile and compressive stress causes the bilayer of these two materials to deflect upwards or downwards.

Mechanical stress in thin film substrates

A point of failure for is the cracking of the buried oxide layer. The yield strength of this layer is typically 250 MPa. However, due to to sharp and wide meandering turns of the released membrane, stress can build up at these corners and cause a brittle failure, which ten propagates down the membrane, as seen in Figure 6.10. Shrinking the cross sectional area significantly, down to around the critical buckling length of silicon prevents these cracks from working, suggesting that the buckling of silicon is causing the build up of stress in these membranes.

6.5 Loss Simulations with Silicon Support Tethers

With silicon support tethers and a full metal structure that is fabrication compatible, we can reevaluate and compare the loss between the SOI substrate and the STAR

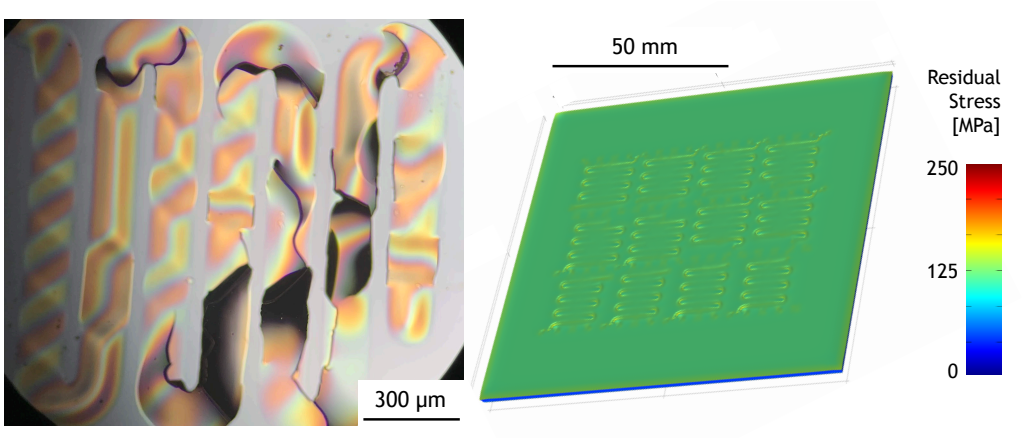


Figure 6.10: Membrane failure and stress simulations.

Table 6.3: Loss contribution table for 15 μm width and gap and tethers that are periodic over 90 microns. For these simulations of the STAR geometry, there are two 250nm x 220nm tethers in the gap.

2D simulation Material /Interface	p_i (participation)		$\tan\delta_i$ (loss tangent)	$x_i = p_i \tan\delta_i$ (loss contribution)	
	SOI	STAR		SOI	STAR
Air	0.7	**0.99985**	0	0	0
Silicon	0.3	6×10^{-5}	5×10^{-7}	2×10^{-7}	3×10^{-11}
Silicon Oxide	1×10^{-3}	$\ll10^{-3}$	2×10^{-3}	2×10^{-6}	$\ll2\times10^{-6}$
Substrate-Air	2×10^{-3}	5×10^{-6}	2×10^{-3}	4×10^{-6}	1×10^{-8}
Metal-Substrate	2×10^{-4}	4×10^{-7}	2×10^{-3}	4×10^{-7}	8×10^{-10}
Metal-Air	6×10^{-6}	8×10^{-5}	3×10^{-3}	2×10^{-8}	$\mathbf{2.4\times10^{-7}}$
			Total loss tangent $\sum x_i$	8×10^{-6}	2.5×10^{-7}
			T_1 limit at 5 GHz (μs)	4	127
			Capacitance/unit length (pF/m)	27	33

structure. Table 6.3 shows a breakdown of participation ratios with assumed loss tangents to obtain loss factors for bulk and interface areas. The total loss tangent is the sum of all loss factors, and with the total loss tangent, we can estimate the T1 limit due to material loss. The capacitance per unit length is comparable between the two structures, suggesting that qubit geometries will require similar designs to achieve the same amount of coupling between elements.

6.6 Fabrication Process

The suspended trace air gap resonator process incorporates a few main steps. First we pattern global marker layers, which include both markers for the electron beam lithography steps, and the optical lithography steps. The second step is a silicon etch

layer, where silicon tethers are defined. The third step utilizes optical lithography, which defines through buried oxide vias. The fourth step defines the metal pattern layer. Finally, we have the final few steps which incorporates optical lithography once again, but is done on backside of the device. This pattern defines the etch for backside of the substrate and allows access to metallize the underside of the structure. The full process is illustrated with these steps in Figure 6.11 and the full list of processing steps are outlined in Appendix G.

The biggest challenge in this process is not the individual steps themselves, but rather the integration of each step to the next, while ensuring material and pattern compatibility. For example, the metal patterning step is broken up into a lift off step and an etching step. The liftoff step is needed to create a conformal coating on an etched, non-planar substrate. However, because liftoff is only compatible with large features, a separate metal etching step is needed to define features that smaller than three times the undercut of the bilayer resist stack used for liftoff. Thus, we use etching for feature below 1 micron and liftoff for features above 1 micron. Another example is the use of polydimethylglutarimide (MicroChem PMGI SF11) as a protective layer for the front side of the device, where aluminum has been deposited. Because photoresist developers commonly use a solution of TMAH, which quickly attacks aluminum, the already patterned metal features need to be protected.

Although there are many more examples, an unexpected process compatibility issue could simply arise to due the preparation of the substrate. During the through-oxide via etching process, the silicon device layer must be etched in-situ with the oxide layer underneath. If the silicon device layer for via patterns are etched in a prior step, a grass formation occurs during the through-oxide etch. This grass is not caused by the photoresist used in the definition of the via, because the same photoresist mask is used in both cases. The formation of grass is mostly likely due to the exposure of the buried oxide to atmosphere, allowing reactions that form at the surface, and leading to amorphous material that serve as micro-masks.

Proof of Concept Structure

A proof of concept structure with the process adopted from qubits on SOI shown in Figure 6.12. The advantage of this process that it does not deviate from the existing

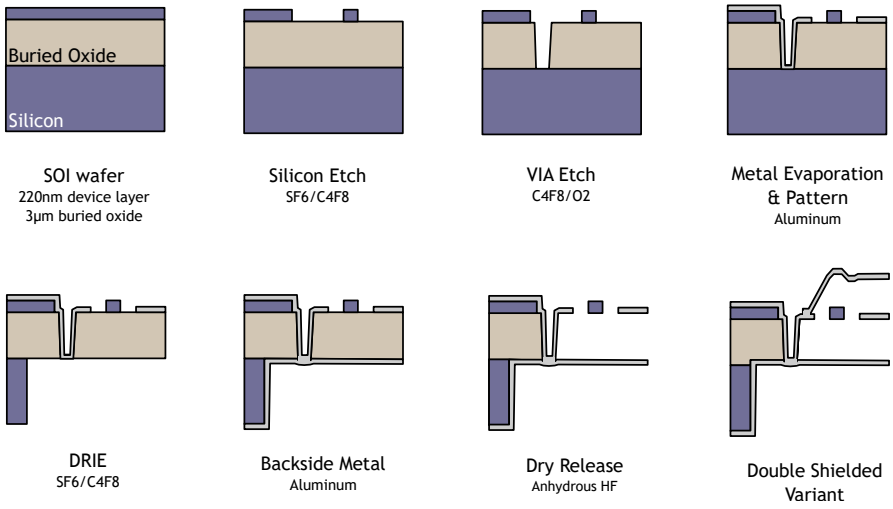


Figure 6.11: Fabrication processing steps. If desired, a double shielded variant can be realized with additional processing, which enables fully shielded "coax-on-chip" transmission lines.

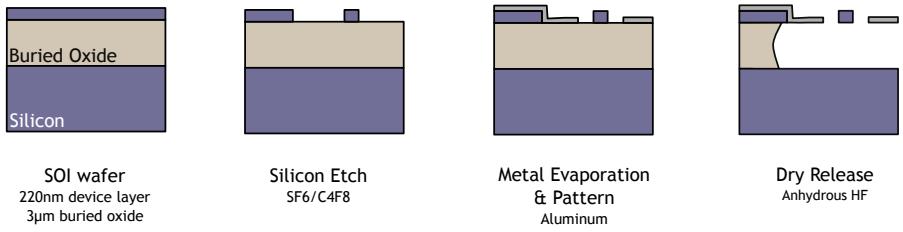


Figure 6.12: Proof of concept process to test the viability of silicon suspension tethers.

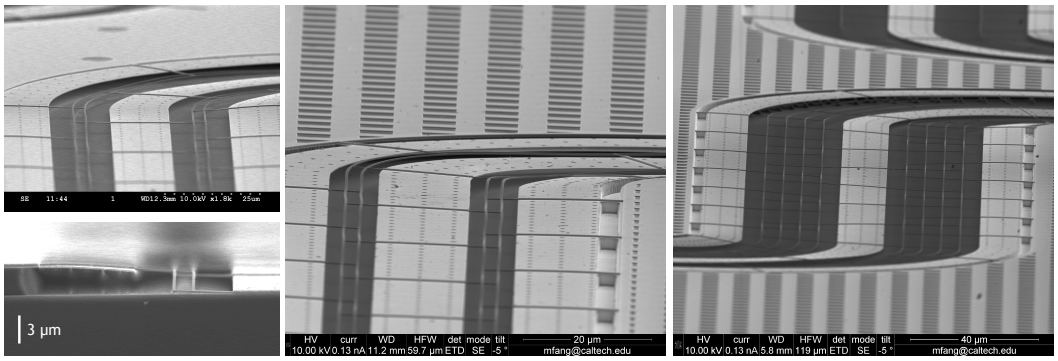


Figure 6.13: Proof of concept results.

SOI process, and the only changes are within the design of the structure. The proof of concept process demonstrates that silicon suspension tethers are a reliable way to suspend the CPW center trace, with very low vertical deflection of the center trace.

6.7 Device Overview

To test both the microwave and loss properties of STAR, as well as to demonstrate compatibility with current SOI device processes, a test chip was designed incorporate both SOI and STAR geometries within the same die, as shown in Figure 6.14. The top feedline (P1 to P2) addresses SOI resonators, where as the other feedlines serve to address STAR. Due to fabrication imperfections and defects from processing on a single die, the yield for STAR was low. For example, thermal grease used to mount the device to a carrier wafer in an etch step leak onto the topside during pump out and prevented many of the resonators attached to ports P7 and P8 to have a backing metal layer. Edge effects also played a role in lowering yield, and preventing the backside etch from fully reaching the buried oxide during the DRIE step. As a result, not all STAR structures could be measured. Processing on the wafer scale should improve yield substantially. Nevertheless, all resonators parameters on this device are shown in Table 6.4. There are a few key dependencies that this device aims to investigate: the density of tethers in the transverse direction (the tether spacing), the density of tethers in the laterally direction (the number of parallel strands), and the width to gap ratio of the top electrodes.

6.8 Measured Quality Factors

Superconducting resonators were fabricated using the STAR process. Because the STAR process was designed to be compatible with existing SOI processes, traditional SOI resonators were fabricated on the same device. A proof of concept

type	freq [GHz]	ϵ_{eff}	width [μm]	gap [μm]	tether spacing [μm]	parallel strands	Z_0 [Ω]
STAR	6.80	1.002	4	4	10	1	104.3
STAR	6.85	1.002	4	4	30	1	104.3
STAR	6.90	1.002	4	4	90	1	104.3
POC	6.95	1.259	4	4	60	1	N/C
STAR	7.00	1.002	4	4	60	4	104.3
STAR	7.05	1.002	4	4	60	3	104.3
STAR	7.10	1.002	4	4	60	2	104.3
STAR	7.15	1.002	4	4	60	1	104.3
STAR	7.20	1.002	6	1	60	1	69.2
STAR	7.25	1.002	5.43	1.86	60	1	80.5
STAR	7.30	1.002	4.86	2.71	60	1	90.5
STAR	7.35	1.002	4.29	3.57	60	1	99.8
STAR	7.40	1.002	3.71	4.43	60	1	108.7
STAR	7.45	1.002	3.14	5.29	60	1	117.1
STAR	7.50	1.002	2.57	6.14	60	1	124.3
STAR	7.55	1.002	2	7	60	1	128.5
SOI	7.60	$\approx$2.09	10	1.1	N/A	N/A	$\approx$50
SOI	7.65	$\approx$2.09	23	2.5	N/A	N/A	$\approx$50
SOI	7.70	2.09	50	5.5	N/A	N/A	$\approx$50
SOI	7.75	$\approx$2.09	10	10	N/A	N/A	N/C
SOI	7.80	$\approx$2.09	10	20	N/A	N/A	N/C

Table 6.4: Structures and parameters on the test device. One proof of concept (POC) resonator was included to emulate Geometry B with a full silicon undercut. For some geometries, the characteristic impedance was not calculated (N/C).

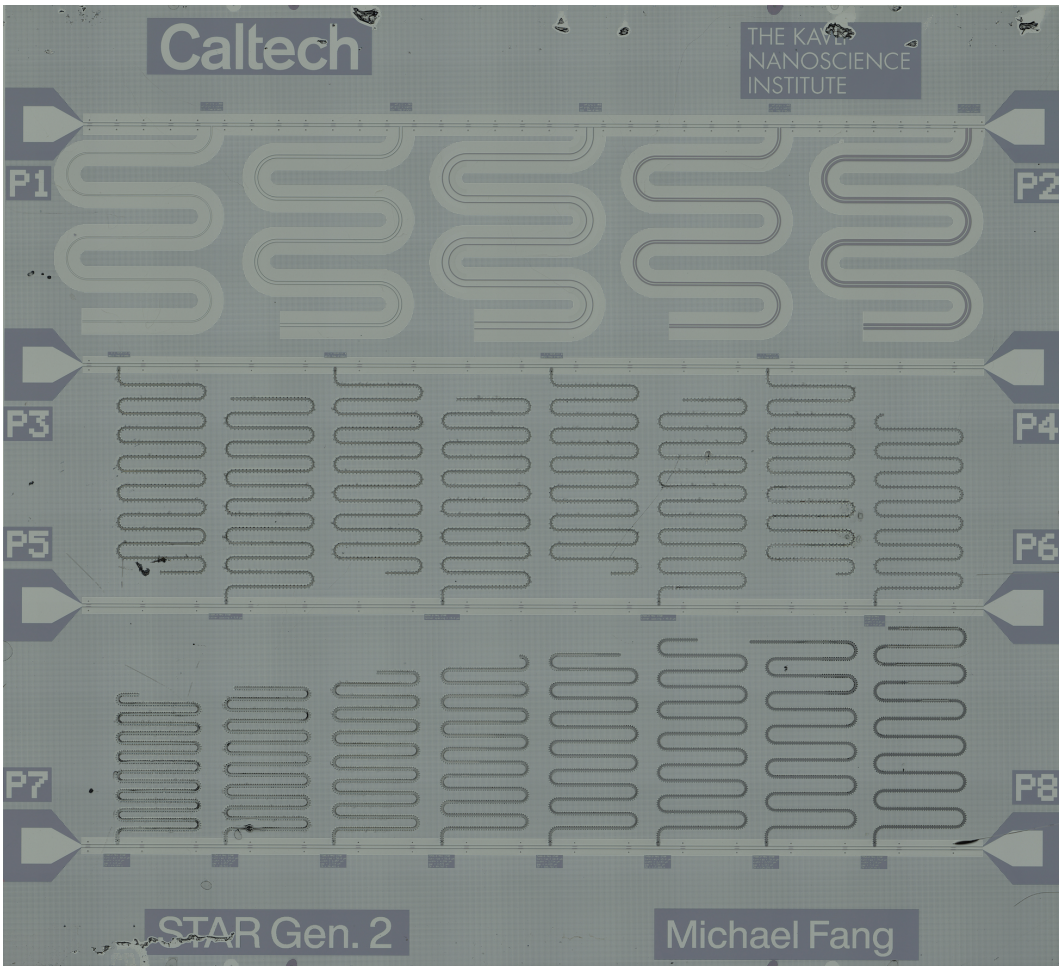


Figure 6.14: Stitched micrograph of the STAR test device.

geometry equivalent to Geometry B in Figure 6.1 was also fabricated on the same device. The resonators were measured across different powers, and the quality factors are shown in Figure 6.16 and the geometries fabricated in these measurements are shown in Figure 6.15. We see that at low powers, all resonators saturate to a TLS limit [66].

However, the quality factors are an order of magnitude below of what loss simulations predict. Going down to single photon levels on the same device, it is apparent that the best STAR geometry improved upon ($Q_i \sim 115 \times 10^3$) the best SOI geometry ($Q_i \sim 10 \times 10^3$). There are some possible reasons for why the quality factors are lower than expected:

Vorticies: The formation of vorticies is unlikely, given the amount of magnetic shielding in the setup and trace widths of the resonators. For resonators with center

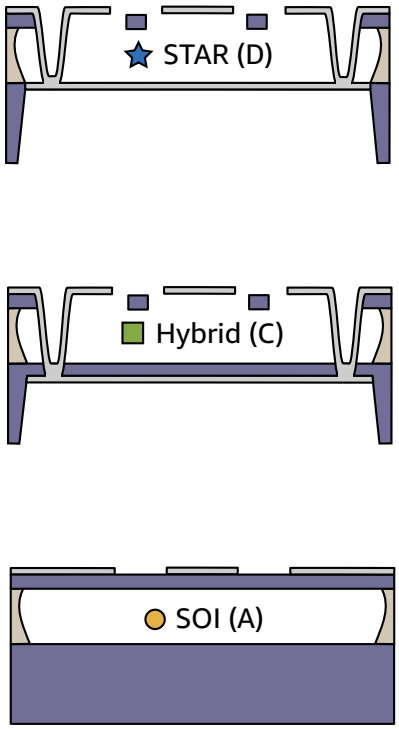


Figure 6.15: Key labels for the measured various geometry types, as used in 6.16.

trace widths as wide as 50μm, this is still a possiblity.

Quasiparticles: A temperature sweep can be performed to look at the effect of quasiparticles on the superconductor. 4K stage temperature can also be sweeped, making it act like an blackbody radiator. A packaging is well shielded, is "light-tight," and should have no dependence on the 4K stage temperature.

Fabrication and TLS: Loss simulations on SOI suggest that Q's can be an order of magitude worse if there is a uniform 3 nm thick layer of photoresist (loss tan 0.02) at the metal-substrate interface. This might be possible given that the metal was patterned use lift-off.

Frequency jitter: It is possible that vibrations (even slow ones) in the setup can cause the frequency to change over time. Because the frequency is unstable, a wider than expected line width is measured. A ring down measurement will indicated the bare line linewidth of the resonator without jitter.

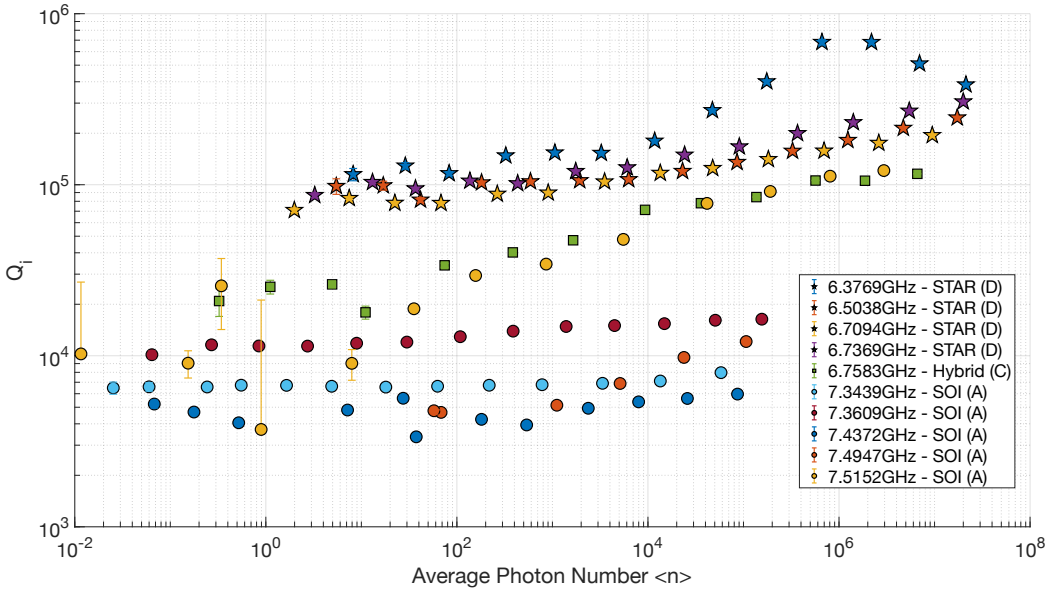


Figure 6.16: Quality factor of STAR and SOI resonator at high and low resonator phonon numbers $\langle n \rangle$. The hybrid structure resembles Geometry C, but with a thicker silicon layer (0.5 - 2 microns) above the backing metal.

The sample temperature was raised from 20milliKelvin to 330milliKelvin to allow some population of quasiparticles (and thereby normal metal islands) on the superconductor to exist. We see in Figure 6.17 that the resonators are well below the temperature regime where quasiparticles start limiting quality factors. Another source of quasiparticle loss could come from stray infrared radiation from the 4K stage of the dilution fridge. The 4K stage temperature was raised from 3.5K to 9.2K, to investigate the effect of quasiparticles generated from stray infrared blackbody radiation. This infrared radiation has more energy than the superconducting gap of Al, and breaks Cooper-pairs. Insufficient shielding could limit the ability to properly characterize TLS loss. Resonator quality factors were measured with an elevated 4K stage temperature. However, no significant temperature dependence was seen [7], suggesting that the sample is well shielded against quasiparticles.

Frequency jitter was ruled out with a ring down measurement as shown in Figure 6.19. On the input side, strong drive tone, gated with a square envelope was applied on resonance. On the output side, the power (or photon number) was measured to look at the resonator response to the drive tone. At the end of the gate, we see a non-exponential decay due to a high power decay rate and a low power decay

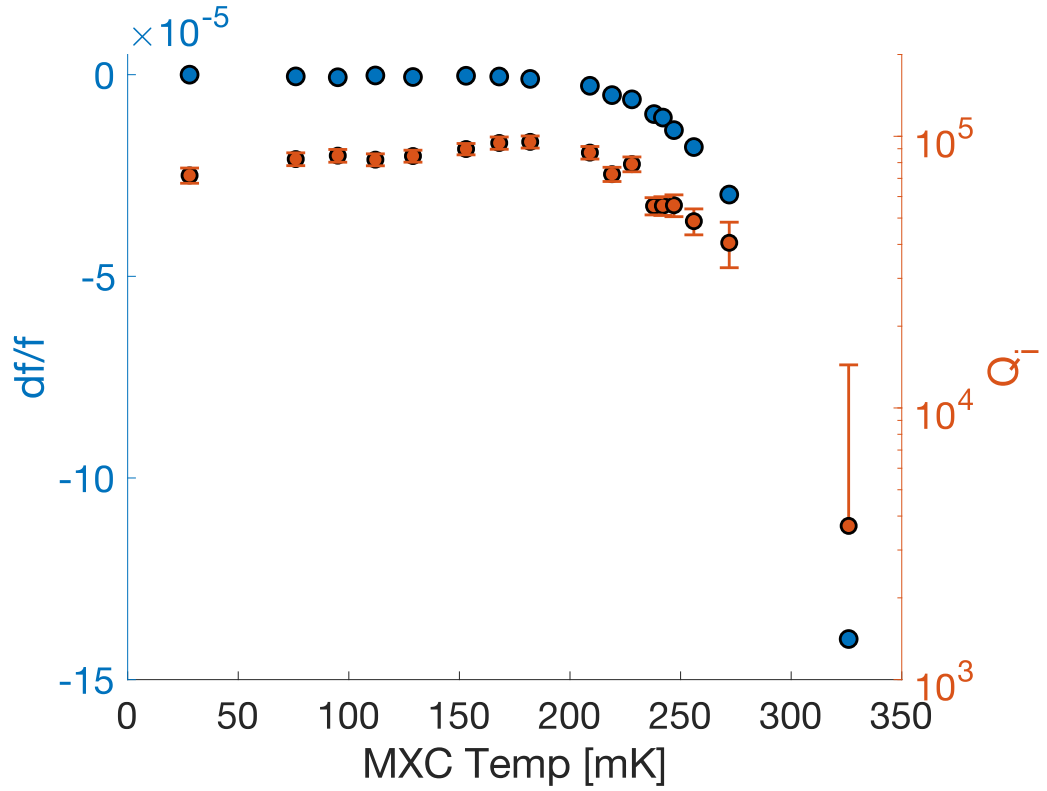


Figure 6.17: Frequency shifts and quality factor of STAR resonators at different sample stage temperatures.

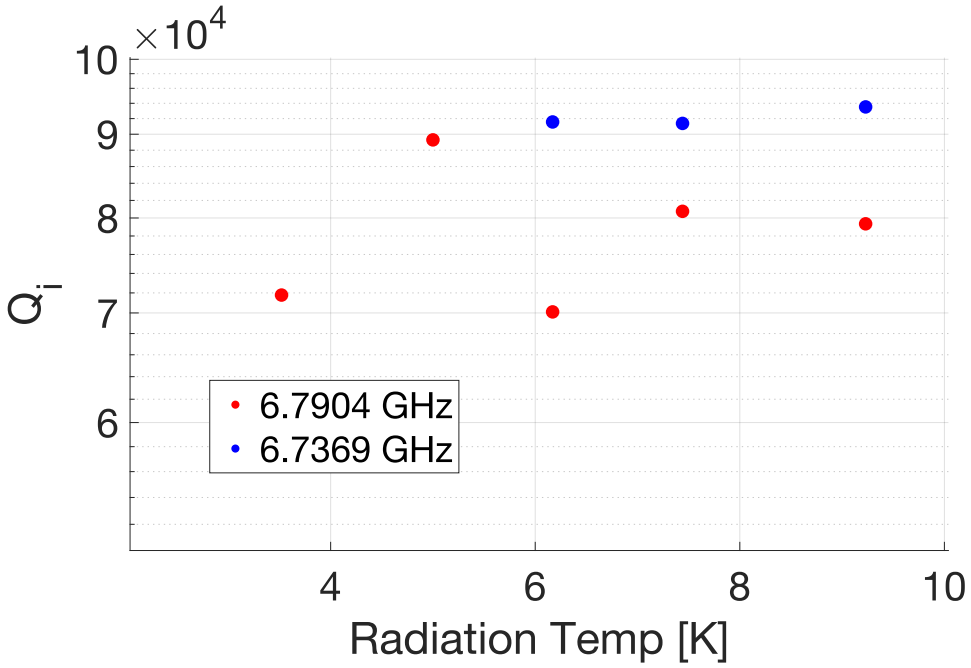


Figure 6.18: Quality factor of STAR resonators when irradiated with Cooper-pair breaking energies using the 4K plate as a radiator as test of the IR shielding.

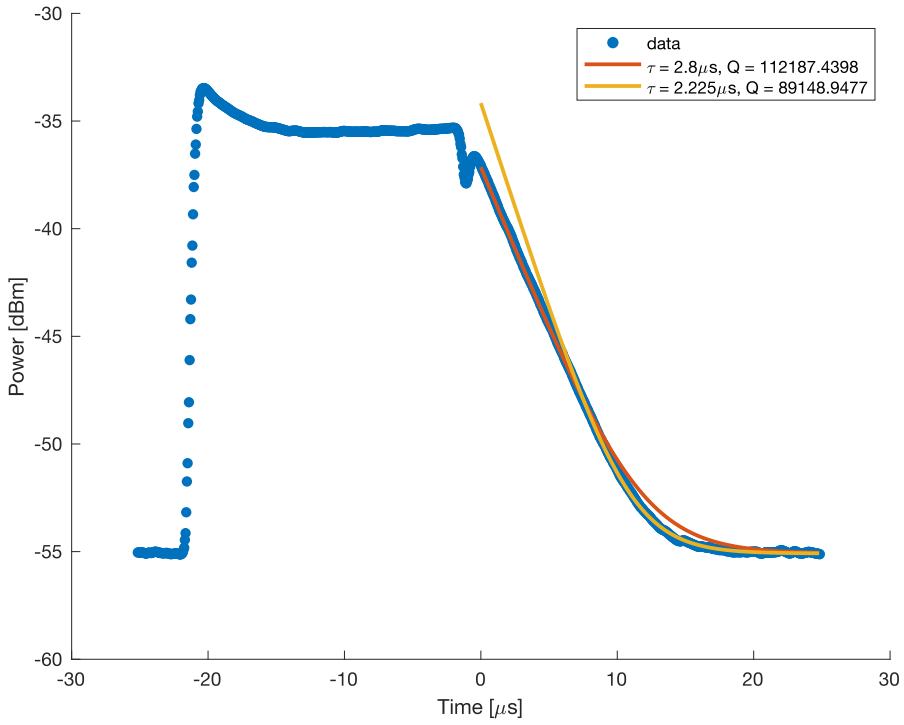


Figure 6.19: Ring down measurement to determine if resonator loss is limited by frequency jitter.

rate. These decay rates correspond to the high and low (TLS-limited) power quality factors seen in Figure 6.16. We see that a fit to these ring down decay rates indicate the same quality factor seen previously, and that STAR resonators are not frequency jitter limited.

Since we can rule out vortex loss for all but one SOI resonator (which had a 50 micron center trace), measured that our device packaging is not sensitive to quasiparticle generating blackbody radiation, looked at ring down measurements to address frequency jitter, and extracted consistent quality factors, it is strongly suggestive that interface loss in playing a big role in low quality factors. The interface participation ratio at the interface i is the interface participation normalized by the total electric field energy

$$p_i = \frac{t_i \epsilon_i \int dx_i \, |E|^2}{W} \tag{6.2}$$

for some thickness t_i, dielectric constant ε_i, along a interface coordinate x_i, and total field energy $W = \sum_i p_i + \sum_b p_b$. I have used the p_i notation to denote interface

participation and p_b to denote bulk participation. In practice, the interface will depend heavily on processing and materials (which sometimes we will not even know the properties for or even substance of). Thus, we can separate out the material dependent (m_i, the material factor) and field dependent (f_i, the field factor) parts as

$$p_i = \frac{m_i f_i}{W} \tag{6.3}$$

$$m_i = t_i \epsilon_i \, \epsilon_i' \tag{6.4}$$

$$f_i = \int dx_i \, |E'|^2 \tag{6.5}$$

where E' is the electric field independent of the interface properties, and ϵ_i' is a material property that is normally consider with the field factor, and is kept separate such that the field factor is only dependent on the bulk properties.

The three interfaces we will consider are the metal-air (ma), metal-substrate (ms), and substrate-air (sa), which have field factors of [107]

$$\epsilon_{\mathrm{ma}}' = \left(\frac{1}{\epsilon_{\mathrm{ma}}}\right)^2; \quad f_{\mathrm{ma}} = \int dx_{\mathrm{ma}} \, |E_{a\perp}|^2 \tag{6.6}$$

$$\epsilon_{\mathrm{ms}}' = \left(\frac{\epsilon_{\mathrm{s}}}{\epsilon_{\mathrm{ms}}}\right)^2; \quad f_{\mathrm{ms}} = \int dx_{\mathrm{ms}} \, |E_{s\perp}|^2 \tag{6.7}$$

$$\epsilon_{\mathrm{sa}\perp}' = \left(\frac{1}{\epsilon_{\mathrm{sa}}}\right)^2; \quad f_{\mathrm{sa}\perp} = \int dx_{\mathrm{sa}} \, |E_{a\perp}|^2 \tag{6.8}$$

$$\epsilon_{\mathrm{sa}\parallel}' = 1; \quad f_{\mathrm{sa}\parallel} = \int dx_{\mathrm{sa}} \left|E_{a\parallel}\right|^2 \tag{6.9}$$

where the sa interface has both parallel and particular components, unlike the ma and ms interfaces, which are in close proximity with a perfectly conducting perpendicular field boundary condition. Now we have

$$m_{\mathrm{ma}} = \frac{t_{\mathrm{ma}}}{\epsilon_{\mathrm{ma}}} \tag{6.10}$$

$$m_{\mathrm{ms}} = \frac{t_{\mathrm{ms}} \epsilon_{\mathrm{s}}^2}{\epsilon_{\mathrm{ms}}} \tag{6.11}$$

$$m_{\mathrm{sa}\perp} = \frac{t_{\mathrm{sa}}}{\epsilon_{\mathrm{sa}}} \tag{6.12}$$

$$m_{\mathrm{sa}\parallel} = t_{\mathrm{sa}} \epsilon_{\mathrm{sa}} \tag{6.13}$$

Note that we can only do this separation for interface participation only, as the bulk fields will vary too much within the thickness of the material. In other words, we

need the correct field E (which should not change significantly within the interface because of small thickness) which is heavily influenced by the surrounding bulk material. Since we understand bulk properties much better than the interface properties, we can take advantage of what we know about the bulk to better understand our interfaces. The total loss tangent is

$$\tan\delta = \sum_i p_i \tan\delta_i + \sum_b p_b \tan\delta_b \tag{6.14}$$

where again, we make a distinction in notion between the interface and the bulk, since we rarely know the loss tangent of the interface material. Given knowledge of the device internal quality factors, we can fit this data to a model that has our field factors and bulk losses. With three interfaces, and unknown material factors m_i and interface loss tangents $\tan\delta_i$, we would have six fit parameters. For simplicity, we can combine the material factor and loss tangent into a material loss factor $\chi_i = m_i \tan\delta_i$. We can see that with

$$p_{\mathrm{sa}} \tan\delta_{\mathrm{sa}} = \frac{\frac{t_{\mathrm{sa}}}{\epsilon_{\mathrm{sa}}} f_{\mathrm{sa}\perp} \tan\delta_{\mathrm{sa}} + t_{\mathrm{sa}}\epsilon_{\mathrm{sa}} f_{\mathrm{sa}\parallel} \tan\delta_{\mathrm{sa}}}{W} \tag{6.15}$$

$$= \frac{t_{\mathrm{sa}} \tan\delta_{\mathrm{sa}}}{W}\left(\frac{f_{\mathrm{sa}\perp}}{\epsilon_{\mathrm{sa}}} + \epsilon_{\mathrm{sa}} f_{\mathrm{sa}\parallel}\right) \tag{6.16}$$

$$\equiv \frac{k_{\mathrm{sa}}}{W}\left(\frac{f_{\mathrm{sa}\perp}}{\epsilon_{\mathrm{sa}}} + \epsilon_{\mathrm{sa}} f_{\mathrm{sa}\parallel}\right) \tag{6.17}$$

we would need two material based fit parameters $k_{\mathrm{sa}} \equiv t_{\mathrm{sa}} \tan\delta_{\mathrm{sa}}$ and ϵ_{sa} to determine the sa interface loss. Thus, we are left with four fit parameters to determine the interface loss: χ_{ma}, χ_{ms}, k_{sa}, and ϵ_{sa}.We find that our fit model takes the form

$$\frac{1}{\tan\delta} = Q_{\mathrm{int}}(\chi_{\mathrm{ma}}, \chi_{\mathrm{ms}}, k_{\mathrm{sa}}, \epsilon_{\mathrm{sa}}) \tag{6.18}$$

$$= \frac{1}{\left(f_{\mathrm{ma}}\chi_{\mathrm{ma}} + f_{\mathrm{ms}}\chi_{\mathrm{ms}} + f_{\mathrm{sa}\perp}\frac{k_{\mathrm{sa}}}{\epsilon_{\mathrm{sa}}} + f_{\mathrm{sa}\parallel}k_{\mathrm{sa}}\epsilon_{\mathrm{sa}}\right)/W + \sum_b p_b \tan\delta_b} \tag{6.19}$$

We obtain a material loss factors $\chi_i = t_i\epsilon_i\epsilon_i' \tan\delta_i$, that can be used to infer reasonable numbers for the thickness, dielectric constant, and loss tangent. The other variables in our fit model will be extracted from numerical simulations such as:

field factors: f_i

total field energy: W

bulk participation ratios: p_b

bulk loss tangents: $\tan\delta_b$

which can be simulated and assumed with a lower margin of error. Using measured resonators of the STAR type and SOI type, fit for these four parameters was applied across different geometries and feature sizes as shown in Figure 6.20. STAR type structures are indicated with resonator indices 1 - 7. Indices 1 - 3 use one parallel strand while increasing the center trace tether spacing with: 10, 30, and 90 microns. Indices 4 - 7 use a 60 micron tether spacing while increasing the number of parallel strands with: 1, 2, 3, and 4 strands. SOI resonators are indexed from 8 - 12 with (width/gaps) of: (10 / 1.1), (23 / 2.5), (50 / 5.5), (10 / 10), and (10 / 20) in microns. A full list of parameters are found in Table 6.4. The initial guess for a cross geometrical fit was chosen to be the assumed material parameters for our COMSOL simulations with $\chi_{ma} = 0.6 \times 10^{-12}$, $\chi_{ms} = 1.54 \times 10^{-12}$, $k_{sa} = 6 \times 10^{-12}$, and $\epsilon_{sa} = 3.9$. However, our fit suggests that χ_{ma} is about 50 times larger and χ_{ms} is much smaller than originally estimated, with k_{sa} about 8 times larger and ϵ_{sa} is relatively close to the predicted parameter value for thermal oxide. It must be emphasized that χ_{ms} has a very weak effect on the quality of fit, and is most likely not a accurate reflection of the loss properties at the metal-substrate interface.

We can use the substrate-air fit to infer for some 3nm interface such that $\tan\delta_{sa} \approx 0.08$. For the metal-air interface, we can also assume a 3nm interface with $\epsilon_{ma} = 5$, that the corresponding loss tangent should be $\tan\delta_{ma} \approx 0.05$. Because the metal-air and substrate-air interface fit values are relatively similar, we can perhaps assume that there is some uniform layer of lossy resist or device contamination that has not been removed. For example, the dielectric constant and loss tangent of Poly (methyl methacrylate) at room temperature is ≈ 4.0 and ≈ 0.017 respectively [104]. The front-side protection step using polydimethylglutarimide (MicroChem PMGI SF11) was baked at very high temperature (200 degrees C) to slow down the attack of aluminum from TMAH-based development of the backside features. Such a high baking temperature has been suggested to make the resist harder to remove [81], and a non-TMAH based developer should be used in the future, to ensure that a hard to remove protection layer is not needed.

Although quality factors were lower than expected for all resonators fabricated on this device, the shared fabrication process allows for a direct comparison between the two geometries. The key takeaway from these results is the following: due to the intrinsic bulk limits of the substrate, we cannot push the quality factors on SOI

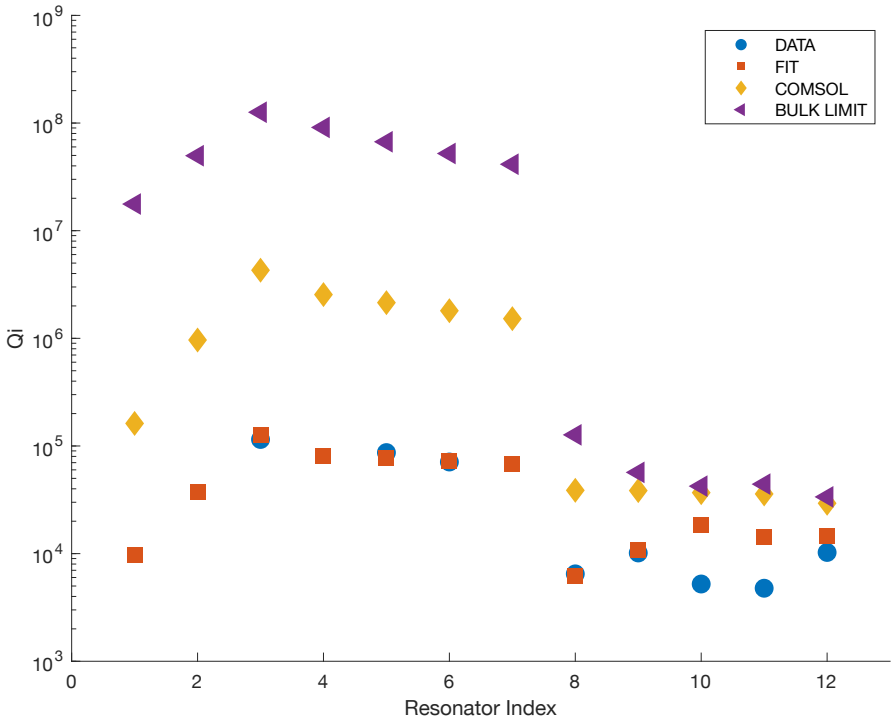


Figure 6.20: Fitted quality factors using simulated field factors from bulk features. The fitted parameters are: $\chi_{\text{ma}} = 30.51 \times 10^{-12}$, $\chi_{\text{ms}} = 3.89 \times 10^{-18} \approx 0$, $k_{\text{sa}} = 49.57 \times 10^{-12}$, and $\epsilon_{\text{sa}} = 4.746$. These parameters were fit to $\log_{10}$ of Q_i to equally weigh residuals for low and high quality factors. The COMSOL simulation with assumed interface loss values from literature. The bulk limit is assuming no interface losses, and only $\sum_b p_b \tan \delta_b$ contributes. STAR structures are indexed from 1 - 7 and SOI resonators are indexed from 8 - 12. SOI resonators with index 10 and 11 do not fit due to other factors such as vortex loss, which is a possibility with a trace width of 50 microns, or other unknown defects in the vicinity of the resonator.

much further through interface loss improvements; however, with the STAR structure, multiple orders of magnitude of improvement is possible if interface losses are suppressed. This is the fundamental distinction between SOI and STAR. The SOI substrate is fundamentally limited by bulk material losses, whereas STAR has multiple orders of magnitude of potential if interface losses are addressed.

An order of magnitude improvement on the same device that has undergone the same processing is a significant improvement, but the STAR structure provides some additional benefits which will aid the scaling of highly connected quantum circuits. As demonstrated in Figure 6.21, the cross sectional area is much smaller

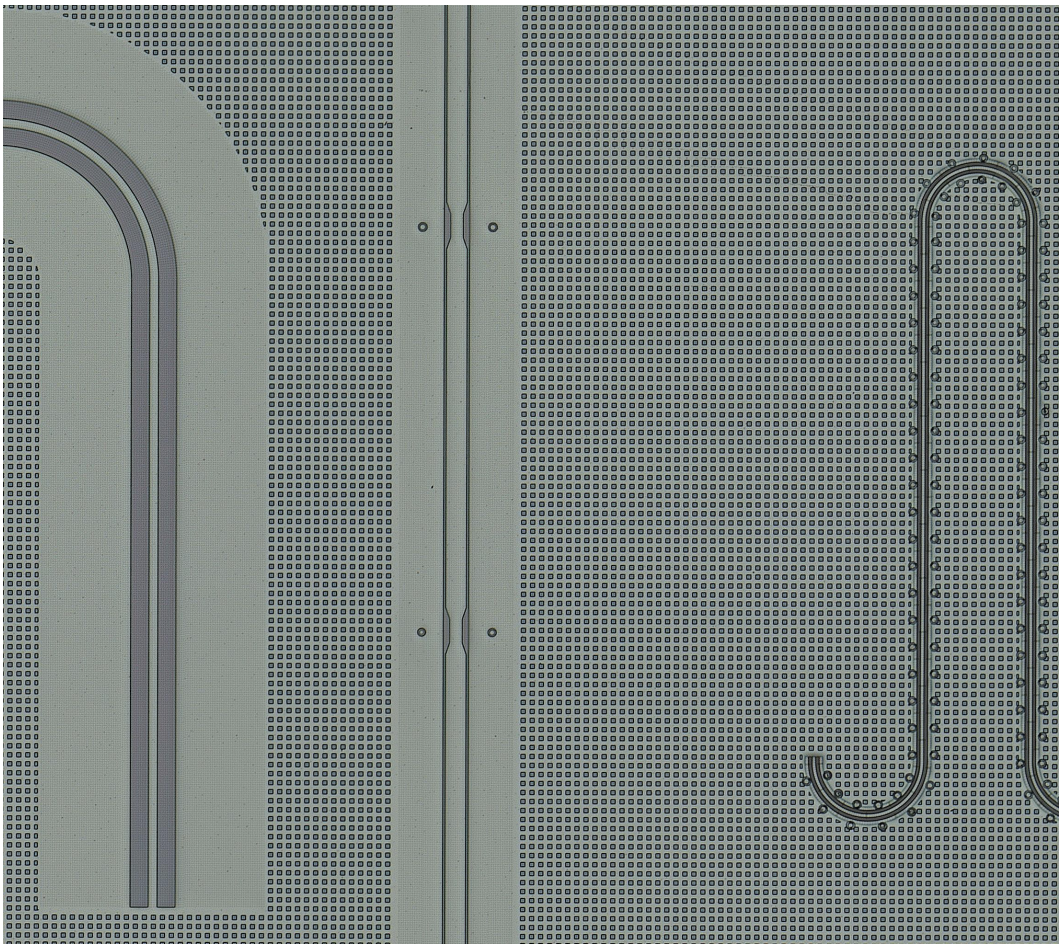


Figure 6.21: Micrograph of the STAR structure (right) next an SOI resonator stucture (left) with an SOI feedline in between. From left to right, the center trace widths of 10, 23, and 5 microns.

than the best performing SOI resonator geometry. The presence of the backing metal prevents microwave crosstalk across the device. In fact, all SOI resonators on this device could be interrogated from a port located on the other side of the device, indicating that crosstalk is extremely high with the SOI CPW geometry. STAR structures on the other hand, due to its air gap dielectric can only be locally addressed with small finger capacitors, and enables highly isolated resonators.

Chapter 7

FUTURE PROSPECTS AND OUTLOOK

7.1 Loss reduction strategy

By increasing fabrication complexity, such as the introduction of support tethers to suspend the metal center trace, or using more exotic superconductors such as TiN or NbTiN, one can yield many fold improvements in lifetime through the mitigation of dielectric loss [22]. This strategy is illustrated in Figure 7.1. However, the cost of fabrication complexity needs to be considered carefully, as the time to develop these improved structures may require much more time and capital resources. As microwave structures with lower loss are needed make highly coherent superconducting qubits, higher quality interfaces are required. The high intrinsic bulk limit of around 10^8 for STAR must be emphasised, if low loss, low radiation, and low crosstalk are also required. The SOI substrate on the other hand, is limited by the bulk to 10^5 for distributed microwave transmission lines. Thus, transmission line structures on SOI will not be a viable approach for the integration of optical and mechanical elements with high quality superconducting qubits. Although the test device characterized in this study did not attain promised improvements of over 30 times due to lossy material on the metal-air and substrate-air interfaces, STAR has a clear advantage with multiple orders of magnitude in potential improvement over SOI.

7.2 Qubits with STAR

Using STAR as a foundation for qubits is promising. We have seen that the capacitance per unit length is comparable to SOI, which allows for sub-millimeter scale qubits. As with any low crosstalk geometry, there will be a trade off between isolation and addressability. Although STAR is very low crosstalk, addressability is a possibly with close-proximity finger capacitors. Such close proximity capacitors would allow control and readout of STAR-based qubits through the XY drive line, the Z line (with low parasitic capacitive coupling), and the readout resonator. Qubit-qubit interactions could be mediated capacitively [8], but there are no restrictions for inductive coupling as well [25][38].

With a removed substrate directly under STAR, a qubit structure would require

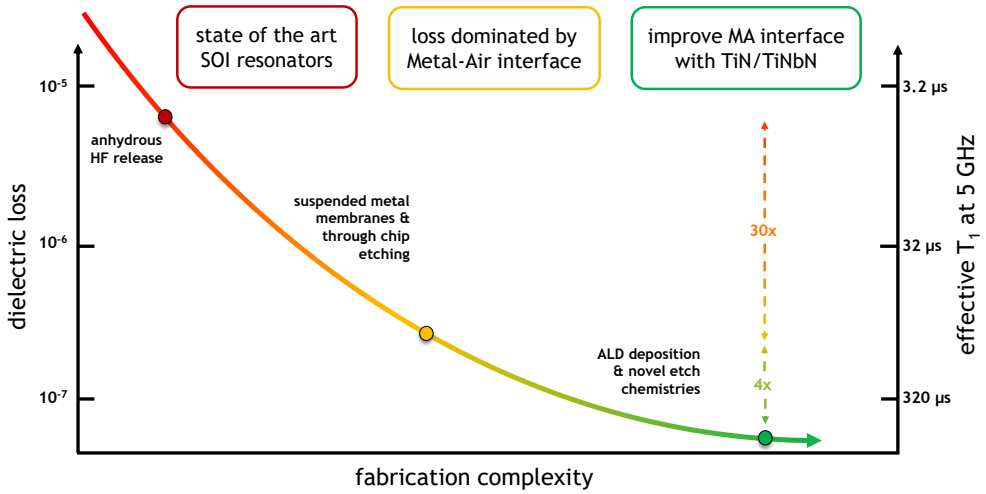


Figure 7.1: A path for loss reduction on SOI.

the suspension of Josephson junctions. This requirement is an advantage, since suspended junctions with 3D transmons have been realized and shown to increase lifetime by about a factor of two [27]. However, these suspended junctions suffered from flux noise, presumably from the new mechanical degree of freedom of the suspended structure. We can leverage the use of silicon support tethers to engineer suspended structures that are more rigid and less susceptible to flux noise generating vibrations. The integration of such junctions into STAR are possible with the current fabrication process. Immediately after the metal patterning step, junctions can be shadow evaporated onto the silicon oxide in the capacitor gap. Because the underlying material is removable with anhydrous HF, the suspension of junctions is no different than the suspension of other features found in STAR.

7.3 CQED CQAD

With improved lifetimes and possibly coherence, one can start leveraging these benefits for applications such as quantum memory for enhanced lifetimes. A possible implementation of this scheme is shown in Figure 7.2. Where a superconducting qubit is coupled to a long lived mechanical quantum memory element that has demonstrated lifetimes of over one second and coherence times of over one hundred milliseconds [60]. To mediate a coupling J_A, we use a high impedance LC coil [30] or Cooper-Pair Box [11] as an interface for the electrical side of the circuit. A low

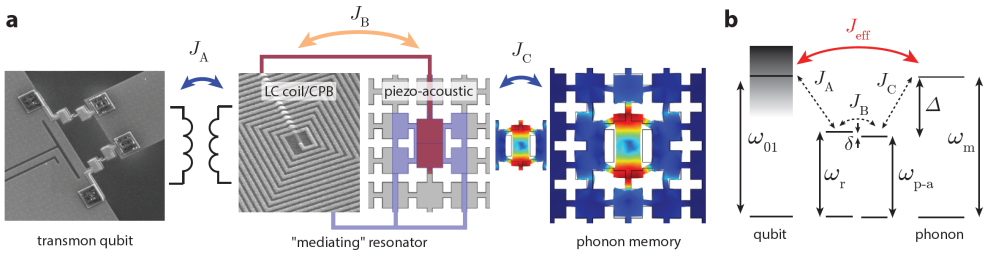


Figure 7.2: a) Coupling term and state transfer elements for a quantum memory module. b) Level diagram of each element with detunings during the swap operation.

loss piezo-acoustic element (aluminum nitride or lithium niobate) transducts with coupling J_B the electrical signal to a mechanical signal and acts as an interface to the mechanical memory element with coupling J_C.

To initialize the state transfer, the qubit is moved from highly detuned with ω_{01} (relative to the memory element and mediating resonators) to being on resonance with the memory element and detuned from the mediating resonator by Δ. During this time, a virtual coupling J_{eff} is realized through the mediating resonator. To calculate this coupling, we consider a relatively simple model for the memory storage system. The full Hamiltonian for the qubit-resonator system with phonon memory element is

$$\hat{H} = \hat{H}_q + \hat{H}_{qr} + \hat{H}_r + \hat{H}_{rm} + \hat{H}_m \tag{7.1}$$

We define each Hamiltonian as

$$\hat{H}_q = \hbar\omega_{01}\frac{\hat{\sigma}^Z}{2} \tag{7.2}$$

$$\hat{H}_{qr} = \hbar J_A\left(\hat{a}_1^\dagger\hat{\sigma}^- + \hat{a}_1\hat{\sigma}^+\right) \tag{7.3}$$

$$\hat{H}_r = \sum_{i=1}^{n}\hbar\omega\hat{a}_i^\dagger\hat{a}_i + \sum_{i=2}^{n}\hbar J_B\left(\hat{a}_i^\dagger\hat{a}_{i-1} + \hat{a}_{i-1}^\dagger\hat{a}_i\right) \tag{7.4}$$

$$\hat{H}_{rm} = \hbar J_C\left(\hat{a}_n^\dagger\hat{b} + \hat{b}^\dagger\hat{a}_n\right) \tag{7.5}$$

$$\hat{H}_m = \hbar\omega_m\hat{b}^\dagger\hat{b} \tag{7.6}$$

where there are n intermediary resonators between the qubit and memory element with coupling J_B between each resonator. The bosonic modes of the resonators are given by $\hat{a}_i$ and the bosonic modes of the phonon memory are given by $\hat{b}$.

We first diagonalize the Hamiltonian for intermediary resonators with eigenvalues of the coupled mode

$$\omega_k = \omega + 2J_B \sin\left(\frac{k\pi}{n+1}\right), \quad k \in \left\{-\frac{n-1}{2}, \cdots, \frac{n-1}{2}\right\} \tag{7.7}$$

Now, we represent the eigenstates of the coupled mode as

$$|\omega_k\rangle = \sum_{i=1}^{n} \alpha_{k,i} \hat{a}_k^\dagger |0\rangle \tag{7.8}$$

where $|0\rangle$ is the vacuum state of the resonator and

$$\left|\alpha_{k,1}\right| = \left|\alpha_{k,n}\right| = \frac{\cos\left(\frac{k\pi}{n+1}\right)}{\sqrt{(n+1)/2}}, \quad \frac{\alpha_{k,1}\alpha_{k,k}}{\left|\alpha_{k,1}\right|\left|\alpha_{k,n}\right|} = (-1)^k \tag{7.9}$$

Suppose the coupled mode operators are $\hat{c}_k$, then the Hamiltonian becomes

$$\begin{aligned}\hat{H} =& \hbar\omega_{01}\frac{\hat{\sigma}^Z}{2} + \hbar\omega_m \hat{b}^\dagger \hat{b} + \sum_{k=1}^{n} \hbar\omega_k \hat{c}_k^\dagger \hat{c}_k + \hbar J_A \alpha_{k,1}\left(\hat{c}_k^\dagger \hat{\sigma}^- + \hat{c}_k \hat{\sigma}^+\right) \\ &+ \hbar J_C \alpha_{k,n}\left(\hat{c}_k^\dagger \hat{b} + \hat{b}^\dagger \hat{c}_k\right)\end{aligned} \tag{7.10}$$

The states of interest for the quantum state transfer are $|\text{qubit}\rangle\,|\text{memory}\rangle = |g0\rangle, |e0\rangle, |g1\rangle, |e1\rangle$. Applying the qubit/memory interaction terms as a perturbation (in the dispersive limit) gives us to second order

$$|e0\rangle_2 = |e0\rangle_0 + 2\pi \sum_k \frac{J_A \alpha_{k,1}}{\omega_{01} - \omega_k} |g0\rangle \otimes \hat{c}_k^\dagger |0\rangle \tag{7.11}$$

$$|g1\rangle_2 = |g1\rangle_0 + 2\pi \sum_k \frac{J_C \alpha_{k,n}}{\omega_m - \omega_k} |g0\rangle \otimes \hat{c}_k^\dagger |0\rangle \tag{7.12}$$

$$|e1\rangle_2 = |e1\rangle_0 + 2\pi \sum_k \frac{J_A \alpha_{k,1}}{\omega_{01} - \omega_k} |g1\rangle \otimes \hat{c}_k^\dagger |0\rangle + \frac{J_C \alpha_{k,n}}{\omega_m - \omega_k} |e0\rangle \otimes \hat{c}_k^\dagger |0\rangle \tag{7.13}$$

The Hamiltonian in matrix form becomes in the basis $(|g0\rangle, |e0\rangle, |g1\rangle, |e1\rangle)$:

$$\hat{H}_{qm} = \tag{7.14}$$
$$\hbar \begin{bmatrix} -\frac{\omega_{01}}{2} + \delta\omega_q & 0 & 0 & 0 \\ 0 & \frac{\omega_{01}}{2} + \delta\omega_q & J_{\text{eff}} & 0 \\ 0 & J_{\text{eff}} & -\frac{\omega_{01}}{2} + \delta\omega_q + \omega_m + \delta\omega_m & 0 \\ 0 & 0 & 0 & \frac{\omega_{01}}{2} + \delta\omega_q + \omega_m + \delta\omega_m \end{bmatrix}$$

where the qubit and memory frequencies have been respectively shifted slightly by $\delta\omega_q$ and $\delta\omega_m$. The cross terms from the $\frac{\left|\langle m^{(0)}|\hat{H}_{int}|n^{(0)}\rangle\right|^2}{E_n - E_m}$ correction in the perturbation go into a coupling term

$$J_{\text{eff}} = \frac{J_A J_C}{2} \sum_k \alpha_{k,1}\alpha_{k,n} \left(\frac{1}{\omega_{01} - \omega_k} + \frac{1}{\omega_m - \omega_k} \right) \tag{7.15}$$

We define $\Delta_q = \omega_{01} - \omega$ and $\Delta_m = \omega_m - \omega$ as the detuning from qubit/memory to the bare resonator frequency, so that using (7.9) yields

$$J_{\text{eff}} = \frac{2J_A J_C}{n+1} \sum_{k=-\frac{n-1}{2}}^{\frac{n-1}{2}} (-1)^k \cos^2\left(\frac{k\pi}{n+1}\right) \left(\frac{1}{\Delta_q - (\omega_k - \omega)} + \frac{1}{\Delta_m - (\omega_k - \omega)} \right) \tag{7.16}$$

$$= \frac{2J_A J_C}{n+1} \sum_{k=-\frac{n-1}{2}}^{\frac{n-1}{2}} (-1)^k \cos^2\left(\frac{k\pi}{n+1}\right) \left(\frac{1}{\Delta_q - 2J_B \sin\left(\frac{k\pi}{n+1}\right)} + \frac{1}{\Delta_m - 2J_B \sin\left(\frac{k\pi}{n+1}\right)} \right) \tag{7.17}$$

Let's take n=2, as is the case with the case with our system

$$J_{\text{eff}} = \frac{J_A J_C}{2} \left[\frac{1}{\Delta_m - J_B} - \frac{1}{\Delta_m + J_B} + \frac{1}{\Delta_q - J_B} - \frac{1}{\Delta_q - J_B} \right] \tag{7.18}$$

and in the dispersive limit where $J_B \ll \Delta = \Delta_m = \Delta_q$

$$J_{\text{eff}} \approx \frac{2J_A J_B J_C}{\Delta^2} \left[1 + \left(\frac{J_B}{\Delta} \right)^2 \right] \tag{7.19}$$

Using some realistic parameters that are typical of these piezo-acoustical and optical devices [12][30][60] [64][65], we find that $J_{\text{eff}} \approx 250$ KHz, corresponding to a state transfer time of about 1μs. Clearly, with a qubit lifetime of 3.5μs on SOI, the qubit would have decayed quite substantially by the time the state transfer is complete (roughly up a fidelity of 75%, assuming $2T_1 = T_2^*$). However, with a tenfold improvement in lifetime as seen with STAR, we can hope to achieve a qubit with a lifetime of 35μs, which would enable higher fidelity (up to 97% in this case) storage and retrieval of long lived quantum states.

The suspended trace air-gap resonator structure offers unique advantages in many different respects. Not only is the structure low loss, by moving the field density

into the metal-air interface and vacuum, there are multiple attributes that cannot be achieved on even conventional silicon and sapphire substrates. STAR takes advantage of the buried oxide layer as a spacer for tightly confined electrodes, and with through oxide vias serving as a shield in the lateral direction, cross sectional areas as small as 25 microns wide by 3 microns high can be achieved. This extent rivals even conventional substrates because of the shielded nature of the geometry. These structures can be placed pitch to pitch with relatively low crosstalk, or extremely low crosstalk if a shielding bridge on the topside is used. In conventional substrates, the fields extend out across the substrate, and even in conventional substrates where a shielding bridge is incorporated [32], crosstalk between neighboring lines through the underlying substrate remains an issue.

Thus, there are exciting opportunities ahead - with new challenges, such as careful studies of surface science at the interfaces and process development to enable new processing techniques. STAR truly enables the integration of high quality superconducting qubits with optical and mechanical systems on their native substrate, allowing for the development of hybrid technologies for distributed quantum computing.

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Appendix A

Z_0 AND EFFECTIVE PERMITTIVITY OF QUASI-TEM MICROWAVE STRUCTURES

A.1 Basic concept

Using various conformal mapping techniques [111] [3], the characteristic impedance and effective permittivity of a microwave structure with a quasi-TEM mode can represented simply by:

$$Z_0 = \frac{Z_0^{\text{air}}}{\sqrt{\varepsilon_{\text{eff}}}} \tag{A.1}$$

$$\varepsilon_{\text{eff}} = \frac{C_{\text{CPW}}}{C_{\text{air}}} \tag{A.2}$$

C_{CPW} is the capacitance per unit length of the structure with all dielectrics in place, and C_{air} is the capacitance per unit length if all delectrics have been replaced by air (i.e. the vacuum capacitance). Thus, we simply need to set up a simulation where we swap out the dielectrics for air and take the ratio of the capacitances. The mode of propagation must be quasi-TEM, because this condition allows us to use the DC capacitance to find the capacitance per unit length of the transmission line.

A.2 Example 1: CPW on SOI

2D geometry

Build half of your geometry (zero charge bndy condition takes care of symmetry)

Leave metal regions as undefined (empty)

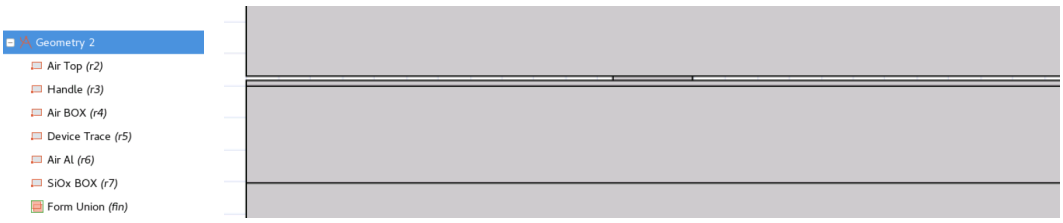

Figure A.1: COMSOL geometry setup with the metal regions left empty.

For a 23 micron trace and 2.5 micron gap on SOI we have:

Materials

For convenience, you can put Air at the top to apply to all domains initially.

Add a Material Switch. One for Si regions, and one for buried oxide regions (if applicable).

Have both Air and the material of your geometry (Si/BOX) under the switch. The idea is to use the switch to change between Air and Si in the silicon regions, similarly for the buried oxide regions.

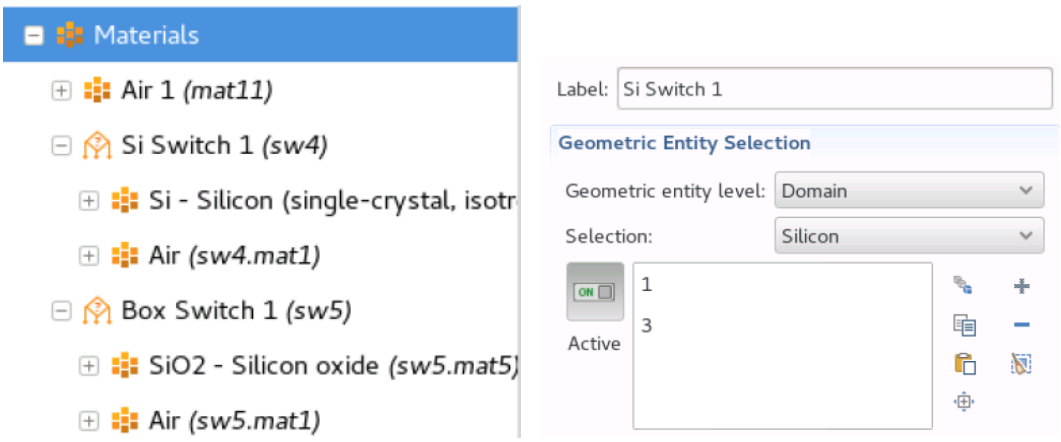

Figure A.2

Electrostatics module

Add Terminal and Ground boundaries to relevant locations. Put 1 V on the terminal.

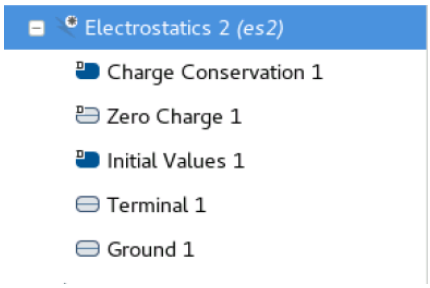

Figure A.3

Study

Do a stationary study with a material sweep. Sweep between the actual material of the substrate and air.

Results

Evaluate the capacitance with different material combinations We see that for the silicon regions (Si Switch) being Silicon (index 1) or Air (index 2) has the largest impact on the capacitance for this structure (the BOX undercut is 100 microns away

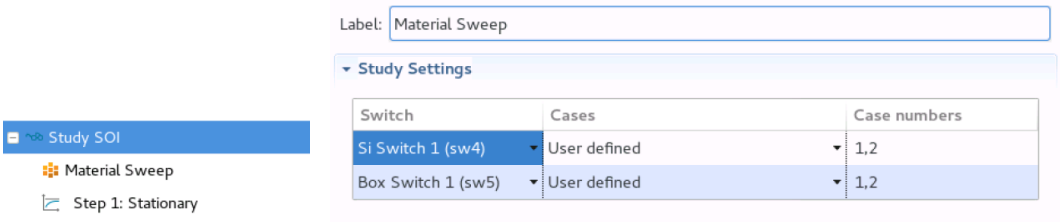

Figure A.4

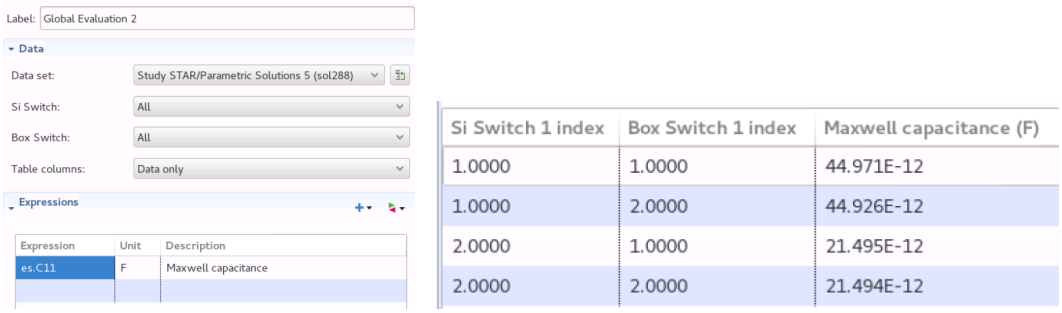

Figure A.5

from CPW). Note that the unit here is actually Farad/meter because we've done a cross section simulation.

A.3 Finding ε effective and Z_0

Thus, using Figure A.5, we can estimate the effective permittivity as: 44.97/21.495 = 2.092. For this particular simulation we had a 23 micron trace and a 2.5 micron gap. For comparison, you can set up a simulation in Sonnet and look at the port results to obtain 2.085 (within a percent accurate). The pro for COMSOL is that this will still work for much more complicated structures. The pro for Sonnet obviously being simplicity of set up and speed.

Also note that with:

$$Z_0^{\text{air}} = \frac{1}{c\, C_{\text{air}}}$$

where c is the velocity of light in free space, we can also find the characteristic impedance from these capacitances as:

$$Z_0 = \frac{1}{c\, \sqrt{C_{\text{CPW}} C_{\text{air}}}}$$

But be extra careful here if you've simulated half of the structure. Don't forget that the simulated capacitances are smaller than the actual capacitances by a factor of two, so adjust for this when finding Z_0. This factor of two did not matter when finding ε_{eff} because the factors cancel out.

With a 23 micron trace and 2.5 micron gap for SOI, we find Z_0 = 53.64 Ohms. Remember again, that the unit of the capacitance result is Farad/meter.

A.4 Example 2: Suspended Trace Air-gap Resonator (STAR

Here is a STAR geometry with 4 micron trace and gap. There is a VIA connecting the two grounds. Silicon is highlighted in blue.

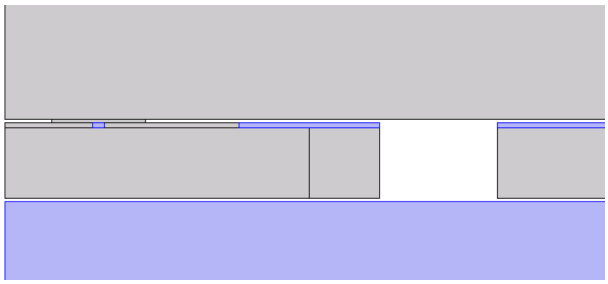

Figure A.6

This is the ground selection under Electrostatics:

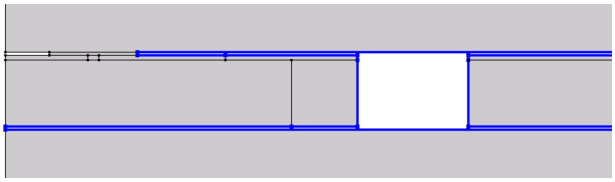

Figure A.7

We obtain:

Si Switch index	Box Switch index	Maxwell capacitance (F)
1.0000	1.0000	17.393E-12
1.0000	2.0000	17.393E-12
2.0000	1.0000	17.354E-12
2.0000	2.0000	17.354E-12

Figure A.8

Which yields:

$$\varepsilon_{\text{eff}} = 1.00225, \quad Z_0 = 96\Omega$$

As expected, the effective permittivity is more or less unity (a built-in feature of STAR) and the characteristic impedance is around 100 Ohm, the design target. Numerical analytics yielded 104.6 Ohms but is assuming that $\varepsilon_{\text{eff}} \equiv 1$, and did not include the fine details such as the slight existence of silicon in the tethers and the rest in device layer.

A.5 Other methods

There are other methods such as calculating the Wave Impedance which can be a little more tedious. You need to find the electric and magnetic fields in the x direction. Alternatively, the characteristic impedance can be found numerically, via the solution to conformal mapping methods.

Listing A.1: Microshield characteristic impedance Z_0 calculation script, written in Julia.

```
# MICROSHIELD CALCULATOR
#
# Michael Fang
# June 2018
#
# Based on the chapter 'Microshield Lines and Couplged Coplanar Waveguide' from
# "Coplanar Waveguide Circuits, Compnents, and Systems" by Rainee N. Simons

using Unitful
import Elliptic

const ξ = sqrt(π^2 - 8)
const ζ = (π - ξ)/4

S_helper(tc) = asin(tc*ζ) + asinh(tc*ζ/sqrt(1 - tc^2)) + (sqrt(1 - tc^2/2*(1 - ζ*ξ))
- sqrt(1 - tc^2/2*(1 + ζ*ξ)))/(tc*ζ)

"""
Capacitances (C_a, C_CR, C_CR_vac) of a rectangular microshield line with parameters:
`trace` - trace width of coplanar waveguide
`gap` - gap width of coplanar waveguide
`extent` - extent of ground plane if finite
`L` - width of cavity in transverse direction
`h` - depth of cavity in transverse direction
`ϵr` - relative permitivity of dieletric under center trace
"""
function microshield_cap(trace, gap, extent, L, h; ϵr = 1)
```

```
    a = trace/2.0
    b = a + gap
    c = extent/2.0
    k1 = c/b*sqrt(b^2 - a^2)/sqrt(c^2 - a^2)
    kp1 = sqrt(1 - k1^2)
    # kp1 = a/b*sqrt(c^2 - b^2)/sqrt(c^2 - a^2)
    C_a = uconvert(u"F/m", 2*Unitful.ϵ0*Elliptic.K(kp1)/Elliptic.K(k1))
    if L/(2*h) < 1.0
        tc = sqrt(big"1.0" - ((exp(big"2.0"*h*π/L) - big"2")/(exp(big"2.0"*h*π/L) +
big"2"))^4)
    else
        tc = ((exp(L*π/(big"2"*h)) - big"2.0")/(exp(L*π/(big"2"*h)) + big"2"))^2
    end
    if tc == 1
        println("NOPE!")
    end
    δ1 = big"1.0"/S_helper(tc)*asin(tc*ζ)
    δ2 = big"1.0" - big"1.0"/S_helper(tc)*asinh(tc*ζ/sqrt(1 - tc^2))
    if 2*a/L < δ1
        δ1_eval(x) = sin(sin(2*x/L*S_helper(tc))/tc)*tc
        ta = δ1_eval(a)
        tb = δ1_eval(b)
    elseif 2*a/L < δ2
        δ2_eval(ψ) = sin(π/4 + ((1 - ψ^2)/tc^2 - 1/2)/(2*ζ))*tc
        ψ(x) = sqrt(1 - tc^2/2*(1 - ζ*ξ)) - tc*ζ*S_helper(tc)*(2*x/L - δ1)
        ta = δ2_eval(ψ(a))
        tb = δ2_eval(ψ(b))
    else
        else_eval(x) = cos(sqrt(1 - tc^2)/tc*sinh((1 - 2*x/L)*S_helper(tc)))*tc
        ta = else_eval(a)
        tb = else_eval(b)
    end
    k2 = ta/tb
    kp2 = sqrt(big"1.0" - k2^2)
    C_CR = uconvert(u"F/m", 2*Unitful.ϵ0*ϵr*Elliptic.K(k2)/Elliptic.K(kp2))
    C_CR_vac = uconvert(u"F/m",2*Unitful.ϵ0*Elliptic.K(k2)/Elliptic.K(kp2))
    return C_a, C_CR, C_CR_vac
end


"""
Effective permitivity of a rectangular microshield line with parameters:
`trace` - trace width of coplanar waveguide
`gap` - gap width of coplanar waveguide
`extent` - extent of ground plane if finite
`L` - width of cavity in transverse direction
`h` - depth of cavity in transverse direction
`ϵr` - relative permitivity of dieletric under center trace
"""
function microshield_eff(trace, gap, extent, L, h; ϵr = 1)
    (C_a, C_CR, C_CR_vac) = microshield_cap(trace, gap, extent, L, h, ϵr = ϵr)
    (C_a + C_CR)/(C_a + C_CR_vac)
```

```
end

"""
Characteristic impedance of a rectangular microshield line with parameters:
`trace` - trace width of coplanar waveguide
`gap` - gap width of coplanar waveguide
`extent` - extent of ground plane if finite
`L` - width of cavity in transverse direction
`h` - depth of cavity in transverse direction
`ϵr` - relative permitivity of dieletric under center trace
"""
function microshield_Z0(trace, gap, extent, L, h; ϵr = 1)
    (C_a, C_CR, C_CR_vac) = microshield_cap(trace, gap, extent, L, h, ϵr = ϵr)
    ϵeff = (C_a + C_CR)/(C_a + C_CR_vac)
    uconvert(u"Ω", 1/(Unitful.c0*(C_a +  C_CR_vac)*sqrt(ϵeff)))
end
```

Appendix B

CAPACITIVE COUPLING STRENGTH *G*

Following the circuit analysis done in other works[29, 39], the Lagrangian for the circuit drawn in Figure B.1 is

$$\mathcal{L} = \left(\frac{\Phi_0}{2\pi}\right)^2 \left[\frac{C_1\dot{\varphi}_1^2}{2} + \frac{C_2\dot{\varphi}_2^2}{2} + \frac{C_c\left(\dot{\varphi}_2^2 - \dot{\varphi}_1^2\right)^2}{2}\right] - U \tag{B.1}$$

where U is the energy contributed by the inductive elements of the circuit. It follows that the conjugate momenta for node variables $\varphi_{1,2}$ are

$$p_{1,2} = \frac{\partial\mathcal{L}}{\partial\dot{\varphi}_{1,2}} = \left(\frac{\Phi_0}{2\pi}\right)^2 \left[C_{1,2}\dot{\varphi}_{1,2} - C_c\left(\dot{\varphi}_{2,1} - \dot{\varphi}_{1,2}\right)\right] \tag{B.2}$$

We solve for the $\dot{\varphi}$ in terms of the momenta

$$\dot{\varphi}_{1,2} = \left(\frac{2\pi}{\Phi_0}\right)^2 \frac{C_{2,1}p_{1,2} + C_c\left(p_1 + p_2\right)}{C_1C_2 + C_1C_c + C_2C_c} \tag{B.3}$$

Now we can write a Hamiltonian as

$$\mathcal{H} = \left(\frac{2\pi}{\Phi_0}\right)^2 \left[\frac{C_2 + C_c}{C_1C_2 + C_1C_c + C_2C_c}\frac{p_1^2}{2}\right. \tag{B.4}$$

$$+ \frac{C_1 + C_c}{C_1C_2 + C_1C_c + C_2C_c}\frac{p_2^2}{2} \tag{B.5}$$

$$\left. + \frac{C_c}{C_1C_2 + C_1C_c + C_2C_c}p_1p_2\right] + U \tag{B.6}$$

so that the coupling term is the p_1p_2 term:

$$\mathcal{H}_c = \left(\frac{2\pi}{\Phi_0}\right)^2 \left[\frac{C_c}{C_1C_2 + C_1C_c + C_2C_c}\right] p_1p_2 \tag{B.7}$$

Recall that we can write the position and momentum operators as

$$\hat{X} = \sqrt{\frac{\hbar}{2m\omega}}\left(a + a^\dagger\right) \tag{B.8}$$

$$\hat{P} = -i\sqrt{\frac{\hbar m\omega}{2}}\left(a - a^\dagger\right) \tag{B.9}$$

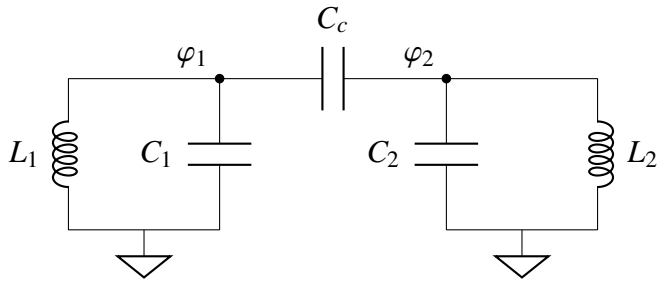

Figure B.1: Circuit model for capacitively coupled resonators. Two resonators coupled via capacitance C_c. φ_1 and φ_2 denote the node flux variables which have conjugate momentum $p_i = \frac{\partial \mathcal{L}}{\partial \dot{\varphi}_i}$.

Also note that the LC resonators in our circuit have a direct analogy to the harmonic oscillator. This is easily seen by focusing on the kinetic terms

$$\frac{\hat{P}_{1,2}^2}{2m_{1,2}} \equiv \frac{1}{2}\left(\frac{2\pi}{\Phi_0}\right)^2 \left[\frac{C_{2,1} + C_c}{C_1C_2 + C_1C_c + C_2C_c}\right] p_{1,2}^2 \tag{B.10}$$

$$\Rightarrow m_{1,2} \equiv \left(\frac{\Phi_0}{2\pi}\right)^2 \frac{C_1C_2 + C_1C_c + C_2C_c}{C_{2,1} + C_c} \tag{B.11}$$

We work in the basis spanned by the energy levels of a harmonic oscillator and see that the momenta can be written

$$p_{1,2} = -i\sqrt{\frac{\hbar\omega_{1,2}m_{1,2}}{2}}\left(a_{1,2} - a_{1,2}^\dagger\right) \tag{B.12}$$

$$= \left(\frac{2\pi}{\Phi_0}\right)\sqrt{\frac{\hbar\omega_{1,2}}{2}\frac{C_1C_2 + C_1C_c + C_2C_c}{C_{2,1} + C_c}}\hat{M}_{1,2} \tag{B.13}$$

with a matrix $\hat{M}$ of coefficients determined from the lowering and raising operators acting on various energy eigenstates. It now directly follows from (B.7) and (B.13) that the coupling frequency g is found from

$$\mathcal{H}_c = hg\hat{M}_1\hat{M}_2 \tag{B.14}$$

$$= h\left[\frac{\sqrt{f_1 f_2}}{2}\frac{C_c}{\sqrt{(C_1 + C_c)(C_2 + C_c)}}\right]\hat{M}_1\hat{M}_2 \tag{B.15}$$

$$\omega_i = 2\pi f_i = \frac{1}{\sqrt{L_iC_i}} \tag{B.16}$$

such that the splitting is $\delta = 2g$. A similar derivation can be found in Daniel Sank's thesis[87]. This toy circuit model is a good approximation for the case where a qubit is capacitively coupled to a resonator when the anharmonicity is small.

Appendix C

TRANSLATING QUBIT COUPLINGS INTO σ OPERATORS

C.1 Single Qubit, $\hat{\sigma}^x$ and $\hat{\sigma}^y$

Consider a general qubit Hamiltonian in the form

$$\hat{H} = \frac{\hat{Q}^2}{2C} + V\left(\hat{\Phi}\right). \tag{C.1}$$

We wish to find an expression relating the operator $\hat{Q}$ and $\hat{\Phi}$. To do so, we look at two commutators:

$$[\hat{\Phi}, \hat{Q}] = i\hbar \tag{C.2}$$

$$[\hat{H}, \hat{\Phi}] = \frac{[\hat{Q}^2, \hat{\Phi}]}{2C} \tag{C.3}$$

where we find that $[\hat{Q}^2, \hat{\Phi}] = -2i\hbar\hat{Q}$ by Eq. C.2. The transitions of the qubit between the ground state to excited state can be written as matrix elements of each operator in the two state basis spanned by $|0\rangle$ and $|1\rangle$. The matrix element corresponding to the transition from the ground to excited state of Eq. (C.3) is

$$\left\langle 1 \middle| [\hat{H}, \hat{\Phi}] \middle| 0 \right\rangle = \frac{\left\langle 1 \middle| [\hat{Q}^2, \hat{\Phi}] \middle| 0 \right\rangle}{2C} \tag{C.4}$$

$$\left\langle 1 \middle| \hat{H}\hat{\Phi} - \hat{\Phi}\hat{H} \middle| 0 \right\rangle = -\frac{i\hbar}{C} \left\langle 1 \middle| \hat{Q} \middle| 0 \right\rangle \tag{C.5}$$

$$(\hbar\omega_1 - \hbar\omega_0) \left\langle 1 \middle| \hat{\Phi} \middle| 0 \right\rangle = -\frac{i\hbar}{C} \left\langle 1 \middle| \hat{Q} \middle| 0 \right\rangle \tag{C.6}$$

$$i\omega_{10} C \left\langle 1 \middle| \hat{\Phi} \middle| 0 \right\rangle = \left\langle 1 \middle| \hat{Q} \middle| 0 \right\rangle \tag{C.7}$$

where we have used $\omega_{10} = \omega_1 - \omega_0$. Similarly, the excited to ground state transition is

$$-i\omega_{10} C \left\langle 0 \middle| \hat{\Phi} \middle| 1 \right\rangle = \left\langle 0 \middle| \hat{Q} \middle| 1 \right\rangle. \tag{C.8}$$

Evaluating the diagonal matrix elements show that $\hat{Q}$ can only have non-zero off diagonal terms since

$$\left\langle 0 \middle| [\hat{H}, \hat{\Phi}] \middle| 0 \right\rangle = (\hbar\omega_0 - \hbar\omega_0) \left\langle 0 \middle| \hat{\Phi} \middle| 0 \right\rangle = 0 \tag{C.9}$$

$$\left\langle 1 \middle| [\hat{H}, \hat{\Phi}] \middle| 1 \right\rangle = (\hbar\omega_1 - \hbar\omega_1) \left\langle 1 \middle| \hat{\Phi} \middle| 1 \right\rangle = 0 \tag{C.10}$$

Consider the potential V in the harmonic limit. We have

$$[\hat{H}, \hat{Q}] = \frac{[\hat{\Phi}^2, \hat{Q}]}{2L} \tag{C.11}$$

Repeating the same procedure as before, we obtain

$$-i\omega_{10} L \left\langle 1 \middle| \hat{Q} \middle| 0 \right\rangle = \left\langle 1 \middle| \hat{\Phi} \middle| 0 \right\rangle \tag{C.12}$$

$$i\omega_{10} L \left\langle 0 \middle| \hat{Q} \middle| 1 \right\rangle = \left\langle 0 \middle| \hat{\Phi} \middle| 1 \right\rangle \tag{C.13}$$

$$\left\langle 0 \middle| \hat{\Phi} \middle| 0 \right\rangle = 0 \tag{C.14}$$

$$\left\langle 1 \middle| \hat{\Phi} \middle| 1 \right\rangle = 0 \tag{C.15}$$

so that $\hat{\Phi}$ will also only have non-zero diagonal elements. With this in mind, we can assume $\hat{Q}$ to have either of two forms

$$\hat{Q} = \alpha \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} = \alpha\hat{\sigma}^x \text{ or } \beta \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix} = \beta\hat{\sigma}^y \tag{C.16}$$

in the two state basis. $\hat{\Phi}$ is found from Eq. (C.7) and (C.8), with $\omega_{10} = 1/\sqrt{LC}$, to be either

$$\hat{\Phi} = -\alpha\sqrt{\frac{L}{C}}\hat{\sigma}^y \text{ or } \beta\sqrt{\frac{L}{C}}\hat{\sigma}^x. \tag{C.17}$$

Thus, we have the following relation between the flux and charge operators:

$$\hat{\Phi} = i\hat{\sigma}^z\sqrt{\frac{L}{C}}\hat{Q} \tag{C.18}$$

or in terms of a Pauli Z rotation operator

$$\hat{R}_Z(\theta) = \exp(-i\theta\hat{\sigma}^z) = \begin{pmatrix} e^{-i\theta} & 0 \\ 0 & e^{i\theta} \end{pmatrix} \tag{C.19}$$

as

$$\hat{\Phi} = \hat{R}_Z\left(\frac{\pi}{2}\right)\sqrt{\frac{L}{C}}\hat{Q} \tag{C.20}$$

where $\sqrt{\frac{L}{C}}$ is equivalent to the characteristic impedance Z_0 of a transmission line. Interestingly, we can rewrite the time derivative of Eq. C.8 and C.12 so that

$$\left\langle 0 \middle| \hat{V} \middle| 1 \right\rangle = Z_C \left\langle 0 \middle| \hat{I} \middle| 1 \right\rangle \text{ and } \left\langle 1 \middle| \hat{V} \middle| 0 \right\rangle = Z_L \left\langle 1 \middle| \hat{I} \middle| 0 \right\rangle \tag{C.21}$$

Thus, it follows that $\hat{V} = \hat{I}\hat{Z}$ with

$$\hat{Z} = \begin{pmatrix} Z_L & 0 \\ 0 & Z_C \end{pmatrix} \tag{C.22}$$

where $Z_L = i\omega_{10}L$ and $Z_C = 1/i\omega_{10}C$.

C.2 Two Coupled Qubits

A Hamiltonian for two qubits with both inductive and capacitive coupling, g_L and g_C, is

$$\hat{H} = \sum_{i=1,2} \frac{\hat{Q}_i^{\,2}}{2C_i} + \frac{\hat{\Phi}_i^{\,2}}{2L_i} + g_C \hat{Q}_1 \hat{Q}_2 + g_L \hat{\Phi}_1 \hat{\Phi}_2. \tag{C.23}$$

We use Eq. (C.18) to rewrite the Hamiltonian as

$$\hat{H} = \sum_{i=1,2} \frac{\hat{Q}_i^{\,2}}{2C_i} + \frac{\hat{\Phi}_i^{\,2}}{2L_i} + g_C \hat{Q}_1 \hat{Q}_2 - g_L \sqrt{\frac{L_1 L_2}{C_1 C_2}} \hat{\sigma}_1^z \hat{Q}_1 \hat{\sigma}_2^z \hat{Q}_2. \tag{C.24}$$

so that if the capacitive $\hat{Q}_1\hat{Q}_2$ interaction is of type $\hat{\sigma}_1^x\hat{\sigma}_2^x$, the inductive $\hat{\Phi}_1\hat{\Phi}_2$ interaction is of type $i\hat{\sigma}_1^z\hat{\sigma}_1^x i\hat{\sigma}_2^z\hat{\sigma}_2^x = \hat{\sigma}_1^y\hat{\sigma}_2^y$. If the capacitive interaction is of type $\hat{\sigma}_1^y\hat{\sigma}_2^y$, the inductive interaction is of type $\hat{\sigma}_1^x\hat{\sigma}_2^x$.

Appendix D

ATTENUATING JOHNSON NOISE IN A DILUTION REFRIGERATOR

D.1 Background

In the 1920s, Johnson showed that a particular noise with some power linearly proportional to temperature exists in all electrical conductors [45]. Shortly afterwards, Nyquist showed that one can use statistical mechanics to derive results consistent with Johnson's experiment [74]. Since Johnson's linear approximation only works for high temperatures, we wish to calculate how the Johnson noise scales down to mK temperatures found in cryogenic apparatuses.

D.2 Derivation

We assume the conductor to be some 1D blackbody (imagine a wire) and calculate its spectral density. Let us first consider the Bose-Einstein distribution:

$$N(n) = \frac{2}{e^{\epsilon_n/k_BT} - 1} \tag{D.1}$$

with a factor of 2 coming from the left and right polarizations of the photon. For a bath of photons with energy $\hbar\omega_n$ we see that the energy is

$$\langle E_n \rangle = \frac{2\hbar\omega_n}{e^{\hbar\omega_n/k_BT} - 1} \tag{D.2}$$

The density of states of photons is found via the 1D wave equation

$$V_n(x,t) = V_0 e^{i(k_n x + \omega_n t)} \tag{D.3}$$

For a conductor of length L and $V_n(0,t) = V_n(L,t)$, we have $n = \frac{L}{2\pi}k_n$ and

$$D(\omega)d\omega = \frac{1}{L}\frac{dn}{d\omega}d\omega = \frac{1}{L}\frac{dn}{dk_n}\frac{dk_n}{d\omega_n}d\omega = \frac{1}{L}\frac{L}{2\pi}\frac{1}{v}d\omega = \frac{d\omega}{2\pi v} \tag{D.4}$$

where the wave velocity v is ω_n/k_n. The power going out of the conductor is half of the total power, so the spectral power is given by

$$P(\omega) = \frac{1}{2}vE(\omega)D(\omega)d\omega = \frac{1}{2\pi}\frac{\hbar\omega}{e^{\hbar\omega/k_BT} - 1}d\omega \tag{D.5}$$

If we expand the exponential

$$P(\omega) = \frac{1}{2\pi}\frac{\hbar\omega}{\left(\frac{\hbar\omega}{k_BT}\right) + \frac{1}{2!}\left(\frac{\hbar\omega}{k_BT}\right)^2 + \cdots}d\omega \tag{D.6}$$

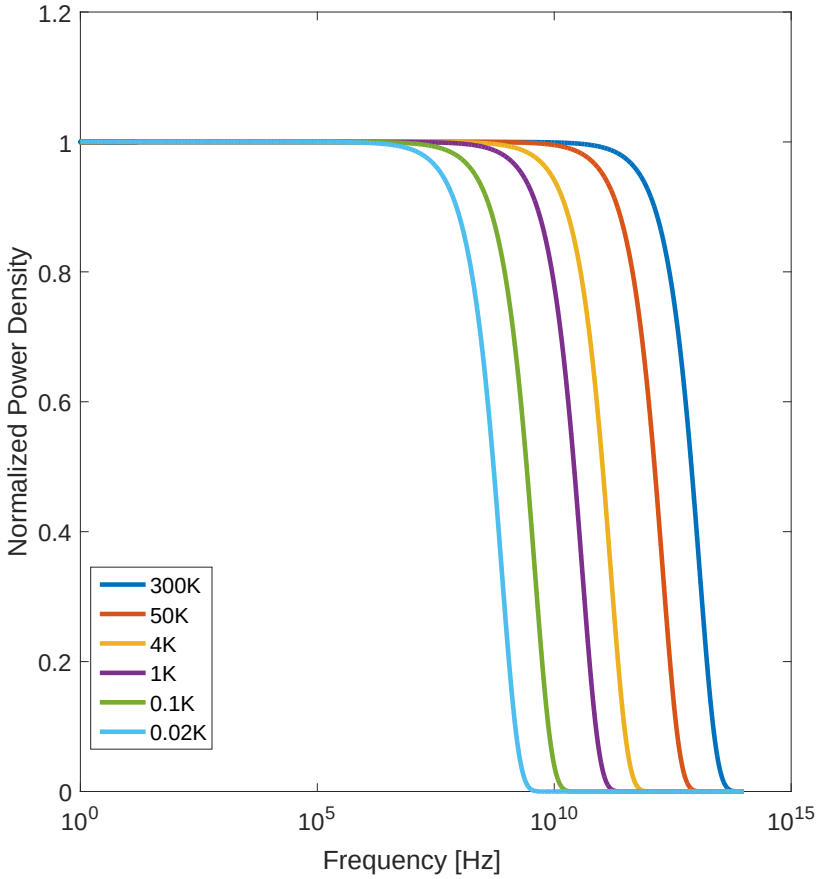

Figure D.1: Normalized spectral density $P(\omega)/k_BT$ vs frequency for some temperatures relevant to a dilution refrigerator.

and keep the first order term, we have

$$P(\omega) \approx \frac{k_BT}{2\pi} d\omega \tag{D.7}$$

The normalized spectral density $P(\omega)/k_BT$ is mostly constant up to some cut off frequency as seen in Fig. 1, so a linear approximation for power holds well. Finally, the total power over some bandwidth 0 to F is

$$\bar{P} = \frac{1}{2\pi} \int_0^{2\pi F} \frac{\hbar\omega}{e^{\hbar\omega/k_BT} - 1} d\omega \approx \frac{1}{2\pi} \int_0^{2\pi F} k_BT\, d\omega = k_BTF \tag{D.8}$$

The total power is shown exactly for a few bandwidths in Fig. D.2. We want to place attenuators on our cryogenic cabling to proportionally suppress Johnson noise at each stage in a dilution refrigerator. For example we see that we would like a 10 dB attenuator on the 60K flange, because the Johnson noise power will be 10 dB lower than at 300K. We would place another 10 dB attenuator at 4K for 10 dB of

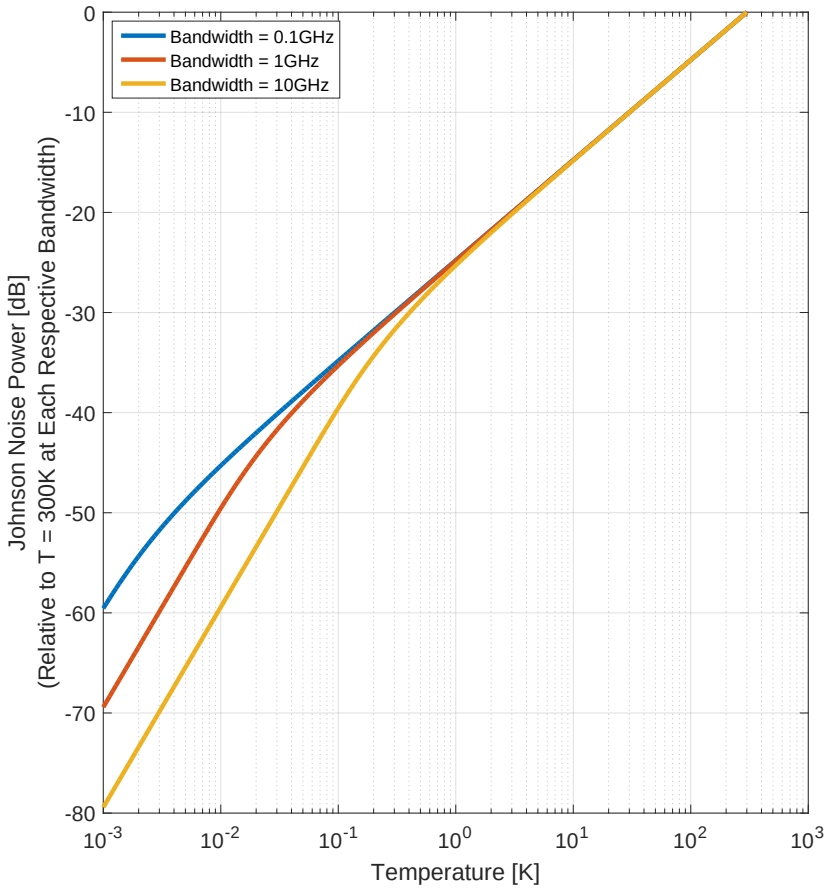

Figure D.2: Johnson noise power $\bar{P}$ (in dB with respect to 300K) vs. stage temperature over each given bandwidth.

further suppression. Alternatively, we could have placed a single 20 dB attenuator at 4K for the 20 dB of suppression needed from 300K.

The Johnson noise power in the 4K to 300K regime is linear, which is why 20dB of suppression translates to an order of 100 smaller temperature. However, we see in Fig. D.2 for the 10 GHz bandwidth below 1K, that the scaling becomes quadratic. Thus, as we go down to 4mK from 4K we would need 40 dB of suppression.

Appendix E

QUBIT EXCITATION AND PULSE SHAPING

Assumed parameters

Qubit Capacitance - C_q = 67.1fF

Junction Area [μm^2] measured in SEM with 0.95 scale correction factor - $A = 0.2340 * .1869 * 0.95^2$

Crtial current density [A/μ m^2] = J =0.344E-6

Qubit Frequency - $\omega_q(\theta, C_q) = \sqrt{\frac{4\pi JA\left|\cos\left(\frac{\theta}{2}\right)\right|}{\Phi_0 C_q}}$

Qubit anharmonicity - $\alpha_q = -\frac{qe^2}{2C_q\hbar}$

Coupling Capacitance - C_c = 52aF

Cosine Envelope

We now introduce a cosine envelope with some temporal width. Define a parameter b (the pulse width) for experimental convenience:

$$\int_{-b/2}^{b/2} \frac{A_0}{2}\left(1 + \cos\left(\frac{2\pi x}{b}\right)\right) dx = \frac{A_0 b}{2} \tag{E.1}$$

The area under a cosine pulse is equal to half the full width of cosine pulse times the pulse amplitude. Let's define a cosine envelope which has a start at $t = 0$. Note that without DRAG, this envelope is purely real.

Applying DRAG

Apply a DRAG correction envelope [26][71] with parameters α and detuning δf:

$$\tilde{f}(t) = \left[f(t) - \left(\frac{i\alpha}{\alpha - \delta f}\right)\frac{d}{dt}f(t)\right] e^{2\pi i \delta f t} \tag{E.2}$$

Qubit Rotations

The unitary operator on the qubit due to some capacitive drive looks like

$$U = \exp(-i\sigma_x\theta) \tag{E.3}$$

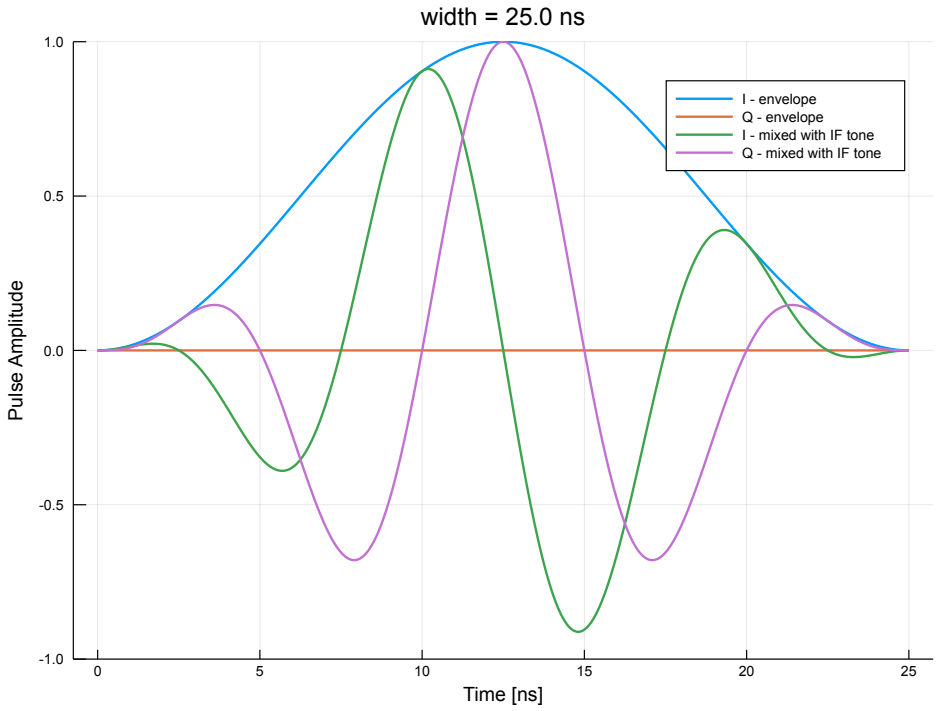

Figure E.1: Cosine pulse envelope with a intermediate frequency (IF) tone.

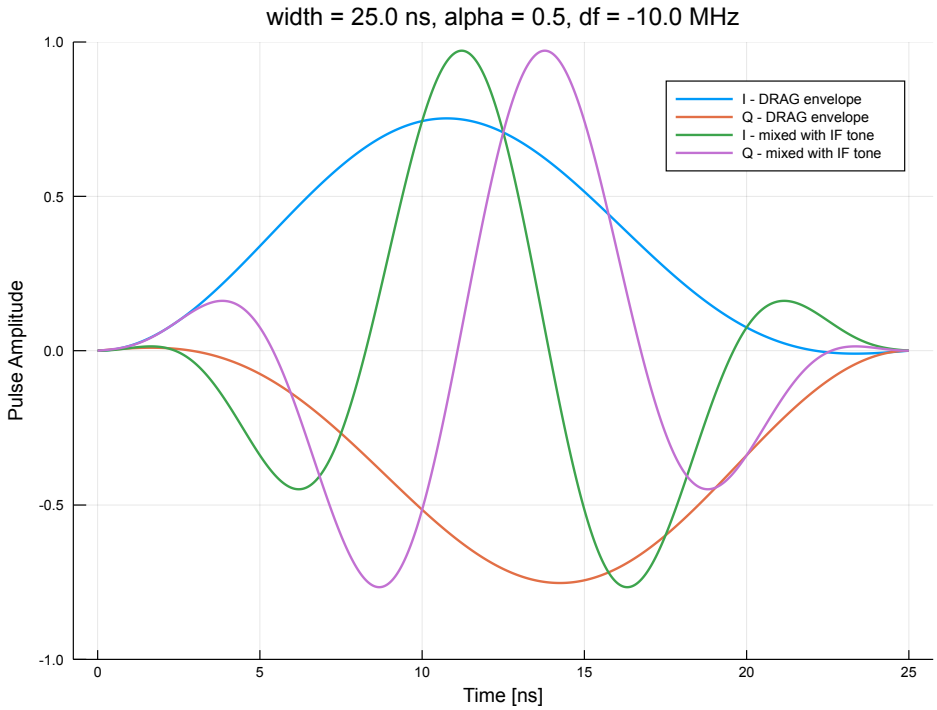

Figure E.2

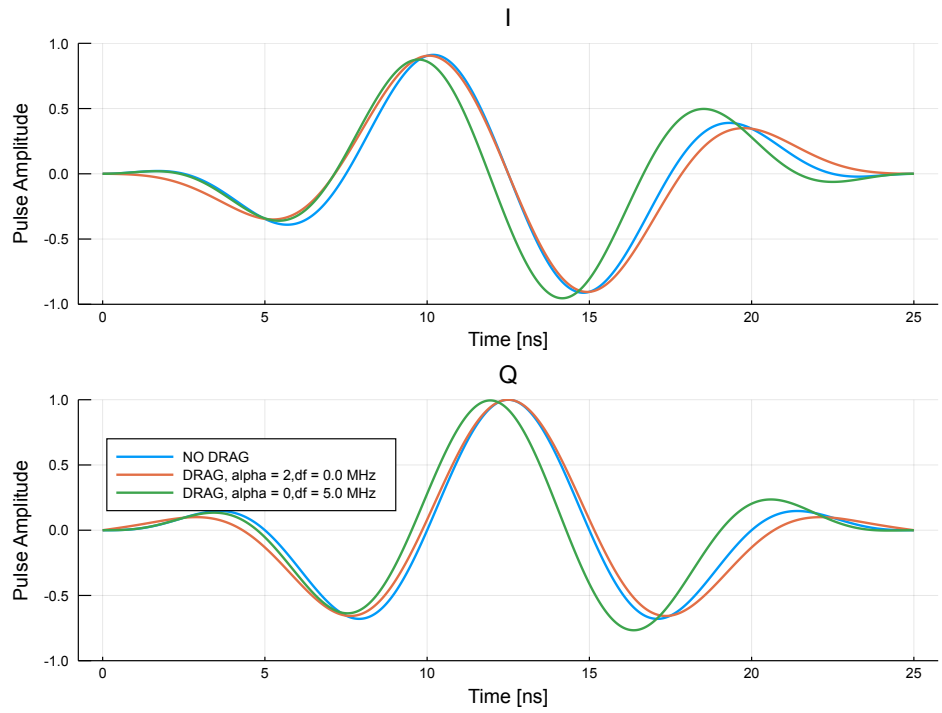

Figure E.3: Modifications to the cosine pulse with slight perturbations to DRAG parameters α and δf.

where θ is the rotation angle which depends on our experimental parameters, such as coupling capacitance and voltage of the drive signal. For convenience, we define a pulse envelope and voltage independent term β [87].

$$\beta = \frac{Q_{zp}}{2\hbar\left(1 + C_q/C_C\right)} \approx \frac{Q_{zp}C_c}{2\hbar C_q} \tag{E.4}$$

in the limit where $C_c \ll C_q$ where $Q_{zp} = \sqrt{\hbar C_q \omega_q/2}$ is the zero point charge fluctuation in the qubit. We see that at an angle of $\theta = \pi/2$, this operator U becomes a $-i\sigma_x$ operator on the qubit. We take the probability $\langle U\rangle^2$ (the square of the expectation value of the operator U) for a 0 to 1 transition given a rotation angle θ, to obtain the excitation dynamics of the qubit as a function of operator rotation angle θ in Figure E.4.

A rotation becomes

$$\theta = \beta V_0 \int e(t)dt \tag{E.5}$$

$$= \frac{\beta V_0 A_0 b}{2} \text{ (cosine envelope with amplitude } A_0 \text{ and width } b) \tag{E.6}$$

with $e(t)$ the pulse envelope and V_0 the voltage amplitude of the pulse at the feedline. To determine the actually voltage at the device drive line, we must know the system

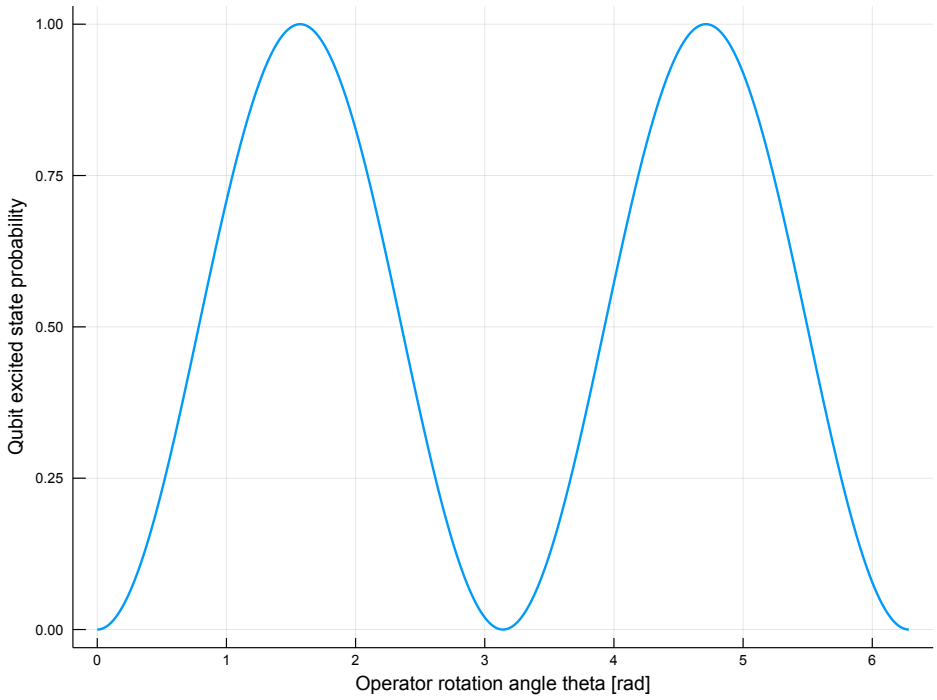

Figure E.4: Qubit excitation probability over different rotation angles θ.

loss from the room temperature electronics at the output of the arbitrary waveform generator (AWG) down to the sample itself. Given the known characteristics of the fridge wiring, IQ mixers losses, and other component losses, an estimate of the attenuation can be generated. We assume 70 dB of fridge wiring loss, mixer losses of typically 5.5 dB with 7.0 dB max, and a voltage gain of 2 (dB gain of 6) with the amplifiers used on the IQ mixing setup, which yields a total effective attenuation of -69.5dB. We can now calculate the expected rotation angle for various pulse amplitudes and widths as shown in Figure E.5 to map out the drive strengths and pulse lengths needed to perform a bit flip on the qubit. Here, the drive strength is a fraction of the full scale output of the AWG ($V_{pp} = 2V_0$), and the drive levels are set by the digital resolution of the AWG (typically 16 bits). We that we can perform a rotation angle θ of $\pi/2$ (which corresponds to a π rotation on the qubit in the Bloch sphere) of around 20 ns, given an AWG output voltage of $V_{pp} = 1.0$V (equal to an amplitude of $V_0 = 0.5$V). From a more practical perspective, we plot the AWG voltage ($V_0 = 1$V) as a function of pulse length in Figure E.6 to satisfy a condition for a π pulse on the qubit, i.e. a $\theta = \pi/2$ rotation.

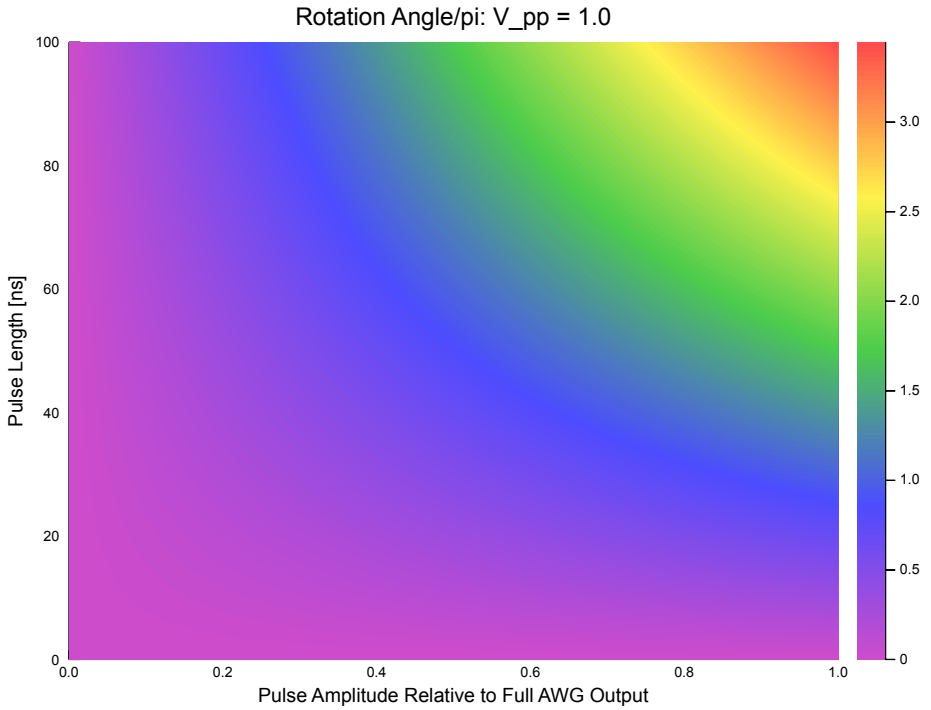

Figure E.5: Rotation angle θ/π for an AWG output voltage of $V_{pp} = 1$V.

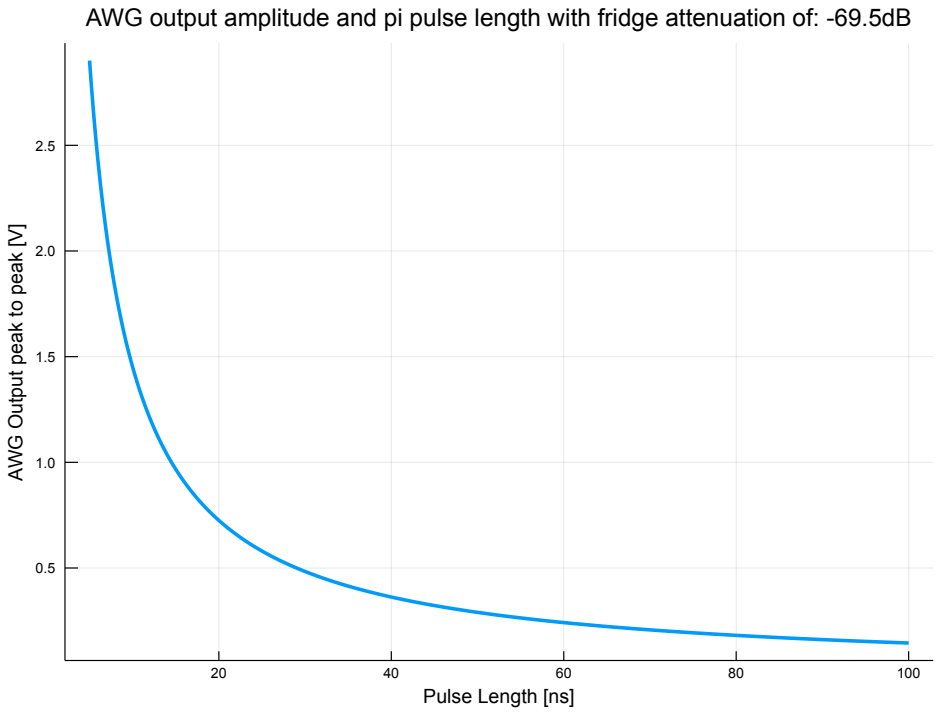

Figure E.6: Translating a pulse length to the AWG output voltage required to perform a π pulse.

Appendix F

ICP-RIE ETCHING PARAMETERS

Table F.1: ICP-RIE optimized etch recipe parameters. *The DC bias cannot be measured reliably with an insulating carrier wafer such as one made of sapphire. **The sapphire wafer also did not have a flat, so the Helium backing formed a perfect seal that resulted zero flow. The Oxford Instruments Plasmalab System 100 is abbreviated as OxP.

Process Parameter	**Etch Recipe**			
	Device Layer	SiO_2	Handle (etch/dep)	Aluminum
C_4F_8 flow (sccm)	84	70	- / 140	-
SF_6 flow (sccm)	30	-	160 / -	-
O_2 flow (sccm)	-	5	-	-
Cl_2 flow (sccm)	-	-	-	18
CH_4 flow (sccm)	-	-	-	4
H_2 flow (sccm)	-	-	-	7
RF power (W)	15.5	150	30 / 10	50
ICP power (W)	600	2200	1750 / 1750	1000
D.C. bias (V)	76	170	N/A*	70
Pressure (mTorr)	15	8	20 / 20	6
He pressure (Torr)	10	10	10	5
He flow (sccm)	20-30	20-30	0**	20-30
Table temp (°C)	15	15	15 / 15	30
Time (sec) or cycles	205	840	200	100
Time/cycle (sec)	-	-	15 / 10	-
Etch rate (nm/min)	45	220	2400	110
Mask	ZEP520A	SPR220-7.0	SPR220-7.0	ZEP520A
Tool	OxP (Silicon)	OxP (DRIE)	OxP (DRIE)	OxP (III-V)
Carrier wafer	Silicon	Silicon	Sapphire	Silicon

Appendix G

FULL STAR FABRICATION PROCESS

The formatted outline of how these fabrication process steps are organized is shown below:

G.0 Process section

a) Process Step

Any notes related to this process step.

G.1 Initial Chip Preparation

a) ACE sonication, IPA sonication, N2 dry

First initial organics cleaning

b) TCE 5min on 80C hotplate, ACE sonication, IPA sonication, N2 dry

TCE is done after photoresist has been stripped. This allows TCE to remove stubborn and hard to remove organics, such as adhesives, grease, or wax.

c) O2 Plasma 5 min

This will burn off any organics that were not removed in the wet cleaning steps. Note that this may slightly roughen the silicon surface and introduce a possibly thicker oxide layer on your silicon, if the oxide has not fully self terminated yet.

d) 10:1 BHF 15 sec

50nm SiOx etched/min. This step is critical and will etch the oxidized silicon surface and terminate the silicon surface with a hydrogen termination. This will act like a passivation layer for about an hour before the surface starts oxidizing again. While passivated, the surface is ideal for good adhesion. Can not avoid this step because you need good resist-to-substrate adhesion when doing liftoff with Nb.

G.2 Alignment Marks

We use niobium (Nb) markers, which are the first pattern of lithography. Niobium is an attractive choice for markers because it is superconducting below 9 Kelvin and it has a high atomic weight, which can be easily seen in electron beam lithography

system. When Nb is electron beam evaporated, it is deposited under very high tensile stress. Therefore, surface preparation is important for good substrate adhesion.

a) Spin ZEP
Pre-bake at 180 C, spin at 3K RPM (~400nm), post-bake at 180 C for 3 min
b) Beam write markers
100μA, 210μC/cm^2, 50nm resolution.
c) O2 Plasma 2 min
At first, it seems strange that this does not make the surface adhesion with Nb any worse. What you really care about is the resist adhesion to substrate, not Nb adhesion to surface to substrate. The main mode of failure is the resist adhesion because the residual stress from evaporating Nb is very high. Although the Nb will adhere well to the resist, the adhesion between resist will be poor. As a result, the evaporated Nb film will buckle up, pulling the resist layer with the Nb away and off the substrate. This will ultimately defeat the point of lift off if the peeling happens in the middle of your evaporation.
d) Evaporate Nb Markers 150nm
e) Lift off in NMP, ACE+ IPA rinse

G.3 Silicon Etch

This step defines the silicon features. The most critical dimensions are the silicon tethers, which are 250nm wide and 220nm thick. a) Spin ZEP
Pre-bake at 180 C, spin at 8K RPM (~220nm), post-bake at 180 C for 3 min. I opted to not do a O2 plasma because any thin atomic layers of ZEP not removed from the previous step will be covered again by ZEP anyway.
b) Beam write Si etch
50μA, 210μC/cm^2, 25nm resolution.
c) Develop
2min30sec in ZED N50, 30 sec rinse in MIBK
d) Etch Si in Oxford ICP-RIE
220nm (standard SOI recipe, DC Bias ~85 V for 3:40) - On the Dielectric etcher in KNI, the Painter JR recipe yields 71 - 73 V with 3:15 to clear. Ultimately, you just want to make sure that your etch give vertical sidewalls and that you overetch tens of nm into the oxide layer.
e) NMP strip, ACE + IPA rinse

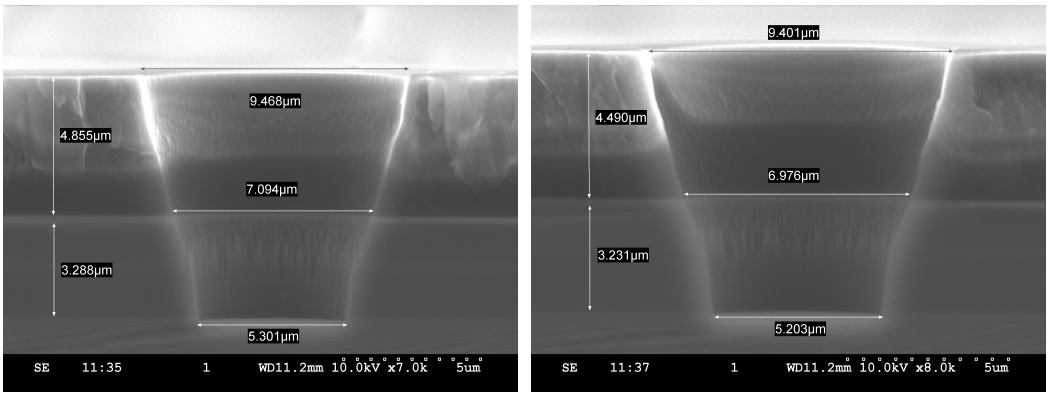

Figure G.1: Via etch.

f) O2 plasma 5 min

Here I do O2 plasma because I am transitioning to a photoresist. I didn't do a HF dip to prevent any undercuts from forming (remember that we have thin tether features now) so be aware that adhesion will not be great.

G.4 Buried Oxide Etch

Photolithography is used in this step because photoresist works better with the silicon oxide etch, which is both physical and long. A set of optical alignment marks are defined in electron beam lithography for cross process alignment.

a) Spin SPR220 - 7.0

Place the scotch tape over the photolith markers, so that you can still see them optically (i.e. photoresist is not covering the markers) when aligning on the photomask. Cold glass slide is a way to introduce a slow ramp in temp. 7 microns on front side (edge bead avoidance with scotch tape) at 4k rpm with 300rpm prespin. Take off scotch tape. Put with cold glass slide on 115 C hot plate for 9 min.

b) O2 plasma 5 min

c) Expose on mask aligner

Suss 1: 15 mW/cm^2 (Ch1) for 40 sec, Suss 2: 10mW/cm^2 (Ch1) for 60 sec. Mount chip to glass carrier with long strips of kapton tape along edges where markers are. Wish I used something better than kaptop tape. The silicone adhesive is pretty nasty and is not easily removed.

d) Let sit overnight for rehydrate resist

This is probably excessive, but somehow it always works out that the last thing I do during the day is mask alignment

e) Post exposure bake

Set hotplate to 115 C place glass wafer on top, place on warm wafer at 90 C, start timer for 8 min when temp hits 113 C. You want to slowly bake the resist, as to not over stress the film, and form cracks. It follows that you want to slowly cool the chip as well. So developing too quickly after this bake is no bueno.

f) Develop in CD MF-26

2 min 15 sec without agitation (or 90 sec to be safe with agitation by hand), rinse in DI water. The developer is basically TMAH in water, so keep in mind material compatibility issues (e.g. TMAH will attack Aluminum). Remember that resist adhesion is not great, so better to keep chip held with tweezers, instead of dropping chip into breaker at the risk of the chip flipping over and rubbing against the bottom. I have seen resist come off due to some sort of rubbing.

g) Optional bake

Convection oven at 90 C for 1 hour (Probably not wanted.) Place chips on glass wafer. There is no reason to do this unless your selectivity is not good enough and you need better etch resistance. I have found this to improve selectivity by a factor of ~2 when deep etching Silicon in SF6/C4F8 based etches. You will of course sacrifice a bit of resolution and the development profile due to the slight softening/reflowing of the resist.

h) Etch in DRIE

First do standard SOI etch, then do SiO2, O2 5 sccm, recipe "Painter - MF SiO2 etch" for 14 min on Si carrier (mount chips with kapton tape to prevent etching of markers) - do not use Al2O3 wafer (causes resist to be dry and hard to remove). The oxide etch is very physical and seems sensitive to the surface prep/conditions. For example it seems better to not etch the VIA pattern during the silicon step. Rather it is better to leave that step for here, where we etch the device layer separately. We then follow up the normal SOI etch with the oxide etch, which gives the best results in terms of etching all the way through and not leaving behind grass.

i) NMP strip, ACE + IPA rinse (with sonication)

j) O2 plasma 5 min

k) 10:1 BHF 10 sec

50nm SiOx etched/min. This will undercut the tethers just so slightly.

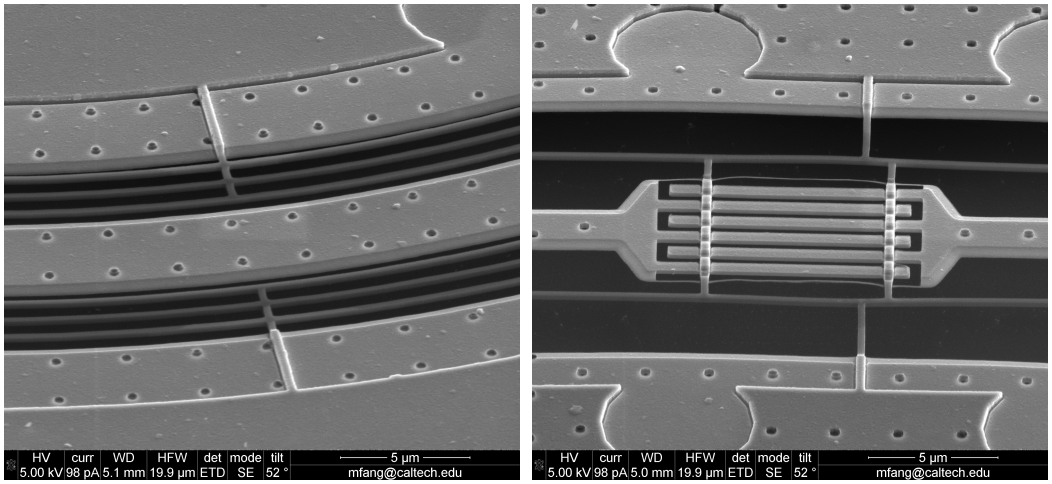

Figure G.2: Two step metal patterning: lift off and etched

G.5 Metal Deposition

Double Metal Pattern Process Only

The definition of the metal pattern is two step process, lift off and local anisotropic etching are combined. The lift off process allows for conformal metal to climb over the tethers, while the anisotropic etch allows smaller features to be defined.

a) Spin PMMA Bilayer

(PMMA EL11, 950A4)(10k spin,6k ramp)/(2.5k spin/2.5k ramp) for lift off. The first step involves evaporating metal with planetary rotation and tilt onto a bi-layer for lift off (this will obviously restrict you to large features)

b) Beam write lift off metal (large features)

Develop in 3:1 IPA:H30 for 90 sec, 10 sec rinse in IPA. Mix IPA:H20 fresh everytime, stir and wait 2 min before development. New mix for each chip

Mixing IPA and H2O is an exothermic process. Being consistent in time before develop will make your development more consistent.

c) O2 plasma 30 sec

d) Global planetary Al evaporation, 200nm, 30 deg, 3rpm

e) NMP strip, ACE + IPA rinse (with sonication)

Lift off for the two step process (first step is lift off, second step is dry etch)

Metal Pattern Process

a) Global planetary Al evaporation, 200nm, 30 deg, 3rpm

Do if not done already during the Double Pattern Process

b) Spin ZEP @ 3K RPM (~400nm)

If doing the two step process, the second step involves doing an anisotropic dry etch of any fine features, such as finger capacitor gaps, release holes, etc.

c) Beam write metal etch

d) Develop in ZED-N50 2min30sec, rinse in MIBK 30 sec

e) Post dev bake, 120 C, 5 min x 2 (cool between)

f) O2 Plasma 1 min

g) Dry etch Al

Used Joshua's Al etch recipe, will need to add an isotropic Cl2 etch at the end to clear Al on sidewalls. 1 min 40 sec ended up being a good time.

h) NMP + solvent clean (good to do if imaging though)

Frontside Protection Process

a) O2 Plasma 5 min (front side up)

b) Spin SF11

Spin on two layers at 4000rpm (with 300rpm edge bead reduction step) on front side (aluminum side), bake at 200 C for 5 min - prevents TMAH attack of aluminum from development and gets etched away by TMAH at 4 nm/s.

c) O2 Plasma 5 min

G.6 Backside Silicon Etch

a) Spin SPR220-7.0

Tape chip down to glass slide (normal scotch tape), front side down. Spin at 2k rpm (with 300 rpm pre-spin) for 60 sec - should yield about 9 microns. Peel off tape to remove edge bead.

b) Bake for 11 min at 115C starting on cold slide

c) Mask aligner

Expose with Ch1 (15mW/cm^2) for 50 seconds, mount chip to glass carrier with long strips of kapton tape along edges

d) Wait overnight to rehydrate

e) Post exposure bake

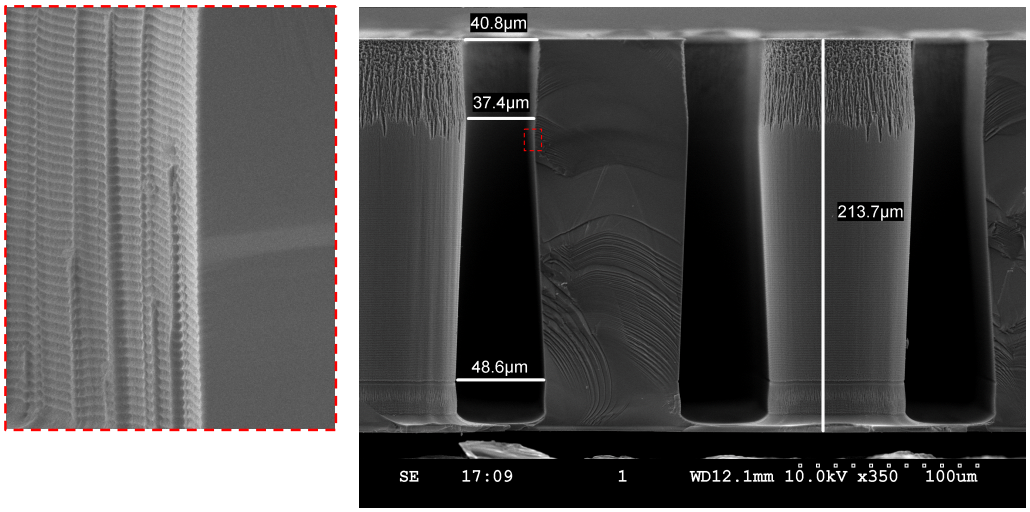

Figure G.3: Through substrate channels fabricated with a deep reactive ion etch.

Set hotplate to 115 C place glass wafer on top, place on warm wafer at 90 C, start timer for 10 min when temp hits 113 C.

f)Develop

CD MF-26 for 2 min with agitation by hand, rinse in DI water

g) Post-development Bake

Convection oven at 90 C for 1 hour on glass wafer

h) DRIE Etch

Mount chip to Al2O3 wafer with kapton tape and Santovac 5 along outer edge of chip. Etch with Painter Si Bosch 2017. Dismount by slowly sliding chip off in lateral direction. For STAR gen 2, need about 200 cycles to clear to oxide. Add in a few 30 second isotropic SF6 steps to better planarize without footing.

i) Solvent clean

Let sit in acetone (removes Santovac and most of photoresist) → IPA → hot NMP (removes SF11, 12.5nm/s at 40 C and also remaining photoresist)→ acetone → IPA.

G.7 Backside Metal Deposition

a) O2 Plasma 15 min (Bottom side up)

Do not use aluminum foil under your chip in this tool. Pieces will ricochet around the chamber when venting.

b) Backside metal evaporation

Mount chips in Plassys with aluminum foil between front side and holder (might

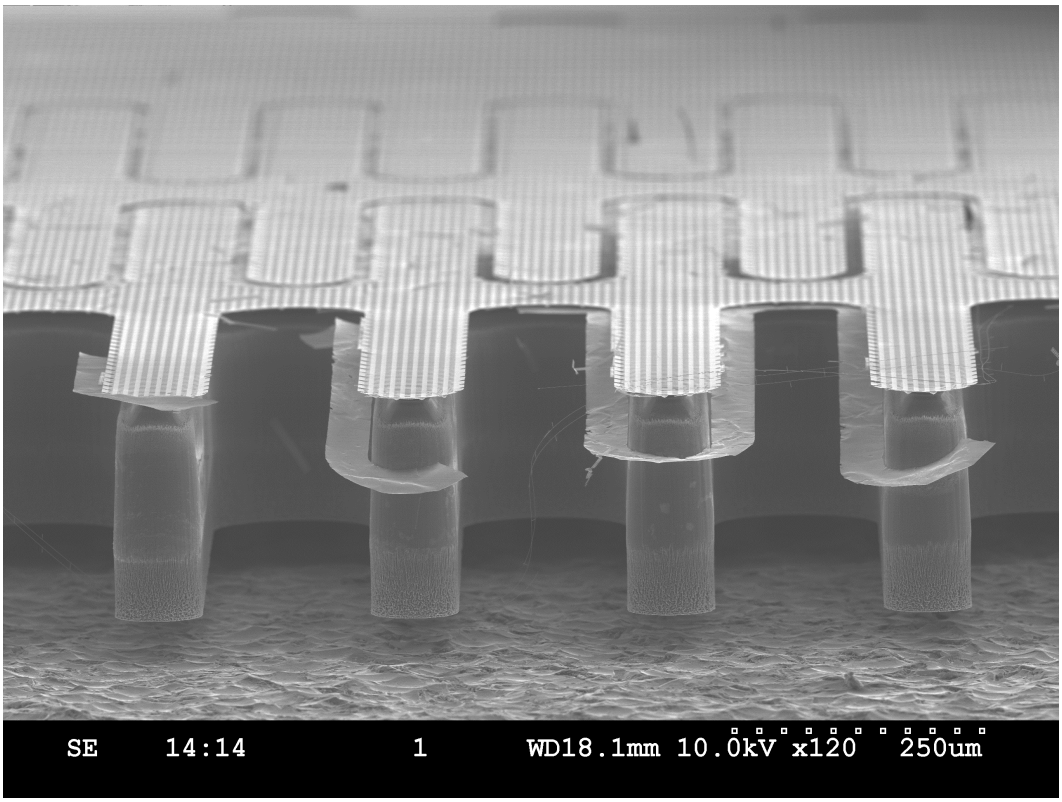

Figure G.4: Backside metalization.

not be necessary). Argon ion mill with top down evaporation (~200nm). Argon ion mill currently melts and reflows photoresist slightly. Deposited 100nm at 0 deg tilt and 100nm at 10 degrees tilt.

c) O2 Plasma 15 min (topside)

d) VHF release

Run recipe 2 for 9 cycles

G.8 Completed device

The anatomy of a completed STAR structure is presented in Figure G.5.

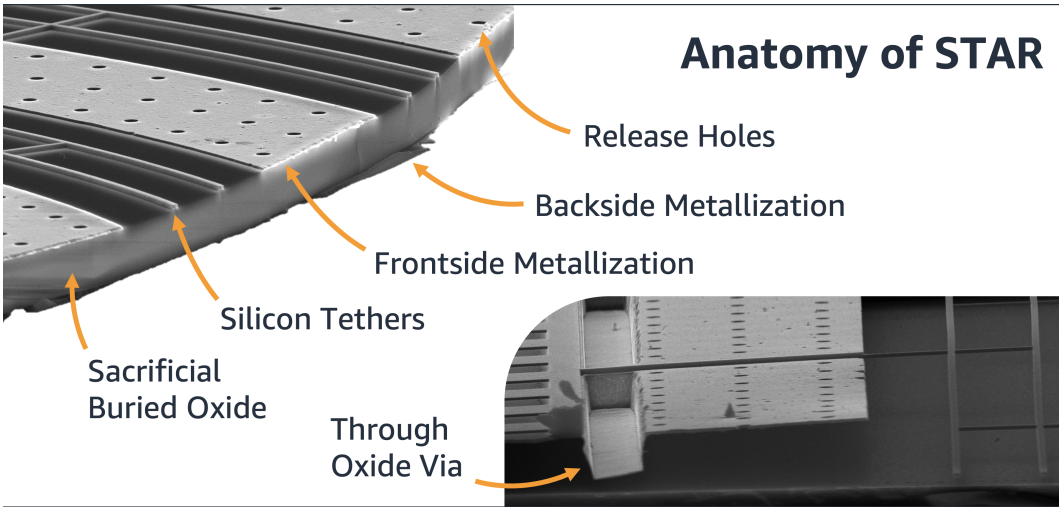

Figure G.5: Anatomy of the STAR structure.