Chapter 5

FABRICATION OF ON-CHIP PHOTONIC DEVICES FOR COUPLING TO DEFECTS IN SIC

In this chapter I describe the fabrication procedure for on-chip photonic devices for coupling to luminescent defects in silicon carbide. The most successful effort was hybrid devices based on crystalline silicon (c-Si) placed on top of 4H-SiC.

5.1 Qubits generation in 4H-SiC

Ion implantation and divacancies

The concept of the hybrid devices that we aim to fabricate is that the photonic mode is confined in a silicon device and is evanescently coupled to luminescent centers located close to the surface of the substrate. In this case we aim to couple to divacancies. Divacancies are common and intrinsic in 4H-SiC and the ZPL of ensemble divacancies can be readily measured in our high-purity semi-insulating 4H-SiC wafers purchased from CREE Inc[32, 34]. Divacancies can also be created using Si or C implantation[38, 78] or electron irradiation[45]. Using implantation is advantageous in our case because the divacancies are created close to the surface. Since we also wanted to generate other color centers based on other elements, we also created divacancies by implantation of ions from the elements Cr and Mo.

Before implantation, we estimated the depth distributions of the implanted ions using computer simulations for Stopping and Range of Ions in Matter (SRIM)[79]. Having divacancies closer to the surface is beneficial because it leads to stronger coupling to the resonator mode. However, generally the proximity to surfaces leads to degradation in the optical and spin properties of the divacancies. Since we were not sure about these tradeoffs, we had some of our samples implanted with 10 and 150 keV implantation energy. For example for Cr implantation the distribution of implanted ions peaked between 9nm and 90nm. We assumed that divacancies will be created similarly to this distribution. The Cr ion density at 10nm depth with dose 10^{13} is estimated to be $10^{19}/\text{cm}^3$. The results of our implantation is shown in the following table, which also indicates if divacancies were observed.

Implanted ion	Implantation energy (keV)	dose (cm^2)	Photoluminescense detected? (1000-1500nm)
N	150	10^9,10^{11},10^{13}	Divacancies
Ni	150	10^9,10^{11},10^{13}	Divacancies
Cr	10, 150	10^9,10^{11},10^{13}	Divacancies, Cr ions
Mo	200	5×10^9, 5×10^{10}	Divacancies, Mo ions

Table 5.1: List of samples with different ion implantation and photoluminescense

Annealing

An annealing process is required such that the generated vacancies migrate and form divacancies. We annealed implanted 4H-SiC in Argon at 900 °C. We chose this temperature because divacancy formation decreases and trivacancies formations starts to dominate over 1400 °C [80]. We tried different annealing time, 30, 120, 240 mins and observed how the ZPL of specific divacancies change. The annealing process includes additional ramp up/down time of 30 mins each, which is kept the same for different annealing time. We note that it might be better to decrease the ramp time to increase PL of divacancies, as suggested by Gällström et al. [81]. The following **??** shows the ZPL of divacancies under different annealing temperature condition.

5.2 4H-SiC transfer

When starting this project, we first attempted to make photonic devices directly in the host material, SiC. Heteroepitaxial growth is available for 3C-SiC but not for 4H, or 6H-SiC. The alternative method is transferring a thin membrane of 4H-SiC onto a different material and fabricating the device directly into the SiC membrane. We transferred a thin layer of ion-sliced 4H-SiC on silica following the procedure similar to the one described in Lee et al. [82].

The transferred membranes were inspected under SEM. As it can be seen in figure 5.1, generally they have large roughness >10nm on the surface. We considered this surface too rough to have good photonic devices fabricated on and changed to hybrid approach that will be discussed in next 2 sections. Also, we did photoluminescence measurements on this material and we discovered that it was full of defects, including divacancies with very broad linewidth (~1 nm for PL1), which would make it difficult to develop devices that work at single photon level.

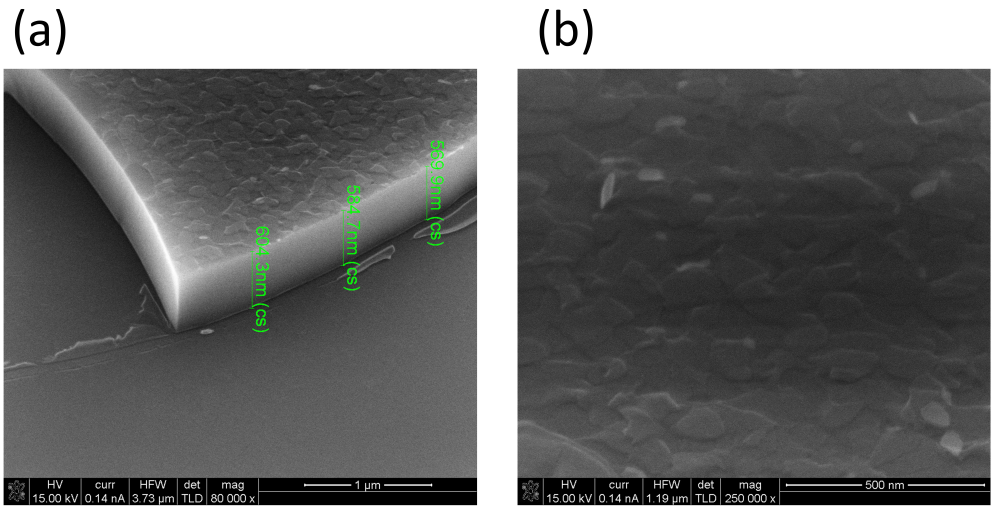

Figure 5.1: SEM image of 4H-SiC membrane surface transferred by smart cut method.

5.3 a-Si:H Deposition

The next technique that we tried was by depositing amorphous silicon onto SiC, with the goal of fabricating the devices directly into the silicon for evanescent coupling to defects in SiC. We deposited hydrogenated amorphous Si (a-Si:H) on 4H-SiC with plasma enhanced chemical vapor deposition (PECVD). We used parameters in table 5.2.The deposition rate is approximately 26 nm/min. The ring resonator devices we fabricated using a-Si only gave best Q ~ 5000. SEM inspection revealed there is noticeable roughness on the surface of a-Si as shown in 5.2. The surface shows grains of a-Si [83, 84]. We tried depositing alumina Al_2O_3 for 20 nm to reduce this effect as there might be substrate dependence on roughness [85, 86]. A 20nm thin layer of alumina between SiC and a-Si doesn't disturb the confined light profile according to simulation. Measurements with higher resolution of roughness were performed under atomic force microscope (AFM). The measured surface roughness was slightly improved compared between a-Si deposition with and without alumina as shown in figure 5.3 (a)(b). The roughness comparison AFM images of a-Si, c-Si and the original substrate are shown in figure 5.3. However, this roughness was still considered too high so we decided to fabricate devices in a crystalline silicon membrane transferred on top of SiC.

Deposition parameters	Values
RF forward power	10 W
5% SiH_4 in Ar flow rate	40.0 sccm
Chamber pressure	801 mTorr
Wafer temperature	200 °C
Deposition rate	26 nm/min

Table 5.2: a-Si recipe

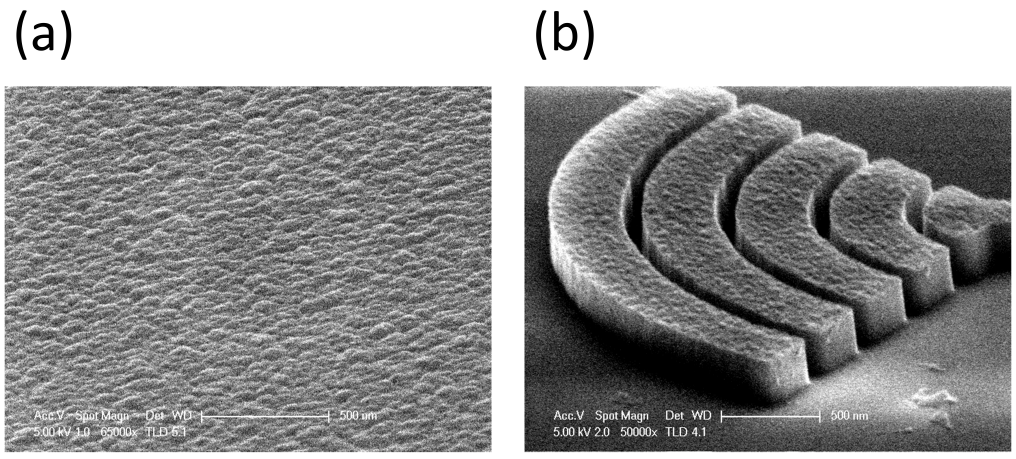

Figure 5.2: SEM images of a-Si roughness. (a) a-Si deposited before any patterning procedure (b) A grating coupler after etching and cleaning. process

5.4 c-Si Membrane Transfer

The fabrication process of the hybrid devices starts with transferring c-Si membrane from silicon on insulator (SOI) chips by Soitec. The SOI wafer has a Si device layer thickness of 500nm, close enough to the desired 360 nm height for the ring resonators. Si is B doped p-type and the buried oxide thickness is 3 um. The c-Si transfer procedure is summarized in table 5.3. The details of each step is described in following sections. This c-Si transfer procedure was inspired from work by Li et al. [87].

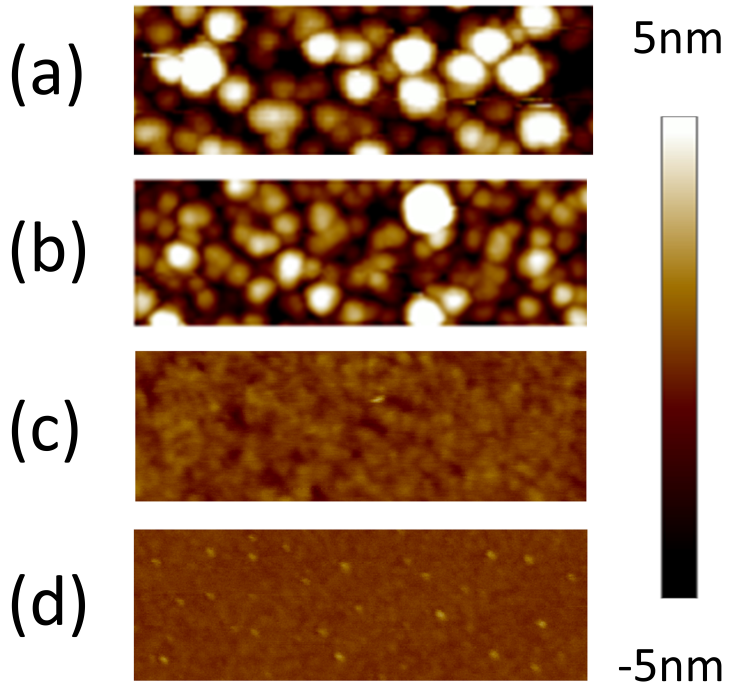

Figure 5.3: AFM images for comparison of roughness. (a) Deposited a-Si. (b) Deposited 20nm alumina then a-Si. (c) Transferred c-Si all on top of 4H-SiC. (d) AFM on the 4H-SiC substrate.

Cleaning

Purchased SOI wafers were dipped in Nanostrip(H_2SO_4, H_2O_2) for one hour. Then they were cleaned in typical solvent rinsing (acetone, methanol, IPA).

Thinning c-Si to desired layer depth

Because it is hard to find SOI chips with the exact Si thickness of what we desire to use for the devices, this step is required to adjust the thickness of the membranes. The oxidization rate can be calculated and fitted based on the theory described by McGuire [88]. The rate depends on different factors such as Si surface charges, dopant concentration or oxygen distribution, pressure, etc. We took a few data points of (oxidation time, oxide thickness) and generated a MATLAB code that fits these to the theoretical curve to estimate the correct oxidation time, which is included in **??**. This calculates for both wet or dry oxidation.

Based on the calculated oxidation time, we performed wet oxidation of 32 mins at 1000 °C. Before and after the oxidation process, there is 1.5 hrs of ramp up/down time in nitrogen environment from/to 700°C. After the oxidation process, we

Step	Description
Cleaning	SOI chips are cleaned with Nanostrip.
Thinning the Si layer	Oxidation and HF wet etching are performed.
Dicing Si membranes	500 μm×500 μm squares are patterned.
Releasing membranes	HF wet etching of BOX layer are performed.
Cleaning 4H-SiC substrate	The surface is changed to hydrophilic state.
Picking up membranes	Quick pick-up with the substrate was performed.
Slow natural drying	Membranes are attached without air or water underneath.
Check membranes quality	Optical microscope and SEM examination are performed.

Table 5.3: c-Si transfer procedure

removed the generated oxide by wet etching with buffered HF. The final thickness of the Si device layer is fitted and calculated in a spectral reflectance analyzer by Filmetric with >95% goodness of fit and is <±10 nm from the desired thickness.

Dicing Si membranes

This step is required to make membranes in small size so that it takes a short time to release the membranes and also increases the success rate of attachment of the membrane to the SiC substrate. Initially we hand cleaved an oxidized SOI chip into 3 mm square small pieces and tried to release the membranes in 52% HF. After 24 hours some of them were still not released and the Si membranes show gradation of color suggesting etching and damage by HF. Also, transferring released membranes in large size easily induce bending and cracking of membranes, which prevents good attachment to the substrate. When the attached membrane will be cleaned or spin coated later, one small opening between the substrate can allow liquid to flow in and the membrane can be flushed away. The same problem occurred when we tried transferring a large membrane with holes spaced regularly. Due to these reasons, we tried membranes with a smaller size of 500 μm × 500 μm and this worked well with >50% yield.

We used a positive resist AZ 5214E for patterning squares on SOI chips. We exposed

spin coated chips with a photomask in a mask aligner photo-lithography system. The mask design is shown in 5.4 (a). The details of the patterning procedure is shown in 5.4. The etch will remove silicon from the exposed part of SOI chips and create separated Si membranes. We used an etching recipe described in table . A patterned SOI chip is shown in 5.4 (b) under optical microscope.

Step	Description
Step	Put SOI chips in the container for 3 mins.
Spin coating	1500 rpm/ 60 s (> 2 μm).
Soft baking	110 °C/ 45 s.
Exposure	5 s (75 mJ in total with 15 mJ /s).
Development	70 s in MF-319 developer.
Cleaning	Solvent cleaning with sonication for 5 mins.
ICP/RIE etching	pseudo-bosch for 8 mins.
Resist removal	Dip in acetone for 3 mins.

Table 5.4: SOI chip square patterning procedure

Releasing the membranes

This step releases Si membranes by detaching the Si device layer from its handle layer. We put small pieces of patterned SOI chips in 52 % HF filled in a small polypropelene jar Si side facing up. Generally it takes 15-30 mins to release all the membranes. We can identify this by the color change of the membranes due to removal of the BOX layer. We prepared large containers filled with water for rinsing membranes. Then we take the chip out slowly without tilting it to prevent membranes from floating away. We put it in water angled to make water go underneath the membrane and flush them away from the handle layer. The membranes are floating on the surface of water. We scoop a single membrane using a plastic spoon and transfer to different containers filled with water several times for cleaning the back side that will be attached to the substrate as shown in figure 5.5. At the end, we transferred the cleaned membrane to a large container filled with clean water where

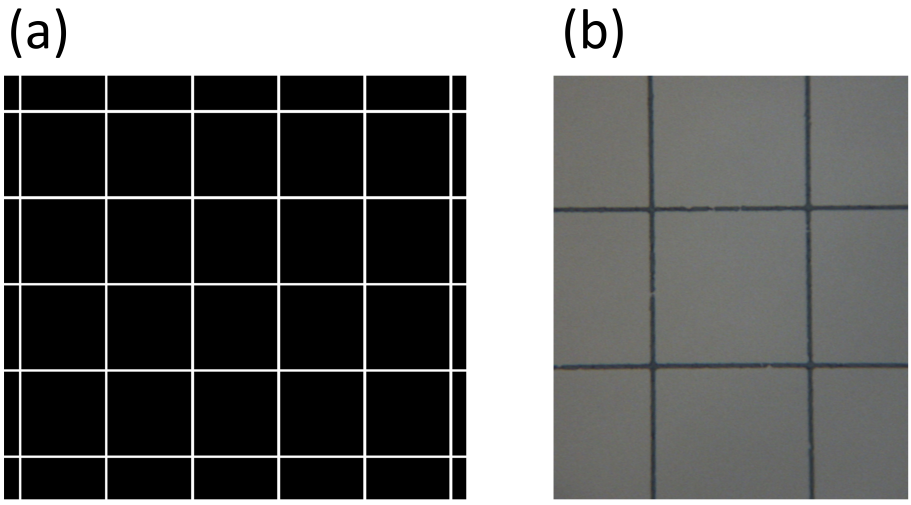

Figure 5.4: (a)Design of the photomask (b)Etched SOI chip after photolithography (light gray: Si, dark gray:SiO_2)

we will be picking it from. At this stage, any membrane that looks bent or folded is discarded. Bending or folding of a membrane often allows water to exist at the interface of the membrane/substrate, which is concluded with >30 trials.

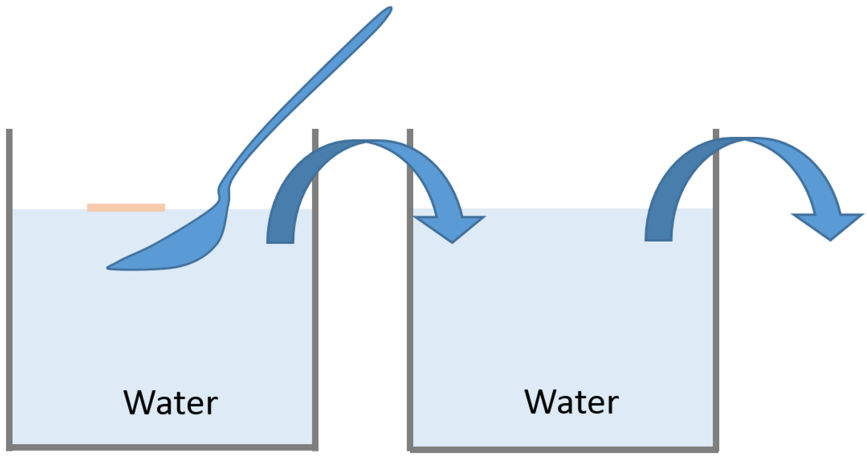

Figure 5.5: Cleaning by transferring a floating membrane to clean water

Cleaning the 4H-SiC substrate

Right before the pick-up process, oxygen plasma cleaning was performed to the 4H-SiC substrate. This step is required to make the substrate hydrophilic such that the bending angle of a picked-up membrane while drying won't be too large. Also, it makes the substrate clean such that water underneath the substrate is easier to move away when the membrane is pushed and attached by Van der Waals force, preventing for water left under the membrane. This step was essential for achieving a high yield of usable membrane area.

Picking up membranes and drying

This step involves transferring floating membranes to the substrate and natural attachment of membranes using Van der Waals force. We hold a cleaned substrate underneath a cleaned floating membrane and quickly pull it upward and toward the membrane out of water. This requires some speed to ensure the membranes stay on the substrate before they flow away. After picking-up the membranes, the substrate is placed in a place without disturbance and the membrane dries slowly. Rapid drying using a hot plate didn't gain good results with many bubbles underneath a membrane. If the substrate is smooth and the membrane is flat, Van der Waals force will push water away and shouldn't leave any water underneath the membrane that can be seen by eye (figure 5.6). After the substrate dried fully we put it on a hot plate with temperature > 150 °C and inspect if any water is left. The following figures 5.7, 5.8 show examples of successful and failed attempts of membrane transfer. After this step, if the membrane has more than 50 % area left without any water or other defects, we will use it in next electron beam writing step. This entire c-Si transfer procedure overall gives ~50 % yield of such usable membranes. Because this transferring method requires physical dexterity and we don't have control over where to put the membrane on the substrate, we wanted to find more reliable methods of fabricating hybrid devices. For this, we attempted to transfer GaAs photonic crystal devices using a nanomanipulator implemented in FIB/SEM system, which is described in A.3.

5.5 c-Si on SiC device patterning and fabrication

Electron beam lithography

All the device patterning was performed under Raith EBPG 5000+ or 5200 system operated at electron energy of 100 keV. ZEP520A positive tone resist is used. Also, our SiC substrate is not conductive so we spin coated conductive polymers,

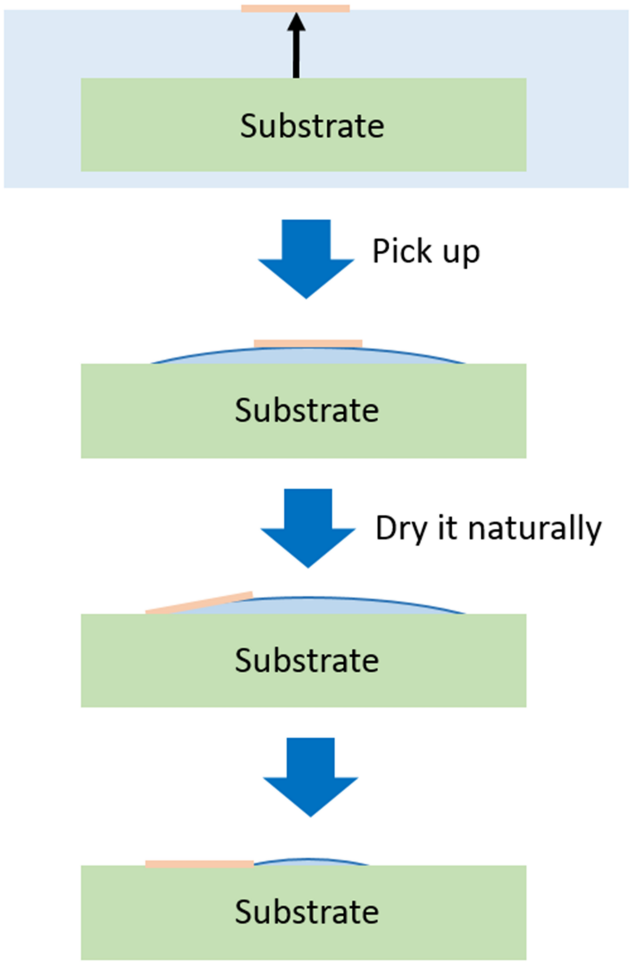

Figure 5.6: Picking up the membrane, drying and attachment on the substrate.

AQUASAVE to prevent electron beam trajectory distortion due to built up charges. The spin coating and development parameters are shown in table 5.5. Ring resonators are patterned with 300 pA, approximately 2 nm beam spot size. The electron scattering induces undesired exposure to nearby exposed locations. Such proximity effect can be corrected by knowing how much electron energy is exposed to neighbor resist by a single pixel exposure. The point spread function distortion due to proximity effect is simulated by Monte Carlo simulation, PENELOPE [89]. We simulated the proximity effect with settings of 10M electrons for the sample layers from the substrate up to ZEP resist.

ICP/RIE etching

A resist reflow technique is used to improve the sidewall roughness caused by resist roughness in the process of development[90]. By heating the resist at right

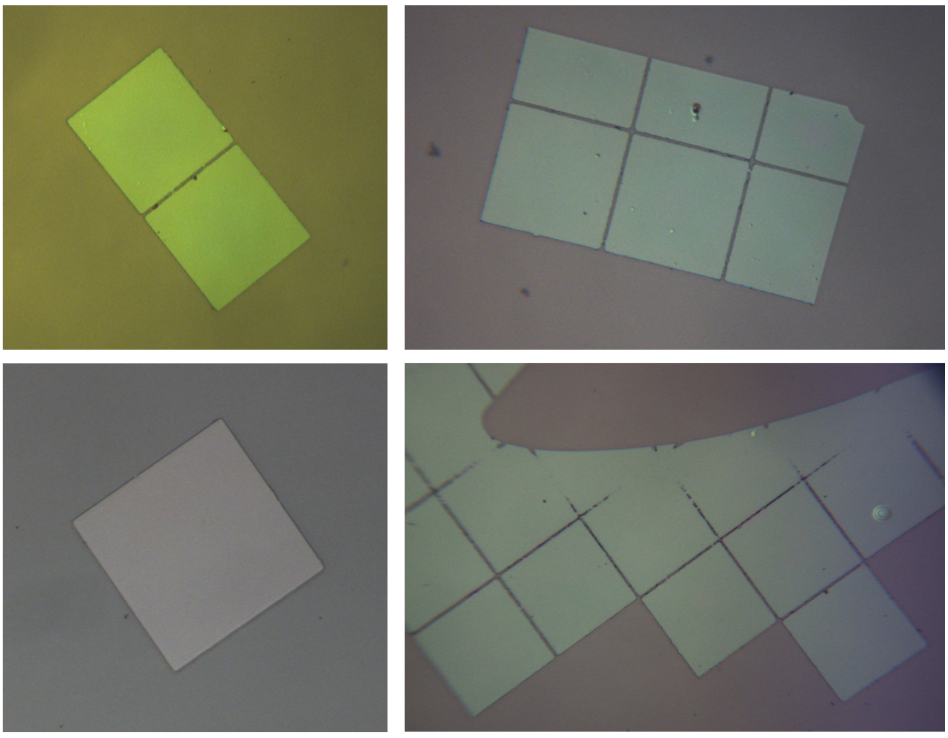

Figure 5.7: Successful membrane transfer. Most membranes are single but some of them are connected.

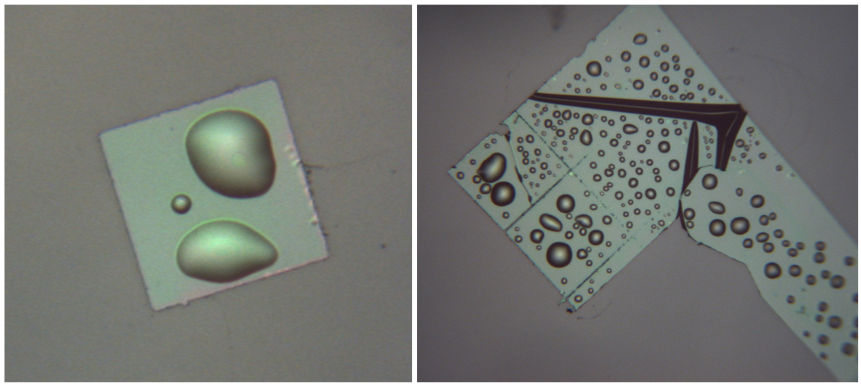

Figure 5.8: Failed membrane transfer. Water scattered underneath the membrane. Heating on a hot plate caused water to evaporate and made bulges on membranes. Wrinkles in membranes allow water to enter and flush of the entire membrane.

Steps	Parameters
Resist spin coating	5000 rpm / 60 s
Baking	180 °C / 3 mins.
AquaSAVE spin coating	1500 rpm / 60 s
Baking	70 °C / 5 mins.
Development	Dip in ZED (slowly stirred) / 3 mins
	then rinse with MIBK / 30s and with water.
Resist reflow	145 °C / 10 mins

Table 5.5: E bean writing resist related procedure

temperature it slowly melts and roughness in the resist is reduced. We put the sample in an oven at 145 °C for 10 mins, which is empirically determined by monitoring the resulted sidewall angle under SEM. As described in a later section for our devices that have quality factor ~ 20000, the resist reflow did not result in a huge improvement in the quality factor (< 10%).

After the reflow process, we etched the sample in SF_6/C_4F_8 plasma for ~ 6 mins with 60 nm /min etching rate. Santovac oil is applied at the back of the sample for fixing the sample and for thermal conduction, which can be easily removed with IPA or acetone. The Si pseudo-bosch recipe we used for etching a-Si and c-Si ring resonators is shown in following table. 5.6.

ZEP resist removal

After etching, we removed the ZEP by dipping the sample in N-Methyl-2-pyrrolidone (NMP) based solvent Remover PG for >12 hrs at 80°C, then we did oxygen plasma treatment for 10 mins and acetone/IPA flush at the end. Some byproducts of oxygen plasma reacting with ZEP are not volatile and there will be residue left as shown in figure 5.9 without solvent cleaning. Dipping in nanostrip after these steps should clean the samples more thoroughly but in my work, all devices were cleaned only with PG remover, oxygen plasma and solvent.

Etching parameters	Values
RF forward power	23 W
ICP forward power	1200 W
DC bias voltage	70 - 90 V
SF_6 flow rate	15.0 sccm
C_4F_8 flow rate	40.0 sccm
Chamber pressure	11.0 mTorr
Wafer temperature	15 °C
Helium backing pressure	4.0 Torr
Etching rate	60 nm/min

Table 5.6: Si pseudo-bosch etching recipe

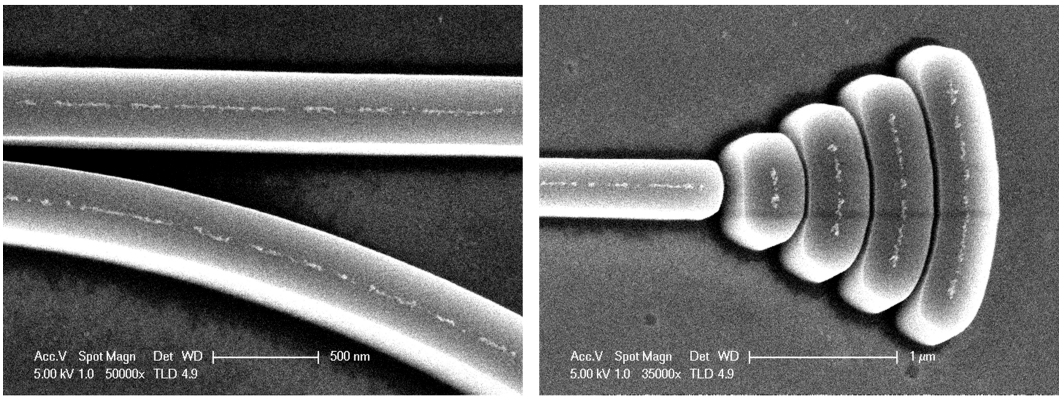

Figure 5.9: Residue of ZEP cleaned with O_2 plasma

Final fabricated c-Si on SiC devices

Figure 5.10 shows a fabricated c-Si on 4H-SiC ring resonator device. Devices written on clean membrane surface without visible bubbles or change in color rarely

had the problem of detaching from the substrate after all the fabrication and cleaning process.

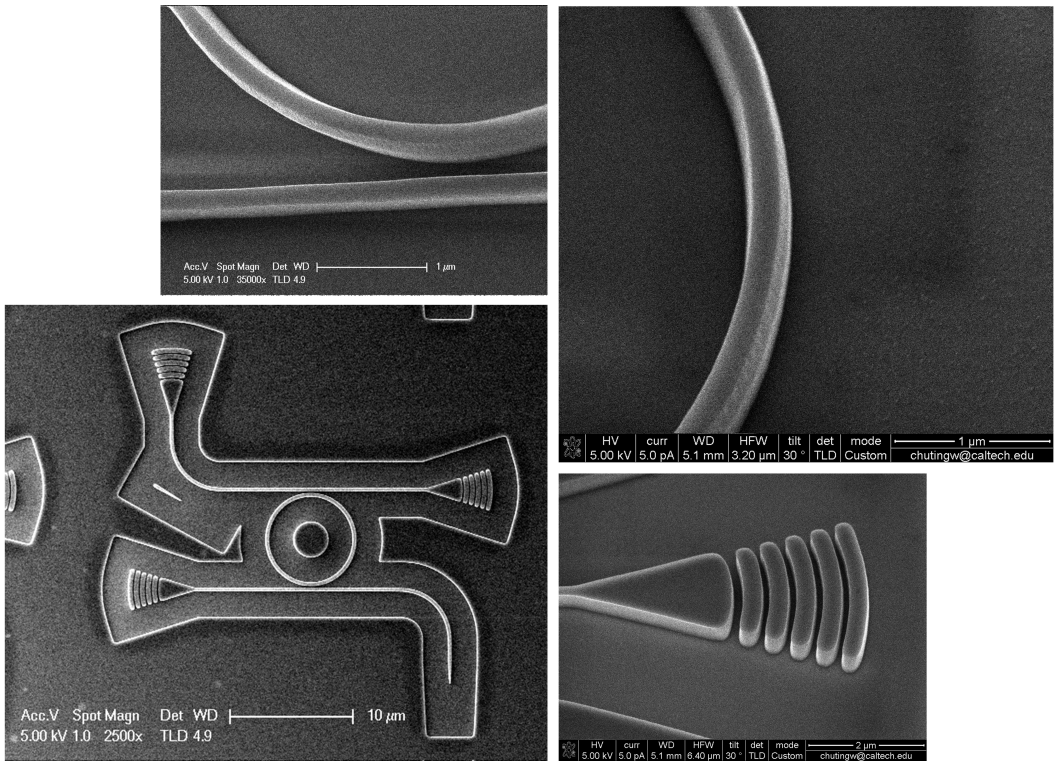

Figure 5.10: SEM image of a c-Si on 4H-SiC final ring resonator device