THE USE OF JUNCTION TRANSISTORS
IN SWITCHING CIRCUITS

Thesis by
Alfred Dale Scarbrough

In Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy

California Institute of Technology
Pasadena, California

1955
Acknowledgments: I wish to express appreciation to the members of my thesis committee for helpful assistance and encouragement during the preparation of this report.

Thanks also are due to the Hughes Aircraft Company for generously providing the transistors used in the experimental work described herein.

To my wife, Ruth, special thanks are due for patiently bearing the trials of a graduate student's wife.
Abstract: The theory of small signal linear junction transistor amplifiers is extended to develop design techniques which can be applied to the non-linear problems of switching circuit design. Many of these techniques differ materially from the corresponding techniques of vacuum tube amplifier design.

The linear theory is oriented toward the study of moderate-gain wide-band amplifiers driving non-inductive loads and being driven from non-inductive sources since switching circuit amplifiers commonly fall into this category, but many of the concepts have application to other amplifiers as well.

As an outgrowth of the linear theory, the transistor parameters which are important in flip-flop operation are discussed, and a new way to measure these parameters is described.

The general theory of flip-flop design is discussed in some detail, and design data is presented for the most useful of the basic flip-flop circuits. Flip-flops were designed by the method presented here and their measured performance compared with the predicted performance. The generally good agreement between theory and experiment is taken as verification of the usefulness of both the design data and the basic concepts used in the derivation of the design data.

It is concluded from this study that junction transistors are practical switching circuit elements, and it is confidently predicted that they will eventually see wide use.
# Table of Contents

<table>
<thead>
<tr>
<th>PART</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td>INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>II.</td>
<td>THE JUNCTION TRANSISTOR AS AN AMPLIFIER</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>Preliminary Ideas</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>The Grounded Base Connection</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>The Grounded Emitter Connection</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>The Grounded Collector Connection</td>
<td>22</td>
</tr>
<tr>
<td></td>
<td>Large Signal Junction Transistor Amplifiers</td>
<td>27</td>
</tr>
<tr>
<td>III.</td>
<td>PULSE MEASUREMENT TECHNIQUES FOR JUNCTION TRANSISTOR PARAMETERS</td>
<td>33</td>
</tr>
<tr>
<td></td>
<td>The Measurement of $C_c$</td>
<td>33</td>
</tr>
<tr>
<td></td>
<td>The Measurement of $\omega_0$</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>The Measurement of $a_o/(1-a_o)$ and $\omega_0(1-a_o)$</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>Direct Measurement of the Grounded Emitter Current Gain Bandwidth Product</td>
<td>38</td>
</tr>
<tr>
<td>IV.</td>
<td>FLIP-FLOP CIRCUITS</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td>Definitions</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td>Restrictions on the Amplifier</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td>Possible Flip-Flop Circuit Configurations</td>
<td>46</td>
</tr>
<tr>
<td>V.</td>
<td>STATIC CONSIDERATIONS IN THE DESIGN OF SYMMETRIC JUNCTION TRANSISTOR FLIP-FLOPS</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>Static Design Objectives</td>
<td>48</td>
</tr>
<tr>
<td></td>
<td>The Basic Flip-Flop Circuit</td>
<td>48</td>
</tr>
<tr>
<td></td>
<td>The Static Flip-Flop Circuit</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>The Selection of $E_n-E_p$</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>The Selection of the Maximum Collector Current</td>
<td>51</td>
</tr>
<tr>
<td></td>
<td>The Selection of $R_4$ and $E_p-E_3$</td>
<td>53</td>
</tr>
</tbody>
</table>
Design Tolerances

The Selection of $R_2$, $R_3$, $E_2$, $I_{op}(\text{min})$, and $a_0(\text{min})$

The Available Output Current and the Selection of $R_1$ and $E_1$

Sample Design of a Symmetric Junction Transistor Flip-Flop

VI. TRANSIENT CONSIDERATIONS IN THE DESIGN OF SYMMETRIC JUNCTION TRANSISTOR FLIP-FLOPS

Transient Analysis Objectives

Notation

Calculation of the Rise Time

Region 1
Region 2
Region 3

The Influence of Circuit Parameters on the Rise Time

Calculation of the Fall Time

Region A
Region B
Region C

The Influence of Circuit Parameters on the Fall Time

Experimental Verification of the Transient Analysis and the Selection of $C_1$

Triggering the Flip-Flop

The Complete Design of the Flip-Flop Circuit

VII. THE USE OF JUNCTION TRANSISTOR FLIP-FLOPS IN DIGITAL COMPUTING CIRCUITS

Logical Description of the Flip-Flop

Diode Gating Networks
A Transistor Figure-of-Merit in Flip-Flop Circuits 112
Increasing the Usefulness of the Junction Transistor Flip-Flop 113

VIII. APPENDIX 118
IX. LIST OF REFERENCES 123
X. FIGURES 124
I INTRODUCTION

The discovery of the transistor in 1948 by Bardeen and Brattain (Ref.1) was an event of singular importance to the electronic world, because it pointed the way to a number of solid state amplifying devices which could compete in many fields with the vacuum tube while offering the distinct advantages of greater ruggedness, smaller size, more efficient operation, and longer life.

Early transistors were a disappointment to many users, partly because manufacturing difficulties had prevented the production of stable, long-lived, devices; and partly because the use of transistors requires a distinctly different approach to circuit design than the use of vacuum tubes. In the years since the introduction of the transistor, improvements in manufacturing techniques have led to the production of devices which have a high order of stability and give promise of realizing the long life expectancy originally predicted. Also, with growing experience in the use of transistors, many of the problems arising from the application of transistors to active circuit design have been solved. The result is that the use of transistors is widespread today and is growing rapidly.

One of the important reasons for this growth in transistor usage was the introduction of the junction transistor, invented by Shockley in 1949 (Ref.2). The junction transistor does not have the characteristic instability which complicates linear circuit design using point contact transistors. It further appears that the junction transistor can be made more easily and cheaply than the point contact
transistor.

For these reasons, the trend in transistor circuit design has been toward the use of junction transistors and away from point contact transistors. However, it seems certain that each will continue to be best for certain uses.

In one field of application, electronic digital computers, the point contact transistor has been used much more extensively than the junction transistor. The reason for this is two-fold. It seemed that the inherent instability of the point contact transistor could be used to advantage in designing simple bi-stable devices and pulse generating and shaping circuits, and the early junction transistors were low frequency devices seemingly more suitable for audio amplifiers than for high speed computing circuits.

Even with presently available junction transistors which have far higher cut-off frequencies than the early units, many typical computer circuits, particularly pulse generators and very high speed flip-flops, can probably best be built with point contact rather than junction transistors.

It seems probable, however, that junction transistors have a place in the computing field; and it is the purpose of this study to evaluate some of the capabilities of these transistors in switching circuits. The work reported here is largely concerned with the use of junction transistors in flip-flop circuits since this is at once the switching circuit of the greatest fundamental importance and the switching circuit to which the junction transistor seems most
directly applicable.

The central problem in the analysis of junction transistor switching circuits, as it often is in engineering practice, is to approximate the physical system in such a way that useful quantitative results can be obtained without prohibitive mathematical complications.

The problem can be solved by first expressing the transistor properties in terms which permit useful, although approximate, solutions to circuit problems when the transistor experiences large signals and high frequencies; and then considering the detailed passive circuitry in terms of the characterization of the transistor, making further approximations if possible, to arrive at a practical solution to the complete problem.

Part II is concerned with the first aspect of the analysis problem, characterization of the transistor. Parts V and VI treat the flip-flop circuit in detail and develop an analytic technique for investigating all of its important properties.

To implement an analysis of this type, it is necessary both to determine which transistor parameters are significant and to find meaningful ways to measure these parameters. The fact that the transistors are to be used as large signal amplifiers suggests that large signal measurements, if they could be properly made, might provide the most useful design information. Fortunately, the large signal analysis suggests many ways that large signal measurements can be made. Part III is devoted to a description of some of the most important large signal measurements to provide a basis for
determining the transistor parameters to be used in the experimental verification of the transient analysis.

It seems desirable to devote some time to a general investigation of flip-flop circuits before attempting to deal with a specific case. Part IV is devoted to such an investigation and discloses the limitations on the amplifier thereby revealing the only possible junction transistor flip-flop circuit configurations.

Part VII is devoted to a discussion of the uses of the flip-flop. It discusses some of its advantages and limitations and presents techniques for using additional transistors to overcome some of its limitations.

The conclusion from the material presented here must be that the junction transistor, by virtue of its performance, is a potential circuit element for use in digital computers. However, a number of considerations such as reliability, cost, size, weight, power requirements, immunity to shock, and availability must also enter into the selection of computer circuit elements.

Reliability is probably the primary consideration in computer design. For hearing aids (Ref.3) and more recently for computers (Ref.4) transistors are proving to be at least as reliable as the best vacuum tubes, and the quality of transistors is being improved rapidly. From the standpoint of cost, transistors are at present at a considerable disadvantage, but this situation is also improving rapidly.

The area of the digital computer field where it appears the junction transistor might be most useful, includes what might be
classified as the moderate speed machines having basic pulse rates of the order of 200 kc. or less. Flip-flops designed with presently available junction transistors are capable of providing useful current outputs of several milliamperes and of changing states in perhaps a microsecond. Such flip-flops can be used as fundamental building blocks for a moderate speed machine. Machines of this type have been used in airborne applications, and it appears that here, where size, weight, and power requirements are important considerations, is the most fruitful place for the application of junction transistors to digital computers.
II THE JUNCTION TRANSISTOR AS AN AMPLIFIER

Preliminary Ideas:

The junction transistor is an active three terminal network element. For the benefit of those who are more familiar with the vacuum tube, another three terminal active circuit element, it may be of benefit to draw a limited analogy between the vacuum tube and the transistor. The three terminals of the vacuum tube are the plate, the grid, and the cathode. The corresponding terminals of the transistor are the collector, the base, and the emitter.

The analogy can be used to find the input and output terminals for the basic amplifier circuits and to determine the phasing of input and output signals.

The transistor always has lower input impedance than the corresponding vacuum tube connection, and one must always consider input current although it is sometimes possible to neglect input voltage. The similarity of the vacuum tube to the transistor is increased considerably if one operates the vacuum tube in the positive grid region.

Physically, the junction transistor consists of a single crystal semi-conductor sandwich, the two extreme regions are of either n or p type semi-conductor and the central region is of the other type. The central region is the base, the two ends are the emitter and collector respectively. The transistor is not ordinarily symmetrical since different impurity concentrations and/or geometry are
required for most efficient functioning of the emitter and collector.

It is evident from the above description that the transistor resembles two junction diodes with a common base. For linear operation, the transistor is connected in such a way that the collector junction is back-biased (the voltage is across the junction in the direction to produce small current flow) and the emitter junction is forward-biased (the voltage is across the junction in the direction to produce large current flow). For n-p-n transistors this means the collector is positive with respect to the base, and the emitter is negative with respect to the base. For p-n-p transistors the polarities are reversed.

There have been many discussions in the literature of linear equivalent circuits for transistors. (Ref.5,6,7) Strictly speaking, these are useful only for small signal operation over a limited frequency range. Of the many possible circuits, the one which seems most appropriate for extension to large signals and wide frequency bands is the equivalent T given in its low frequency form in fig.II-1*.

The attractive feature of this circuit is that the circuit elements have some correspondence with the physical characteristics of the transistor. Thus we identify $r_c$ with the resistance of the collector barrier, $r_e$ with the resistance of the emitter barrier, and $r_b$ with the spreading resistance of the base region. The current generator constant $a$ is almost the same as the current

*The figures are grouped together at the end of the report.
gain parameter $a$ of the transistor.

This last statement is easily seen to be true by considering the set of linear equations represented by the equivalent circuit,

$$v_e = (r_e + r_b) i_e + r_b i_c$$  \hspace{1cm} (II-1a)

$$v_c = (a r_c + r_b) i_e + (r_b + r_c) i_c.$$  \hspace{1cm} (II-1b)

The current gain parameter is by definition the negative of the ratio of $i_c$ to $i_e$ with $v_c$ equal to zero (i.e., with the collector short circuited). We have then

$$a = -\left. \frac{i_c}{i_e} \right|_{v_c=0} = \frac{a r_c + r_b}{r_b + r_c} = \frac{a}{1 + \frac{r_b}{r_c}} \approx a$$  \hspace{1cm} (II-2)

since $r_c \gg r_b$ for junction transistors.

From the physical theory of transistors we know that each junction has a capacity associated with it. (Ref.2) It might seem to be necessary to shunt both $r_c$ and $r_e$ by suitable condensers as a first step toward extending the equivalent circuit to high frequencies. We recall, however, that $r_e$ is approximately the forward resistance of a diode and hence is very small. An approximate analysis shows that the time constant of the emitter junction is very small compared to the other time constants of the circuit, so we simplify the equivalent circuit by including only the collector capacity.

Another result from the physical theory is that $a$ has the frequency dependence of a delay line (Refs.8,9). This frequency dependence introduces reactive components at high frequencies which must be considered in any realistic attempt to study the high
frequency behavior of transistors. It is theoretically impossible to develop an exact equivalent circuit for the frequency variation of \( \alpha \) since it would require an infinite number of circuit elements. The approach has been used to put this frequency dependence into the equivalent circuit by injecting the current through one or two sections of lumped constant delay line (Ref. 10). The equivalent circuit is a cumbersome tool when it gets as complicated as even the simplest transistor equivalent circuit, however, it provides a convenient description of the important transistor parameters.

For switching circuit analysis it is convenient to use the circuit of Fig. II-1 and simply assign \( \alpha \) the first order frequency dependence which was calculated for \( \alpha \). In terms of the LaPlace transform variable, \( s \), this becomes

\[
\alpha = \frac{s_0 \omega_0}{s + \omega_0} \tag{II-3}
\]

The zero frequency value of this function is \( s_0 \) and \( \omega_0 \), the cut-off frequency, is the angular frequency at which the amplitude of \( \alpha \) is down by \( (2)^{-1/2} \). We note that this is also the point at which the phase shift is 45 degrees. In actual transistors, these two points do not occur at the same frequency since (II-3) is only approximately true. This introduces some small complications in the theory which will be discussed later.

Various more complicated equivalent circuits have been proposed which represent the high-frequency small-signal behavior of the transistor more closely than the circuit proposed here. For extension
to large signals, these refinements are perhaps unjustified in view of the approximations which must be made to treat the problem at all. Experience indicates that the proper approximations applied to this simple circuit will yield good first order solutions to switching circuit problems. For that reason the equivalent circuit of fig. II-2 has been chosen as the simplest characterization of the transistor which can profitably be used in switching circuit analysis. The rest of this work will be expressed in terms of that characterization.

Typical values for the equivalent T parameters for a junction transistor might be

\[
\begin{align*}
r_c &= 5 \times 10^6 \text{ ohms} \\
C_c &= 45 \text{ mmfd.} \\
r_e &= 30 \text{ ohms} \\
r_b &= 60 \text{ ohms} \\
\omega_0 &= 5 \times 10^6 \text{ rad./sec.} \\
a_0 &= .96
\end{align*}
\]

It is desirable to develop approximate expressions for such things as input impedance, output impedance, transfer impedance, open circuit voltage gain, and short circuit current gain for the various transistor connections. In doing this we will make use of the approximate values of the equivalent T parameters. That is, we will assume that \( r_e \) and \( r_b \) are always small compared to \( r_c \) or \( r_c(1-a_0) \) and that time constants obtained by multiplying \( r_e \) and \( r_b \) by any circuit capacity are always negligible compared to other time constants in the circuit.
The circuits to be considered in detail are those which have generator impedances $Z_g$ and load impedances $Z_L$ which consist of a parallel combination of a resistor and a condenser. That is $Z_g$ consists of $r_g$ and $C_g$ in parallel, and $Z_L$ consists of $r_L$ and $C_L$ in parallel. In keeping with this notation we introduce the symbol $Z_c$ which denotes the parallel combination of $r_c$ and $C_c$.

The generator and load impedances are of such size that careful consideration must be given to approximations involving them. Ordinarily the resistive component of either load or source is much smaller than $r_c$, but the reactive terms can not be dropped because of this. As an example of the typical approximation procedure, the term $Z_g/Z_c$ would be approximated as

$$
\frac{Z_g}{Z_c} = \frac{C}{r_g C_g} \left( \frac{1}{C} + s \right) \approx \frac{C_c s}{C \left( s + \frac{1}{r_g C_g} \right)}
$$

(II-4)

Exact expressions for the various impedance and gain functions are derived in Ref. 10 for the characterization of fig. II-2. In the following sections the frequency dependence of $\alpha$ is inserted in these expressions to develop useful approximations for the gain and impedance functions in each of the three basic connections.

The Grounded Base Connection:

The grounded base connection is characterized by low input impedance, high output impedance, and no phase reversal. The current gain is less than one, but because of the high ratio of output to
input impedance, power and voltage gain greater than one can be achieved.

The input impedance is given by

\[ Z_{in} = \frac{1}{Y_{in}} = \frac{\frac{r_e}{r_b} + Z_c \left[ \frac{r_e + r_b(1 - a)}{r_b + Z_c + Z_L} \right] + \left( \frac{r_e}{r_b} + r_b \right) Z_L}{r_b + Z_c + Z_L} \]

\[ \approx \frac{s \omega_0^2}{C_L(s + \omega_0) + \left( \frac{r_e}{r_b} + r_b \right) C_L(s + \frac{1}{r_L C_L})} \]

\[ = \left( \frac{r_e}{r_b} + r_b \right) \left\{ s^2 + \frac{s C_L \omega_0}{C_L + C_c} \left[ \frac{1}{\omega_0 r_L C_L} + \frac{r_e + r_b(1 - a_0)}{r_e + r_b} + \frac{C_c}{C_L} \right] \right. \]

\[ + \left. \frac{\omega_0}{r_L(C_L + C_c)} + \frac{r_e + r_b(1 - a_0)}{r_e + r_b} \right\} \]

\[ (s + \frac{1}{r_L(C_L + C_c)}) (s + \omega_0) \]

This network function has two poles in the left half-plane on the real axis; and two zeros, also in the left half-plane, which may be either real or complex conjugate depending on the parameters of the circuit. The magnitude of \( Z_{in} \) for any frequency is the product of the distances from the point on the imaginary axis representing that frequency to the poles divided by the product of the distances from the point to the zeros. It follows from this geometric picture that the maximum value of the magnitude of the input
impedance occurs at either zero or infinite frequency. For the above expression, the maximum value occurs at infinite frequency and is \( r_e + r_b \), a very small quantity.

The fact that the input impedance is small for all values of frequency makes possible a very important simplification in many practical circuits. If the driving impedance is large compared to the input impedance, one can compute the emitter current on the assumption that the emitter voltage is zero. This is the dual of the common assumption of vacuum tube theory that the grid current is zero.

Even though it results in a reduction of the power gain of a transistor stage, it is often desirable to drive the transistor from a high impedance source (relative to the input impedance) since this offers the advantages of greater bandwidth and more linear operation.

It is instructive to examine the input impedance for the simple special case of \( r_L \) very small. Taking the limit of expression (II-5) as \( r_L \) goes to zero gives

\[
Z_{\text{in}} = \frac{(r_e + r_b) \left[ s + \omega_o \frac{r_e + r_b (1 - a_o)}{r_e + r_b} \right]}{s + \omega_o}.
\]  

(II-6)

An equivalent circuit for this expression is given in fig. II-3 together with the values of the elements of the circuit. This circuit has the same zero and infinite frequency impedance as the more complicated expression of (II-5). It is seen that the low frequency reactive component of the input impedance of the grounded base
connection with $Z_L = 0$ is inductive.

It is instructive in connection with the result of (II-6) to point out some of the limitations of the approximate formulas developed here. A glance at the equivalent circuit of Fig. II-2 shows that the high frequency input impedance with the collector grounded must approach $r_e$ as the frequency becomes very high. This is in contrast to equation (II-6) which says it approaches $r_e + r_b$. This does not mean that the approximate formulas have no validity, but simply that they apply to a restricted frequency range. In practice, they can be applied with fair accuracy at frequencies up to the cutoff frequency. We have simply neglected high frequency poles and zeros of the form $\gamma (s + \frac{1}{\tau})$ where $\gamma$ is small.

The output impedance of the grounded base connection is

$$Z_{out} = \frac{1}{Y_{out}} = \frac{(r_b + Z_c) Z_g + r_e Z_c + r_e r_b + r_b Z_c (1 - a)}{Z_g + r_e + r_b}.$$  \hspace{1cm} (II-7)

If $Z_g$ is large compared to $r_e + r_b$,

$$Z_{out} \approx Z_c.$$  \hspace{1cm} (II-8)

The transfer impedance of the grounded base stage is

$$Z_t = \frac{(r_b + a Z_c) Z_L}{Z_L + r_b + Z_c} \approx \frac{a Z_L}{1 + \frac{Z_L}{Z_c}} \approx \frac{a \omega_o}{(C_c + C_L) (s + \omega_o)} \left[ s + \frac{1}{r_L (C_L + C_c)} \right].$$

(II-9)

If the transistor is driven from a voltage source $E_g$ through a series impedance $Z_g$ which is large compared to the input impedance,
the input current $i_e$ becomes

$$i_e = \frac{E_g}{Z_g}$$  \hspace{1cm} (II-10)

and the output voltage $e_c$ becomes

$$e_c = i_e Z_t = \frac{E_g}{Z_g} Z_t.$$

We define the ratio of $e_c$ to $E_g$ as the voltage gain $A_t$ and we have

$$A_t = \frac{e_c}{E_g} = \frac{Z_t}{Z_g} = \frac{a_o \omega_o}{Z_g(C_c + C_L)(s + \omega_o) \left[ s + \frac{1}{r_L(C_L + C_c)} \right]}.$$  \hspace{1cm} (II-12)

For the special case of $r_L(C_L + C_c)$ small this reduces to

$$A_t = \frac{a_o \omega_o r_L}{Z_g(s + \omega_o)}.$$  \hspace{1cm} (II-13)

If $Z_g$ is simply a resistance, the cut-off frequency of $A_t$ is $\omega_o$. A more interesting case occurs when $Z_g$ consists of a resistor $r_g$ in parallel with a condenser $C_g$. Then

$$A_t = a_o \omega_o \frac{r_L c_g}{(s + \frac{1}{r_g C_g})}.$$  \hspace{1cm} (II-14)

If we choose $1/r_g C_g = \omega_o$, the expression for voltage gain becomes

$$A_t = \frac{a_o r_L}{r_g}$$  \hspace{1cm} (II-15)

which is first order independent of frequency. This means that the cut-off frequency becomes $1/r_L(C_L + C_c)$ which was assumed to be very
much greater than \( \omega_0 \). Thus we see that under certain conditions it is possible to extend the bandwidth of a grounded base transistor amplifier by driving it through a suitable compensating input impedance.

The voltage gain of a grounded base amplifier is

\[
A_e = \frac{(r_b + a Z_C) Z_L}{(r_e + r_b) Z_L + r_e Z_C + r_e r_b + r_b Z_C(1-a)} \approx \\
\frac{a_o r_L}{\omega_0 (r_e + r_b)(C_L + C_C)} s^2 \left\{ \frac{r_e + r_b}{\omega_0} + r_L C_C (r_e + r_b) + r_L C_L \left[ r_e + r_b (1-a_0) \right] \right\} s + r_e + r_b (1-a_o).
\]

(II-16)

If we consider the special case of \( r_L (C_L + C_C) \) negligible compared to the other time constants of the circuit, the voltage gain reduces to

\[
A_e = \frac{a_o \omega_0 r_L}{(r_e + r_b) \left( \frac{\omega_0 [r_e + r_b (1-a_0)]}{r_e + r_b} + s \right)}
\]

(II-17)

which has cut-off frequency \( \omega_c \) given by

\[
\omega_c = \frac{\omega_0 [r_e + r_b (1-a_0)]}{r_e + r_b}.
\]

(II-18)

The cut-off frequency \( \omega_c \) is always less than \( \omega_0 \), but it may approach it if \( r_b \) is much smaller than \( r_e \). If the amplifier is driven out of a zero impedance generator, \( \omega_c \) will be the cut-off frequency of the voltage gain from the generator to the output. If the amplifier is driven through a resistor, which is effectively the same as increasing
\( r_e \) in (II-18), the cut-off frequency approaches \( \omega_0 \); and if the proper compensating input condenser is used, the cut-off frequency can be increased to \( 1/r_L(C_L + C_C) \).

The increase in the bandwidth does not necessarily result in an increase in the gain bandwidth product. Driving from a zero impedance source results in a gain bandwidth product of \( a_o \omega_0 \frac{r_L}{(r_e + r_b)} \) driving through a resistor \( r_g \) which is large compared to \( r_e + r_b \) reduces the gain bandwidth product to \( a_o \omega_0 \frac{r_L}{r_g} \), and driving through the compensated input impedance results in a gain bandwidth product of \( a_o/r_g(C_L + C_C) \). The compensated gain bandwidth product may be either greater or less than the gain bandwidth product of the transistor driven from a zero impedance source depending on the values of the circuit constants.

The open circuit voltage gain is obtained from (II-16) by letting the load impedance become infinite. It is

\[
A_e(\text{open circuit}) \approx \frac{a_o \omega_0}{C_L(r_e + r_b)(s + \omega_0)(s + \frac{1}{r_c C_C})} \quad (II-19)
\]

The zero frequency value of this is

\[
\frac{a_o r_c}{r_e + r_b} \quad (II-20)
\]

It is apparent that even though the current gain is less than one in this connection, large values of open circuit voltage gain are possible because of the high ratio of \( r_c \) to \( r_e + r_b \).

The short circuit current gain of the grounded base connection is approximately \( a \) as given by (II-3).
The Grounded Emitter Connection:

The grounded emitter connection has higher input and lower output impedance than the grounded base stage. It produces a phase reversal and has both current and voltage gains greater than one.

The input impedance of the grounded emitter stage is

\[ Z_{in} = \frac{1}{Y_{in}} = \frac{(r_e + r_b) Z_L + r_e Z_c + r_e r_b + r_b Z_c (1-a)}{Z_L + r_e + Z_c (1-a)} \]  

(II-21)

\[ r_L (r_e + r_b) (C_L + C_c) s^2 + \{ (r_e + r_b) (1 + r_L C_c \omega_o) + r_L C_L \omega_o [r_e + (1-a_o) r_b] \} s \]

\[ \approx \frac{\omega_o [r_e + r_b (1-a_o)]}{r_L (C_L + C_c) s^2 + \{ 1 + \omega_o r_L [C_c + (1-a_o) C_L] \} s + \omega_o (1-a_o)} \]

This expression, like the expression for the input impedance of the grounded base connection is difficult to use for practical computation. Since the poles of (II-21) are real, it falls into the class of expressions which have their maximum absolute value at either zero or infinite frequency. In this case the maximum value of the input impedance occurs at zero frequency and is

\[ Z_{in(max)} = r_b + \frac{r_e}{1-a_o} \]  

(II-22)

The expression for the input impedance of the grounded emitter connection becomes much simpler for the special case of \( r_L \) small. Taking the limit of (II-21) as \( r_L \) goes to zero yields,

\[ Z_{in} = \frac{(r_e + r_b) s + \omega_o r_e + \omega_o r_b (1-a_o)}{s + \omega_o (1-a_o)} \]  

(II-23)
An equivalent circuit for this expression is given in fig. II-4 together with the values of the elements of the circuit. This circuit has the same zero and infinite frequency impedance as the more complicated expression of (II-21). It is seen that the low frequency reactive component of the input impedance of the grounded emitter stage is capacitive.

The input impedance of the grounded emitter stage is much higher than the input impedance of the grounded base stage; nevertheless, it is frequently desirable to drive the grounded emitter stage from such a high impedance generator that the input impedance can be neglected when calculating the base current. This results in improved linearity and easier computation, and can with proper compensation result in better frequency response.

The output impedance of the grounded emitter stage is

\[ Z_{\text{out}} = \frac{r_e r_b + Z_c [r_e + r_b (1-a)] + Z_g [r_e + Z_c (1-a)]}{r_b + r_e + Z_g} \]

\[ \approx Z_c (1-a) \approx \frac{s + \omega_0 (1-a_0)}{C_c (s + \omega_0) (s + \frac{1}{r_e C_c})} . \]

An equivalent circuit for the output impedance is given in fig. II-5.

The transfer impedance of the grounded emitter stage is

\[ Z_t = \frac{(r_e - a Z_c) Z_L}{Z_L + r_e + Z_c (1-a)} \]

\[ R = \frac{a_0 \omega_0}{(C_L + C_c) s^2 + \left[ \frac{1 + \omega_0 r_L [C_c + (1-a_0) C_L]}{r_L (C_L + C_c)} \right] s + \frac{(1-a_0) \omega_0}{r_L (C_L + C_c)}} . \]
If the transistor is driven from a voltage source $E_g$ through a series impedance $Z_g$ which is large compared to the input impedance, the input current $i_b$ becomes

$$i_b = \frac{E_g}{Z_g} \quad (II-26)$$

and the output voltage $e_c$ becomes

$$e_c = i_b Z_t = \frac{E_g}{Z_g} Z_t. \quad (II-27)$$

If the ratio of $e_c$ to $E_g$ is defined as a voltage gain $A_t$,

$$A_t = \frac{e_c}{E_g} = \frac{Z_t}{Z_g} = \frac{a_o \omega_o}{Z_g (C_L + C_C)} \frac{1}{s^2 + \frac{1}{r_L \omega_o} \left[ \frac{C_L}{C_L + C_C} +(1-a_0)C_L \right] s + \frac{(1-a_0)\omega_o}{r_L (C_L + C_C)}}. \quad (II-28)$$

For the special case of $r_L$ small, this reduces to

$$A_t = -\frac{a_o \omega_o r_L}{Z_g \left[ s + \omega_o (1-a_0) \right]} \quad (II-29)$$

If $Z_g$ is a resistance, the cut-off frequency of $A_t$ is $\omega_o (1-a_0)$.

If $Z_g$ is a resistor $r_g$ in parallel with a condenser $C_g$, $A_t$ becomes

$$A_t = -\frac{a_o \omega_o r_L C_g}{s + \frac{1}{r_g C_g}} \quad (II-30)$$

By choosing $\frac{1}{r_g C_g} = \omega_o (1-a_0)$, we can make (II-30) frequency independent. For practical purposes, where $r_L$ is not zero, this means that one can cancel the low frequency pole of (II-28) and the actual cut-off frequency will then be determined by the high frequency pole. Thus we see that in the grounded emitter connection
it is possible to increase the bandwidth by driving through a suitable compensating input impedance.

The voltage gain of the grounded emitter stage is

$$A_e = \frac{(r_e - a Z_c) Z_L}{(r_e + r_b)Z_L + r_e Z_c + r_e r_b + r_b Z_c(1-a)} \approx \frac{a_o r_L}{r_L(r_e + r_b)(C_e + C_c)} s^2 + \left[ \frac{r_e + r_b}{\omega_o} + \frac{r_L}{\omega_o} C_e(r_e + r_b) + r_L C_c [r_e + r_b(1 - a_o)] \right] s + r_e + r_b(1 - a_o).$$  \hspace{1cm} (II-31)

We note that to the degree of approximation involved here this is the same (except for the negative sign) as the expression for voltage gain in the grounded base connection.

The voltage gain when $r_L$ is small is

$$A_e \approx \frac{a_o \omega_o r_L}{(r_e + r_b) \left( \frac{r_e + r_b(1 - a_o)}{r_e + r_b} \right) + s} \hspace{1cm} (II-32)$$

and the open circuit voltage gain is

$$A_e(\text{open circuit}) \approx \frac{a_o \omega_o}{C_L(r_e + r_b) (s + \omega_o) \left( s + \frac{1}{r_c C_c} \right)} \hspace{1cm} (II-33)$$

which has the zero frequency value

$$\frac{a_o r_c}{r_e + r_b}. \hspace{1cm} (II-34)$$

The short circuit current gain is
\[ A_1 = \frac{a Z_c - r_e}{r_e + Z_c (1 - a)} \approx \frac{a}{1 - a} \approx \frac{a_o \omega_o}{s + \omega_o (1 - a_o)} \]  

(II-35)

The low frequency value of the short circuit current gain is \( a_o / (1 - a_o) \) and the cut-off frequency is \( \omega_o (1 - a_o) \).

**The Grounded Collector Connection:**

The grounded collector connection has the highest input impedance and lowest output impedance of the basic transistor connections. It has voltage gain less than one, but the current gain is greater than one and substantial power gains are available. The connection does not provide a phase reversal.

The input impedance of the grounded collector stage is

\[ Z_{in} = \frac{r_e r_b + Z_c [r_e + r_b (1 - a)] + Z_L (r_b + Z_c)}{r_e + Z_c (1 - a) + Z_L} \]

\[ \approx \frac{Z_L Z_c}{Z_L + Z_c (1 - a)} \approx \frac{Z_L}{Z_c} \frac{1 - a}{1 - a} \]

(II-36)

which has the form of an impedance \( Z_L (1 - a) \) in parallel with \( Z_c \).

If \( Z_L \) is a resistor and condenser in parallel,

\[ \frac{Z_L}{1 - a} \approx \frac{s + \omega_o}{C_L (s + \frac{1}{r_L C_L}) [s + \omega_o (1 - a_o)]} \]

(II-37)

In the situation of greatest practical interest, \( \omega_o \) is much larger than either \( \omega_o (1 - a_o) \) or \( 1 / r_L C_L \). Under these conditions, (II-37) represents an impedance which cannot be realized as a passive circuit since it has a negative real part at sufficiently high
frequencies, (Ref. 11). To see this, set \( s = j\omega \) and write (II-37) in rationalized form as

\[
\frac{Z_L}{1-a} = \frac{\omega_o^2(1-a_o) + \omega_o \omega \left[ \frac{1}{\omega_o \frac{r_L}{r_L C_L} - 1} \right] + j \omega \left[ \frac{\omega_o(1-a_o)}{\frac{r_L}{r_L C_L}} - \frac{\omega_o^2}{\frac{r_L}{r_L C_L} - \omega_o^2} \right]}{C_L \left\{ \omega_o^4 + \omega_i^2 \left[ \omega_o^2 (1-a_o)^2 + \frac{1}{\frac{r_L}{r_L C_L}^2} \right] + \frac{\omega_o^2 (1-a_o)^2}{\frac{r_L}{r_L C_L}^2} \right\}}
\]  

(II-38)

It is evident from this expression that at sufficiently high frequencies, the input impedance of the grounded emitter connection looks like a series negative resistor and a capacitor (at a single frequency only, since both the resistance and capacitance are functions of frequency.)

A useful approximate expression for the real part of (II-38) can be obtained when \( 1-a_o + 1/\omega_o \frac{r_L}{r_L C_L} \) is negligible compared to one. Let

\[
u = \frac{\omega_o \frac{r_L}{r_L C_L}}{\omega_o (1-a_o)} \]  

(II-39)

and

\[
K = \frac{1}{\omega_o \frac{r_L}{r_L C_L} (1-a_o)} + \omega_o \frac{r_L}{r_L C_L} (1-a_o). \]  

(II-40)

Then the real part of (II-38) is approximately

\[
\frac{Z_L}{1-a} \bigg|_{\text{Real part}} \approx \frac{r_L}{1-a_o} \frac{1-u}{1+u^2+u K}. \]  

(II-41)

The minimum value of this occurs at
\[ u = 1 + (2 + K)^{3/2} \]  

(II-42)

and has the value

\[ \frac{r_L}{1 - a_0} = \frac{1}{2 + K + 2(2 + K)^{3/2}}. \]  

(II-43)

Since the input impedance of the grounded collector stage has a negative real part at sufficiently high frequencies, the possibility of instability exists when the grounded collector stage is driven from a generator even though the output impedance of the generator can be represented as a passive network. A simple way to investigate the stability of the grounded collector stage when an arbitrary admittance \( Y \) is connected across the input terminals is to add admittance \( Y \) to the input admittance \( Y_{\text{in}} \) which is the reciprocal of (II-37). Zeros of the resulting admittance are zeros of the characteristic equation of the network hence if all the zeros of \( Y + Y_{\text{in}} \) are in the left half-plane the amplifier will be stable.

For most switching circuit uses of the grounded collector amplifier, \( Y \) consists of a parallel resistor and condenser to ground. Then

\[ Y = G + Cs \]  

(II-44)

and

\[ Y + Y_{\text{in}} = \frac{(s + a_1)(s + a_2)}{s + \omega_0} \]  

(II-45)
where
\[ a_1, a_2 = \frac{C \omega_c + G + C_L \omega_c (1 - a_0) + \frac{1}{r_L}}{2 (C_L + C)} \left\{ \frac{1}{1 + \left[ \frac{h(C_L + C) G \omega_c + \frac{\omega_c (1 - a_0)}{r_L}}{1 - \left[ C \omega_c + G + C_L \omega_c (1 - a_0) + \frac{1}{r_L} \right]^2} \right]^2} \right\}^{1/2}. \]

For this case, stability is assured.

If \( Y \) consists of an inductance \( L \) to ground,
\[ Y = \frac{1}{L s} \]  

(II-47)

and,
\[ Y + Y_{in} = \frac{C_L L s^3 + C_L L \left[ \frac{1}{r_L} C_L + \omega_c (1 - a_0) \right] s^2 + \left[ \frac{C_L L \omega_c (1 - a_0)}{r_L C_L} + 1 \right] s + \omega_c}{L s (s + \omega_c)}. \]

(II-48)

This will be unstable if
\[ \omega_c > \left[ \frac{1}{r_L} C_L + \omega_c (1 - a_0) \right] \left[ \frac{L}{r_L} - \omega_c (1 - a_0) + 1 \right]. \]

(II-49)

Networks having more complicated values of \( Y \) are analyzed in the same way, but they will not be considered here since they occur rarely in practical switching circuits.

Once stability is assured grounded collector transistors can be used to reduce the loading on critical circuits. Under these conditions low frequency input impedance is of primary importance in determining the rise time of the driving circuit. A single time constant approxima-
tor to the input impedance is very useful for studying this case.

It is obtained by neglecting the \( s \) term in the numerator of (II-47) and neglecting the \( s^2 \) term obtained by multiplying out the denominator. The result is
\[
\frac{Z_L}{1-s_a} \approx \frac{r_L}{1-s_o} \quad \frac{1}{1+\omega_o r_L C_L (1-a_o)} \quad \frac{\omega_o}{\omega_o (1-a_o)}
\]

(II-50)

which is just the impedance of a resistor \(r_L/1-a_o\) in parallel with a condenser \(C_L (1-a_o) + 1/\omega_o r_L\).

To a first approximation then, the input impedance of a grounded collector amplifier driving a parallel RC load is the impedance of a parallel RC circuit with

\[
R_{in} = \frac{r_C r_L}{r_L + r_C (1-a_o)}
\]

(II-52)

and

\[
C_{in} = C_C + C_L (1-a_o) + \frac{1}{r_L \omega_o}.
\]

(II-52)

It will be noted that the input capacity contains a term which is dependent on the load resistance and the cut-off frequency of the transistor. It is imperative that transistors having high cut-off frequencies be used in this connection when low resistance loads are driven and high speed operation is required. For example, if \(r_L\) is 1,000 ohms and \(\omega_o\) is \(10^7\), the input capacity due to this term is 100 mfd, which may well be the major part of the input capacity.

The output impedance of the grounded collector amplifier is

\[
Z_{out} = \frac{r_e r_b + Z_c (r_e + r_b (1-a)) + [r_e + Z_c (1-a)] Z_g}{r_b + Z_c + Z_g}
\]

(II-53)

This impedance may be represented by one of the two passive equivalent circuits given in fig. II-5.
The voltage gain of the grounded collector amplifier stage is

\[ A_e = \frac{Z_c Z_L}{r_e + Z_c \left[ r_e + r_b (1 - a) \right] + (r_b + Z_c) Z_L} \approx 1. \]  \hspace{1cm} (II-54)

For all the circuits of interest here, we may safely disregard any frequency dependence of the voltage gain. However, the transistor in this connection shares with the cathode follower the property of conducting in one direction only so the output waveform cannot follow the input waveform unless the time constants of the load circuit and the cut-off transistor are such that the output voltage can fall as fast as the input voltage.

Since there are two types of transistors, npn and pnp, which conduct in opposite directions, it is possible to construct a simple grounded collector amplifier which will amplify positive and negative pulses with equal ease and drive a capacitive load without the necessity of expending power in a small load resistor. The circuit for this amplifier is given in fig. II-6.

The current gain of the grounded collector amplifier is

\[ A_i = \frac{-Z_c}{r_e + (1 - a)Z_c} \approx \frac{-1}{1 - a} \approx \frac{s + \omega_o}{s + \omega_o (1 - a_o)}. \]  \hspace{1cm} (II-55)

Because of the high value of current gain, substantial power gains are available in this connection even though the voltage gain is less than one.

**Large Signal Junction Transistor Amplifiers:**

Any attempt to make an exact analysis of the large signal behavior of junction transistors, even one based on the approximate
equivalent circuit, leads immediately to prohibitive computational
difficulty. This statement is doubly true if the analysis is to be
applied to flip-flop circuits because of the added complication of
positive feedback.

The difficulty is principally due to the non-linearity of most
of the elements of the equivalent circuit, even in the normal
operating range of the transistor where the emitter junction is
forward biased and the collector junction is back biased. In
switching circuits it is sometimes desirable to operate the transis-
tor cut-off (both junctions back biased) or saturated (both junctions
forward biased). The parameters of the equivalent circuit change
abruptly at the boundaries of the various operating regions.

One approach to the analysis of circuits which operate in more
than one region is to assume that the elements of the equivalent
circuit are linear in each operating region and that they change
abruptly at the boundary of the region. By matching currents and
voltages at the boundaries of the operating regions, it becomes
possible to calculate the behavior of the circuit (Ref.12).

Another analysis uses an analytic approximation for the non-
linearities (which is still non-linear of course) based on the
fundamental physics of the transistor (Ref.13,14). This method is
a very satisfying one particularly for calculations in the satura-
tion region. However, practical considerations still require the
assumption of linear equivalent circuit elements (calculated from
the analytic approximation) in each of the three regions of opera-
tion.
The flip-flop circuits to be analyzed here permit several important simplifications which make the assumption of linear equivalent circuit elements largely unnecessary and yet permit the calculation of circuit performance using linear techniques. These simplifications are possible because:

1. The transistors are driven through impedances which are large compared to the input impedance of the transistor.

2. The load resistance is small compared to the collector resistance.

3. Operation in the saturated region is prohibited.

The importance of condition 1 can easily be seen from fig. II-7. Curve A is a plot of collector current as a function of emitter current and exhibits a truly remarkable linearity. Curve B is a plot of collector current as a function of emitter voltage and is extremely non-linear. The difference in the two curves is a result of the non-linearity of the input impedance. If the transistor is operated in such a way that the input current is determined by external impedances (condition 1), curve A shows that the output current can be easily computed by a linear equation

\[ I_c = -a I_e + I_{co} \]  

(II-56)

which applies over the whole operating region.

In the grounded emitter and grounded collector connections, the base current is the control parameter. Since

\[ -I_e = I_c + I_b \]  

(II-57)
equation (II-56) can be written
\[ I_c = I_b \frac{a}{1 - a} + I_c \frac{1}{1 - a} \]  
(II-58)

For many transistors plots of \( I_c \) vs. \( I_b \) are also quite linear even though non-linearities in (II-56) are multiplied by the large factor \( a/(1 - a) \). Fig. II-8 is such a plot for a number of typical diffused junction n-p-n transistors. The impressive linearity of the current plots suggests that the small signal transfer impedances can be used for large signal analysis with good accuracy when condition 1 is met.

Because the load resistance is small compared with the collector resistance, changes in collector resistance which occur with changes in the operating point have a second order effect on the output of the amplifier. Hence the assumption that the collector resistance is constant does not seriously affect the accuracy of the analysis.

Because of condition 3 above, the collector is always back biased and the collector impedance is high. Under these conditions if the input impedance can be considered negligibly small (though non-linear), the approximate formulas developed above for the remaining network functions do not contain the non-linear resistances \( r_b \) and \( r_e \). The important transistor parameters have been reduced to \( a_o \), \( \omega_o \), \( r_c \), and \( C_c \). The collector resistance is ordinarily negligibly large in the circuits to be considered. Of the remaining parameters \( a_o \) and \( \omega_o \) are relatively independent of operating point and
therefore can be considered constant with reasonable accuracy. $C_c$ is not independent of the collector voltage but is considered to be constant in this analysis in the interest of simplicity. In practice this results in small error because the amplifier ordinarily drives a capacity which is large compared to $C_c$ and also the value of $C_c$ which is used, is obtained by a measurement technique which gives the best linear approximation to $C_c$ over the actual operating range.

Operation in the saturated region has been prohibited because saturated flip-flops change state more slowly and require greater trigger impulses than unsaturated flip-flops. This is a result of an effect known as minority carrier storage. If the transistor amplifier is driven by either a current or voltage pulse, the output increases as the input is increased until the voltage across the collector junction becomes zero at the peak of the pulse. If the input is further increased no additional minority carriers can be removed from the base region by the collector so a concentration of these carriers builds up in the base region. When injection ceases at the emitter (at the end of the pulse) the collector voltage remains at the saturated value until the excess carriers have diffused out of the base region or recombined in it. It is easy to obtain delays of the order of 100 microseconds by this method if sufficient drive is available. Since any delay is detrimental to flip-flop operation, minority carrier storage (saturation) should be avoided for optimum design of flip-flop circuits.

In the cut-off region, both junctions are back biased and may be regarded as high resistances shunted by condensers. In the circuits to be described, the resistances will be negligibly large, but
the capacities may be important in some cases. The emitter capacity can be measured in the same way as the collector capacity.

It is of interest in determining the static stability of a flip-flop to be able to compute the currents which flow when the transistor is cut-off. When the emitter junction is back biased, a small current flows in the reverse direction. Equation (II-56) actually still applies in this case (Ref.13) which indicates that the collector current is slightly less than \( I_{co} \) and the emitter current has some small value in the reverse direction. The base current is the difference between the emitter current and the collector current and hence has a magnitude which is somewhat greater than the collector current. In the circuits to be discussed, the back voltage across the emitter is much less than the back voltage across the collector, hence the emitter current is very small relative to the collector current. A satisfactory approximation is to set \( I_e = 0 \) in (II-56) as the condition for cut-off. A current \( I_{co} \) then flows in both the collector and base of the cut-off transistor.

The principal effect of increasing the temperature of operation of a transistor is to increase \( I_{co} \) since \( I_{co} \) varies exponentially with temperature in such a way as to double every 8 to 10 degrees C. At room temperature, \( I_{co} \) will ordinarily be a few microamperes and will be entirely negligible. However, at elevated temperatures, the stability of the flip-flop may be impaired because of the high value of cut-off current. For this reason, the flip-flop design equations necessarily include \( I_{co} \) so that a particular circuit design can allow for a specified temperature rise.
III PULSE MEASUREMENT TECHNIQUES FOR JUNCTION TRANSISTOR PARAMETERS

The previous discussion has pointed out that $C_c$, $\omega_0$, and $a_0$ are the most important parameters governing the behavior of transistors in switching circuits. Since these parameters are only quasi-linear, more accurate calculations can be made using these parameters if they can be measured in such a way that an effective value over the contemplated operating range is obtained.

The pulse measurement techniques proposed here, based on the approximate network functions previously derived, permit such large signal measurements of the transistor parameters.

The Measurement of $C_c$

Equation (II-8) shows that the output impedance of a grounded base amplifier with the emitter open is $Z_c$ which consists of a large resistor $r_o$ in parallel with $C_c$. It is desired to measure this condenser in terms of an ideal condenser which would require the same charge to change from voltage $V_1$ to $V_2$. A circuit to accomplish this is given in fig. III-1a. The collector voltage on the transistor is constrained to be $V_1$ or some more positive potential by the battery and the high quality germanium point contact diode. If a rectangular positive pulse of good rise time (perhaps 0.1 microseconds) and short duration (perhaps 2 microseconds) having an amplitude of $2(V_2 - V_1)$ is applied to the variable condenser, the collector at the transistor will rise with the pulse to a voltage $V_1 + 2(V_2 - V_1) C/(C + C_x)$ where $C_x$ is the sum of the stray
capacity, $C_s$, and $C_c$. If $C$ is adjusted until the peak of the collector pulse is at $V_2$, the collector has the prescribed voltage swing and $C = C_x$. Narrow pulses are used so that there is no perceptible discharge of the condensers during the pulse. The value of $C_s$ is measured by removing the transistor and $C_c = C_x - C_s$.

A more convenient method using an inverting amplifier is given in fig. III-1b. A null at the oscilloscope indicates that $C$ is adjusted so that the collector pulse has half of the amplitude of the pulse from the pulse generator. For a further refinement $C$ is calibrated in incremental capacity from its minimum capacity and shunted by a trimmer which can be adjusted to compensate for the stray capacity. The collector capacity can then be read directly from the calibrated condenser.

The collector capacity measured by this technique is just the ratio of the voltage change $V_2 - V_1$ to the charge necessary to cause the collector voltage to change from $V_1$ to $V_2$. Therefore, if this capacity were charged from a constant current source, the time required to charge from $V_1$ to $V_2$ would be exactly the same as the time required to charge a linear condenser of capacity $C_c$ under the same conditions. The actual waveforms would be different of course, but since charging time is usually of more importance than waveshape and since conditions approximating constant current charging occur frequently in switching circuits, it appears that the collector capacity measured by this method is the most reasonable linear approximation to the collector capacity over the particular voltage range.
It is interesting to deduce the relationship between the usual small signal collector capacity $C_{cs}$ and $C_c$ measured by the pulse technique. The small signal collector capacity is defined as

$$C_{cs} = \frac{dQ}{dV} \quad \text{(III-1)}$$

and according to theory (Ref.8) is given by

$$C_{cs} = KV^{-k} \quad \text{(III-2)}$$

where $K$ is a constant, $V$ is the collector voltage, and $k$ has the value $1/2$ for step junctions (which diffused junctions approximate) and $1/3$ for graded junctions (which grown junctions approximate).

Combining (III-1) and (III-2)

$$KV^{-k} dV = dQ \quad \text{(III-3)}$$

which can be integrated to give the charge required to change the collector voltage from 0 to $V_2$,

$$Q = \frac{K}{1-k} V_2^{(1-k)} \quad \text{(III-4)}$$

from which we have

$$C_c = \frac{Q}{V_2} = \frac{C_{cs}}{1-k} \quad \text{(III-5)}$$

The value of $C_c$ over a range from 0 to $V_2$ is thus the product of a constant which depends on the junction and $C_{cs}$, the small signal collector capacity at collector potential $V_2$.

Substituting into (III-2) from (III-5) and taking the logarithm yields

$$\log C_c = -k \log V_2 + \log \frac{K}{1-k} \quad \text{(III-6)}$$
Thus a plot of $C_C$ vs. $V_2$ on log-log paper should be a straight line with slope $-k$. Fig. III-2 is such a plot for a number of diffused junction transistors. It is seen that $k$ does indeed have a value very close to the theoretically correct value of $1/2$.

The Measurement of $\omega_0$:

The basic circuit for the measurement of $\omega_0$ is given in fig. III-3. The load resistor $r_L$ is chosen so small that the approximation of equation (II-13) is valid. Under these conditions expression (II-14) shows that the amplifier is first order frequency independent if $RC = 1/\omega_0$. Frequency independence can easily be detected if the circuit is driven by a voltage pulse having a very accurate rectangular shape and the output is observed by a broadband oscilloscope. The condition for frequency independence is that the output waveshape be as nearly as possible a replica of the input waveshape. Typical waveforms for a particular transistor in the circuit of fig. III-3 are shown in fig. III-4 as they appear for different values of $C$. From this figure it is apparent that it is relatively easy to obtain the proper value of $C$.

The Measurement of $\frac{a_0}{1-a_0}$ and $\omega_0(1-a_0)$:

It might seem to be redundant to offer methods of measuring both $\omega_0$ and $\omega_0(1-a_0)$, but from a practical point of view, it is desirable to be able to measure both of these quantities. The measurement of $\omega_0$ is the measurement of the frequency at which the current gain of the grounded base amplifier is down by 3 db. The measurement of
\( \omega_o(1-a_o) \) is a measurement of the frequency at which the current gain of the grounded emitter connection is down 3 db. These two frequencies will have the indicated relationship only if \( a \) has the postulated frequency dependence which specifies both the amplitude and phase shift of \( a \) as a function of frequency. It is preferable to measure \( \omega_o(1-a_o) \) when the transistor is to be used in the grounded emitter connection, and \( \omega_o \) when it is to be used in the grounded base connection.

The basic circuit for measuring \( a_o/(1-a_o) \) and \( \omega_o(1-a_o) \) is given in fig. III-5. In this circuit, \( r_L \) is chosen to be so small that the approximation of equation (II-29) is valid and \( R_2 \gg r_L \). Equation (II-30) shows that the amplifier is first order frequency independent if \( 1/RC = \omega_o(1-a_o) \). Frequency independence is detected as before by driving the amplifier with a rectangular pulse and adjusting the condenser for best output waveshape. Typical waveforms obtained during this measurement are given in fig. III-6. It can be seen from this figure that the proper adjustments are easily made.

In order to operate the circuit, point A is observed with a wideband oscilloscope while C is adjusted for best output waveshape. The oscilloscope is then transferred to point B and \( R_2 \) is adjusted for null. Under these conditions,

\[
\omega_o(1-a_o) = \frac{1}{RC} \quad \text{(III-7)}
\]

\[
\frac{E_o}{R_2} = \frac{E_i}{R_1} \quad \text{(III-8)}
\]
using (II-30)

\[
\frac{E_0}{E_1} = \frac{R_2}{R_1} = \frac{a_0 r_L}{R(1-a_0)}
\]  \hspace{1cm} (III-9)

so

\[
\frac{a_0}{1-a_0} = \frac{R_2 R}{R_1 r_L}.
\]  \hspace{1cm} (III-10)

R\textsubscript{2} may be calibrated directly in terms of \(a_0/(1-a_0)\) and C may be calibrated directly in terms of \(\omega_0(1-a_0)\) for greatest operating convenience.

**Direct Measurement of the Grounded Emitter Current Gain Bandwidth Product:**

In the transient analysis of transistor circuits, the product \(a_c \omega_0\) occurs frequently. If the transistor is used in the grounded emitter connection, it is to be understood that this quantity is actually the grounded emitter gain bandwidth product, \([a_0/(1-a_0)](1-a_0)\omega_0\) which, as was shown above, is not necessarily equal to the gain bandwidth product in the grounded base connection. While this product may be obtained from the above measurement, it is more convenient to measure it directly. One circuit which permits measuring this product over a large current swing at a constant collector voltage is given in fig. III-7.

In the absence of an input pulse, the transistor is drawing a small current \(I_{co}/(1-a_0)\). \(E_1\) and \(R\) are adjusted to give the desired current \(I\) and the collector voltage \(E_c\) is adjusted to the desired value by adjusting the clamp voltage \(E_2\). If a rectangular
pulse from a low impedance pulse generator is applied to the relatively small input condenser C the condenser will charge to the peak amplitude of the pulse in a very short time (0.2 microseconds is a typical value) due to the low input impedance of the transistor. It is therefore possible to make the simplifying assumption that the input signal can be approximated by a current impulse of magnitude EC. Since the transistor has a very low impedance load, the forward resistance of a diode, the output current resulting from the input current impulse is given by the product of the current impulse and the inverse transform of the short circuit current gain of the grounded emitter stage given by (II-35). The collector current resulting from the input current impulse EC is then

\[ I_c = -a_0 \omega_0 EC e^{-\omega_0 (1 - a_0) t} \]  

(III-11)

No appreciable voltage will be developed at the collector until the peak value of \( I_c \) exceeds the initial clamp current I. If EC is adjusted until the peak value of \( I_c \) is just equal to I,

\[ a_0 \omega_0 = \frac{I}{EC} \]  

(III-12)

which provides the desired measurement of the gain bandwidth product.

The principal difficulty in making this measurement is to detect precisely when the peak value of \( I_c \) is equal to I since the clamp diodes do not have zero forward resistance. A circuit arrangement to aid in detecting this critical value of peak current is included in fig. III-7. The clamp circuit is actually two diodes in parallel with an inductance in series with one of them. The inductance is chosen
to have a natural period when shunted by the oscilloscope which is short compared with \( \frac{1}{\omega_0(1-a_0)} \) (0.3 microseconds is an appropriate value). If the current impulse is not large enough to disconnect the diodes, the inductance cannot ring. However, if the impulse disconnects the diodes, the inductance will ring. The peak value of \( I_c \) is taken to be equal to \( I \) at the first visible sign of ringing. This is a much more sensitive method of detection than observing the collector voltage with the oscilloscope. Typical waveforms obtained during this measurement are given in fig. III-3.

The values of grounded emitter gain bandwidth product were measured for a number of transistors as a function of collector voltage and peak current. The results of these measurements given in fig. III-9, show that in general \( a_0 \omega_0 \) goes down as the peak current is increased and goes up as the collector voltage is increased.

In the subsequent transient analysis, it is desired to use the best average value of \( a_0 \omega_0 \) as a constant in predicting the transient behavior of the transistor in flip-flop circuits. Although \( a_0 \omega_0 \) is not subject to extreme variation over the operating region, fig. III-7 shows that the choice of the proper value is a matter of some conjecture unless the transistor is operated at constant collector voltage with a known current swing. When these conditions are not met, the value of \( a_0 \omega_0 \), which is used in computation is the value measured when the collector voltage and peak current are approximately equal to the average values of these quantities in the interval over which it is desired to measure \( a_0 \omega_0 \).
IV FLIP-FLOP CIRCUITS

Definitions:

One of the most important switching circuits is the bi-stable circuit commonly known as a flip-flop. In recent years the meaning of this term has been extended to include a wide variety of devices which have two distinguishable stable states which may or may not be static. In this section a somewhat restricted class of flip-flop circuits (which nevertheless includes the most common circuits) will be examined from a general point of view to determine the requirements on the active elements used in the circuit.

The type of flip-flop considered here is a static, bi-stable device characterized by output signals which are one of two possible voltage states. It is possible to cause the circuit to change rapidly from one stable state to the other by applying suitable input triggering signals. Circuits based on negative resistance properties of devices such as point contact transistors are not considered because junction transistors (and vacuum tubes as they are normally used) do not exhibit negative resistance phenomena.

Restrictions on the Amplifier:

The flip-flops to be discussed here can be considered as being made from a stable three-terminal amplifier, having input terminal 1 and output terminal 2 with terminal 3 grounded, by connecting terminals 1 and 2 together. If terminal 1 is connected to terminal 2,
\[ I_1 = -I_2 \quad \text{(IV-1)} \]

and

\[ E_1 = E_2. \quad \text{(IV-2)} \]

To see if flip-flop operation is possible, it is necessary to examine the singular points of the system. The singular points are those sets of values of the variables \( I_1, I_2, E_1, \) and \( E_2 \) for which equations (IV-1) and (IV-2) are satisfied and for which the first and all higher derivatives of the variables with respect to time are zero. Clearly all singular points are points of equilibrium. A singular point is called a stable singular point if a region in the neighborhood of the singular point can be found such that a small initial displacement from the singular point results in small displacements of the variables with these displacements going to zero as time goes to infinity. It has been shown quite generally that stability of singular points of non-linear systems can be determined from an examination of the stability of the small signal linear system approximating the actual system in the neighborhood of the singular point (Ref. 15).

In order to meet the design requirement of two stable states, the circuit formed when terminals 1 and 2 are connected together must have two stable singular points. It will be shown that it will also have an unstable singular point; and conversely, that the existence of the proper type of unstable singular point requires the existence of two other singular points which may be stable.

If both of conditions (IV-1) and (IV-2) are imposed simultaneously
an amplifier which can be used to make a flip-flop will exhibit unstable behavior over some part of the operating region. However, either of the conditions can be enforced independently and stable operation will obtain. For example, current generators could be used to make \( I_1 = -I_2 = I \). For every value of \( I \) a definite value of \( E_1 \) and \( E_2 \) would be determined.

If a plot of \( E_1 \) vs. \( E_2 \) is made as \( I \) is varied, a curve is obtained which might resemble fig. IV-1. Points A, B, and C where the curve intersects the line \( E_1 = E_2 \) are singular points since the curve was taken point by point so that all the time derivatives were zero. For two stable states to exist, points A and C must be stable singular points. Point B will be an unstable singular point since if points 1 and 2 were connected together a small increase in \( E_1 \) would tend to produce a larger increase in \( E_2 \) which would tend to produce a larger increase in \( E_1 \) and so on.

Unstable singular points such as the one at B, which can be shown to be unstable from the zero frequency behavior of the system in the neighborhood of the singular point, will be called d.c. unstable singular points. These points are easily recognized from a curve such as fig. IV-1 since the slope of the \( E_1 \) vs. \( E_2 \) curve is greater than 1 at a d.c. unstable singular point.

Since saturation is a characteristic of all physical amplifiers, the existence of a d.c. unstable singular point requires the existence of two additional singular points which are not d.c. unstable. The stability of these points must be determined by small signal analysis of the system in the neighborhood of the points.
In terms of the above definitions, a flip-flop can be formed by shorting together the input and output of a stable amplifier if the amplifier is such that a d.c. unstable singular point is formed and the additional singular points are stable.

The flip-flop conditions can be put in a more useful form by writing the small signal linear equations for the amplifier in the neighborhood of point B. These are

\[ i_1 = G_{11} e_1 + G_{12} e_2 \]  
\[ i_2 = G_{21} e_1 + G_{22} e_2 \]  

where the G's are the low frequency small signal admittance parameters of the amplifier and the lower case e's and i's are the differences between the actual currents and voltages and the values they would have at point B.

Since the amplifier is unconditionally stable,

\[ G_{11} G_{22} - G_{12} G_{21} > 0. \]  

When 1 is connected to 2, the admittance equation for the resulting network is

\[ i = \left( G_{11} + G_{22} + G_{12} + G_{21} \right) e \]  

and since this is to be unstable,

\[ G_{11} + G_{22} + G_{12} + G_{21} < 0. \]  

This inequality is sufficient to assure that singular point B will have the proper type of instability.
It is shown in the appendix that a consequence of inequalities (IV-1) and (IV-6) is that the short circuit current gain $A_{sc}$ is

$$|A_{sc}| = \frac{|G_{21}|}{G_{11}} > 1$$  \hspace{1cm} (IV-7)

and the open circuit voltage gain $A_{oc}$ is

$$|A_{oc}| = \frac{|G_{21}|}{G_{22}} > 1.$$  \hspace{1cm} (IV-8)

Therefore, a stable amplifier which is to be used to make a flip-flop by shorting its input to its output must have at the central singular point both d.c. open circuit voltage gain greater than one and d.c. short circuit current gain less than minus one.

The discussion thus far has been concerned primarily with those conditions which produce d.c. instability at the central singular point. It is equally important for flip-flop operation that the circuit be stable at the extreme singular points. At either extreme singular point, small signal linear equations can be written

$$i_1 = Y_{11} e_1 + Y_{12} e_2$$
$$i_2 = Y_{21} e_1 + Y_{22} e_2.$$  \hspace{1cm} (IV-9)

The condition for stability when the input is shorted to the output is that

$$Y = Y_{11} + Y_{12} + Y_{21} + Y_{22}$$  \hspace{1cm} (IV-10)

have no zeros in the right half-plane.

It is impossible to discuss this function unless the nature of the non-linearity is specified. In one very important special case, which is the only one of concern here, the amplifier has zero small
signal gain for all frequencies at the extreme singular points. For this case, the extreme singular points are unconditionally stable.

**Possible Flip-flop Circuit Configurations:**

The above theory can be used to discard a large class of potential flip-flop amplifiers. In particular it has been shown that it is impossible to construct a flip-flop consisting solely of grounded base stages since it is impossible to get d.c. short circuit current gain greater than one in absolute value in the grounded base connection. Similarly, it is impossible to construct a flip-flop consisting solely of junction transistors in the grounded collector connection since it is impossible to get d.c. open circuit voltage gain greater than one in the grounded collector connection. It is possible to construct a flip-flop using a grounded base stage for voltage gain and a grounded collector connection for current gain. The grounded emitter stage provides both current and voltage gain greater than one in absolute value, but it also causes a phase reversal which makes it necessary to use two transistors in this connection to construct a flip-flop. Thus, the minimum number of junction transistors required to construct a flip-flop circuit is two, and these must be arranged either as a grounded base stage with a grounded collector stage, or as two grounded emitter stages.

Some insight into the relative usefulness of the two possible junction transistor flip-flops using no more than two transistors can be obtained by considering the analogous vacuum tube flip-flop circuits, for the preceding theory also shows that there are just
two possible vacuum tube flip-flop circuits using only two tubes.

The first of these circuits, using two grounded cathode tubes, is the familiar grid to plate coupled circuit which is analogous to the transistor flip-flop using two grounded emitter stages. This will be called the symmetric flip-flop because of its symmetrical complementary output signals and because it can be triggered in a symmetrical way by identical pulses applied to different but similar parts of the circuit.

The second vacuum tube circuit, the cathode coupled flip-flop, uses one grounded grid and one grounded plate stage. This is analogous to the transistor flip-flop having one grounded base and one grounded collector stage. This circuit will be called the unsymmetric flip-flop. It has the disadvantages of having only one output (this can be overcome by a circuit modification) and of requiring unsymmetrical triggering. These disadvantages have made the cathode coupled flip-flop relatively unused.

It appears that the symmetrical transistor flip-flop will also be much more generally useful than the unsymmetrical flip-flop. Therefore, the detailed design equations are derived for that type of flip-flop.
V STATIC CONSIDERATIONS IN THE DESIGN OF SYMMETRIC JUNCTION TRANSISTOR FLIP-FLOPS

Static Design Objectives:

The goal of the static design of flip-flops is to assure that the circuit will have two stable states when it is required to supply or absorb a specified load current and when there are specified variations in transistor and circuit parameters, temperature, and supply voltage. Other topics of practical interest such as the determination of the required trigger signals and the transient waveforms after triggering are discussed separately.

The Basic Flip-Flop Circuit:

The junction transistor flip-flop chosen as the basic circuit for consideration here is given in fig. V-1. The reasons for choosing this particular configuration will become clear as the design criteria determining allowed values of the various circuit elements are discussed. It may seem that the inclusion of clamp diodes to limit the collector voltage swing is an unnecessary luxury, and indeed this may be true in certain applications. However, it is presumed that the flip-flops discussed here will be used as standard elements in digital computers and will be expected to drive logical gating networks. In this application it is highly desirable that the flip-flop be capable of supplying or absorbing specified currents at specified voltages which are essentially independent of the load current as long as it does not exceed the specified value. The clamp diodes provide a convenient way of accomplishing this objective. In some applications, the lower clamp diode could be eliminated and
transistor saturation used to set the lower voltage. If this is done, the minority carrier storage effect limits the ability of the trigger pulse to turn the saturated transistor off and the high speed operation of the circuit is impaired.

The following treatment will develop a technique for synthesizing circuits of the form of fig. V-1 meeting physically realizable design requirements. In the process, the limits on realizability imposed by the transistor will be explored so that reasonable requirements can be specified and intelligent criteria for the selection of transistors for use in flip-flops can be set up.

The Static Flip-Flop Circuit:

The static flip-flop design information can be obtained from consideration of the circuit of fig. V-2 which is just the circuit of fig. V-1 after removal of all of the circuit elements which do not have current flowing through them when the circuit has reached steady state conditions.

In accordance with the approximations discussed in part II, the collector and base leads of $T_n$, the "off" transistor, have a temperature sensitive current $I_{con}$ flowing through them as indicated on the figure. $I_{cp}$, the collector current of $T_p$, the "on" transistor, also contains a temperature sensitive part for from equation (III-1)

$$I_{cp} = I_{ep} + I_{cop}.$$  \hspace{1cm} \text{(V-1)}

Since

$$I_{ep} = I_{bp} + I_{cp},$$  \hspace{1cm} \text{(V-2)}
the base current of $T_p$ in terms of its collector current can be written as

$$I_{bp} = I_{cp} \frac{(1 - a_o)}{a_o}$$  \hspace{1cm} (V-3)$$

The current through the common emitter resistor is just the emitter current of $T_p$, so the common emitter voltage is

$$E_e = I_{ep} R_4 + E_3 = \frac{R_4}{a_o} (I_{cp} - I_{cop}) + E_3$$  \hspace{1cm} (V-4)$$

In the following discussion it is assumed that conducting diodes $D_2$ and $D_3$ have sufficiently low impedance that the collector voltages of $T_p$ and $T_n$ can be taken as $E_p$ and $E_n$ respectively. $I_p$ and $I_n$ are thus currents which could be supplied or absorbed respectively by an external load without materially affecting the collector voltage of the transistors. It is also assumed that the base to emitter impedance of the conducting transistor is so low that the base of the conducting transistor has the same potential as the emitter to simplify calculation of the base current. Actually, the emitter to base voltage is a function of the emitter current and may be as high as a few tenths of a volt, but this is generally negligible compared to the collector voltage swing.

The base voltage of the non-conducting transistor is given as $E_e = \delta$. The transistor will be cut-off for all $\delta > 0$.

**The Selection of $E_n - E_p$:**

One of the difficulties of flip-flop design is deciding where to start since a number of the variables may be chosen arbitrarily. The
point of view adopted here is that the nominal voltage swing \( E_n - E_p \) is the first thing to specify since it is normally determined by the circuits which are to be driven by the flip-flop. For stability, the voltage swing must be chosen to be large compared to the expected variations in the voltages to which the collector is clamped and the possible voltage drops across the clamp diodes, but it must at the same time be smaller than the maximum collector voltage rating of the transistor.

With presently available transistors a practical upper limit for the voltage swing is perhaps 30 volts although many transistors with higher voltage ratings have been produced. It will be shown from power considerations that high values of collector swing and high values of "on" current cannot be achieved simultaneously.

Selection of the Maximum Collector Current:

The most common design objective is to obtain the largest possible available load current from the flip-flop consistent with the desired swing and the capabilities of the transistors. To meet this condition, the largest possible value of maximum collector current is chosen. One way of choosing this is to use the maximum collector current rating of the transistor, although there is considerable experimental evidence to suggest that the maximum current rating can be exceeded without damage to the transistor if the power dissipation limit is carefully respected.

It is important to choose a value of maximum current which will prevent the average collector dissipation from exceeding the rated value even under transient conditions. The average collector power
dissipation can be calculated for the maximum possible trigger rate by the methods to be presented for the transient analysis of flip-flop circuits. Unfortunately, this is a laborious process. For design purposes, an approximate rule-of-thumb method of assuring that the average collector dissipation will be below the rating is vastly more convenient to use.

In fig. (V-3) the grounded-emitter collector characteristic of a typical transistor is plotted together with a hyperbola representing the rated collector dissipation of 0.044 watts. On such a diagram, a straight line connecting the two points corresponding to the two stable states of the transistor gives a good approximation to the average path of the state point during the flipping cycle. For the idealized case, one point would be at \( E = E_n - E_p, \) \( I = 0, \) and the other point would be at \( E = 0, I = I_m, \) where \( I_m \) is the maximum current that should be drawn by the transistor. The line connecting these two points would be tangent to the rated power dissipation curve. If the rated power is \( P_r, \) the equation for such a line is

\[
I = \frac{4 P_r}{(E_n - E_c)^2} (E - E_n + E_c). \tag{V-5}
\]

The relationship between the maximum current which should be drawn and the voltage swing is then

\[
I_m = \frac{4 P_r}{E_n - E_c}. \tag{V-6}
\]

This relation will be regarded as a convenient approximation relating the voltage swing and the maximum allowed current to the
power rating of the transistor. It expresses one of the important ways in which transistor characteristics limit flip-flop design. As a factor of safety it might be desirable to use a power somewhat less than the rated power in (V-6), but experience with flip-flops designed with $P_r$ equal to the rated power seems to indicate that such a procedure results in excellent transistor life.

On the basis of these considerations, it is possible to choose a value of $I_S$, the maximum current which will be drawn by the transistors in the flip-flop. $I_S$ should not exceed $I_m$, but it may be less than $I_m$ either because of a current limitation of the transistor or because it is desired to conserve power.

The Selection of $R_h$ and $E_p - E_3$:

The first consideration governing the choice of these parameters is the necessity of keeping the static power dissipated by the transistor in the "on" state below the rated power dissipation. The operating point of the transistor having the collector characteristics of fig.V-3 can be found by a simple construction. The collector voltage referring to fig.V-2 is just $E_p - E_3 = (I_c + I_b)R_4$, so a plot of the line

$$E = E_p - E_3 = (I_c + I_b)R_4$$  \hspace{1cm} (V-7)

on the collector characteristic of fig.V-3 is the locus of possible operating points. The operating point will then be determined by the base current supplied to the transistor. If the locus of possible operating points lies entirely within the region under the
rated power curve, any transistor which is put in the circuit will operate within its rating. It will be noted that the locus of possible operating points is always farther from the rated power curve than the straight line

\[ E = E_p - E_3 - I_c R_4 \] (V-8)

regardless of the current gain of the particular transistor. Therefore, if the circuit is designed so that the line (V-8) lies entirely within the region under the rated power curve, any transistor which might be put into the circuit will operate within its power rating.

The maximum power dissipated along line (V-8) is

\[ P = \frac{(E_p - E_3)^2}{4 \Delta R_4} \] (V-9)

Ordinarily a safety factor \( K_p \) is employed to make

\[ P = K_p P_r \]

where \( K_p \) is a number less than one. Thus one relation between \( E_p - E_3 \) and \( R_4 \) is

\[ 4 K_p P_r R_4 = (E_p - E_3)^2 \] (V-10)

which assures that the collector dissipation in the "on" state will always be less than \( K_p P_r \).

The second condition on \( E_p - E_3 \) and \( R_4 \) results from the necessity of limiting the current drawn by the flip-flop to \( I_s \). This is accomplished by designing the flip-flop so that the transistor will saturate when \( I_c = I_s \). Since this will occur only
with high values of current gain, a good approximation which sets an upper limit for \( I_s \) is to assume that \( I_b \) is zero so that saturation occurs at the intersection of the straight line (V-8) and the saturation line, point \( S \) on fig. V-3. If the slope of the saturation line is \( R' \), the saturation value of current is given by

\[
I_s = \frac{E_p - E_2}{R_4 + R'}.
\] (V-11)

The value of \( R' \) depends on the type of transistor and it also varies from transistor to transistor within a given type. Diffused junction transistors have a value of \( R' \) which is so small that it can be taken to be zero for most purposes. Crowed junction transistors may have values of \( R' \) of the order of 200 ohms which may not be negligible in determining saturation current. The value of \( R' \) to be used in (V-11) is the minimum value for the type of transistor to be used since this is intended to define a maximum value of the saturation current.

The correct choice of \( R_4 \) and \( E_p - E_2 \) satisfies both (V-10) and (V-11). Solving these equations simultaneously for \( R_4 \) yields

\[
R_4 = \frac{2K_p P_r}{I_s^2} - R' + \frac{2K_p P_r}{I_s^2} \left( 1 - \frac{R' I_s^2}{K_p P_r} \right)^{1/2}.
\] (V-12)

If \( \frac{R' I_s^2}{K_p P_r} \) is much less than one, this can be approximated by

\[
R_4 = \frac{K_p P_r}{I_s^2} \approx 2 R'.
\] (V-13)

In practical circuits it is usually desirable to use standard values for the resistors. To obtain a standard value for \( R_4 \) from
(V-12) or (V-13), an approximate value for $K_p$ is chosen and a value of $R_u$ is computed using one of these equations. This value of $R_u$ will not be a standard value in general so the next smaller standard value is chosen. This results in a slightly smaller value of $K_p$ than that originally chosen, but this is inconsequential.

The value of $R_u$ (and therefore of $K_p$) should be chosen to be as large as possible consistent with long life of the transistors because the rate of change of collector current with respect to $a_o$ is smaller for larger values of $R_u$. This statement, which will be proved presently, indicates why the particular circuit arrangement with a common emitter resistance was chosen. Maximum power dissipation could have been limited by resistors in the collector circuits between the collectors and the clamp points, but this would have resulted in a smaller range of $a_o$ for a given range of collector current than the circuit chosen.

Once the value of $R_u$ is chosen, the value of $E_c - E_3$ is obtained from (V-11).

This treatment has assumed that the power supply voltages are entirely arbitrary which is the usual case for computing circuits. If the power supply is limited to certain standard values such as multiples of 1.5 volts, the next value below that calculated for $(E_p - E_3)$ in (V-11) may be chosen with a slight reduction of $I_s$ and a negligible effect on the final design of the circuit.

**Design Tolerances:**

In digital computer circuits where many flip-flops are used,
reliability is of primary importance. Since it is impossible to
maintain zero tolerance on power supply voltages, resistance
values, and transistor parameters, it is imperative to design the
circuit to supply certain minimum available currents and have two
stable states with a specified tolerance on every circuit parameter.

It was unnecessary to consider tolerances on $E_p - E_3$ and $R_4$
in selecting nominal values of these parameters because of the use
of the safety factor, $K_p$, which is sufficient to prevent normal
variations of these parameters from causing excessive collector dis-
sipation. However, the remainder of the static design problem must
be approached with the knowledge that every circuit parameter has an
allowed variation which must be considered. For this purpose it is
convenient to introduce the following notation:

\[
1 + \frac{\Delta E_2}{E_1} = \varepsilon_1 \\
1 - \frac{\Delta E_1}{E_1} = \varepsilon_2 \\
1 + \frac{\Delta E_2}{E_2} = \varepsilon_3 \\
1 - \frac{\Delta E_2}{E_2} = \varepsilon_4 \\
1 + \frac{\Delta E_P}{E_P} = \varepsilon_5 \\
1 - \frac{\Delta E_P}{E_P} = \varepsilon_6 \\
1 + \frac{\Delta E_n}{E_n} = \varepsilon_7 \\
1 - \frac{\Delta E_n}{E_n} = \varepsilon_8 \\
1 + \frac{\Delta R_1}{R_1} = \varepsilon_9 \\
1 - \frac{\Delta R_1}{R_1} = \varepsilon_{10} \\
1 + \frac{\Delta R_2}{R_2} = \varepsilon_{11} \\
1 - \frac{\Delta R_2}{R_2} = \varepsilon_{12} \\
1 + \frac{\Delta R_3}{R_3} = \varepsilon_{13} \\
1 - \frac{\Delta R_3}{R_3} = \varepsilon_{14} \\
1 + \frac{\Delta R_4}{R_4} = \varepsilon_{15} \\
1 - \frac{\Delta R_4}{R_4} = \varepsilon_{16}
\]
where the \( A \)'s represent the allowed deviation in the particular parameter.

\( E_3 \) has been arbitrarily chosen as the reference potential and therefore has no variation.

The Selection of \( R_2, R_3, E_2, I_{cp}(\text{min}) \) and \( a_0(\text{min}) \):

The nodal equation at the base of the conducting transistor is

\[
I_b = I_{cp} \frac{(1-a_0)}{a_0} = \frac{I_{cop}}{a_0} = \frac{E_n}{R_{2p}} + \frac{E_2}{R_{3p}} = E_e \left( \frac{1}{R_{2p}} + \frac{1}{R_{3p}} \right), \quad (V-15)
\]

and at the base of the non-conducting transistor

\[
E_e \left( \frac{1}{R_{2n}} + \frac{1}{R_{3n}} \right) = \frac{E_n}{R_{2n}} - \frac{E_2}{R_{3n}} = I_{con} = \delta \left( \frac{1}{R_{2n}} + \frac{1}{R_{3n}} \right) \geq 0. \quad (V-16)
\]

If the inequality is satisfied and \( I_n \) and \( I_p \) are both greater than zero so that \( E_n \) and \( E_p \) are determined, the flip-flop will have two stable states.

Eliminating \( E_e \) from \((V-15)\) and \((V-4)\) and solving for the collector current gives

\[
I_{cp} = \frac{E_n}{R_{2p} + \frac{E_2}{R_{3p}} + \left( \frac{R_4}{a_0} \frac{I_{cop}}{2} \right) - E_3 \left( \frac{1}{R_{2p}} + \frac{1}{R_{3p}} \right) + \frac{I_{coc}}{a_0}}{1 - \frac{a_0}{a_0} + \frac{R_4}{a_0} \left( \frac{1}{R_{2p}} + \frac{1}{R_{3p}} \right)}. \quad (V-17)
\]

The derivative of this with respect to \( a_0 \) is

\[
\frac{d I_{cp}}{d a_0} = \frac{I_{cp} \left( \frac{E_n}{R_{2p}} + \frac{E_2}{R_{3p}} - E_3 \left( \frac{1}{R_{2p}} + \frac{1}{R_{3p}} \right) \right)}{1 - a_0 + R_4 \left( \frac{1}{R_{2p}} + \frac{1}{R_{3p}} \right)}. \quad (V-18)
\]

which proves the assertion that the circuit sensitivity to \( a_0 \) is
materially improved by the presence of $R_4$ if $R_4(1/R_{2p} + 1/R_{3p})$

is appreciably greater than $1 - a_o$.

If $E_e$ is eliminated from (V-16) by using (V-15) the result is

$$\frac{R_{2p}}{R_{2n}}\frac{R_{3p}}{R_{3n}}\frac{(R_{2n} + R_{3n})}{(R_{2p} + R_{3p})} \left[ \frac{E_n}{R_{2p}} + \frac{E_2}{R_{3p}} + \frac{I_{cop}}{a_0} - \frac{I_{cp}}{a_0}(1 - a_o) \right]$$

$$= \frac{E_e}{R_{2n}} - \frac{E_2}{R_{3n}} - I_{con} \geq 0.$$  \hspace{1cm} (V-19)

Replacing particular resistance values with nominal values plus or minus tolerances chosen to make the inequality most difficult to satisfy makes it possible to write the worst case of (V-19) as

$$\frac{R_2 \varepsilon_{11}}{R_2 \varepsilon_{12}} \frac{R_3 \varepsilon_{13}}{R_3 \varepsilon_{14}} \left[ \frac{E_n \varepsilon_{38}}{R_2 \varepsilon_{11}} + \frac{E_2}{R_3 \varepsilon_{13}} + \frac{I_{cop}}{a_0} - \frac{I_{cp}}{a_0}(1 - a_o) \right]$$

$$= \frac{E_e \varepsilon_{52}}{R_2 \varepsilon_{12}} - \frac{E_2}{R_3 \varepsilon_{14}} - I_{con} \geq 0$$  \hspace{1cm} (V-20)

where consideration of what constitutes a worst case of terms involving currents and $E_2$ has been temporarily deferred.

By making the reasonable assumption that the tolerance on $R_2$ is equal to the tolerance on $R_3$,

$$\varepsilon_{11} = \varepsilon_{13} \quad \text{and} \quad \varepsilon_{12} = \varepsilon_{14}$$  \hspace{1cm} (V-21)

and (V-20) becomes
From (V-17)

\[
\frac{I_{cp}(1-a_o)}{a_o} = \frac{E_n}{R_2p} - \frac{E_2}{R_3p} + \frac{R_4}{a_o I_{cop} - E_3} \left( \frac{1}{R_2p} + \frac{1}{R_3p} \right) + \frac{I_{cop}}{a_o} \cdot \left( \frac{1}{R_2p} + \frac{1}{R_3p} \right)
\]

which approaches zero as \( a_o \) approaches one. Thus, the worst case of \( I_{cp}(1-a_o)/a_o \) in (V-22) occurs when \( I_{cp} \) and \( a_o \) have their minimum allowed values, which reinforces the intuitive belief that transistors having high values of \( a_o \) should be more stable in a particular circuit than transistors having lower values of \( a_o \).

The terms involving \( I_{cop} \) in (V-23) and (V-22) almost cancel leaving a small term which tends to make the inequality easier to satisfy. Setting \( I_{cop} \) equal to zero in these equations contributes a very small error in the safe direction for the worst case.

The worst case for \( I_{con} \) is the maximum value that any transistor can have at the highest temperature at which the circuit will be operated. Using the symbol \( I_{com} \) for this maximum allowed value of \( I_{co} \), equation (V-22) can be rewritten in the form of a design inequality for \( R_2 \) as

\[
R_2 \leq \frac{E_n E_8 - E_p E_5}{I_{com} \varepsilon_{12} + \varepsilon_{11} \frac{I_{cp(min)} \left( \frac{1-a_o(min)}{a_o(min)} \right)}}.
\]

Eliminating \( E_e \) from (V-16) by using (V-4) gives
\[
\left[ \frac{\frac{R_1}{a_o} (I_{cp} - I_{cop}) + E_3}{1} \right] \left( \frac{1}{R_{2n}} + \frac{1}{R_{3n}} \right) = \frac{E_c}{R_{2n}} - \frac{E_2}{R_{3n}} - I_{con} \geq 0. \quad (V-25)
\]

By selecting \( E_3 \) as the reference potential so that \( E_3 \) is zero, solving for \( R_3 \) and using the worst case of component variation, \( (V-25) \) can be written in the form of a design inequality for \( R_3 \) as

\[
R_3 \leq \frac{R_2 \varepsilon_{12}}{\varepsilon_{13}} \left[ \frac{\frac{R_4 \varepsilon_{16} \left( \frac{I_{cp}^{(\text{min})} - I_{com}}{a_o^{(\text{min})}} \right) - E_2 \varepsilon_3}{E_p \varepsilon_5}} \right. \\
\left. \left( \frac{I_{cp}^{(\text{min})} - I_{com}}{a_o^{(\text{min})}} \right) + I_{com} R_2 \varepsilon_{12} \right] 
\quad (V-26)
\]

In order to meet the condition that the impedance locking from the base of the "on" transistor into the network be large compared to the impedance locking into the base, \( R_3 \) must be greater than perhaps 5,000 ohms. On the other hand, high values of \( R_3 \) may undesirably increase the recovery time after triggering.

The value of \( E_2 \) in \( (V-26) \) is simply chosen to give a desirable value of \( R_3 \). In most cases this can be accomplished, and a power supply can be eliminated, by setting \( E_2 = E_3 = 0 \).

The choice of \( I_{cp}^{(\text{min})} \) and \( a_o^{(\text{min})} \) to be used in \( (V-24) \) and \( (V-26) \) depends on the transistor variation that must be tolerated and the required available current output of the flip-flop. \( I_{cp}^{(\text{min})} \) must of course be chosen to be less than \( I_s \) and might be from 0.5 to 0.7 of \( I_s \). As \( a_o \) changes from \( a_o^{(\text{min})} \), the minimum acceptable value of \( a_o \), to \( a_o^{(\text{max})} \), the value of \( a_o \) which results in \( I_s \), the collector current varies over its allowed range. Therefore, the greater the allowed range of collector current, the greater the tolerable range of \( a_o \) for the transistors used. Furthermore, from
(V-18), smaller values of \(a_o\) (min) result in larger tolerable ranges of \(a_o\).

It is not possible to choose arbitrarily small values of \(a_o\) (min) and \(I_{cp}\) (min) however, because smaller values for these quantities result in smaller available output currents. Thus a choice of these parameters requires a compromise between conflicting objectives. An approximate equation relating the available output current and \(a_o\) (min) and \(I_{cp}\) (min) is derived in the next section and can be used to help resolve the conflict.

It is seen from (V-17) that \(I_{cp}\) is a function of \(R_2\) and \(R_3\) so it is not possible to obtain exactly the chosen value of \(I_{cp}\) (min) and \(a_o\) (min) by satisfying the design inequalities for \(R_2\) and \(R_3\). If \(R_2\) and \(R_3\) are chosen to be as near to the equality as possible, the value of \(I_{cp}\) obtained for \(a_o\) (min) will be very close to \(I_{cp}\) (min). It is also desirable to use values near the equalities because this results in larger available output currents. The advantage of a design procedure using inequalities is that it permits the selection of standard values of resistance which is practically of much greater value than the ability to specify in advance the exact current for a given value of \(a_o\).

The Available Output Current and the Selection of \(R_1\) and \(E_1\): 

The nodal equations at the two collectors are

\[
I_n = \frac{E_1 - E_n}{R_{lp}} - \frac{E_n - E_e}{R_{2p}} - I_{con} \quad (V-27)
\]
and

\[ I_p = I_{cp} = \frac{E_n - E_p}{R_{1n}} + \frac{E_p - (E_e - 5)}{R_{2n}} \]  \hspace{1cm} (V-28)

These values of \( I_n \) and \( I_p \) will change with variations in the circuit parameters. However, there are certain values of \( I_n \) and \( I_p \), designated \( I_{nd} \) and \( I_{pd} \), which will always be exceeded regardless of allowed variation around the design values of the parameters. \( I_{nd} \) and \( I_{pd} \) are the useful output (or input) currents of the flip-flop since they can be supplied (or drawn) for all variations of the parameters within the designated tolerances.

Using the notation of (V-14), the worst case for \( I_n \) and \( I_p \) can be written

\[ I_{nd} = \frac{E_1 \epsilon_2 - E_n \epsilon_7}{R_1 \epsilon_9} - \frac{E_n \epsilon_7 - E_e(\text{min})}{R_2 \epsilon_{12}} = I_{com} \]  \hspace{1cm} (V-29)

\[ = \frac{E_1 \epsilon_2 - E_n \epsilon_7}{R_1 \epsilon_9} - \frac{1}{R_2 \epsilon_{12}} \left[ E_n \epsilon_7 - \frac{R_4 \epsilon_{16}(I_{cp(\text{min})} - I_{com})}{a_6(\text{min})} \right] = I_{com} \]

and

\[ I_{pd} = I_{cp(\text{min})} - \frac{E_1 \epsilon_1 - E_p \epsilon_6}{R_1 \epsilon_{10}} \]  \hspace{1cm} (V-30)

For stability under all allowed parameter variations, both \( I_{nd} \) and \( I_{pd} \) must be greater than zero.

An approximate solution for the sum of \( I_{nd} \) and \( I_{pd} \) obtained by setting all the \( \epsilon \)'s equal to unity, approximating \( E_n - E_e \) by \( E_n - E_p \), neglecting cut-off current terms, and using \( R_2 \) given by the equality in (V-24) is
\[
I_{nd} + I_{pd} \approx I_{cp}(\text{min}) \left( 2 - \frac{1}{a_0(\text{min})} \right) = \frac{E_n}{R_1} - \frac{E_p}{R_1}. \quad (V-31)
\]

All of the terms which have been neglected tend to reduce this sum. This equation gives some insight into appropriate values for \(I_{cp}(\text{min})\) and \(a_0(\text{min})\) and shows in particular that a flip-flop of this type cannot be made with \(a_0 < 1/2\). It also shows that the total available current is essentially independent of \(E_1\) so that it can be distributed as desired between \(I_{cd}\) and \(I_{nd}\) by varying \(E_1\) once \(R_1\) is chosen, and it shows that \(R_1\) should be large for maximum useful output current.

The transient analysis will show that the time required for the flip-flop to change states is reduced for large values of \(R_1\), hence from two points of view, \(R_1\) should be chosen to be as large as possible. The difficulty with large values of \(R_1\) is that they result in large power dissipations in \(R_1\) since \(E_1\) must also be large. This suggests the possibility of choosing \(R_1\) to be as large as possible and still dissipate no more power than a certain specified value, \(P_1\).

The maximum power dissipated in \(R_1\) is given by

\[
P_1 = \frac{(E_1 E_1 - E_p E_6)^2}{R_1 E_{10}} \quad (V-32)
\]

which can be solved for \(E_1\) to give

\[
E_1 = \frac{E_p E_6 + (P_1 R_1 E_{10})^{1/2}}{E_1} \quad (V-33)
\]

Substituting this value of \(E_1\) into \((V-29)\) and solving for \(R_1\) yields
\[ R_1 = \frac{N_3 - 2N_1 N_2 + N_3 (1 - \frac{4N_1 N_2}{N_3})^{1/2}}{2N_1^2} \]  

(V-34)

where

\[ N_1 = \left[ I_{\text{ind}} + I_{\text{com}} + \frac{E_1 E_7 - E_2 (\text{min})}{R_2 E_{12}} \right] E_9 \]

\[ N_2 = E_1 E_7 - E_p \frac{E_6 E_2}{E_1} \]  

(V-35)

\[ N_3 = \left( \frac{E_2}{E_1} \right)^2 E_{10} P_1. \]

Similarly, substituting (V-33) into (V-30) gives

\[ R_1 = \frac{P_1}{E_{10} (I_{\text{cp}} (\text{min}) - I_{\text{ed}})^2}. \]  

(V-36)

The value of \( R_1 \) obtained from (V-34) or (V-36) will not in general be a standard value of resistance. If the next lower standard value of resistance is chosen and the appropriate value of \( E_1 \) is calculated from (V-29) or (V-30) the resulting dissipation in \( R_1 \) will be less than \( P_1 \).

The specification of the maximum power to be dissipated gives one relation between \( R_1 \) and \( E_1 \). It is therefore no longer possible to specify both \( I_{\text{ind}} \) and \( I_{\text{pd}} \) and solve (V-29) and (V-30) for \( R_1 \) and \( E_1 \). If the maximum power is not specified, it will be found that the condition for physical realizability on \( R_1 \), that it be positive, will limit the permissible choices of \( I_{\text{ind}} \) and \( I_{\text{pd}} \) to values such that their sum is appreciably less than \( I_{\text{cp}} (\text{min}) \). Moreover, if either \( I_{\text{ind}} \) or \( I_{\text{pd}} \) were chosen, it would be found that larger values of the other current within the permissible range.
went with larger values of $R_1$ and with increasing dissipation in $R_1$. By specifying the maximum power dissipation, it is possible to select either $I_{cd}$ or $I_{nd}$ and the maximum power, secure in the knowledge that the other current will have its maximum value consistent with the specified power dissipation.

With this approach, the condition for physical realizability of $R_1$ is revealed in equation (V-34) for since $R_1$ must be real,

$$\frac{l_1 N_1 N_2}{N_3} < 1.$$  \hspace{1cm} (V-37)

Since $I_{nd} \geq 0$, the most favorable case occurs with $I_{nd} = 0$ so that flip-flop operation is possible if

$$P_1 \geq \frac{l_1 E_2 E_1^2}{E_{10} E_{20}^2} \left[ E_n E_7 - \frac{E_p E_6 E_2}{E_1} \right] \left[ I_{com} + \frac{E_n E_7 - E_6(\min)}{R_2 E_{12}} \right].$$  \hspace{1cm} (V-38)

Any larger value of power dissipation can be chosen and flip-flop operation will be possible. The value of $P_1$ which should be chosen depends on the overall design objectives and must be left to the discretion of the circuit designer.

The choice of $I_{pd}$ or $I_{nd}$ as the current to specify depends on the load which the flip-flop is to drive. If the loading is to be primarily to positive potentials, $I_{nd}$ is specified to be a small current which allows the remainder of the available current to appear as $I_{pd}$, the useful current in this case. Conversely, if the loading is to be primarily to negative potentials, $I_{pd}$ is specified as a small current so that the remainder of the available current will appear as $I_{nd}$, the useful current in this case.
Sample Design of a Symmetric Junction Transistor Flip-Flop:

The preceding theory has provided enough information to complete the static design of a symmetric junction transistor flip-flop. As an illustration of the application of this theory to a practical design problem, a sample design will be calculated based on the following assumptions:

1. The transistors to be used are n-p-n diffused junction transistors having a peak collector voltage rating of 30 volts, a collector dissipation rating of 40 milliwatts, and negligible cut-off current at room temperature.

2. The output voltage swing should be 10 volts and the available output current should be as large as possible.

3. The flip-flop should be required to operate at room temperature only, but it should tolerate 5% changes in the resistance values and 10% changes in the supply voltages.

The saturation value of the collector current for this design is taken to be \( I_m \) given by (V-6)

\[
I_s = I_m = \frac{h_P}{E_n} = \frac{h \times 0.04}{10} = 0.16 \text{ AMP} . \tag{V-39}
\]

Since the transistors used are the diffused junction type, \( R_f \) can be taken to be zero in (V-13). The value of \( K_p \) which is chosen is 0.7. The resulting value of \( R_i \) is

\[
R_i = \frac{h \times 0.7 \times 0.04}{0.16^2} = 436 \text{ ohms}. \tag{V-40}
\]
The next smaller standard value of resistance is \(430\) ohms, so this is chosen as the design value.

\(E_3\) is chosen to be zero, and \(E_p\) computed from (V-11) as

\[E_p = I_s R_4 = 0.016 \times 430 = 6.9 \text{ volts.} \tag{V-41}\]

Seven volts is used as the design value since this results in a negligible change in the saturation current. To get the 10 volt swing, \(E_c\) is therefore 17 volts.

Because of the specified tolerances on the resistors and supply voltages,

\[\begin{align*}
E_1 &= E_3 = E_5 = E_7 = 1.01 \\
E_2 &= E_4 = E_6 = E_8 = 0.9 \\
E_9 &= E_{11} = E_{13} = E_{15} = 1.05 \\
E_{10} &= E_{12} = E_{14} = E_{16} = 0.95
\end{align*} \tag{V-42}\]

It is now necessary to select an approximate value of \(I_{cp}(\text{min})\) and a value of \(a_c(\text{min})\). The value of \(I_{cp}(\text{min})\) must be appreciably below \(I_s\) to allow a practical range of values of \(a_c\).

For this design \(I_{cp}(\text{min})\) is chosen to be 0.01 amperes, and \(a_c(\text{min})\) is chosen to be 0.95. The choice must be conditioned by the available transistors and the desired output current.

The value of \(R_2\) can now be calculated from (V-24) as

\[R_2 = \frac{E_{11} E_8 - E_p E_5}{E_{11} I_{cp}(\text{min})} \frac{a_c(\text{min})}{1 - a_c(\text{min})} \tag{V-43}\]

\[= \frac{(17 \times 0.9 - 7 \times 1.1) 	imes 0.95}{1.05 \times 0.01 \times 0.05} = 1375 \times 10^3 \text{ ohms.}\]
The next smaller standard value of resistance, 13,000 ohms, is chosen as the design value.

Setting \( E_2 \) equal to zero permits the value of \( R_3 \) to be calculated from (V-26) as

\[
R_3 = \frac{R_2 \varepsilon_{12}}{\varepsilon_{13}} \left[ \frac{R_4 \varepsilon_{16}}{E_{cp}(min)} \frac{I_{cp}(min)}{a_0} = \frac{E_p \varepsilon_{15} - R_4 \varepsilon_{16}}{a_0} \right]
\] (V-44)

\[
= \frac{13 \times 10^3 \times 0.95}{1.05} \frac{430 \times 0.95 \times 0.01}{0.95} = 14.85 \times 10^3
\]

Again, the next smaller standard value of resistance, 13,000 ohms, is chosen as the design value.

Using an approximate expression for \( P_1 \) in (V-38)

\[
P_1 \geq \frac{4(E_n - E_p)^2}{R_2} = \frac{4 \times 10^2}{13 \times 10^3} = 0.0308 \text{ watts.}
\] (V-45)

It is apparent that flip-flop action will be possible if appreciably more than 0.03 watts are dissipated in \( R_1 \). For this design, \( P_1 \) is chosen to be 0.25 watts. This is a convenient value because it permits the use of half-watt resistors derated by fifty percent, a practice which is common in the digital computing field.

For the kind of gate circuits which would ordinarily be used with this flip-flop, it is desirable to have most of the available current appear as \( I_{pd} \). Therefore, \( I_{nd} \) is specified as 0.001 amperes and an approximate value of \( R_1 \) is computed from (V-34) using (V-35) and (V-4).
\[ E_e(\text{min}) \approx \frac{R_i}{a_0(\text{min})} \frac{\varepsilon_16 I_{cp}(\text{min})}{E_{n7}} = \frac{430 \times 0.95 \times 0.01}{0.95} = 4.3 \quad (V-46) \]

\[ N_1 = I_{nd} \varepsilon_9 + \varepsilon_9 \frac{E_{n7} - E_e(\text{min})}{E_{p12}} = 0.001 \times 1.05 + 1.05 \frac{17 \times 1.1 - 4.3}{13 \times 10^3 \times 0.95} = 2.273 \times 10^{-3} \quad (V-47) \]

\[ N_2 = E_{n\varepsilon_9} - F_p \frac{\varepsilon_6 \varepsilon_2}{\varepsilon_1} = 17 \times 1.1 - \frac{7 \times 0.9 \times 0.9}{1.1} = 13.54 \quad (V-48) \]

\[ N_3 = \left( \frac{\varepsilon_2}{\varepsilon_1} \right)^2 \varepsilon_10 P_1 = (1.1)^2 \times 0.95 \times 0.25 = 0.159 \quad (V-49) \]

\[ N_3 = 2N_1 N_2 + N_3 \left( 1 - \frac{1}{1.54} \right)^{1/2} \]

\[ R_1 = \frac{0.159 - 2 \times 2.273 \times 10^{-3} \times 13.54 + 0.159 \left( 1 - \frac{4 \times 2.273 \times 10^{-3} \times 13.54}{0.159} \right)^{1/2}}{2 \times (2.273 \times 10^{-3})^2} \]

\[ = 16.65 \times 10^3 \text{ ohms.} \]

The next smaller standard value of resistance, 16,000 ohms is chosen as the design value.

Solving (V-29) for \( E_1 \) and substituting into the resulting expression gives

\[ E_1 = \frac{1}{\varepsilon_2} \left[ I_{nd} R_1 \varepsilon_9 + \frac{R_1 \varepsilon_9}{R_2 \varepsilon_{12}} (E_{n\varepsilon_9} - E_e(\text{min}) + E_n \varepsilon_9) \right] \]

\[ = \frac{1}{0.9} \left[ 0.001 \times 16 \times 10^3 \times 1.05 + \frac{16 \times 1.05}{13 \times 0.95} (17 \times 1.1 - 4.3) + 17 \times 1.1 \right] \]

\[ = 61.4 \text{ volts.} \quad (V-51) \]

The value of \( I_{pd} \) is obtained by substituting into (V-30) as
\[ I_{pd} = I_{cp\text{ (min)}} = \frac{E_1 E_1 - E_p E_6}{R_1 E_0} \quad (V-52) \]

\[ = 0.01 - \frac{61.4 \times 10^3}{16 \times 10^3 \times 0.95} = 0.00596 \text{ AMP} \]

The value of \( a_o \) which will give the saturation value of current can be computed by solving (V-17) for \( a_o \) and using the tolerance notation to write the worst case as

\[ I_s - I_{com} \left( \frac{R_4 \cdot R_2 E_2 E_1}{R_2 \cdot R_3 E_1} + 1 \right) \]

\[ a_o(\text{max}) = \frac{E_n E_7 + E_2 E_3 + I_s \left[ 1 - R_4 E_6 \left( \frac{1}{R_2 E_2} + \frac{1}{R_3 E_3} \right) \right]}{R_2 E_2 + R_3 E_3} \quad (V-53) \]

\[ = \frac{0.016}{1.7 \times 10^3 \times 0.95} = 0.974 \]

This completes the static design of the flip-flop which will supply a load current of 1 ma. at 7 volts when loaded to a negative potential and will absorb a current of 5.96 ma. at 17 volts when loaded to positive potentials if the transistors used have values of \( a_o \) less than 0.974 and greater than 0.95 for any possible variation of the resistors within 5\% of the design values and any possible variation of the supply voltages within 10\% of the design values. The flip-flop will be stable for higher values of \( a_o \), but the transistors will be saturated in the "on" state and will become progressively harder to trigger as \( a_o \) increases. The unloaded flip-flop will be stable for smaller values of \( a_o \), but it will no longer be able to absorb the design value of load current.

The nominal values of the resistors are \( R_1 = 16,000 \text{ ohms} \),
\[ R_2 = R_3 = 13,000 \text{ ohms, and } R_4 = 430 \text{ ohms.} \] The nominal values of the supply voltages are \( E_1 = 61.4 \text{ volts, } E_2 = E_3 = 0, E_p = 7 \text{ volts, and } E_n = 17 \text{ volts.} \)

Transient considerations which govern the selection of the remainder of the parameters of the flip-flop will be discussed in detail in part VI.
VI TRANSIENT CONSIDERATIONS IN THE DESIGN OF
SYMMETRIC JUNCTION TRANSISTOR FLIP-FLOPS

The transient analysis of flip-flop behavior makes it possible
to complete the specification of the parameters of the flip-flop and
to determine the triggering requirements and flipping times or per-
haps output waveshapes. An additional, and perhaps even more important
result, is that sufficient insight into the practical problem of select-
ing transistors for use in high speed flip-flop circuits can be gained
to permit satisfactory criteria for transistor selection to be
established.

For the transient analysis of the behavior of the flip-flop cir-
cuit after triggering, it is desirable to consider the case where
the flip-flop is used to drive a capacitive load to ground. Any
resistive load can be considered to be in parallel with the load
resistor $R_1$ and therefore simply changes its numerical value and
the value of the potential to which it returns. In practical cir-
cuits, the load is often a diode gating network so it is not
necessarily true that the load is the same for positive going
signals as for negative going signals. Furthermore, the two output
loads are not necessarily balanced. For design purposes, it is suf-
ficient to choose the circuit constants for satisfactory operation
with the maximum anticipated value of load capacity since the circuit
always performs better with smaller values of load capacity.

It is unnecessary to complicate the transient analysis by in-
cluding the effect of tolerances on the components since the
transient performance of the flip-flop is not critically sensitive
to small variations in the parameters which are selected on the
basis of the transient analysis. However, for detailed accurate
prediction of the behavior of a particular circuit, it may be
necessary to make calculations based on the values of the components
in that particular circuit.

Notation:

The transistor which is initially conducting is denoted by \( T_p \)
and the transistor which is initially non-conducting is denoted by
\( T_n \). The subscripts \( p \) and \( n \) will be used generally to refer to
quantities which are related to these transistors. Thus, \( C_{cp} \) is
the collector capacity of \( T_p \), \( C_{Ln} \) is the load capacity on the
collector of \( T_n \), etc.

It is necessary to consider a number of different operating
regions for each of the transistors in the flip-flop. A region is
characterized by the fact that a particular set of equations may
be used to describe the behavior of a transistor in a given region.
When the transistor enters a new region, the equations describing
its behavior must be changed. A complete solution to the transient
problem is found by finding solutions in each of the operating re-
gions and matching boundary conditions.

The rising waveform at the collector of \( T_p \) is analyzed in
three operating regions. Region 1 starts with the trigger pulse
and terminates when the base of \( T_n \) starts to conduct. Region 2
starts when the base of \( T_n \) starts to conduct and terminates when
the collector voltage of \( T_p \) rises to \( E_n \). Region 3 starts when
the collector voltage of \( T_p \) rises to \( E_n \) and continues indefinitely.

The falling waveform at the collector of \( T_n \) is analyzed on the basis of four operating regions. Region A starts with the trigger pulse and terminates when the base of \( T_n \) starts to conduct. Region A is identical in time with region 1. Region B starts when the base of \( T_n \) starts to conduct and terminates when the collector current of \( T_n \) becomes equal to the clamp current \( I_n \). Region C starts when the collector current of \( T_n \) becomes equal to \( I_n \) and terminates when the collector voltage of \( T_n \) becomes equal to \( E_p \). Region D starts when the collector voltage of \( T_n \) becomes equal to \( E_p \) and continues indefinitely.

Regions B and C must be further divided into sub-regions which depend on the region of operation of the collector of \( T_c \). Thus, regions B2, B3, C2, and C3 are possible operating regions for the collector of \( T_n \) depending on the operating region of the collector of \( T_p \). Not all of these sub-regions are possible in one flipping sequence since as time passes the operating region must progress in numeric or alphabetic sequence. The most common sequence of operating regions for the collector of \( T_n \) is A, B2, C2, C3, D. The only other possible sequences are A, B2, B3, C3, D; A, B2, C3, D; and A, B2, C2, D. It is not necessary to consider sub-regions in region D because the transient is effectively over when region D has been entered.

The time of arrival of the trigger impulse is taken to be \( t = 0 \). The time at the end of a region is denoted by \( t \) with the subscript of that region. Thus the time at the end of region 2 is \( t_2 \), the
time at the end of region C3 is \( t_{C3} \), etc. In addition, it is convenient to have a time variable which is zero at the start of a particular region and has a final value equal to the time spent in that region. The symbol \( \tau \) is used for this purpose with a subscript which designates the particular region of operation. The symbol \( \tau' \) is used to denote the final value of \( \tau \) in a given region and therefore the time spent in that region. Thus, time in region B2 which starts from zero at the start of region B2, is denoted by \( \tau_{B2} \), and the total time spent in region B2 is \( \tau'_{B2} \).

**Calculation of the Rise Time:**

To initiate the flipping action, the negative trigger pulse is applied to the base of \( T_p \), the transistor which is initially conducting. The combined effect of the trigger pulse and of the signal coupled from the collector of \( T_n \) by \( R_2 \) and \( C_1 \) as \( T_n \) turns on is to turn \( T_p \) off almost instantaneously and keep it off.

The "off" transistor appears very much like two back biased diodes, one between the collector and base and the other between the base and the emitter. If the base had no signal on it during the collector rise, the effect of the cut-off transistor in its collector circuit could be represented by connecting \( C_{cp} \) to ground (\( r_{cp} \) is ordinarily negligibly large). Actually, a negative going signal appears on the base which depends on the magnitude of the trigger signal, the circuit constants, and the characteristics of the other transistor. Since transistor action has ceased, the coupling through \( C_{cp} \) and \( r_{cp} \) is the only coupling between the base
and collector of $T_p$.

Any attempt to account for the effect of the base signal analytically results in a great complication of the transient analysis. It therefore appears attractive to examine the errors which would arise if the effect of the cut-off transistor were approximated by a capacity $C_{cp}$ to ground. The effect of base voltage variations in this case could be included by letting $C_{cp}$ be $C_{cp}' = C_{cp}(1 - \frac{dE_b}{dE_c}/\frac{dE_c}{dt})$ where $\frac{dE_b}{dt}$ is the rate of change of base voltage and $\frac{dE_c}{dt}$ is the rate of change of collector voltage. The rate of change of base voltage might be of the same order as the rate of change of collector voltage so a rather large error in $C_{cp}$ occurs by omitting this term. There are two reasons why this error can be ignored. The first is that the rate of change of the base voltage is ordinarily positive immediately after the trigger signal and negative after the other transistor starts to change its state so there is some tendency for the errors to average out over a flipping cycle. The second is that $C_{cp}$ is in parallel with $C_{lp}$ and $C_{lp}$ both of which are ordinarily much larger than $C_{cp}$. Therefore, relatively large errors in $C_{cp}$ do not cause significant errors in the total shunt capacity.

It has been assumed here that $C_{ji}$ is so large that the emitter can be considered to be at signal ground. This is the condition for the selection of $C_{ji}$. It is also desirable to keep the time constant $C_{ji}R_{ji}$ small enough so that steady state conditions are reached in the minimum interval between triggering pulses in the
event that the transistors in the flip-flop are not balanced. The performance of the flip-flop is not critically dependent on the value of $C_4$.

Region I:

Initially, transistor $T_p$ acts as a delay line. The input pulse is applied, and nothing happens at the output for a short time of the order of 0.05 microseconds. This is also the order of the fall time of the pulses used for triggering and so is difficult to measure accurately. Fortunately, for all practical applications of transistors to flip-flop circuits, the delay time is small compared to the total rise or fall time and therefore can be neglected without contributing appreciable error to the solution.

In the first region, the base of $T_n$ has not yet begun to conduct and therefore presents a high input impedance which is just that of the back biased emitter and collector junctions to signal ground. The resistive component of this impedance is ordinarily negligibly large; but the capacitive component $C_{bn}$ should be included.

Since the collector voltage of $T_p$ is initially clamped to $E_p$, the circuit of fig. VI-1 can be used as a transient equivalent circuit for determining $E_p$, the transient collector voltage of $T_p$, during the first region. It is desired to find the transient resulting when switch $S$ is opened.

The first region of operation is terminated when the base of $T_n$ starts to conduct. The voltage change of the base of $T_n$
between the conducting and the non-conducting states is designated by the symbol $\delta$. One of the design conditions for stable operation was that $\delta$ be greater than zero for all allowed variations in the circuit elements and the supply voltages. Since $\delta$ is a cushion to absorb the effect of the tolerances in the components, it is different from flip-flop to flip-flop even though the nominal values of the circuit elements are the same. For accurate calculation of the time spent in region 1, $\delta$ must be measured for the particular circuit, or calculated from the measured (as opposed to the nominal) values of the components in the particular circuit.

For the short time spent in region 1, it is possible to make the simplifying assumption that $C_L$ and $C_{bn}$ do not discharge appreciably through their shunting resistors. Therefore, if $\delta_p$ is the change in collector voltage which corresponds to a change $\delta$ at the base, we have

$$\delta_p = \delta \frac{C_L + C_{bn}}{C_L}.$$  \hspace{1cm} (VI-1)

Even though $\delta_p$ is variable, it is always a small part of the possible change of $E_v$. Therefore, it is reasonable to assume that the whole of region 1 is contained in the initial linear part of the charging transient.

The initial current into the output node is just

$$I_{R_1} = \frac{E_1 - E_p}{R_1} - \frac{E_p}{R_2 + R_3}.$$  \hspace{1cm} (VI-2)

and the effective capacity to ground is the sum of $C_{np}$, $C_{lp}$, and
the series combination of $C_1$ and $C_{bn}$. Since the initial rate of change of the output voltage is essentially constant in region 1, the time required for the output voltage to change $\delta_p$ volts, which is the time spent in region 1, is

$$\tau_1^* = \delta_p \left( \frac{C_{cp} + C_{Lp}}{C_1 + C_{bn}} \right) \frac{1}{I_{R_1}}. \quad (VI-3)$$

The approximations involved in deriving this expression for $\tau_1^*$, while they may contribute appreciable error to the solution for $\tau_1^*$, do not result in significant errors in the total rise time because $\tau_1^*$ is a relatively small fraction of the total rise time.

Region 2:

When the base of $T_n$ starts to conduct, the circuit enters region 2. In this region, the base of $T_n$ is effectively clamped to $E_c$ so the equivalent circuit for determining the transient voltage rise in region 2 becomes that of fig. VI-2. By making the indicated substitutions, this circuit can be further simplified to that of fig. VI-3.

The circuit is a simple charging circuit so the voltage on the condenser at time $\tau_2$ after the switch is opened is given by

$$E_x = E_p + \delta_p + (E_x - E_p - \delta_p) \left[ 1 - \exp\left(-\frac{\tau_2}{R_r C_r}\right) \right] \quad (VI-4)$$

where

$$E_0 = \frac{E_e R_1 + E_1 R_2}{R_1 + R_2} = \left( \frac{E_e}{R_2} + \frac{E_1}{R_1} \right) R_r \quad (VI-5)$$

$$R_r = \frac{R_1 R_2}{R_1 + R_2}, \quad C_r = C_{1p} + C_{cp} + C_{Lp}.$$
The quantity of principal interest is \( \tau_2 \), the time required for the voltage to rise to \( E_n \). This is obtained by solving (VI-4) as

\[
\tau_2 = R_C C_T \log_e \left( \frac{E_T - E_C - \delta_p}{E_0 - E_n} \right). \tag{VI-6}
\]

Region 3:

Region 3 of the rising waveform starts when \( E_T = E_n \) and continues indefinitely with no change in the collector potential.

The Influence of Circuit Parameters on the Rise Time:

It is apparent from (VI-6) that the rise time is essentially independent of the transistor parameters with the exception of the collector capacity of \( T_p \). The emitter voltage of course, is dependent on the value of \( a_0 \), but the dependence is quite small.

The rise time increases with \( C_1 \), but it will be shown that substantial values of \( C_1 \) are nevertheless desirable.

The rise time is dependent on the value of \( R_2 \) in a very complicated way since \( R_2 \) enters in both \( R_T \) and \( E_T \). However, \( E_e/R_2 \) is ordinarily a small term compared with \( E_T/R_1 \). If it could be neglected, the circuit would charge to a final value that varied with \( R_2 \) starting with an initial slope which was independent of \( R_2 \). Thus, lowering \( R_2 \) would increase the rise time.

The effect of the \( E_e/R_2 \) term is to tend to decrease the rise time as \( R_2 \) is lowered \( (E_e \) increases when \( R_2 \) is decreased), but the first effect usually predominates although the sensitivity of the rise time to variations in \( R_2 \) is not great.

Since the value of \( R_2 \) is specified from static considerations, the circuit designer has little opportunity to improve the rise time.
by varying $R_2$. However, he has great latitude in choosing $R_1$ and $E_1$, so it is of more practical value to find the effect of these parameters on the rise time. From equation (VI-4) it is apparent that increasing $E_1$ increases the final voltage, $E_0$, and decreasing $R_1$ increases the final voltage and reduces the time constant. Therefore, both increasing $E_1$ and reducing $R_1$ tend to reduce the rise time.

The static analysis showed that the available useful current from the flip-flop is increased when $R_1$ is increased. It is necessary to increase $E_1$ at the same time so that the ratio $E_1/R_1$ remains approximately constant if it is desired to preserve the original current distribution (approximately) between the two clamp diodes. From (VI-5), if the ratio $E_1/R_1$ remains constant, the ratio $E_0/R_T$ will also remain constant.

The initial rate of change of $E_T$ is given by

$$\frac{dE_T}{dt} \bigg|_{T_2=0} = \frac{E_0 - E_2}{R_T C_T} = \frac{1}{C_T} \frac{E_0 - E_2}{R_T} = \frac{E_0 + \delta E}{R_T}. \quad \text{(VI-7)}$$

Since $E_0/R_T$ is constant, the slope increases with $R_T$. Therefore, both the final value and the initial slope are increased, and the rise time is reduced, by increasing $R_1$ and maintaining $E_1/R_1$ constant.

The limiting value of slope which can be obtained in this way is

$$\lim_{R_1 \to \infty} \frac{1}{C_T} \frac{E_0}{R_T} = \frac{E_0 + \delta E}{R_T} = \frac{1}{C_T} \left( \frac{E_1}{R_1} - \frac{E_0 + \delta E - E_2}{R_2} \right). \quad \text{(VI-8)}$$
Calculation of the Fall Time:

The transient equivalent circuit for obtaining $E_r$, the falling waveform at the collector of $T_n$ is given in fig.VI-4. Transistor $T_p$ was turned off by the trigger pulse so the input impedance to its base is again approximated by a capacity $C_{bp}$. The triggering components do not enter the circuit since they have been removed by back biasing of the trigger diode.

For many purposes, this equivalent circuit is unnecessarily complicated. The analysis is appreciably simplified and, since the falling waveform is not extremely sensitive to loading, the error is not excessive if it is assumed that the time constants are such that $C_{ln}$ maintains a constant charge during the time when $T_n$ is turning on. This allows $C_{ln}$ and $R_2$ to be replaced by an equivalent battery and reduces the a.c. load on $T_n$ in region C to a single parallel resistor and capacitor made up of a resistance equal to the parallel combination of $R_1$ and $R_3$ and a condenser equal to the sum of $C_{ln}$ and $C_{bp}$. This simplified equivalent circuit is given in fig.VI-5.

Region A:
Region A occurs before the base of $T_n$ starts to conduct and is identical in time with region l. There is no appreciable change in $T_n$ in region A.

Region B:
Region B starts when the base of $T_n$ starts to conduct and terminates when $I_{cm} = I_n$. During this interval, the collector load impedance of $T_n$ is the forward resistance of a diode and is
therefore very low. The Laplace transform of the collector current from (II-35) is therefore

\[ I_{cn}(s) = \frac{I_{bn}(s) \cdot a_{on} \cdot \omega_{on} \cdot I_c(\tau = 0)}{s + \omega_{on}(1 - a_{on})}. \] (VI-9)

The initial condition on \( I_{cn} \) is necessary because region B must be divided into sub-regions to account for the discontinuity in the base current between regions 2 and 3.

The current into the base of \( T_n \) during region 2 is

\[ I_{bnB2} = \frac{E_r}{C_1} + \frac{E_r - E_e}{R_2} = \frac{E_e}{R_3}. \] (VI-10)

Substituting \( E_r \) from (VI-4) into this expression gives

\[ I_{bnB2} = D_1 + D_2 e^{-\frac{\tau_2}{R_1 C_r}} \] (VI-11)

where

\[ D_1 = \frac{E_o}{R_2} - E_e \left( \frac{1}{R_2} + \frac{1}{R_3} \right) \] (VI-12)

\[ D_2 = \frac{C_1}{R_r C_r} - \frac{1}{R_2} \left( E_o - E_p - \delta_p \right). \]

At the end of region 2, the current in the base drops abruptly to the steady state value

\[ I_{bn3} = \frac{E_n}{R_2} - E_e \left( \frac{1}{R_2} + \frac{1}{R_3} \right). \] (VI-13)

The Laplace transform of the output current in region B2 is obtained by substituting (VI-11) into VI-9) as
\[ I_{cnB2} = \frac{s + \frac{D_1}{(D_1 + D_2)R_C C_r}}{s(s + \frac{1}{R_C C_r})[s + \omega_{on}(1 - a_{on})]} \]  \hspace{1cm} (VI-14)

The inverse transform of this can be written as

\[ I_{cnB2}(\tau_{B2}) = \frac{a_{on} D_1}{1 - a_{on}} + \frac{a_{on} \omega_{on} D_2 R_C C_r}{\omega_{on}(1 - a_{on})R_C C_r} \times \frac{e^{-\frac{\tau_{B2}}{R_C C_r}}}{1}
+ \frac{a_{on} \omega_{on}(1 - a_{on})(D_1 + D_2)R_C C_r}{\omega_{on}(1 - a_{on})R_C C_r - 1} \times e^{-\omega_{on}(1 - a_{on})\tau_{B2}}. \hspace{1cm} (VI-15)\]

To put this in more tractable form, let

\[ x = \frac{1}{R_C C_r} \]
\[ \omega_{on}(1 - a_{on}) = ux \hspace{1cm} (VI-16)\]
\[ D_2 = m D_1. \]

Substituting these values into (VI-15) gives

\[ I_{cnB2}(\tau_{B2}) = \frac{a_{on} D_1}{1 - a_{on}} \left[ 1 + \frac{u}{u - 1} \right] \times e^{-x \tau_{B2}} = (1 + \frac{u}{u - 1}) \times e^{ux \tau_{B2}}. \hspace{1cm} (VI-17)\]

For almost all cases of interest, both \( x \tau_{B2} \) and \( ux \tau_{B2} \) are much less than 1; so adequate accuracy is obtained by expanding the exponential terms of (VI-17) and keeping only the first two terms of each series. Doing this yields

\[ \frac{I_{cnB2}(1 - a_{on})}{a_{on} D_1} = u(1 + m) x \tau_{B2}. \hspace{1cm} (VI-18)\]

If region 2 lasts long enough for the collector current to build up to \( I_n \), equation (VI-18) can be solved for \( \tau'_{B2} \) as

\[ \tau'_{B2} = \frac{I_n(1 - a_{on})}{a_{on} D_1 x u(1 + m)} = \frac{I_n}{a_{on} \omega_{on}(D_1 + D_2)}. \hspace{1cm} (VI-19)\]
If it is desirable to find \( \tau^i_{B2} \) more accurately, the value obtained from (VI-19) can be used as an approximate solution and a better value computed by Newton's method. To apply this method, let \( \tau^{(n)}_{B2} \) be the \( n \)th approximation to \( \tau^i_{B2} \). Then the next approximation is

\[
\tau^{(n+1)}_{B2} = \tau^{(n)}_{B2} - \frac{F(\tau^{(n)}_{B2})}{F'(\tau^{(n)}_{B2})}. \tag{VI-20}
\]

where

\[
F(\tau^{(n)}_{B2}) = \frac{a_{on}D_1}{1-s_{on}} \left[ 1 + \frac{um}{u-1} e^{-x\tau^{(n)}_{B2}} - (1 + \frac{um}{n-1}) e^{-ux\tau^{(n)}_{B2}} \right] - I_n \tag{VI-21}
\]

\[
F'(\tau^{(n)}_{B2}) = \frac{a_{on}D_1}{1-s_{on}} \left[ -\frac{xum}{u-1} e^{-x\tau^{(n)}_{B2}} + ux(1 + \frac{um}{u-1}) e^{-ux\tau^{(n)}_{B2}} \right]. \tag{VI-22}
\]

In the event that region 2 does not last long enough for the collector current to build up to \( I_{cn} \), the value of \( I_{cn}(\tau^i_2) \) is computed by setting \( \tau_{B2} = \tau^i_2 \) in (VI-17). This value is the initial condition on \( I_c \) in region B3.

In region B3, the transform of the collector current of \( T_n \) is then

\[
I_{cnB3}(s) = \frac{I_{bn3} s_{on} \omega_{on} + I_{cn}(\tau^i_2)}{s + \omega_{on}(1-s_{on})} = \frac{I_{cn}(\tau^i_2)}{s} \frac{s + I_{bn3} s_{on} \omega_{on}}{s [s + \omega_{on}(1-s_{on})]} \tag{VI-23}
\]

and the collector current is the inverse transform,
\[
I_{en}(\tau_{B3}) = \frac{I_{bn3} a_{on}}{1 - a_{on}} \left[ \frac{I_{bn3} a_{on}}{1 - a_{on}} = I_{en}(\tau'_{B3}) \right] e^{\omega_{on}(1 - a_{on}) \tau_{B3}}. \quad (VI-24)
\]

This can be solved for \(\tau'_{B3}\), the value of \(\tau_{B3}\) which makes
\[
I_{en}(\tau_{B3}) = I_n \quad \text{to give}
\]
\[
\tau'_{B3} = \frac{1}{\omega_o (1 - a)} \log \left\{ \frac{I_{bn3} a_{on} - I_{en}(\tau'_{B3})(1 - a_{on})}{I_{bn3} a_{on} - I_n (1 - a_{on})} \right\}. \quad (VI-25)
\]

**Region C:**

In region C, the collector of \(T_n\) is no longer clamped to \(E_n\).

From (II-25), the transfer impedance is
\[
Z_T(s) = \frac{s a_{on} \omega_{on}}{C_f + C_{cn}} \frac{1}{s^2 + \frac{s}{R_f(C_f + C_{cn})} (1 + R_f[C_{cn} + C_f(1 - a_{on})] + \frac{\omega_{on}(1 - a_{on})}{R_f(C_f + C_{cn})}}. \quad (VI-26)
\]

where
\[
R_f = \frac{R_1 R_3}{R_1 + R_3}, \quad (VI-27)
\]
and
\[
C_f = C_{Ln} + C_{bp} \quad (VI-28)
\]

which can be written as
\[
Z_T(s) = \frac{-a_{on} \omega_{on}}{C_f + C_{cn}} \frac{1}{(s + \alpha)(s + \gamma)}. \quad (VI-29)
\]

where
\[
\alpha = \frac{1 + R_f \omega_{on} [C_{cn} + C_f(1 - a_{on})]}{2 R_f(C_f + C_{cn})} \left\{ 1 + \left[ \frac{\omega_{on}(1 - a_{on}) R_f(C_f + C_{cn})}{1 + R_f \omega_{on} [C_{cn} + C_f(1 - a_{on})]} \right]^2 \right\}^{1/2} \quad (VI-30)
\]

and
\[ \gamma = \frac{1 + R_f \omega_{on} [C_{cn} + C_f (1 - a_{on})]}{2 R_f (C_f + C_{cn})} \left\{ 1 - \left[ 1 - \frac{\omega_{on} (1 - a_{on}) R_f (C_f + C_{cn})}{1 + R_f \omega_{on} [C_{cn} + C_f (1 - a_{on})]} \right]^{\frac{1}{2}} \right\} \]

(VI-31)

The second term under the radical is always much less than 1, so for practical computation, it is usually desirable to expand the square root and keep only the first two terms of the expansion. The approximate values of the roots obtained by this process are

\[ \gamma \approx \frac{\omega_{on} (1 - a_{cn})}{1 + R_f \omega_{on} [C_{cn} + C_f (1 - a_{on})]} \quad \text{(VI-32)} \]

\[ \alpha \approx \frac{1 + R_f \omega_{on} [C_{cn} + C_f (1 - a_{on})]}{R_f (C_f + C_{cn})} - \gamma \quad \text{(VI-33)} \]

In region C, the base current is given by (VI-11) as

\[ I_{bc2} = D_1 + D_2 e^{-\frac{\tau_B}{R_f C_r}} = D_1 + D_2 e^{-\frac{\tau_B}{R_f C_r}} \]

\[ = D_1 + D_2 e^{-\frac{\tau_B}{R_f C_r}} \quad \text{for } \tau_B + \tau_C \leq \tau_2' \text{ (region C2)} \]

and by (VI-13) for \( \tau_B + \tau_C > \tau_2' \text{ (region C3)} \).

The Laplace transform of (VI-3h) is

\[ I_{bc2}(s) = \frac{D_1}{s + \frac{R_f C_r}{D_1 + D_2 e^{-\frac{\tau_B}{R_f C_r}}}} \quad \text{(VI-35)} \]

If

\[ D_2 e^{-\frac{\tau_B}{R_f C_r}} = m_2 D_1 \quad \text{(VI-36)} \]

(VI-35) can be written
\[ I_{bC2}(s) = \frac{D_1(1+m_2)(s + \frac{x}{1+m_2})}{s(s + x)}. \] (VI-37)

The transform of the change in collector voltage at \( T_n \) can be written as the product of the transfer impedance and the transform of the base current. If this change in collector voltage is denoted by \( \Delta E_C \), the output voltage is

\[ E_C = \Delta E_C + E_n. \] (VI-38)

In region C2, both the initial value and the initial rate of change of \( \Delta E_C \) are zero so the transform of \( \Delta E_C \) is

\[ \Delta E_{FC2}(s) = I_{bC2}(s) Z_T(s) = \frac{-s \omega \omega_{on} D_1(1+m_2)(s + \frac{x}{1+m_2})}{(C_f + C_n) s(s + x)(s + a)(s + y)}. \] (VI-39)

The inverse transform of this is

\[ \Delta E_{FC2}(\tau_{C2}) = \frac{-s \omega \omega_{on} D_1(1+m_2)}{(C_f + C_n)} \left( A_1 + A_2 e^{-x \tau_{C2}} + A_3 e^{-a \tau_{C2}} + A_4 e^{-y \tau_{C2}} \right) \] (VI-40)

where

\[ A_1 = \frac{1}{(1+m_2)a} \]

\[ A_2 = \frac{m_2}{(1+m_2)(a-x)(y-x)} \] (VI-41)

\[ A_3 = \frac{a - \frac{x}{1+m_2}}{a(x-a)(s-a)} \]

\[ A_4 = \frac{-\frac{x}{1+m_2}}{(x-y)(a-y)}. \]

Since both the initial value and the initial slope of \( \Delta E_C \) are zero,
\[ A_1 + A_2 + A_3 + A_4 = 0 \]  \hspace{1cm} (VI-42)

and
\[ x A_2 + a A_3 + \gamma A_4 = 0. \]  \hspace{1cm} (VI-43)

For all cases of practical interest, \( \gamma \tau < 1 \); so expanding \( e^{-\gamma \tau} \) and retaining only the first two terms results in small error. By doing this and substituting from (VI-42) and (VI-43)

\[
\Delta E_{T2}(\tau_{C2}) = -\frac{\omega_{on} D_1 (1 + m_2)}{(C_T + C_{cn})} \left[ A_2 \left( e^{-x \tau_{C2}} + x \tau_{C2} - 1 \right)
+ A_3 \left( e^{-a \tau_{C2}} + a \tau_{C2} - 1 \right) \right]. \]  \hspace{1cm} (VI-44)

If region 2 is sufficiently long for \( \Delta E_T \) to swing through \( E_p - E_n \) volts, the value of \( \tau_{C2} \) can be obtained by finding an approximate solution of (VI-44) by graphical or other means and improving it by Newton's method. If \( \tau_{C2}^{(n)} \) is the \( n \)th approximation to \( \tau_{C2} \), the next approximation is given by

\[
\tau_{C2}^{(n+1)} = \frac{F(\tau_{C2}^{(n)})}{F'(\tau_{C2}^{(n)})} \]  \hspace{1cm} (VI-45)

where

\[
F(\tau_{C2}^{(n)}) = E_p - E_n - \frac{\omega_{on} D_1 (1 + m_2)}{C_T + C_{cn}} \left[ A_2 \left( e^{-x \tau_{C2}^{(n)}} + x \tau_{C2}^{(n)} - 1 \right)
+ A_3 \left( e^{-a \tau_{C2}^{(n)}} + a \tau_{C2}^{(n)} - 1 \right) \right] \]  \hspace{1cm} (VI-46)

and
\[
F'(\tau'(n)) = \frac{a_{on} \omega_{on} D_1 (1 + m_2)}{C_f + C_{cn}} \left[ A_2 x(e^{-x \tau'(n)} - 1) - A_3 a(e^{-a \tau'(n)} - 1) \right]
\]

(VI-47)

If region 2 is not long enough to allow \( \Delta E_f \) to swing through \( E_n = E_p \) volts, initial conditions for region C3 can be derived from (VI-44). These are

\[
\Delta E_f(\tau'_2) = \frac{-a_{on} \omega_{on} D_1 (1 + m_2)}{C_f + C_{cn}} \left[ A_2 (e^{-x \tau'_2} + x \tau'_2 - 1) \right]
\]

(VI-48)

\[
+ A_3 (e^{-a \tau'_2} + \tau'_2 - 1)
\]

and

\[
\Delta E'_f \bigg|_{\tau'_2} = \frac{a_{on} \omega_{on} D_1 (1 + m_2)}{C_f + C_{cn}} \left[ A_2 x(e^{-x \tau'_2} - 1) + A_3 a(e^{-a \tau'_2} - 1) \right].
\]

(VI-49)

To examine \( \Delta E_f \) in region C3, it is necessary to add the initial condition terms to the transform equation. Since the \( s^2 \) term arose from a second derivative with respect to time, and the \( s \) term arose from a first derivative, the complete transform equation for \( \Delta E_f \) in region C3 can be written

\[
\Delta E_{fC3}(s) = \frac{a_{on} \omega_{on} I_b(s)}{C_f + C_{cn}} + s \Delta E_f(\tau'_2) + \Delta E'_f \bigg|_{\tau'_2} + (s + \alpha) \Delta E_f(\tau'_2)
\]

(VI-50)

Substituting in the value of \( I_{bn3} \) from (VI-13) makes it possible to write this as
\[ \Delta E_{fC3}(s) = \frac{-s \omega_{on} I_{bn3}}{(C_f + C_{cn})s(s + a)(s + \gamma)} + \frac{\Delta E_f(\tau'_{2})}{(s + a)(s + \gamma)} \]

\[(VI-51)\]

Taking the inverse transform yields

\[ \Delta E_{fC3}(\tau_{C3}) = \frac{-s \omega_{on} I_{bn3}}{(C_f + C_{cn})} \left[ \frac{1}{\alpha \gamma} + \frac{-\alpha \tau_{C3}}{\gamma} + \frac{-\gamma \tau_{C3}}{\alpha \gamma (\alpha - \gamma)} \right] \]

\[ + \frac{\Delta E_f(\tau'_{2})}{\gamma - \alpha} \left[ \gamma + \frac{\Delta E_f(\tau'_{2})}{\gamma - \alpha} \right] e^{-\alpha \tau_{C3}} - (a - \frac{\Delta E_f(\tau'_{2})}{\gamma - \alpha} e^{-\gamma \tau_{C3}}) \]

\[(VI-52)\]

By expanding and retaining only the first two terms, this can be written as

\[ \Delta E_{fC3}(\tau_{C3}) = \frac{-s \omega_{on} I_{bn3}}{(C_f + C_{cn})} \left[ \frac{e^{-\alpha \tau_{C3}} + \alpha \tau_{C3} - 1}{\alpha (\alpha - \gamma)} \right] \]

\[ + \frac{\Delta E_f(\tau'_{2})}{\gamma - \alpha} \left[ \frac{\gamma e^{-\alpha \tau_{C3}} + \alpha \gamma \tau_{C3} - \alpha}{\gamma - \alpha} \right] + \Delta E_f(\tau'_{2}) \left[ \frac{e^{-\alpha \tau_{C3}} + \gamma \tau_{C3} - 1}{\gamma - \alpha} \right] \]

\[(VI-53)\]

In most cases \( \gamma \tau_{C3} \ll 1 \) and \( \alpha \gg \gamma \) so (VI-53) can be further approximated as

\[ \Delta E_{fC3}(\tau_{C3}) \approx \frac{-s \omega_{on} I_{bn3}}{(C_f + C_{cn})a^2} \left( e^{-\alpha \tau_{C3}} + a \tau_{C3} - 1 \right) + \Delta E_f(\tau'_{2}) \]

\[ + \Delta E_f \left| \frac{\tau_{C3}}{a - e^{-\alpha \tau_{C3}}} \right| \]

\[(VI-54)\]

Approximate solutions for \( \tau'_{C3} \) the time required for \( \Delta E_{fC3} \) to fall through \( E_n - E_p = \Delta E_f(\tau'_{2}) \) volts can be obtained by plotting or by guessing and improved by Newton's method. If \( \tau'_{C3}^{(n)} \) is the \( n \)th approximation to \( \tau'_{C3} \), the next approximation is given by
\[ \tau_{C3}^{(n+1)} = \tau_{C3}^{(n)} - \frac{F(\tau_{C3}^{(n)})}{F'(\tau_{C3}^{(n)})} \]  

(VI-55)

where

\[ F(\tau_{C3}^{(n)}) = \left\{ \left[ E_n - E_p + \Delta E_f(\tau_2) \right] a + \Delta E_f \right\} \frac{C_f + C_{cn}}{a_{on} \omega_{on} I_{bn3}} \]

(VI-56)

and

\[ F'(\tau_{C3}^{(n)}) = c e^{-a \tau_{C3}^{(n)}} \left[ \frac{1}{a} + \Delta E_f \right] \frac{C_c + C_{cn}}{a_{on} \omega_{on} I_{bn3}} = 1. \]

(VI-57)

The Influence of Circuit Parameters on the Fall Time:

The above equations are sufficient to enable one to plot \( \Delta E_f \) as a function of time or to determine the fall time if the circuit constants are known. Unfortunately, it is difficult to tell from a study of these equations which parameters are most important in determining the fall time. Since one of the principal objectives of a study of this kind is to determine criteria for transistor selection for use in flip-flop circuits, it is profitable to consider another approach to the transient analysis which, while it is less convenient for a particular case, is capable of giving a better picture of the relative importance of the various circuit and transistor parameters in determining the fall time.

Previously, the transform of the output current or voltage has been obtained by taking the product of the transform of the input...
current and the appropriate network function. $\Delta E_f(t)$ is the inverse
transform of the product. An alternative method of evaluating the
response as a function of time requires the use of the convolution
theorem

$$\mathcal{L}^{-1} F_1(s) F_2(s) = \int_0^t f_1(t-\tau)f_2(\tau) \, d\tau = \Delta E_f(t) \quad \text{(VI-58)}$$

where $f_2(t)$ is the base current of $T_n$ and $f_1(t)$ is the response
of the transistor to an impulse of current.

The physical interpretation of the convolution integral is that
the time response of a system driven by $f_2(t)$ can be obtained by
summing the response to an infinite number of impulses which together
make up the function $f_2(t)$. At time $t-\tau$ seconds before $t$, $f_2(t)$
had the value $f_2(\tau)$. An impulse of this magnitude at time $\tau$ produces
a response at time $t$ of $f_1(t-\tau)f_2(\tau)$.

The advantage of using the convolution theorem to study the time
response of $T_n$ is that $f_2$ is not a function of the parameters of
$T_n$. Therefore, the effect of these parameters on the fall time can
be determined from $f_1$ alone. Similarly, the effect of the coupling
condenser is contained entirely within the $f_2$ term so that its in-
fluence on the fall time can be determined from $f_2$ alone.

The functions $f_1$ and $f_2$ which will be studied never change
sign in the region of interest. If it is possible to change either
$f_1$ or $f_2$ in such a way that it becomes greater in absolute value
at every point in the interval $0 < \tau < t$, this change will obviously
produce an output signal which has a larger absolute value. Since all of the parameter changes which are to be studied affect \( f_1 \) and \( f_2 \) in this way, this fact can be used as a simple criterion for determining the effect of a particular parameter on the fall time.

In Region B, \( f_1 \) is obtained by taking the inverse transform of the short circuit current gain. From (II-35) this is

\[
f_{1B}(t) = a_1(t) = s_{on} \omega_{on} e^{-\omega_{on}(1-s_{on})t}.
\]  

(VI-59)

Increasing \( s_{on} \) produces both a higher initial value and a larger time constant and hence a faster fall. The effect of increasing \( \omega_{on} \) can be ascertained by differentiating (VI-59) with respect to \( \omega_{on} \) to get

\[
\frac{d}{d \omega_{on}} A_1(t) = a_{on} \left[ e^{-\omega_{on}(1-s_{on})t} - \omega_{on}(1-s_{on})t \right]. \tag{VI-60}
\]

Since this is positive for \( \omega_{on}(1-s_{on})t < 0.567 \) which includes all cases of interest here, increasing \( \omega_{on} \) reduces the fall time.

Since \( s_{on} \) is restricted to values near one, more benefit can be derived from increasing the value of \( \omega_{on} \), a parameter which varies widely from transistor to transistor.

To apply the criterion to region C, \( f_1 \) is taken as the inverse transform of the transfer impedance. From (VI-29)

\[
f_{1C}(t) = \frac{-s_{on} \omega_{on} e^{-at} - \frac{\gamma t}{\gamma - \alpha}}{C_f + C_{on}}.
\]  

(VI-61)
If

\[ \alpha = P \]  

(VI-62)

(VI-61) can be written as

\[ f_{1C}(t) = \frac{-a_{on} \omega_{on} \cdot t}{C_f + C_{cn}} P_0 \]  

(VI-63)

where

\[ P_0 = \frac{e^{-at}}{ct \left( \frac{1}{P} - 1 \right)} \]  

(VI-64)

\( P_0 \), which is a function of \( at \) and \( P \) only, is plotted in fig.VI-6. The function is very insensitive to \( P \) for large values of \( P \).

For the circuits considered here \( P \) will always be greater than ten. Furthermore, the transient will be terminated for \( at \) less than perhaps four. As long as these conditions are met, only a very small error is made by using the value of \( P_0 \) obtained by letting \( P \) go to infinity. By doing this (VI-63) can be written

\[ f_{1C}(t) = \frac{a_{on} \omega_{on}}{(C_f + C_{cn})a} (e^{-at} - 1) \]  

(VI-65)

The initial slope of this function is

\[ \frac{df_{1C}(t)}{dt} \bigg|_{t=0} = \frac{-a_{on} \omega_{on}}{C_f + C_{cn}} \]  

(VI-66)

and the final value is

\[ \lim_{t \to \infty} f_{1C}(t) = \frac{-a_{on} \omega_{on}}{(C_f + C_{cn})a} \]  

(VI-67)

By using (VI-33) and neglecting \( \gamma \) in comparison with \( \alpha \) this can be written as
\[
\lim_{t \to \infty} f_{1c}(t) = \frac{-a_{on} \omega_{on} R_f}{1 - R_f \omega_{on} \left[C_f + C_{cn}(1 - a_{on})\right]} \quad (VI-68)
\]

From (VI-66) it is apparent that increasing \(a_{on}\) or \(\omega_{on}\) or decreasing \(C_f\) or \(C_{cn}\) will increase the initial slope. Similarly from (VI-68) the final value increases when \(a_{on}\), \(\omega_{on}\), and \(R_f\) increase and decreases when \(C_f\) or \(C_{cn}\) increase.

Functions of the form of (VI-65) become greater in absolute value for all \(t\) if either the final value or the initial slope is increased. Therefore, the fall time is reduced by increasing \(a_{on}\), \(\omega_{on}\) or \(R_f\) and by reducing \(C_f\) or \(C_{cn}\).

The cut-off frequency \(\omega_{on}\) is again the most important transistor parameter determining the transient response of the flip-flop circuit. Even though the denominator of (VI-68) contains a term in \(1 - a_{on}\) this term is ordinarily so small compared to the other terms in the denominator that the fall time is not extremely sensitive to \(a_{on}\) even near \(a_{on} = 1\). Therefore, \(a_{on}\) within its useful range is not a particularly important parameter in determining the fall time. The relative importance of \(C_{cn}\) depends on the capacitative load. In practical circuits \(C_L\) is likely to be larger than \(C_{cn}\) thereby making it relatively unimportant in determining the fall time.

In region 2, \(f_2\) is given explicitly by (VI-11). The initial value of this function is

\[
f_{22} \bigg|_{t=0} = \frac{E_0}{R_2} - E_e \left(\frac{1}{R_2} + \frac{1}{R_3}\right) + \left(\frac{C_f}{R_f C_T} - \frac{1}{R_2}\right)(E_0 - E_p - \delta_p) \quad (VI-69)
\]

and the final value is
\[ f_{22} \bigg|_{t \rightarrow \infty} = \frac{E_0}{R_2} = E_s \left( \frac{1}{R_2} + \frac{1}{R_3} \right) \]  

(VI-70)

Actually the collector swing of \( T_p \) is clamped so that the final value is never reached. The function follows (VI-69) until the end of region 2 and then changes discontinuously to the value given by (VI-13).

The final value is always greater than \( I_{bn3} \) and the value of \( f_2 \) at the end of region 2 must be greater than or equal to \( I_{bn3} \). The initial value, however, may be greater than or less than \( I_{bn3} \) depending on the value of \( C_1/R_f C_r \). For short fall times, the initial value of \( f_2 \) should be as large as possible. Since \( C_1/C_r \) increases monotonically to unity as \( C_1 \) goes to infinity, the fall time decreases as \( C_1 \) increases (the rise time increases of course).

The above observation can be used as a basis for the selection of the optimum value of \( C_1 \). One possibility is to select \( C_1 \) so that the rise time is equal to the fall time. Another possibility is to select \( C_1 \) in such a way that the rate of change of rise time with respect to \( C_1 \) is equal to the negative of the rate of change of the fall time with \( C_1 \).

The most satisfactory way of making this selection appears to be to plot the rise and fall times as a function of \( C_1 \) and estimate the proper value of \( C_1 \) from the curves.

The graphical method is quite satisfactory because sufficient information can be obtained from the above transient analysis to select the best values for the resistors in the flip-flop circuit. Using these values for the resistors together with the values for the worst transistors to be used (lowest \( \omega_{on} \) and \( a_{on} \), highest
and the maximum anticipated load, one can plot curves with \( C_1 \) as the only variable which will hold in the worst case. Values of \( C_1 \) picked on this basis will provide optimum operation for the worst case and the curves that are obtained will make it possible to determine the maximum rise and fall times which will be encountered in actual operation of the circuit.

The optimum value of \( R_1 \) can be picked on the basis of a compromise between conflicting demands. It was shown in the static analysis that increasing \( R_1 \) increased the useful output current of the flip-flop for a given transistor current, and it was shown in the analysis of the rise time that increasing \( R_1 \) while maintaining the ratio \( R_1/E_1 \) constant preserved the current distribution between the clamps and decreased the rise time. From (VI-68) increasing \( R_1 \), which also increases \( R_p \), decreases the fall time. Therefore, the operation of the circuit is improved by increasing \( R_1 \) (and \( E_1 \)), but the improvement in these various aspects of circuit performance for a given increase in \( R_1 \) gets rapidly smaller as \( R_1 \) becomes larger. The limit on the size of \( R_1 \) is imposed by the power dissipated in it since the power increases linearly with \( R_1 \) for large values of \( R_1 \). Based on these considerations, the value of \( R_1 \) must be selected by the exercise of engineering judgment.

The values of \( R_2 \) and \( R_3 \) are determined from the static analysis. However, at the cost of introducing an additional power supply, \( R_3 \) can be chosen at will. \( R_3 \) appears as a very small term in (VI-69) and (VI-70) and as one of the parallel resistors
forming \( R_2 \) in (VI-68). Thus increasing \( R_3 \) will tend to decrease the fall time, although the influence of \( R_3 \) is very small. It is likely that \( R_3 \) will be chosen on the basis of static considerations rather than to minimize rise and fall times.

From (VI-69) it is apparent that reducing \( R_2 \) will reduce the fall time, and it was shown that it also reduces the rise time. The value of \( R_2 \) is fixed by the maximum current which is to flow through the transistor. These relations imply that other things being equal, flip-flops drawing large currents tend to change states rapidly.

High speed operation of flip-flops of the type discussed here is obtained by designing for the maximum practical value of current, selecting the largest practical value of \( R_2 \), and choosing the optimum value of \( C_1 \) for the particular transistors which are available. Best results are obtained for high values of \( \omega_{on} \) and low values of \( C_c \). The value of \( a_{on} \) is less important, but high values tend to reduce the flipping time. High values of \( a_{on} \) may be undesirable for other reasons (such as reducing the usable range of \( a_{on} \) as discussed in part V.

Experimental Verification of the Transient Analysis and the Selection of \( C_1 \):

To illustrate the technique of selecting \( C_1 \) and to provide verification of the transient analysis, a flip-flop was constructed using the values of resistors given in the sample static design developed in part V. The parameters of four transistors were measured by the methods of part III and were found to have the values given in Table VI-1.


<table>
<thead>
<tr>
<th>Parameter</th>
<th>T-7327</th>
<th>T-7708</th>
<th>T-7743</th>
<th>T-2790</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_0 \omega_0$</td>
<td>$7.28 \times 10^6$</td>
<td>$5.32 \times 10^6$</td>
<td>$5.57 \times 10^6$</td>
<td>$3.77 \times 10^6$</td>
</tr>
<tr>
<td>$a_0/(1-a_0)$</td>
<td>25.4</td>
<td>33.3</td>
<td>34.5</td>
<td>17.5</td>
</tr>
<tr>
<td>$C_c$ (Region 1)</td>
<td>60 mmfd.</td>
<td>85 mmfd.</td>
<td>140 mmfd.</td>
<td>98 mmfd.</td>
</tr>
<tr>
<td>$C_c$ (Region 2)</td>
<td>32 mmfd.</td>
<td>40 mmfd.</td>
<td>72 mmfd.</td>
<td>55 mmfd.</td>
</tr>
<tr>
<td>$C_b^*$</td>
<td>48 mmfd.</td>
<td>67 mmfd.</td>
<td>83 mmfd.</td>
<td>77 mmfd.</td>
</tr>
</tbody>
</table>

Table II-1

In addition, $I_n$, $E_\phi$, and $\phi$ were measured in the flip-flop circuit for each transistor. The best of the transistors, T-7327 was used in turn with each of the other transistors in the flip-flop. For each of these combinations, the rise and fall times were computed by the methods described above for no load and for a 450 mmfd. capacitive load as a function of the coupling condenser $C_1$. The results of these computations are plotted as the theoretical curves of figs. VI-7a to VI-7f. The measured values of rise and fall times are plotted as the experimental points on the same curves. The reasonably good agreement between theory and experiment indicates that the methods presented here are capable of predicting flip-flop rise and fall times with engineering accuracy.

* The value of $C_b^*$ is found by taking the sum of the small signal collector capacity for the operating collector voltage and the emitter capacity for a swing of $\phi$. 
The curves of fig. VI-7 reveal much of interest to the circuit designer. The transistors were chosen to illustrate the effects of parameter variation. Transistors 7708 and 7743 have substantially the same value of $a_\circ \omega_0$ but 7708 has significantly less collector capacity. A comparison of fig. VI-7a and fig. VI-7c shows that slightly better fall times are obtained from 7708, but 7743 is still a useful transistor. A comparison of fig. VI-7b and VI-7d shows that 7708 also has significantly better rise times.

Transistor 2790 was chosen to illustrate the effect of a low value of $a_\circ \omega_0$. Figure VI-7e shows that this transistor is definitely inferior to the other transistors. The difference between T-2790 and T-7327 when they are used together in a flip-flop is seen by comparing fig. VI-7f and fig. VI-7e.

It is evident that substantial values of $C_1$ are necessary for satisfactory operation, but the value is not extremely critical. The better transistors require values of $C_1$ in the neighborhood of 200 mmfd, but the optimum value for T-2790 is about 350 mmfd. Transistor 2790 will not operate satisfactorily with capacitive load for values of $C_1$ appreciably below 350 mmfd. The flip-flops operate satisfactorily with values of $C_1$ in excess of the optimum value with no degradation of performance except for increased rise time. The required value of $C_1$ is substantially independent of the load capacity which makes the construction of standard flip-flops which can be used in digital computers feasible.
Triggering the Flip-Flop:

Any completely accurate triggering theory must take into account the properties of both transistors in determining the required trigger pulse to cause the flip-flop to change states. However, practical experience with the type of circuit described here shows that the required trigger signal depends primarily on the characteristics of the transistor which is turned off by the trigger signal and only slightly on the characteristics of the other transistor. This fact suggests the possibility of developing a simplified theory which depends only on the characteristics of the transistor being triggered. To do this requires an assumption of some sort about the quality of the second stage of the flip-flop. It will be assumed that the second stage is such that it will provide sufficient current to keep the first stage off and allow flipping to proceed if the first stage is turned completely off by the trigger signal. This requirement will be met if the second transistor is a high quality unit (in the sense that \( a_0 \omega_0 > 6 \times 10^6 \) per second).

The required trigger signal calculated on the basis of this assumption will be called the minimum satisfactory trigger signal. In many practical flip-flop circuits, the minimum satisfactory trigger signal is very close to the signal required to force the flip-flop to change states.

Fig. VI-8 is an equivalent circuit which is suitable for determining the response of \( T_p \) to the trigger pulse. It is assumed that sufficient base current is supplied through a negligibly
high impedance to produce a current $I_p$ through the clamp diode $D_2$. It is also assumed that the input pulse is approximately rectangular and that it is wide enough (0.5 microseconds is ample) to allow $C_2$ to charge completely. Assuming $R_5$ is negligibly large, the quantity of charge transferred from the transistor is $EC_2$. This charge is transferred very rapidly so small error is made by making the simplifying assumption that the trigger signal can be approximated by a current impulse of amplitude $EC_2$ into the base of $T_p$.

The short circuit current gain of the transistor is given by (II-35). This equation may be taken to apply to the initial response to a current impulse because the clamp diode provides a low impedance as long as any current is flowing through it and the load capacity prevents any instantaneous change of collector voltage for further changes in the collector current.

The response of the network to an impulse $EC_2$ is given by (III-11) as

$$I_o = -a_{op} \omega_{op} EC_2 e^{-a_{op}(1 - a_{op})t}.$$  \hspace{1cm} (VI-71)

No voltage will be developed at the collector unless the peak value of $I_o$ exceeds $I_p$. The condition for the minimum satisfactory trigger signal is that the peak value of $I_o$ should equal the total current which is flowing through the transistor initially. The initial current is $I_c$ so the minimum satisfactory trigger impulse is given by
\[ EC_2 = \frac{I_c}{a_{op} \omega_{op}} \]  

(VI-72)

For larger values of \( EC_2 \), equation (VI-72) becomes meaningless since the transistor can only turn off current which was flowing at the start of the transient. When the trigger impulse exceeds the value given by (VI-72) the base of the transistor becomes a high impedance and \( C_1 \) charges to a value determined by the circuit constants and the amplitude of the trigger signal. The transistor remains cut-off until \( C_1 \) has discharged enough to allow the base to become conducting. Thus the effectiveness of trigger impulses greater than the minimum satisfactory trigger impulse is determined primarily by the passive elements rather than by the transistor, and relatively small increases in the trigger amplitude above that required to achieve the cut-off condition may maintain the cut-off condition for some time. This circumstance explains why the minimum satisfactory trigger ordinarily gives a working approximation to the minimum trigger signal required to cause the flip-flop to change states.

A comparison of the calculated minimum satisfactory trigger signal with the measured trigger signal required to cause the flip-flop to change states is given in fig. VI-9. The flip-flop circuit and the transistors used are the same ones used in obtaining the results shown in fig. VI-7.

The Complete Design of the Flip-Flop Circuit:

The above theory has provided sufficient information to complete
the design of the flip-flop which started with the static analysis. It is ordinarily desirable to have the circuit trigger with a pulse having an amplitude no greater than the output voltage swing. However, for greatest usefulness, the input condenser should be as small as possible. From fig. VI-9 a suitable compromise for the value of $C_2$ is 350 mmfd. for transistors as good as or better than the ones used here.

The remaining circuit parameters are uncritical. The value chosen for $C_4$ is 0.1 mfd. The value of $C_2 R_5$ must be small enough to allow the voltage at their junction to return to its steady state value between trigger impulses, but $R_5$ must be large compared to the input impedance of the transistor. A value of 6,800 ohms for $R_5$ meets these conditions satisfactorily.

The complete flip-flop schematic diagram together with the values which have been chosen for the circuit parameters by this design process is given in fig. VI-11.
VII THE USE OF JUNCTION TRANSISTOR FLIP-FLOPS
IN DIGITAL COMPUTING CIRCUITS

Logical Description of the Flip-Flop:

In order to describe the behavior of the flip-flop some sort of logical notation is required. Each flip-flop has two outputs which can be denoted by $Q$ and $Q'$. The two stable states of the flip-flop are denoted by 1 and 0 and the state of a particular output is also denoted by a 1 or 0. The convention used here is that the most positive state of the output is 1, the most negative state is 0. Thus when the flip-flop is in state 1, $Q = 1$ and $Q' = 0$; and when the flip-flop is in state 0, $Q = 0$ and $Q' = 1$. Subscripts can be used to designate the particular flip-flop under discussion.

In addition, for a complete description of flip-flop behavior, some sort of time notation is required. In digital computers a clock signal is ordinarily used in such a way that a pulse applied at the $n^{th}$ clock time determines the state of the flip-flop at the $n + 1^{st}$ clock time. The time is designated by a superscript thus $Q^n_s = 1$ states that flip-flop $s$ is in state 1 at the $n^{th}$ clock time.

There are two inputs to the flip-flop designated $J$ and $K$. An impulse applied to input $J$ at the $n^{th}$ clock time is designated $J^n_s = 1$.

With this notation, the truth table for the flip-flop is
\begin{align*}
\begin{array}{cccc}
  j^n & k^n & q^n+1 & q^{n+1} \\
  0 & 0 & q^n & q^n \\
  1 & 0 & 1 & 0 \\
  0 & 1 & 0 & 1 \\
  1 & 1 & \text{indeterminate} \\
\end{array}
\end{align*}

This truth table differs from the truth table for the ordinary vacuum tube flip-flop in that the flip-flop does not change states reliably when both inputs are present simultaneously. This makes counter circuits slightly more complicated, but puts no real restriction on the use of the circuit since diode gates can always be provided to prevent simultaneous triggering of the two inputs.

**Diode Gating Networks:**

One type of diode gate which might be used with this flip-flop is given in fig.VII-1 which shows the two basic gates the "and" and "or" gates which are designated by the logical symbols \( \cdot \) and \( + \) respectively. These two gates make it possible to mechanize any logical function.

If the junction of the diodes in either of the gates of fig.VII-1 is at 17 volts at the clock pulse time, it will be driven to 7 volts by the clock pulse thereby providing a signal to the input of the flip-flop. If the junction is at 7 volts, the clock pulse diode is always disconnected and no signal is provided to the flip-flop. In the "or" gate, the junction is at 17 volts if either A or B is at 17 volts. In the "and" gate, the junction is at 17 if A and B are at 17 volts. Since every change in the diode gating network takes
place at the clock pulse time, no changes in A or B ever cause extraneous inputs to the flip-flop.

The "or" gate must be preceded by a higher level "and" gate to prevent shorting the clock pulse. Occasionally this results in wasted diodes, but the gating circuits of digital computers are so complicated that single level "or" gates seldom are necessary. A practical "or" gate which mechanizes the function $A \cdot B + C = 1$ is given in fig. VII-2. Gates of this type can be cascaded indefinitely as alternate "and" and "or" gates.

The cardinal rule in mechanizing gates of this type is that at least one diode at each node must be conducting at the clock time so that the potential at each node is definitely established. In order to do this and allow for tolerances on resistors, diodes, and supply voltages, the currents required from the flip-flops go up with the level of the gate.

To specify the currents required to operate a multilevel gate, the following notation is used: $V_{1n}$ is the absolute value of the maximum potential difference between the voltage to which the $n^{th}$ gate resistor is returned and the output level of the flip-flop which maximizes this potential. This includes the tolerances on the supply voltages. $V_{2n}$ is the absolute value of the minimum potential difference between the voltage to which the $n^{th}$ gate resistor is returned and the output level of the flip-flop which minimizes this potential. This also includes tolerances on the power supply voltages. $AE_{\text{max}}$ is the maximum value of the output voltage swing of the flip-flop.
\( R_n \) is the \( n^{th} \) level gate resistor and \( \Delta R_n \) is the permitted change in \( R_n \).

\[
\varepsilon_{in} = 1 + \frac{\Delta R_n}{R_n}
\]

\[
\varepsilon_{2n} = 1 - \frac{\Delta R_n}{R_n}
\]

\( D_n \) is the number of input diodes to the \( n^{th} \) level gate.

\( I_d \) is the maximum value of current which flows through a diode back biased by \( \Delta E_{\text{max}} \) volts.

\( \tau \) is the clock interval.

\( C \) is the input capacity of the f.f. plus stray capacity.

\[
I_{in} = \frac{\Delta E C}{\tau}
\]

is the constant value of current required to cause the input voltage of the flip-flop to change through \( \Delta E \) volts in \( \tau \) seconds.

The control potential at the input of the flip-flop can be changed \( \Delta E \) volts in no more than \( \tau \) seconds by supplying or withdrawing a current at least as great as \( I_{in} \). \( R_1 \) will be small enough to do this for every parameter variation if

\[
R_1 \leq \frac{V_{21}}{I_{in} \varepsilon_{11}} \quad \text{(VII=1)}
\]

Any diode into the first level may have to carry a current

\[
I = \frac{V_{11}}{R_1 \varepsilon_{21}} + D_1 I_d + I_{in} \quad \text{(VII=2)}
\]

The second level gate resistor may therefore have to carry a
current

\[
\frac{V_{22}}{R_2 \varepsilon_{12}} = \frac{V_{11}}{R_1 \varepsilon_{21}} + D_1 I_d + I_{in}
\]  \hspace{1cm} (VII-3)

which requires that the resistor be chosen as

\[
R_2 \leq \frac{V_{22}}{\varepsilon_{12}} \frac{1}{\frac{V_{11}}{R_1 \varepsilon_{21}} + D_1 I_d + I_{in}}
\]  \hspace{1cm} (VII-4)

Any diode into the second level may have to carry a current

\[
\frac{V_{12}}{R_2 \varepsilon_{22}} + D_2 I_d
\]  \hspace{1cm} (VII-5)

In general, the \(n\)th level gate resistor is

\[
R_n \leq \frac{V_{2n}}{\varepsilon_{1n}} \frac{1}{\frac{V_{1n-1}}{R_{n-1} \varepsilon_{2n-1}} + D_{n-1} I_d}
\]  \hspace{1cm} (VII-6)

and the current which must be carried by a diode into the \(n\)th level is

\[
\frac{V_{1n}}{R_n \varepsilon_{2n}} + D_n I_d
\]  \hspace{1cm} (VII-7)

The diode supplies current to "or" gates and withdraws current from "and" gates.

In certain cases it will be found that a logical expression is used repeatedly throughout the computer. It is economical of diodes to generate this function once and supply current from the function to the several places where the function is used. If \(I_{max}\) is the maximum current as calculated above that this function will ever be required to supply, the gate resistor required for one of these so
called "pipe" functions is

\[ R_n \leq \frac{V_{\text{on}}}{I_{\text{max}}} \]  \hspace{1cm} (VII-8)

When the current loading of a flip-flop is being computed it should be remembered that the logical expressions being formed may be such that the currents required by the gates that the flip-flop drives are shared by a number of flip-flops. Because of this the current required from the flip-flop may be much less than the sum of the currents required by the gates the flip-flop drives.

**A Transistor Figure of Merit in Flip-Flop Circuits:**

It is apparent from the above discussion that a useful figure of merit for a flip-flop is given by the available output current divided by the product of the output swing and the input capacity. This is approximately equal to the number of gates the flip-flop will drive divided by the clock interval.

The minimum output swing is determined by parameter tolerances and triggering considerations, but it is probably in the neighborhood of 5 to 10 volts so most improvements in this figure of merit must come by increasing the output current and decreasing the input capacity.

The simplified triggering theory showed that the ratio of collector current to input capacity was proportional to the product \( \alpha_c \alpha_b \). Thus, this product is a reasonable figure of merit for transistors in flip-flop circuits.
Increasing the Usefulness of the Junction Transistor Flip-Flop:

The figure of merit for the flip-flop designed here is approximately 1/10 the figure of merit which could be obtained from a vacuum tube flip-flop using a twin triode vacuum tube. It is necessary therefore to consider ways in which additional transistors can be used to increase the effectiveness of the transistor flip-flop if it is to compete successfully with the vacuum tube flip-flop.

One possibility is to use the grounded collector amplifier, the analog of the cathode follower, to drive capacitive loads and amplify the available current. The grounded collector transistor has the disadvantage relative to the cathode follower of having a lower input impedance. However, it has a compensating property of negligible d.c. shift between the input and output which makes it very useful in switching circuit work. Because of this property, it can be used within a diode gating network either to amplify "pipe" functions or to effectively reduce the input capacity of the flip-flop while still preserving the d.c. level essential to successful gating. The transistor requires no filament wiring and generates negligible heat. Both factors are favorable to its being included in a diode network.

The network amplifier may be required to pass currents in one direction only since it feeds a diode load. Since there are both n-p-n and p-n-p transistors available, it is possible to choose an n-p-n when supplying current to the load and a p-n-p when absorbing current from the load. This makes it possible to drive large or small loads efficiently since the current through the emitter return
resistor need be only large enough to discharge the stray capacity in the clock interval. The circuit for the network amplifier is given in fig. VII-3.

The input impedance of the gating network amplifier can be approximated by the methods of part II as a resistance given by (II-51) and a condenser given by (II-52) in parallel. These values are to be computed for the maximum load assuming that the transistor to be used has the lowest allowable value of \( r_c \), \( a_o \), and \( \omega_c \) and the highest allowable value of \( C_c \). It was shown in (II-54) that the frequency dependence of the voltage gain for the grounded collector stage was negligible for the frequencies considered here. Therefore, the emitter voltage will change by \( \Delta E \) volts in \( \tau \) seconds if sufficient current is provided to change the base voltage by \( \Delta E \) volts in \( \tau \) seconds. The base resistor must be capable of supplying the current demanded by the input impedance of the amplifier just as the first gating resistor was required to supply the current demanded by the input impedance of the flip-flop circuit. Therefore, if the required input current computed from the input impedance is used as \( I_{in} \), the above gating formulas can be used to determine the values of the load resistors in any diode gates driving the network amplifier.

The low values of collector dissipation of high frequency transistors seriously limit the usefulness of the gating network amplifier. The maximum collector voltage must be at least as great as the desired output swing, and the maximum value of
collector current when the collector voltage is high must be at least equal to the possible changes in load current which in practical cases is equal to the load current. For a 10 volt swing a typical collector dissipation of 40 milliwatts limits the output current to 0.4 ma. When tolerances and safety factors are considered, the design value of output current must be reduced to perhaps half of that figure. This limitation is so restrictive that the circuit in its simple form has limited usefulness as a network amplifier and is almost entirely useless as a booster amplifier to increase the current output of the flip-flop.

In those cases where a small amount of the voltage swing can be discarded, a grounded collector amplifier can be constructed which uses the transistor much more efficiently. This is done by arranging a diode clamp circuit in such a way that the transistor has only cut-off current flowing through it when it has maximum collector voltage. Circuits for p-n-p and n-p-n grounded collector amplifiers using this idea are given in fig. VII-3. To make the discussion definite consider the n-p-n circuit. The base swings between $E_2$ and $E_1$ where it is assumed that $E_2$ is the more positive of the two voltages. The collector is returned to a voltage $E_2 + \delta_1$ where $\delta_1$ is a small positive voltage chosen to be as small as possible and still keep the transistor out of saturation. The emitter is returned through a diode to a potential $E_1 + \delta_2$. The diode is connected so that the emitter cannot go negative with respect to $E_1 + \delta_2$. The value of $\delta_2$ is chosen
so that the transistor will be cut off when the base voltage of the transistor is $E_1$. Under these conditions, the transistor will be required to supply only cut-off current when its collector voltage is $E_2 + \delta_1 - (E_1 + \delta_2)$ so that the collector dissipation in this stable state is low. When the base voltage is $E_2$ the transistor has to supply the full load current, but the collector voltage is just $\delta_1$ which is a small voltage. If $\delta_1$ is 1 volt, for example, the load current could be 40 ma, before the collector dissipation is exceeded in this stable state. During the transition between the two states high values of collector dissipation are encountered, but these do not damage the transistor provided the average dissipation is within the rating.

This circuit is particularly suited as a booster amplifier for the output current of the flip-flop since a small reduction in the output voltage swing is easily made negligible by proper design of the flip-flop, and the flip-flop changes state rapidly thereby minimizing the average collector dissipation of the transistor.

In circuits where high speed operation is not of primary importance, the collector of the booster amplifier can be returned to the upper clamp voltage, $E_n$ (for n-p-n), and the clamp diode omitted. When the output of the flip-flop tries to rise above $E_n$, the collector of the grounded collector transistor becomes forward biased thereby preventing the output from rising appreciably above $E_n$. This drives the output transistor into saturation and introduces a delay, typically of the order of a microsecond, in the output when the flip-flop changes state.
Transistors used in this way require low values of saturation collector voltage.

By combining the grounded collector amplifiers on both input and output with the junction transistor flip-flop it is possible to design flip-flops for operation in the range below a pulse repetition rate of perhaps 200 kc. which compare favorably with a vacuum tube flip-flop having a cathode follower amplifier using receiving type tubes. The transistor circuit is considerably more complex, but better transistors are becoming available, and it can be expected that increasingly better results will be obtained with these transistors.
VIII APPENDIX

The purpose of this appendix is to show that an amplifier having small signal admittance equations

\[ i_1 = G_{11} e_1 + G_{12} e_2 \]
\[ i_2 = G_{21} e_1 + G_{22} e_2 \]

where the G's obey the inequalities

\[ G_{11} G_{22} - G_{12} G_{21} > 0 \]  \hspace{1cm} (VIII-1)

and

\[ G_{11} + G_{22} + G_{12} + G_{21} < 0 \]  \hspace{1cm} (VIII-2)

has the property that

\[ |G_{21}| > G_{11} \]  \hspace{1cm} (VIII-3)

and

\[ |G_{21}| > G_{22} \]  \hspace{1cm} (VIII-4)

In the forward direction, the open circuit voltage gain \( A_{oc} \) is

\[ A_{oc} = \left. \frac{e_2}{e_1} \right|_{i_2 = 0} = \frac{G_{21}}{G_{22}} \]

and the short circuit current gain \( A_{sc} \) is

\[ A_{sc} = \left. \frac{i_2}{i_1} \right|_{e_2 = 0} = \frac{G_{21}}{G_{11}} \]
To have positive feedback, $G_{21}$ must be negative since $G_{11}$ and $G_{22}$ are positive.

In the reverse direction, the open circuit voltage gain $A'_{oc}$ is

$$A'_{oc} = \frac{e_1}{e_2} \bigg|_{i_1 = 0} = -\frac{G_{12}}{G_{11}}$$

and the short circuit current gain $A'_{sc}$ is

$$A'_{sc} = \frac{i_1}{i_2} \bigg|_{e_1 = 0} = \frac{G_{12}}{G_{22}}$$

The sign of $G_{12}$ is not specified, but

$$|G_{21}| > |G_{12}|$$

since by hypothesis, the forward direction is the direction of greatest gain.

If the sign of $G_{12}$ is (+), inequality (VIII-1) is automatically satisfied and

$$G_{11} + G_{22} + G_{12} < |G_{21}|$$

which shows that both (VIII-3) and (VIII-4) are satisfied.

If the sign of $G_{12}$ is (−), inequality (VIII-1) becomes

$$G_{11} G_{22} > |G_{21}| \bigg| G_{12} \bigg| \quad \text{(VIII-5)}$$

and (VIII-2) becomes

$$G_{11} + G_{22} < |G_{21}| + \bigg| G_{12} \bigg| \quad \text{(VIII-6)}$$

Now suppose that
\[ G_{22} > G_{11} \]

and further suppose

\[ G_{22} > |G_{21}|. \]

Then from this and (VIII-6)

\[ 0 < G_{22} = |G_{21}| < |G_{12}| - G_{11} \]

so

\[ G_{11} < |G_{12}|. \]

The admittance coefficients can now be arranged as a monotonically decreasing sequence

\[ G_{22} > |G_{21}| > |G_{12}| > G_{11}. \]

Now let

\[ |G_{12}| = G_{11} + \delta_1 \]
\[ |G_{21}| = G_{11} + \delta_1 + \delta_2 \]
\[ G_{22} = G_{11} + \delta_1 + \delta_2 + \delta_3 \]

where all the \( \delta \)'s are positive numbers.

Substituting these values into (VIII-6)

\[ G_{11} + G_{11} + \delta_1 + \delta_2 + \delta_3 < G_{11} + \delta_1 + \delta_2 + G_{11} + \delta_1, \]

or

\[ \delta_3 < \delta_1. \]

And substituting into (VIII-5)

\[ G_{11}(G_{11} + \delta_1 + \delta_2 + \delta_3) > (G_{11} + \delta_1 + \delta_2)(G_{11} + \delta_1), \]
or
\[ G_{11} \delta_3 > G_{11} \delta_1 + \delta_1^2 + \delta_1 \delta_2. \]

But since \( \delta_3 < \delta_1 \),
\[ G_{11} \delta_1 > G_{11} \delta_1 + \delta_1^2 + \delta_1 \delta_2, \]
or
\[ \delta_1^2 + \delta_1 \delta_2 < 0, \]

which is impossible.

Since \( G_{11} \) and \( G_{22} \) enter symmetrically into the inequalities, the error can only be in the assumption \( G_{22} > |G_{21}| \).

To test this let
\[ G_{22} < |G_{21}|. \]

Then from (VIII-6) and the above,
\[ 0 > G_{22} - |G_{21}| < |G_{12}| - G_{11} \]

so
\[ |G_{12}| < G_{11}. \]

The admittance coefficients can now be arranged in monotonically decreasing order as
\[ |G_{21}| > G_{22} > G_{11} > |G_{12}|. \quad (VIII-7) \]

Let
\[ G_{11} = |G_{12}| + \delta_1^1 \]
\[ G_{22} = |G_{12}| + \delta_1^1 + \delta_2^1 \]
\[ |G_{21}| = |G_{12}| + \delta_1^1 + \delta_2^1 + \delta_3^1 \]
where the $\delta'$s are positive numbers.

Substituting these values into (VIII-6)

$$|G_{12}| + \delta'_{1} + |G_{12}| + \delta'_{1} + \delta'_{2} < |G_{12}| + \delta'_{1} + \delta'_{2} + \delta'_{3} + |G_{12}|$$

or

$$\delta'_{1} < \delta'_{3}$$

and substituting into (VIII-5)

$$(|G_{12}| + \delta'_{1})(|G_{12}| + \delta'_{1} + \delta'_{2}) > (|G_{12}| + \delta'_{1} + \delta'_{2} + \delta'_{3})(|G_{12}|)$$

or

$$|G_{12}| \delta'_{1} + \delta'_{1} \delta'_{2} + \delta'_{1} \delta'_{2} + |G_{12}| \delta'_{3} >$$

But since $\delta'_{1} < \delta'_{3}$,

$$|G_{12}| \delta'_{1} + \delta'_{1} \delta'_{2} + \delta'_{1} \delta'_{2} > |G_{12}| \delta'_{1}$$

or

$$\delta'_{1}^{2} + \delta'_{1} \delta'_{2} > 0$$

which is true for all values of the $\delta'$'s.

Inequality (VIII-7) therefore, gives the correct order of the admittance coefficients except for a possible inversion of the order of $G_{11}$ and $G_{22}$ and the inequalities (VIII-3) and (VIII-4) are proved.
REFERENCES


FIGURE II-1
LOW FREQUENCY EQUIVALENT CIRCUIT
OF A JUNCTION TRANSISTOR

FIGURE II-2
HIGH FREQUENCY EQUIVALENT CIRCUIT
OF A JUNCTION TRANSISTOR
\[ R_1 = r_e + r_b \]
\[ R_2 = \frac{r_e + r_b}{r_e a_c} \left[ r_e + r_b (1 - a_c) \right] \]
\[ L = \frac{(r_e + r_b)^2}{\omega_0 r_b a_o} \]

**FIGURE II-3**

EQUIVALENT CIRCUIT OF GROUNDED BASE INPUT

INPUT IMPEDANCE WITH \( r_L = 0 \)

\[ R_1 = r_b + \frac{r_e}{1 - a_o} \]
\[ R_2 = \frac{r_e + r_b}{r_e a_c} \left[ r_e + r_b (1 - a_c) \right] \]
\[ C = \frac{r_e a_o}{\omega_0} \frac{1}{\left[ r_e + r_b (1 - a_c) \right]^2} \]

**FIGURE II-4**

EQUIVALENT CIRCUIT FOR GROUNDED EMITTER

INPUT IMPEDANCE WITH \( r_L = 0 \)
If $RC > \frac{1}{\omega_o(1-a_o)} > \frac{1}{\omega_o}$

$$
R_1 = \frac{a_o R}{\omega_o RC - 1} \\
C_1 = \frac{1}{a_o \omega_c} (\omega_o RC - 1) \\
R_2 = \frac{R (RC \omega_o (1-a_o) - 1)}{RC \omega_o - 1} \\
C_2 = \frac{C (RC \omega_o - 1)}{RC \omega_o (1-a_o) - 1}
$$

If $\frac{1}{\omega_o(1-a_o)} > RC > \frac{1}{\omega_o}$

$$
C_1 = C \\
R_1 = \frac{R}{1 + RC \omega_o a_o} \\
R_2 = \frac{R (1-a_o)}{a_o [1 - RC \omega_o (1-a_o)]} \\
L = \frac{R}{a_o \omega_o [1 - RC \omega_o (1-a_o)]}
$$

Grounded Emitter $R = r_e$, $C = C_e$

Grounded Collector $R = r_g$, $C = C_g + C_e$

**FIGURE II-5**

EQUIVALENT CIRCUITS FOR GROUNDED EMITTER AND GROUNDED COLLECTOR OUTPUT IMPEDANCE
FIGURE 11-5

GROUNDED COLLECTOR AMPLIFIER FOR
Both Positive and Negative Pulses
FIGURE II-7

COLLECTOR CURRENT vs. EMITTER CURRENT AND EMITTER VOLTAGE FOR A TYPICAL GROUNDED BASE JUNCTION TRANSISTOR
Collector current vs. base current for a number of grounded emitter transistors

$E_c = 2 \text{ volts}$

FIGURE II-8
FIGURE III-1 A

E = 2(V_2 - V_1)

FIGURE III-1 B

INVERTING AMPLIFIER

E = 2(V_2 - V_1)

CIRCUITS FOR MEASUREMENT OF G_c
FIGURE III-2

COLLECTOR CAPACITY VS. AMPLITUDE OF MEASURING PULSE

THEORETICAL CURVES AND EXPERIMENTAL POINTS
FIGURE III-3

CIRCUIT FOR MEASURING GROUNDED BASE CUT-OFF FREQUENCY

input pulse

H. scale 1 μsec/cm.
V. scale 3 volts/cm.

output pulse

RC = 1.5 x 10⁻⁷
H. scale 1 μsec/cm.
V. scale 0.3 volts/cm.

FIGURE III-4

WAVEFORMS OBTAINED DURING MEASUREMENT OF GROUNDED BASE CUT-OFF FREQUENCY OF T2790
FIGURE III-5
CIRCUIT FOR MEASUREMENT OF GROUNDED Emitter CURRENT GAIN AND CUT-OFF FREQUENCY

INPUT PULSE
H. scale 100 µsec/cm.
V. scale 3 volts/cm.

CUTPUT PULSE
H. scale 100 µsec/cm.
V. scale 0.3 volts/cm.
RC = 3.0 x 10^-7

CUTPUT PULSE
H. scale 100 µsec/cm.
V. scale 0.3 volts/cm.
RC = 3.7 x 10^-7

FIGURE III-6
WAVEFORMS OBTAINED DURING MEASUREMENT OF GROUNDED Emitter CUT-OFF FREQUENCY OF T2750
FIGURE III-7
CIRCUIT FOR MEASUREMENT OF GROUNDED EMITTER GAIN-BANDWIDTH PRODUCT

SUPERIMPOSED BASE AND INPUT WAVEFORMS
H. scale 1/2 μsec/cm.
V. scale 3 volts/cm.

OUTPUT
EC = 5 x 10^{-7}
H. scale 1/2 μsec/cm.
V. scale 1/10 volt/cm.

FIGURE III-8
WAVEFORMS OBTAINED DURING MEASUREMENT OF GROUNDED EMITTER GAIN-BANDWIDTH PRODUCT

OUTPUT
EC = 3.9 x 10^{-7}
H. scale 1/2 μsec/cm.
V. scale 1/10 volt/cm.

OUTPUT
EC = 3.0 x 10^{-7}
H. scale 1/2 μsec/cm.
V. scale 1/10 volt/cm.
A. T7327 $E_C = 10$ volts
B. T7327 $E_C = 2$ volts
C. T7708 $E_C = 10$ volts
D. T7708 $E_C = 2$ volts
E. T2790 $E_C = 10$ volts
F. T2790 $E_C = 2$ volts

FIGURE III-9
CUT-OFF FREQUENCY AS A FUNCTION
OF COLLECTOR VOLTAGE AND CURRENT
FIGURE IV-1

SINGULAR POINTS OF A FLIP-FLOP AMPLIFIER
FIGURE V-1

BASIC FLIP-FLOP CIRCUIT
FIGURE V-2

STATIC FLIP-FLOP CIRCUIT
FIGURE V-3

TYPICAL GROUNDED EMITTER COLLECTOR CHARACTERISTIC
FIGURE VI-1

TRANSIENT EQUIVALENT CIRCUIT FOR REGION 1
FIGURE VI-2

TRANSIENT EQUIVALENT CIRCUIT FOR REGION 2
\[ E_0 = (E_0 R_1 + E_1 R_2)(R_1 + R_2)^{-1} \]
\[ R_r = R_1 R_2 (R_1 + R_2)^{-1} \]
\[ C_r = C_1 + C_{cp} + C_{LF} \]

**FIGURE VI-3**

SIMPLIFIED TRANSIENT EQUIVALENT CIRCUIT FOR REGION 2
FIGURE VI-4

TRANSIENT EQUIVALENT CIRCUIT FOR OBTAINING FALL TIME
\[ C_f = C_{Lm} + C_{bp} \]

**FIGURE VI-5**

**SIMPLIFIED TRANSIENT EQUIVALENT CIRCUIT FOR OBTAINING FALL TIME**
Figure VI-6

$P_0$ as a function of $\alpha t$ and $F$
A. Fall time of T7708, \( C_L = 450 \text{ mmfd.} \)

B. Rise time of T7327, \( C_L = 450 \text{ mmfd.} \)

C. Fall time of T7708, \( C_L = 0 \).

D. Rise time of T7327, \( C_L = 0 \).

Theoretical curves and experimental points

**FIGURE VI-7a**

RISE TIME OF T7327 AND FALL TIME OF T7708

AS A FUNCTION OF COUPLING CAPACITY
A. Fall time of T7327, $C_L = 450$ mmfd.

B. Rise time of T7708, $C_L = 450$ mmfd.

C. Fall time of T7327, $C_L = 0$.

D. Rise time of T7708, $C_L = 0$.

Theoretical curves and experimental points

FIGURE VI-7b

Rise time of T7708 and fall time of T7327 as a function of coupling capacity
A. Fall time of T7743, $C_L = 450$ mmfd.

B. Rise time of T7327, $C_L = 450$ mmfd.

C. Fall time of T7743, $C_L = 0$.

D. Rise time of T7327, $C_L = 0$.

Theoretical curves and experimental points

FIGURE VI-7c

RISE TIME OF T7327 AND FALL TIME OF T7743

AS A FUNCTION OF COUPLING CAPACITY
A. Fall time of T7327, $C_L = 450 \text{ mmfd}$.

B. Rise time of T7743, $C_L = 450 \text{ mmfd}$.

C. Fall time of T7327, $C_L = 0$.

D. Rise time of T7743, $C_L = 0$.

FIGURE VI-7d

RISE TIME OF T7743 AND FALL TIME OF T7327

AS A FUNCTION OF COUPLING CAPACITY
FIGURE VI-7e

Rise time of T7327 and fall time of T2790 as a function of coupling capacity
A. Fall time of T7327, $C_L = 450$ m&nfd.
B. Rise time of T2790, $C_L = 450$ m&nfd.
C. Fall time of T7327, $C_L = 0$.
D. Rise time of T2790, $C_L = 0$.

Theoretical curves and experimental points

FIGURE VI-7f

RISE TIME OF T2790 AND FALL TIME OF T7327

AS A FUNCTION OF COUPLING CAPACITY
FIGURE VI-8

EQUIVALENT CIRCUIT FOR DETERMINING

THE RESPONSE TO THE TRIGGER IMPULSE
FIGURE VI-9

MINIMUM SATISFACTORY TRIGGER SIGNAL AND EXPERIMENTAL VALUES OF REQUIRED TRIGGER SIGNAL
FIGURE VI-10

COMPLETE FLIP-FLOP SCHEMATIC
Inputs A and B are at either +7 or +17 volts. The clock pulse is a negative pulse with its base at +17 and its peak at +7 volts.
FIGURE VII-3
GATING NETWORK AMPLIFIERS

FIGURE VII-4
FLIP-FLOP BOOSTER AMPLIFIERS