ELECTRONIC PROPERTIES OF HETEROSTRUCTURES AND DEFECTS IN COMPOUND SEMICONDUCTORS

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ABSTRACT

This thesis deals with the electronic characteristics of semiconductor heterostructures and with the electrical properties of semiconductors which are used in the growth of heterostructures. Chapter 2 describes electrical measurements which were made on heterostructures composed of the compound semiconductors AlAs and GaAs. Specifically, the mechanisms for current transport perpendicular to one or more AlAs layers sandwiched between two degenerate GaAs layers were studied, with an emphasis on elastic and inelastic tunneling through the AlAs layers at low temperatures. Tunneling currents occur because the conduction band offset between AlAs and GaAs causes the AlAs to act as a barrier to electrons in the GaAs. Samples composed of single or multiple layers of AlAs sandwiched between GaAs layers were grown by metal organic chemical vapor deposition (MOCVD) and by molecular beam epitaxy (MBE). Electron transport perpendicular to the AlAs barriers was studied as a function of temperature, doping, and layer thickness by making I-V, first derivative (dI/dV), and second derivative (d^2I/dV^2) measurements on these samples. The I-V curves give information about current transport mechanisms. If the dominant mechanism is tunneling, the I-V curves reflect mostly elastic tunneling currents. Structure in the derivatives of the I-V curves indicates the presence of inelastic and resonant tunneling processes. The elastic tunneling measurements give an understanding of the structure of the barriers since these measurements depend on barrier thickness, barrier spacings, and barrier height. Inelastic tunneling measurements can be used to identify the fundamental excitations in the tunneling barrier which can couple to the tunneling electrons; thus, inelastic measurements give additional information about the properties of the barrier. First and second derivatives were measured using modulation techniques.

The main results of this study were the identification of the dominant cur-

rent transport mechanisms across the AlAs barriers as a function of temperature and AlAs layer thickness, the observation of inelastic tunneling currents due to the excitation of phonons, and the observation of resonant tunneling currents. Measurements on MOCVD grown samples with a single p-type AlAs barrier indicated that thermionic emission was the dominant mechanism for current transport over the barrier at room temperature. At low temperatures, leakage currents dominated if the barrier was thicker than approximately 100 Å, while tunneling currents were dominant in the samples with thinner AlAs barriers. Electron self-energy effects due to the coupling of electrons and optical phonons in the GaAs, and the inelastic-excitation of longitudinal optical phonons in the AlAs were observed in the tunneling current through samples with 50 Å thick AlAs barriers. This was the first observation of these effects in the AlAs/GaAs system. Measurements were also made on MOCVD grown samples with a single, n-type AlAs barrier. *I-V* curves for these samples did not have the expected dependence on AlAs layer width. Reproducible structure was still present in the second derivative spectra. A possible explanation for the differences between samples with n-type and p-type barriers which is based on band bending in the AlAs barrier is given. Measurements on MOCVD grown samples with $Al_xGa_{1-x}As$ barriers were made with results similar to those for pure AlAs barriers. Negative resistance regions were observed in the I-V curves of samples with multiple AlAs layers, indicating the presence of resonant tunneling effects. Tunneling measurements on MBE grown structures with a single AlAs barrier did not give reproducible or consistent results.

Chapter 3 presents an investigation of the deep-level defect structure of CdTe using the technique of deep-level transient spectroscopy (DLTS). Layered structures composed of the compound semiconductors CdTe and HgTe or of the alloy $Hg_{1-x}Cd_xTe$ may have interesting properties. To realize these properties it is important to understand the electrical characteristics of CdTe and HgTe.

The electronic properties of CdTe and HgTe are complicated by the fact that native defects may dominate the electrical characteristics of the crystals. An understanding of the deep-level defect structure of CdTe is, thus, important. DLTS measurements can be used to determine the energy of a deep-level with respect to the band edges, the concentration of the level, and its carrier capture cross section. DLTS measurements are made by monitoring changes in the capacitance of a diode caused by capturing carriers at levels in the depletion region of the diode and then thermally emitting the carriers back to the conduction and valence edges.

Measurements were made on a variety of CdTe crystals. Nominally undoped, Cu-doped and In-doped CdTe crystals were studied. Some of the crystals were observed before and after anneals in Cd-vapor, Te-vapor, or in a purified H_2 ambient. Characteristics of deep levels which are seen in all of the n-type CdTe samples are presented. These levels were attributed to native crystal defects or to impurities which are commonly incorporated into CdTe. Levels were also observed which were common to all of the p-type crystals. The same explanation was given for the origin of these traps. A few levels which were specific to certain crystals were also observed and were attributed to unidentified impurities. Deep states were present in the In-doped CdTe which were not observed until the sample was illuminated with above band gap light at low temperatures. Other levels were induced to appear by stressing the CdTe crystals. In general, anneal conditions had a large effect on the concentrations of both shallow and deep levels in the crystals, but did not alter which deep levels were present and their relative concentrations. Modest sample heating (400K) during the process of making DLTS measurements could change the amplitude of levels, sometimes causing new levels to appear or previously observed levels to no longer be observed.

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CHAPTER 1

APPLICATIONS OF TUNNELING SPECTROSCOPY AND DEEP-LEVEL TRANSIENT SPECTROSCOPY TO SEMICONDUCTORS AND SEMICONDUCTOR HETEROSTRUCTURES

1.1 INTRODUCTION

Recent advances in lithography and crystal growth techniques are making it possible to produce semiconductor devices with submicron characteristic dimensions. As these dimensions approach the mean free path of carriers in the semiconductor and as the abruptness of interfaces in the devices reach the same order of magnitude as the wavelength of the carriers, the wavelike nature of the carriers may become observable. The impact of this effect on semiconductor device physics will be two-fold. First, quantum effects will begin to play a role in the performance of conventional devices scaled to these small dimensions. Second, it may be possible to fabricate new semiconductor structures which use quantum effects to produce interesting electrical properties. One area of research which shows promise in terms of making devices that exhibit quantum effects involves the study of layered semiconductor structures.

Improvements in the fields of molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) now make it possible to grow thin epitaxial layers of one semiconductor on top of another semiconductor while maintaining the crystalline structure of both materials. Layer thicknesses as small as 20 Å with interfaces as abrupt as a few monolayers can be produced.[1,2] Since the two semiconductors which make up the layers will have different band gaps, there is a discontinuity in the conduction band and valence band at the interface between them. A number of novel electronic structures based on layered semiconductors have been proposed. The properties of these structures are the result of quantum effects produced by the small characteristic dimensions of the semiconductor layers and by the band offsets at the semiconductor interfaces. In addition to allowing quantum effects to be observed, these new materials may be useful in answering questions of fundamental significance about the two semiconductors from which the layered crystals are built and about the interfaces between the layers. Studies of layered materials may also extend our under-

standing of how reductions in the dimensions of conventional semiconductor devices are going to affect device characteristics. Examples of such structures are semiconductor superlattices, resonant tunneling devices, and electron filters. These are described next.

A semiconductor superlattice consists of alternating slabs of two semiconductors grown epitaxially on top of one another. In general, lattice matched semiconductors are used although there have been recent reports of the growth of strained layer superlattices.[3] The end result of the growth is a new crystal with a much larger basis set than that of the constituent semiconducting materials. Theoretical studies of such crystals indicate that varying the relative and absolute layer thicknesses should allow the band gap, effective masses, and phonon dispersion curves of the new crystal to be varied.[4,5] This makes it possible to grow a semiconducting crystal with its properties tailored to a specific application. The electronic characteristics of alloys of lattice matched semiconductors can also be tailored to desired values by varying the alloy composition, but, in some instances, the superlattice may have superior characteristics to the equivalent alloy.[6]

A structure consisting of two or more thin layers of $Al_{1-x}Ga_xAs$ separated by thin layers of GaAs was considered by Tsu *et al.*[7] $Al_{1-x}Ga_xAs$ has a larger band gap than GaAs. Most of the band gap offset at the $Al_{1-x}Ga_xAs$/GaAs interface occurs in the conduction band. Resonant electronic states are present in the GaAs layers as a result of the confinement of the electron wavefunction to the GaAs by the conduction band offset. These resonances were shown to give rise to negative differential resistances in current transport perpendicular to the layers.

Mailhiot *et al.* suggested a scheme for using the tunneling properties of a single $Al_{1-x}Ga_xAs$ barrier in a GaAs device as a filter to keep the slower L-point GaAs electrons out of the device active region while allowing the Γ-point

electrons to enter this region.[8] Such a structure would be an electron filter.

The calculations which predicted the properties of the above structures relied heavily on knowing certain properties of the two semiconductors from which they were fabricated and of the heterojunction interface between the semiconductors. The values of the band offsets at the interfaces were important parameters in the calculations and are the subject of some controversy. Most of these applications involved electronic states with energies in the band gap of one of the two constituent semiconductors. In the resonant tunneling structure and the electron filter, electrons tunnel through unallowed regions in the middle of the $Al_{1-x}Ga_xAs$ gap. The superlattice conduction and valence band states are usually at an energy which is in the gap of one of the two constituent semiconductors. A knowledge of the electronic band structure in the band gap of the larger band gap material (the complex band structure of the material) is necessary in the calculations. Implicit in all of these devices is an assumption that the mean free path of the carriers is greater than the characteristic dimensions of the structure. For a superlattice to have the calculated properties, the carriers must travel several periods of the superlattice before scattering. In the tunneling structures, the carrier wavefunction must remain coherent across the barrier. An understanding of transport mechanisms in these layered materials is required.

Both of the projects which will be discussed in this thesis were inspired by a desire to determine whether the predicted properties of quantum effect devices can be realized, and, at the same time, to gain an understanding of the characteristics of layered semiconductor structures and of the materials from which they are built. Chapter 2 describes a study of electronic transport perpendicular to AlAs layers in AlAs/GaAs heterojunctions grown by MOCVD with an emphasis on elastic and inelastic tunneling through the layers. The $Al_{1-x}Ga_xAs$/GaAs system is one which has been used quite frequently in ex-

perimental and theoretical studies of semiconductor heterojunctions. As was mentioned above, an AlAs layer imbedded in GaAs acts as a barrier to GaAs conduction band electrons. Elastic tunneling through such a barrier provides information about the coherence length of the electron wavefunction, and about the complex band structure of the barrier material. Inelastic currents provide information about the coupling of electrons to excitations in the barrier as they pass through it. In Chapter 2, the mechanisms for electronic transport across such barriers will be presented as a function of the width of the AlAs barrier, the sample temperature, and the dopings of the AlAs and GaAs layers. Tunneling currents were observed in some of the structures. Inelastic excitations of characteristic phonons in the AlAs/GaAs system were also observed. Structures with two AlAs barriers exhibited resonant tunneling currents which were a clear indication of the presence of the quantum size effects which are predicted in the calculations on resonant tunneling structures.

Two other semiconductors which may be good candidates for the growth of layered structures are HgTe and CdTe. Although there have been calculations of the properties of HgTe/CdTe heterostructures,[4,6] there have been few experimental studies of such structures.[9] An important parameter in the calculations is the valence band offset between HgTe and CdTe which is usually assumed to be near zero. Chapter 3 of this thesis grew out of an attempt to measure the conduction band offset at the interface between HgTe and CdTe. HgTe was grown epitaxially on CdTe by an MOCVD technique.[10] The measured offsets between the HgTe and CdTe were smaller than expected. A possible explanation for this was that surface treatments of the CdTe substrate prior to growth of the HgTe layer were creating large concentrations of defects at the growth interface. The defects could pin the Fermi level at the interface reducing the result of the offset measurement. Deep-level transient spectroscopy (DLTS) measurements were made to look for defects near treated and untreated CdTe

surfaces. A Schottky barrier was evaporated on the CdTe surfaces to make the measurements. Although no Fermi-level pinning defects were discovered near the treated CdTe surfaces, a great deal was learned about the deep-level structure of the CdTe substrates used in the epitaxial growth of HgTe on CdTe. The results of this study are reported in Chapter 3.

The rest of this chapter is outlined as follows: Section 1.2 will discuss the principles of elastic and inelastic tunneling measurements. A discussion of the concepts involved in making DLTS measurements on Schottky barrier devices will be given in Section 1.3. Section 1.4 is a summary of Chapters 2 and 3.

1.2 ELASTIC AND INELASTIC TUNNELING MEASUREMENTS

Electronic tunneling has been studied for quite some time. It has been used to look at the energy gap and superconducting density-of-states in metal-insulator-superconductor junctions.[11] Tunneling has allowed the observation of wavevector conserving phonons in Ge and Si tunnel diodes.[12] Inelastic tunneling spectroscopy is a technique which compliments Raman scattering and infrared absorption in looking at the vibrational modes of molecules.[13] Longitudinal optical phonons,[14] plasma oscillations,[15] two-dimensional subbands and Landau levels[16] have all been observed by studying elastic and inelastic tunneling currents.

A tunnel junction usually consists of two conducting layers of material (electrodes) separated by a thin insulating layer of material (barrier). In some of the cases mentioned above, the conducting layers are metals and the insulating layers are metal oxides. The junctions described in Chapter 2 are composed of two degenerate layers of GaAs separated by one or more thin layers of AlAs which act as a barrier to the electrons in the GaAs because of the conduction band

offset between AlAs and GaAs. The characteristic dimensions of the insulating layer must be small enough for there to be a measurable probability for carriers to tunnel from one side of the junction to the other. The barrier widths are usually in the range of 100 Å. When a tunnel junction is biased, carriers flow from one electrode to the other by tunneling through the barrier region. If a carrier passes through the barrier and conserves its energy, elastic tunneling has occurred. If fundamental excitations in the barrier (such as vibrations of a local impurity state or of the bulk phonons of the barrier material) can be created by the tunneling carrier, it may pass through the barrier, create such an excitation, and lose the associated excitation energy. This is inelastic tunneling. Each of these processes can contribute to the total tunneling current through a tunnel barrier. Fig. 1.1 is a diagram of a potential barrier illustrating both tunneling mechanisms. The potential barrier could represent the conduction band offset of one of the AlAs/GaAs structures which will be discussed in Chapter 2.

In general, the elastic tunneling current gives information about the barrier penetration probability. As the bias voltage on the tunnel junction is scanned, the tunneling electrons at the Fermi level of the more negative electrode will sample the tunneling probability as a function of energy (neglecting changes in the shape of the barrier). If the probability of tunneling through the barrier region is a strong function of the energy of the incident electron (as it is in the case of the resonant tunneling structure previously mentioned), the elastic tunneling current as of function of bias will reflect this dependence. Inelastic currents give information about excitations which can occur in the barrier. Tunneling electrons of a given energy cannot create an inelastic excitation unless there are empty states in the opposite electrode at an energy which is lower by the excitation energy. If the excitation energy is $\hbar\omega$, there is a threshold voltage at $\hbar\omega/e$. Below this voltage the inelastic current will be zero (if the sample temperature is near absolute zero). Inelastic currents are observed as a thresh-

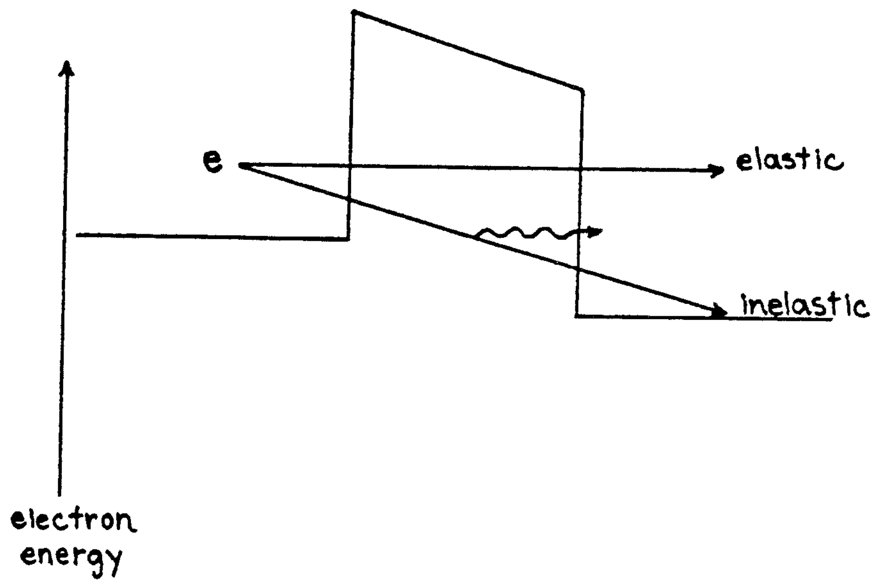

Figure 1.1: Potential energy diagram for a tunneling structure illustrating elastic and inelastic tunneling through the potential barrier.

old in the total current at a voltage equal to the excitation energy measured in electron volts. Quantum effects which result from the characteristics of the barrier are usually observed as structure in the elastic current. The relationship between the voltages where structure is observed and the physical nature of the effect giving rise to the structure is usually more complicated in this case than in inelastic tunneling. A discussion of tunneling currents will now be given to illustrate these points.

If the amount of current passing through a tunnel junction is not too large, the electronic distributions in the electrodes will be close to their equilibrium values. We may then think of the electrodes as independent of one another. The electronic wavefunctions of the system may be approximated by a set of single particle wavefunctions which are confined to one or the other of the electrodes and which satisfy the Hamiltonian for that electrode. The tunnel barrier can be thought of as introducing a perturbing Hamiltonian which allows transitions to occur from states in one electrode to states in the other. Transition rates, r, can be determined using time dependent perturbation theory. r will be a function of the termination of the single particle wavefunctions in the barrier and of the overlap in the barrier region between single particle wavefunctions from the left and right electrodes. r is thus determined by the complex band structure in the barrier region and by the shape of the barrier (it is a function of electron energy and the applied bias). If the tunneling process is inelastic, r is also related to the strength of the interaction between the electron and the excitation process. This description of electronic tunneling is known as Bardeen's transfer Hamiltonian model.[17] Although the transfer Hamiltonian method is not always appropriate, it can be used to illustrate the fundamental principles behind elastic and inelastic tunneling measurements.

When electrons pass through the barrier it is usually assumed that they conserve their component of crystal momentum parallel to the barrier ($\vec{k}_{||}$). If

they tunnel elastically, energy will also be conserved. For fixed energy E and parallel momentum $\vec{k}_{\|}$, the elastic current passing from filled states in the left electrode to unoccupied states in the right electrode will be given by

$$I_{lr}(E,\vec{k}_{\|}) = e\tau_{el}\rho_l\rho_r f(E)(1 - f(E + eV)) \tag{1.1}$$

where τ_{el} is the transition rate for elastic tunneling, ρ_l and ρ_r are the density of states in the left and right electrode restricted to $\vec{k}_{\|}$ (these are a function of $\vec{k}_{\|}$, energy, and applied bias), f is the Fermi function of the left electrode, and V is the applied bias which is assumed to drop completely across the barrier (a positive applied bias will lower the energy of the electrons in the right electrode relative to the left). Eq. 1.1 is basically the transition probability from a state in the left electrode to a state in the right electrode with the same energy and parallel component of wavevector multiplied by the number of electrons available for tunneling in the left electrode and the number of empty states available in the right electrode. There will also be a tunneling current from the right electrode to the left electrode which will be given by

$$I_{rl}(E,\vec{k}_{\|}) = e\tau_{el}\rho_l\rho_r f(E + eV)(1 - f(E)). \tag{1.2}$$

The values of τ_{el} from right to left and from left to right are equal. This can be seen from the form of τ_{el}. See, for example, Ref. 17. The net current from left to right at this energy and wavevector will be given by the difference,

$$I(E,\vec{k}_{\|}) = e\tau_{el}\rho_l\rho_r(f(E) - f(E + eV)). \tag{1.3}$$

The total current from left to right is found by summing this over all possible energies and parallel components of wavevector

$$I_{el} = \int_{-\infty}^{\infty} dE(f(E) - f(E + eV)) \int \frac{d^2 k_{\|}}{(2\pi)^2} \rho_l \rho_r \tau_{el}. \tag{1.4}$$

When the bias on the junction increases, two factors contribute to the additional current passing through the barrier. First, the transition rate (τ_{el}) for a state of a given energy relative to the Fermi level of the left electrode increases because the shape of the tunnel barrier changes. Second, more electrons in the left electrode are available to tunnel to the right electrode. This is reflected in the $f(E) - f(E+eV)$ term in Eq. 1.3. If the applied bias is small compared to the potential barrier amplitude, the product $\rho_l \rho_r \tau_{el}$ will not be a strong function of bias V or of the energy E for the range of energies where $f(E) - f(E+eV)$ is not near zero. Eq. 1.3 reduces to

$$I \approx C_{el} \int_{-\infty}^{\infty} (f(E) - f(E+eV))dE = C_{el}eV. \tag{1.5}$$

Near zero bias we expect the tunneling current to be proportional to voltage. The slope of the tunneling I-V curve at zero bias is used to define the zero-bias resistance. The zero-bias resistance is in turn a reflection of the penetration rate τ_{el} for an unbiased barrier, and should, for example, increase exponentially with the width of the barrier. A comparison of zero-bias resistances calculated using the transfer Hamiltonian method and measured for GaAs/AlAs/GaAs tunneling structures is presented in Chapter 2. As the bias is increased, the change in the barrier shape eventually makes the largest contribution to increases in the tunneling current. At this point the bias effectively reduces the width of the tunneling barrier and the current grows exponentially with bias.[18] From Eq. 1.4, if the tunneling probability is a strong function of energy, the elastic tunneling current will reflect this because τ_{el} will vary as a function of energy. The same is true for a variation in the electron density-of-states in the two electrodes since both densities enter Eq. 1.4. This confirms the statements made above about quantum effects being observable in the elastic tunneling current as function of bias.

If it is possible for the electron to create an excitation in the barrier as it tunnels through the barrier, there will be an inelastic contribution to the

tunneling current. The transfer Hamiltonian method may again be used to calculate the current, but in this case (assuming a positive bias) only electrons tunneling from the left electrode to the right electrode need to be considered. The excitations which the electrons create as they pass through the barrier are usually associated with such things as vibrations of defects in the barrier, vibrations of the lattice which makes up the barrier (phonons), oscillations of the electron plasma associated with the barrier, etc. At the low temperatures associated with these measurements, most of these will be in their ground state, and the flow of electrons from the right electrode to the left electrode with the absorption of an excitation quantum is not likely to occur. The inelastic current will, therefore, be given by

$$I_{in} = \int_{-\infty}^{\infty} f(E)(1 - f(E + eV - \hbar\omega))dE \int \frac{d^2 k_{\|}}{(2\pi)^2} \rho_l \rho_r \tau_{in}, \qquad (1.6)$$

where the energy width of the excitation has been assumed to be zero. This equation is similar to Eq. 1.3 except for the difference in the form of the Fermi factors and in the transmission rate τ_{in}. The excitation energy is $\hbar\omega$. This energy has been subtracted from the argument of the Fermi factor of the right electrode to take into account the fact that an electron which tunnels inelastically ends up in a lower energy state. The value of τ_{in} will depend on the strength of the interaction between the tunneling electron and the process which is being excited in the barrier. As was the case for elastic tunneling, the form of the tunneling current for biases near $\hbar\omega/e$ will be dominated by the Fermi-factor contribution, so the current at temperature T will be given by,

$$I_{in} \approx C_{in} \int_{-\infty}^{\infty} f(E)(1 - f(E + eV - \hbar\omega))dE =$$

$$C_{in}(eV - \hbar\omega) \frac{e^{\frac{(eV - \hbar\omega)}{kT}}}{e^{\frac{(eV - \hbar\omega)}{kT}} - 1}. \qquad (1.7)$$

At absolute zero and for eV less than $\hbar\omega$, the inelastic current is zero. For eV greater than $\hbar\omega$ the inelastic current is given by $C_0(eV - \hbar\omega)$. Eq. 1.6

indicates that there is a threshold at the voltage $\hbar\omega/e$ above which an inelastic contribution to the tunneling current occurs as stated earlier in this section. If the temperature is greater than zero, the threshold still exists but is not as sharp.

Although the transfer Hamiltonian is not necessarily applicable to all tunneling situations, the principles that have been illustrated about the form of elastic and inelastic tunneling currents in low bias regimes are generally true. The above arguments have followed the outline of Ref. 18.

In general, the effects described above are too small to be easily seen in the I-V curve for a tunneling device. Sensitive measurements of the derivatives of tunneling I-V curves are usually required to detect such things as inelastic tunneling, density-of-states effects in the electrodes, and quantum size effects due to the structure of the barrier region. Typically, the first and second derivatives are measured. The biases at which structure is observed in the derivative spectra for a tunnel junction and the magnitude of the structure can be used to determine the properties of the junction. In the case of inelastic tunneling, Eq. 1.7 can be used to show that a step is expected in the first derivative and a peak in the second derivative of the I-V curve at the excitation energy. The magnitude of the peak can give information about the strength of the coupling between the electron and the excitation. Tunneling measurements are usually made at low temperatures to increase the resolution of the measurement. For example, the second derivative of the inelastic current as a function of voltage (Eq. 1.6) is a symmetric peak centered around $\hbar\omega/e$. The peak amplitude is proportional to $1/kT$ and its half width or resolution is given by $5.4kT$.[19] At 4.2 K the resolution is about 2 meV. Appendix A describes techniques for making first and second derivative measurements on tunneling structures at low temperatures.

Tunneling is an ideal way to study the properties of structures which have characteristic dimensions small enough to exhibit quantum effects in their elec-

tronic properties, since these quantum effects almost always manifest themselves in the current-voltage relation for the structures. Chapter 2 describes a study of current transport through AlAs barriers in GaAs/AlAs tunnel junctions using the techniques of elastic and inelastic tunneling.

1.3 DLTS MEASUREMENTS

A deep level in a semiconductor is one with an energy which is in the middle of the band gap or one in which the electronic wavefunction associated with the level has a very broad extent in k-space. Deep levels are many times characterized by large capture cross sections and low thermal emission rates for carriers in the semiconductor. They can act as very efficient recombination centers, and sometimes as generation centers. In most instances, deep levels are not desirable in a semiconductor. It is very important to be able to detect their presence and determine their propeties since deep levels can have a big impact on the electrical characteristics of a semiconductor, and on the properties of devices made from the semiconductor. Unfortunately, many of the conventional techniques for determining the properties of electronic states in semiconductors do not work on deep traps. As an example, carrier recombination at deep levels is quite frequently nonradiative, so the levels are not observed in luminescence measurements. Deep-level transient spectroscopy (DLTS) was developed to allow measurements of the properties of deep states in semiconductors to be made.[20] DLTS is one of several techniques which infer the properties of deep levels in the depletion region of a diode by observing changes which occur in the diode capacitance as the deep levels change charge state. Thermally stimulated capacitance and photocapacitance also work in this manner.

The basic principles of DLTS measurements will be illustrated by consider-

ing a Schottky barrier on an n-type semiconductor. We assume that deep levels which have a much larger capture cross section for electrons than for holes are present in the depletion region of the Schottky barrier. These levels are majority carrier deep levels since they capture the majority carrier in the semiconductor. Fig. 1.2 illustrates this situation. Part (a) of the figure shows the Schottky barrier under reverse bias. The occupation of the deep levels as a function of position has been indicated in the figure. If the bias on the device is reduced (or if it is forward biased) as in part (b) of Fig. 1.2, carriers are introduced into the depletion region and captured by the traps which are present in the depletion region. If the bias is returned to its original value, the depletion width W will be larger than before because of the charges trapped in the depletion region. Since the capacitance of the device is given by

$$C = \frac{\epsilon A}{W}, \tag{1.8}$$

the capacitance of the device will be reduced. Immediately following the bias pulse, the carriers will be thermally emitted (d) with emission rate e_n from the deep levels. As the concentration of trapped charges decreases, C will increase until it returns to its initial value. To summarize, applying a voltage pulse to the reverse biased diode results in a capacitance transient. The characteristics of the transient are related to deep levels in the depletion region of the diode. DLTS is the production and analysis of such transients to determine the properties of the deep levels giving rise to the capacitance transients.

Let the concentration of a particular deep state as a function of distance from the barrier be $N_d(x)$ and let the trapped charge at some time t after a bias pulse be $n_d(x)$ where $0 \leq n_d(x) \leq N_d(x)$. If $N_d(x) \ll N_s$ where N_s (the shallow level concentration) is assumed to be constant, the change in the depletion width (ΔW) caused by the filled deep levels in a region of width Δx at postion x is

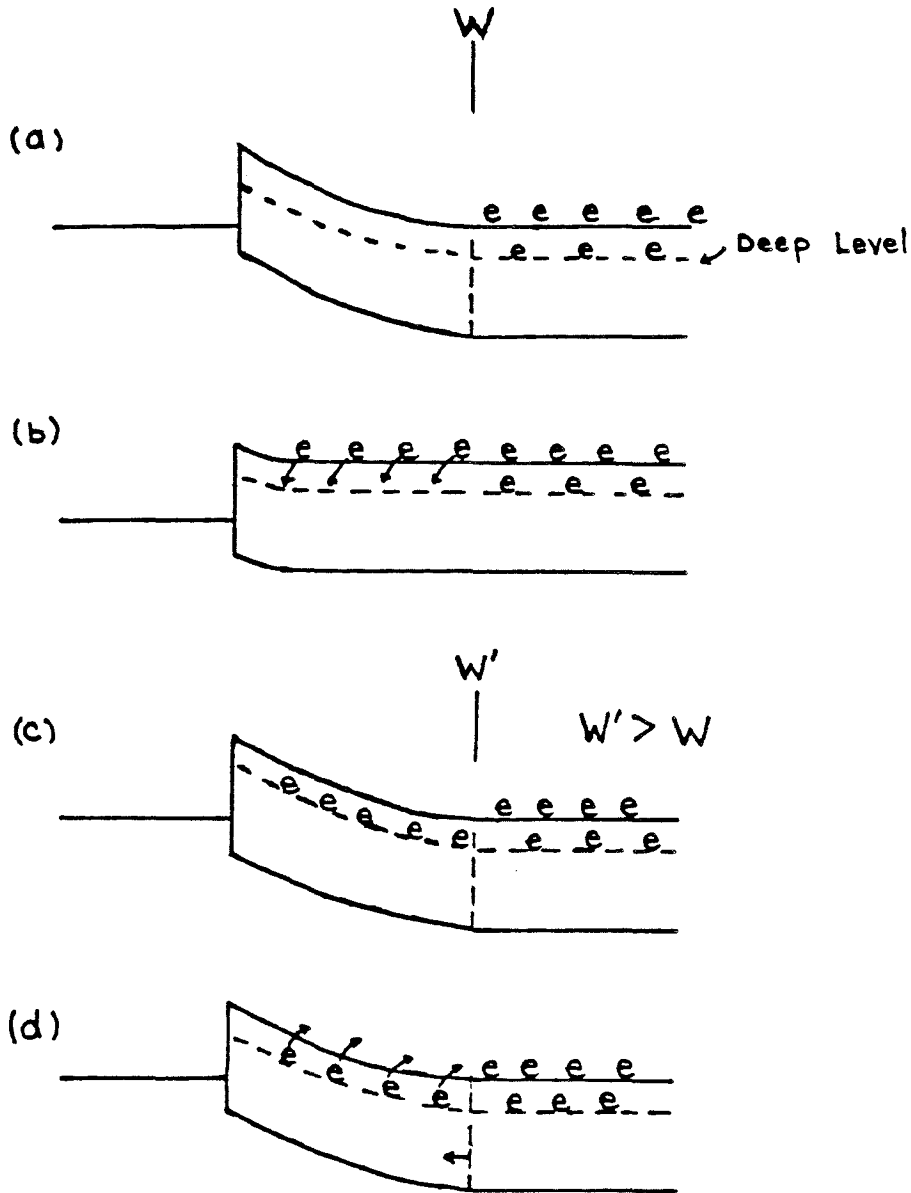

Figure 1.2: Band diagram as a function of position for a reverse biased Schottky barrier on an n-type semiconductor with deep levels in the depletion region.(a) Diode is in steady state. Depletion width is W.(b) The reverse bias on the diode is reduced and deep levels capture electrons. (c) The bias is returned to its original value, but the depletion width (W′) has increased because of the trapped charge in the depletion region. (d) As the charge is thermally emitted to the conduction band, the depletion width returns to its original value.

given by

$$\Delta W = \frac{n_d x \Delta x}{N_s W}. \tag{1.9}$$

The change in capacitance ($\Delta C(x)$) caused by filling these levels is given by

$$\frac{\Delta C(x)}{C} = -\frac{n_d(x)}{N_s W^2} x \Delta x. \tag{1.10}$$

Eq. 1.10 can be integrated to get the total change in capacitance at time t,

$$\frac{\Delta C}{C} = -\frac{1}{N_s W^2} \int_0^W n_d(x) x dx. \tag{1.11}$$

The trapped charges will be thermally emitted back to the conduction band following the bias pulse with rate e_n which is the thermal emission rate. The concentration of trapped charges at position x at time t ($n_d(x,t)$) is an exponential in time with rate e_n. From Eq. 1.11 ΔC must also be an exponential in time with rate e_n,

$$\Delta C = \Delta C_0 e^{-e_n t}. \tag{1.12}$$

In the bulk semiconductor the thermal emission rate and the electron capture rate for a deep level must be equal by detailed balance. The thermal emission rate is usually proportional to a Boltzmann factor $\exp(-\Delta E/kT)$ where ΔE is the depth of the level relative to the conduction band edge. In Ref. 21 it is shown that these two facts lead to a thermal emission rate given by

$$e_n = \frac{\sigma_n v_n N_c}{g} \exp(-\Delta E/kT), \tag{1.13}$$

where σ_n is the capture cross section for electrons, v_n is the electron thermal velocity, N_c is the effective density of states, and g is the degeneracy of the level.

As was stated above, in DLTS measurements a bias pulse is applied to a diode and the resulting capacitance transients (Eq. 1.12) are analyzed to determine the properties of the deep levels in the diode depletion region. The decay rate associated with the capacitance transients gives e_n. If the emission

rate is found at a range of temperatures, the slope of a plot of the logarithm of e_n/T^2 as a function of $1/T$ (an Arrhenius plot) will give the depth of the level relative to the conduction band (the division by T^2 takes into account the temperature dependence of v_n and N_c in the prefactor to the exponential which gives e_n). If N_d is not a function of position and all of the traps in the depletion region are filled by the bias pulse, Eq. 1.11 can be integrated to give

$$\Delta C_0 = C\frac{N_d}{2N_s}. \tag{1.14}$$

The initial value of the capacitance transient can be used to determine the deep-level concentration relative to the shallow level concentration. If the bias pulse is increased by a small increment, traps in a new part of the depletion region which is closer to the Schottky barrier will be filled and ΔC_0 will increase. The increase can be related to the concentration of traps in the new region through Eq. 1.10 where x and Δx are obtained from a plot of depletion width as a function of applied bias. In this manner a profile of the deep-trap concentration as a function of position can be obtained. If the pulse is fast enough so that not all of the traps are filled, the initial amplitude of the capacitance transient as a function of pulse duration can be used to determine the capture cross section of the trap.

The above analysis has many simplifying assumptions. The effects of electric fields in the depletion region on e_n have been neglected. The occupation of the deep levels at the edge of the depletion region has not been considered. Additionally, if the concentration of deep-levels is too large, the linear analysis given above does not work, and the transients will not be exponentials. However, the above discussion does present the fundamental principles of the technique. It can easily be extended to the case of p-n junctions where one side of the junction is heavily doped or to Schottky barriers on p-type semiconductors. One difference between the p-n junction and Schottky barrier measurements is that,

in a p-n junction, minority carriers can be introduced into the depletion region by forward biasing the diode. This makes it possible to see traps which have a larger capture cross section for minority carriers than for majority carriers (minority carrier traps). With a Schottky barrier there is very little minority carrier current when the diode is forward biased, so only majority carrier traps are observed.[22] There are a number of methods for analyzing capacitance transients to obtain e_n and ΔC_0 which are the two quantities used to determine the properties of the traps. The rate window concept is discussed and used in the analysis of capacitance transients in Chapter 3.[20]. A simple DLTS system is also described in Chapter 3. For a more complete analysis of the DLTS technique see, for example, Refs. 20, 21, and 24.

1.4 SUMMARY OF THESIS

Chapter 2 of this thesis presents the results of a study of current transport perpendicular to AlAs layers in AlAs/GaAs heterojunctions with an emphasis on observing tunneling currents. The purpose of this study was to determine whether coherent electron transport across AlAs barriers could be observed and to look for quantum effects in tunneling through structures where the characteristic dimensions were small enough that such effects should occur. Additionally, it was hoped that some insights into the electronic properties of AlAs, GaAs, and AlAs/GaAs heterojunctions would be obtained. The samples used in this study were grown by MOCVD and MBE and consisted of one or more thin AlAs barriers sandwiched between two thick layers of degenerate GaAs. A description of the preparation of devices on the samples and of the I-V, first derivative, second derivative and capacitance measurements made on the devices is given. Measurements were made as a function of temperature, device area, AlAs layer

thickness, and the doping of the AlAs and GaAs. A discussion of current transport as a function of temperature is presented. Current transport at high temperatures in MOCVD samples with a single, p-type AlAs barrier was due to thermionic emission over the AlAs barrier. At lower temperatures the dominant current transport mechanism depended on barrier thickness. Calculations of zero-bias resistance as function of barrier width using the transfer Hamiltonian method and a WKB approximation are presented and compared with experimentally measured resistances. The comparisons suggest that leakage currents are dominant in samples with barriers thicker than 100 Å, while tunneling is the dominant transport mechanism in structures with 50 Å thick barriers. Results of inelastic tunneling measurements on the samples are presented. Inelastic measurements reveal structure at the GaAs and AlAs longitudinal optical phonon energies which is attributed to a self-energy effect in the GaAs and the inelastic excitation of AlAs phonons by the tunneling electrons. In addition to being the first observations of inelastic tunneling in the AlAs/GaAs system, these results confirmed the fact that tunneling currents were being observed in samples with thin barriers. Measurements on samples with n-type barriers are also discussed. N-type barrier samples did not have the proper dependence of zero-resistance on AlAs layer width, although reproducible structure was still observed in the derivative spectra. An explanation for the differences between n and p-type barriers based on band bending in the AlAs layer is given. Similar measurements made on MBE grown structures did not give reproducible or consistent results. The differences between MOCVD and MBE grown sampes are also discussed.

Devices prepared on MOCVD grown samples with two AlAs layers exhibited negative differential resistances. These are attributed to resonant tunneling effects and are the first observation of such effects in MOCVD grown AlAs/GaAs double barrier structures. A discussion of the origin of the negative resistances is given along with an explanation of asymmetries with respect to bias in the

I-V curves.

A study of deep levels in n-type and p-type CdTe using DLTS techniques is described in Chapter 3. The purpose of this study was to gain an understanding of the deep-level defect structure of CdTe, and of changes in this structure produced by various annealing treatments. Characteristics of deep levels which are seen in all of the n-type CdTe samples are presented. These levels are attributed to native crystal defects, to impurities which commonly occur in CdTe, or to native defect-impurity complexes. Certain levels were also common to all of the p-type CdTe samples. A discussion of the properties of these levels is given. They are also identified as due to native defects or impurities. Determining the physical origin of the deep states common to all the CdTe samples is complicated by the strong role native defects and defect complexes play in the electronic properties of CdTe. Certain levels in In-doped, n-type CdTe were not observed until the sample had been illuminated at low temperatures with above band gap light. DLTS spectra exhibiting these effects are presented along with a possible explanation for the unusual optical characteristics of these levels. Other levels were induced to appear by stressing the CdTe crystals. A discussion of these levels is also given. In general it was observed that anneal conditions did not have a large effect on the levels present in the CdTe, although they did have a large effect on the amplitudes of such levels. The effects of modest sample heating on the DLTS spectra of the samples will also be discussed.

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CHAPTER 2

ELASTIC AND INELASTIC TUNNELING THROUGH AlAs/GaAs HETEROSTRUCTURES

2.1 INTRODUCTION

AlAs and GaAs both crystallize in the zincblende lattice structure. They are latticed-matched with lattice constants that differ by less than a few tenths of a percent. This allows the two materials or an alloy of them ($Al_xGa_{1-x}As$) to be grown on top of one another with very few strain induced defects at the growth interface while maintaining the zincblende structure. Techniques such as molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) have made it possible to grow crystalline heterostructures composed of layers of AlAs and GaAs or of the alloy $Al_xGa_{1-x}As$. Reproducible layers with thicknesses as small as 20 Å have been grown.[1] The interfaces between the layers have been estimated to be as abrupt as one or two monolayers.[2] The ability to produce such materials has generated considerable interest, both from the ability to study the fundamental physical processes occurring at the interfaces and from device applications of such materials. Some of these applications were discussed in Chapter 1. An undérstanding of transport perpendicular to AlAs/GaAs interfaces is important to these applications and may also add to our basic understanding of processes occurring at the interfaces or in the layers from which a heterostructure is formed. This chapter presents the results of a study of electronic transport perpendicular to crystals composed of one or more AlAs layers sandwiched between GaAs layers, with an emphasis on elastic and inelastic tunneling through the AlAs layers.

Electrons moving from GaAs to $Al_xGa_{1-x}As$ across a heterojunction must cross an energy barrier. This occurs because GaAs (which is direct) has a smaller bandgap than AlAs (which is indirect with its conduction band minimum occurring at the X-point). This causes a discontinuity in the conduction band and valence band at the interface between AlAs (or $Al_xGa_{1-x}As$) and GaAs. Most of the discontinuity occurs in the conduction band, causing a layer of AlAs to act as a barrier to electrons in the GaAs.[3] The conduction band offsets

between AlAs and GaAs form the sides of the barrier.

Studies of current transport perpendicular to a single $Al_xGa_{1-x}As$ barrier structure sandwiched between two layers of GaAs have been reported.[4,5,6,7] In most of these cases the samples were grown by MBE and the barrier thicknesses were greater than 300 Å. The currents observed in these studies were attributed to two main processes (Fig. 2.1). The first is thermionic emission over the offset barrier at temperatures greater than about 150 K.[2,3] The second is tunneling through the barrier.[1,4] Tunneling was observed at low temperatures but with biases comparable to the $Al_xGa_{1-x}As$/GaAs conduction band offset. Several of the studies indicated that more current passed through the barrier at low temperatures and biases than expected from both thermionic emission and tunneling[4,5] indicating that some form of leakage was occurring.

We have made measurements of the current-voltage (I-V), first derivative (dI/dV) and second derivative (d^2I/dV^2) curves, and capacitances of devices prepared on MOCVD and MBE grown samples with a single AlAs barrier imbedded in GaAs. The thicknesses of the AlAs barriers in this study were less than 300 Å. Thinner barriers were used to enhance the tunneling current through the barrier relative to other transport mechanisms, and, thus, to allow the study of elastic and inelastic tunneling at biases less than 100 mV. Transport measurements were made as a function of temperature, doping of the AlAs layers and GaAs layers, thickness of the AlAs barrier, and method of sample growth. In the MOCVD grown samples, the mechanisms for current transport were found to be critically dependent on the doping of the AlAs barrier. Samples with Mg-doped, p-type AlAs barriers behaved as expected for a tunneling structure. They exhibited thermionic emission at room temperature. At low temperatures tunneling was dominant in samples with barriers less than 100 Å thick, while leakage dominated for those with thicker barriers. The inelastic tunneling spectrum (second derivative spectrum) for samples with thinner barriers exhibited structure due to

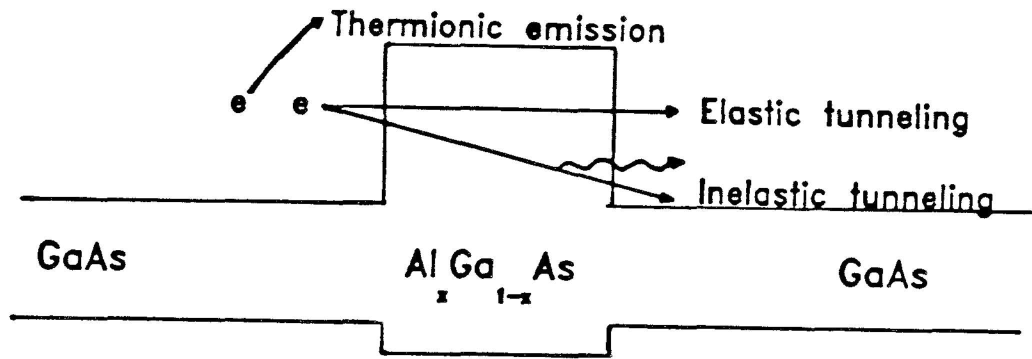


Figure 2.1: Schematic diagram of the conduction and valence band offsets for an $Al_xGa_{1-x}As$ /GaAs tunneling structure illustrating ideal transport mechanisms across the $Al_xGa_{1-x}As$ barrier. In general, these processes are in competition with other current transport mechanisms such as impurity assisted tunneling, edge currents, and hopping conduction across impurities.

a density-of-states effect in the GaAs caused by coupling between the electrons and longitudinal optical (LO) phonons in the GaAs. Additional structure was observed and attributed to the inelastic excitation of LO phonons in the AlAs by the tunneling electrons. This was the first observation of inelatic tunneling in the AlAs/GaAs system. When the AlAs barrier was doped n-type with Se, the low temperature sample resistance did not have the expected dependence on the AlAs layer thickness, yet reproducible structure was still present in the second derivative spectrum. Although a definitive explanation for the difference between n and p-type barriers has not been found, possible explanations will be presented below. Measurements were also made on a few MOCVD grown samples with high Al content $Al_xGa_{1-x}As$ barriers. Results were similar to those for AlAs barriers. Electronic transport perpendicular to the AlAs barriers in samples grown by MBE was consistent with tunneling at low temperatures, but no reproducible structure was visible in the inelastic tunneling spectrum for this material.

Samples composed of two AlAs barriers sandwiched between GaAs layers were also prepared by MOCVD. Resonant tunneling through the two barriers was observed. Similar observations have been made on MBE grown samples[8,9] and on MOCVD grown multiple quantum well lasers,[10] but this is the first such observation on a double AlAs barrier grown by MOCVD.

The rest of the chapter will discuss the measurements made on these samples and the conclusions that can be drawn from the measurements. Section 2.2 will describe the sample preparation and measurement techniques. In Section 2.3 the results of measurements on single barrier samples will be given along with a discussion of these results and the interpretations. Section 2.4 will present and discuss the results of measurements on samples with more than one barrier, followed by a summary and conclusions in Section 2.5.

2.2 EXPERIMENTAL PROCEDURES

2.2.1 Sample growth

The MOCVD samples used in this study were grown in an atmospheric pressure, cold wall, vertical chamber MOCVD reactor using commercially available trimethylgallium, trimethylaluminum, and arsine as sources. Hydrogen selenide provided Se which was the n-type dopant used. The p-type dopant was Mg. It was provided by bis(cyclopentadienyl) magnesium.[11] Growth temperatures were typically near 800 °C. The samples were grown by R.D. Burnham and the growth system and technique are more completely described elsewhere.[12,13]

Substrates for the MOCVD growths were ⟨100⟩ oriented, Si-doped GaAs wafers. The Si doping concentration was approximately 4×10^{18} cm^{-3}. Samples with a single AlAs barrier were grown as follows: An epitaxial Se-doped layer of GaAs was grown on top of the substrate followed by a thin layer of AlAs. A final Se-doped GaAs was then grown. The dopings in the GaAs layers were typically $1 - 5 \times 10^{18}$ cm^{-3}, and their thicknesses were approximately 3 μm. The AlAs layer was either doped n-type with Se or p-type with Mg. The doping concentrations were estimated to be about 1×10^{18} cm^{-3}. AlAs layer thicknesses from 50 to 250 Å were used. Samples with a single $Al_{.75}Ga_{.25}As$ barrier were also prepared as described above.

Samples with two AlAs barriers were grown by MOCVD following the same procedure used for single AlAs barrier samples except for the following: After the growth of the first AlAs layer, a thin undoped, GaAs layer followed by another AlAs layer was grown before the final GaAs layer was grown. The AlAs layers were doped p-type with Mg at about 1×10^{18} cm^{-3}. The thicknesses of the AlAs layers and central GaAs layer were estimated to be 50 Å.

The dopings given above for the AlAs and $Al_xGa_{1-x}As$ were estimates

based on measurements of doping as a function of the gas flow rates during growth of lower aluminum content $Al_xGa_{1-x}As$ and could be in error. The layer thicknesses are estimates from transmission electron microscopy (TEM) data on the growth of thin layers of AlAs, GaAs and $Al_xGa_{1-x}As$. Since the growth rates vary when the source gases are changed, the thicknesses given could be in error by 10 to 20 %. Later on in this chapter results will be presented which indicate that both the dopings and the thicknesses differ from the given values.

MBE samples were obtained from three different sources. All were grown on ⟨100⟩ oriented GaAs substrates doped with Si at greater than $1-2\times10^{18}$ cm^{-3} and had the same layered structure as the single barrier MOCVD samples. Three wafers were prepared by Dr. G. W. Wicks of Cornell University using a Varian Gen II MBE system. In these samples the initial GaAs layer grown on the substrate was 0.3 μm thick and doped with Si. The AlAs which was grown on the GaAs was nominally undoped. This layer was either 50, 100, or 150 Å thick (Cor 1, Cor 2, and Cor 3). The final GaAs layer was 0.7 μm thick and doped with Si. The dopings in the GaAs layers were 1×10^{18} cm^{-3}. The GaAs layers were grown at 640 °C. At the end of the growth of the layer nearest the substrate, the temperature was raised to 680 °C. The AlAs was then grown at 680-700 °C with a growth rate of 2500 Å/hour.

L. Peter Erickson of Physical Electronics grew two samples using a model MBE 425b Physical Electronics MBE. In these growths, the GaAs layer closest to the substrate was 0.85 μm thick. The final GaAs layer was 1.3 μm thick. The AlAs layer was nominally undoped with thicknesses of 50 and 65 Å(Phi 1 and Phi 2). The epitaxial GaAs layers were doped with Si at $1-2\times10^{18}$ cm^{-3}. The growth temperature for both the GaAs and AlAs was 600 °C. The AlAs growth rate was 4000 Å/hour.

The final two MBE samples came from Dr. L. Salmon of Hughes Research

Laboratories and were grown in a Riber 1000 MBE system. The first GaAs layer in these samples was 1.0 μm thick, while the final layer was 1.5 μm in thickness. Both layers were Si-doped at 5×10^{18} cm^{-3}. In one sample the barrier was 100 Å of undoped AlAs (MBE 359), while the next sample had a 100 Å thick $Al_{.3}Ga_{.7}As$ barrier (MBE 358) which was also nominally undoped. The growth temperatures for both of these samples was approximately 600 °C. The AlAs growth rate was around 4000 Å/hour, while the growth rate for the $Al_{.3}Ga_{.7}As$ was ~ 14000 Å/hour.

The widths of the AlAs and $Al_xGa_{1-x}As$ layers for all of the MBE samples were calibrated from measurements of the widths of thicker layers and errors of a few angstroms are reasonable.

Most of the results which will be presented in the next section deal with electrical measurements on the single and multiple barrier MOCVD grown samples. The MBE samples were studied for comparison with the MOCVD grown material. Table 2.1 lists the various samples used in this study and their characteristics.

2.2.2 Sample preparation

Devices were prepared on the wafers described above by defining mesas more than 4 μm in depth on the epitaxial GaAs face of the wafers and fabricating Au-Ge/Ni ohmic contacts on the surface of the mesa and on the GaAs substrate.[14] The first step in this procedure was to fully evaporate, at 10^{-6} torr, small quantities of a eutectic mixture of Au-Ge (12% Au, 78% by weight) from a tungsten boat onto the surface of the final epitaxial GaAs layer of the samples. The thickness of the Au-Ge film was usually slightly more than 1000 Å. Following this, a layer of Ni was deposited without breaking vacuum. The Ni layer was considerably thinner than the Au-Ge layer, although its thickness

TABLE 2.1

Sample	Growth Technique	Barrier Composition	Barrier Thickness	GaAs Doping (cm^{-3})	Barrier Doping (cm^{-3})
H003	MOCVD	AlAs	60 Å	Se – 6×10^{18}	Se – 1×10^{18}
H056	MOCVD	AlAs	60 Å	Se – 6×10^{18}	Se – 1×10^{18}
H083	MOCVD	AlAs	120 Å	Se – 5×10^{18}	Se – 1×10^{18}
H098	MOCVD	AlAs	175 Å	Se – 6×10^{18}	Se – 1×10^{18}
H099	MOCVD	AlAs	250 Å	Se – 7×10^{18}	Se – 1×10^{18}
H125	MOCVD	AlAs	50 Å	Se – 5×10^{18}	Mg – 1×10^{18}
H160	MOCVD	AlAs	50 Å	Se – 3×10^{18}	Mg – 1×10^{18}
H135	MOCVD	AlAs	100 Å	Se – 5×10^{18}	Mg – 1×10^{18}
H115	MOCVD	AlAs	150 Å	Se – 5×10^{18}	Mg – 1×10^{18}
H151	MOCVD	AlAs	150 Å	Se – 1.5×10^{18}	Mg – 1×10^{18}
H226	MOCVD	$Al_{.75}Ga_{.25}As$	80 Å	Se – 2×10^{18}	Se – 1×10^{18}
H244	MOCVD	$Al_{.75}Ga_{.25}As$	80 Å	Se – 2×10^{18}	Mg – 1×10^{18}
MBE 358	MBE	$Al_{.3}Ga_{.7}As$	100 Å	Si – 5×10^{18}	undoped
MBE 359	MBE	AlAs	100 Å	Si – 5×10^{18}	undoped
Cor 1	MBE	AlAs	50 Å	Si – 1×10^{18}	undoped
Cor 2	MBE	AlAs	100 Å	Si – 1×10^{18}	undoped
Cor 3	MBE	AlAs	150 Å	Si – 1×10^{18}	undoped
Phi 1	MBE	AlAs	65 Å	Si – 1×10^{18}	undoped
Phi 2	MBE	AlAs	50 Å	Si – 1×10^{18}	undoped
H283*	MOCVD	AlAs	50 Å	Se – 5×10^{18}	Mg – 1×10^{18}
H327*	MOCVD	AlAs	50 Å	Se – 5×10^{18}	Mg – 1×10^{18}

*double barrier samples, barrier separation 50 Å

Table 2.1: Characteristics of single and multiple barrier tunneling samples.

was never actually measured. Circles of positive photo-resist were prepared on the metallized sample surface using conventional photolithography. The samples were than placed in a Au etch (a potassium iodide solution) to remove the metal layer from the regions between the circles. Following this the sample was placed in a 4:1:1 H_2SO_4:H_2O_2:H_2O GaAs etch until the regions between the photo-resist protected surfaces had been etched through the top GaAs layer and the AlAs barrier. This left behind mesas (80-1000 μm in diameter) with the AlAs layers in the mesas electrically isolated from one another. The photo-resist was removed and the substrate face of the sample was metallized with Au-Ge/Ni as described above. The sample was then annealed at approximately 420 °C on a tungsten strip heater in a flowing forming gas (15%H, 85%He) for 15 seconds. The anneal is the final step in preparing Au-Ge/Ni ohmic contacts.[14,15] More will be said about the characteristics of these contacts in the discussion of results. The samples were affixed to standard TO-5 transistor headers using silver paint. The mesa surfaces were ultrasonically wire bonded to the pins on the header.

Samples were also prepared to study the properties of Au-Ge/Ni and Au Schottky barriers on GaAs in relation to tunneling measurements. A layer of GaAs doped with Se at 1×10^{18} cm^{-3} was grown by MOCVD on a degenerate GaAs substrate. A Au-Ge/Ni ohmic contact was prepared on the substrate face as described above. Following this, the sample was dipped in 4:1:1 etch to chemically polish the epitaxial GaAs layer, and Au or Au-Ge/Ni circles were defined on the epitaxial sample surface by evaporation through a shadow mask at 10^{-6} torr. Again the samples were mounted on headers.

2.2.3 Electrical measurements

The transport measurements made on devices prepared from the AlAs bar-

rier structures included *I-V* measurements, and the first derivative, and second derivative of the *I-V* curves. These measurements were made at temperatures from slightly greater than 300 K to 2 K. The *I-V* curves were obtained by applying dc currents to a device and measuring the resultant dc voltage across the device. The inverse of the slope of the *I-V* curve at biases of ±3 mV was defined to be the zero-bias resistance of the device. First derivative spectra were obtained by modulation techniques. The measurement frequency was 5 kHz. Second derivatives of the *I-V* curves were obtained by harmonic generation at a fundamental frequency of 50 kHz. A tunneling spectrometer similar to the one designed by Lambe and Jaklevic was built to make these measurements.[16] An extensive discussion of the theory behind the first and second derivative measurements and of the design of the measurement systems is given in Appendix A1.

Capacitance measurements were also made on these devices. The measurements were made as a function of bias, temperature, and frequency. A model 72BD Boonton capacitance meter operating at 1 MHz with a modulation voltage of 5 mV was used to make most of the measurements. Frequency dependent measurements from 10 kHz to 200 kHz were made using a lockin amplifier. The specifics of how this measurement was made are also included in Appendix A1.

2.3 OBSERVATIONS AND INTERPRETATIONS ON SINGLE BARRIERS

2.3.1 Ohmic contacts

With the increased use of GaAs in electronic devices, there has been considerable effort devoted to developing and studying ohmic contacts to GaAs.

Contacts to p-type GaAs are not too difficult to make.[17] Unfortunately, n-type GaAs is usually of greater interest because the small electron effective mass makes possible high electron mobilities and thus high speed device applications. The most commonly used contacts to n-type GaAs are based on Ge alloys. Au-Ge/Ni contacts are probably most frequently used.[14,15,18,19,20] A description of the preparation of these contacts was given in Section 2.2.2. Although this contact is still not well understood, it is believed that Ge acts as a donor in the GaAs and diffuses into Ga vacancies which are produced beneath the metal layer during the anneal stage of contact formation. The layer of GaAs under the metal becomes degenerate and has a low contact resistance to the metal.[19] The actual contact layer has been shown to be very complicated. Various phases of Ni, Ga, As, and Ge alloys form and penetrate into the GaAs. Which phases are present is dependent on anneal temperature, anneal time, and the composition of Au, Ge, and Ni in the starting metallization.[19,20] Kuan *et al.*[20] have suggested that the contact resistance is dependent on which of these phases is in contact with the Ge doped layer of GaAs beneath the contact, because this phase determines the amount of Ge doping in the GaAs layer. Most estimates of the penetration depth of the contact into the GaAs are around 1000 Å[18,20] although one source observed contact related effects to a depth of two or three microns.[21]

For the purposes of this study, a low resistance contact was required, so a Au-Ge/Ni contact was used. The layers of GaAs which were to be contacted on these samples were degenerately doped. In general, any metal could have been evaporated onto the GaAs to form a Schottky barrier with a depletion width small enough to allow significant tunneling currents. The result would be a contact with a low enough resistance for many applications, but in this particular case a better contact was required. For GaAs dopings as high as 5×10^{18} cm^{-3} the depletion width of a Schottky barrier would still be near 100

Å. Since the tunneling currents passing through AlAs barriers as thin as 50 Å were under study, this type of contact would have had a resistance of the same magnitude as the active region. The above mentioned Au-Ge/Ni contact was used because it was easy to prepare and could give contact resistances which were negligible compared to the tunneling resistances of the barriers, but care had to be taken in preparing the contact. In this study the anneal temperature was especially important.

When a comparison was made of second derivative measurements at 4.2 K on the Au and Au-Ge/Ni Schottky barriers described above (a Au-Ge/Ni Schottky barrier can be thought of as an unannealed contact), the spectra were quite different. The spectrum for the Au barrier was very similar to spectra reported in previous studies of tunneling through Schottky barriers on GaAs.[22] These results will be discussed later. Spectra for the Au-Ge/Ni barriers were dominated by 5-10 mV oscillations throughout the entire bias range studied. The positions of the oscillations and their amplitudes were not reproducible from device to device or even on the same device after it had been warmed to room temperature and cooled again to 4.2 K. The eutectic temperature of Au and Ni is near 360 °C. When AlAs barrier devices were prepared with contacts annealed at temperatures 10 or 15 °C above the eutectic temperature, the contact resistance was large enough that most of the voltage drop occurred across the contacts. This is in agreement with the published work.[20] The second derivative spectrum for such devices was also dominated by the oscillations seen in the Au-Ge/Ni Schottky barriers (Fig. 2.2). When the anneal temperature was increased to 420 °C the contact resistance decreased sufficiently to be negligible compared to the device active region. This was tested by comparing the impedance from contact to contact on the epitaxial GaAs layer before it was etched, to the device impedance after etching. For this anneal temperature, contact dependent oscillations were still observed on occasion, but their amplitude was considerably less

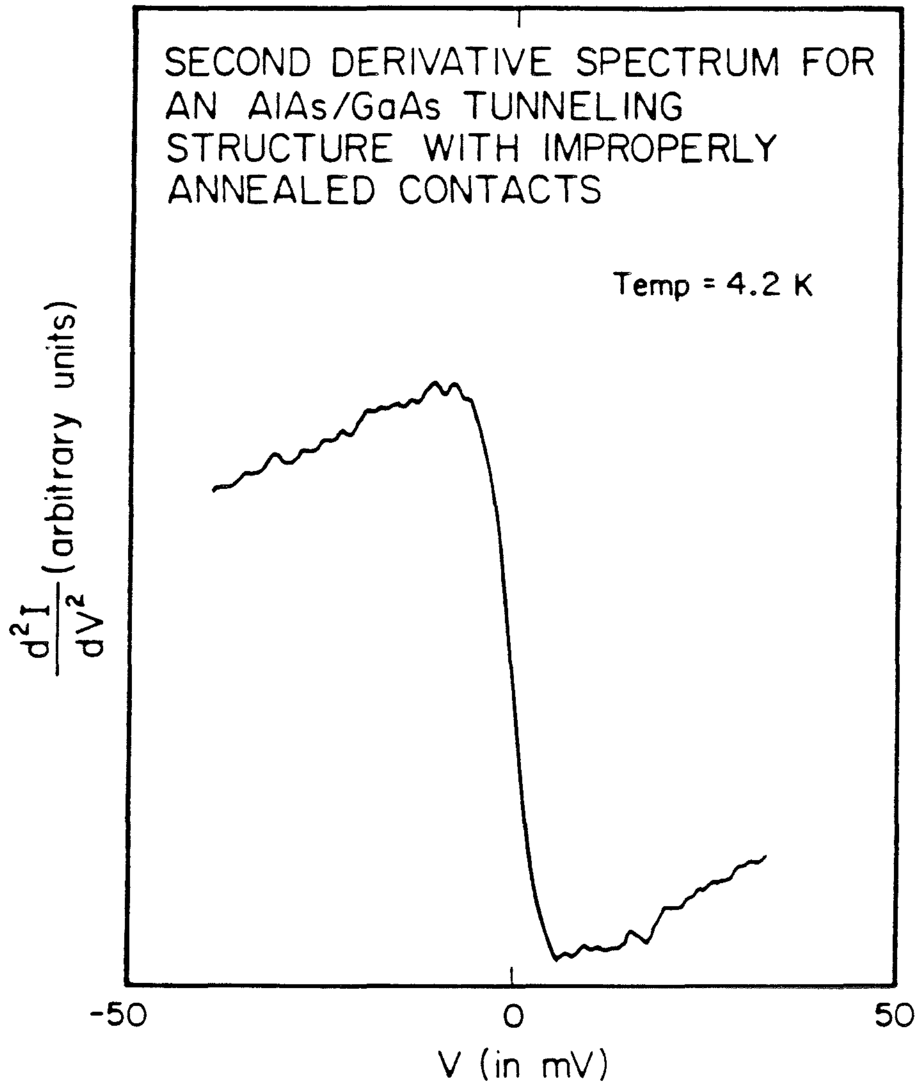


Figure 2.2: Second derivative spectrum for an AlAs/GaAs tunneling structure with improperly annealed contacts. The anneal temperature was approximately 380 °C, and the contact resistances were larger than the active region resistance. The oscillations in the spectrum were due to the contacts and are not reproducible from device to device.

than the device dependent peaks in the second derivative spectrum which will be discussed in Section 2.3.2.3. The results of this contact study provide verification that the observations described in the next section were due to device active regions (conduction through the barrier) rather than to contacts.

2.3.2 Transport through an MOCVD grown sample with a single, p-type barrier

2.3.2.1 Temperature dependent transport

The characteristics of the single barrier MOCVD samples were critically dependent on the doping of the AlAs layer. Fig. 2.3 shows I-V curves at 4.2 K for devices of the same diameter on samples with n-type and p-type AlAs barriers of different widths. The current passing through the p-type barriers decreases with barrier width as expected. For n-type barriers there is very little dependence on barrier width. Results of the measurements on MOCVD grown samples with a single p-type AlAs barrier will be presented first.

Fig. 2.4 is a plot of the base ten logarithm of I/T^2 as a function of $1/T$ for a fixed bias voltage of 0.1 V, where I is the current passing through the device, and T is temperature. The sample on which these measurements were made was H151 which has a p-type barrier with a thickness of ~150 Å. The curve has an exponential dependence at high temperatures indicating thermally activated currents in this temperature range. An activation energy of ~450 eV is derived from the slope in this region. This activation energy should correspond to an energy barrier presented to the electrons in the GaAs by the AlAs layer. Fig. 2.5 is a diagram of the conduction band minima energies, without including electrostatic band bending, for the single barrier structures under study. The energies were taken from Casey and Panish.[3] Two processes could be occurring.

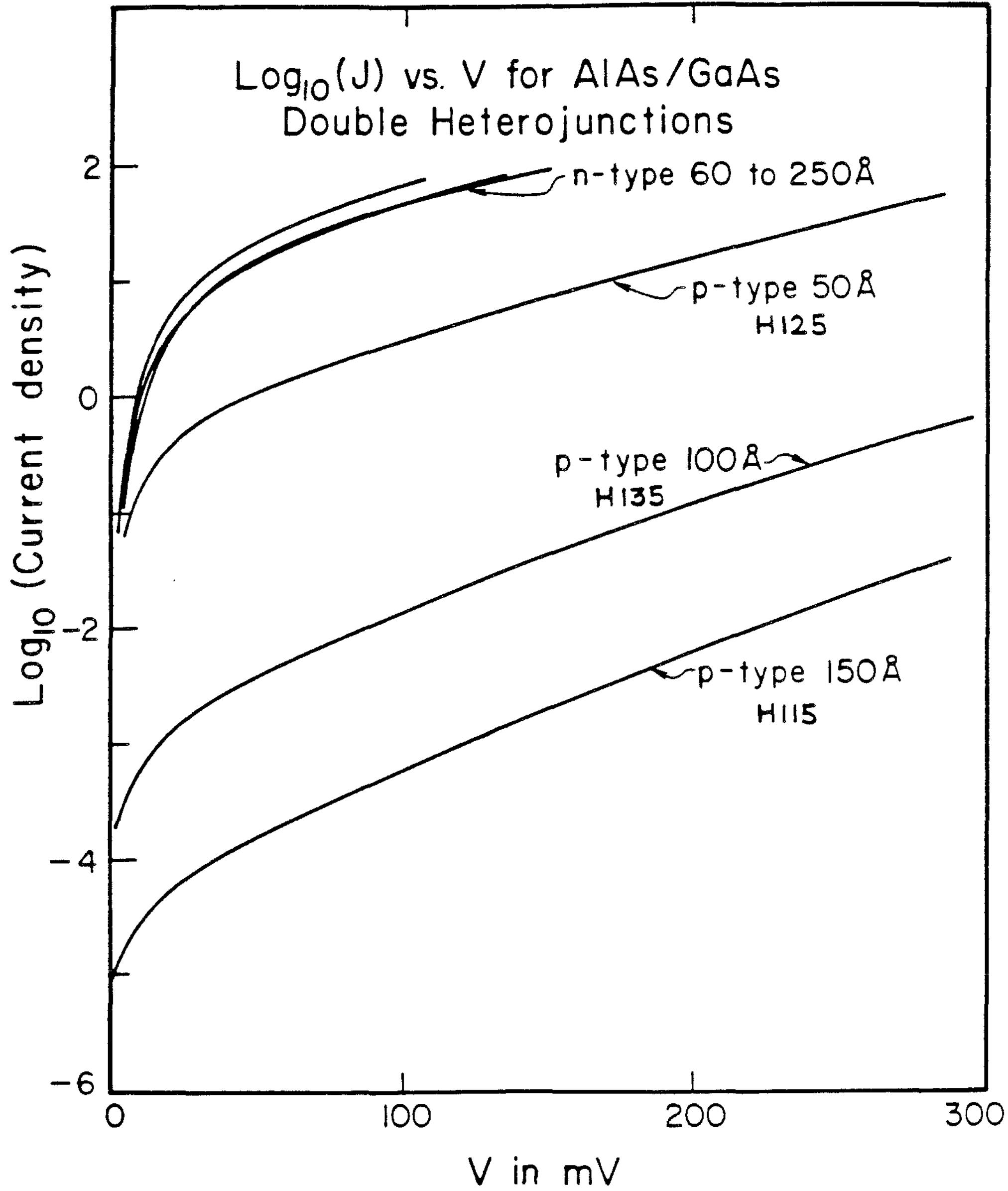


Figure 2.3: *I-V* curves at 4.2 K for devices of the same diameter on samples with n-type and p-type AlAs barriers of different widths.

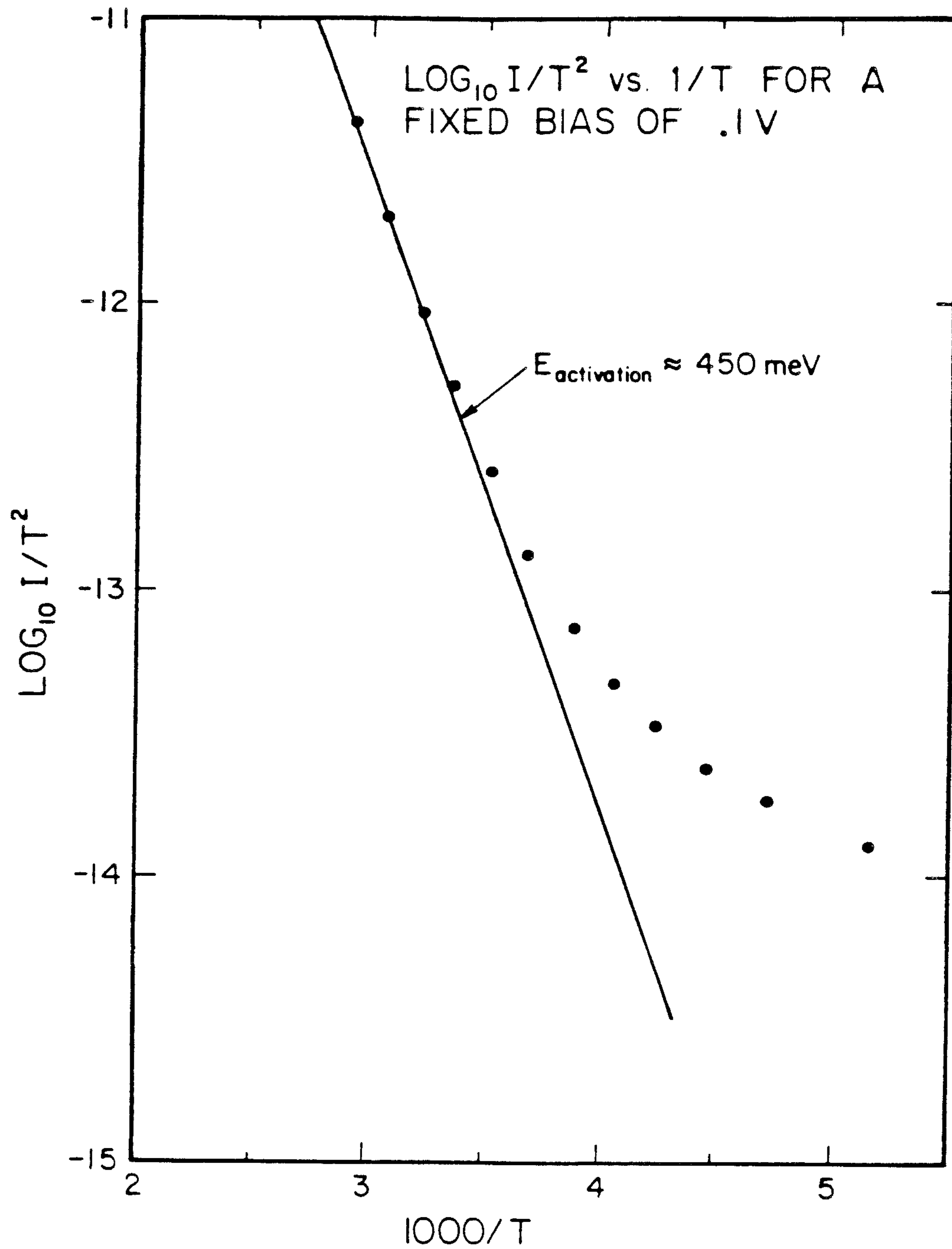


Figure 2.4: Logarithm of I/T^2 as a function of $1/T$ for a fixed bias voltage of 0.1 V. I is current and T is temperature. The sample used was H151.

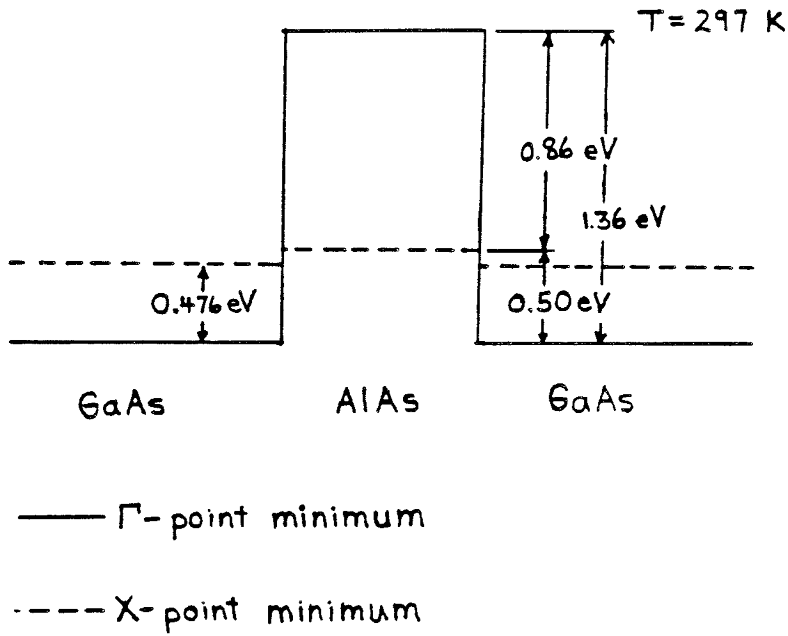


Figure 2.5: Conduction Band minima energies for an AlAs/GaAs tunneling structure. Electrostatic band bending or changes in band gaps due to the degeneracy of GaAs layers have not been included.

Some of the electrons at the GaAs Γ-point may have sufficient thermal energy to reach the AlAs X-point and pass over the barrier, or electrons may be thermally populating the GaAs X-point and then passing over the AlAs barrier. Both processes would be thermally activated with approximately the same activation energy as was measured. Band bending as a result of doping in the AlAs would actually change the average activation energy by about 50 millivolts for a 150 Å thick barrier, but the degeneracy of the GaAs layers would reduce the activation by a part of the Fermi energy. A theoretical study of transport through AlAs barriers has indicated that the probability of an electron in the Γ-point minium of GaAs passing through the AlAs by coupling to states at the AlAs L-point is considerably less than the probability of an L-point minimum GaAs electron of the same energy passing through the AlAs L-point.[23] It seems likely that the same symmetry considerations should apply to tunneling by coupling to the AlAs X-point. This seems to suggest that the second process given above is more likely. A comparison of the Richardson's constant obtained from Fig. 2.4 to the Γ-point and X-point Richardson's constants for GaAs (8 and 144 $A\text{-}cm^{-2}\text{-}K^{-2}$ respectively[23]) should clarify which path the electrons take. The measured constant, which is about .5 $A\text{-}cm^{-2}\text{-}K^{-2}$, is more nearly consistent with the first process, but this may only indicate that, although high temperature transport is thermally activated and involves conduction via the AlAs X-point, the transport mechanism is too complicated to be described by the simple thermionic emission model presented here. Other studies of MBE grown $Al_xGa_{1-x}As$ barrier samples have also reported a reduced Richardson's constant obtained from this type of measurement.[6]

2.3.2.2 Measurements and calculations of zero-bias resistance

At lower temperatures, the curve in Fig. 2.4 flattens out, indicating more

current is passing through the barrier than expected from thermionic emission. To determine the source of this extra current, measurements of *I-V* curves were made at 4.2 K. Some of these were presented in Fig. 2.3. Zero-bias resistances as a function of barrier width were determined from the *I-V* measurements and are plotted in Fig. 2.6.

Zero-bias resistances were also calculated using a simplified model for the single barrier system and were plotted on the same figure. The calculations were done following the method of Kurtin *et al.*[25] This scheme is based on Bardeen's transfer Hamiltonian model[26] which was presented in Chapter 1. A set of single particle wavefunctions is used to describe the electrons in each GaAs region. These wavefunctions are GaAs wavefunctions in the effective mass approximation which decay into the AlAs layer and into the opposing GaAs layer. A WKB approximation to the form of the wavefunction in the AlAs is used

$$\Phi_{AlAs}(x) = CK_x^{-\frac{1}{2}} e^{i\vec{k}_{\|}\cdot\vec{r}_{\|}} \times exp\left(-\int_{x_a}^{x} k_x dx\right). \qquad x_a < x < x_b \qquad (2.1)$$

In this equation x_a and x_b are the boundaries of the AlAs layer where a and b denote the two GaAs layers, C is a normalization constant, $\vec{k}_{\|}$ is the component of the wave vector of the electron parallel to the interface (assumed conserved), and k_x describes the attenuation of the electron wavefunction in the AlAs barrier. This attenuation constant may be thought of as the x-component of the complex wave vector of the electron in the AlAs barrier.

Substitution of these single particle wavefunctions into the time dependent Schröedinger equation results in an expression for the probability per unit time of a transition of an electron from a single particle wavefunction in one GaAs layer to a single particle wavefunction in the other layer of GaAs. A summation of this expression over all the states in the two GaAs electrodes taking into consideration the occupation of the states, leads to the following formula for the

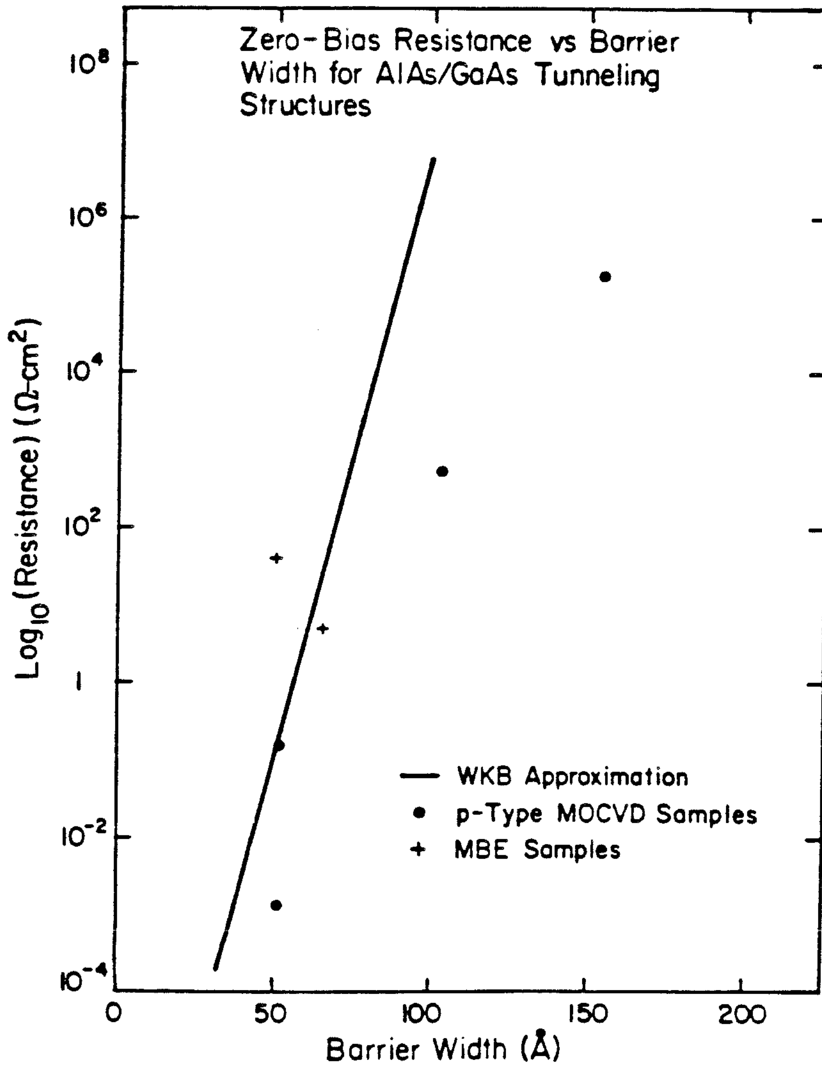


Figure 2.6: Calculated and measured zero-bias resistances as a function of barrier width. The calculations were based on a transfer Hamiltonian model and WKB wavefunctions.

current density

$$J(V) = \frac{2e}{h}\int dE \int \frac{d^2k_{\|}}{(2\pi)^2}(f_a(E) - f_b(E))exp(-2\int_{x_a}^{x_b} k_x(E,\vec{k}_{\|},x)dx). \quad (2.2)$$

In this equation f_a and f_b are Fermi factors for electrons in GaAs regions a and b, respectively. Eq. 2.2 corresponds to Eq. 1.4 in Chapter 1. The calculations were carried out for a temperature of zero degrees Kelvin, so f_a and f_b were either 1 or 0 as a function of E.

The complex wave vector k_x for a state depends on energy separation of that state from the AlAs band edges and on $k_{\|}$, the component of $\vec{k}$ parallel to the barrier. The energy dependence was obtained from a two-band model of the complex band structure in the AlAs $\langle 100\rangle$ direction.[27] The complex band used connected the Γ_{1c} conduction band minimum and Γ_{15c} light hole valence band maximum and was given by ($k_{\|}$ assumed equal to zero)

$$E = E_0 \pm \frac{\hbar^2\gamma}{m_{\pm}^*}(-k_x^2+\gamma^2)^{\frac{1}{2}} \qquad \gamma = \left(E_g/(\hbar^2(\frac{1}{m_+}+\frac{1}{m_-}))\right)^{\frac{1}{2}} \quad (2.3)$$

where m_+ was the electron effective mass, m_- was the hole effective mass (taken to be $.067m$ and $.074m$, respectively, where m is the free electron mass),[3] E_0 is the energy at the branch point in complex $\vec{k}$ space associated with these two band extrema, and the plus or minus sign is chosen depending upon whether E is greater or less than E_0. Neglecting other complex bands which might have contributed to the tunneling probability was reasonable, since, in the energy range of interest, the complex k associated with these bands had a large magnitude. Since this term enters as an attenuation length in an exponential, the tunneling probability associated with other complex bands would be much smaller than in the case of the band chosen.[27]

Following the method of Kurtin et *al.* again[25], we make the following approximation to the dependence of k_x on $k_{\|}$ given E

$$k_x(E,\vec{k}_{\|},x) = \left(k^2(E,0,x)+k_{\|}^2\right)^{\frac{1}{2}}. \quad (2.4)$$

Substitution of this into Eq. (2.2) allows the integration of $k_{||}$ to be approximated, leading to the following equation

$$J(V) = \frac{e}{2\pi h}\int dE\Big(\frac{exp(-2\int_{x_a}^{x_b} k(E,0,x)dx}{\int_{x_a}^{x_b}\frac{dx}{k(E,0,x)}}\Big)\big(f_a(E) - f_b(E)\big). \tag{2.5}$$

which was then integrated numerically to solve for $J(V)$ and the zero-bias resistance. In making this integration it was assumed that the applied bias voltage drop occurs linearly across the AlAs barrier. The range of integration in the energy integral of Eq. (2.5) was from the conduction band edge to the Fermi level of the GaAs electrode which was biased negative with respect to the other GaAs layer. The Fermi level in the GaAs was obtained from

$$\frac{1}{3\pi^2}\big(\frac{2m_+^*}{\hbar^2}E_f\big)^{\frac{3}{2}} = n \tag{2.6}$$

where n is the electron concentration in the GaAs taken to be 5×10^{18} cm^{-3}, and m_+^* is the GaAs electron effective mass. A value of $.067m$ was used for this.[3]

This model has a number of limitations in terms of describing the experimental situation. In particular, the WKB approximation is not valid in situations where the potential at the AlAs/GaAs interface changes much more abruptly than the wavelength of the Fermi electrons in the GaAs ($\sim$ 120 Å for n=5×10^{18} cm^{-3}). The resistances predicated by the model are very sensitive to the AlAs effective masses used, and values for these are not well known. The approximation implied in Eq. 2.4 is not valid in the center of the AlAs band gap because the value of $k_{||}x$ is not very sensitive to changes in E at this energy. Here, increasing $k_{||}$ while holding E fixed does not result in as small a value for $k(E,\vec{k}_{||},x)$ as predicted by Eq. 2.4. Band bending in the AlAs was not included. This limitation is not too important since k_x is not very sensitive to energy in the energy ranges that correspond to the low bias voltages used in the calculation of the zero-bias resistances. An additional problem, which has not

been addressed in this or any other study to my knowledge, is the impact on the tunneling current of local fluctuations in the electrostatic potential due to the ionized dopants in the barrier. These impurities are spaced around 100 Å apart on the average. This separation is close to the barrier widths. It is possible that the tunneling probability near one of these defects is greater than the probability calculated from the average potential barrier seen by the electrons, because of the strong band bending near the ionized dopant. In general, the slope of the calculated line comes from fairly fundamental considerations of the physical properties of the AlAs and is as valid as the complex band structure in Eq. (2.3) and the trapezoidal barrier shape used in the calculation are, while the intercept is more model dependent and may be off by quite a bit.

In spite of the above limitations, for barrier thicknesses near 50 Å, the MOCVD samples had resistances that agreed reasonably well with the calculations (Fig. 2.6). For thicker barriers the measured zero-bias resistance fell below the calculated value. Fig. 2.6 shows that the deviation of the measured zero-bias resistances from the calculated values increased as barrier thickness increased. This suggests that some form of leakage was dominating current flow through the thicker barriers, while the main contribution to the current through the thinner barriers was from tunneling. It is also interesting to note that an increase in resistance of an order of magnitude should occur for a 7 Å change in thickness. From Fig. 2.6 we see that, although sample H125 and H160 were assumed to have the same AlAs layer thickness, the AlAs barrier in H160 was probably thinner. The tunneling measurement gives a sensitive test of thickness, but, since tunneling currents will always pass through the thinnest part of a barrier, the decreased resistance in H160 does not necessarily imply that the average barrier width was less, but rather that the minimum barrier width was less.

Possible leakage mechanisms in the thicker barriers might include conduc-

tion through crystal defects in the AlAs, hopping conduction across deep levels in the AlAs gap, and currents resulting from edge effects. Fig. 2.7 contains plots of the base ten logarithm of zero-bias resistance as a function of the logarithm of device area for two samples, H160 and H135. The AlAs barrier in H160 was approximately 50 Å thick and the slope of the line passing through the points corresponding to the highest resistances is near -2, indicating current was proportional to area (points of highest resistance were used under the assumption that, if leakage were occurring, it would be less significant in these devices). In fact, the three points marked with an x were measurements on devices in close proximity (within 5000 Å of one another), and the slope for these points is almost exactly -2. The spread in the rest of the points probably reflects variations across the wafer in the thickness of the AlAs layer (resistances have an exponential dependence on width) rather than leakage. These results are consistent with the interpretations given above for Fig. 2.6, which indicate that the current flowing through devices prepared on H160 was tunneling current and should have been proportional to area. In contrast, the resistance as a function of area plot for H135 has a slope between -1 and -2. In Fig. 2.6 sample H135 is one of the first samples to show large deviations in resistance from the tunneling calculations, suggesting that the leakage observed in H135 may have been due in part to edge effects.

Variations of slightly more than an order of magnitude in zero-bias resistance occurred for samples with barriers thicker than H135. Although the device resistances for these samples decreased as device area increased, the variations made it harder to determine how resistance scaled with diameter, because the area of the largest device used in the measurements was only two orders of magnitude larger than the area of the smallest device. The resistivities given in Fig. 2.6 for these samples were the largest obtained. Measurements of the first and second derivatives of the I-V curves gave an additional indication that tunneling

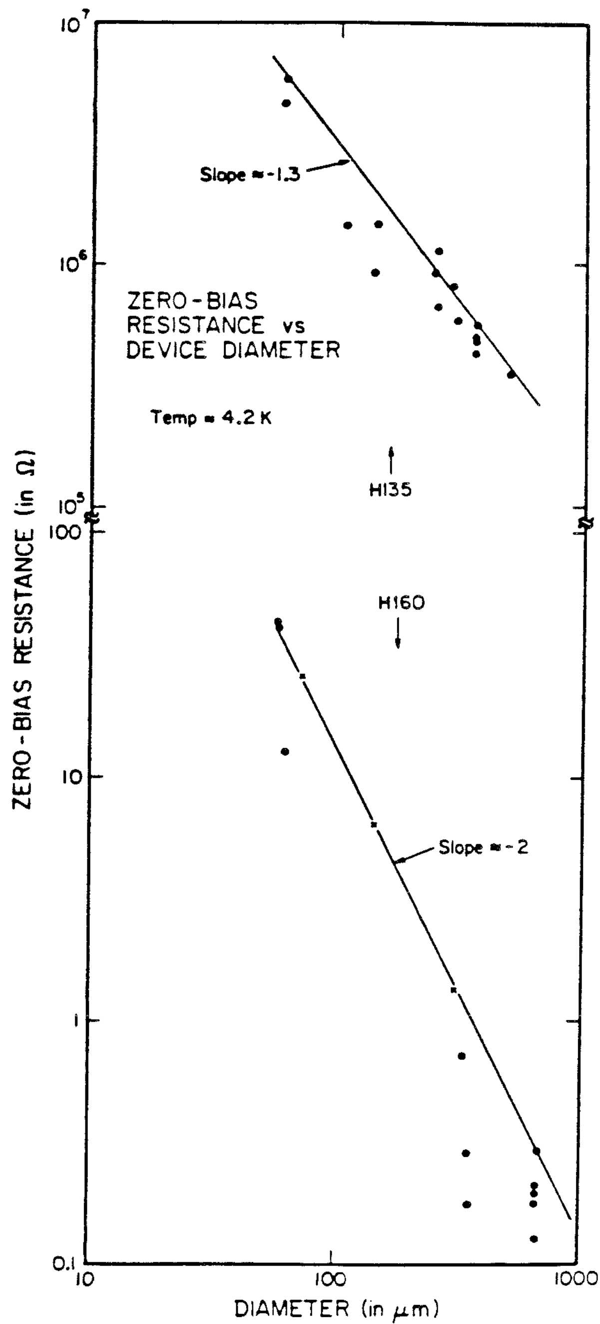


Figure 2.7: Base ten logarithm of zero-bias resistance as a function of the logarithm of device area for devices fabricated on H160 and H135. The measurements were made at 4.2 K.

was being observed in the samples with thinner barriers.

2.3.2.3 Inelastic tunneling measurements

When first and second derivatives of the *I*-*V* curves of the MOCVD samples with a single, 50 Å thick, p-type, AlAs barrier were made, reproducible structure was observed at the GaAs and AlAs longitudinal optical (LO) phonon energies. Fig. 2.8 gives *I*-*V* and first derivative curves for devices made from sample H125 and H160. Although the first derivative spectra for the two samples differ, both samples exhibit a cusp at approximately 36 meV in both bias directions. This has been labeled **a** in Fig. 2.8. In the spectrum associated with H160 there is also a conductance peak at zero-bias and additional structure at 70-80 meV. A second derivative spectrum for H125 is given in Fig. 2.9. The derivative of the cusp seen in dI/dV is present at $\sim$ 36 meV and has once again been labeled **a**. An additional peak is present near 50 meV (between 47.5 and 49.0 meV) in both bias directions and has been labeled **b**.

The structure which has been labelled **a** corresponds in energy to the GaAs LO phonon energy. Observations similar to this have been made in tunneling through Schottky barriers formed on degenerate GaAs.[22,28] A second derivative spectrum for a Au Schottky barrier on GaAs (the preparation of which was previously described) has been included in Fig. 2.10. The Schottky barrier observations have previously been attributed to a self-energy effect in the GaAs electrode caused by electron-optical phonon interactions.[28]

An important part of this explanation is that inelastic excitations in a tunnel barrier increase the probability of an electron passing through the barrier as the bias is increased above the excitation energy. There is a threshold voltage in the *I*-*V* curve, corresponding to the excitation energy, above which there is a change in the slope of the *I*-*V* curve (as was shown in Chapter 1). As the bias

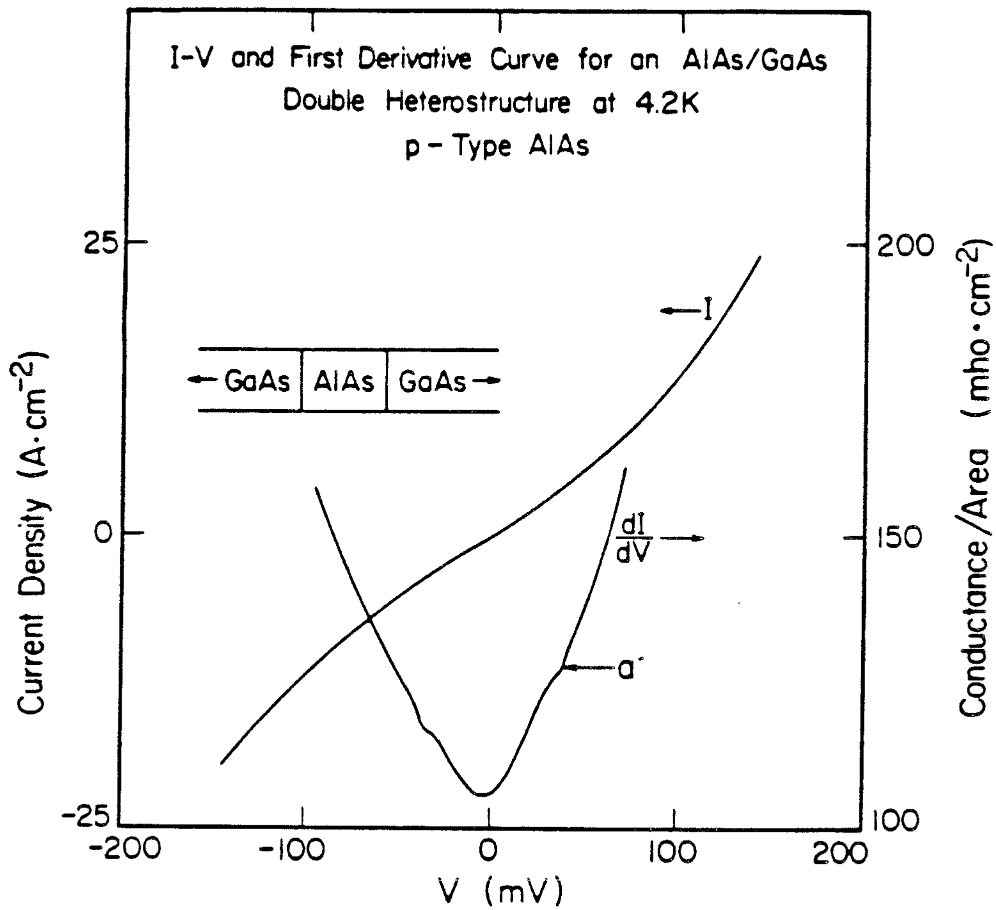


Figure 2.8: *I-V* and first derivative curves for devices made from H125 and H160. Measurements were made at 4.2 K. The cusp labeled **a** is attributed to a density-of-states effect in the GaAs electrode layers caused by electron-optical phonon coupling in the degenerate GaAs.

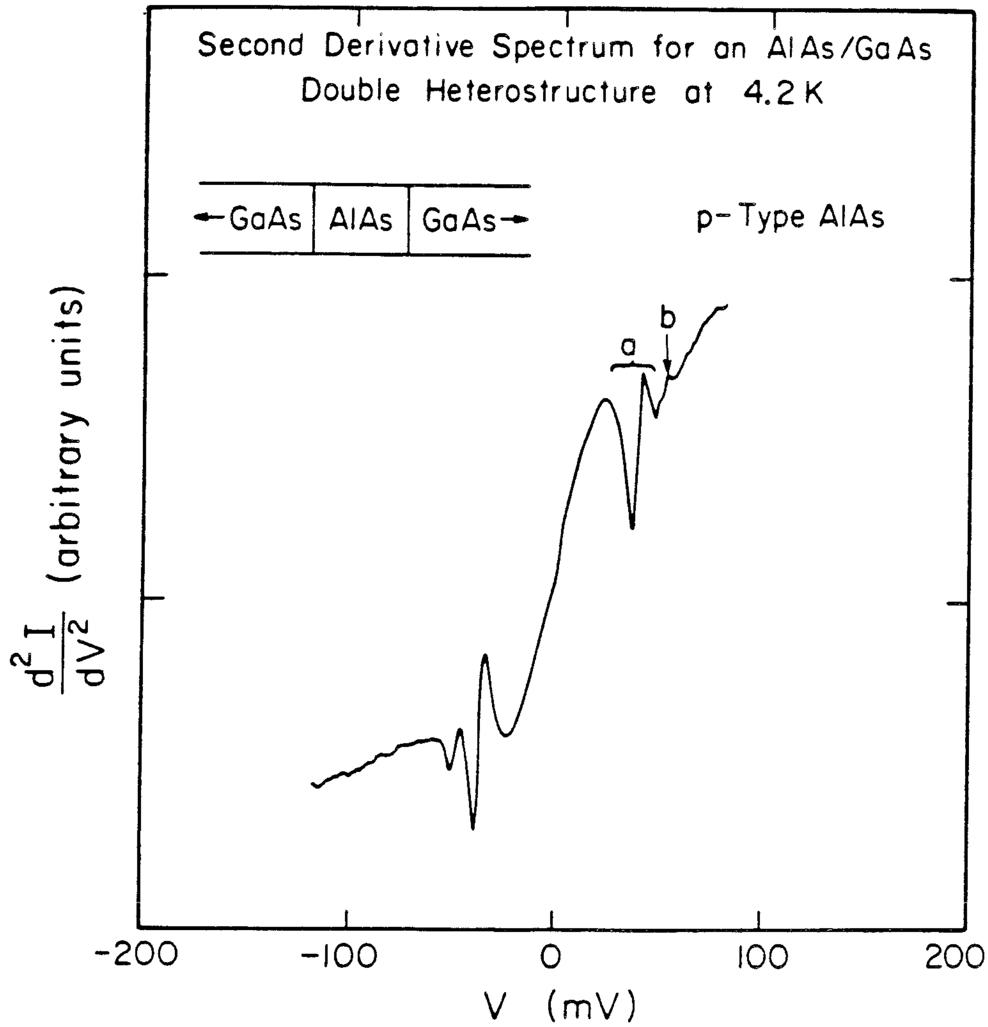


Figure 2.9: Second derivative spectrum at 4.2 K for a device fabricated on sample H125. The structure labeled **a** is associated with a density of states effect caused by electron-optical phonon coupling in the GaAs layers. The peak labeled **b** is caused by the inelastic excitation of AlAs longitudinal optical phonons by the tunneling electrons.

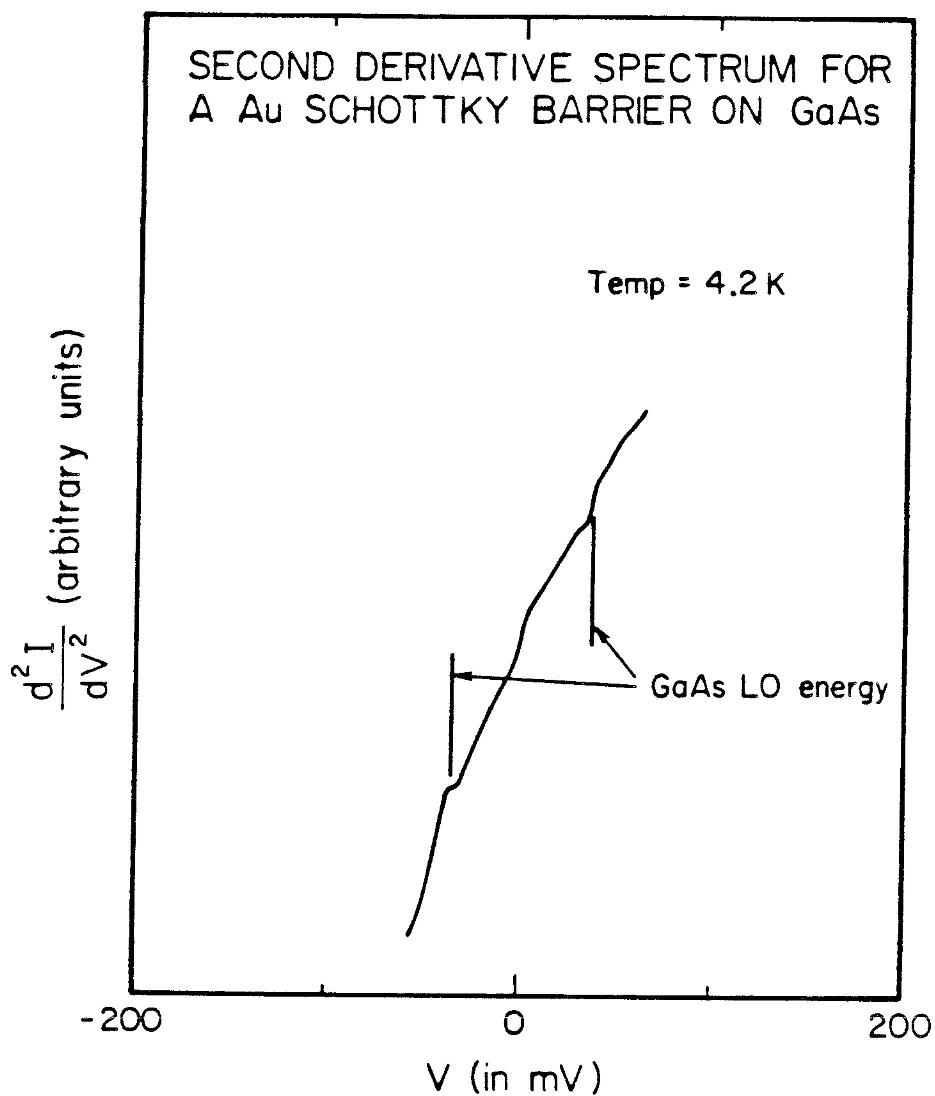


Figure 2.10: Second derivative spectrum at 4.2 K for a Au Schottky barrier on degenerate GaAs. Structure due to a density of states effect caused by electron-optical phonon coupling in the degenerate GaAs is visible in forward and reverse bias.

is increased in the reverse direction the same change should occur. Thus the first derivative should show symmetric steps at the excitation voltage while the second derivative should exhibit peaks which are antisymmetric with respect to bias. The structure in the Schottky barrier spectrum appears as a cusp rather than a step in the first derivative and is is symmetric with respect to bias in the second derivative, suggesting that it is not an inelastic excitation. Davis *et al.*[28] was able to model the Schottky barrier second derivative spectrum by considering a change in the density of states in the degenerate GaAs at energies above and below the Fermi level which were equal to the LO phonon energy. The changes were caused by the phonon contribution to the dielectric function governing the interaction of the electrons with the lattice (polaron effects). In one bias direction the structure observed arose because of the change in the density of states at energies greater than the Fermi energy, and in the other bias direction it reflects the change in the density of states below the Fermi level energy. The same effects would be expected to occur in the AlAs tunnel barriers studied here. For this reason and because the structure seen in forward bias in the GaAs Schottky barrier second derivative spectrum (Fig. 2.10) closely resembles structure **a** seen in the AlAs tunnel junction spectrum (Fig. 2.9), structure **a** is attributed to the same effect. One difference between the structures in the GaAs Schottky barrier and AlAs tunnel junction is that the structure in the AlAs tunnel junction is antisymmetric with respect to bias. This occurs because the AlAs tunneling structure is symmetric and, at a bias of 36 mV of either polarity, both the above and below Fermi level contributions to changes in the density of states will be contributing to the structure observed, giving rise to an antisymmetric second derivative spectrum.

The peak at ~50 meV is attributed to the inelastic-excitation of AlAs LO phonons by the tunneling electrons. The slight deviation of the excitation energy from previously published values for the phonon energy of 50 meV[29] may be

accounted for in a number of ways including the fact that the 50 Å thick barrier may be thin enough that its properties could deviate slightly from the bulk properties of AlAs. These deviations might be the result of the termination in GaAs of phonons confined in the thin AlAs layer or they may arise from strain in the AlAs layer due to the small lattice mismatch between GaAs and AlAs. Additionally, there could be some grading between the GaAs and AlAs. This would also have an impact on the termination of the AlAs phonons, especially if the vibration amplitude is large near the interface as it would be in the case of surface phonons associated with the interface.

These inelastic tunneling results were completely reproducible across wafer H125. For purposes of comparison, Fig. 2.11 presents second derivative spectra for both H125 and H160 in the ± 100 meV range. In both cases the region from -60 meV to 60 meV has been fitted to a straight line, and then this line has been subtracted off as a background. The spectra are very similar with structures a and b observable in both. The voltage range of Fig. 2.11 includes the decrease in conductivity observed in Fig. 2.8 for H160 near 70-80 meV. Although this structure has not been completely identified, it may be a Fermi level effect or due to the excitation of plasma oscillations in the degenerate GaAs.[30] The doping profile in the GaAs for H160 is actually different from that of H125. In H125 the GaAs is doped at 5×10^{18} cm^{-3} uniformly across the GaAs layers. In H160 the doping is 6×10^{18} cm^{-3} up to 0.5 μm either side of the barrier where the doping drops to 2.5×10^{18} cm^{-3}. Lowered doping near the barrier would lower the energy associated with Fermi level effects and the energies of either bulk or interface plasma oscillations. It might have an effect on the strength of the coupling to plasmons. Additionally, Fig. 2.6 suggests that the thickness of the AlAs barrier in H160 may be less than in H125 because of its lowered zero-bias resistance. This may also alter the magnitude of effects associated with inelastic excitations in the barrier. It is possible the effects similar to the decrease in

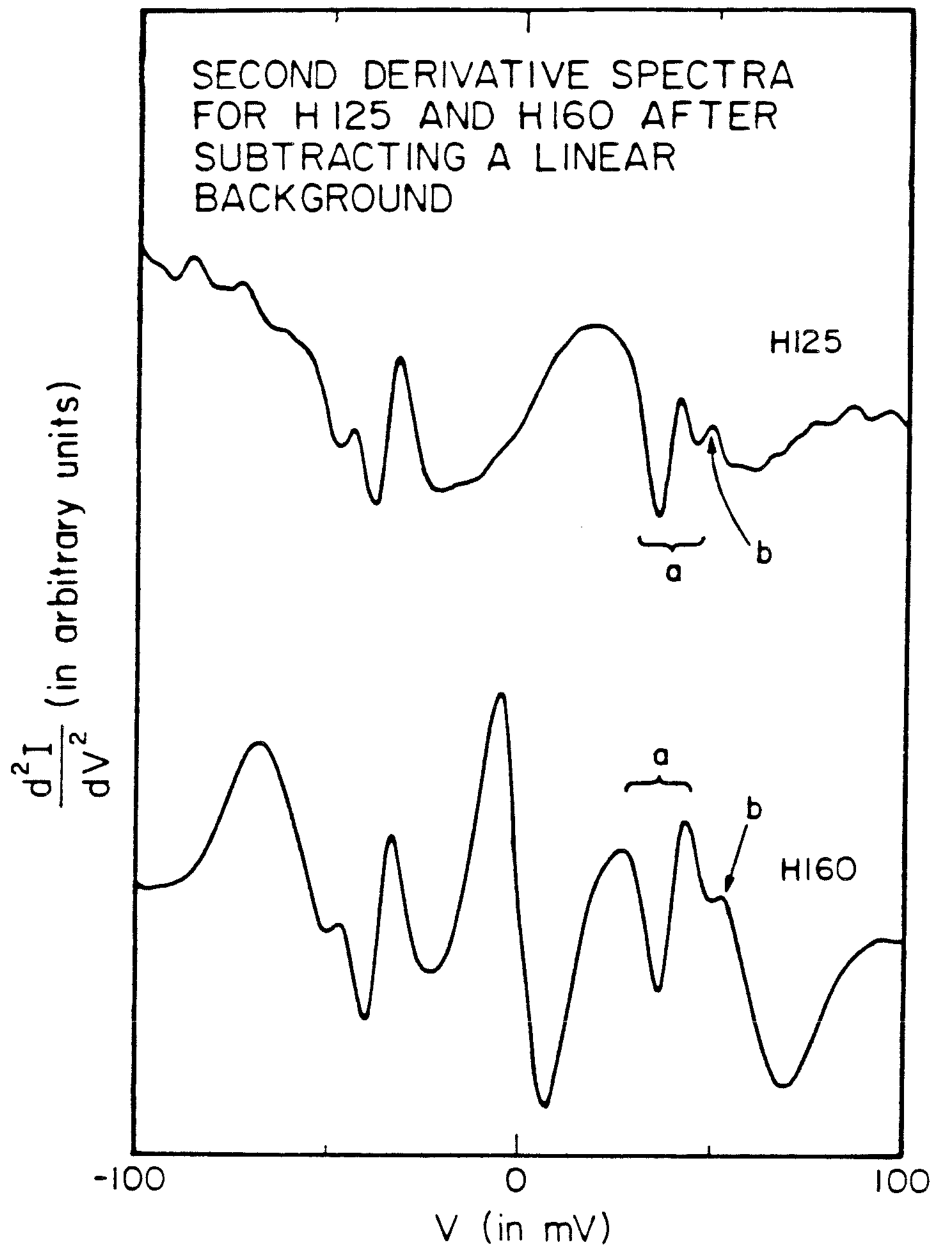


Figure 2.11: Second derivative spectra for devices prepared on H125 and H160 at 4.2 K. In both cases the region from -60 to 60 mV has been fitted to a straight line which was subtracted off.

conductance seen in the first derivative spectra for H160 may be present at higher energies in H125, but with lower signal. Also, the differential resistance of H125 may be sufficiently small in this range that the sample loads down the second harmonic bridge, making the observation of these effects more difficult. To really test these interpretations of the 70-80 meV structure in spectra for H160, more samples with a variety of dopings in the GaAs layer would have to be studied.

These are the first observations of inelastic tunneling or density-of-states effects in tunneling through a pure semiconductor analogue to a metal-insulator-metal tunneling structure, and they are the first inelastic tunneling observtaions in the AlAs/GaAs system. Inelastic and density-of-states effects have been observed previously in pure semiconductor systems and in metal-semiconductor systems. Examples are the observation of wave vector conserving phonons in Esaki diodes, the observation of LO phonons in tunneling through Schottky barriers, and tunneling out of two dimensional subbands in metal-oxide semiconductor systems. A review of these is given in Ref. 31.

Second derivative measurements on the AlAs barrier samples with thicker barriers did not uncover any reproducible effects. This is not surprising since current flow in these samples was probably due to leakage and not tunneling. The observation of resistances which were consistent with tunneling and of tunneling associated structure in the derivative spectra for samples with 50 Å thick barriers indicates that for this thickness, tunneling is the dominant current carrying mechanism. Leakage is probably still present in the samples with thinner barriers, but since the tunneling current varies exponentially with thickness, while most leakage mechanisms are probably linear, the tunneling current dominates for thin barriers.

2.3.2.4 Capacitance measurements

Studies of the capacitance of MOCVD samples with a single, p-type barrier were made as a function of temperature and frequency. In analogy to a metal-insulator-metal system, it is expected that the capacitance of a sample with degenerate layers of GaAs on either side of an AlAs barrier of width w would be given by

$$C = \frac{\epsilon A}{w}. \tag{2.7}$$

Several studies of MBE grown $Al_xGa_{1-x}As$ barrier samples have obtained accurate barrier widths using capacitance measurements and Eq. 2.7.[4,6] Many of the samples used in this study were very conductive at room temperature, making capacitance measurements difficult to make. To make accurate capacitance measurements, two possible methods of avoiding the resistance problems were used. Increasing the frequency of the measurement increases the capacitive phase of the complex conductance. When the frequency is high enough that this component of the conductance is of the same order of magnitude or larger than the resistive component, most instruments can accurately measure the capacitance. In the case of the AlAs barrier samples, cooling the samples increased their resistive impedance considerably allowing their capacitances to be measured. Still, in the samples with the thinnest AlAs barrier, the dc resistance was too low at all temperatures to allow capacitance measurements to be made.

Measured capacitances were independent of frequency from 10 kHz to 1 MHz in the samples where measurements could be made throughout this frequency range. They were also independent of the applied sample bias. Both of these results are expected for such a system. As sample temperature was decreased from room temperature to 4.2 K, the capacitance decreased by around 5 %. This was probably due to a change in the distribution of electrons in the

GaAs near the AlAs as temperature was reduced (an increase in the screening length), but the AlAs layer widths calculated from Eq. 2.7 were consistently too large by factors of 3 to 5. The deviation seemed to be worse for samples in which the doping in the GaAs layers was lower.

On the basis of the above tunneling measurements and calculations and TEM measurements, it is believed that the AlAs layer widths predicted from growth rates are accurate to at least 20%. Hence, the capacitance derived widths are in error. The AlAs barriers are doped p-type, and it is possible that some of the p-type dopant (Mg) is incorporated into the n-type GaAs adjacent to the AlAs barrier. If a layer of GaAs next to the AlAs were compensated or even p-type, this would increase the effective width as measured by capacitance since electrons would accumulate and deplete in the n-type GaAs region next to the layer contaminated with Mg. A second explanation involves the screening length in the GaAs layers. Because the AlAs is doped p-type and fully depleted, there is a layer of GaAs next to the AlAs which is depleted of electrons. The width of this region is governed by the screening length in the GaAs. If this depletion region is sufficiently wide, the effective width from capacitance measurements will be different from the barrier width by approximately the sum of the screening lengths on both sides of the GaAs. Both of these explanations are consistent with the observation that the capacitance derived widths in samples with a lower GaAs doping are in greater error, since a GaAs layer of greater width could be compensated by the Mg and the screening length in the GaAs would also increase if the GaAs doping were lower. Since capacitance measurements made in the previously mentioned studies of MBE grown samples were made on materials with undoped $Al_xGa_{1-x}As$ barriers, these problems would not have arisen and the correct widths would be obtained from Eq. 2.7. An alternative explanation is that some GaAs is incorporated into the barrier making at least part of the barrier have an $Al_xGa_{1-x}As$ rather than pure AlAs composition.

The width of the barrier would be greater due to the extra GaAs in the barrier. None of the TEM results on layers grown by these MOCVD techniques reveal any such grading.

2.3.3 Measurements on MOCVD grown samples with a single, n-type barrier

As was previously mentioned, the MOCVD samples with a single, Se-doped AlAs barrier did not have the proper relationship between current and barrier thickness for a tunneling structure (Fig. 2.3). The *I-V* curves for these samples exhibited increasing resistance as temperature was decreased until $\sim$ 30 K at which point the *I-V* curve and sample resistance stayed the same down to 4.2 K. From Fig. 2.3 it is seen that the low temperature *I-V* curves for samples with barriers ranging in thickness from 60 to 250 Å were almost identical. The zero-bias resistivity of these samples increased by less than an order of magnitude as the AlAs layer thicknesses increased from 60 to 250 Å.

Fig. 2.12 gives an *I-V* curve and first derivative spectrum for a sample with a 60 Å thick AlAs layer (H003). Changes in slope which are as large as 60% are visible in the *I-V* curve and in the first derivative spectrum. A second derivative spectrum for the same sample is presented in Fig. 2.13. The spectrum is antisymmetric with respect to bias with five peaks corresponding to increases in conductivity present in each bias direction. The peaks are located at about 23, 50, 70, 125, and 145 meV, with the two peaks at 50 and 70 meV the most prominent. There is also a strong zero-bias anomaly. The second derivative spectra were reproducible from wafer to wafer independent of the AlAs layer thickness, although there were 5-10 meV variations in the positions of the peaks. Variations of similar magnitude also existed between the forward and reverse-bias positions of the peaks on some of the wafers.

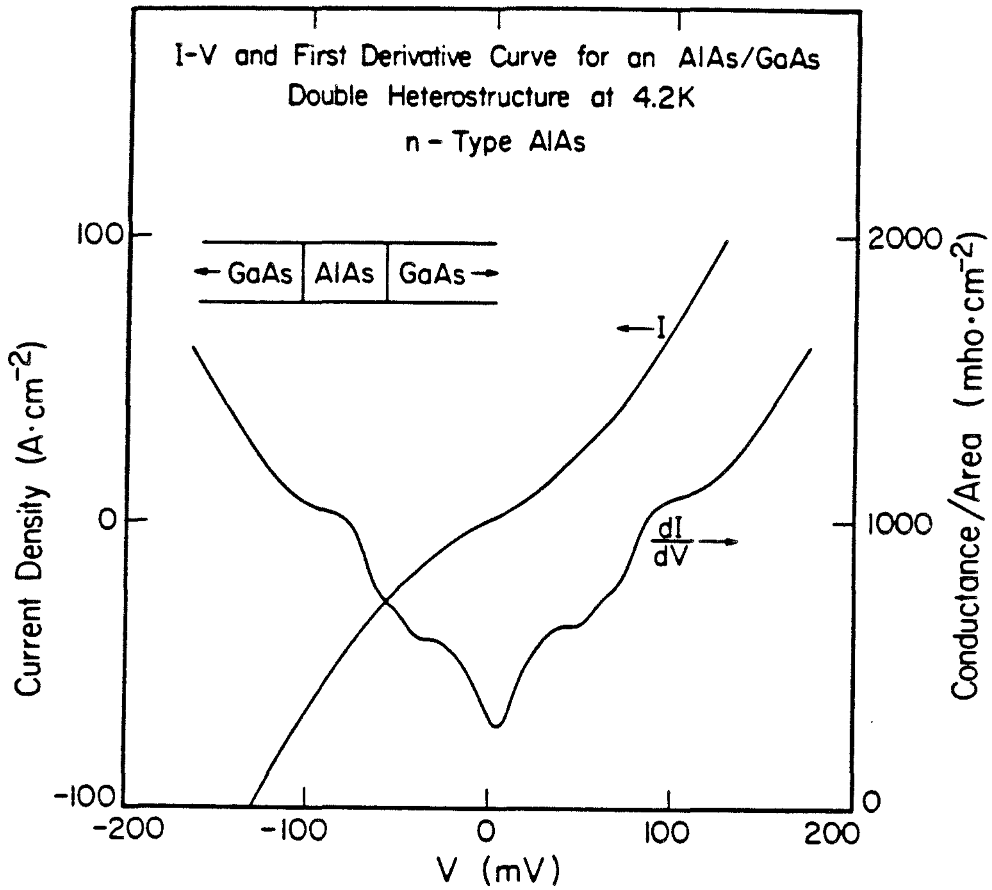


Figure 2.12: An I-V curve and first derivative spectrum for a device prepared on sample H003, which had a Se-doped barrier. The measurements were made at 4.2 K.

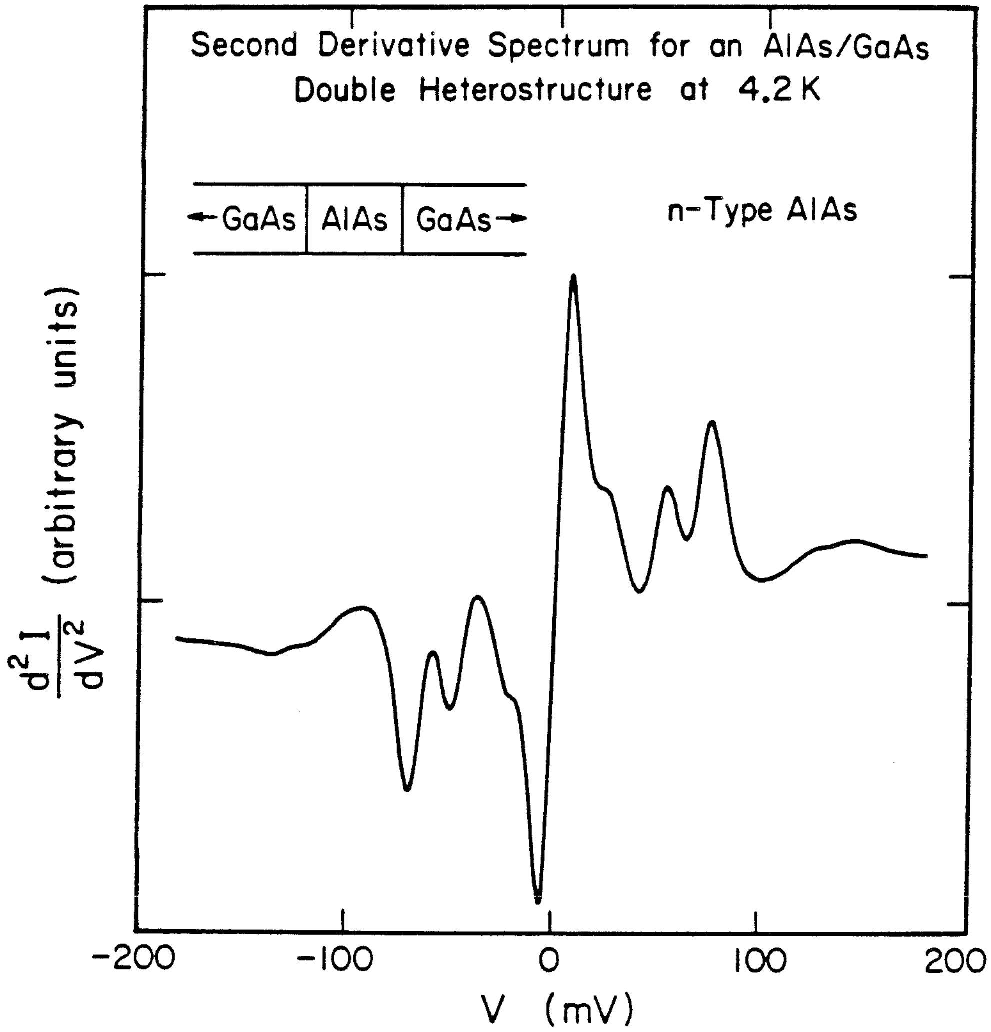


Figure 2.13: Second derivative spectrum at 4.2 K for a device made on sample H003, which had a Se-doped barrier.

An explanation for the measurements on the n-type barrier samples would have to account for two basic observations. The first is the apparent insensitivity of the *I-V* and derivative measurements to the barrier thickness, and the second is the appearance of very reproducible structure in the derivative spectra. No definitive explanations for these observations have been found, but some possible explanations can be proposed.

If transport in the n-type AlAs samples is the result of tunneling, the actual tunneling barrier must not be increasing with the physical width of the AlAs layer. From Fig. 2.5 it is seen that the energy difference between the AlAs conduction band minimum (at the X-point) and the GaAs conduction band minimum (at the Γ-point) is only about 450 meV. If the doping in the AlAs layer was sufficient, band bending in the AlAs could bring the AlAs X-point down to the GaAs Fermi level. Once the X-point is at the same energy as the GaAs Fermi level, increasing the AlAs layer width only adds a conducting layer of AlAs between two heterojunction GaAs/AlAs Schottky barriers. Hence the resistance would not depend on AlAs layer thickness.The bending required would be less than the X-point to Γ-point energy because the Fermi level of the degenerate GaAs is above the GaAs conduction band edge. This situation is illustrated in Fig. 2.14 which shows the conduction band edge profile as a function of position in a sample with a 100 Å thick AlAs layer. The GaAs doping was taken to be 5×10^{18} cm^{-3}. The potential in the GaAs was calculated using classical nonlinear Thomas-Fermi screening. The AlAs had dopings from $1 - 7 \times 10^{18}$ cm^{-3} and was assumed to be fully depleted. From Fig. 2.14, a doping of 7×10^{18} cm^{-3} is sufficient to cause such band bending.

The actual doping required may be even less. In this model the charge from the ionized dopants has been assumed to spread evenly across the 100 Å layer. For a doping of 1×10^{18} cm^{-3} the average spacing between dopants is $\sim$100 Å which is approximately the same as the barrier widths. For local regions

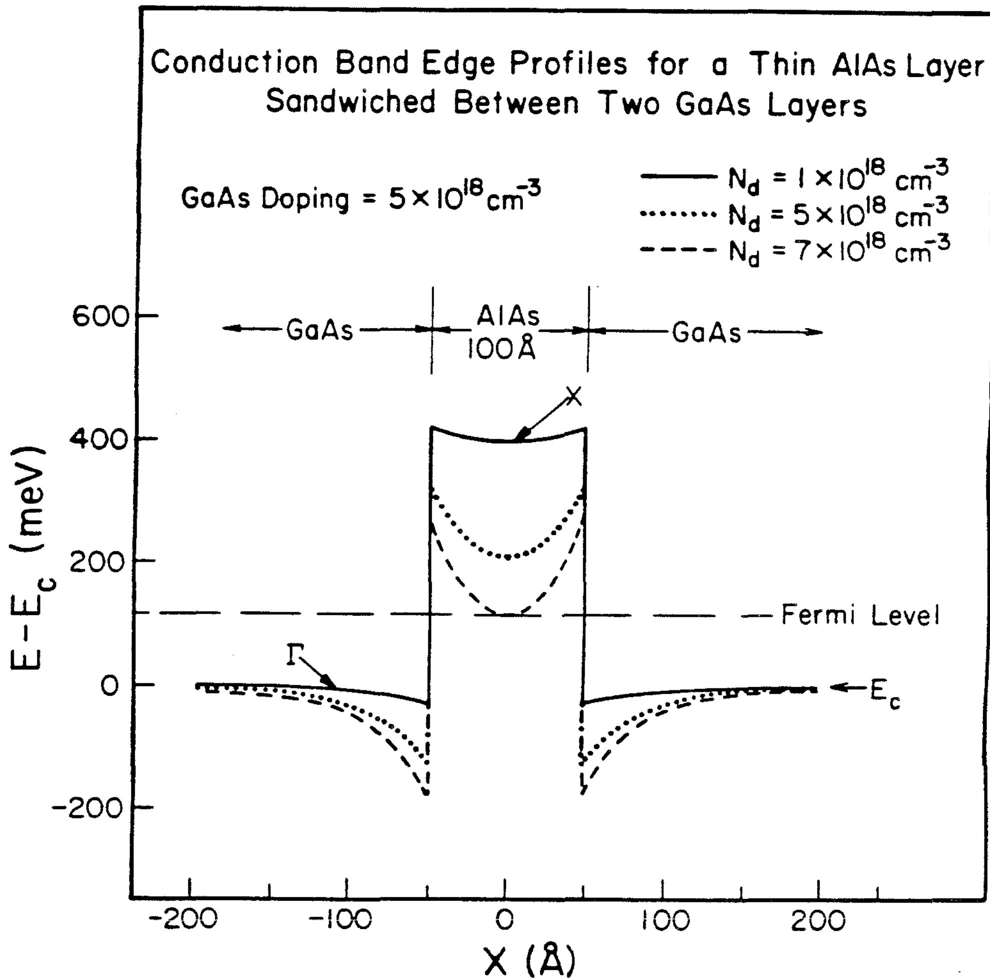


Figure 2.14: Conduction band edge profile of an AlAs/GaAs tunneling structure with an n-type barrier including electrostatic-band-bending. Nonlinear Thomas-Fermi screening was used in the GaAs, and the AlAs was assumed to be fully depleted. The GaAs doping was 5×10^{18} cm^{-3} and the AlAs doping was varied from $1 - 7 \times 10^{18}$ cm^{-3}.

near an ionized impurity, the band bending should be much larger than the average bending given by the above model, and the tunneling current may pass through these local regions because of the exponential dependence of tunneling probability on the square root of the energy barrier. A similar point was made in the comments about the zero-bias resistance calculations which were given above.

Similar band bending should occur for p-type barriers, but the amount of bending required to bring the valence band maximum in AlAs near the Fermi level is quite a bit larger than for an n-type barrier. It is also possible that the estimated dopings in the barriers for these two cases are wrong, with the n-type barriers having a doping larger than 1×10^{18} cm^{-3}. An error in the doping estimates could be due to an incorrect calibration of the doping for various hydrogen selenide flow rates, diffusion of Se into the barrier from the surrounding GaAs, or to impurities introduced during the growth.

If band bending in the AlAs were the cause of the unusual dependence of resistance on barrier width, the peaks in the second derivative spectrum could arise from a number of sources. They could indicate the excitation of characteristic phonons in the AlAs/GaAs system by tunneling electrons (possibly wave vector-conserving phonons resulting from electrons moving from direct to indirect conduction band minima) or vibrational modes of impurities in the barrier. In any case, a voltage drop would occur across each barrier, causing the voltages at which the bulk or local phonon associated peaks occur to differ from the phonon energies. If electronic states were present at the GaAs/AlAs interface because of lattice defects or impurities, it is possible that the peaks in the second derivative could indicate the onset of impurity assisted tunneling through these states. Also, there may be electronic states which are bound in the dimension perpendicular to the barrier in the band bending regions in the GaAs layer near the AlAs interface (2-dimensional electronic states). The peaks in the second

derivative could indicate the biases at which these two-dimensional bands pass above the Fermi energy on the other side of the AlAs barrier. This bias must be greater than the Fermi energy which is typically around 100 meV in these samples, so this is an unlikely explanation.

A second explanation for the dependence of resistance on AlAs layer width is that more impurities or defects may be incorporated into the AlAs layer when it is doped with Se than with Mg, giving rise to impurity conduction in the barrier. This would not have an exponential dependence on barrier width, but it would not account for the structure in the second derivative spectra.

2.3.4 Results on samples with a single, MOCVD grown, $Al_xGa_{1-x}As$ barrier

Measurements of the *I-V* curves and first and second derivative spectra of devices fabricated on two MOCVD grown samples with a single $Al_{.75}Ga_{.25}As$ barrier were also made. The growth parameters for these samples are given in Table 2.1. Observations similar to those presented above for AlAs barrier samples were made. When the barrier was doped n-type with Se, the low temperature sample resistance was considerably less than for a Mg-doped barrier of the same width. Structure is visible in both forward and reverse bias at voltages between 30 and 50 meV in a second derivative spectrum for a sample with a p-type Mg-doped barrier with an estimated width of 80 Å (H244). Presumably this is an observation of the same effects present in the samples with p-type AlAs barriers: a density of states effect in the GaAs caused by electron-phonon coupling, and the direct excitation of LO phonons in the $Al_{.75}Ga_{.25}As$ barrier, but it is not possible to pick specific energies out of the second derivative spectrum. The density-of-states effect should occur at approximately the same energy as in the AlAs barrier case because it reflects a property of the GaAs

electrodes, but two LO phonon frequencies should be present in $Al_{.75}Ga_{.25}As$ with energies of 32 and 49 meV.[32] Some broadening of the peaks in the 30-50 meV range of the second derivative spectrum would be expected because of this and may account for the inability to pick specific phonon related peaks out of the second derivative spectrum. In contrast to samples with n-type AlAs barriers, no reproducible structure was visible in the second derivative spectrum for an 80 Å thick $Al_{.75}Ga_{.25}As$ barrier sample in which the barrier was doped n-type (H226). An additional observation in the samples with $Al_{.75}Ga_{.25}As$ was that the low temperature *I-V* curves conducted considerably more current than would be expected both from calculations and from comparisons with samples with AlAs barriers.

2.3.5 Samples grown by MBE

The electrical measurements described above were also made on MBE grown samples with a single $Al_xGa_{1-x}As$ barrier. Physical characteristics of these samples are included in Table 2.1. All but one of them had a pure AlAs barrier. Not much discussion of the measurements on these samples will be included here, because in general the results were not reproducible, and in many cases they were not internally consistent. Qualitative observations of the properties of devices made on these wafers will be catalogued below according to their source for comparison with the MOCVD results given above.

When devices with diameters of approximately 80 μm were prepared on MBE 358 and 359 (obtained from Hughes) both of which had barrier thicknesses around 100 Å, nearly half of the devices were shorts. The remaining devices had zero-bias resistances which varied by several orders of magnitude. This variation occurred both in a local region of the wafer ($\sim$ 1 mm) and across the wafer. Devices with diameters of 360 μm or greater were always shorts. If the shorts

were attributed to a defect, the surface defect density would be nearly 40,000 cm^{-3}. No reproducible structure was observed in the derivative spectra.

The thicknesses of the AlAs barriers in the Cornell samples were estimated to be 50 Å, 100 Å, and 150 Å, respectively, for Cor 1, Cor 2 and Cor 3. Two of the wafers from Cornell (Cor 2 and Cor 3) also had zero-bias resistances which fluctuated by several orders of magnitude from device to device although the problem of obtaining shorted devices was not observed. Additionally, the largest impedances obtained from Cor 2 were larger than the largest resistances measured for Cor 3, even though Cor 3 was supposed to be 50 Å thicker than Cor 2. In contrast, Cor 1 gave much more reproducible zero-bias resistances. The I-V curves for this sample remained unchanged as a function of temperature from 77 to 4.2 K. The zero-bias resistance for this sample has been plotted on Fig. 2.6 and is consistent with the tunneling calculations. As was previously mentioned, the width used in the plot was taken from calibrations of the growth of thicker AlAs layers and could be in error by several angstroms. Again, no reproducible structure was observed in the derivative spectra.

The final two MBE samples were Phi 1 and 2. The estimated thicknesses of the AlAs barriers in these samples were 60 and 50 Å, respectively. The uniformity of sample resistance in this case was better than Cor 2 and 3 but poorer than Cor 1. Zero-bias resistances for the most resistive devices on these samples are presented in Fig. 2.6 and are also consistent with the calculated resistances for tunneling. The I-V curve froze out at 77 K, but no reproducible structure was present in the derivative spectra.

In general it was observed that in terms of the measurements made in this study, the MBE grown samples were less uniform across a given wafer. Fig. 2.15 contains I-V curves for three devices of equal size in close proximity to one another on each of the two samples H135 and Cor 2. There are much larger fluctuations in the I-V curves from device to device in the MBE grown

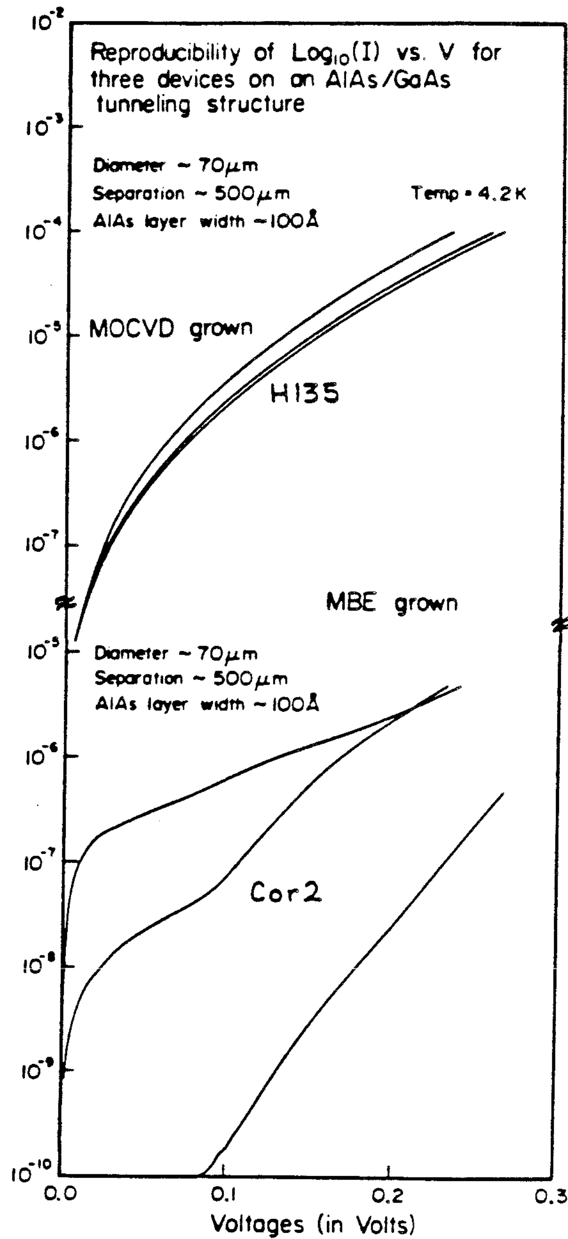


Figure 2.15: *I-V* curves for three neighboring devices of equal diameter (~ 80 μm) fabricated on samples H135 and Cor 2. Measurements were made at 4.2 K. Both structures had barrier widths which were estimated to be 100 Å.

material (Cor 2) than in the MOCVD sample (H135). The MBE samples had a larger zero-bias resistance in those wafers which were fairly uniform and did not exhibit the same inelastic tunneling structure as an MOCVD grown sample with a p-type barrier of the same width.

In comparing these two sets of samples with respect to the associated measurement techniques, some things must be kept in mind. First, the thicknesses of the top GaAs layers in the MBE grown samples were generally less than one micron while in the MOCVD grown samples this thickness was greater than 3 μm . In the above discussion of ohmic contacts on GaAs it was noted that in most cases, the damage depth resulting from Au-Ge/Ni contacts is less than 5000 Å, but it may be possible that some of the nonuniformity observed is related to the penetration of the contact into the AlAs layer. This seems unlikely since some of the samples were more uniform than others, although they had the same top GaAs layer thickness. Also, there has not been as much effort to study the growth of high Al content $Al_xGa_{1-x}As$ by MBE as by MOCVD. The dopants in the GaAs layer were different in the two growth techniques. This would not be expected to have an impact on the measurements. The AlAs barriers in the MBE samples were undoped while the barriers in the MOCVD samples were doped rather highly. The difference in the *I-V* curves for n-type and p-type MOCVD barriers indicates that the doping in the barrier is very important, and, as was mentioned above, the local region around an impurity may have a large impact on the tunneling current. The doping in the p-type MOCVD barrier samples could have the effect of smoothing out fluctuations in the resistance which are due to other defects that are present in the layer (basically by reducing the resistance to a value lower than would be expected for a device fabricated over one of these defects), while in the MBE grown layers, only these residual impurities would affect the device resistance and the statistics of the distribution of the residual defects would cause the variations in resistance.

This explanation also seems unlikely since one of the MBE wafers was very uniform while the others showed fluctuations, and it cannot account for impedances in some of the devices prepared on MBE samples which were lower than those of devices on MOCVD samples of the same barrier thickness. It is possible that the thinnest MBE barriers samples grown are too resistive to see any of the second derivative structure, because the second derivative signal is below the detectable limit of our system. The fact that the largest resistances measured for MBE samples are larger than the resistance of MOCVD grown samples of the same estimated barrier width may be due to errors in the calibration of widths, or to the possibility that ionized dopants in the p-type MOCVD barriers reduce the tunneling resistance of the barrier structure as was mentioned above.

2.4 RESONANT TUNNELING THROUGH MULTIPLE BARRIERS

2.4.1 Principles of resonant tunneling

Based on the results of the measurements on a single AlAs barrier sample, an attempt was made to observe resonant tunneling through a two-barrier structure. The growth of this sample was described in Section 2.2.1. Fig. 2.16 is a schematic diagram of the valence band maximum and conduction band minimum as a function of position (excluding electrostatic band bending) for this structure. If regions II and IV were infinitely thick, stationary states which are bound in the direction perpendicular to the barriers would exist in the GaAs well formed by regions II, III, and IV. Because regions II and IV are finite, quasistationary states are present in the well, and tunneling electrons moving perpendicular to

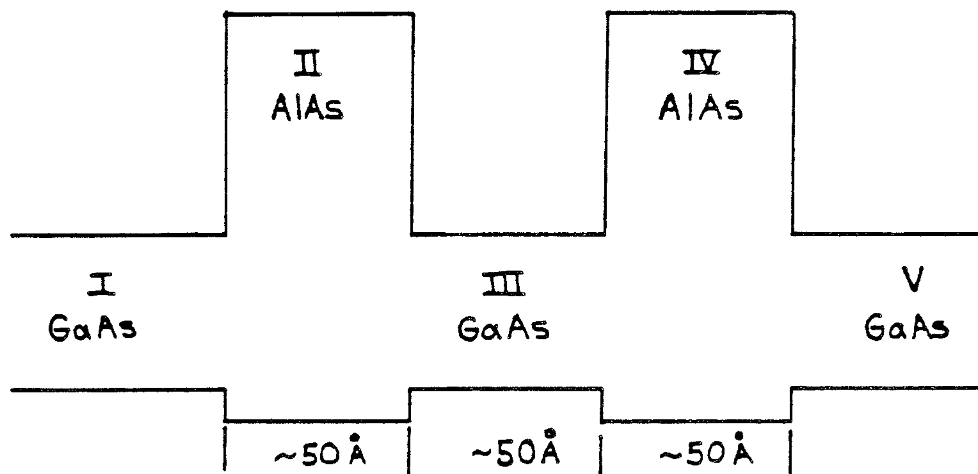


Figure 2.16: Schematic diagram of the valence band maximum and conduction minimum as a function of position for a double barrier structure. Band bending has not been included. The barrier thicknesses in the samples studied (H283, H333) were estimated to be 50 Å, while the GaAs well was also about 50 Å wide. The barriers were doped p-type with Mg at about 1×10^{18} cm^{-3}.

the barrier with an energy equal to the energy of a quasistationary state will have a large transmission probability. Since the structure under study is three dimensional and electrons in the well are free to move transverse to the barriers, the quasistationary states are really the minima of two-dimensional bands, and in considering tunneling perpendicular to the barriers, the conservation of wave vector parallel to the barrier must be included.

The details of the *I-V* curve expected for a two-barrier structure were originally worked out in a simple approximation by Tsu *et al.*[33] These calculations predicted a current maximum at voltages where the Fermi level in either GaAs outer layer approximately coincides with the energy of the state in the well. The *I-V* curve for tunneling through a double barrier structure should thus exhibit a negative resistance region. If the structure is symmetric and biasing the sample does not shift the energy of the states in the wells too much (the stark shift to the energy is second order in this case), the negative resistance should occur in both bias directions and at energies slightly greater than twice the resonant energy in the well (equal voltage drops occur across each barrier).

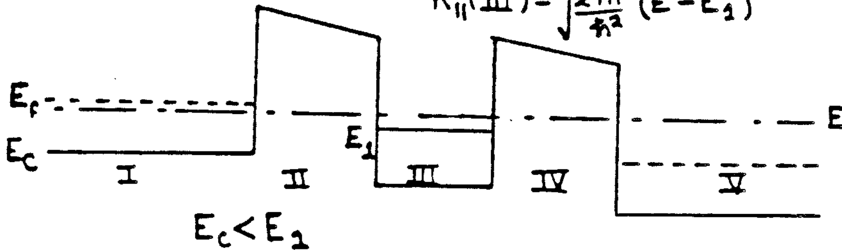
An important part of the argument leading to negative resistances is the conservation of the transverse wave vector of tunneling electrons in addition to energy conservation. This is schematically illustrated in Fig. 2.17. If we consider a state of energy E in the GaAs electrode and a corresponding state of energy E in the well, the value of $k_{\|}$ in the well is given by

$$k_{\|}(III) = \sqrt{\frac{2m^*}{\hbar^2}(E - E_1)} \tag{2.8}$$

where E_1 is the subband minimum energy, and m^* is the conduction band effective of GaAs. For the GaAs electrode, $k_{\|}$ has values between

$$0 < k_{\|}(I) < \sqrt{\frac{2m^*}{\hbar^2}(E - E_c)} \tag{2.9}$$

where E_c is the energy of the conduction band edge in region I. We see from Eq. 2.8 and Eq. 2.9 that when the structure is biased such that E_1 is between E_f



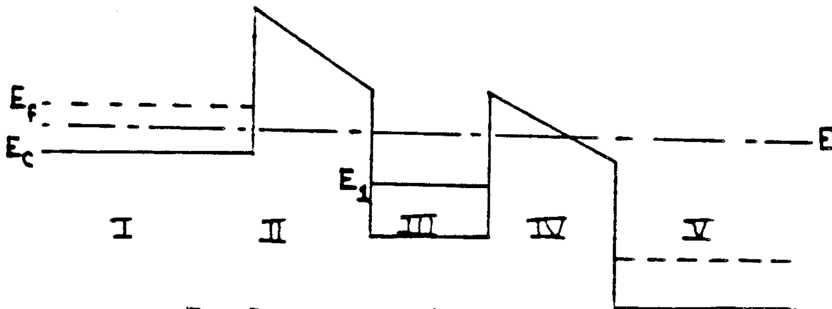


Figure 2.17: Schematic of the conduction band minimum as a function of position in a double barrier structure illustrating that conservation of $k_{\parallel}$ can lead to a negative resistance. In the top part of the figure, the Fermi level of the GaAs electrode lines up with the resonant band in the barrier, and states with the same energy and $k_{\parallel}$ can be found in both the electrode and the well. In the bottom part of the figure, the bias has increased and, although there are states of the same energy in the two-dimensional resonant band and in the GaAs electrode, $k_{\parallel}$ in the resonant band is always larger than in the electrode, so $k_{\parallel}$ can not be conserved and the tunneling probability is reduced leading to less current flow and negative resistances.

and E_c in energy, where E_f is the Fermi energy in the GaAs electrode, as it is in the top part of Fig. 2.17, there will always exist a state of energy $E > E_1$ in the GaAs electrode which has the same $k_{||}$ as the states of energy E in the well. If the bias is increased such that E_c is greater in energy than E_1, $k_{||}(I)$ for a given state of energy E will always be less than $k_{||}(III)$ for states of energy E in the well, and the tunneling probability will be reduced leading to less current flow and a negative resistance in the *I-V* curve. The above argument is not rigorously true since the states in the well are not bound but are resonances.

Chang *et al.*[8] observed structure in the *I-V* curves of MBE grown double barrier structures with $Al_xGa_{1-x}As$ barriers and identified it as due to resonant tunneling. The negative resistances associated with these measurements had nearly unity peak to valley ratios. More recently, Solner *et al.*[9] have reported large negative resistance regions in the *I-V* curves of MBE grown double barrier structures.

The resonant tunneling measurements being reported in this thesis were made on two MOCVD grown samples (H283 and H333). The barriers were composed of pure AlAs doped with Mg at $\sim 1 \times 10^{18}$ cm^{-3} and were 50 Å thick. These properties were chosen for the two barriers because single barrier samples with AlAs layers having these properties exhibited tunneling currents at low temperature. The width of the GaAs well was chosen to be 50 Å based on elementary calculations of the resonant energies. Resonant energies in the well were approximated by finding the energies of the bound states in the well under the assumption that regions II and IV in Fig. 2.16 were infinite. These calculations were carried out in the effective mass approximation. The effective mass hamiltionian for the x coordinate (perpendicular to the barrier) in a given region after separation of variables was

$$H = \frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial x^2} + V \qquad (2.10)$$

where m^* and V are the effective mass and conduction band edge energy in the

region. The boundary conditions applied were the continuity of φ and $\frac{1}{m^*}\frac{\partial\varphi}{\partial x}$ across each boundary where φ is the effective mass wavefunction.[34] The effective masses and band gaps in each region were taken from Casey and Panish.[5] The conduction band offset was taken to be 0.85 of the total bandgap discontinuity.[5] Band gap parameters at 4.2 K were used. Comparison of the results of these calculations when applied to the structure in the work of Chang *et al.*[8] to the results of their measurements gives resonable agreement. Two states are predicted at energies of 0.10 and 0.41 eV above the GaAs conduction band edge. The average values of the measured voltages in forward and reverse bias at which the resonances occurred were 0.15 and 0.66 eV. These values are a little less than twice the calculated values. In the work of Solner *et al.*[9], the predicted energies are 0.08 and 0.26 eV. Only one peak was reported in that paper at a voltage of 0.24 eV which does not correspond to twice either of the calculated values. This suggests that the actual growth parameters were different from those reported. In the current study, the predicted resonant energies are 0.11 and 0.45, where the Γ-point effective mass has been used in the AlAs for reasons mentioned in Section 2.3.2.2.

2.4.2 Results and conclusions on double barrier samples

Fig. 2.18 presents an *I-V* curve in the positive bias direction for a device fabricated on H283. Structure is observed in the positive bias direction at approximately 70 meV and 390 meV. The *I-V* curve flattens out near the 70 meV region, and a negative resistance region is observed in the 390 meV range of the *I-V* curve. The negative resistance is larger than that reported in Ref. 34, but smaller than in Ref. 35. No structure is observed in the negative bias region indicating that, although the sample growth was supposed to be symmetric, an asymetry of some kind exists. When *I-V* curves were taken at 4.2 K, the results

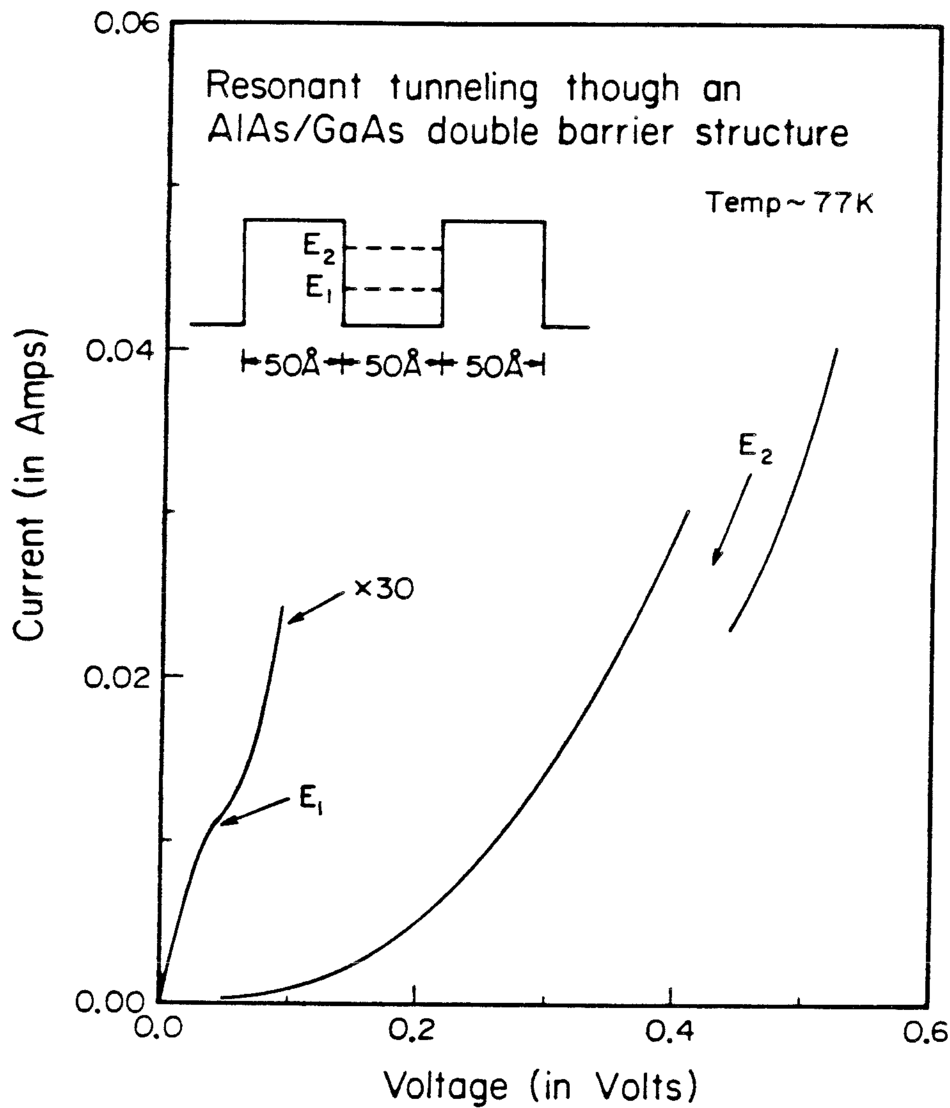


Figure 2.18: An *I-V* curve at 77 K in the positive bias direction for a device prepared on a double barrier sample (H283). Structure is present at 70 meV and negative resistance is observed near 390 meV. These correspond to resonant tunneling through the ground state and first excited state subbands in the GaAs well between the two barriers. Similar structure was not observed in the negative bias direction.

were nearly identical to those in Fig. 2.18. The structure at 390 meV is still visible at temperatures exceeding 200 K, although negative resistances are not observed at these temperatures.

First and second derivative spectra were taken of devices made from the double barrier sample to determine the temperature range throughout which resonant tunneling effects could be observed, and whether any structure was present in the negative bias region of the devices which was related to resonant tunneling but unobservable in the *I-V* curve. Second derivative measurements at room temperature show structure near 390 meV, indicating that resonant tunneling effects are still observable at this temperature. A second derivative spectrum for this material at 4.2 K exhibits unidentified structure near zero bias, oscillations are present in the -50 meV range, and structure corresponding to a dip in conductivity is present at -200 meV. In the positive bias direction the only structure seen was related to the resonant effects at 70 meV and 390 meV. No additional structure is seen for bias voltages between ± 0.7 eV.

The bends in the low temperature *I-V* curve for this sample at 70 meV and 390 meV are almost certainly due to resonant tunneling effects. The fact that these are not seen in reverse bias is a clear indication that the sample is asymmetric. The exact nature of this asymmetry cannot be determined without making additional measurements such as TEM measurements of layer thicknesses, layer abruptness, and of the morphology of the growth in the region of the barrier. These are currently under way.

There are several possible explanations for the asymmetry. The most likely is that the barriers are not of the same width. If one barrier is seven or more angstroms thicker, its tunneling resistance will be at least an order of magnitude larger than the resistance of the other barrier, as was shown above in the calculations of resistances of single barrier samples. This would mean that most of the voltage drop in the structure would occur across this barrier. If a bias

were applied which made the GaAs electrode next to this barrier negative with respect to the other GaAs layer, at a bias approximately equal to the resonant state energy, the Fermi level in this electrode would line up with the resonant state minimum and enhanced tunneling would occur. Indeed, the measured biases for resonant tunneling to occur of 70 and 390 meV are relatively close to the calculated values for the energies of these states (110 and 450 meV). On the other hand, if the bias were reversed, it would take a very large voltage to bring the Fermi level of the second GaAs layer up to the resonant band in the well, since most of the voltage drop would be occurring across the opposite barrier. The observations in the second derivative spectra would then be explained as follows. The structure in reverse bias at -50 meV may be related to the GaAs and AlAs LO phonon structure observed in the single barriers. It may not have been visible in the forward bias region because of the large second derivative signal arising from the resonant tunneling structure at 70 meV. The structure at -200 meV could then be due to tunneling in which the electrons originate in the GaAs layer next to the thinnest barrier, with most of the voltage drop occurring across the opposite barrier. This explanation does not account for the resonant structure at -200 meV being smaller than the forward bias resonant signal. In this sample the positive bias direction corresponds to the GaAs layer next to the substrate being negative with respect to top layer of GaAs. This would imply that the first AlAs layer grown was the thickest. When sample H327 was grown, an attempt was made to make the width of the second AlAs barrier grown closer to that of the first barrier. Resonant effects were again observed but in the negative bias direction.[35] This is consistent with the above explanation.

If defects accumulate at one of the interfaces during sample growth (either impurities or lattice defects such as dislocations), the tunneling characteristics might depend on whether the defects are encountered before or after the elec-

trons pass through the resonant states and thus depend on bias direction. This explanation seems unlikely since similar effects were not observed in the single barrier samples (inelastic effects occurred symmetrically with bias), and because it is unlikely that the location of such defects relative to the two barriers would change from one sample to the next although the bias direction, where strong resonant effects were observed, did.

A third explanation is that the structural asymmetry is due to grading at the growth interfaces. Once again, this explanation would not account for the change from one sample to the next in the polarity of bias where strong resonant effects were observed. Grading would be expected to occur at the same interfaces from one growth to the next leading to strong resonant structure in the same bias direction.

2.5 SUMMARY

This chapter presents a study of electron transport perpendicular to AlAs and $Al_xGa_{1-x}As$ barriers sandwiched between layers of GaAs. Transport in samples with a single, p-type AlAs barrier which was grown by MOCVD was observed to occur by thermionic emission at room temperature and low bias voltages. At low temperatures, transport was mainly due to tunneling if the barrier thickness was near 50 Å. For thicker barrier samples, leakage dominated the low temperature transport. Reproducible structure was observed in the second derivative spectrum at 4.2 K for samples with 50 Å thick barriers. The structure was associated with a density-of-states effect in the GaAs electrode caused by coupling between electrons and LO phonons in the GaAs and with the inelastic excitation of AlAs LO phonons. This was the first observation of these effects in the AlAs/GaAs system. The resistivity of MOCVD samples with a single, n-type

AlAs barrier was nearly independent of barrier width. Reproducible structure was observed in the derivative spectra, but a definitive explanation for the behavior of these samples has not been found. Some possible explanations were presented. Similar results were obtained in measurements made on MOCVD grown samples with an $Al_xGa_{1-x}As$ barrier. Devices prepared on single barrier structures grown by MBE did not, in general, give reproducible results in terms of the measurements made here. Current-voltage curves for devices prepared on MOCVD grown samples with two AlAs barriers separated by a thin layer of GaAs exhibited resonant tunneling effects. Negative resistances were observed which correspond to resonant tunneling through the two-dimensional bands created in the GaAs well. The *I-V* curves for these devices were not symmetric. The asymmetry was tentatively attributed to a difference in the widths of the two AlAs layers.

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CHAPTER 3

ELECTRONIC PROPERTIES OF DEEP LEVELS IN CdTe

3.1 INTRODUCTION

Electronic properties of II-VI compound semiconductors are not well understood. The situation is complicated by comparison to III-V and column IV semiconductors because of the presence of native defects and defect complexes in the II-VI materials in addition to impurities incorporated into the crystals during growth. These native defects, which are the result of the wide phase stability region of II-VI compounds, often dominate the electrical characteristics of II-VI crystals.

CdTe is a II-VI semiconductor which exhibits large deviations from stoichiometry. Annealing CdTe under a fixed partial pressure of its constituents, Cd and Te, can modify the defect structure of the crystal and even change the material from p-type to n-type.[1,2] CdTe is recently of considerable interest. Most of this interest stems from its use as a substrate for the growth of the lattice-matched ternary $Hg_{1-x}Cd_xTe$. It has been suggested that superlattices composed of alternating layers of HgTe and CdTe may have important applications and also illustrate some interesting physical properties.[3,4] CdTe has also been proposed for use as a nuclear detector and in solar cells. An understanding of the electronic properties of deep levels in CdTe would certainly be useful in these applications. A study of the deep levels in CdTe might also add to the understanding of defects and their formation in II-VI materials. There have been a number of studies of deep levels in CdTe.[1] The results of these measurements are difficult to compare because of the variety of techniques which were used and because of differences which may exist between the crystals used in the studies. The technique of deep-level transient spectroscopy (DLTS)[5] provides more sensitive and reproducible information about deep levels in semiconductors than the techniques used in previous deep-level measurements on CdTe.

This chapter describes a DLTS study of deep levels in both n-type and p-type CdTe. DLTS and capacitance-voltage (C-V) measurements were made

on nominally undoped CdTe and on CdTe which was intentionally doped with In and Cu. All of the material studied was bulk-grown. Comparisons were made between measurements on crystals in as grown conditions and following anneals in fixed activities of Cd or Te, or following anneals in an H_2 ambient as might be done before growing $Hg_{1-x}Cd_xTe$ on a CdTe substrate.[6] Levels were observed which were present in all of the CdTe crystals. These were attributed to native defects or to impurities which are commonly incorporated into CdTe during growth. Some levels were seen which were specific to certain crystals and, therefore, probably due to an impurity which is present in that crystal. No levels could be associated with Cu. In one of the In-doped crystals, levels were observed which exhibited a persistent photo-effect. In general, the deep-level structure of CdTe was very sensitive to temperature cycling, and could change completely if a sample was heated to temperatures above 400 K.

The rest of the chapter is organized as follows: Section 3.2 will give a description of the crystals used in this study and of their preparation for DLTS measurements. In Section 3.3 the measurement techniques used will be discussed. Results of these measurements will be given in Section 3.4. Section 3.5 is a discussion of these results, followed by conclusions in Section 3.6.

3.2 CRYSTAL CHARACTERISTICS AND SAMPLE PREPARATION

Properties of each of the samples which were studied are listed in Table 3.1. The crystals were named as given in Table 3.1 to remain consistent with previous publications.[7,8] All of the samples were grown by Bridgman techniques except for crystal B which was grown by the traveling heater method. Three of the crystals were doped n-type with In. IN1 had an In concentration of approximately 1×10^{18} cm^{-3}. Although the In concentrations in IN2 and IN3

TABLE 3.1

Crystal	Dopant (cm^{-3})	Shallow Level Concentration (cm^{-3})	Comments
IN1	In (10^{18})	7×10^{17}	n-type, Grown by Eagle Picher, Ind.
IN2	In	2×10^{17}	n-type, Grown by II-VI Corp. Annealed in Cd vapor at 750 °C for 6-12 h.
IN3	In	6×10^{17}	n-type, Grown by Eagle Picher, Ind. Annealed in Cd vapor at 750 °C for 6-12 h.
UN1	Nominally undoped	2×10^{15}	n-type, Grown by Eagle Picher, Ind. Annealed in Cd vapor at 750 °C for 6-12 h.
A	Nominally undoped	$5 - 8 \times 10^{15}$	p-type, Grown by II-VI Corp.
B	Nominally undoped	6×10^{14}	p-type, Grown by Radiation Monitor. Traveling heater method.
C	Nominally undoped	$2 - 3 \times 10^{16}$	p-type, Grown by Rockwell Int.
D	Nominally undoped	1.5×10^{15}	p-type, Grown by II-VI Corp.
E	Nominally undoped	$> 2 \times 10^{16}$	p-type, Crystal "B" annealed in Te vapor at 800 °C for 2 h.
F	Cu (10^{16})	1.2×10^{16}	p-type, Grown by II-VI Corp.
G	Nominally undoped	6×10^{15}	p-type, Grown by Texas Instruments.

Table 3.1: Shallow level concentrations, doping, and origin of the CdTe crystals used in DLTS measurements.

were not known exactly, it was known that they were several orders of magnitude less than in IN1. Crystal F was Cu-doped at around 1×10^{16} cm^{-3}. Cu is an acceptor in CdTe.[1] The rest of the samples were not intentionally doped during growth.

CdTe can be grown n-type or p-type depending upon whether it is grown in an excess of Cd or Te.[1] Subsequent anneals of the crystals in Cd or Te can change the donor or acceptor concentrations of the crystals by changing the native defect concentrations. All of the n-type crystals in this study except IN1 had initial shallow level concentrations which were too low to allow DLTS measurements to be made on them. For this reason,the n-type crystals (except IN1) were annealed under saturated Cd pressure at 650-800 °C for 6-12 h, thus raising their carrier concentrations. In the case of the p-type samples, all of the samples had a large enough acceptor concentration initially to allow the measurements to be made. For comparative purposes, crystal E was produced by annealing some of crystal B in Te at 800 °C for around 2 h.

Samples were annealed by sealing them in an evacuated quartz ampule with a quantity of elemental Cd or Te. The ampule was cleaned prior to the anneal by rinsing it in HF followed by a rinse in deionized water. The ampule was then heated in a flame until it glowed white. The Cd and Te were etched in a nitric acid solution. After the sample and the Cd or Te had been placed in the ampule, it was evacuated to a pressure below 10^{-3} Torr using a sorption pump, and the open end of the ampule was sealed. The CdTe and Cd or Te were moved to opposite ends of the ampule, which was then inserted into a furnace at the anneal temperature and left for the desired length of time. When the anneal was complete, the sample was quenched by inserting the ampule into a beaker of water.

The electrical measurements described in this chapter were made on Schottky barrier devices which were prepared on the CdTe crystals. Au Schottky

barriers were used on the n-type samples. Two methods for preparing Schottky devices were used on crystal IN1. In both techniques, clean surfaces of CdTe were prepared by cleaving bulk CdTe in air to expose a {110} sample face. One set of samples was immediately placed into an ion pumped vacuum system where 160 μm diameter Au dots were evaporated through a shadow mask onto the cleaved CdTe surfaces. A second set of samples was annealed at 350-370 °C for 1 h in a Pd purified H_2 ambient before Au dots were deposited onto the annealed, cleaved surfaces. Au Schottky barrier devices were also prepared on air cleaved surfaces of the rest of the n-type samples in the manner described above for IN1. No H_2 annealing treatment was used on the rest of the n-type samples.

Both Au and Cd barriers were used in the electrical measurements made on p-type CdTe crystals. The Au and Cd Schottky barriers were prepared in two different ways. In the first method, 160 μm diameter dots were evaporated onto air-cleaved {110} sample surfaces through a shadow mask in an ion pumped vacuum system at 10^{-6} Torr. In the second method of preparation, Au or Cd was evaporated onto polished {111} sample surfaces which had been etched for 5 min in a 0.5% Br-Methanol solution. These dots were 500 μm in diameter.

Before making measurements on the Schottky devices, ohmic contacts had to be fabricated on the samples. Contacts to the n-type CdTe crystals were prepared by soldering indium onto one of the sample faces with a low temperature soldering iron. In the case of the Schottky devices prepared on air cleaved faces of the CdTe crystals, the In contact was actually affixed to the crystal before cleaving the crystal to avoid heating the cleaved face while it was exposed to air. Indium contacts were prepared on the H_2 annealed samples after they were annealed but before deposition of the Au Schottky barrier. Low resistance contacts to p-type CdTe are more difficult to prepare. In the procedure followed here, the rear face of the sample was etched in a K_2CrO_7 and H_2SO_4 solution. After the etch Ni or a Cu/Au alloy was evaporated onto the back face of the

sample to provide the contact.[9]

3.3 MEASUREMENT TECHNIQUES

The electrical measurements performed on devices prepared on the CdTe crystals included DLTS and C-V measurements. The DLTS measurements will be described first. In chapter 1 it was shown that the capacitance of a reverse biased Schottky diode can be used to infer the properties of deep levels in the depletion region of the diode. The diode is reverse biased; then the reverse bias is reduced and traps in the depletion region capture carriers. The bias is returned to its previous value and the carriers are thermally emitted from the deep levels. The capacitance of the diode changes as the carriers are emitted from the levels, resulting in an exponential capacitance transient. The rate associated with this transient is the thermal emission rate from the trap. Analysis of this rate as a function of temperature gives the activation energy of the trap. The initial amplitude of the transient can be used to find trap concentrations and capture cross sections.[10] There are a number of ways of extracting the desired information from the capacitance transients. The most common method uses a double boxcar integrator. This technique is explained in some detail in Ref. 5. A brief explanation will be given here. The dual boxcar integrator samples the capacitance transient at two times, t_1 and t_2, after the bias pulse is applied to the sample and takes the difference between these two values. The capacitance decays back to the value it had before the pulse with a rate equal to the thermal emission rate from the trap. Because of this, the shape of the capacitance transient changes with temperature as does the signal from the dual boxcar. At low temperatures very few trapped carriers have been emitted by times t_1 and t_2. The sample capacitance is approximately the same at these two times,

and the signal from the dual boxcar is near zero. At very high temperatures, all of the carriers have been emitted by times t_1 and t_2, and, once again, the capacitances at these two times are equal, so the signal from the boxcar is zero. At some intermediate temperature the shape of the capacitance transient will be such that the dual boxcar signal will be a maximum. If the transients are exponential, it can be shown that the decay rate of the exponential will be given by

$$\frac{1}{\tau} = \frac{ln(\frac{t_1}{t_2})}{(t_1 - t_2)} \tag{3.1}$$

at the temperature where the boxcar signal is a maximum. The initial amplitude of the capacitance transient can be found from the amplitude of the DLTS signal maximum. By fixing the sampling times of the boxcar, t_1 and t_2, repetitively pulsing the sample, and measuring the difference in the capacitance at these two times as a function of sample temperature while the temperature is scanned, a DLTS spectrum is produced. If the depletion region of the diode contains a deep level, the spectrum will exhibit a peak at the temperature where the thermal emission rate from the deep level has the value given by Eq. 3.1. If more than one level is present, there will be a peak in the spectrum for each level. The rate set by Eq. 3.1 is called the rate window of the scan. In general, once a rate window has been set, the deeper in the gap a level is, the higher the sample temperature has to be for the level to have the emission rate set by the rate window. Thus the peaks associated with deeper levels will usually occur at higher temperatures. The temperature axis of a DLTS scan can be thought of as an energy axis and each peak represents a level. The amplitude of the peak is its relative concentration. It should also be added that peaks in a DLTS scan can be both positive and negative depending upon the sign of the capacitance change caused by the carrier trapped at the deep level during the bias pulse. In this study only traps which captured the majority carrier were seen, so the peaks were always negative.

A system for producing and analyzing capacitance transients in a diode is diagrammed in Fig. 3.1. It is based on a Boonton model 72BD capacitance meter with a 100 mV, 1 MHz test signal and a dual boxcar integrator. The power supply is used to reverse bias the Schottky barrier through the bias connections provided in the rear of the capacitance meter. A pulse generator is connected to the primary of a pulse transformer. The secondary of the pulse transformer is connected in parallel with a resistor. The transformer secondary and the resistor are placed in series with the diode being studied. When a pulse is applied to the transformer, a voltage drop occurs across the resistor and decreases the bias on the diode, thus providing a reduced bias pulse. The resistance of the resistor is chosen to be much less than the capacitive impedance of the sample at 1 MHz. In this manner, the capacitance meter still measures the actual capacitance of the sample. The capacitance transients produced by reducing the bias on the Schottky barriers are fed from the capacitance meter into the double boxcar integrator, which produces a DLTS spectrum as the temperature is scanned.

Conventional capacitance meters have some limitations when used in a DLTS system. Changing the pulse width by any significant amount requires changing the pulse transformer. When a diode is pulsed, its capacitance changes by a large amount causing the amplifiers in the capacitance meter to overload. A transient with a time constant shorter than the overload recovery time cannot be measured. The output time constant of the Boonton meter used in this system was around 100 μs. Transients with time constants smaller than this could not be measured even if the meter did not overload during the pulse. A fast capacitance bridge was developed by Lang [10] to allow faster transients to be measured. Such a system was also used in these measurements. Both systems gave the same results on any particular sample.

Temperature was scanned by mounting the sample in a glass dewar through which nitrogen gas was flowing. The nitrogen gas could be cooled by bubbling

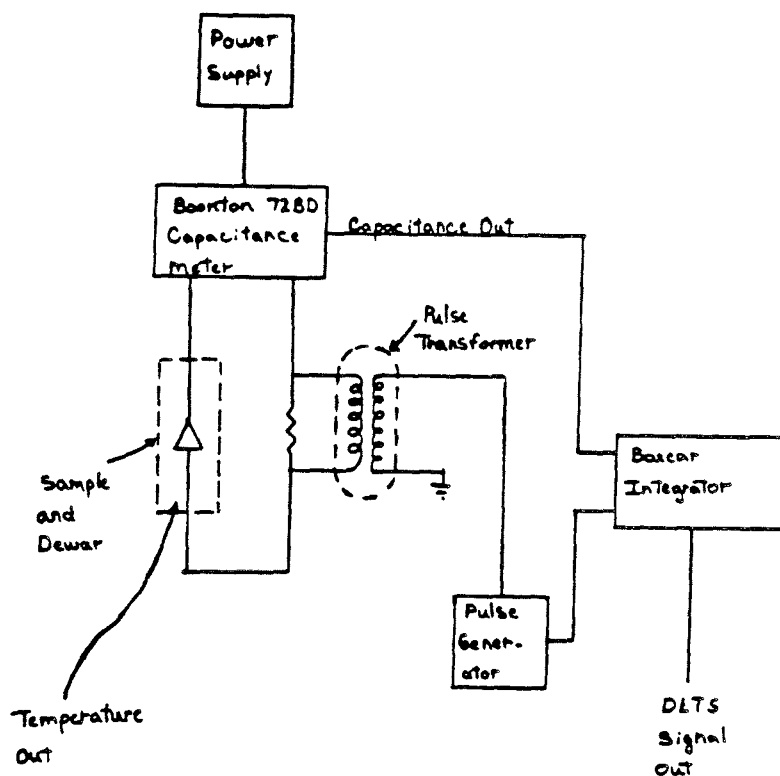

Figure 3.1: Block diagram of a DLTS system based on a model 72BD Boonton capacitance meter.

it through liquid nitrogen prior to entering the dewar. There was also a heater in the nitrogen inlet to the dewar which allowed the gas to be heated before reaching the sample. The temperature of the sample could be scanned from around 100 K to 400 K, using this method. Temperature was measured by placing a type T thermocouple in close proximity with the sample (in many cases both the thermocouple and the sample were affixed to a sapphire plate to maintain good thermal contact and at the same time electrical isolation). The Schottky barriers were electrically contacted by using a Au wire pressure contact.

Reverse bias capacitance characteristics for the Schottky barriers prepared on the CdTe crystals were recorded at room temperature using a model 71A Boonton capacitance meter with a 15 mV, 1 MHz test signal. The capacitance of a Schottky barrier under reverse bias voltage V is given by

$$C = \frac{\epsilon A}{W} \qquad W = \sqrt{\frac{2\epsilon}{Nq}(V + V_{bi})} \tag{3.2}$$

where C is the capacitance, ϵ is the dielectric constant of the semiconductor, N is the space charge concentration in the depletion region (assumed uniform), e is the charge on an electron, W is the depletion width, and V_{bi} is the built-in voltage (Schottky barrier height). From this we find

$$\frac{1}{C^2} = \frac{2}{\epsilon A^2}\frac{1}{Ne}(V + V_{bi}). \tag{3.3}$$

A plot of $1/C^2$ as a function of V should be a straight line. The slope can be used to find N, the shallow level concentration. If N is not uniform, the slope will give N as a function of depth from the Schottky barrier. Deep levels complicate the measurement but are not a problem if their concentration is low enough.

Secondary ion mass spectroscopy (SIMS) was used to depth profile the indium concentration at H_2 annealed and unannealed faces of IN1.[11] The primary

bombardment beam was O_2^+. Positive ions of Cd^{112}, Te^{130}, and In^{115} were collected. The In^{115} ion current was normalized to the Te^{130} signal.

3.4 RESULTS

3.4.1 Measurements on n-type CdTe

There is negligible minority carrier injection in a Schottky barrier device if the barrier height is considerably less than the band gap (as is the case for Au or Cd barriers on n or p-type CdTe).[12] Because of this, only majority carrier traps could be observed in these measurements. In the n-type CdTe, these would correspond to traps which can capture and emit electrons. In p-type crystals, traps would be observed which capture and emit holes. The results of measurements on n-type CdTe crystals will be presented first. Shallow level concentrations (N_D-N_A) for all of these samples were calculated from C-V data and are presented in Table 3.1.

We begin our discussion with the results of measurements on crystal IN1. When devices were prepared on air cleaved faces of IN1, the shallow level concentrations given in Table 3.1 were obtained from the C-V measurements. Since the shallow level concentration is near the In concentration in the material, most of the In donors were uncompensated by acceptors, suggesting this crystal was initially on the Cd excess side of the phase stability region for CdTe. Devices prepared on H_2 annealed surfaces of IN1 gave shallow level concentrations of 3×10^{15} - 5×10^{16} cm^{-3}. SIMS measurements on an H_2 annealed face of IN1 showed a minor surface buildup of In followed by a 2-3 μm layer depleted of In by a factor of two relative to unannealed faces (Fig. 3.2). DLTS spectra for unannealed and H_2 annealed faces of IN1 did not differ markedly as a result of

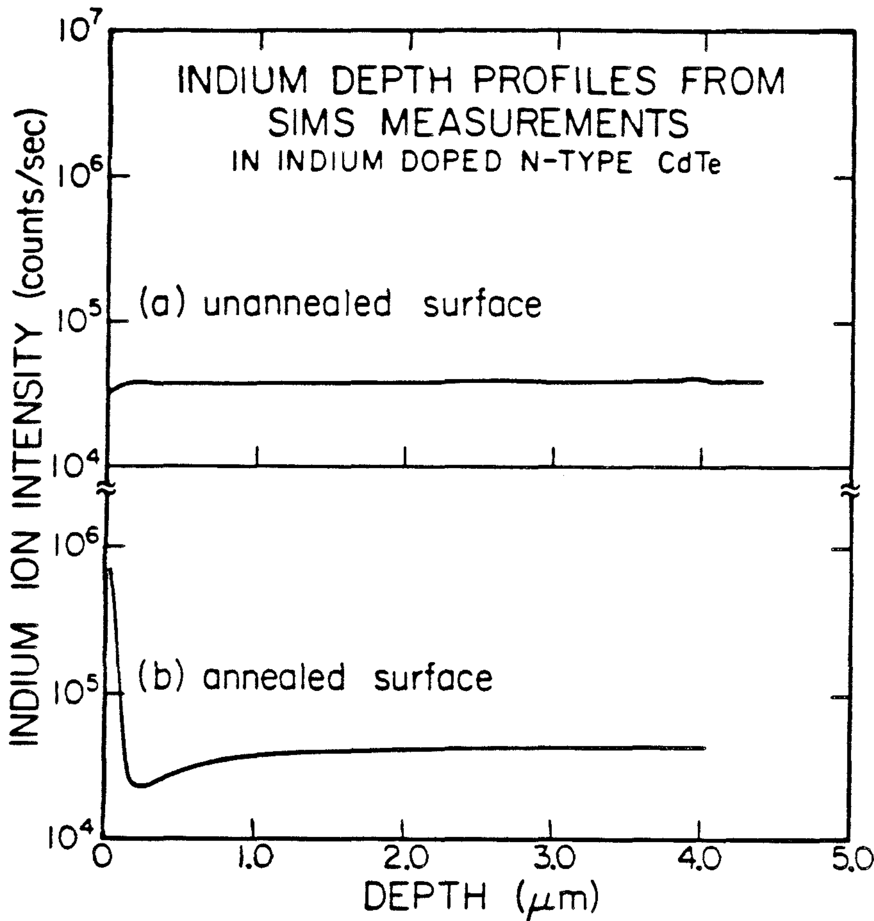

Figure 3.2: Indium depth profiles on H_2 annealed and unannealed faces of Crystal IN1. The unannealed face has a uniform concentration of In as a function of depth. The annealed face shows a minor surface buildup of In followed by a 2 μm layer which is depleted of In by a factor of two or less. Both crystals have the same In concentration at a depth of 3 μm or greater.

the two methods of sample preparation. These DLTS measurements probed a region extending 1-2 μm below the metal CdTe interface. Typical DLTS spectra are given in Fig. 3.3.

Three main electron traps were observed in the temperature range from 100-400 K for IN1 (E1, E2, and E3). A shoulder was visible on the low temperature side of E2 (E2a). Some of the samples also exhibited a level at a lower temperature than E1 which has been labeled E1a. Three different rate windows were used in taking the data in Fig. 3.3 to allow both E1a and E3 to be observed within the temperature range accessible to the DLTS system. The activation energies of levels E1 and E2 were determined from Arrhenius plots of the thermal emission rates from the levels (Fig.3.4). They were 0.34 $\pm$ .06 and 0.77 $\pm$ .05 eV, respectively. The concentrations of E1 and E2 were approximately 3% and 8%, respectively, of the shallow level concentrations in both H_2 annealed and unannealed samples of IN1. Level E3 was not studied in detail. For most of the rate windows accessible with the DLTS system, E3 was observed at sufficiently high temperatures that rapid changes occurred in the Schottky barrier device characteristics. The diodes became leaky and peaks in the DLTS spectra changed in amplitude. Similar observations have been made in previous measurements on CdTe Schottky barriers.[13]

The DLTS spectrum for IN1 was modified by illumination with above band gap light. This effect is illustrated for both air cleaved and H_2 annealed IN1 in Fig. 3.5. The dashed spectrum was taken as the sample was cooled from room temperature to 100 K. During this scan the sample was kept in the dark. The sample was held at 100 K and illuminated with a HeNe laser (any above band gap illumination had the same effect). After exposure to the laser light, a DLTS spectrum was taken with the sample in the dark as temperature was increased (solid curve). In the H_2 annealed samples, E1a increased in amplitude, a new level (E1b) appeared, and a background (E1c) which is visible in the difference

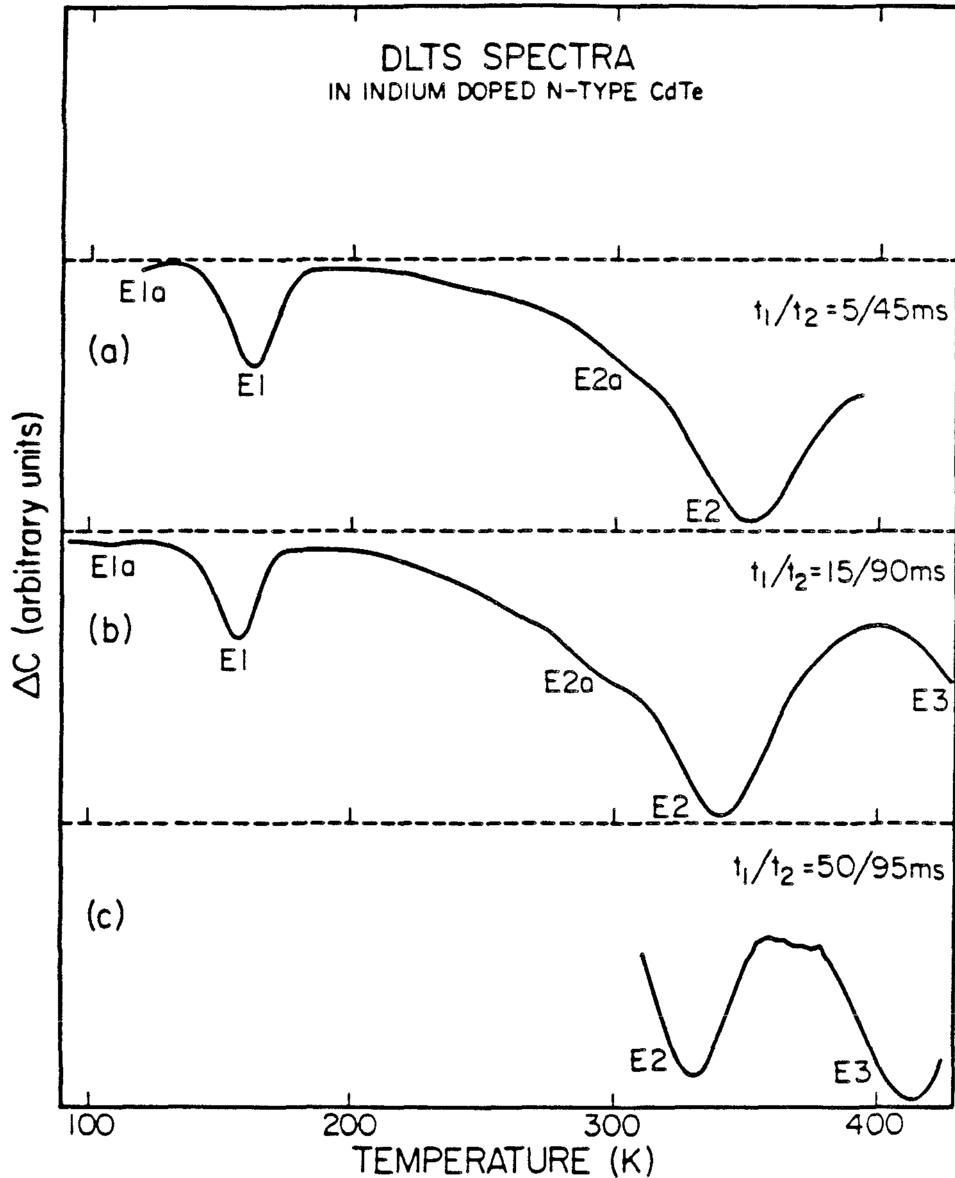

Figure 3.3: DLTS spectra for electron traps in CdTe crystal IN1. The positions of the boxcar windows during the scan are given by t_1 and t_2.(a) A typical spectrum in IN1. (b) Spectrum in IN1 with a smaller rate window. (c) Spectrum in IN1 using an even smaller rate window to show level E3.

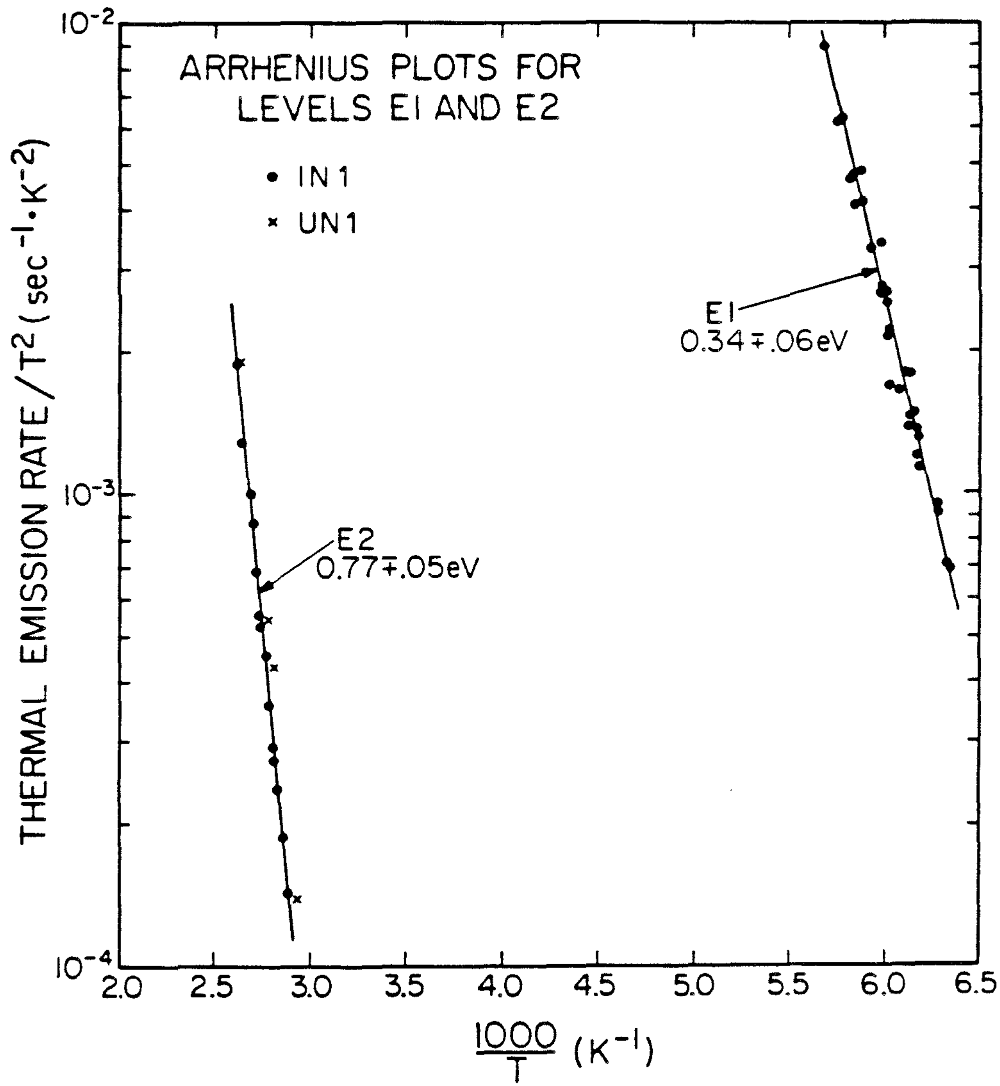

Figure 3.4: Arrhenius plots for traps E1 and E2 seen in n-type CdTe samples.

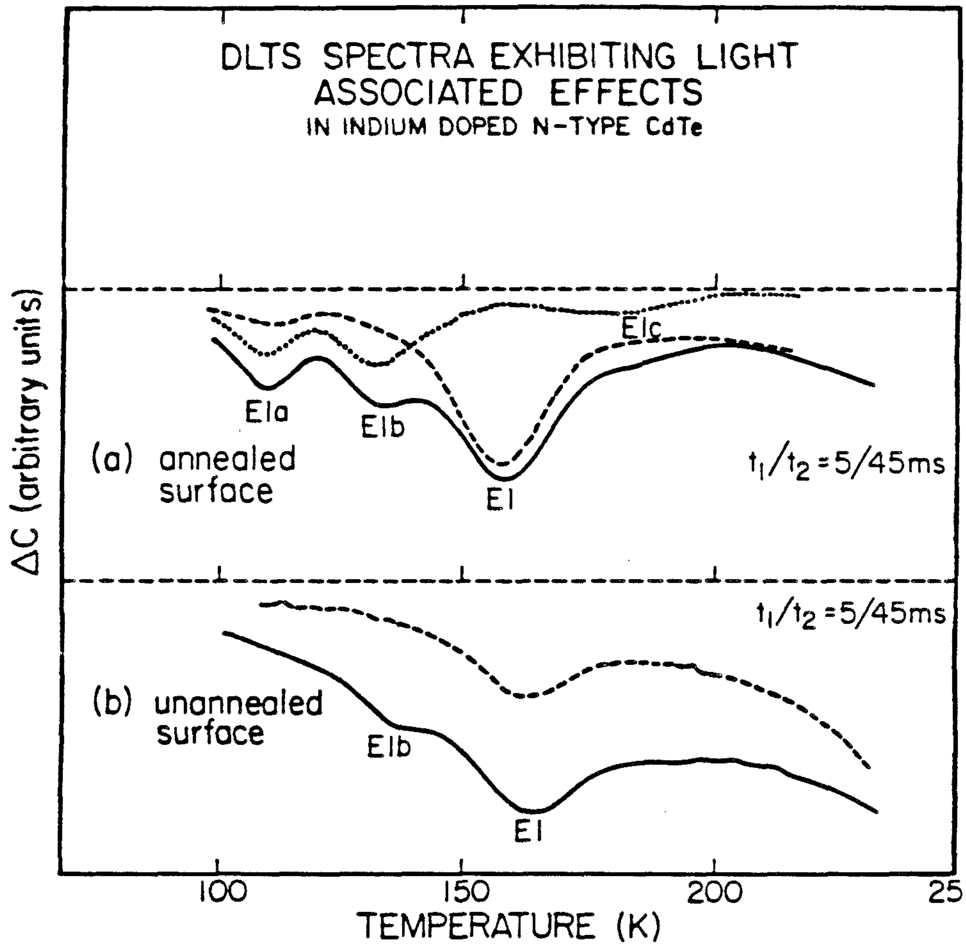

Figure 3.5: DLTS spectra for H_2 annealed (a) and unannealed (b) IN1 in the temperature range of E1 showing the effect of illuminating the sample with above band gap light. The dashed line is the spectrum before illumination, the solid line is the spectrum following illumination, the dotted line in (a) is the difference of these two.

spectrum (dotted curve) appeared under E1. Unannealed samples also showed an increase in the amplitude of E1a. Peaks associated with E1b and E1c could not be resolved, but the overall background of the DLTS signal increased in the temperature range where these peaks were observed in the H_2 annealed samples. The device capacitance at 100 K also increased by 5%-15% as a result of illumination. Changes in the device capacitance and DLTS spectrum persisted for a least an hour after the light source was removed provided the sample temperature remained at 100 K or less during the hour. This observation was independent of the value or polarity of the biasing voltage maintained during the hour. Once the sample was warmed to room temperature, subsequent dark scans again yielded the dashed spectrum of Fig. 3.3. If, following illumination, the sample reached a maximum temperature of between 100 and 200 K, a DLTS scan of the temperature range around peak E1 still showed some of the additional structure, but the effects produced by the light were diminished. This made measurements of the activation energies of E1a, E1b, and E1c difficult. Activation energies for E1a and E1b were estimated as suggested by Lang[10] from the formula

$$E_a \approx \alpha k T_m. \qquad 3.4$$

E_a is the activation energy for the level, k is the Boltzmann constant, T_m is the temperature of the peak maximum (or minimum) and α is a constant. The value of α depends upon the rate window chosen and on the capture cross section of the level in question. Assuming E1, E1a, and E1b have similar capture cross sections allows α to be determined and gives the estimates 0.24 and 0.30 eV for the activation energies of E1a and E1b, respectively. The capture cross section for the trap enters α logarithmically, so a small error in the cross section estimate does not cause a large error in the estimated energies.

Two other In-doped CdTe crystals (IN2 and IN3) were studied using DLTS. Spectra for these crystals are given in Fig. 3.6. The shallow level concentrations

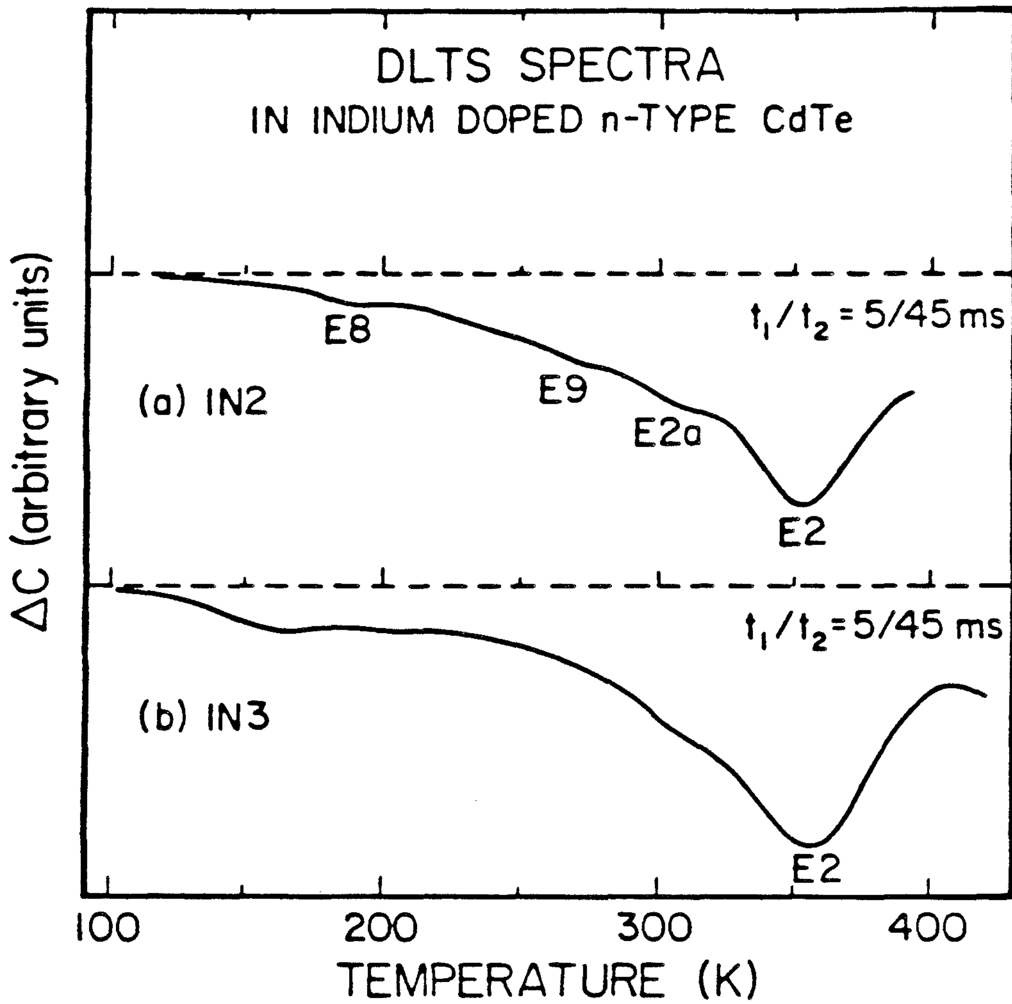

Figure 3.6: DLTS spectra for two n-type CdTe crystals doped with In. (a) Spectrum for IN2. (b) Spectrum for IN3.

following the Cd anneals for IN2 and IN3 were larger than the In-doping in the two crystals, possibly due to other impurities in the crystals or to defects introduced during the anneals. Once again levels E2 and E2a are present. E2a is not visible in the spectrum for IN3 in Fig. 3.6. E3 was also observed in most of these devices, although the temperature range of Fig. 3.6 does not include E3. Other levels are present in these spectra (E8 and E9) which were not seen in IN1. In both of these materials, illumination at low temperatures did cause a capacitance change and an increase in the low temperature background of a subsequent dark DLTS scan, but no new peaks could be resolved from this background. IN3 did have a small peak in the temperature range where E1 was seen in IN1.

The final n-type sample upon which DLTS measurements were made was UN1. Deep levels E2, E2a, and E3 were also observed in this sample. The Arrhenius plot for Level E2 given in Fig. 3.4 contains points taken from UN1. The concentration of E2 was $\sim 5\%$ of the shallow level background concentration. Additional electron traps were observed in this material (E4-E7). No optical effects similar to those present in the In-doped samples were seen in this material, but a stress related effect was discovered. Fig. 3.7 gives typical DLTS spectra for UN1 and illustrates this stress effect. Level E6 was not observed until the crystal was mechanically stressed. Pressure was applied with a blunt probe to the crystal face near the diode to be measured. The solid spectrum in Fig. 3.4 was taken following the application of stress to the crystal. This spectrum was obtained by first cooling the sample to 100 K and then taking DLTS data as the sample was warmed to 400 K. The dashed spectrum was taken immediately after the solid spectrum as the sample was cooled. Peak E6 is missing in the dashed spectrum. Some of the other peaks appear to have a reduced amplitude although this may be due to the loss of the background due to level E6. If the sample was not heated above room temperature following the stress treatment,

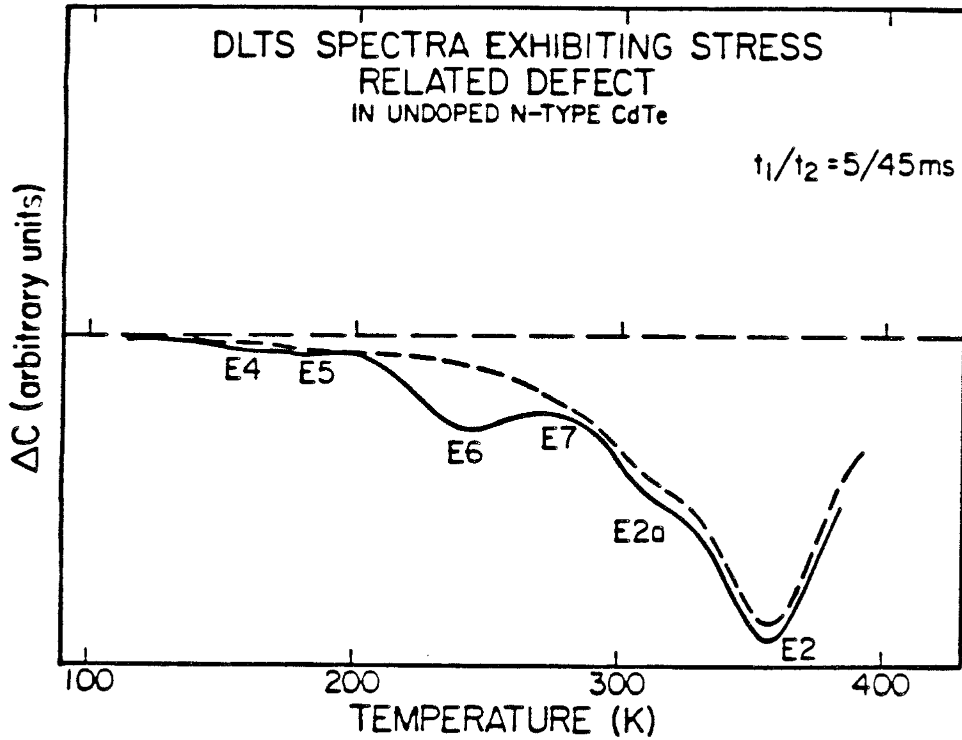

Figure 3.7: A DLTS spectrum for UN1 showing the effect of stress and subsequent sample heating on the levels observed. The boxcar windows are given by t_1 and t_2. The solid spectrum was taken after stress was applied to the crystal; the dashed spectrum was obtained after heating the sample to 400 K in the process of obtaining the solid spectrum.

E6 continued to be observed in the DLTS scans. Elevated temperatures must have allowed the crystal to relax.

The results described so far for crystals IN2, IN3, and UN1 were obtained from material which had been annealed in saturated Cd vapor (as described in the last section) at temperatures between 650 and 750 °C. When the anneal temperature was increased above 750 °C, the results were slightly different. The space charge concentrations obtained from C-V data were in general larger when the crystal was annealed at a higher temperature. If the anneal temperature were increased from 650 to 780 °C, a little less than an order of magnitude increase occurred. For this reason the values given in Table 3.1 are not exact. The DLTS spectrum of a sample annealed at temperatures exceeding 750 °C was dominated by a level at approximately the same temperature location as E2a. Level E2 was still observable, but its amplitude was lower than the amplitude of the new level. The activation energy of the new level was 0.60 ± .05 eV. The deep level concentrations in a sample annealed at higher temperatures were all a few percent of the shallow level concentration. These same observations were made in all three of the Cd annealed crystals.

3.4.2 Measurements on p-type CdTe

Results of the electrical measurements on p-type CdTe crystals will be presented next. Shallow level concentrations (N_A-N_D) for the p-type CdTe crystals are given in Table 3.1. As was mentioned above, only majority carrier (hole) traps were measurable in the p-type samples. No differences were observed in the DLTS spectra of p-type CdTe crystals as a result of the method of device preparation.

Four majority carrier deep levels were seen in the p-type crystals in the temperature range from 100–300 K. Figs. 3.8–3.11 give characteristic DLTS spectra

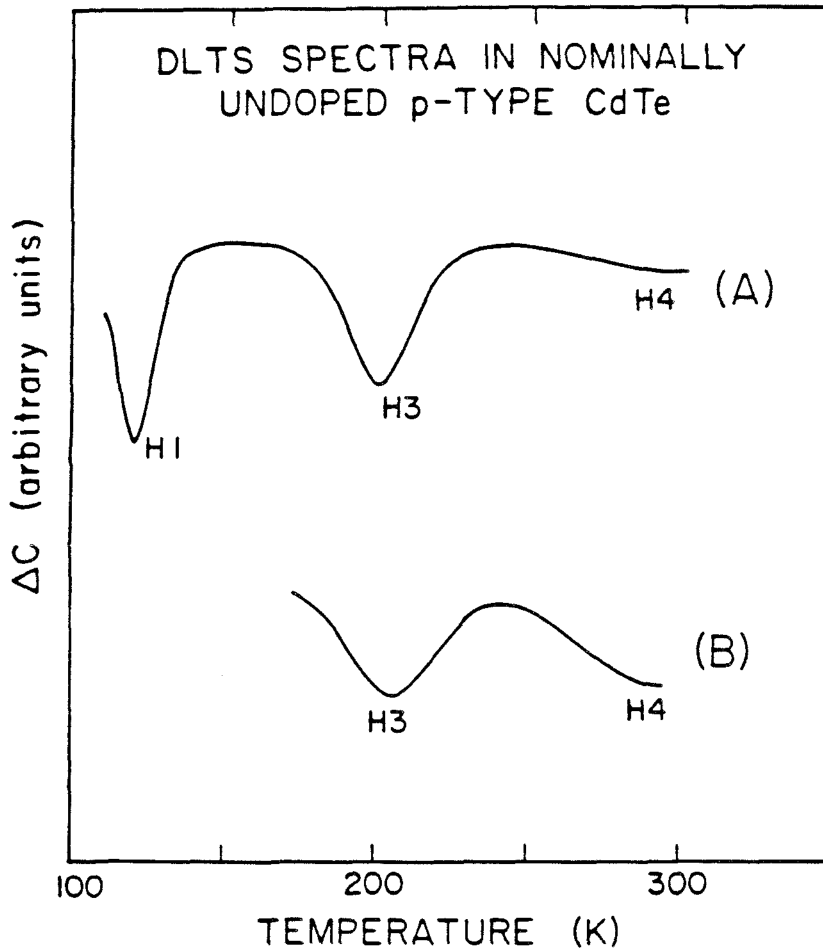

Figure 3.8: Characteristic DLTS spectra for hole traps in nominally undoped, p-type CdTe crystals A and B. The positions of the boxcar windows during the scans were $t_1 = 5$ ms and $t_2 = 45$ ms.

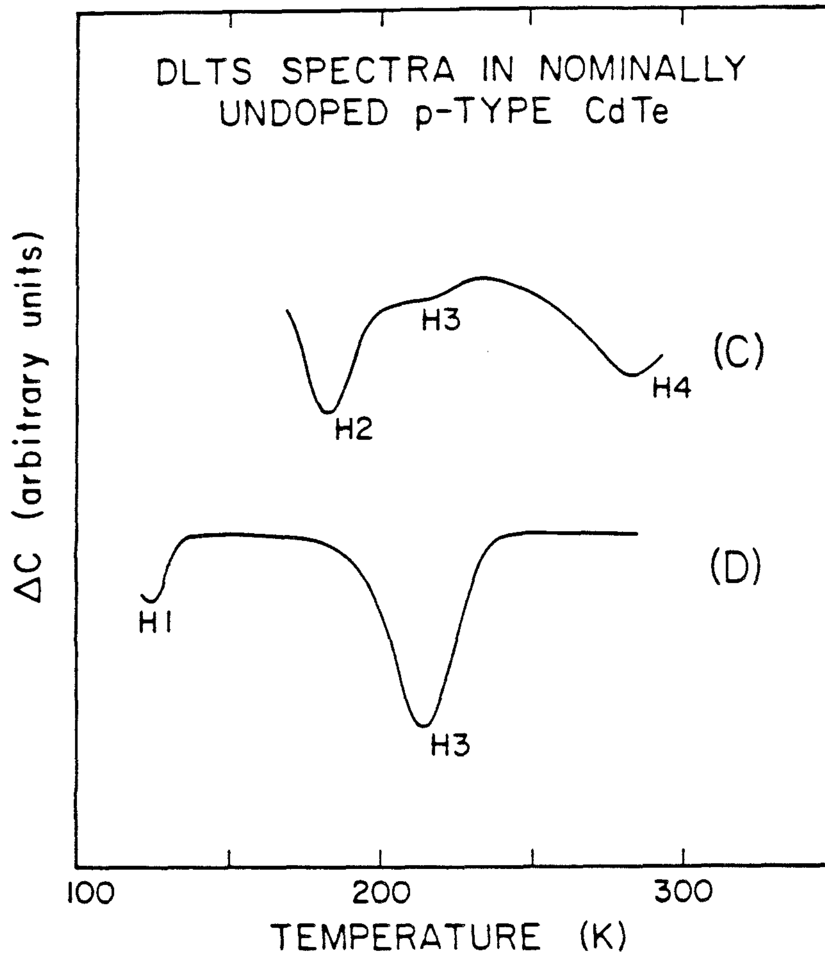

Figure 3.9: Characteristic DLTS spectra for hole traps in nominally undoped, p-type CdTe crystals C and D. The positions of the boxcar windows during the scans were $t_1 = 5$ ms and $t_2 = 45$ ms.

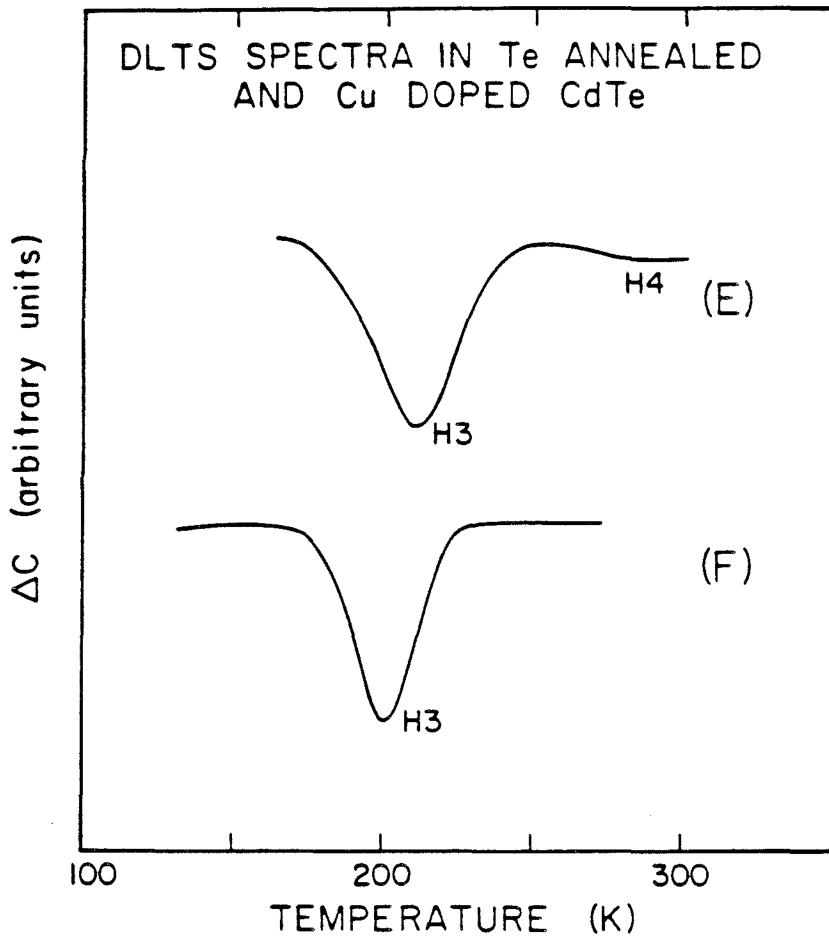

Figure 3.10: Characteristic DLTS spectra for Te-annealed (E) and Cu-doped (F) p-type CdTe. The positions of the boxcar windows during the scans were $t_1 = 5$ ms and $t_2 = 45$ ms.

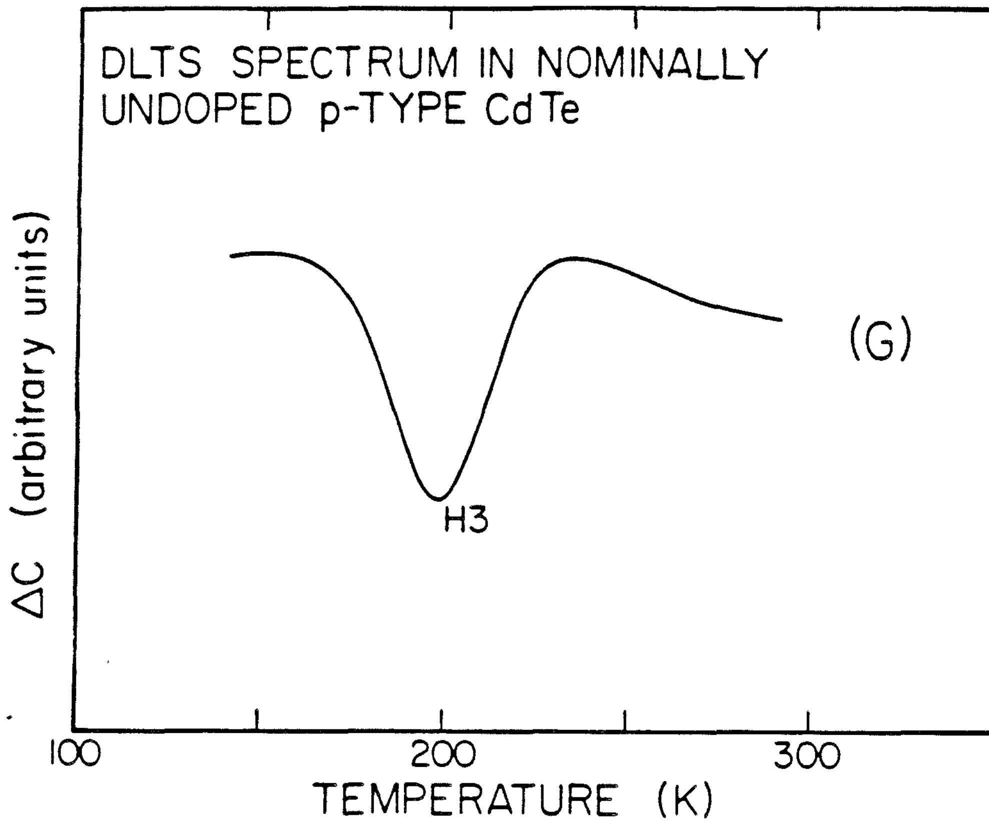

Figure 3.11: Characteristic DLTS spectra for hole traps in nominally undoped, p-type CdTe crystal G. The positions of the boxcar windows during the scans were $t_1 = 5$ ms and $t_2 = 45$ ms.

for the samples. The four levels have been labeled H1-H4. Deep-level H1 was seen in A (Fig. 3.8) and D (Fig. 3.9) at concentrations of 1×10^{14} and 3×10^{13} cm^{-3}, respectively. As in the case of the traps in the n-type samples, these concentrations are a few percent of the shallow level concentrations. H1 may have been present in F but at a very low concentration. The low temperature region where H1 occurred was scanned for all the crystals, although it is only shown for A and D. Level H2 was only seen in crystal C (Fig. 3.9). Its concentration was between 2×10^{13} and 3×10^{14} cm^{-3}. Levels H3 and H4 were seen in all of the crystals (Figs. 3.8–3.11). Level H3 appeared over approximately a 5 K range of temperatures in the samples studied. This variation was even observed in samples taken from the same crystal. The concentrations of H3 in crystals A through D were 4×10^{13} - 4×10^{14}, 1×10^{12}, 3×10^{13} - 3×10^{14} and 2×10^{13} - 1×10^{14} cm^{-3}, respectively. In G (Fig. 3.11) its concentration was 4×10^{12}. H3 in E and F will be discussed below.

There was a lot of fluctuation in the trap concentrations, as can be seen from the above values. These fluctuations even occurred from device to device on the same sample. In the case of level H4 this effect was more pronounced. At the sensitivity used in the spectrum chosen for D in Fig. 3.9, the level was not visible, although, in other cases, its concentration matched that of H3. These deep trap concentrations were estimated from the formula

$$2\frac{\Delta C}{C} = \frac{N_d}{N_s}, \tag{3.5}$$

where C is the capacitance of the diode, ΔC is the change in capacitance caused by completely filling the deep level, N_d is the deep-level concentration, and N_s is the shallow level concentration taken from table 3.1.[5] Effects due to the edge of the depletion region are neglected using this method, but such accuracy is not necessary in light of the large variations in trap concentrations which were mentioned above.

Material E was CdTe which had been taken from crystal B and annealed in Te vapor at 800 °C for about two hours. The anneal caused the shallow level concentration to increase by two orders of magnitude. This is similar to the effect of Cd vapor anneals on n-type CdTe crystals. As can be seen from Fig. 3.10, H3 and H4 were still present. H3's concentration was approximately 5×10^{14} cm^{-3}. This value is also about two orders of magnitude higher than prior to the anneal.

Crystal F had been doped with Cu at about 10^{16} cm^{-3}. This concentration is close to the shallow level concentration obtained from the C-V profile and may indicate that the Cu dopants were not strongly compensated by native defects. The DLTS spectrum for F, as seen in Fig. 3.10, contains H3 at a concentration of 4×10^{13} cm^{-3}, a value similar to that found in the undoped crystals. H4 was also present at a much lower concentration and is not seen in the spectrum shown. Attempts were also made to dope crystals with Cu following procedures outlined by Ref. 14. Again, there were no new levels or significant enhancements of existing levels.

Other trapping states were visible in the above room temperature range of the spectra, but it was not possible to study them, because, after the samples were heated to 400 K in the process of taking the data, changes occurred in the DLTS spectra. Levels which were seen above room temperature left completely. Some of the below room temperature levels also suffered concentration increases or decreases of as much as an order of magnitude. The direction of the change was not always the same. For this reason no above room temperature spectra are given. The DLTS spectra shown are for unheated samples immediately after preparation.

Arrhenius plots for levels H1-H4, along with their associated activation energies, are given in Fig. 3.12. Capture cross sections for the various states in both n-type and p-type CdTe were not directly measurable with our system,

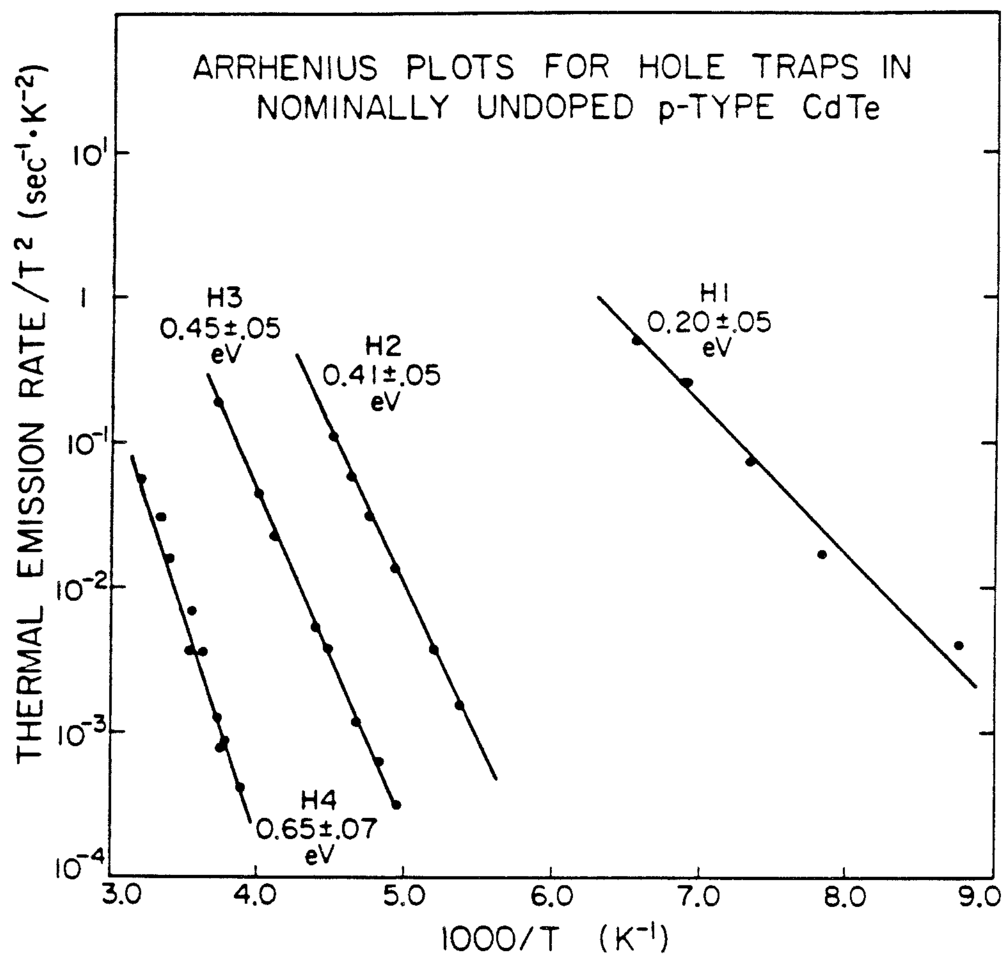

Figure 3.12: Arrhenius plots for the four majority carrier deep levels seen in DLTS measurements on p-type CdTe.

because, for the shortest reduced bias pulse we could apply ($\approx$ 20ns), all the levels were completely filled. From this we can place a lower bound of 5×10^{-14} cm^2 on the capture cross sections of the traps for their associated majority carrier, a value which is in reasonable agreement with that determined from the y intercepts of the Arrhenius plots. Because of this, the activation energies in Figs. 3.4 and 3.12 have not been corrected for temperature dependent cross sections. No correction for electric field effects has been applied either. The data used for H3 in Fig. 3.12 is for a particular device. When other devices were used, the temperature fluctuations mentioned above caused the line to shift, but the slope stayed within the error range given.

3.5 DISCUSSION

The effect of H_2 annealing on material IN1 was studied because such an anneal may be performed as one of the cleaning steps in the growth of HgTe or the alloy $Hg_{1-x}Cd_xTe$ on CdTe by chemical vapor deposition techniques (CVD),[6] and it is desirable to know what effect the anneal has on the defect structure of the CdTe. The anneal did not introduce any new deep levels or cause any existing levels to leave. The predominant effect of H_2 annealing IN1 was the observed drop in shallow level concentration, and the approximately proportional drop in deep level concentrations. The decrease in In concentration at annealed surfaces as measured by SIMS is not sufficient to account for the observed drop in shallow donor concentration. Two possibilities remain. Either the In became electrically inactive, as might happen if indium telluride precipitates had formed, or native defects were introduced which compensated the In donors.

Level E2 is present in all of the n-type samples. This identification is supported by the fact that plots of the emission rate as a function of temperature

for E2 in different crystals are the same. Data from both IN1 and UN1 have been included in the Arrhenius plot of Fig. 3.4 to illustrate this point. The shoulder identified as E2a in each of the n-type samples probably arises from a level which is present in all of the n-type samples. The same can be said for peak E3. This suggests that E2, E2a, and E3 are probably associated with native defects or with impurities which are commonly found in CdTe crystals. Impurities could have been introduced during the Cd vapor anneals. Since IN1 was not annealed in Cd vapor and levels E2, E2a, and E3 were present in its DLTS spectrum, it does not seem likely that the levels are due to impurities introduced at anneal time. When the CdTe crystals were annealed at higher temperatures, a new level dominated the spectrum although E2 was still visible. The new level could actually have been E2a with an increased amplitude. The properties of E2a were not determined well enough to say for certain. This change in the DLTS spectrum with anneal temperature suggests that the concentrations of the centers responsible for levels E2 and the new level are dependent on the Cd partial pressure and sample temperature during the anneal. Levels E4-E9 observed in some of the samples may have been present in all of the n-type crystals. The background was too large to make conclusive measurements.

Two other studies of n-type CdTe have been made using DLTS measurements.[15,16] Some of the crystals used in these studies were annealed in Cd-vapor to raise the shallow level concentrations in the samples. In Ref. 15 two levels labeled E7 and E8 were observed which had activation energies near that of E2 in this study (0.66 and 0.80 eV, respectively). The authors also noted that the relative amplitudes of peaks in their spectra changed as a function of the Cd-vapor pressure during the anneal. In Ref. 16 two crystals were studied. The first had a deep state labeled EH5 which had an activation energy of 0.78 eV. This almost certainly corresponds to E2 seen in this study. In the second crystal studied in Ref. 16, a level labeled EG6 was observed with an activation

energy of ~0.84 eV which was assigned the same origin as EH5 and probably also corresponds to level E2 reported here. It is interesting to note that all of the DLTS spectra presented here for n-type CdTe and described in Refs. 15 and 16 are very similar in the temperature range from room temperature to 400 K.

Levels E1, E1a, E1b, and E1c are probably In related. They would be expected to appear in IN2 and IN3 with concentrations several orders of magnitude less than in IN1, because the In concentration in IN1 is so much larger than in IN2 and IN3. If they did have concentrations which were within the detectability limits of the DLTS, they would probably have been buried in the background of other peaks present in IN2 and IN3. A deep state with a low concentration was visible in IN3 at approximately the right temperature to be E1. Above band gap illumination of IN2 and IN3 did cause an increase in the DLTS background at the temperature where E1 should be visible. This might be expected if the optically induced levels were present at a very low concentration. Electron emission from E1b, E1c and to a certain extent E1a occurs only after above band gap illumination. The predominant effect of this illumination is the creation of electron-hole pairs in the depletion region. Since electrons can be introduced into the depletion region electrically, the appearance of these levels in the spectrum can be attributed to the presence of holes in the depletion region. This suggests that there are associated hole traps in the depletion region which must bind holes before these electron traps can be observed. Increased device capacitance following illumination supports this conclusion. Similar conclusions have been drawn from observations of DLTS spectra in InP.[17] Persistent photoconductivity and photocapacitance have previously been observed in CdTe,[18,19] but this is the first study correlating them with changes in DLTS spectra.

In the work of Ref. 16, In-doped samples were studied with DLTS. For a sample with a shallow level concentration of 1.4×10^{17} cm^{-3} the spectrum was very much like that obtained for H_2 annealed IN1. Three levels labeled EH1,

EH2, and EH3 were observed which had nearly the same activation energies and relative concentrations as E1b, E1a, and E1 observed here (as mentioned above, a level EH5 corresponding to E2 in this study was also observed). Although levels with energies and concentrations near those of E1, E1a, and E1b were reported in Refs. 15 and 16, three states with these energies were not observed together in any of the other crystals studied here or in the two other DLTS studies of CdTe. This adds additional evidence that they may be In related. It would be interesting to know if the spectrum in Ref. 16 was taken with the sample exposed to light.

Identifying the centers responsible for levels E1a, E1b, and background E1c is not possible without additional information. We can, however, propose a model. Because all of the levels are affected by illumination, it seems likely that the centers responsible for each of these levels are of a similar nature. One possibility is that each center results from a different configuration of a defect complex involving In.

The crystal defects responsible for the deep levels observed in the p-type CdTe could not be directly identified. Still, it is possible to draw some conclusions about them based on the results of these measurements. Levels H1 and H2 were specific to certain crystals and are, therefore, likely candidates for impurities. Levels H3 and H4, on the other hand, were present in all of the p-type crystals. As was the case for level E2 in the n-type material, they could be the result of a common impurity, native defects, or even grosser crystal defects (such as Te precipitates). There have been previous reports of levels approximately 0.3 eV from the valence band that were due to Cu, Au and Ag.[2,18] Identifications were based on associating the levels that were observed with the crystal dopants. Although Au and Ag diffusions have yet to be tried, the present work seems to indicate that the levels we observe are not due to Cu, since the presence of Cu in crystal F did not enhance any of the levels seen, and because the

attempts at Cu doping did not significantly increase the concentrations of any of the traps. It is possible that there are deep levels associated with Cu, but that the temperature range of this study did not include Cu related peaks.

In both the n and p-type crystals, concentrations of deep levels in as-grown crystals were generally 10^{14} cm^{-3} or less. Although this is quite low, fluctuations were also seen in the concentrations of traps from device to device on a given sample. Even more disturbing were the changes in peak amplitudes produced by very modest sample heating (400 K). These fluctuations and amplitude changes were more prevalent in the p-type crystals. Since the same levels were observed for both Au and Cd barriers on the p-type crystals, it is unlikely that the changes occurred as a result of diffusion of the barrier metal into the active region of the CdTe diode.

In attempting to identify the origins of the levels seen in the n-type and p-type CdTe, the situation is complicated by the need to understand the role played by native crystal defects. Those levels which were only present in a few crystals (E1, E1a, E1b, H1, and H2) are almost certainly associated with impurities, but the center giving rise to a particular level could be due to a complex which is composed of an impurity and a native defect. Some levels such as E2 in n-type CdTe and H1 and H2 in p-type CdTe were present in all of the samples. It is tempting to assign these deep levels to native crystal defects. This would help account for the variation in the concentration of these levels when the crystals were annealed under various conditions such as in H_2, in Cd vapor, or in Te vapor. It might also help explain why some of the states had large concentration changes when the samples were heated to 400 K. Still, impurities may be able to account for these levels. Some impurities such as Si are expected to occur commonly in CdTe because of the method of growth (a Si crucible is used.) An anneal which changes the Cd or Te activity of a crystal could cause an impurity to change sites, and therefore change the concentration of a level

which is due to the impurity in a particular configuration. An example of this might be a change in the concentration of In-Cd vacancy complexes caused by anneals in Cd vapor. It is really only possible to say that levels such as E2, H3, and H4 are due to crystal defects or to impurity related defects where the concentration of the defect can be altered by changing the Cd or Te activity of the crystal.

3.6 CONCLUSIONS

In this chapter the results of DLTS and C-V measurements on n-type and p-type CdTe have been reported. Levels were observed which were common to all of the n-type samples (E2) and which had been observed in other DLTS studies of CdTe. Other states (E2a, and E3) were probably present in all of the n-type crystals. In an In-doped sample, several peaks (E1a, E1a, and E1c) were observed only after illumination of the sample with above band gap light at low temperatures. These levels along with E1 were probably indium related. One sample exhibited a deep level when it was stressed. The level left when the stress was relieved by warming the sample. DLTS measurements on p-type CdTe crystals revealed four deep levels (H1-H4) in the temperature range from 100-300 K. Levels H1 and H2 only occurred in a few of the samples leading us to believe that they were associated with impurities in the crystals. H3 and H4 were in every crystal and may be related to native defects or common impurities. Measurements on Cu doped samples indicate that the levels seen in p-type CdTe are not due to residual Cu in the CdTe. In both n and p-type CdTe, variations were noticed in the concentrations of the observed levels from device to device on a given sample. Significant changes in trap concentrations as a result of modest sample heating were also seen. These effects were more pronounced in the p-type material.

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APPENDIX A

MEASUREMENTS OF THE DERIVATIVES OF CURRENT-VOLTAGE CURVES AND MEASUREMENTS OF CAPACITANCES USING MODULATION TECHNIQUES

A.1 INTRODUCTION

This appendix covers the details of the tunneling and capacitance measurements which were made in the study described in Chapter 2 of this thesis. It is organized into the following sections. In Section A.2 the mathematics of modulation techniques as applied to the measurements of first derivatives (dI/dV) and second derivatives (d^2I/dV^2) of I-V curves will be presented along with the reasons for using these techniques. Section A.3 will illustrate how these techniques were implemented in taking first derivatives. The second derivative measurement system will be discussed in detail in Section A.4. The system used in making frequency dependent capacitance measurements will be described in Section A.5

A.2 MODULATION TECHNIQUES

As was explained in Chapter 1, inelastic and resonant tunneling effects are usually observed in the derivative spectra of the I-V curves of tunneling devices. The most obvious way to take the derivative of an I-V curve is to apply a current source to the device under study, measure the resultant voltage, and numerically differentiate the I-V curve thus obtained. There are two major difficulties with this method. The measurements made using this technique are DC measurements, and 1/f noise is large at low frequencies, so a considerable amount of averaging is required to obtain a good signal to noise ratio in the derivatives. Coupled with this problem is the dynamic range limitation of the instruments used to measure the voltage and current. The smallest voltage and current increments measurable determine the ultimate sensitivity to changes in the slope of the I-V curve. Both of these difficulties are avoided when modulation techniques are employed. The frequency of the modulation signal can

be picked to improve the signal-to-noise ratio relative to DC measurements. Modulation techniques, in some sense, take the difference between two voltages before digitizing the result, while the DC technique described above digitizes and then takes the difference. The dynamic range limitation is thus removed. Although the fundamental limitation in a DC measurement system is dynamic range, voltmeters can be purchased with a dynamic range of 10^5, so, in general, the noise problems are more important in a realistic system.

Modulation techniques involve varying one of the two variables I and V sinusoidally while observing the Fourier components of the signal associated with the other variable. Consider a device with a current-voltage curve given by $I(V)$. If a small sinusoidal modulating voltage $\Delta v = v_\omega \sin \omega t$ is superimposed on a fixed voltage V_0 and applied to the device, the device current as a function of time ($I(t)$) can be expanded in a Taylor series to give

$$I(t) = I(V_0) + \frac{dI}{dV}(V_0)\ v_\omega \sin \omega t + \frac{1}{2}\frac{d^2 I}{dV^2}(V_0)\ {v_\omega}^2 \sin^2 \omega t + \cdots. \qquad (A.1)$$

The largest contribution to the component of the current at frequency ω comes from the second term in the above expansion. Other terms of higher order in $\sin \omega t$ also contribute to the current at the fundamental frequency (such as the $\sin^3 \omega t$ term since $\sin^3 x = \frac{3}{4} \sin x - \frac{1}{4} \sin 3x$), but these terms have prefactors of the form $\frac{d^n I}{dV^n} {v_\omega}^n$ which are negligible as long as I as a function of V is sufficiently smooth and v_ω is sufficiently small. From this we see that a measurement of the amplitude of the current at the fundamental frequency ω gives

$$\frac{dI}{dV}(V_0)\ v_\omega, \qquad (A.2)$$

and if v_ω is known, the first derivative of $I(V)$ at bias V_0 can be obtained. The largest contribution to the current at the second harmonic frequency (2ω) comes from the third term in Eq. A.1. The amplitude of the second harmonic signal is

$$\frac{1}{4}\frac{d^2 I}{dV^2}(V_0)\ {v_\omega}^2. \qquad (A.3)$$

Given v_ω the second derivative of $I(V)$ at the bias V_0 can be found.

There are a few important points to make about this technique. The signal at the fundamental frequency (Eq. A.2) is proportional to v_ω, while the second harmonic signal (Eq. A.4) varies as $v_\omega{}^2$. In an actual measurement system, increasing v_ω increases the signal to noise ratio. This is especially true in the case of the second derivative. On the other hand, increasing v_ω also increases the contribution of higher order terms in Eq. A.1 to the fundamental and harmonic signal since their contribution is proportional to $(v_\omega{}^n)$ and $n > 2$. Said in a different way, increasing v_ω decreases the resolution. This is a trade-off which is inherent in measurements by harmonic generation.

The $I(V)$ relation which was expanded in Eq. A.1 gives the steady-state current which would pass through a device if a particular voltage V were applied to the device (it is basically the I-V curve which would be obtained from the DC measurement scheme described above). The expansion in Eq. A.1 makes the assumption that the response of the current to voltage is the same at frequency ω as it is in steady state, but this is not necessarily true. Most tunneling structures have significant capacitances. The steady state response of the current to applied voltage for a tunneling structure only reflects the resistive component of the structure's impedance. When a high frequency sine wave is applied to the device, a contribution to the current through the device from the structure's capacitance must be included in equation A.1 to obtain the actual current passing through the device. In the measurement systems discussed below, the differences between the AC and DC responses of real devices become very important.

The design of the first derivative system, which is given below, essentially follows Eq. A.1 (except V is considered to be a function of I). In the case of the second derivative measurement, the system described below takes into account the need to reduce the modulating voltage for the purpose of improving resolution, and at the same time obtain the maximum signal-to-noise ratio from

measurements on real tunneling devices.

A.3 FIRST DERIVATIVE MEASUREMENT

The circuit diagram for the basic system used in making first derivative measurements is given in Fig. A.1. The ideas are rather simple and will only be discussed briefly. Resistors R_1 and R_2 are chosen to be much greater than the sample impedance. If v_ω is the modulation voltage being output by the sine wave generator, the modulation voltage appearing across the sample is

$$v_{mod} \approx \frac{v_\omega}{R_1}\left(\frac{1}{R_s} + i\omega C_s\right)^{-1} \tag{A.4}$$

where R_s and C_s are the differential sample resistance and capacitance, respectively. If the frequency is low enough or C_s is small enough, the term in ωC_s can be neglected and

$$v_{mod} \approx \frac{v_\omega}{R_1} R_s. \tag{A.5}$$

Scanning V_{ramp} (the DC bias being applied by the voltage source) allows V_s (the DC bias on the sample) to be scanned, and if R_1 and v_ω are known, the lockin amplifier will output v_{mod} which will be captured by the signal averager and can be normalized to give R_s as a function of V_s. Since R_s is dV/dI, the signal averager captures the first derivative spectrum (or the inverse of it). The ramp is usually scanned repetitively and the traces averaged to increase the signal to noise ratio. The sample is cooled by placing it in a liquid helium storage dewar.

In terms of the modulation technique explanations of the last section, a sine wave source with a large resistor at its output becomes a current source of frequency ω with the current amplitude given by $i_\omega \approx \frac{v_\omega}{R_1}$. Similarly, a voltage ramp with a large resistor at its output becomes a current source with current

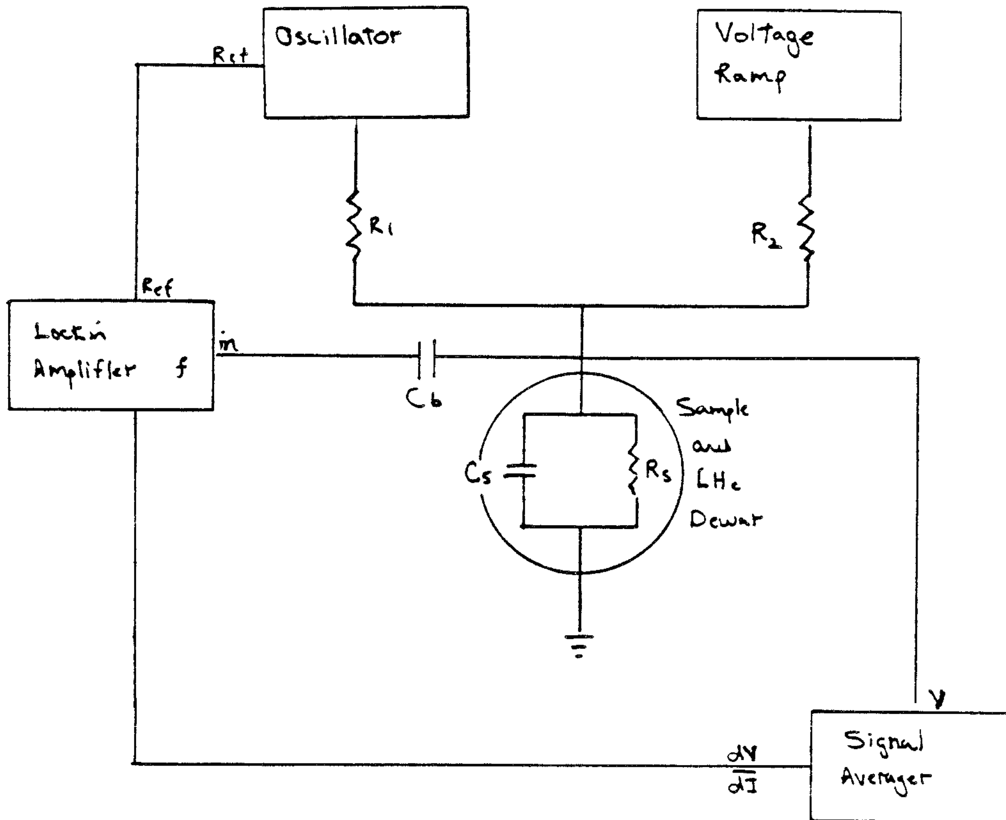

Figure A.1: Diagram of the first derivative system used in making the measurements given in Chapter 2.

$I_0 \approx \frac{V_{ramp}}{R_2}$. In analogy to Eq. A.1, we find

$$V_s(t) = V_s(I_0) + \frac{dV}{dI}(I_0)\ \frac{v_\omega}{R_1} \sin \omega t \cdots \tag{A.6}$$

and the amplitude of the voltage at the fundamental frequency becomes

$$\frac{dV}{dI}(V_0)\ \frac{v_\omega}{R_1} \tag{A.7}$$

as given in Eq. A.5.

Note that although Eq. A.7 agrees with Eq. A.5, it does not contain the capacitive term given in Eq. A.4. This happens because, as was mentioned in the last section, Eq. A.7 is an expansion of the steady-state I-V curve and does not include any capacitive contributions to the current. The approximation made in Eq. A.5 involves neglecting this capacitance. First derivative measurements were made at a frequency of 5 kHz or less to reduce problems associated with the intrinsic sample capacitance. The reduction of stray capacitances in the system became important in the first derivative measurements on more resistive samples. In general the system was calibrated and the effects of stray and sample capacitances were checked by making measurements on known resistances of approximately the same value as the sample resistance. The capacitor C_b in Fig. A.1 was chosen to have a value that blocked the DC ramp voltage and avoided overloading the lockin amplifier, while, at the same time, it allowed the lockin to see the modulation signal. This method of taking the first derivative was used because it provided sufficient signal-to-noise to see the desired features and was relatively simple to set up. More elegant systems can certainly be built. In the case of the second derivative measurement, a more carefully designed system was required.

A.4 SECOND DERIVATIVE MEASUREMENTS

A system similar to the one described in the last section could have been used to make second derivative measurements. The signal-to-noise ratio of such a system would have been poor for two reasons: Second derivative signals are usually smaller than first derivative signals. The noise figure of the the lockin preamplifier is large for the low frequencies at which the measurement is made and for the typical resistances of the samples which were studied. As an example, the noise figure of a PAR model 113 preamplifier at a frequency of 1 kHz and sample impedance of 50 Ω is around 20 db. This means that the noise voltage added by the amplifier to the signal from a 50 Ω sample is about ten times the room temperature Johnson noise of the sample. Most of these measurements are made with the sample at 4.2 K, so the noise added by the amplifier is actually about 85 times larger than the actual sample Johnson noise. The Johnson noise of the sample is the fundamental limit to the second harmonic voltage which could be generated by the sample and seen. The noise voltage of the amplifier, then, limits the minimum value for v_ω, the modulation voltage applied to the sample, to a value about $9 \approx \sqrt{85}$ times larger than the fundamental limit set by the Johnson noise. This is a significant degradation in the sensitivity of the second derivative measurement.

To reduce the noise problems, the frequency of the measurement is usually increased, and a step-up transformer is used at the lockin input to match the sample impedance and the measurement frequency to the operating point at which the lockin preamplifier has the best noise figure. When this is done, the sample capacitance becomes a problem. At higher frequencies, the capacitance shorts out the AC voltages which appear across the sample. Also, stepping up the sample impedance allows the sample to see a reduced lockin amplifier input impedance. Both of these effects work to decrease the second harmonic signal and, once again, degrade the signal-to-noise ratio. The system for measuring

second derivatives which will be described below deals with the problems associated with the significant sample capacitances and with reduced lockin amplifier input impedances shorting out the second harmonic signal across the sample.

Before discussing the specifics of the measurement system, some of the problems caused by large sample capacitances will be illustrated by finding the amplitude of the second harmonic voltage ($v_{2\omega}$) appearing across a sample when the voltage at frequency ω appearing across the sample is given by v_ω. In this analysis it will be assumed that there is a voltage across the sample at frequency ω given by v_ω, a voltage across the sample at frequency 2ω which is given by $v_{2\omega}$, a voltage across the sample at 3ω which is given by $v_{3\omega}$, etc. The values of all of these voltages are variable and may in fact be zero, except for v_ω which is fixed. Basically this is a break-up of the total voltage across the sample into its Fourier components. The sample may be modeled as a nonlinear resistor of differential resistance R_s in parallel with the sample capacitance given by C_s. The total current at frequency 2ω passing through the sample can be found by adding the currents at frequency 2ω which would be produced if each of the Fourier components of the voltage were applied across the sample independently (a linear analysis such as this neglects mixing in the nonlinear tunneling element, but mixing terms will be of lower order than the terms which are considered). Only v_ω and $v_{2\omega}$ contribute to the current at frequency 2ω. The voltage v_ω creates a second harmonic current through the nonlinear sample resistance which is given by

$$\Delta I_1 = -\frac{1}{4}\frac{d^2 I}{dV^2} {v_\omega}^2 \tag{A.8}$$

as was shown in Eq. A.1. Since the voltage $v_{2\omega}$ also appears across the sample, it will produce a current at frequency 2ω passing through the sample. Following Eq. A.1, this current is given by,

$$\Delta I_2 = v_{2\omega}\frac{dI}{dV} e^{i\phi} \tag{A.9}$$

where a phase factor has been introduced to allow $v_{2\omega}$ to be out of phase with ΔI_1. Since the second harmonic voltage across the sample is also being applied to the linear circuit elements in parallel with the sample, the current through these elements is

$$I_{2\omega} = -\frac{v_{2\omega}}{Z}e^{i\phi} \tag{A.10}$$

where Z is the effective impedance of the rest of the circuit as seen by the sample. The minus sign reflects the fact that when current flows through the complex impedance Z in the positive direction, it is flowing through the sample in the negative direction. Now, $I_{2\omega} = \Delta I_1 + \Delta I_2$ so

$$v_{2\omega}e^{i\phi}(\frac{1}{Z} + \frac{dI}{dV}) = \frac{1}{4}\frac{d^2I}{dV^2}{v_w}^2. \tag{A.11}$$

Since $v_{2\omega}$ is the quantity which will be measured in the system, it is desirable to have it be as large as possible. It is a maximum when $Z = \infty$.

One of the components of Z is the impedance of the sample's own capacitance. In general, tunneling samples have large capacitances, because they are made in such a way that two highly conductive materials are separated by 50 to 100 Å of a dielectric. Large sample capacitances result in small impedances in parallel with the nonlinear resistance of the tunneling device. From Eq. A.1 it is desirable to have the capacitive impedance of the sample much larger than the sample resistance. This is usually not the case. For example, from Fig. 2.6, a 100 Å thick AlAs barrier sample in this study had a resistance of 1000 Ω-cm^2. The capacitance of such a device should have been about 10^6 pf, but the capacitance was probably three times smaller as explained in Chapter 2 ($\sim 3 \times 10^5$ pf). The system was operated at $2\omega = 100$ kHz. The capacitive impedance of this sample would have been around 0.5 Ω-cm^2 which is considerably less than the sample resistance; hence $\frac{1}{Z}$ in Eq. A.11 would be very large and $v_{2\omega}$ very small. Effectively, this means that the second harmonics generated by the sample are shorted out by the capacitance of the sample (as was mentioned above),

and the second harmonic signal appearing across the sample is reduced. The second derivative system which will now be described, was designed to make the complex impedance seen by the sample Z as large as possible at the frequency 2ω while maintaining a constant voltage v_ω at frequency ω across the sample.

The second derivative measurement system (tunneling spectrometer) is diagrammed in Fig. A.2. A more detailed breakdown of some of the components listed in Fig. A.2 is given in Fig. A.3. A discussion of the main components of the system as they relate to the design principles will be presented first. Following this the characteristics of the various components making up the system will be discussed. This tunneling spectrometer is based on the second derivative system developed by Lambe *et al.*[1]

A Tektronixs SG505 sine wave generator was chosen as the modulation voltage source in Fig. A.2, because it had very little harmonic distortion (< 90 db). This oscillator had the added advantage of providing a separate reference channel which was electrically isolated from the output. Low harmonic distortion was required to avoid introducing any background on the harmonics generated by the sample. The sine wave from the oscillator feeds into a set of step-down transformers (TR1:, TR2: and TR3:) and a notch filter. The transformers lower the output impedance of the oscillator (which is 600 Ω) to a value which is less than the sample impedance at the operating frequency (ω). To the sample, the oscillator looks like a low impedance voltage source at frequency (ω). The notch filter serves two purposes. First, it filters out any harmonics that may still exist in the oscillator. This function is not too significant since the sine source is very pure, and nonlinearities in the passive devices from which the filter is composed probably introduce more harmonics than are removed. The main function of the filter is to isolate the sample from the sine wave generator at the harmonic frequency (2ω). When the sample looks back at the input (at frequency 2ω), it sees the high impedance of the notch filter (reduced by a factor of ten by the

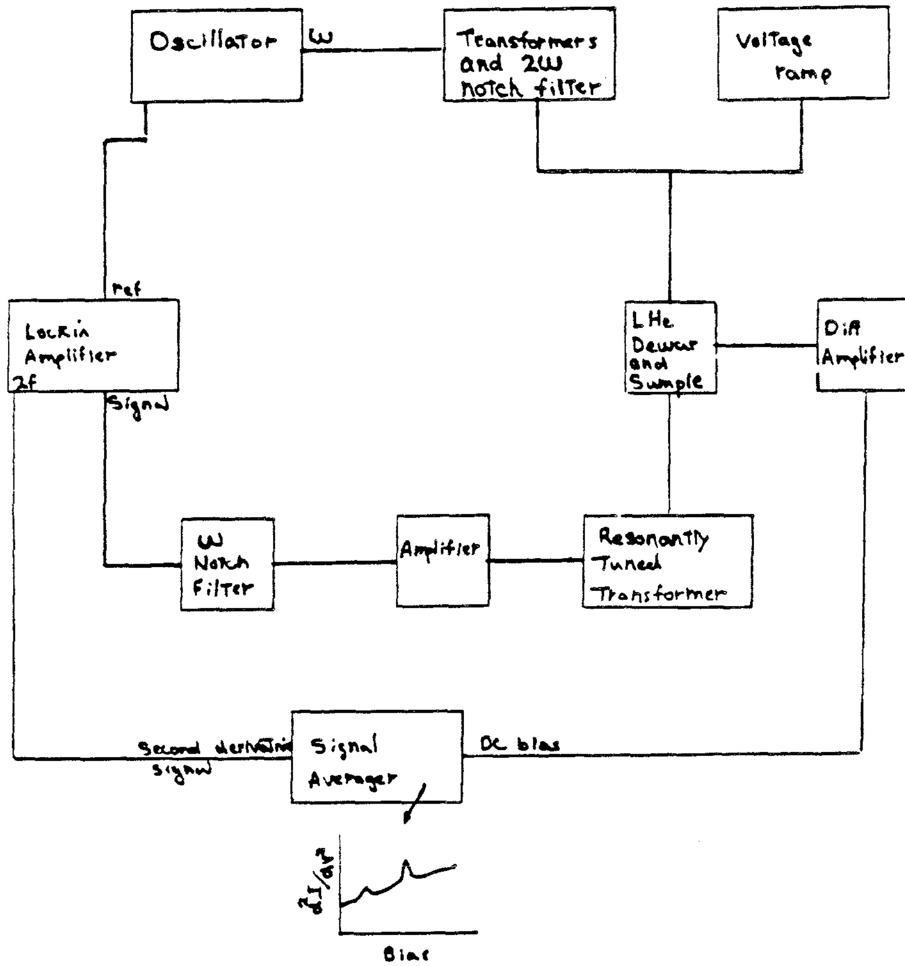

Figure A.2: Schematic diagram of the second harmonic detection system (tunneling spectrometer) used in the measurements of second derivatives of I-V curves.

Figure A.3: A more detailed breakdown of the components in the input, sample, and output sections of Fig. A.2.

second input transformer). Two choices for the second of the input transformers are possible. These two transformers have different turns ratios and thus allow a wider range of sample impedances to be used in the measurement system. The output of the transformers and filter is added to a ramped DC bias. The transformer output passes through a large capacitor (C_3) to avoid running a DC current through the secondary of the last input transformer. A large inductor (L_2) is placed in series with the output of the voltage ramp. This makes the output impedance of the voltage ramp very large at frequency ω but small at the ramp frequency. This signal is applied to the sample.

To remove the problems described above which are created by sample (and stray) capacitances, and at the same time, amplify the signal before it reaches the preamplifier, a resonantly tuned output was used. A variable capacitor (C_4) is placed in series with the primary winding of a 1:1 output transformer (TR4:). Since the output transformer secondary is coupled to a high input impedance amplifier, no current passes through the secondary, and the primary acts like an inductor in the analysis of the impedance, Z, seen by the sample. The capacitor and inductor are tuned so their impedance is inductive and of the same magnitude as that of the stray and sample capacitances. The sample then sees an infinite impedance at 2ω, and $v_{2\omega}$ is a maximum with a magnitude of

$$\frac{1}{4}\frac{dV}{dI}\frac{d^2I}{dV^2}{v_\omega}^2 \qquad (A.12)$$

as can be seen from Eq. A.11. The current passing through the resonant transformer primary is $v_{2\omega}\omega C_s$. The voltage at frequency 2ω presented to the input amplifier by the secondary coil of the output transformer beomes

$$\frac{1}{4}\frac{dV}{dI}\frac{d^2I}{dV^2}{v_\omega}^2\omega^2 C_s L_p. \qquad A.13$$

From Eq. A.13 we see that the spectra given in Chapter 2 were not truly proportional to $\frac{d^2I}{dV^2}$ but rather to $\frac{dV}{dI}\frac{d^2I}{dV^2}$. As long as $\frac{dV}{dI}$ does not change too

much over the range of measurement, this is not a real problem. We also see that the second harmonic signal is proportional to v_ω^2, and that in certain instances it can be helpful to add capacitance in parallel to a low capacitance sample to increase the signal. In general, the output signal (Eq. A.13) is larger than the value of $v_{2\omega}$ appearing across the sample. The transformer is basically stepping up the signal and impedance of the sample to match the operating point at which the preamplifier has the best signal-to-noise ratio. The capacitance in the resonantly coupled transformer was tuned by maximizing the second harmonic signal at the output of the preamplifier.

The preamplifier used was a PAR model 113 preamp. Following the preamplifier, the signal passes through a notch filter to remove the signal at the fundamental frequency and avoid overloading the lockin amplifier. This notch is placed after the preamplifier to avoid adding noise to the signal before it is amplified for the first time. The signal from the notch filter is applied to the input of the lockin amplifier, a reference signal is obtained from the sine wave generator, and the lockin is set to the second harmonic frequency. The system was set up in such a way that a four-point contact could be made to the tunneling structure.[2] In this case, the leads which connect the sample to the resonant transformer are both floating. To measure the bias across the sample and the amplitude of the modulation voltage, a unity gain differential amplifier is connected between these two leads. The measurement of the bias voltage is critical since it gives the energy associated with structure in the second derivative spectrum. The differential amplifier was required to be accurate to within 1 mV for a large range of sample impedances. It was built following the design in Ref. 3, although it should be possible to buy one with the proper characteristics. The signal from the lockin amplifier and from the differential amplifier are recorded by the signal averager, giving $v_{2\omega}$ as a function of the sample bias. The voltage ramp is repetitively scanned and the traces are averaged to improve

the signal-to-noise in the second harmonic measurement even further.

Samples were cooled by immersion in a liquid helium storage dewar. Temperatures between room temperature and 4.2 K were obtained by suspending the sample in the cold gas above the liquid helium. The temperature was measured with a silicon diode. A fundamental frequency of 50 kHz was used. This was high enough to obtain a good noise figure from the preamplifier. Although a noise figure was not measured for the complete system, it was possible to see the change in the Johnson noise at 100 kHz of a 100 Ω resistor which was placed in the sample holder when the resistor was cooled from room temperature to 77 K. Extra capacitance was added in parallel to the resistor.

All of the coils used in the transformers and filters were wound by hand. They were designed with large Q's at 50-100 kHz. This was to done to reduce resistive losses in the coils, since these would contribute both to the noise in the system, and to the output impedance of the sine wave generator at 50 kHz as seen by the sample. The windings in the coils were rather long, and the skin depth of the current passing through a copper wire at a frequency of 50 kHz is around 0.1 mm. These two facts can make the coils have a significant series resistance. This problem was reduced by using Litz wire (90 strands of 44 gauge wire) to wind the coils. The capacitors used in the filters were mica dipped capacitors because they were not as subject to resistive losses in this frequency range as other types of capacitors.

The notch filters were simple LC filters. The inductance in the filter coil was adjusted to tune the notch frequency to the desired value. The resistor between the two capacitors in the filter (Fig. A.3) was varied to adjust the depth of the notch. The capacitors (C) and inductors (L) had to obey the following relation

$$LC = \frac{2}{\omega^2}. \qquad (A.14)$$

Varying L and C within the constraint imposed by this equation adjusted the width of the frequency range in which the filter still had significant resistance

(the Q of the filter). To make this width as small as possible, L was reduced to the smallest value where a good Q could still be obtained for the coil. Capacitor C_1 (Fig. A.3) was installed in the 2ω notch filter to compensate for the fact that the filter still had an observable impedance at 50 kHz. The impedance was inductive and increased the output impedance of the oscillator as seen by the sample. The value of the capacitance was chosen to cancel out the inductive impedance of the coil.[4]

In general this system worked well. The major problem involved the output impedance of the sine source as seen by the sample. As the bias on the tunneling samples was increased, the differential resistance of the sample decreased. At some point this value reached the same approximate value as the output impedance of the sine source, filter, and transformer combination. At this bias the 50 kHz voltage across the sample decreased and the second harmonic signal dropped rapidly. The range of voltages over which the second derivative could be measured was limited by this. The output impedance of the sine source and transformers was not actually the 600 Ω output impedance of the oscillator reduced by the turns ratio squared. Stray inductances in the coils making up the transformers and filter actually made the main contribution to this impedance. The system could be improved by rewinding the coils in the input section to obtain lower stray inductance or by providing a feedback mechanism to increase the amplitude of the oscillator output to maintain a fixed value of the modulation voltage at the sample.[5]

A.5 FREQUENCY DEPENDENT CAPACITANCE MEASUREMENTS

A circuit diagram for the measurement of sample capacitances in the range of 10-200 kHz is presented in Fig. A.4. Resistor R_1 is chosen to have a value

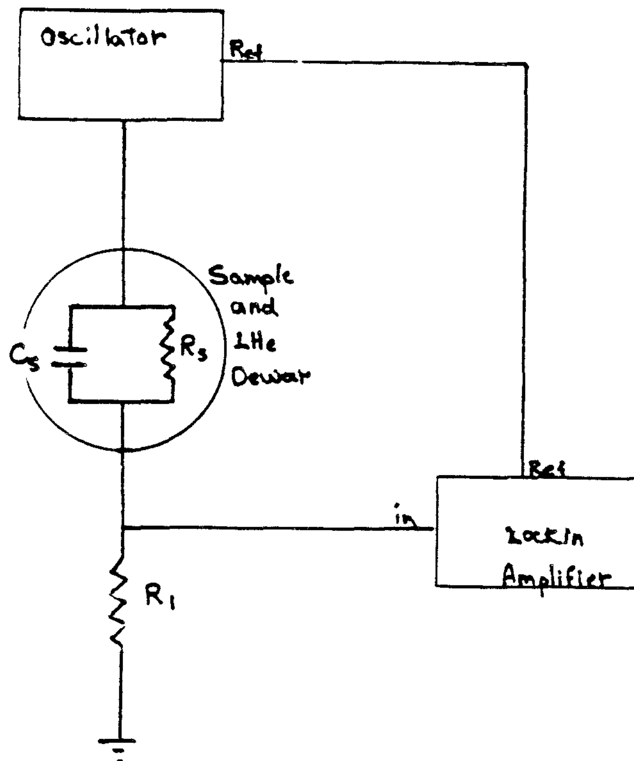

Figure A.4: Circuit diagram of the system used in measuring frequency dependent capacitances for the tunneling samples discussed in Chapter 2.

which is much less than the magnitude of the sample impedance at the measurement frequency. The amplitude of the modulation voltage across R_1 is then given by

$$v_{mod} \approx v_\omega R_1 (i\omega C_s + \frac{1}{R_s}) \qquad (A.15)$$

where v_{mod} is the magnitude of the voltage across the resistor R_1, v_ω is the voltage being output by the oscillator, and C_s and R_s are the sample resistance and capacitance. Given v_ω and R_1, the component of the modulation voltage which is in phase with the reference signal gives the conductance of the sample. The component which is 90 degrees out of phase yields the sample capacitance. The phase of the phase sensitive detector in the lockin can be adjusted to pick off both of these values.

In practice, the dynamic range of the lockin does not allow a particular phase to be measured if the other phase is more than a factor of ten larger than it. It is mainly for this reason that the range of frequencies at which capacitances could be measured with this system was 10-200 kHz, because the lockin itself can operate at frequencies below 10 Hz. At these low frequencies the resistive component of the sample conductance was far larger than the capacitive component. In chapter 2 it was mentioned that cooling the samples increased their resistance and sometimes increased the range of measureable frequencies. Samples were cooled in the same way as they were cooled in the derivative measurements. The system was usually tested by making known measurements on known resistances and capacitances of about the same values as those of the sample being studied. The resistance of R_1 had to be kept small enough that capacitances in the cable from R_1 to the lockin and in the cable from the sample to R_1 had a much larger impedance than R_1, or else these stray capacitances would have changed the phase angles and calibrations of the measurement.

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