Optimization of CCD charge transfer for ground and space-based astronomy

Thesis by

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Abstract

This thesis will be of particular interest to anyone integrating Charge-Coupled Devices (CCDs) into any precision scientific imaging instrument, especially so in space. The first part of the thesis concerns optimization of a CCD camera as a whole. CCDs for the WaSP imager at the Hale telescope are characterized using a minimal amount of data using just a flat-field illumination source. By measuring performance over the entire parameter space of (clock and bias) inputs and analyzing the multidimensional output (linearity, dynamic range, read noise etc), optimal operating conditions can be selected quickly (and possibly automatically). With ever growing sizes of detector arrays such as the recently launched Gaia mission, the upcoming Euclid mission and ground-based cameras such as the LSST (189 CCDs), the task of streamlining detector optimization will be increasingly important. In the second (larger) part, the optimization of Charge Transfer Efficiency (CTE) is explored in particular. In modern CCDs, CTE is caused by lattice defects in the bulk silicon and is significantly worsened by radiation exposure, which is unavoidable in space. As shown in the literature, just a year of exposure to high energy solar proton radiation at low earth orbit can result in CTE reducing to 0.9999 for a signal level of 10,000e^- — problematic for most precision astronomical measurements. Here, CTE degrading traps are fully explored in an undamaged CCD to new levels of accuracy. Several unique species are identified, and their population statistics are analyzed by both wafer and sub-pixel location. Subsequently, easily applied CTE measurement techniques are presented, yielding results with new levels of accuracy, concluding in the presentation of a new trap mitigating readout clocking scheme. This scheme can be readily applied to any CCD employing a

parallel transfer gate without readout speed penalty. It is proposed that the results herein may be used to construct a simple model to predict CTE given a temperature, readout timing and signal level. This model could then be used to automatically optimize CTE for any CCD, given only its trap parameter statistics.

List of Acronyms

ADC – Analog to digital converter

ADU – Analog-digital unit

AR – Anti-reflective

CCD – Charge coupled device

CDS – Correlated double sampling

CEI – Center for electronic imaging

CMR – Common mode rejection

COO – Caltech optical observatories

CTE – Charge transfer efficiency

CTI – Charge transfer inefficiency

DCDS – Digital CDS

DLTS – Deep level transient spectroscopy

DN – Digital number

DSNU – Dark signal non-uniformity

EPER – Extended pixel edge response

ESA – European space agency

FOV – Field of view

FPER – First pixel edge response

FWC – Full well capacity

FWHM – Full width-half maximum

GUI – Graphical user interface

HST – Hubble space telescope

JPL – Jet propulsion laboratory

LED – Light emitting diode

LFC – Large format camera

MDL – Micro-devices laboratory

MOS – Metal oxide semiconductor

MOSFET – MOS field effect transistor

OTG – Output transfer gate

PKA – Primary knock-on atom

PRNU – Pixel response non-uniformity

PSD – Power spectral density

PSF – Point source function

PTC – Photon transfer curve

QE – Quantum efficiency

RC – Resistor-capacitor

RFT – Reset feed-through

RG – Reset gate

SNR – Signal to noise ratio

STA – Semiconductor Technology Associates

SW – Summing well

TCAD – Technology computer aided design

TG – Transfer gate

t-SNE – t-Distributed stochastic neighbor embedding

UV - Ultraviolet

VIB – Vacuum interface board

WDL – Waveform definition language

WF/PC – Wide-field/planetary camera

WFIRST – Wide-field infrared space telescope

ZTF – Zwicky transient facility

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1 Introduction (CCD basics)

In a large number of existing and planned astrophysical science instruments today, the CCD is the sensor of choice (for imaging in the optical to UV regions of the electromagnetic spectrum). The technology has been improving steadily over its 50-year history and as of now CCDs are very well understood and can be manufactured to a high precision, with remarkable charge transfer efficiencies. This progress has been spurred by the ever-burgeoning accuracy and precision imaging requirements for both ground and space-based telescopes around the world. Camera focal plane sizes and data rates have also been increasing in a commensurate fashion such that it will soon be common for instruments to house several dozens of wafer-scale CCDs with multiple output channels each, requiring individual tuning for optimal performance.

This thesis centers on the optimization of a camera with three CCDs, focusing on the primary wafer-scale CCD from e2v Technologies (now known as e2v-Teledyne). Two features have been explored in detail due to the relevance to usage of CCDs in space. The confirmation (on sky) of UV sensitivity enhancement by a backside processing method known as delta-doping, and the optimization of Charge Transfer Efficiency (CTE), which is degraded by the presence of silicon lattice defects. These defects are induced by radiation damage and their effect often limits the useful lifetime of CCDs. CTE degradation receives most attention since this seriously compromises measurement precision which is often the motivation to observe from space. All CCDs are inevitably manufactured with silicon lattice defects and this is the limiting factor for charge transfer performance even prior to

radiation damage. This is significantly worsened with radiation damage which comes in the form of charged particles or electromagnetic waves. The defects formed introduce energy levels in the forbidden silicon bandgap, and these act as transition states that enable the capture and emission of charges between the valence and conduction bands, resulting in image smearing and image degradation. This can in turn result in a loss in accuracy of flux and shape measurements that are frequently required for a high degree of precision in most applications.

The impact of these trapping sites depends on the operating parameters of the CCD and can thus be minimized by choice of charge transfer timing, voltage levels and operating temperature. In the first chapter, the fundamentals of CCD operation are described in order to provide a basis for the discussions of the main body of work. For a comprehensive education on all things CCDs, the reader is highly encouraged to digest the material contained in [19] otherwise known as the "CCD Bible".

1.1 Semiconductors

The CCD is essentially composed of a large sheet of silicon and its operation is governed by basic semiconductor principles. A semiconductor's conductivity is somewhere between that of a metal and an insulator. The bandgap (energy difference between the valence and conduction bands) is on the order of kT, where k is Boltzmann's constant. For insulators, this bandgap is $\gg kT$, so there are no charges promoted to the conduction band, and for conductors there is no bandgap so that it is always filled with charges. The bandgap is a property of the material, and for silicon it is approximately 1.1eV [10].

Electronic states always exist at discrete energy levels for individual atoms. The number of these states increases when atoms interact. Thus, in a solid, a continuum of states arises, forming energy 'bands' and 'gaps'. Conductivity in a material is enabled by partially filled energy bands; completely filled bands contain electrons that cannot move in energy (accelerate) and empty bands have no electrons. In semiconductors, there is a gap between the highest filled band and the lowest empty band. These two bands are termed the valence and conduction bands, respectively, since if electrons made the jump from the lower to the higher band, the material then begins to conduct. Thermal excitation enables electrons to make this jump for semiconductors whereas for insulators the gap is too large.

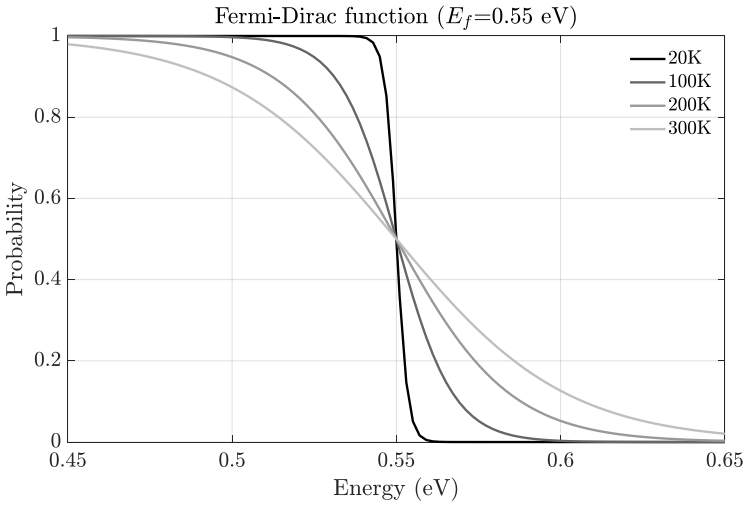


Figure 1.1 Fermi-Dirac function at different temperatures for a Fermi level of 0.55eV.

The valence-conduction bandgap exists in an energy range containing the Fermi level. This is the energy level which has a 0.5 probability of containing charge under thermal equilibrium conditions. It is also the highest occupied energy state at a temperature of 0K. The probability of an energy level being occupied is given by the Fermi-Dirac distribution

function [10] in equation (1.1). This function is plotted in figure 1.1 for different temperatures.

$$f(E) = \left(1 + \exp\left(\frac{E - E_f}{kT}\right)\right)^{-1} \tag{1.1}$$

The Fermi level determines the electrical properties of the semiconductor and this level can be adjusted by adding impurities or "dopants". In the case of silicon, doping with higher group elements (groups V and VI, typically Phosphorus and Arsenic) inserts extra electrons into the conduction band and raises the Fermi level. Silicon doped in this way with extra electrons is termed n-type. On the other hand, if doped with lower group elements (groups II and III, typically Boron or Aluminium), the Fermi level is lowered, and extra holes become present. This type of silicon would be p-type.

1.1.1 P-N Junction

The p and n type silicon have an excess of holes and electrons respectively, though they are both electrically neutral, being balanced by their ionized dopant atoms. These two types of silicon may be joined together to form a p-n junction. The result is that the free carriers (electrons and holes) combine at the junction, rendering the silicon on either side of the junction no longer neutral. An electric field develops across the junction that eventually becomes strong enough to stop carrier diffusion, and thus, electron-hole recombination. At thermal equilibrium, the Fermi levels of the two materials must align and a junction potential step is created. There is a carrier free region in the vicinity of the junction that is carrier depleted, referred to as the depletion region. This is illustrated in figure 1.2. A modern CCD is essentially a large p-n junction and the depletion region is

necessary in order to distinguish photo-generated charge from pre-existing free charge. The depletion region thickness can be altered by adjusting the dopant concentrations, doping elements, and the backside voltage bias.

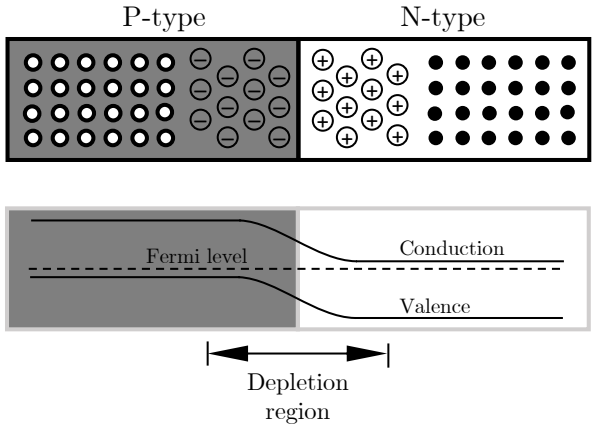


Figure 1.2 P-N junction showing depletion region and band bending caused by the alignment of Fermi levels at equilibrium.

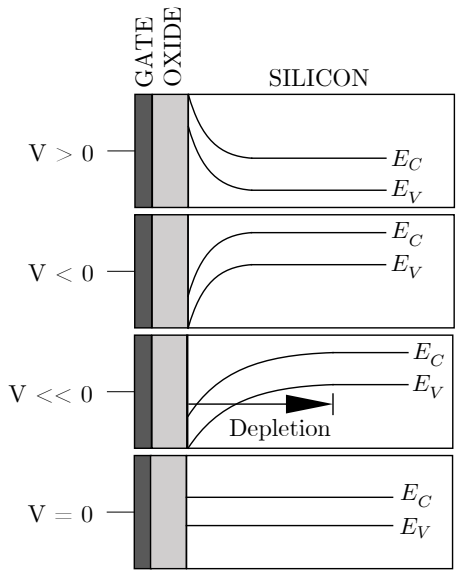
1.1.2 MOS Capacitor

The Metal-Oxide-Semiconductor capacitor arrangement is ubiquitous in electronics applications since it is found in the gate structure for MOSFETs. A schematic is shown in figure 1.3 for an n-type semiconductor along with the potential distribution. The idea is that the properties of the semiconductor can be controlled by biasing the metal gate. By doing so, four distinct cases are possible, described below.

1. Accumulation ($V > 0$). In this case the positive gate bias attracts the majority electron charge carriers to the oxide interface and bends the energy bands positively.
2. Flat band ($V = 0$). With no gate voltage applied the majority carriers remain where they are and no band bending occurs.

3. Depletion ($V < 0$). Here, the bands are bent negatively and carriers and repelled into the material, creating a depletion region near the oxide interface.

4. Inversion ($V < V_T$). Once the gate voltage becomes low enough, minority carriers (holes in this case) arrive at the oxide interface to balance the increasingly negative charge being added to the gate. This pins voltage at the oxide interface, limiting the amount of band bending.



5.

6. **Figure 1.3** MOS capacitor operation modes.

1.2 CCD Operation

Originally conceived in 1969 at Bell Labs by William Boyle and George Smith, the fundamental CCD design was originally intended for use as an electronic recirculating memory device (well before the invention of Random-Access Memory), which emulated a rotating magnetic disk by moving a signal through a circular shift register. The ability to transfer charge from capacitor to capacitor made them suitable for this purpose. However, these devices were also sensitive to light so that data could also be stored by focusing an

image on an array of these capacitor shift registers and then storing the data. The image sensor was thus invented and described in a paper released in 1970 [3]. CCDs are now ubiquitous in imaging applications for many industrial, medical, and scientific purposes because of their near perfect quantum efficiency (QE), very low readout noise and high dynamic range.

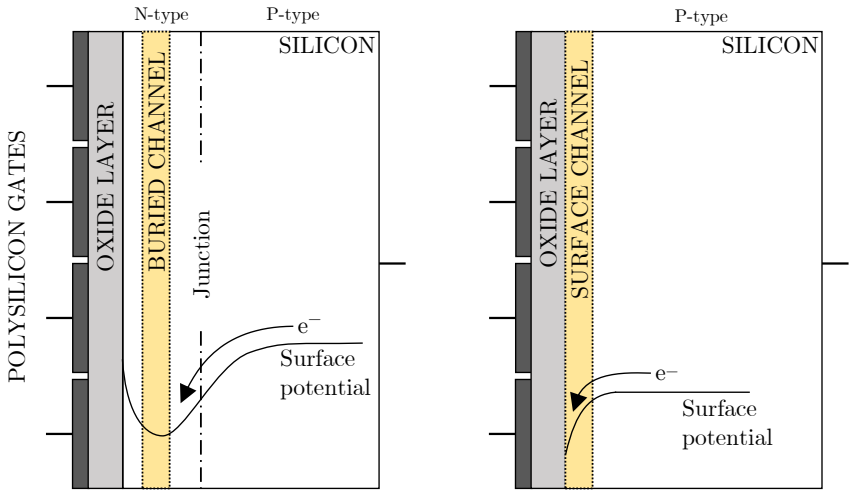


Figure 1.4 Representative four phase CCD pixel cut showing the surface and buried channel variants with surface potential profiles.

At its core, the CCD is an array of MOS capacitors arranged in groups of "pixels" operated in deep-depletion mode (figure 1.4). A pixel typically consists of two to four capacitors or "phases" and the charge is stored in a "buried channel", a short distance under the oxide interface. By the appropriate biasing of the gate electrodes, the charge may be moved around in the array. Modern CCDs consist of tens of megapixels with pixel sizes between $4 - 15$ µm. Previous iterations on the CCD design contained the charge at the surface [3], using a "surface channel" as shown by the location of the potential well in figure 1.4. It soon became clear that this was unsatisfactory since there exist far too many trapping sites

at the oxide interface so that charge transfer is poor. Subsequently the buried channel variant was conceived by inserting a (~3µm thick) layer of silicon that is doped oppositely to the original (creating a junction) [44]. This is pictured in figure 1.4 and the result is that a buried potential well is formed (the channel).Two CCD variants exist — the n-channel (transporting electrons) and p-channel (transporting holes) although they operate in the same fashion. For the body of this work, an n-channel device was used.

All the gate electrodes in the array are connected by row so that a single contact is made that spans the entire row. The pixels are separated into columns by the introduction of "channel stops", regions of heavily doped silicon in the regions between pixels in the row. Additionally, each phase of each pixel is linked by phase number in the column direction (in the row direction for the horizontal registers) so that the gates are synchronized. This minimizes the number of voltage clock drivers needed for operation. This is illustrated in figure 1.5 along with a typical voltage clocking cycle. Each row of the image is transferred into the horizontal shift registers one line at a time. Between line shifts, the horizontal registers are completely read out pixel by pixel at the output node.

How is the performance of a CCD measured? The overall performance is composed of the individual performance measures of charge generation, charge collection, charge transfer, and readout (conversion to voltage). The ways these are measured are briefly discussed in the proceeding sections.

1.2.1 Charge Generation and Collection

The arrival of photons is proceeded by the generation of charge carriers by the photoelectric effect. The photons may either enter through the polysilicon electrodes (front-side illuminated) or through the bulk silicon (backside illuminated). Front-side illuminated devices have the drawback of losing a portion of the photon flux due to the presence of the front-side circuitry. Backside illuminated devices do not have this issue although they must be backside thinned during manufacture to minimize the distance that photo-generated charge carriers must travel to reach the buried channel (described in [14]). They are also generally more expensive. The benefit of having a backside illuminated device is then its **Quantum Efficiency** (QE). This is the percentage of incident photons that are detected. QE depends on the reflectivity, device thickness, depletion width, and device resistivity.

Once generated, charge diffuses through the silicon to where it is then collected in the buried channel. The maximum amount of charge that can be held in the buried channel potential well is defined as the **Full Well Capacity** (FWC). Early CCDs had FWCs of around $6 \times 10^4 e^-$ whereas today for the same pixel sizes of 15µm, FWC can be up to $5 \times 10^5 e^-$ according to [19]. If FWC is exceeded, charge will begin to "bleed" into adjacent pixels (along a column) which is called "blooming". Another parameter of importance in the context of collection is the pixel to pixel non-uniformity. Under perfectly uniform illumination, not all pixels will respond uniformly. This is due to manufacturing process variability that affects the sizes of the pixel boundaries.

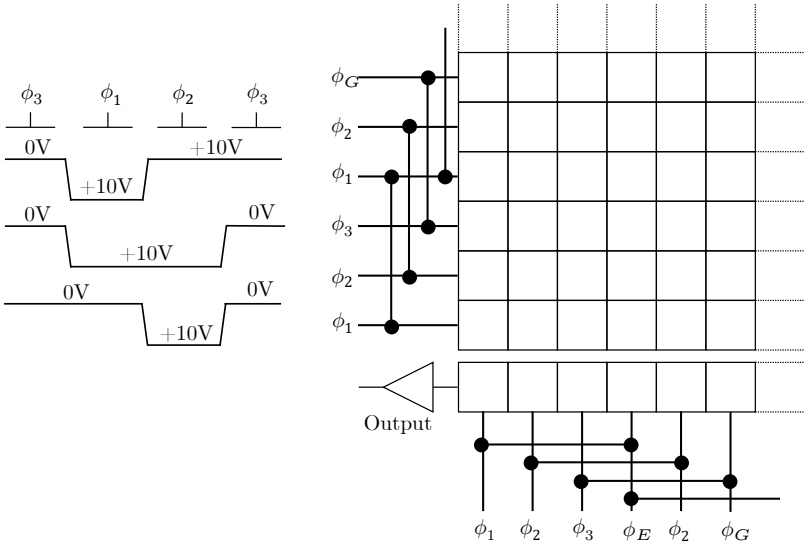


Figure 1.5 CCD array clocking operation and electrode wiring.

1.2.2 Charge Transfer

The end of the collection stage is the end of the CCD "exposure". The readout sequence starts with the transfer of charges to the output electronics. Charge in a given pixel is transferred vertically down the array column into the horizontal shift register and then across to the output node. Each row is transferred simultaneously and each pixel is digitized sequentially. The primary measure of performance in this stage is the **Charge Transfer Efficiency** (CTE). This parameter is a major subject of this work and factors influencing CTE are discussed in sections 3.1 and 4.1. CTE is defined as the fraction of charge conserved after transfer from one pixel to the next. Therefore, the further a pixel in the array is from the output node, (in terms of number of transfers) the more it will be affected by CTE issues.

Often Charge Transfer Inefficiency (CTI) will be quoted for a CCD instead of CTE and these quantities are related by the relation, $\mathrm{CTI} = 1 - \mathrm{CTE}$. Among the several factors

increasing CTI, the presence of lattice defects is the most challenging as they are both naturally forming during the manufacturing process, and unavoidable under radiation exposure. In this thesis we will explore how much of an issue this is for a new backside illuminated CCD and how to get around it — this is important for radiation-damaged CCDs.

1.2.3 Output Circuit

The final stage is part two of the readout process which involves the charge measurement and digitization. The schematic of a single stage voltage buffer output is shown in figure 1.6. This configuration is termed a source-follower or common-drain amplifier (with the addition of a reset switch). The output node on a CCD is a floating capacitor so that the voltage across this capacitor is defined by the charge that is dumped on its plates (from the last horizontal pixel). The charge on the output or sense node is converted to a voltage at the output. In the CCD used for this work, the output consists of a two stage capacitively coupled source-follower design for low noise performance and high responsivity.

The key parameters here are the **Responsivity** and the **Gain**. The responsivity refers to the change in output voltage per unit of charge that is loaded onto the sense node. This is typically on the order of a µV per unit charge. Once the charge is sensed, it is digitized by an Analog to Digital Converter (ADC) module. In this way, each pixel's value is recorded as a Digital Number (DN) and the scaling of DN per unit charge is called the electronic gain of the output signal chain.

It is at the output where various noise sources are introduced, since up until then there is no uncertainty in the amount of charge contained in a charge packet (aside from Poisson noise in the size of the charge packet, and a very small fraction of charge left behind due to trapping).

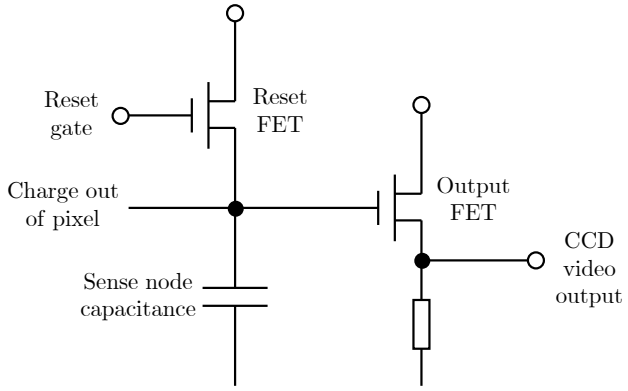


Figure 1.6 Standard CCD on-chip output circuit schematic (source-follower).

1.3 Noise Sources

Dark current

As mentioned earlier, the valence-conduction bandgap is comparable to the molecular scale factor for energy, kT so that charge carriers can be promoted between bands thermally. This leads to the generation of signal without illumination which is indistinguishable from photo-generated charges. The mean dark current can be measured and subtracted but there is no such remedy for its noise which exhibits Poisson noise. This dark current has various sources within the CCD and has been studied in great detail as it is an inherent feature of the silicon. Primarily, dark current emanates from the channel surface oxide interface (due to the large concentration of trapping states) and the depletion region [19]

It is ultimately roughly an exponential function of temperature so devices are typically cooled to minimize the dark current effects to a manageable level. In addition to cooling, gate electrodes may also be operated in inverted mode. During inversion, minority carriers enter from the channel stop region to the surface, recombining with majority carriers that are thermally generated, leaving only bulk material to contribute to the dark current.

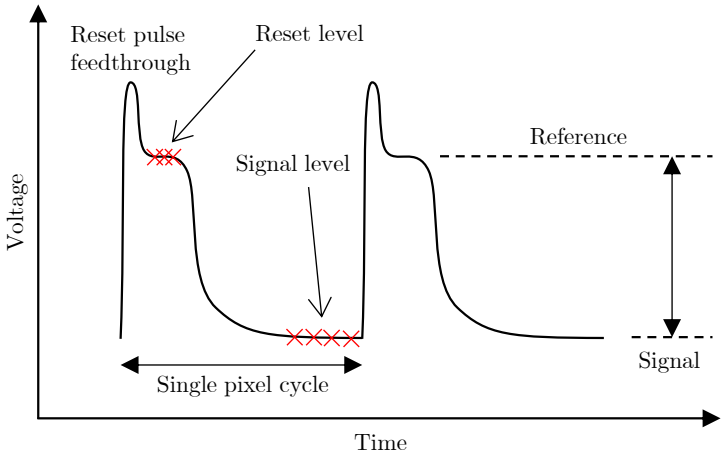


Figure 1.7 Representative CCD output video waveform showing CDS sampling process.

The addition of noise from dark current comes from both the inherently probabilistic nature of the thermal charge generation and also from the Dark Signal Non-Uniformity (DSNU). DSNU refers to the variability of dark signal production rate from pixel to pixel since each pixel will have some structural uniqueness. This also gives rise to pixels producing abnormally high levels of dark current which are termed "hot pixels" – highly undesirable features in a CCD.

Signal noise

The discretization of charge and photons leads to shot noise (first introduced by Walter Shottky in 1918). It is given as $\sigma_{\text{shot}} = \sqrt{S}$ where S is the expected signal level. The SNR

of a given signal level only accounting for shot noise is thus also $\sqrt{S}$. For small signals this is a problem and so exposures are lengthened to boost signal, S and thus, SNR. Another signal noise source is introduced by the same cause of DSNU which is called Pixel Response Non-Uniformity (PRNU). This is the variability of sensitivity to light from pixel to pixel.

kTC noise

The operation of the reset switch after the measurement of each pixel value leads to a thermally generated noise source otherwise known as Reset noise. The voltage across the output node capacitor relative to the reference level gives the value of the pixel. This reference level, however, is a fluctuating quantity due to thermal activity due to the channel resistance of the reset transistor. The noise term in units of e^- is given as $\sqrt{kTC}/q$ where q is the electronic charge (1.6×10^{-19}C) and C is the output node capacitance.

Reset noise is countered by the application of Correlated Double Sampling (CDS). In this method, two output samples every pixel cycle, one once the output has been reset and one after signal has been dumped onto the node. Individually, each measurement is affected by noise but the difference will not be since the measurements are correlated. This difference takes the variation in reset level out of the equation. In figure 1.7 the samples used from a representative output waveform from a CCD for the CDS operation are shown.

Read noise

The process of operating the output amplifier on the CCD also leads to noise which has various sources. The two primary sources are Johnson noise (which has a white noise power spectral density, caused by the thermal agitation of charge carriers in a conducting

medium) and Flicker noise (which has a pink noise PSD, caused by trapping states in the Si-SiO_2 interface). The output amplifier is typically Flicker noise limited at low readout speeds of 100kHz and below, whereas it is Johnson noise limited for higher speeds. Read noise is reduced by frame averaging.

1.4 Photon Transfer Function

The acquisition of the photon transfer function for a CCD camera is one of the most important parts of the characterization process and is discussed at length in [18]. This function describes the relationship between the input (electrons) and output (digital numbers) of the electronic signal chain. From the photon transfer curve (PTC), numerous performance measures may be derived such as read noise, gain constant, FWC, amplifier responsivity and more. Without extolling the merits of the PTC too much, the basics of how to construct one are as follows.

The mean number of electrons registered by the CCD per pixel, n_e after a given exposure time, can be found from the recorded mean number of DN per pixel, n_s, and is related to n_e by,

$$n_e = g \cdot n_s$$

where g represents the gain of the CCD in electrons/ADU. Since n_e obeys Poisson statistics the noise in the number of arriving photons in a pixel, $\sigma_{n_e} = \sqrt{n_e}$. The measured noise, σ_{n_s} is defined as follows:

$$\sigma_{n_s}^2 = \left(\sigma_{n_e}/g\right)^2 + r^2 = (\sqrt{n_e}/g)^2 + r^2 = n_s/g + r^2$$

Here, r represents the read noise (and possibly other sources of noise). So $\sigma^2_{n_s} \propto n_s$, where the constant of proportionality is $1/g$.

The variance of the number of ADU in a pixel, $\sigma^2_{n_s}$ is found from a pair of illuminated flat field images. Many pairs of flat field images are used to calculate the value of g, each pair at a different exposure time (and hence different values of n_s). It is required in each frame to subtract the bias level of the CCD and the dark current accumulated in the same exposure time. This necessitates the acquisition of a 'dark' frame (shutter closed) for each pair of flat field images. Each flat field image is then adjusted by subtracting from it, the dark frame image. Then, the variance calculated from the difference of the two images in a pair is equal to $2\sigma^2_{n_s}$. The mean number of counts in each frame in a pair is averaged to give n_s.

1.5 Radiation Damage

Radiation damage mechanisms depend on the type and energy of particles impinging on the CCD. Damage-causing high energy particles come in three categories: photons, charged particles (electrons and protons), and neutral particles (predominantly neutrons). Of course, electromagnetic radiation (photons) is the signal that is being imaged, but high energy photons may still cause damage. This damage is not direct but rather through the generation of high energy charged particles (Compton scattering or pair production). Neutrons on the other hand, cause damage primarily by the exchange of kinetic energy rather than coulombic interactions. This causes serious lattice displacement defects. Charged particles create similar kinds of damage but through force field interactions

(Rutherford scattering) that can cause defect clusters whose size depends on the incident particles' energy.

It should be noted that the type of damage that this work is concerned with is of the permanent type — transient effects are also possible, such as the creation of ionization tracks, which will affect any number of exposures and then dissipate after some time. Permanent damage can refer primarily to either surface or bulk material damage and figure 1.8 illustrates some of these mechanisms of damage. At the surface, one type of high energy particle damage results in the creation of e-h pairs in the SiO_2 as shown in [15]; in this case, mobile electrons are swept into the buried channel whereas the holes remain in the oxide, generating an electric field which is equivalent to an electrode voltage change. Another type of surface damage results in the increase in the number of band-gap energy states caused by dangling bonds at the Si-SiO_2 interface; this leads to an increase in the amount of dark current produced, although it can be mitigated by inverted mode operation.

The most serious performance degrading radiation damage occurs in the bulk silicon. Elastic and inelastic collisions in the lattice displace silicon atoms, creating vacancy and interstitial defects. These two defect types may also combine to form "Frenkel pairs", which is a third kind of defect. The minimum amount of energy to dislodge an atom from the lattice is 25eV (equivalent to an electron with an energy of 260 KeV) as noted in [22] and excess energy will be transferred to the dislodged atom, commonly termed the "Primary Knock-on Atom" (PKA) in the form of kinetic energy. The PKA goes on to displace more

atoms and the final situation consists of clusters of Frenkel pairs and vacancy defects that migrate in the lattice to form stable defect configurations with impurity/dopant atoms such as carbon, phosphorus, boron or oxygen. These are the defects that diminish CTE and are (indirectly) the subject of Chapters 3 and 4 of this work, where, a more thorough discussion of lattice defects is presented.

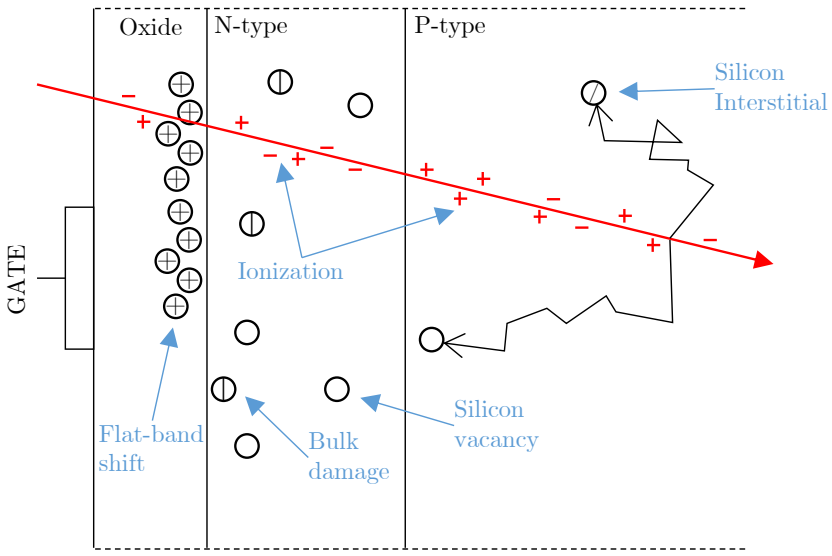


Figure 1.8 Types of radiation damage (adapted from [19]).

2 The WaSP instrument

2.1 Introduction

The **Wa**fer-**S**cale camera for the **P**rime focus of the 200-inch Hale telescope (WaSP) was developed to succeed the Large Format Camera (LFC) at the Palomar observatory on Palomar mountain. The instrument's purposes are

1. To boost the P200 imaging capabilities by providing better QE, noise performance, speed, and image quality, lowering maintenance overhead all with modern components;
2. To overcome limitations and problems that LFC presented such as instrument freezes, image gaps, low speed, outdated software, and low astrometric distortion and;
3. To provide a testbed for the development of detector software and output electronics that will be used for the Zwicky Transient Facility (ZTF) [7].

The instrument focal plane is composed of a single AR-coated 6k x 6k format e2v 231-C6 CCD covering an 18.4 arcminute diameter field of view accompanied by two 2k x 2k format AR-coated and delta-doped STA3600 CCDs (operated in frame transfer mode), at a common pixel pitch of 15µm and plate scale of 0.18"/pixel. The detectors are temperature stabilized at 165K and cooled by liquid nitrogen in a vacuum dewar with a hold-time of 24 hours at room temperature ambient conditions. CCD signals are routed to the outside through pre-amplifiers mounted on a multilayer vacuum interface board sealed between two halves of the dewar. Signals are then digitized on the STA Archon CCD controller

electronics (mounted directly on the camera) and passed onward through fiber optic cabling from the prime focus to the instrument computer on the telescope dome floor. Figure 2.1 displays the general arrangement of components on the instrument.

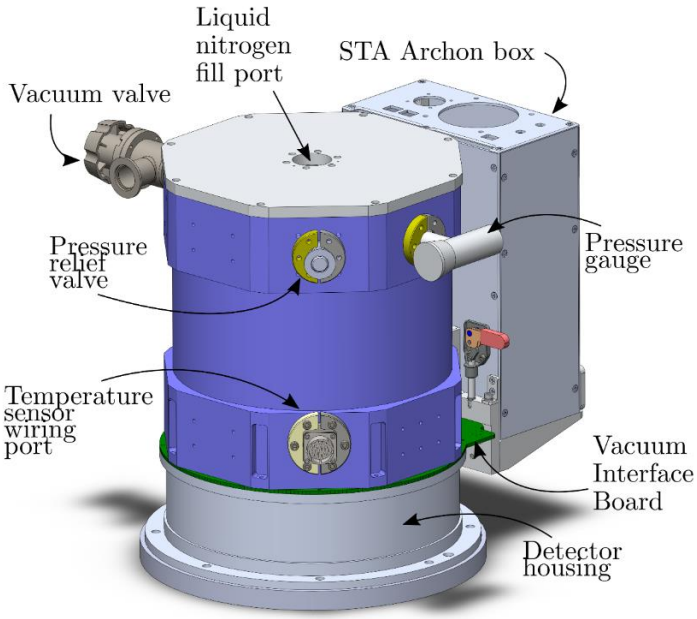


Figure 2.1 WaSP camera dewar with mounted Archon electronics.

This chapter presents a general description of the instrument, some aspects of the instrument design, details and results of the detector characterization and some preliminary results of the camera's first light and commissioning activities. Finally, early test results to demonstrate the u' band sensitivity boost of the delta-doped sensors are presented.

2.2 Design

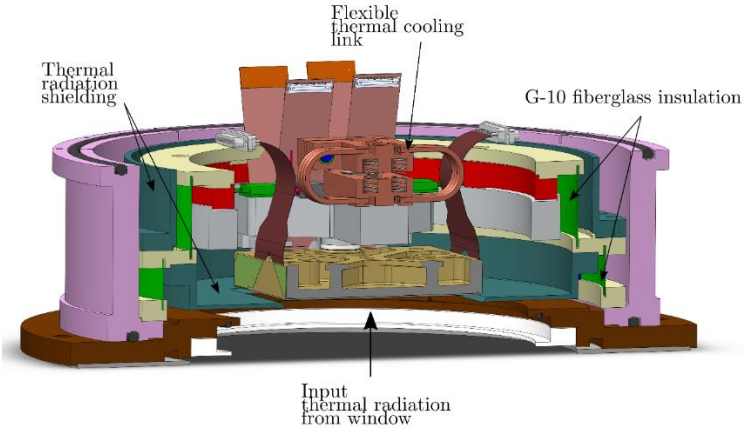


Figure 2.2 (cutaway) Detector housing contents showing main e2v CCD, lateral thermal shielding and braided thermal cold link.

2.2.1 Mechanical and thermal

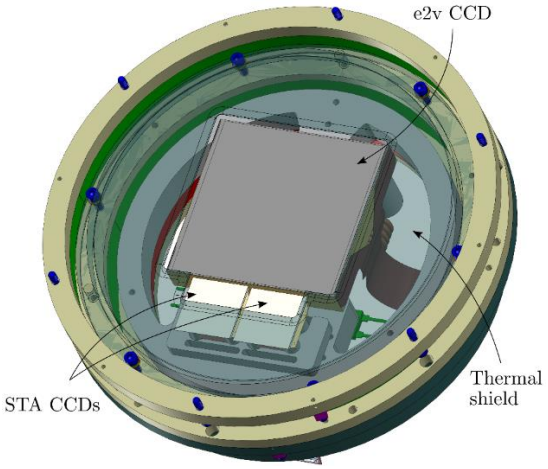


Figure 2.3 Detector housing contents showing CCDs, thermal shield (shown semi-transparent) and fixtures.

The WaSP mechanical design was created at JPL and assembled, tested, characterized, and integrated at Caltech. Figure 2.1 shows the assembled instrument indicating the primary components. In summary, it consists of the detectors, the detector electronics and the cooling system. The electronics consist of the vacuum interface board and the Archon

CCD controller (mounted to the instrument dewar). In figure 2.1, The top half (purple) in this figure contains the liquid nitrogen tank that provides cooling power to the focal plane located in the bottom portion via a flexible thermal link. This thermal link is pictured in the cutaway of figure 2.2.

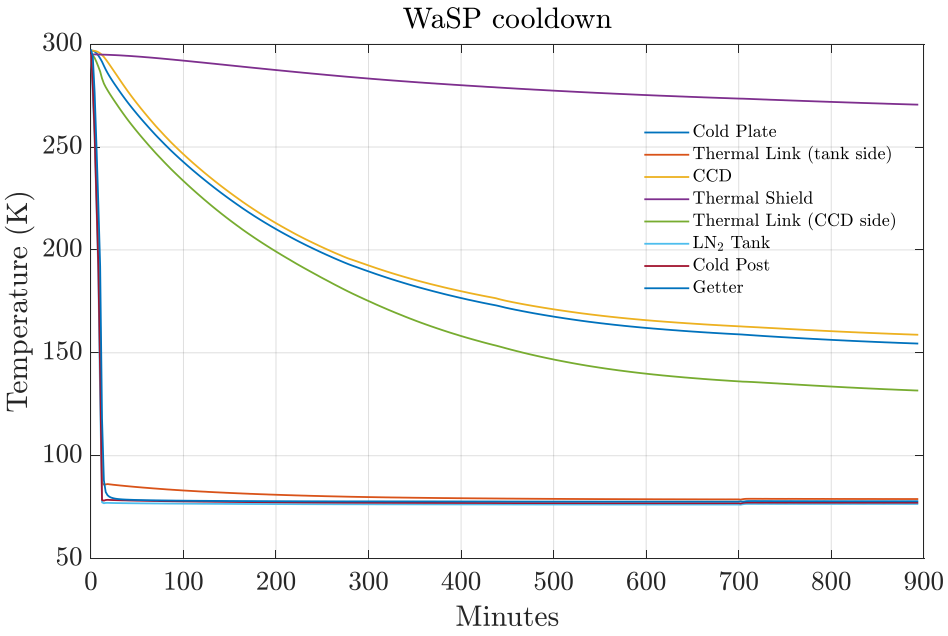


Figure 2.4 Cooling cycle showing expected cooling time and temperature differentials between sensor locations.

Cooling efficiency is managed by minimizing convective, radiative, and conductive heat transfer. The dewar is maintained at a pressure much less than 1mTorr (when cooled) by a large activated charcoal getter that is shown in figure 2.5. A typical pump-down (using the Pfeiffer HLT260 vacuum pump) after exposure of the dewar internals to atmosphere (with 50% humidity) for two days is shown in figure 2.6, indicating a typical wait of 6 – 7 hours until satisfactory pressure is achieved (before cooling). Conductive heat transfer is limited by G10 fiberglass standoffs, isolating the LN2 tank and CCD focal plane fixtures to the dewar walls.

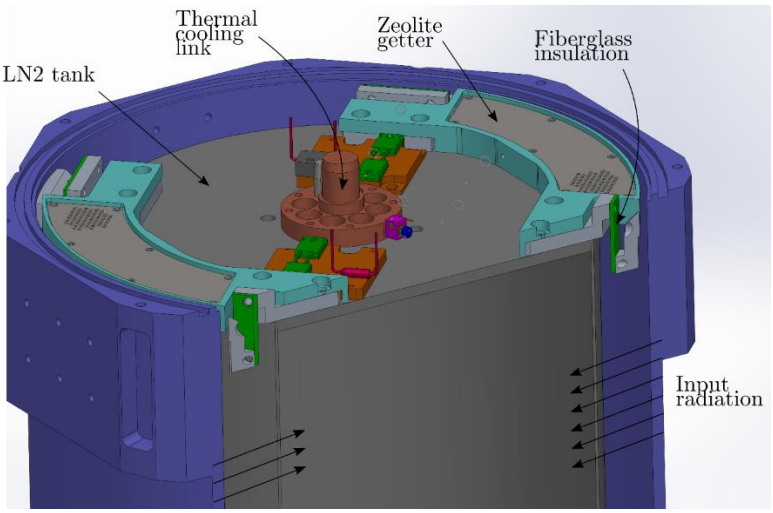


Figure 2.5 .(cutaway) Internals of LN2 dewar section showing cold finger (center) which interfaces with thermal link shown in figure 2.2.

Furthermore, wire thicknesses for temperature sensors and heat resistors were minimized. Wiring, however, presented an optimization problem in that the thinner a wire becomes, the lower the conducted heat transfer – but also the higher the temperature of the wire becomes, resulting in higher a higher radiated power over the length of the wire. Thermal radiation presents the largest source of input thermal power, entering from the dewar window and walls. The design therefore incorporates shielding around the detector assembly as shown in figures 2.2 and 2.5.

An iterative thermal model was constructed, based on the relevant material densities, conductivities, emissivities, heat capacities, and view factors. This allowed the calculation of the detector temperature and its "hold-time" given a full tank of LN_2, given an ambient temperature. According to this model, a thermal load of around 10 W is expected under room temperature conditions, with around 80% that power composed of thermal radiation. Temperature hold-time (until LN_2 depletion) is predicted to be just over 28 hours, and

indeed, the observed hold-time in normal use at the observatory is measured to be 24 hours, on average.

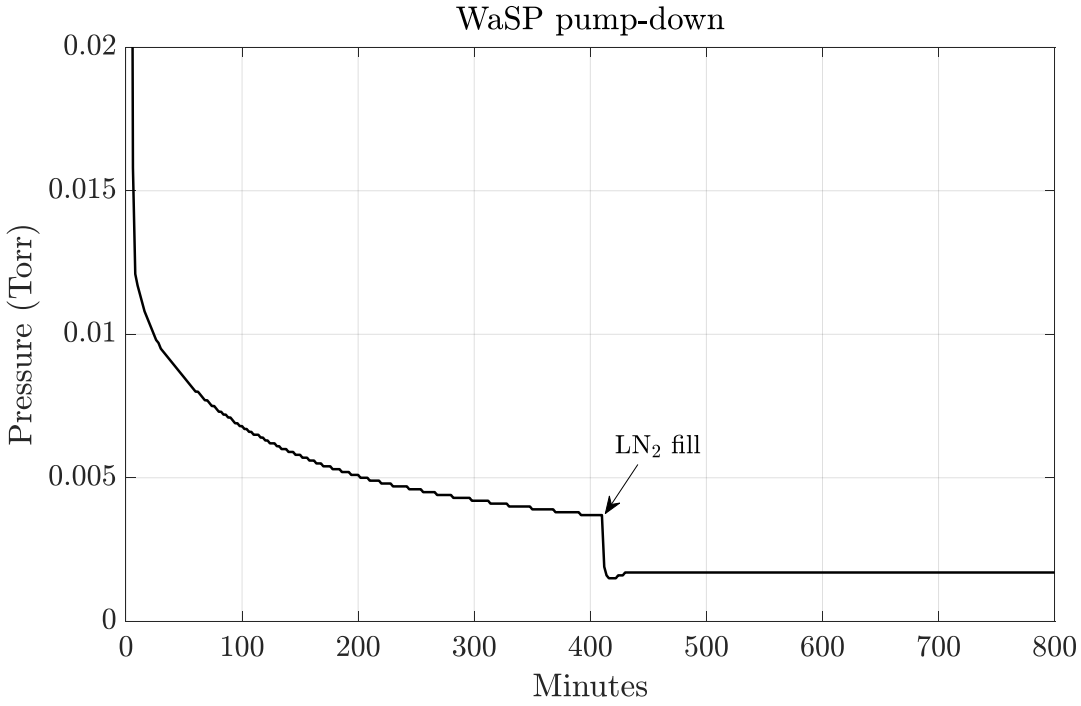


Figure 2.6 Pump-down cycle showing expected time to vacuum (start of cooling).

2.2.2 Signal chain

The CCDs were controlled using a fully customizable Archon controller from STA (who also supplied the guider and focus CCDs) [4]. CCD clocking and voltage biasing was performed using the interchangeable clock and bias card modules in the controller, while CCD output was handled by the available ADC cards. Archon can accommodate up to 4 ADC modules and each module is equipped with 4 fully differential AC-coupled 100 MHz 16 bit channels, which then lead to a digital CDS processor whose input range can be toggled from either 1.33V or 4V (for WaSP, a 4V input range was selected).

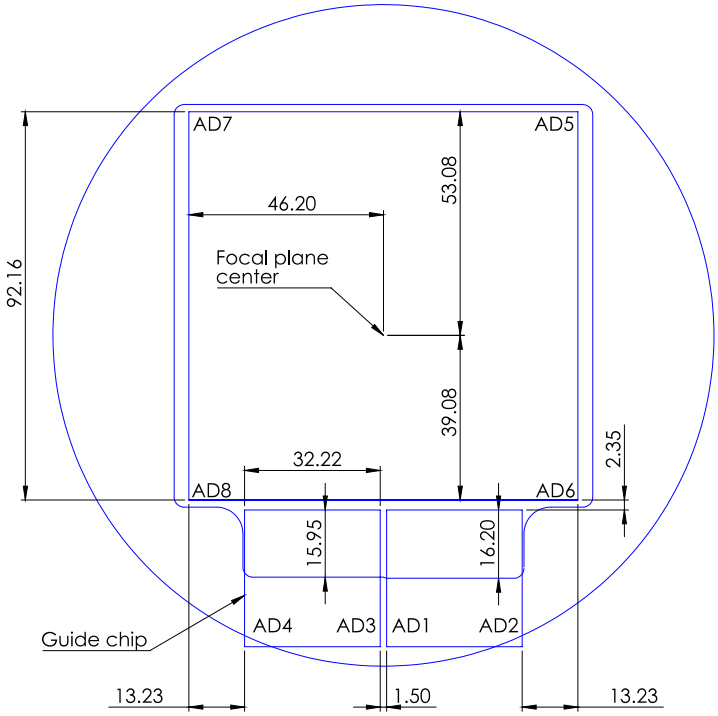


Figure 2.7 Focal plane layout in the context of the Hale telescope prime focus FOV with CCD output channels indicated (all dimensions in mm). All CCDs have a common pixel pitch of 15µm.

From figure 2.7 it is shown that the WaSP detectors have a total of 8 outputs which required 2 ADC cards on the Archon controller. Each e2v chip output is a two-stage source follower design (as described in figure 1.6) with a user defined second stage load resistance. The STA chips have a single stage output with a user defined load resistance. Output amplifier responsivities and loads used are given in table 2.1.

Table 2.1 On-chip amplifier responsivity (vendor specification).

CCD	**Responsivity (µV/e^{-})**	**Load resistance (kΩ)**
e2v	7	5
STA	5	20

The e2v CCD is equipped with replica dummy outputs for each output for common mode rejection (CMR). This is performed by differential pre-amplifiers installed on the vacuum

interface board before reaching the Archon controller. The STA chips are not so equipped, so the 4 redundant outputs (due to their frame transfer mode of operation) on their illuminated side were used for CMR. The simplified pre-amp schematic is shown in figure 2.8 with resistance values in table 2.2. The pre-amp gain is then $(R_1 + R_2 + R_3)/R_2$, thereby allowing an estimate of the electronic gain of the system; these numbers are given in table 2.2. Note that the gains listed for the on-chip amplifiers are estimates only and have not been measured directly. It is based on the assumption that a single stage source-follower is typically expected to have a gain of approximately 0.8.

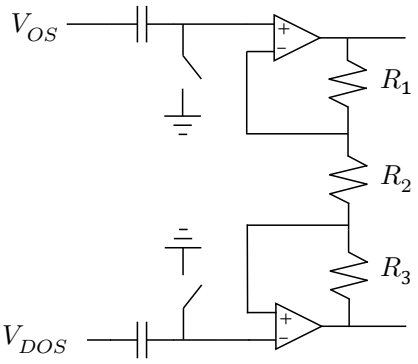


Figure 2.8 Simplified VIB differential pre-amp schematic.

Table 2.2 Electronic gain calculation for output electronics for the WaSP CCDs.

	e2v	**STA**
On-chip amplifier	0.8	0.8
VIB pre-amplifier	$(0.15 + 1 + 0.15)/1 = 1.3$	$(1.5 + 1 + 1.5)/1 = 4$
System (expected)	$\frac{62.5\,\mu V/DN}{1.3 \cdot 0.8 \cdot 7\,\mu V/e^-} = 6\,.\,9$ e$^-$/DN	$\frac{62.5\,\mu V/DN}{4 \cdot 0.8 \cdot 7\,\mu V/e^-} = 2.2$ e$^-$/DN

2.3 Detector performance

Most characterization for the detectors was performed using the same simple experimental setup consisting of a timing controlled LED in a dark box. Various characteristics of the detector were investigated and some of those results are given here.

2.3.1 Characterization

Photon Transfer

The photon-transfer curves (PTC) for all CCDs were generated using the "shutter-less photon transfer" method described in [19]. In this method a mechanical shutter is not used and the detector is continuously exposed during readout. This produces a ramped illumination profile in the vertical direction in the image due to each row having an exposure time proportional to its distance to the horizontal registers. Each row is then collapsed into a figure of mean signal and variance, thereby giving enough data for a PTC within a single frame. One can also do away with the need for frame differencing since the fixed pattern noise contained in a single row is small. PTCs for the main e2v science and STA guider/focus CCDs are presented in figures 2.15 and 2.16.

The non-linearity of the e2v sensor PTCs is of particular curiosity here (figure 2.15). The phenomenon responsible for this is the so called "brighter-fatter" effect described in [1]. The larger a signal packet in a given pixel becomes, the more confined the pixel boundaries become due to electrostatic repulsion. This is illustrated in figure 2.9 and the result is charge sharing, manifesting as sub-poisson signal variance in the PTCs, more pronounced in the range of higher signals. According to [41], the PTC is then more appropriately

modelled by a quadratic function of the form $\sigma^2 = \gamma S - \nu S^2$, where γ defines the gain (DN/e$^-$) and ν is a non-linearity parameter. These fits are included in figure 2.15 along with the linear fits for comparison, and it is seen that there is a non-trivial difference between the gain estimations from each fit. The STA guide/focus CCDs do not seem to exhibit as much PTC non-linearity despite having a similar dynamic range and identical pixel pitch. Additionally, as noted in [1], whether the device is of the high-ρ deep depletion variant has no bearing on the extent of this effect.

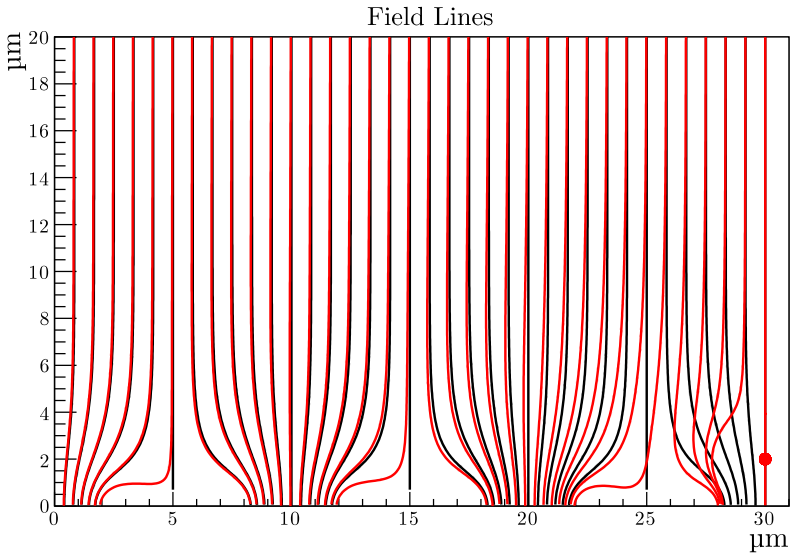


Figure 2.9 Charge collection region (simulation) cross-section of CCD from [1]. Black potential field lines are changed to the red when a 50ke$^-$ charge packet is introduced at the location indicated by the red spot. The right-most pixel then becomes smaller.

Dark current

Dark current from the e2v CCD was measured (using a single dark frame) by binning the image prior to readout by 10 px in both vertical and horizontal directions. Furthermore, a time delay of 2s was introduced between the digitization of each successive line, yielding a ramp in dark signal in the row direction whose slope may be measured with respect to

"exposure" time. The result is shown in figure 2.17 and the mean dark signal is measured as 9.7×10^{-3} DN/s for a 10 by 10 px region of the sensor at a temperature of 165K. Converting this to the appropriate units, we have,

$$\frac{(9.7 \times 10^{-3} \text{ DN/s} \times 5.9 \text{ e}^-/\text{DN})}{100 \text{ px}} \times 1 \text{ hr} = 2.1 \text{ e}^-/\text{px/hr}$$

The quoted dark signal by e2v is 3 e^-/px/hr at 173K so this measurement is in line with expectations.

Linearity

Linearity is a measurement of the electronic gain variation with respect to signal size. Ideally, there is zero variation i.e., perfect linearity. In practice, variation is introduced by the sense node capacitance non-linearity and the dependence of output amplifier gain on signal. By adjusting bias voltages, non-linearity can be minimized. Traditionally, linearity is assessed by analyzing residuals of a linear fit to measured signal-vs-exposure time data. This requires several exposures (frames) for a single linearity measurement. It is then time consuming to optimize linearity for the several different operating conditions (bias levels) of the CCD. A novel quick measurement method is described in [42] where a linearity measurement may be produced with a single pair of flat-field illuminated frames. In this technique, a gain variation is computed for all signals above the flat field illumination level used. The result for the e2v CCD is produced in figure 2.18. The linearity performance is within 1% over the full dynamic range of the sensor and was achieved by tuning the Reset and Output drain levels to 19V and 31V respectively. It should be noted that other

parameters, such as signal sampling window size, also have influence on linearity, and this can be a point of further investigation.

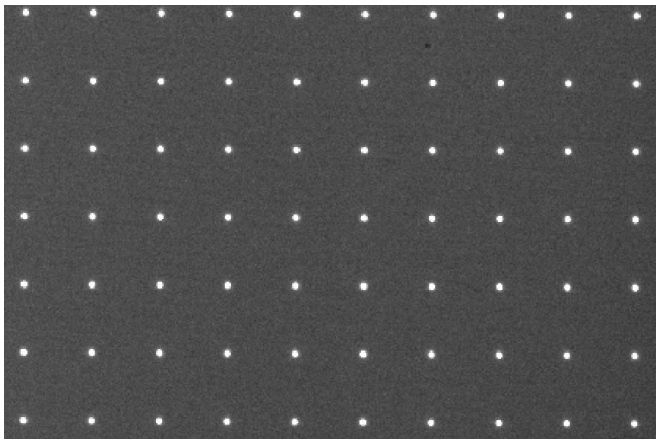


Figure 2.10 Spot grid projected image on the WaSP guider CCD with a substrate bias of 40V.

Read noise

Read noise is simply computed from the dispersion in the signal values of extended pixels (overscan). Digital Correlated Double Sampling (DCDS) [4] applied on Archon is intended to reduce this noise. DCDS performance improves with the number of samples averaged for the reset and signal levels (figure 1.7). The available window in which samples can be accurately taken depends also on the clocking scheme used (since sampling while the video waveform is settling introduces non-linearity due to the non-linear dependence of settling time on signal amplitude). An experiment was thus performed in which the number of samples taken of the reset and signal levels was varied and the results are shown in figure 2.19. Read noise is clearly optimized for an equal number of reset and signal samples and no restriction (up to 20) was seen in the number of samples that can be taken. Nonetheless,

it is shown that if the reset or signal sampling window widths need to be traded (keeping the total pixel time constant) it can be done with an insignificant penalty in read noise.

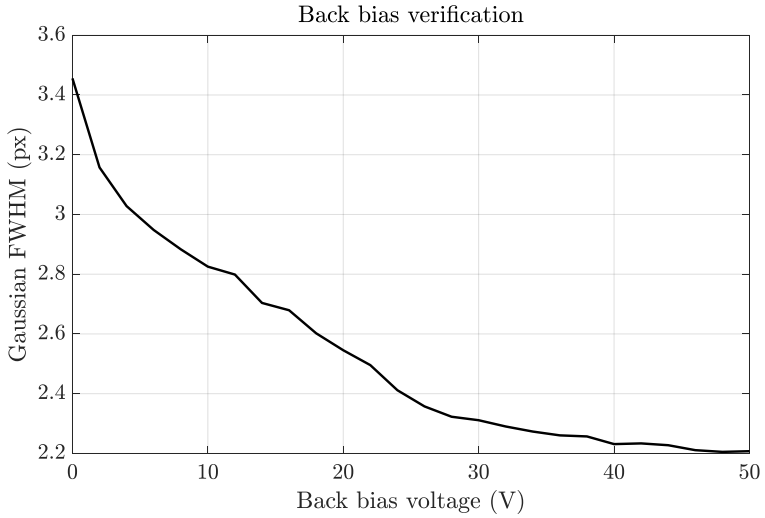


Figure 2.11 Mean PSF FWHM using an isotropic Gaussian fit of all spots in figure 2.10 plotted as a function of back bias voltage.

Back-bias verification

The STA sensor back bias voltage is supplied separately to Archon (whereas that for the e2v sensor is 0V). To determine the appropriate back-bias level to use and to verify its functionality, the camera was installed in the Precision Projector Laboratory [34] and illuminated using the available spot projector delivering a spot optical PSF FWHM well under the 15µm width of the pixel. Images (such as figure 2.10) were taken while the substrate bias was varied from 0V to 50V in increments of 2V. The spots were fitted with an isotropic 2D Gaussian profile and the corresponding FWHM has been plotted in figure 2.11. A back bias of 20V was chosen, considering that a benefit of less than 0.5 px is seen by comparing the FWHM at 20V to that at 50V. It is concerning however that the spot FWHM remains well above 2 px even at a substrate bias of 50V.

2.3.2 Challenges

PTC bump

Under certain conditions related to the parallel gate voltages, PTC anomalies are introduced in the form of variance dips. An example of this is shown in figure 2.14. This effect has been noted in at least one other detector characterization campaign [8]. In that study it was noted that the dips appeared when the phase collection voltage was set to a level between 2V and 4V. The dip is seen as a sudden reduction in noise at a particular signal level before resuming the expected linear trend until full well. This indicates the occurrence of charge mixing once a certain signal threshold is reached, which also ceases beyond another threshold, as noted in research presented in [9]. The dip has been observed to occur in a wide range of signals in the range depending on the chosen collection and barrier phase voltage levels.

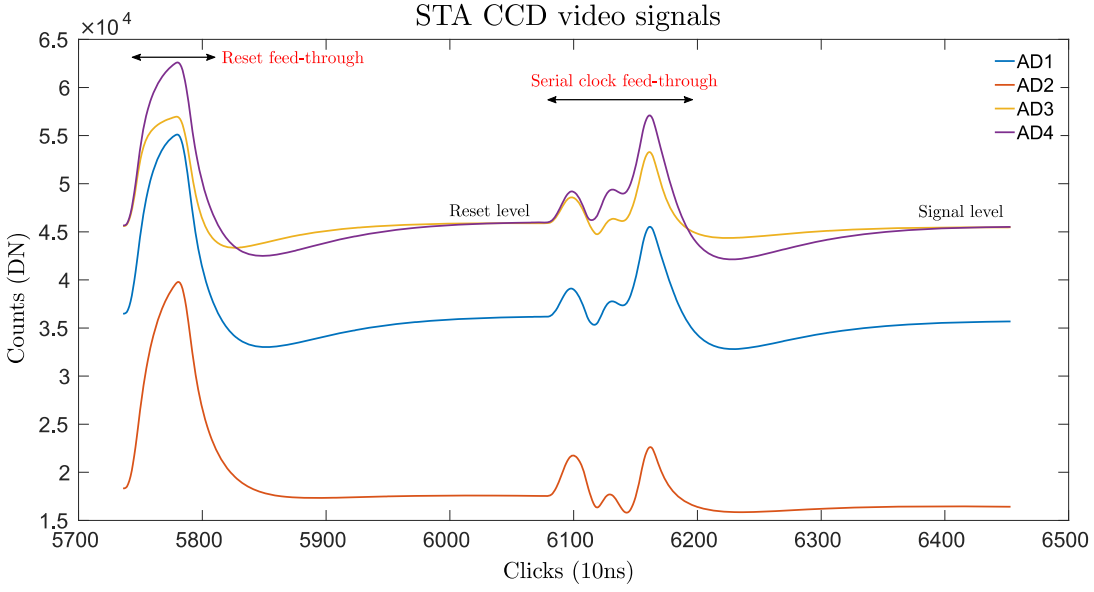


Figure 2.12 Video signals (for one pixel cycle, arbitrarily offset vertically for clarity). from each output on the STA guider and focus CCDs.

Malfunctioning STA CCD output

All attempts to read data from AD2 on the STA CCD designated as the focus chip on WaSP proved unsuccessful. This resulted in AD3 being the sole output for this detector thereby limiting the focus chip frame-rate. Inspecting the video signals from all outputs revealed very slow settling times which has so far eluded explanation (figure 2.12). Furthermore, from AD2 it was seen that the signal level was relatively unchanged with respect to the reset level regardless of the level of illumination.

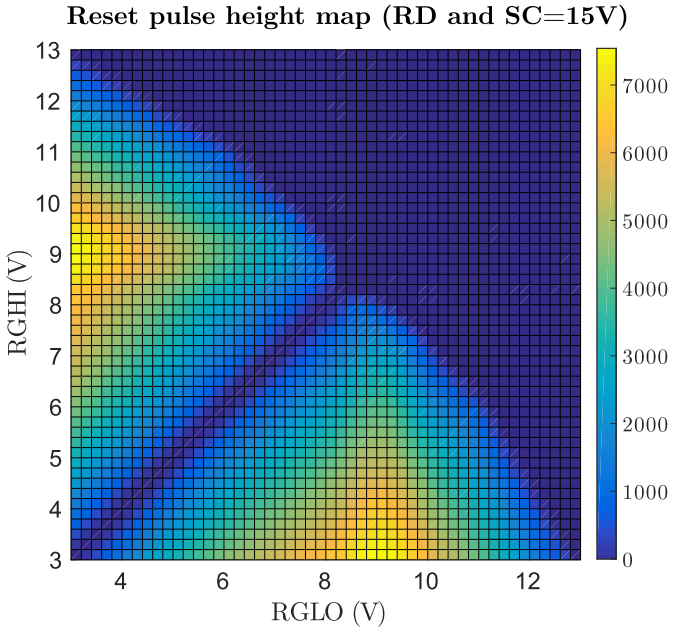


Figure 2.13 Reset feed-through pulse height (DN) as the RG high and low levels are varied. Pulse height increases until threshold voltage, V_T, but then decreases.

It was initially suspected that the reset switch was not functioning properly for the AD2 output and so a test was conducted to rule this out. To observe whether the reset switch was opening and closing correctly (that it is not permanently on or off), the reset feed-through (RFT) pulse was measured for varying reset gate (RG) high and low levels. During reset, RG is pulsed to the high level for a small duration and then returned low, thereby

draining the sense node of charge and allowing a measurement of the (no charge) reference level. The sense node will respond to RG voltage changes (the feed-through) so long as the switch is closed.

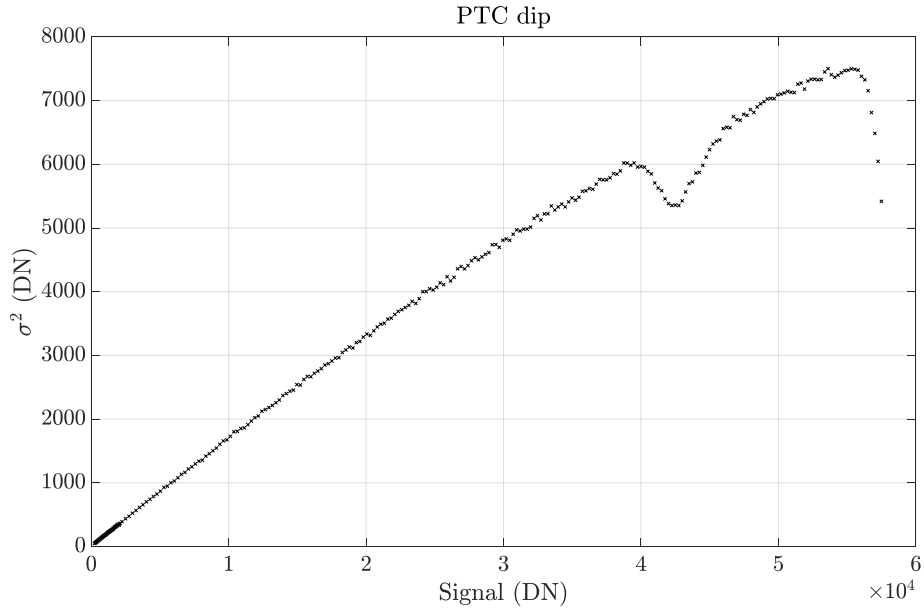


Figure 2.14 e2v Photon transfer curve exhibiting a noise "dip" at 4.3×10^4e-. The dip appears at different signal levels depending on the parallel gate voltages used.

Figure 2.13 shows the result of this test. For a given RG-lo value, the reset pulse height increases with RG-hi up to a maximum and then decreases. This maximum occurs consistently at 9V indicating that this is the threshold voltage, V_T of the reset MOSFET. The behavior that is not expected, however, is the gradual reduction in the RFT pulse height with increasing RG-hi value — it is expected that the RFT remains at a constant height beyond $R_{G,hi} = V_T$. This occurs to the point where if $R_{G,hi}$ is high enough (with $R_{G,lo} < V_T$), no RFT is observed, raising the question of whether the reset switch is always on in this condition.

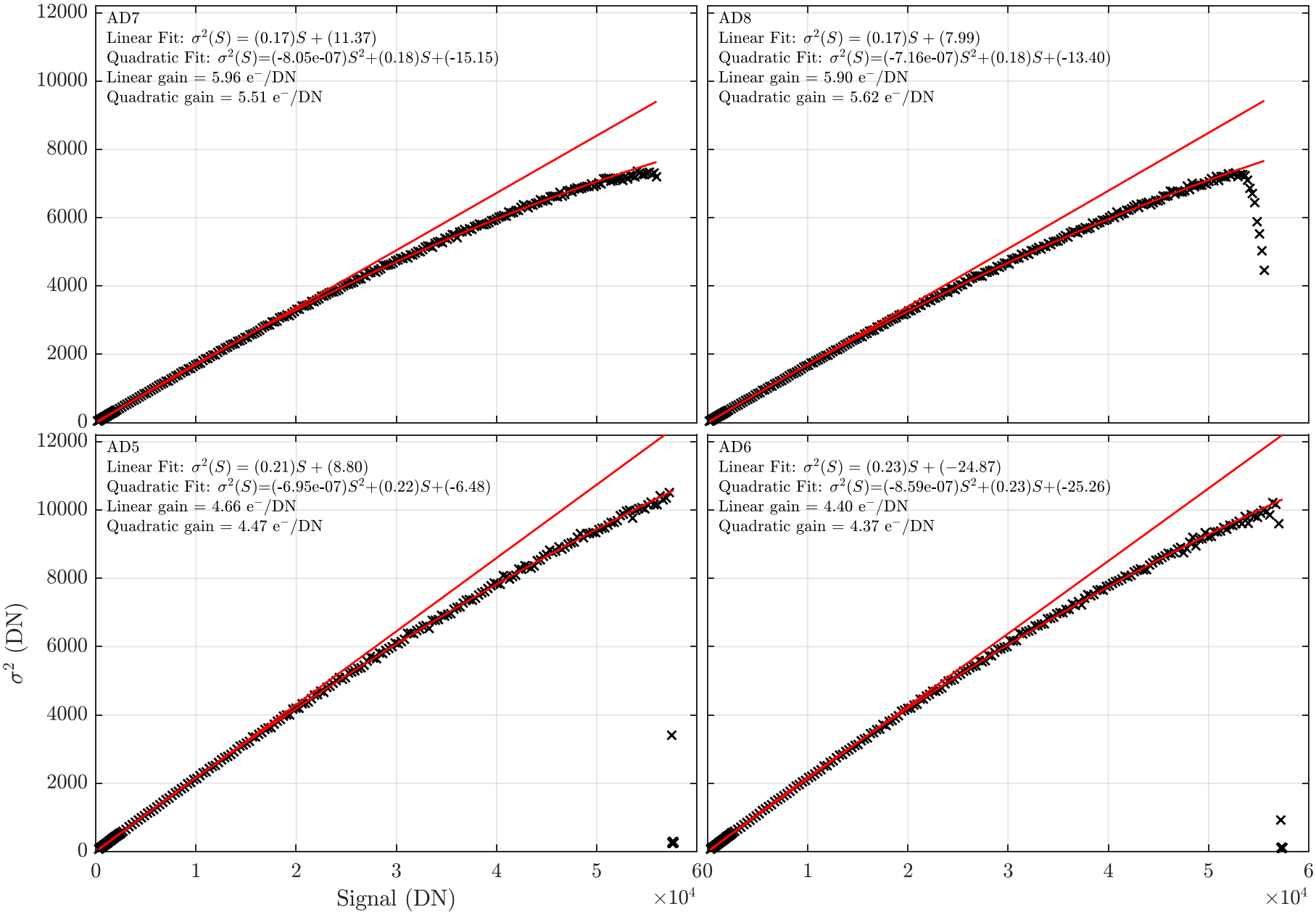


Figure 2.15 Photon transfer curves by output (main e2v CCD).

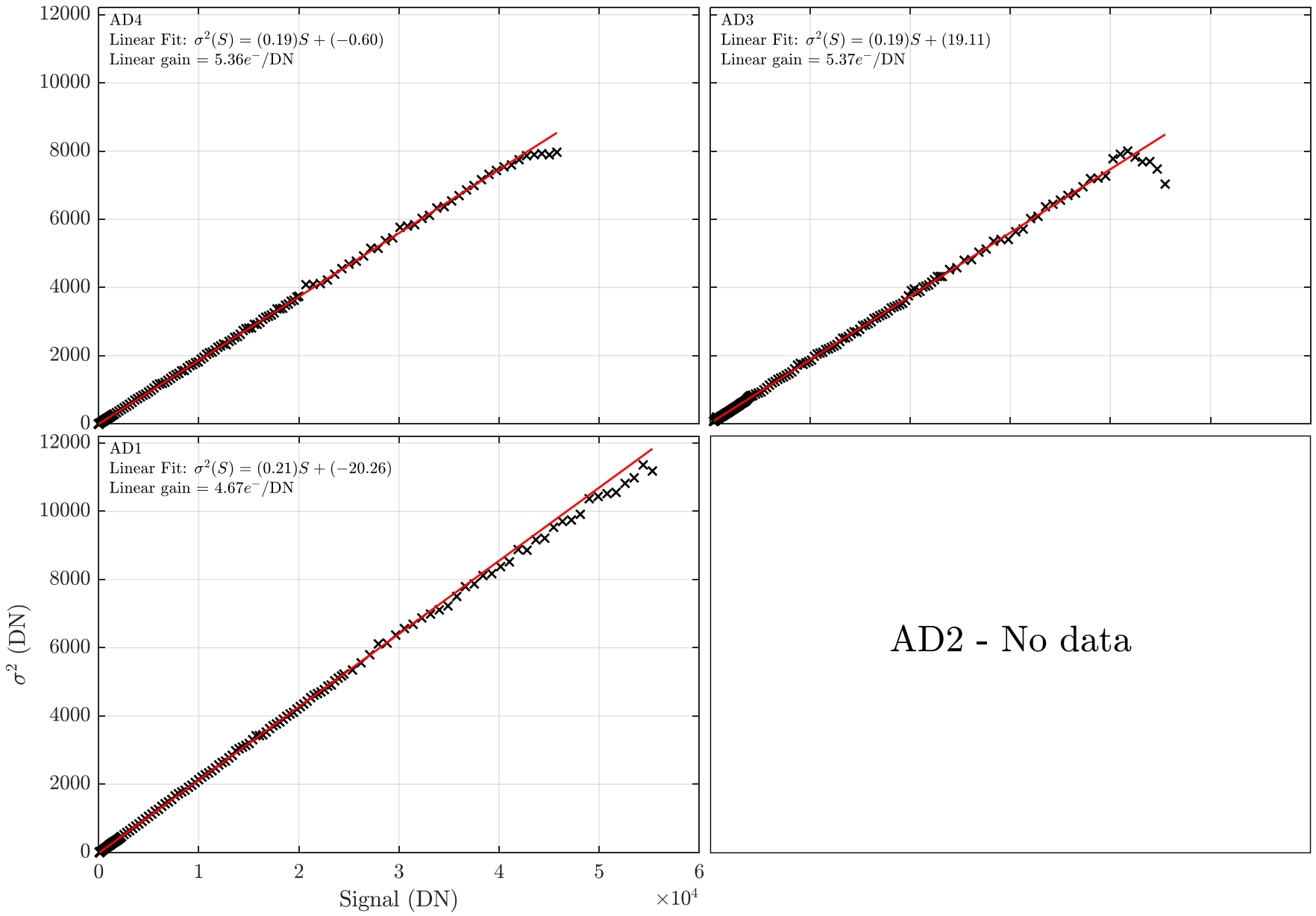


Figure 2.16 Photon transfer curves by output (peripheral STA CCD).

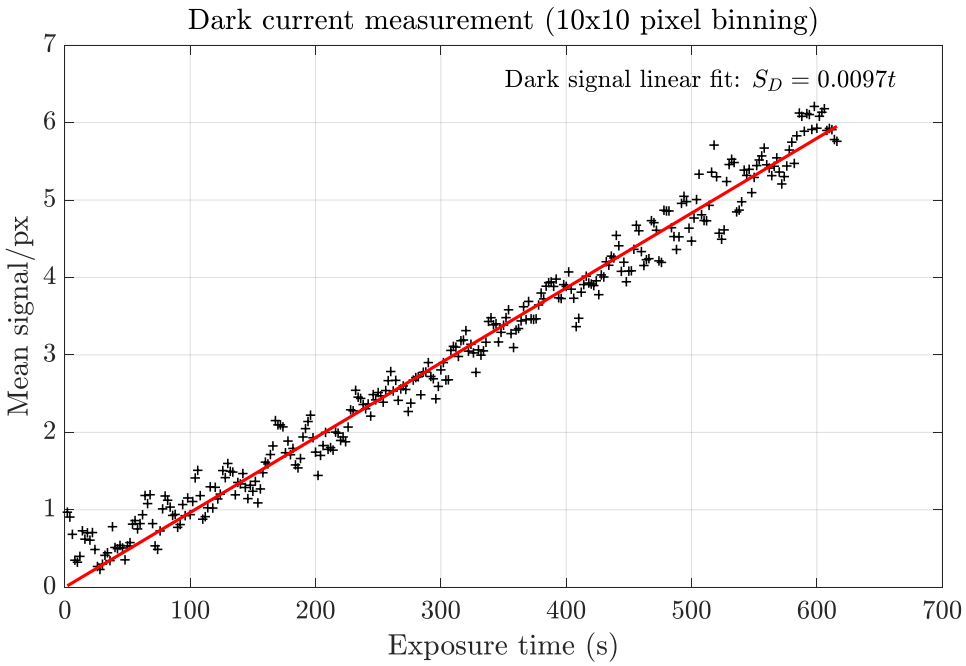


Figure 2.17 Mean dark counts per second per 10 x 10px region of the CCD.

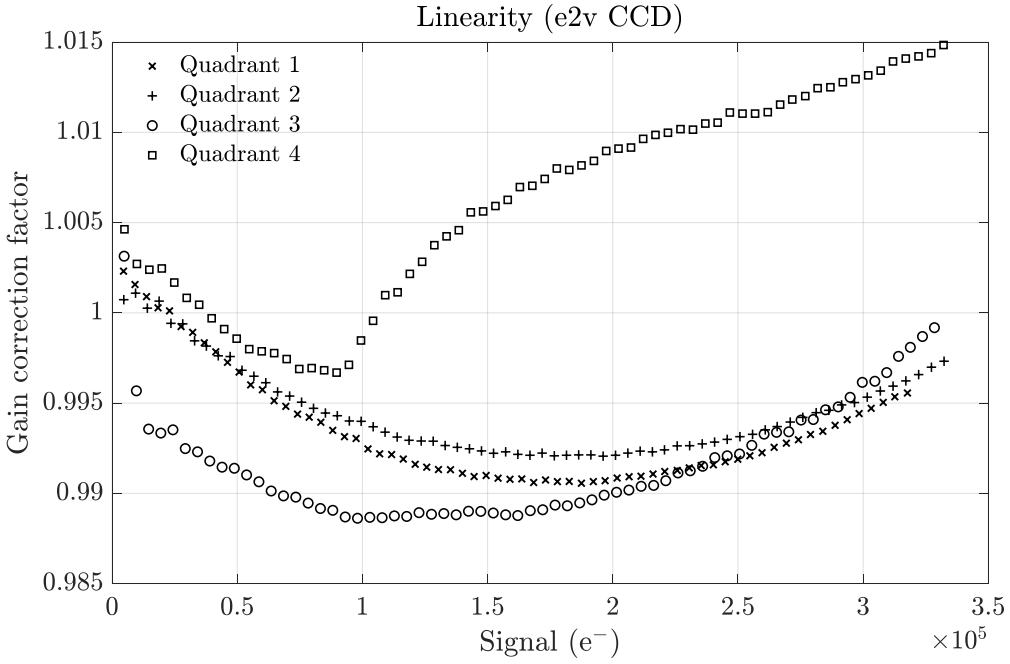


Figure 2.18 Linearity performance of the e2v sensor for all outputs showing non-linearity close to $< 1\%$.

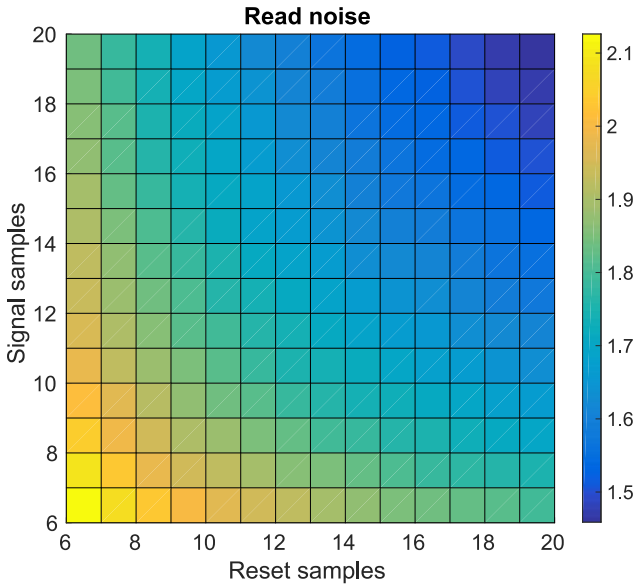


Figure 2.19 e2v CCD read noise (in DN with a conversion gain of 5.8e$^-$/DN) as a function of number of samples taken in the signal and reset windows of the video waveform.

2.4 Integration at Hale telescope

Figure 2.24 shows the detector housing with VIB electronics after detectors have been successfully integrated to the instrument, mid 2016. In late 2016, the WaSP instrument was installed at the 200" Hale telescope at Palomar mountain. Figure 2.20 shows the instrument along with peripheral components consisting of a mechanical shutter, filter wheel, corresponding power supplies and control electronics, Lakeshore temperature controller, and fiber optic interface electronics with associated cabling. The telescope is pictured in figure 2.21, indicating primary mirror and prime focus, while figure 2.22 depicts the instrument installation also showing the Wynne (coma corrector) optics at the bottom of the prime focus cage.

Figure 2.20 WaSP instrument with peripheral components.

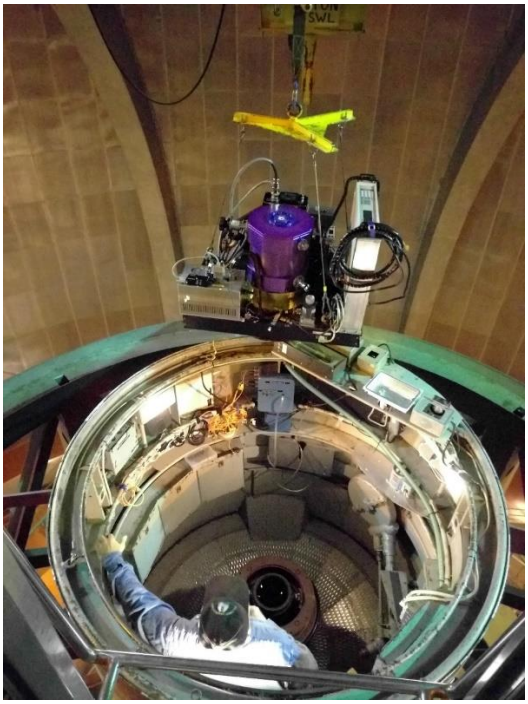


Figure 2.22 WaSP being lowered into the prime focus cage.

Figure 2.21 Hale 200" telescope with primary mirror (bottom) prime focus (top) and equatorial mount (right to left).

Image credit: Justin Belicki

Figure 2.23 Composite r',g',i' tricolor first-light images taken during camera commissioning.

The instrument was intended to allow for auto-guiding and auto-focus using the peripheral STA CCDs. Additionally, capability for sub-array fast readout and dithering modes are also requirements which necessitated careful CCD waveform timing arrangements to facilitate all modes of operation. The Waveform Definition Language [20] was used extensively for this purpose and has enabled several customizable use modes for the camera in conjunction with the included software GUI.

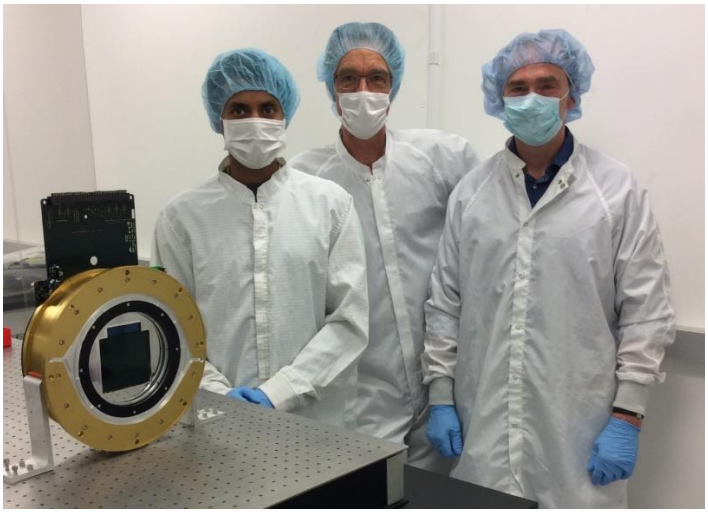


Figure 2.24 Assembled WaSP focal plane pictured with (left to right) the author, Principle Electronics engineer, R. Smith, and COO Mehcanical engineer, Alex Delacroix.

2.5 Delta-doped CCDs

The two STA CCDs used for guiding and focus on the instrument have been "delta-doped" by the Microdevices Laboratory (MDL) group at JPL. Delta-doping was conceived in 1992 [13] to fully maximize CCD QE response across the spectrum (barring limitations from Si reflectivity). On-sky demonstrations of delta-doped CCDs for astronomical science, however have been a long time coming, which is the purpose of incorporating them into

the WaSP imager. Currently the only other project utilizing delta-doped scientific CCDs is the Faint Intergalactic Redshifted Emission Balloon (FIREBALL-2) mission [12]. This experimental 1m telescope-on-a-balloon contains a fiber-fed UV spectrograph and is the second iteration of an experiment to study the intergalactic and circumgalactic medium emission. A successful flight was conducted in September 2018, although results are yet forthcoming. In the meantime, the science benefits offered by exceptional QE performance from delta-doped CCDs are still to be discovered.

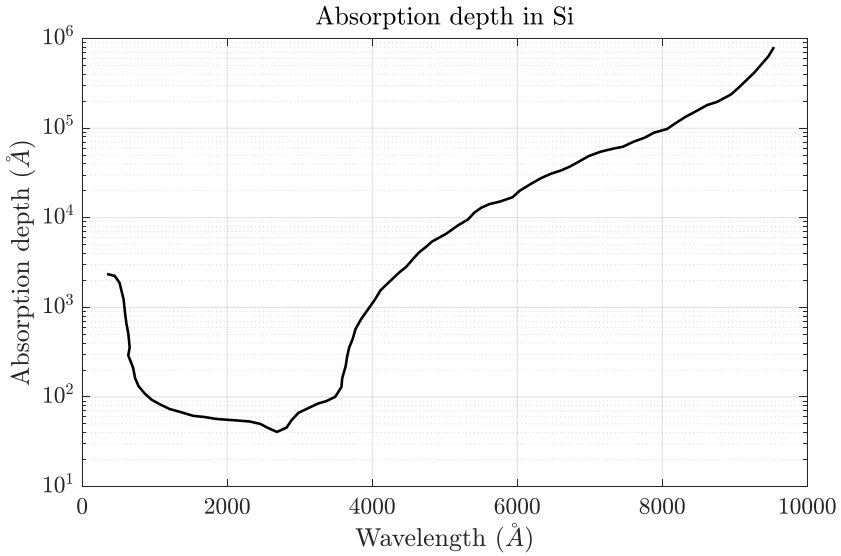


Figure 2.25 Photon absorption depth in Si as a function of wavelength, taken from [19].

2.5.1 Delta-doping principles

The formation of the Si-SiO_2 interface in CCDs results in the presence of fixed positive charges at the interface location. In the case of backside illuminated CCDs (most scientific CCDs nowadays), this presents a QE and QE hysteresis problem since this layer of positive charge creates a backside potential well which serves as a collection area for photo-generated charges that are created either within the potential well or in the nearby field-

free region (which then diffuse toward the back surface). According to figure 2.25, the absorption depth of UV photons (100 nm $< \lambda <$ 300 nm) is between 1 and 10 nm whereas the backside potential well can extend up to 1 µm past the interface. This presents a problem for QE in the UV range since charge is likely to be swept into the backside well and recombine with surface states instead of proceeding further in the silicon to be collected in the signal channel. A significant fraction of charge generated by absorption beyond the backside well is also lost of there is no back-surface processing to negate the charge generated by oxide growth.

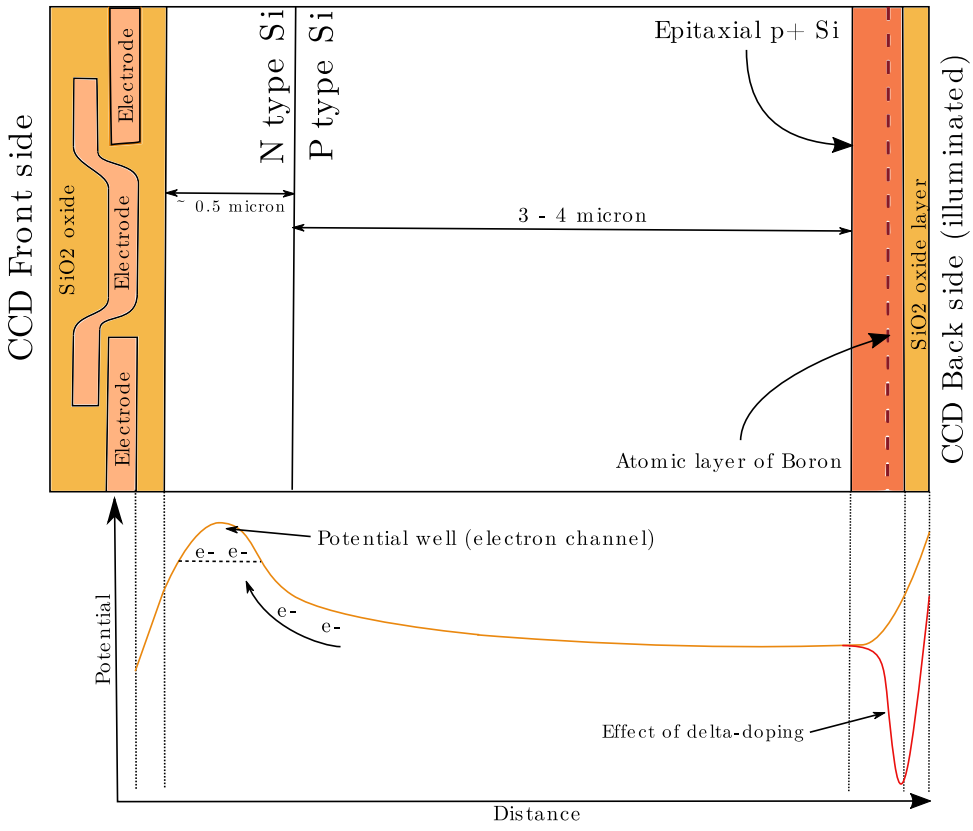


Figure 2.26 Pixel slice through the depth of a CCD showing the effect of δ-doping.

A number of methods have been conceived to deal with this issue as detailed in [19] with varying levels of effectiveness and longevity. Delta-doping stands out among these due to

its permanent nature and its effectiveness (down to shorter wavelengths). The principle, in short, is that by the application (via Molecular Beam Epitaxy) of a monatomic layer of boron (resembling a δ-function) on the backside of the CCD (subsequently protected by a 2.5nm layer of Si), the backside potential well thickness can be confined to be less than 1 nm. This is because this implanted boron layer acts as a sheet of negative charge. The effect of different layer thicknesses is illustrated in figure 2.27, taken from [13]. The narrowest monatomic "δ-doping" layer yields a backside well thickness of around 0.7nm.

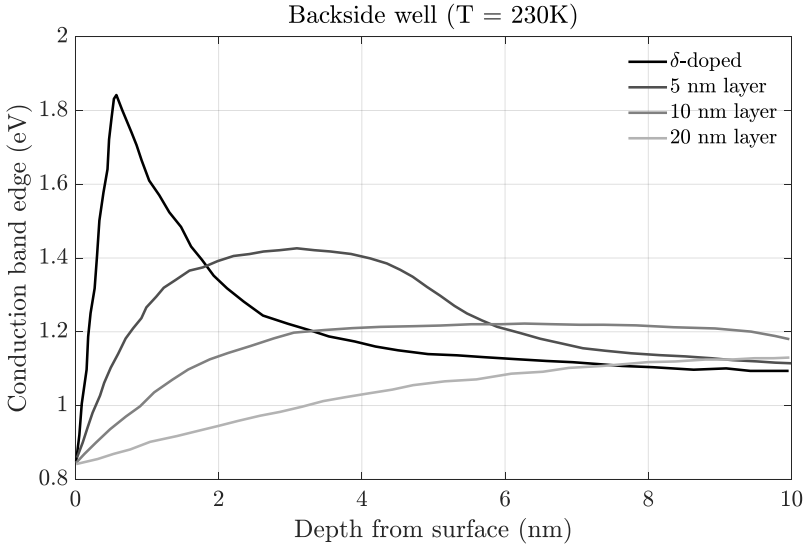


Figure 2.27 Shortening of the backside potential well as the implanted Boron layer becomes thinner, taken from [13].

Figure 2.26 illustrates the location of this layer in the context of the larger path of the photo-generated charge to the signal channel well. By the introduction of the boron layer implant, low absorption depth photons (UV photons in particular) will be detected as opposed to being lost to the larger (deeper) backside well that appears without the implant.

2.5.2 Sensitivity measurements on-sky

To show that the laboratory demonstration of delta-doped sensors can be reproduced on-sky, a test was conducted to measure the sensitivity boost offered when observing blue objects with the 2k×2k delta-doped CCD, normally used as a guider in WaSP. Four standard star targets were selected (listed in table 2.3) of which three were blue and one red; the red target was chosen as a point of comparison.

Table 2.3 B – V magnitude for standard stars tested (3 blue and 1 red).

Target	**B – V magnitude**
Hz44	– 0.406
Feige92	– 0.308
Hz43	– 0.372
Ross627	0.231

Since the sensors are located differently on the focal plane as depicted in figure 2.7, vignetting and spatial variation of filter leak needed to be taken into account. To this end, each target was imaged at various positions from edge to edge of the focal plane — figures 2.30 and 2.31 show the locations each target was imaged at for both the r' and u' filters.

Assuming all vignetting and filter leak effects can be eliminated, we may (roughly) predict the expected sensitivity boost for a standard star in a given filter offered by the delta-doped sensor. This is done by combining the known spectral flux density for each target, F_ν, with the QE curves for each sensor, integrated with the filter band-pass function $f_t(\nu)$ — shown in equation (2.1) (where the g and m subscripts denote properties pertaining to the guider and main chips respectively). The QE curves for each sensor and WaSP filter band-passes are shown in figure 2.28. This yields the expected collected flux 'boost factors' for each target listed in table 2.4 for the two filters u' and r'.

$$\text{Boost factor} = \int_{-\infty}^{\infty} \left(f_t(\nu) \cdot F_\nu \cdot QE_g(\nu) \right) d\nu \Big/ \int_{-\infty}^{\infty} \left(f_t(\nu) \cdot F_\nu \cdot QE_m(\nu) \right) d\nu \qquad (2.1)$$

Before going on sky, flat field and bias calibration frames were taken, which may also give an indication of the differences in sensitivity between the two sensors. Figure 2.34 depicts a u' band flat-field signal (for a 60s exposure time to the high lamps in the dome) color map of a portion of the focal plane on a shared color scale. Figure 2.33 shows the same in r' band (for a 30s exposure time). The sensitivity increase is evident in the u' flats. Figures 2.32 and 2.35 further show corresponding sample column profiles across both sensors. In r' band the guider and main chip are matched in QE so the flat field continues the roll-off profile in the guide chip. In u' band, however, there is a jump in measured signal.

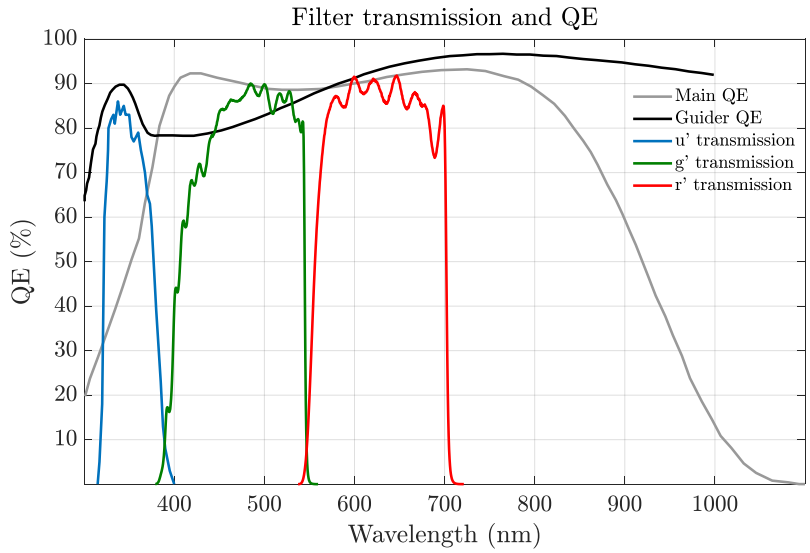


Figure 2.28 Filter transmission (u' g' and r' filters) and QE curves from [17].

Figures 2.36 to 2.39 show on-sky aperture photometry measurements for the aforementioned targets in r' and u' band filters as a function of radial distance from the center of the focal plane. Immediately evident is the increase in flux as radial distance is

increased – this is most likely due to filter leak which is more pronounced closer to the edges of the filter. Filter leak is apparent for both filters used. This data can be used to estimate the filter leak profile as a function of radial distance, since as per figure 2.29 taken from [31] vignetting of the prime focus image does not come into play within the radial distances considered here.

Table 2.4 Expected **u'** band sensitivity boost from the delta-doped sensor.

Target	**Expected boost**
Hz44	1.75
Feige92	1.69
Hz43	1.76
Ross627	1.68

The distinction between fluxes measured on the guider and main chip are indicated in the plots. Aperture photometry was done according to the standard method described in [16] with a generous 15 pixel FWHM central aperture. It was seen that PSFs on the guider chip were generally taller, indicating less charge diffusion than on the main science chip. Frames were not flat-fielded and all pixel values were converted to absolute units of e^-. Aperture photometry results indicate that targets consistently contained less flux on the guider than on the main chip. This is at odds with the numbers presented in table 2.4 and data shown in figures 2.34 and 2.33. The effect is unlikely a result of filter leak since it is observed in both u' and r' band since such a leak should work in favor of locations at higher radial distances. Since this is a step change difference in flux on the focal plane the source of this difference must be contained in the detector system itself. In light of this, the boost indicated in figure 2.33 from flat-field illumination would be the more definitive

result. Further investigation is required to determine the actual band-pass of the filters used for observations and whether any other losses are at play.

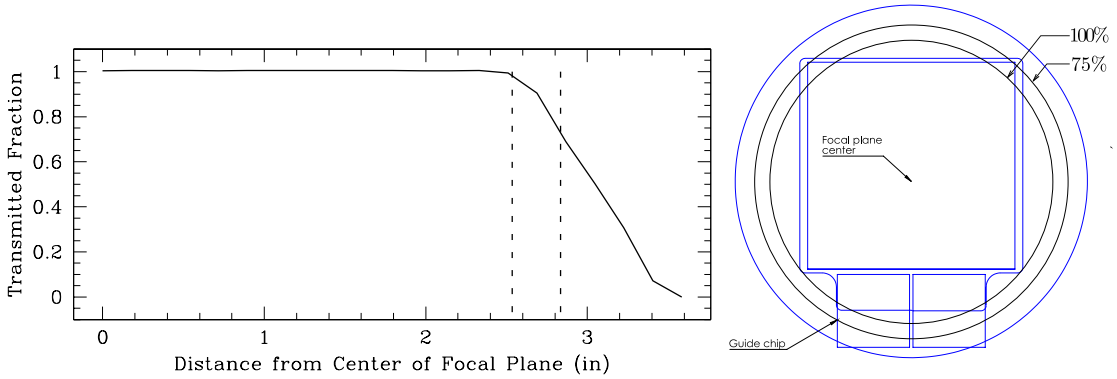


Figure 2.29 P200 Prime focus FOV vignetting profile (from [31]) with 100% and 75% line markers indicated in both left and right figures.

2.6 Summary

WaSP is currently in regular use at the Hale telescope, currently integrated with the existing shutter and filter wheel assembly (plans are in place to refresh these components in the next months at the time of writing this document). It has served its function in being the trailblazer in operating with Archon electronics for the ZTF project. The flexibility offered by the introduction of WDL and the capability of Archon to make the waveform definitions for each CCD parameterized and scriptable are great benefits when it comes to efficiency in detector characterization. Vast amounts CCD performance data can be quickly generated for a variety of input parameters, thereby allowing for rapid optimization of multiple performance metrics with respect to the multitude of input controls. This becomes especially useful when dealing with several CCDs in the same camera, as has been shown during the characterization of the WaSP CCDs.

The guider and focus CCDs that were delta-doped by JPL and delivered to Caltech exhibited some problems in such as malfunctioning outputs and low readout speed limitations which were attributable to the use of an untested fully depleted thick CCD. Nonetheless they have been made operational and have been tested on-sky to compare blue photometry SNR to that of the main e2v CCD. While u'-band flat field images show an boost in sensitivity of ~20% in this band-pass, it is below the expected performance, given the measured QE performance. Imaging blue standard stars in u' band yielded lower flux measurements by the delta-doped CCD compared to the e2v — further measurements are required to eliminate unknown systematic effects. A possible explanation is red-leak affecting the u'band filter.

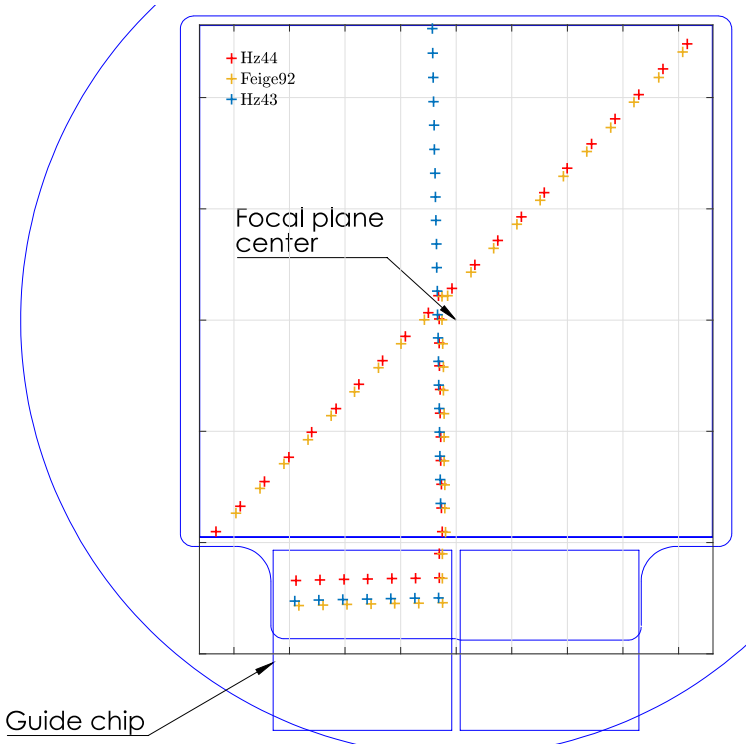


Figure 2.30 Target imaging locations on the focal plane in **r'** filter.

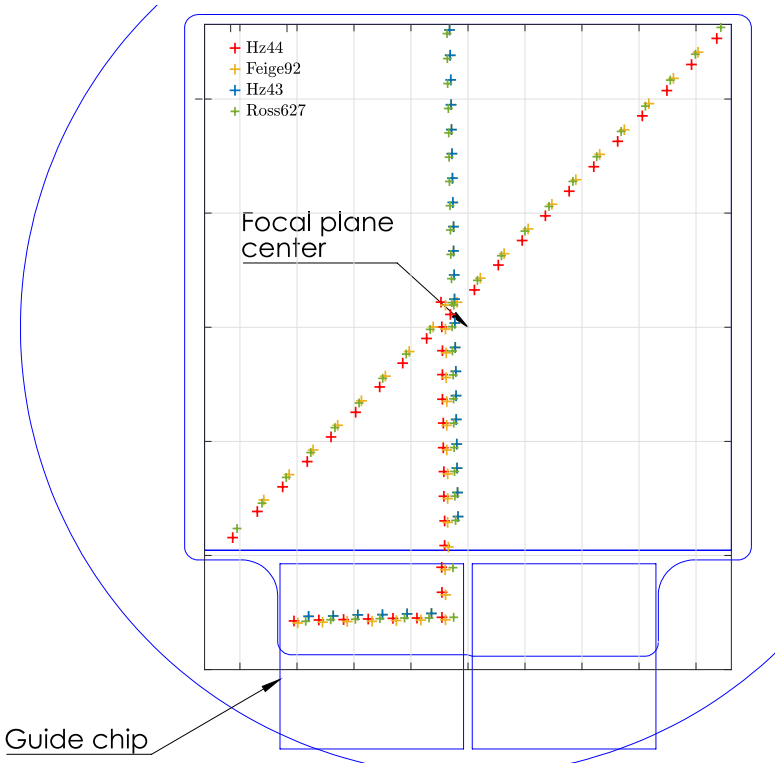


Figure 2.31 Target imaging locations on the focal plane in **u'** filter.

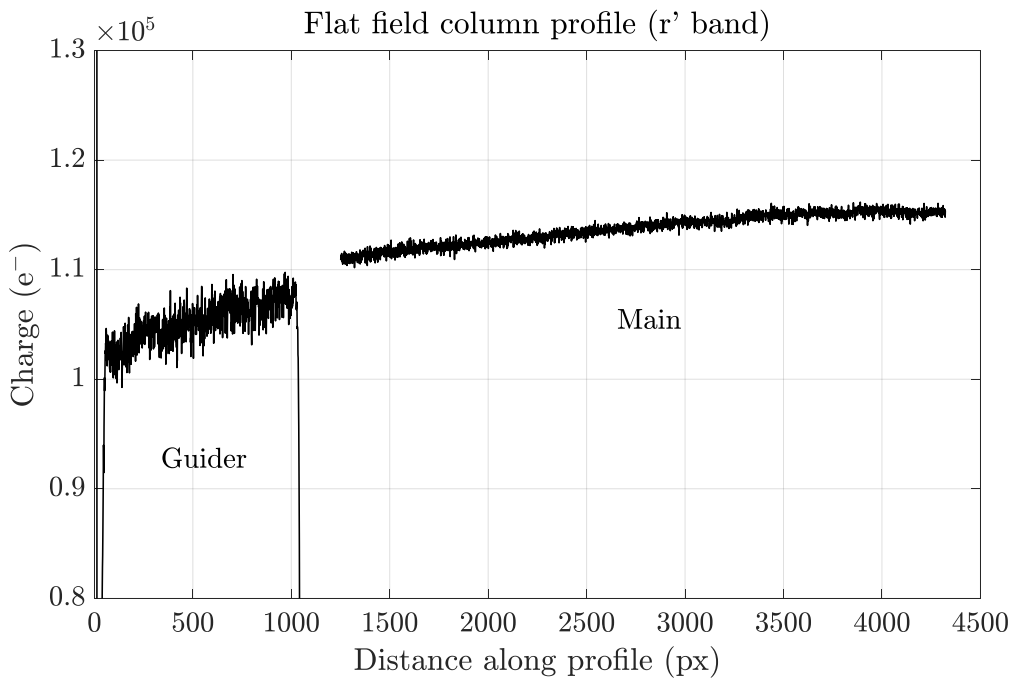


Figure 2.32 Column slice of **r'** band flat across both guider and a portion of the main chip.

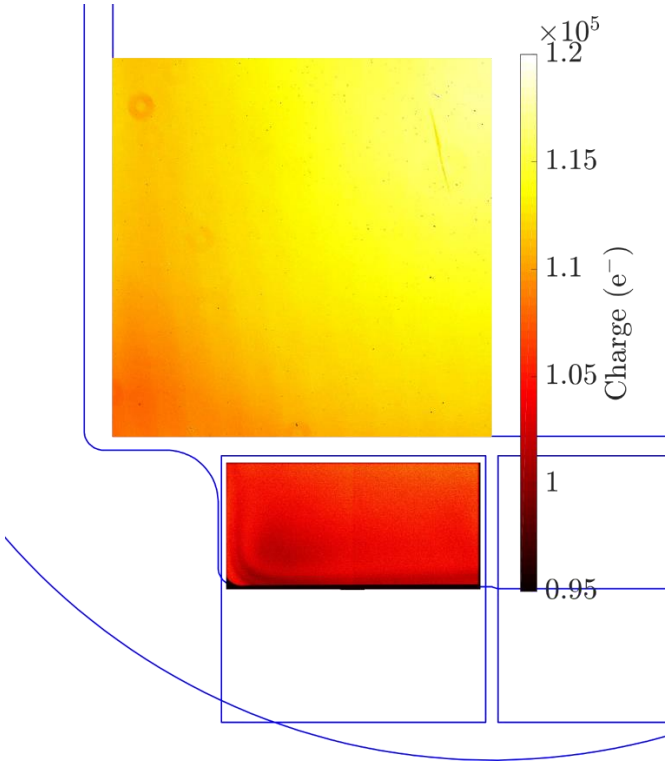


Figure 2.33 Color map of **r'** band flat across both guider and a portion of the main chip.

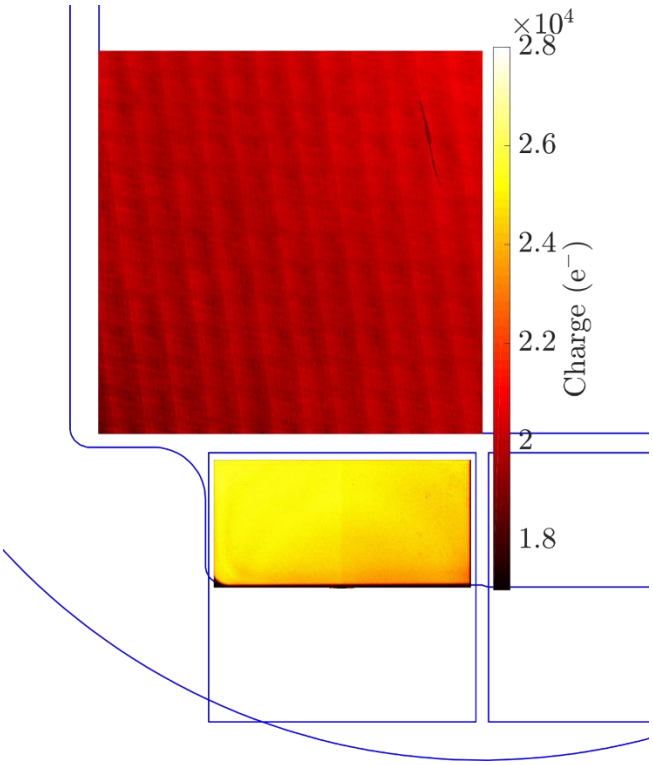


Figure 2.34 Color map of **u'** band flat across both guider and a portion of the main chip.

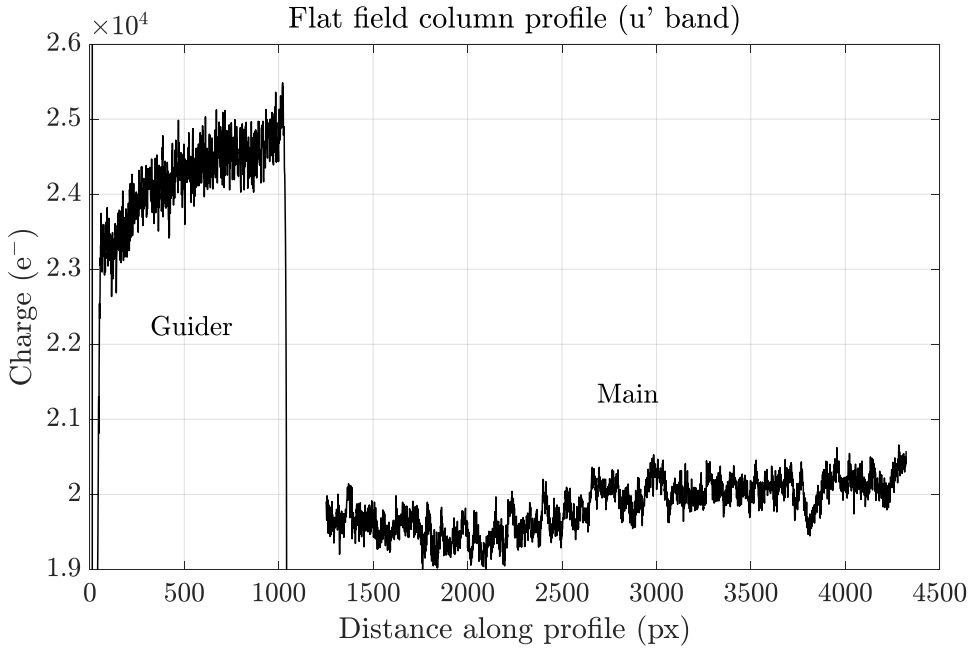


Figure 2.35 Column slice of **u'** band flat across both guider and a portion of the main chip.

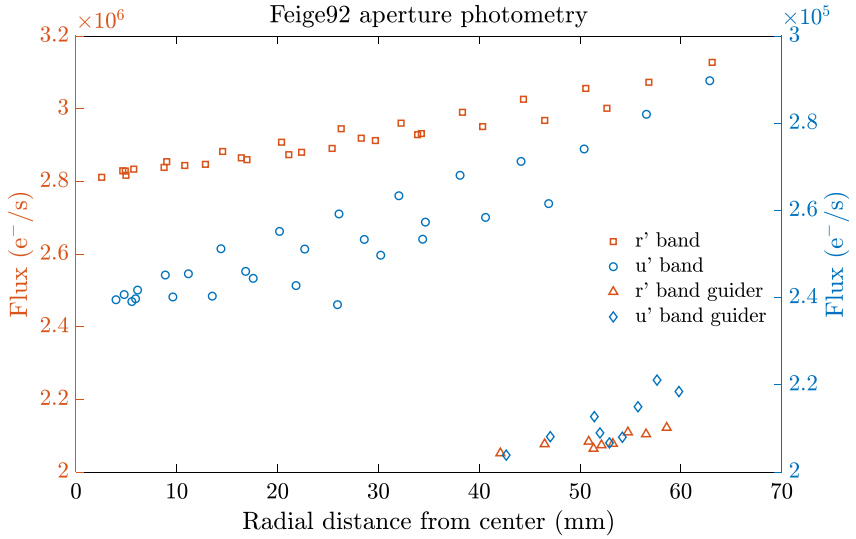


Figure 2.36 Aperture photometry for Feige92.

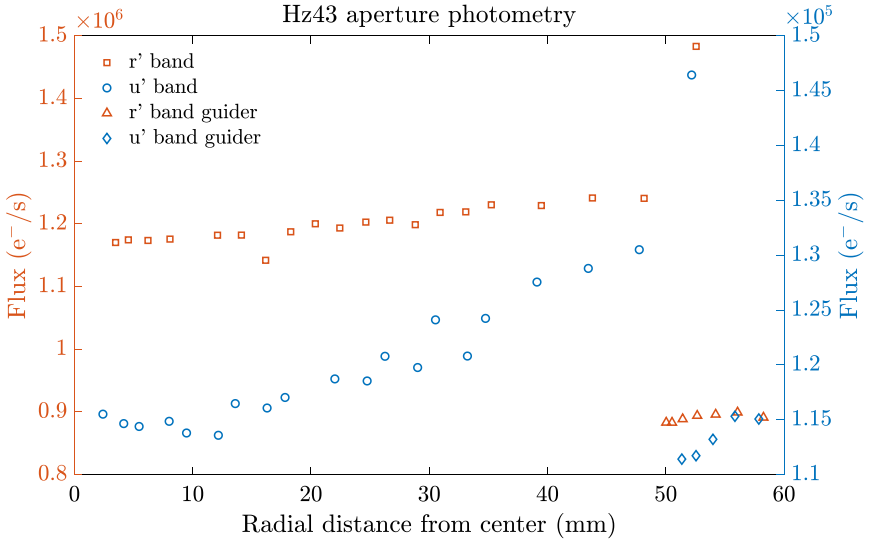


Figure 2.37 Aperture photometry for Hz43.

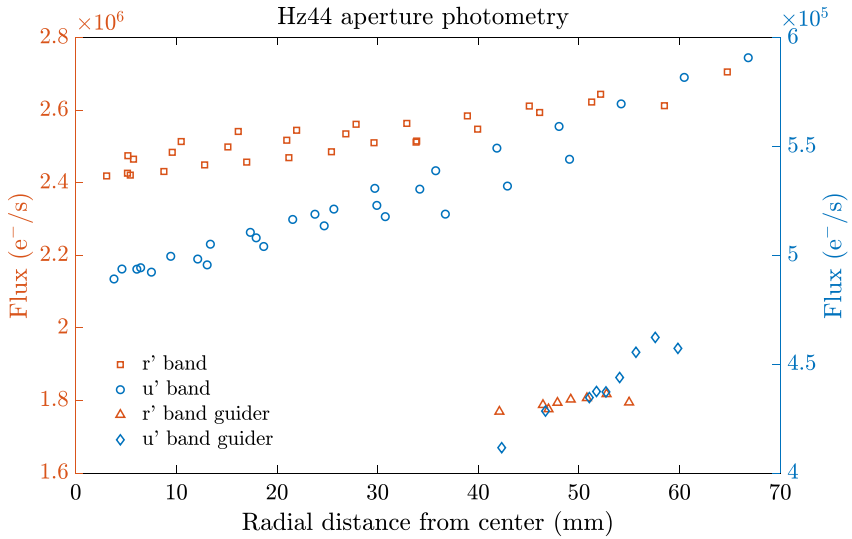


Figure 2.38 Aperture photometry for Hz44.

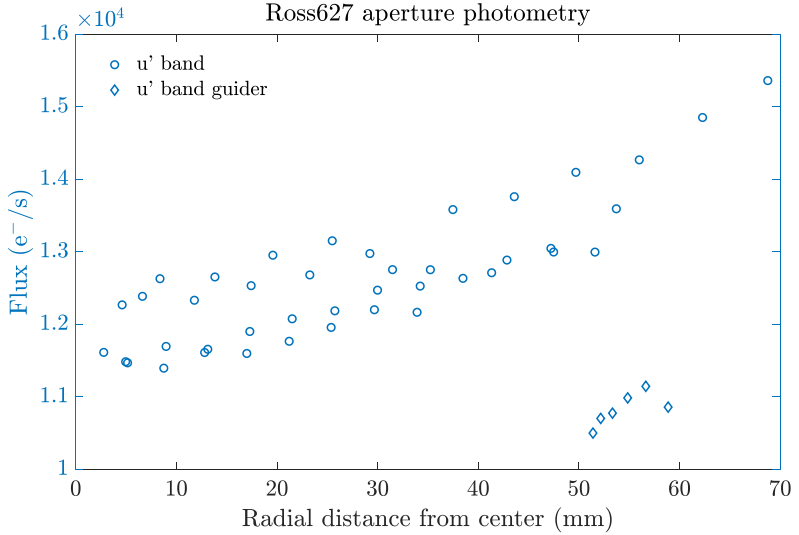


Figure 2.39 Aperture photometry for Ross627.

3 Trap pumping investigation of the E2V CCD231-C6

3.1 Introduction

In this chapter we describe the method and results of a CTE investigation performed using the WaSP camera (which utilizes new un-damaged CCDs). Specifically, the limitation on CTE presented by bulk lattice traps is explored, with detailed general-population characteristics of these traps. Bulk traps are a certain type of trap and traps are one factor among others that affect CTE. The existence of bulk traps, however, is the primary CTI causing effect in modern CCDs.

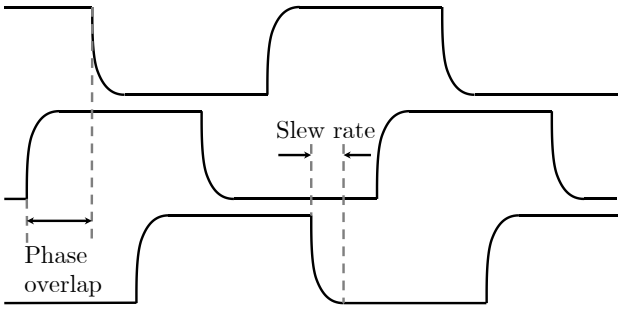
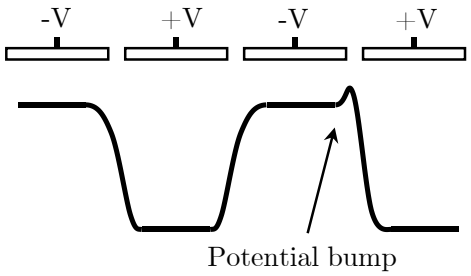


Figure 3.1 Waveform timing diagram (for a 3-phase device) showing overlap and slew-rate requirements.

CTE is the measure of a CCD's efficiency in transporting a charge packet from one pixel to the next ie. the fraction of a charge packet size (number of charge carriers) transferred. The parallel and serial registers are usually made with differently sized phases and are operated separately. Thus, CTE must be measured separately for both. As described in section 1.2.2, charge is transferred across phases by appropriately raising and lowering electrode potentials to storage and barrier states. To ensure good CTE, electrode voltage

slew times must be sufficiently low, otherwise blooming will occur. At the same time, phase overlap must be sufficiently high (higher than the charge diffusion time constant) to ensure decent CTE. This is depicted in figure 3.1.



- **Figure 3.2** Source of process and design traps. Indicated, is a bump in the potential field profile caused by a process defect.

Factors that determine CTE are

- Fringing field drift: This is the shape of the electric field near the edges of the phases. Fringing fields must be managed properly by defining appropriate clock slew-rates and clock levels.
- Self-induced drift: This is the effect of mutual repulsion of charge carriers. This effect is the first to take effect during the charge transfer process.
- Thermal diffusion drift: This is thermal scattering of charge. Temperature is the governing parameter of this effect and it is dominant in the absence of the aforementioned two. The effect decreases with decreasing temperature (despite carrier mobility increasing due to settling of the lattice structure).

Once the above effects are managed by tuning the CCD gate voltages, the remaining CTE limiting factor is to do with traps located in the signal channel. Generally, this is the case in modern CCDs, since when using manufacturer recommended gate voltages and timings,

CTE is routinely in the range of 0.99999 and 0.999999 (although this figure is dependent on signal level, as will be elaborated on in chapter 4).

3.1.1 Trap formation, locations and effects on data

Traps can be classified into the following four categories:

1. Design traps
2. Process traps
3. Bulk traps
4. Radiation traps

The first two types trap charge by means of an alteration in the electric potential field in the path of charge transfer. This is depicted in figure 3.2. Design traps are those that are caused by improper design features. This most usually occurs in areas of the CCD where electrodes vary in width, causing a constriction in the signal path. With bad specification, this area may result in a potential "bump": a design trap. Process traps on the other hand are potential "bumps" caused by errors in the manufacturing process. These are errors such as the peeling of the edges of polysilicon gates and dopants being injected in places they should not. Design and process traps are capable of trapping on the order of tens to thousands of electrons. As quite a mature technology, CCDs are nowadays relatively immune to these things.

The second two types correspond to energy states between the valence and conduction bands of the Si lattice (as depicted in figure 3.3). They typically capture one electron at a time (though not strictly, as we will show later) and have a fixed volume density depending

on the purity of the silicon and – in the case of traps caused by radiation damage – the incident radiation flux density. Since CCDs are normally manufactured using high quality silicon, bulk traps are typically not a concern for ground-based astronomy since CTE is good enough except in very high precision applications. Radiation caused traps on the other hand are almost always a concern. As will be demonstrated, for bulk and radiation traps, trap capture and emission is dependent on pixel clock rate, temperature, charge packet size, and charge packet density.

Even as CCD manufacturing standards rise, so too do their requirements for the purpose of precision astronomical measurements. Lattice traps remain the next challenge to overcome in terms of improving CTE. High-precision radial velocity measurement by ground based instruments is a prime case in point as described in [21]. It was determined that CTI was responsible for shifts in measured radial velocity of several m s^{-1}. The remedy used was to calibrate the effect and correct it during data reduction. A limitation of this approach, however, was that the CTI dependence on signal level was not completely understood and hence not faithfully modelled, causing uncertainty in the correction.

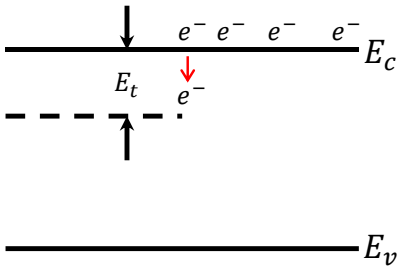


Figure 3.3 Source of bulk and radiation induced traps. Defects create trap energy states in the forbidden bandgap.

Looking to space applications, CTE is, for example, an unsolved challenge to the Euclid mission (undertaken by ESA) which will be making precise galaxy shape measurements (using the VISible imaging instrument) for weak gravitational lensing studies [32]. According to simulations, for a p-channel CCD, the mission will exceed the shape measurement error budget within four years solely due to diminishing CTE. The situation is much worse for n-channel CCDs which are more susceptible to radiation damage due to the different mechanisms for creating traps for holes and electrons. For the WFIRST coronagraph which is to perform direct imaging of exoplanets, the expected planet signal is at most a few electrons [28]. Extensive work is underway to determine how to retain this signal as it traverses the silicon on the way to the output amplifier. All approaches are being considered to tackle this issue – from hardware modifications (introducing notched signal channels) to optimized clocking, modeling and post facto correction and also simply lengthening exposure times (at the expense of observing cadence).

3.1.2 Types of traps in CCDs and mechanism of CTI

Trapping in CCDs is generally modelled using the Shockley-Read-Hall model for the rate of carrier generation and recombination (also known as trap-assisted generation and recombination) [35]. This process consists of four sub-processes and these are depicted in figure 3.4. According to this model,

$$U = \frac{pn - n_i^2}{p + n + 2n_i \cdot \cosh\left(\frac{E_i - E_t}{kT}\right)} N_t v_{th} \sigma \tag{3.1}$$

where U is the net rate of generation/recombination (carriers s^{-1} cm^{-3}), N_t is the trap density (cm^{-3}) at energy level E_t (eV), E_i is the intrinsic Fermi level (eV), σ is the carrier

cross section (cm^2), v_{th} is the thermal velocity (cm s^{-1}), T is temperature (K) and n, p are the concentrations of free electrons and holes respectively (cm^{-3}) [19]. A positive U indicates a net recombination of electron-hole pairs and a negative U indicates a net generation of electron-hole pairs.

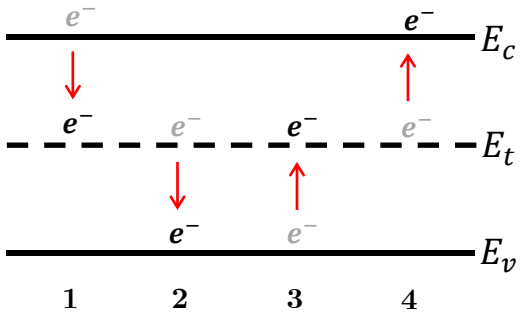


Figure 3.4 Recombination and generation processes modelled by equation (3.1).

From this relation, the carrier lifetime can be expressed as,

$$\tau_c = \frac{1}{N_t v_{th} \sigma} \tag{3.2}$$

where τ_c is the capture time constant in an exponential decay process. The emission time constant, τ_e is defined as,

$$\tau_e = \frac{1}{N_c v_{th} \sigma} \exp\left(\frac{E}{kT}\right) \tag{3.3}$$

where N_c is the density of conduction band states (cm^{-3}). The thermal velocity v_{th} is given by,

$$v_{th} = \sqrt{3kT/m_{e,c}} \tag{3.4}$$

where $m_{e,c}$ is the electron effective mass for conductivity ($m_{e,c} = 0.26m_0$ where $m_0 = 9.11 \times 10^{-31}$ kg, the rest mass of an electron). The density of conduction band states is given by,

$$N_c = 2 \cdot \left(2\pi \cdot m_{e,d} \cdot \frac{kT}{h^2}\right)^{3/2} \tag{3.5}$$

where $m_{e,d}$ is the electron effective mass for calculation of density of states ($m_{e,d} = 1.08m_0$).

From the point of view of CCD charge transport, it is the capture and emission time constants that are of critical importance. The probability of capture/emission within the interval $[0, t]$ of a given trap in a CCD is then,

$$P_{c,e} = 1 - \exp(-t/\tau_{c,e}) \tag{3.6}$$

where t is the dwell time (s) of the carrier in the vicinity of the trap. These time constants can be measured on a trap by trap basis for a CCD and thus, by then deriving the corresponding energy level of the trap from Eq.(3.3) the trap can then be identified by cross-referencing the literature on known silicon trap characteristics.

The defect types typically found in silicon are well documented as the semiconductor is ubiquitous in microelectronics where such knowledge is highly relevant. A comprehensive reference is found in [29]. In essence, CTE causing traps are known as **point defects** in the Si lattice of which there are two types: **intrinsic** and **extrinsic** point defects. Intrinsic point defects are formed when lattice elements are displaced, causing vacancies and self-interstitials. Extrinsic point defects are formed due to the presence of foreign impurities which are either naturally occurring or introduced as dopants (figure 3.5). Naturally occurring impurities are those such as carbon and oxygen while typical dopants are phosphorus and boron.

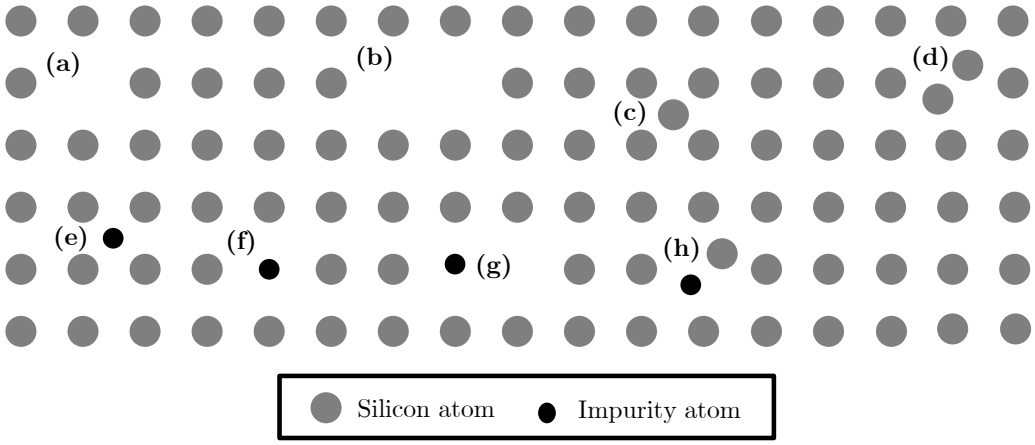


Figure 3.5 Silicon lattice point defects. (a) Vacancy, (b) Divacancy, (c) Self-interstitial, (d) Interstitialcy, (e) Interstitial impurity, (f) Substitutional impurity, (g) Impurity-Vacancy pair, (h) Impurity-Self-interstitial pair.

In recent work on CCD traps, extrinsic point defects resulting from an un-irradiated CCD have been identified [37]. Based on an assumed cross section σ, two defects purported to match those found in pocket pumping experiments are stated to be the carbon-interstitial-phosphorus-substitution (C_iP_s) and the boron-interstitial-oxygen-interstitial (B_iO_i). These are traps with energy levels closest to those calculated from the trap time constants measured at different temperatures. However, since the number of traps resulting from impurities are so numerous and span a large range of energy levels it becomes difficult to speculate on the identity of any particular trap. Furthermore, identification of such bulk traps has since been limited to very few efforts as most groups have directed their efforts to investigating radiation damage traps which result in intrinsic point defects (vacancies and self-interstitials).

3.2 Trap characterization

Traditionally, the technique of Deep Level Transient Spectroscopy (DLTS) is used to characterize charge carrier traps in semiconductors. In this method, a voltage is pulsed across a diode of the semiconductor connected in reverse bias to fill traps in the depletion region. During trap thermal emission, a transient capacitance is induced due to the recovery of the trap charge states. The measurement of this capacitance is repeated for varying voltage pulse frequencies and from this data, a 'resonance' frequency can be identified where the measured transient capacitance is maximum. This reveals the energy level of the trap species. A limitation of this method is that all trap species are probed at the same time. However, the Laplace DLTS technique overcomes this by employing Laplace transforms to delineate species by energy level [46]. Nonetheless, DLTS results are only used as a cross-reference here as CCDs are not amenable to this method.

Trap studies in the context of CCD CTE have been most recently spearheaded by the Center for Electronics Imaging (CEI) which is a department at the Open University (located in Milton Keynes, UK). The CEI group has been contracted to develop CCDs for the ESA Euclid and NASA WFIRST missions which both require exceptional CTE for mission success. In their experiments, CCDs are (partially) exposed to a certain dose of high energy protons (typically at an independent facility) and trap emission time constants are measured using the pocket-pumping technique. Their extensive studies have identified five species of intrinsic point defects (for n-channel CCDs) that most significantly impact performance; they are outlined in table 3.1.

The silicon E and A center defects are variations of the Si self-interstitial defect while the two divacancy defects are the single and double donor configurations of the same defect. One of the defects has yet to be identified. The functions $\tau(T)$ that these values of σ and E yield according to Eqs (3.2 – 3.5) are depicted in figure 3.6. It should be noted that p-channel CCDs are susceptible to different species of defects that can be found in [11].

Table 3.1 CCD radiation traps – known energy levels and cross-sections in the literature.

Defect	E_t (eV)	σ (cm^2)
Si-E	0.46	5×10^{-15}
(V-V)$^-$	0.39	2×10^{-15}
Unknown	0.3 – 0.34	5×10^{-16}
(V-V)$^{--}$	0.21	5×10^{-16}
Si-A	0.17	1×10^{-14}

Table 3.2 CCD pre-irradiation traps – known energy levels and cross-sections in the literature.

Defect	E_t (eV)	σ (cm^2)
C_iP_s (III)	0.23	3×10^{-15}
B_iO_i	0.27	5×10^{-16}
C_iP_s (IIB)	0.32	1.5×10^{-14}

Pre-irradiation defects have been identified in the references ([37] and [6]) although these defect species attributions are speculative due to the error bounds on the calculated energy levels. Nonetheless, these are tabulated in table 3.2 below. The carbon-phosphorus defect complex has five configurations according to [29] and two of these are suspected to be CTE causing traps. The remaining trap is a combination of interstitial boron and oxygen.

3.2.1 Pocket pumping

The term 'pocket-pumping' refers to the method of filling charge traps (charge pockets) and allowing them to emit (pump) into pixels/charge packets that they did not originate

from. It is a powerful technique, first used to characterize traps by pixel location and size (number of electrons trapped) [19]. This is accomplished by exposing the CCD to a flat field and then clocking the image forwards and backwards by a certain number of phases/pixels over and over again. During the process, traps are filled when a charge packet surrounds it and emit when the charge packet has left. The packet which the emitted charge joins depends on whichever packet is closest. Thus, if charge is 'pumped', it is transferred from a given pixel to either the preceding or subsequent pixel/packet (see figure 3.8). After pocket pumping, one can expect an image such as that in figure 3.7 (left).

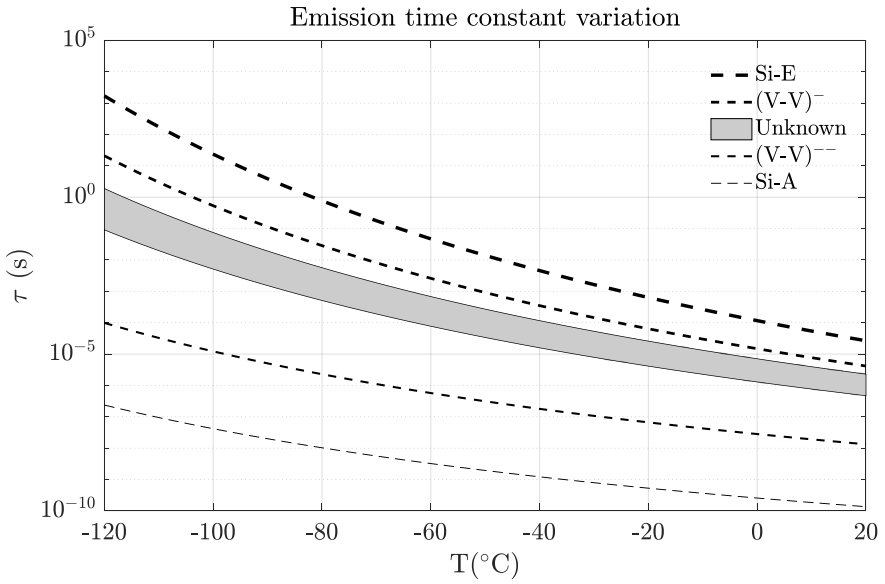


Figure 3.6 Radiation traps from table 3.1 – emission time constants as a function of temperature according to equations (3.2 – 3.5) and trap parameters E and σ.

It is worth noting that the pumping sub-scheme illustrated in figure 3.8, is for a three phase device of equal phase widths which is not always the case. In the illustrated case, the scheme can be notated as 1-2-3-2 (the sequence of phases traversed each cycle). Here, traps in phase 1 will pump 'backwards' (in the parallel readout direction), producing a

dark pixel with a *subsequent* bright one. Traps in phase 3 (not pictured) will pump 'forwards' producing a dark pixel with a *preceding* bright one. Traps in phase 2 will not pump. This is because the closest charge packet to any trap in phase 2 is always the originating packet. Traps in phase 2 can be probed by the sub-scheme 2-3-1'-3. Of course, in this scheme, traps in phase 1 are also probed (again) but they can be differentiated from those in phase 2 by the orientation of the dipole. All sub-schemes combined comprise the pumping scheme for the device.

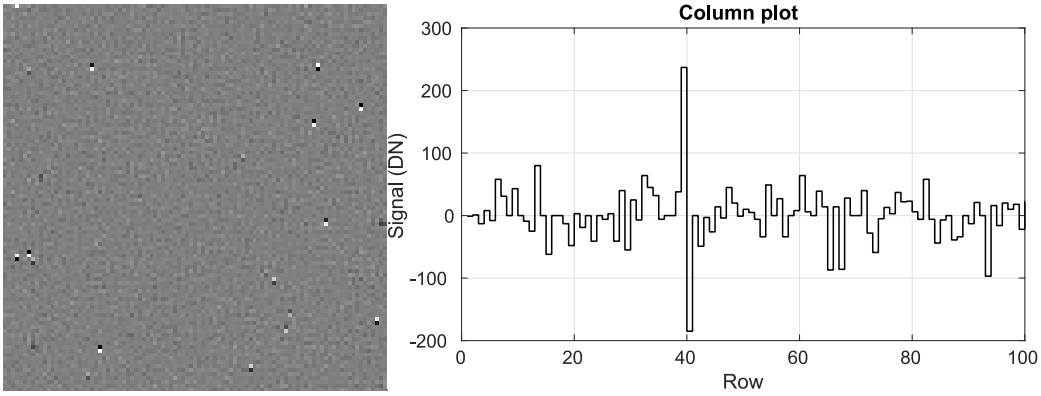


Figure 3.7 Left: Pocket pumped image sample. Right: Column plot (of mean subtracted signal counts) clearly showing a trap dipole at row 40.

There are a few caveats to be mentioned for this method. Firstly, the situation is of course more complicated for the case of more than a single trap within a phase. This case, however, is treated as rare and thus unaccounted for (a possible source of error). Secondly, the scheme must be modified for different architectures (as is the case for this report) according to the number of phases in a pixel and for non-uniform phase widths — this is because the scheme defines the fraction of the pixel/phases probed. The phase width and phase separation between packets will define the fraction of the pixel/phase probed.

Examples of unconventional pumping schemes to account for such variations can be found in [39] and [6].

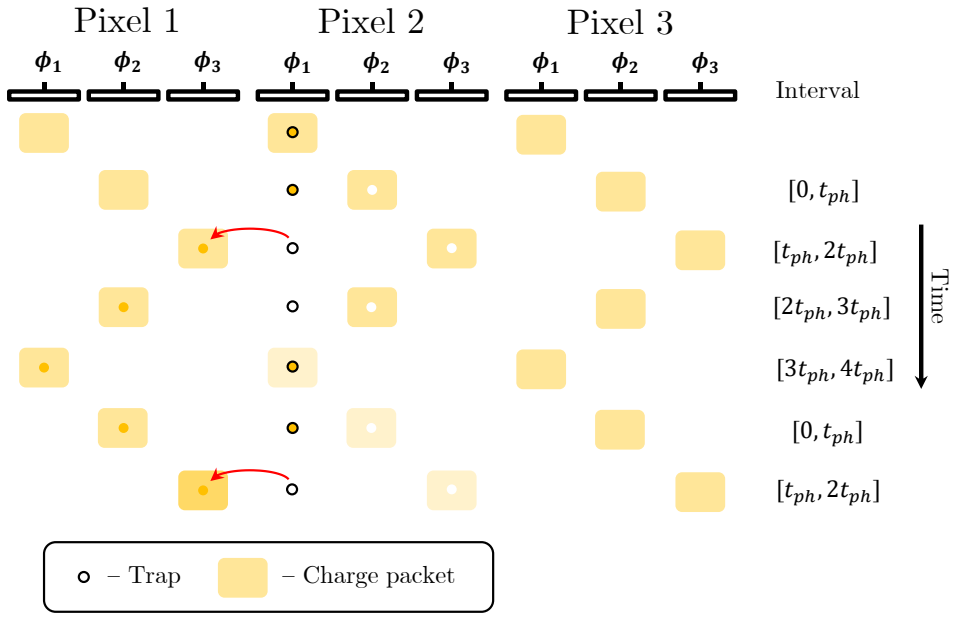


Figure 3.8 Sub-scheme (1-2-3-2) for a three phase pumping scheme showing a trap in phase 1 that is pumping. Traps in phase 3 (not shown) will also pump in the same way.

A pocket pumped image from a CCD should in principle have a uniform dipole density across the image because the trap density is also constant. This density, however, will be determined by the flat-field signal level used for pocket pumping. This is because the mean charge packet size defines the volume of silicon probed in each pixel and thereby the probability of a trap encounter. The trap volume density is then $N_t \,/\, (N_p \cdot V_c)$ where N_p is the number of pixels, V_c is the charge packet volume, and N_t is the total number of dipoles (traps) found. The flat-field signal therefore must be set high enough to see a decently representative number of traps. However, if set too high it may take an unreasonable number of pumping cycles to produce measurable dipoles above the shot

noise. Furthermore, if there is significant flat-field variation, there will be a commensurate variation in the density of traps revealed across the device.

3.2.2 Trap parameters

After pocket pumping N cycles (typically on the order of thousands), one can expect column profiles such as that in figure 3.7 (right). Each dipole is composed of bright and dark pixels with levels S_1 and S_2 DN, measured relative to the local mean level. The dipole intensity, I of a given trap is then $I = |S_1 - S_2|/2$; the amount of signal 'pumped' which is a measure of the pumping efficiency. According to figure 3.8, a trap pumps if trapped charge is emitted in the interval, $t_{ph} < t < 2t_{ph}$. By equation (3.6), the probability of emission in this interval is,

$$P_e(t_{ph} < t_{emit} < 2t_{ph}) = \exp\left(-\frac{t_{ph}}{\tau_e}\right) - \exp\left(-\frac{2t_{ph}}{\tau_e}\right)$$

Thus assuming that a trap captures D electrons in each pump cycle with a probability of capture P_c, the dipole intensity is given by $I = NP_cP_eD$. So as a function of the phase time, t_{ph},

$$I(t_{ph}) = NDP_c\left[\exp\left(-\frac{t_{ph}}{\tau_e}\right) - \exp\left(-\frac{2t_{ph}}{\tau_e}\right)\right] \tag{3.7}$$

By repeating the pocket pumping experiment for varying values of t_{ph}, the dipole intensity I can be measured (example in figure 3.9) and then $I(t_{ph})$ fitted by least-squares to determine τ_e (and P_c and D) for a given trap. Typically, $D = 1\text{e}^-$.

Once all traps are characterized by emission time constant τ_e, the process can be repeated for various temperatures, T to obtain curves resembling those in figure 3.6. This allows

the use of equation (3.3) to employ least squares fitting in order to obtain the two parameters, σ (the capture cross sectional area) and E (the trap energy level below the conduction band; $E = E_c - E_t$). Peaks in the histogram of traps in terms of their energies and cross sections should correspond to known trap parameters documented in a reference such as [29]. Once the atomic composition of the trap is known, its behavior under various conditions can be predicted and its formation can even possibly be limited at the manufacturing point of the CCD.

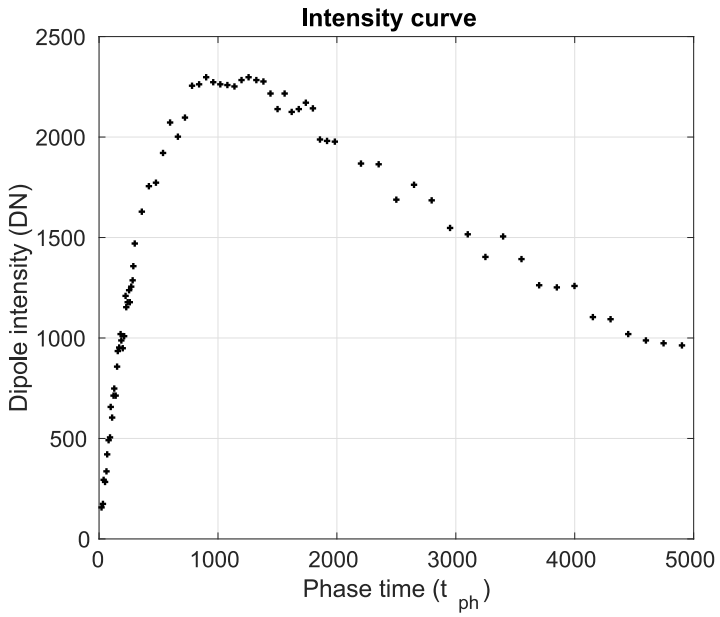


Figure 3.9 Sample dipole intensity curve for a single trap pumped at different frequencies (phase times, t_{ph} (μs)). By fitting equation (3.7) to this, τ_e can be determined.

3.3 Pocket pumping the CCD231-C6

Pocket pumping was employed on the same detector described in section 2.3 and it is worth noting that the experimental setup was also the same. This highlights the simplicity of using pocket pumping for trap characterization. In chapter 4, it will be shown that the

very same setup can also be used to accurately measure total deferred charge and thus, CTE.

3.3.1 Pumping scheme

As indicated in figure 1.4, the 231-c6 is a four-phase device. A natural extension of the pumping scheme portrayed in figure 3.8 is to extend it by including the fourth phase so the phase sequence of a sub-scheme becomes 1-2-3-4-3-2 (see figure 3.10). In this scheme however, traps are probed from three phases in a single pumping scheme so the dipole orientation is no longer sufficient to determine which phase the trap is in. Furthermore, the trap will pump within a different time interval depending not only on which phase it is in but also *where* in the phase it is in. This complicates matters since the pumping interval determines the form of equation (3.7).

Figure 3.11 shows the total area under a pixel in which traps will pump for this scheme. If the dipole is caused by a trap in region 1, according to figure 3.10 it will pump in the interval $[t_{ph}, 4t_{ph}]$. For region 2 it will pump in the interval $[2t_{ph}, 3t_{ph}]$ and for region 3 it will pump in the interval $[t_{ph}, 2t_{ph}]$. Thus, the trap must be distinguished from other traps by location to know which equation to fit to the dipole intensity curve. Nonetheless this scheme was in fact used by pocket pumping experiments in the past until only recently. See [11] and [39].

As it turns out, a simpler scheme is one almost the same as that used for the three phase device (figure 3.12). In this scheme, traps under half of each of two different phases are probed in a given sub-scheme. Note that the situation is different for the case of non-

uniform phase-widths unless alternate phases are the same size. In the case of the 231-c6, phases 1 and 3 are 4 µm and phase 2 and 4 are 3.5 µm so there is no issue. Four sub-schemes are then required to complete the pumping scheme (to probe the entire pixel), which can be used to determine the number of traps in each phase and their locations (to within half a phase). Figure 3.13 indicates the pixel region probed by sub-scheme. For example, sub-scheme 1 (1-2-3-2) probes half of phases 1 and 3. Sub-scheme 2 (2-3-4-3) probes half of phases 2 and 4 etc.

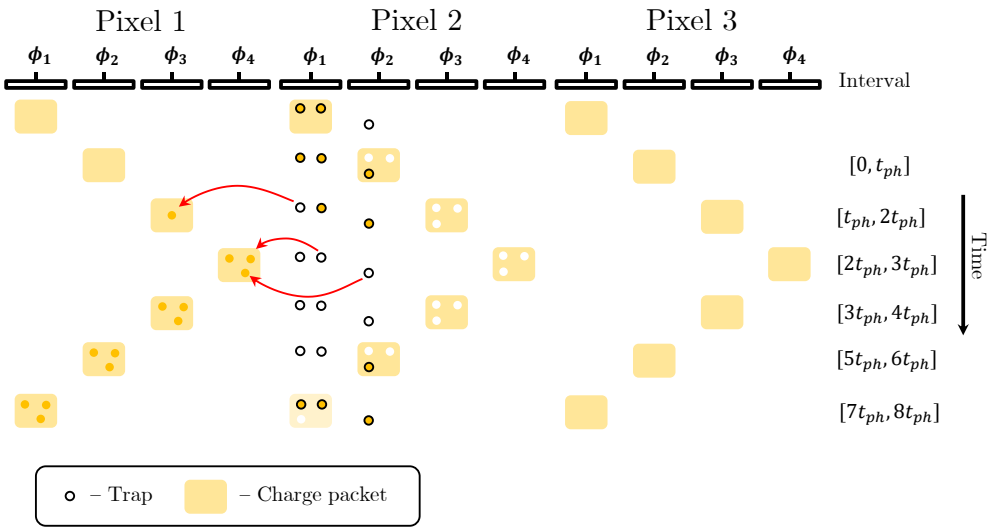


Figure 3.10 Four phase pumping scheme showing a traps in phases 1 and 2 that are pumping. Each trap pumps inside a different time interval. Traps in phases 3 and 4 pump in the same way (not shown).

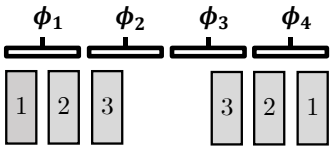


Figure 3.11 Traps in different regions of the pixel will cause different dipole intensities if pumped using the scheme in figure 3.10.

The illumination level was set by an exposure of 2 s to a level of 6500 DN or approximately 37 ke$^-$ (a gain of 5.7 e$^-$/DN). It was found that this level is sufficient for the size of dipoles created by pumping with $N = 10000$ times. There was a variation in the flat-field level by approximately 500 DN from the edges to the center of the image although this is not expected to significantly alter the number of traps observed (this is proven in the next chapter).

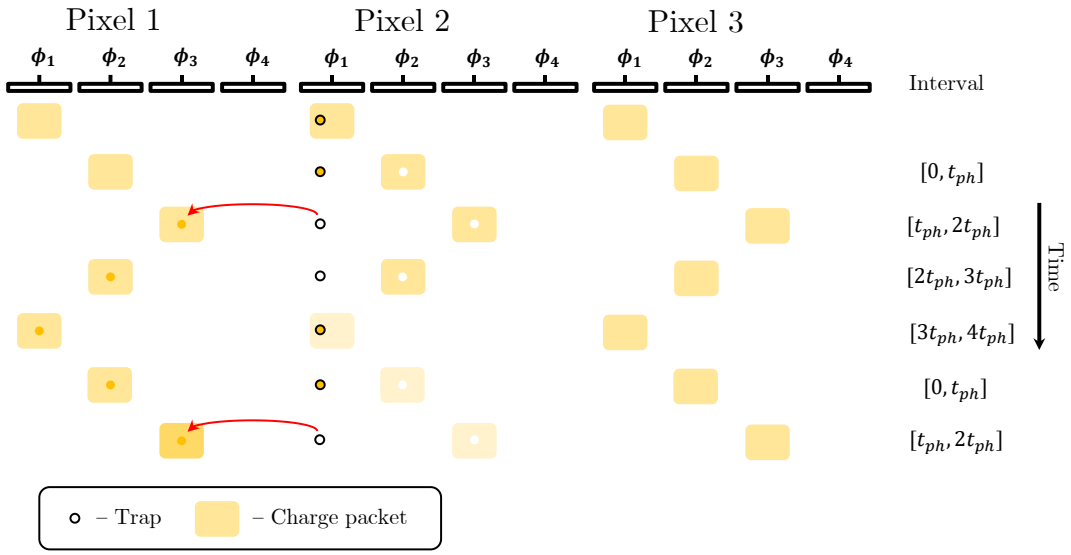


Figure 3.12 Simpler pumping scheme for a 4-phase device. Pictured is the sub-scheme, 1-2-3-2 – almost the same as for 3-phase.

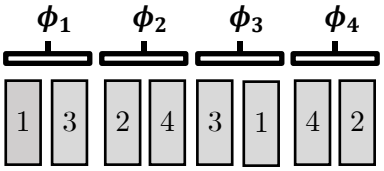


Figure 3.13 Regions of a pixel probed by each sub-scheme of the pumping scheme illustrated in figure 3.12 (which shows sub-scheme 1). The sub-schemes are 1) 1-2-3-2, 2) 2-3-4-3, 3) 3-4-1'-4, 4) 4-1'-2'-1' (where the apostrophe denotes phases of the next pixel).

A final detail to be mentioned is that attention must be paid to the range and step size of t_{ph} to be used. As shown in figure 3.9, the shape of the curve is ideally resolved on both

sides of the dipole intensity peak for accurate parameter fitting – this defines the range of t_{ph}. However, the step size should be set to the appropriate size so as to resolve the peak but also complete the pumping experiment in a reasonable amount of time. Without an estimate of the range of time constants of each trap species beforehand, this will take some trial and error.

3.3.2 An optimized scheme

The dipole intensity for the pumping scheme depicted in figure 3.12 is described by equation (3.7). In this scheme (traversing four phases each cycle), the charge packet dwells for a period of t_{ph} in each phase and the pumping cycle is repeated N times. Thus, the time taken T for a single pumped frame is,

$$T = 4t_{ph}N \tag{3.8}$$

The range of t_{ph} as stated previously is determined by the emission time constant τ_e of the trap species being probed. If τ_e is high, then the experiment time (range of t_{ph} values to be tested) can become impracticably high.

Can we reduce the number of times pumped, N? No, since N determines the peak value of $I(t_{ph})$, the dipole intensity which is required to be high enough to be measured above the shot noise. In equation (3.7), the maximum value of the function $I(t_{ph})$ is $N/4$. For a required dipole intensity I_R, $N = 4I_R$ so that N is fixed. How then can we reduce the experiment duration? It can be shown that by varying the dwell times in each phase during the pumping process, the experiment can be shortened while achieving the same dipole intensities as in the original pumping scheme.

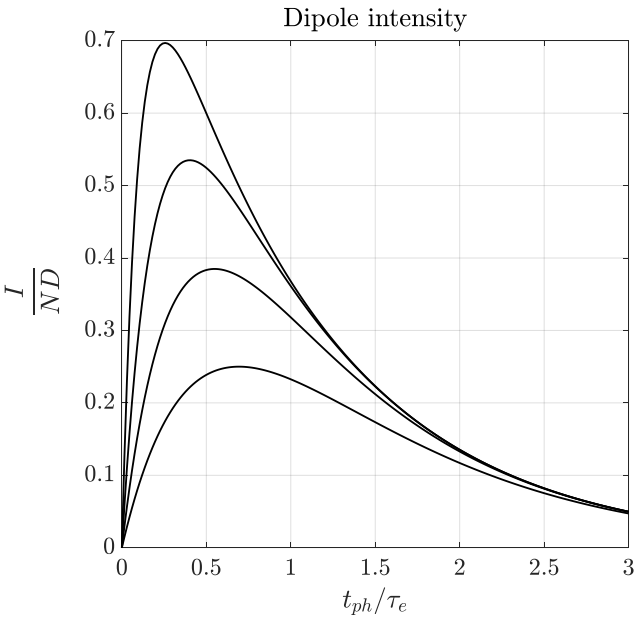


Figure 3.14 Dipole intensity function for $n = 1,2,3,4$. The peak value of I rises with n (assuming $P_c = 1$).

In the original scheme, traps pump if emitted in the interval $[t_{ph}, 2t_{ph}]$. To increase the dipole intensity we can increase the pumping interval to say, $[t_{ph}, nt_{ph}]$ where $n > 2$. Then, in the sub-scheme 1-2-3-1, the time spent in phases 1 and 3 is $(n-1) \cdot t_{ph}$ and the time spent in phase 2 remains t_{ph}. Equation (3.7) then becomes,

$$I(t_{ph}) = NP_cD\left[\exp\left(-\frac{t_{ph}}{\tau_e}\right) - \exp\left(-\frac{nt_{ph}}{\tau_e}\right)\right] \tag{3.9}$$

A plot of equation (3.9) for different values of n is shown in figure 3.14. The peak value of I rises with n. The peak value of equation (3.9) occurs at,

$$\left.\frac{t_{ph}}{\tau_e}\right|_{peak} = \frac{\ln(n)}{n-1} \tag{3.10}$$

and is given by,

$$I\left(\frac{t_{ph}}{\tau_e}\right)\Big|_{peak} = N(n^{1/(1-n)} - n^{n/(1-n)}) \tag{3.11}$$

N is then given in terms of the required dipole intensity I_R by $N = I_R/(n^{1/(1-n)} - n^{n/(1-n)})$ for any value of n. What is the best value for n? Considering the total time for the experiment, equation (3.8) becomes,

$$T = 2n \cdot t_{ph} N \tag{3.12}$$

This becomes (at peak pumping efficiency or peak I),

$$T = (2n \cdot t_{ph}\big|_{peak}) \cdot I_R/(n^{1/(1-n)} - n^{n/(1-n)})$$

Substituting (3.10),

$$T = \frac{4\tau_e I_R \cdot n \cdot \ln(n)}{(n-1)(n^{1/(1-n)} - n^{n/(1-n)})}$$

Setting an arbitrary constant $C = 4\tau_e I_R$,

$$T(n) = C\frac{n^2 \ln(n)}{(n-1)^2} n^{1/(n-1)} \tag{3.13}$$

We find that the total time for the pocket pumping experiment is a function of n. This is plotted in figure 3.15.

Plotting $T(n)$, a local minimum can be observed at approximately $n = 8$. Thus, a pumping scheme 1-2-3-2 with a dwell time of t_{ph} in phase 2 and $7t_{ph}$ in phases 1 and 3 is the scheme that will take the least amount of time to characterize traps. It is worth noting that compared to the original scheme of equal dwell times ($n = 2$), the optimized scheme ($n = 8$) takes 34% less time since $T(8) \,/\, T(2) \;= 0.66$, i.e., the optimized scheme will take 34% less time to pump traps to the same peak dipole intensity as the original scheme.

A comparison of the optimized and original schemes in actual use is made in section 3.4.5, where they are both used in characterizing the same set of traps, given the same amount of time in both experiments. It is shown that, all things being equal, the optimized scheme reveals more traps.

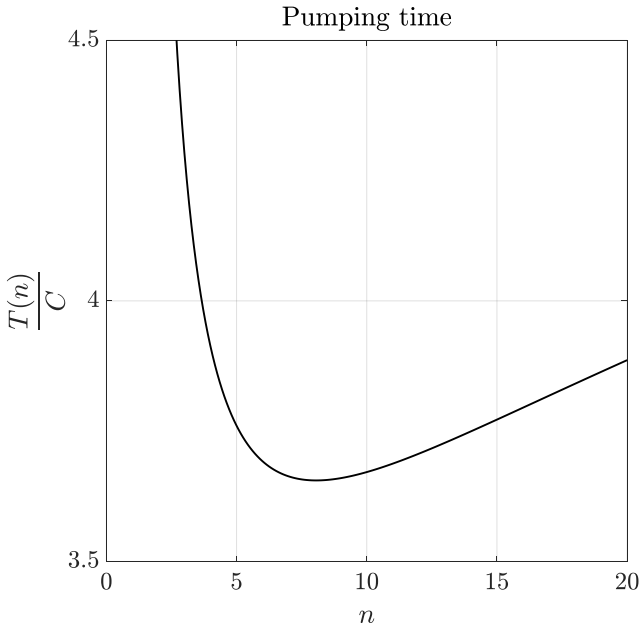


Figure 3.15 Pumping experiment time as a function of n showing a local minimum.

3.4 Data reduction and results

Pocket pumping data was taken using the same setup as used for general detector characterization described in section 2.3 (consisting simply of the camera facing a red LED on a light tight box). The temperature of the detector is reported as the reading on the thermocouple mounted on rear of the CCD package (which is one of many temperature sensors in the instrument according to figure 2.4). In order the reduce data size, pocket pumping was performed on the half of the CCD served by outputs E and F (or AD outputs 7 and 8) according to figure 2.7. All waveforms were programmed in the WDL and

MATLAB was used to load and script them on the Archon controller. Pocket-pumping experiments were performed at detector temperatures of 175K, 180K, 185K, and 190K.

3.4.1 Trap mapping

The first step in trap characterization is determining their locations. These are indicated by the locations of the characteristic dipoles shown in figure 3.7 in the column direction. Dipole identification was performed using a simple threshold selection algorithm without any treatment for trap clustering or groups of traps since the trap density in a new CCD was low enough for this to not be an issue.

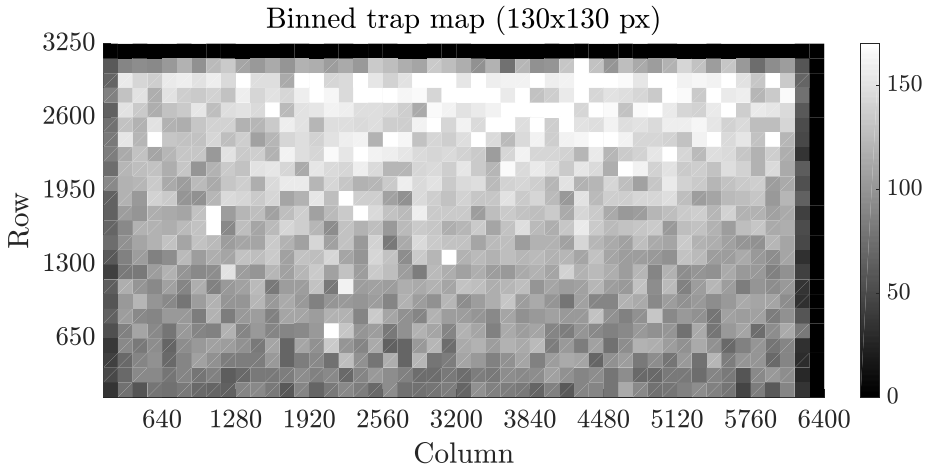


Figure 3.16 Binned trap map showing a gradient from the outer edge of the chip (bottom) to the middle of the chip (top).

The algorithm operates as follows:

1. Rearrange pocket pumped image to a single column by concatenating all image columns.
2. For each pixel in the column:
   i) Find all pixel values relative to the moving mean signal (mean subtract).

ii) The pixel is part of a dipole if,

a) the current *and* subsequent pixel's absolute values are over 4 times the moving standard deviation and,

b) the current pixel value multiplied by the subsequent pixel value is negative.

iii) If the pixel is a dipole, calculate the dipole intensity by taking the absolute value of the difference between the current and subsequent pixels.

3. Convert pixel index to image coordinates to give the trap pixel location.
4. Determine and record the dipole orientation and thus the trap phase location.

The moving (local) mean and variance are used, owing to the fact that the flat field was not uniform. The result of the above described trap search method yields traps distributed throughout the detector. As mentioned earlier, this was taken using a signal level of approximately 35000e^-. The total number of traps is approximately 130000 (at a temperature of 175K) between 6144×3080 pixels. The pixel size is quoted as 15 µm with a channel stop width of 4 µm. Assuming a buried channel depth of 0.5 µm, the total volume per pixel of Si probed is then $15 \times 11 \times 0.5 = 82.5$ µm^3. The volume density of traps is then $130000/(6144 \times 3080 \times 82.5 \times 10^{-10}\text{cm}^3) = 8 \times 10^5$ cm^{-3}. This volume density seems to be consistent with results found in pre-irradiated devices tested at the CEI.

A first glance, the trap map seems to support the assumption of a uniform trap density (of around 1 trap per 150 pixels); however, when binning is applied, the result is figure 3.16, where a clear gradient is observed from the edge of the chip to the middle. The cause of this is yet unclear. A possible explanation for this variation is the variation in

illumination level across the chip (explained in section 3.2.1). This is unlikely, both since the variation was not more than 3000 e^- and the flat field variation is concentric (centered roughly at the center of the chip). Another possible explanation is the process used during production of the silicon wafer during manufacture; however this is also likely to instead produce a radially symmetric variation since processing routines usually involve rotation (such as wafer lapping which is done by rotating the silicon ingot slices against abrasive material).

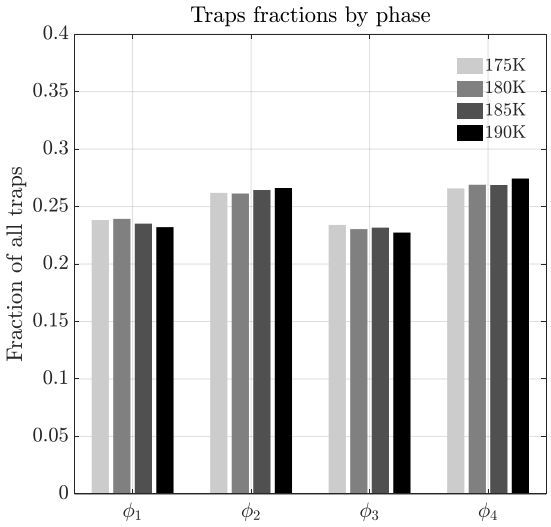


Figure 3.17 Trap fractions by pixel phase and temperature.

Table 3.3 Total number of traps identified by temperature.

Temp	Total traps
175K	129881
180K	134544
185K	125197
190K	122091

It should be noted that the total number of traps cannot be accounted for in a single pumped frame as this will only be a snapshot of the number of traps visible at a particular pumping frequency (with phase time, t_{ph}). At a given pumping frequency, only a subset

of the total number of traps will be detectable above the signal noise and hence the total number of traps must be the aggregate of all unique traps observed over the range of pumping frequencies tested. Figure 3.18 shows this variation in the number of traps seen in a given frame compared to the total number of traps seen across the range of t_{ph}. The plateau of the cumulative trap number curve indicates that no more new traps are being seen as t_{ph} increases; this plateau level can be taken as the total number of traps revealed by the given pumping scheme.

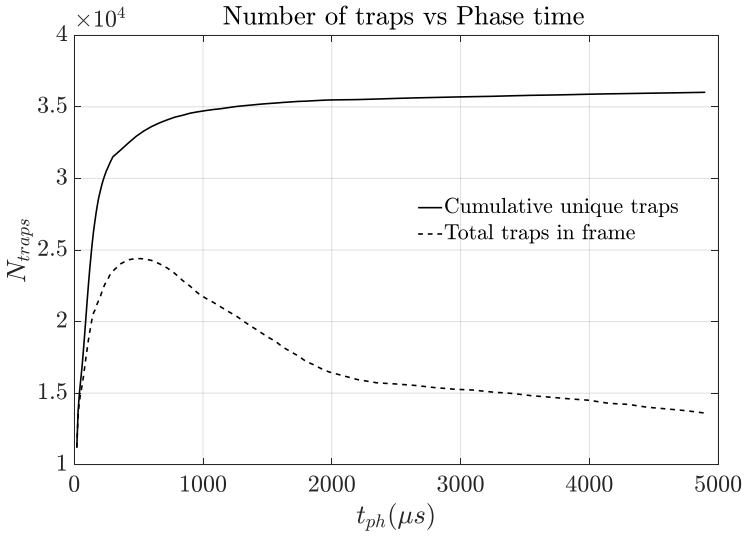


Figure 3.18 Cumulative traps and number of traps by frame as pocket pumping experiment proceeds by phase time, t_{ph}.

Table 3.3 shows that the total number of traps detected seems to be somewhat independent of temperature. We can further breakdown the trap population statistics to the population of traps by pixel phase number as shown in figure 3.17 which shows negligible variation with temperature. From this data we can also see two distinct populations in phases 1/3 and phases 2/4. It is known that phases 1/3 and have widths of 4µm each and phases 2/4 have widths of 3.5µm each. It is possible that the narrower phases 2/4 cause the charge

packet to occupy regions deeper in the channel than when it is in phases 1/3 (wider phases). This would lead to the conclusion that more traps are encountered the deeper the channel is.

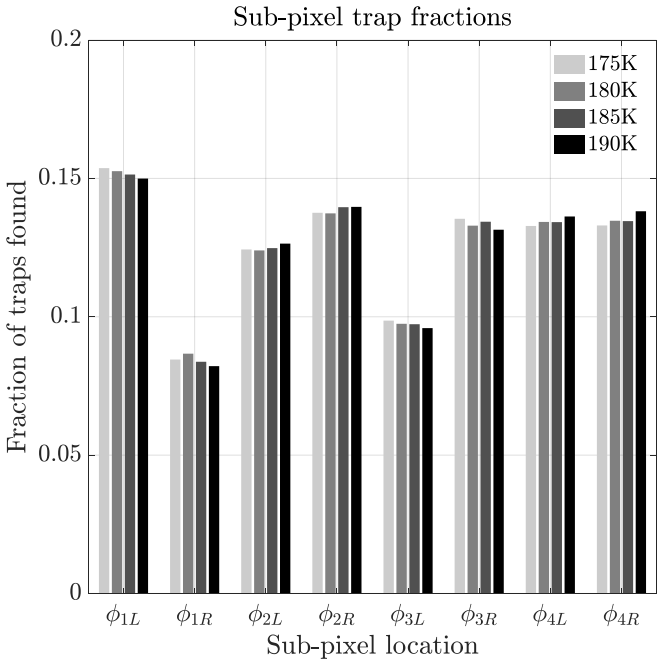


Figure 3.19 Trap fractions by sub-pixel-phase location and temperature.

We can further break down the trap populations by sub-phase location as shown in figure 3.19. Aside from negligible temperature variation again, we can also see the portions of the pixel in which there are distinctly fewer traps than others. This break in symmetry could be expected *if* phase 2 was wider than phase 4. Should this be the case, then the sub-scheme 3-4-1'-4 would probe less than two halves of a pixel. This would result in the observed less-than-expected number of traps reported in regions ϕ_{1R} and ϕ_{3L} although it would also have the added effect of yielding a more-than-expected number of traps in regions ϕ_{1L} and ϕ_{3R} (which is true for ϕ_{1L} but not for ϕ_{3R}). However the widths of each phase as specified by e2v do not support this (though it is possible that manufacturing

errors have resulted in unexpected phase widths). Further visual examination of the chip layout is required to corroborate the trap populations with phase widths.

3.4.2 Emission time constants

Since the complete pumping experiment must be completed before even mapping traps, determining emission time constants can proceed immediately after. A dipole intensity is calculated as described earlier for each trap and at each phase time tested. Figure 3.20 shows sample curve fits to the data of single traps over the range of t_{ph}. Fitting was done using the `lsqcurvefit` routine in MATLAB which is a non-linear least-squares solver employing the damped least-squares method.

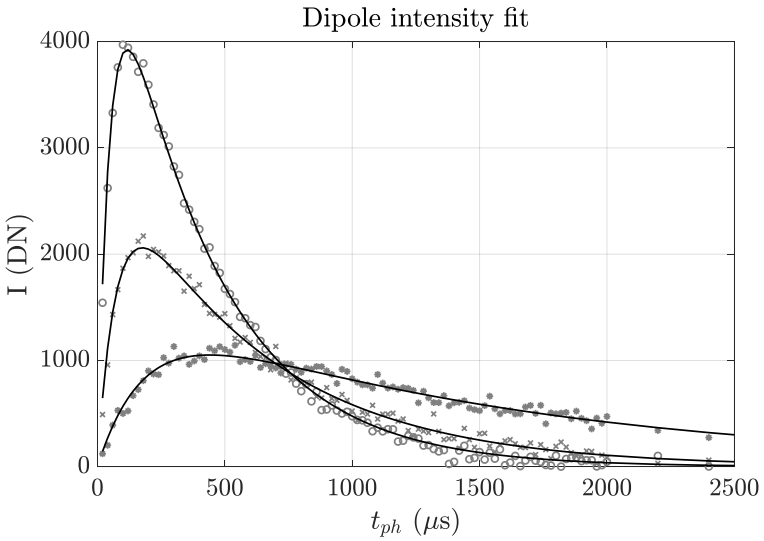


Figure 3.20 Sample dipole intensity curve data and curve fits. Horizontal peak location indicates τ_e and peak height indicates $P_c D$.

The large majority of traps yield well behaved dipole intensity curves and so goodness of fit criteria were not used to eliminate badly fit curves. Equation (3.9) (for $n = 8$) is fit to each dipole intensity curve and the two parameters solved for are $P_c D$ and τ_e. Note that

$P_c D$ is representative of the amplitude of the curve and τ_e represents the horizontal location of the peak.

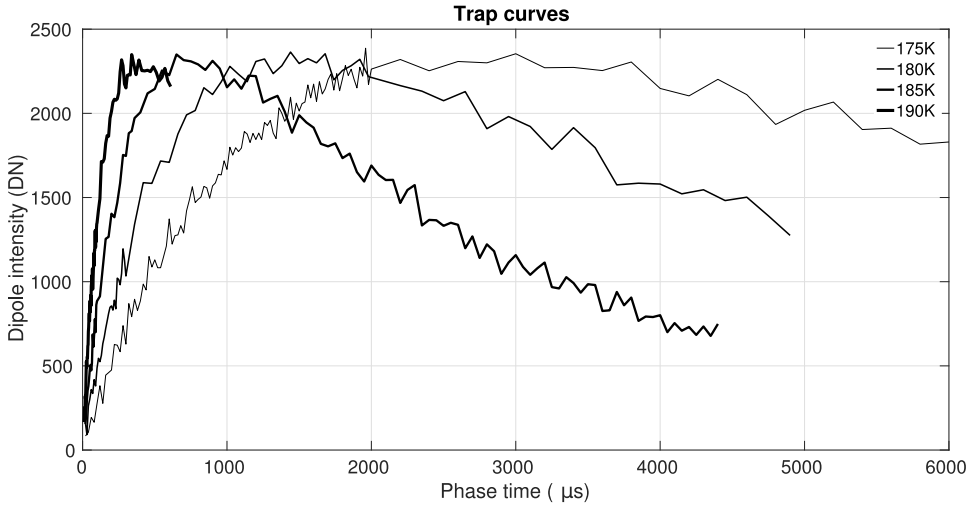


Figure 3.21 Sample dipole intensity curve data for a *single trap* at all temperatures.

Fitting all traps for all temperatures results in the τ_e histograms shown in figures 3.24 to 3.27. It is observed that there are four distinct species of traps identified at each temperature. For each species, the expected exponential decay of time constant with respect to temperature according to equation (3.3) is observed. For an example of how the dipole intensity curve varies as a function of temperature for a given trap, see figure 3.21.

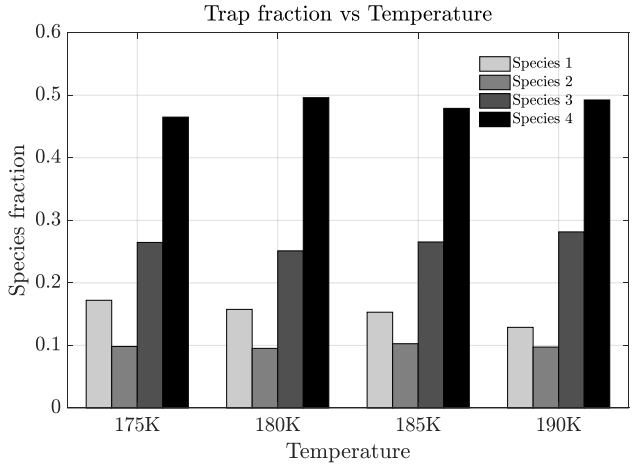


Figure 3.22 Trap fractions by species and temperature.

An interesting observation is the distribution in τ_e within a given trap species which is asymmetric. At least some of this spread must be due to noise and the extent of the noise contribution can be estimated by its symmetric component. Looking at the dipole intensity curve fits, it is unlikely that the remainder of the spread is due to error – rather it is likely a result of the trap level band width.

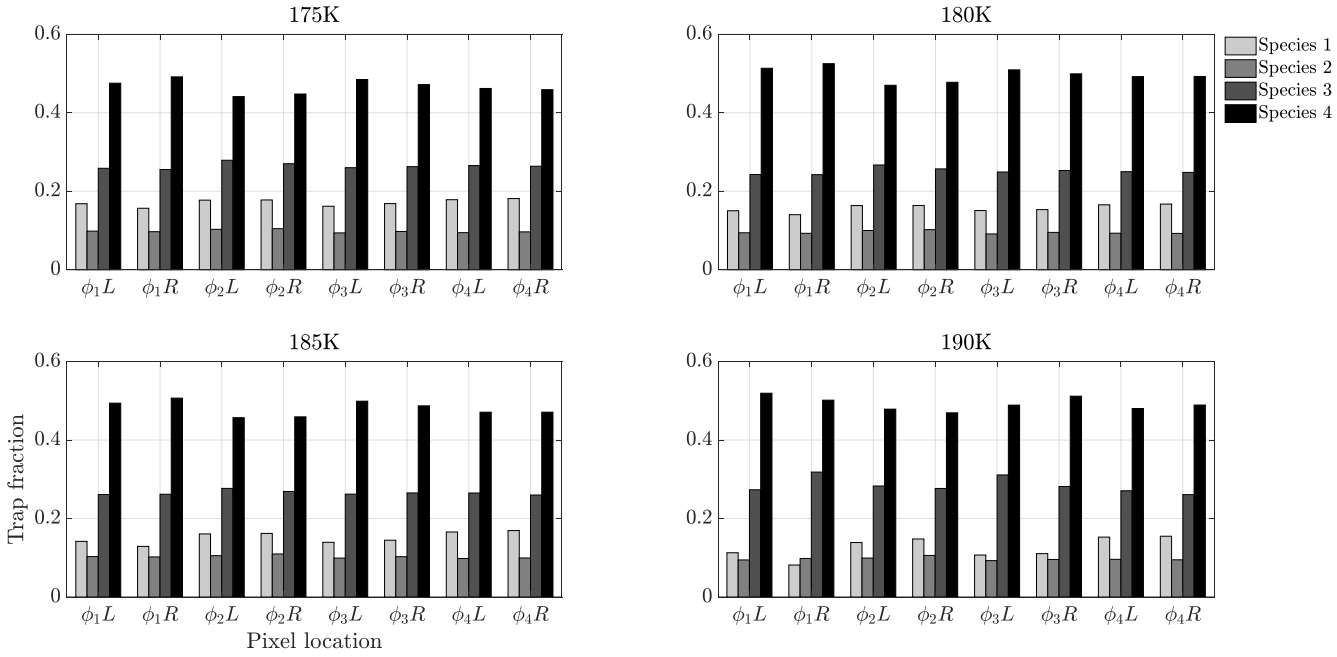


Figure 3.23 Trap fractions by species, sub-pixel-phase location, and temperature.

Calculating each species' contribution to the total trap population, we arrive at figure 3.22. Species 1 through 4 refer to the four peaks seen in figures 3.24 to 3.27 from left to right (or smallest emission time constant to the largest). The fractions are roughly invariant with respect to temperature albeit for a non-negligible reduction in the proportion of species 1 traps at higher temperatures. The majority of traps (at just under 50%) is represented by species 4 which has the largest emission time constant.

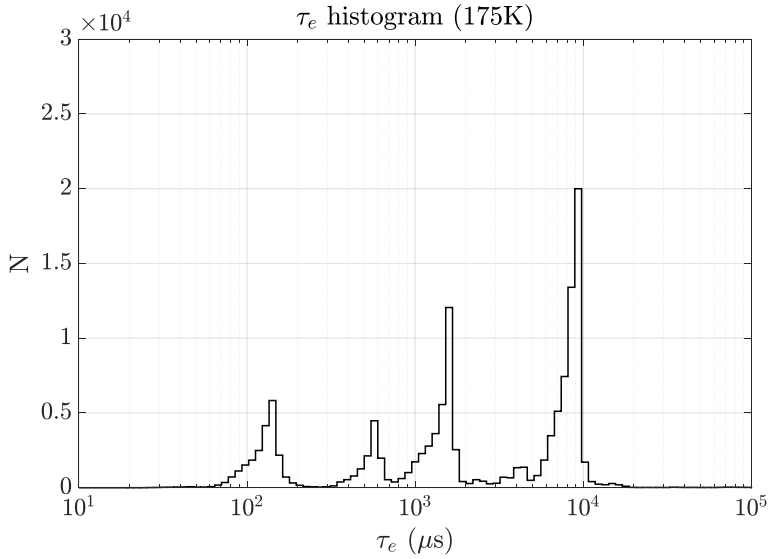


Figure 3.24 τ_e histogram measured at 175K.

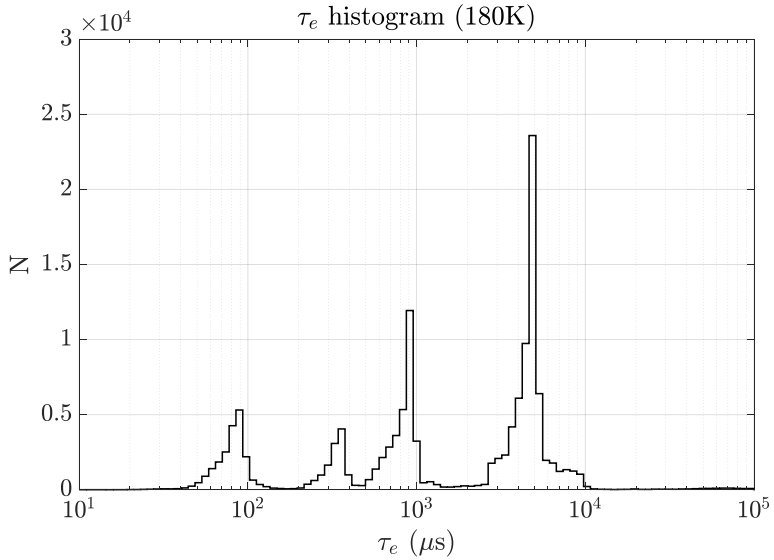


Figure 3.25 τ_e histogram measured at 180K.

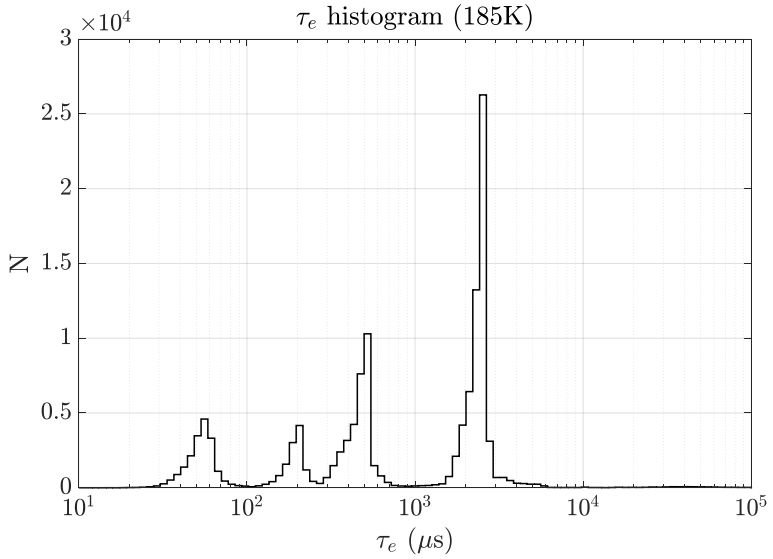


Figure 3.26 τ_e histogram measured at 185K.

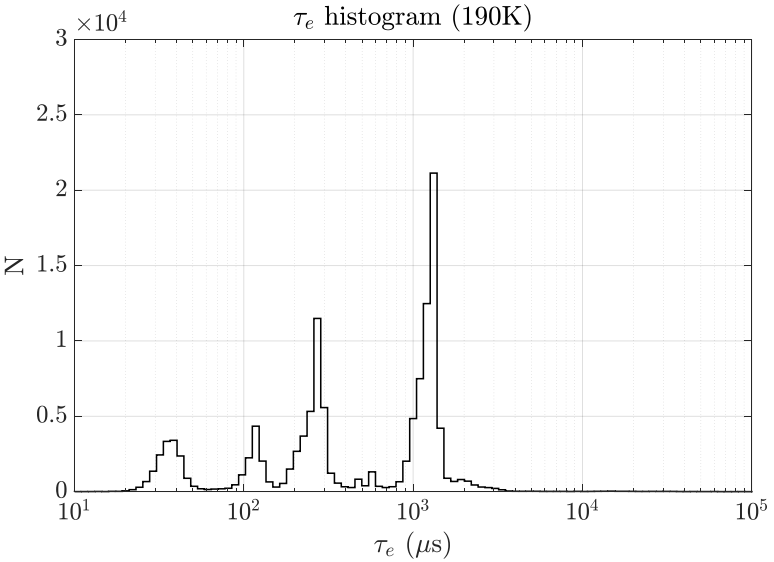


Figure 3.27 τ_e histogram measured at 190K.

Additionally, since both trap species and intra-pixel trap location data are available, it is then possible to test for species population trends as a function of intra-pixel location (shown in figure 3.23). No obvious trends are observed.

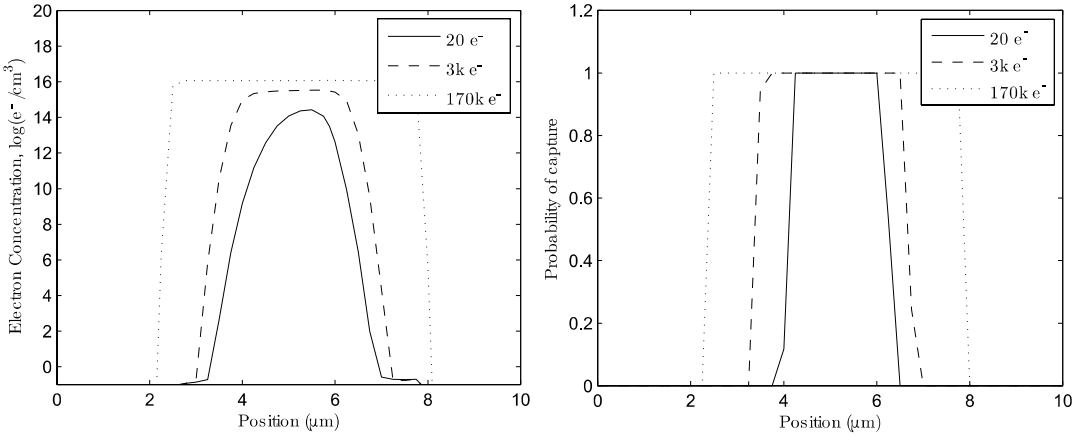


Figure 3.28 Results from Silvaco ATLAS simulations on charge concentration and capture probability from [24].

3.4.3 Trap depth

Histograms of the parameter $P_c D$ are shown in figures 3.30 to 3.33 for the temperatures tested. There are clear drop-offs at values of 1 and 2 ostensibly because D can only take on integer values and $0 < P_c < 1$. Therefore, all traps observed have a depth of, at most, 2e⁻. We can also see that there is a peak at $P_c D = 1$ and $P_c D = 2$ or equivalently, $P_c = 1$. This can be explained by noting that the capture probability, P_c is a function of the local charge packet density at the site of the trap. Beyond a certain density threshold, $P_c = 1$ and so there must be a region of a certain radius inside the charge packet which is greater than this threshold. This is confirmed by Silvaco ATLAS simulations presented in [24], reproduced here in figure 3.28. This shows a top-hat profile for the value of P_c as a function of distance from the electron charge cloud. If this profile is accurate, however, there should

be larger peaks than those observed – it is likely that the true P_c profile is a sloped top-hat.

Viewing the P_cD and τ_e data together reveals correlation between trap species and trap depth (see figures 3.34 to 3.37). Firstly, this reveals that there does not seem to be a correlation between P_c and τ_e for a given trap species – we can see an asymmetric distribution in both time constant and trap depth. Secondly, this data reveals the single species (species 2, the least populous type of trap) having a trap depth of $2e^-$ while the other three have a depth of $1e^-$. In semiconductor defect parlance this would be referred to as the double-donor energy level of a particular defect. Identification of these traps based on these data is dealt with in section 3.4.4.

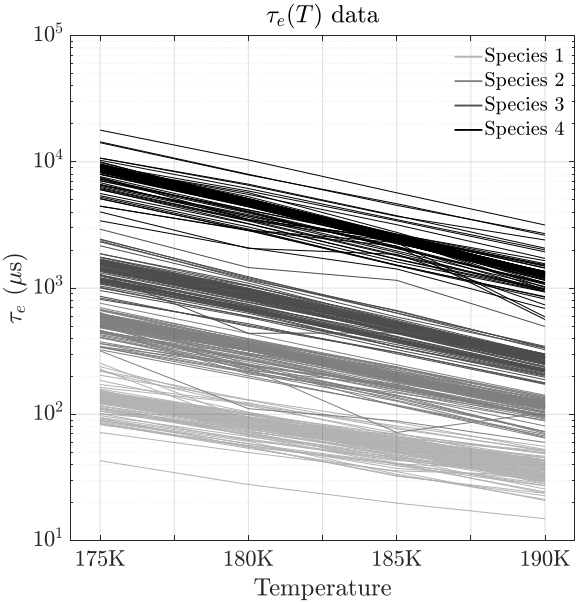


Figure 3.29 Emission time constant data plotted over temperature for randomly selected sample groups of 100 traps per species.

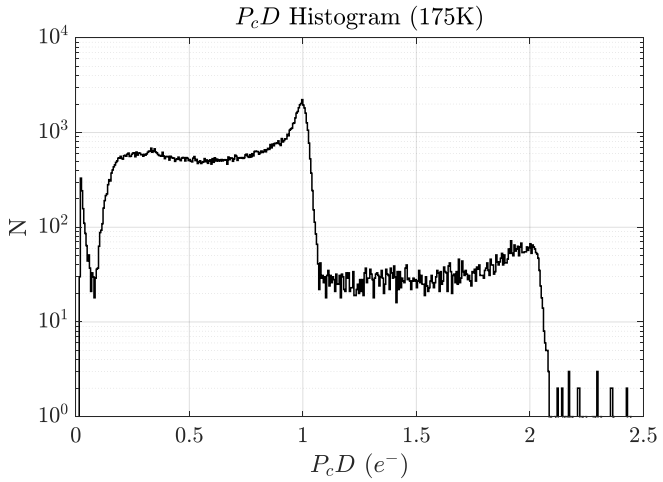


Figure 3.30 P_cD histogram measured at 175K.

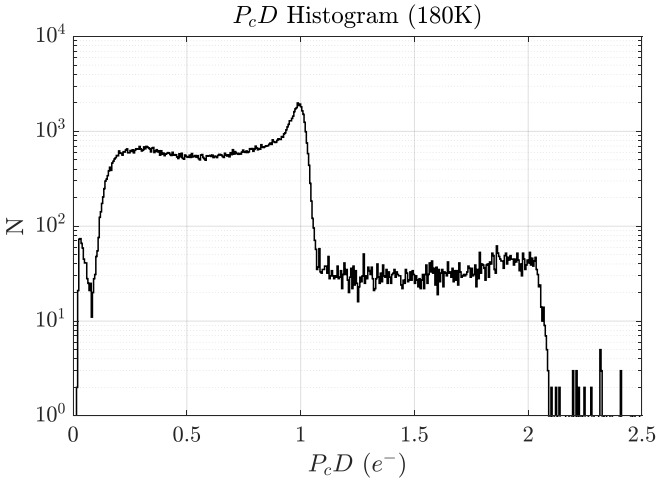


Figure 3.31 P_cD histogram measured at 180K.

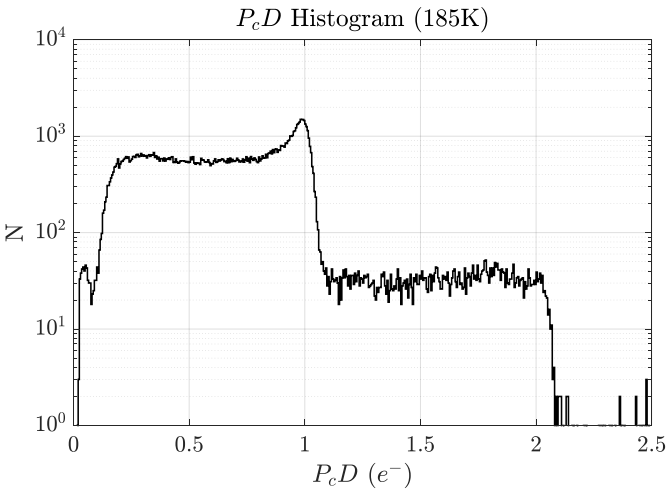


Figure 3.32 P_cD histogram measured at 185K.

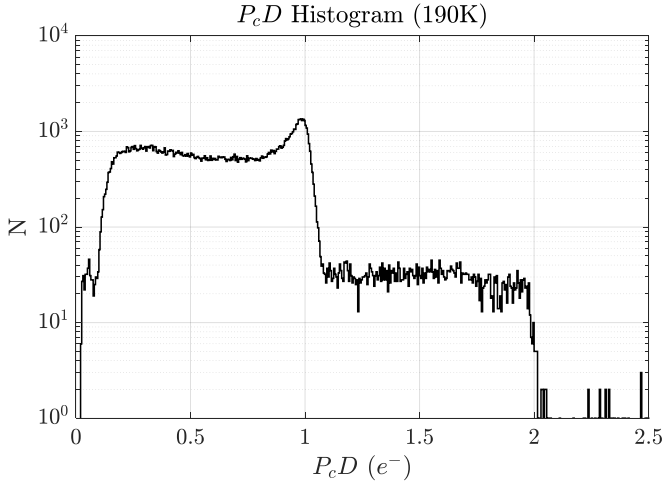


Figure 3.33 P_cD histogram measured at 190K.

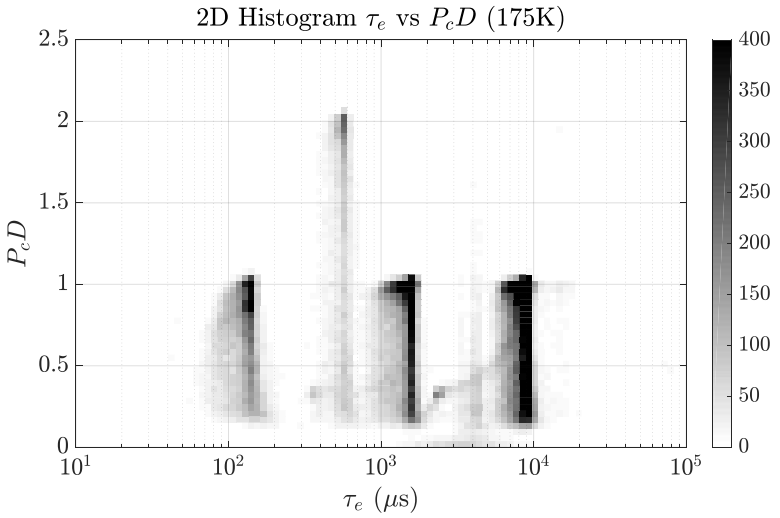


Figure 3.34 τ_e vs P_cD at 175K.

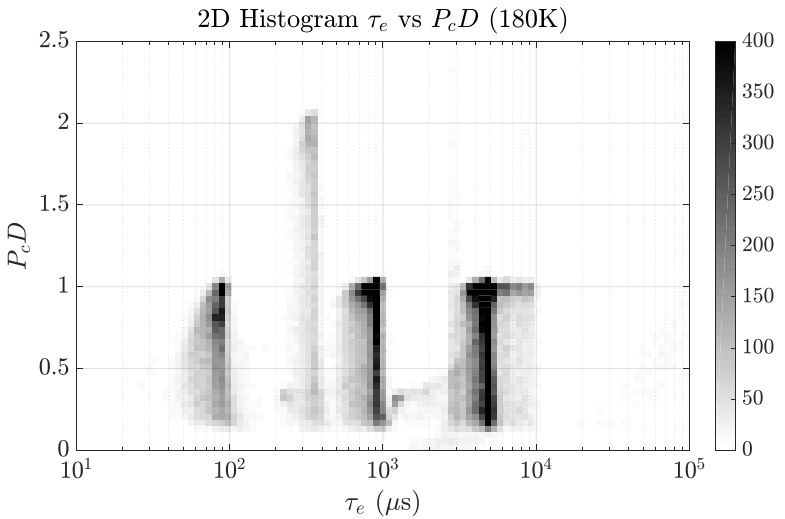


Figure 3.35 τ_e vs P_cD at 180K.

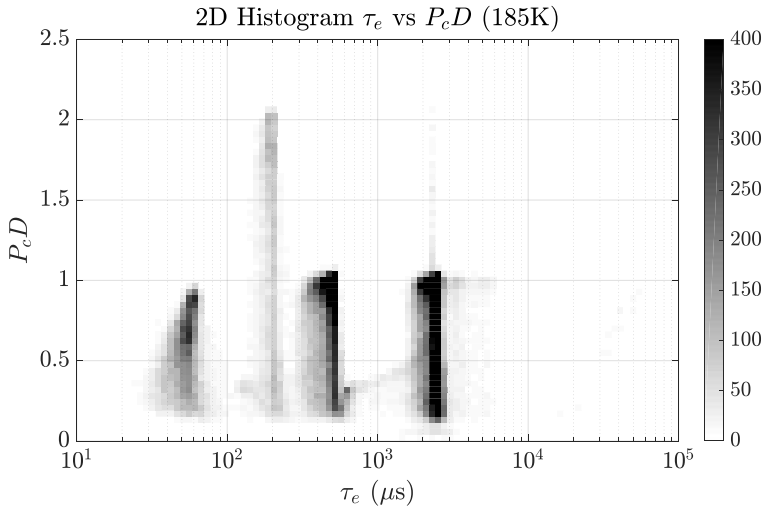


Figure 3.36 τ_e vs P_cD at 185K.

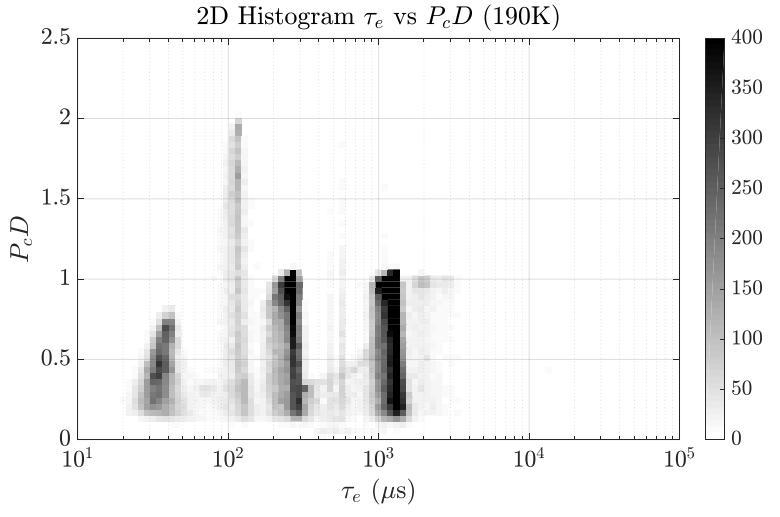


Figure 3.37 τ_e vs P_cD at 190K.

3.4.4 Trap parameters

Using equations (3.2) to (3.5) the trap characteristic parameters, σ (capture cross-sectional area in cm^2) and E_t (trap ionization energy in eV) can be determined by fitting to the profiles for $\tau_e(T)$ obtained experimentally. This information can then possibly be used to identify traps by type and composition, and then in turn predict trap behavior in other conditions or even determine the conditions required for annealing a certain trap species.

Due to trap mobility, not all traps remain in the same pixel location between pocket pumping experiments – no attempt was made to track these as this is not the case for the majority of traps (roughly 80%) which remain stationary. After identifying all stationary traps, $\tau_e(T)$ is fitted for every trap. Figure 3.29 shows the time constant variation with temperature by species.

Table 3.4 Identified species by trap parameters, E_t and σ.

Defect	E_t **(eV)**	σ **(cm²)**
Species 1	0.210	3×10^{-17}
Species 2	0.265	3.5×10^{-16}
Species 3	0.29	6×10^{-16}
Species 4	0.32	9×10^{-16}
(?) Species 5	0.27	2×10^{-17}

Figure 3.39 then shows the 2D histogram of σ and E_t. As expected, the four species delineate themselves into distinct groupings though looking at the data in terms of a single parameter would make it difficult to distinguish species. An interesting observation is that there is a possible fifth species observed with $E_t = 0.26$ and $\sigma = 2 \times 10^{-17} cm^2$. This becomes clearer when plotting histograms of the individual parameters by species in figures

3.40 and 3.41. The peaks of each species are clearly visible and are summarized in table 3.4. The possible fifth species is evidenced by a daughter peak in the histograms of species 4. This daughter peak was not distinguishable in the histogram distributions of τ_e yet it becomes visible in terms of energy and cross-section.

For a comparison of τ_e vs T curves based on these parameters, see figure 3.38. While these data are of the same orders of magnitude as those presented in recent literature, the precise energy levels and cross-sections do not seem to correspond identically to previously identified known defects. It is possible that there is some error introduced due to the actual temperature of the backside (photosensitive side) of the CCD not being accurately represented by the thermocouple sensor mounted on the rear of the detector package (which is also a possible error source for the reference data).

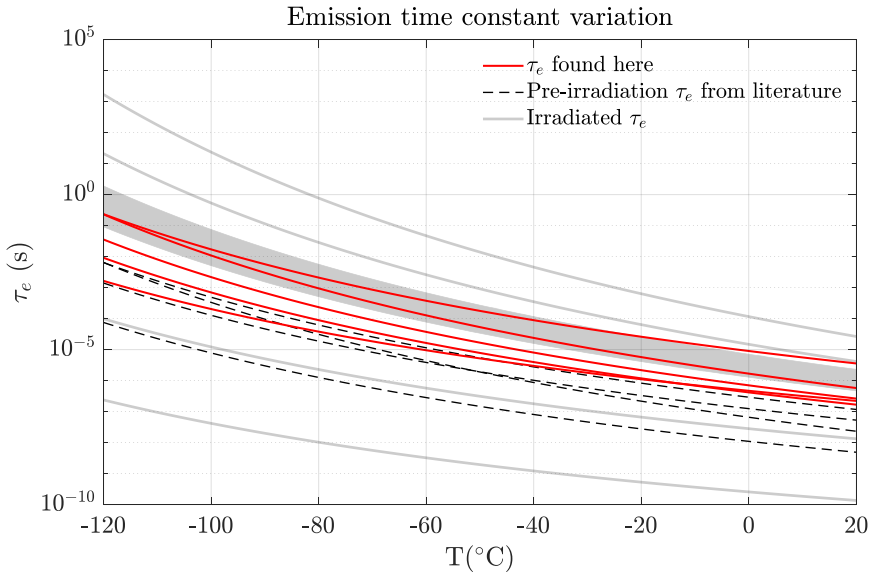


Figure 3.38 Predicted emission time constant variation over temperatures of interest (for all traps identified in comparison to traps identified in the literature).

CCD traps identified in the literature are summarized in table 3.5. It should be noted that the post-irradiation defects are not usually present (in any significant numbers) in a new device, both because the silicon is of a high grade, and the thermal processing during manufacturing subjects the silicon to temperatures that would anneal certain types of those defects. Of the pre-irradiation defects the B_iO_i trap stands out as having parameters close to those of species 2. In fact, in [29] we find that this defect has a double-donor energy level at 0.27 eV, in agreement with the trap depth analysis done earlier which also identifies species 2 as a double-donor defect.

As for the remaining species, these may be variant configurations of the C_iP_s defect as this defect is reported to have a range of energies of the same range as these species. Any specific attributions would be fairly speculative and so further experiments would be required to make accurate assignments to these defects.

3.4.5 Comparison of pumping schemes

Section 3.3.2 described a time-optimized scheme for the pocket pumping process which was used for all the results presented in this chapter. As a test for whether the new scheme is more efficient, pocket pumping results in the form of time constant histograms were compared for the old and new schemes, given the same amount of time spent in each experiment (10 hours for each pumping sub-scheme – 40 hours for each scheme). The results are shown in figures 3.42 and 3.43. The number of traps found in the new scheme was approximately 1.3×10^5 whereas that in the old scheme was approximately 1.04×10^5 – a 28.5% difference. It can be seen however that there is overall agreement in the time constant location of each species and also the time constant distribution in each species.

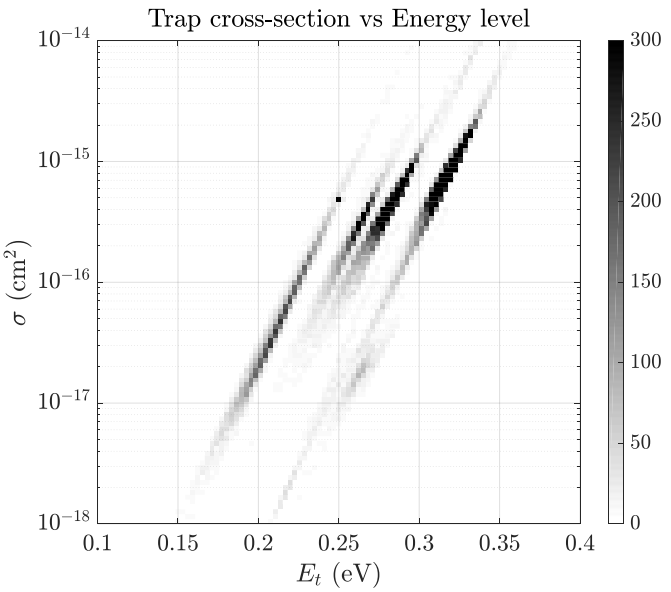


Figure 3.39 2D histogram of E_t and σ showing the four species and revealing a possible fifth species.

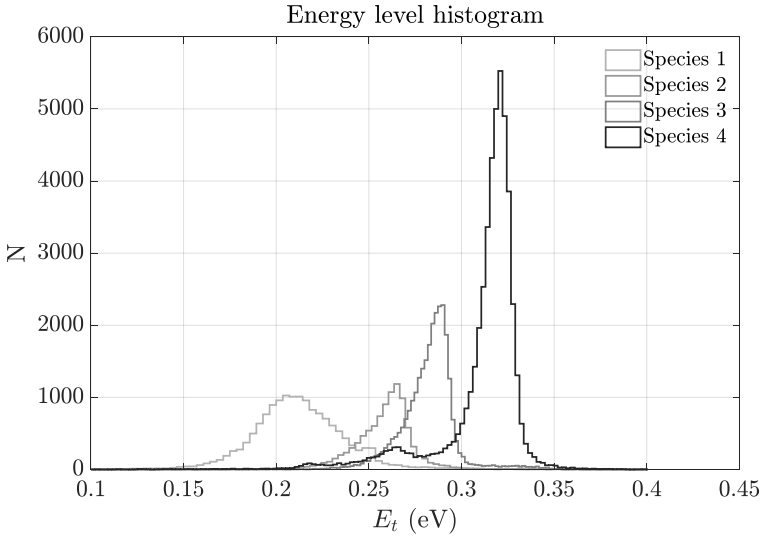


Figure 3.40 Histograms of E_t by trap species.

The main point is that the number of traps detected is greater over all species found (figure 3.42). The P_cD values of the additional traps uncovered using the new scheme can be seen in figure 3.43. This is expected since all traps in the new scheme are pumped to greater

dipole intensities and so traps with lower capture probabilities, P_c, become detectable whereas these remain undetected in the old scheme.

Table 3.5 Literature identified traps by parameters (E_t, σ) and source.

Defect	E_t **(eV)**	σ **(cm²)**	**Reference/notes**
C_iP_s	0.21	5×10^{-16}	[37] Pre-irradiation
No attribution	0.245	5×10^{-16}	
B_iO_i	0.265	5×10^{-16}	
C_iP_s (III)	0.23	3×10^{-15}	[6] Pre-irradiation
C_iP_s (IIB)	0.31	1.5×10^{-14}	
Si-E	0.46	5×10^{-15}	[11] Post-irradiation
$(V\text{-}V)^-$	0.39	2×10^{-15}	
No attribution	0.3 – 0.34	5×10^{-16}	
$(V\text{-}V)^{--}$	0.21	5×10^{-16}	
Si-A	0.17	1×10^{-14}	

A second point is that while the spread in time constants is similar in both schemes, the spread in P_cD is markedly different. This is also expected since the new scheme pumps traps to greater dipole intensities or greater signal to noise ratios which results in more accurate curve fits to the dipole intensity curves. Therefore, the capture probability is more accurately estimated in the new scheme.

It should be noted that the time taken for the experiment depends on the resolution and range of the phase-times tested which can vary between experiments and schemes. Thus, this test is a very rough approach to demonstrating the greater efficiency of the new scheme and a more thorough approach is warranted in the future. At the very least, there is more than satisfactory agreement of results between the two schemes.

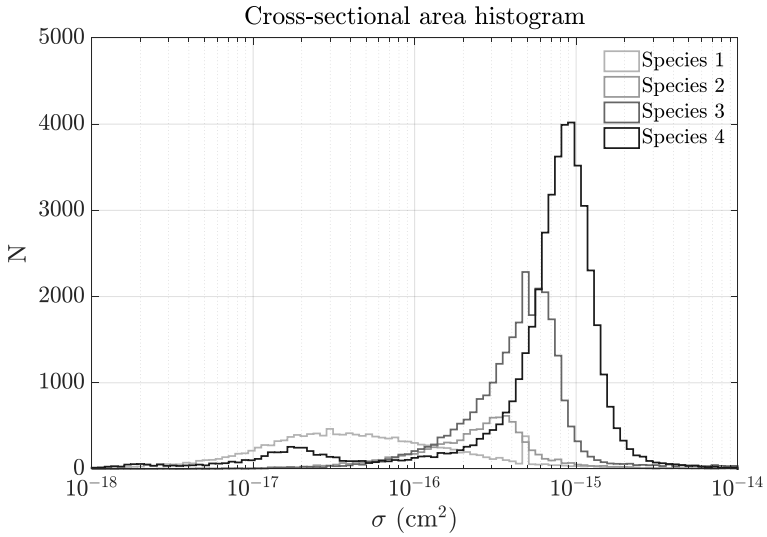


Figure 3.41 Histograms of σ by trap species.

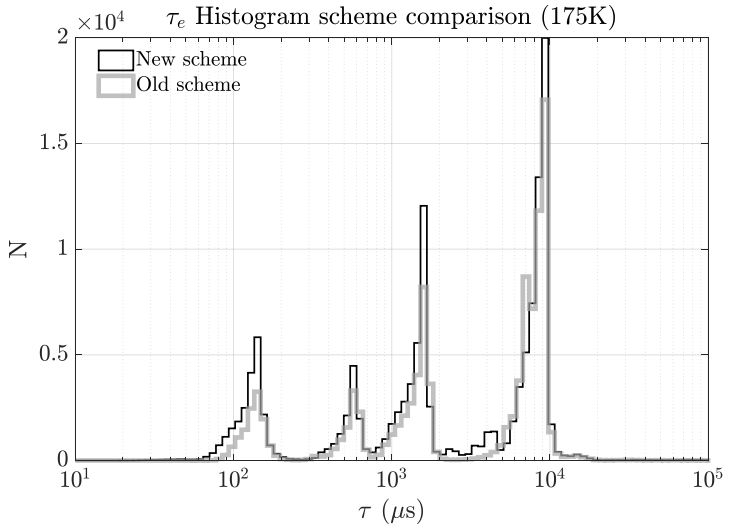


Figure 3.42 Emission time constant histogram comparison of old and new pumping schemes showing a greater number of traps detected across all species.

3.5 Summary

Buried channel silicon bulk traps in the image region of a new e2v CCD231-c6 four-phase sensor have been fully characterized using the pocket pumping method. To do this, an appropriate pumping scheme was found and additionally optimized for maximum

experiment time efficiency. The optimized scheme is shown in principle to take 2/3 the amount of time as the original scheme in order to acquire the same results. Given the same amount of time in a comparison of both schemes, it was demonstrated to identify 28% more traps and also give a more accurate estimation of the capture probability, P_c.

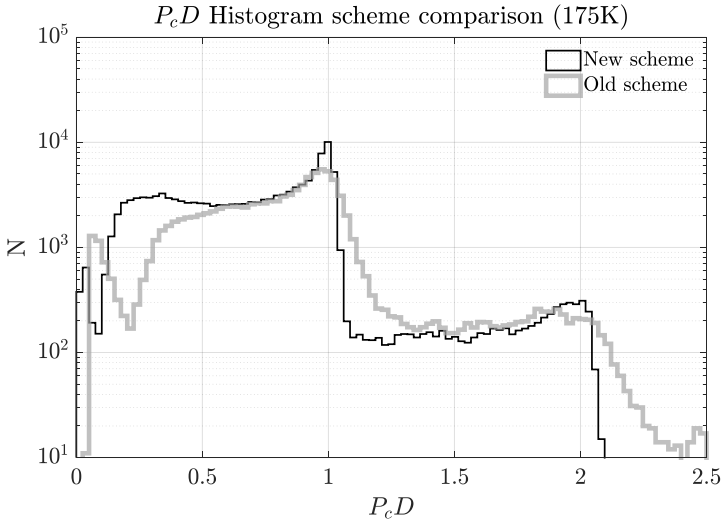


Figure 3.43 P_cD histogram comparison of old and new pumping schemes showing the increase in the detected number of low P_c traps.

Four traps species populations have been identified and their emission time constants measured at four different temperatures. The emission time scales range between 0.1 to 10ms at a temperature of 175K and 0.01 to 1ms at a temperature of 190K. Just under half of all traps are represented by the species with the largest emission time constant while the remaining three species represent a share of 10 – 30% each. The same species distribution of traps was found in all regions of a pixel in the CCD although there was variation observed in the *total* number of traps depending on region of the pixel.

The capture probability multiplied by trap depth (P_cD) has also been measured for all traps. P_cD is always less than 2 and its distribution shows discontinuities at $P_cD = 1$ and

2, indicating that all traps capture at most, $2e^-$. In fact, it was found that only one trap species has a trap depth of $2e^-$ (a double-donor type defect) and is the species least represented among all the traps. Additionally, it was found that the majority of traps have a capture probability of 1 at the signal level tested ($35000e^-$) and this was shown to be expected, according to previous analysis on charge density as a function of position in the charge cloud.

Trap assisted recombination theory allows for the calculation of defect parameters in terms of mid-band energy level and capture cross sectional area. Traps can then be matched on the basis of these parameters to defects in the literature with known atomic configurations. All traps were found to have mid-band energies of $0.21 - 0.32$ eV below the conduction band and capture cross-sectional areas of $10^{-17} - 10^{-15}$ cm^2. Comparing to reference data, it was shown that the double-donor species corresponds well to the boron-interstitial-oxygen-interstitial (B_iO_i) defect while the others were tentatively presumed to be variations of the carbon-interstitial-phosphorus-substitution (C_iP_s) defect.

4 Trap mitigation: Concurrent multilevel clocking

In the previous chapter, bulk silicon lattice traps in the signal channel were located and fully characterized. In this chapter it is shown that precisely measured CTI matches the measured trap populations, thereby showing that the bulk traps identified are indeed the source of CTI. Techniques are presented to accurately measure CTI/deferred charge with only the use of a flat field illumination light source. It is shown that these techniques cannot only substitute for Fe^{55} CTI measurements but are in fact more comprehensive, efficient, and versatile in revealing the charge transfer performance of a CCD in the multidimensional parameter space of temperature, line transfer time, and signal level.

Results from these techniques are presented for parallel charge transfer performance as functions of these parameters. Further, CTI reducing clocking techniques are described and then experimentally demonstrated by comparing deferred charge results to the conventional clocking scheme for many parameter combinations inside the parameter space. Finally, it is shown that mean deferred charge can be predicted from the mean trap population distributions, trap properties and number of transfers for any parameter combination by using a simple Monte Carlo method of simulating trap capture and emission.

4.1 Introduction

4.1.1 Conventional CTI mitigation

In order to combat the effects of bulk trapping CTI, several approaches can be taken. They can be categorized into three types: those that avoid trapping, those that boost charge recovery, and those that correct images affected by charge trapping.

1. Trap avoidance

a) *Pre-flash/Charge injection*: In the first category there are two ways to prevent charge trapping: the first is to 'satiate' the traps by pre-filling them prior to exposure (and then readout). In this method, traps may be pre-filled either optically or electronically. In the optical method, a simple flat-field source is used to introduce a "Fat-zero" signal. This was done for example in the case of WF/PC 1 on the Hubble Space Telescope. In the electrical method, Fat-zero is introduced electrically through the process of charge injection. This works by correctly setting the output drain potentials such that charge is injected under the OTG and SW. This charge can then be sent anywhere in the chip by clocking appropriately and the entire CCD can be filled with charge if desired. A disadvantage of this method however is that Fat-zero is accompanied by shot noise which adds to the read noise floor. Further, this method is only effective against process and design traps since bulk and radiation traps are spread evenly through the bulk channel and it would require more charge than the full well capacity to fill all of them.

b) *Notched channel*: The second way to prevent charge trapping is to introduce a notch in the potential well to concentrate charge in the center of the channel. This decreases the probability of encountering traps during charge transfer. The notch is created by injecting a narrow dopant implant (typically phosphorus) under the gate oxide. A small notch on the order of a few V is created which then confines the path of small charge packets so that they do not encounter as many traps.

2. Image correction

With good enough understanding of how traps behave it is possible to reassemble images with signal trails resulting from trapping. Several models have been developed using this approach such as in [5], [24], and [36] where CTI is *added* to estimates of the true sky images and then compared to the actual data images. This is iterated until the actual data images can be reproduced by applying CTI models to the true sky image estimate. For the example of HST, early models achieved a 90% correction for signal trails – this has improved now to the level of 98% correction. Still however, increasingly stringent astrometry requirements necessitate further corrections, particularly at the low signal levels where the CTI models are less accurate.

3. Improving charge recovery

Trapped charge is released shortly after trapping according to the trap emission time constant. Recovery is achieved if emission occurs into the originating packet – the lower the emission time constant relative to the readout speed, the higher the chance of recovery. Methods to boost recovery are therefore to (a) decrease readout speed, (b) increase temperature (thereby decreasing emission time constants), and (c) shape the

gate potentials to direct de-trapped charge to rejoin the originating packet as is done for example in [27]. There are obvious costs to both (a) and (b) which warrants careful optimization with knowledge of trap parameters. On the other hand, (c) is essentially free with no adverse impact on CCD performance. This chapter deals with these methods of CTI mitigation.

4.1.2 CTI measurement

X-ray transfer

The transfer of x-ray events across the CCD is the standard most widely accepted method of measuring the quality of charge transfer as it is considered to be the method that is least susceptible to spurious results. The x-ray photons are typically generated via electron capture using Iron-55 (^{55}Fe, a radioactive isotope) which has a half-life of 2.74 years. An x-ray photon generates a signal of 1620e$^-$ (at room temperature) in silicon which manifests as a single pixel event in the CCD array. To measure horizontal CTE a signal vs horizontal pixel scatter plot is produced where the single pixel event line separates itself from the read noise floor with a scattering of pixel sub-events filling the space in between. CTI is then,

$$\mathrm{CTI}_{\mathrm{X-ray}} = S_D \,/\, (X \cdot N_P) \tag{4.1}$$

where S_D is the total deferred signal in e$^-$, X is the x-ray signal (1620e$^-$ for a ^{55}Fe source) and N_P is the total number of pixel transfers. The same procedure can then be used to measure parallel CTI by using the scatter plot of signal vs vertical pixel instead.

Extended Pixel Edge Response (EPER)

The EPER method is a popular and simple technique that estimates S_D in equation (4.1) by summing the signal appearing in the immediate extended or over-scan pixels after the image pixels are read. This requires only a flat-field illumination source and is the technique used in this chapter. Both horizontal and vertical CTI can be measured by recording extended pixel signals in each direction by equation (4.2),

$$\mathrm{CTI}_{\mathrm{EPER}} = S_D \,/\, (S \cdot N_P) \tag{4.2}$$

where S is the flat field signal in e^-. The challenge in this technique is that length and size of the deferred charge tail depends on the readout speed, CCD temperature, signal strength, and trap emission time constants. Because of these variables, EPER has traditionally been dismissed as merely a relative CTE measurement technique until even recently, as shown in [43]. It will be argued in this chapter, however, that EPER can, in fact, give more robust and complete measurements if done correctly. Further, because ^{55}Fe measurements are expensive, time consuming and yield an incomplete view of charge transfer performance, the EPER techniques presented herein will be far more preferable in many applications due to their expediency and low cost.

First Pixel Edge Response (FPER)

FPER measurements follows the same experimental arrangement as EPER. The idea is that charge traps are filled by the first line of charge to pass over them and total deferred charge may be estimated by the amount of charge missing from the first line of signal. This test is restricted to CCDs with split control of the upper and lower halves of the image area. To make the measurement, one begins with a half illuminated CCD by

dumping half of an entire flat field. The remaining half is then read out through the empty region with the first line filling all traps in its path. Deferred charge is then the amount of lost charge in the first row of pixels of the image. CTI is once again defined as in equation (4.2).

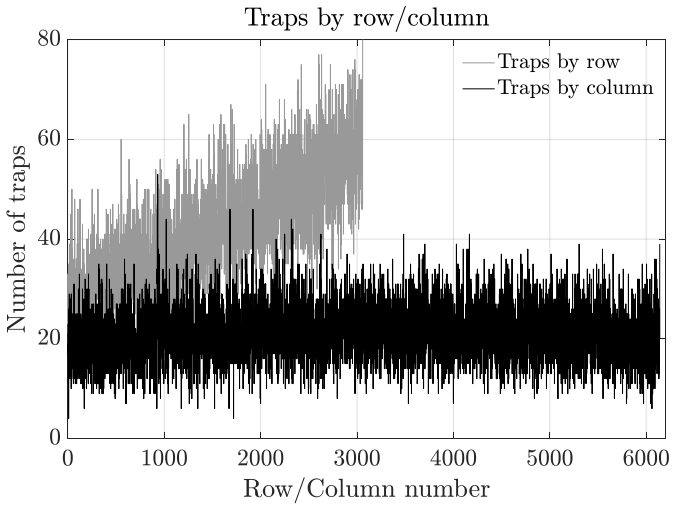


Figure 4.1 Number of traps seen by a signal of $3.5 \times 10^4 e^-$ by row and column.

4.2 CTI measurement results

4.2.1 Extended Pixel Edge Response (EPER)

Given its simplicity, the EPER method was used to measure vertical deferred charge due to bulk traps identified in chapter 3. As shown in figure 3.16 there is a variation in the number of traps over the CCD which may point to a variation in the EPER signal depending on column. However, when plotting figure 3.16 by row and column in figure 4.1 we can see that all variation is manifested in the vertical direction (across rows) and the mean number of traps per column remains constant. In fact, the mean number of traps seen per column is approximately 20. According to figure 3.22, two of these (10%) will be

of the double-acceptor type, resulting in an expected total deferred charge of 22 electrons or 3.86 DN which is comparable to the detector read noise (around 2.1 DN or 12e$^-$). Measuring the deferred charge of a single column at the level of 0.5e$^-$ to a 5σ accuracy would then require 120 EPER measurements or frames with extended pixels. To determine the deferred charge behavior over the entire parameter space, this presents a challenge since each frame requires time to readout the full detector with the addition of the necessary number of extended pixels.

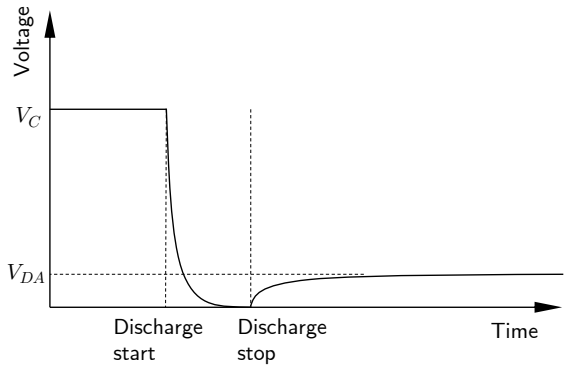


Figure 4.2 Residual voltage, V_{DA} on a capacitor resulting from dielectrically absorbed charge.

4.2.2 Methods to accelerate EPER measurement

The measurement can be expedited by two techniques. The first is to collapse EPER signals over many columns in a single frame. Figure 4.1 shows that we may consider column-wise EPER as a random variable with a mean and standard deviation of 22e$^-$ and 6.3e$^-$ respectively. What is the 5σ detection limit of deferred charge, D_L, when binning m EPER pixels in a row? We have that,

$$\frac{D_L \cdot m}{6.3\sqrt{m} + 12} = 5$$

So $D_L = 0.5\text{e}^-$ for $m = 4200$ pixels which is less than the available 6144 columns in the CCD.

We may do better using an additional technique which allows for many EPER measurements in a single frame rather than having to acquire many frames. In CCDs with a split image area it is possible to illuminate the detector and dump half the charge while retaining the other half; this is illustrated in figure 4.3. From this point, it is possible to operate the top half of the chip to push a line of charge (or any number of lines) into the lower half of the chip, at which point the lower half resumes clocking downward with the top half remaining stationary. In this way, lines of charge can be spaced by enough rows for an EPER tail so that many tails can be read in a single frame (figure 4.3). Supposing that n EPER tails are generated in a single frame, the SNR equation then becomes,

$$\frac{D_L \cdot m \cdot n}{(6.3\sqrt{m} + 12) \cdot \sqrt{n}} = 5$$

D_L is then 0.08e^- for $m = 4200$ and $n = 40$. Thus by this method, deferred charge can be measured to a great degree of accuracy from a single frame and an example of such a measurement is shown in in figure 4.4. Such a measurement is obtained in the span of a minute (or however long is required to read out two frames at the line timing being considered).

Certain challenges were faced when making such measurements, however, and they are described as follows.

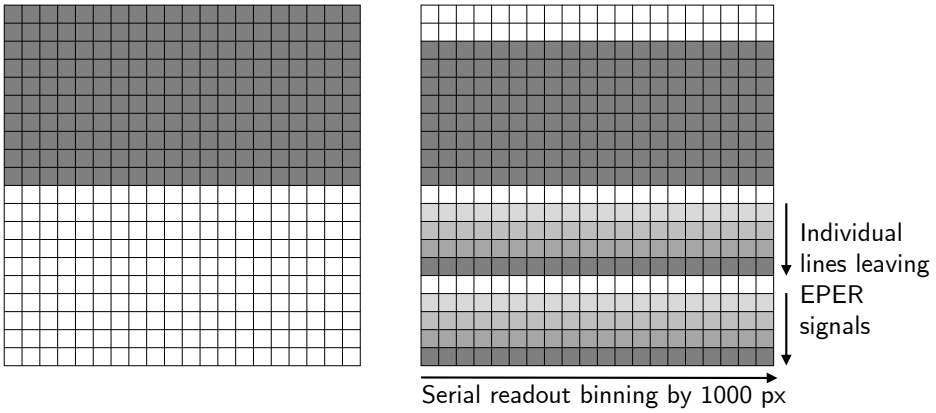


Figure 4.3 Deferred charge measurement technique. (Left) Flat-field illuminated CCD with half the chip emptied. (Right) Lines are clocked from the top half into the bottom half at regular intervals, leaving individual EPER tails.

Dielectric absorption

Measuring a small signal such as the deferred charge immediately after reading large image pixel signals in the aforementioned method is challenging not only because binning image pixels would cause blooming but also because of dielectric absorption. This is a sort of remnant or memory effect in capacitors. When the sense node capacitor is loaded with charge, molecular dipoles inside the dielectric material in the capacitor become polarized, thereby storing energy in the dielectric material. Upon discharge, these molecular dipoles do not immediately completely resume random orientation but do so over some period of time. Thus the capacitor develops a 'residual' voltage (figure 4.2) even after complete discharge. This is due to the gradual (random) re-orientation of the molecular dipoles that pulls charge onto the capacitor plates to neutralize the resultant voltage change.

This charge release will interfere with deferred charge measurements if it is significant, as is the case after measuring large signal pixels. The way to mitigate this is to avoid reading signal pixels (by dumping the signal lines) since for deferred charge, it is the tail that is of

interest. This of course implies that one may only observe either the signal or the deferred charge, but since mean values are being considered these are not expected to change frame to frame.

Photo-luminescence (Phosphorescence/Fluorescence)

At the level of the deferred charge, all spurious sources of small signals become important to account for. After dark current and light leak are under control, an often overlooked effect is photo-luminescence – delayed photon emission after photo-excitation. Post illumination of the CCD, if there are any photo-luminescent materials in the vicinity, their emission will be superimposed on the deferred charge tails, thereby giving the impression of very poor charge transfer performance due to the large charge tails observed.

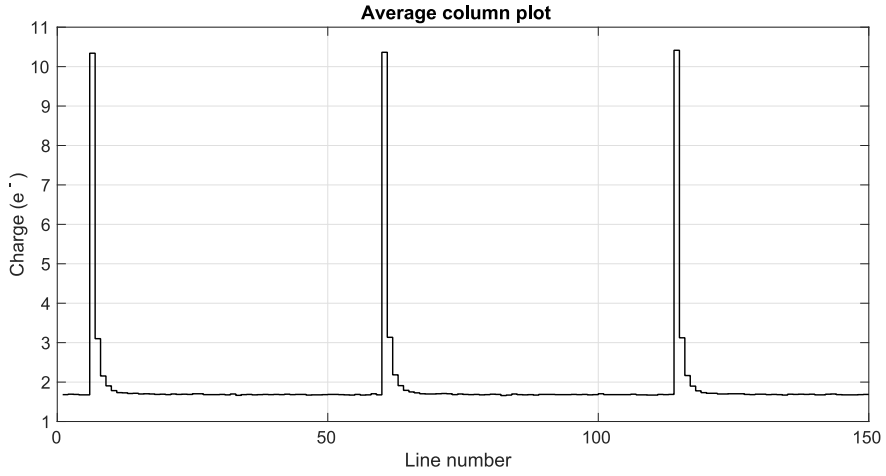


Figure 4.4 Sample deferred charge tails measured by binning and averaging. The signal used was $3.5 \times 10^4 e^-$ and the signal pixels were dumped during readout. Total deferred charge is calculated by summing all pixels comprising the tail.

This was a major source of confusion in the experiments detailed here because luminescence is also an exponentially decaying process of internal energy transitions (like charge trap

emission) – it will act to introduce charge trails after illumination in the same way as bulk traps. Distinguishing the two is not straightforward — it was only discovered by noting that there were no traps in the CCD with time constants on the order of what was necessary to be observing the large charge tails measured. When a delay was introduced after illumination the charge tails were dramatically shortened, indicating some source of photo-luminescence. This delay time was increased until the charge tails were relatively constant (approximately 120s), indicating that the photo-luminescence had died out to insignificant levels before the readout process.

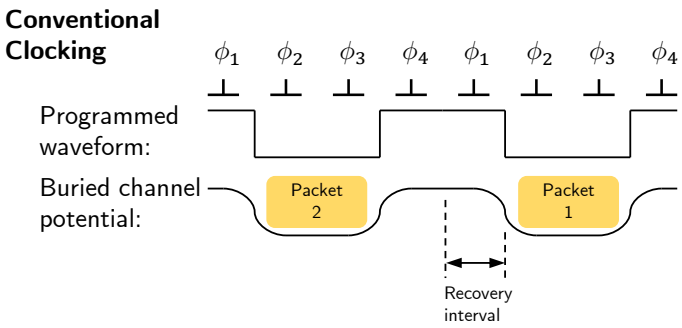


Figure 4.5 Two-phase storage parallel line transfer indicating recovery interval for de-trapped charge. Charge is recovered if emitted shortly after the phase goes into barrier mode.

4.2.3 CTI vs Line transfer time

The primary factor influencing charge transfer efficiency is the readout speed (line time). This is because trapped charge is recovered to the extent that packets are transferred slowly from phase to phase. As shown in figure 4.5, trapped charge that emits under a barrier phase immediately after the charge packet has passed will roll down the potential well and be recovered by the originating charge packet. This is due to the natural slope of the buried channel potential field. The recovery time interval is directly related to the

total line transfer time so that reading slower will boost the charge transfer efficiency. This process of charge recovery also depends on the serial register readout rate for reasons that are explained in section 4.5.

This readout rate affects not only the total deferred charge but also the length of the deferred charge tail – the greater the pixel rate, the more pixels the tail will be spread over. If spread over too large a number of pixels, the SNR of each pixel in the tail can become low. For this reason, EPER has traditionally been seen as prone to yield ambiguous results. However, as is shown in later sections, if the emission time constant landscape is known, the readout speed can be appropriately set. In this way the deferred charge tail can be confined to few enough pixels to maintain very high SNR, thereby yielding highly accurate deferred charge estimates.

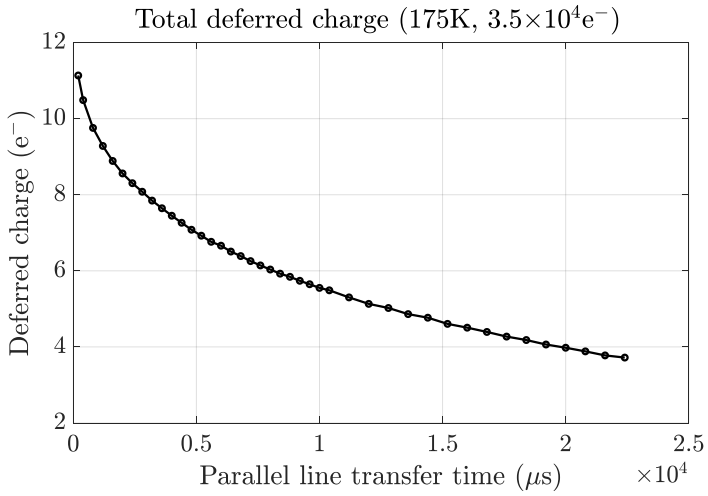


Figure 4.6 Measured deferred charge as a function of parallel line transfer time.

Figure 4.6 shows the variation of deferred charge with increasing parallel line transfer time at a signal level of 3.5×10^4e- and a temperature of 175K (higher temperatures are considered in section 4.2.5). The serial pixel rate was held constant at 1.22µs per pixel

while signal was binned serially by 1000px giving a total serial register readout time of 9760µs (8 binned pixels per row). Parallel line transfer times of 200µs to approximately 22ms were tested with a varying increment size to resolve the trend features.

It is seen that deferred charge decreases with line time exponentially. From figure 3.24 we know that almost all traps have emission time constants below 10ms so that with an approximately 10ms total line time, most traps will have released recovered charge or have emitted within the first extended pixel. Therefore, as total line time drops below 10ms, we would expect to see an uptick in the amount of deferred charge; this is confirmed in figure 4.6 by the large slope seen at the lowest *total* line times (including serial transfer time) tested (around 10ms). Since enough pixels were required for the column averaging, total line times less than 10ms could not be tested.

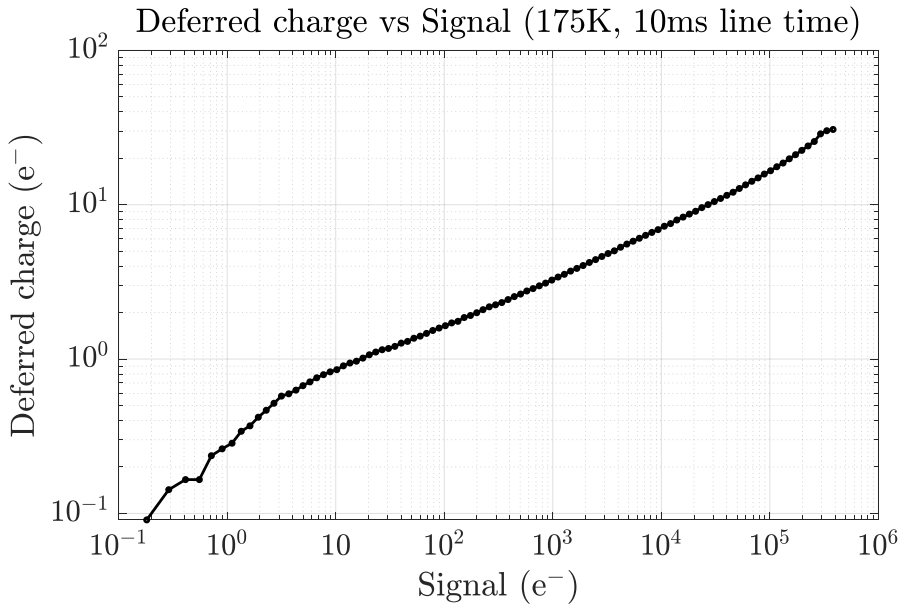


Figure 4.7 Measured deferred charge as a function of transferred charge packet size (signal).

Realistic line times for this CCD format are approximately 3ms for which deferred charge would be much higher. Nonetheless, at 10ms, half of all 22e$^-$ of trapped charge is deferred (11e$^-$). Conversely, at 32ms, this drops to below 4e$^-$ – a 65% reduction. Further increasing line time will see diminishing returns as the trend suggests.

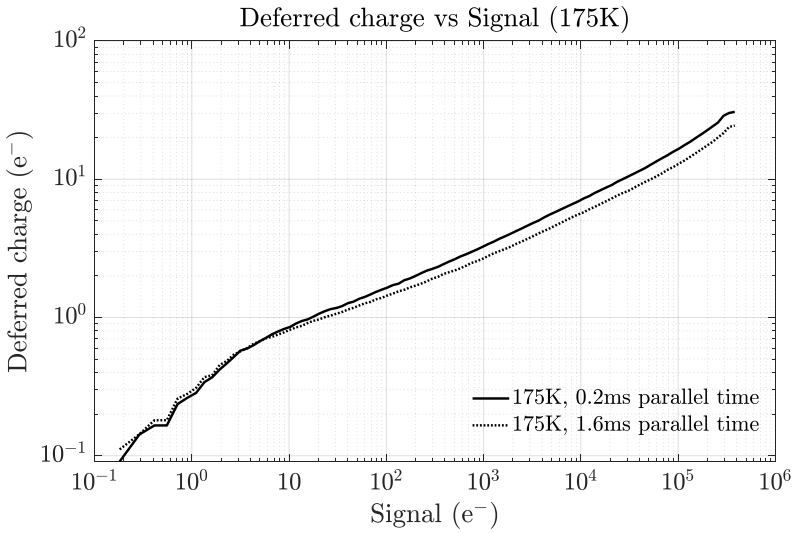


Figure 4.8 Measured deferred charge as a function of signal at two line times of 0.2ms and 1.6ms.

4.2.4 CTI vs Signal level

CTI also varies with signal packet size for the simple reason that the larger the size of the packet, the larger its cross-sectional area and hence, the more traps it is likely to encounter in the channel. This effect is well known and is being studied increasingly extensively (for example in the Euclid and Gaia missions) in the context of CTI modeling such as in [38] incorporating TCAD simulations (usually using the Silvaco software suite). Analytical models for the charge cloud size and density distribution are also being pursued for example in [30] although this requires intimate knowledge of the CCD architecture and implant profiles to be accurate [33]. These parameters are important in measuring CCD CTI,

however, since they govern the probability of charge capture for any given trap and in turn, the total deferred charge.

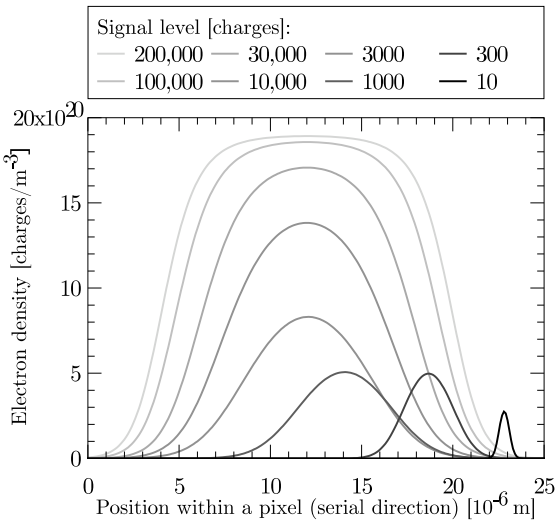


Figure 4.9 Charge packet density variation along the length of a pixel from analytical calculations presented in [30].

Figure 4.7 shows the total deferred charge measured over the dynamic range of the CCD at 175K. As explained in 4.2.1, the signal and deferred charge may not be observed in the same frame due to dielectric absorption. The flux from the light source was therefore measured beforehand to determine the conversion from exposure time to photons received (figure 4.10). The total deferred charge with respect to signal seems to follow a power law with a slope of approximately 0.32. The trend breaks down at the lower signals since the capture probabilities for low signal packets come to the fore. The well behaved region is in the range of $10e^-$ to $100{,}000e^-$ where the deferred charge varies from $1e^-$ to around $16e^-$. This small variation in deferred charge for such a large signal range highlights the fact that as the charge cloud grows in total charge contained, the volume and cross sectional

area do not increase as would be expected for a *fixed density* charge cloud. This is confirmed by analytical calculations in [30] and reproduced here in figure 4.9.

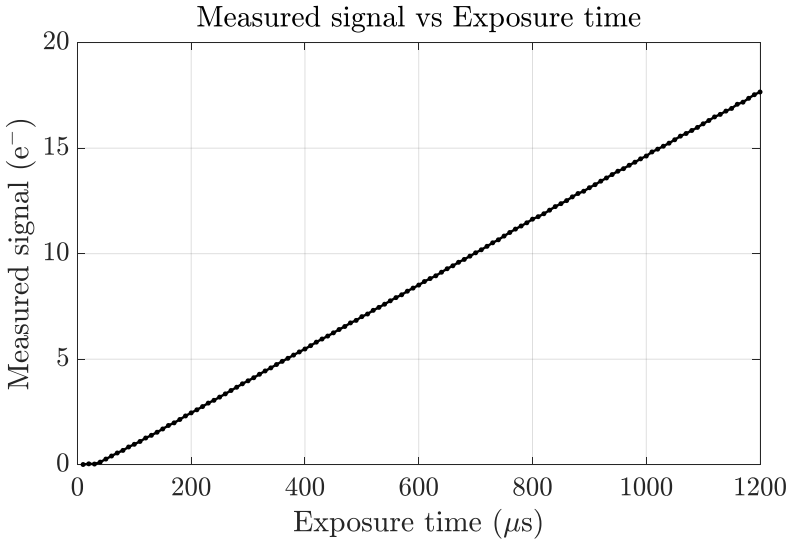


Figure 4.10 Mean signal per pixel vs exposure time for calibrating the illumination source.

Considering deferred charge in both dimensions of line transfer time and signal size we find the trend shift observed in figure 4.8. The effect appears to be that the slope of the power law is simply decreased for increasing line time (0.29 for a parallel line transfer time of 1.6ms as opposed to 0.32 for 0.2ms). The effect of temperature on these curves are explored in 4.2.5 but it is already clear that the effect on CTI by these parameters can be modelled quite simply to provide a quick method of predicting CTE changes with operating conditions.

Figure 4.11 reproduces the data from figure 4.7 in terms of CTI using equation (4.2). Also indicated is the expected CTI result from an Iron-55 measurement — the value that would be quoted by a CCD manufacturer when quoting specifying transfer performance. The EPER data indicates that ^{55}Fe measurements would yield a CTI of around 8×10^{-7} which

is close to the 10^{-6} measurement by e2v. The two figures are consistent, considering that slow line times were used for the EPER measurements. The data shows, however, that CTI can vary by at least four orders of magnitude over the CCD dynamic range. This, coupled with the fact that the slope of this curve is dependent on line rate, shows that CTE performance comparisons between devices on the basis of Iron-55 CTE measurements may not be the same (or even hold true) for much higher or lower signals than that generated by ^{55}Fe x-rays (1620e$^-$).

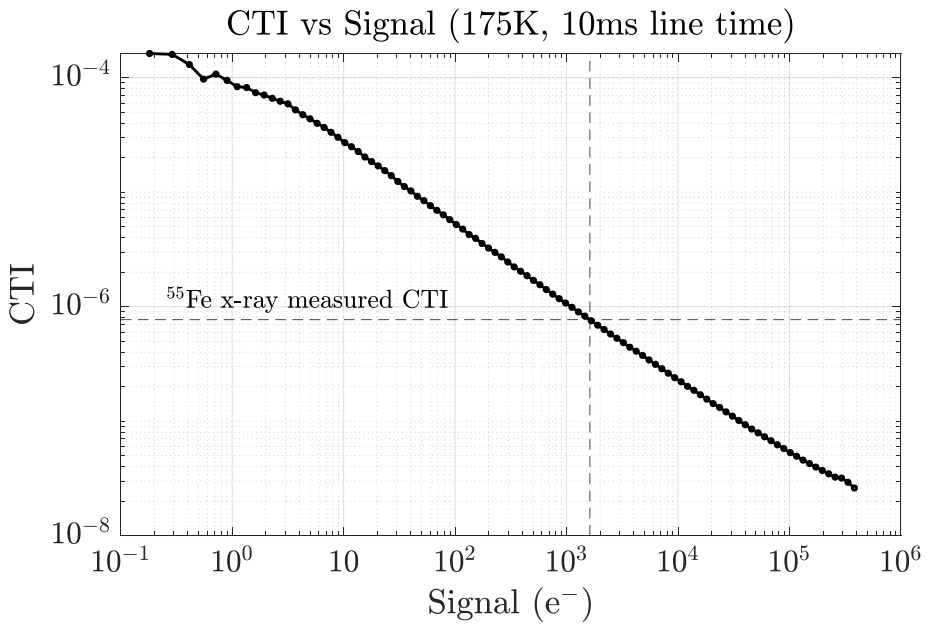


Figure 4.11 Figure 4.7 presented in terms of CTI with the expected Fe^{55} result indicated by crosshairs.

4.2.5 CTI vs Temperature

Increasing temperature accelerates trap emission, thereby improving charge transfer by boosting recovered charge. Figure 4.12 shows the improvement of total deferred charge vs parallel line time with temperature increments of 5K. The reduction in deferred charge is maximized at different line times depending on which temperatures are being compared;

this is due to the relative positions of the emission time constants at each temperature. Figure 4.13 shows the data of figure 4.7 taken at the same temperatures as before. On the log scale it seems the effect of temperature is to offset the curves in the vertical direction (in contrast to the effect of line time). Understanding each of these effects is important to building a model for CTI in order to efficiently optimize CCD timing.

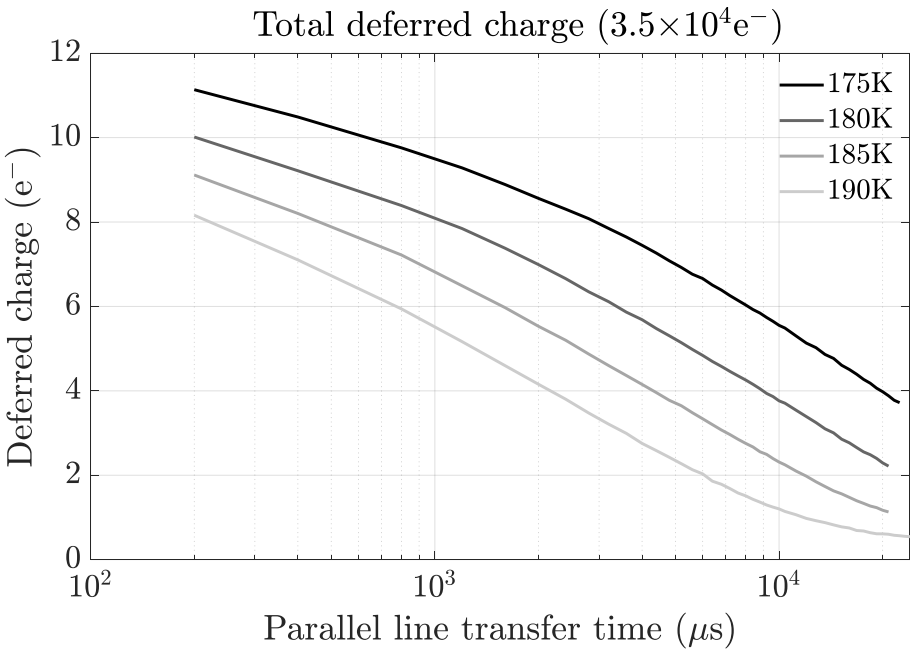


Figure 4.12 Extension of figure 4.6 to different temperatures.

Although increasing temperature improves charge recovery by reducing emission time constants, it also increases the rate of dark signal production (dark current), since dark current is essentially thermal generation of minority carriers from various places throughout the CCD. In [19] we find an empirical expression combining the contributions of the various sources of dark current as follows:

$$D_R = CT^{1.5} \exp\left(\frac{E_g}{2k_B T}\right) \tag{4.3}$$

Here, D_R is the mean dark current in $e^-/s/px$, C is a constant and E_g is the silicon bandgap energy (eV) which is temperature dependent as shown in [25] and given by,

$$E_g = 1.1557 - \frac{7.021 \times 10^{-4} \cdot T^2}{1108 + T}$$

The constant C can be solved for by measuring dark current at room temperature. Once an empirical model is made describing CTI vs temperature using data such as in figures 4.12 and 4.13, this can be combined with equation (4.3) to establish a figure of merit to be optimized.

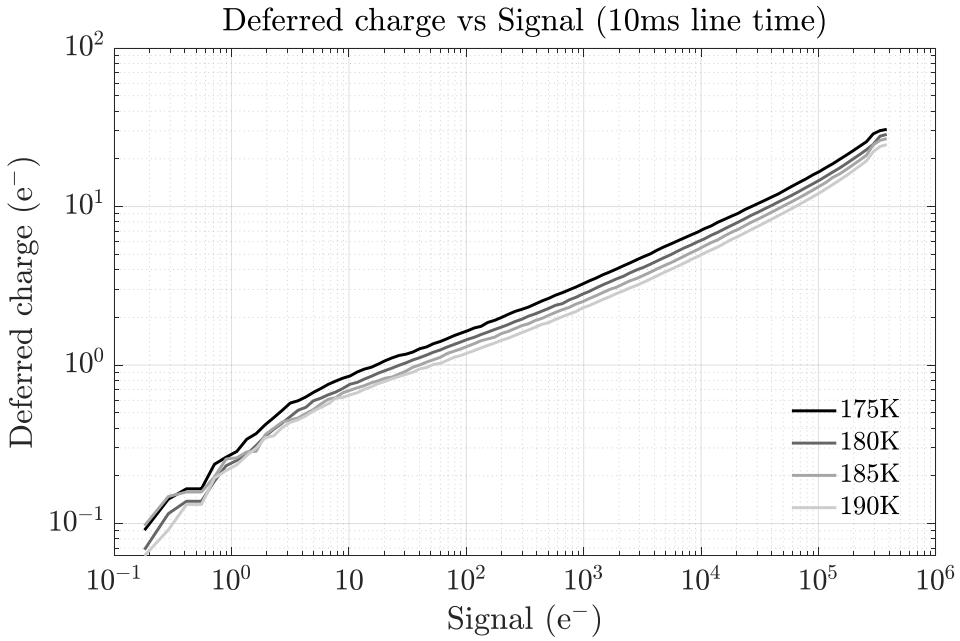


Figure 4.13 Extension of figure 4.7 to different temperatures.

4.2.6 Very low signal CTI

As mentioned earlier the CTI power law trend breaks down at very low signals according to figure 4.11. To resolve this region of the curve, many measurements were taken in the same fashion as before and the signal pixels were measured directly (as opposed to being inferred from exposure time) since a) in the low signal regime, signal is given by measured

signal + deferred charge; measured signal will not be proportional to exposure time because deferred charge is not proportional to exposure time, and b) the signal of interest is small enough to not cause any significant dielectric absorption.

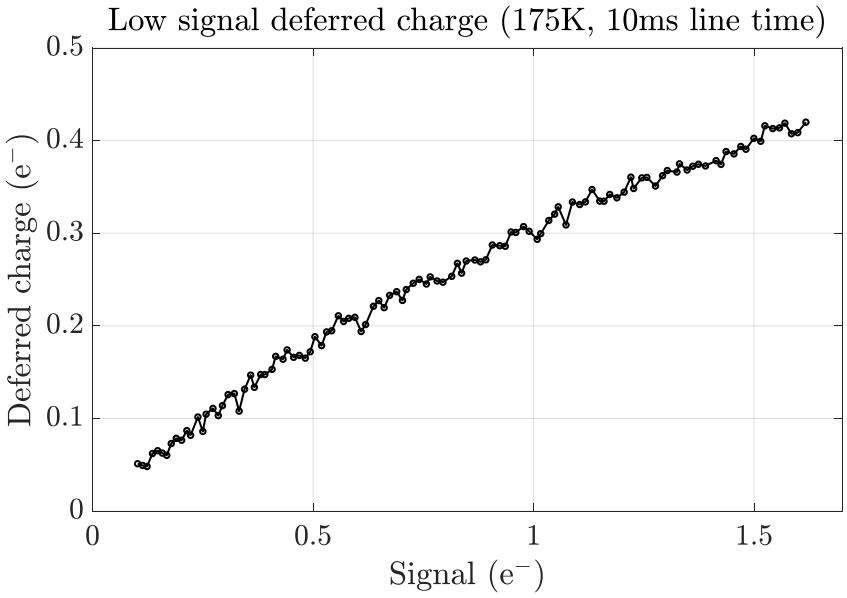


Figure 4.14 Mean deferred charge per pixel vs mean charge packet size transferred.

The result is shown in figure 4.14. In this figure the horizontal axis represents the mean measured signal and the vertical, the mean deferred charge. The original signal before the 3080 transfers is therefore the sum of these two. For a mean measured signal of 0.75e$^-$ the deferred charge is 0.25e$^-$ indicating that a single electron traversing 3080 rows has a ¼ probability of being lost at a line rate of 10ms. This probability will of course be higher for faster line transfer times. This result in itself has ramifications for photon counting applications, especially so in space where it is indicative of the best case beginning-of-life charge transfer performance of a photon counting CCD camera.

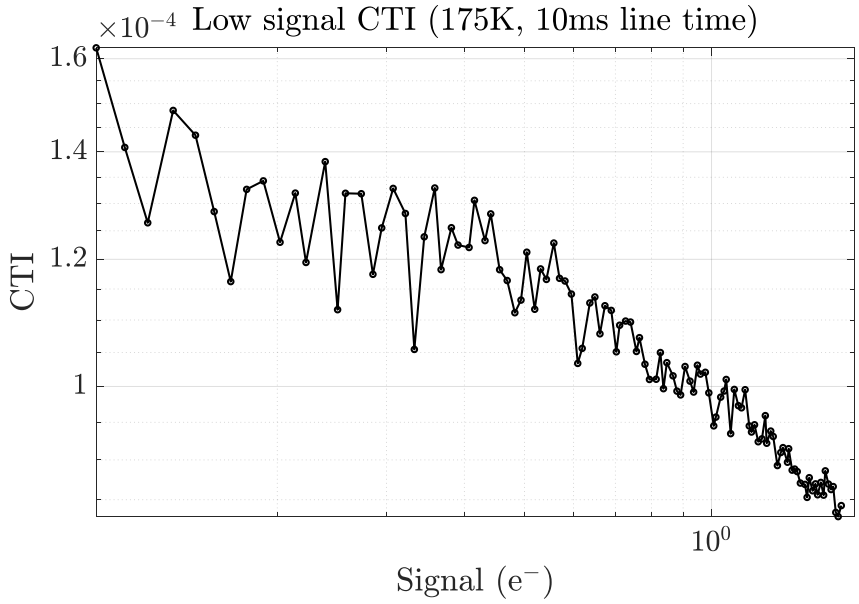


Figure 4.15 Data of figure 4.14 presented in terms of CTI.

4.3 Multilevel clocking

Figure 4.5 illustrates the mechanism of trapped charge recovery. We may use optimized clocking schemes to enhance this effect and accurately test their efficacy using the previously described deferred charge measurement methods. One such clocking scheme is the multi-level scheme which calls for the use of an intermediate clock level between the barrier and storage voltage levels for each phase.

4.3.1 Method

Multi-level clocking has been first reported in use by Neil Murray [27], formerly of the CEI at Open University in the context of charge transfer performance. Figure 4.16 illustrates the principle on which multilevel clocking boosts charge recovery. In this figure, phase 1 is in the process of returning to a barrier phase but pauses at an intermediate level. In this state, the volume of silicon in which charge recovery will occur is greater than that in the

case of conventional bi-level clocking (figure 4.5). This is because the recovery interval is defined by the region of negative gradient of the buried channel potential. This potential gradient can also be introduced using buried channel implants and using pseudo two-phase clocking as is done in [6]. Nonetheless, results from the literature for this method are limited at best, showing somewhat of a reduction in CTI for an irradiated device using x-ray transfer measurement methods. Here we demonstrate highly detailed, accurate measurements of CTI reduction using multilevel clocking.

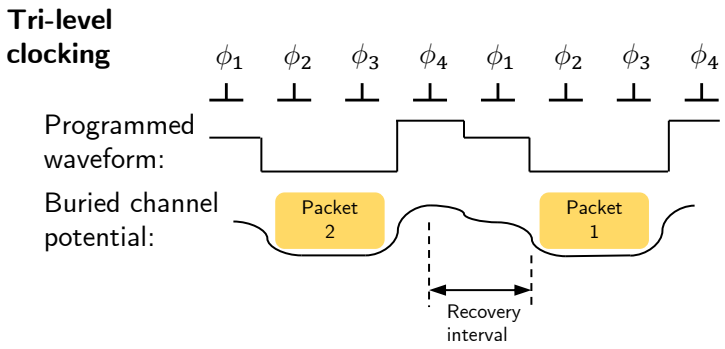


Figure 4.16 Representation of potential profile along the column direction. Charge trapped from packet 1 will return to packet 1 if emission occurs while the trap is positioned within the recovery interval indicated.

The value of the intermediate level required depends on the signal size being measured. The closer this level is to the storage phase level, the steeper the potential gradient is and the greater the silicon volume of charge recovery. In this case, however, if the signal packet is also large it may occupy the phase in the intermediate level also, thus preventing charge de-trapping under that phase. Therefore, the intermediate level should be set as high as possible but low enough to leave a deep enough storage potential well for signal packets to be contained in full storage phases.

4.3.2 Results

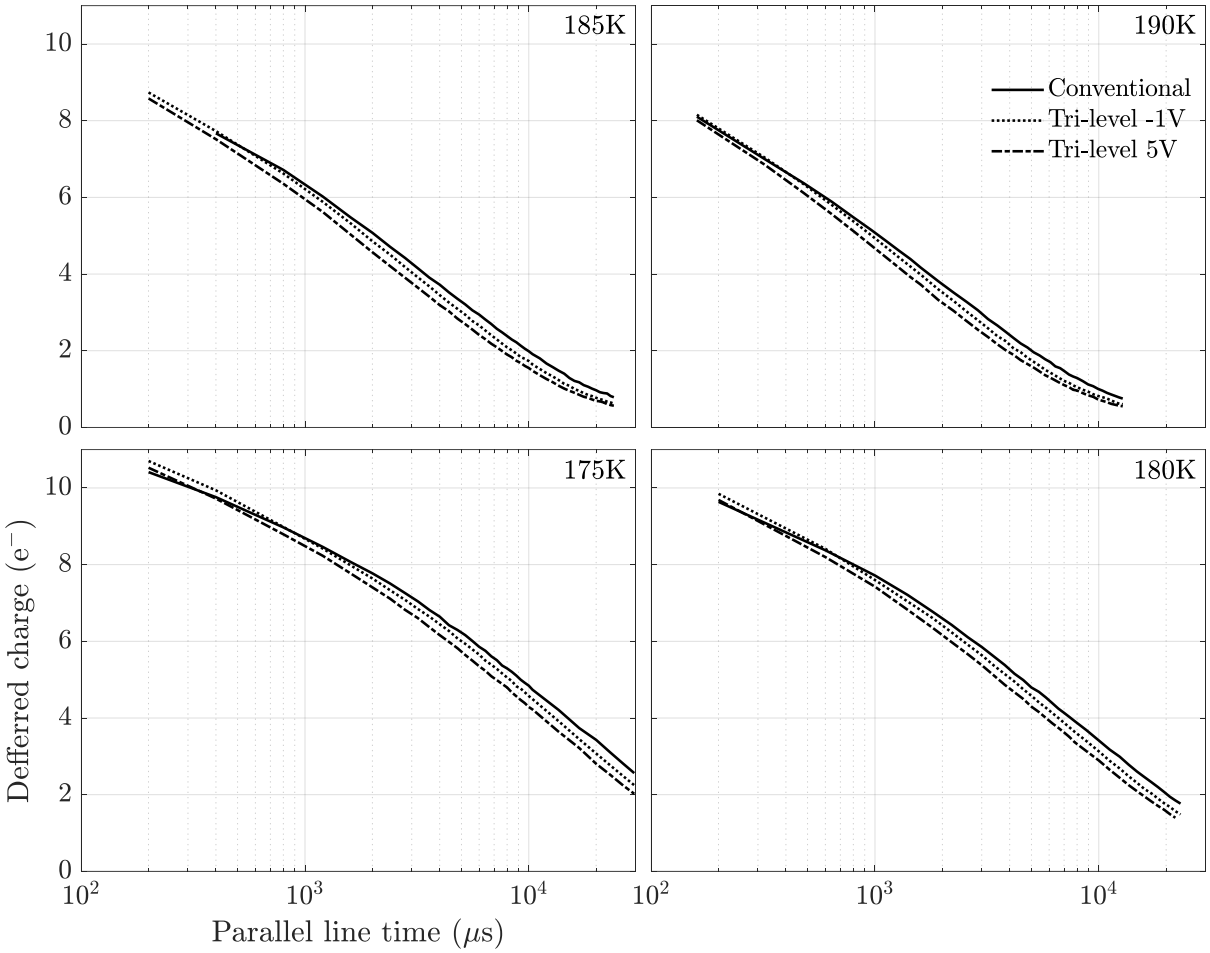


Figure 4.17 Tri-level clocking deferred charge performance comparison across temperature and between intermediate levels used (-1V and 5V) where the gate high and low levels were -3V and 7V respectively.

Figure 4.17 shows the improvement in deferred charge when the additional transition to the intermediate voltage level is introduced. Three curves are shown for each temperature, comparing conventional clocking to tri-level clocking at intermediate levels of -1V and 5V while the parallel phases have storage and barrier levels of 7V and -3V respectively. The comparison is made across all four temperatures tested and the comparison is consistent. While the deferred charge reduction offered by the use of tri-level clocking is clear, the

improvement is marginal, returning at best, slightly less than a single electron of trapped charge at the longer line transfer times.

Despite the meager improvement seen using the technique, the comparison between the benefit using the -1V intermediate level vs that of 5V holds up to expectation. The use of an intermediate level closer the storage level offers greater charge recovery. This implies that the 2V storage potential well is deep enough to contain the $3.5 \times 10^4 e^-$ signal packet without spilling into the phase at the intermediate level.

4.4 Concurrent clocking

As mentioned in section 4.2.3, it is advantageous to use a slower parallel line transfer in order to maximize total recovered charge. The trade-off is a slower CCD readout and thus a penalty in overall observing cadence for the camera. In this section it is argued that the conventional readout process utilizes an unnecessarily fast parallel line transfer by limiting the operation of the parallel registers to only when the serial registers are idle. Operating these concurrently, however, allows a parallel line transfer only as fast as required for the entire row of serial registers to clock out. This is possible to do in CCDs with a dedicated transfer gate, TG (last gate) separating the image area from the serial registers. Transfer gates are included in most CCDs from e2v and are common in those from other manufacturers, also (notable exceptions are CCDs manufactured by STA who recently omitted TGs from their designs).

4.4.1 Method

Both parallel and serial clocks may be operated simultaneously so long as there is no interaction between parallel and serial register charges – this occurs while TG is closed (a barrier phase). As indicated in figure 4.18, this is already possible in the normal readout scheme. This figure depicts the parallel line transfer process for a four phase CCD. Conventionally the serials are stopped during this process; however, they only need be paused during the period shaded in red. The green region indicates the period that TG is closed. Further, the time that TG is open can be drastically reduced by employing the following method to transfer charge to the serial register without any transitions on the parallel clocks. The ascending sequence of potentials is set up on the last parallel clock, TG, and serial clocks so that charge moves from the parallel clock electrode to the serial register as soon as TG barrier is lowered as shown in figure 4.19.

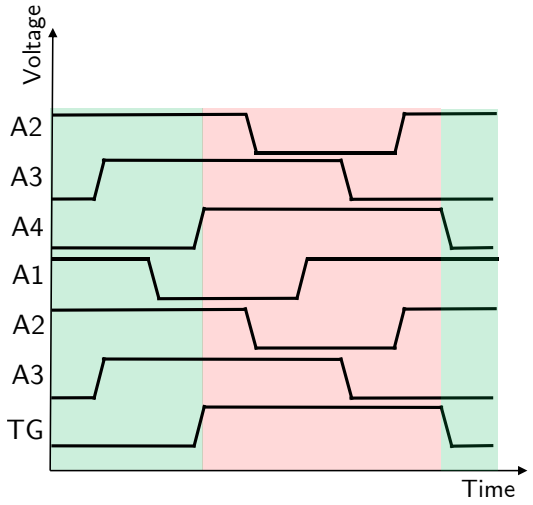


Figure 4.18 Parallel gate timings for last two lines in the array (8 gates/phases). Green region indicates time that TG is a barrier (serials can be clocking). Red region indicates TG in storage (serials must be paused).

In this figure, gate potentials are indicated with a solid black line, a higher level corresponding to more negative potential. After an exposure, (state 1) phases A1, A2, and A3 are in collection mode and state 2 describes the first transition in the parallel line shift waveform. Charge is shuffled down the line in the usual manner with all states separated by equal time intervals with the exception of states 3 and 4. State 3 depicts the line dump and the transition from 2—3 with 3—4 occurring in quick succession. The combination of these time intervals represents the length of the TG pulse.

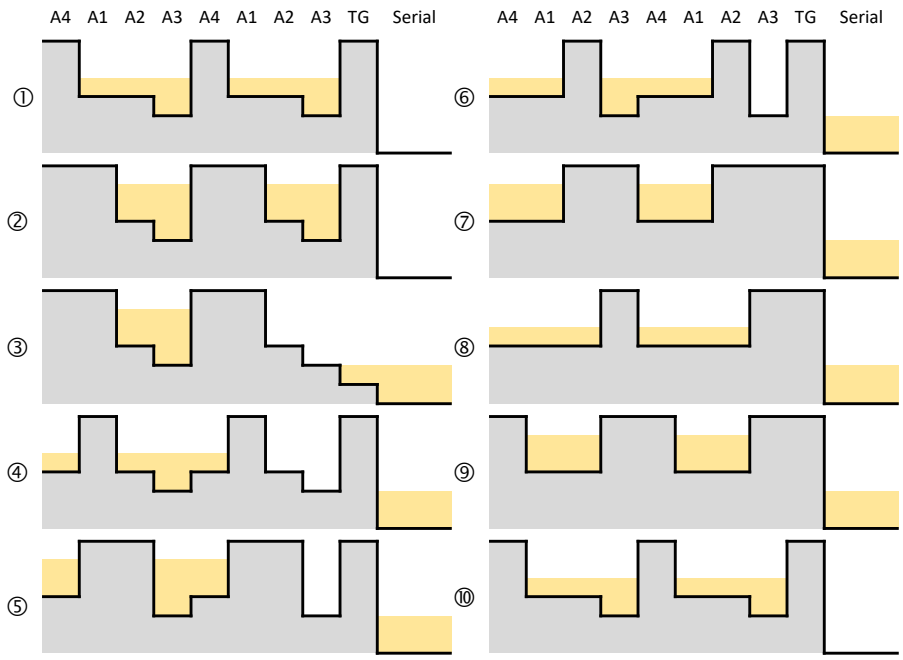


Figure 4.19 Concurrent clocking state diagrams for phases in the last two lines. Serial clocks are paused only between the transition between states 2 and 4.

The key step is shown in state 3 that occurs only briefly. From state 2 to 3, TG is lowered (positively biased) very quickly, which is made possible since it is driven on a dedicated line, separate from the parallel clock phases. In order for the line of charge to be transferred quickly into the serial register, rather than using a parallel phase to eject the charge, a

potential gradient is created using the last gate, TG and serial register. In this case, a gradient of 2V per gate was used (see state 3 in figure 4.19). Thus, A1, A2, and A4 have clock swings from –3V to 7V, A3 has a swing from –3 to 9V, TG from –3 to 11V and the serial register is held at 13V. Once the line has been dumped, TG is quickly returned to its barrier potential and serial clocking resumes as usual. It should be noted that in transition 3—4, charge atop TG may be sent back into preceding phases if serial storage phases are not set positively enough. No back-wash is observed with the voltages chosen. Figure 3 shows the new timing diagram overlaid on the original from figure 4.20. The green region highlighting the period that concurrent clocking may occur has expanded to encompass almost the entire line time.

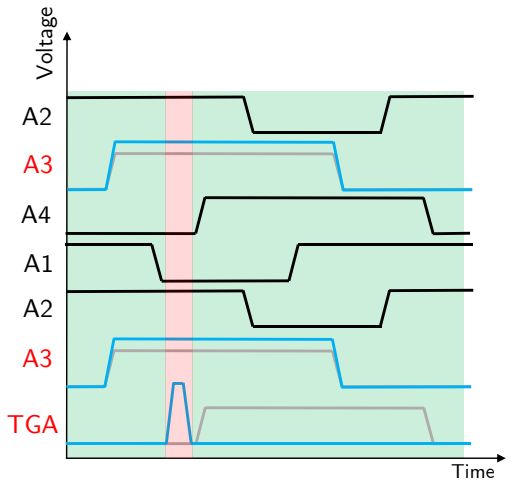


Figure 4.20 Concurrent clocking timing diagram showing brief TG pulse in which serials are paused.

The Waveform Definition Language (WDL, developed by the COO) was used for defining waveforms [40], that makes the concurrent pixel readout and parallel shift quite simple. The line transfer as described in figure 4.19 has a total of 9 transitions, each programmed as an individual waveform inserted between a block of pixel reads. The Archon runs serial

clocking continuously, breaking only to initiate one of these waveform transitions intermittently. Although the number of pixels read between clock transitions can be varied, in practice we have kept this constant with the exception of transitions 2—3 and 3—4 between which no serial clocking may occur. Thus, in WDL pseudo-code, a readout sequence will be represented as follows:

```
SEQUENCE readOut {
      fastTGpulse();
      serialClocking(pixels);
      transition4_5();
      serialClocking(pixels);
      transition5_6();
      …
      serialClocking(pixels);
      transition1_2();
      RETURN
}
```

TG Pulse width

When concurrently clocking, the line transfer overhead is determined by the length of the transfer gate pulse. We have already accelerated the line dump by introducing a staircase potential gradient – so how short can the TG pulse be? The transfer gate electrode is connected to the TG pin by low impedance metal traces to both ends. The polysilicon electrode has significant resistance, so propagation of a level transition from edges to center is governed by the distributed resistance and capacitance. A pulse with duration shorter than the time constant of the distributed RC network will be significantly attenuated in

the middle of the sensor, causing incomplete charge transfer due to the TG not reaching sufficiently high potential.

Trailing charge was measured for varying pulse widths using the textbook method for the EPER method (signal contained in first over-scan line). Signal was plotted as a function of distance from the edge of the CCD. When TG pulses are too short, charge transfer is very poor at the center of the chip. Figure 4.21 shows that the transfer gate pulse can acceptably be as short as 10µs (to achieve satisfactory charge transfer) which is a very small line overhead compared to the 3.1ms pixel read time at a 1MHz pixel rate.

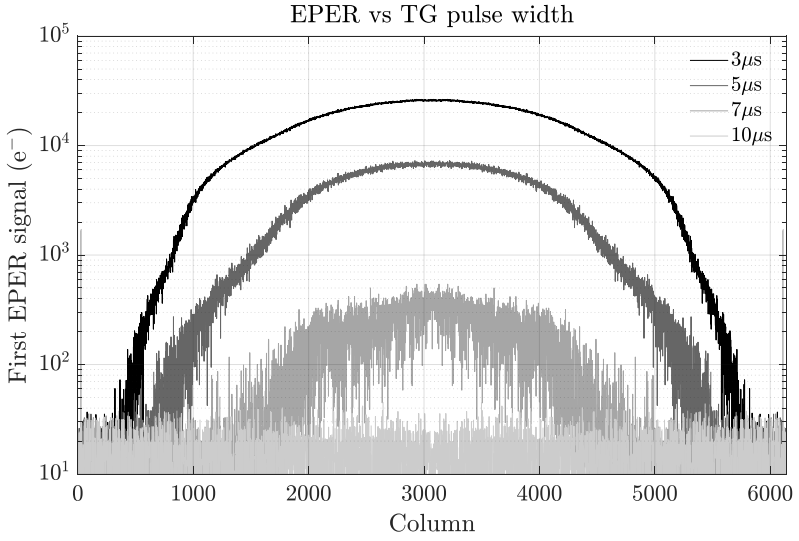


Figure 4.21 Mean signal per pixel in first over-scan pixel vs TG pulse width. A flattened profile across columns indicates complete charge transfer across the TG.

Fixed pattern **reduction**

The concurrent clocking scheme creates a fixed pattern as shown in figure 4.22. Each band corresponds to a different state of the parallel clocks. Figure 4.23 shows that the amplitude is about 100DN (600e-). We will show below that the fixed pattern is caused by the

transient voltage developed across the impedances in the substrate current return path when current flows to charge the parallel clock capacitance. The fixed pattern can be suppressed by any one of the following methods, or a combination, if greater precision is required:

- Bias frame subtraction (figure 4.24).
- Common mode rejection for differential signal readout (figure 4.25).
- Substrate current nulling by coincident ramped parallel clocks (figure 4.26).

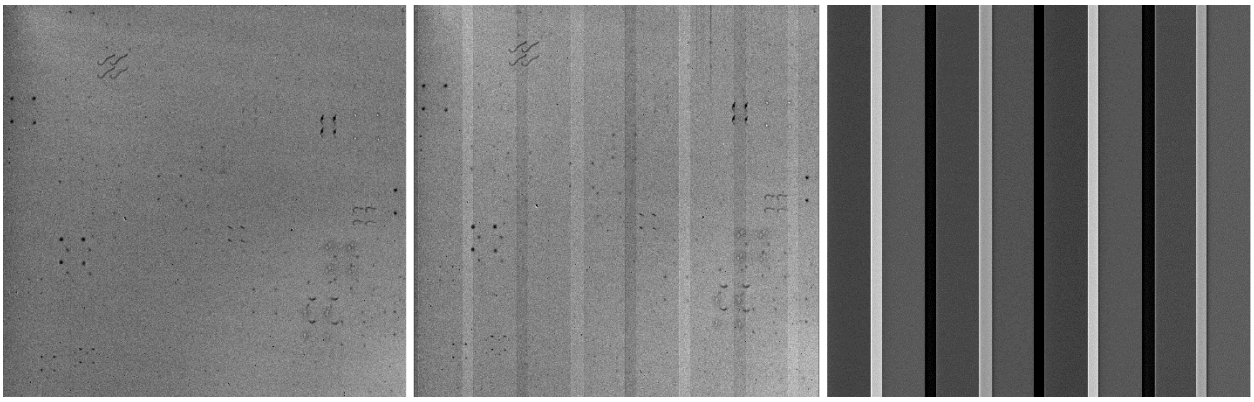


Figure 4.22 (Left) Conventionally clocked flat field image. (Middle) concurrently clocked flat field image. (Right) image difference.

Explanation for fixed pattern

Why does the fixed pattern arise? A rising edge on any parallel clock must charge capacitances both to substrate and to neighboring clock phases (figure 4.28). For a transition on a single clock, capacitances to neighboring phases and to substrate must be charged. The current flowing out of the P_1 driver (for example) in figure 4.28 splits 3 ways and returns to the P_4 and P_2 drivers via the respective inter-phase capacitances, C_{P14} and C_{P12} and flows into the substrate through C_{P1}.

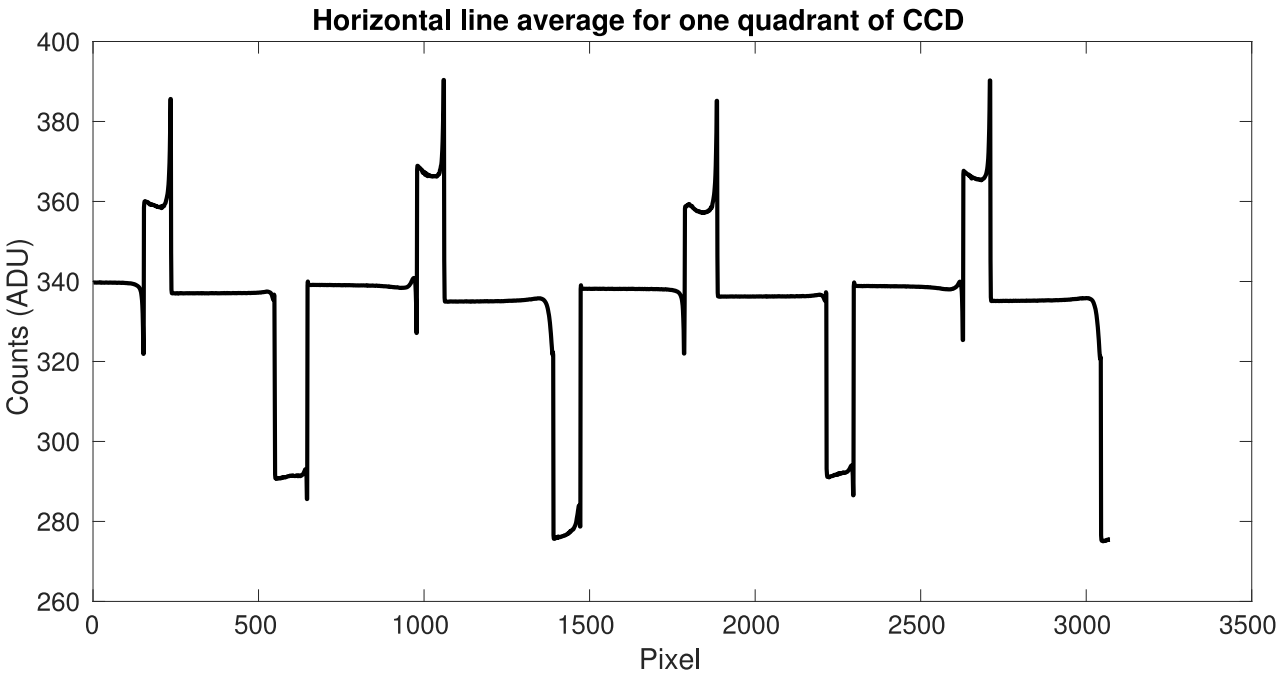


Figure 4.23 Concurrent clocking fixed pattern.

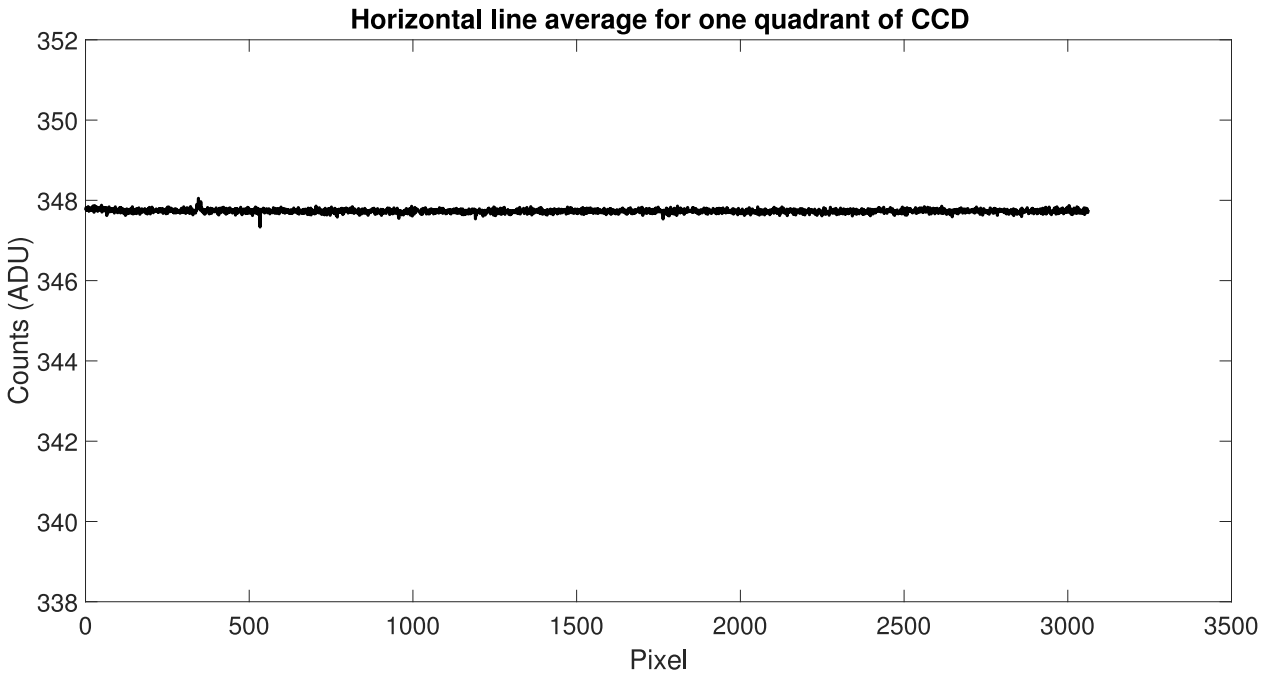


Figure 4.24 Concurrent clocking fixed pattern after bias subtraction.

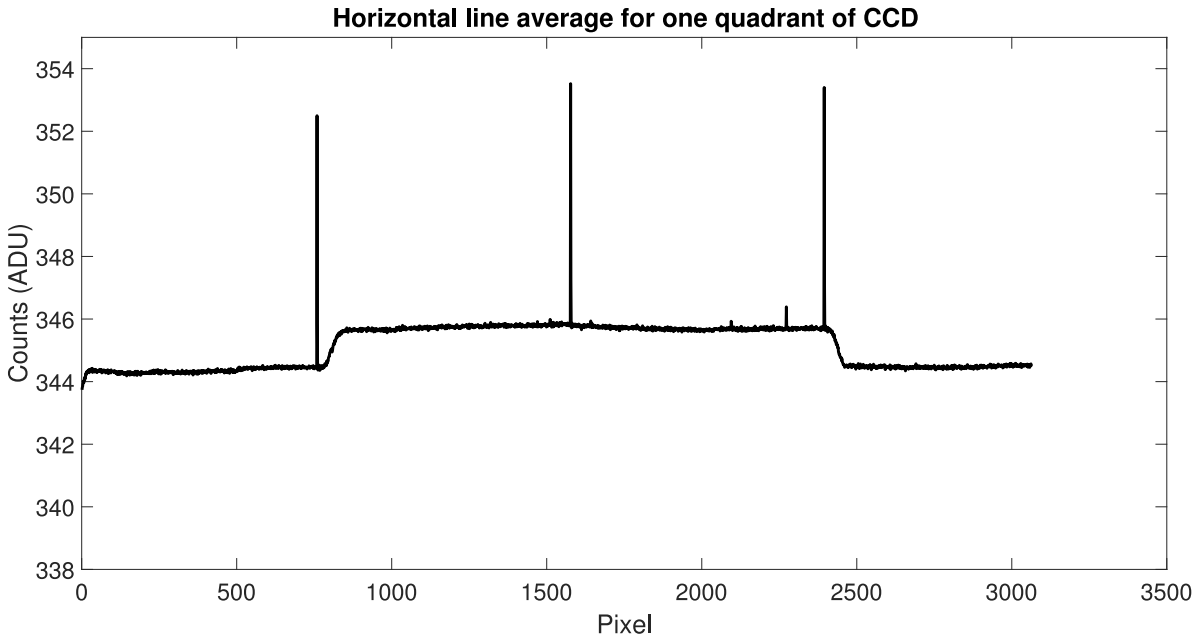


Figure 4.25 Concurrent clocking fixed pattern after common-mode rejection.

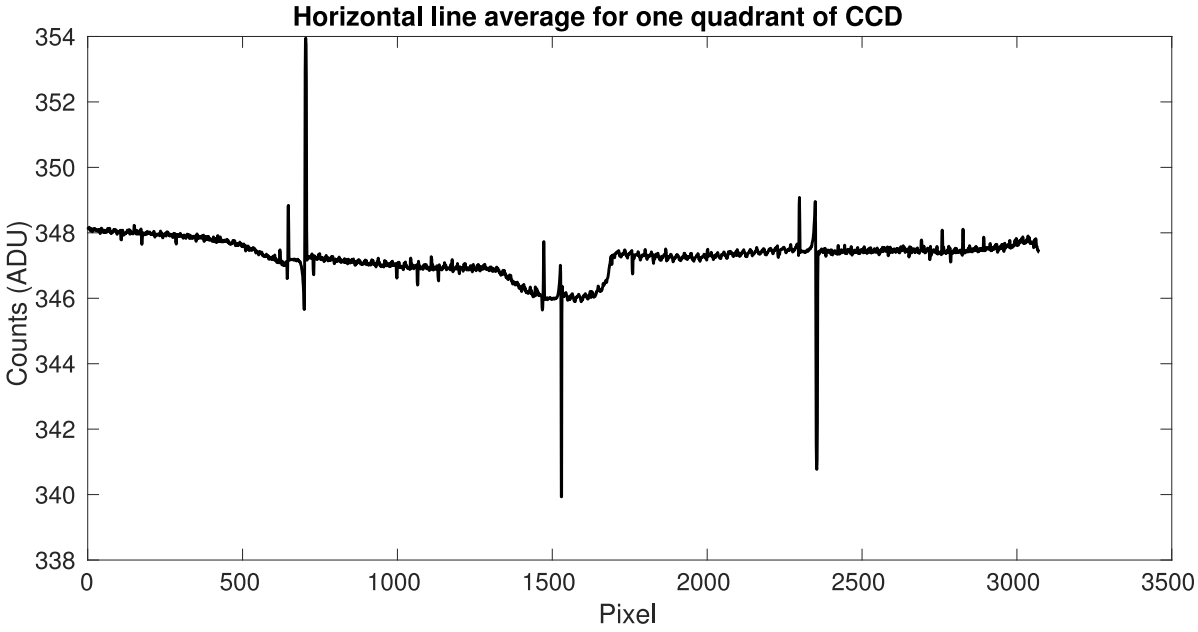


Figure 4.26 Concurrent clocking fixed pattern after substrate current nulling.

This substrate current must flow in a loop returning to where it started in the clock driver. Along the way it encounters impedances Z_B (bond wire inductance) and Z_{SS} (cabling inductance and resistance) and thus generates a voltage transient.

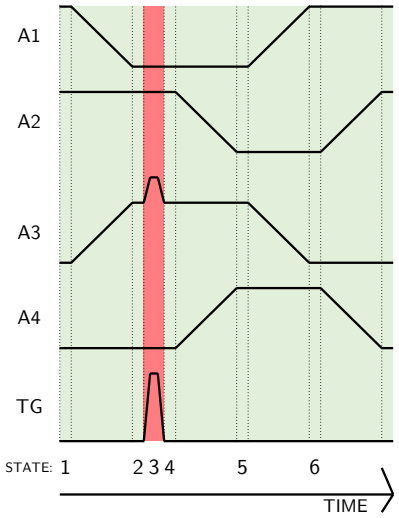


Figure 4.27 Modification of figure 4.20 with coincident ramped clocks for substrate current nulling.

A transient on the substrate side of the load resistor, R_L, couples through the potential divider formed by R_L and the source follower output impedance, which is the reciprocal of transconductance, g_m.

Thus the transient induced on the video is,

$$(i_1 + i_2)Z_{SS} \Big/ (1 + g_m \cdot R_L)$$

The coupling from substrate to source follower input will depend on the ratio of sense node capacitance to substrate and other parasitic capacitors. This ratio is unknown but we can say that the transient will be proportional to,

$$(i_1 + i_2) \cdot (Z_B + Z_{SS})$$

We may suppress this transient by noting that when two clock edges have opposite slopes, the currents into the substrate cancel. For perfect cancellation, we simply require that at every instant,

$$i_1 + i_2 \;=\; 0$$

$$C_{P1}\frac{\partial V_1}{\partial t} + C_{P2}\frac{\partial V_2}{\partial t} = 0$$

So for linear slopes,

$$C_{P1}\frac{\Delta V_1}{\Delta t_1} + C_{P2}\frac{\Delta V_2}{\Delta t_2} = 0$$

We require the edge transition time to be matched ($\Delta t_1 = \Delta t_2$), so that cancellation occurs during the entire transition. And so,

$$C_{P1}\Delta V_1 + C_{P2}\Delta V_2 = 0$$

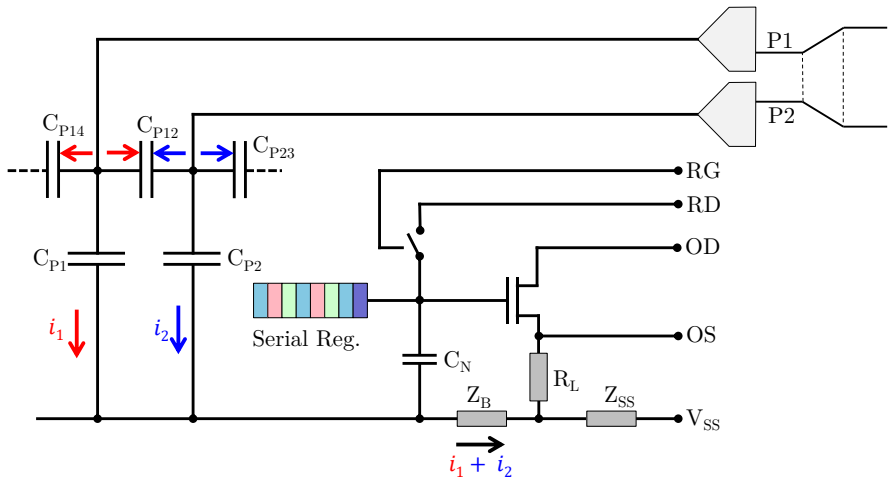


Figure 4.28 Schematic demonstrating the mechanism of substrate induced current.

Voltage swings are adjusted to compensate for different capacitance to substrate for each phase to balance the substrate currents. Slew rates are lowered to their minimums to minimize the error in voltage changes from the controller. Figure 4.27 shows the parallel

clock phase timing once this has been implemented. Figure 4.19 is then modified so that two consecutive parallel clock transitions occur at once, reducing the number of transitions to four.

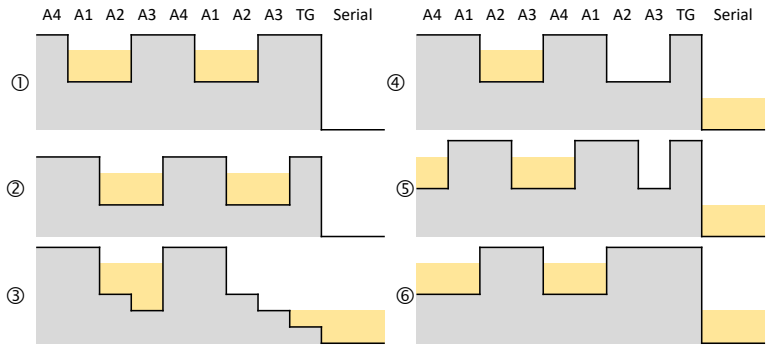


Figure 4.29 Corresponding state diagrams for figure 4.27.

The final sequence is clocked as shown in Figure 4.29. All clock swings are equal save for the TG pulse which is composed of transitions 2–3–4. In this way there are only four transitions in the line transfer. Figure 4.26 demonstrates the reduction in the magnitude of the fixed pattern signal using this approach. Although the pattern has been shown to be a term that may simply be subtracted, more slew-rate tweaking will allow for further reduction.

4.4.2 Results

The charge recovery benefit offered by extending the line transfer process through the simultaneous operation of the serial registers (concurrent clocking) is shown in figure 4.30. Also shown for comparison is the charge deferral seen using the conventional and tri-level clocking schemes in addition to the combination of the concurrent and tri-level schemes. The comparison is made with respect to the parallel line transfer time, P_t in the

conventional clocking scheme. The serial transfer time, S_t was held constant at 9760µs in both schemes so as not to confound the measurements with differing serial CTI. Accordingly, the parallel transfer time in the concurrent scheme was set to be,

$$P_{t,co} = S_t + P_{t,cv} = T_t$$

where T_t is the total line time (parallel and serial transfer times combined), $P_{t,co}$ and $P_{t,cv}$ are the parallel line transfer times in the concurrent and conventional schemes respectively. Each point on the horizontal axis in figure 4.30 thus corresponds to the same T_t for all schemes so that the schemes are compared on the equal basis of total CCD readout time.

It is immediately evident that the charge recovery offered by concurrent clocking can be significantly greater than that in the conventional case depending on the line time and temperature. Deferred charge is reduced by up to 40% at the shortest line times at a temperature of 175K whereas reductions of up to 90% are seen at a temperature of 190K. The percentage reduction increases with lowering line time and increasing temperature. This is in line with expectation since the difference between $P_{t,cv}$ and $P_{t,co}$ increases for lower T_t (since S_t is constant). The deferred charge in the conventional case reduces (improves) with increasing $P_{t,cv}$. The fractional improvement offered by concurrent clocking increases with the ratio, $P_{t,co}/P_{t,cv}$. It should be noted that S_t used in these experiments was 9760µs (the time required to read 9000 pixels at 1MHz). Typically, however, S_t is much less than this — normally around 3ms for a quad output CCD such as that used here.

The addition of tri-level clocking to the concurrent clocking scheme once again provides a consistent boost in recovered charge. Still though, the improvement is marginal.

Perhaps an interesting point is that at a temperature of 190K it is observed that there is a point where it becomes more advantageous to clock conventionally than concurrently (from the deferred charge point of view), whether using tri-level clocking or not. It can be surmised that this point exists at all temperatures and depends on the distribution of trap emission time constants relative to the line transfer time used. How can one determine where this point is under different conditions? How can one predict the amount of CTI reduction offered by concurrent clocking under different conditions? This will be explored in section 4.5.

4.5 Modeling deferred charge

Deferred charge has now been characterized in detail for a particular set of operating conditions. A complete picture of the traps at play in this context has been explored in chapter 3. It can be shown that by using this trap picture and simulating the exponential trap emission process, the deferred charge data can be reproduced – a model that can be used in the complete optimization of CCD charge transfer performance.

Here, a simple charge transfer simulation using a Monte-Carlo method is shown to quickly yield accurate estimates of deferred charge. Given an accurate representation of the trap landscape, the method can be adapted to suit any desired clocking scheme. The basic idea is to simulate the emission process of each trap in a column for a particular line rate and temperature to determine whether the charge is recovered or not. If not, the task is to

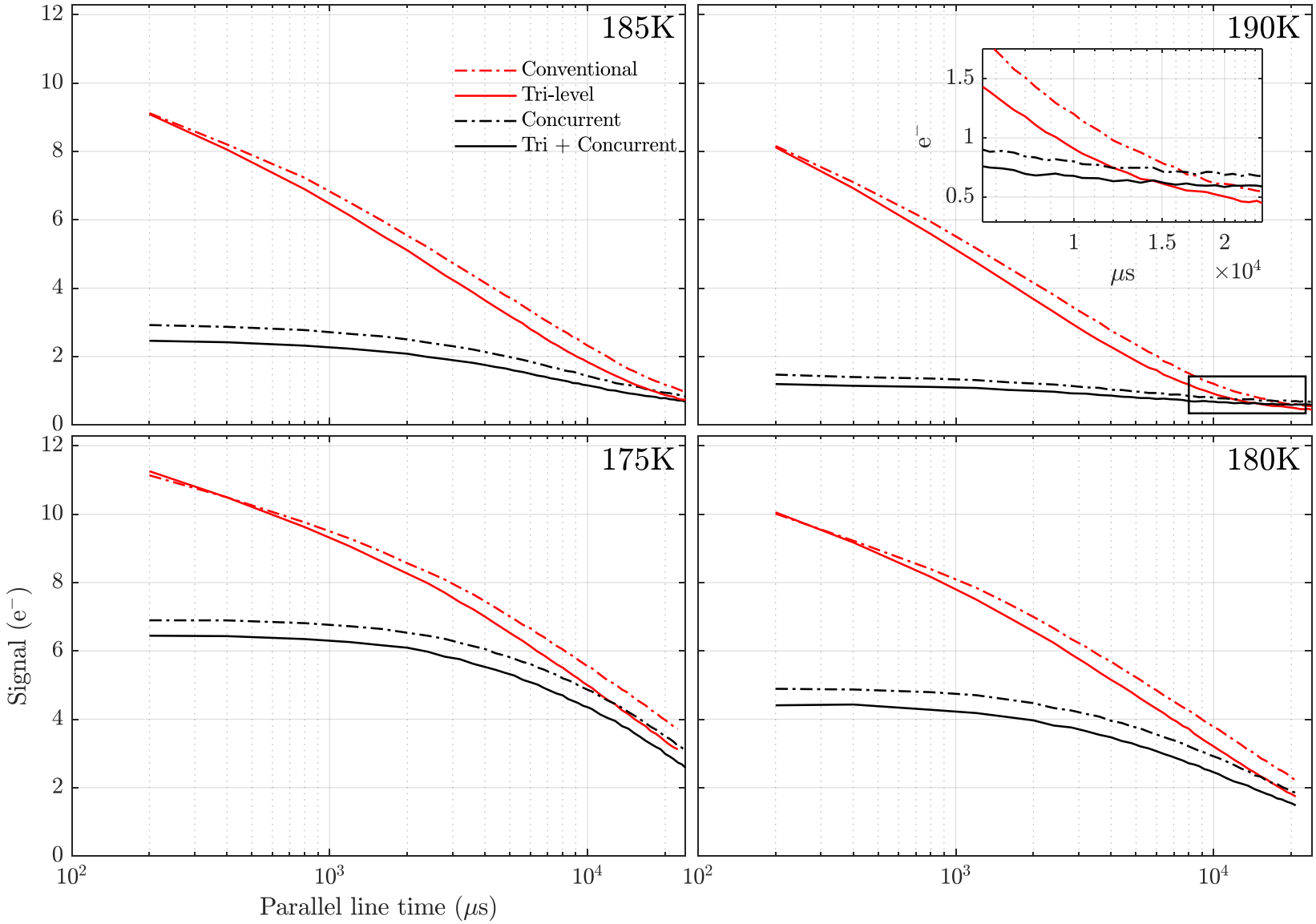


Figure 4.30 Experimental data comparing deferred charge performance of all schemes at four temperatures.

determine which extended pixel the emitted charge will join. This is done for each trap in the column (for 20 traps per column as determined from figure 4.1), and several thousand such columns are simulated. The EPER profiles for each column are then averaged to give a final result. This is repeated for all temperatures and line rates of interest; the process is described in figure 4.32.

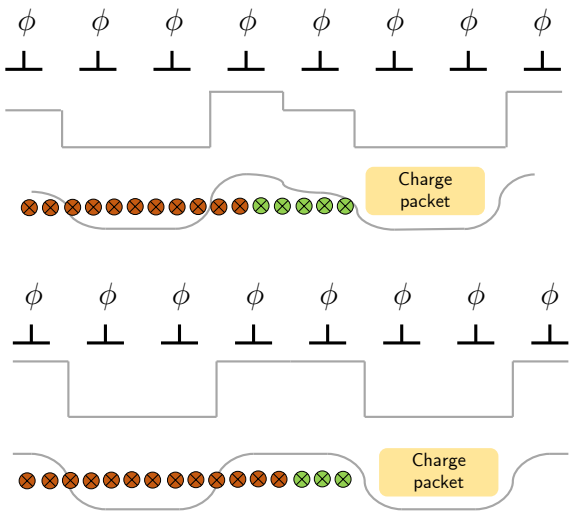


Figure 4.31 Diagram of the last charge packet in the column. Traps emitting in green locations do not cause CTI (released charge is recovered) – those that emit in the red locations do (released charge is lost). Top is the case for tri-level clocking, bottom is that for conventional clocking.

To determine the EPER signal due to a single trap, the trap is first randomly chosen from the pool of all identified traps at a particular temperature, giving a random τ_e(emission time constant) and $P_c D$ (product of capture probability and trap depth). Next, the phase location of the trap is randomly chosen from the four available phases followed by the random assignment of which half of the phase it is in. An emission time is sampled for the trap using a simulation of the exponential process. Depending on the clocking scheme, each phase will have a unique timing cycle – the sampled trap emission time will determine

where in the cycle the trapped charge is released and the configuration of phases at that time will determine the pixel destination of the de-trapped charge.

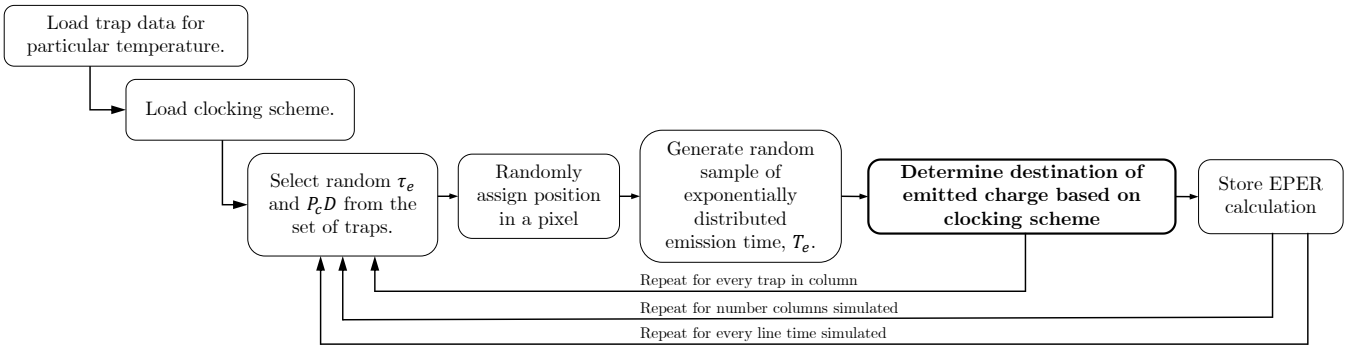


Figure 4.32 EPER modeling routine flowchart.

Figure 4.31 gives an illustration of the movement of de-trapped charge depending on emission time/trap location. Care must be taken to accurately represent the timing used – including the parallel clocks being paused during serial pixel readout, end of line overhead time etc. A further consideration is the *amount* of de-trapped charge from a single trap. This is simply given by P_cD as this quantity incorporates the probability of the trap capturing charge to begin with. P_c, however, is a function of signal level and so any such EPER simulations will only represent EPER seen using the same signal level as was used to generate the trap data.

Figure 4.36 presents plots of the EPER model predictions (total deferred charge) for the same line times as those used for the experimental data shown in figure 4.30. In the model, the amount of charge in each extended pixel is calculated. However, the total deferred charge is calculated as the total recovered charge subtracted from the total trapped charge (this obviates the need to integrate the extended pixel charge tail). The model results are

in general agreement with the data to within 1e- across all line times, temperatures, and clocking schemes. This is the definitive evidence to demonstrate that it is indeed predominantly bulk trap CTI that is being measured. Certain behaviors in the performance of the individual schemes, however, are not evident in the model results.

In the experimental results, tri-level clocking seems to offer little to no benefit at the shortest line times tested while offering at most, a 0.7e- boost in recovered charge over all line times. The model results, however, show a consistent recovered charge boost due to tri-level clocking of approximately 1e- across all line times at all temperatures. These differences can be attributed to the variation in the number of traps per column which was assumed to be 20 according to figure 4.1. When examined closely using a median filter with a 50px window the spatial variation in the number of traps per column becomes evident as shown in figure 4.35. It is further evident in this figure that most of this variation is being caused by the species 4 trap identified in chapter 3.

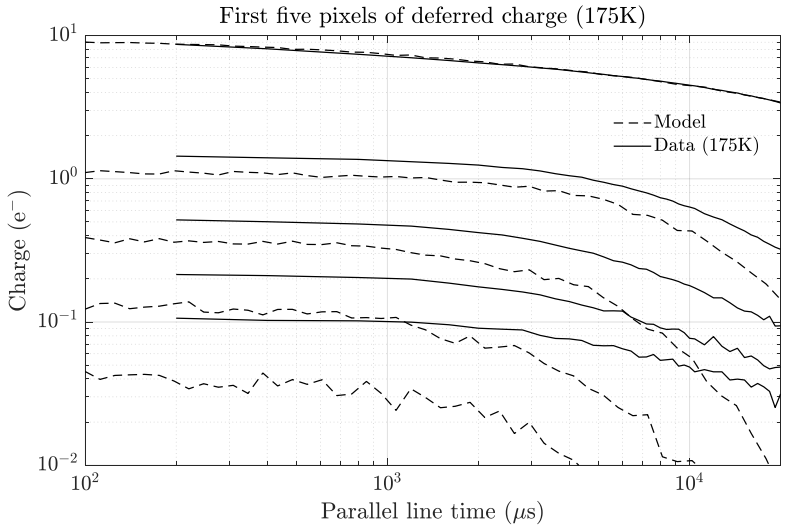


Figure 4.33 Model and data comparison for the first 5 EPER pixels for a temperature of 175K, assuming 20 traps/column.

The model results also suggest that the cross-over point (between the conventional and concurrent schemes) seen in the experimental results is not predicted just from the clocking scheme and trap statistics. Indeed, by simulating to very long line times, the model predicts, at worst, identical performance between the concurrent and conventional schemes. Even though this crossover is only expected at line transfer times much longer than normally used, where exactly this point occurs requires further investigation.

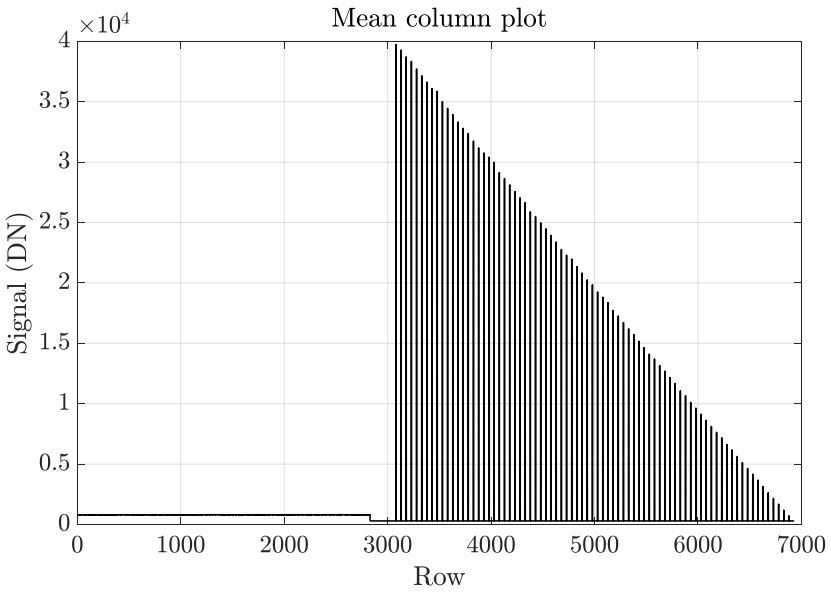


Figure 4.34 Mid-line binning can be used to generate single pixel rows of signal of any size.

Figure 4.33 shows a model/experimental comparison of deferred charge on a pixel by pixel basis for the first 5 extended pixels (for a sample temperature of 175K). Charge deferred to the first extended pixel is predicted quite well although subsequent pixels are underestimated. The model predicts shorter and smaller charge tails that drop off quickly with increasing line time; the charge tails seen in the data seem to persist for longer. The possible explanation of residual phosphorescence is somewhat negated by the highly accurate prediction of the first extended pixel. The same can be said of the suggestion of

dark current as another possible explanation. Further experiments are required to ensure this is not an electronics issue.

The most likely explanation for the model inadequacy however is that charge recapture is not being taken into account. The deferred charge itself is a signal packet that is susceptible to trapping and further deferral. These are secondary effects with additional complexity and would require accurate estimations of the number of traps seen as a function of signal level, i.e., the data of figure 4.13. With this effect taken into account, the modelled deferred charge tail would be elongated, thereby bringing it closer to the data.

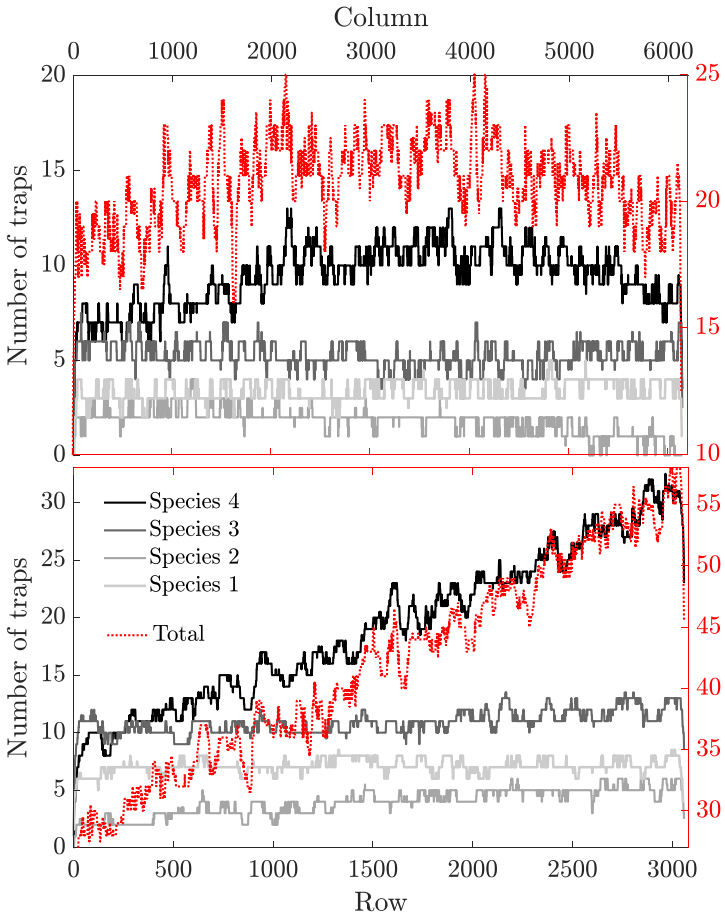


Figure 4.35 Median filtered (50 px window) trap statistics by row and column. Species 4 is responsible for almost all spatial variation.

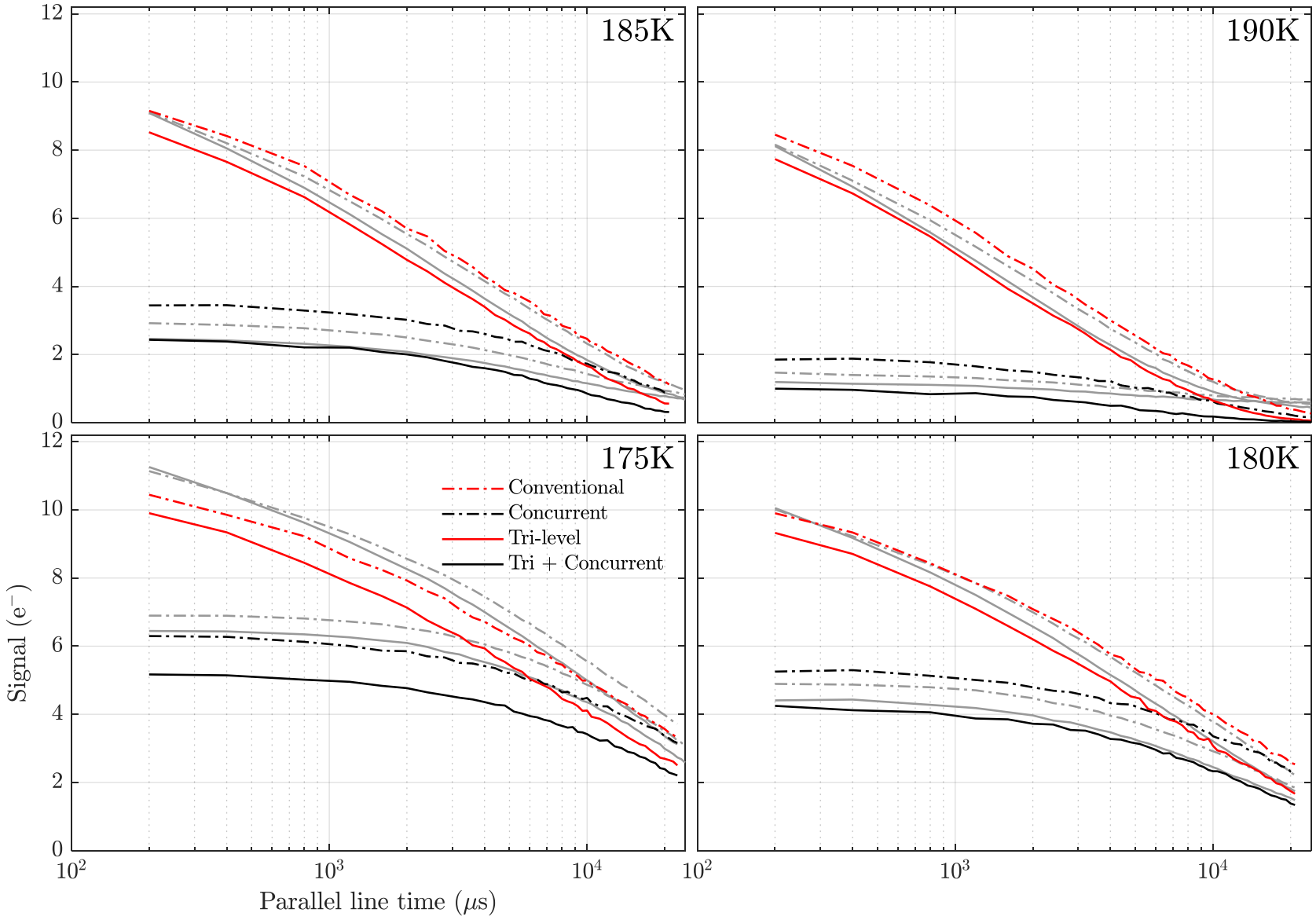


Figure 4.36 Comparison of modeling predictions for results given in figure 4.30.

4.6 Deferred charge effects on spectral peaks

The deferred charge measurement method described in section 4.2.1 offers the possibility of synthesizing arbitrary signal profiles in the parallel direction much like an astronomical source that is wavelength dispersed in the vertical direction. This is useful in conjunction with the improved clocking methods described earlier to measure the actual improvement in the accuracy of real data. It can be seen for example how spectral peaks shift or even interact (due to bulk trapping CTI) depending on size and location on the chip. Whereas conventionally this is done using simulations such as in [2], herein is a method to directly measure the effect of bulk traps on known input spectra.

Figure 4.34 shows an example column profile demonstrating the ability to generate a spectral peak of arbitrary height, limited only by the number of rows available in the charge filled half of the CCD. In this figure, pixels up to the 3080^{th} row contain the lower half of the flat-field image succeeded by some empty pixels. What follows is a descending ramp of peaks spaced by equal intervals of 50 pixels. This is accomplished by clocking an incrementally decreasing number of summed rows from the upper half into the lower half of the chip. By modulating this 'mid-line bin factor' one may create an arbitrary profile resembling portions of astronomical spectra.

A simple test using this flexibility is to observe the interaction of spectral peaks as a function of separation distance (number of pixels). Figure 4.37 shows the result of clocking two rows of charge down the array, separated by an incrementing number of pixels from 1 to 30. When the signals are in close proximity, the traps that are filled by the leading signal pixel do not empty fast enough to be refilled by the following signal pixel. Thus the

leading peak 'shields' the follower peak, with the majority of the charge tail being composed of deferred charge from the first peak. As expected then, at a separation of 10 pixels, charge is deferred from both peaks. The second peak is still, however, marginally taller than the first owing to some traps still being filled when passed by the second peak. Finally, at a separation of 30 pixels an equal amount of charge is deferred from both peaks as all of the same traps are filled and emptied twice.

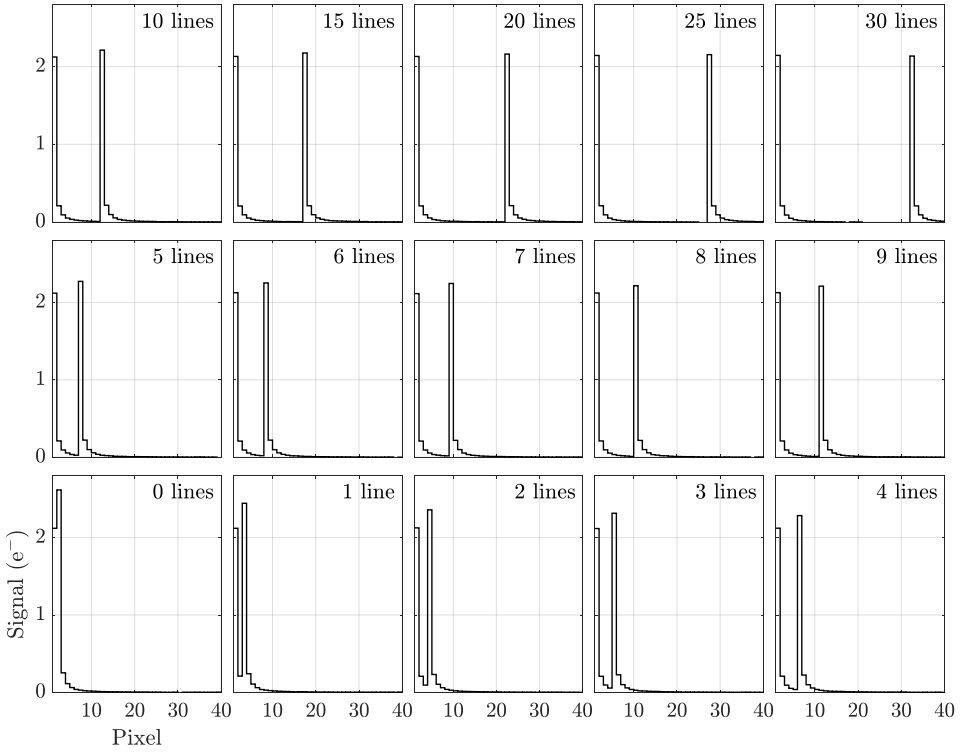


Figure 4.37 Deferred charge measurements of two lines of charge sent down the array spaced by an incrementing number of pixels.

Figure 4.38 shows the result of a similar experiment performed with a group of three peaks. As expected, the second two peaks maintain almost equal heights while being taller than the first. This is due to them being shielded from charge trapping of those traps with emission time constants greater than the signal separation time. It should be mentioned

that very small signals were used in order to observe the signal and signal trails in the same context. Further tests involving differently sized peaks with varying separations will give insightful results since the number of traps seen varies with signal packet size; while it is beneficial to prefill traps with a leading disposable signal packet, those traps will emit their stored charge some time later (and contaminate data) unless they are kept satiated by *similarly sized* signal packets. This condition is seldom achievable with real data.

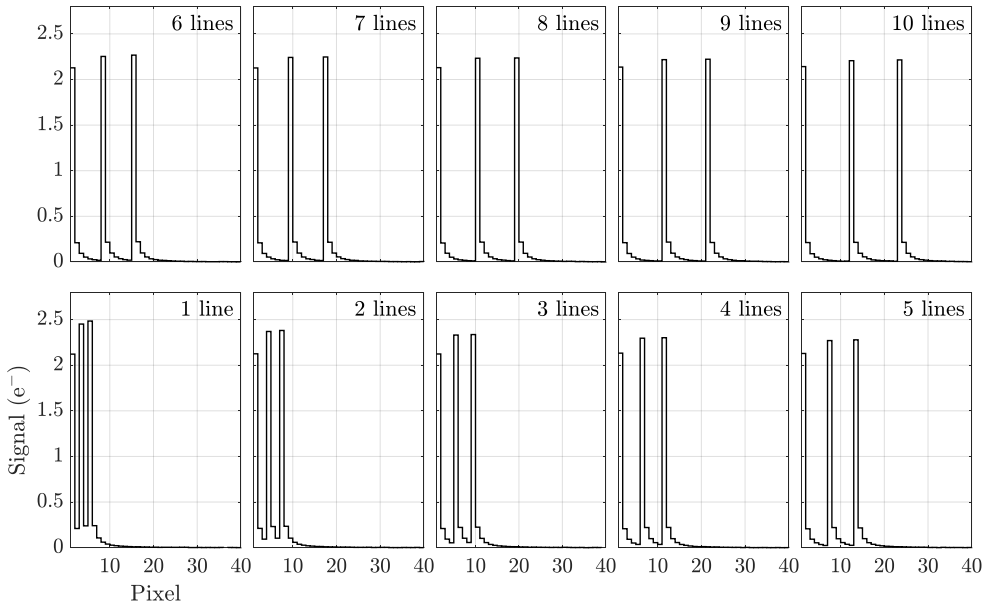


Figure 4.38 Deferred charge measurements of three lines of charge sent down the array spaced by an incrementing number of pixels.

4.7 Serial CTI

All data presented in previous sections concern CTI in the parallel direction (CCD image phases). Serial CTI due to bulk traps however has not been considered although it is arguably just as (if not, more) significant in contributing to systematic error in CCD imaging data. To truly optimize CCD timing for optimum charge transfer, serial CTI must be fully characterized and managed with parallel CTI. While it is a fundamentally different

area of the CCD, the serial registers can be characterized in the same fashion as the parallel registers, albeit with some modifications. This is necessary since, while the trap density is expected to be the same as that in the parallel registers, the number of relevant traps as a function of signal level is likely different, due to the differing channel size and geometry in the serial registers.

Nonetheless, trap characterization would proceed much quicker than in the parallel case since there is only one row of traps to characterize as opposed to several thousands of columns of traps. By varying the pumping frequency from row to row, emission time constants may be extracted from a single pocket pumped frame since all data required for generating the dipole intensity curve will be contained in the frame. Deferred charge measurements on the other hand will take longer to acquire since there is not the ability to collapse thousands of measurements (columns) as was done in the parallel case. Thus, the read noise is applied to each measurement.

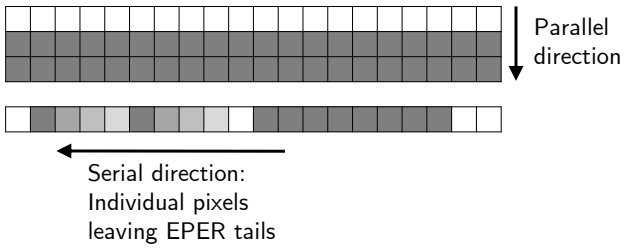


Figure 4.39 Single frame multiple EPER measurements are also possible in the serial direction for a quad readout CCD.

Even still, the ability to generate many horizontal EPER measurements in a single frame remains in the case of the quad readout CCD. Once a new line is clocked into the serial registers, half of the serial pixels may be cleared out through a single output. From the

remaining half, individual pixels may then be directed toward the same output at arbitrarily spaced intervals in which EPER tails can be measured (figure 4.39). The signal to noise equation then becomes (for a read noise of 12e$^-$),

$$\frac{D_L \cdot mn}{12\sqrt{mn}} = 5$$

where m is the number of rows of deferred charge averaged and n is the number of horizontal EPER measurements Thus, for the same deferred charge 5σ detection limit of 0.08e$^-$ and $n = 40$ measurements every row, $m = 1.4 \times 10^4$ which is over twice the number of rows available in a single frame. Thus, a single horizontal EPER measurement will require three frames as opposed to one for the parallel case (in order to achieve the same accuracy).

4.8 Summary

The EPER method for estimating CCD CTE has been used to great effect in determining absolute CTI due to bulk traps. Whereas the technique has traditionally been considered only useful for relative CTI measurements, here it is demonstrated that by significantly boosting over-scan SNR, the EPER technique offers a versatile and efficient method to measure deferred charge to the level of 0.1e$^-$ at a 5σ accuracy using a single flat field frame (for the CCD used here). SNR is boosted by collapsing all columns of deferred charge – this is possible since it is shown that all columns in the CCD are statistically similar in trap numbers. Further, by making use of the independent control of the top and bottom set of parallel gates, many EPER measurements of each column can be made *within* the same frame.

Using this enhanced EPER technique, CTI has been examined in detail on a brand new E2V 231-C6 CCD which already delivers exception charge transfer performance (very low CTI) out of the box. Archon controller scripting has enabled the acquisition of many data spanning the parameter space of line transfer time, temperature and signal level. CTI improves with increasing line transfer time and temperature; it worsens with increasing signal level. It is worth noting that such variability is not readily available from results obtained with the standard method of Fe^{55} x-ray testing. As an example, for the CCD in question, Fe^{55} results yield a CTI on the order of 10^{-6} whereas data herein shows that in actuality, CTI varies from 10^{-4} to 10^{-8} depending on the signal level being considered. The CTI trends uncovered follow simply described functions which can conceivably be used to predict CTI for any combination of parameters.

These tools to accurately characterize CTI are important for developing techniques to reduce CTI. Using them, a simple new clocking scheme has been shown to drastically cut down on deferred charge during readout which can be readily implemented on any CCD currently in use with a dedicated transfer gate separating the parallel and serial registers. This enables the concurrent operation of both sets of registers (by keeping transfer gate as a barrier) so that the parallel line transfer may be increased with no readout time penalty. In experimental data, this is shown to reduce deferred charge by up to 90% in conjunction with increasing temperature. This is shown to be further improved by using tri-level clocking to boost trapped charge recovery.

Finally, it has been shown that knowledge of the trap landscape such as that obtained in chapter 3 is sufficient to predict CTI as a function of readout timing and temperature (the

same can ostensibly be done as a function of signal size though this was not attempted here). This is done simply using Monte-Carlo simulations of charge transfer through a single column for several thousands of columns, each containing a random distribution of traps. This raises the possibility of ultimately constructing a model that can predict and minimize the amount of deferred charge under any combination of operating conditions, in the context of variables such as dark current, read noise, frame rate, etc. This would need to be done in conjunction with optimizing serial CTI, so any further work in this direction would need to begin with charge transfer studies of the serial registers.

5 Conclusions

The results presented in this thesis have opened the area of CCD optimization and, in particular, CTE optimization to new approaches. The efforts in characterizing the CCDs in the WaSP instrument were illuminating, not only to inform the characterization of the ZTF detectors but also with respect to efficiently characterizing CCDs in general. The CTE limits of the primary WaSP CCD has been studied in detail and the results are pertinent to anyone with CCD charge transfer concerns. In one of the first of such studies, bulk trap behavior and population statistics are revealed for the e2v 231-c6 CCD, showing a non-trivial number of traps peppered throughout the chip that can be identified with at least four different atomic defect configurations. It is shown that the EPER method of measuring CTI can be highly effective and in fact preferable compared to the accepted standard method of using an Fe^{55} x-ray source. The optimized EPER technique is used to expose the charge transfer behavior of the e2v CCD under different conditions. Additionally, clocking schemes have been presented that are relatively easy to implement and that can potentially drastically improve CTI.

There are three primary conclusions to take away from this work:

1. **Charge traps can be more numerous and diverse than past studies indicate, even in an undamaged brand-new CCD.**

The trap study presented here is one of very few (possibly only two, the other being in [6]) documented studies done on a new CCD. Here, four traps species are clearly identified by emission time constant histograms with no ambiguity between trap types based on τ_e.

Furthermore, when identifying traps by their band-gap energy levels, a possible fifth species emerges. Thus, the number of trap species identified on a freshly minted CCD is greater than that previously seen and, moreover, so are their population densities.

While other trap studies have omitted most details of their identified trap population statistics, some indication of trap density can be deduced by comparing τ_e histogram peak heights between studies making sure to use roughly the same histogram bin widths. Doing this shows a significantly greater number of traps (1 trap per 150px) identified here and the results are detailed in section 3.4.1. Here, traps have been surveyed on the basis of species, temperature, distribution on the array and sub-pixel location. Overall, the distribution of 4 primary species was roughly in the ratio of 3 to 2 to 4 to 8 in order of increasing τ_e. While it was found that this ratio did not significantly change with sub-pixel location or temperature, there was subsequently found to be appreciable variation across the detector array. Moreover, this variation was mostly caused by the species with the largest τ_e.

The quality of the data here is attributable to the meticulous trap dipole identification/fitting and, primarily the time optimization of the trap pumping scheme detailed in section 3.3.2. The modification of the conventional pumping scheme is based on the correct choice of dwell times in each phase of the pocket-pumping cycle. Implementation of this new scheme is also made straightforward with a CCD controller such as Archon due to its parameterizable waveform scripts. Because the new scheme has been efficiency optimized, one can achieve higher SNR for a given pocket pumping experiment. A single pocket pumping experiment typically elapsed 24 hours to fully resolve

the dipole intensity curve of all traps at a given temperature and to determine their parameters accurately.

2. The EPER technique is a very accurate method for CTE measurement that can be used to verify CTE models.

The EPER technique is a relative CTE measurement technique because it measures left over charge or missing charge that is emitted on the time scales of the CCD readout. Fe^{55} CTE measurements are absolute because they measure the final size of the original charge packet after traversing the CCD array. For this reason, Fe^{55} has been the method of choice for the definitive measure of CTE. However as shown in the present work, if applied using appropriate clocking techniques (section 4.1.2), EPER can yield deferred charge measurements to an accuracy of below $0.1e^-$ such that an insignificant portion of the deferred charge tail will be missed by the measurement. If it is the case that the relevant trap emission time scales are very large, then the CCD temperature can be increased to bring these time scales within the range of CCD readout speeds to be able to measure their deferred charge.

This is preferable for two reasons. The first is that this method doesn't require a dedicated setup to expose the CCD to an Fe^{55} x-ray source — rather, it only requires a flat-field illumination source (which is even available on any facility class telescope). The second is that it allows for CTE measurement at any signal level. This is important since the number of relevant traps is dependent on the size of the charge cloud being transferred. In an Fe^{55} test however, CTE is examined only for a signal of $1620e^-$ (this number is, in fact, dependent on temperature, as mentioned in section 4.2.5). This may be fine for evaluating

relative CTE performance between devices. However, as shown in section 4.2.6 very low signal CTE can be drastically worse than that observed at even moderate to low signal levels.

Modeling using a Monte-Carlo method has been used to verify the EPER measurements here. The results show that the observed deferred charge signals are consistent with what is expected based on the number of traps seen in a given column. CTE has thus been measured accurately over the parameter space of temperature, readout speed and signal level.

3. The concurrent clocking scheme improves CTE under almost all conditions. The higher the temperature, the better it performs.

The term "concurrent clocking" is coined here to refer to the simultaneous operation of the parallel and serial registers during CCD readout. This is enabled by the use of the parallel transfer gate that is always a barrier except during the fast line dump from the parallels to the serials (described in section 4.4.1). While beneficial, in that it eliminates the parallel line transfer overhead, it has the much greater benefit of boosting recovered charge. This is due to the fact that when the CCD is clocked concurrently, charge packets spend an equal time in each parallel pixel phase whereas in the conventional clocking scheme, packets spend the majority of time in one parallel pixel phase and a comparatively small amount of time in the remaining phases. Spreading the wait time evenly over all phases allows an equal amount of charge recovery from trapped charge in all phases.

The concurrent clocking scheme has been demonstrated along with tri-level clocking using the deferred charge measurement techniques developed earlier. Results show up to a 90%

improvement in deferred charge as a result of employing the scheme, at the highest temperature (190K) and fastest readout tested (800kHz pixel rate). Furthermore, the trends show improvement only increasing with temperature and readout speed. It is seen, however, that at very low speeds, concurrent clocking performs slightly worse than conventional clocking. This is the only feature of the experimental results that is not reflected in the modeling of deferred charge based on individual trap emission processes. The deferred charge performance of the scheme can nonetheless be well estimated (to within $0.5e^-$) by modeling. Given that it is a relatively simple modification of the conventional clocking scheme, it can readily be applied on CCDs currently in use.

6 Further Work

1. **A generalized CTE optimization model provided the trap species and their population distributions.**

CTE is a major concern for any modern precision astronomical camera and any astronomical camera in space. A CTE investigation however can take a significant amount of time when accounting for a plethora of tests, experimental facility setup and radiation campaigns (in the space case). The EPER results here show that CTE trends with respect to operating conditions are well behaved and could be described by simple models. Further, using CCD trap information, CTE can be predicted using simple Monte-Carlo methods as functions of readout speed and temperature. Modeling CTE as a function of signal level cannot be done only with trap statistics, however, since this instead requires information on the scaling of charge cloud volume with respect to charge cloud size (number of charges).

In the present work, it has been shown that CTE can be described as a power-law function of signal level for most of the dynamic range.

Therefore, all the pieces are in place to form a generalized CTE model for CCDs as a function of trap species parameters. Particularly required would be trap energy levels and cross-sectional areas (for $\tau_e(T)$ functions to be derived), trap densities, and a function to describe the charge packet cross-sectional volume as a function of signal size. Alternatively, without trap parameters, functions to describe deferred charge as functions of line time and temperature could also be used. An investigation would need to be performed to determine the minimum amount of information required to accurately predict CTE for any set of operating conditions. In the present work it has only been shown so far that CTE can be accurately predicted as a function of line time and temperature.

It should be noted that the above refers to parallel CTE only. Regarding overall CTE, serial CTE needs to be accounted for and optimized in conjunction with the parallel. This should not present a significant challenge since the serial registers operate in the same fashion, albeit on different timescales. Thus, maximizing overall CTE will involve modeling deferred charge for both the parallel and serial registers. This promises to be a challenging yet very tractable problem.

Once such a model is created it needs to be incorporated into a more general model for CCD performance as mentioned in the previous point. This is because for example, improving CTE by increasing temperature is detrimental to the dark current. Models of dark current as functions of temperature exist do exist, so this can be balanced against CTE by simulations. As mentioned earlier, the CCD temperature requirement is also

driven by power dissipation, but most importantly the camera or spacecraft thermal management system. The interaction between these variables highlights the need for the ability to rapidly evaluate the impact of one operating parameter on the rest of a system involving CCDs. Therefore, a generalized CTE model is an important step in this direction.

2. The ability to automate the acquisition of individual CCD characteristics opens the possibility of automating CCD optimization.

In the process of tuning the CCDs for WaSP, many of the characterization procedures were automated by taking advantage of scripting capabilities with Archon. This meant, however, that inputs were tuned sequentially in a predetermined order. To truly be optimized, the CCD should be tuned in the multidimensional space of input parameters with respect to the multidimensional output parameters. A characterization test involving a sample group of 4 input and 4 output parameters was conducted to test this possibility. The dataset was analyzed using a visualization tool (t-SNE, described in [23]) that simplifies the picture of high-dimensional data points. Using this tool, data point clusters were easily identified, and the CCD could be manually optimized for this parameter subset.

The natural extension of this is to automate the data point cluster selection and hence automate the CCD optimization process. Since most characterization can be done with flat-field illumination, the experimental testbed for this task is not complicated. The approximate total number of primary inputs in CCD tuning are clock and bias levels and CDS deinterlacing parameters (approximately 10 or so inputs). Care must be taken such that input ranges are within safe limits and that there are no unsafe combinations for the CCD. Assuming these precautions, the main challenge is optimizing the amount of time

required to probe the entire input parameter space. A further point of investigation would be how to efficiently probe the input space by automatically eliminating input combinations that are clearly yielding sub-optimal CCD performance.

7 References

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