

Silicon Integrated Arrays: From Microwave to IR

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The logo for the California Institute of Technology (Caltech), featuring the word "Caltech" in a bold, orange, sans-serif font.

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To my love Sara
and
to my parents.

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ABSTRACT

Integrated chips have enabled realization and mass production of complex systems in a small form factor. Through process miniaturization many novel applications in silicon photonics and electronic systems have been enabled. In this thesis I have provided several examples of innovations that are only enabled by integration. I have also demonstrated how electronics and photonics circuits can complement each other to achieve a system with superior performance.

PUBLISHED CONTENT AND CONTRIBUTIONS

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NOMENCLATURE

- AGC.** Automatic Gain Control.
- AOC.** active optical cable.
- ASEPD.** Adjustable Self-Equalizing Photo-Diode.
- ASIC.** Application Specific Integrated Circuit.
- CFRP.** Carbon Fiber Reinforced Plastic.
- CMU.** Clock Multiplier Unit.
- DAR.** Distributed Active Radiator.
- DDD.** Displacements Damage Dose.
- DFB.** Distributed Feed-Back.
- EDFA.** Erbium Doped Fiber Amplifier.
- EIRP.** Effective Isotropic Radiated Power.
- GEO.** Geostationary Earth Orbit.
- IC.** Integrated Circuit.
- ILFD.** Injection Locked Frequency Divider.
- LEO.** Low Earth Orbit.
- LNA.** Low Noise Amplifier.
- LUT.** Look-up Table.
- MCU.** Micro-Controller Unit.
- MMF.** multi-mode fiber.
- MPD.** Multi-Port Driven.
- MZI.** Mach-Zehnder Interferometer.
- MZM.** Mach-Zehnder Modulator.
- NCI.** Nanophotonic Coherent Imager.
- OPM.** Optical Phase Modulator.
- PA.** Power Amplifier.

PER. Power-Enhancement Ratio.

PLL. Phase Locked Loop.

PV. Photovoltaics.

QAM. Quadrature Amplitude Modulation.

Rectenna. Rectifying Antenna.

Rectenna. Rectifying Antenna.

RF. radio frequency.

SEPD. Self-Equalizing Photo-Detector.

SiP. Silicon Photonics.

SMF. single-mode fiber.

SNR. Signal-to-Noise Ratio.

SOI. silicon on insulator.

SSB. Single Side-Band.

SSPI. Space Solar Power Initiative.

TIA. Trans-Impedance Amplifier.

TID. Total Ionization Dose.

TRP. Total Radiated Power.

VCO. Voltage Controlled Oscillator.

VGA. Variable Gain Amplifier.

VSWR. Voltage Standing Wave Ratio.

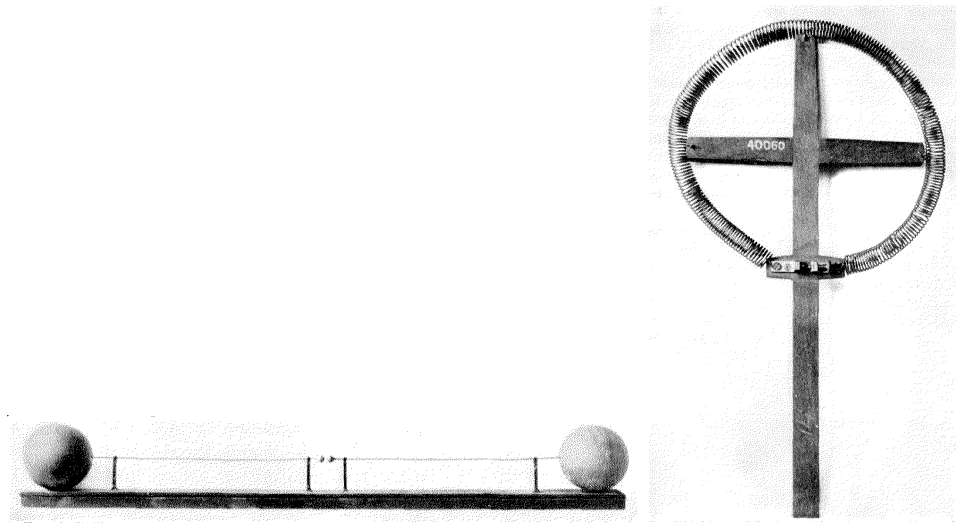
Chapter 1

INTRODUCTION

James Clerk Maxwell is considered the founding father of electro-magnetism. He consolidated the works of other great scientists such as Ampere and Faraday in a set of equations from which he derived the electromagnetic wave propagation equation and showed that these waves propagate at the speed of light. Thus, it can be said that he was the first person who connected light to electromagnetism. While the wave nature of the light was well known at the time, it took more than twenty years to discover the electromagnetic wave propagation produced by electricity and magnetism. Heinrich Hertz discovered these waves by using a spark gap and a simple dipole antenna in the transmitter side and a loop antenna in the receiver side as shown in figure 1.1. He initially thought that these waves have no practical use; however, engineers soon recognized the importance of these waves as a means of radio telegraphy. In less than 20 years, trans-Atlantic communication was possible. This achievement attracted more attention to radio-frequency (RF) communication and soon many different electronic circuitry components and architectures were invented that allowed manipulation of the lower frequency portion of the electromagnetic spectrum.

The electromagnetic spectrum is shown in figure 1.2, which spans from radio waves to gamma rays. Even though the same underlying physical principle applies to optical wave propagation, advancement in optical components and architectures that allowed manipulation of optical waves remained very limited. This can mainly be attributed to the very small wavelengths of visible and infrared spectrum which requires very precise systems to manipulate and control them. Recent advancement in lithography has enabled mass production of many precise and well controlled systems on a very small scale with very low cost and has revolutionized the design of optical and photonic systems.

Similar to RF transceivers in the beginning of 20th century, the main driving force for development of integrated photonics is communication. The development of extremely low loss optical fibers and very large available bandwidth in such fibers have been the the main motivation of research in the field of optical fiber communication. The deployment of TAT-8, the first transatlantic optical fiber cable, in



(a) Hertz first transmitter

(b) Hertz loop receiver

Figure 1.1: Hertz transmitter and receiver [23].

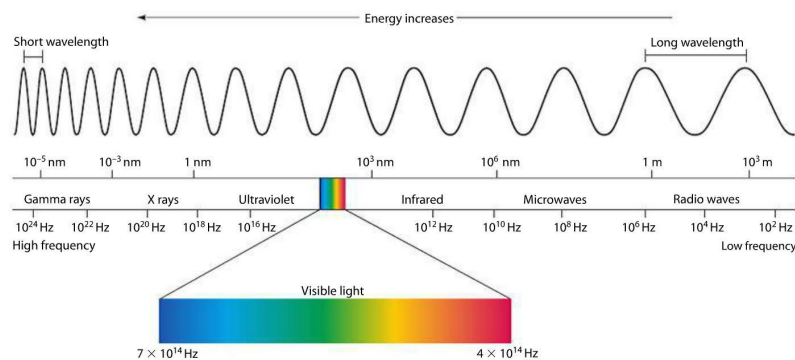
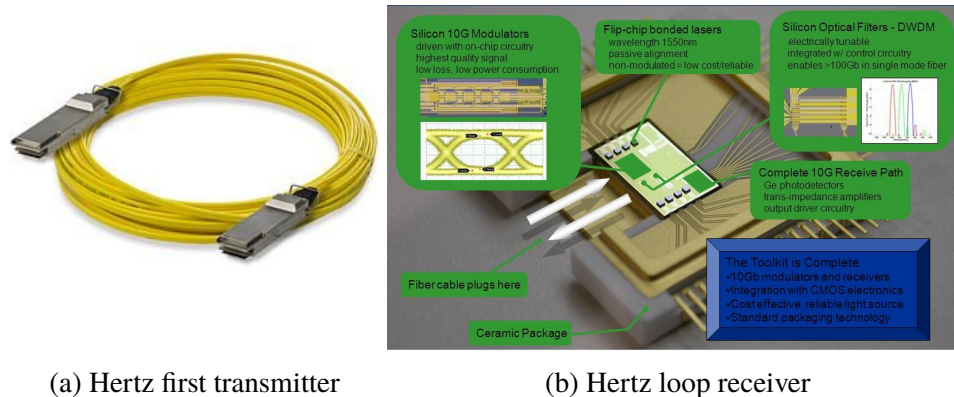


Figure 1.2: Electromagnetic spectrum

1988 allowed close to 40,000 phone conversations at the same time between Europe and North America. The high cost of deployment of optical links dropped rapidly as faster and cheaper optical modulators and photodiodes became available. The invention of EDFA in the end of the 1980s further reduced the cost of deployment of long-haul optical links.

As the Internet boomed in the late 1990s, many attempts were made to build local area networks out of optical fibers. The integration of laser and optical modulators had already brought the price of components down. However, the cost of deployment remained high due to time-consuming cleaning and aligning the connections. Multi-mode fibers (MMF) allowed lower cost deployment, but they lost the main advantage of single-mode optical fibers (SMF) which was the bandwidth. Soon optical fibers



(a) Hertz first transmitter

(b) Hertz loop receiver

Figure 1.3: Active optical cables marries the ease of use of copper cables with speed of fiber optics.

lost the battle to electronic systems that took advantage of Moore's law and provided a lower cost and more reliable solution for local area networks.

Soon researchers in optical communication realized that they could take advantage of Moore's law and beat the electronics in their own home turf with the use of Silicon on insulator (SOI) wafers. Silicon is transparent in the optical communication wavelengths of 1310nm and 1550nm and has much larger index of refraction compared to silicon dioxide, both are the materials that can be cheaply produced and precisely patterned. The large index contrast between silicon and silicon dioxide allows very tight confinement of light inside the silicon waveguide and having very small bend radii [88]. The cost reduction resulted from Co-integration of electronic circuits with photonic circuits on the same package or even on the same die as well as the increasing demand for higher data rates of server farms paved the way for a new category of optical interconnects called active optical cables (AOC) as it is shown in Fig. 1.3. These cables accept electrical inputs and outputs and perform the electro-optical and opto-electrical conversion in the connector. So from the end user they are no different than an electrical cable. This simplifies the use of the cables as no fiber cleaning and alignment is needed by the end user and hence the cost of deployment is reduced. One other benefit of these cables is that they can be designed to be compatible with electrical connectors such as Ethernet, Thunderbolt, or SFP++, but allow for much higher data rates over larger distances.

Silicon-photonics (SiP) applications is not limited only to transceiver applications. The platform enables realizing very complex optical systems in a single chip that can be easily mass produced with very low cost. Thanks to high precision lithography,

optical components can be fabricated with very tight tolerances and with very good matching to each other. Similar to electronic ICs where matching of elements is vastly utilized by designers, similar design techniques can be utilized in SiP to achieve systems that would be otherwise very complex or expensive.

It can be argued that one of the most prominent advantage of SiP platform is empowering the manipulation of light in nanometer scale level. This allows engineering the wavefront of light, and as will be presented later in chapters 4 and 5, it will be seen how this can create new systems that were not possible to make previously.

1.1 Contributions

The contributions of this work can be categorized into three main categories of photonics, electronics/antenna design, and combining electronics and photonics to obtain superior systems.

The following is a list of contributions in the photonics category:

- First demonstration of optical phased array transmitter with rapid beam steering capability.
- First demonstration of a lens-free projection system utilizing optical phased arrays.
- First demonstration of optical phased array receiver with heterodyne architecture.
- First demonstration of lens-free imaging with an optical phased array receiver.
- Demonstration of a 3D imager with highest measured depth accuracy.
- Resolving the bandwidth/quality factor trade-off of micro-ring resonators with a differential driven coupling modulation scheme.
- Footprint reduction of high-speed Mach-Zehnder (MZI) by wrapping the interferometer around itself in a spiral shape.
- Proposing a new design approach to increase bandwidth and power handling ability of Ge photodiodes in a standard SiP SOI process.

The electronic circuit design contributions encompass the work done in space solar power initiative (SSPI) which at the time of this writing is an on going project with

collaboration of Professor Harry Atwater and Professor Sergio Pellegrino research groups. The aim of the project is to harvest solar energy from space and transfer the power via RF waves generated by kilometer scale phased-array transmitter towards earth. Our group is responsible for RF power generation, phase and timing synchronization, antenna design, and RF power recovery. My contributions to this project can be summarized as follows:

- RF phase synchronization through design of a phase adjustable Clock Multiplier Unit (CMU).
- Design of SAR ADCs for on-chip calibration and sensing as well as digital control circuitry
- Design of rectennas for wireless power recovery with both off the shelf and CMOS integrated Schottky diodes.

The other contribution of this work in the electronic/electromagnetism category is proposal of new multi-port antenna. Below is a list of contributions associated with this proposed antenna structure:

- Proposal of the first proximity field power combining radiator, aimed to increase the radiation power density from an integrated circuit while reducing the optimum drive impedance, allowing higher power delivery from low voltage CMOS transistors.
- Design and fabrication of a tile-able transmitter with programmable phase control enabling the first hybrid nearfield/farfield power combination topology.

A holistic approach towards electronic and photonic circuits allows for creation of systems that can improve performance of either photonic or electronic circuits by taking advantage of what other technology better provides. For example, silicon photonics provide very high bandwidth low loss delay lines which can be used to improve the performance of electronic circuitry such as data equalizers. Below is a list of contributions that utilize this holistic approach in design:

- First demonstration of a self-equalizing photodiode which can be used to improve data rate of optical communication links.

- Laser linewidth reduction with dedicated ASIC .
- Frequency tunable mm-Wave generation through electro-optical mixing.

1.2 Organization

In the following chapters of the thesis, I will present a summary of my research over the last 6 years of my studies at Caltech.

In chapter II I will provide a background on integrated photonics with an emphasis on silicon photonics. Chapter III will present self-equalizing photodiode and adjustable self-equalizing photodiode design and measurement results. Optical phased array transmitter and receiver implementation and measurement results are presented in chapters IV and V, respectively. Chapter VI presents the integrated silicon photonic LIDAR imager.

In chapter VII I'll present a new approach and methodology to design on chip antennas targeted for high power CMOS radiators. A prototype implementation of such methodology is also presented. Chapter VIII summarizes the joint effort in SSPI project to provide globally available electricity produced from space.

The rest of my contributions in laser line-width reduction, electro-optical mm-Wave power generation and radiation, enhanced optical ring resonator based modulators, MZI modulator footprint reduction, photo-diode bandwidth improvements, and proposal and design of on chip optical tweezers are summarized in chapter IX. The conclusion of my thesis and future works are presented in chapter X.

Chapter 2

SILICON PHOTONICS: INTEGRATING COMPLEX OPTICAL SYSTEMS ON A CHIP

2.1 Photonics Integration on Silicon

As the demand for faster data links has increased over the last decade, the penetration of optical fiber communication has out grown from long haul continental and inter-continental to shorter haul networks in urban and rural networks. Since the main cost of such networks is dominated by the cost of deployment (excavation, fiber placement, etc.) there was no justification to further reduce the cost of the active devices such as optical transceivers, switches, and repeaters. The main motivation in such networks was and still remains to be to increase the data rate that can be sent through a single fiber. Traditionally this effort was focused on utilizing the full bandwidth available in optical fibers. As shown in Fig. 2.1. For long haul communication, this would be the window at around 1550nm due to availability of erbium doped fiber amplifiers and provides close to 11.5THz of bandwidth. This large bandwidth could not be utilized completely through a single channel, and hence multiple channels are used in wavelength multiplexing systems. Coherent modulation schemes such quadrature amplitude modulation (QAM) can be also used in each channel to increase the spectrum efficiencies and hence improve the data rates. In order to further increase data rate, multi-core fibers [145] have been introduced which allow incredible speeds well above 1Pb/s over a single fiber.

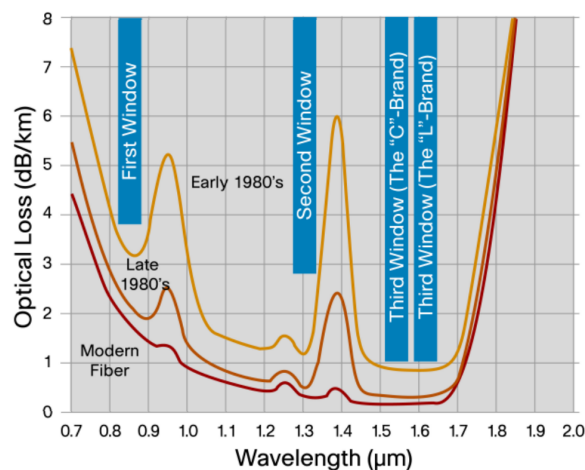


Figure 2.1: Optical fiber loss for different wavelengths [1].

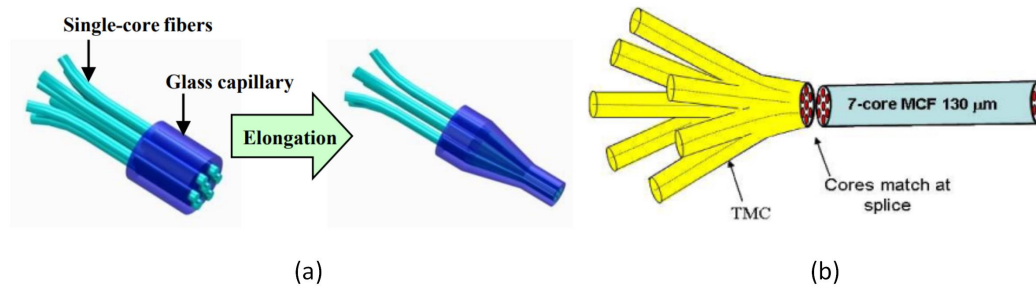


Figure 2.2: Connecting single mode fibers to multi-core fibers. (a) Creation of bundle [128] and (b) alignment needed for splicing [185].

These fibers as shown in Fig. 2.2 require very complex connector and splicing apparatus, but the cost of fiber deployment justifies the use such complex and expensive connectors and splicers.

The reliability and advantages of optical fiber links have now been completely proven by the several decade long deployment and utilization around the world and there is no doubt that fibers will replace copper in wide area networks such as urban networks. Almost no telecom service provider deploys copper based links anymore, and up until recently copper has only been limited to smaller networks such as within building and office networks, where the lower cost and difficulty of deployment does not justify the the use of optical links.

The emergence of cloud computing and cloud service providing has been a big game changing for optical link communications. The proliferation of such services has resulted in growth of large datacenters providing such services. Copper based links are not capable of providing the bandwidth-distance product that these data centers require, and hence optical links have become ubiquitous in such centers. Multi-mode (MM) fibers in conjunction with VCSEL based transmitters have been the dominant player in the market since the large optical core of the fiber requires less tolerance in alignment of laser to the fiber and fiber to fiber, which in turns results in lower price of components and ease of deployment. However, MM fibers suffer from mode dispersion and have a much lower bandwidth-distance product compared to single mode fibers. Multiplexing data in a single MMF is complicated. Mode division multiplexing requires complicated MIMO digital signal processing to deconvolve the crosstalk between the different modes, and is quite power hungry [142]. Also complicated setups are required to Multiplex the modes in and out of the MMF as shown in Fig. 2.3.

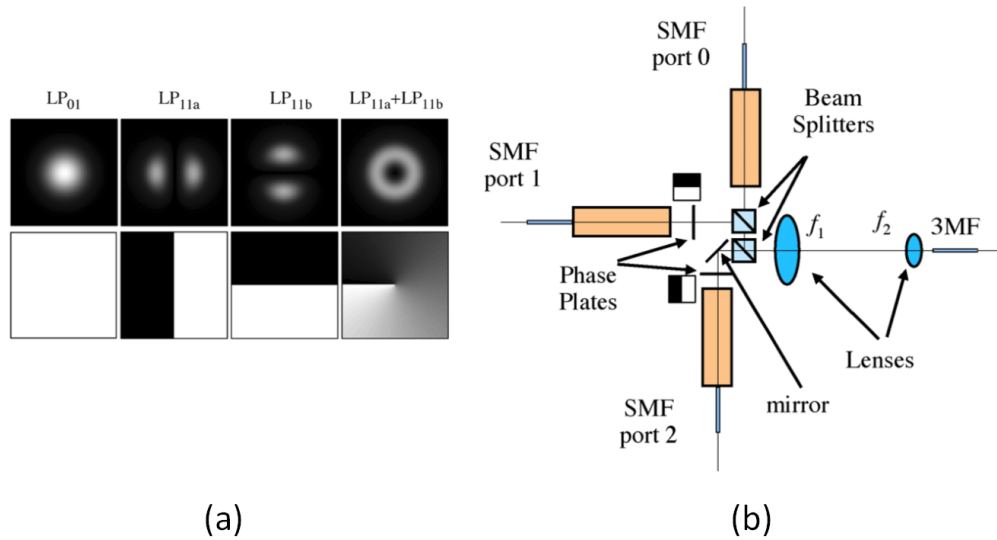


Figure 2.3: (a) Examples of amplitude (top) and phase (bottom) profiles of modes excited in a few-mode fiber for MDM. (b) Setup required to multiplex the modes in and out of the fiber [142].

As mentioned earlier, reliable high data rates through single mode fibers have been demonstrated through WDM and lately through spatial division multiplexing (SDM) and this has attracted interest to utilize same techniques in datacenters. Unfortunately the cost and complexity of such systems makes their use in datacenters prohibitive. Integrated photonics and especially silicon photonics have shown an attractive solution to the cost and complexity problem of high speed optical links. Integration allows one to make very complicated systems in large volumes with a very low cost and since silicon processing is quite advanced, thanks to large electronic industry based on silicon based ICs, it has been chosen as one of the industry platforms for integrated photonics. The precision of IC fabrication in silicon allows for higher yields of components and systems compared to other integrated platforms [159]. However, silicon has its own disadvantage for photonic processing as it does not have a direct bandgap and as a result generating photons is very inefficient on silicon. In the following parts of this section, I'll give brief overview of the different silicon photonics platforms and their advantage and disadvantages.

SiP on Bulk Silicon

If silicon photonics is intended to be fabricated along with bulk silicon electronic devices such as BJTs, this platform is the cheapest and easiest option. In this type of platform, the waveguides and other photonic components can be realized by

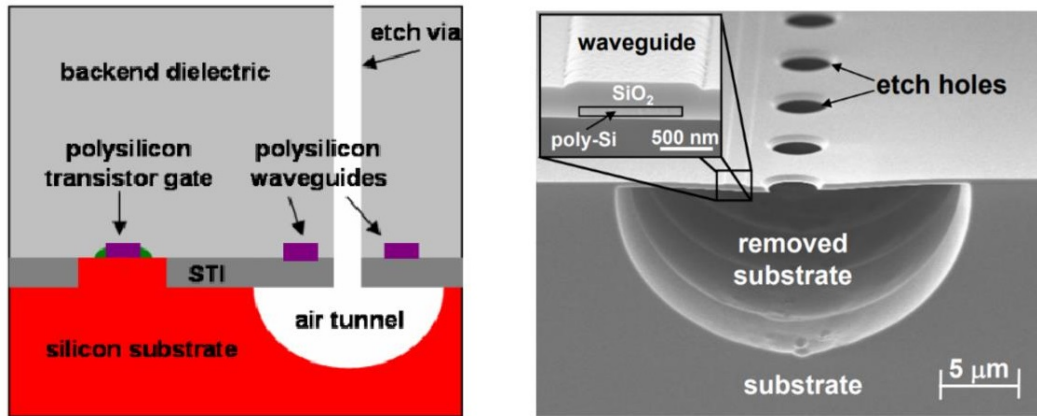


Figure 2.4: Removal of substrate to reduce leakage of light to the substrate [78].

deposition and etch of polycrystalline silicon [17, 78], deposition of amorphous silicon and later converting it to crystalline silicon [90], or deposition and etch of silicon nitride.

There are two challenges with the deposition of polycrystalline silicon as waveguides. One is the high loss of optical propagation in the waveguide, which occurs due to light scattering at the grain boundaries and absorption of light due to the dangling bonds on the surface of the grains [17], and the other challenge is the leakage to the substrate in CMOS processes, where the silicon oxide thickness (STI layer) under the the waveguides is not not large enough to prevent the leakage of light to the substrate[78].

There are several methods to reduce the loss of polycrystalline optical waveguides and some of them need to be applied concurrently. Surface polishing to reduce the surface roughness of the waveguides and hence reducing the scattering as well as hydrogenation of the waveguide to reduce the dangling bonds on the grain boundaries have been suggested as effective methods to improve the loss performance [17]. Even with these techniques losses are above 10dB/cm [90].

In order to improve the confinement of the light in the waveguide and reduce the leakage to the substrate, [78] proposes a method to remove the substrate underneath the polycrystalline waveguide. This method as shown in Fig. 2.4 can improve the loss to close to 10dB/cm for the polycrystalline waveguides.

It is possible to further reduce the loss of the silicon waveguide in a bulk process by converting the deposited amorphous silicon to crystalline silicon as proposed by [90]. The steps required to achieve this are shown in Fig. 2.5. First a trench is etched

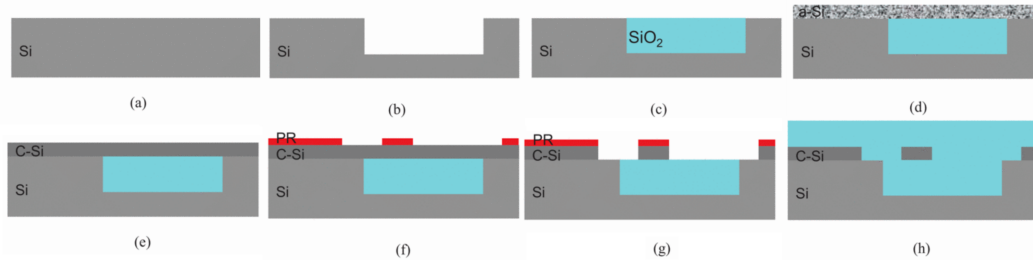


Figure 2.5: Creating single crystals from amorphous silicon to reduce the loss of optical waveguide [90].

in the bulk Si and is filled with silicon dioxide. After CMP and planarization, a thin layer of amorphous silicon is deposited on the surface of the wafer covering both the silicon and silicon dioxide regions. Through a process called solid phase epitaxy, the amorphous silicon is converted to single crystalline using the substrate as seed. Through this crystallization the loss of the optical waveguide can be reduced to around 6dB/cm, which is still higher than what can be achieved with SOI processes. Nonetheless, crystallization step requires extra thermal processing which may affect doping profiles and hence is not CMOS compatible.

The other option is to deposit silicon nitride (Si_3N_4) and use the index contrast between silicon nitride and silicon dioxide to confine light. The waveguides created by nitride may exhibit lower confinement compared to silicon due to lower index contrast; however, they can achieve very low loss of 0.1dB/m if bending losses are ignored [33]. Multiple layer of optical waveguides can also be formed using nitride and light can couple from one layer to other layer simply by running the two layers along each other (Fig. 2.6). The downside of using silicon nitride is that it is not a semiconductor so no fast modulator can be made out of it.

Silicon on Insulator Based SiP

Silicon on insulator (SOI) is the most widely adopted platform for silicon photonics. Soitec invented a method [16] to achieve well defined and high quality SOI wafers which is now widely used for silicon photonic platforms. Figure 2.7 shows the process steps of making SOI wafers. The fabrication of the SOI wafer involves two wafers. One is used as a substrate and the other is used to create the device layer on SOI process. The desired thickness of oxide layer under the silicon layer is first grown on the substrate wafer. The device wafer undergoes a heavy dose of proton implantation such that small cracks are formed underneath the device wafer surface. The device wafer is then flipped and thermally bonded to the substrate wafer. Due

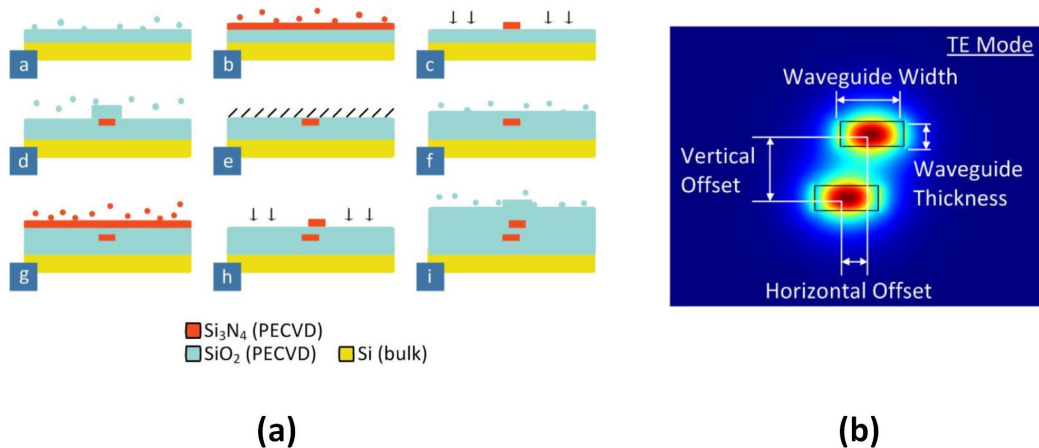


Figure 2.6: (a) A fabrication steps of a multi-layer silicon nitride optical platform and methods to couple light from one layer to the other layer [151].

to the presence of the cracks in device wafer, splitting the wafer results in leaving a thin layer of single crystalline silicon on the substrate wafer. After CMP polishing the desired thickness of silicon is obtained on the SOI process.

Waveguides are obtained in the SOI process by simply placing a photoresist where the waveguide needs to be and etching away the rest of the silicon. Low loss waveguides of 0.4dB/cm for single mode silicon waveguides [79] and extremely low loss of 0.026dB/cm [101] with multi-mode fibers can be achieved.

The SOI process also provides the ability to modulate the phase of light through a process called free carrier plasma dispersion, which allows fabrication of high speed modulators for optical links. Epitaxial growth of germanium on SOI enables integration of photodiodes on the same wafer. The availability of CMOS transistors on SOI processes implies that silicon photonic and electronic circuits can coexist on the same wafer as well.

SOI/Bulk hybrid SiP Platform

As mentioned in the previous subsection, SOI platform enables integration with CMOS electronic devices. Optical modulators, however, typically require large amplitude swings which can be well addressed with BJTs and HBTs. Also SOI process is not well suited for high power application as the oxide layer impedes the heat transfer from the transistors to the heat sink.

To address the mentioned issues, IHP (innovation for high performance Microelectronics) research center in Germany has developed a hybrid bulk/SOI process which

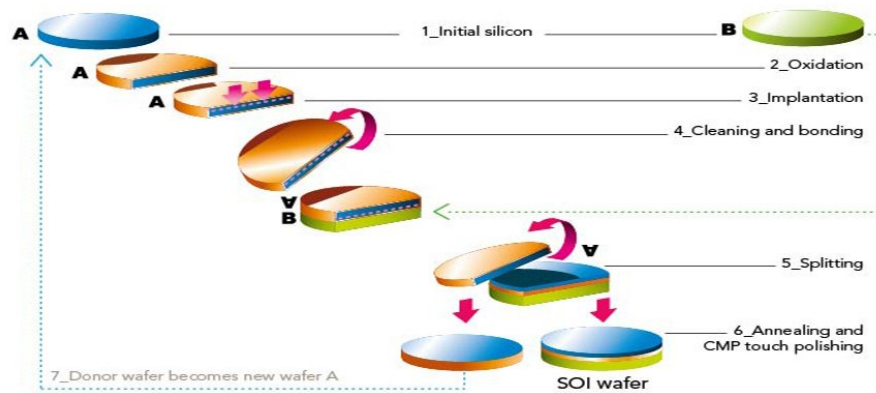


Figure 2.7: Fabrication steps for SOI wafers [6].

can accommodate high performance photonics as well as high performance high power SiGe HBTs. The cross section of the EPIC process is shown in Fig. 2.8. In this process the electronics and photonics circuits are developed in two separate partitions. The fabrication starts with an SOI wafer. The silicon and buried oxide (BOX) at the location where the electronic devices are to be placed are etched away and silicon is epitaxially grown until its height exceeds the height of BOX. A CMP process insures that the SOI and epitaxially grown layers are leveled. The transistors are fabricated in the epitaxially grown substrate (which is essentially a bulk region) while the photonic components are fabricated on the SOI partition. This process can achieve superior performance compared to solutions where electronics and photonics are in separate dies, since the length and capacitance of the RF lines is minimized.

Hybrid Si and III-V Platforms

One of the main deficiencies of silicon-photonics platforms is the lack of light source in silicon. Since silicon does not have a direct band gap, it is not possible to make efficient laser diodes in silicon. Although there has been reports of all silicon lasers [39, 141], they rely on optical pumping of the silicon which still necessitates an off chip light source.

While an off chip light source may be used with silicon photonics, integration of lasers on SiP reduces the number of fibers that needs to be connected to the chip and hence reduces the cost of fabrication. A solution to integrate laser on SOI process is to epitaxially grow III-V semiconductors on silicon. The lattice mismatch between

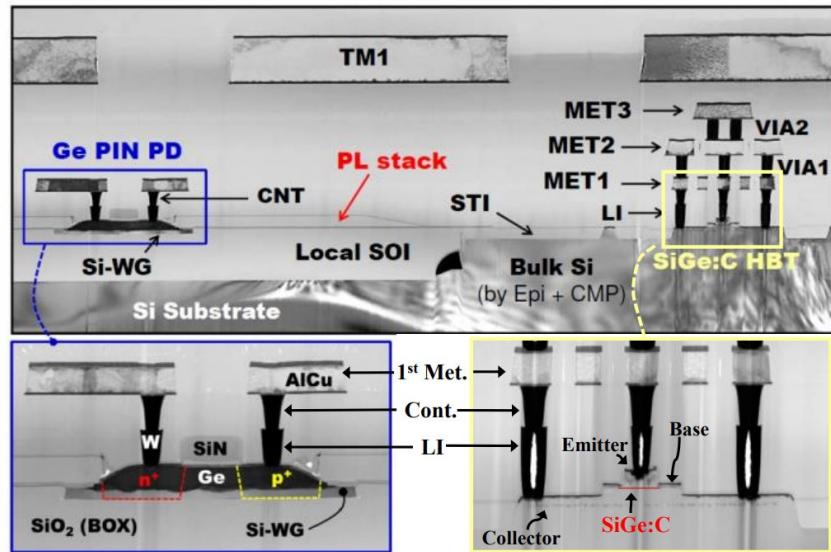


Figure 2.8: Cross section of EPIC process developed by IHP [106]. In this process both bulk SiGe/CMOS devices and SOI photonics structures are integrated.

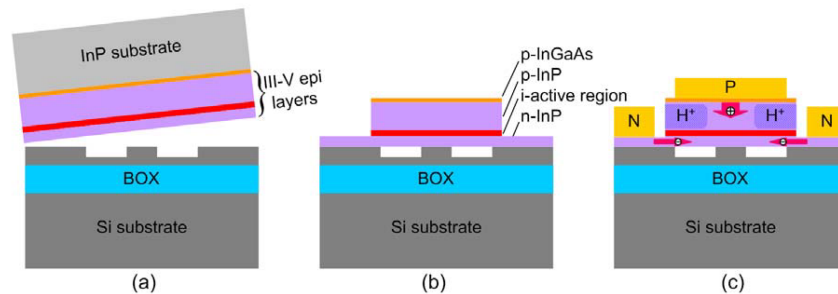


Figure 2.9: Process of (a) bonding (b) etching and (c) contact formation in a III-V gain medium on SOI process. No stringent alignment during placement is required [103].

the two semiconductors results in high dislocation rates which reduces the yield of process. The other approach is to bond a III-V electrically pumped gain medium onto a SOI process and form the laser cavity on silicon platform [103]. The bonding can be done either at wafer level or with individual devices. No stringent alignment accuracy during the placement is needed if the unprocessed III-V substrate is placed first and processing is performed afterwards (Fig. 2.9). Since the laser cavity is formed on silicon process, by designing cavities that are resonant at non overlapping wavelengths, it is possible to create lasers that are tuned at different wavelengths for WDM transceivers [18].

2.2 Devices and Components Available in Silicon Photonics

Waveguides

Waveguides are the fundamental block in silicon photonics. They allow routing the optical signals from one point to another point. Due to very high frequency of optical signals, metallic waveguides are quite lossy due to skin effects and dielectric waveguides are the only option for integrated photonics. One of the main characteristics of waveguide that needs to be considered during the design is the number of modes that the waveguide supports for a given wavelength. Multimode waveguides are typically avoided in designs unless they are specifically needed for their special properties such as lower loss or when mode conversion is needed. Single mode waveguides can be designed with different width/heights and they come with different flavors of strip and strip loaded waveguides as shown in Fig. 2.10. Among the parameters that need to be considered during design are the waveguide loss due to surface roughness, the confinement of the optical mode (i.e. how packed the waveguides can be routed without noticeable coupling), the minimum bend radius that can be achieved, the ability to apply electrical field to the optical mode, etc.

The main contributors in the loss of silicon waveguides are surface roughness, free carrier absorption, mode coupling to the substrate, or the metal routing on top of the waveguide. Strip loaded and wider (multimode) waveguides are less affected by the surface roughness and hence have typically lower loss[127].

Adiabatic tapers can be used to attach different types of waveguides to each other. These tapers which are several wavelengths long, and gradually change the optical mode from one waveguide to the other to avoid excessive loss due to scattering or back reflection. Usually the longer the taper, the better they become. In applications where the length of the taper needs to be kept short, optimizing the taper can allow for shorter tapers, but typically the bandwidth of operation is sacrificed.

Fiber to Chip Couplers

No matter how complex of an optical system can be implemented inside a chip, there is no use for such a chip if an effective and robust way to couple light in and out of the chip does not exist. There are two approaches for coupling light in and out. One is to use edge couplers in which the light is emitted in parallel with the surface of the chip and a lensed fiber is placed on the edge of the chip, similar to the one shown in Fig. 2.11(a) and the other approach is to have surface emitting grating couplers (Fig. 2.11) which emit the light in angle close to normal to the surface of

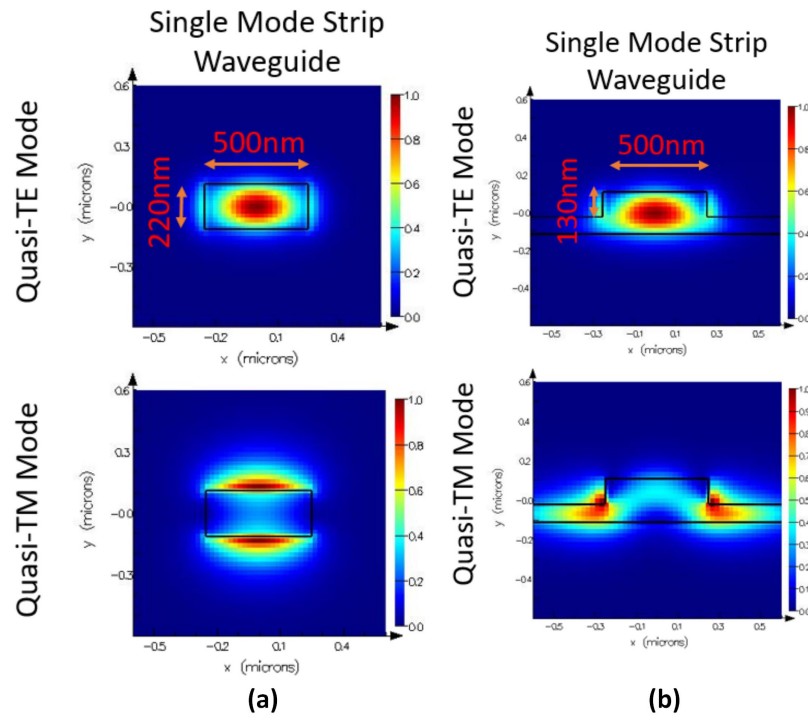


Figure 2.10: (a) Single mode strip and (b) strip loaded waveguides and the profile of quasi TE/TM modes that it supports.

the chip and the fibers are placed and glued on the surface of the chip as shown in Fig. 2.11(c).

Edge couplers provide a lower profile assembly and have relatively low coupling loss and are polarization independent; however, they require more footprint on the PCB. Grating couplers provide a smaller footprint, allow coupling to fiber from any location on the chip, wafer probing, and they also allow use of arrays to densely couple multiple fibers to the chip, but the coupling efficiency is typically polarization dependent and the packaging height is not small and they have lower optical bandwidth compared to the edge couplers.

Power Splitters/Combiners

In order to split optical power into multiple paths or combine the optical power arriving from multiple paths, several structures can be used. Of the most widely used ones are Y-junctions, MMI couplers, and directional couplers, which are shown in Fig. 2.12.

A Y-junction is simply formed by tapering the waveguide to a thicker waveguide and then splitting off from the middle. In order to achieve low loss and reflection from the

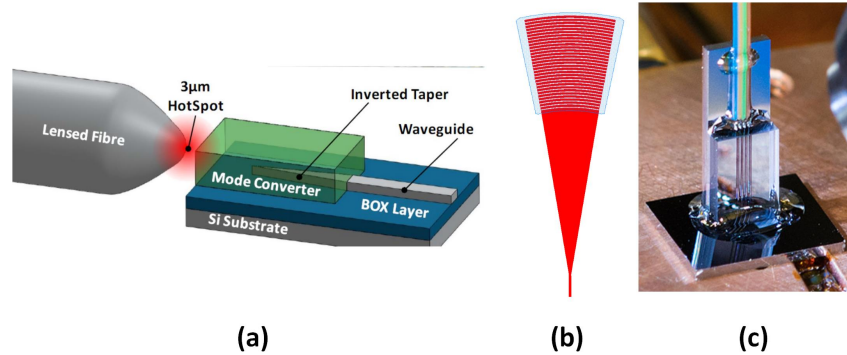


Figure 2.11: Chip to fiber couplers. (a) Edge coupler [44] (b) grating coupler layout and (c) packaging [5].



Figure 2.12: (a) Y-Junction, (b) MMI coupler, and (c) directional coupler

Y-junction, the taper needs to be long and gradual. Given an input of $E_{in} = A_{in}e^{j\omega t}$ to the left port (single input side), the outputs of a symmetric Y-junction will have the same power and phase of $E_{out} = \frac{\sqrt{2}}{2}A_{in}e^{j\omega t+\phi}$. On the other hand if the light enters from only one of waveguides on the right hand side of Fig. 2.12(a), half of the power exits from the port on the left and the other half is scattered out. Y-junction are very wide band and tolerant to process variations and as a result are the choice for splitting/combining optical power.

MMI and directional couplers are 4-port devices and the light entering from one port will exit from the other ports with equal power but with 90° phase shift with respect to each other. If equal optical power enters from two ports on one side of these couplers, depending on the phase relation between the ports, optical power can be steered from from one port to other. MMI coupler are very useful when robust equal split by two are needed, but their loss is wavelength dependent. Directional couplers allow for a controllable split ratio and are more wide band, however, their performance is highly dependent process variations. Any change in the gap or the thickness of the grating coupler will affect the coupling ratios. Finding the right dimensions for robust directional couplers has been a topic of research [117].

Optical Crosses

Most of silicon photonics platforms only provide one layer of photonic waveguides. In some photonic layout topologies and applications such as gyroscopes [157] it is not possible to route the optical signal without any crossings. Fortunately there are designs that allow very small form factor crosses with low loss and high isolations [34, 108].

Modulators

Optical modulators allow manipulation of amplitude and phase of light. Phase modulators typically rely on changing the index of refraction of the waveguide and amplitude modulators rely on either changing the loss of the waveguide or utilize interferometry to convert phase modulation to amplitude modulation.

Phase Modulators

Most of integrated optical phase modulators rely on changing the effective index of the waveguide or part of the waveguide. The phase shift that is introduced is proportional to the amount of index change and the length of the waveguide. If the index of refraction of waveguide of length L is changed by Δn , the optical phase of light traveling through the waveguide changes by:

$$\Delta\phi = \frac{2\pi L}{\lambda_0} \Delta n \quad (2.1)$$

where λ_0 is the free space wavelength of the optical signal.

There are three methods to modify the index of refraction of a semiconductor:

- **Change of Temperature:**
Silicon index of refraction has a relatively high temperature dependency with a thermal coefficient of around $1.8 \times 10^{-4} K^{-1}$ at $\lambda_0 = 1550\text{nm}$ [102]. This property of silicon while disadvantageous in temperature invariant designs is very useful for making compact phase shifters.
- **Free carrier plasma dispersion:**
The light in a doped semiconductor waveguide interacts with the free carriers in the semiconductor. The result of this interaction is a change in the absorption spectrum as well as index of refraction of doped semiconductor compared to the un-doped semiconductor [125]. Electrons and holes interact differently and have different equations for the change of index. The change of index of

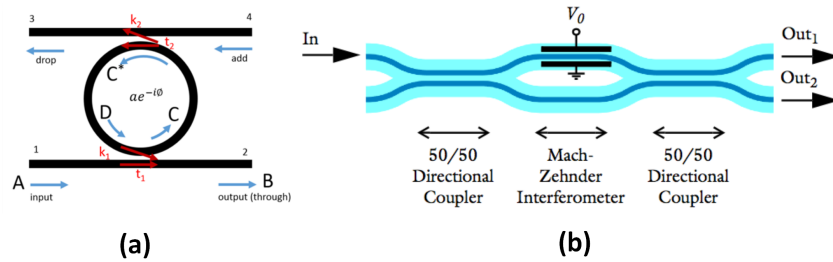


Figure 2.13: (a) Ring resonator [3] and (c) MZI modulator [4].

refraction due to electrons, Δn_e , and holes, Δn_h , can be written as [155]:

$$\Delta n_e = -8.8 \times 10^{-22} \Delta N_e \quad (2.2)$$

$$\Delta n_h = -8.5 \times 10^{-18} (\Delta N_h)^{0.8} \quad (2.3)$$

where ΔN_e and ΔN_h are the change in the free electrons and holes, respectively.

- **Non-linear effects** The index of refraction of a non-linear material can be changed by applying a strong electric field across it. Of the non-linearities that can be used, Pockels effect is most desirable for phase modulators as it provides a linear phase shift versus the applied voltage. Silicon has a center symmetrical crystalline structure and as a result the Pockels effect in silicon is negligible. However, applying strain on the silicon film of SOI through deposition of silicon-nitride will introduce asymmetry in the crystalline structure and introduces Pockels effect which can be utilized for phase modulation [50]. Depositing non-linear polymers on slot waveguides have also been utilized for high frequency phase modulation [19].

Amplitude Modulators

High speed amplitude modulators are replacing VCSELS and LEDs for on-off keying optical modulations. The speed that a laser can be turned on and off depends on the photon life time in the laser cavity and is becoming a bottle neck in high speed optical links. Amplitude modulators can provide higher speed of operation. Amplitude modulators can be categorized based on their method of operation into two categories. The first category utilizes the change in index of waveguide to modulate the amplitude and the other one directly modulates the amplitude by changing the absorption coefficient of the waveguide.

Ring resonator based modulators and Mach-Zehnder interferometers (MZI) use the change of index to modulate the light amplitude. A ring resonator is shown in Figure 2.13(a). The resonance frequency of the ring depends on the dimensions of the ring as well as the effective index of refraction of the waveguide. Changing the effective index of refraction will change the resonance frequency. If the laser wavelength is set at the resonant frequency, the intensity of the light coming out of through port or the drop port changes when the resonant wavelength of the resonator is changed. Similar to modulation of lasers, the speed of a ring modulator is limited by the photon lifetime of in the ring. In chapter IX we present a new ring modulator whose bandwidth is not limited by the photon life time in the ring. The other drawback of the ring resonators is that they require tuning of the resonator such that it aligns with the wavelength of the laser and this adds complexity; however, ring resonators are favorable in many applications for their small size and low power consumption.

A simplified block diagram of MZI modulator is shown in Fig. 2.13. In an MZI, the input light is split in two paths, in each path experiences a phase shift and then is recombined. Depending on the phase shift that is introduced, the output light can switch from one output of the directional coupler to the other. By placing a fast phase modulator in one or both paths (arms) of MZI, an amplitude modulator is obtained. Depending on type of phase shifter used, MZI modulators can have a length from several hundred micrometers to several millimeters. For high speed applications, the RF electrode design needs to take into account the traveling time of photon through the phase shifter such that the RF signal is phase matched with the modulated optical signal traveling through the phase shifter.

It is also possible to directly modulate the amplitude of light by changing the absorption coefficient of the waveguides. Free carriers not only create a phase shift, but they also result in absorption; however, to achieve noticeable extinction ratios, long modulators are needed which reduce the bandwidth of operation. Another approach is to use Franz-Keldysh effect or quantum confined stark effect which essentially modify the bandgap of a semiconductor through application of strong electrical fields [138]. For SOI process, Ge or SiGe semiconductors are the choice for utilizing this effect around 1550nm. If a pure Ge structure is used, the electro-absorption effect is most present at around 1615nm [71], while adding Si to Ge will increase the bandgap of semiconductor and allow for operation at lower wavelengths [156]. Very high speed and compact amplitude modulators can be obtained using Franz-Keldysh effect but they require extra processing steps for fabrication.

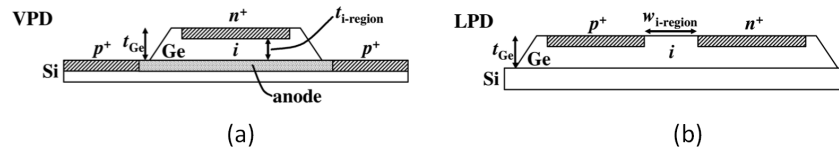


Figure 2.14: Ge based photodiodes in SOI process. (a) Vertical and (b) Lateral designs [105].

Photodiodes

Photodiodes are important part of any electro-optical system and are responsible to convert optical signals to electrical ones. While silicon photodiodes are widely used in CMOS cameras, they cannot be used in a SiP SOI process since the wavelength of interest in SiP platform is chosen above the bandgap of the silicon so that silicon is transparent and can be used as waveguides. In order to detect optical signal a material with smaller band gap is required. Ge is well suited since the lattice mismatch of 4.2% can be addressed by introducing SiGe buffer layers [175].

Two possible implementation of Ge photodiode are shown in Fig. 2.14. Germanium has a higher index of refraction compared to silicon hence the light entering the Ge PD will be mainly confined on the top Ge layer and will produce electron-hole carriers. In the vertical structure, the generated carriers are swept vertically while in the lateral one, they are swept horizontally. The carriers in the vertical structure travel shorter path and have smaller transit time; however, the electrical series resistance to the junction (anode side) and junction capacitance is higher compared to the lateral structure. In chapter 9 I will introduce a special case of lateral PD which is targeted to low transit time and higher power application.

SELF-EQUALIZING PHOTODIODES

3.1 Necessity of Channel Equalization

One of the greatest challenges in increasing optical data transmission rates is the inherent bandwidth limitations of electrical and electro-optical components of the communication link. In a bandwidth limited data transmission link, the high frequency components of the transmitted data generally get attenuated more than the lower frequency components of the spectrum. The result of this bandwidth limitation is often closed eye diagrams on the receiver side where it will be more challenging for the receiver circuitry to recover the data.

The problem of channel bandwidth limitation is well studied [27, 135], where low bandwidth electrical transmission lines are used, bandwidth limited distortion of the signal has been addressed through equalization techniques. These techniques essentially restore the signal by introducing a high-pass filter into the data link. The role of the high pass filter is to balance the ratio of the high frequency components to the low frequency components of the received signal. Since the bandwidth limitation in wireline communication is mainly dominated by the channel and not the electronic

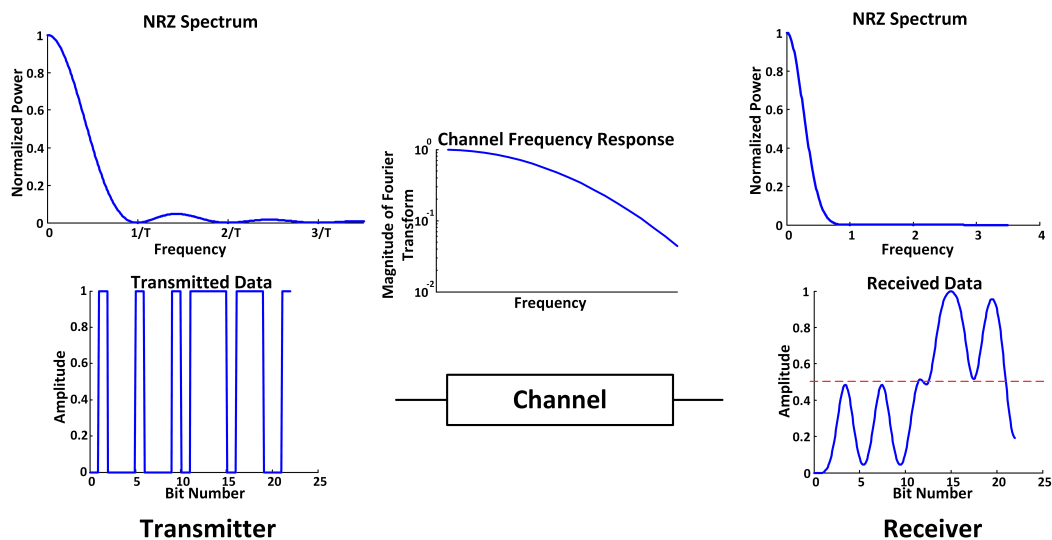


Figure 3.1: Effect of bandwidth limited channel on the transmitted data. A simple threshold based data recovery is not possible after removing the high frequency content of the signal.

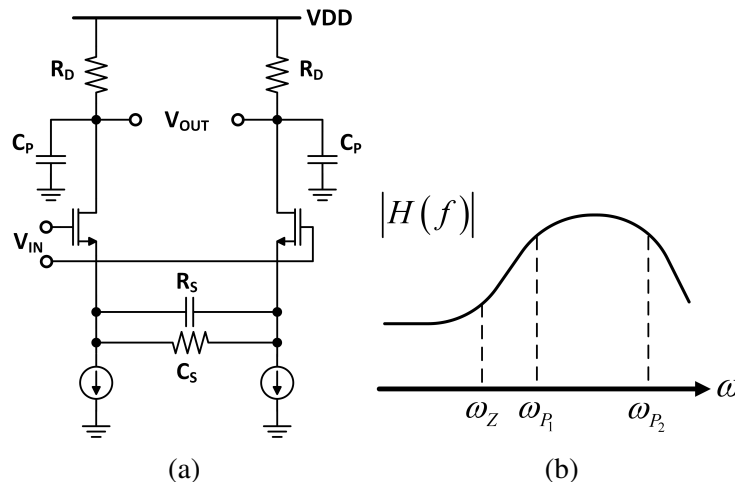


Figure 3.2: (a) Example of equalizers implemented in electrical domain [68]. (b) Typical transfer function of electrical equalizers. Due to parasitic capacitances, such equalizers are band-limited.

circuitry, the equalizers can easily be implemented in the electronic circuitry. In optical links, however, the bandwidth limitation arises from the electronic circuitry and the electro-optical components. In such systems, implementing equalizers in already bandwidth limited electronics is challenging and thus equalizers need to be implemented in the optical domain, which can suffer from its own shortcomings. In this chapter, we present a hybrid electro-optical approach for equalizing the receiver signal in the photo-diodes of an optical link. Section 3.2 provides a brief background on the effects of bandwidth limitation on data transmission and how equalization overcomes these effects. Section 3.3 explains our proposed hybrid electro-optical approach. Measurement results are presented in section 3.4, and the chapter is concluded in section 3.5.

3.2 An Overview of Equalization Techniques

The data transmitted through a band limited channel will lose most of its high frequency content. This effectively smoothens the received data waveform. If the bandwidth of the channel is much smaller than half of the symbol rate, the received data will be distorted to the extent such that a simple threshold based data estimator will not work (Fig. 3.1). By implementing a high pass filter in the transmitter side, receiver side, or both, it is possible to reverse the distortions caused by the band-limited channel. In wireline communications, high-pass filters in the transmitter side will increase EMI to adjacent channels, while in WDM systems, it will increase the crosstalk between the channels if not enough guard band is put in place. On

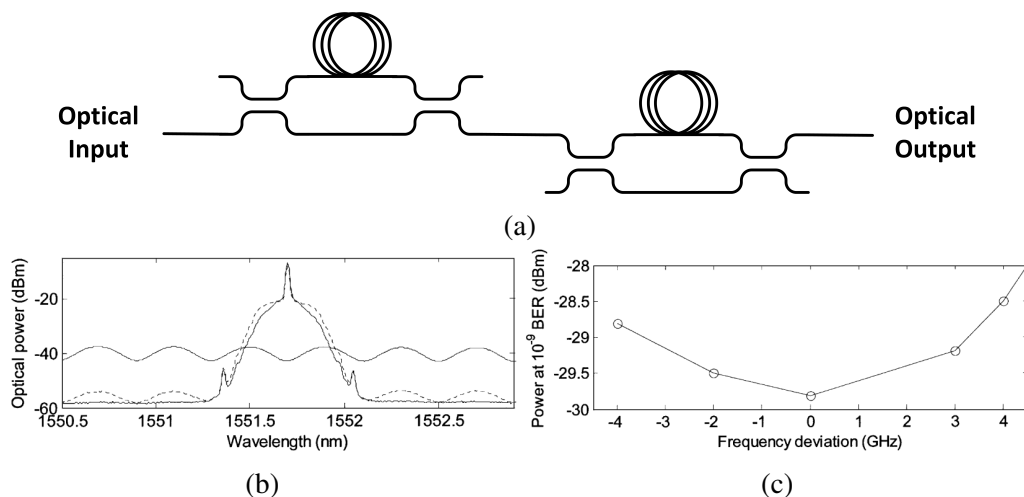


Figure 3.3: (a) An example of optical equalizer implementation [56]. (b) Measured optical spectra of the modulated signal without (solid line) and with (dotted line) equalization. The sinusoidal line shows the transmissivity through the equalizer. (c) Equalizer sensitivity vs. laser frequency deviation [56].

the other hand, placing the high pass filter in the receiver side will deteriorate the sensitivity of the receiver. This is because the high pass filter attenuates the lower frequency components of the signal to level the overall frequency response, and as a result the overall signal power will be lowered relative to noise. This reduction in overall signal to noise ratio can be somewhat mitigated by placing an amplifier before the equalizer.

In an optical data communication link, the receiver equalizer can be placed either in optical or in electrical domain of the receiver. An examples of equalizer implemented in the electrical domain is shown in Fig. 3.2a [68], where the high-pass filter is integrated with the amplifier to form an active high-pass filter. The electrical amplifier has a limited bandwidth and as a result the frequency response starts to drop beyond a certain frequency (Fig. 3.2b). In summary, the equalizer implemented in the electrical domain benefits from tunability, flexibility, and the ease of amplification of the signal before equalization; however, such an equalizer is limited by the bandwidth of the technology used.

An optical equalizer, on the other hand, can enjoy the wide bandwidth of the optical system [56, 57, 67]. An example of optical equalizer reported in [56] is shown in Fig. 3.3a where an optical filter is formed using Mach-Zehnder Interferometer (MZI) structures. The optical filter produces a sine wave shaped response and by setting the center of the valley of the response to the laser wavelength (carrier

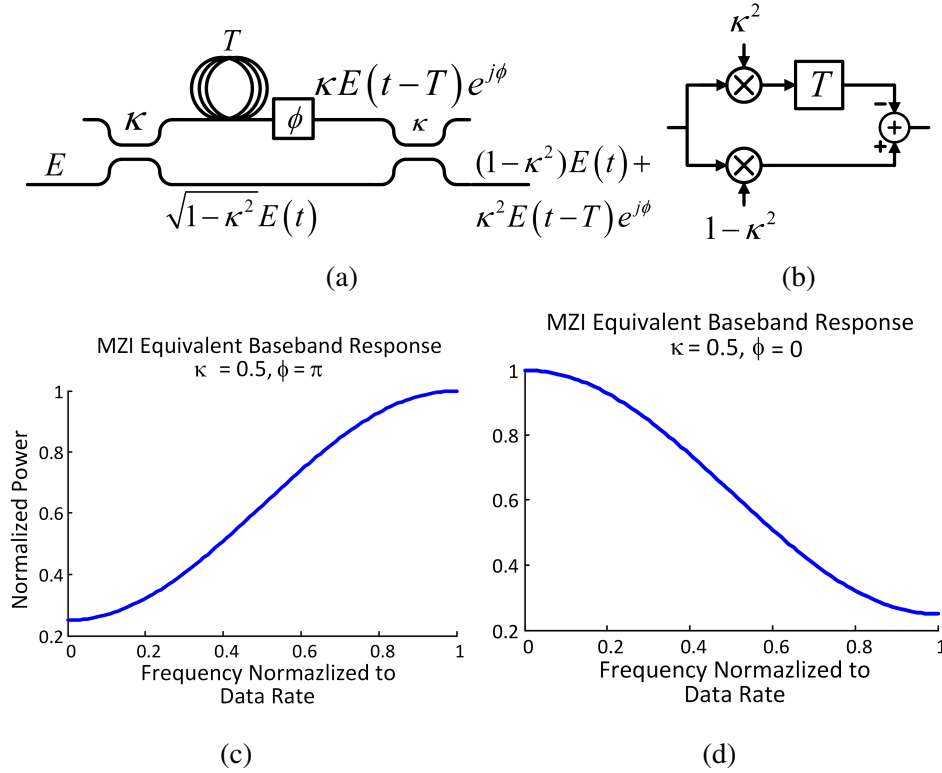


Figure 3.4: (a) Example of an FIR optical equalizer implementation. (b) Block diagram of the desired filter. (c) An example of desired response. (d) Undesired response of same implementation due to laser wavelength drift.

frequency) it is possible to equalize the data transmission (Fig. 3.3b). As shown in Fig. 3.3c, the equalization is sensitive to deviation of frequency of the laser or drift in the optical filter. As a result, tight temperature control loops are required to assure minimal frequency deviation of the laser and the filter. We will briefly analyze the operation of an MZI based optical equalizer to explain the source of the sensitivity of the optical equalizer to frequency deviation of the laser.

The high-pass filter for an optical equalizer can be easily implemented with an MZI structure acting as an FIR filter. Such a filter as shown in Fig. 3.4b equalizes the received signal by subtracting a proportion of delayed version of the input signal from the non-delayed proportion. An optical waveguide can provide the delay, while the subtraction is done in the right hand side coupler of the MZI shown in Fig. 3.4a. If the output of the MZI is fed to a photo-diode the output current, I_{out} , would be:

$$I_{out} = R \left[\left(1 - \kappa^2\right)^2 P(t) + \kappa^4 P(t - T) + 2\kappa^2 \left(1 - \kappa^2\right) \sqrt{P(t)P(t - T)} \cos(\phi) \right] \quad (3.1)$$

where R is the photo-diode responsivity, $P(t)$ is the input optical power, κ is the

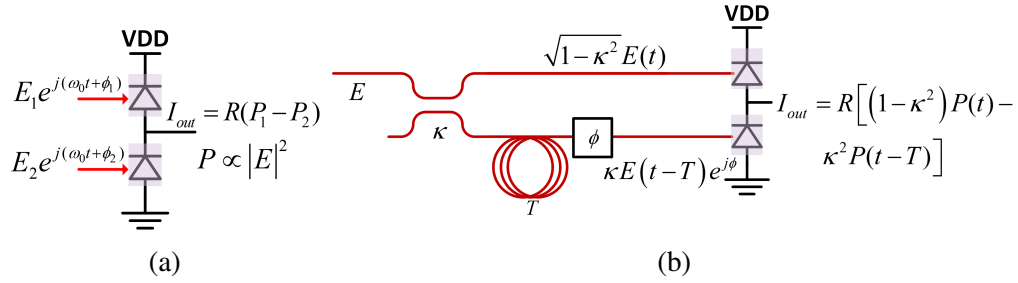


Figure 3.5: (a) Optical phase independent subtraction by using photo-diodes. (b) A carrier wavelength insensitive hybrid electro-optical equalizer.

coupling coefficient of the coupler in the MZI, T is the delay of the waveguide, and $\phi = \omega_0 T$ is the phase shift associated with the delay line at laser frequency, ω_0 .

This presents several challenges. First the profile of the response cannot be fully controlled, leading to suboptimal results. Second, the frequency response of the equalizer is dependent on ϕ . Two examples of equalizer frequency response are shown in Fig. 3.4c and 3.4d for $\phi = \pi$ and $\phi = 0$, respectively. For $\phi = \pi$, the combiner properly subtracts the delayed version of the input from the non-delayed version and hence the equalizer acts as a high-pass filter, as intended. However, if due to frequency drift of the laser, ϕ becomes zero, the combiner adds the two optical signals and as a result, the frequency response of the equalizer becomes a low-pass one. Due to process variation in fabrication and temperature fluctuations, the exact effective index of an optical waveguide and hence the value of ϕ cannot be determined *a priori*, and hence control loops are required to assure $\phi = \pi$ for the operating wavelength. In the following section we describe how to resolve the laser wavelength dependency of the optical equalizer by proposing a hybrid electro-optical approach.

3.3 Design and Implementation

As mentioned in the previous section, the root cause of the wavelength dependency of the equalizer is the optical combiner, where subtraction of the delayed signal from non-delayed signal is sensitive to the wavelength drift of the laser. In order to remove this sensitivity, we propose to convert the optical signals to an electrical signal through a photo-detector and then perform the subtraction in the electrical current domain. A photo-diode produces a photo-current proportional to its input optical power, irrespective of the input optical phase. Subtraction of the delayed signal from the non-delayed one can be done in current mode by simply connecting

the output of photo-diodes to the same node such that one sources current while the other sinks it, as shown in Fig. 3.5a. By removing the right-hand side combiner of equalizer in Fig. 3.4a and substituting it with a photo-diode based subtraction circuit a hybrid electro-optical equalizer is achieved. The output current of the equalizer shown in Fig. 3.5b can be written as:

$$I_{out} = R \left[\left(1 - \kappa^2\right) P(t) - \kappa^2 P(t - T) \right] \quad (3.2)$$

As it can be seen from the equation, the frequency response of the equalizer in this case is not dependent on the carrier laser wavelength. It should be noted that carrier wavelength sensitivity of the equalizer is not completely removed as the coupling factor of the directional coupler, κ , which sets the equalization strength, is still wavelength dependent; however, this dependency is significantly lower than what is achievable with purely optical equalizers. Also there exist approaches that increase the bandwidth of the coupler and reduce the wavelength sensitivity [48, 179]. As a proof of concept we developed two different equalizers [8, 11] in a silicon-photonics platform provided by IME. The details of the platform is provided in [159]. The system integrates all the equalization functionalities as well as optical to electrical conversion in one chip, and hence it can be viewed as a self-equalizing photo-detector (SEPD).

The block diagram of the implemented prototype is shown in Fig. 3.6a. The input optical signal is split by a ratio of 23/77 by the first directional coupler. The larger portion of the split enters a photodiode without further added delay while the smaller portion passes through a 50ps delay line before splitting by another directional coupler with split ratio of 34/66. The thru portion of the coupler directly enters the second photodiode while the coupled portion is further delayed by 50ps before opto-electrical conversion. The electrical current produced by the delayed optical signals is subtracted from the current produced by the zero-delay optical signal, resulting in a signal flow diagram shown in Fig. 3.6b. The frequency response of the equalizer can be written as:

$$I_{out} = C_1 - C_2 e^{-j\omega T} - C_3 e^{-2j\omega T} \quad (3.3)$$

where $C_1 = RP(1 - \kappa_1^2)$, $C_2 = RP\kappa_1^2(1 - \kappa_2^2)$, and $C_3 = RP\kappa_1^2\kappa_2^2$ are set by the coupling coefficients, κ_1 and κ_2 , of first and second directional coupler, respectively.

In order to minimize the number of photo-diodes and hence the capacitive loading of the output node, a dual input photo-diode (DIPD) is proposed. The structure of

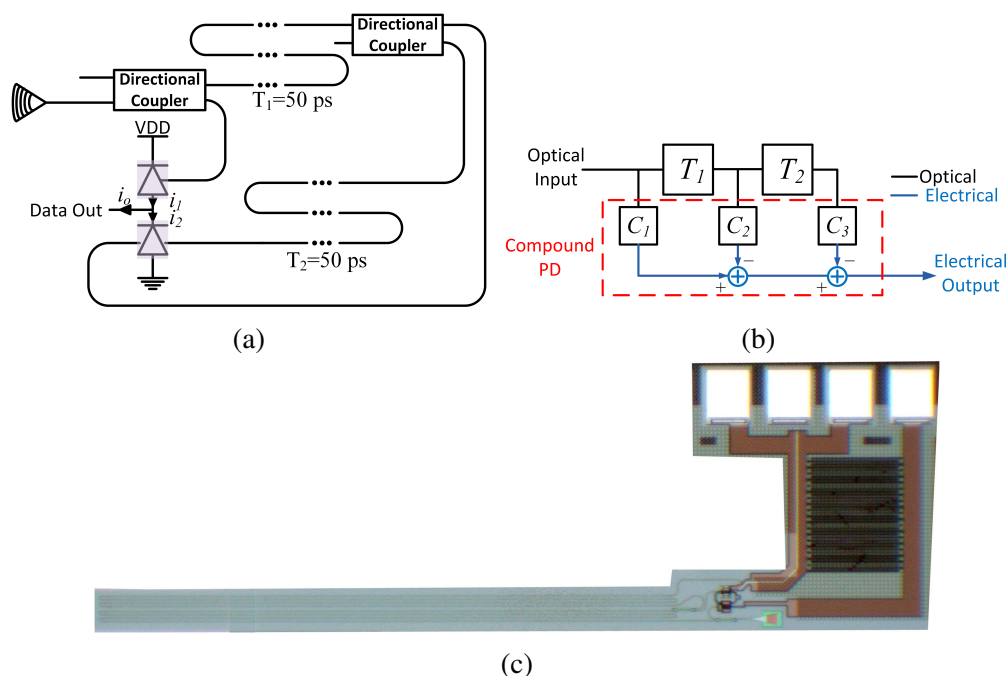


Figure 3.6: Implemented 2-tap self-equalizing photo-detector. (a) The block diagram. (b) Equivalent signal flow diagram. (c) Die photo of the implemented IC.

a dual input photo-diode is shown in Fig. 3.7a. The vertical buildup of the diode is similar to the single input work reported in [126]. By adding a second optical input in the opposite direction of the first optical input, it is possible to effectively sum the optical power of the two signals and convert them to electrical current within one photo-diode structure, cutting the overall junction capacitance on the summing node by half. The relative phase of the optical signals has no effect on the output current, as the optical signals travel in the opposite directions of each other.

While the SEPD provides a simple solution to improve the bandwidth of communication channel and hence increase the data rate, it does not allow for dynamic bandwidth adjustment. In order to provide a more flexible solution and to be able to adjust the bandwidth enhancement of the equalizer, programmable coupling factors are required. Also, to be able to equalize a more variety of data rates and channels, a larger number of taps with smaller delays must be utilized.

To adjust the frequency response of the equalizer, the tap coefficients of the FIR filter need to be programmable. This can be easily achieved by dynamically controlling the intensity of light incident on each photodiode. A thermally controlled MZI 1×2 optical switch is used to dynamically control the optical power flow [7]. The

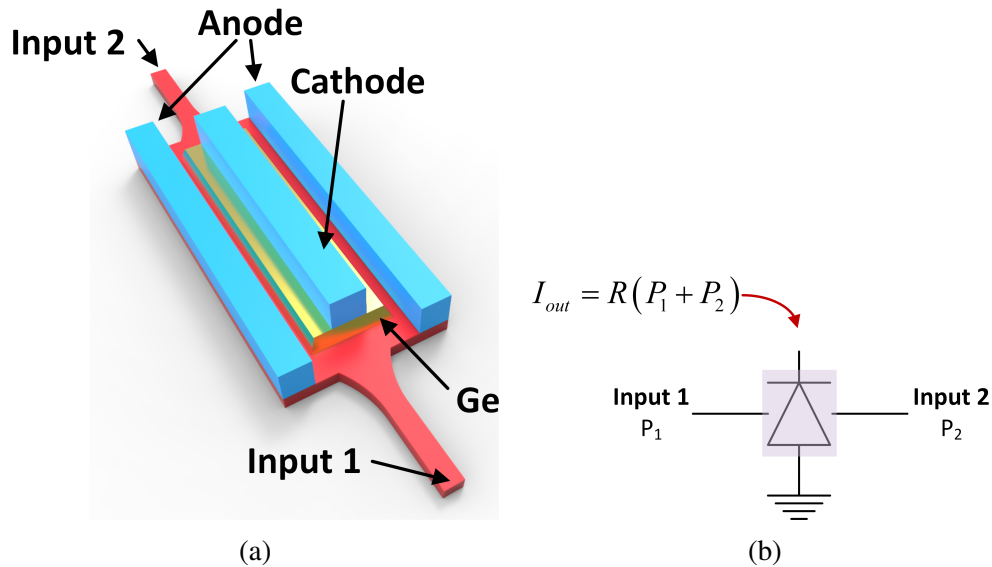


Figure 3.7: (a) Dual input photo-diode and (b) its symbol. Optical power of two signal is summed and converted to electrical current within one junction.

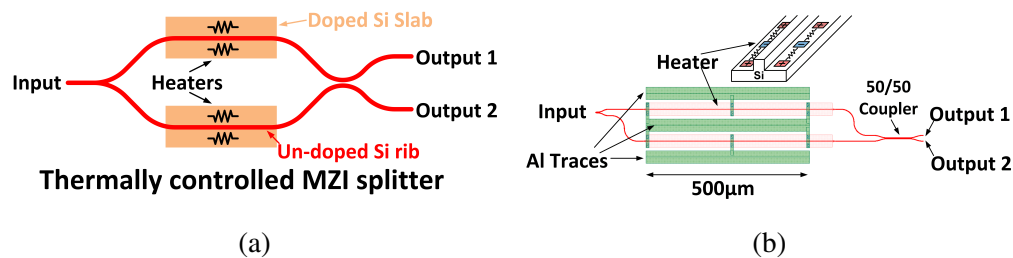


Figure 3.8: Dynamic tap coefficient adjustment with a thermally controlled MZI. (a) Schematic diagram of the MZI and (b) the corresponding layout. Heaters are implemented by doping the slab section of the waveguide and passing current through them.

schematic and layout of the thermally controlled MZI is shown in Fig. 3.8. The input power is split between the two outputs of the MZI with an adjustable ratio by controlling the amount of the phase shift between the two arms of the MZI. The phase shift is introduced by heating the waveguide in one arm of the MZI and hence changing the refractive index of the silicon waveguide. In order to minimize the amount of electrical power needed for a desired phase shift, the resistive heaters are implemented in the slab section of a strip-loaded waveguide by doping the slab section of the waveguide. This assures that the least thermal resistance of the heaters to the waveguide as thermal conductivity of silicon is almost 100 times that of silicon dioxide. Another method used to reduce the electrical power needed for adjusting split ratio is to place thermal phase shifters on each arm of the MZI. Only one arm

of the MZI is heated at any time. This will reduce the maximum required phase shift provided by the phase shifters to 90° compared to 180° needed when only one phase shifter is used and hence reduces the power consumption by a factor of two.

As a demonstration of the concept, we designed a prototype implementing the signal graph flow shown in Fig. 3.9b with $T = 25ps$. The block diagram of the design is shown in Fig. 3.9a. As it can be seen from the signal flow graph, the first two tap coefficients, C_0, C_1 , have a fixed sign, while the sign of the other coefficients are selectable. The sign of the coefficient can be set by selecting the direction of the photo current in the output node. If the photocurrent is added to the output node, the sign is positive and if it is subtracted the sign is negative. This can be achieved by placing the photodiodes as shown in Fig. 3.9a and use an optical switch to route the optical signal of the corresponding tap coefficient to either the upper or the lower photodiode. Each tap that has a selectable sign needs an optical splitter. So the optical splitters 4, 6, and 7 in Fig. 3.9a select the sign of the coefficients while the optical splitters 1, 2, 3, and 5 select the tap coefficients. The overall frequency response of the adjustable self-equalizing photodiode (ASEPD) can be hence written as:

$$I_{out} = RP [C_0 - C_1 e^{-j\omega T} \pm C_3 e^{-j3\omega T} \pm C_4 e^{-j4\omega T}] \quad (3.4)$$

where R is the responsivity of the photodiodes, P is the input optical power, and C_0 to C_4 are the adjustable tap coefficients.

In this design we used DIPD to keep the capacitance loading of the output node low. However, due to increased number of taps, the number of photodiodes attached to the output node is doubled compared to the previous implementation. In order to reduce the drop in bandwidth due to capacitive loading, photodiodes corresponding to higher tap coefficients are designed to be smaller than the photodiode of tap C_0 . While reducing the length of the photodiodes slightly reduces the responsivity, the sensitivity of the receiver is not reduced noticeably given the smaller photocurrent needed for the higher tap coefficients. Based on recent advances in Ge photodiodes implemented on silicon photonics platform, the bandwidth of the photodiode is mainly dictated by the transit time of the carriers and as a result the junction capacitance of the photodiode is no longer a limiting factor in the bandwidth [46]. By utilizing such photodiodes, there would be no bandwidth penalty due to extra capacitive loading at the output node because of multiple photo-diodes. This means that SEPD concept can be utilized to enhance the bandwidth limitation of transit-

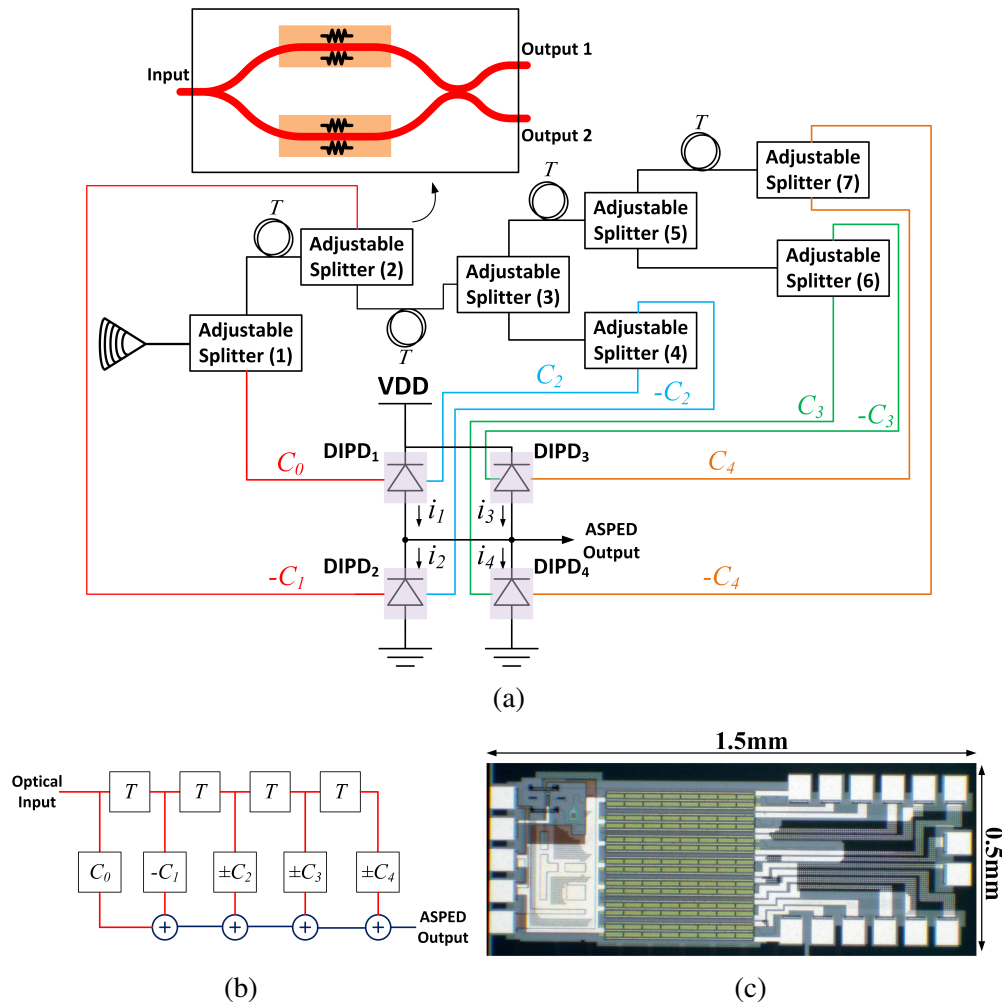


Figure 3.9: The block diagram of implemented adjustable self-equalizing PD (ASEPD) and (b) its signal flow diagram, (c) the die photo of the ASEPD

time limited photodiodes as well as bandwidth limitation due to other components in the transceiver link.

3.4 Measurement Results

To demonstrate the equalization capability of the two-tap SEPD, its performance was compared against a 35GHz photodiode in a 12.5Gbps data link. In Fig. 3.10a we can see that the electro-optical frequency response of the channel is improved by using the proposed SEPD. The channel frequency response shows a very low 3dB bandwidth of 1.5GHz when a 35GHz photodiode is used. The SEPD is able to compensate the loss introduced by the modulators and coaxial cables and hence improve the bandwidth to 5.8GHz. We also measured the eye opening before and after using SEPD. The result shown in Fig. 3.10b clearly proves the ability of SEPD

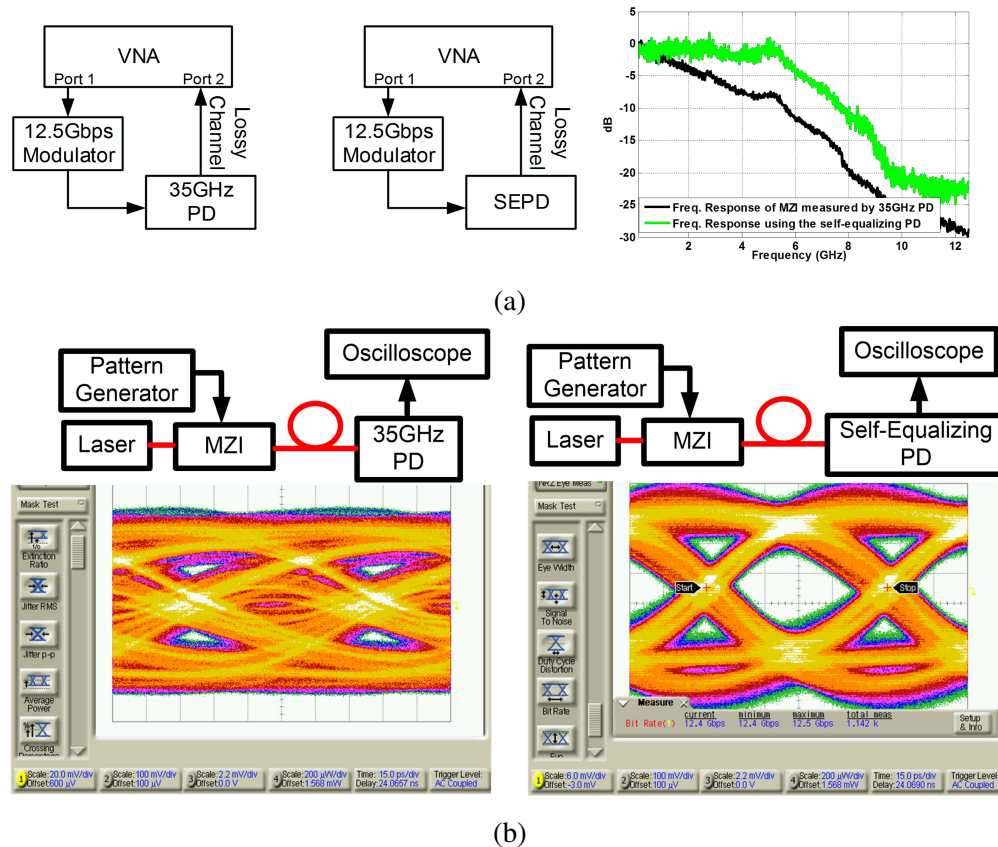


Figure 3.10: Measurement results showing bandwidth enhancement in a bandwidth limited optical link. (a) Measurement setup for measuring the electro-optical bandwidth using a 35GHz PD and SEPD and measured comparison of the two frequency responses showing 7dB of enhancement. (b) Comparison of 12.5Gbps eye-diagrams of the received data without and with SEPD.

to equalize the data and improve the eye opening.

Fig. 3.11 shows the adjustability of frequency response in the adjustable self-equalizing photo detector. Depending on the values and sign of the coefficients a wide variety of frequency responses can be realized with the architectures. As a result, a wide variety of data channels can be equalized.

The ability of the equalizer to improve the eye-opening of the received signal is shown in Fig. 3.12a. In the left image, we are showing the 25Gbps received eye diagram, detected with a 35GHz photodiode. The eye is closed because a 12.5Gbps modulator is used which doesn't have sufficient bandwidth for 25Gbps operation. Substituting the commercial photodiode with the proposed AESPD results in an open eye diagram, showing that a data-rate enhancement factor of two is possible.

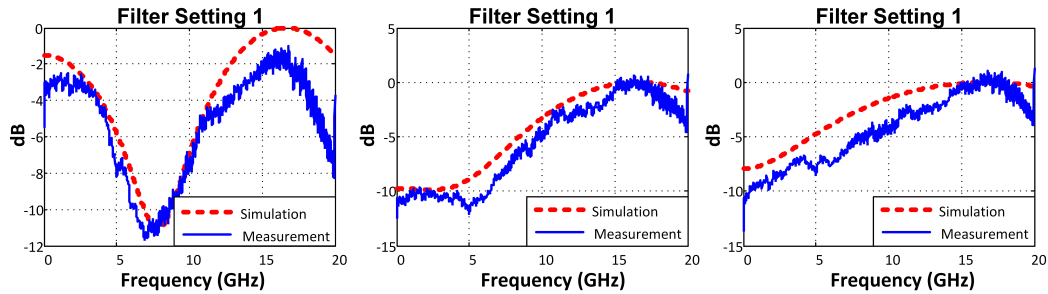


Figure 3.11: Demonstration of frequency response adjustment capability in ASEPD.

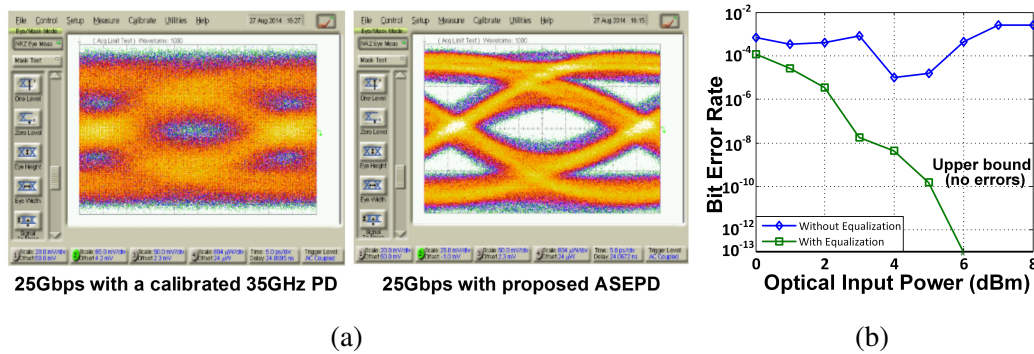


Figure 3.12: (a) Demonstration of eye opening capability of the ASEPD at 25Gbps. (b) Demonstration of improvement in receiver sensitivity before and after utilization of ASEPD for a bandwidth limited channel at 12.5Gbps.

Fig. 3.12b shows the improvement in the sensitivity of the receiver in a bandwidth limited channel when ASEPD is used in a 12.5Gbps link with PRBS 7 pattern generator. Without equalization and using one of the on-chip photodiodes, the best bit-error-rate (BER) achieved is 10^{-5} . Using the ASEPD, the sensitivity of the receiver improves. No errors were detected in one hour of measurement which demonstrates BER better than 10^{-13} .

3.5 Conclusion

In this chapter we demonstrated an electro-optical approach to equalize and improve the receiving optical signal in an optical communication link and perform the electro-optical conversion in one device. The proposed approach overcomes some of the shortcomings that are inherent to fully electrical or fully optical equalizers. Two working prototypes of the concept in which one has fixed tap coefficients and consumes no power and the other has adjustable tap coefficients and is suited for a wide variety of optical links were demonstrated. It was shown that both prototypes are capable of equalizing the received eye-diagram and allow for higher data rate

transmission than otherwise would have been possible.

*Chapter 4***LENS-FREE PROJECTION SYSTEMS USING OPTICAL PHASED-ARRAYS****4.1 Introduction**

Small form-factor optical projectors continue to be an integral part of consumer electronics. It is not difficult to envision mobile devices equipped with low power yet high resolution microchip video projectors in the near future [183]. In addition, low-cost and low power design enables wide range use of miniaturized projectors in portable low-cost 3D imaging and holography systems as well as in the gaming and entertainment industry. Conventionally, optical projectors are implemented using digital light processing (DLP), light emitting diode (LED) based DLP, liquid crystal display (LCD), and liquid crystal on silicon (LCOS) technologies. In a DLP projector, the projector lamp illuminates the DLP chip surface which consists of a large array of micro mirrors. Each mirror is digitally controlled and can either reflect the light into the lens (state 'on') or away from the lens (state 'off'). Since the lamp in DLP projectors is inefficient and bulky, it has been replaced with efficient LEDs in more recently manufactured DLP projectors. In LCD projectors, the pixels are set to 'on' and 'off' states using parallel LCD panels. The LCOS technology is a hybrid of LCD and DLP technologies since it uses mirrors to reflect the light and uses LCD panels to block light. Despite a few disadvantages, overall, the DLP technology has better optical efficiency and projection performance than other display systems [82]. However, even with LED based light sources, a DLP projector requires a lens, often a prism, and is inefficient due to waste of optical power by micro-mirrors in 'off' state.

Optical phased array technology can also be used to implement projection systems. Although optical phased arrays (OPA) have been studied [9, 12, 60, 115, 146, 160, 164, 176], they have not been widely used compared to their electrical counterparts [123, 149]. However, recent advancements in integrated photonic platforms have enabled realization of reliable and compact optical phased arrays with applications in communication, LIDAR, imaging, tracking, targeting, switched fabric networks, routers, and sensing. Today, light detection and ranging (LIDAR) with beam steering capability plays a key role in autonomous vehicle technology [180]. In this paper,

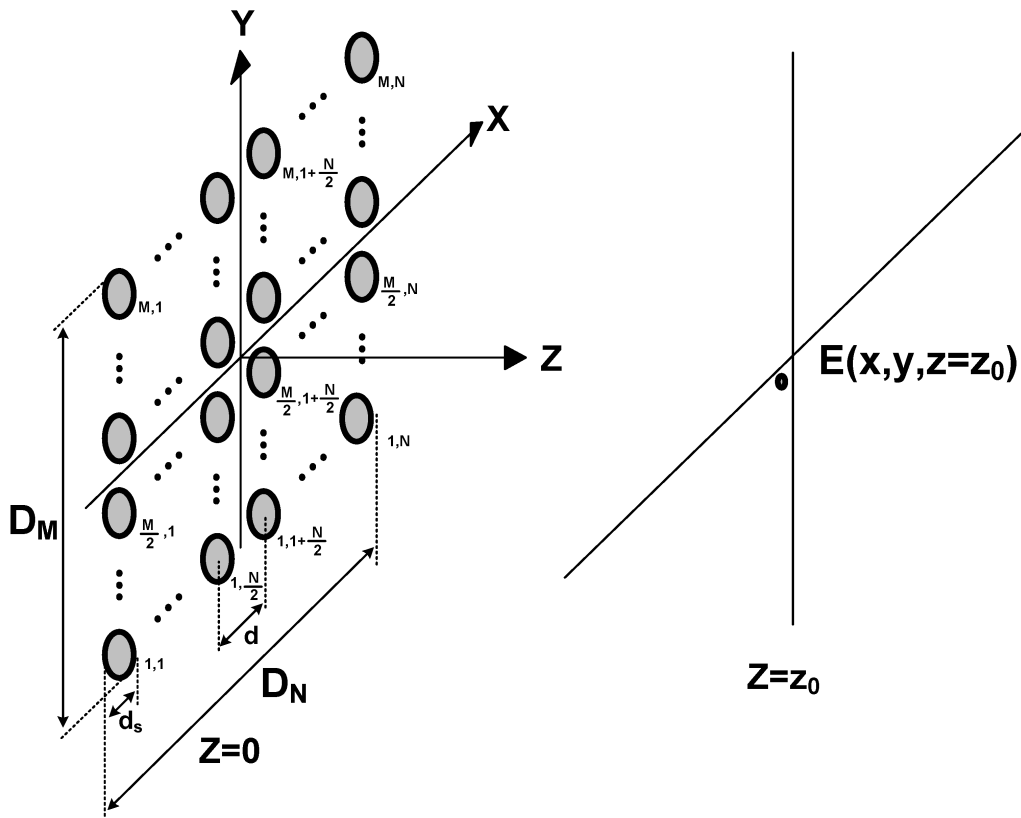


Figure 4.1: The $M \times N$ -element optical phased array.

we report an efficient integrated projection system based on a fast steering optical phased array. The proposed architecture can project an image by vector or raster scan of the beam spot on the screen without use of a lens or any other optical components. This allows the entire projection system to be integrated on a single photonic chip with no mechanical movements at all. The phase shifters of the OPA are p-i-n phase modulators with bandwidth of 200MHz, enabling ultra-fast beam steering. Using the proposed integrated 4×4 OPA, image and video projections are demonstrated. An optimization algorithm is implemented to compensate for the phase dependent attenuation of the p-i-n modulators enabling high quality yet fast beam steering. Due to low power consumption, compact size, and low cost of mass production, this integrated projection solution lends itself more towards being utilized in mobile devices.

4.2 Integrated Optical Phased Arrays

An optical phased array consists of an array of photonic antennas that emit at the same frequency. The phase of the emitted optical wave from each antenna can

be independently adjusted enabling control of the far-field wave front. Generally, there are two types of optical phased arrays. One scheme includes phase locking of an array of lasers to a stabilized reference laser using electro-optic phase locked loops (EOPLL) and offset the phase of individual array elements to perform beam forming and steering [12, 146]. In this case, a high power beam may be formed since by coherent locking of all laser elements, the total power of the output beam could be as high as the total power of all laser elements together and an intensity that increases with the square of the number of elements for a fixed space array. However, phase locking of individual lasers to a reference laser could be a challenging task. Moreover, the residual phase noise of laser elements reduces the power combining efficiency as the number of elements increases [104]. Similar to conventional electrical phased arrays, optical phased arrays can be implemented by having a single laser source and multiple phase shifters. In this case, the laser output is divided into multiple optical branches with an independently controlled optical phase shifter placed on each branch. An optical antenna (e.g. grating coupler or edge coupler) is placed at the end of each branch forming an array of emitters. By adjusting these phase shifters a controllable coherent optical wave front can be formed [9]. These phase shifters can be implemented as passive delay/phase elements [160], or active phase shifters [9, 60, 160]. In this scheme, no EOPLL is required. Moreover, in the absence of the residual phase noise of EOPLLs, the OPA can incorporate a large number of radiating elements. Therefore, this scalable OPA architecture is more suitable for implementation of a high resolution projection system.

In order to perform a rapid beam steering required for image formation using raster or vector scanning, phase shifters with fast electro-optic response are required. Although OPAs based on thermo-optic phase shifters have been demonstrated [160], the large thermal time constant associated with these phase shifters limits the maximum beam steering rate. MEMS based phase shifters enable the realization of arrays with large fill-factors [176]. However, their large mechanical time constant presents a practical challenge in utilizing them for OPA based projection systems. The p-n or p-i-n junction based phase shifters have a much faster electro-optic response compared to thermo-optic or opto-mechanical phase shifters and are better candidates for implementation of the OPA based projection systems.

Figure 4.1 shows a two-dimensional optical phased array where $M \times N$ radiating elements with a physical aperture which is d_s on its side are spaced apart by d along

the x and y axis. Assuming Gaussian beam profile for all elements and considering radiation along the z axis at wavelength λ_0 , the electric field for each element on the plane of the phased array ($z = 0$) can be written as

$$E_{mn}(x, y, 0) = E_{mn,0} e^{jm\Delta\phi_m} e^{jn\Delta\phi_n} e^{-\frac{4}{d_s^2}[(x-md)^2+(y-nd)^2]} \quad (4.1)$$

where $E_{mn,0}$, m , n , $\Delta\phi_m$, and $\Delta\phi_n$ are the element field constant coefficient, element index along x axis, element index along y axis, and the constant phase difference between adjacent elements along the x and y axis, respectively. In this case, using the Fraunhofer far field approximation [69], and assuming all elements to have the same field constant coefficient of $E_{mn,0} = E_0$, the far field intensity of the electric field at $z = z_0$ can be calculated as

$$I(x, y, z_0) = \frac{E_0^2 d_s^4 \pi^2}{16 \lambda_0^2 z_0^2} e^{-\frac{\pi^2 d_s^2}{2 \lambda_0^2 z_0^2} (x^2 + y^2)} |AF_x|^2 |AF_y|^2 \quad (4.2)$$

where

$$AF_x = \sum_{k=1}^M e^{j\left(\frac{2\pi d}{\lambda_0 z_0} x - \Delta\phi_m\right)k}$$

and

$$AF_y = \sum_{k=1}^N e^{j\left(\frac{2\pi d}{\lambda_0 z_0} y - \Delta\phi_n\right)k}$$

are normalized array factors along x and y axis, respectively and can be calculated as:

$$|AF_x| = \frac{\sin\left[M\left(\frac{\pi d}{\lambda_0 z_0} x - \frac{\Delta\phi_m}{2}\right)\right]}{\sin\left[\frac{\pi d}{\lambda_0 z_0} x - \frac{\Delta\phi_m}{2}\right]}, \quad \text{and} \quad |AF_y| = \frac{\sin\left[N\left(\frac{\pi d}{\lambda_0 z_0} y - \frac{\Delta\phi_n}{2}\right)\right]}{\sin\left[\frac{\pi d}{\lambda_0 z_0} y - \frac{\Delta\phi_n}{2}\right]} \quad (4.3)$$

Equation 4.3 indicates that by adjusting $\Delta\phi_m$ and $\Delta\phi_n$, the formed beam can be steered in x and y directions, respectively. Also, the spot size formed on a screen placed at $z = z_0$ is inversely proportional to the array area, $A = MNd^2$. Moreover, the projection area inside which the beam can be steered is proportional to $\lambda_0 z_0 / d_s$.

4.3 Amplitude-Phase Coupling Effect

Consider the case that the amplitude of phased array elements are not the same. This is for example the case where p-n or p-i-n junction based phase shifters are used in the phased array. Based on Kramers-Kronig relations [100], the insertion loss of these modulators is proportional to the amount of the generated phase shift. The

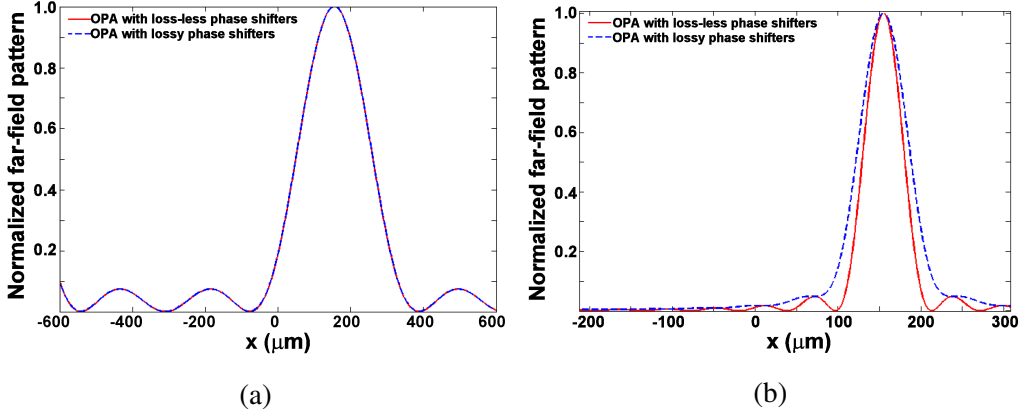


Figure 4.2: The cross section of the array patterns formed at $z_0 = 3\text{cm}$ plane for an OPA with $d = 50\mu\text{m}$ and $\lambda = 1.55\mu\text{m}$ for both loss-less and lossy phase shifters. (a) $M = N = 4$, $\alpha = \frac{\pi}{8}\text{rad}^{-1}$, $\Delta\phi_m = \Delta\phi_n = \frac{\pi}{3}$, and (b) $M = N = 16$, $\alpha = \frac{3\pi}{10}\text{rad}^{-1}$, $\Delta\phi_m = \Delta\phi_n = \frac{\pi}{3}$.

normalized array factor for the 2D phased array in Fig. 4.1 with unequal electric field amplitudes is written as

$$AF = \frac{1}{E_0} \sum_{k=1}^M \sum_{k'=1}^N E_{mn} e^{j\left(\frac{2\pi d}{\lambda_0 z_0} x - \Delta\phi_m\right)k} e^{j\left(\frac{2\pi d}{\lambda_0 z_0} y - \Delta\phi_n\right)k'} \quad (4.4)$$

Assuming that the electric field amplitude loss of the phase modulator increases linearly with the amount of the phase shift, the electric field magnitude for element kk' can be modeled as

$$E_{kk'} = E_0(1 - \alpha k \phi_m)(1 - \alpha k' \phi_n) \quad (4.5)$$

where α is the phase dependent loss coefficient in rad^{-1} . Combining Eqns. 4.4 and 4.5 results in

$$AF = \underbrace{\sum_{k=1}^M (1 - \alpha k \phi_m) e^{j\left(\frac{2\pi d}{\lambda_0 z_0} x - \Delta\phi_m\right)k}}_{AF_{x,u}} \times \underbrace{\sum_{k'=1}^N (1 - \alpha k' \phi_n) e^{j\left(\frac{2\pi d}{\lambda_0 z_0} y - \Delta\phi_n\right)k'}}_{AF_{y,u}} \quad (4.6)$$

where $AF_{x,u}$ and $AF_{y,u}$ are the 1D array factors for the 2D phased array with unequal field amplitudes per element. Using the following identities

$$\sum_{k=1}^M q^k = q \frac{q^M - 1}{q - 1}, \quad \text{and} \quad \sum_{k=1}^M k q^k = q \frac{1 - (M+1)q^M + Mq^{M+1}}{(1-q)^2} \quad (4.7)$$

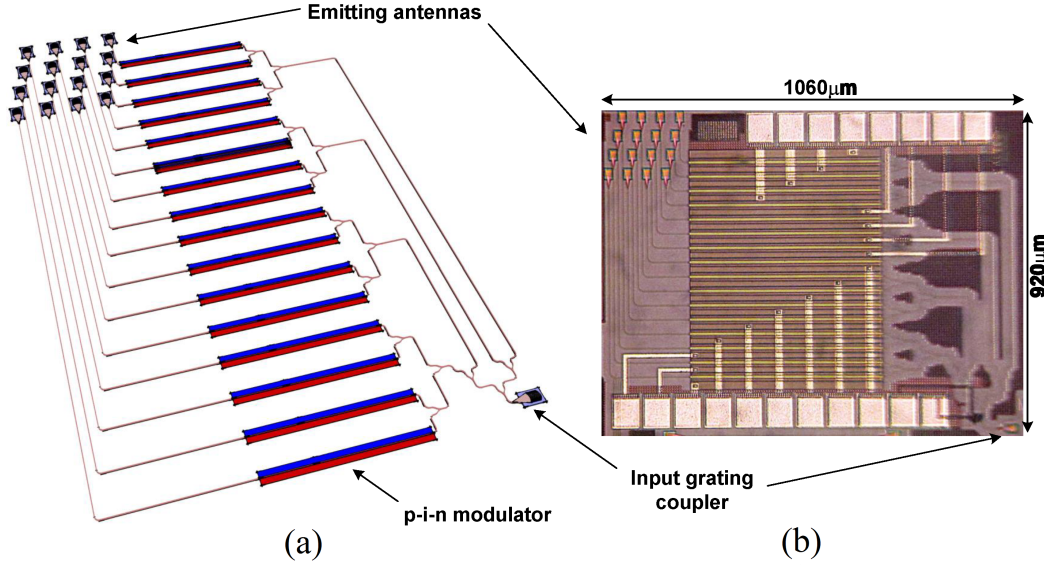


Figure 4.3: (a) The structure of the reported 4×4 integrated optical phased array with perchannel high speed phase control and (b) the chip micro-photograph of the fabricated OPA.

the magnitude squared of $AF_{x,u}$ and $AF_{y,u}$ can be written as

$$|AF_{x,u}|^2 = |AF_x|^2 \left[\left(1 - \frac{M+1}{2} \alpha \phi_m \right)^2 + \frac{\alpha^2 \phi_m^2}{4} [\cot(u_m) - M \cot(Mu_m)]^2 \right] \quad (4.8)$$

$$|AF_{y,u}|^2 = |AF_y|^2 \left[\left(1 - \frac{N+1}{2} \alpha \phi_n \right)^2 + \frac{\alpha^2 \phi_n^2}{4} [\cot(u_n) - N \cot(Nu_n)]^2 \right] \quad (4.9)$$

where $u_m = \frac{\pi d}{\lambda_0 z_0} x - \frac{\Delta \phi_m}{2}$ and $u_n = \frac{\pi d}{\lambda_0 z_0} y - \frac{\Delta \phi_n}{2}$. Equation 4.9 shows that the array factor of the array with linear phase dependent loss per element can be written as the array factor of the equivalent uniform array times a positive loss dependent factor. For this case, it can be shown that as long as $\alpha \leq \frac{1}{M \phi_m}$ and $\alpha \leq \frac{1}{N \phi_n}$, the main lobe of this lossy array is aligned with that of the equivalent uniform loss-less array and can be steered with exact same per-element phase settings. Figure 4.2 shows two examples of this case.

4.4 Proposed Integrated Optical Phased-Array with Per-Channel High Speed Phase Control

Figure 4.3a shows the structure of the reported optical phased array. The light is coupled into the input grating coupler through a single-mode optical fiber and then is guided to a Y-junction splitter network through silicon nano-waveguides. The splitter network uniformly splits and guides the coupled light into 16 p-i-n phase

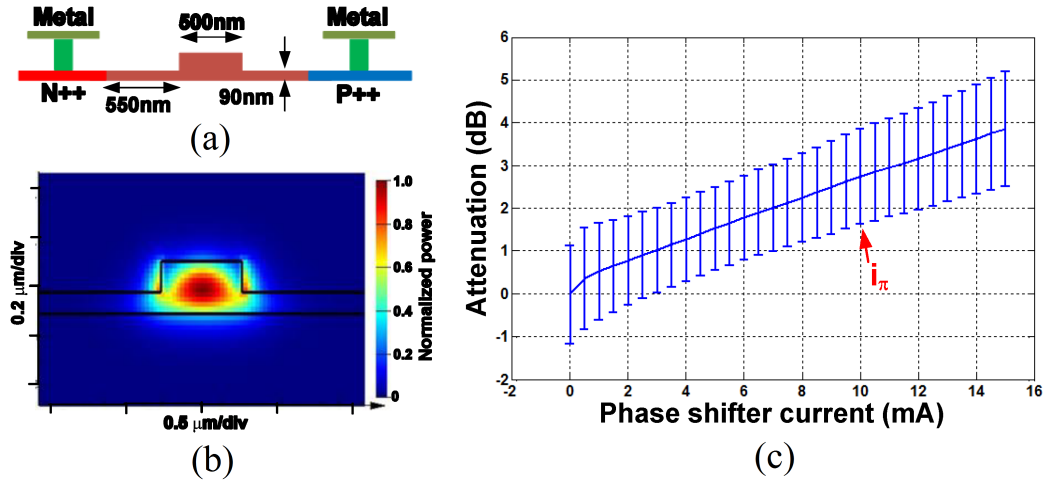


Figure 4.4: (a) The cross section of the p-i-n phase modulator used in the proposed OPA, (b) the propagation mode profile of the modulator, and (c) the measured excess attenuation of the p-i-n modulators in proposed OPA.

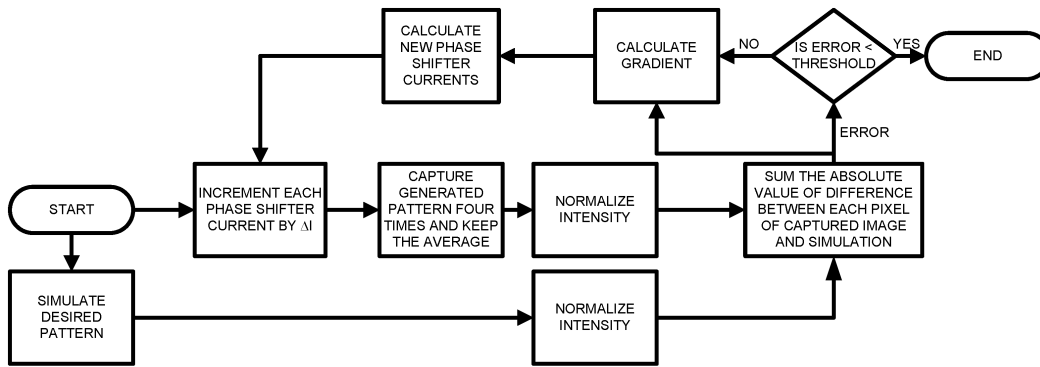


Figure 4.5: The flowchart of the optimization process.

modulators. The phase modulated optical waves are then guided to the radiating antenna (grating coupler) array. The radiating elements are arranged in a 4×4 parallelogram lattice in order to accommodate the optical routing. The center-to-center spacing between adjacent radiation element is $50 \mu\text{m}$. The photonic micro-photograph is shown in Fig. 4.3b. The total area of the fabricated micro-projector chip is less than 1mm^2 .

The cross section of the phase modulator and its propagation mode profile are depicted in Fig. 4.4a and b, respectively. The phase modulator is a p-i-n diode formed on a strip loaded optical waveguide that operates in forward bias. As more current passes through the diode, more free carriers are injected into the waveguide. Interaction of these free carriers with the optical field changes the effective index of

the waveguide, altering the phase of the optical wave propagating in the modulator. The lifetime of the carriers in the modulator waveguide is about 0.7ns, resulting in more than 200MHz modulation bandwidth. Therefore, the forward biased p-i-n phase modulator allows much faster phase control compared to a thermal phase shifter and hence enables fast beam steering necessary in projection. The measured I_π of the p-i-n phase modulators is about 10mA.

Based on the Kramers-Kronig relations, the optical insertion loss of carrier injection based phase modulators is directly related to the amount of optical phase shift introduced by the modulator. The measured excess attenuation of typical p-i-n modulator in our design versus modulator current is depicted in Fig. 4.4c, where a linear fit to the data points results in phase-to-amplitude coupling factor (defined in Eqn. 4.5) of $\alpha = \frac{1}{8\pi} [rad^{-1}]$. In this case, following the analysis presented in section 4.3 and for $N = M = 4$, it can be seen that as long as the phase increments between array elements satisfies $\Delta\phi_m, \Delta\phi_n \leq 2\pi$, the main lobe of our proposed array is aligned with the equivalent uniform lossless array, and hence the same element phase settings may be used to steer the beam to the desired angles. However, fabrication process variations can result in different coupling factors for different p-i-n phase modulators. Figure 4.4c shows the variations in insertion loss of different p-i-n modulators used in the fabricated phased array. The error bars on this graph represent the range of the measured insertion loss of all 16 p-i-n modulators at each bias current. These variations result in different phase-to-amplitude coupling factors for different p-i-n modulators in the OPA. In order to compensate for these undesired variations, a calibration process is required. In the calibration phase, for each desired steering angle, the per-modulator phase setting of the equivalent uniform loss-less OPA is used as the initial point. Then an optimization algorithm is used to find a set of currents required for all phase modulators to minimize the error in the steering angle compared to the uniform loss-less OPA.

In the optimization process, first the image captured by the IR camera corresponding to the main lobe of the phased-array pattern is compared against that of a simulated uniform loss-less phased-array pattern. Since the dynamic range of the camera is limited and some saturation may occur, the simulation pattern is adjusted to account for saturation. The optimization error is defined as the pixel-wise Euclidean distance between the simulated pattern and the captured image and is used to guide the gradient descent optimizer. In each iteration, the gradient of the error is calculated by perturbing the current of each phase shifter and observing the changes in the

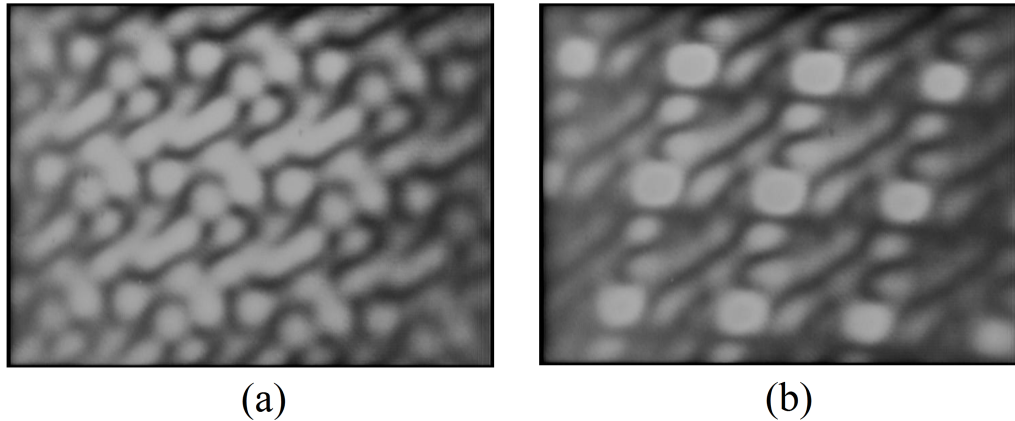


Figure 4.6: The pattern of the OPA for zero relative phase setting ($\Delta\phi_m = \Delta\phi_n = 0$) captured using FJW View-R-Scope 85400A IR camera;(a) before gradient decent optimization, and (b) after gradient decent optimization.

captured pattern as well as the error. At the end of each iteration, the currents of the phase shifters are modified by a small amount in the opposite direction of the gradient. In practice, it was observed that if only a single lobe of the OPA pattern is used for error calculations, the gradient descent leads to reasonably accurate results. Once the error between the actual image and the desired simulated image becomes smaller than a pre-programmed threshold, the current settings for all modulators are saved for the target steering angle and the system start optimization for another target angle. The process continues until the optimized current settings for all desired steering angles are saved in a look-up table. To enable the fastest possible operation speed, for any steering angle input to the OPA, the current settings are instantly loaded from the look-up table to all modulators. The flowchart of the optimization process is depicted in Fig. 4.5.

One important undesired effect in the optimization process is the noise of the IR camera. In order to overcome this effect, in the calibration phase, multiple images were captured and the final image was formed by averaging these images.

4.5 Measurement Results and Image and Video Projection

The nanophotonic projector chips were fabricated in IME silicon-on-insulator technology node [127] where silicon-on-insulator wafers with a $0.22\mu\text{m}$ top silicon layer and $2\mu\text{m}$ buried oxide are used. Three levels of silicon etching were available. The pixels are grating couplers with about 40% coupling efficiency that were designed using two levels of etching. The average optical loss of 500nm wide and 220nm

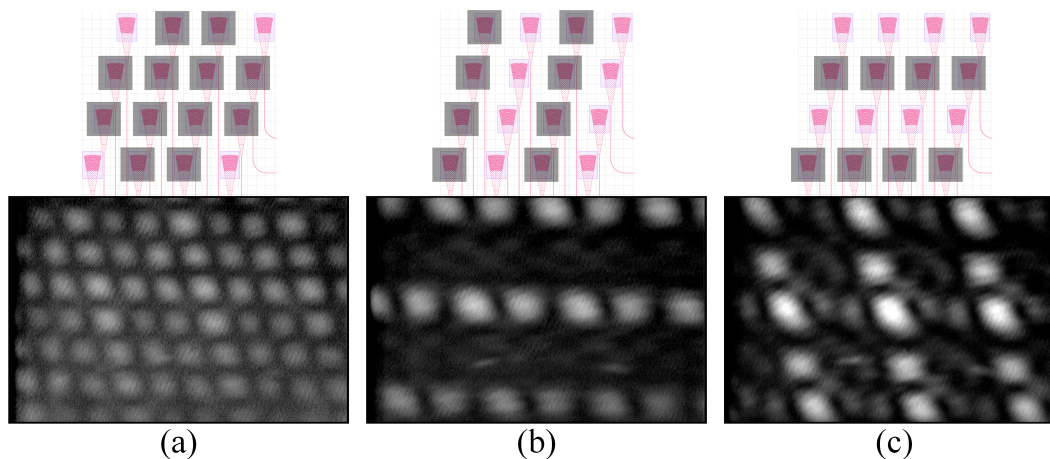


Figure 4.7: Top: the OPA element radiation status (only highlighted elements are radiating), bottom: the far-field pattern. (a) The far-field pattern of the OPA when all elements except for the ones at the corners of the array are turned off (b) the far-field pattern of the OPA when elements on every other columns are turned off, and (c) the far-field pattern of the OPA when all elements on every other rows are turned off.

thick silicon waveguide is about 1.8dB/cm. No post processing was performed on the fabricated chips. The fabricated chips were mounted on a printed circuit board (PCB) and electrically connected to it using bond wires. No temperature control was required. A commercially available DFB laser emitting 3mW at $\lambda_0 = 1550\text{nm}$ is used for all measurements. All measurements have been carried out at the room temperature.

As discussed in section 4.4, due to process variations, it is not possible to accurately predict the amount of the phase shift and insertion loss introduced by the p-i-n modulator for a given current setting. Therefore, the OPA pattern for certain current setting may deviate from the expected pattern. Figure 4.6a shows the pattern of the OPA for zero relative phase setting ($\Delta\phi_m = \Delta\phi_n = 0$) captured using "FJW View-R-Scope 85400A" IR camera placed a few centimeters away from the OPA chip surface. The image distortion introduced by the effect of process variation is significantly reduced after gradient decent optimization is performed (Fig. 4.6b).

Since the insertion loss of p-i-n modulators can be controlled by the amount of the modulator current, it is possible to control the radiating power of individual OPA elements. In the extreme case, an OPA radiating element can be effectively turned off by injecting 20mA of current to the corresponding p-i-n modulator. Figure 4.7a shows the far-field pattern of the OPA when all OPA elements are turned off

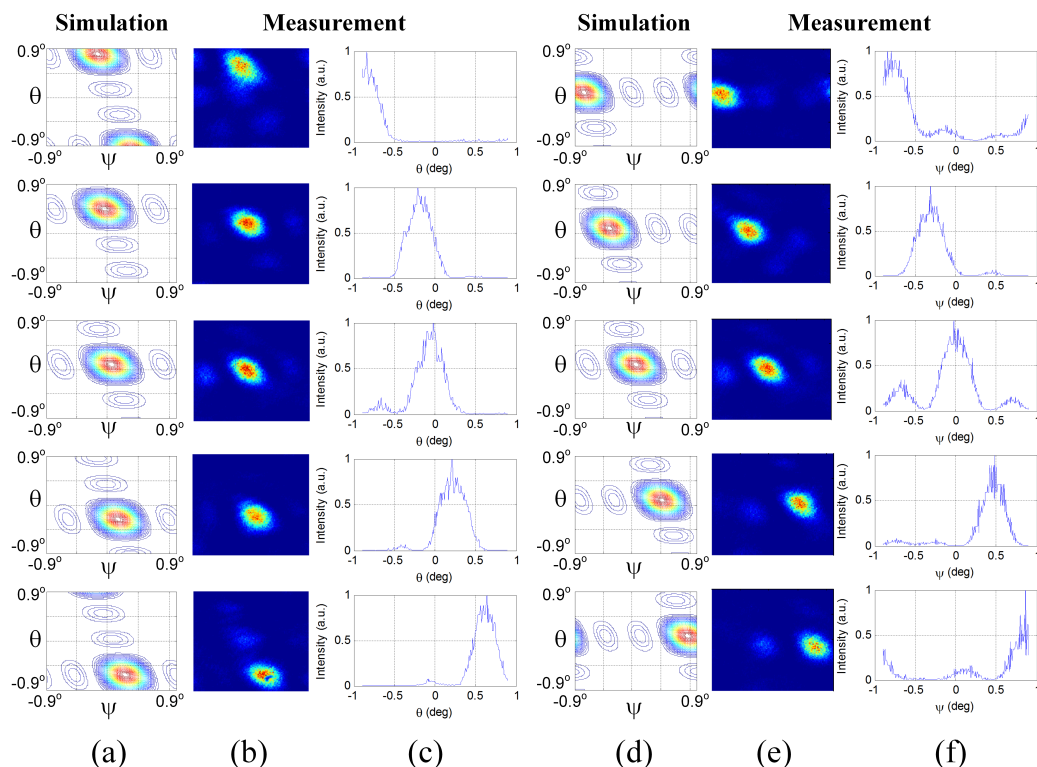


Figure 4.8: The vertical beam steering; (a) simulation, (b) measurement, and (c) far-field pattern cross section. The horizontal beam steering; (d) simulation, (e) measurement, and (f) far-field pattern cross section.

except for the elements located at the corner of the array. As expected, the beam spacing is reduced. In a different experiment, the elements located on every other column are turned off. In this case, the vertical lobe spacing is increased while the horizontal spacing remains the same. This is depicted in Fig. 4.7b. Similarly, as shown in Fig. 4.7c, when the elements on every other row are turned off, the horizontal lobe spacing increases. In order to demonstrate reliable two-dimensional beam steering, after calibration phase, gradual beam steering in both vertical and horizontal directions has been performed which is compared with the simulated pattern in Fig. 4.8. As shown, the OPA is capable of two-dimensional beam steering over full vertical and horizontal lobe spacing periods. Figures 4.8a and 4.8b show that the measured vertical beam spot movements are in close agreement with the corresponding simulations. Figure 4.8c shows the cross-section of the measured far-field pattern of the OPA. Similarly, Figs. 4.8d, 4.8e, and 4.8f show the horizontal beam spot movements. Note that the vertical beam steering has some small horizontal shift due to the parallelogram lattice structure of the array.

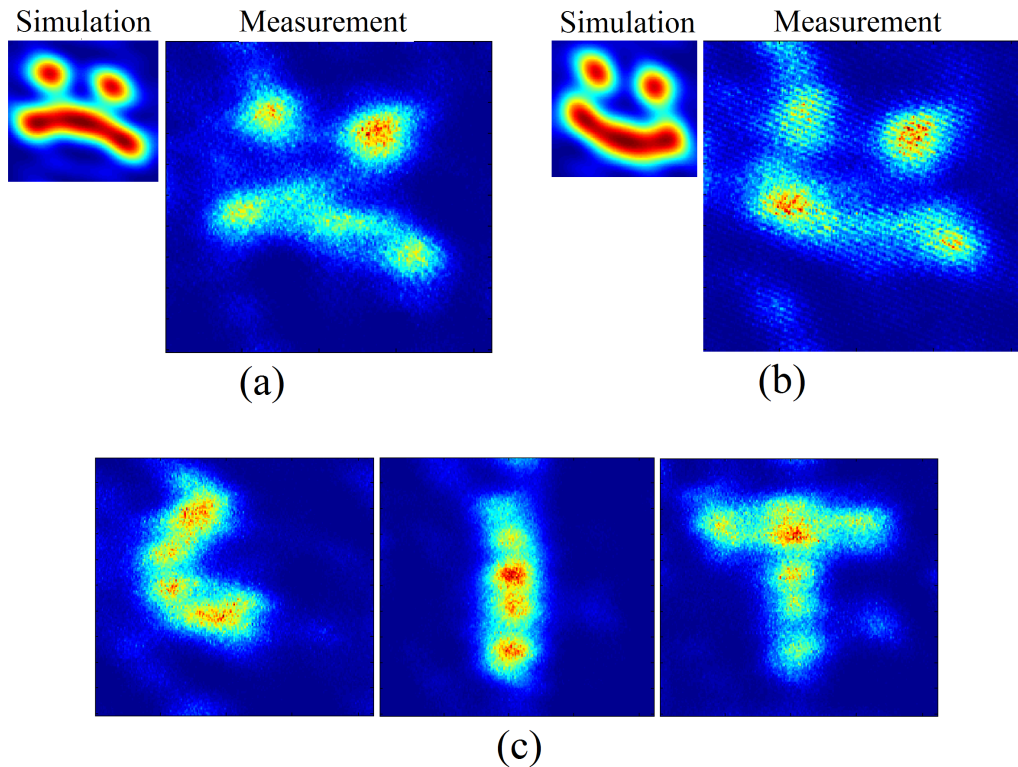


Figure 4.9: Projected images by fast vector scan of the beam spot; (a) smiley face (simulation on left), (b) sad face (simulation on left), and (c) individual letters of CIT (California Institute of Technology).

After the calibration is performed, the OPA can be used as a projector by quick vector or raster scan of the beam spot on the screen. Figures 4.9a and b show the simulated and projected smiley and sad faces that are formed by fast vector scan of the beam spot, respectively. The entire image was captured in real time with a single snapshot of the IR camera. Figure 4.9c shows the projected images of letters ‘C’, ‘I’, and ‘T’ for California Institute of Technology.

4.6 Conclusion

We have reported an integrated projection system based on a two-dimensional optical phased array where p-i-n phase shifters with 200MHz bandwidth are used for rapid beam steering which enables real time projection of an image by fast vector scanning. We have implemented an optimization algorithm to compensate for the phase dependent attenuation of the p-i-n modulators. Using fast vector scan of the beam spot, images were formed and recorded within a single snapshot of the IR camera. This work is a step towards utilizing integrated photonics platforms in realization of integrated projection systems with a large number of emitters

making low-cost high performance integrated projectors available for varieties of applications in near future.

*Chapter 5***LENS-FREE IMAGING SYSTEMS USING OPTICAL PHASED-ARRAYS****5.1 Introduction**

An optical phased array receiver with beamforming and steering capabilities can serve many functions including lens-less camera, compact LiDAR, active sensor, etc. Silicon photonics fabrication processes have enabled integration of many optical elements on a single chip. On-chip high performance components such as modulators, grating couplers, and photodiodes in close proximity enable novel designs that were not practical in bench-top implementation. Silicon-photonics OPA transmitters have attracted much interest recently [10, 51, 83, 85, 132, 171]. An OPA transmitter includes an array of grating couplers that radiates light out of the chip. By controlling the phase of the light feeding each radiating element, a beam can be formed and steered to send the light to a desired direction analogous to microwave phase array transmitters [74]. Since electromagnetic wave propagation is reciprocal, a similar array structure, in principle, can detect and determine the light intensity at a particular angle, thereby forming a gazing beam, operating as a phased array receiver. Microwave phased array receivers have been investigated and implemented in the past [73]. OPA transmitter is fed with an optical signal, which is split into several branches that go through phase shifters into grating couplers. There are challenges in designing an OPA transmitter, such as achieving high efficiency and controlling stray light which is the part of input light that does not couple to the chip. However, the trade-offs in an OPA receiver are qualitatively and quantitatively different from those in an OPA transmitter as the signal-to-noise levels are substantially different in an OPA receiver. Thus, the back-end of a receiver should be designed to handle and process the received light accordingly [61, 62].

In this paper, a one-dimensional OPA receiver is presented. The OPA receiver collects light from a desired direction. The direction of reception can be altered electronically by controlling the relative timing and phase of the receiver elements. Scanning the field of view by steering the gazing beam and forming an image of the target in front of the chip by assembling the data for different bearings can effectively turn the OPA receiver into a lens-free camera.

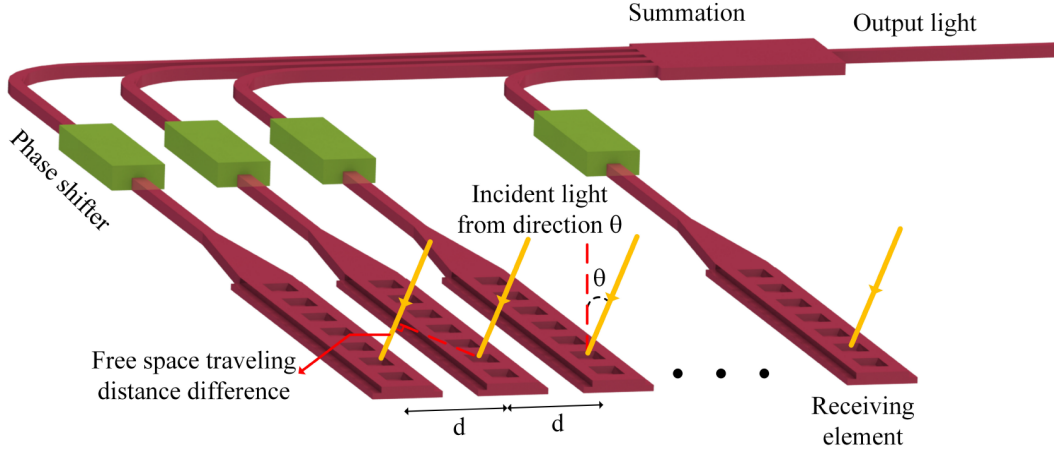


Figure 5.1: Conceptual schematic of a 1D optical phased array receiver.

First, a brief explanation of the fundamentals of the phased array receiver and its use as an imager is presented. Next, the design of the presented OPA receiver is discussed. Finally, the measurement setup and results are presented.

5.2 Phased Array Receiver

The conceptual schematic of a 1D phased array receiver is shown in Fig. 5.1. An array of receiving elements forms the synthetic aperture. In a uniform array, elements are placed at spacing of d . Light impinging at angle θ arrives at different elements with different delays. Having the first element on the left at $x = d$, the k^{th} element is located at $x = kd$. Thus, the path difference that light impinging at angle θ should travel to reach the first element compared to the k^{th} element is $kd \sin(\theta)$ and it arrives at the k^{th} element sooner by

$$t_k = \frac{kd \sin(\theta)}{c}, \quad (5.1)$$

in which c is the speed of light. This time difference corresponds to a phase difference of

$$\phi_k = \frac{2\pi kd \sin(\theta)}{\lambda} \quad (5.2)$$

Therefore, having a plane wave impinging at angle θ on the first element, the received signal by the k^{th} element is

$$r_k(t) = e^{i(\omega t + \phi_k)} \quad (5.3)$$

In an direct-conversion OPA receiver, the time of arrival difference for the light at θ_0 is compensated by applying the phase shift of

$$\phi_{d_k} = \frac{2\pi k d \sin(\theta_0)}{\lambda} \quad (5.4)$$

to the coherent light received from the k^{th} element.

This effectively steers the beam to the angle θ_0 . Assuming omnidirectional receiving element pattern, the resulting output signal after the summation is

$$r(t) = \sum_{k=1}^n r_k(t) e^{-i\phi_{d_k}} = \sum_{k=1}^n e^{i(\omega t + \phi_k - \phi_{d_k})} = e^{i\omega t} \sum_{k=1}^n e^{\frac{2\pi k d \sin(\theta - \theta_0)}{\lambda}} \quad (5.5)$$

in which n is the number of elements of the array. All the signals associated with the wave front impinging from θ_0 are in-phase after the phase shifts are applied. Summing the signals in this setting results in constructive interference for the light coming from direction $\theta = \theta_0$. If the spacing between elements is less than $\lambda/2$, light arriving from any other direction will not be in phase for all the elements and thus will produce a smaller amplitude after summation. For $d > \lambda/2$, there exist other angles that the signal from all the elements happen to be in phase at the summation.

Figure 5.2 shows the normalized reception gain, i.e., the magnitude of $r(t)$ for a phased array with 5 elements, element spacing d of 2λ , and $\theta_0 = 0$. Since light arriving from angle $\theta = 0$ sums up constructively, the phased array has the maximum gain at $\theta = 0$. The lobe at θ_0 is called the main lobe. The main lobe is defined as the gazing beam of the OPA receiver, which is the desired direction of receiving the incident light on the chip. To receive light from a different θ_0 , phase shifts should be adjusted using equation 5.2. Having electronically controllable phase shifters, the gazing beam can be steered electronically to collect information from a different angle selectively. The extra lobes for the case of $d > \lambda/2$ are the grating lobes and the smaller lobes in between are side lobes. At the angles that side lobes appear, the phase shifted signals sum up partially constructive. The angular spacing between the main lobe and a neighboring grating lobe is the field of view of the phased array and it is a function of the element spacing. The field of view for the array of Fig. 5.2 is 30° .

The individual receiving elements also have a certain reception pattern, that indicates how strong the wave coming from different angles couple into the waveguide on the chip. Grating coupler pattern depends on its geometry, constituting material, and the wavelength it is working at. The overall reception of a phased array system is

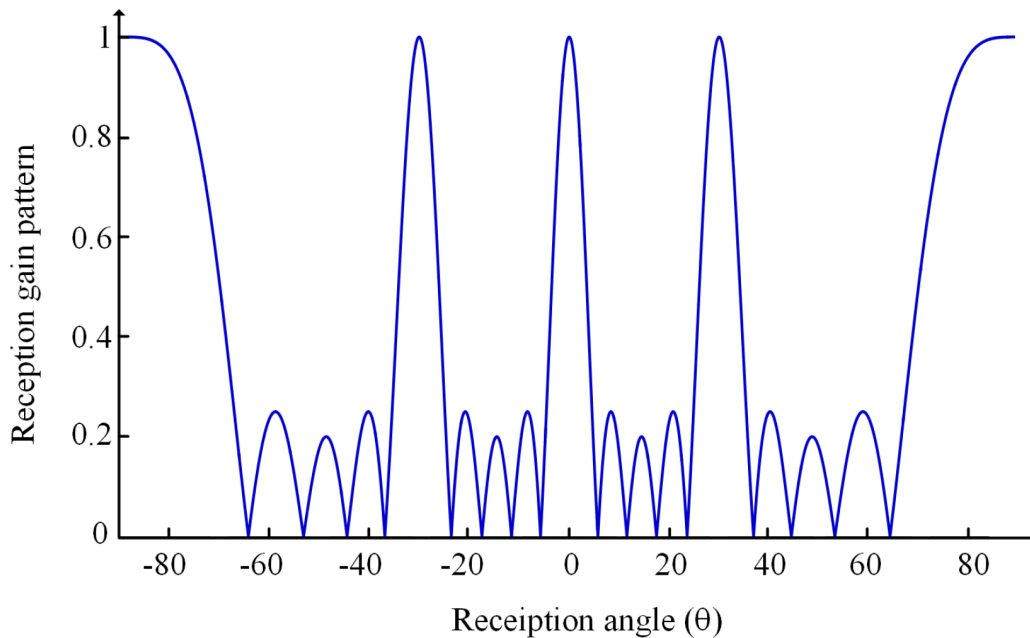


Figure 5.2: Array pattern for a 5-element array with spacing 2λ and omnidirectional.

the product of the receiving element pattern and the array pattern. In practice, the grating lobes are often attenuated by the pattern of the individual elements, and are significantly less important.

Through the use of a tunable phase shifter per element to adjust ϕ_{d_k} , it is possible to steer the pattern and thereby the main lobe to receive signals from different directions. The OPA receiver can form various gazing beams at different angles by using different phase settings. An image can be formed by scanning this gazing beam and measuring the signal received from all the directions.

Grating lobes that are not suppressed enough by the individual element pattern can also be easily filtered spatially if more grating lobe rejection is required. Increasing the number of array elements reduces the side lobe level, an effect that can pick up signal from undesirable directions. For a given element spacing, a higher number of elements results in a narrower beam width. When the number of elements are fixed, beam width reduces by increasing the element spacing as well, at the cost of a reduced field of view.

5.3 OPA Receiver Design

The simple conceptual explanation of the phased array receiver in the previous section does not naturally lend itself to a practical implementation of the lens-less camera. One of the main issues is the very low strength of the received signals and

the system's sensitivity to the shot noise of the photodiodes (used for converting optical signals to electrical signals) as well as the thermal noise of the electrical amplifiers. Moreover, stray light that is not processed by the phased array system is picked up by the photodiodes directly and produces unwanted output.

To overcome these issues, we propose a heterodyne OPA receiver architecture, as illustrated in Fig. 5.3. In heterodyne mixing, two signals with different frequencies are mixed with each other. In this design [61], one of the light signals, $E_i(t)$, illuminates the object and reflects back toward the surface of the chip. It has the optical frequency of $f_0 + f_i$.

$$E_i(t) = a \cos[2\pi(f_0 + f_i)t + \phi_i] \quad (5.6)$$

A strong reference light with frequency $f_0 - f_r$ is the second signal in mixing, $E_{ref}(t)$, where

$$E_{ref}(t) = A \cos[2\pi(f_0 - f_r)t + \phi_r] \quad (5.7)$$

The mixed component is the product of the two signals, $E_i(t)E_{ref}(t)$. The nonlinear nature of the photodiode is used to perform multiplication of the two signals. Adding the two signals and feeding it to a photodiode yields the low frequency component of the product, $I(t)$, which is at the frequency of $(f_0 + f_i) - (f_0 - f_r)$ (the beat tone), i.e.,

$$I(t) = 2RaA \cos[2\pi(f_i + f_r)t + \phi_i - \phi_r] \quad (5.8)$$

where R is the responsivity of the photodiode. Equation equation 5.8 shows that the amplitude of the strong reference light, A , appears as gain for the detected signal. Amplifying the incident signal before detection in this scheme makes it more robust to noise. As a result, weak signals are detected and the system has a better sensitivity for capturing the incident light. In addition, the output signal of the photodiode is at a frequency different from the incident and reference lights. Therefore, it is easily differentiated from the stray light that reaches the photodiode in the post electronics processing in the electrical domain.

In a direct detection receiver, $f_i = f_r = 0$, and laser light with frequency f_0 is used for both illumination and reference. Thus, fluctuations of ϕ_i and ϕ_r due to thermal

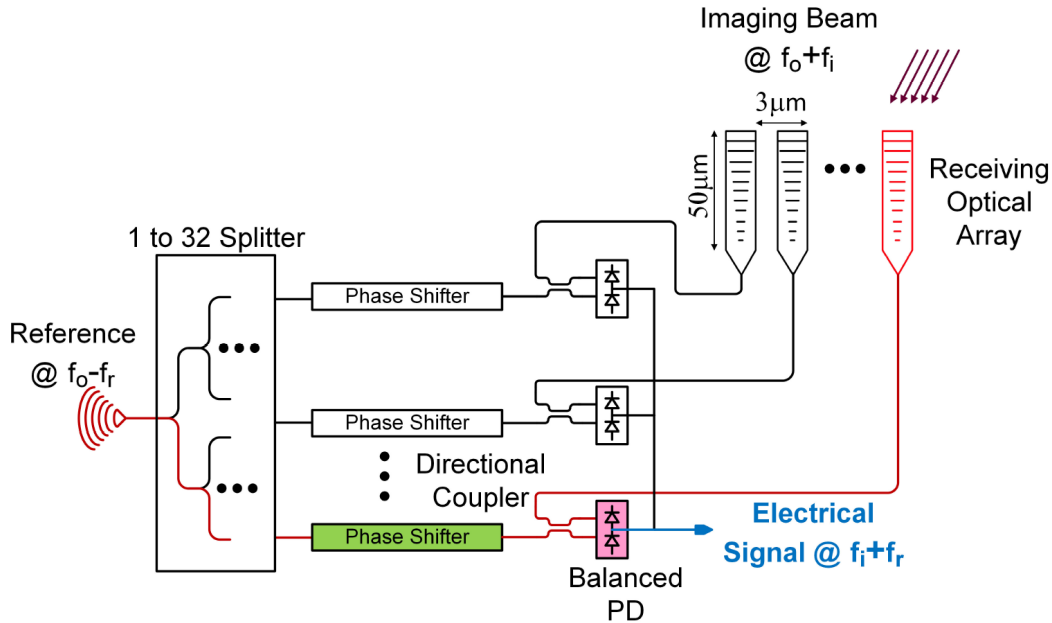


Figure 5.3: The schematic structure of the designed heterodyne OPA receiver. Colored path shows the processing of a single element.

variations and mechanical vibrations in the optical paths appear as amplitude fluctuations in direct detection. The other key advantage of the heterodyne architecture is that fluctuations of these two phases appear as phase noise, which does not change the overall detected power in the output mixed component. Phase fluctuations are more tolerable compared to the amplitude fluctuations in direct detection method.

While conceptually phase shifting the impinging signal may sound straightforward, the received signal generally can be very small, and therefore the signal losses due to the phase shifters can be detrimental. To overcome these challenges, we propose performing the phase shift in the reference path of the heterodyne receiver in an LO-phase shifting architecture. This reference phase shifting architecture has been used in RF integrated circuits in the past [73], and can be used to great effect in optical phased arrays.

One Dimensional Receiver

In the case of OPA transmitters, grating couplers are usually used to couple light from on-chip waveguides to free space [85, 132, 136]. For receiving operation, grating couplers are designed to efficiently couple the light impinging on their surface into the propagating mode of a waveguide. These grating couplers function as the receiving elements of the array. Each grating coupler is a $50\mu\text{m}$ by $2\mu\text{m}$ slab

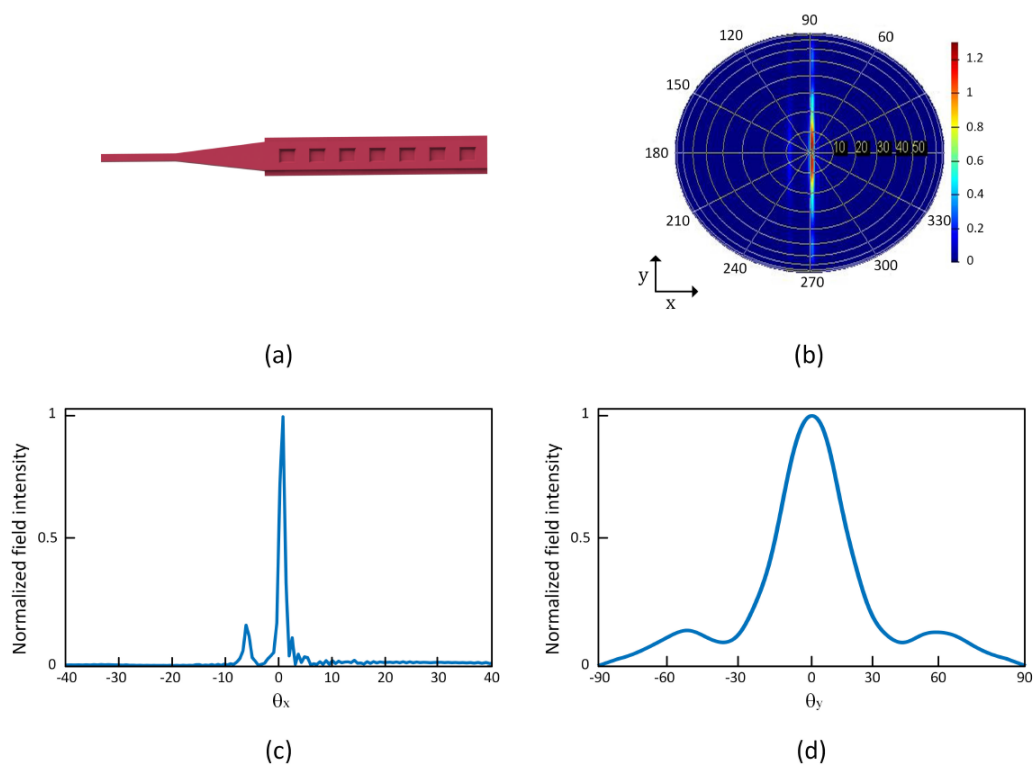


Figure 5.4: (a) Simplified illustration of 1D grating coupler (b) Far-field pattern of the grating coupler on a hemisphere (c) Far-field pattern of the grating coupler at $\theta_y = 0$ (d) Far-field pattern of the grating coupler at $\theta_x = 1^\circ$.

of 220nm thick silicon. The gratings are achieved via periodic slots that are etched 60nm into the silicon slab. The grating period is 560nm with a 60% duty cycle. Figure 5.4 shows the grating coupler far-field pattern. The length of the grating coupler is along the x-axis and the width is along the y-axis. Since the width is short compared to the wavelength, 1550nm, the pattern is wide along the y-axis. The long dimension, $50\mu\text{m}$, yields a narrow pattern along the x-axis. Grating couplers are placed in a 1D array along the y-axis. The overall pattern of the phased array is the product of the grating coupler pattern and the array pattern. Therefore, the total pattern is narrow along both axes and it is electronically steerable along the y-axis by adjusting the phase shifts applied to each element.

In the proposed design, laser light with 1550nm wavelength is used for illumination and imaging. Thirty two grating couplers, Fig. 5.3, are used as array elements with element spacing of $3\mu\text{m}$, which results in a theoretical 3dB beamwidth of 0.82° and

field of view of 31.1° ¹. Since the total receiver pattern is the product of the array pattern and grating coupler pattern, the beamwidth is further narrowed to 0.68° .

Each grating coupler receives the incident light and diffracts it into a dielectric waveguide. Dielectric single mode channel waveguides [10] 220nm by 500nm in size are used to route optical signals on the chip. Each waveguide is routed to a directional coupler with coupling ratio of 50%, which is added to a reference signal fed to the other input port of the directional couplers. The coupling region of the directional coupler [173] is designed to be $17.7\mu\text{m}$ long with a 200nm gap for 3dB coupling. As a result, 50% of each input port transfers to the two output ports.

The strong reference optical signal is provided to the chip via an optical fiber through a focusing grating coupler [165], Fig. 5.5(a). The reference light is then split through a 5 level chain of splitters to thirty two paths. Reference and incident light phases affect the mixed component phase the same way. Therefore, the phase shift required for the phased array elements can be applied to the reference path instead of the received signal path. Having the phase shifters in the reference path significantly reduces the attenuation of the weak incident light path, which increases the system sensitivity. Thirty two thermal phase shifters apply the proper phase shifts to the reference signals. Each thermal phase shifter, Fig. 5.5(b), includes a dielectric waveguide that carries the optical signal with two doped regions on the two sides. The doping areas are resistive and heat up when current passes through them. The temperature change in the vicinity of the waveguide changes the refractive index of silicon and thus the optical path length changes. As a result, the phase of the optical signal at the output of the phase shifter can be adjusted by controlling the voltage applied to the resistors. Thermal time constant of the phase shifter architecture specifies the speed of switching between phases. In this design, the frequency response of the thermal phase shifter has 3dB bandwidth of around 1KHz.

The outputs of the phase shifters are fed to the other input port of the directional couplers. The two outputs of the directional coupler are equal to half of the sum of the phase shifted version of two inputs. Phase shift comes from the 90° inherent phase shift associated to the directional couplers. Thus the envelopes of the two outputs are 180° out of phase and form a differential signal. The phase shifts in the reference paths are also embedded in the envelope phase of the thirty two directional couplers outputs.

¹As a point of reference this corresponds to a lens with 50mm focal length on a DSLR with 1.5 crop-factor

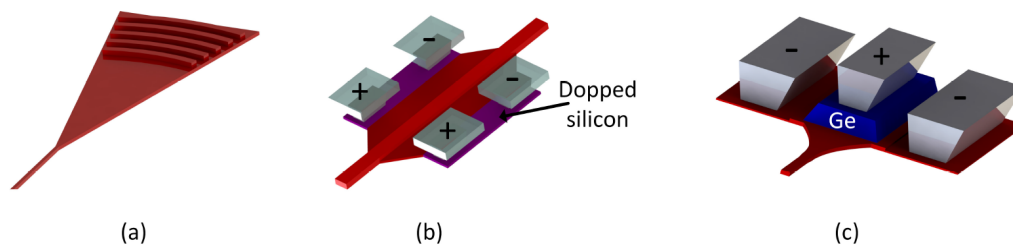


Figure 5.5: (a) Focusing grating coupler (b) Thermal phase shifter (c) Germanium photodiode

Epitaxially grown $4 \times 16 \mu\text{m}^2$ on-chip germanium photodiodes with responsivity of 0.4 A/W are used to convert the optical signals to electrical signals. Fig. 5.5(c) shows the structure of the photodiode which include germanium on top of a tapered waveguide to absorb the 1550 nm light and doped regions for electrical contact. A balanced photodiode architecture [75] is used to extract the envelope of these signals. Applying proper DC voltages to the two ends and the middle node puts them in reverse bias. The two outputs of the directional coupler are connected to the photodiodes and the output current at the middle node of the balance structure is a single ended signal which is proportional to the differential envelopes of the optical signals. Connecting the middle nodes of all the balanced photodiodes sums their currents and forms the summation point of the phased array. This electrical signal is routed to a pad on the chip so that it could be read by the off-chip electronic circuitry.

The designed OPA receiver is fabricated on a silicon on insulator (SOI) process with bulk oxide thickness of $2 \mu\text{m}$. The height of dielectric waveguides on the chip is 220 nm and two etch levels of 60 nm and 90 nm are used for designing grating couplers and modulators. There is also germanium photodiode in the process that makes efficient optical-electrical conversion possible. Figure 5.6 shows the fabricated chip.

Two-Dimensional Imager

The schematic diagram of the phased array receiver camera is shown in Figure 5.7 and the fabricated chip in Figure 5.8. An 8×8 array of grating couplers capture the incident light on the chip surface and each grating coupler guides the light into a waveguide. In this heterodyne scheme, each waveguide is then routed to a directional coupler where the received light is combined with the reference light. The output

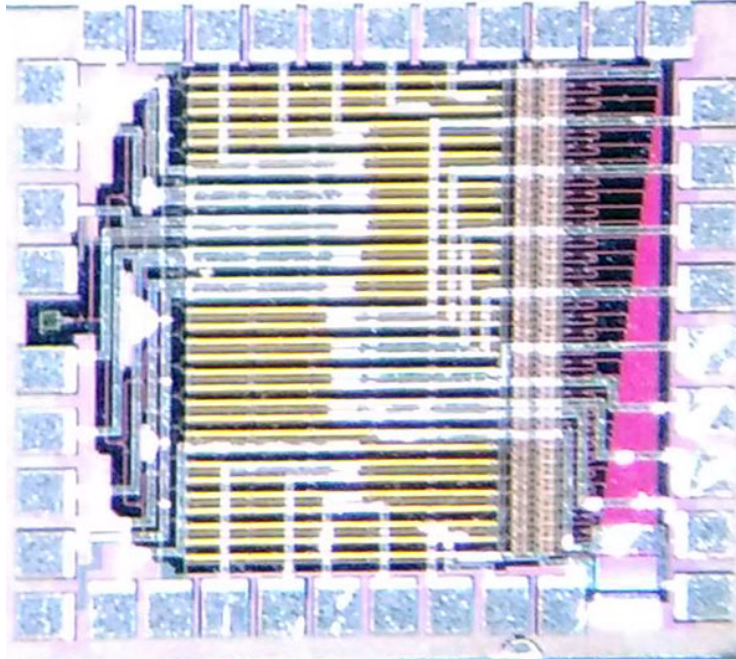


Figure 5.6: Fabricated OPA receiver chip.

of the directional coupler is fed to a pair of balanced photodiodes where the signal is mixed down to an electrical intermediate frequency (IF) in the MHz range. The output current of all the photodiodes associated with the receiving elements are summed up by placing them in parallel electrically producing the output signal of the receiver. The reference light is coupled in through a grating coupler and split into 64 paths. Each path goes through a PIN diode phase shifter and feeds a directional coupler. A receive beam is formed by adjusting the phase shifts of each path so that the amplitude of the signal arriving from a certain direction adds constructively, while rejecting the intensity of incident light from other directions. This is tantamount to looking in a certain direction.

5.4 Measurement setup

A printed circuit board (PCB) is designed to control the phase shifters on the chip and process the output current of the photodiodes. Thirty two digital-to-analog converters (DAC) followed by amplifiers are used to drive the phase shifters. The output voltage range of amplifiers is sufficient to provide 2π optical phase shift per phase shifter. A microprocessor serves as the interface between a desktop computer and the PCB. It receives commands from the computer and sends codes associated with different phase shifts to DACs. A low noise transimpedance amplifier converts the output current of the chip to voltage signal. The amplified voltage is then input

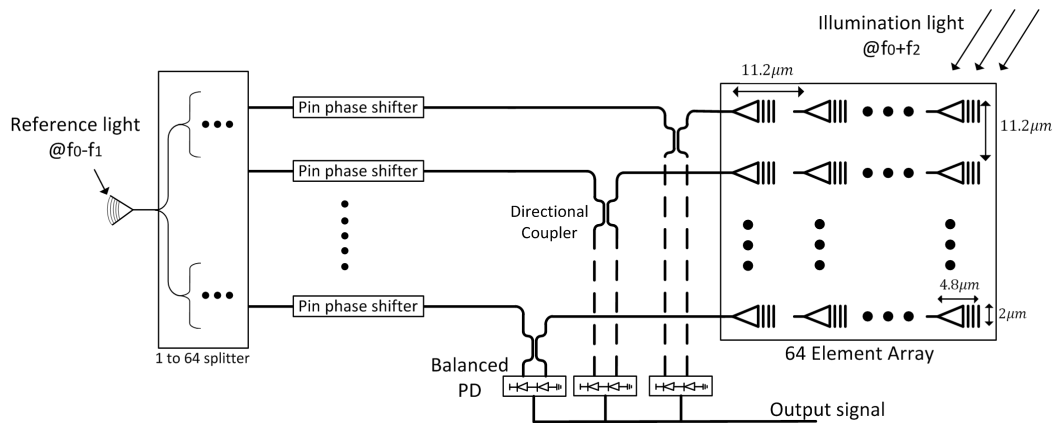


Figure 5.7: Block diagram of 8×8 phased array receiver

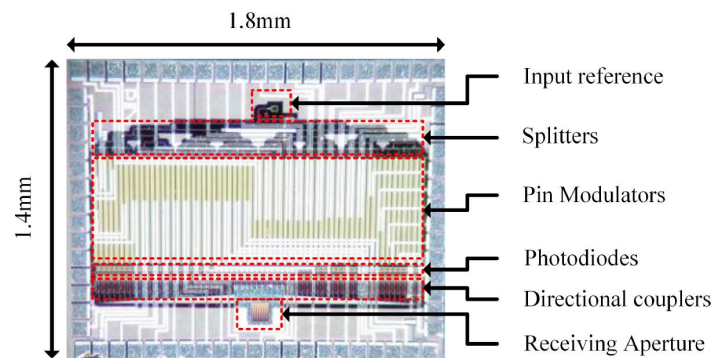


Figure 5.8: Die photo of fabricated 8×8 OPA receiver chip implemented in IME process.

to a spectrum analyzer for extracting and analyzing the data.

The reference light input to the chip is carried by a polarization maintaining optical fiber (PMF). The fiber tip is glued and fixed on the on-chip grating coupler so that movements of the measurement setup do not affect the reference signal intensity.

Optical setup includes a 1550nm laser, which is the only light source in the system. The output light of the laser is then split into two paths for reference and illumination. After passing through two polarization controllers, signals are input into two single side band (SSB) modulators. Polarization controllers are used to set the proper polarization for the SSB modulators. SSB modulators shift the optical frequency of illumination and reference light by $f_i = 1.15\text{MHz}$ and $f_r = 1.75\text{MHz}$, respectively. Therefore, the envelope of the mixed signal on the chip has the frequency of 2.9MHz. This frequency was chosen to be high enough to avoid the $1/f$ noise of the electronics and DC offsets. The output of SSB modulators passes through two other polarization

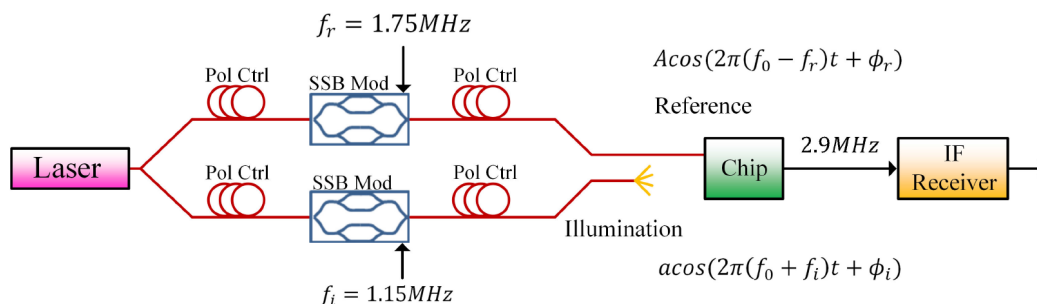


Figure 5.9: Block diagram of the measurement setup.

controllers. The reference path is fixed on the chip. To characterize the performance of the chip, a point source should be put at different angles in front of the chip. The output signal of the system at each angle for a given phase shifter setting yields the reception gain pattern. When a gazing beam is formed, light from most angles is rejected. Maximum output signal is achieved when the point source illuminates the chip from the gazing direction. In this setup, the point source is in a fixed location in front of the chip and the PCB is mounted on a turn table. By rotating the chip, the relative angle between the source and the chip is changed during the characterization process. The optical schematic of the setup is shown in Fig. 5.9.

5.5 Measurement and Results

Due to fabrication mismatches and surface roughness of the fabricated waveguides on the chip, the delay and phase shift that light experiences traveling through the waveguides deviates from an ideal rectangular waveguide. Therefore, a calibration process is needed to compensate for the phase offsets which are fixed values for each chip. To perform the calibration, the chip is aligned to be at the center of rotation on the turn table. The illumination fiber shines light on the aperture. The turn table is used in the measurement and calibration process to rotate the chip for different reception angles. Once all the phase shifters are adjusted, the received light from all the elements add up in phase. The output current amplitude is maximized for this setting. Therefore, a gazing beam is formed for the calibrated angle. A gradient ascent algorithm is used to maximize the output current amplitude by adjusting the phase shifters during the calibration process.

Measurement Results of One-Dimensional Receiver

After the calibration is finished, phase shifter settings for gazing beams of all the angles are achieved. By applying the setting for each angle, the gazing beam forms

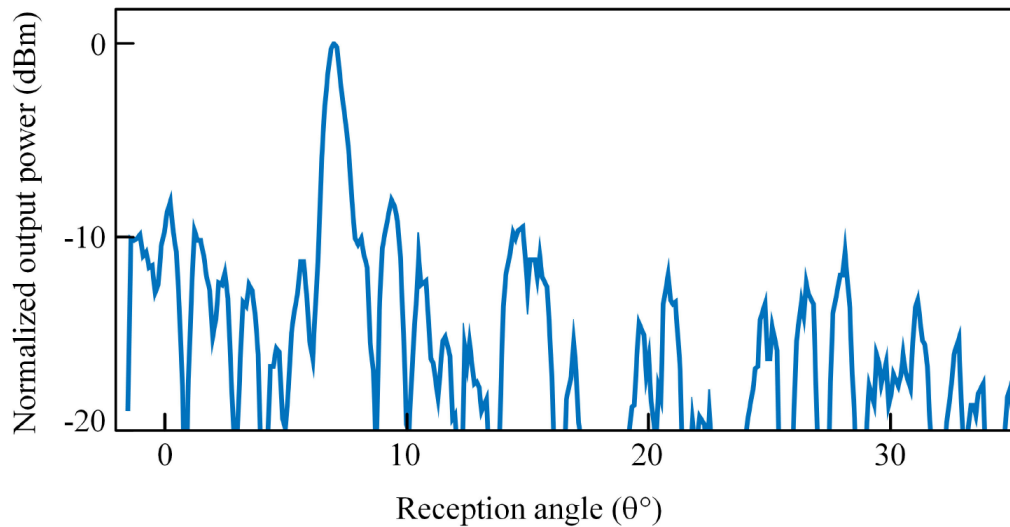


Figure 5.10: Measured reception pattern of the OPA receiver for 7° .

toward that angle. To characterize the reception pattern, phase shifters are set to the setting found by calibration for each angle. The reception patterns are extracted by rotating the turn table and measuring the amplitude of the output signal. The gazing beam for 7° is illustrated in Fig. 5.10. The width of the gazing beam is 0.74° . The first grating lobe happens at 30° which is consistent with the spacing between elements in this design. The maximum side lobe level is at least 10dB smaller than the main beam. The side lobe level can be further reduced by increasing the number of elements or adding amplitude control for the received signal at each element to improve the image quality.

Figure 5.11 shows the measured patterns for different angles from 0° to 30° . The phase shifter setting for each of these patterns is loaded to DACs through the microprocessor that is controlled with a desktop computer. By loading each setting, light coming from a certain direction is collected. Putting the information collected from all the angles together yields the image of the object in front of the chip.

To demonstrate the imaging capability of the OPA receiver, a barcode shape object is made by cutting through a copper sheet. A piece of diffusive paper is attached to the copper piece to scatter the light illuminating it. The dimension of the object is 2cm and it is put at 4cm in front of the chip to cover the 30° field of view. The object is illuminated from the backside. By scanning the reception angle the image of the barcode is captured. The schematic of the object, the physical object, and the captured image after applying correction for geometrical misalignments in gray

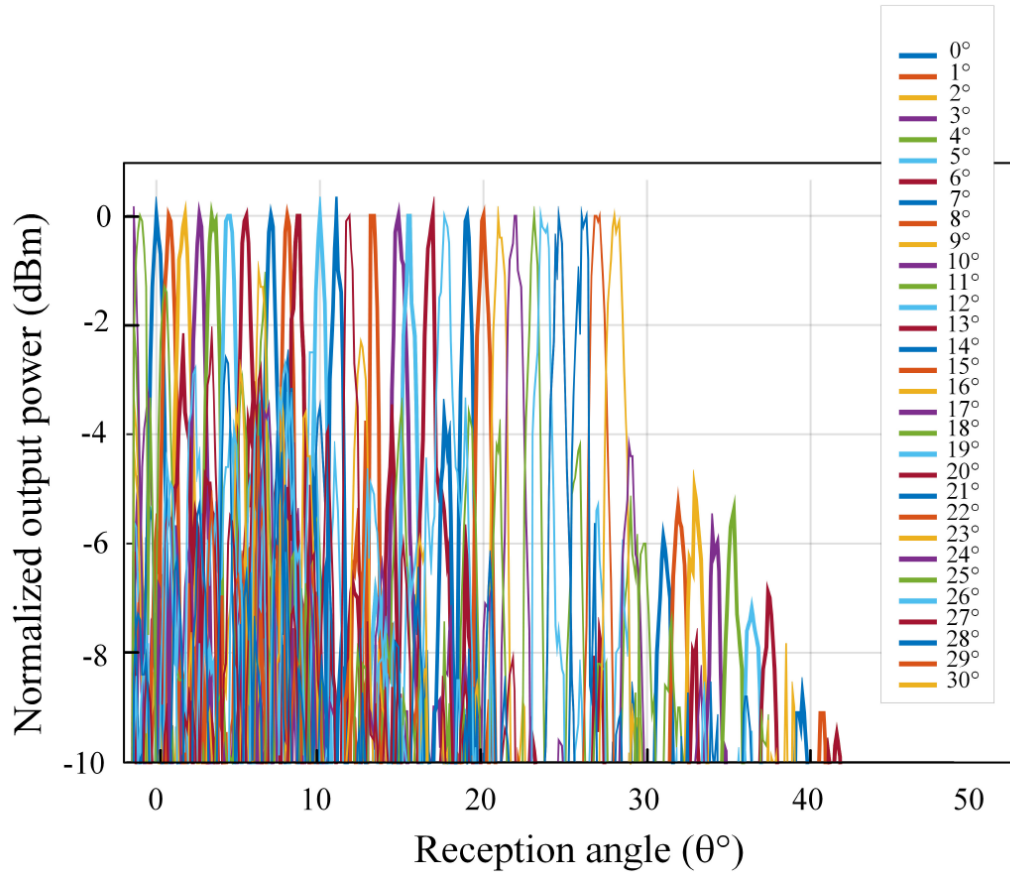


Figure 5.11: Measured reception pattern of the OPA receiver for $0^\circ - 30^\circ$.

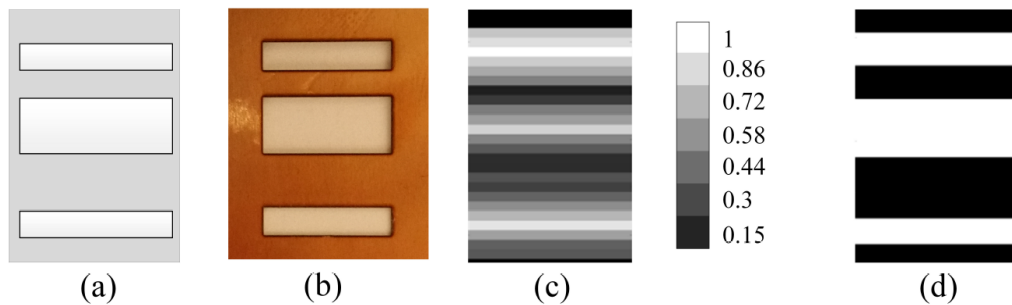


Figure 5.12: (a) Barcode design, (b) Fabricated barcode from copper sheet, (c)-(d) Captured image of the barcode in gray-scale and B&W with the OPA camera.

scale and black and white is shown in Fig. 5.12. The angle with the strongest captured signal is colored white. Black represents a signal at least 8dB weaker and the range in between is colored in gray scale. For the black and white image Fig. 5.12(d), -4dB is chosen as the threshold in the middle of the range.

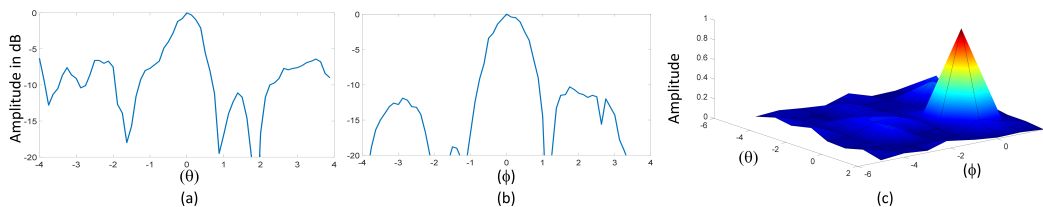


Figure 5.13: (a) Normalized receiving pattern cross section of yz-plane (b) Normalized receiving pattern cross section of xy-plane. (c) Normalized 3D pattern.

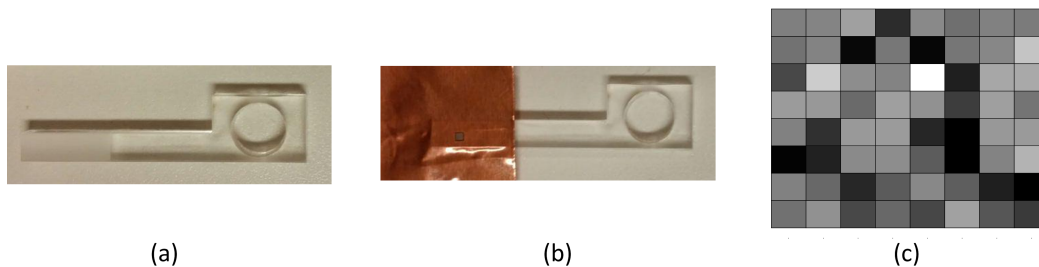


Figure 5.14: (a) Sanded plexiglass (b) Copper tape covered imaging target. (c) Captured image in gray scale.

Measurement Results of Two-Dimensional Receiver

The same calibration scheme used in 1D receiver is used to find the optimum settings of the 2D receiver. The result of optimization provides a lookup table for phase shifter settings to form receiving beams for different azimuth, ϕ , and elevation angles, θ . Figure 5.13 shows the measured receiving pattern after calibration for 0° . The beam width is 0.75° and grating lobes are 8° apart enabling an 8-pixel by 8-pixel image.

To illustrate the imaging function of the receiver, a copper tape with a hole is pasted on the plexiglass to block the light except at the hole. The surface of the plexiglass is sanded to enhance scattering, Figure 5.14a and 5.14b. The image of the object is captured by loading the phase setting for different angles and measuring the optical density at each pixel. Figure 5.14c shows the gray scale graph of the measurement result. The white bright spot clearly shows the position of the hole.

5.6 Conclusion

The first heterodyne optical phased array receiver is presented in this paper. The OPA receiver aperture is an array of receiving elements. The impinging light on the surface of the chip is processed on chip that functions as a phased array. The optical phased array chip can gaze into a desired angle that is electronically steerable. The OPA receiver chip operates as a lens-less camera by scanning the field of view and

capturing the light intensity coming from different directions. The operation principle and the design architecture are presented and the ability of the chip to capture the light arriving from a single direction is characterized. Imaging capability of the chip is also presented by imaging a simple barcode pattern as a proof of concept. Thirty two receiving elements are used for the receiving aperture. Increasing the number of receiving elements improves the resolution of such a camera.

LIDAR IMAGER WITH SUB-MM DEPTH RESOLUTION

6.1 Introduction

Three-dimensional (3D) imaging has many applications in bio-medical imaging, nano-particle characterization, security, robotics, and gesture recognition. Although 3D imaging systems have been studied, they are usually realized either as single pixel detectors [40, 64, 95, 114] or as bench-top systems with simple detector arrays [41, 84, 113]. Silicon nanophotonic processes use similar steps as their electronic counterparts, leading to higher yields, and compatibility with electronic integrated circuits. This combined with the low loss and high confinement of silicon waveguides [77] make the silicon photonics an ideal platform for coherent 3D imaging and projection systems [9, 12, 160] with high resolution and pixel count.

Infrared (IR) optical electromagnetic waves are promising candidates for high-resolution 3D imaging due to their short wavelength. These wavelengths can be processed efficiently by integrated silicon-on-insulator (SOI) nanophotonic platforms with high confinement and relatively low loss. A recent demonstration of phased array transmitters [9, 160] is an example of the advantage of SOI platforms in implementing complex nanophotonic systems. The high fabrication yields and potential for integration with silicon electronics necessary for additional signal processing make SOI nanophotonic processes a suitable platform for realization of nanophotonic coherent imagers (NCI) with large number of pixels in a small area at low cost. In this chapter we report a nanophotonic coherent imager that uses an array of integrated silicon photonics antennas to couple the impinging infrared electromagnetic wave into a series of nanophotonic waveguides, which coherently process the optical signals to measure the instantaneous phase and amplitude of the incident wave on each pixel to form a 3D image of the target object. An electrically generated frequency chirp is used to produce a linearly chirped optical wave that illuminates the object. A part of this optical signal serves as a reference and is coherently combined with the received signal by each pixel on the silicon nanophotonic chip to produce an electrical output. The proposed NCI uses time-domain signal detection and processing of this electrical output to resolve the relative phase and power of the incident wave at each pixel. This simultaneously enables high

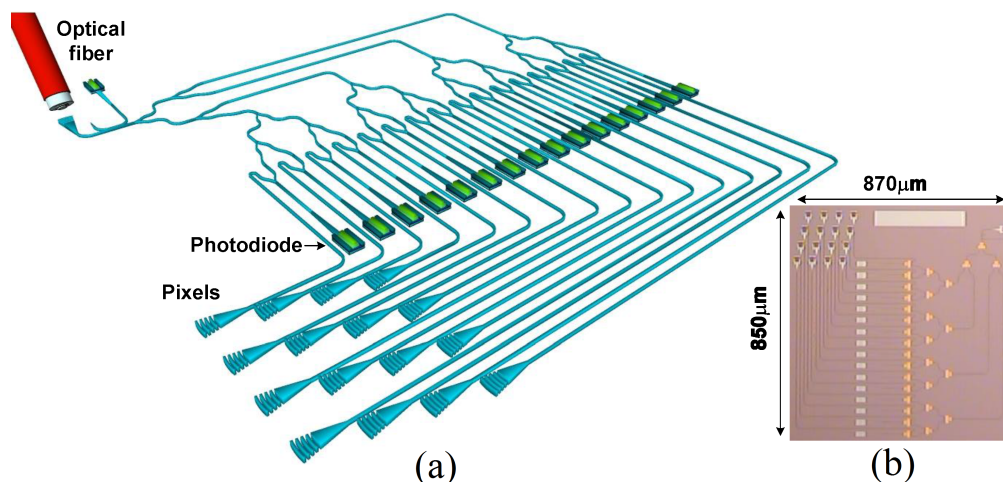


Figure 6.1: (a) The structure of the 4×4 NCI, in which the light coming from the object is collected using 16 grating couplers (pixels) is shown. A fraction of the coherent light that is used to illuminate the object is guided using an optical fiber and is coupled into the chip through a grating coupler. This coupled light is combined with the collected optical signals from the object and is photo-detected using on-chip silicon-germanium photodiodes. (b) The NCI micro-photograph implemented on standard IME silicon-on-insulator process.

depth resolution and large dynamic range, overcoming some of the limitations of conventional frequency domain FMCW approaches. The NCI chip can be used in 3D reflective, transmissive, and index contrast imaging modes with a high spatial resolution of about $15 \mu\text{m}$ over a large dynamic range of 0.5m without use of a wide range highly linear tunable laser source. To our knowledge, this is the first coherent imager that enables multiple phase sensitive imaging schemes via a single nanophotonic chip.

6.2 Coherent Imager Architecture

The structure of the 4×4 NCI is depicted in Fig. 6.1a. A part of the laser output that is used to illuminate the target object being imaged is coupled into the input grating coupler through an optical fiber and then is guided to a Y-junction splitter network through silicon nano-waveguides. This coupled coherent light, the reference signal, is split into 16 equal intensity optical signals. The incoming light from the object is coupled into nano-waveguides through an array of grating couplers [77] serving as pixels. The received light from each pixel is then combined with a part of the reference signal in a Y-junction combiner [87] and is converted to electrical current using a silicon-germanium photo-detector [92]. Figure 6.1b shows the NCI micro-

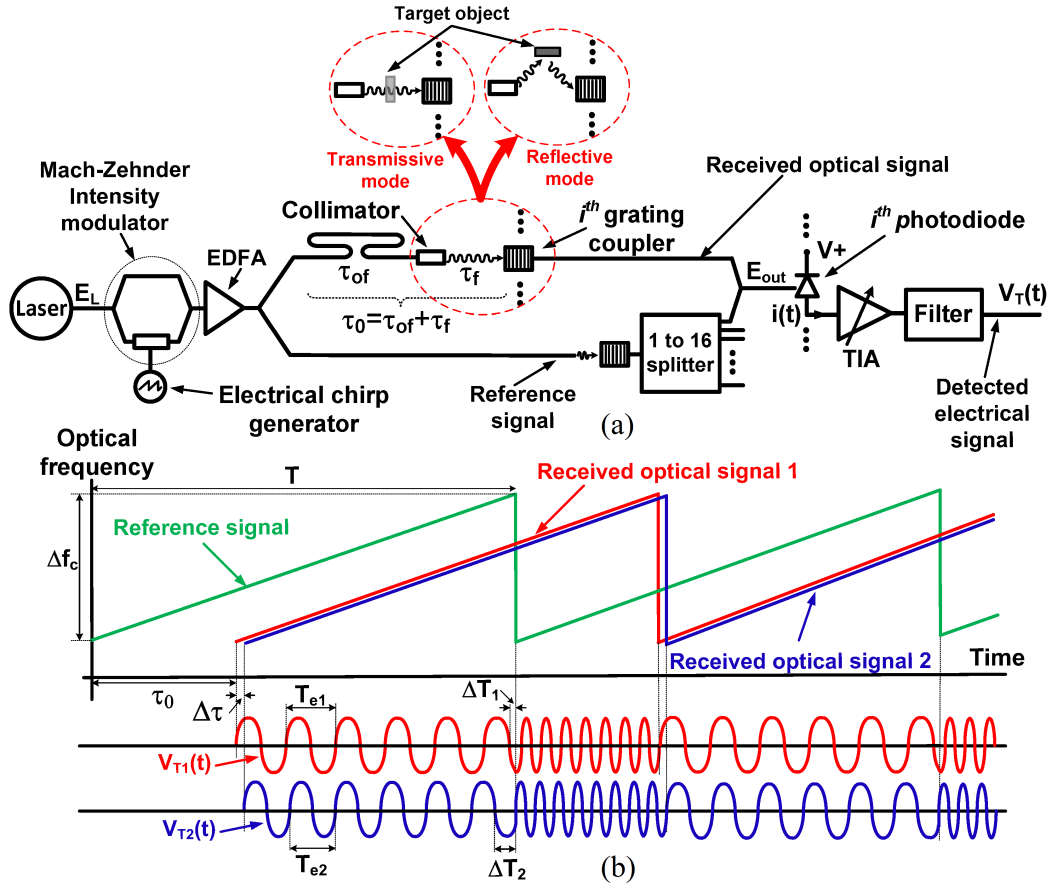


Figure 6.2: Simplified block diagram of the imaging system for one pixel (grating coupler) is shown. (b) The optical and electrical signals at different points of the imager are depicted. The number of zero crossings per chirp period is used as a coarse estimate for the delay difference between the top arm and the bottom arm. The time difference between the last zero crossing in $V_{T1}(t)$ and $V_{T2}(t)$ and the end of the frequency ramp is used to find the fine estimate for the relative delay between two arms.

photograph implemented on IME SOI photonic process [127]. The implemented NCI can be used in the transmissive, reflective, and index contrast imaging modes.

Theory of Operation

Figure 6.2a shows the imaging system for i^{th} grating coupler. The output electric field of the laser emitting with power P_0 at angular frequency ω_0 is represented by $E_L(t) = \sqrt{P_0}e^{j\omega_0 t}$. The laser output is intensity modulated with a frequency-chirped electrical voltage $v(t)$ using a Mach-Zehnder modulator (MZM). The use of an electrically generated frequency chirp eliminates the need for a tunable laser source with highly linear chirp response. An erbium-doped fiber amplifier (EDFA)

is placed after the modulator. The parameter G accounts for the gain of the EDFA and the loss of the MZM. The EDFA output is split into two branches using a fiber optic fusion coupler. The light in the top branch is collimated and used as the illumination source. Part of the light coming from the target object is coupled into the NCI chip by the i^{th} grating coupler. The light in the bottom branch, the reference signal, is also coupled into the NCI chip. The coupled reference signal is split into 16 branches and combined with the signal from the i^{th} grating coupler in a Y-junction. The Y-junction output is then photo-detected and the photo-current $i(t)$ is wire-bonded to the electronic circuit. The grating coupler efficiency and the on-chip waveguide loss in the top branch are represented by γ , while β accounts for the excess loss of the 1-to-16 on-chip splitter and the grating coupler efficiency. The total delay difference between the top and the bottom arms, τ_0 , consists of the delay in the optical fiber, τ_{0f} , and the free-space delay, τ_f . As shown in Fig. 6.2a, in the transmissive mode, the target object which is substantially transparent at the operating wavelength is placed between the collimator and the grating coupler. In this case, τ_f increases as the light slows down in the target object. In the reflective mode, the light is reflected from the object and forms an image on the pixel array (not shown). For this case, τ_f contains information on the spatial depth of the target object.

In order to study the principle of operation of the imager, it is useful to consider the case that the collimator is directly illuminating the pixel array and therefore, τ_f represents the free space delay and depends on the distance between the collimator and the pixel array. In this case, the electric field of the combined signal, E_{out} , can be written as

$$E_{out} = \frac{\sqrt{GP_0}}{4} e^{j\omega_0 t} \left[\sqrt{\beta} \left(1 + e^{j \frac{v(t)}{V_\pi} \pi} \right) + \gamma e^{-j\phi} \left(1 + e^{j \frac{v(t-\tau_0)}{V_\pi} \pi} \right) \right] \quad (6.1)$$

where V_π and ϕ are the MZM gain and the optical phase difference between the top and the bottom arms at the combining point, respectively. The electrical voltage $v(t)$ represents an electrical linear frequency-chirped signal and can be written as

$$v(t) = a_0 \cos \left(\omega_e t + 2\pi \alpha t^2 \right) \quad (6.2)$$

where a_0 , ω_e , and α , are the amplitude, the starting point of the electrical frequency chirp, and the frequency chirp rate in $\left[\frac{\text{Hz}}{\text{s}} \right]$, respectively. Substituting Eq. 6.2 into Eq. 6.1 and using the Jacobi-Anger expansion (i.e., $e^{jz \cos(\theta)} = \sum_{k=-\infty}^{\infty} (j)^k J_k(z) e^{jk\theta}$),

the DC and AC components of the photodiode current can be written as

$$i_{AC} = \frac{1}{4}RP_0G\sqrt{\beta\gamma}\cos(\phi)\sum_{n=1}^{\infty}J_n^2\left(\frac{a_0}{V_\pi}\pi\right)\cos\left(4n\pi\tau_0\alpha t + n\omega_e\tau_0 - 2n\pi\alpha\tau_0^2\right) \quad (6.3)$$

$$i_{DC} = \frac{1}{8}RP_0G\left[\beta + \gamma + \sqrt{\beta\gamma}J_0^2\left(\frac{a_0}{V_\pi}\pi\right)\cos(\phi)\right] \quad (6.4)$$

where R is the photodiode responsivity and J_n represents the Bessel function of the first kind. The photodiode current is amplified and converted to a voltage using an off-chip trans-impedance amplifier (TIA) with adjustable gain. Considering only the fundamental component, the output voltage, $V_T(t)$, can be written as

$$V_T(t) = \frac{1}{4}K_{TIA}RP_0G\sqrt{\beta\gamma}J_1^2\left(\frac{a_0}{V_\pi}\pi\right)\cos(\phi)\cos\left(4\pi\tau_0\alpha t + \omega_e\tau_0 - 2\pi\alpha\tau_0^2\right) \quad (6.5)$$

where K_{TIA} is the controllable gain of the TIA. Equation 6.5 shows that the frequency of the detected signal is a linear function of the delay difference between the received signal and the optical reference signal. This detection scheme is similar to that of a FMCW radar [97], since the optical reference signal and the detected signal at each pixel will be at different optical frequencies due to the difference in their propagation delays. Therefore, different time delays between the reference signal and the receive signal at each pixel results in different electrical frequencies detected at corresponding photodiode of the NCI chip.

Defining the frequency sweep range, $\Delta f_c = \alpha T$, and using Eq. 6.5 the period of $V_T(t)$ can be calculated as

$$T_e = \frac{T}{2\tau_0\Delta f_c} \quad (6.6)$$

where T is the chirp period. Two cases are studied in Fig. 6.2b. In case 1, the total delay difference between top and bottom arms in Fig. 6.2a is set to τ_0 . In case 2, the distance between the collimator and the i^{th} grating coupler of the NCI is slightly increased, such that this total delay difference increases to $\tau_0 + \Delta\tau$. For case 1 and case 2, electrical signals $V_{T1}(t)$ and $V_{T2}(t)$ with different frequencies appear at the output of the filter, respectively. By knowing the chirp rate α and counting the number of zero crossings in V_{T1} or V_{T2} , a coarse estimate for the delay difference τ_0 can be achieved. However, the amount of the small delay difference between cases 1 and 2, $\Delta\tau$, can not be estimated by counting the number of zero crossings of V_{T1} or V_{T2} . In order to find a fine estimate for $\Delta\tau$, the time difference between the last zero crossing in $V_{T1}(t)$ and $V_{T2}(t)$ and the end of the frequency ramp (i.e., ΔT_1 and ΔT_2) can be used. First, from Fig. 6.2b the chirp period, T , can be written in terms

of the periods of V_{T1} and V_{T2} as

$$T = \tau_0 + NT_{e1} + \Delta T_1 = \tau_0 + \Delta\tau + NT_{e2} + \Delta T_2 \quad (6.7)$$

where N represents the number of full periods of $V_{T1}(t)$ or $V_{T2}(t)$ that appears within the chirp period T . In this case, assuming $\Delta\tau \ll \tau_0$, the difference between ΔT_1 and ΔT_2 can be calculated as

$$\Delta T_2 - \Delta T_1 = N(T_{e1} - T_{e2}) \quad (6.8)$$

Using Eq. 6.6 the difference between the periods of $V_{T1}(t)$ and $V_{T2}(t)$ can be written as

$$T_{e1} - T_{e2} = \frac{T}{2\Delta f_c} \left(\frac{1}{\tau_0} - \frac{1}{\tau_0 + \Delta\tau} \right) \stackrel{\Delta\tau \ll \tau_0}{\approx} \frac{T}{2\Delta f_c} \left(\frac{\Delta\tau}{\tau_0^2} \right) \quad (6.9)$$

Also, from Fig. 6.2b, $N = \frac{T - \tau_0}{T_{e1}}$ is calculated. In practice, τ_0 is much smaller than the chirp period T and hence, $N = \frac{T}{T_{e1}}$ is assumed which together with Eqs. 6.6, 6.8, and 6.9 can be used to find $\Delta\tau$ as

$$\Delta\tau = \frac{\tau_0}{T} (\Delta T_2 - \Delta T_1) \quad (6.10)$$

Therefore, the minimum detectable delay or the delay resolution is written as

$$\Delta\tau_{\min} = \frac{\tau_0}{T} (\Delta T_2 - \Delta T_1)_{\min} \quad (6.11)$$

where $(\Delta T_2 - \Delta T_1)_{\min}$ is the minimum detectable value for $(\Delta T_2 - \Delta T_1)$ which is mainly limited by the total timing jitter of the detected electrical signal. This total timing jitter depends on the timing jitter of the electronic detection system, the timing jitter of the electrical chirp generator, and the signal-to-noise ratio (SNR) at the input of the electronic detection system. Note that $\Delta\tau_{\min}$ sets the imaging resolution in all NCI modes of operation as it defines the smallest detectable thickness for a given refractive index in transmissive mode, the smallest detectable refractive index variations for a given thickness in index contrast imaging mode, and the depth resolution in reflective mode. For example, defining the depth resolution in free space as $\Delta x_{\min} = \frac{1}{2}C_0\Delta\tau_{\min}$ in reflective mode, for a $(\Delta T_2 - \Delta T_1)_{\min}$ of 5ns, $\tau_0 = 5ns$, and $T = 0.5ms$, a depth resolution of $\Delta x_{\min} = 7.5\mu m$ can be achieved. The factor of $\frac{1}{2}$ is added to account for half of the round-trip delay in the reflective mode. Also note that even if the number of zero crossings for $V_{T1}(t)$ and $V_{T2}(t)$ are not the same within the chirp period, T , the aforementioned $\Delta\tau_{\min}$ calculation can be used for fine resolution detection, as the electrical receiver measures T_{e1} and T_{e2} accurately

and accounts for different number of zero crossings per chirp period for $V_{T1}(t)$ and $V_{T2}(t)$.

One important challenge in the implemented NCI is that the phase difference between the top and bottom arms in Fig. 6.2a, ϕ , may vary slowly with time due to the presence of a thermal gradient between two arms. This results in a slow amplitude fluctuation for the detected signal as Eq. 6.3 suggests. However, the DC component of the photo-current in Eq. 6.4 also experiences the same thermal fluctuation and is used to form a phase correction loop by placing a thermal phase modulator on the optical reference signal path. This feedback loop together with an automatic gain control (AGC) loop in electronic detection circuit keeps the amplitude of the detected electrical signal constant. Also, note that the variations in the term $(\omega_e \tau_0 - 2\pi\alpha\tau_0^2)$ in Eq. 6.5 are negligible compared to ΔT_1 (or ΔT_2) and do not affect the performance of the reported imager.

Transmissive Imaging Mode

The block diagram of the transmissive measurement setup is illustrated in Fig. 6.3a. A laser source is intensity modulated with a frequency-chirped electrical signal. In transmissive imaging mode, the collimated beam passes through the object and impinges on the NCI chip. The generated photo-current resulting from beating the reference optical signal and the received signal by each pixel is amplified using an array of TIAs, filtered, and captured by the detection system. In this mode, the object being imaged is substantially transparent at the laser operating wavelength. The object is placed between the collimator and the NCI chip. In this mode, a motorized micro-positioner moves the object by equivalently 16-pixel increments to emulate a larger pixel array. At each position, different parts of the collimated beam that are passing through the parts of the object with different spatial depths experience different time delays when arriving at the corresponding pixels of the NCI chip.

As discussed in section 6.2, the coarse spatial depth of the object being imaged is automatically calculated by counting the number of zero-crossings per chirp period and the fine spatial depth of the object is calculated by measuring the time difference between the last zero crossing in one chirp period to the end of the chirp period. By combining these coarse and fine depth detection schemes, a very fine depth resolution over a large spatial dynamic range can be achieved.

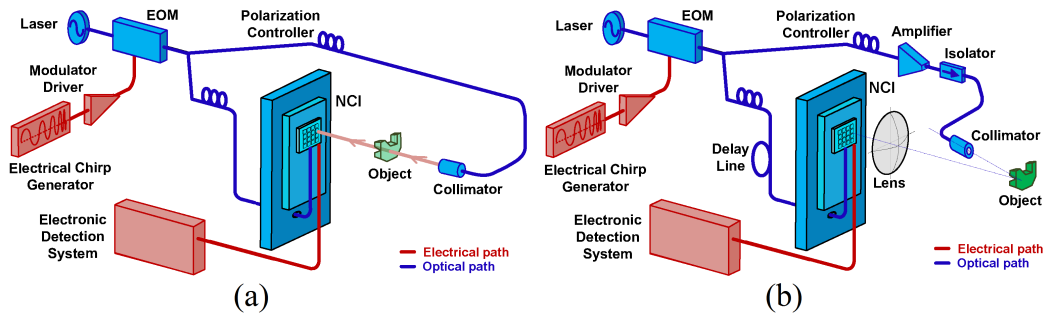


Figure 6.3: The block diagram of the transmissive measurement setup using integrated NCI is shown. The collimated infrared beam passes through the substantially transparent object (at the operating wavelength) and is collected by the 16 pixels of the imager. The collected optical signal is combined with the reference signal, a fraction of the coherent source output is used for illuminating the object, and is photo-detected. The photo-current is then directed to the electronic detection system. (b) The block diagram of the reflective mode measurement setup is depicted. The amplified output of the coherent source is collimated and is used to illuminate the object. A lens is used to form an image on the NCI pixel array.

Reflective imaging mode

In the reflective measurement setup, a collimator is used to coherently illuminate the object and the image is formed on the pixel array using a lens, as depicted in Fig. 6.3b. The detection scheme is identical to that of the transmissive mode. However, the optical power at the output of the collimator is increased to improve the signal-to-noise ratio at the input of the electronic detection system. In this mode, to emulate a larger pixel array, the pixel array is moved using an automated micro-positioner with increments of 4×4 pixels while keeping the lens stationary.

6.3 Measurement results

The NCIs were fabricated in IME silicon-on-insulator technology node [127] where silicon-on-insulator wafers with a $0.22\mu\text{m}$ top silicon layer and $2\mu\text{m}$ buried oxide are used. Three levels of silicon etching were available. The pixels are lensed grating couplers with effective area of $17\mu\text{m} \times 17\mu\text{m}$ and with 40% average coupling efficiency that were designed using two levels of etching. Traveling wave photodiodes were designed based on epitaxial growth of germanium on top of silicon waveguides and have measured responsivity of 0.7A/W . An average optical loss of 1.8dB/cm for a 500nm wide and 220nm thick silicon waveguide was measured. Two aluminum metal layers with thickness less than $1.5\mu\text{m}$ were available. No post processing was done on the fabricated chips. The fabricated chips were mounted on a printed

circuit board (PCB) and electrically connected to the PCB using bond wires while the optical fiber carrying the reference optical signal was attached to the reference grating coupler. No temperature control was required. All measurements have been carried out at the room-temperature.

For all measurements, a laser source emitting at $\lambda_0 = 1.55\mu\text{m}$ is intensity modulated with a frequency-chirped electrical signal. The frequency of the electrical signal increases linearly with time from 1MHz to 3.8GHz, over $500\mu\text{s}$, periodically. To measure the minimum depth resolution in the transmissive mode, first the collimator output power is set to 10mW. In this case each grating coupler receives about $4\mu\text{W}$. Then, the free-space distance between the collimator and the NCI is changed using the motorized micro-positioner. For each position, 10 measurements per pixel were conducted. The measured distance vs. actual distance is depicted in Fig. 6.4a. The error bars on this graph represent the range of all 160 measurements for each distance setting. The highest range of error occurs for the $100\mu\text{m}$ distance measurements (shown as an inset) where a $15\mu\text{m}$ deviation from the actual value can be observed corresponding to a $15\mu\text{m}$ depth resolution. This depth resolution is in close agreement with the predicted value from Eq. 6.11, for $(\Delta T_2 - \Delta T_1)_{\text{min}} \approx 5\text{ns}$, $\tau_0 = 5\text{ns}$, and $T = 0.5\text{ms}$.

In a different experiment, a 40mm thick Plexiglas cube was placed next to two small pedestals with approximate thickness of $150\mu\text{m}$ and $225\mu\text{m}$, respectively (Fig. 6.4b-left). The 3D transmissive image shown in Fig. 6.4b-right demonstrates that a high spatial resolution over a large dynamic range can be achieved with a single measurement and without modifying the measurement setup and parameters. In another experiment, the 3D transmissive image of a hollow pyramid made of Plexiglas (Fig. 6.4c-top) was formed which is depicted in Fig. 6.4c-bottom. For all transmissive measurements, the output power of the collimator is set to 10mW. Due to scattering from abrupt edges of the target object, the SNR of the received signal at corresponding pixel may be reduced significantly resulting in inaccurate zero-crossing detection. To avoid this uncertainty, the pixels with low SNR are tagged automatically during the imaging stage and in the post-processing stage, their values are automatically replaced by the average of the surrounding pixels. Figure 6.4d shows the refractive index contrast imaging that is conducted using the transmissive imaging setup. In Fig. 6.4d-top, a sheet of Polycarbonate with typical index of 1.56 is placed next to a sheet of Plexiglas with typical index of 1.47. Both sheets have thickness of 1mm. The image in Fig. 6.4d-bottom shows a clear difference in the

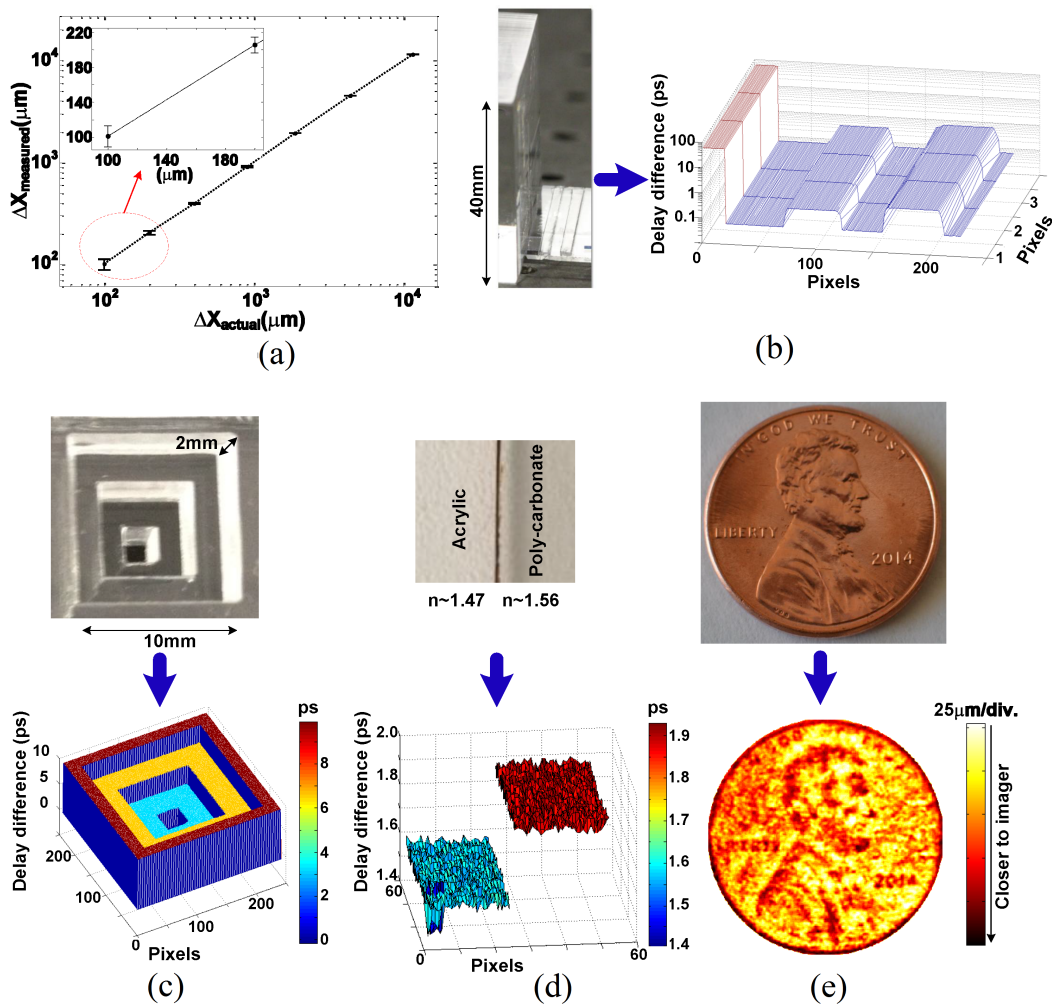


Figure 6.4: Fig. 4. (a) The measured distance vs. actual distance in μm for transmissive mode is shown. (b) The concurrent high depth resolution and large dynamic range offered by the integrated NCI in the transmissive mode is demonstrated. A 4cm object and two small pedestals with sub- $100\mu\text{m}$ depth difference are concurrently imaged (left: the object, right: the 3D image). (c) The transmissive 3D image of a transparent pyramid is shown (top: the object, bottom: the 3D image). (d) The index of refraction contrast imaging using integrated NCI is demonstrated; top: two materials with the same thickness, bottom: the index contrast image. (e) The depth image of the US one-cent coin taken using the integrated NCI in the reflective mode is shown. The measured free-space relative propagation delay corresponding to the image depth is represented by pixel colors; pixels represented by dark red are closer to the imager. The image is approximately extended over $140\mu\text{m}$ of spatial depth.

detected thickness corresponding to the contrast in the index of refractions of two materials.

In reflective mode measurements, the collimator output power is set to 120mW and each pixel receives about $0.2\mu\text{W}$ in presence of the lens. Fig. 6.4e-bottom shows the reflective depth image of a US one-cent coin (in Fig. 6.4e-top) where in the setup in Fig. 6.3b, a micro-positioner is used to move the 4×4 NCI with increments of 4×4 pixels (without moving the lens) to mimic a larger coherent pixel array. The 3D image in Fig. 6.4e-bottom has a depth resolution of about $15\mu\text{m}$ and lateral resolution of $50\mu\text{m}$ limited by the on-chip pixel spacing.

6.4 Conclusion

We have demonstrated a nanophotonic coherent imager implemented on a silicon photonics platform where all optical signal processing and detection is done on a single photonic chip. Use of low-cost and robust silicon photonics platform combined with modified FMCW detection scheme enables 3D imaging with high depth resolution of $15\mu\text{m}$ over a large dynamic range of 0.5m. Using the implemented integrated NCI, we have conducted high resolution index of refraction contrast imaging, 3D transmissive, and 3D reflective imaging. Use of silicon photonics platform enables realization of NCIs with a large number of pixels, making low-cost high performance NCIs available for a variety of applications in the near future.

*Chapter 7***A COMPACT HIGH POWER MM-WAVE RADIATOR FOR LOW VOLTAGE CMOS TECHNOLOGY****7.1 Motivation**

Low-cost mm-wave silicon integrated signal generation and processing enable many applications, such as silicon-based automotive radars for self-driving cars and wireless communications. One of the challenges encountered in commercialization of such systems is the high packaging and testing costs, and high sensitivity to antenna parameters, which can diminish the advantage of integrated silicon solutions. On chip antennas have been proposed as a solution to reduce the packaging costs [28, 38]. Using high resistivity substrates [49] or substrate thinning can significantly improve the radiation efficiency of the antenna and as a result the use of on chip antennas compared to off chip antennas will provide lower loss. Link budget analysis of systems (e.g., radar) necessitates high power (high EIRP) transmitters while system resolution analysis suggests higher frequency of operation for better spatial resolution. The scaling of CMOS transistors facilitates the latter requirement but unfortunately the lower breakdown voltage of the transistors reduces their maximum power handling capabilities at a given radiator impedance. Several approaches have already been implemented to address this issue each with its own shortcoming. Power combining multiple PA outputs with passive on-chip power combiners [45] adds extra loss and reduces the overall efficiency, spatial power combining using phased arrays [167, 186] consumes a large die area. Power combining at the antenna [[49, 124]] has been proposed as an approach to address these challenges. In this chapter, I will introduce a special PA/radiator power combining approach with optimal PA load design using strongly-coupled antennas in close proximity. This approach utilizes techniques of power combining in free space and favorable drive point impedance design, using on-chip power-amplifiers and radiators to achieve high radiated output power.

7.2 Radiator Design

As mentioned in the motivation chapter, spatial power combining in standard phased array systems consumes large die area as the array elements are spaced at half wavelength. In order to reduce area, it is possible to place the antennas closer to

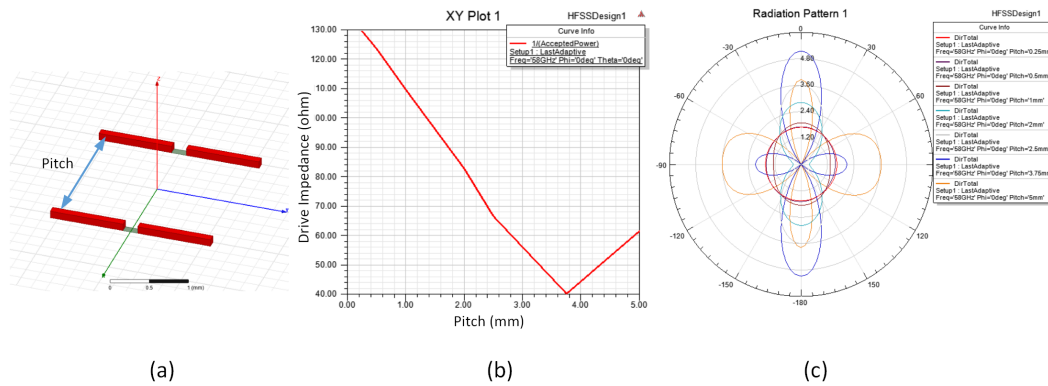


Figure 7.1: Coupling of two dipole antennas. (a) Simulation setup. (b) Effective drive impedance and (c) radiation pattern as a function of pitch of the two dipoles.

each other, however, bringing the antenna elements closer to each other introduces strong coupling between the antenna elements that needs to be addressed in order to design the correct driver for them. In order to observe the effect of coupling between densely packed antenna arrays and its effect on driver impedance, we start with two simple antennas and gradually decrease the distance between them. Among the different antenna structures, liner antennas such as dipole and slot antennas are more suitable for small area array placement since they have small dimensions across the antenna and can be placed closely to each other.

Figure 7.1 shows the simulation results of two dipoles as they get closer to each other. In the simulation setup, each dipole is driven with a voltage source, V , with magnitude of 1V and the total radiated power, $P_{rad,total}$ (which is equal to accepted power in case of perfect conductors) is calculated in simulation. The effective antenna resistance when both ports are driven in phase can be calculated by using the following equation:

$$R_{ant} = \frac{V^2}{2(P_{rad,total}/2)} \quad (7.1)$$

Because of symmetry half of the radiated power is associated to each dipole, hence, the $2(P_{rad,total}/2)$ is used in the denominator. The result of effective antenna resistance is shown in Fig. 7.1(b). When the antennas are far from each other, their mutual coupling is small and each antenna has a resistance close to a single dipole resistance. As they become closer, their coupling increases. In a dipole antenna the coupling between the antennas is such that the induced voltage from one antenna is in phase with the voltage driven from the other antenna and as a result the current flowing from the ports reduces and the impedance goes higher. In the limit case that the pitch reduces to zero, two ports are effectively in parallel and driving a single

dipole antenna and as a result each port will see twice the impedance of the dipole antenna. Similar simulation and discussion can be made when there are more than two dipole antennas in the array. Suppose that there are N “tightly” coupled dipole antennas in a sub-wavelength array. The $N-1$ antennas that couple to i^{th} antenna will effectively reduce its port current by a factor of N , and thus the driving impedance will increase by a factor of N .

Clearly dipole antennas are not suitable for sub-wavelength array spatial power combining in CMOS. The reason is that while power combining may be obtained by using multiple antennas, the increase in drive impedance makes matching to the antennas a challenge. In CMOS technology the voltage swing that can be achieved from transistors is limited by the breakdown of the transistors which has reached below a volt in recent advanced nodes. Transistors output impedance, however, can be easily lowered by utilizing more fingers in parallel. So in order to extract more power from CMOS transistors, it is desirable to lower the antenna impedance so that more power can be extracted from the transistors. In a dipole array with N tightly coupled elements, the total radiated power with fixed voltage swing is given by:

$$P_{rad,array} = N \times \frac{V^2}{R_{port}} \quad (7.2)$$

$$= N \times \frac{V^2}{NR_{dipole}} \quad (7.3)$$

$$= \frac{V^2}{R_{dipole}} \quad (7.4)$$

$$= P_{rad,dipole} \quad (7.5)$$

So effectively no power enhancement is obtained by using tightly coupled dipole antennas.

Now let's consider slot antennas which are dual of dipole antennas. Using Babinet's principle [36], it is expected that impedance of the slot antennas will be lowered as they are placed in an array. Simulation verifies this theory and it can be explained easily if we notice that the coupling between slot antennas is such that a voltage source on one slot induces a voltage with 180° phase shift compared to the other slot voltage source, as a result the current that passes through the other port increases and the impedance is dropped.

Figure 7.2 shows an example of tightly coupled slot antenna array and the effective driving impedance and radiated power for different number of elements. If the

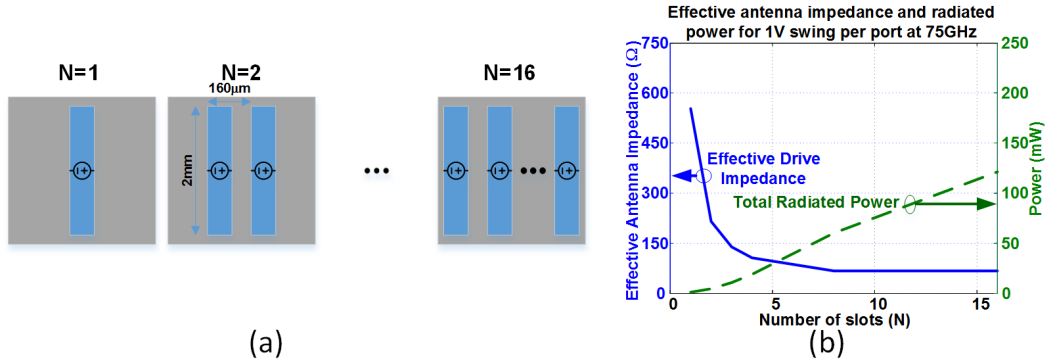


Figure 7.2: (a) An example of tightly coupled slot array antenna. (b) Effective drive impedance of tightly coupled slot antennas and total radiated power assuming 1V swing per port.

tight coupling is maintained, the effective driving impedance for N elements will be $R_{port} = R_{slot}/N$, as a result, the total radiated power is as follows:

$$P_{rad} = N \times \frac{V^2}{R_{port}} \quad (7.6)$$

$$= N \times \frac{V^2}{R_{slot}/N} \quad (7.7)$$

$$= N^2 \times \frac{V^2}{R_{slot}} \quad (7.8)$$

$$= N^2 P_{rad,slot} \quad (7.9)$$

Thus, for tightly coupled slots, the radiated power increases quadratically as the number of elements increases. Of course there is a limit to this scaling. As the number of slots increases and their distance increases (assuming a minimum feasible pitch), the tightly coupled condition does not hold anymore and the impedance does not scale anymore. For an infinite size array the impedance converges to a value that is pitch dependent. The smaller is the pitch, the smaller will be the impedance. As a result the radiated power will asymptotically become linearly proportional to N as number of elements increases. This change of growth rate can be seen in Fig. 7.2(b) after $N=8$.

The discussion above assumed no substrates for the antennas. With the substrate in place, the equations will not be as straightforward as the substrate modes will affect the port impedance. Adding new elements or changing the pitch of the elements will excite different substrate modes and hence both the radiation pattern and antenna impedance will be affected. The CMOS process we use has a $300\mu\text{m}$ thick silicon

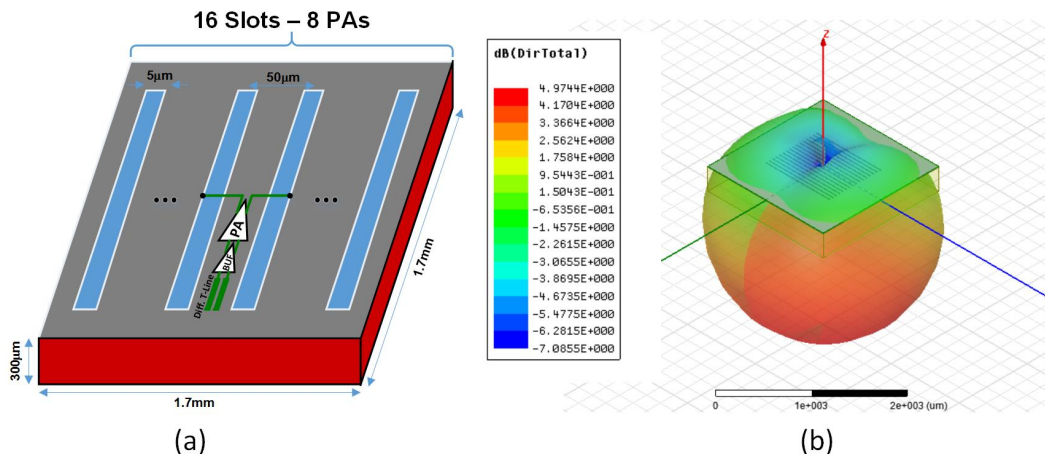


Figure 7.3: (a) Dimension of implemented on chip slot array. (b) Simulated radiation pattern.

substrate. At 77GHz this thickness does not support resonant modes, however there exist sidewall reflections that affect the trend seen above.

The pitch of array was forced by the minimum size the PA could be fit and the number of elements were chosen to be 16 as it was the closest power of two integers that would make a square-shaped overall radiator. The dimensions of implemented integrated antenna are shown in Fig. 7.3(a) and the associated radiated pattern is shown in Fig. 7.3(b). The antenna achieves 46% radiation efficiency. The slot antenna was designed such that the impedance seen from each port is inductive to cancel out the parasitic capacitances of the transistors. As it can be seen from Fig. 7.4, the radiator stays inductive for a broad range of frequencies and a relatively wideband operation is obtained from the antenna.

The schematic and layout of the PA is shown in Fig. 7.5. Since the driving impedance is small, the transistors need to be sufficiently large to be able to drive the port. As a result large input capacitance is presented in the cascode node and also the input of the PA. These large capacitances consume large power if not properly resonated out. A shunt resonant inductor was designed to cancel out the capacitance of the cascode node and improve the PA efficiency. The input capacitance of the PA was absorbed in the Buffer's output inductor. The required inductance was very small due to large parasitic capacitances and high frequency of operation and as a result the inductors could fit within the allocated space.

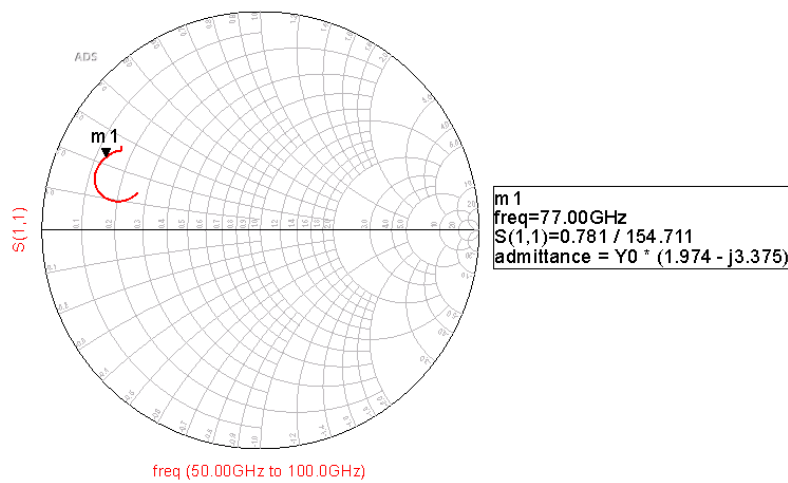


Figure 7.4: Effective impedance of radiator from each port (All ports are driven in phase).

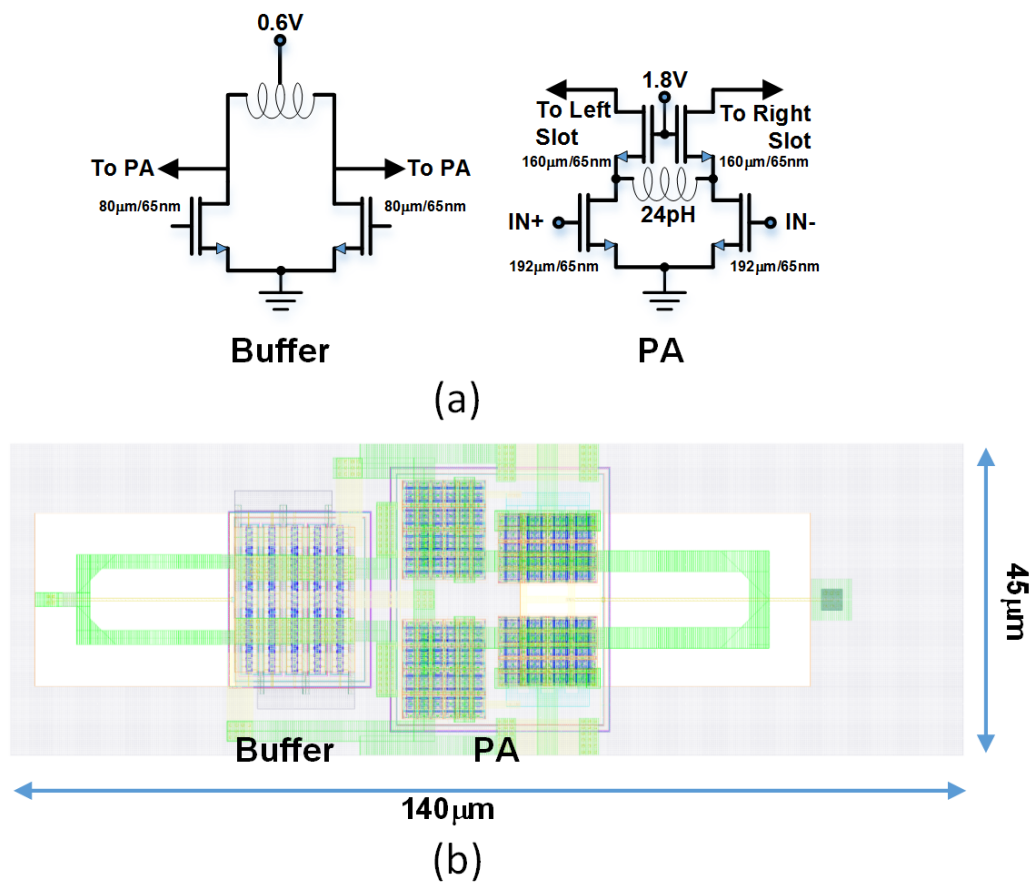


Figure 7.5: (a) Schematic of PA driver (Buffer) and PA. (b) Layout of the PA and Buffer

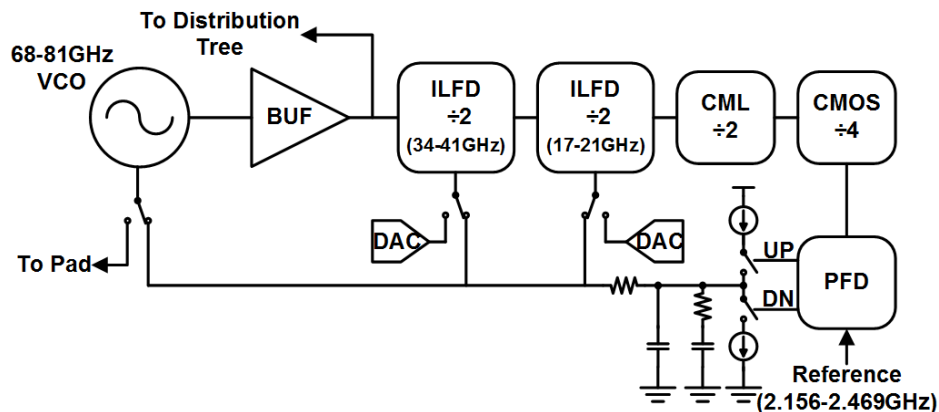


Figure 7.6: Block diagram of implemented IC.

7.3 PLL Design

In order to be able to incorporate the individual ICs as radiating elements in a larger phased array system, a phase locked loop was implemented to synchronize the radiators in the array. The designed PLL multiplies the 2.156GHz-2.489GHz input by a factor of 32 to achieve 10GHz of tuning range centered at 74GHz. It is possible to use the PLL for synthesis of wide-band chirp required for accurate distance measurements in radars. The 10GHz locking range allows one to achieve 1.5cm of depth resolution.

The block diagram of implemented IC is shown in Fig. 7.6. The VCO is a cross coupled oscillator with no current tail and was designed to provide a tuning range of 67GHz to 83GHz. The first two stages of frequency dividers are injection locked frequency dividers that utilize varactors to enhance the locking range of the dividers. The tuning range of each divider was designed to be half of the previous stage such that similar control voltage that controls the VCO can be used to tune the injection lock dividers. The schematics of the VCO and injection locked frequency dividers (ILFD) are shown in Fig. 7.7. The ILFD is an oscillator whose center frequency is designed to be half of the VCO center frequency. The VCO forces zero crossing on the output of ILFD oscillator at each cycle of VCO frequency. As a result any phase drift in the free running ILFD is reset twice on each cycle and hence the ILFD phase locks to the VCO. ILFD consumes less power than a flip-flop based divider but does not provide quadrature outputs.

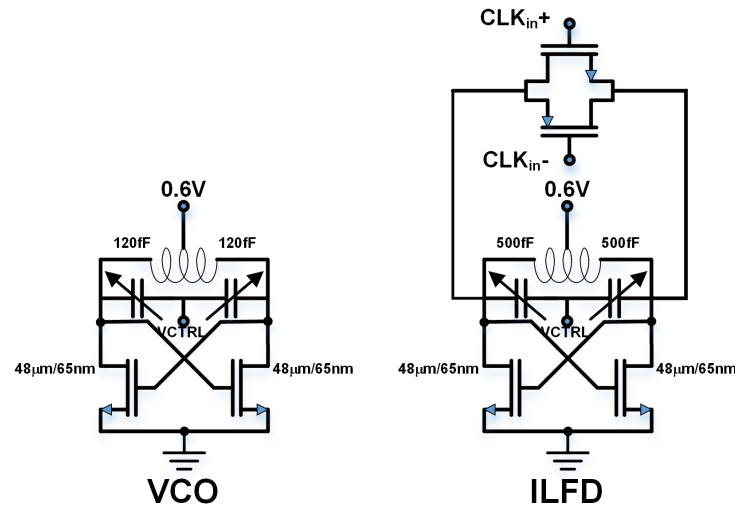


Figure 7.7: Schematic of VCO and ILFD

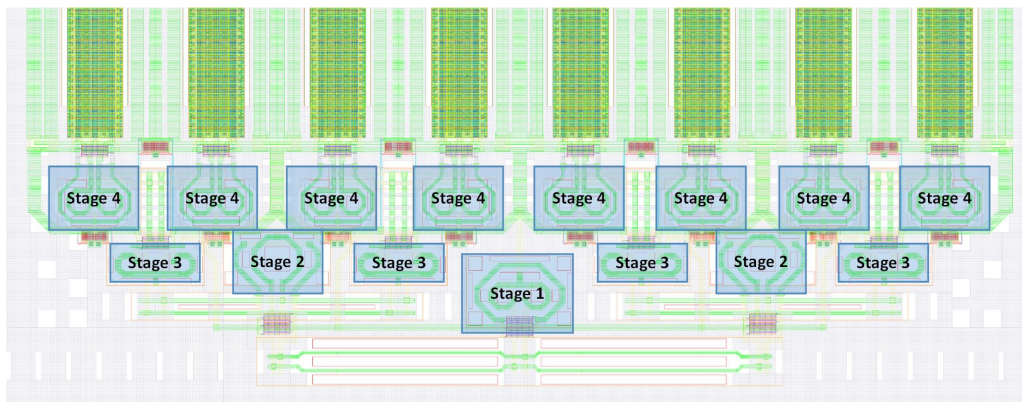


Figure 7.8: Layout of the 77GHz distribution tree.

7.4 Distribution Network

A half H-tree clock distribution network was designed to distribute the 77GHz signal across the chip. Each antenna port has to be driven in phase, and therefore a symmetric H-tree distribution is needed. Four buffer stages were designed to split the signal from the VCO to the 16 antennas (the last stage of buffer drives two PA buffers). The design started from the PA input and the next stage was designed with the loading of previous stage including the loading from the traces accounted for. The layout of the distribution tree is shown in Fig. 7.8.

7.5 Measurement Results

The chip was fabricated in TSMC 65nm process. The die photo of the chip is shown in Fig. 9.22(a). Top aluminum layer was used as the antenna layer. Design

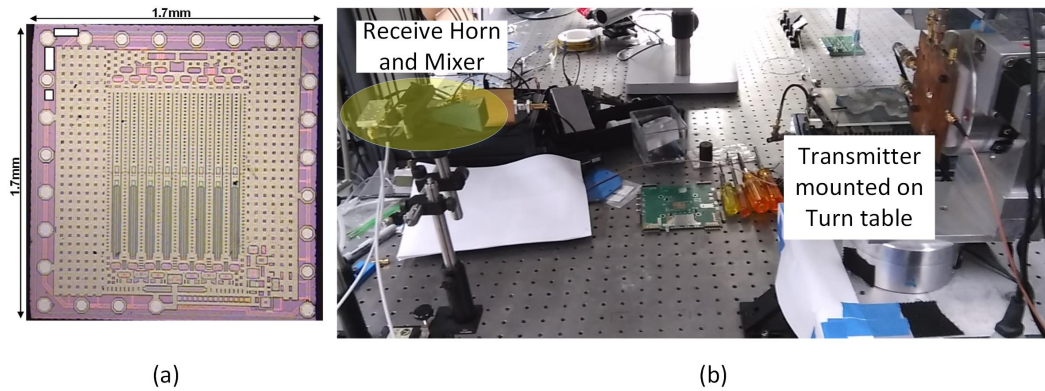


Figure 7.9: (a) Die photo of fabricated chip. (b) Measurement Setup

rules of fabrication requires cheeing the aluminum layer, but since the holse are much smaller than the wavelength, they should not affect the radiation pattern. The cheeing was avoided on the edge of the slots where the maximum current density was observed in EM simulation. The openings in the aluminum layer for the transmission lines and inductors were kept smaller than wavelength by periodically connecting the opening with either RDL layer or using lower metal layers.

The chip was placed inside the square that was cut from a PCB and wirebonded to the PCB traces. In order to provide thermal pathway to for the chip, a CVD grown diamond film was placed on the backside of the chip. HFSS simulation revealed severe pattern degradation (multiple lobe emission) due to the excited modes in the diamond slab. Investigation of other different shapes and slab thicknesses and materials resulted in using an aluminum oxide hemispherical lens with a diameter of 6.35mm. Since alumina's dielectric constant is very close to that of silicon, the radiative fields will not bounce back on the chip/lens interface and no substrate modes are excited in the silicon substrate. HFSS simulation also demonstrated that the radiation efficiency increases from 46% to 51% through use of alumina lens. Thinning the substrate from $300\mu\text{m}$ to $100\mu\text{m}$ also increased the radiation efficiency to 75%, but in our measurements we did not thin down our substrates.

Measurement Setup

The radiator was mounted on a computer controlled turn table for pattern measurement. Absolute power measurements for measuring EIRP was performed using Agilent V8486A and W8486A power sensors with 15dBi WR-15 and 25dBi WR-12 standard horns, respectively. The spectrum and pattern measurements were performed by down-converting the signal using PMP-WM harmonic mixer and

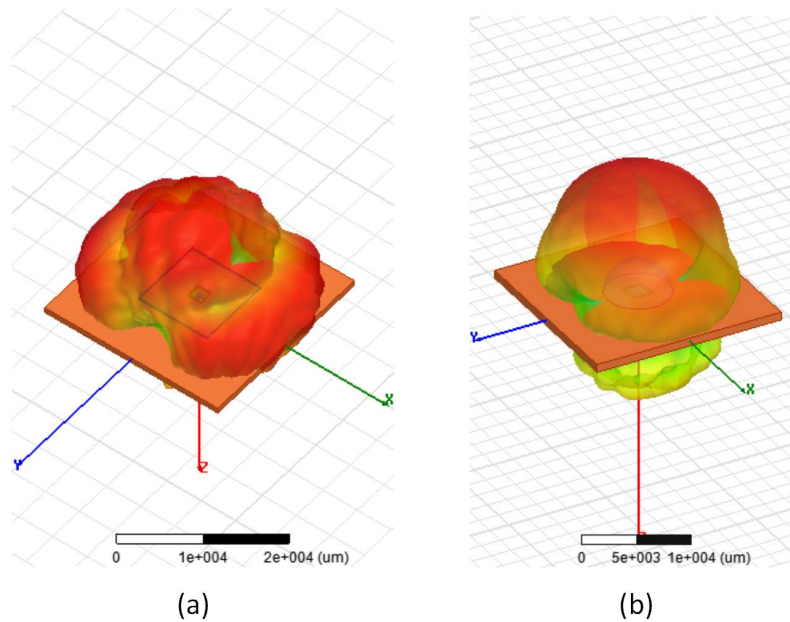


Figure 7.10: (a) Radiation pattern with $1\text{ cm} \times 1\text{ cm} \times 300\mu\text{m}$ diamond heatsink and (b) with 6.35mm diameter hemispherical aluminum oxide lens.

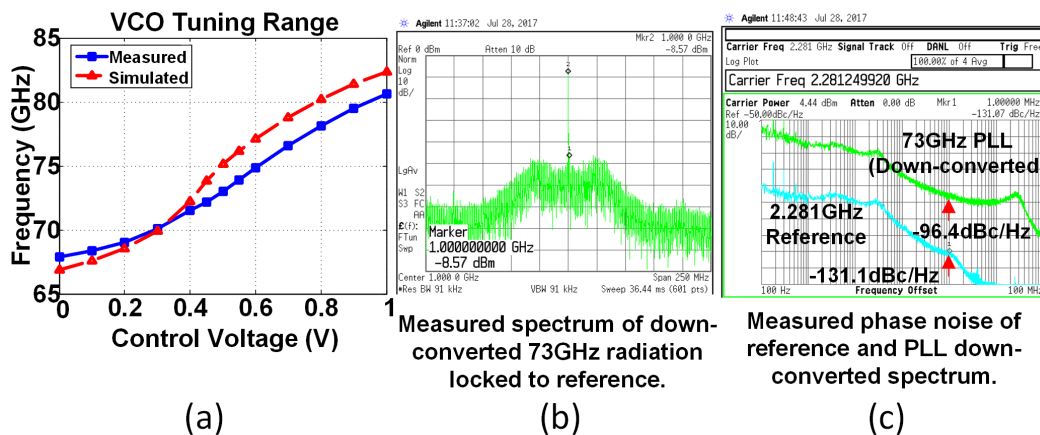


Figure 7.11: (a) Tuning range of VCO. (b) Down-converted spectrum of locked PLL at 73GHz. (c) Phase noise measurement of the VCO

observing the spectrum on an Agilent E4448A spectrum analyzer.

PLL Tuning and Phase-noise

Fig. 7.11 shows the spectrum and frequency measurement of the system. The VCO tuning range was directly measured by breaking the PLL loop and connecting the VCO control voltage to a pad via an SPDT switch (the switch is shown in Fig. 7.6). The measurement closely tracks the simulation but the turning range is slightly

lower in the measurement that can be attributed to inaccurate varactor modeling. The phase locked spectrum of 73GHz signal after downconversion is shown in Fig. 7.11(b). The output phase noise of the oscillator was also measured and is plotted in Fig. 7.11(c). Below the PLL bandwidth, the phase noise is determined by the reference phase noise. Due to 32 multiplication factor, the PLL had around 30dB higher phase noise compared to the reference.

Radiation Pattern

The radiation pattern of the antenna was measured using the turn table and standard horn antenna. The full 3D pattern measurement was used to measure the antenna absolute directivity using the following equation:

$$D(\theta, \phi) = \frac{EIRP(\theta, \phi)}{TRP} \quad (7.10)$$

$$= \frac{EIRP(\theta, \phi)}{\frac{1}{4\pi} \int_0^{2\pi} \int_0^\pi EIRP(\theta, \phi) \sin \theta d\theta d\phi} \quad (7.11)$$

$$\approx \frac{4\pi \times EIRP(\theta, \phi)}{\sum_{i=1}^N \sum_{j=1}^M EIRP(i\Delta\theta, j\Delta\phi) \sin(i\Delta\theta)} \quad (7.12)$$

Note that the EIRP is present at both the nominator and denominator, so absolute (calibrated) measurements of EIRP is not necessary for directivity measurements. As long as the mixer stays in the linear region, the unnormalized power read from the spectrum analyzer is sufficient for directivity measurements.

Figure 7.12 shows the measured patterns of the antenna at several frequencies. As it can be seen the measured pattern matches very well with the simulated pattern at 77GHz and the antenna pattern stays fairly consistent over the frequency of tuning range.

The EIRP of the antenna was measured using standard horn antennas and Agilent V8486A and W8486A power sensors. The exact gain of the horn antenna was calculated using online tools [2] for each given frequency. The measurements were done over three different distances and EIRP was calculated using Friis equation and measured power by the power sensors using the following equation:

$$EIRP(dBm) = P_{PA} + G_{ant} \quad (7.13)$$

$$= TRP + D_{ant} \quad (7.14)$$

$$= P_{RX}(dBm) - G_{RX}(dB) + 20 \log [R(m)] + 20 \log [f(GHz)] \quad (7.15)$$

The measurement shows a maximum directivity of 13dBi and EIRP of 35.7dBm for the IC operating from a 1.8V PA supply while consuming 1006mA.

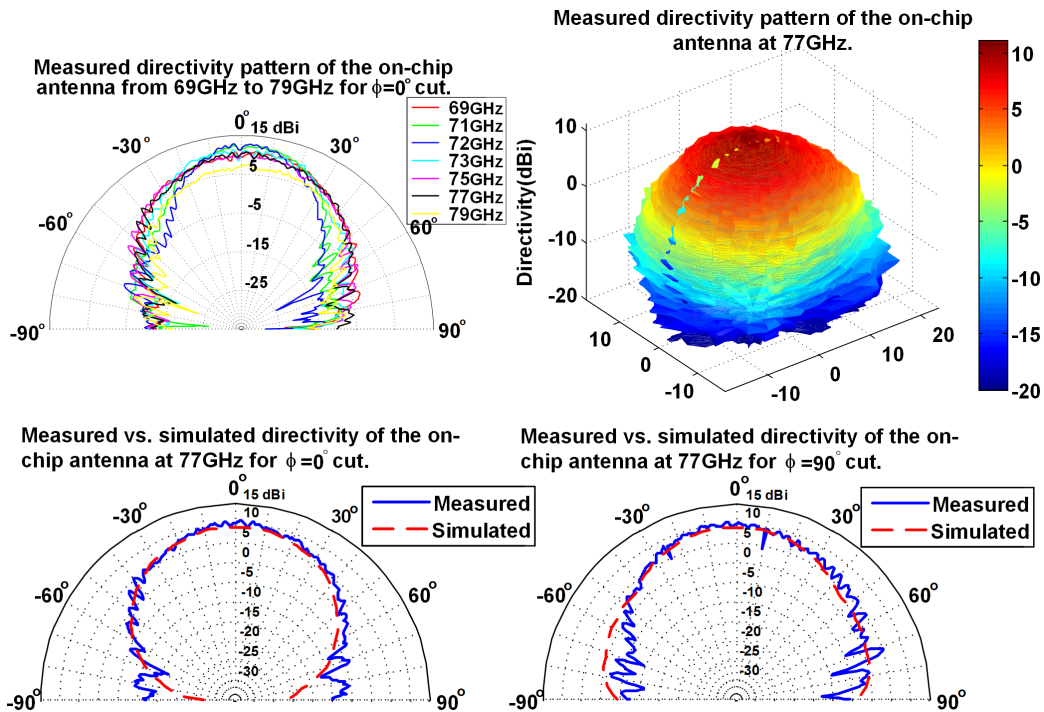


Figure 7.12: Measured pattern of the antenna from 69GHz to 79GHz. The full 3D pattern for 77GHz is shown on top right.

From the measured EIRP and directivity, total radiated power (TRP) can be also obtained using equation 7.14. The maximum measured TRP is 24.4dBm and gradually drops with increasing frequency to 20dBm at 77GHz. By using the simulated efficiency of the radiator, it is possible to calculate the power delivered by the PAs to the antennas. Calculation shows that all the PAs combined deliver over 27dBm of power to the antenna ports corresponding to a drain efficiency of 30.8%. Figure 7.13(c) shows the uniformity of the power delivered to the ports of the antennas. Due to edge effects, the slots at the end of the array experience a different impedance and accept lower power; nonetheless, the variation is small and around 20%.

The summary of the chip measurement results are provided in Table 7.1 where it is compared with other works on CMOS mm-Wave radiators.

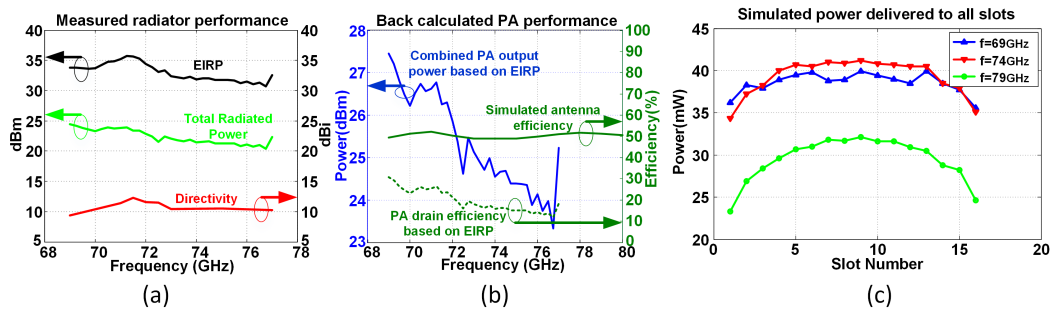


Figure 7.13: (a) Measured EIRP, Directivity and TRP of the radiator. (b) Simulated antenna efficiency and calculated total PA output power and its drain efficiency. (c) Simulated power delivered to each port of the radiator.

	This Work	[1]	[4]	[6]	[8]	[9]
Process	65nm CMOS	32nm SOI	180nm SiGe	45nm SOI	32nm SOI	65nm CMOS
Frequency(GHz)	69-79	134.5	108-114	53-63	58.3-60.5	88-99
EIRP(dBm)	35.7	6.0	24.5	33.1	17.1	35
On Chip Antenna	YES	YES	NO	YES	NO	NO
Radiator Directivity (dB)	12.2	7.1	17	6.9	32.5	36 (Dish Ant.)
Tot. Rad. Power (dBm)	24.4	-1.3	7.5	26.2	N/A	0
Antenna Efficiency	52%	39%	45%	74.5% (Uses High Res. Sub.)	N/A	N/A
PA P _{sat} (dBm)	27.4	N/A	11	27.9	N/A	N/A
PA Efficiency	30.8% (Drain Eff.)	N/A	N/A	23.4% (PAE)	N/A	N/A
Phase Noise (dBc/Hz)	-96.4@1MHz	N/A	N/A	N/A	-113 @10MHz	-85.6 @1MHz
Total DC Power(W)	PA+PLL/Distrib 1.81+0.55=2.36	0.17	3.4	N/A	0.23	0.6
Chip Area(mm ²)	2.9	1.2	39	10.5	9 (RX+TX)	4.32 (RX+TX)

Table 7.1: Comparison table of proposed radiator with state of the art designs.

WIRELESS POWER TRANSFER FROM SPACE

8.1 Introduction

Collecting solar power in space and transmitting it to the earth has been considered first by science fiction writer Isaac Asimov in a novel he published in a science fiction magazine in 1941 [26], and the first proposal for such a system goes back to 1968 [66]. The main advantage of placing the solar cells in the space is the increased reliability and continuous availability of solar energy in space. Unlike terrestrial solar plant, space based solar plants are not affected by weather or day and night cycles. The other advantage of placing the solar plant in space and beaming the energy toward earth is the ability to provide on-demand power to any point on earth. The high cost of deployment of such system which is mainly dominated by the high cost of numerous launches that is needed to place such a system into the earth's orbit, has been the main impediment in realization of such system [110].

Reducing the weight and volume of system as well as eliminating the need to assemble such system in space with the aid of humans or robots is necessary to make realization of such system possible. To do this the lightweight photovoltaic cells need to be integrated with RF microelectronic circuitry to create a high efficiency yet low mass solar energy to RF conversion.

8.2 General Proposed Concept

The design approach is a modular and flexible integrated solar power to RF power conversion unit that can be constructed with very lightweight materials and assembled into larger arrays that can be wrapped and packed inside a rocket. Figure 8.1 shows a simplified diagram of such a module or *tile*. A single tile utilizes small solar cells that combined with lightweight solar concentrators collect solar energy from a large area, an integrated RF generator that produces RF wave with well controlled frequency and phase, and an antenna that transmits the RF energy. The module is self contained and it can be repeated to collect solar power from a larger area and produce higher output RF power with more directivity. The tiles are fabricated on thin polyimide films and supported by carbon fiber frames which allows the structure to be flattened for packing and will be automatically unfolded and deployed. A module is a connected array of such tiles. Multiple modules can be combined to

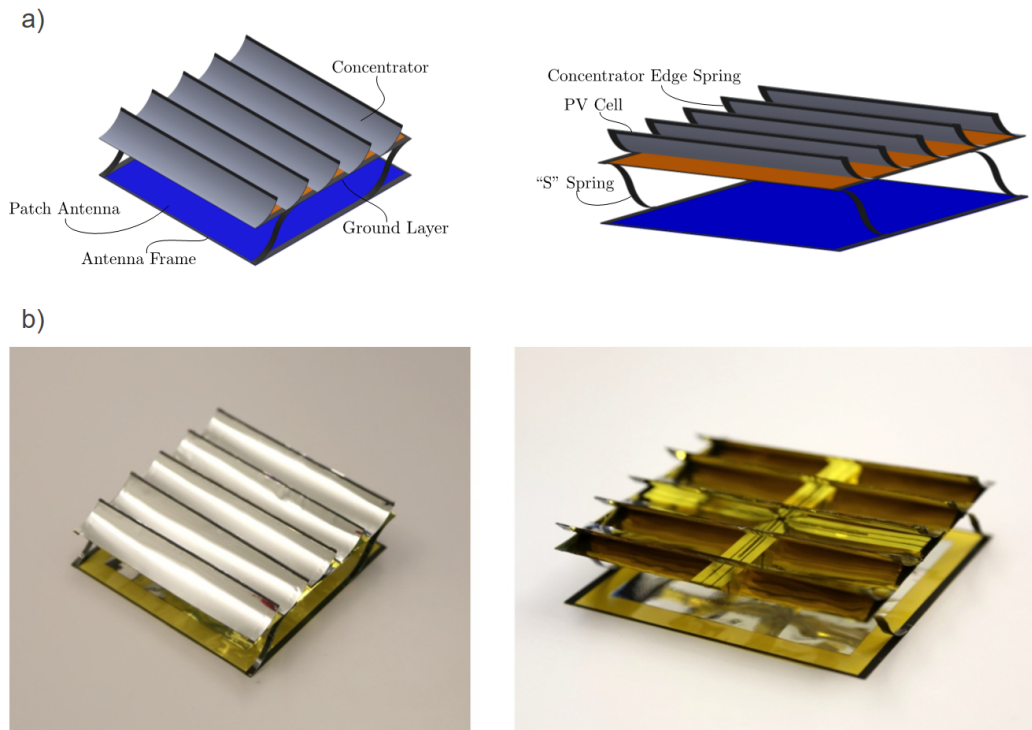


Figure 8.1: (a) Schematics of general modular tile architecture and (b) Fabricated mock-up prototypes.

produce arbitrarily large space based power station in space. Thruster will be used to adjust the position and attitude of the modules with respect to sun and each other. The RF power from each tile is frequency and phase synchronized and as a result the power station forms a massive phased array radiator that beams the RF energy to a small area on earth where the power is collected and converted to DC power. Figure 8.2 shows a conceptual drawing of the station in orbit.

The two key advantages that the modular approach provides are mass reduction and scalability. The integration of solar and RF energy conversion in one tile removes the mass associated with power distribution network while making the tile a self contained unit that can be repeated many times without major redesign of the RF/photovoltaics.

We now examine in detail the three specific areas of study where we have focused our efforts for design of our space based solar power array followed by additional discussion of more general and integrated system considerations.

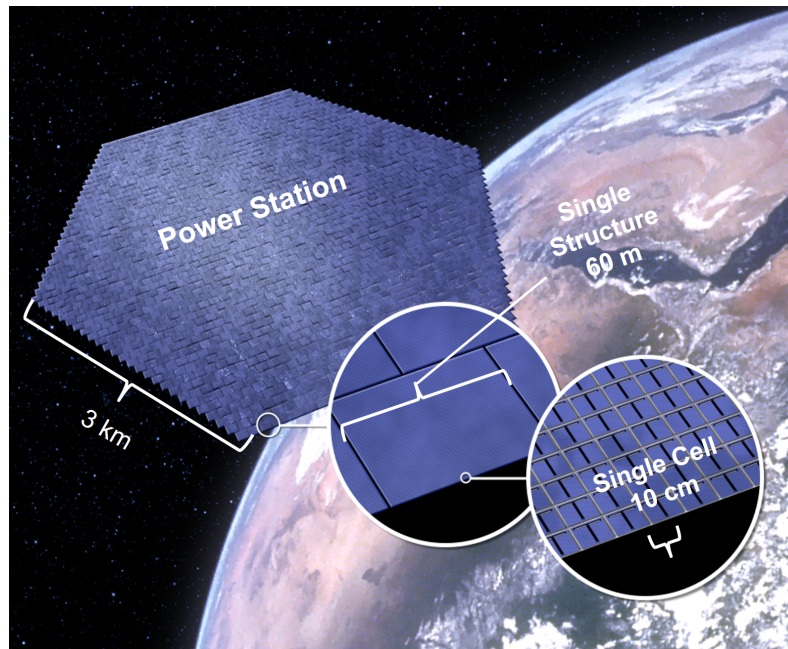


Figure 8.2: Conceptual drawing of the power station in orbit with detail inset showing the organizational hierarchy.

8.3 Photovoltaics

Specific Power and Conversion

The ratio of power to mass of solar cells is one of the most important factors in selection of space based solar cells. Most of space based solar cells employed recently are high efficiency and radiation tolerant multi-junction solar cells made of III-V semiconductor materials. These cells have typically power to mass ratio of around 180W/Kg individually and around 70W/Kg considering the weight of protective radiation shield and panel structure [93]. The cover glass used as the radiation shield constitutes a large fraction of total weight of space solar panels.

Optical Concentrators can be used to collect solar power from large area and focus it on a small photovoltaic material. This method has been used in terrestrial applications to reduce to cost of PV where the cost of panel is dominated by the high efficiency PV used. The higher the concentration factor is, the smaller the PV becomes, however, the cost of optical concentrator increases as higher fabrication tolerances are needed. The same concept can be used for solar application where light weight concentrators made from aluminum coated polyimide can be used to reduced the weight and hence the cost of the space based solar panel. The use of concentrators not only reduces the weight of solar cell used, but also it reduces the mass of radiation shield needed for the PV cell.

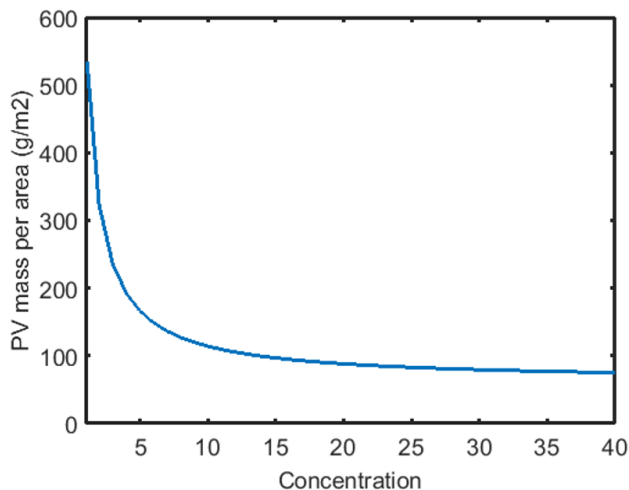


Figure 8.3: Areal density vs. concentration for PV + concentrator.

Figure 8.3 shows an approximate calculation of the areal density (g/m^2) of a typical photovoltaic with a Kapton based concentrator as a function of concentration factor. Here, the concentrator is a parabolic reflector made of a $10\ \mu\text{m}$ polyimide coated with $10\ \mu\text{m}$ layer of aluminum for reflectivity and thermal conduction. This calculation also assumes $75\ \mu\text{m}$ of ceria-doped coverglass covering the cell, $30\ \mu\text{m}$ of Cu metal at the rear of the solar cell, and $10\ \mu\text{m}$ of active GaAs solar cell material. It can be seen that even with modest concentration factors, the weight per tile is significantly reduced up to concentrations larger than 20-30 \times , due to the ratio of mass per area of the cells vs. reflectors. Studies show that optical concentration increases photovoltaic device efficiency [168], making concentration concepts even more attractive relative to flat plate photovoltaic designs.

Epitaxial Lift-off

It is possible to achieve very lightweight PV cells by thinning or removing the growth substrate of the semiconductor material. Due to direct band-gap structure of high efficiency III-V based solar cells, the active region of the cell is extremely thin and on the order of $10\ \mu\text{m}$, as a result the Ge based growth substrate of the semiconductor can be removed to achieve lower weight with no performance penalty. An epitaxial lift-off process (ELO) [172] has been developed that provides a fast and reliable method to achieve such thin solar cells. This process as shown in Fig. 8.4, not only reduces the weight of the solar cells by a factor of 15, but also makes the cells flexible and increases the cells efficiency due to photon recycling. The method also reduces the cost of the fabrication of III-V solar cells as it allows reuse of the growth

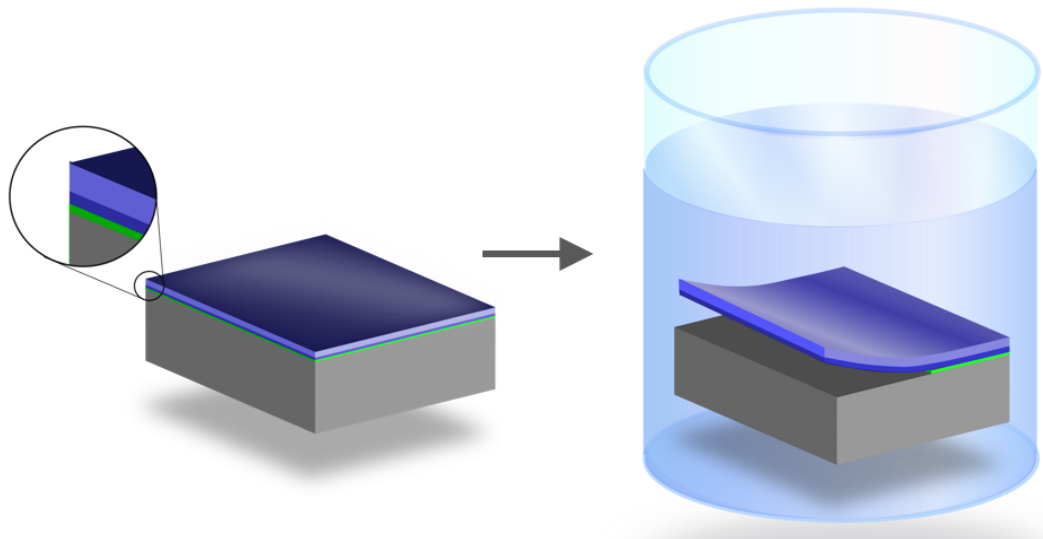


Figure 8.4: Schematic of the epitaxial liftoff process. The weight of the photovoltaic component can be further reduced by removing the inactive growth substrate from the device.

substrate [118].

Concentrator Optical Design

Our selected concentrator design is shown in Figure 8.5. The concentrating element is a one-dimensional half parabola reflector that focuses incident sunlight onto the back of the neighboring reflector, where the photovoltaics are located. In this application the half parabola has a few advantages over the more common full parabolic concentrator. Most importantly, it allows for the photovoltaics to be placed on a metallic, thermally conductive heat sink that provides for efficient heat extraction. This surface also acts as the solar reflector, reducing weight and structural complexity through its multifunctional design. Since only one side of the mirror needs to reflect incoming sunlight, the rear of the reflector can be coated with a custom material with high thermal emissivity, increasing the overall heat rejection and reducing the operating temperature of the photovoltaics. Additionally, the half-parabola can be stowed flat for launch and subsequently deployed more easily than a full parabola. The concentrator vanes are simply flattened when stowed and spring back to their designed shape upon deployment, as discussed with more detail in the Structures section.

The structural portion of the reflector is made of polyimide (e.g. Kapton) with a thickness of $5\text{-}25\mu\text{m}$. To increase heat rejection, a black polyimide can be used

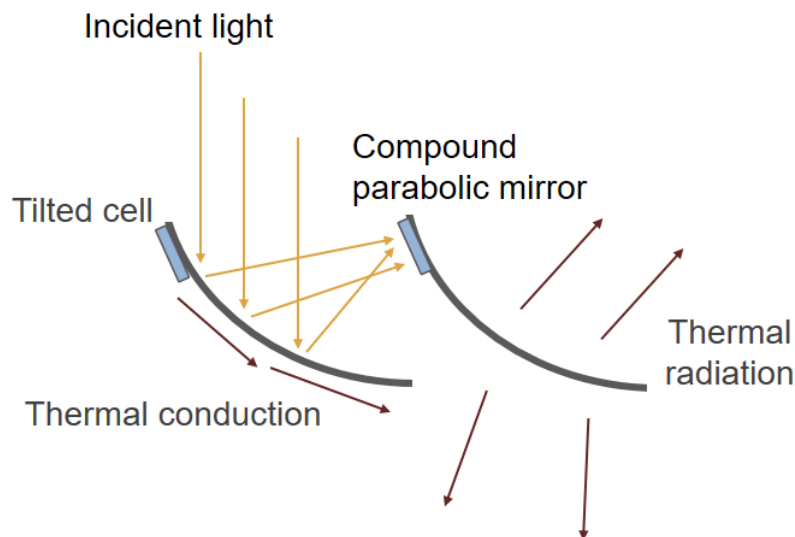


Figure 8.5: Schematic of parabolic half trough concentrator.

that has a high thermal emissivity (~ 0.88) at thicknesses of $25\mu\text{m}$ or less [58]. The sun-facing side of the reflector is coated with $1\text{-}10\mu\text{m}$ of Al for thermal conduction and topped with $\sim 100\text{nm}$ of Ag for efficient optical reflection. The reflectors will be held in place with the correct shape by custom carbon fiber springs, attached at various points and at the edges of the parabola.

To determine optical performance, we performed ray-tracing simulations as a function of incident angle along both optical axes for a $20\times$ parabolic half-trough concentrator, shown in Figure 8.6. In general, the angular tolerance along the concentrating axis will decrease as the concentration factor is increased for any type of optical concentrator [153], as is the case here (Figure 8.6(a)). The optical efficiency is always less than 1 even for a perfect geometry due several factors including metal absorption and rays that miss the target due to the ± 0.26 degree angular spread of the sun. The angular response for the parabolic half trough concentrator design is asymmetric around normal incidence, with relatively flat response in one of the directions. For a $20\times$ concentrator, the angular tolerance is $\sim 1.5\text{-}2$ degrees, within pointing accuracy capabilities of common small satellites [52]. Along the non-concentrating axis (Figure 8.6(b)) the angular tolerance is much higher, which could allow for tilting or slewing the satellite throughout orbit to balance RF transmission efficiency with solar collection efficiency (described in more detail below).

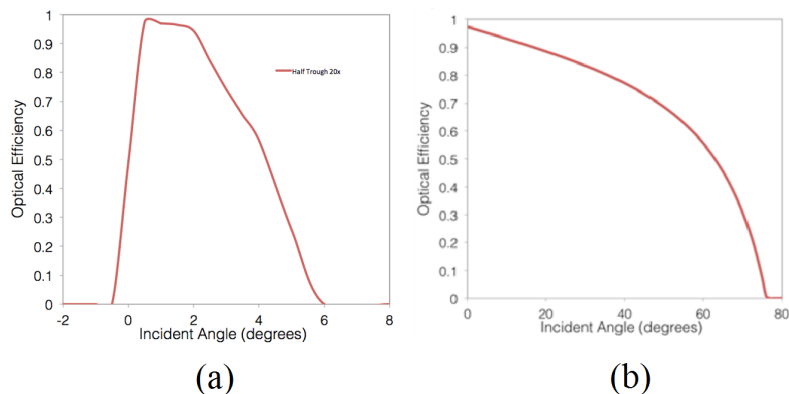


Figure 8.6: Simulated optical efficiency as a function of angle for 20 \times concentration along a) the concentrating axis and b) along the non-concentrating axis.

Concentrator Thermal Design

The lack of convection or external thermal conduction in space makes thermal management one of the most challenging aspects of space based concentrator photovoltaics. Using COMSOL Multiphysics, we have calculated steady state temperature profiles for numerous variations of our design under different degrees of concentration. An effective input heat load of 650 W/m² was used, calculated from the efficiency and bandgap of state of the art triple junction inverted metamorphic solar cells [178] with the assumption that we can prevent absorption of low energy photons to minimize thermal loads. We also account for expected absorption in the cover glass and in the Ag reflector. For this calculation, we also assumed a rear emissivity of 0.88 [58], front side emissivity of 0.5 (Ag coated with 4 microns of SiO₂ or Al₂O₃), and cover glass on the front surface of the photovoltaics (75 μ m Ce doped SiO₂, emissivity 0.88). Figure 8.7 shows the temperature at the location of the photovoltaic device for different concentration factors and a 20 μ m thick Al on the back side.

Typical single and dual junction solar cells prepared with epitaxial lift-off have been shown to have temperature coefficients as low as 0.1%/K [107, 152], all referenced to operation at 25 $^{\circ}$ C. To maintain sufficient efficiency and durability, the operating temperature of the photovoltaics should be kept below 100 $^{\circ}$ C, which is achievable for 20 μ m aluminum thicknesses as shown in Figure 8.7.

Performance Estimates

In order to estimate the overall efficiency of the photovoltaics component of our space based power system, we performed a more detailed calculation taking into account

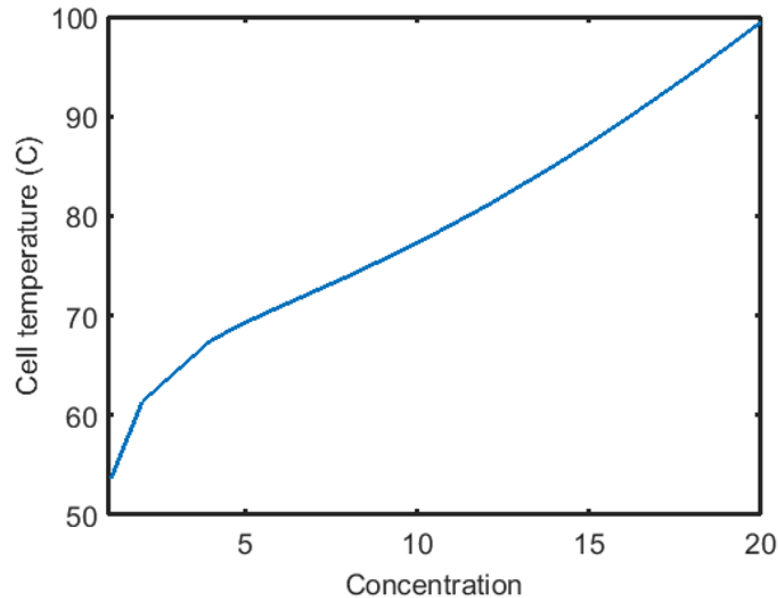


Figure 8.7: Thermal simulations for different concentration and $20\mu\text{m}$ aluminum heat spreader

several factors. First, we multiplied the optical efficiency obtained via ray tracing with the external quantum efficiency of a state of the art inverted metamorphic triple junction solar cell [178] and weighted it by the available photocurrent from the AM0 spectrum to determine the expected current density generation of each subcell in the concentrator system (Figure 8.8). The current limiting junction is the top cell, with a J_{sc} of 16.16 mA/cm^2 . Using this J_{sc} and values for open circuit voltage (3.04 V) and fill factor (84%) for this solar cell [178], we obtain an expected overall efficiency of 29.9% for the PV system (concentrator plus solar cell) under AM0 illumination. After taking into account thermal considerations, we expect an operating efficiency exceeding 25% over a temperature range of 100-115°C, using typical temperature coefficients of $\sim 0.05\text{-}0.1$ absolute $\%/^{\circ}\text{C}$.

PV Summary

In conclusion, we described the design and estimated efficiency of a parabolic half trough concentrator and photovoltaics for use in a space based power generating system. The parabolic half trough concentrator could potentially be flattened and extended during deployment. Optical ray tracing and numerical heat transfer calculations show that this design will allow the photovoltaics to operate at $\sim 25\text{-}30\%$ overall efficiency while maintaining reasonable operating temperatures under 100°C. The area mass density of this design is 98 g/m^2 , which corresponds to a spe-

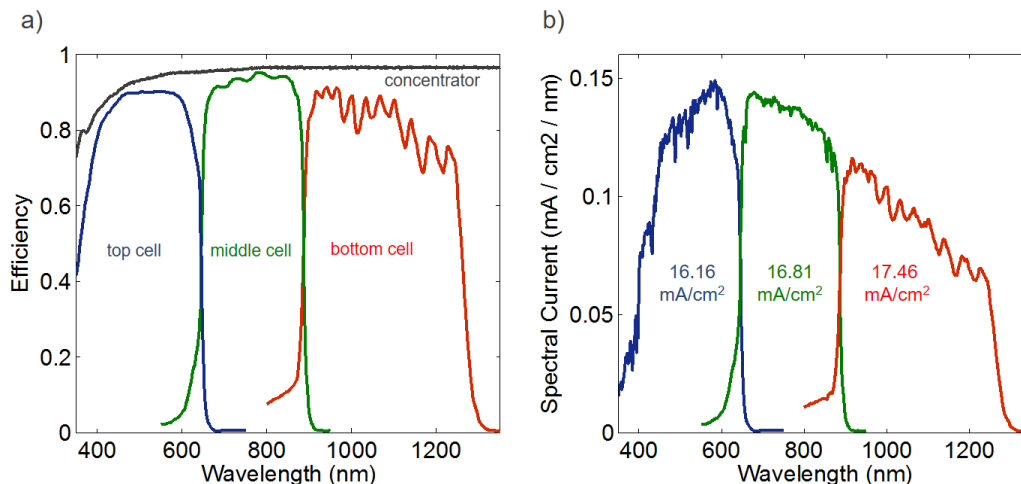


Figure 8.8: a) Optical efficiency as a function of wavelength for a 20x Ag Venetian blind concentrator (gray) and external quantum efficiencies for each junction of a common triple junction space solar cell. b) Expected spectral current generation for a triple junction solar cell in a 20x Venetian blind Ag concentrator under AM0 illumination.

cific power of 3.18 kW/kg at 20 suns when a 75 micron thick glass radiation shield is included. Future design iterations have the potential to reach specific powers as high as 10kW/kg.

8.4 Microwave Power Generation and Control

Introduction and Enabling Technology

Using a large number of electronic microwave power transmitters operating with well-controlled, synchronous phase and possibly amplitude allows forming a beam that focuses to a spot on the surface of the earth. The operation of such an array is analogous to the operation of a lens. In contrast to a lens used for focusing a beam of light, the delay of the electromagnetic radiation (or the phase for an otherwise slowly changing beam) can be electronically controlled, such that the emitting surface has a geometry that is by one degree independent of the desired phase- and delay offsets as well as allowing the beam to be electronically steered.

In comparison to traditional arrays that generate the power centrally and phase shift it locally (e.g. compare discussion in [73]), generating and controlling the microwave power emission locally has several advantages, among them that no global DC or RF power routing is required and small local power density even with a large amount of total output power produced,. This in turn helps with thermal management as well as reducing DC and RF power losses. This non-traditional mode of operation

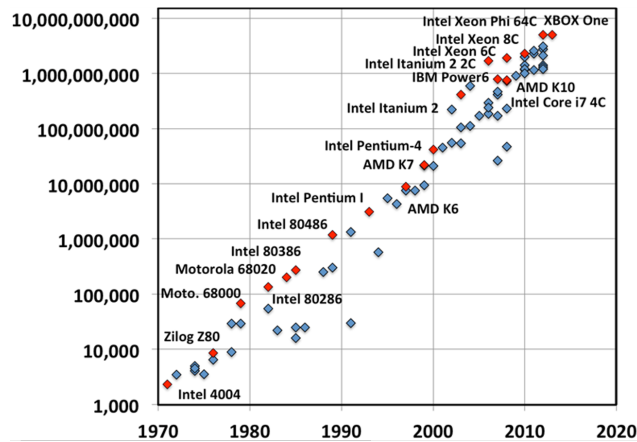


Figure 8.9: Transistor count of commercial CPUs by year [166]

is supported by the availability of modern integrated circuit process nodes that allow economic fabrication of hundreds of millions of highly-integrated circuits that include both the RF circuits to generate and control the microwave power locally as well as the digital processing power as predicted by Moore's Law (Figure 8.9[166]).

With continuing advancements made in Silicon and CMOS process technologies driven largely by the continuing need for increasing computing power, traditional approaches based on III-V technologies have, therefore, increasingly incorporated or been replaced by silicon-based technologies (e.g. [73, 123]). When silicon-based technologies are incorporated, they are frequently used for back-end operations such as digital control, pre-power signal generation and receiver functionality, while transmit-receive (T/R) switches, power amplifiers (PAs) and low-noise amplifiers (LNAs) are implemented in III-V technologies in a multi-chip system solution (e.g. [137]). Because of system requirements unique to wireless power transfer from space as well as continuing CMOS technology improvements, we are targeting a fully integrated, single system-on-chip (SoC) solution to reduce cost and weight as will be detailed in later sections. Finally, as will be discussed later, performance of CMOS circuits and systems operating in an environment with ionizing radiation uniquely benefit from continuing technology scaling, compared to any other processes [109]. This also presents a strong argument for integrating all electronic functionality in one technology and SoC.

Choice of Operating Frequency

The operating frequency of the system significantly impacts the performance, size, and cost of the system in many ways. In this section, we will discuss the most important aspects.

Everything being equal, the frequency of operation most directly affects the achievable spot size of the focused beam on Earth. Assuming an overall system efficiency, η_{sys} , the diameter d of a disc-shaped system in space is $d = \sqrt{\frac{4P}{\pi I \eta_{sys}}}$, where P is the power to be available on Earth and I is the intensity of the solar radiation (1.36kW/m²). Thus, assuming $\eta_{sys}=15\%$, a disc with a diameter of 2.5km is required to collect 1GW of power on Earth. For an aperture of this size, the far-field, or Fraunhofer Region, begins for distances [Balanis] of $R > \frac{2d^2}{\lambda}$, where λ is the wavelength of the radiation. At 1GHz and 36,000km distance, this aperture would be a disc of 2.32km diameter, and the distance to the first diffraction minimum on the ground would be approximately given by $1.22 \frac{R\lambda}{d}$ or 5.6km, in which 84% of the total radiated power will be located. At 10GHz, a circular aperture in space of 740m marks the beginning of far-field operation, with a first diffraction minimum at a distance of 1.8km on the ground. In other words, the product of ground station size and space station size scales linearly with wavelength. Above 10GHz, atmospheric absorption due to water vapor around 22.2GHz can become relevant at higher precipitable water vapor levels [112]. In addition, spatial and temporal control of the individual tiles becomes increasingly more difficult at higher operation frequencies due to increased electronic phasing errors for constant timing and location errors. We note that Friis transmission equation, frequently used to estimate power transfer efficiencies, is inapplicable here, because of operation close to or at near-field conditions. For example, Friis equation can be expressed as:

$$\frac{P_r}{P_t} = \frac{A_r A_t}{\lambda^2 R^2} \quad (8.1)$$

assuming 100% efficient antennas, where A_r and A_t are the transmit and receive apertures, R is the distance and λ the wavelength, which, for our 10GHz example yields an overly optimistic ratio of 93.8% of received power to transmitted power.

Peak intensity at the center of the spot is related to the total power P_0 , the aperture A and the distance R by e.g. $\frac{P_0 A_t}{\lambda^2 R^2}$. Thus, in our examples, the peak power intensity would be around 42W/m² assuming 20% system efficiency. The density falls off to 50% and 25% of its peak value at 42% and 58% of the way to the first minimum, respectively. The peak power density at the first side-lobe is <2% the peak density of

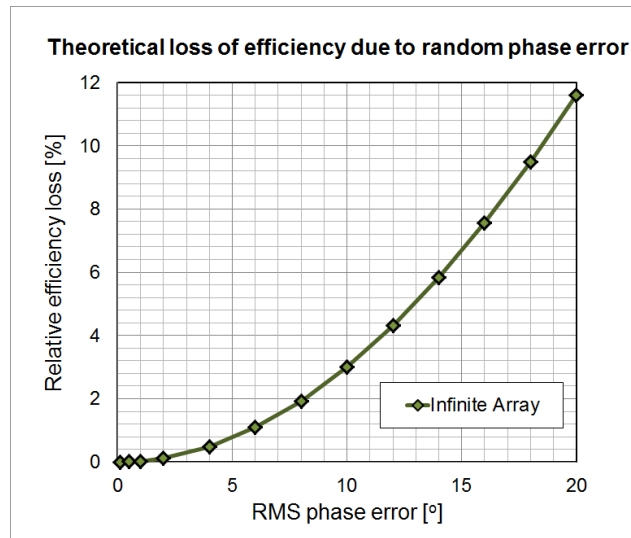


Figure 8.10: Theoretical loss of RF power in main lobe due to random phase errors.

the main lobe or $<1\text{W}/\text{m}^2$. Increasing the aperture in space collects proportionally more power, in addition to resulting in higher peak power concentrations, mitigated though by spreading of power compared to the theoretical Airy pattern due to near-field effects. The formation of a concentrated spot on the ground relies on the ability to accurately control the phases of the radiating elements. For random, uniformly distributed phase errors with a maximum excursion of $\pm\delta_{max}$ the efficiency compared to a perfect phase distribution is given by [30] $\text{sin}^2(\delta_{max})$ in the limit of an infinitely sized array. For normally distributed phase errors, we can calculate an equivalent $\delta_{max} = 3\delta_{rms}$ from the RMS error with incurring a minimal error at small phase offsets. This is plotted in Figure 8.10. Thus, even at 10 degrees RMS phase error, we still retain 97% efficiency. This is supported by independently run MATLAB[®] simulations.

Random phase errors occur due to electronic noise and incomplete knowledge and control of the physical shape of the system. Total jitter of electronic inverters/buffers is a function of total power used as well as the process technology used (with faster technologies yielding less jitter for a given amount of power consumption). Control of the physical shape is a function of the accuracy of the shape information available and the speed with which the electronics can react to changes in shape. Since changes due to vibrations are much slower than the operation speed of the electronics, measurement accuracy of shape error is the limiting factor for maintaining correct phasing. Shape determination with an RMS error of 1mm (in the direction to the ground receiver) corresponds to 12° RMS error at 10GHz and 95.7% efficiency.

One of the key consequences of our local and modular approach is that DC power generated locally will mostly be consumed and converted to RF power locally. Since insolation is constant in space, the amount of available solar power is constant per unit area of the satellite. Assuming half-wavelength antenna spacing, the absolute antenna size and spacing is determined by the choice of operation frequency, and the amount of DC power per antenna element is a strong function of the frequency of operation chosen and the efficiency of the photovoltaics (PV).

As the insolation in space is fixed, and assuming $\lambda/2$ spacing, the power per antenna is given by $\eta I \left(\frac{\lambda}{2}\right)^2$ where I is the insolation ($\sim 1.36 \text{ kW/m}^2$), η is the combined PV and DC-to-RF efficiency and λ is the RF wavelength. The nominal output power per RF amplifier is half of that amount if we generate two polarizations independently. Thus, while at 1GHz and 20% overall efficiency the nominal output power is, thus, 3W per amplifier, this amount will drop to 30mW at 10GHz, power levels that are readily obtainable even in low-voltage, advanced CMOS technology nodes. For an antenna impedance of 50Ohm, a peak voltage of $V_{pk}=1\text{V}$ allows us to generate 10mW or 40mW for peak voltages of 2V (e.g. if we use cascoded transistors). We can define a power-enhancement ratio (PER) that is the ratio of the required power to the power generated over an easily realizable impedance (e.g. 50Ω) assuming peak voltage limited operation. Using passive components, it can be shown [21] that the efficiency using n sections of passive, impedance transforming networks using inductors and capacitors is given by:

$$\left(1 - \frac{\sqrt{\sqrt[n]{PER} - 1}}{Q}\right)^n \quad (8.2)$$

where Q is the quality factor of the inductors (assuming capacitors have much higher Q , a reasonable assumption). Thus, with a PER of 300, and a Q of 15, we would lose 40% of the RF energy in passive impedance-transformation networks for $n=4$, the optimal number of sections. This loss of RF energy due to higher required power-enhancement ratios counteracts the higher active efficiency at lower operating frequencies. Simulated overall efficiencies taking these effects into account for $Q=20$ and $Q=50$ are shown in Fig. 8.11 for a representative 65nm CMOS process node.

At lower RF frequencies and higher power levels, an option would be to use separate power amplifier device technologies such as GaAs, InP or GaN based processes that can tolerate higher peak voltages and would thus require lower PERs. However, this would create significant overhead with regards to signal routing and on-off-

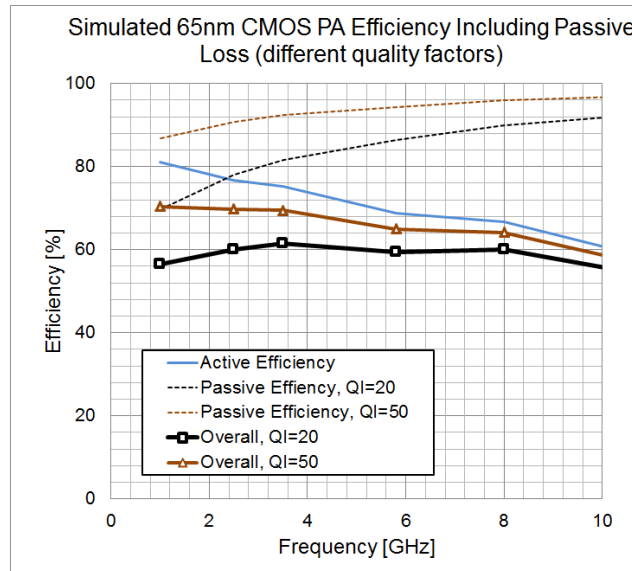


Figure 8.11: Simulated active only, passive only and overall PA efficiency over frequency for required output power levels and power enhancement ratios.

chip transitions, in addition to increased cost. Because power requirements even at 1GHz are within the limit of what can be achieved in CMOS technologies for power amplification [20], a single CMOS SoC promises to be the lowest-cost, lowest weight solution.

DC to RF Power Conversion in CMOS

The core realization of DC to RF power conversion happens in an RF power amplifier. As a result, efficient power amplifiers are highly desirable for such task. Since linearity of amplification is not a concern in wireless power transmission, efficient switching power amplifiers such as class E [94, 116], class F [99] or related classes of amplifiers can be used. Choosing the right technology to realize the power amplifier is based on targeted efficiency, frequency of operation, RF power generated per phased array element, cost, reliability and radiation hardness. While traditionally integrated power amplifiers have been realized with III-V technologies such as GaAs or InP due to their larger band-gap and hence higher breakdown and output voltages, relatively recent innovations in integrated power combining topologies such as distributed active transformer (DAT) [20–22] have allowed medium power (hundreds of milliwatts to several watts) PAs with lower voltage CMOS devices with comparable power added efficiencies (PAE). MOSFETs which are mainly used as digital switches in CMOS logic circuits can be readily used as switches in switching power amplifiers. The continuous reduction of feature sizes in CMOS technology

has resulted in very fast transistors which can switch over a hundred billion times a second which is the result of reduction of parasitic capacitances while keeping their switch resistance almost constant. The reduction of transistors maximum voltage handling has resulted in lower RF power generation per device; however, due to distributed nature of the proposed solar power generation, each element does not need to provide high power levels and hence CMOS based power amplifiers [35] can be easily integrated along with the timing generation circuitry and controlling logic in a single chip, minimizing cost and complexity of the design while increasing the robustness of RF power generation circuitry.

Timing and Phase Control

To generate a phase-coherent microwave spot on the ground, phase coherence of the transmitters needs to be maintained within approximately 10° RMS at the microwave frequency across the array as discussed above. This coherence requirement needs to be maintained for the tiles in space, but does not apply to systematic offsets relative to the ground receiver (the mean distance of the entire system), as any systematic error in the mean distance to the space system appears as a phase offset common to all transmitters in space. An error in the other two position coordinates (elevation and azimuth) can shift the spot on the ground equal to said error, but errors on the order of meters (as achieved by GPS, for example) are insignificant compared to the spot size of the microwave beam on earth.

From this observation and noting that computational power can be made available locally on the tile level (e.g. via an integrated microcontroller or processor), a hierarchical reference distribution and phase correction scheme offers itself as a solution Fig. 8.12. In this scheme, the position of the modules relative to one another or central modules can be determined by triangulation, through the use of wirelessly transmitted reference signals (shown as module-to-module communication) and absolute clocks (comparable to the operation of global-positioning system, but for shorter distances and hence much improved accuracy). Within a module, a reference signal (red arrow) is distributed to each tile between nearest neighbors, while the motion of the tile, e.g. due to rotation or vibrations is tracked and the information is broadcast (blue arrows) from the module center to the tiles. Finally, general communication between each tile and the module control unit (center) can also be locally routed from tile to tile (green arrows). With locally available processing power on each tile, continuous correction to the arriving reference phase can be computed, predicted, and applied on the tile level. The amount of data that needs

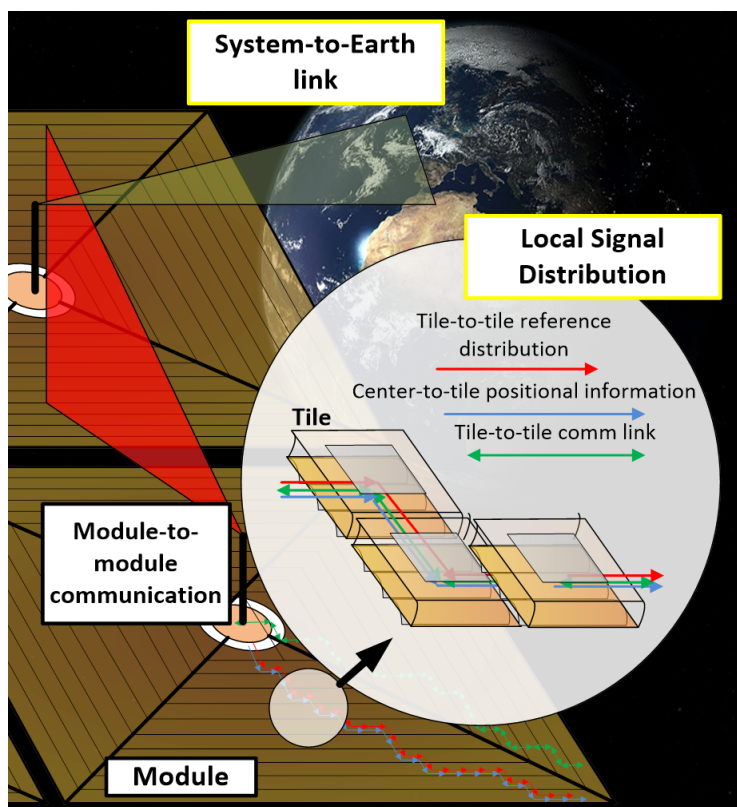


Figure 8.12: Hierarchical signal and reference distribution.

to be broadcast across the module is relatively limited due to the limited number of degrees of freedom as well as the limited number of important vibrational modes.

Since the reference phase itself needs to be distributed from a central location in the module to a million tiles or more and, hence, some form of intermediate buffering is necessary. With a module layout utilizing a tile-to-tile distribution, and a module width of W , the reference signal will be buffered on average $N=W/\lambda$ times, and the average jitter is given by:

$$J = J_0 \sqrt{\frac{1}{N} \sum_{i=1}^N i} = J_0 \sqrt{\frac{N+1}{2}} \approx J_0 \sqrt{\frac{W}{\lambda}} \quad (8.3)$$

where J_0 is the jitter of an individual amplifier. If we allow the jitter contribution of the reference distribution chain to be half of the total allowable contribution, the average jitter would be 1.5ps and hence for an individual reference buffer jitter of 47fs within the reference signal bandwidth of interest (i.e. approximately the loop bandwidth of the on-chip phase-locked loop) and a module width of 30m, which is obtainable even for reasonable power consumption. This can be further improved

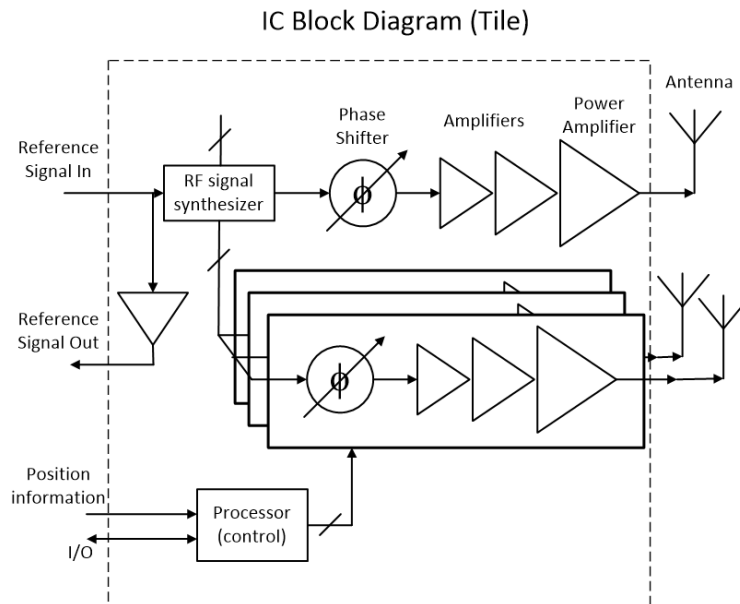


Figure 8.13: Simplified block diagram of RF integrated tile electronics. The reference signal is used to locally generate an RF signal and can be locally buffered for redistribution.

by schemes that use fewer distribution steps, i.e. employing a more hierarchically organized distribution approach.

Shown in Fig. 8.13 is a simplified block diagram of the functionality within each tile of the integrated circuit system. Assuming a PV efficiency of 30%, the available DC power per antenna is 90mW at 10GHz. Using the figure-of-merit (FOM) calculations in [169] as a benchmark for a FOM of -235dBc/Hz, 1mW of power consumption results in RMS jitter 1.8ps RMS, an acceptable number at 10GHz without undue power overhead. Microcontrollers running on several mW of power consumption with CoreMark™ [129] scores exceeding 100 are commercially available and would provide more than sufficient computing power for operational control.

8.5 Antenna Design

During the operation of the system, electromagnetic microwave power should be radiated in a beam in only one hemisphere to avoid excessive microwave power loss. This requires either the use of one or more reflecting ground planes such that radiation can physically only occur into one hemisphere or, alternatively, a 3-dimensional arrangement that actively or passively controls radiation to be (preferably) into one hemisphere. Using the third physical dimension to control the hemispherical direction of radiation, however, has the disadvantage that deployment may be complicated

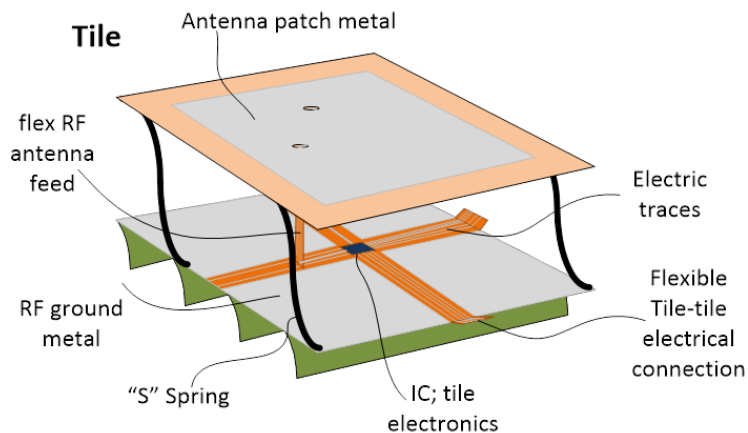


Figure 8.14: Tile structure (not shown to scale) showing patch antenna metal and ground layer, location of integrated circuit and electrical connections

due to the additional layers required, but may be a design alternative under some employment scenarios.

Patch antennas with their low form-factor, their integrated ground-plane and their ability to provide reasonable impedance, are, thus, a natural candidate. To save mass, the vacuum of space is chosen as the dielectric medium between the ground plane and the patch. This leads to a geometry shown in Fig. 8.14.

Providing two feeds to the patch antennas allows the generation of both horizontally and vertically polarized fields. Since the phase between the polarization can also be controlled, circular polarization can also be achieved assuming that no amplitude control is applied. Because the permittivity and permeability of vacuum is one, classical design formulas (e.g. [134]) would indicate a patch width of close to half a wavelength, similar to the spacing preferable for the antennas in the arrays themselves (to avoid additional grating lobes). The element antennas can be sized somewhat smaller, however, since the presence of the adjacent array antennas naturally tunes the array to the half wave-length spacing (compare simulation results). Furthermore, the spacing requirement of half a wavelength can be slightly relaxed since grating side-lobes will be small for relatively shallow steering angles (i.e. those preferably used for the system).

Losses in patch antennas originate from one of three sources [31]: conductor losses, dielectric losses, and excitation of surface modes. Because $\epsilon_r=1$, the cut-off frequency for the the TE and TM surface modes given by [133],

$$f_c = \frac{nc}{\sqrt{\epsilon_r - 1}} \quad (8.4)$$

Ripple height	Simulated Efficiency	Impedance [Ω]
0	95.8%	135+59j
$\lambda/60$ – horizontal	95.8%	141+61j
$\lambda/40$ – horizontal	96.1%	142+61j
$\lambda/33$ – horizontal	95.6%	146+62j
$\lambda/60$ – vertical	95.6%	141+61j
$\lambda/40$ – vertical	95.9%	144+61j
$\lambda/33$ – vertical	95.8%	146+62j

Table 8.1: Impact of ripples in support structure on antenna performance.

where c is the speed of light, n is the mode number (e.g. $TM_0, TE_1, TM_1, \dots, TE_n, TM_n$ for grounded dielectric substrate), d is the distance between the patch and the ground and $\epsilon_r=1$ is the permittivity of vacuum. Therefore, the only substrate “mode” that can propagate is the TM_0 mode which corresponds to sideways radiation. Dielectric losses are not present, and, hence, the only antenna losses are due to electric losses, potentially allowing high antenna efficiency.

To assess the effect of unevenness in the thin-film material, full electromagnetic simulations of an infinite patch antenna array with triangularly shaped ripples of various sizes were performed using ANSYS High-Frequency Structure Simulator (HFSS). The results are listed in Table 8.1. The patch-to-ground height spacing is $\lambda/15$, and results are similar for both linear polarizations (with regards to orientation, denoted as “horizontal” and “vertical”) and results are within the tolerance of the simulation.

Heat Dissipation

Conversion losses in the DC-to-RF conversion process manifests itself as generated heat, and has to be dissipated to the environment. The heat generated by the electronics in the tile due to RF converter losses is

$$P_{diss} = I \cdot A_{tile} \cdot \eta_{PV} \cdot (1 - \eta_{RF}) \quad (8.5)$$

where I is the solar irradiance, A_{tile} is the tile surface area, η_{PV} is the PV conversion efficiency and η_{RF} is the DC-RF conversion efficiency. In order to decouple potential issues with RF-IC heat dissipation from other parts of the system a simplified model was examined, in which a source of heat, modeling the IC, heats a thin aluminum sheet on a thin, gray body material, modeling the polyimide structural material. The aluminum sheet conducts heat away, and the gray body. A background temperature

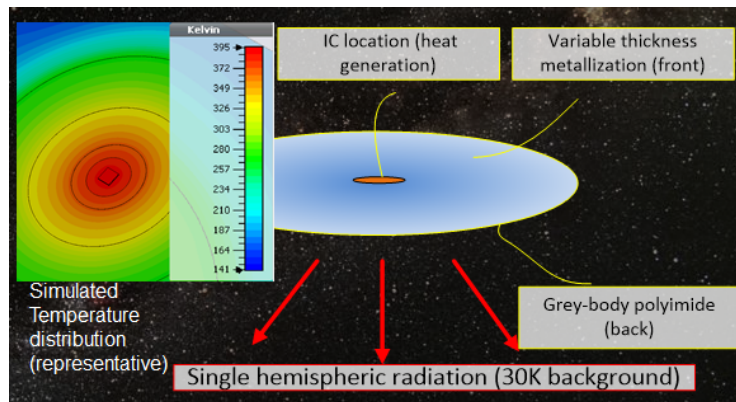


Figure 8.15: Simulation setup for simulating the temperature rise of the integrated circuit in the tile.

of 30K is assumed. Radiation occurs into one hemisphere effectively assuming that the PV side is blocked from effectively radiating heat. The problem setup constrains the tile size and the total amount of metal per tile. The metal thickness decreases monotonically from the center of the tile at the location of the integrated to the sides. The simulation setup is shown in Fig. 8.15. For simplicity, radial symmetry was assumed in all simulations.

Three metalization profile scenarios were considered: the first profile has quadratically increasing metalization thickness from a thickness of zero at the tile edge (“zero edge thickness”). The second profile keeps the total metal volume constant underneath any constant width annulus around the center (“equal volume”). For the third profile, a Nelder-Mead optimization is run to select the heights of five different plateaus around the center. The thickness z in mm versus the distance x from the center in mm is shown in Fig. 8.16 for all three profiles. In all scenarios, the total volume (mass) of metal used is held constant at the volume occupied by a constant thickness metalization of $5\mu\text{m}$ (50mm^3).

Fig. 8.17 shows the simulated IC temperature for these three profile assumptions for 2W and 0.5W per IC, equivalent to operation at 1GHz and 2GHz (taking into account the reduced tile area). As expected, temperature decreases as the sources of heat are more evenly distributed over the available area (corresponding to more sources producing less heat, equivalent to operation at higher RF frequencies). The Nelder-Mead optimized profile is the most efficient metalization profile of the three profiles investigated.

Shown in Fig. 8.18 is the effect of doubling and halving the total amount of metal

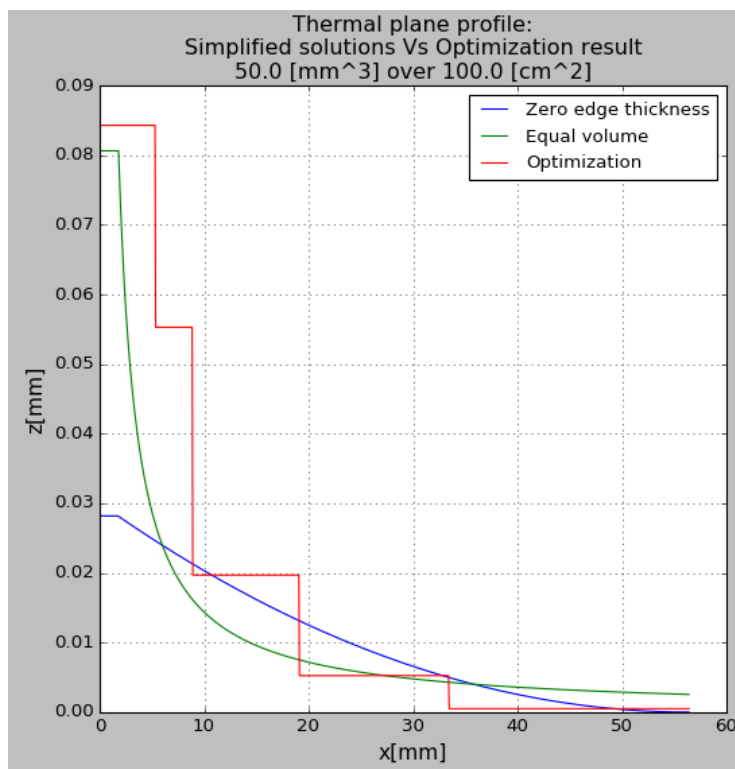


Figure 8.16: Metallization thickness profiles from center (IC location) to edge of tile for a nominal metallization of $5\mu\text{m}$ Al equivalent.

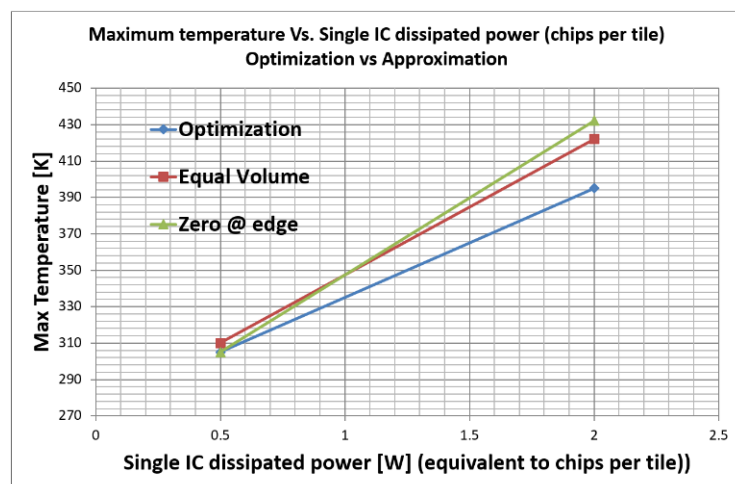


Figure 8.17: Simulated IC temperature for three metalization profiles using a total Al volume of 50mm^3

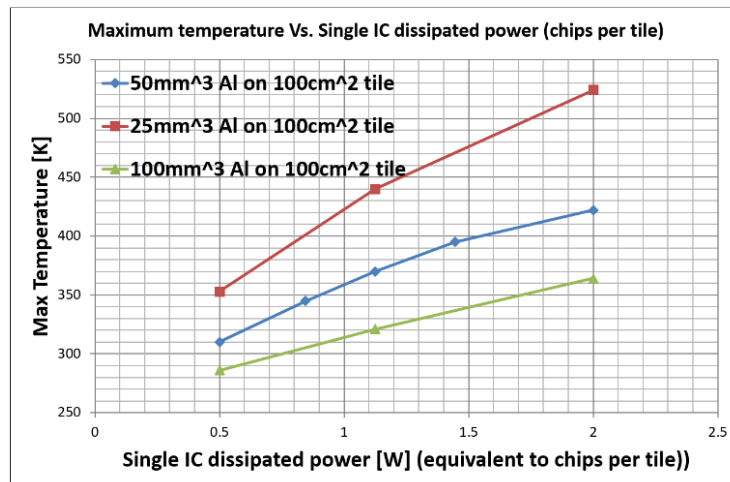


Figure 8.18: Effect of Aluminum thickness on the IC's temperature.

used, again as a function of amount of heat per source (IC). The simulations are based on uniform distribution of Al (which is not the most optimum method). Compared to constant thickness metalizations, the IC temperature is reduced by hundreds of degrees Kelvin in all scenarios and acceptable under various metalization and power dissipation scenarios.

Radiation Effects

Tolerating the harsh radiation environment in space and ensuring acceptable system lifetime poses additional challenges compared to ground-based designs. For system-lifetimes of 10yrs, total ionization doses measured in Mrad may have to be absorbed and tolerated by the electronics even if noticeable radiation shielding is used (compare discussion in section V, subsection D). In addition, designs need to tolerate and correct for single-event effects such as corruption of random-access memory data due to, for example, a cosmic-ray strike. An additional challenge to designing for radiation tolerant systems using integrated circuit processes is the observed variability in achieved tolerance within the same lot or even on the same wafer [43].

Compared to other technologies, modern small-feature size CMOS technology nodes have shown to be more capable of handling stress due to ionizing radiation, as well as to have more promise to benefit from technology scaling compared to bipolar and III-V processes[6]. Measurements of aging in the presence of radiation have shown that the change in threshold voltage gets smaller as the feature size of the technology reduces[26]. This can be attributed to the fact that advanced node

technologies have much lower gate oxide thickness which reduces the probability of a radiation generated electron get trapped in the oxide and change the threshold voltage [109]. Also the oxide thickness in many advanced technologies is so thin that the electrons can tunnel through and produce a leakage current. While this effect is an undesired phenomena in digital circuit design as it introduces static power dissipation, tunneling of electrons increases the tolerance of the MOSFETs to radiation as the electrons inserted in the gate oxide do not stay trapped for long time, and as a result after the radiation event the threshold voltage recovers.

Thus, for deep-submicron CMOS processes, the total ionization dose (TID) affects thick-oxide interfaces (e.g. field-oxide or shallow-trench isolation) more strongly than gate oxides due to the larger oxide thicknesses. These effects, however, can be greatly mitigated by choosing custom layout techniques with enclosed transistors and closed gate structures to prevent increased leakage currents and hence power consumption over time in radiative environments [70, 154], in addition to periodic thermal annealing [54, 72]. Using these techniques, analog integrated circuits capable of withstanding tens of Mrad TID can be implemented in commercial CMOS processes.

Finally, single-event effects in CMOS circuits, while not causing long-term damage, affect the operation of digital circuits by corrupting digital information. As with the analog portion of the circuits, design and layout techniques for memory cells [42] as well as integrating redundancy and error-correction methods into the ASIC design flow (e.g.[119]) can mitigate these effects and result in greatly improved robustness in operation. Due to the large number of circuits in the space-based system, the (temporary) failure of any individual tile has an insignificant effect on overall performance, and periodic global status monitoring can detect local, non-destructive faults and correct them (e.g. via a reboot).

8.6 Structures and Deployment

The structural design follows the general theme of modular design with repeatable units that can be assembled in different stages to form larger structures. In addition to being modular, the structure is required to be ultra-light, thin, foldable and deployable so that a large number of them can be launched simultaneously, thereby minimizing the launch costs. The design is based on a rich history of research in the field of deployable membrane-like structures and origami-inspired folding patterns for space structures. In this section, we begin by discussing the structural

design concept for a tile, followed by discussion of other elements leading up to the structural architecture of a single spacecraft (a module).

Tile Structural Concept

The tile structure must be lightweight, must maintain positional accuracy of the various components, and must be able to be flattened for packaging and pop into its operational state when deployed. Here we describe the structural design of four tile components: the concentrators, the support layer, the patch antenna, and the antenna standoff springs.

As shown in Figure 8.1, the concentrator consists of a thin, metalized polymer film supported by a carbon fiber reinforced plastic (CFRP) frame. The frame consists of edge springs that have the appropriate parabolic profile. Additional springs with identical profiles may be included along the length of the concentrator. At the top edge is a thin CFRP membrane that maintains straightness. Each concentrator is able to flatten through the elastic deformation of the parabolic springs to a flat state.

The support layer consists of a thin polymer film supported at the edges by a square CFRP frame. The patch antenna is similar in design.

The patch antenna is held below the ground layer by four CFRP springs that have an “S” profile. These springs can flatten such that the patch antenna plane rests directly below the support layer; once deployed, they provide the necessary separation between the patch antenna and the ground plane.

Module Structural Architecture

As shown in Figure 8.19, the tiles are arranged together in strips. Several CFRP battens connect the tiles to two edge longerons. These longerons run the entire length of a strip and support its edges. These CFRP longerons provide out-of-plane bending stiffness to the strips. To enable the spacecraft packaging scheme, these longerons must be able to be flattened and rolled [86]. As such, the longerons have a cross-section similar to a Triangular Rollable and Collapsible (TRAC) boom [32]. All strips have the same width, but may have different lengths.

The strips are arranged in concentric squares, as shown in Figure 8.20. They are connected at either end to diagonal cords. At one end, the diagonal cords are attached to a central hub, and at the other end, the diagonal cords are connected to tips of deployable booms (e.g. the Northrop Grumman AstroMast [63] or the ATK coilable booms [120]). The booms, clamped to the hub at the center, are

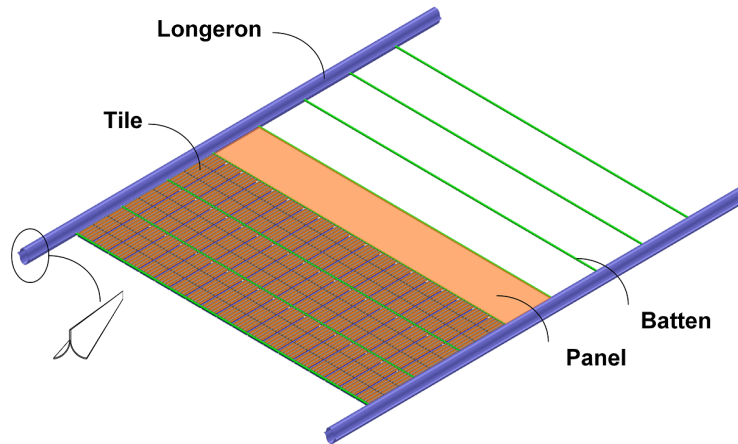


Figure 8.19: A short segment of a single strip. The longeron has a cross-section similar to a TRAC boom. For clarity, some of the tiles have been omitted.

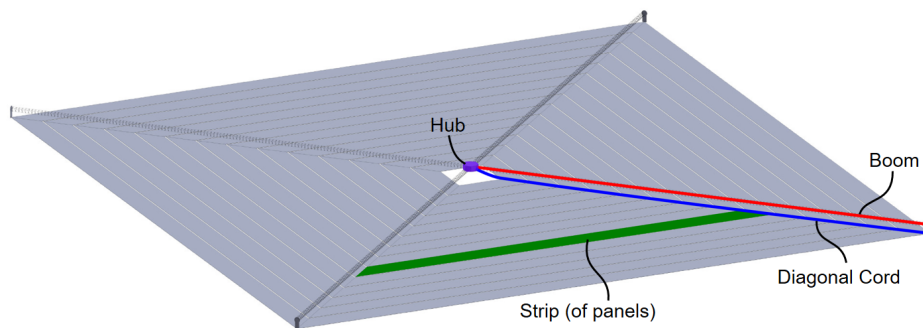


Figure 8.20: Spacecraft structural architecture.

located along the diagonals of the squares. These booms provide the motive action during deployment. After deployment, the diagonal cords are tensioned, and the cord tension is reacted by the booms. Each strip is connected to its neighboring strips using ligaments, which are short tension lines. These ligaments allow for the transmission of tension between strips, and they implement the slipping folds crucial to the module packaging scheme.

Module Structural Design and Performance

A simple numerical structural model of this architecture was implemented. Taking a loading case and a performance metric described below, the individual structural elements were designed through an optimization procedure.

Expected sources of dynamic loading are attitude control forces and torques, and vibrational noise from attitude control actuators (e.g. thrusters, reaction wheels,

or control moment gyros). However, the attitude control system can be designed to decouple structural dynamics from the spacecraft attitude dynamics, such that the attitude control forces are small. Additionally, the actuators can be sufficiently isolated from the structure such that the vibrational noise from these sources is negligible. Expected sources of static or quasi-static loading are solar radiation pressure, gravity gradient, and D'Alembert forces produced during attitude control maneuvers. Of these loading cases, solar radiation pressure is expected to dominate; the spacecraft will operate in a geosynchronous orbit where gravity gradient forces are minimal, and the attitude control maneuvers are expected to be slow. Therefore normal solar radiation pressure loading will be used as the loading case in the structural design. Modeling the spacecraft as a perfectly reflective flat plate provides a conservative upper bound on the pressure loading of $9.1\mu Pa$.

The key metric in the design of the spacecraft is specific power. Since the present exercise deals exclusively with the structural design, the effects of the structural design on the specific power will be isolated and considered independently. In particular, the effects of structural deflections on power generation and transmission are considered, as is the mass of the structural components.

The most efficient tile arrangement is with all tiles pointed directly at the sun (which maximizes power generation efficiency), arrayed regularly in a single plane (which maximizes power transmission efficiency). Any angular deviations from such an arrangement reduce the performance of the concentrators, and any translational deviations reduce the performance of the microwave phased array.

If the translational deviations are small enough and slow enough, they can be measured and corrected for by introducing appropriate phase delays at each tile location. A system to perform these measurements and corrections will be implemented. The proposed solution includes sun sensors spread over the structure measuring the relative angles from the Sun. This type of sensor is very light and small as it is a simple combination of a quad-photodiode with an aperture hole. The integration from angles to position is done through a modal reconstruction. The shape of the structure is partitioned into target vibration modes and the combined measurements calculates their amplitude. The number and locations of the sensors is optimized to capture enough modes while lowering the influence of measurement noise on the final reconstructed shape. Simulations on a simplified model of a strip with state-of-the-art sensors have shown that the maximum root mean square error is in the order of a millimeter. This position information is then fed back to the electronics

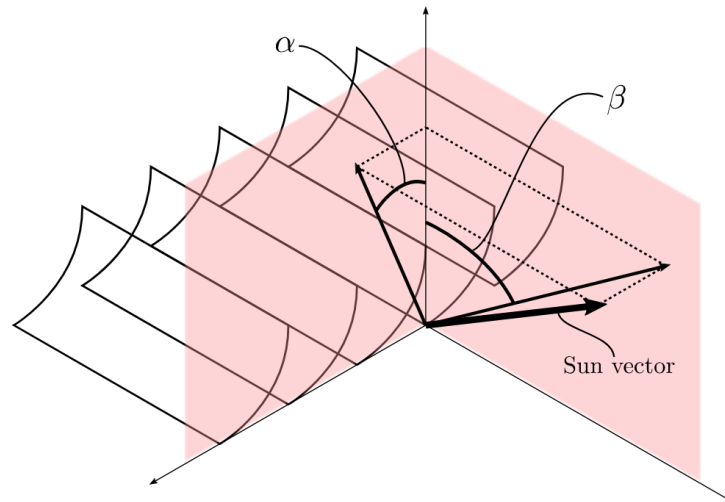


Figure 8.21: The sun vector at each tile is decomposed into a component in the plane of concentration, at an angle α to the tile normal, and a component perpendicular to the plane of concentration, at an angle β .

of each antenna. Thus, the present structural design exercise will consider only the effect of angular deviations from the nominal planar configuration of the tiles.

The performance metric used to evaluate the structural design is the specific concentrated power: the total power concentrated on the photovoltaic cells divided by the total mass of the spacecraft. The total concentrated power depends on the incoming solar power flux (1370 W/m^2) and the average tile concentrating efficiency.

The performance of the concentrators in the tiles depends on the local sun angle. As shown in Figure 8.21, the local sun vector can be decomposed into a component within the plane of concentration, which makes an angle α with the local tile normal, and a component perpendicular to the plane of concentration, which makes an angle β with the local normal. The optical efficiency of the concentrators depends on α and, with lower sensitivity, on β . In the present study, the concentrators across the entire spacecraft are arranged to be all parallel. This allows the spacecraft can slew in a manner that changes the global β angle without changing the global α angle, thus minimizing the effect of such slews on concentrating efficiency.

For this initial analysis, it is assumed that the spacecraft is pointed directly at the sun. Due to solar radiation pressure, the structure deflects out-of-plane, resulting in nonzero α and β angle at each tile location. To compute these deflections and thus these angles, the following structural model was constructed.

The strips were modeled as beams. The ligament connections between the strips

were not accounted for in this initial model. The diagonal cords were modeled as lines under tension, and the booms were modeled as beam-columns. For fixed side length $L = 60\text{m}$, this simplified model has only four structural parameters that control the deflected shape of the spacecraft: the bending stiffness of the boom, the bending stiffness of a strip, the number of strips in a quadrant (which controls the width of each strip), and the diagonal cord tension.

The other component of the performance metric is the spacecraft mass. It was estimated by accounting for the mass of the tiles, the hub, the strip structure, the booms, and the diagonal cords. The tile mass was calculated by multiplying the expected tile areal density of 80g/m^2 by the total spacecraft area. The tile mass does not change with changes in the structural design of the spacecraft. The hub mass was assumed to be fixed at 50kg . This estimate is based on the use of nano-satellite components and includes the propulsion system. The mass of the strip structure was calculated by taking a homogenized strip linear density (accounting for the cross-sectional area of the longerons, the density of the longeron CFRP material (1600 kg/m^3), and the battens), and multiplying it by the total strip length. The boom mass was estimated by using a homogenized linear density. The diagonal cord mass was calculated by estimating an appropriate cross-sectional area (taken to be the area that results in 0.1% strain given the desired diagonal cord pre-tension), and using this area to calculate the diagonal cord linear density (using a volumetric density of 1600 kg/m^3).

The booms were taken to have the properties of the ATK Coilable Boom for the ST8 Sailmast with a bending stiffness of 8035Nm^2 and a linear density of 70g/m [120]. For this choice of boom architecture, the optimal design exists at a diagonal cord tension of 3.84N , 20 strips per quadrant, and a strip bending stiffness of 10.78Nm^2 . The mass of this $60\text{m}\times 60\text{m}$ spacecraft is found to be 369kg , leading to an overall areal density of 102 g/m^2 .

To achieve the desired strip bending stiffness of 10.78Nm^2 , the two longerons supporting the strip must each have a bending stiffness of half this value, i.e. 5.39Nm^2 . Assuming a Young's modulus of 140GPa (typical of carbon fiber composites), a TRAC cross-section with a flange radius of 10mm and a flange thickness of $68.5\mu\text{m}$ was designed to provide this bending stiffness. A TRAC flange thickness of $68.5\mu\text{m}$ leads to a flattened longeron thickness of $137\mu\text{m}$. Assuming the flattened tiles and the flattened battens are thinner than the flattened longerons, the flattened strip thickness can be taken to be $137\mu\text{m}$ for the purposes of the following packaging

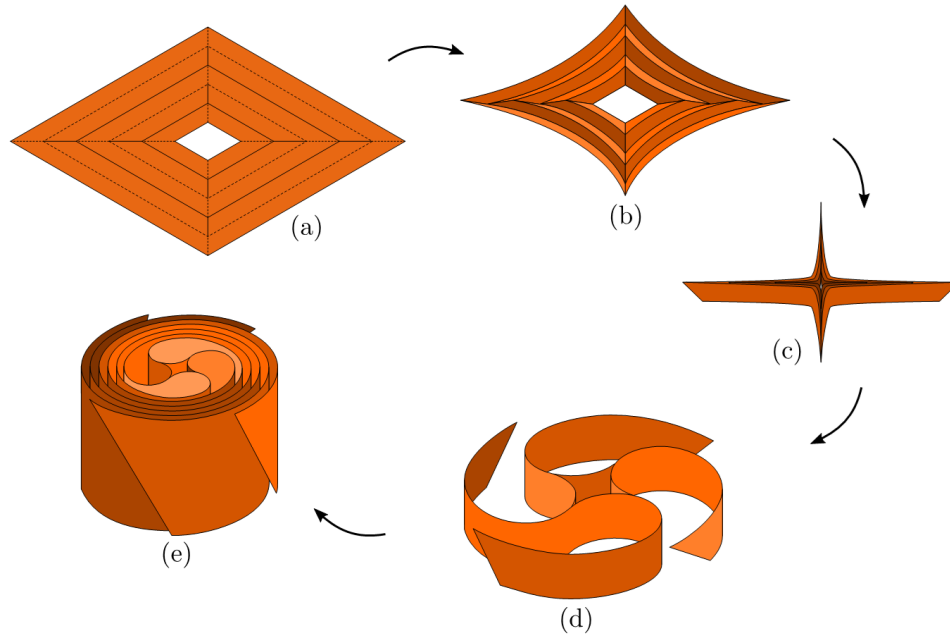


Figure 8.22: Spacecraft packaging concept. For clarity, only the outermost strips are shown in (d) and (e).

study.

Module Packaging Concept

The spacecraft packaging concept relies on slipping folds that connect the strips to each other. A slipping fold allows for both rotation about and translation (or slip) along the axis of the fold. These slipping folds are implemented using the aforementioned ligament connections between the strips. Slipping folds allow for sheet-like structures to be folded and wrapped tightly and efficiently, while accommodating the finite thickness of each strip. Crucially, the strips experience no extension during folding and the maximum bending stresses in the wrapped state can be predicted and controlled. It has been demonstrated that for parallel slipping folds, packaging efficiencies of up to 73% can be achieved [25].

Figure 8.22 shows a conceptual illustration of the module fold pattern with 5 strips. It consists of a number of concentric equally spaced squares, alternating between mountain and valley folds. Additional folds run along the diagonals of the squares, creating degree-4 vertices (points at which 4 folds meet) at every corner of every square (except the innermost and outermost squares).

Folding along these lines produces a star-like shape with four arms, as shown in Figure 8.22(c). Wrapping these arms results in a compact packaged cylindrical form (see Figure 8.22(e)). There are five voids in the packaged form; one in the center, and one associated with each wrapped arm. The slipping folds allow for adjacent strips to slide past each other, accounting for the different radii of the strips in the wrapped configuration.

Key descriptors of the packaged form – the packaged height and the packaged diameter, the packaging efficiency, and the maximum slip – can be estimated using a kinematic volume-based model [24]. For a 60m x 60m structure, with 20 strips per quadrant, a flattened strip thickness of $137\mu\text{m}$, and a minimum bend radius of 13.7mm (designed to impart no more than 0.5% strain in the longerons), the packaging efficiency was estimated to be 95.6%. The packaged configuration of the spacecraft was estimated to occupy a cylinder with a diameter of 0.92m and a height of 1.50m. In this packaged form, the maximum slip between strips was estimated to be 16.8 mm, which defines the ligament length.

The compact packaging technique enables the launch of many modules in a single launch vehicle. Figure 8.23 shows the number of modules that can fit in the payload fairing of a single launch vehicle for different types of launch vehicles and different packaging efficiencies. Except for NASA's Space Launch System (SLS), in all other cases, the number of 0.92 m wide modules that can be accommodated is limited by the total mass carrying capability of the launch vehicle. However, if the packaging efficiency reduces, we end up in a regime where the total number of modules is limited by how many can be fit within the available volume.

8.7 Discussion on System Integration

Total System Mass

The photovoltaic concentrator portion of the tile has an area mass density of 98 g/m². Of this, 62 g/m² is comprised of the 10 micron polyimide mirrors with 10 microns of aluminum and 4 microns of SiO₂, which provide thermal conduction and improved mirror emissivity, respectively. At 20 suns the cells and their radiation shielding contribute only 26g/m². The remaining mass comes from the carbon fiber springs and other structural elements.

The electronics and its supporting structures add mass to the overall system through several components: electrical and electronic connections (both at DC and at radio-frequencies), mass of the supporting structures and materials, and the mass of

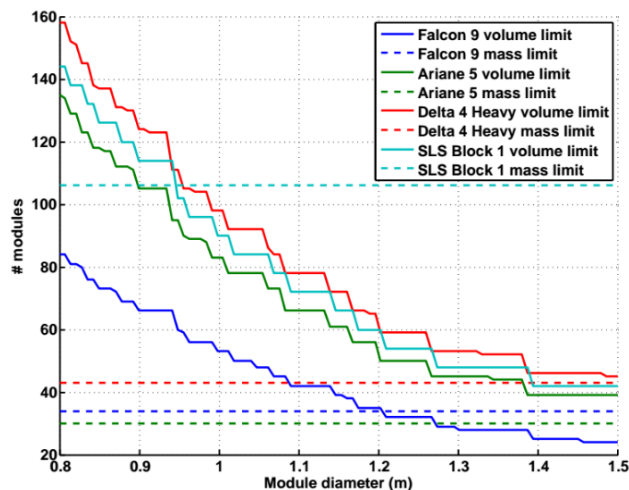


Figure 8.23: Number of modules that can be fit within the payload fairing of typical launch vehicles for different diameters of the packaged modules.

the silicon integrated circuits themselves. For the silicon mass, we conservatively estimate a $5\text{mm} \times 5\text{mm} \times 0.3\text{mm}$ IC per 100cm^2 tile, yielding $10\text{mg}/1\text{W}$ RF power if we assume a PV conversion efficiency of 30% and an DC-to-RF conversion efficiency of 50%. For the weight of conductors, we note that the skin depth for aluminum at 1GHz, approximately $2.75\mu\text{m}$. As discussed in a later section, to achieve sufficient heat distribution, we require a minimum of one layer of $5\mu\text{m}$ Al equivalent, which can function as a DC supply connection. The sheet resistance of $5\mu\text{m}$ Al is $6\text{m}\Omega/\square$, sufficient to conduct DC currents from the PV to the circuits if we allow for locally thicker metal at current bottlenecks (e.g. the IC location). Two additional conductor layers $2\mu\text{m}$ thick and 50% fill ratio to pattern the patch antenna as well as interconnections yields a total mass of $190\text{mg}/\text{tile}$ or $90\text{mg}/\text{W}$ of Al. Simulations of antenna efficiency versus metalization thickness indicate that good efficiencies are achievable for thicknesses less than skin depth. Two layers of polyimide for a total thickness of $20\mu\text{m}$ yields close to $160\text{mg}/\text{W}$. Finally, taking into account a radiation shield of $1000\mu\text{m}$ Alumina adds $50\text{mg}/\text{W}$. The per tile weight of electronics and related electrical connections is, then, $310\text{mg}/\text{W}$ or approximately $60\text{g}/\text{m}^2$, of which approximately 51% is the weight of the polyimide, 29% is the weight of the metalization and 20% is the weight of the electronics and radiation shielding.

Using the point design presented in this paper, the individual mass contributions for each component of a $10 \times 10\text{cm}$ tile is shown in Table 8.2(a). In total, the tile has a mass of 1.6g and an areal density of $160\text{g}/\text{m}^2$. At the $60 \times 60\text{m}$ module, the

Layer	Material	Thickness (μm)	Mass (g)
Concentrator Reflective	Al	10	0.324
Concentrator Backing	Kapton	10	0.170
Front Emissive Layer	SiO ₂	4	0.122
PV Cell	III-V layers + Cu	40	0.257
Tile Support	Kapton	10	0.142
Routing Layer	Al	5	0.135
Antenna Backing	Kapton	10	0.142
Antenna Conductive	Al	2	0.054
Si IC + Shield	Si/Al ₂ O ₃	300/1000	0.116
Carbon Fiber Frame	Carbon	various	0.138
Total			1.6

(a)

Component	Mass (kg)
Tiles (@ 160 g/m ²)	576
Hub	50
Strip structure (longerons + battens)	19
Booms	12
Diagonal cords	0.01
Total	657

(b)

Table 8.2: (a) Breakdown of mass contributions and total mass for a 10cm×10cm tile. and (b) for a 60m×60m module

total mass breakdown including all additional structural elements is shown in Table 8.2(b).

Orbital Consideration

One of the primary challenges with space-based solar power is the design and maintenance of a satellite constellation in formation flight. In the past decade, substantial amount of research has been done on the guidance, navigation and control of formation flying satellites [147, 148, 163, 174]. Formation flight has also been demonstrated in space by missions such as GRACE [96], GRAIL [187], TanDEM-X [98] and PRISMA [131].

A critical decision in the orbital design of the space solar constellation is the choice of the orbit altitude. From a launch cost perspective, low Earth orbits (LEO) are easier to get to and place less stringent requirements on the beamwidth of the antenna array. But a LEO constellation would not be able to generate power ~40% of the time on account of being eclipsed by the Earth. While the constellation could be placed in a terminator orbit (polar sun-synchronous 6am-6pm), it leads to a highly inefficient orientation for RF transmission. The LEO constellation would also require a network of ground-based receivers on Earth to continuously relay power from the space-based array. Moreover, in low Earth orbit, one has to deal with orbital perturbations due to atmospheric drag, Earth oblateness and solar radiation pressure, further complicating the guidance, navigation and control problem.

On the other hand, a constellation in the geostationary orbit (GEO) can radiate all

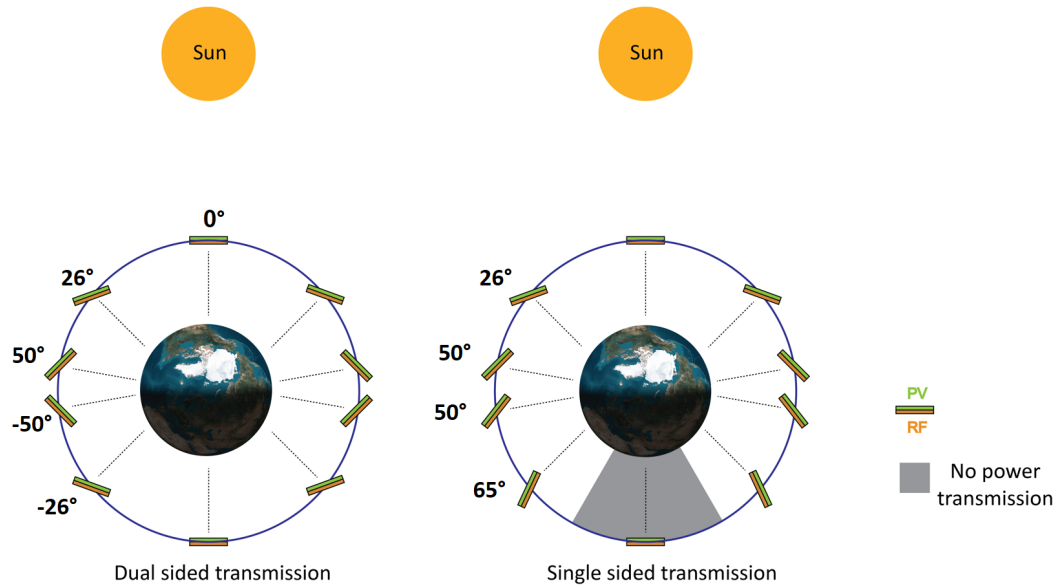


Figure 8.24: Single and dual-sided capacity factor schematic.

its power to a single ground-based receiver. The spacecraft are in view of the sun at all times, except for a few days in the year close to the equinoxes when the Earth eclipses the sun for up to an hour each day. While the electronics in GEO have to survive a harsher radiation environment, maintaining a constellation in formation flight is relatively easier since we only have to deal with orbital perturbations from solar radiation pressure. Keeping these factors in mind, the point design presented in this paper assumes that the constellation is in a geostationary orbit.

Capacity Factor

The total power delivered to the receiver array on Earth depends on two major geometrical factors 1) angle made by the photovoltaic concentrators with the incoming solar radiation 2) angle made by the transmitting patch antenna array with the receiving station on Earth. Taking these two factors into account, we can estimate the desired optimum orientation for the modules at each location in the geostationary orbit. This optimum orientation depends on whether the RF energy can be transmitted through the photovoltaic layer and these two scenarios are presented in Fig. 8.24.

As shown in the figure, the modules rotate continuously to achieve the right balance between collecting solar power at a favorable angle and transmitting RF power efficiently to the ground receiver. In the case of dual-sided transmission, power is generated and transmitted throughout the orbit but there is a rather sudden flip in

the orientation, when the modules are at locations corresponding to 6 am and 6 pm local time. The single sided transmission case does not require any sharp attitude maneuvers but the system has to go through a phase of not being able to transmit any power to the ground receiver. Based on current estimates, the dual-sided system is expected to deliver 1.56 times more power than the single-sided system. However, this would require the design of RF-transparent photovoltaic concentrators with two separate planes for RF transmission or equivalently, PV-transparent RF antennas. Engineering solutions for dual-sided systems and their corresponding mass penalties are currently being evaluated.

Radiation Discussion

We evaluated the radiation environment for our space based solar power system operating in GEO and LEO orbits including the effect of trapped protons and electrons, solar protons and galactic cosmic rays. Total Ionization Doses (TID) and Displacements Damage Dose (DDD) are presented for different space based solar power components that we have described in the current paper. Results are summarized to evaluate potential system degradation and to perform system trade studies, optimizing main component design for radiation hardness, radiation shielding, and expected power profile over system operating lifetime. The initial focus is on ionizing effects on micro-electronics degradation (TID analysis) and non-ionizing radiation effects on solar cells degradation (DDD analysis) effects of particle radiation; evaluation of concentrators will be performed in the future.

Geostationary orbit is in the outer radiation belt and is dominated by high energy trapped electrons and solar protons from the solar events, which are the primary sources for solar cell degradation.

For typical solar panels on GEO orbit with ~75 microns of the front cover glass shielding and semi-infinite back shielding as a solid back panel, solar cells are exposed to $\sim 5 \times 10^{14} \text{ e}^-/\text{cm}^2$ equivalent 1MeV electron fluence after 15 years of operation. This exposure typically causes degradation to approximately 87% initial performance for 3-junction (3J) GaAs solar cells. For SSPI ultralight concentrating photovoltaic system design and 3J GaAs cells as an example with 75 microns of front cover glass and mass equivalent shielding on the reverse, the equivalent 1 MeV electron fluence at the cell interface will be $\sim 2 \times 10^{15} \text{ e}^-/\text{cm}^2$ after 15 years in GEO orbit, reducing cell performance. (Simulation results we performed using NOVICE and AE9/AP9/SPM fluxes, with RDC coefficients available for 3J GaAs cells.)

In the ultra-light system design, the mass of the cover glass is a major factor in the overall mass of the PV subsystem. This presents the challenge of achieving SSPI PV performance in the GEO radiation environment, while maintaining a physically light and flexible system design. Advanced technologies in two critical areas are under consideration: coverglass development and radiation hard ultrathin solar cells. Recent experimental results reported [162] for ultrathin cell development (IMM 3J 30.8% efficiencies) show 14% power reduction after exposure to 3×10^{15} 1MeV e^-/cm^2 equivalent fluence (in contrast to current operational performance in space for GaAs cells $\sim 30\%$ of power reduction after similar exposure). Solar cell radiation tests will be required to accurately predict degradation of several generations of advanced cells selected for SSPI and to evaluate different types of protective cover material.

For the SSPI integrated circuit (IC), the trapped electrons flux is a dominating factor for TID in the GEO environment. NOVICE simulated IC depth / dose curves show the IC will have an absorbed dose of 1Mrad with ~ 40 mils (1000 microns) of ceramic shielding for 15 years of operation. This amount of shielding is not a challenge for system weight considerations due to the small size of the IC. To mitigate radiation effects at these levels, there are several novel approaches to fabricate rad-hard components, even in commercial production, by applying advanced design techniques.

At LEO, with opportunities for initial SSPI scaled demonstration, it is becoming common to use commercial-off-the-shelf (COTS) components. Low Earth Orbit spans a range of altitudes which starts below, and reaches into, the inner Van Allen Belt. Below the inner Van Allen radiation belt (approximately 600 km) the environment is relatively benign, and the low energy electron environment is orders of magnitude lower than at GEO orbit. The TID environment at LEO increases steeply with altitude as the orbit enters the inner Van Allen Belt which has high concentrations of both trapped electrons and trapped protons. Specific consideration will be required for any particular proposed LEO orbit testing for SSPI small scale operation for concept demonstration.

Ground Receiver and Rectenna

The ground receiver is designed as an array of RF to DC converters (rectennas) that collect and convert the transmitted RF power on earth. A general structure for a rectenna element consists of the receive antenna, a low pass filter, diodes for RF-

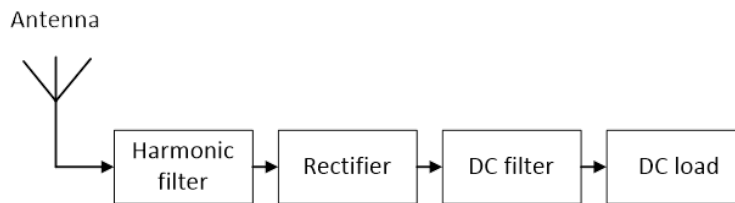


Figure 8.25: General rectenna structure.

DC conversion and a filtering element to suppress AC components in the rectified waveform (Fig. 8.25).

One of the most important performance metrics of the ground rectennas is the RF-to-DC power conversion efficiency. Besides losses in the passive impedance matching and filtering components, various non-idealities in the diode, such as ohmic resistance, non-zero turn-on voltage and package inductance and junction capacitance, limit the conversion efficiency and maximum frequency of operation. Based on results reported in the literature, we expected conversion efficiencies in the range of 60%-85% at frequencies of interest using current technologies as evidenced by recently reported efficiencies of 73%, 85%, 83%, and 60% at 2.45GHz[161], 2.14GHz [140], 4.5GHz [55], and 10GHz [177], respectively.

Mechanical Prototype of Tile

Initial tile mockups, one of which is shown in Figure 8.26, were constructed to demonstrate the feasibility of this concept. In these mockups, the ground layer was constructed using 10cm×10cm, 7.5 μ m-thick polyimide film (Dupont Kapton HN), supported at the edges by a frame of 120 μ m-thick pultruded carbon fiber rods. The patch antenna layer was built using a similar technique, using 7.5 μ m-thick polyimide film and a pultruded carbon fiber rod frame. The ground and antenna layers have representative conductive aluminum layers deposited on them. The “S” springs were constructed using carbon fiber composite material. The initial 10cm×10cm tile mockup has a mass of 1.56g. The tile mass is expected to decrease to at least 0.8g.

8.8 Clock multiplication with programmable phase control

Generating accurate timing is one of the most important challenges in large scale arrays. In our proposed architecture, we provide the timing reference at a lower frequency than the radiation frequency. The main advantage of having a reference timing on a separate frequency is the minimization of phase pulling. Radiated

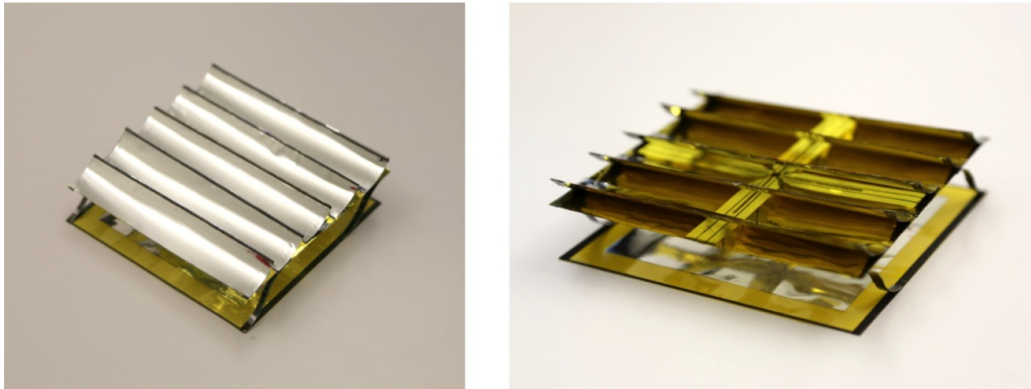


Figure 8.26: Initial mechanical prototype of our space based solar power tile.

frequency can couple to the reference distribution network and affect the timing if they have similar frequencies. Having the timing on a much lower frequency allows easy filtering of the coupled signal. The other advantage of using a low frequency timing distribution is reducing the complexity of such networks. Distribution of high frequency reference timing signal on a large scale array is not only complex, but it requires placement of multiple repeaters as the high frequency signals attenuate more quickly.

By using a phase locked loop (PLL) it is possible to up convert the frequency of the timing signal. While distribution of 10GHz signal on the IC is possible, it will consume noticeable power. One approach is then to distribute the low frequency input timing and produced the 10GHz signal close to the PA. The main problem with this approach is the large area that is required for the loop filter of the PLL and the power consumption of the VCO. PLL loop filter bandwidth should be designed less than $1/10^{\text{th}}$ of the reference frequency and since the input reference is 50MHz, this loop bandwidth is less than 5MHz. In order to have such a small loop filter bandwidth, large loop capacitance is required. The PLL does not track the reference input phase beyond the bandwidth frequency, and low bandwidth of the PLL means that the VCO phase noise should drop quickly. Lower phase noise for the VCO implies higher current consumptions (for a given inductor Q).

In order to address these issues, we propose a two step frequency conversion as shown in Fig. 8.27. In the first step, a central PLL multiplies the timing reference frequency to 2.5GHz which is easily distributed on chip using low power CMOS logic gates. In the second step the 2.5GHz signal is multiplied to 10GHz using a second PLL which can be designed to be very small and low power since the PLL

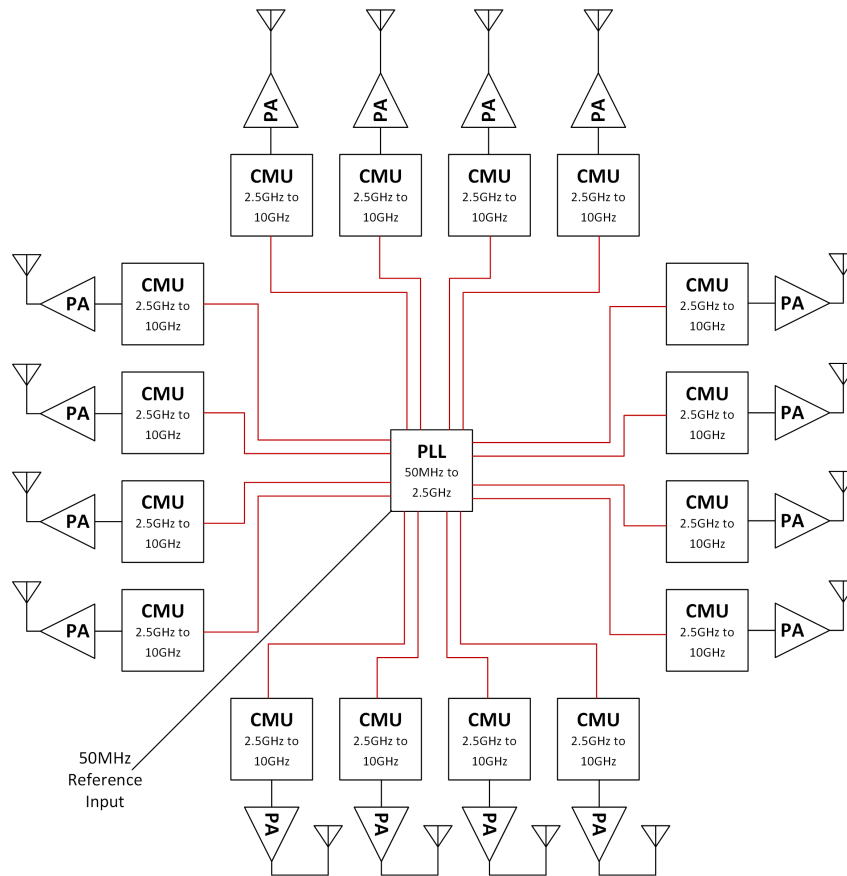


Figure 8.27: Block diagram of reference distribution inside the DC to RF IC.

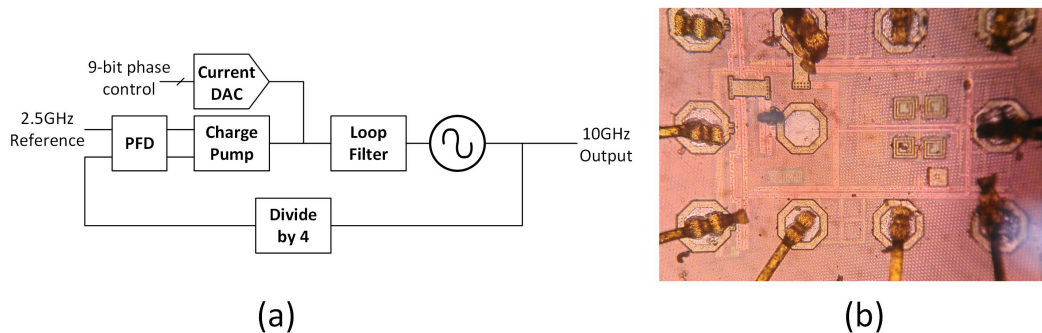


Figure 8.28: (a) Block diagram of clock multiplier unit (CMU). (b) Die photograph of the test structure.

bandwidth can be designed to be much higher. In this part, I will describe the design of the second stage clock multiplier unit (CMU) which is also responsible to provide programmable timing adjustment.

The block diagram of CMU is shown in Fig. 8.28. The main difference between CMU and a typical PLL is the addition of current DAC that injects or subtracts

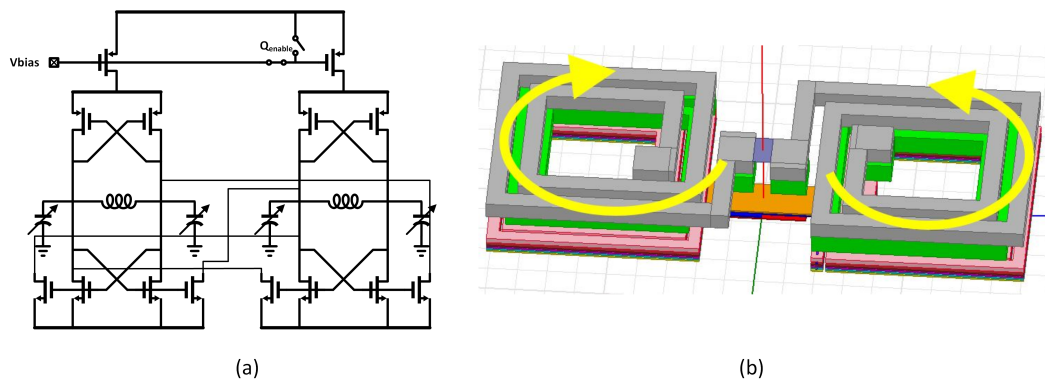


Figure 8.29: (a) Quadrature VCO schematic (b) Compact figure 8 inductor design for the QVCO

current to the output of charge pump. Since in steady state, the current that enters the loop filter should have a zero DC value (otherwise the VCO control voltage rails to GND or VDD), the injected current by the DAC should be canceled by the DC value from the charge pump. The DC current from the charge pump is linearly proportional to the phase offset between the reference signal and the divide by 4 output. Hence, by changing the DC value of the injected current phase offset between reference and divider output can be modified. Since the divider output follows the phase of the VCO (with factor of 4 difference), this method allows to both multiply the 2.5GHz frequency and adjust the phase of 10GHz signal simultaneously in one circuit block.

The schematic of quadrature VCO with the ability to power off the quadrature section is shown in Fig. 8.29(a). In order to minimize the size of the VCO, the inductors footprint needed to be minimized. A 3-turn stacked inductor in a figure 8 configuration was used chosen as the inductor (Figure 8.29(b)). The figure 8 shape of the inductor helps reducing the coupling between the PA radiation and the PLL. The inductor has a small footprint of $70\mu\text{m} \times 35\mu\text{m}$, inductance of 2.8nH and quality factor of 6. The VCO is tunable from 9.3GHz to 11.8GHz and consumes 1mW and 2mW with quadrature being off and on, respectively.

In order to divide the 10GHz clock, a fast flip-flop is required. A CML based flip flop can easily operate beyond 10GHz but consumes high power. CMOS logic gates consume less power but cannot operate at 10GHz. Dynamic logic gates, however, can operate up to 12GHz in TSMC 65nm process. A true single phase flip flop [81] based on dynamic logic gates was chosen for the divide by two operation. The schematic of the divide by two is shown in Fig. 8.30(a). The divider consumes less

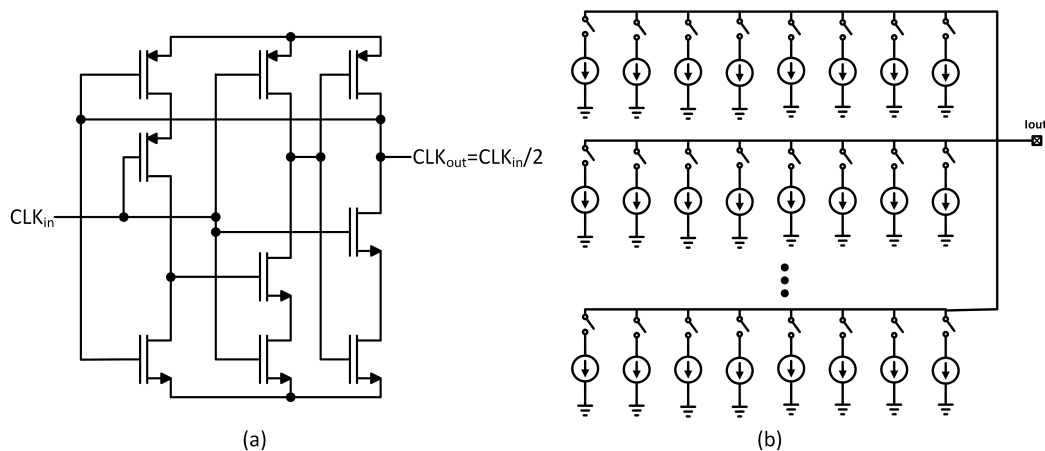


Figure 8.30: (a) Clock divider based on true single phase DFF, (b) Thermometer coded current DAC

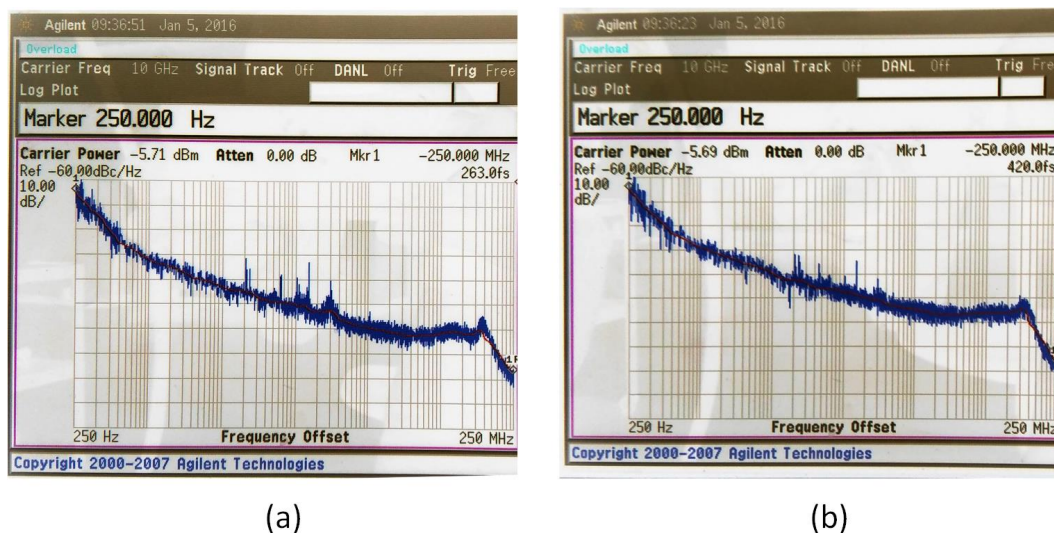


Figure 8.31: Phase noise and jitter of the CMU test structure when (a) DAC current is set to zero and (b) when DAC current is at full range

than 150uA of current at 10GHz.

The schematic of the current DAC is shown in Fig. 8.30(b). It is an 8-bit thermometer-coded DAC which drives a selectable current mirror. The ninth bit of DAC controls the current mirror and can set the current to be sourced or sunk from the charge pump node. A thermometer topology was selected to insure monotonicity of the phase shift.

The jitter measurement of CMU is shown in Fig. 8.31 in two cases when the DAC current is set to zero and when it is at maximum value. The total integrated jitter

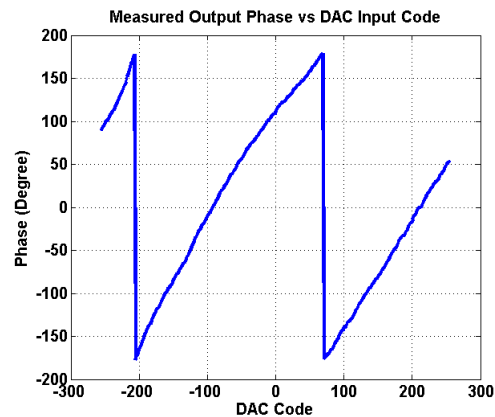


Figure 8.32: Measured output phase vs DAC input code of CMU.

from 250KHz to 250MHz is around 260fs when the DAC is set to zero. When the DAC is turned on, its current noise (filtered by the loop filter) will introduce jitter to the PLL. As it can be seen from Fig. 8.31(b) the jitter increases to 420fs.

The phase control ability of the CMU is shown in Fig. 8.32. As it can be seen the output phase changes monotonically with respect to the programming code and it covers more than 360° which is required for developing beam forming algorithms.

8.9 High efficiency, high power rectenna design

Wireless power transfer using radio frequency is widely utilized in low power applications such as RFID tags and transponders. Higher power rectifiers are desired for applications such as wireless power transfer from space to earth [111] or for terrestrial applications such as wireless charging of portable devices. An RF rectifier has the reverse power flow of a power amplifier (PA). While PA converts DC power to RF power, a rectifier converts the RF power back to DC. A power amplifier design can be used as rectifier [139] with similar rectification efficiencies to the PAE of the amplifier. A schottky diode rectifier can also benefit from the efficiency enhancement techniques used in PA design such as harmonic termination to achieve higher efficiencies at a lower cost [140]. In this paper we present the design of a harmonically terminated schottky diode rectifier with high power recovery capabilities.

Rectifier Design Methodology

Fig. 8.33(a) shows a basic RF rectifier and the voltage and current waveforms of for a parasitic free diode is shown in Fig. 8.33(b). In order to maximize the conversion efficiency which is the ratio of the DC output power to the power delivered to the

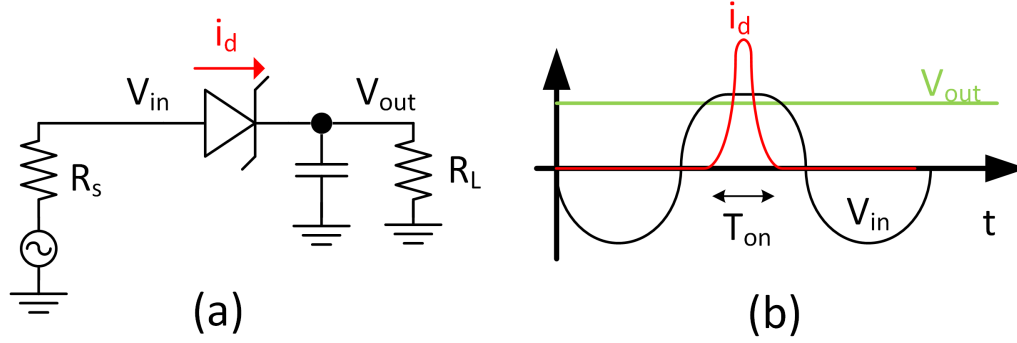


Figure 8.33: (a) Schematic of a simple diode rectifier and (b) the corresponding voltage and current waveforms.

rectifier, the ratio of the loss in the diode to the DC power delivered to the load has to be minimized. The average power lost in the diode, P_d , can be expressed as:

$$P_d = \frac{1}{T} \int_{T_{on}} V_d I_d dt \quad (8.6)$$

$$= \frac{1}{T} \int_{T_{on}} (V_{d_0} + I_d R_d) I_d dt \quad (8.7)$$

$$= \frac{1}{T} V_{d_0} \int_{T_{on}} I_d dt + \frac{R_d}{T} \int_{T_{on}} I_d^2 dt \quad (8.8)$$

where I_d is diode current, R_d is the diode series resistance, V_{d_0} is the intrinsic turn-on voltage of the diode, T_{on} is the period over which the diode conducts, and T is the period of once cycle. The diode current replenishes the charge lost in the capacitor in one cycle, and hence we have:

$$\int_{T_{on}} I_d dt = I_L T \quad (8.9)$$

where $I_L = V_{out}/R_L$ is the load current. The second term in equation 8.8 is the ohmic loss of the diode which is proportional to the mean square average of the current. Using the following inequality:

$$\frac{1}{T_{on}} \int_{T_{on}} I_d^2 dt \geq \left(\frac{1}{T_{on}} \int_{T_{on}} I_d dt \right)^2 \quad (8.10)$$

and substituting equation 8.9 into 8.8:

$$P_d \geq V_{d_0} I_L + R_d I_L^2 \frac{T}{T_{on}} \quad (8.11)$$

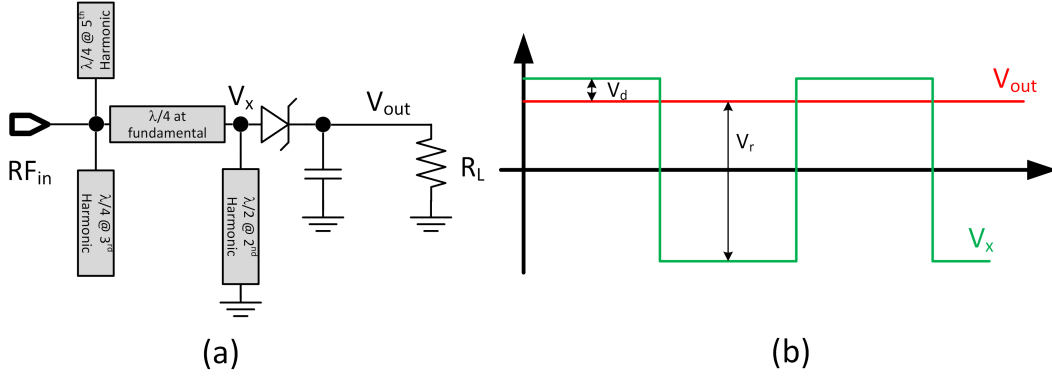


Figure 8.34: (a) Block diagram of proposed harmonic termination for the rectifier, and (b) idealized voltage waveforms.

The conversion efficiency of the rectifier can be written as:

$$\eta_c = \frac{P_{out}}{P_{accepted}} \quad (8.12)$$

$$= \frac{P_{out}}{P_{lost} + P_{out}} \quad (8.13)$$

$$= \frac{V_{out} I_L}{V_{out} I_L + P_d} \quad (8.14)$$

$$\leq \frac{V_{out}}{V_{out} + V_{d0} + I_L R_d \frac{T}{T_{on}}} \quad (8.15)$$

where V_{out} is the output DC voltage. It should be noted that the equality holds if and only if I_d is constant over T_{on} . Constant I_d forces constant V_{in} over the on period of the diode. From equation 8.15 we deduce that increasing T_{on} will increase the efficiency. This is why square waveforms of a class F type harmonic termination as shown in Fig. 8.34 are desirable for rectification applications.

The maximum efficiency of the diode can be obtained when V_{out} is maximum and also the current passing through the diode is small enough such that the voltage drop in the series resistance of the diode is negligible. Based on Fig. 8.34(b) the following relation between V_{out} , V_d , and the reverse voltage on the diode, V_r , is held:

$$V_{out} = \frac{V_r + V_d}{2} - V_d \quad (8.16)$$

$$= \frac{V_r - V_d}{2} \quad (8.17)$$

The maximum output voltage that can be achieved is when the output voltage is maximized which translates to when the diode is close to the breakdown voltage: $V_{out,max} = (V_{BR} - V_d)/2$. As a result the maximum efficiency of a diode rectifier

cannot exceed the following value:

$$\eta_{c,max} = \frac{V_{BR} - V_{d0}}{V_{BR} + V_{d0}} \quad (8.18)$$

$$= \frac{1 - \frac{V_{d0}}{V_{BR}}}{1 + \frac{V_{d0}}{V_{BR}}} \quad (8.19)$$

$$\approx 1 - 2 \frac{V_{d0}}{V_{BR}} \quad (8.20)$$

Equation 8.20 gives an upper bound for rectification efficiency. To get close to the bound in equation 8.20, the input RF voltage swing which is the fundamental component of the square wave shown in Fig. 8.34(b) should be $\frac{2}{\pi} (V_{BR} + V_{d0})$ in order to drive the diode to close to break down voltage, while the RF current should be small enough such that voltage drop across the diode does not become comparable to the diode turn-on voltage. If the diode's series resistance is large, this implies a large RF source impedance. In practice matching network losses and limited Q factor of the parasitic capacitance/inductance of the diode will result in lower values of efficiencies. For a diode with low resistance and parasitic capacitance it is possible to get close this maximum value.

The block diagram of the proposed rectifier is shown in Fig. 8.34(a). The diodes is placed in series and the anode is connected to the RF side while the cathode is connected to the DC side. This allows for low capacitance loading of the RF side as the metal contact in the n-type schottky diodes forms the anode and has a smaller parasitic capacitance compared to the cathode which is formed on the semiconductor substrate. The rectifier utilizes a class F matching network to shape the waveforms and block the harmonics from reflecting back to the source. The anode of the schottky diode is connected to a $\lambda/2$ short stub at second harmonic. This stub provides a short impedance at second and close to short impedance at higher even harmonics, thus it prevents generation of even harmonic voltages at the anode of the schottky diode. At fundamental frequency, the stub is close to $\lambda/4$ and will act as an open. It also provide the DC current path for the rectifier. The $\lambda/4$ open stubs at 3rd and 5th harmonics prevent these odd generated harmonic to radiate back to the RF source, hence improving the efficiency. The $\lambda/4$ line at fundamental between these open stubs and the anode of the diode assures that these stubs appear as an open at the 3rd and 5th harmonics at the anode of the diode and hence do not block generation of those harmonics. Consequently, the waveform on the diode can be as very close to a square wave as class F network requires. At

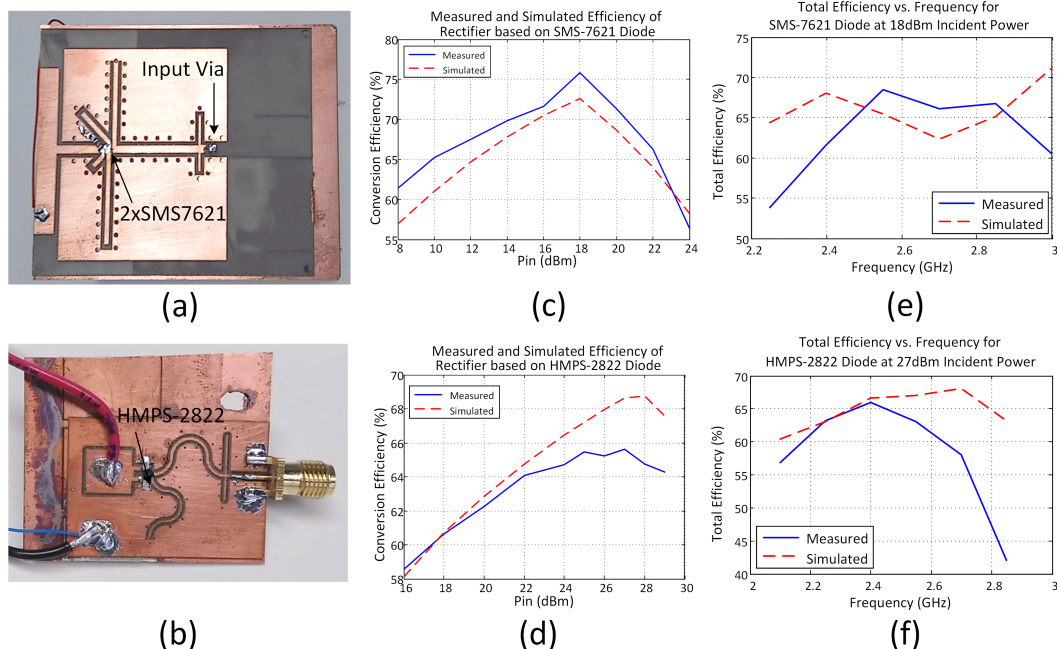


Figure 8.35: (a)-(b) Two prototypes of the rectifier designed with (c), (d) their conversion efficiencies over input power and (e), (f) total efficiencies over frequency.

fundamental frequency, however, these stubs have a capacitive reactance, and after the $\lambda/4$ transformation they will have an inductive reactance on the anode of the diode. By adjusting the width of these stubs, thus it is possible to cancel the parasitic capacitance of the diode. The $\lambda/4$ at fundamental transformation can also be used to adjust the amplitude of the RF signal at V_x , hence allowing maximum efficiency for the given input power.

Among the commercially available low barrier schottky diodes, Skyworks SMS7621-060 and Avago HMPS-2822 were chosen for prototyping. The former has 0.26V turn-on voltage and very little parasitic inductance and capacitance but suffers from low breakdown voltage of 5.5V and has 12Ω of series resistance. The upper conversion efficiency limit of this diode is thus around 91%. The latter diode has a turn-on voltage of 0.34V and has higher breakdown voltage of 15V. This diode has 12ohm of series resistance and has larger parasitic capacitance. The upper conversion efficiency limit of this diode is 95%.

The rectifier based on SMS-7621 was implemented on 32mil thick Rogers 4003 substrate and the HMPS-2822 rectifier was implemented on 7.3mil Rogers 4350 substrate. To measure the efficiencies of the rectifiers, the output of the signal generator was amplified by GaAs power amplifier. A Ditom D312080 isolator was

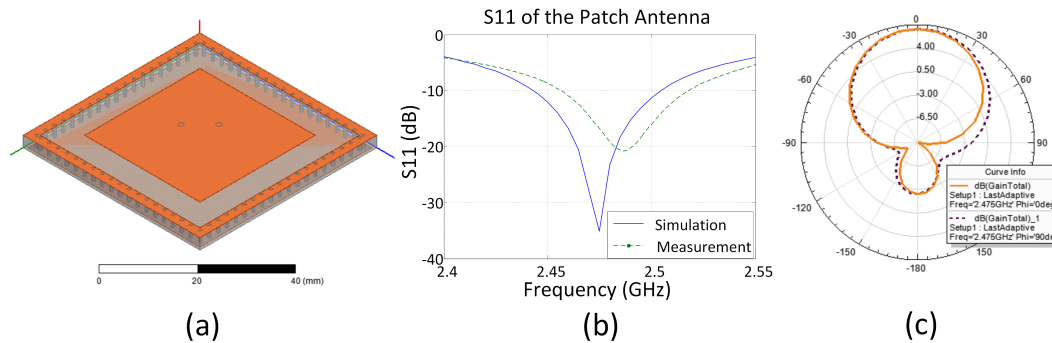


Figure 8.36: (a) The dual polarized patch antenna and (b) its S11

placed after the PA to insure 50 ohm source load to the rectifier, however, the isolator only provides 9dB of isolation which necessitates the use of a load tuner to match the source impedance to 50 ohms for each measurement point. The conversion efficiencies and total efficiencies of the rectifiers at optimum load value is plotted in Figs 8.35(c)-(f). The maximum conversion and total efficiency 75.8% and 68.5% is obtained from the SMS-7621 rectifier at incident power of 18dBm at 2.55GHz. The HMPS-2822 rectifier achieves 66% and 65.6% of conversion and total efficiency at 2.4GHz and 27dBm input power, respectively. These results include the loss of the matching network which sometimes are de-embedded when reported in other works.

Rectenna Design

A dual polarized patch antenna was designed and simulated in HFSS on a 120mil Rogers 6002 substrate and a test antenna was fabricated to verify the design (Fig. 8.36a). The simulated and measured S11 and radiation pattern of the patch antenna is shown in Fig. 8.36(b) and (c), respectively. The simulation predicts a 94% radiation efficiency for the antenna. By placing a rectifier for each port of the antenna, the two cross polarization components of the incident wave are independently rectified.

A 2×3 array of this patch antenna along with the rectifier based on HMPS-2822 was fabricated on a 3-layer board. The array includes 12 rectifiers, with a peak efficiency of 65.6% for an incident power range of 27dBm to 40dBm. Thus the array can produce 240mW to over 6W of DC output power. In our lab we were able to test the rectenna up to around 13mW/cm² of incident power for which we were able to recover around 1.9W of DC power. The output power of the rectenna vs the output load is plotted in Fig. 8.37(c). The total power incident on the physical aperture of the array is 2.05W.

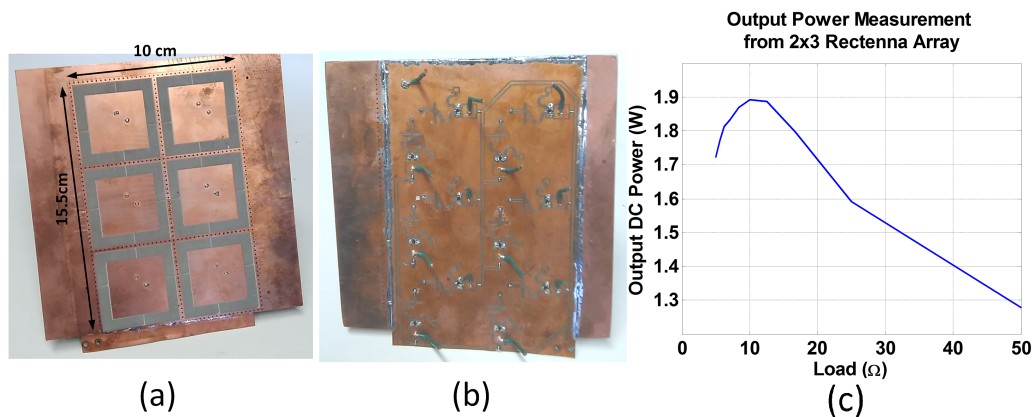


Figure 8.37: (a) Front and (b) back side of the 2x3 rectenna array. (c) Output DC power vs load.

8.10 PA Stacking: As regulator free solution to PA and PV voltage mismatch

CMOS radio-frequency integrated circuits (RF ICs) have continued to penetrate and will eventually dominate various high-frequency applications, many of which have been the sole domain of other technologies in the past. This is primarily due to the favourable yield, achievable system complexity, and cost structure of CMOS SoCs in large-scale production. MIMO (e.g., [15]) and phased-array systems consisting of a large number of radiators and chips continue to be of great interest in various communications, sensing, ranging, and energy management systems to increase their range, data rates, and performance.

The design of fully integrated power amplifiers (PAs) in CMOS technologies for these applications is challenging due to the low breakdown voltages of CMOS transistors compared to other technologies. Cascode or stacked transistor techniques (e.g., [47, 80, 89]) have been used to reduce the voltage stress on any single transistor. However, MIMO and phased array systems require independent control of the signal characteristics of each channel (e.g., phase and amplitude), which presents a challenge in stacked design due to the strong coupling of the voltages and currents of individual stages. In this paper, we propose a novel architecture that stacks the power amplifier in supply domain and, thereby, reuses the supply current while operating from a high supply voltage and allowing for independent control of the operation point of different stages. The architecture is devised to withstand a broad range of intended variations (phase and amplitude), as well as unintended deviations (load mismatch and temperature fluctuation) of the operation conditions among the stages in the stack.

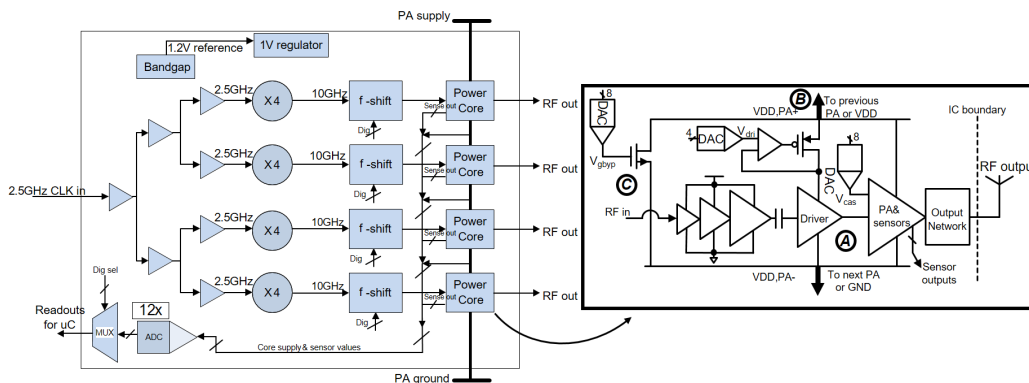


Figure 8.38: Simplified block diagram of the integrated X-Band power amplifier quad

Proposed Stacked Architecture

To achieve independent control of power cores in a stack of multiple amplifying stages, the DC voltage and operating conditions of the individual amplifiers need to be dynamically monitored, as a change in operating conditions of any one amplifier in the stack affects all other PAs. Furthermore, PA bias needs to be constantly actuated to operate each PA under known and safe conditions to guarantee long-term reliability. For a phased-array transceiver, all RF output phases need to be adjustable, with some amplitude control highly desirable. To address these requirements, we implemented a fully integrated power amplifier quad that operates four PAs in a stack from a nominal 3.2V supply, while providing full phase and amplitude control, as shown in the block diagram of Fig. 8.38.

Each of the four power cores implements a full amplifier chain that amplifies a phase controlled signal RF_{in} to the desired output power level of 17dBm while operating the power consuming driver and PA stage from a floating supply. Operational sensors monitor the local supply voltage drop as well as the PA core current consumption and voltage stress. Local ADCs convert the sensor outputs for use with digital operation and feedback control.

Implemented Prototype

Shown in fig. 8.38, each of the four driver and PA output stages (marked A) are operated from a separate local supply domain (marked B). Both stages are biased using digitally controllable driver supply/PA gate bias voltage V_{dri} and PA cascode voltage V_{cas} , which can be used to lower or increase the supply current drawn from the PA supply domain and set the output power.

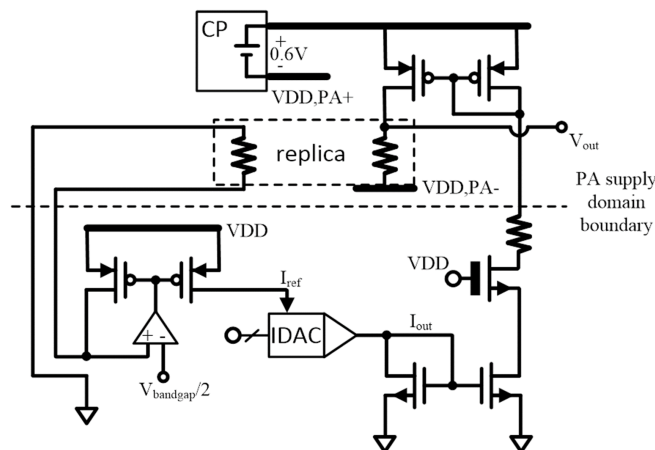


Figure 8.39: Bias current generation used for crossing supply domain boundaries. DACs and regulators operate in the common supply domain, providing currents across boundaries to generate voltage offsets proportional to a bandgap voltage in the PA supply domains

All bias voltages are referenced to the local PA ground voltage to provide constant biasing conditions to the driver and output stage. The bias voltages are digitally controlled and compared to a known bandgap bias voltage. A simplified circuit diagram is shown in Fig. 8.39. Biasing currents for all nodes are generated by a current DACs (IDACs) operating in a common 1V supply (lower half of figure). Reference currents for each of the IDACs are generated to provide a voltage drop commensurate with a bandgap voltage over a resistor in each core. Replica resistors in the cores are then biased with currents proportional to the reference currents to generate known drops across these resistors.

In the event of a sudden undesirable change in the load condition seen by any of the power cores resulting in reduced supply current, a digitally controllable bypass device (marked C in Fig. 8.38) is activated to maintain the overall branch current keeping the voltage drops across all stacked stages within a pre-specified range of variations. Each PA output stage includes a cascode peak voltage sensor and a DC current sensor. On-chip ADCs convert the output of these sensors as well as the absolute voltage levels of the local PA supply voltages to allow a microcontroller to make the appropriate adjustment on these via V_{dri} , V_{cas} and V_{gbyp} using the IDACs. These bias voltages are generated using on-chip current-mode DACs as described above.

In order to complete a digital feedback loop and full operational control, detectors for the DC current and (cascode) peak voltage are implemented within the PA

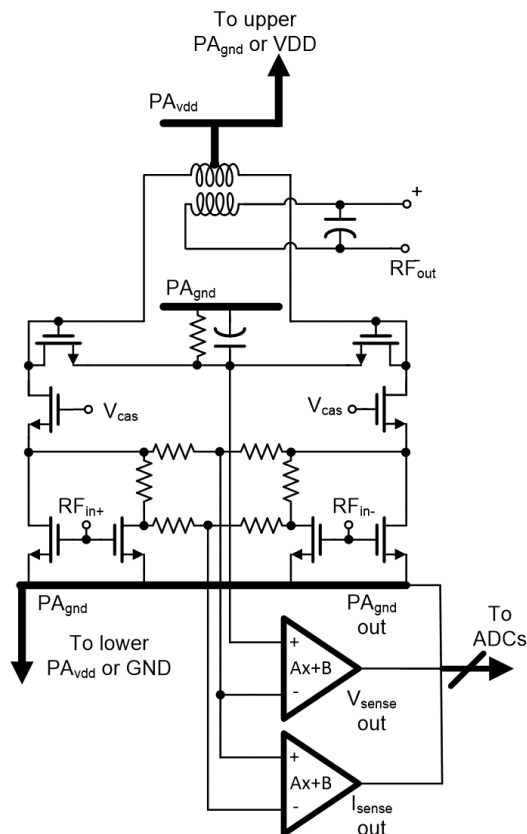


Figure 8.40: Circuit detail for PA core, cascode peak voltage, and DC current detectors, as well as supply level readout for digitally assisted operation

core (Fig. 8.40) together with ADCs for digital readout of detector values and intermediate supply voltage levels. Linear voltage amplifiers with preset offsets are used to limit the detector output to a known window of operationally relevant outputs. The amplifiers use input choppers to limit errors due to noise and mismatch from 25mV_{rms} input referred to 500 μ V_{rms}, allowing to use small geometry devices and limiting required current overhead. The ADCs are realized using an 8-bit SAR architecture including periodic offset compensation. ADC outputs are selected and serialized to be readable by a microcontroller (MCU) via a standard SPI interface. The SPI interface also allows the MCU to program all operational registers (e.g., for bias voltages). The on-chip RF signal is synthesized and phase-shifted from an input clock at one fourth of the output frequency using on-chip clock multiplier units that consume less than 5mA of current while providing digital output phase control.

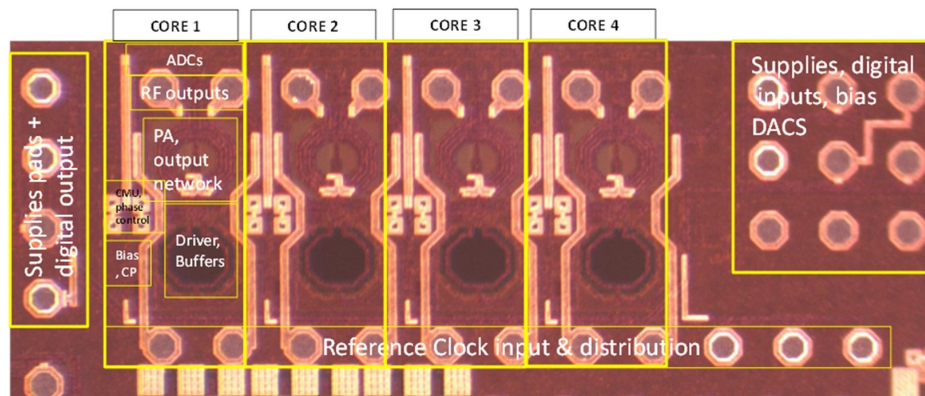


Figure 8.41: Die photograph of implemented power amplifier quadrant

Measurement Results

A fully integrated, four PA stack (quad) including integrated output transformer and impedance matching networks, sensors, clock-multiplier units (CMUs) and phase shifters, is implemented in a bulk 65nm CMOS process. Fig. 9.22 shows the die photograph. Total die area is $0.8\text{mm} \times 2.3\text{mm}$. An off-chip MCU based on an ARM® Cortex-M0® processor supports operation of all aspects of the system. Four power cores are stacked to operate from an overall 3.2V voltage supply (compare Fig. 8.38 and Fig. 8.42). The MCU continuously reads sensor values for all four PAs and implements a software Proportional-Summary-Difference (PSD) controller to adjust the gate voltages of the bypass devices (C in Fig. 8.38). PSD values to provide stable and well-damped controller operation were determined using manual adjustment of coefficients. Plotted in Fig. 8.42 is the actual transient response of all local power amplifier supply voltages to a disturbance of operating conditions at $t=0$ as measured and recorded by the on-chip ADCs and the MCU, respectively.

The use of fully digital operational control allows for great flexibility in controller operation for various applications. A look-up tables (LUTs) alternative to the implemented controller enables determining the load VSWR and operation conditions of each power amplifier and adjusting the biasing conditions optimally to a large number of different circumstances. Because multiple sensors are employed, sensor errors changing with operating conditions (e.g. PVT and VSWR) can be greatly mitigated.

The individual PA output power and PAE versus frequency under nominal conditions are plotted in Fig. 8.43. In the targeted phased-array system, output power is combined in space, with the total RF output power of 23dBm for the quad from

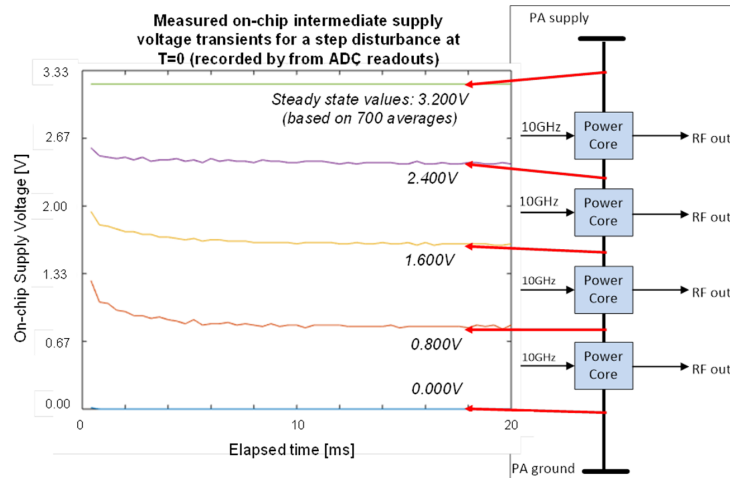


Figure 8.42: Measured supply voltage regulation for PSD controller under disturbance at iteration $t=0$

Measured PAE and Output Power versus Frequency

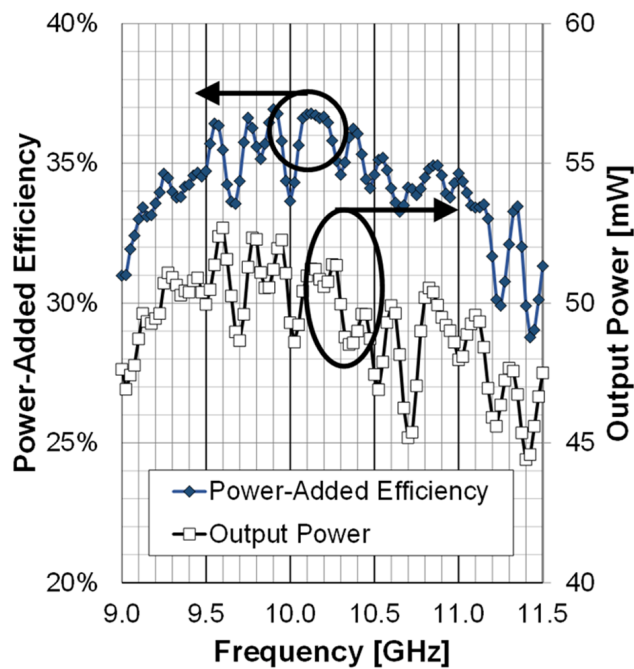


Figure 8.43: Measured PAE and output power over frequency

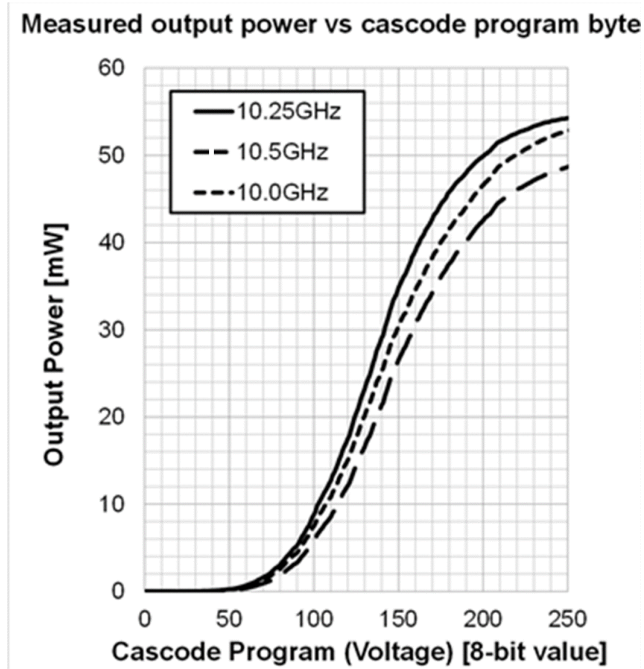


Figure 8.44: Measured output power over cascode voltage

a 3.2V supply and nominal antenna impedances of 50Ω that are transformed using fully-integrated on-chip 2:1 transformer baluns. In-space power combining was experimentally verified by adjusting programmed output phases to maximize broadside radiated power. Taking into account PCB antenna gains and efficiencies, free-space performance compares well to simulations (within measurement error of 0.5dB). Amplitude control via the cascode voltages is shown in Fig. 8.44 for operation at 10.0, 10.25 and 10.5-GHz.

Phase-shifting performance of the integrated CMUs is verified by measuring steady-state output waveforms using a sampling oscilloscope as the effective 9-bit phase setting value is varied (for positive and negative signs). Zero-crossing times of the output signal can be varied by 140ps, providing phase control well in excess of 360° as shown in Fig. 8.45 (including standard deviation). Measured output jitter is less than 500fs RMS when using a spectrum analyzer.

Table 8.3 shows a performance summary and comparison to state-of-the-art CMOS PA implementations. It shows the desirability of the proposed supply sharing and controller scheme for MIMO and phased-array applications.

In summary, the presented novel power amplifier supply sharing scheme is well suited for phased-array and MIMO applications for communications, sensing, rang-

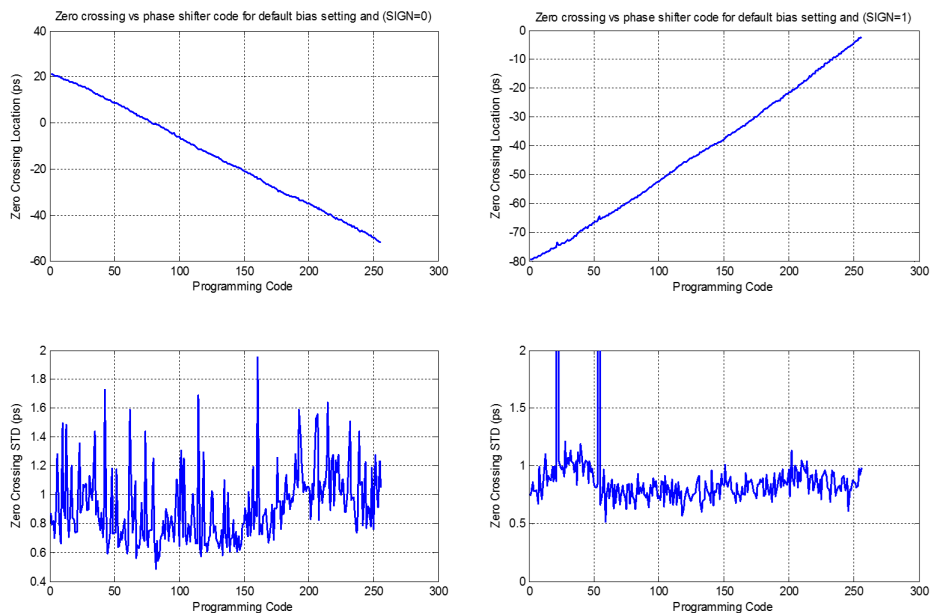


Figure 8.45: Measured relative signal zero crossing location and standard deviation versus phase program for positive (left) and negative (right) code settings. The absolute crossing times for a programming code of zero coincide for a total of 140ps of timing control.

Reference	Frequency (GHz)	P_{sat} (dBm)	V_{sup}	PAE	Drain Efficiency	Technology
[15]	5.0	26.7	3.3	-	25.3	65nm Bulk CMOS
[89]	29	23.7	5.2	29	-	45nm SOI CMOS
[80]	5.9	22.2	1.2	-	49.2	40nm LP CMOS
[47]	10	22.8	4.8	25.7	-	45nm SOI CMOS
[53]	10	24.5	3.0	18	-	180nm CMOS
[130]	9	20.3	2.6	28.9	-	110nm CMOS
This Work	10	23.0	3.2	37.0	-	65nm Bulk CMOS

Table 8.3: Performance summary and comparison to prior work.

ing, and energy management systems

OTHER WORKS

9.1 Integrated Laser Linewidth Reduction

Introduction

Phase noise reduction of lasers has important applications in optical communications, ranging, THz signal generation, electro-optical oscillators, and spectroscopy. Although bench-top power-hungry semiconductor laser linewidth reduction schemes using feedback [158] and feedforward architectures [14] have been demonstrated, a chip based solution leveraging the integration for power and size reduction has not been demonstrated to this date. In this paper, modern RF techniques and architectures are used to integrate the electronic circuitry of a laser phase noise reduction system on a 65nm CMOS process. Hybrid integration of this electronic chip with our fabricated SOI photonic chip results in significant power and area reduction compared to typical bench-top laser phase noise reduction systems. As indicated in [14] and [13], feedback based laser phase noise reduction schemes typically are not capable of offering large phase noise reduction bandwidth due to the feedback loop stability issue. On the other hand, feed-forward schemes can reduce the phase noise over larger bandwidth.

Integrated Feed-Forward Phase Noise Reduction of Lasers

Figure 9.1(a) shows the conceptual block diagram of a feed-forward laser phase noise reduction scheme, where the laser phase noise is first measured and then is fed forward to an optical phase modulator (OPM) to reduce the phase fluctuations of the laser. Figure 9.1(b) shows our proposed realization of the feed-forward phase noise reduction scheme. The laser source output is split into two branches. The bottom branch is coupled into the photonic frequency discriminator that uses a grating coupler serving as an optical pad. The photonic frequency discriminator generates an electrical current proportional to the frequency noise of the source [14]. This frequency noise is the derivative of phase noise of the source within the bandwidth of the discriminator (over 1GHz in our design.) The RF chip is wire-bonded to the back-side-coupled photo-diode at the output of the discriminator to receive the small current representing the frequency noise.

To suppress the phase fluctuations of the source, the OPM should be driven by a

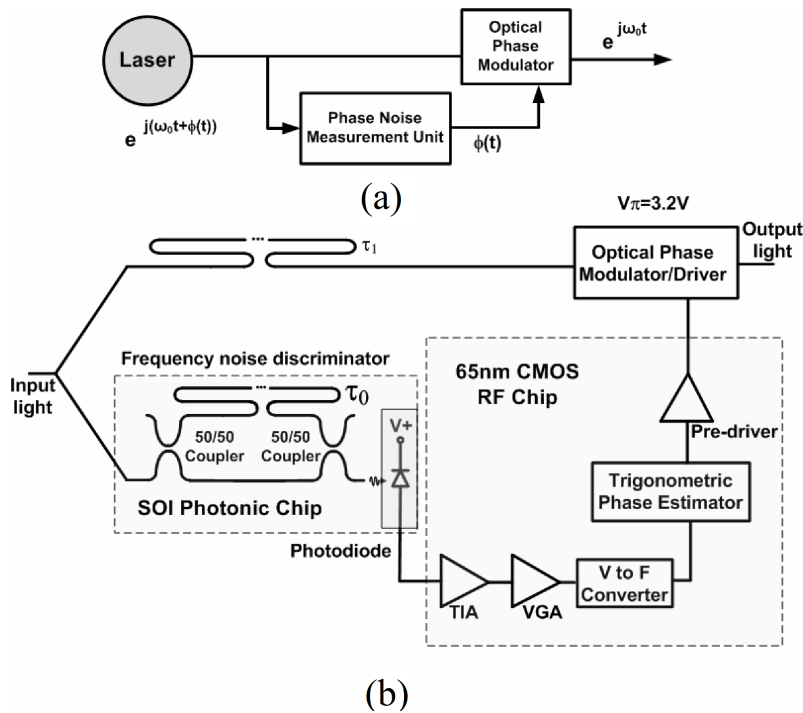


Figure 9.1: (a) The conceptual block diagram of a feed-forward laser phase noise reduction, and (b) the block diagram of the proposed phase noise reduction scheme.

properly conditioned signal, representing the source phase noise, $\phi(t)$. However, to obtain this proper $\phi(t)$, one must perform an ideal integration and appropriate scaling of the frequency noise signal generated by the frequency discriminator. Despite its conceptual simplicity, this task presents a significant practical challenge due to the unbounded nature of phase noise. This is because $\phi(t)$, essentially being the integral of white noise, closely follows a Brownian motion, whose variance increases linearly with time. Therefore, its corresponding voltage increases indefinitely with time and at some point either saturates the electronic circuitry or damages the off-chip OPM. As a result, an alternative non-saturating integration mechanism followed by a properly scaled phase wrapping process is required.

Electronic Quadrature Trigonometric Wrapping Integration

To overcome the challenging constraints imposed by the unbounded nature of $\phi(t)$, we propose a quadrature trigonometric wrapping integration scheme. This architecture is implemented in a CMOS RF chip, whose block diagram is shown in Fig. 9.2. The photo-current is received and amplified by an integrated trans-impedance amplifier (TIA) and converted to a voltage that is fed to a variable gain amplifier (VGA). The TIA is based on a regulated cascode structure.

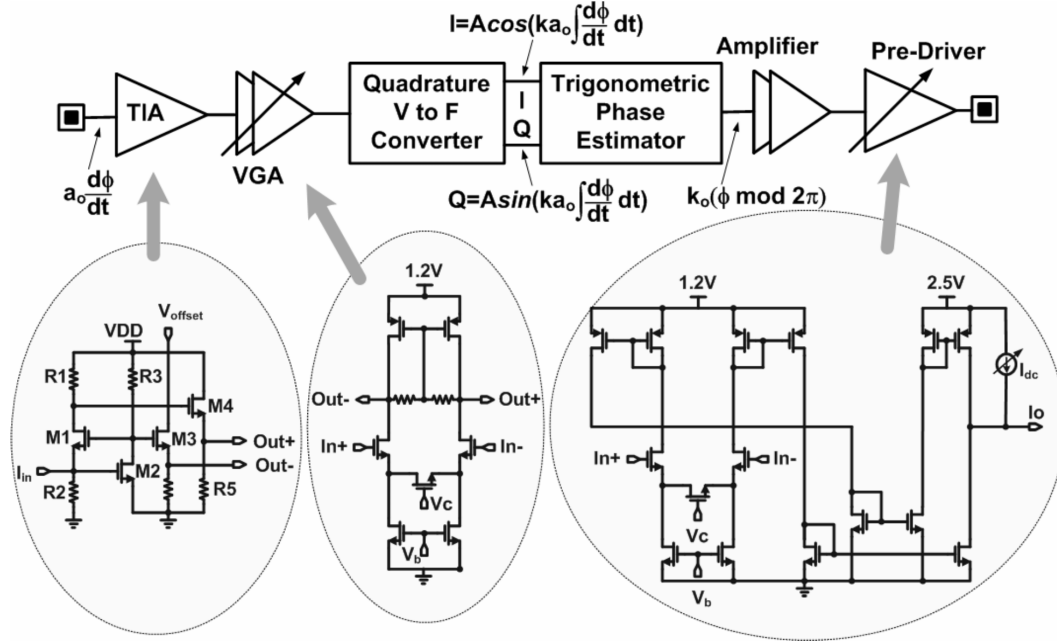


Figure 9.2: The block diagram of the proposed architecture implemented in a CMOS RF chip.

To achieve wrapping integration with proper scaling, a voltage-to-frequency converter followed by a trigonometric phase estimator block is used. Fig. 9.3 shows the block diagram of a direct V-to-F converter [59]. It consists of two loops. One loop converts voltage to frequency and the other loop adjusts the amplitude. Assuming ideal integrators and multipliers, the outputs of such a system can be written as

$$I_{out} = A \cos\left(\int v_{in} dt\right), \quad Q_{out} = A \sin\left(\int v_{in} dt\right) \quad (9.1)$$

This architecture emulates a VCO with a free-running frequency of zero. However, in a practical system with non-zero input offset, the center frequency of the V-to-F converter is nonzero. The schematic for the two integrators in Fig. XXX3 indicates that the integration is approximated by a low-pass filter created by lowering the output pole of an OTA. The amplitude restoration loop in the V-to-F converter brings the pole of this low-pass filter close to zero frequency, thus emulating an ideal integrator.

The trigonometric phase estimator takes the in-phase and quadrature signals generated by the V-to-F converter and calculates their phases. Its operation is based on the following robust phase approximation:

$$\phi \approx \frac{3.73 \sin(\phi)}{1.68 \cos(\phi) + \sqrt{\sin^2(\phi) + 4.5}} \quad (9.2)$$

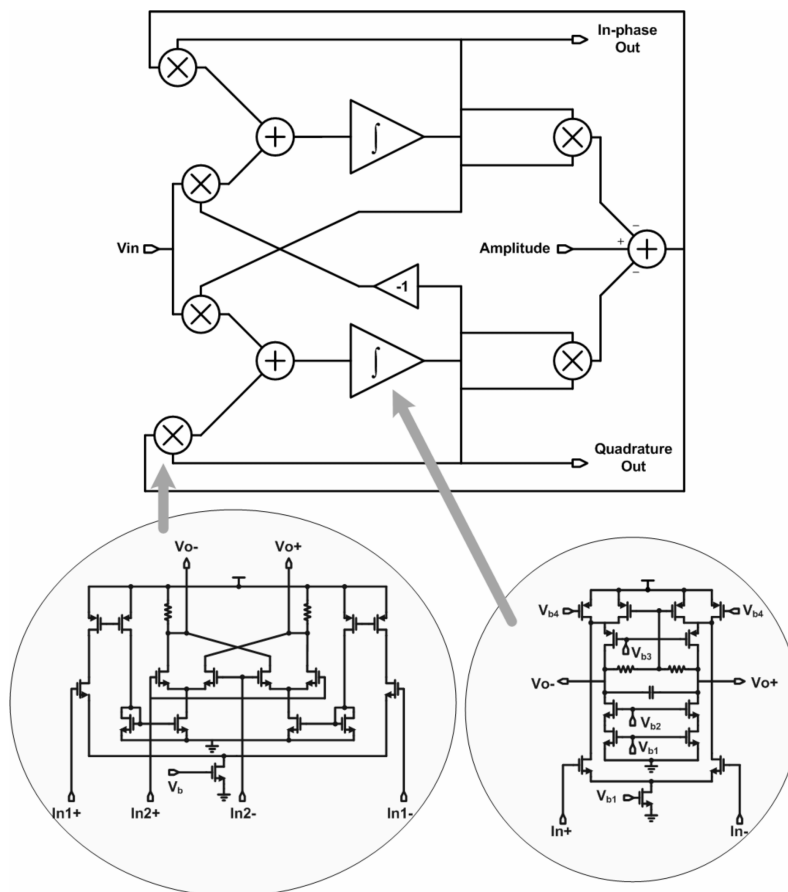


Figure 9.3: (a) The block diagram of a direct voltage-to-frequency converter, (b) the folded balanced Gilbert cell multiplier, and (c) the non-ideal integrator.

By using a simple sign detection scheme, Eqn. 9.2 can be used to estimate all values of $\phi \pmod{2\pi}$. One main advantage of this approximation is that it can be implemented using only three basic functions, namely, a current divider, a squarer, and a square-rooter. The circuit schematic of these blocks are depicted in Fig. 9.4. The operation of the squarer and square-rooter circuits is based on the assumption of long channel length transistors operating in pinch-off. The sum and difference of the drain currents of M2 and M8 are proportional to the square of the differential signal applied between the gates of M4 and M5, and the square root of the drain current of M1, respectively. The current divider is designed based on the trans-linear circuits principle described in [91].

The modulator pre-driver in Fig. 9.2 is a V-to-I converter with adjustable gain and output DC voltage level.

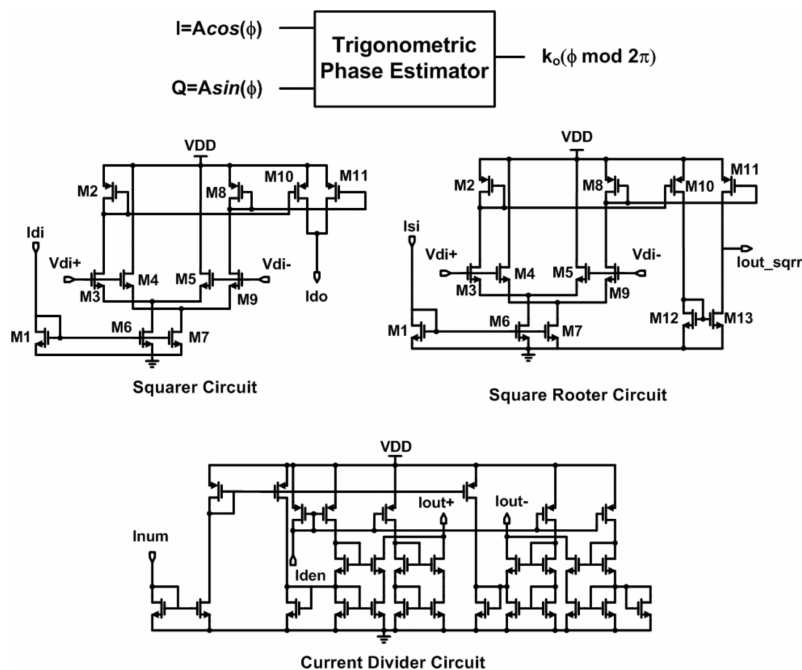


Figure 9.4: The schematics of the squarer, the square-rooter, and the current divider as the building blocks of the trigonometric phase estimator are shown.

Photonic Frequency Noise Discriminator

Figure 9.5 shows the integrated frequency noise discriminator implemented in IMEC SOI process with minimum feature size of 100nm. An integrated Mach-Zehnder interferometer (MZI) with delay difference of 400ps between its two arms is used to create interference between the coupled light and its time delayed version. This MZI is formed using SOI waveguides with 500nm width and 220nm heights. The directional couplers at the input and output are designed as a 50/50 power splitter/combiner. The output of the MZI is backside-coupled to a photodiode forming a frequency noise discriminator. Grating couplers with loss of about 3dB are used as optical pads.

Measurement Result

Figure 9.22 shows the micro-photograph of the RF chip fabricated in a 65nm CMOS process and the hybrid integration with photonic SOI chip (with 100nm minimum feature size) and the photodiode.

First, by coupling the output of a conventionally available DFB laser emitting 10mW optical power at 1553nm to the photonic chip the response of the photonic frequency noise discriminator is measured. Figure 9.7 shows the frequency spectrum of the

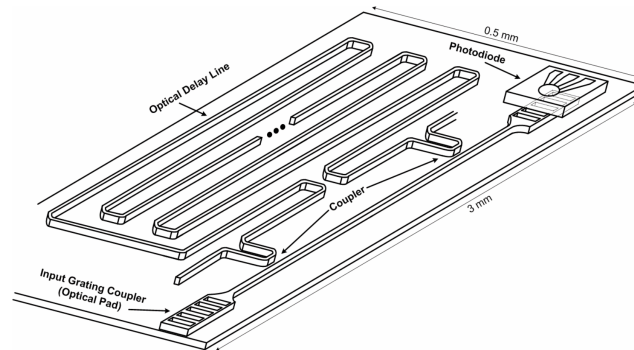


Figure 9.5: The integrated frequency noise discriminator implemented in IMEC SOI process.

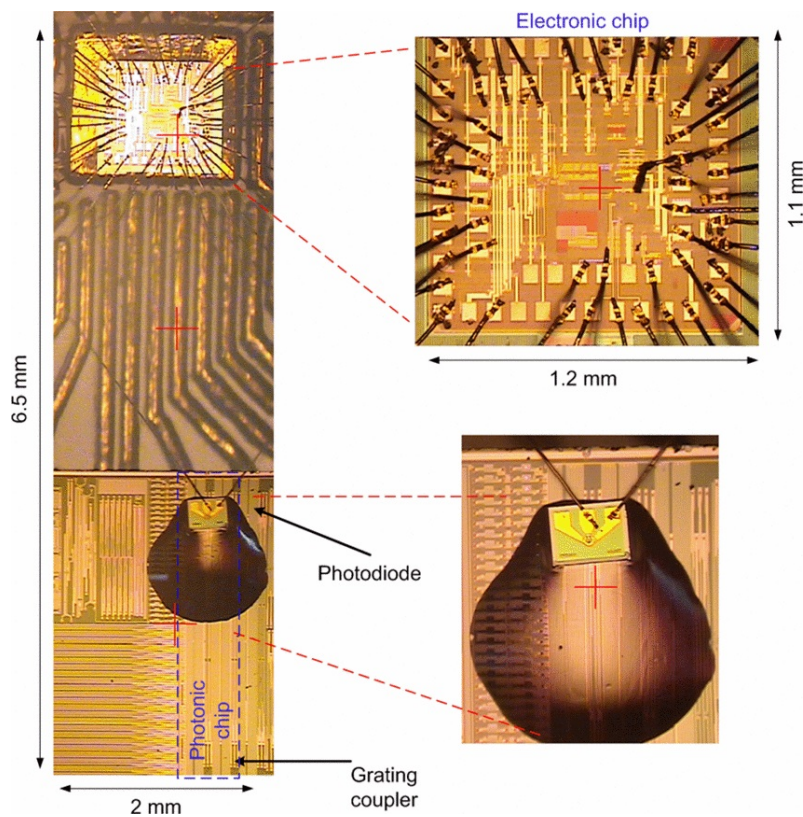


Figure 9.6: The micro-photograph of the RF chip (fabricated in a 65nm CMOS process) and the hybrid integration with photonic SOI chip (with 100nm minimum feature size) and the photodiode.

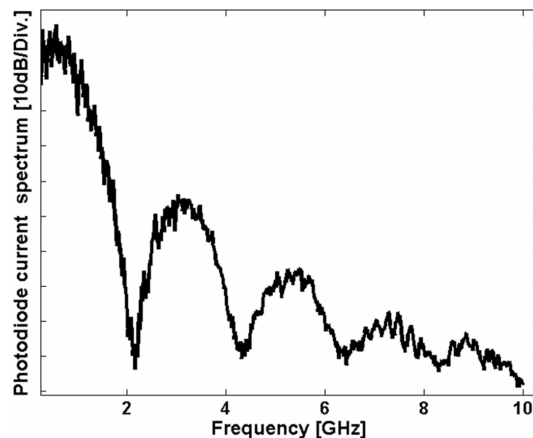


Figure 9.7: The output frequency spectrum of the photonic frequency discriminator chip.

photodiode current after electrical amplification. The response follows closely the behavior predicted in [14] and the null-spacing in the response represents 400ps of delay difference between MZI arms.

Figure 9.8(a) shows the measurement setup for the standalone RF chip. A noise source in conjunction with a $5k\Omega$ resistor at the chip input provides a current noise with $10\mu A$ amplitude to the RF chip. This noise level is in the same order as the typical DFB laser discriminated frequency noise. The output of the RF chip pre-driver is captured using a real-time oscilloscope. As shown in Fig. 9.8(b), the input noise and the ideal derivative of the output (after about 4ns delay adjustment) are in close agreement suggesting a close-to-ideal integration performed by the RF chip. The phase wrapping process can also be observed from the zoomed-in version of the pre-driver output.

Figure 9.8(c) shows the phase noise reduction measurement setup. The output of the OPM is down-converted to electrical domain by beating it with a tunable laser (with a linewidth less than 50kHz) and monitoring the heterodyne spectrum. The heterodyne laser spectrum before and after phase noise reduction was measured, as depicted in Fig. 9.8(d). This measurement shows that the original linewidth of the laser is reduced from 6MHz to 250kHz, which is equivalent to approximately 14dB improvement in the phase noise. The performance of this work is compared with that of a few published works in Table 9.1.

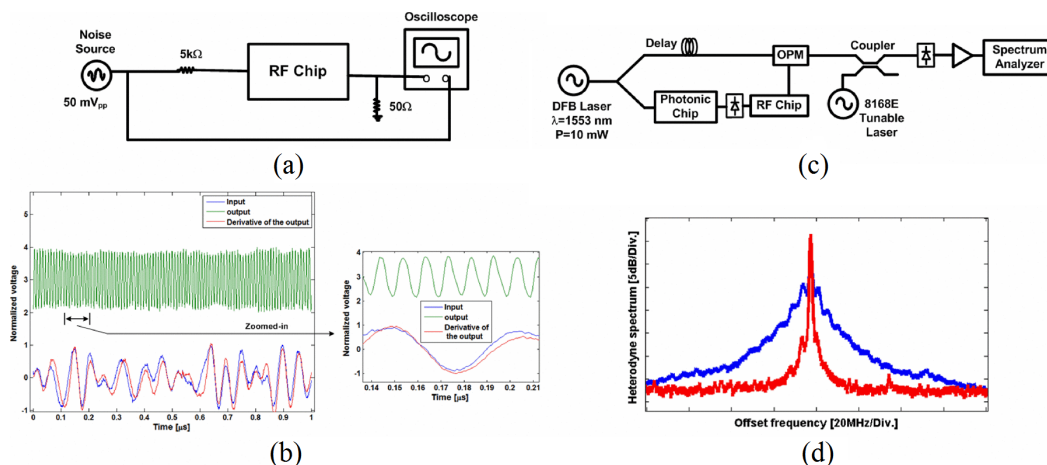


Figure 9.8: (a) The RF chip stand-alone measurement setup, (b) the measured integration and wrapping performance of the RF chip, (c) the laser phase noise reduction measurement setup, and (d) the measured laser spectrum before and after phase noise reduction.

Ref.	Laser Type	Phase Noise Reduction BW	Linewidth (Orig. - Reduced)	Power Consumption	Area	Method
[158]	External Cavity	<1MHz	100KHz - 1Hz	N/A	Bench-top	Electrical feedback
[14]	DFB	330MHz	2.6MHz - 160KHz	>30W	Bench-top	Feed-forward
[13]	DFB	200MHz	7.5MHz - 1.8KHz	>25W	Bench-top	Feed-forward
This Work	DFB	200MHz	6MHz - 250KHz	160mW	Electronic chip: 1.32 mm ² Photonic chip: 1.5 mm ²	Feed-forward

Table 9.1: Performance summary and comparison with other works

9.2 Electro-optical mm-Wave Power Generation and Radiation

There is a growing demand for compact and cost-effective generation of mm-wave and sub-mm-wave electromagnetic (EM) radiation with growing applications in communication, imaging, sensing, and ranging. Two candidates are the all-electrical approach in low cost silicon-based electronics (e.g., [37],[150],[184]) and optoelectronic mixing of two signals with close wavelengths. In either case, the coupling of electromagnetic energy from an on-chip generation source to the desired radiative mode is challenging due to substrate modes at those frequencies, making it necessary to use bulky and expensive external components (e.g., a silicon lens). Recent development of multi-port driven (MPD) [37] and distributed active radiators (DAR) [150] on the electronic generation of the signal have led to new methods for efficient generation and radiation of mm- and sub-mm-waves from on-chip radiators on a small silicon substrate without an external lens. Similar approaches can be used to

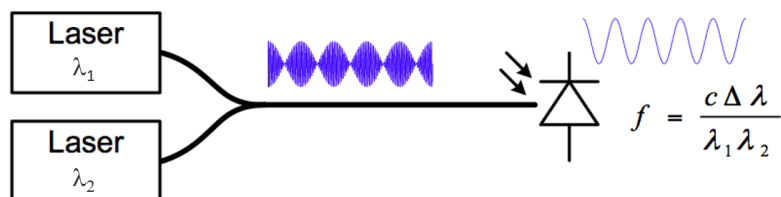


Figure 9.9: Optoelectronic mm-Wave generation.

produce a compact silicon based optoelectronic source of sub-mm and THz signals.

Figure 9.9 shows the concept of optoelectronic RF and mm-Wave generation. In this scheme, light with two wavelengths are combined via a photodiode (PD) to produce an output at a mm-wave radio frequency (RF) at their frequency difference in the electrical domain that feeds an antenna. This technique has been used with traditional single-port antennas using external silicon lenses either in a hybrid approach or on non-silicon substrates [122],[121].

An optically driven MPD approach can overcome some of the challenges faced by an all-electronic approach, such as the limited frequency tuning range (often a few GHz or lower), higher phase noise (leading to higher bit error rate or reduced image resolution.), power loss in routing of signals and producing necessary phase shifts in an MPD due to the high attenuation of on-chip electrical transmission lines, as well as cross-talk between transmission lines and the radiating antennas, all of which forces the antenna performance away from its optimum. At the same time, it can be used to produce compact sources without the need for an external lens or antennas, benefiting from the best of both worlds. This is particularly conducive to integrated silicon photonics where the saturated current per diode can be small, making it necessary to divide the optical power and send it to multiple diodes to achieve higher RF power, where an efficiency distributed power combining strategy is a must. The radial multi-port driven (MPD) antenna enables this use of multiple driving PD's and performs impedance matching, power combining and radiation through a single structure [37]. A cohesive co-design of the photonic, electronic, and electromagnetic structures enables greater performance by minimizing loss due to power combining, impedance matching, and power transfer.

Radiator Design

The optical MPD radiator consists of a radial MPD antenna, the PD drivers, and an on-chip optical distribution network implemented on a silicon photonics process. The

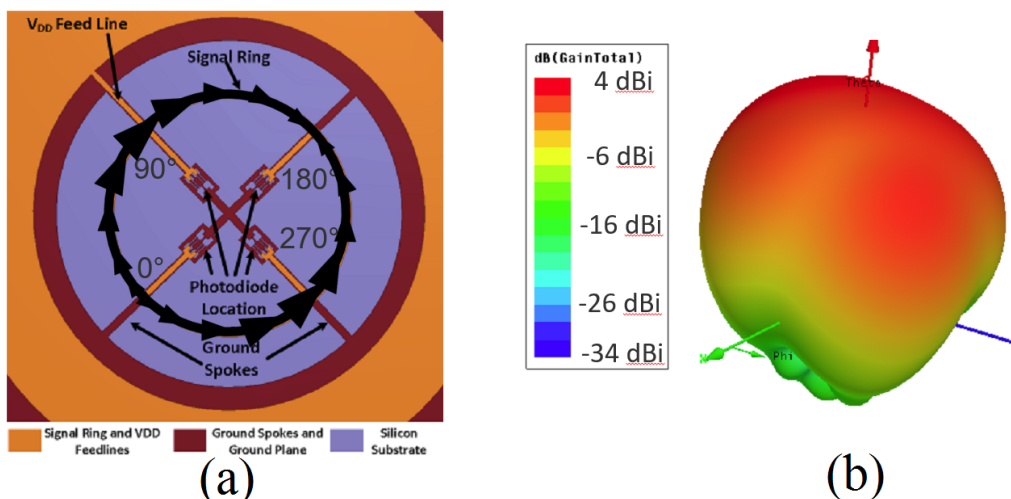


Figure 9.10: (a) Multi-port radiator with traveling wave current overlay and (b) associated radiation pattern with silicon substrate at 180GHz

silicon-on-insulator (SOI) process uses a $2\mu\text{m}$ buried oxide, and a metal stack with 2 layers [76]. The radial MPD antenna is made up of a signal ring that is driven by a pair of PDs at four points against a pair of radially oriented ground ‘spokes’. When the currents produced by the PDs are at the correct phase (0° , 90° , 180° , and 270°), they create a traveling current wave around the signal ring and quadrature phased standing waves along the ground spokes that produce a circularly polarized radiated field as seen in Fig. 9.10(a).

The waveguides are implemented as strip waveguides that are $0.5\mu\text{m}$ wide and $0.22\mu\text{m}$ thick. To create the phase shift in the RF signal, the lengths of the optical waveguides are staggered. The phase of the beat signal is dependent on the difference in phases of the optical signals. This means that the physical length of the delay is on the order of the RF wavelength, not the optical wavelengths, and thus mismatch in phase due to process variation or thermally induced index change is decreased by three orders of magnitude ($\Delta f/f$), and each 90° phase delay is $82\mu\text{m}$. This delay in the waveguide has a simulated loss of 0.01 dB, much less than the loss of a 90° phase delay produced electrically at these frequencies.

The optical signal is coupled into the chip using a grating coupler with loss of 3-4 dB and is split into four signals using two stages of Y-junction dividers. The silicon waveguides are small enough compared to the wavelength of the RF signal that they have a negligible effect on antenna performance once the signal is converted into the electronic domain, and thus can be routed independently of the antenna design, an

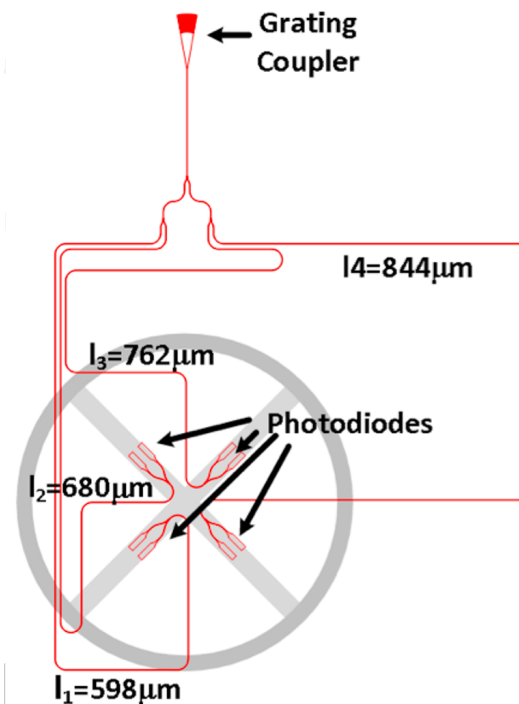


Figure 9.11: Layout of optical multi-port driven radiator's optical distribution network.

advantage of having the input distribution in a different domain from the radiation. The waveguides are routed to the four drive points of the antenna and are split once again with a Y-junction divider just before the diodes, as can be seen in Fig. 9.11.

By sizing the ring just larger than one wavelength in circumference, the traveling wave on the ring will have a 180° phase shift as it travels half way around the ring, and will have a 180° change in direction due to the curvature of the ring. This means that at any instant, there will be two maximum currents on the ring at opposite sides that are pointed in the same direction, and these two maxima then rotate around the ring creating the circular polarization. While the currents on the spokes produce standing waves that on their own would be linearly polarized, the phase of the currents on the two orthogonal spokes are in quadrature, so the radiation produced by the currents on the spokes is also circularly polarized, and with correct sizing will be close to in phase with the fields radiated from the ring. The ground spokes connect to an outer ground plane that is pulled back $\lambda/4$ from the ring, which helps to minimize coupling to the substrate modes, and directs most of the current on the ground spokes through the middle of the radiator. The DC power for the diodes is supplied through the signal ring on a $\lambda/4$ transmission line that produces a high

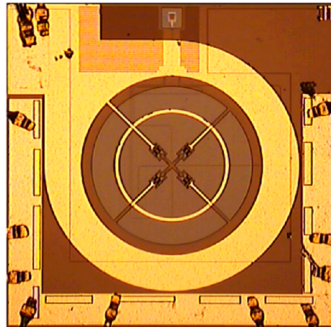


Figure 9.12: Die photo of the fabricated optoelectronic radiator.

impedance looking outward from the ring, thus minimizing the transmission line's effect on the radiation. The simulated radiation pattern of the antenna using Ansoft HFSS FEM solver is shown in Fig. 9.10(b). It shows a single beam that is fairly wide, which is desirable for a single element of an integrated radiator. This means that the element can be placed in a phased array in the future with a large beam steering range.

The 8 photodiodes have a simulated 3dB bandwidth of 25 GHz, limited by the junction capacitance. While the RF power produced by the photodiodes drops above this frequency, the photodiode can still operate at much higher frequencies at lower power levels. The dimensions of the antenna are chosen to maximize output power of the PDs by providing an input impedance near the optimal match.

Measurement results

The chips (Fig. 9.12) were mounted on a PCB and optically probed, with wire-bonds providing DC biasing. The optical signal was created by combining output from a tunable laser (HP8168E) with the output from a distributed feedback (DFB) laser (NEC NX8562L), both operating in C band. that is then amplified with an EDFA. The optical power going into the optical probe is 750 mW. The radiated signal is received with a WR-5 22dB gain linearly polarized horn antenna located 6cm from the chip that feeds an 11th harmonic mixer. The down-converted signal is amplified and measured with a spectrum analyzer, as shown in Fig. 9.13. The harmonic mixer is calibrated against a calorimeter based Erikson power meter (PM4). The PDs have a reverse bias of 3V, and a photocurrent of 45mA. The calibrated spectrum at 180 GHz is shown in Fig. 9.14(a), and shows a broadside effective isotropic radiated power (EIRP) of -9.7 dBm. The linearly polarized receive antenna was rotated in the plane parallel to the chip to verify the chip's radiation is circularly polarized.

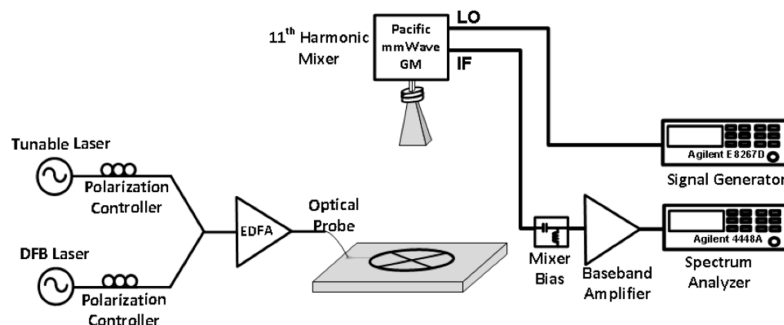


Figure 9.13: Measurement setup.

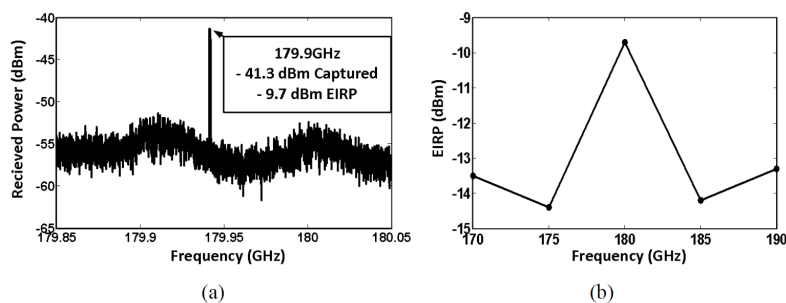


Figure 9.14: Calibrated spectrum of the measured broadside radiation at 180 GHz (a), and measured frequency response of the effective isotropically radiated power (EIRP) in the broadside direction (b).

The broadside EIRP is plotted versus frequency in Fig. 9.14(b), and shows EIRP greater than -15 dBm from 170 GHz through 190 GHz.

Conclusion

A 180 GHz optically driven MPD radiator implemented in an integrated silicon photonics process was demonstrated to highlight the benefits that optical integration can have on integrated radiators as well as the benefits of a coordinated co-design of photonic, electronic and electromagnetic blocks within the radiator.

9.3 Breaking the Bandwidth/Quality-Factor Trade-off in Optical Ring Resonators

Improving bandwidth-density product in fully integrated silicon photonic systems necessitates a corresponding enhancement in modulator performance. Ring resonator modulators are promising candidates to realize compact, high-speed, and low-power silicon photonic transceivers [170]. Intensity modulation is commonly achieved by index modulation or coupling modulation. It is desirable to have high-Q rings as, for a given extinction ratio, higher Q results in better energy efficiency.

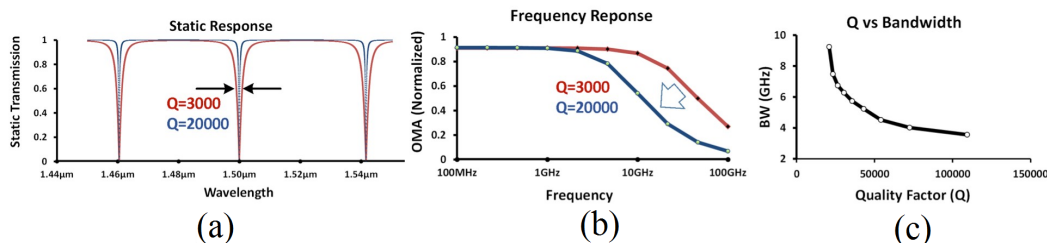


Figure 9.15: Index-modulated ring's (a) static transmission (b) optical frequency response (c) simulated Q vs -3dB bandwidth

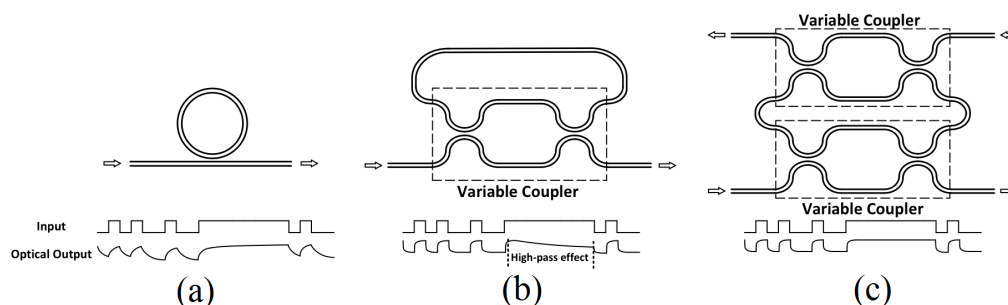


Figure 9.16: (a) Index-modulated ring (b) Coupling-modulated ring (c) Proposed differential ring modulator

However, there is a trade-off between Q of the ring resonator modulator and its optical bandwidth. As previously shown [144], the time domain dynamic transmission of the ring, $T(t)$ can be written as

$$T(t) = \sigma(t) + \frac{\kappa(t)}{\kappa(t - \tau)} a(t) e^{-j\phi(t)} [\sigma(t - \tau) T(t - \tau) - 1] \quad (9.3)$$

where σ and κ are transmission and coupling coefficients, a is the attenuation, ϕ is the phase shift inside the ring and τ is the resonator round trip.

Fig. 9.15 shows numerical solution of equation 9.3 using an iterative approach. The Q-bandwidth trade-off in an index-modulated ring is shown in Fig. 9.15 (b) and (c), which results in the low-pass response for the index-modulated ring of Fig. 9.16 (a). Conversely, a high-pass response can be obtained using the coupling modulated ring of Fig. 9.16 (b), with a sufficiently fast variable coupler. In this case, a long sequence of 1's causes energy droop in the ring and signal degradation (Fig. 9.16 (b)). We propose a differential ring modulator that overcomes the Q-bandwidth trade-off in ring modulators (Fig. 9.16 (c)). This structure does not exhibit droop in energy stored in the ring.

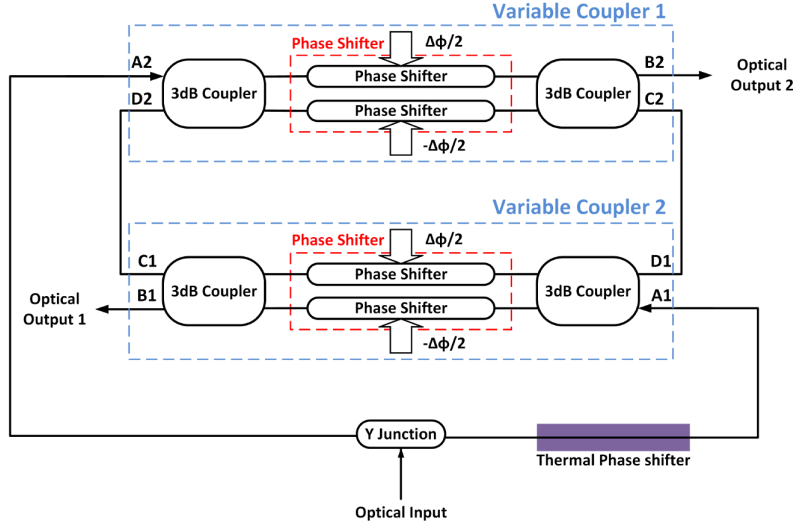


Figure 9.17: Block diagram of the differential ring modulator

Proposed Modulator Structure

The block diagram of the proposed structure (shown in Fig. 9.17) consists of two variable couplers [143], each of which consists of two differential phase shifters and two 3dB couplers. A Y-junction with a controllable thermal phase shifter is used to split the input beam into two beams with the same phase (A_1 and A_2). The variable couplers operate out of phase and when coupling of one increases the other decreases. The proposed DRM achieves considerably lower V_π compared to a regular MZI modulator. Considering the electric field at various locations in the DRM, it can be shown that at resonance the static transmission is

$$\left| \frac{B_1}{A_1} \right|^2 = \frac{\left(a - \left| \cos \frac{\Delta\phi}{2} \right| \right)^2}{\left(1 - a \left| \cos \frac{\Delta\phi}{2} \right| \right)^2} = \frac{\left(a - \left| \cos \left(\frac{V}{2V_\pi} \pi \right) \right| \right)^2}{\left(1 - a \left| \cos \left(\frac{V}{2V_\pi} \pi \right) \right| \right)^2} \quad (9.4)$$

where a is the loss factor and V_π is the voltage required to achieve a differential phase shift of π in phase shifters. Critical coupling (where maximum extinction ratio is achieved) happens when

$$V_{\pi, DRM} = \frac{2}{\pi} V_\pi \cos^{-1}(a) \quad (9.5)$$

Therefore, for a Q of 32,000, $V_{\pi, DRM}$ is 8 times smaller than V_π . The DRM structure maintains the energy stored in the ring constant in all conditions. This can

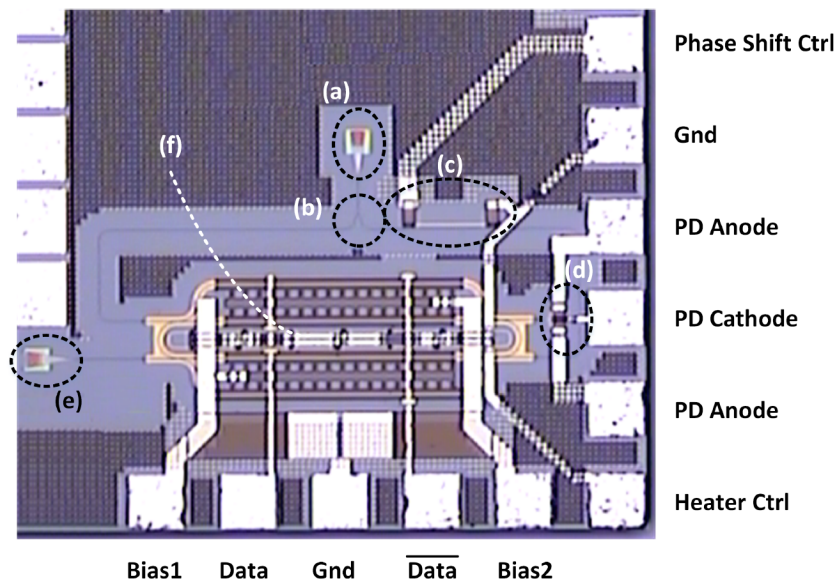


Figure 9.18: Die micrograph of the fabricated prototype and measurement setup. (a) Optical input grating coupler (b) Y-junction (c) heater for phase shift controller (d) photodiode connected to one output for testing purposes (e) Optical output grating coupler

be demonstrated by calculating the amplitude of C_1 and C_2 (shown in Fig. 9.17) when data switches from 1 to 0 (Equation 9.6).

$$|C_1|^2 = |C_2|^2 = \sin\left(\frac{\Delta\phi}{2}\right) \times \frac{1 + \frac{a^2}{4} \cos^2 \frac{\Delta\phi}{2}}{1 - \frac{a^2}{4} \cos^2 \frac{\Delta\phi}{2}} \quad (9.6)$$

Intuitively, by modulating the couplers differentially, the overall coupling to the ring remains constant. Thus, the variation of energy stored in the ring is minimized.

Measurements

A prototype chip has been fabricated in OpSIS IME platform [181] and occupies less than 0.35mm^2 (Fig. 9.22). Grating couplers are used for optical input and output. A heater is placed at in the center of the ring for uniform distribution of temperature. A second heater is placed at one of the Y-junction's branches to calibrate phase mismatch between the two inputs of the ring. The second output of the ring is connected to an on-chip photodiode for testing. The chip was wire-bonded to a custom designed PCB that carries high-speed, and DC signals. A tunable laser source followed by an EDFA was used as the input and the output was monitored by an optical sampling scope. The high-speed differential data signals were driven

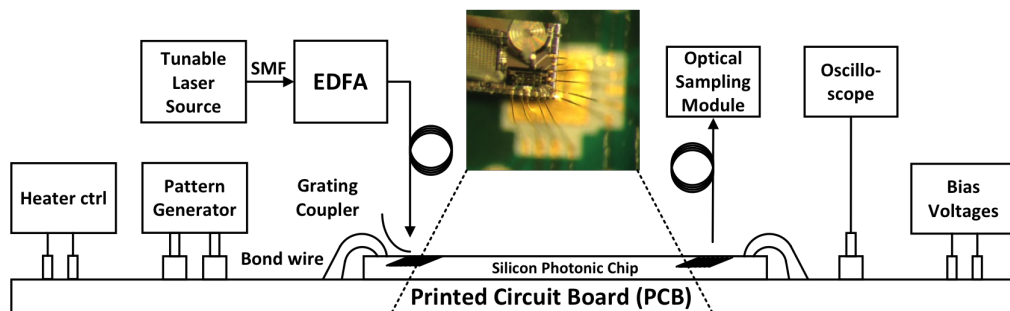


Figure 9.19: Measurement setup

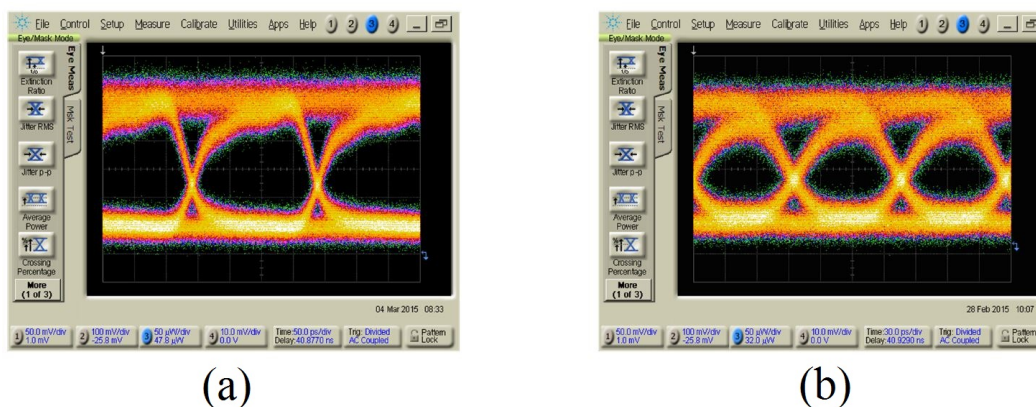


Figure 9.20: Output eye diagram of the differential ring modulator opening at (a) 5Gbps (b) 10Gbps

by a PRBS 31 sequence using a pattern generator. The voltage swing for each single-ended signal was 1.75V p-p. Fig. 9.20 shows measured eye diagrams at the output for 5Gb/s and 10Gb/s data streams. The extinction ratio of the output optical data is measured to be 6.2dB. Some of the noise seen at the output is associated with the EDFA noise and limited sensitivity of the optical sampling scope. Fig. 9.21 (a) shows measured static transmission of the ring near one operational wavelength bias points. From this measurement, varying the input voltage of the heater, and was measured to be 12.3pm/mW.

Conclusions

A differential ring modulator structure is presented that breaks the optical bandwidth/quality factor trade-off known to limit the speed of high-Q ring modulators. This structure maintains the total energy stored in the ring constant, unlike coupling modulation schemes, and hence the ring does not suffer from power droop when



Figure 9.21: (a) Measured steady-state transmission of the ring near a notch (b) tunability of the ring

long sequences of 1's or 0's are transmitted. A prototype has been fabricated and 10Gb/s operation of the ring is demonstrated.

9.4 Reducing Mach-Zehnder Interferometer Footprint

High-speed traveling wave Mach-Zehnder interferometers (MZI) are widely used in optical communication networks for optical signal modulation. Typical traveling wave structures use linear transmission line structures that are a few millimeters long [29, 65], and as a result the reported MZI structures have high aspect ratios and consume a large silicon area. This poses a challenge in using MZI modulators in silicon photonic ICs where the cost needs to be minimized. Also, a long aspect ratio prevents integration of the MZI in smaller photonic chips where the maximum dimensions of the chip are constrained. We propose a spiral MZI modulator that achieves a low aspect ratio for a long modulation length by wrapping the straight transmission lines and waveguides into a spiral shape. Figure 9.22 shows the die-photo of the proposed spiral MZI. The input and output ports of the MZI are located outside of the spiral so that the structure can be used in more complex photonic circuits. The P and N type doped regions are laid one after the other on a 90nm silicon slab layer while the 220nm optical waveguide is located on the diode junction. The PN junction forms a carrier-depletion mode phase shifter on each arm of the MZI operating in a push-pull fashion. The partial cross section of the MZI structure for two turns of the spiral is shown in Figure 9.23. The electrical signal travels through a co-planar transmission line that is capacitively loaded by the junction capacitance of the phase shifter. This capacitive loading reduces the propagation speed of the electrical signal which helps to reduce the velocity mismatch between the electrical and optical propagation waves. As it can be seen in the cross section,

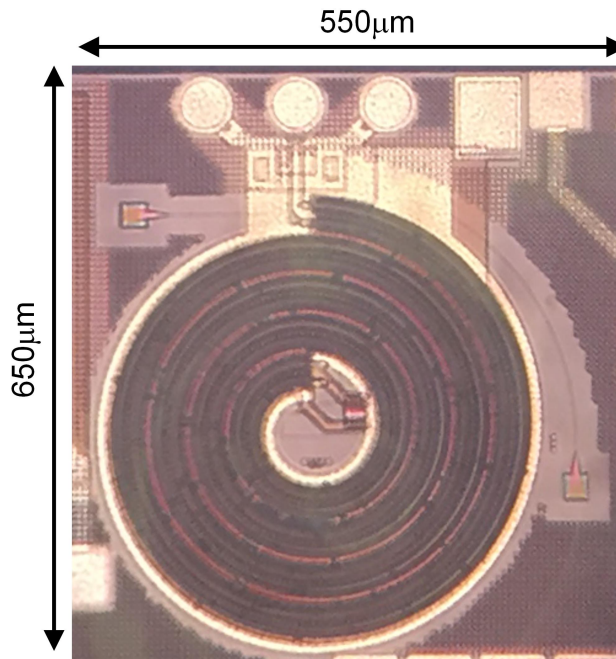


Figure 9.22: Die photo of spiral MZI modulator

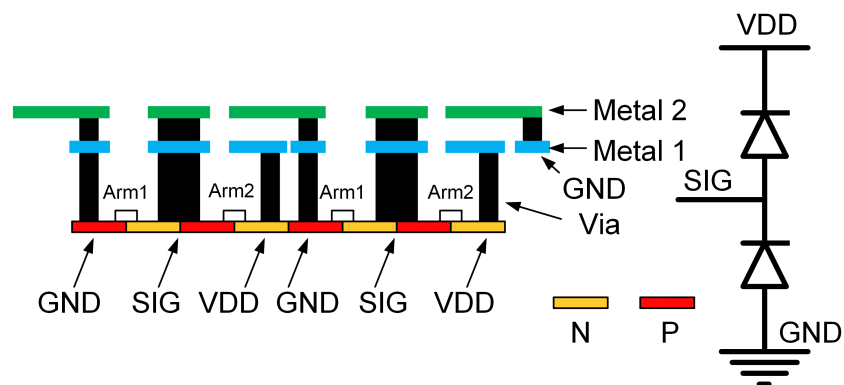


Figure 9.23: Partial cross section of the MZI structure. The spiral MZI allows for a push-pull operation of the phase shifters

the signal line is shielded by two ground planes on the side, so that the cross talk between the turns of the MZI is minimal. The ground plane is extended over the VDD trace to provide a bypass capacitor on the VDD line and minimize the voltage ripples on the VDD line. The end of the transmission line is terminated with an on chip 50 ohm termination.

The chip was fabricated on an IME process through OPSIS. The fabricated test chip shown in Figure 9.22 fits two 3mm long phase shifters in an area of 550x650μm². The measurement setup used to characterize the bandwidth of the modulator is shown in

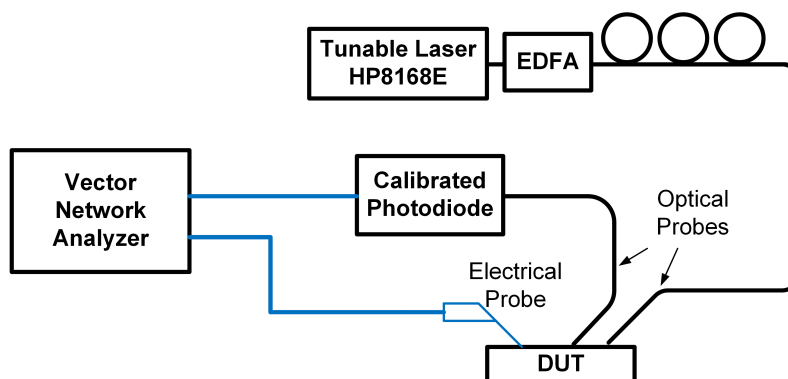


Figure 9.24: Measurement setup for characterizing the modulator Bandwidth

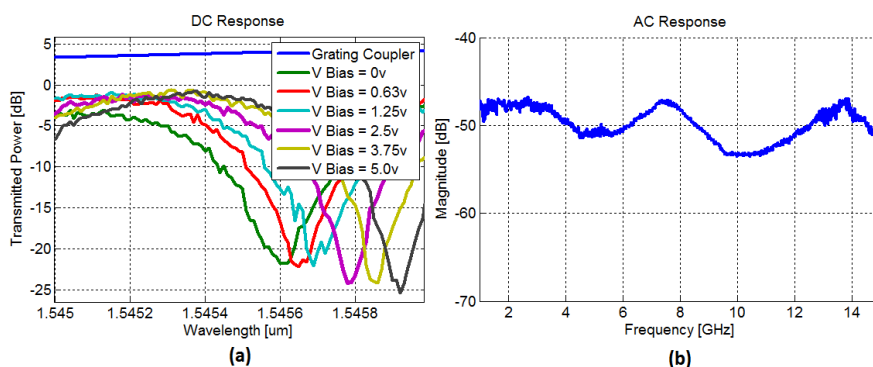


Figure 9.25: (a) Measured DC response of the modulator (b) Measured frequency response of the modulator

Fig. 9.24. The network analyzer was first calibrated for the loss of the cables. The network analyzer drives the MZI through electrical probes. The resulting modulated laser light is converted back to electrical signal via a 30GHz calibrated photodiode (Optilab PD-30) and is read by the network analyzer.

The DC response of the modulator is shown in Figure 9.25(a) with $V_{\pi}L = 2.27V\text{-cm}$. The measurement frequency response is shown in Figure 9.25(b). The 3dB bandwidth of the modulator is 9GHz. The non-flat frequency response can be attributed to the mismatch between the MZI transmission line impedance and the on chip load termination. Using the designed MZI we demonstrate the 12.5Gbps modulation eye diagram in Figure 9.26(a), and the 20Gbps modulation eye diagram in Figure 9.26(b).

9.5 Improving Photodiode Bandwidth and Power Capability

Photodiodes are responsible for conversion of optical signals to electrical domain. Among the properties of the photodiodes the most important factors are their band-

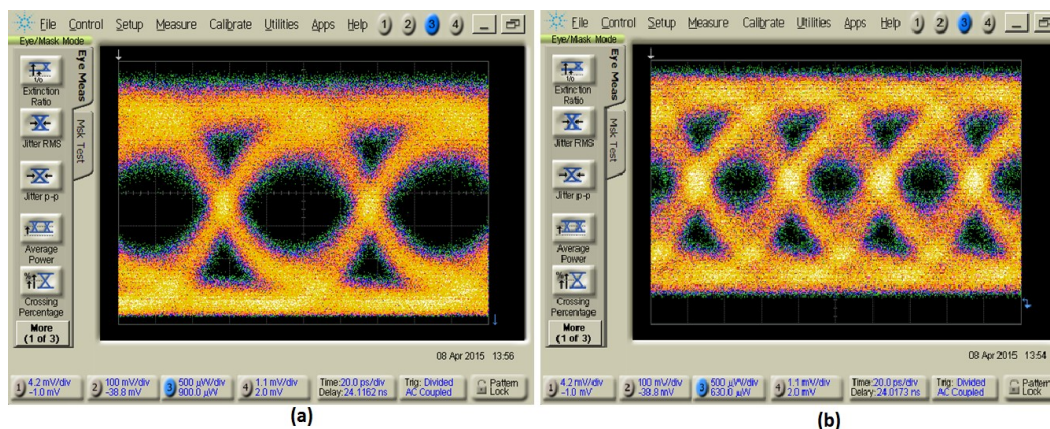


Figure 9.26: (a) 12.5Gbps eye diagram, (b) 20Gbps eye diagram.

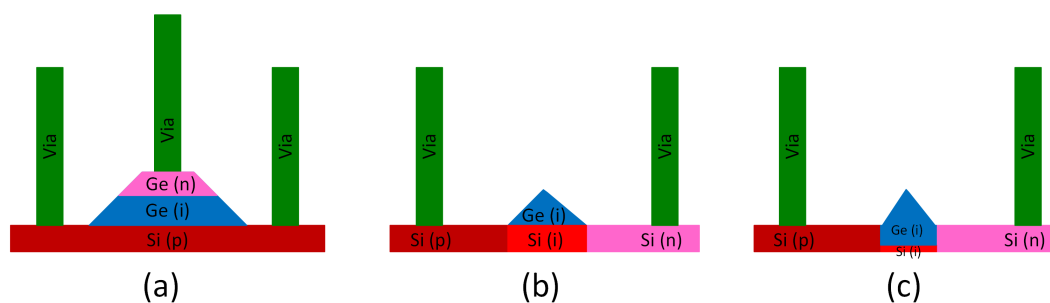


Figure 9.27: (a) Vertical PD provided in IME design kit. (b) Lateral PD utilizing self stop property of Ge growth. (c) Proposed lateral PD with reduced transit time due to increased overlap of junction electrical field and generated free carriers

width, power handling and sensitivity (dynamic range). Low dark photodiode are desirable for lower shot noise and high power photodiodes are desirable for mm-Wave generation. In some applications where the optical link budget is not tight and there is enough optical power available at the receiver, a high power photodiode may be able to directly drive the electronic circuitry without a TIA. In this section I will describe a traveling wave photodiode structure, compatible with typical SiP foundry processing with Ge which allows for both high power and high bandwidth of operation.

The photodiodes that come with the design kit library of IME process are of the vertical structure as shown in Fig. 9.27(a) [126]. These photodiodes suffer from a large dark current of 3 μ A and low responsivity due to absorption of photons by the metallic contact interface on the germanium. To improve the responsivity of the photodiodes, lateral diodes with no metal contact on the germanium was proposed by [182]. The cross section of the diode is shown in Fig. 9.27(b). Due to crystal

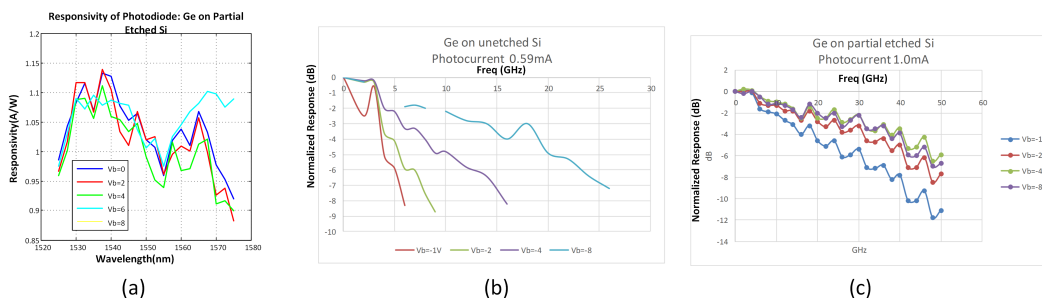


Figure 9.28: (a) Measured responsivity of proposed PD for different reverse bias voltages. (b) Frequency response of PD on unetched Si for photocurrent of 0.6mA. (c) Frequency response of proposed photodiode for photo current of 1.0mA.

growth orientation, localized epitaxial layer of Ge has a sidewall angle of 25° . If the base layer of Ge has less than $1\mu\text{m}$ width, germanium top will have zero width and a pyramid shape is obtained. The light entering this photodiode will be confined in a single mode in the Ge layer and since there is no metal contacts, all the absorbed photons will generate free carriers. [182] observed an order of magnitude lower dark current for these photodiode, however, the photodiodes demonstrated transit time limited bandwidth which improves with increasing the reverse bias. The increased transit time is attributed to both larger width of junction ($1\mu\text{m}$ as opposed to 500nm in the vertical structure) and lower electric field intensity as only the fringe of the electrical field overlaps with the germanium, where the carriers are generated.

In order to improve the transit time the structure shown in Fig. 9.27(c) is proposed. In this structure, the germanium is grown in the partially etched silicon and is fully enclosed by the silicon. This allows for stronger overlap of electrical fields with carrier generation site in germanium. The width of the germanium was also reduced to $0.5\mu\text{m}$ to reduce the transit time. One side effect of smaller width (and as a result smaller height) is lower confinement of optical mode in Ge. As a result a longer PD is needed to absorb most of the photons. This increases the junction capacitance but allows for higher optical power handling of the photodiodes as the optical power is absorbed over a longer distance and charge space screening appears at higher optical powers.

To evaluate the proposed photodiodes, two identical layout of photodiodes were submitted for fabrication. In one of them the germanium was grown on unetched silicon and in the other the germanium was grown on partially etched silicon. Both photodiodes showed similar dark current of around 10nA at 4V reverse bias; however, the proposed photodiode on partial etched silicon demonstrated superior bandwidth

and photocurrent capability compared to the photodiode on the unetched silicon.

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