DESIGN AND STABILITY ANALYSIS TECHNIQUES FOR SWITCHING-MODE NONLINEAR CIRCUITS: POWER AMPLIFIERS AND OSCILLATORS

Thesis by

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Abstract

A design technique for kW-level switching-mode power amplifiers is presented. Several push-pull pairs, independently tuned to Class-E/F_{odd}, are combined by a distributed active transformer. The zero voltage switching (ZVS) condition is investigated and modified for the Class-E/F_{odd} amplifier with a non-ideal output transformer. All lumped elements including the DAT, the transistor package, and the input-power distribution network are modeled and optimized to achieve the ZVS condition and the high drain efficiency. Two power amplifiers are implemented at 29 MHz, following the technique. The amplifier with two push-pull pairs combined exhibits 1.5 kW output power with 85 % drain efficiency and 18 dB gain. When four push-pull pairs are combined, an output power of 2.7 kW is achieved with 79 % drain efficiency and 18 dB gain.

Nonlinear stability analysis techniques, based on an auxiliary generator and pole-zero identification, are introduced to predict and eliminate the instabilities of power amplifiers. The techniques are applied to two switching-mode power amplifiers that exhibited different instabilities during the measurements. Self-oscillation, chaos, and hysteresis of a Class-E/F_{odd} amplifier with a distributed active transformer are investigated by the stability and bifurcation analysis tools. An in-depth analysis of the oscillation mechanism is also carried out, which enables an efficient determination of the topology and location of the required global stabilization network. As the other application, the anomalous behavior observed in a Class-E power amplifier is analyzed in detail. It involves hysteresis in the power-transfer curve, self-oscillation, harmonic synchronization, and noisy precursors. To correct the amplifier performance, a new technique for elimination of the hysteresis is proposed, based on bifurcation detection through a single simulation on harmonic-balance software. Also investigated are the circuit characteristics that make the noisy precursors observable in

practical circuits and a technique is derived for their elimination from the amplifier output spectrum. All of the stabilization and correction of the amplifiers are experimentally validated.

A simple nonlinear technique for the design of high-efficiency and high-power switching-mode oscillators is presented. It combines existing quasi-nonlinear methods and the use of an auxiliary generator in harmonic balance. The auxiliary generator enables the oscillator optimization to achieve high output power and DC-to-rf conversion efficiency without affecting the oscillation frequency. It also imposes a sufficient drive on the transistor to enable the switching-mode operation with high efficiency. The oscillation start-up condition and the steady-state stability are analyzed with the pole-zero identification technique. The influence of the gate bias on the output power, efficiency, and stability is also investigated. A Class-E oscillator is demonstrated using the proposed technique. The oscillator exhibits 75 W with 67 % efficiency at 410 MHz.

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Chapter 1

Introduction

The tremendous expansion of wireless communications in the 21st century pushes the performance of each component of communication systems to more and more stringent specifications. In power amplifiers, the performance issues include efficiency, linearity, output power, and spectral purity. In particular, the efficiency has been of great significance to power amplifier designers because it affects the lifetime, reliability, and cost of the entire system. This is also the situation for power amplifiers in industrial, scientific, and medical (ISM) applications such as induction heating, plasma generation, RF-driven lighting, or RF imaging.

Switching-mode amplifiers such as Class-D, E, F, and E/F have been proposed in the context of the demand for high-efficiency power amplifiers. They achieve the high efficiency at the expense of linearity, through the switching operation of the transistor and the appropriate harmonic tuning of output impedance. Recent advances in transistor technology enable the switching-mode concepts to be extended to the applications of higher output power as well as higher frequency. However, it is still challenging to build solid-state power amplifiers with several kW output power for ISM applications, although in comparison with vacuum-tube power amplifiers, they would have light weight, compact size, and high reliability. Judicious selection of the solid-state device and the operating mode of amplification should be made in order to generate and handle enormous voltage and current at the output. Also, a very efficient technique for power combining is required to achieve several kW from solid-state devices, since it is difficult to obtain such a high power level from a single transistor.

Stability is an important design issue in all types of RF and microwave circuits. Instabilities, such as spurious oscillations, noisy precursors, chaos, hysteresis, solution jumps, etc., degrade or disrupt the original performance of each circuit. They also may destroy the active device itself due to the excessive terminal voltage or current induced from its abnormal operation. The stability analysis of switching-mode power amplifiers is especially essential because of their strongly nonlinear operating behavior, which gives many more possibilities for instability. Unfortunately, most of these instabilities come from parametric oscillations and are difficult to predict by conventional linear stability analysis techniques. Instead, nonlinear techniques, taking into account the steady-state solution driven by large input signal, are required in order to detect and remedy such parametric instabilities. To be practical, the techniques should be general enough to be applied to any kind of amplifiers and should be implemented on commercial harmonic balance simulators.

This dissertation presents design and implementation techniques for solid-state power amplifiers that generate the output power up to 2.7 kW. Several vertically double-diffused MOS (VDMOS) are tuned to Class-E/F_{odd} mode [1] to achieve high efficiency. The output power from each VDMOS is then combined using a distributed active transformer (DAT) [2]. The amplifier with four VDMOS combined exhibits 1.5 kW output power with 85 % drain efficiency and 18 dB gain at 29 MHz. The output power of 2.7 kW is achieved with 79 % drain efficiency and 18 dB gain, when eight VDMOS are combined by the DAT.

Motivated by common observation of various instabilities during the measurements of switching-mode amplifiers, this dissertation presents nonlinear approaches for stability analysis of power amplifiers. Based on bifurcation detection tools including pole-zero identification and an auxiliary generator, the region for stable operation is delimited with respect to circuit parameters of interest. These tools are implemented in a commercial harmonic balance simulator with an optimization engine. Different instabilities are also analyzed in a large-signal operating regime by combining the bifurcation detection tools with other simulation techniques such as conversion-matrix approach and envelope-transient

simulation. All of these stability analysis techniques are applied to stabilize two switching-mode amplifiers that have shown various instabilities: spurious oscillation, hysteresis of the oscillating solution, and chaotic spectrum in a Class-E/F_{odd} amplifier, and noisy precursors and hysteresis of the power-transfer curve in a Class-E amplifier. These instabilities are predicted, analyzed, and finally eliminated in a global manner of operation, using the stability analysis techniques.

Interestingly, the nonlinear stability analysis is beneficial not only to suppressing critical instabilities in power amplifiers, but also to promoting desirable oscillations in other nonlinear circuits such as oscillators or synchronized circuits. This dissertation also presents a nonlinear design technique for high-power switching-mode oscillators, based on the stability analysis tools. By combining existing quasi-nonlinear design techniques with an auxiliary generator, a switching-mode oscillator can be designed, such that the output power and efficiency are optimized at a fixed oscillation frequency. Intensive stability analyses are carried out for oscillation start-up and steady-state solutions using pole-zero identification. The technique is experimentally verified by the design of a Class-E oscillator at 410 MHz.

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S. Jeon, A. Suárez, and D. B. Rutledge, "Global stability analysis and stabilization of a Class-E/F amplifier with a distributed active transformer," *IEEE Trans. Microwave Theory & Tech.,* vol. 53, no. 12, pp. 3712−3722, Dec. 2005.

S. Jeon and D. B. Rutledge, "A 2.7-kW, 29-MHz class-E/F_{odd} amplifier with a distributed active transformer," *2005 IEEE MTT-S Int. Microwave Symp. Dig.*, Long Beach, CA, Jun. 2005, pp. 1927−1930.

Chapter 2

Design Considerations of Switching-Mode Power Amplifiers

Power amplifiers are widely used in the applications of wireless communication, radar, and industrial, scientific, and medical (ISM) fields. In wireless communication and active radar applications, power amplifiers amplify different RF input signals, depending on the modulation scheme, to feed sufficient transmitting power to antennas. ISM applications such as induction heating, plasma generation, RF-driven lighting, or imaging require RF power sources that generate a significant amount of RF power.

Since each application has a different operating condition and requirement of the power amplifier, no single or unified technique exists for the optimum design that is suitable for all applications. Designers have to consider the important performance issues of the power amplifier for a particular application. Then, they select or invent appropriate components and techniques at every design step, from the choice of transistors to the entire architecture. This custom-fit property makes a power amplifier one of the most expensive blocks in a whole system of applications.

Switching-mode power amplifiers have been proposed and developed for the applications that require high efficiency. By operating the transistor as a switch rather than a current source and employing appropriate output harmonic terminations, the amplifiers can achieve 100 % efficiency in principle. The linearity of switching-mode amplifiers, however, is very poor since the amplifiers are driven into a deep saturation region. Therefore, typical

applications of switching-mode amplifiers are RF power generation systems in ISM fields and communication systems modulated with a constant-envelope signal.

There are many design considerations to be addressed for the switching-mode power amplifiers. Proper choice of operating class, transistors, power-combining technique, and thermal management must be done, based on the performance criteria required for each particular application. The criteria include operating frequency, output power level, bandwidth, gain, and stability as well as efficiency and linearity.

A difficult situation frequently encountered in the switching-mode power amplifier design is that the strongly nonlinear operating nature of the amplifiers usually puts more challenges to meeting all of the required specifications. For instance, the nonlinear behavior of the transistor not only degrades the linearity demanded for communication systems with non-constant envelope modulation scheme [3], but also gives much possibility to induce instabilities [4] that are detrimental to both the amplifier and the whole system. These instabilities are generated in the large-signal operating regime of the amplifiers, so that they are extremely difficult to predict and (or) eliminate by using conventional small-signal stability analysis such as *k*-factor or stability circles.

Moreover, there exist some inherent trade-offs between performance criteria of power amplifiers: efficiency and linearity, operating frequency and gain, operating frequency and output power, bandwidth and gain, etc. These trade-offs are also applied to switching-mode power amplifiers in the same way. Designers usually optimize one criterion of performance while sacrificing the other but keeping it within an acceptable level, depending on the applications. Thus, the design of power amplifiers demands a wide view of all criteria involved in the requirements as well as a careful application of detailed design techniques.

This chapter discusses the main design issues and considerations for switching-mode power amplifiers in a broad perspective. The important criteria for amplifier performance will

be dealt with first, and then followed by the technologies and considerations involved with the switching-mode amplifier design.

2.1 Performance Criteria of Switching-Mode Power Amplifiers

There are numerous criteria to evaluate the performance of switching-mode power amplifiers. The most significant criterion is obviously the efficiency, which is why the switching-mode techniques have been proposed. At the expense of linearity, the amplifiers can achieve high efficiency, ideally up to 100 % from their deeply saturated operation. Operating frequency, output power, gain, and bandwidth should also be considered at the design stage in order to choose proper active devices or design technologies. In this section, major performance criteria in switching-mode power amplifiers are reviewed.

2.1.1 Efficiency

2.1.1.1 Definitions

An amplifier is not a magical circuit that amplifies an RF input signal to a larger level without any additional power input. In fact, every amplifier requires DC power supplies that provide the ability of RF amplification. Figure 2.1 shows a diagram of typical power flow in a generalized amplifier, where an input-drive source is assumed to generate an RF signal at frequency f_0. By the law of energy conservation, the total amount of power entering into an amplifier has to be same to the total amount coming out from it.

$$P_{\text{in}}(f_0) + P_{\text{DC}} = \sum_k \left\{ P_{\text{out}}(kf_0) + P_{\text{diss}}(kf_0) \right\} \tag{2.1}$$

Due to the nonlinear operation of an amplifier, many harmonics are generated in RF output power $P_{\text{out}}(kf_0)$ and dissipated power $P_{\text{diss}}(kf_0)$. The input DC power is calculated by

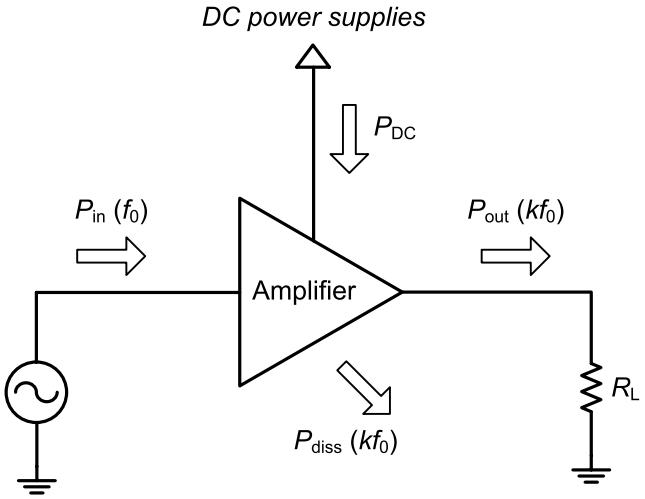


Figure 2.1: Typical power flow in a generalized amplifier.

$$P_{DC} = f_0 \int_{1/f_0} v_{dc}(t) i_{dc}(t) \cdot dt \ , \tag{2.2}$$

where $v_{dc}(t)$ and $i_{dc}(t)$ represent DC voltage and current supplied from DC power supplies, respectively.

Efficiency is defined by a ratio of the amount of power "produced" to the amount "expended" in the amplification:

$$\eta = \frac{P_{\text{produced}}}{P_{\text{expended}}} \ . \tag{2.3}$$

According to different definitions of the power "produced" and "expended", respectively, there exist several definitions of efficiency, also.

First, if we consider the fundamental component of RF output, i.e., $P_{out}(f_0)$ as produced power and the total input power delivered to the amplifier, i.e., $P_{in}(f_0) + P_{DC}$ as expended power, then the efficiency is defined as

$$\eta_{\mathrm{T}} = \frac{P_{\mathrm{out}}(f_0)}{P_{\mathrm{in}}(f_0) + P_{\mathrm{DC}}} = \frac{P_{\mathrm{out}}(f_0)}{\frac{P_{\mathrm{out}}(f_0)}{G} + P_{\mathrm{DC}}} \quad , \tag{2.4}$$

where

$$G = \frac{P_{\mathrm{out}}(f_0)}{P_{\mathrm{in}}(f_0)} \tag{2.5}$$

is the power gain. This *total efficiency* is the most physical definition of efficiency, because it takes into account all meaningful energy flow into and out of the amplifier. However, particularly in power amplifiers, the *drain efficiency* (for FET amplifiers) or *collector efficiency* (for BJT amplifiers) is more commonly used to measure the efficiency as follows:

$$\eta_{\mathrm{D}} = \frac{P_{\mathrm{out}}(f_0)}{P_{\mathrm{DC}}} \quad . \tag{2.6}$$

This definition is based on the view that a power amplifier is basically a power converting circuit from DC input to RF output. Thus, the drain efficiency measures a quality factor of the power conversion. Almost all DC power is supplied from drains (or collectors), and this is why it is called drain (or collector) efficiency. The drain efficiency is useful when input power level is of no primary significance, which falls into the cases that either gain is very high or the input-drive source is assumed to generate sufficient power without extra constraints. It should be noted that the total efficiency approaches the drain efficiency if the gain is high. Another advantage of the drain efficiency is the isolation of the efficiency calculation from power loss in the input circuitry. This enables the drain efficiency to serve as a comparison criterion for performance of different amplifier operating classes that are entirely determined by bias condition and output termination. Also, this is why the drain efficiency is commonly used to evaluate the performance of switching-mode amplifiers, where the input drive is assumed to be sufficiently large to saturate the transistors.

The most widely used definition of efficiency in all types of amplifiers, however, is the *power-added efficiency*, in which the produced power from an amplifier is defined as the RF power "added" by an amplifier, i.e., the difference between the RF input and output at f_0:

$$PAE = \frac{P_{\text{out}}(f_0) - P_{\text{in}}(f_0)}{P_{\text{DC}}} = \frac{P_{\text{out}}(f_0)}{P_{\text{DC}}}\left(1 - \frac{1}{G}\right) = \eta_{\text{D}}\left(1 - \frac{1}{G}\right) . \tag{2.7}$$

In fact, this definition is not correct in a physical point of view, because the RF input power is included in the "produced" power of the amplifier. If the gain is below unity, it even could be negative. However, the advantage of the power-added efficiency is that it combines the gain with the drain efficiency. When a power amplifier is used within a system, the input signal is provided from the previous stage that has a common limitation on the output power level. Thus, the gain of the power amplifier, in this case, is a critical factor to determine the efficiency of the overall system as well as of the amplifier itself. From equation (2.7), the power-added efficiency will approach to its maximum value, which is the drain efficiency, as the gain increases.

2.1.1.2 Why High Efficiency?

The high efficiency of power amplifiers leads to low power consumption, low temperature rise, high operation reliability, and low cost. In limited energy-budget operating conditions such as battery-operated systems or space applications, the low power consumption is very important, because it dominates the operation time. Let us suppose that the total available energy E_{avail} and the required amount of produced power P_{produced} are fixed for an instance. Then, the total operation time is calculated by

$$t_{\text{op}} = \frac{E_{\text{avail}}}{P_{\text{expended}}} = \eta \frac{E_{\text{avail}}}{P_{\text{produced}}} , \tag{2.8}$$

where η is defined from equation (2.3). Thus, the operation time increases in proportion to efficiency. The low temperature rise is important particularly in high power applications in

which the design of a proper heatsink is a critical issue. The dissipated power during the operation is calculated by

$$P_{\text{diss}} = P_{\text{expended}} - P_{\text{produced}} = \left(\frac{1}{\eta} - 1\right) P_{\text{produced}} \ . \tag{2.9}$$

From equation (2.9), low efficiency gives rise to large dissipated power that generates high temperature rise, since most of the dissipated power is converted to heat. The high temperature during the operation makes the amplifier stray from its nominal performance and the amplifier itself may even fail. Thus, a heatsink has to be carefully designed to extract the large amount of heat out of the amplifier and to maintain a safe operating temperature, which requires additional cost. This is why high efficiency is needed for high operation reliability and low cost.

Numerous ways have been proposed to improve the efficiency of power amplifiers. The most popular way is to design switching-mode amplifiers including Class-D [6], E [7], F [8], and E/F [1] that are able to achieve 100 % drain efficiency in principle. These switching-mode operations will be discussed more in detail in Section 2.2.2. Other classical techniques for efficiency enhancement are the Doherty [9] and bias-adapted amplifiers [10], which are usually employed to boost the efficiency in backed-off transconductance amplifiers.

2.1.2 Linearity

The linearity of amplifiers implies the ability to correctly reproduce the amplitude and phase of the input signal at the output. The amplitude of the output should be linearly proportional to that of the input, while the phase difference between the two should remain the same. The high linearity of amplifiers is necessary when the input signal contains both amplitude and phase modulation.

Unfortunately, switching-mode amplifiers have notorious performance of linearity when operated in normal conditions. Figure 2.2 shows qualitative power-transfer curves of an

ideally linear amplifier and a typical switching-mode amplifier, respectively. Since typical gate bias of switching-mode amplifiers is below threshold (or pinch-off) voltage, the transistor still remains turned off when the input power is very small, as shown in Figure 2.2 (b). Thus no output power comes out except a small amount of leakage power passing through feedforward capacitance of the transistor. When the input signal is increased enough to make the transistor turn on, the output power grows rapidly, which is marked by the transition region. After a short interval of input power at transition, the amplifier enters into the saturation region, where the output power keeps an almost constant level while the input power increases further. It is the saturation region where switching-mode amplifiers are supposed to operate typically.

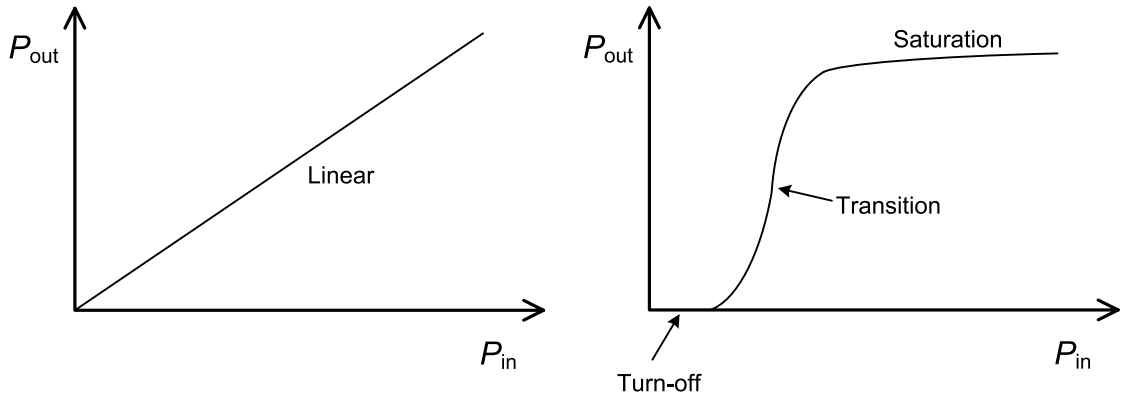


Figure 2.2: Comparison of qualitative power-transfer curves between an ideally linear amplifier (a) and a typical switching-mode amplifier (b).

The strongly nonlinear behavior of switching-mode amplifiers limits their applications to communication systems with constant-envelope modulation schemes such as CW, FM, FSK, and GMSK (used in GSM). Another typical application is RF power generation for ISM fields that requires high efficiency and does not need high linearity. Sometimes,

switching-mode amplifiers are biased above threshold voltage [11], [12], [13], which improves the linearity, particularly at high frequency. In the power transfer curve of those amplifiers, the turn-off region as in Figure 2.2 (b) does not exist anymore and the transition region shows linear behavior. However, in a strict point of view, they are not typical switching-mode amplifiers, but are closer to overdriven transconductance amplifiers. The classification of amplifiers will be discussed in Section 2.2, although it is not so clear that there have been many debates on the classification.

Classical techniques to improve the linearity of switching-mode amplifiers are EER (Envelope Elimination and Restoration) and LINC (LInear amplification using Nonlinear Components). The EER technique was originally proposed by Kahn [14] and successfully applied to transmitters with a time-varying envelope at HF/VHF-band [15], L-band [5], and X-band [16]. In the EER system illustrated in Figure 2.3, the RF input signal is decomposed into two components that contain phase and amplitude (envelope) information, respectively. A power amplifier is driven by the phase component signal where the envelope component has been eliminated. If the amplifier operates in ideal switching-mode, the RF output amplitude will be determined only by its DC bias voltage, not by the input drive signal. This bias voltage is modulated with the amplitude (envelope) signal component of the RF input. Hence, the envelope of the RF output is restored in proportion to that of the RF input.

The LINC technique shown in Figure 2.4 dates back to the 1930s [17] and has been applied from HF [18] to microwave frequencies [19]. The signal component separator performs AM-to-PM modulation to the RF input signal and generates two constant-envelope signals with outphase relationships to each other. Two switching-mode amplifiers are used to amplify each of the outphasing signals with high efficiency. By combining two phase-modulated output signals from the amplifiers, the amplitude component of RF input is recovered.

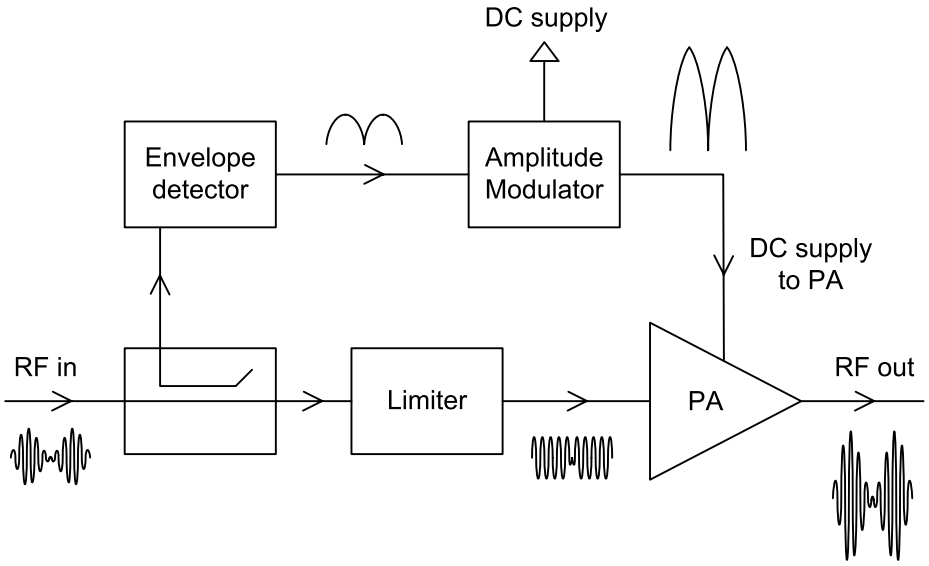


Figure 2.3: Simplified envelope elimination and restoration (EER) system.

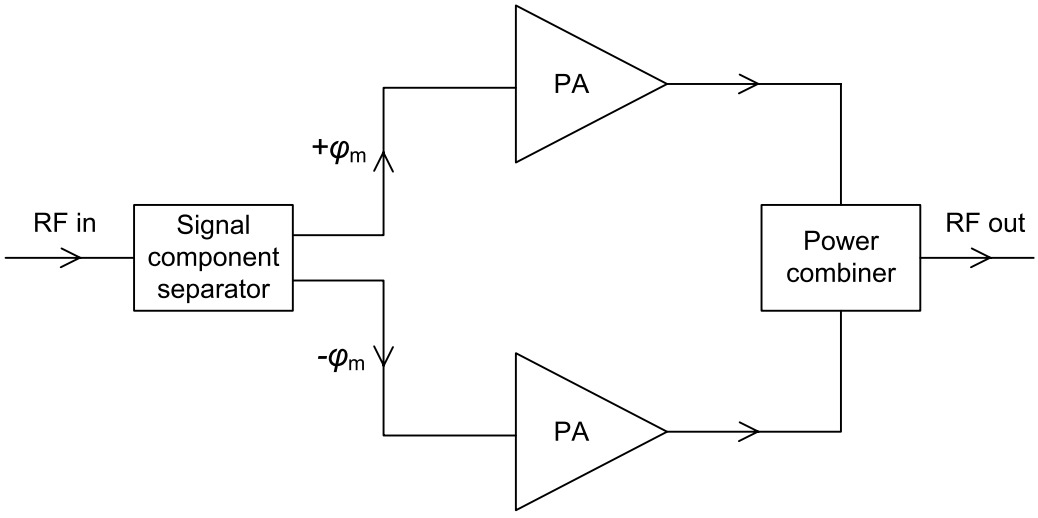


Figure 2.4: Simplified linear amplification using nonlinear components (LINC) system.

2.1.3 Output Power

The required output power of amplifiers is determined entirely by the aimed applications. It ranges from several dBm for wireless handsets to hundreds of kilowatts for ISM applications. For example, GSM handsets for 900 MHz require up to 2 W peak output power, while RF power generators for induction heating need from 100 W to 100 kW at ISM bands such as 13.56, 27.12, 900−930, 2450 MHz, etc.

In the case of communication systems with complex modulation schemes such as CDMA, the output power varies dynamically following the modulated input signal. Then, peak envelope power (PEP) is defined by instantaneous output power when the RF output signal reaches its maximum swing. On the other hand, average power is calculated as the time average of the instantaneous output power. The ratio between them, called peak-to-average power ratio, is an important parameter in envelope analysis of linear power amplifiers. However, in switching-mode amplifiers, output power commonly refers to the peak envelope power because the input drive, in most applications, is fixed to make the amplifiers operate in PEP condition. Sometimes, the output power is specified and measured under two different conditions: continuous wave (CW) and pulsed operating conditions, depending on applications. For example, most radar applications or some ISM applications including plasma generation need pulsed operation rather than CW. Output power level along with efficiency determines the amount of power that has to be extracted out of the operating amplifiers by heatsink. Pulsed operation obviously puts less stringent requirements on the heatsink. If duty cycle and efficiency in pulsed operation are D and η, respectively, then the dissipated power that should be extracted by heatsink is

$$P_{\text{diss,pulsed}} = D \cdot \left(\frac{1}{\eta} - 1 \right) P_{\text{out,pulsed}}, \tag{2.10}$$

where $P_{\text{out,pulsed}}$ is the output power in pulsed operation. When D approaches unity, it becomes equation (2.9), which is the dissipated power in CW operation.

Output power has a trade-off with operating frequency mainly due to the limitation of solid-state device technology. This is why vacuum-tube devices including klystron, magnetron, and traveling wave tubes are still used to generate very high output power (up to tens of MW) at high frequency (up to 100 GHz or higher). However, due to the innovative advance of power transistor technology, solid-state power amplifiers are recently replacing vacuum-tube devices up to around the 5 kW output power level. Efficient power-combining techniques are essential to achieve such high output power with high efficiency, because the maximum power that a single solid-state device can generate is still limited to hundreds of watts even at HF/VHF frequencies [20].

2.1.4 Operating Frequency

Historically, switching-mode amplifiers have been proposed and demonstrated at low frequencies (HF and lower) [7], [8], [21]. This is not only because of the frequency limitation of active devices, but also because of the inherent operating mechanism of each switching-mode that confines its application to low frequency. In particular, classic design equations for Class-D [22] and Class-E [23] have been derived on the assumption of lumped circuit elements. Those equations are fully valid at HF/VHF frequencies to obtain decent switching-mode operations. However, as operating frequency goes up, it is hard to achieve normal switching-mode operations and resulting high efficiency only with the equations, due to distributed characteristics of circuit elements, limited switching speed of transistors, and increased susceptance of drain-shunt capacitance.

Recently, several switching-mode amplifiers have been demonstrated at UHF and microwave frequencies as a result of modification of design equations and transistor technology improvements. Transmission-line Class-E amplifiers were demonstrated at frequency as high as X-band [16], [24]. Class-D operation, which has been traditionally used at very low frequency such as audio frequency, was adapted to build a UHF high-efficiency amplifier [25]. Although all of the high-frequency amplifiers operate in sub-optimal

switching-modes rather than in the ideal modes, the drain efficiency is still much higher than any other transconductance amplifiers, reaching even 80 % at X-band [24]. Nonetheless, it should be noted that efficiency and gain are generally degraded as operating frequency increases.

2.1.5 Gain and Bandwidth

Gain of power amplifiers, defined in equation (2.5), have not been of primary concern for most switching-mode amplifiers. The amplifiers have been designed at low frequency and the inherent gain of transistors is very high at that frequency. In this case, power-added efficiency becomes almost the same as drain efficiency, which, therefore, has been exclusively used to measure the efficiency performance of the amplifiers. Also, in RF generator applications, the most concerns are output power level and DC power consumption, not the gain, because the input RF source is assumed to provide whatever amount of drive power required for switching-mode operation. However, as operating frequency increases, the gain drops rapidly and becomes one of the important criteria to be considered in switching-mode amplifier design. The power-added efficiency also drops and shows a fair difference from the drain efficiency. When the amplifier is used in a system, particularly in a communication system, this power-added efficiency may be more important performance than the drain efficiency. To compensate for the degraded gain and power-added efficiency, preamplifiers can be employed before the power amplifier and generate sufficient input drive.

Bandwidth of amplifiers can be defined in different ways. For small-signal linear amplifiers, it is usually defined as the width between two frequencies where the gain drops by 3 dB from its peak value. Although this definition can also be used for switching-mode power amplifiers, the more widely used bandwidth is the one defined by output power, as shown in Figure 2.5. Bandwidth that fulfills a certain level of efficiency is usually used for switching-mode amplifiers, too.

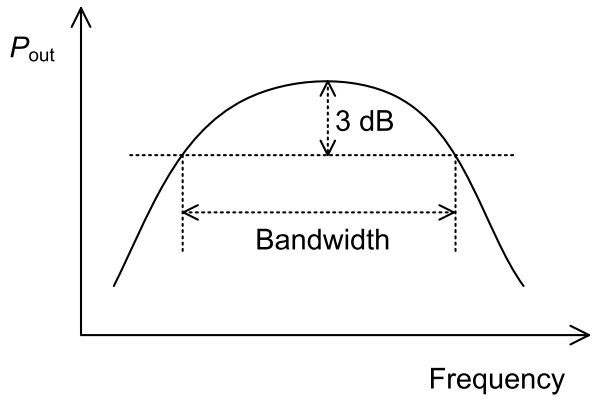


Figure 2.5: Definition of bandwidth in terms of output power.

Intrinsically, switching-mode amplifiers have more or less narrow bandwidth. Resonant tanks at the fundamental frequency and (or) harmonics are required in the output circuitry in order to shape output voltage and current waveforms in switching-modes, which limits the frequency response of the amplifiers. It is difficult to implement those resonant tanks that present the appropriate impedance at each harmonic for wide range of drive frequency. To overcome the constraint of narrow bandwidth, several techniques have been demonstrated, including multi-band [26] and broadband [27], [28] switching-mode amplifiers.

2.2 Operating Classes of Power Amplifiers

Switching-mode power amplifiers are implemented in several different ways. Including transconductance amplifiers altogether, there exist numerous types of power amplifiers that have been proposed up to now. The most classical way to classify power amplifiers is to designate each type as Class-A, AB, B, C, D, E, F [22], and so on. This classification is based on DC bias condition, conduction angle, output terminations at fundamental and harmonics, etc. However, it should be noted that the classification is somewhat ambiguous, so that an amplifier could fall into two or more classes. Sometimes, one class may converge to another as operating conditions change.

The operating classes can be categorized into two broad categories for convenience. Classes-A, AB, B, and C are categorized as transconductance amplifiers. Switching-mode amplifiers refer to Class-D, E, and F. This section discusses basic operation theory of each class.

2.2.1 Transconductance Amplifiers

In transconductance amplifiers, the transistor operates as a voltage-controlled current source, as in a traditional way. Each different class is determined based on the conduction angle, which is defined as a portion out of one whole period (2π) when the transistor conducts non-zero drain current. Designers can choose different conduction angles from 0 to 2π and the corresponding classes, by changing bias voltages and input-drive power.

2.2.1.1 Class-A

The bias point for Class-A amplifiers is located in the middle of I-V characteristics of the transistor, shown in Figure 2.6. For the peak power operating condition, the DC voltage is biased at the middle point between the knee voltage V_{knee} (in case of FET) and maximum allowable voltage V_{max} of the transistor. Also, the DC current is biased at the middle between zero and maximum allowable current I_{max}. In this way, the load line of the amplifier becomes straight centered at the bias point. The typical drain voltage and current waveforms are shown in Figure 2.7. Note that the transistor conducts drain current all the time, which means the conduction angle is 2π.

Since the Class-A amplifiers are always operated in the transconductance region (neither the triode nor the cut-off region) as shown in Figure 2.6, the output current (or output voltage) should follow the same waveform as the input voltage with minimum distortion. This indicates the strong aspect of the Class-A amplifiers, which is high linearity. However, the most serious drawback of the Class-A operation is low efficiency. Due to the DC bias point in the middle of I-V characteristics, high quiescent current flows when high voltage is

presented simultaneously. It generates huge power dissipation in the transistor, not in the output load. Actually, the maximum allowable drain efficiency of Class-A amplifiers is calculated only as 50 % [4]. This low efficiency limits the application of the Class-A operation to low-power driver amplifiers or the amplifiers that require extremely high linearity.

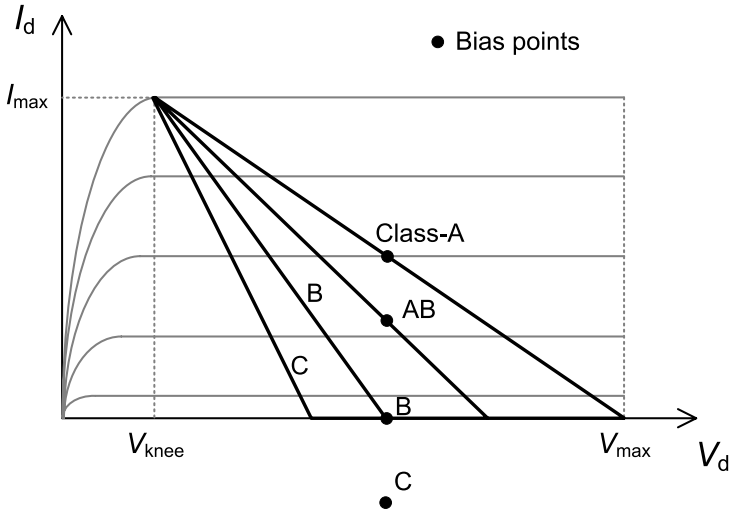


Figure 2.6: Bias points and load lines of transconductance amplifiers.

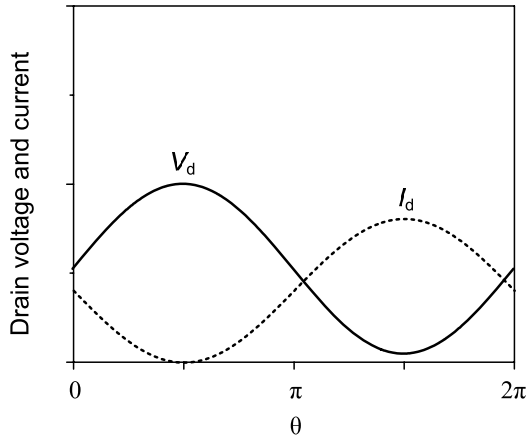


Figure 2.7: Drain voltage and current waveforms of ideal Class-A amplifiers**.**

2.2.1.2 Class-B, AB

The gate bias in Class-B amplifiers is located at the threshold voltage of the transistor, while the drain bias is similar to that of Class-A amplifiers, as shown in Figure 2.6. Thus, when the transistor is driven by sinusoidal input, it is turned on for half of the drive time. For the other half of the time, the transistor is turned off and the load line follows the zero-current section. Consequently, the conduction angle of Class-B amplifiers is π, and the drain current waveform becomes a half-sinusoid, as shown in Figure 2.8. The maximum drain efficiency achieved at the peak envelope power condition reaches 78.5 %. Class-B amplifiers are usually configured as a push-pull pair, which combines half-sinusoids from each amplifier, operated 180° out-of-phase, and produces a full sine waveform in the output.

Class-AB is another common operating class used for linear amplification. The bias point for Class-AB is located between Class-A and B. Thus the conduction angle is between π and 2π, and the maximum drain efficiency is between 50 % and 78.5 %. Due to the compromised characteristics of fairly high efficiency and linearity, this operating class is widely employed for amplifiers in communication applications.

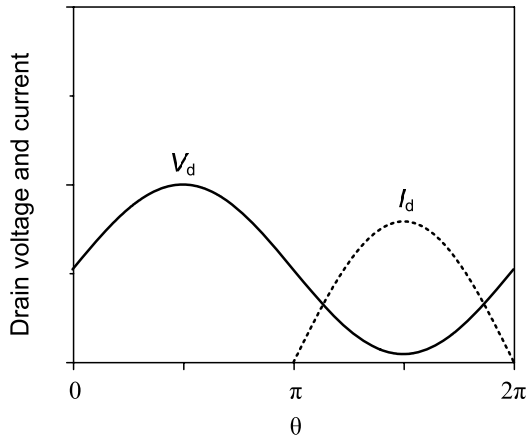


Figure 2.8: Drain voltage and current waveforms of ideal Class-B amplifiers.

2.2.1.3 Class-C

The gate bias for Class-C is located below the threshold voltage, so that the conduction angle becomes less than π. Figure 2.9 shows the drain voltage and current waveforms of typical Class-C amplifiers. The current waveform is distorted from the sinusoidal or half-sinusoidal one in Class-A or B, which degrades the linearity severely. At the expense of low linearity, however, the Class-C amplifiers can achieve high efficiency, typically 75–80 %. The drain efficiency increases as the conduction angle decreases, and it can achieve 100 % drain efficiency in principle when the conduction angle becomes zero. Unfortunately, this operating condition is not practical because the output power also becomes zero with a zero conduction angle. Due to the high efficiency, the Class-C is widely used in high-power amplifiers for CW and FM transmitter applications.

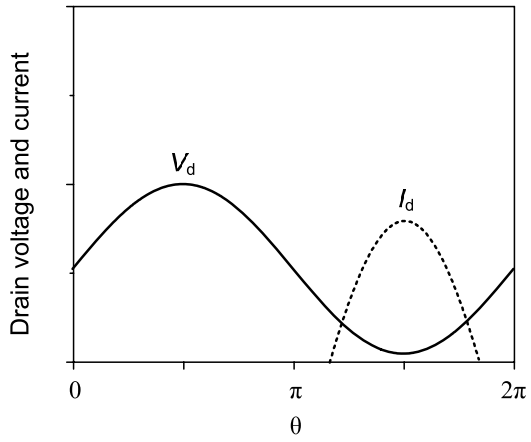


Figure 2.9: Drain voltage and current waveforms of ideal Class-C amplifiers.

2.2.2 Switching-Mode Amplifiers

In switching-mode amplifiers, the transistor is driven by a very large input signal, so that the transistor operates as a switch rather than a current source unlike transconductance amplifiers. The greatest advantage of switching mode is the ability to achieve the high

efficiency and high output power simultaneously. By minimizing the overlapping of non-zero drain voltage and non-zero drain current waveforms, power loss in transistors is significantly reduced, which means the increase of efficiency. In principle, the drain efficiency of switching-mode amplifiers can be up to 100 % without output power degradation. Although many loss mechanisms, such as ohmic loss and discharge loss, degrade the efficiency from 100 % in the real world, they still achieve above 90 % at HF [7], 80 % at VHF [29], and 70 % at UHF and microwave frequencies [24], [25], [30], [31]. On the other hand, the linearity of switching-mode amplifiers is very poor, because the output power is not a function of the input power during the ideal switching operations. The input drive controls only the on-off operation of the transistor, not the level of the output power. Therefore, switching-mode amplifiers are commonly employed for CW operation or constant-envelope modulation schemes that require less linearity. In order to improve the linearity of switching-mode amplifiers, several system approaches have been proposed like EER and LINC, which are described in Section 2.1.2.

2.2.2.1 Class-D

Class-D uses two transistors that are usually driven in push-pull, so that they are alternatively switched on and off. By this two-pole switching operation of transistors, the drain voltage (in voltage-mode Class-D) or drain current (in current-mode Class-D) is shaped to a rectangular waveform [4]. The output circuitry contains a bandpass filter that generates sinusoidal output from the rectangular waveform of the drain terminal. Ideal drain voltage and current waveforms are shown in Figure 2.10. Since there is no overlapping between drain voltage and current waveforms, it can achieve 100 % drain efficiency. However, practical Class-D amplifiers suffer from discharge loss generated in transistor output capacitance. When the switch (that is, the transistor) is turned on, the charge stored in the transistor output capacitance is discharged instantaneously through the on-switch. The amount of power loss involved with this discharge [4] is calculated as

$$P_{\text{loss}} = 2C_{\text{out}}V_{\text{dc}}^2 f \ , \tag{2.11}$$

where C_{out}, V_{dc}, and f are transistor output capacitance, DC supply voltage, and operating frequency, respectively. As can be seen in equation (2.11), the power loss increases with high supply voltage and high frequency. This is why the Class-D is rarely used for the power amplifiers at high frequencies above VHF.

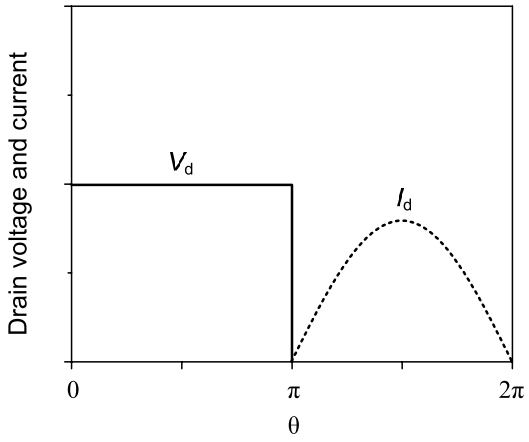


Figure 2.10: Drain voltage and current waveforms of ideal Class-D amplifiers.

2.2.2.2 Class-E

Class-E is one of the most popular switching-mode operations due to its high efficiency characteristic and very simple circuitry as well. Usually, a single transistor is employed as a switch and single-ended output is taken, although push-pull operation is also possible [23]. The basic schematic of the Class-E amplifier is shown in Figure 2.11. The transistor operates as an ideal switch, but practically it includes small on-resistance and output capacitance (represented by C_{out}). The externally connected shunt capacitance C_{p} is charged and discharged along with the transistor output capacitance following the RF cycle and shapes the drain voltage and current waveforms to fulfill the optimum Class-E operation. When the switch is off, the capacitors are charged and the drain voltage V_{d} rises and falls without drain

current I_d. When the switch is on, the current rises smoothly with no voltage across the capacitors. The drain voltage and current waveforms for ideal Class-E operation are shown in Figure 2.12. By avoiding the overlapping of voltage and current, it can achieve 100 % drain efficiency ideally. The series resonant tank operates close to the input-drive frequency f_0, so that the harmonics are filtered out and the output voltage V_o becomes sinusoidal. The important point regarding this resonant tank is that it should be designed in such a way that the resonant frequency is a little off from the exact input-drive frequency. Actually, a small amount of additional inductance (called detuning inductance $L_{detuning}$) is required, which makes the resonant frequency a little lower than f_0. That is,

$$L_0 = L_{res} + L_{detuning} \ , \tag{2.12}$$

where L_{res} is the inductance to make a resonance exactly at f_0 with C_0:

$$f_0 = \frac{1}{2\pi\sqrt{L_{res}C_0}} \ . \tag{2.13}$$

The detuning inductance makes the drain voltage fall to zero value with zero slope with respect to time, at the time when the switch is turned on. These conditions are called ZVS (zero voltage switching) and ZdVS (zero-voltage slope switching), which play significant roles in eliminating discharge loss from the shunt capacitors C_{out} and C_p.

Assuming the optimum operating conditions that the voltage waveform satisfies the ZVS and ZdVS and the duty cycle of input drive is 0.5, the following design equations are derived [4]:

$$C_p + C_{out} = \frac{0.1836}{2\pi f_0 R_L} \ , \tag{2.14}$$

$$L_{detuning} = \frac{1.1525 R_L}{2\pi f_0} \ , \tag{2.15}$$

where R_L is load resistance and f_0 is operating frequency. In equation (2.14), the required shunt capacitance decreases with the operating frequency. Thus, at high-frequency operation, the transistor output capacitance C_{out} can be, by itself, large enough to satisfy equation (2.14), and the external shunt capacitance C_p is not usually connected [32].

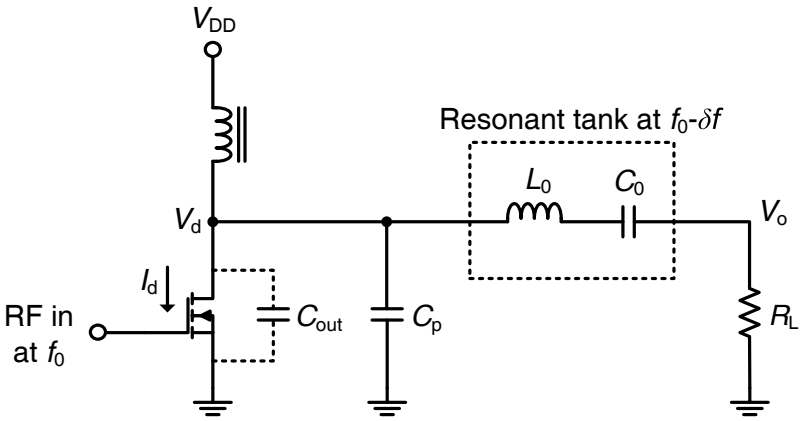


Figure 2.11: Basic schematic of a Class-E amplifier.

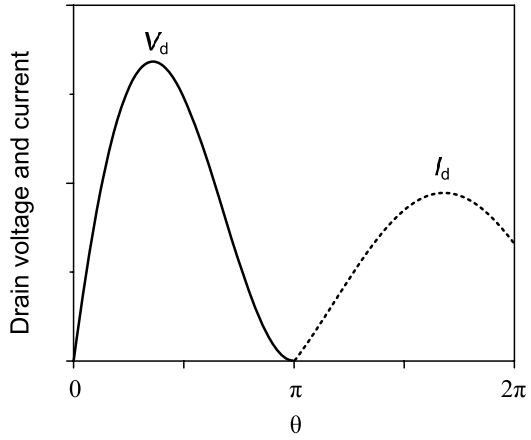


Figure 2.12: Drain voltage and current waveforms of ideal Class-E amplifiers.

2.2.2.3 Class-F

Class-F is basically derived from Class-B with multiple harmonic resonant filters. The sinusoidal voltage waveform of Class-B is shaped to a rectangular one for Class-F by appropriate harmonic tuning: open circuit at all odd harmonics and short circuit at all even harmonics. Figure 2.13 shows the ideal drain voltage and current waveforms of Class-F amplifiers, where no overlapping between the two suggests an ideal 100 % drain efficiency. The ideal Class-F amplifier is implemented conceptually with bandstop filters, as in Figure 2.14. Obviously, the output circuitry of Class-F amplifiers is very complicated in order to obtain the ideal voltage and current waveforms. However, in practical Class-F amplifiers, harmonic filters are usually employed only up to third harmonic although the efficiency is a little degraded. Class-F^{-1} (inverse Class-F) is the dual mode of Class-F operation. By terminating open circuit at even harmonics and short circuit at odd harmonics, the voltage and current waveforms are swapped from those of Class-F, so that half-sinusoidal voltage and rectangular current waveforms are produced.

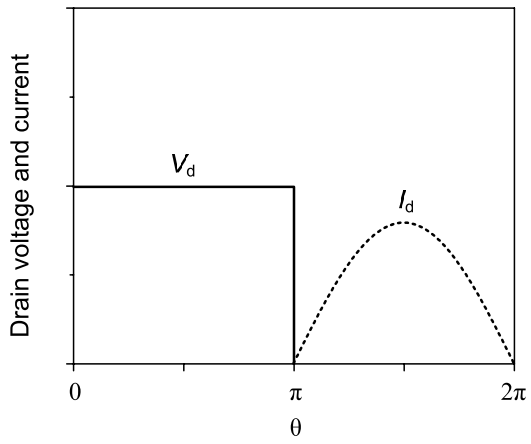


Figure 2.13: Drain voltage and current waveforms of ideal Class-F amplifiers.

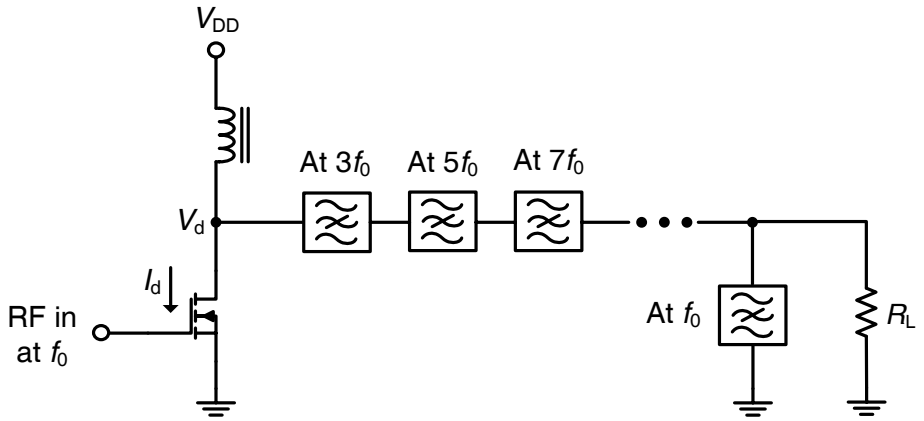


Figure 2.14: Conceptual schematic of a Class-F amplifier.

2.2.2.4 Class-E/F

Class-E/F is a mixed operating mode between Class-E and Class-F^{-1}, proposed by Kee, *et al*. [1]. The basic idea is that by combining the two operating modes for output harmonic terminations, the Class-E/F takes advantages from both modes to achieve high output power and efficiency. According to how the Class-E and Class-F^{-1} tunings are employed at each harmonic frequency, several family members of Class-E/F are developed: For example, Class-E/F_2, Class-E/$F_{2,3,4}$, Class-E/F_{odd}, Class-E/$F_{odd,2}$, etc. Class-E/F_x represents the mixed operating mode, such that Class-F^{-1} termination is employed at x harmonics while Class-E termination is used at the other harmonics [33].

Nonetheless, the most commonly used member in practical amplifiers is the Class-E/F_{odd} due to its simplicity of implementation. Figure 2.15 shows the basic schematic of a Class-E/F_{odd}-tuned amplifier. It consists of a pair of transistors, an output parallel resonator at operating frequency, detuning inductance $L_{detuning}$, and load resistance R_L. The two transistors are driven by strong 180° out-of-phase input signals, and operate as switches with output capacitance in parallel. Due to the push-pull operation, the center line of the pair becomes virtual ground at the fundamental and odd harmonics, and virtual open at the even harmonics. Thus, each drain terminal will be shorted to ground at odd harmonics as in Class-F^{-1}, and be

terminated by shunt capacitance C_s at even harmonics as in Class-E. The detuning inductance is required for the ZVS condition, and can be calculated as a function of C_s as follows [33]:

$$L_{\text{detuning}} = \frac{1}{(2\pi f)^2 C_s} \quad . \tag{2.16}$$

The ideal waveforms of Class-E/F_{odd} are shown in Figure 2.16. The voltage is sinusoidal while the current is superposition of rectangular and sinusoidal components. The advantage of Class-E/F_{odd} over Class-F^{-1} is the fairly simple circuitry of Figure 2.15, while it can achieve the waveforms like the ideal Class-F^{-1}. The lower peak voltage, lower rms current, and higher shunt capacitance tolerance are other benefits, compared to the Class-E operating mode. In some cases, additional even harmonic tuning is presented to Class-E/F_{odd} to achieve higher efficiency. One of the examples is Class-E/$F_{odd,2}$ shown in [34].

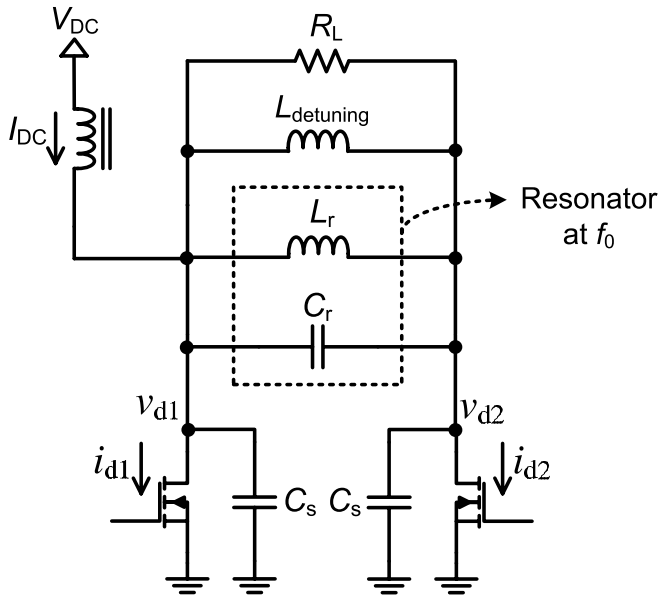


Figure 2.15: Basic schematic of a Class-E/F_{odd} amplifier.

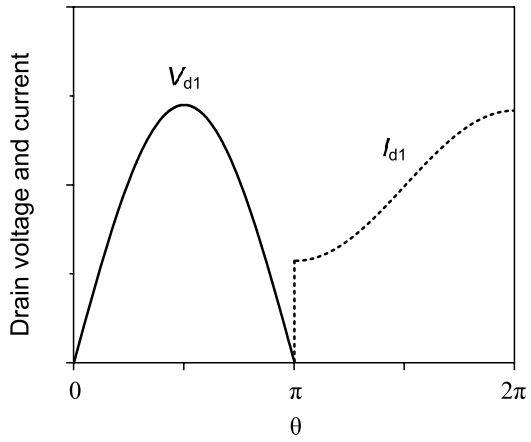


Figure 2.16: Drain voltage and current waveforms of ideal Class-E/F_{odd} amplifiers.

2.3 Stability

Although instabilities are encountered in all RF and microwave circuits, power amplifiers, especially switching-mode power amplifiers, have great potential to exhibit one or several types of instabilities simultaneously. In addition to the linear feedback mechanism that makes an oscillation, the strong nonlinearity of power amplifiers pushes them into an unstable region. The large RF signal periodically stimulates nonlinear circuit elements at the operating frequency, in such a way that the time-varying nonlinear elements exhibit negative resistance and induce those instabilities. These parametric instabilities tend to occur more commonly in switching-mode amplifiers, due to the extremely large input-drive level required for saturated operation of transistors. Actually, several instabilities have been observed experimentally during measurements of many switching-mode amplifiers developed at Caltech, some of which have been reported in [35]. Interestingly, the instabilities are observed only under a certain set of operating conditions, which include input-drive power, frequency, bias voltages, and temperature. For example, the switching-mode amplifier in [35] showed oscillations when driven by input power below a

certain level, while they showed decent amplifier performance without any instability for sufficiently high input-drive power.

2.3.1 Types of Instabilities

The types of instability commonly encountered in power amplifiers or switching-mode amplifiers are illustrated in Figure 2.17.

Figure 2.17 (a) shows sub-harmonic oscillation (particularly, frequency division by two), in which the oscillation frequency is related with the input-drive frequency f_{in} due to frequency division. The power amplifiers that have a binary power combining structure give much possibility to show sub-harmonic oscillation at half of the input-drive frequency, coming from their odd-mode oscillation characteristic [36]. However, sub-harmonic oscillation at the frequency divided by N larger than two is also observed at several switching-mode amplifiers.

The spurious oscillation at frequency f_{osc} not related with the input-drive frequency, as shown in Figure 2.17 (b), is the most commonly observed instability. Usually, the oscillation frequency is lower than the input-drive frequency and intermodulation products between the two are presented in the spectrum, which drives the amplifiers into a quasi-periodic regime. This type of oscillation originates from a Hopf bifurcation in which a pair of complex-conjugate poles crosses the imaginary axis into the right-hand side of the complex plane [37].

The chaos shown in Figure 2.17 (c) gives a continuous spectrum in the frequency domain, so that it looks like the noise floor of the measurement is arbitrarily boosted for a continuous frequency interval. However, chaos is not a random noise process but a deterministic phenomenon extremely sensitive to its initial condition. There are many routes that lead to chaos [38], including a quasi-periodic route with more than three non-commensurate frequency bases, a period-doubling route with continuous flip

bifurcations, and a torus-doubling route with frequency division of two non-commensurate frequency components. Although chaos has applications in communication systems [39], it is usually considered an undesirable instability in power amplifiers. Due to its continuous characteristic of spectrum, time-domain techniques are employed to predict the chaos in simulation rather than frequency-domain ones. However, harmonic balance can be efficiently employed to analyze the routes to chaos, i.e., the preceding stages just before evolving into chaos.

Noisy precursors are also observed often in many power amplifiers. They are different from oscillations, in that the circuit still operates in a stable periodic regime and no distinct spectral line is shown in the spectrum other than the input frequency and its harmonics. Actually, the noisy precursors present spectral bumps with some frequency interval as shown in Figure 2.17 (d), which are caused by noise amplification with reduced stability margin. When complex-conjugate poles in the left-hand side of the complex plane are located very closely to the imaginary axis, these noisy bumps are shown centered at the frequency of the poles and the intermodulated frequencies with the input signal. As the poles approach the imaginary axis by varying one or more circuit parameters, the bumps become narrower in bandwidth and higher in power [40]. In most cases, these bumps are eventually changed to oscillation spectral lines at a single frequency when the poles cross the imaginary axis into the right-hand side.

Other types of instabilities observed commonly in power amplifiers are hysteresis and jumps of solutions. Those two are related to each other because one is a usual cause for the other. Figure 2.17 (e) shows hysteresis and jumps presented in power-transfer characteristics of amplifiers. Two turning points, T_1 and T_2, induced by the D-type bifurcation make an unstable section in the amplifier periodic solution curve between the two points. Then, two jumps, J_1 and J_2, are observed when the input power is increased and decreased, respectively. The hysteresis and jumps are also observed in the oscillatory solutions as well as the amplifier solutions.

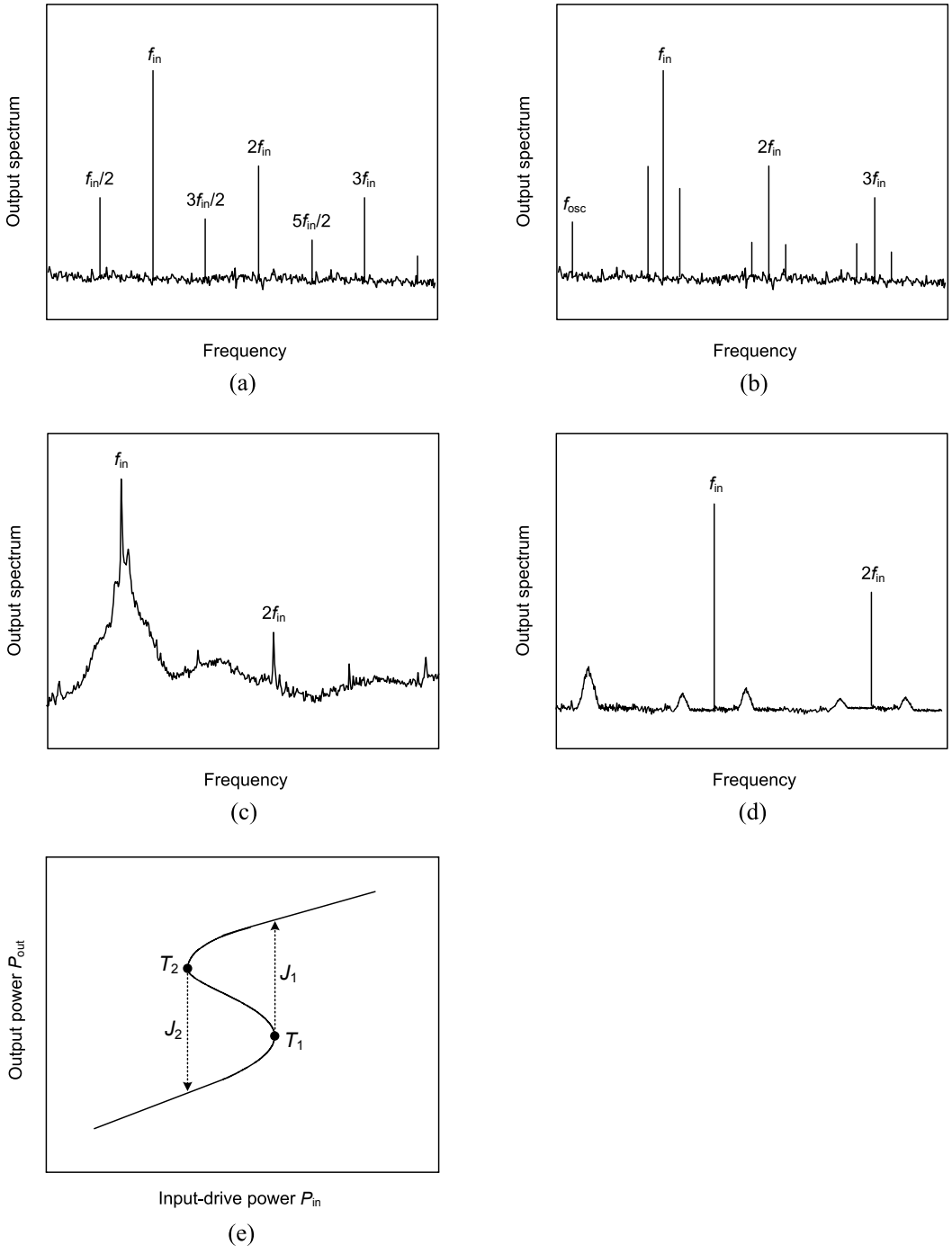


Figure 2.17: Types of instability commonly observed in power amplifiers. (a) Sub-harmonic oscillation. (b) Spurious oscillation at frequency unrelated with the input drive. (c) Chaos. (d) Noisy precursors. (e) Hysteresis and jump of solutions.

2.3.2 Stability Analysis Techniques

Instabilities in power amplifiers degrade amplifier performance such as output power, gain, and efficiency. They also give rise to unwanted interference with adjacent channels for communications. Moreover, active devices may be destroyed during the operation, due to excessive high voltage and current raised by suddenly provoked instabilities. Hence, these instabilities should be analyzed and eventually eliminated in simulation at the design stage or at the modification stage of the circuit after the first testing. The ways to analyze instabilities of RF and microwave circuits are categorized into linear and nonlinear techniques.

The linear techniques include the calculation of k- and Δ-factors of two-port represented networks. The analysis using the stability circles is also in the same category. These techniques are very powerful and simple to apply to any linear circuits. However, due to the fact that they are based on linear S-parameters, it is difficult to extensively apply to nonlinear circuits such as power amplifiers.

The nonlinear techniques are based on bifurcation detection of large-signal steady-state solution of the nonlinear circuits. The large-signal periodic solution can be efficiently obtained by harmonic balance simulation. In order to find the bifurcation of the large-signal solution and also to determine its stability, pole-zero identification and auxiliary generator are employed along with harmonic balance simulation. In Chapter 4, these stability analysis techniques will be described more in detail.

Chapter 3

Switching-Mode Power Amplifiers for ISM Applications

The high-efficiency power amplifier is a key component for various applications in the HF and VHF bands. The applications include plasma generation, RF heating, semiconductor processing, and medical imaging at industrial, scientific, and medical (ISM) frequencies such as 13.56, 27.12, and 40.68 MHz [41], [42]. FM transmitters for broadcasting also need high-efficiency power amplifiers. The output power level required for these applications is typically 1−50 kW. Solid-state power amplifiers are now replacing vacuum-tube power amplifiers up to the 5-kW level as the transistor technology progresses. However, it is hard to achieve such an output power from a single transistor, and thus the power amplifier needs an efficient power-combining structure.

The distributed active transformer (DAT) has been proposed as an efficient way to combine the output power from several push-pull amplifiers by connecting the secondary circuit of magnetically coupled 1:1 transformers in series [2]. It also provides each transistor with the output impedance transformation in order to boost the available power from the given device. The DAT was originally demonstrated for a CMOS integrated power amplifier. The power amplifier fabricated by a 0.35-μm CMOS process combined eight transistors using the DAT, and achieved 1.9 W output power with 41 % power-added efficiency at 2.4 GHz [43].

For ISM applications, the DAT is applied to a discrete amplifier with kilowatt-level output power, and is implemented by lumped elements. Several push-pull pairs of vertically double-diffused MOS (VDMOS), independently operated in Class-E/F_{odd} mode, are combined by the DAT. The DAT is built of two stacked copper slabs, which are thick enough to handle high current. The Class-E/F family has been proposed to take full advantage of both Class-E and Class-F^{-1} characteristics [1]. A 1.1-kW Class-E/$F_{2,odd}$ power amplifier was demonstrated at 7 MHz with a drain efficiency of 85 % [44].

In this chapter, two Class-E/F_{odd} power amplifiers using the DAT structure are presented at 29 MHz. One exhibits an output power of 1.5 kW with a drain efficiency of 85 % from two push-pull pairs. The other combines four push-pull pairs and achieves 2.7 kW output power with 79 % drain efficiency. In order to simulate the amplifiers in harmonic balance simulator, the transistor is modeled based on an ideal switch with on-resistance and output capacitance. The DAT of the stacked copper slabs is also modeled by a magnetically coupled equivalent circuit. The parameters of the equivalent circuit are extracted as functions of the slab length after a series of measurements and curve fitting, and are optimized for satisfying the zero voltage switching (ZVS) condition.

3.1 Class-E/F_{odd} Operation with Distributed Active Transformer

Due to the distributed nature of the DAT and the symmetry formed between two adjacent pairs, the complete amplifier can be divided into several independent push-pull amplifiers for analysis convenience. The equivalent circuit of a single push-pull amplifier is shown in Figure 3.1 with a transistor modeled as an ideal switch in parallel with a capacitance C_s. L_m and L_{l1} represent a magnetizing and a leakage inductance of the output transformer with a finite coupling coefficient k, respectively. The leakage inductance of the secondary winding is absorbed in the detuning reactance X_L.

We can extend the analysis of Kee, *et al*. [1] to Figure 3.1 in order to find the condition of the fundamental load admittance required for satisfying the ZVS condition:

$$\begin{aligned} Y_{\mathrm{L}} &= \frac{1}{R_{\mathrm{L}} + jX_{\mathrm{L}}} = G_{\mathrm{L}} + jB_{\mathrm{L}} \\ &= \frac{2n^2 I_{\mathrm{DC}}}{\pi^2[1-\omega_0^2(C_{\mathrm{s}}+C_{\mathrm{r}})L_{l1}]V_{\mathrm{DC}}} - jn^2\left[\frac{\omega_0(C_{\mathrm{s}}+C_{\mathrm{r}})}{1-\omega_0^2(C_{\mathrm{s}}+C_{\mathrm{r}})L_{l1}} - \frac{1}{\omega_0 L_{\mathrm{m}}}\right] \end{aligned} . \tag{3.1}$$

Several important observations can be made about the load condition. Both G_{L} and B_{L} are functions of different circuit parameters: the leakage inductance, the capacitance in the resonant tank, as well as the transistor output capacitance. In a Class-E/$\mathrm{F}_{\mathrm{odd}}$ amplifier with an ideal output transformer, however, B_{L} is a function of a single parameter, that is, the transistor output capacitance [1]. The load susceptance in equation (3.1) compensates not only for the transistor output capacitance, but also for a deviated reactance in the resonant tank. The deviation from the ideal parallel resonance at the operating frequency ω_0 is caused by the leakage inductance. The required load susceptance may even be capacitive depending on the coupling coefficient of the transformer, while it is always inductive in an amplifier with an ideal transformer.

The fact that the load resistance should be positive in any case imposes a condition on the operating frequency as follows:

$$\omega_0 < \sqrt{\frac{1}{(C_{\mathrm{s}}+C_{\mathrm{r}})L_{l1}}} . \tag{3.2}$$

From equation (3.2), it is clear that the coupling coefficient of the output transformer should be maximized in order to increase the operating frequency for a given active device and a given Q-factor of the resonant tank. Note that equation (3.1) will be equal to the load condition for the ZVS in [1] and no frequency limitation will be presented by equation (3.2), if the transformer is ideal ($k = 1$).

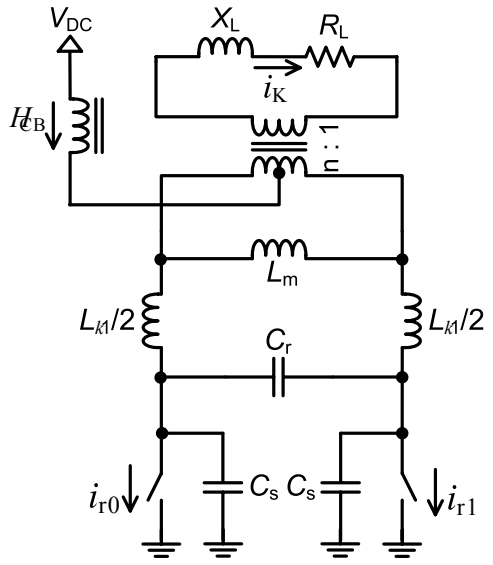


Figure 3.1: A Class-E/F_{odd} push-pull amplifier with a non-ideal output transformer.

3.2 Discrete Implementation of DAT

The DAT is implemented by two copper slabs with a cross section of 4.8 mm × 1.3 mm, stacked up together 10 mm above the ground plane as shown in Figure 3.2. The copper slabs are isolated from each other by an enamel coating on the surface. The lower slab behaves as the primary circuit of a 1:1 transformer. The two ends of the slab are connected to each drain of the transistors in a push-pull pair. The upper slabs of four push-pull pairs, serving as the secondary circuits, are connected in series. They present a 1:2N step-down impedance transformation of load impedance to each transistor, where N is the number of push-pull pairs combined. The DAT also combines the output power of 2N transistors by adding up AC voltages, magnetically coupled to the secondary circuits.

Since the output transformer gives the required inductances for resonance and detuning as well, it is imperative to model the transformer accurately for simulation. Figure 3.3 shows the equivalent circuit model of a unit section of the DAT, which corresponds to the output slab transformer of one push-pull pair in Figure 3.1. 4-port S-parameter measurements were

performed for slab transformers of different lengths with a network analyzer. The circuit parameters are then extracted as functions of the slab length by fitting the measured S-parameters to the simulated ones, shown in Figure 3.4. Note that only six S-parameters need to be fitted due to the reciprocity and the symmetry of the slab transformer. As expected, all circuit parameters are linearly proportional to the length except the coupling coefficient, which showed a constant value of 0.84. The extracted parameters are listed in Table 3.1. The parasitic capacitances between the slab and the ground are negligibly small. It also should be noted that the Q-factor of the copper slab is 600, so that the ohmic loss and the resulting heat problem can be drastically reduced, especially under the condition of the high current flow in this power amplifier.

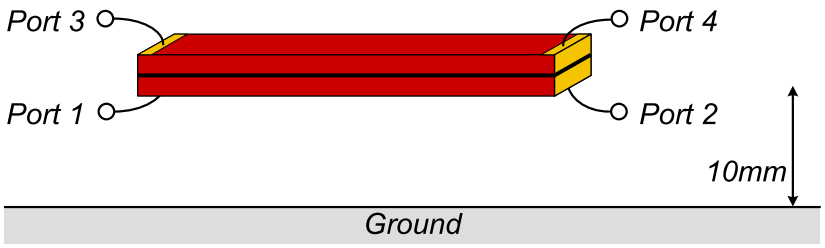


Figure 3.2: Structure of the slab transformer: a section of the DAT.

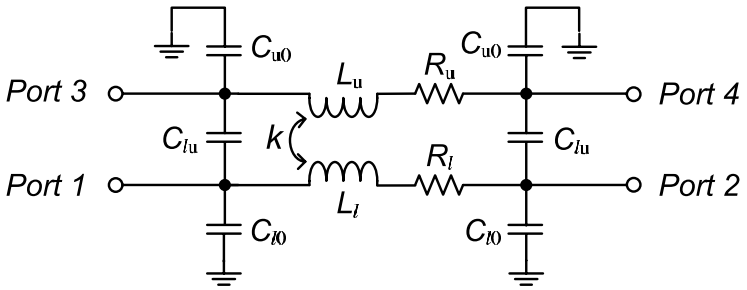


Figure 3.3: 4-port equivalent circuit model of the slab transformer.

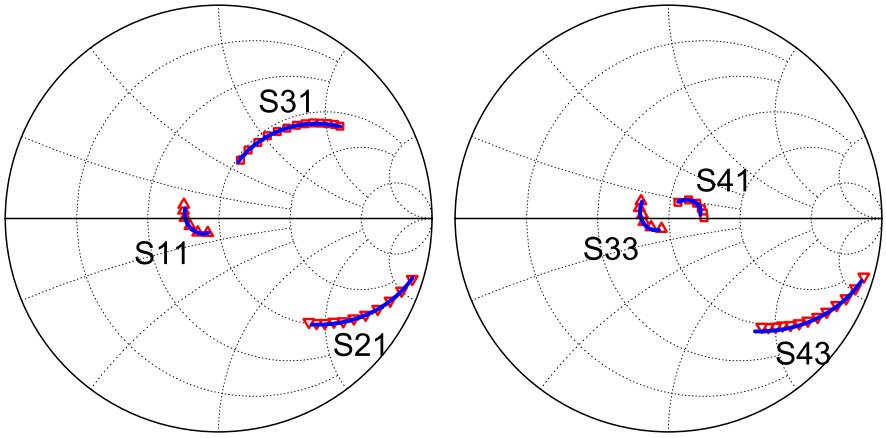


Figure 3.4: Measured (symbol) and simulated (line) S-parameters of the slab transformer: slab length of 7.5 cm, 50−200 MHz.

Table 3.1: Extracted result of slab transformer parameters

Parameters	Extracted result
L_u	4.7 nH / cm
L_l	4.3 nH / cm
C_{lu}	1.7 pF / cm
R_u, R_l	~ 1.3 mΩ / cm

3.3 1.5-kW, 29-MHz Class-E/F$_{odd}$ Amplifier with a DAT

A high-efficiency power amplifier is developed, based on the two important operating concepts, i.e., Class-E/F$_{odd}$ and DAT. The complete schematic of the amplifier is shown in Figure 3.5. Two push-pull pairs are combined by the DAT to achieve 1.5 kW at 29 MHz. Each pair is tuned to Class-E/F$_{odd}$ mode by output resonant capacitance C_{res} and magnetization inductance of primary circuit of the DAT. Due to the double-differential

driving characteristics [43], any two adjacent transistors including M_1 and M_4 are driven 180° out-of-phase. The input network consists of input matching circuitry and input-power distribution network. A 3:1 transformer and LC matching components are employed for the input matching. It should be noted that the transformer also serves as an input balun by grounding the center tap of the secondary circuit, so that a balanced signal is produced to drive push-pull pairs. The input-power distribution network is physical traces that distribute and deliver the balanced signal to each of four gate terminals. In order to correctly simulate and build the amplifier, the proper choice of active device and input-power distribution network along with their accurate modeling is essential.

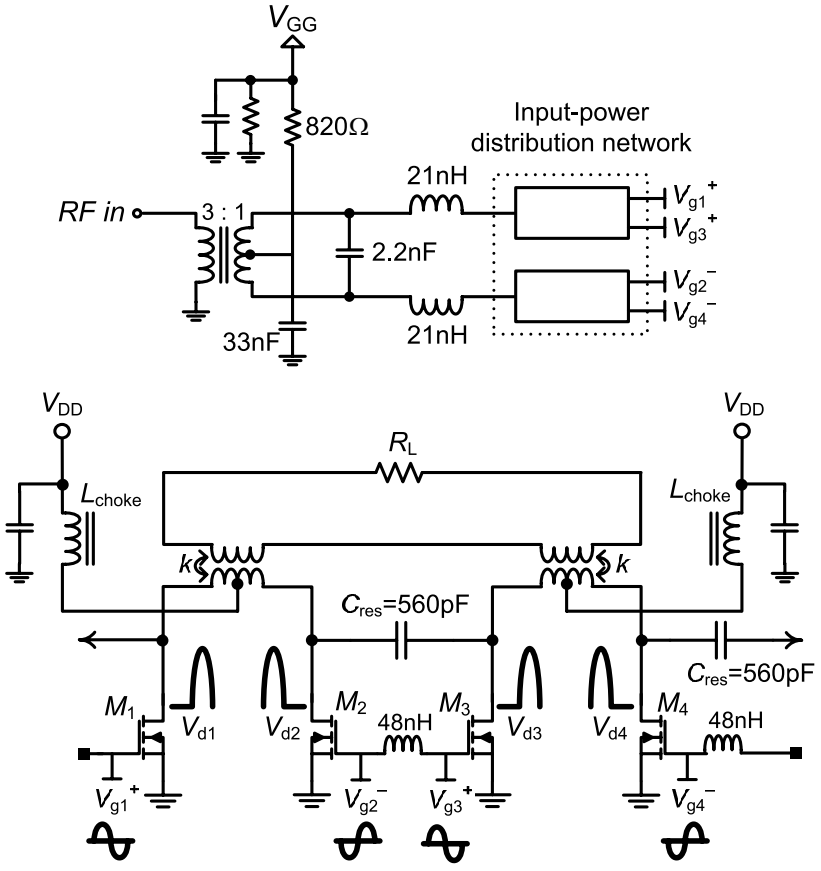


Figure 3.5: Complete schematic of a 1.5-kW, 29-MHz power amplifier. Desired voltage waveforms at gates and drains are represented.

3.3.1 Active Device

The amplifier employs the ARF473 VDMOS from Advanced Power Technology. It is a pair of matched power transistors in a common source configuration with 500 V of maximum drain-to-source voltage and 10 A of continuous drain current for each transistor [45]. To simulate the amplifier performance in harmonic balance, a nonlinear model of the transistor is indispensable. Due to lack of accuracy of vendor-provided model, the transistor has to be measured and modeled in-house. Fortunately, the input characteristic of the transistor is not required to model for predicting output power and drain efficiency. Thus the transistor is simply modeled by a switch with on-resistance R_{on} in series and nonlinear output capacitance C_{out} in parallel, as shown in Figure 3.6. R_d and L_d represent the transistor package parasitics that play important roles in simulation of high-frequency transient ringing [46].

The output capacitance and parasitics are extracted from measurements of the transistor by a HP 4194A impedance analyzer. The output impedance is measured for 1−100 MHz while gate bias is applied below the threshold voltage. Then, the transistor parameters are optimized such that the simulated impedance curve is fitted to the measured one. The extracted output capacitance is shown in Figure 3.7 as a function of drain bias. The nonlinear capacitance is implemented by a reverse-biased diode in the simulator. The parasitics are bias independent and show 0.4 Ω of R_d and 3 nH of L_d.

The on-resistance is extracted from DC I-V characteristics of the transistor. The inverse of the slope of I-V curves in the triode region is considered as sum of its on-resistance and parasitic resistance, since the operating point is located in the triode region when the transistor is on. Figure 3.8 shows the extracted on-resistance as a function of gate bias. When gate bias is very high, that is, when the transistor is completely turned on, the on-resistance is around 0.45 Ω.

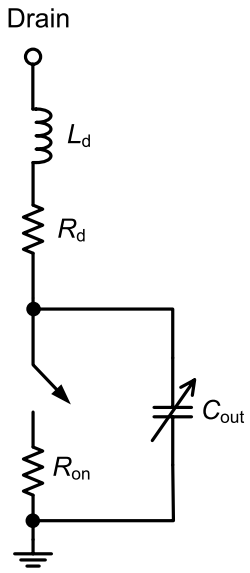


Figure 3.6: Simple switch model of the transistor used for amplifier simulation.

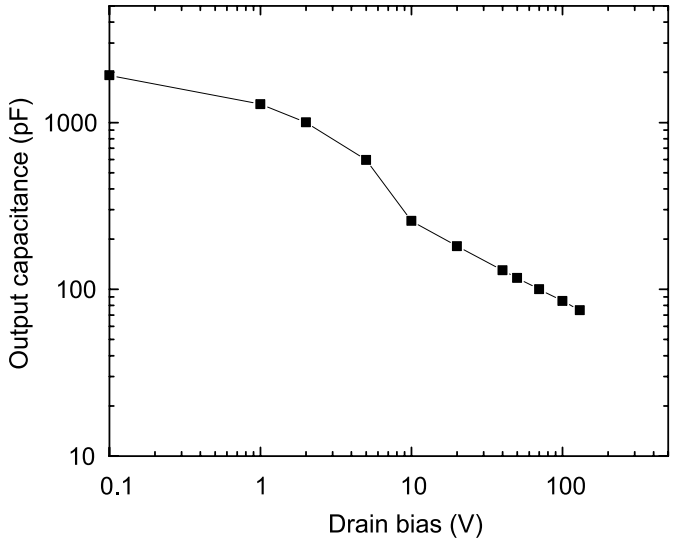


Figure 3.7: Extracted output capacitance of ARF 473 VDMOS.

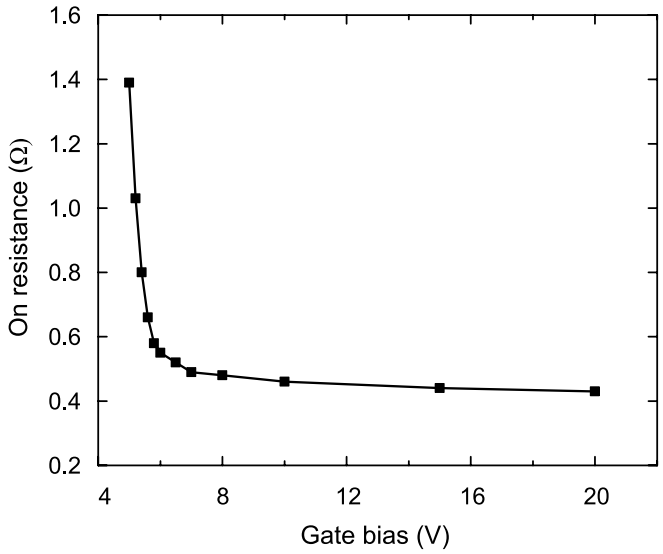


Figure 3.8: Extracted on-resistance of ARF 473 VDMOS.

3.3.2 Input-power Distribution Network

In order to fulfill Class-E/F_{odd} tuning at the output, not only two transistors in each push-pull pair, but also the two push-pull pairs each other should be driven by 180° out-of-phase signals. Hence it is imperative to generate a well-balanced out-of-phase signal from single-ended RF input and to distribute the signal to each gate terminal without perturbing the balance, that is, the 180° out-of-phase property. In particular, design of good input-power distribution network is very critical to achieve high drain efficiency. Unfortunately, the design is challenging because several physically long traces and their inter-connection are much more likely to break the balance of the drive signal.

In this amplifier, a multi-layered board is used to boost the balance of two input signals, 180° out of phase to each other. Each input signal is distributed to transistors through different layers as shown in Figure 3.9. Single-ended RF input is converted to balanced signals by the input balun. One signal is distributed to two gate terminals through the top layer indicated by blue, while the other through the middle layer indicated by cyan. Multi-

layered distribution traces eliminate the need to use air bridges that would be necessary to connect traces in a single-layered board and perturb the balance of signals. The multi-layered traces are simulated and optimized in an EM simulator, Sonnet [47], which gives a multi-port S-parameter of the input-power distribution network. This simulated S-parameter is plugged into the schematic of the amplifier for harmonic balance simulation. Figure 3.10 shows the simulated voltage waveforms at four gate terminals. It can be seen that all drive signals of the four transistors are well-balanced relative to each other, 180° out of phase.

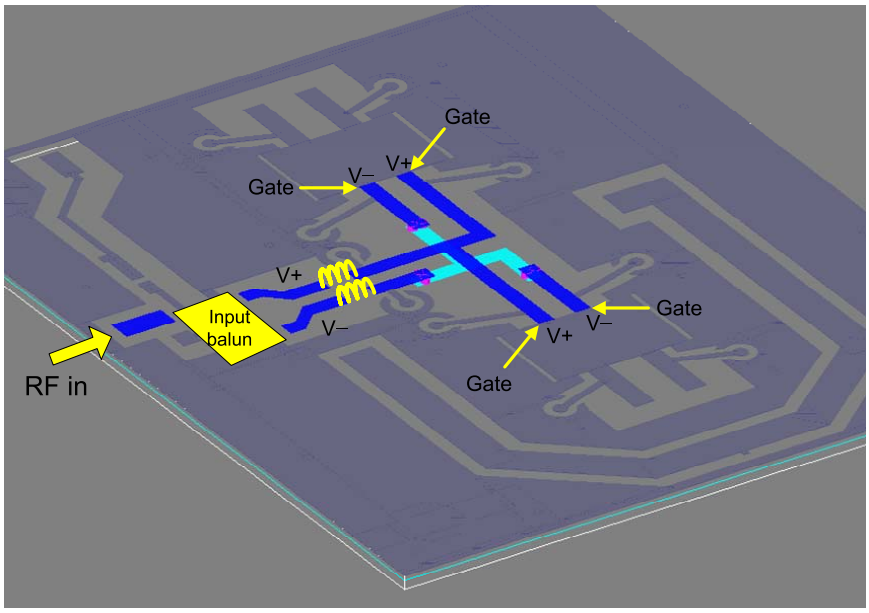


Figure 3.9: Input-power distribution network in a multi-layered board. Blue and cyan traces are on the top and middle layers, respectively.

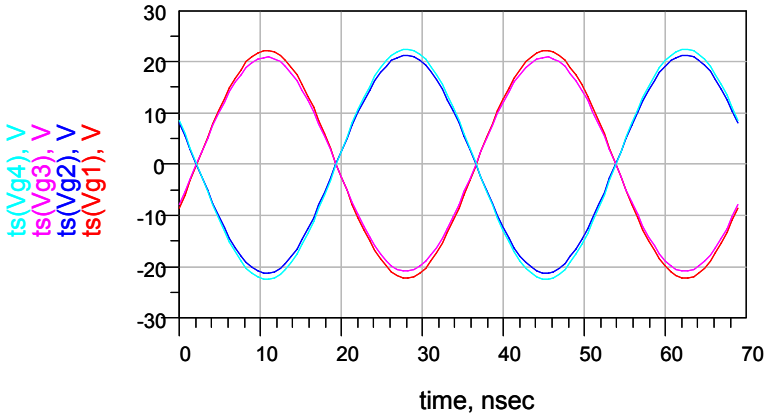


Figure 3.10: Simulated voltage waveforms at each of four gate terminals fed by input-power distribution network.

3.3.3 Performance Simulation

With accurate models of the DAT, transistor, and input-power distribution network together, the amplifier is simulated by harmonic balance. From the simulation, it is found that the output power and drain efficiency are strongly dependent on the parameters of the output resonant tank, particularly the magnetization inductance of the output transformer. Figure 3.11 shows the simulated output power and drain efficiency versus the copper slab length of the DAT. There exists an optimum length to achieve the highest drain efficiency, while the output power keeps a similar value around the length. For a length of 9.4 cm, the output power of 1.6 kW is predicted with the maximum drain efficiency of 87 % when the drain bias voltage is 110 V. It should be noted that the optimum length gives 40 nH of inductance to the resonant tank, which resonates along with 560 pF capacitance at the frequency higher than the operating frequency of 29 MHz. This mistuning of the resonator comes from the excessive susceptance component in equation (3.1) that is required to fulfill the ZVS condition.

The simulated voltage and current waveforms of a switch with 1.6 kW are shown in Figure 3.12. It can be easily seen that the ZVS condition is well-fulfilled. The high-frequency

ringing at VHF that is superimposed on the waveforms results from a parasitic resonance with package inductance and resistance [46]. However, it has small influence on the drain efficiency because the conduction angle of the two waveforms does not overlap each other.

Out of the total power loss of 13 %, the loss from transistors is the largest at 7.5 %, followed by the loss from capacitors in the resonant tank and the DAT, which is 3.3 % and 1.7 %, respectively.

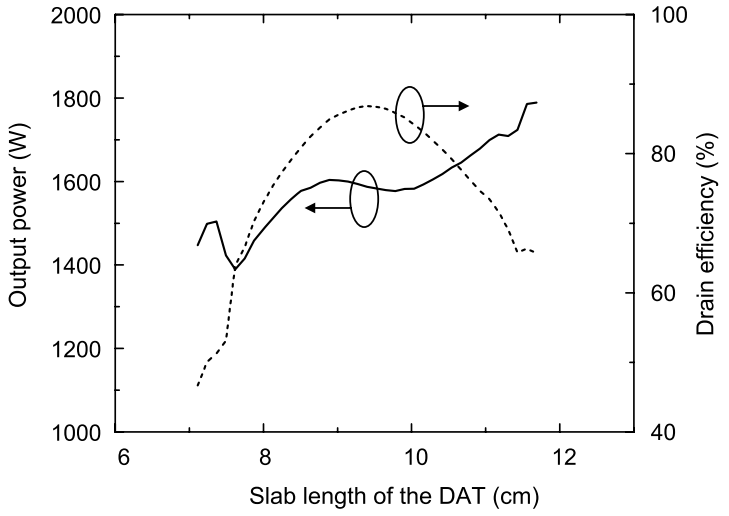


Figure 3.11: Simulated output power and drain efficiency versus slab length of the DAT.

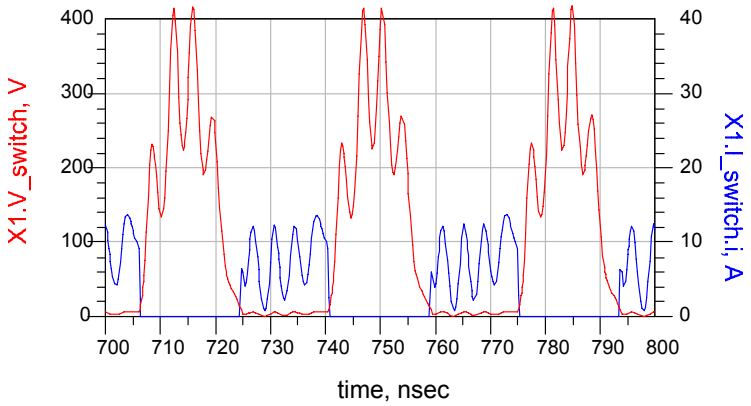


Figure 3.12: Simulated switch voltage and current waveforms for 1.6 kW output power.

3.3.4 Implementation of the Amplifier

The amplifier is constructed on an FR-4 circuit board, as shown in Figure 3.13. The transistor packages are mounted directly on a water-cooled heatsink. The 3:1 input transformer is built from a binocular powdered-iron core with three turns of wire. For the capacitor C_{res} in the resonant tank, an ATC 100E porcelain capacitor with a maximum working voltage of 2500 V and Q of 450 at 29 MHz is used. Since the DAT presents a balanced RF output, an external 1:1 output balun, B1-5K Plus from Radioworks, is employed for driving a conventional unbalanced load. The balun has a bandwidth of 2−50 MHz, a loss of 0.3 dB at 29 MHz, and a power rating of 5 kW at 3.5 MHz. Total circuit size is 15.2 cm × 12.2 cm.

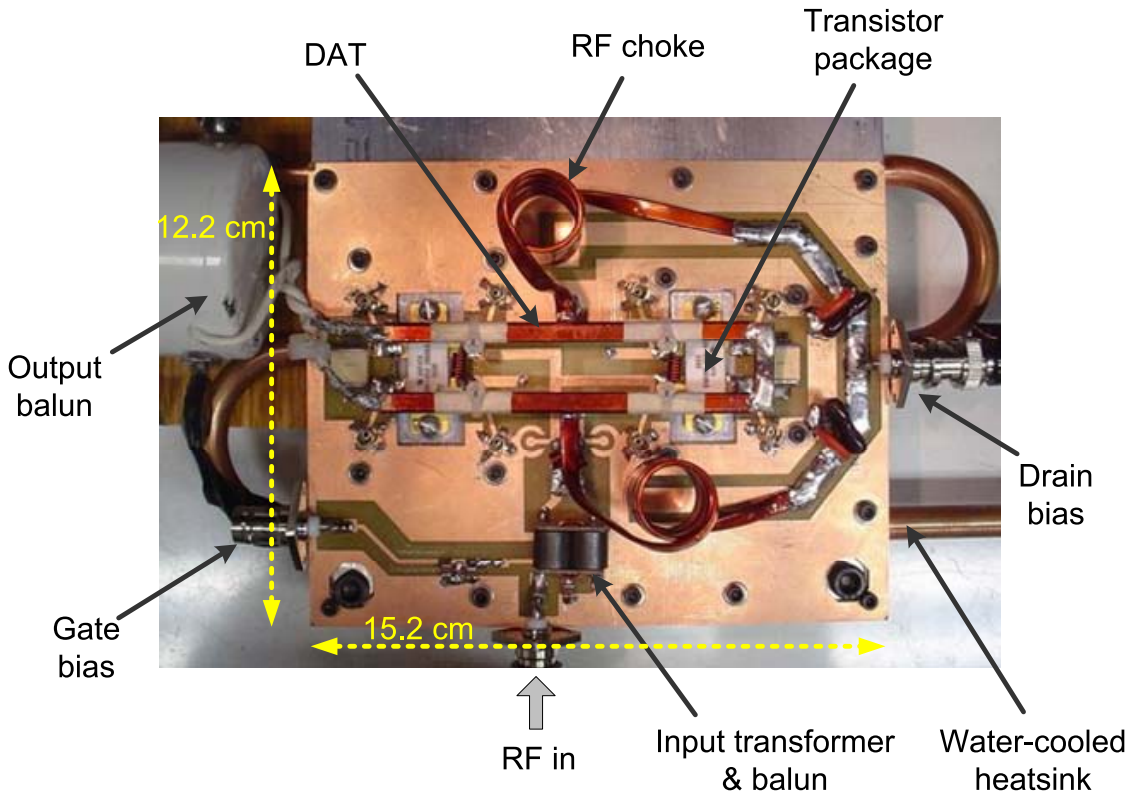


Figure 3.13: Photo of the 1.5-kW, 29-MHz power amplifier.

3.3.5 Experimental Results

Due to its huge output power level, special attention should be taken to build the measurement setup of the power amplifier. The complete block diagram of the measurement setup is shown in Figure 3.14. The RF input drive is applied by a Yaesu FT-840 transceiver. The input and output power of the amplifier is measured by Bird 4022 and 4024 power sensors respectively, which are connected to Bird 4421 power meters. Especially, the Bird 4024 power sensor can measure power up to 10 kW for 1.5−32 MHz. The output power is attenuated by a Bird 8329 oil-filled 30-dB attenuator and a JFW 20-dB attenuator in cascade. Then, the output spectrum is taken using an Agilent E4407B spectrum analyzer. The drain voltage is measured by a digital multimeter while a Hall-effect device is used to measure the drain current higher than 10 A. A 4-channel digital oscilloscope, Tektronix TDS3014B, is connected to each of the four drain terminals to monitor the drain voltage waveforms. All measurement instruments are controlled by National Instrument LabVIEW, so that all measurements are taken almost simultaneously with minimum time delay. It helps to minimize a possible thermal effect on the measured results of amplifier performance. The heatsink of the amplifier has meandering copper tubes through which water flows to extract heat from the amplifier. An external water pump is used for forced water flowing. The DC power supply is built by connecting several 12-V sealed lead-acid batteries in series, which turns out to be a decent DC source with low source impedance and low noise. Figure 3.15 shows a photo of the measurement setup.

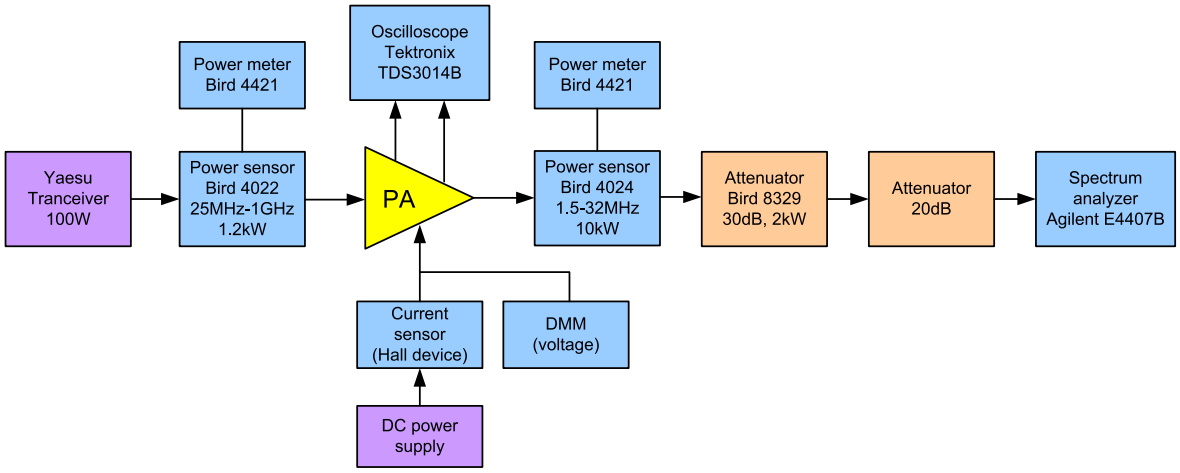


Figure 3.14: Block diagram of measurement setup for high-power amplifiers.

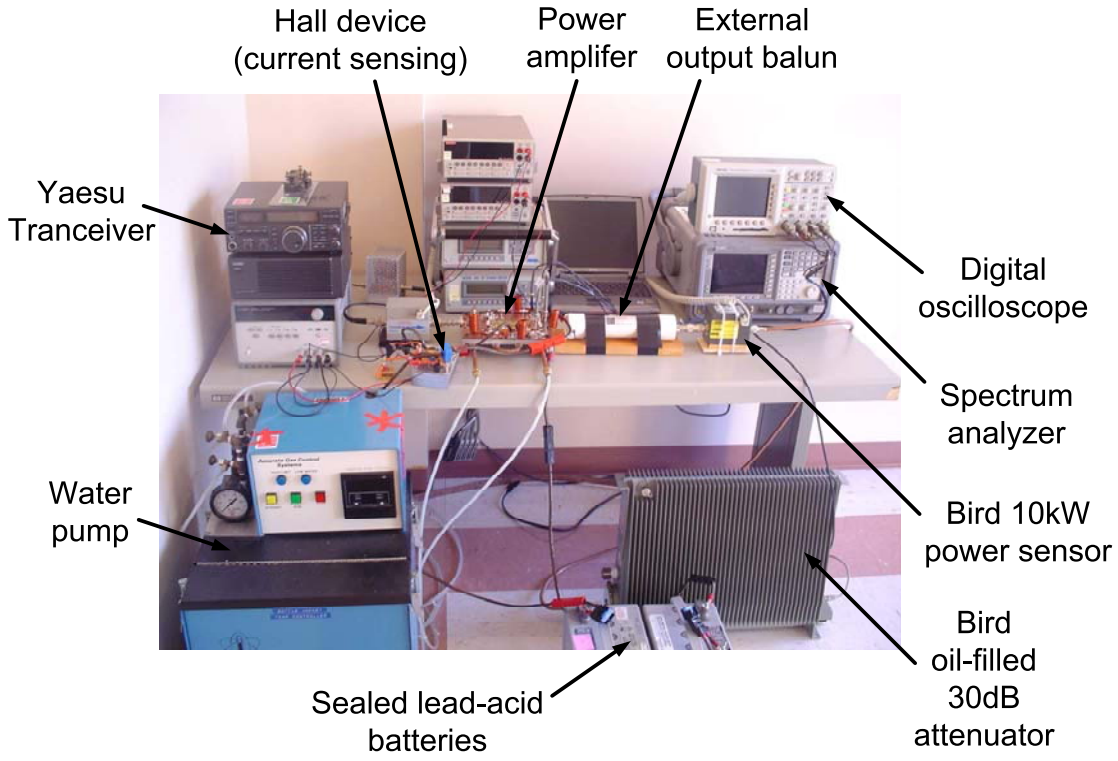


Figure 3.15: Photo of the measurement setup.

The measured drain efficiency and gain versus the output power is shown in Figure 3.16. The output power is varied by changing the drain bias voltage. The gain increases with the output power, because the input-drive power required for switching operation of transistors is not varied much with the drain bias. The drain efficiency also increases and is saturated in high output power. At a drain bias of 107 V, the maximum output power of 1.5 kW is achieved with 85 % drain efficiency and 18 dB gain. The input SWR is 1.6. Note that this measurement was taken when the input-drive power was large enough to make the transistors turned on and off completely, so that the desired Class-E/F_{odd} operation was ensured. With input-drive power below the optimum value, the amplifier showed interesting instabilities, which will be presented in Chapter 5.

The measured output spectrum for 1.5 kW is shown in Figure 3.17 (a). All even harmonics are more suppressed than odd harmonics due to the push-pull characteristic of the amplifier. The highest harmonic is the ninth with 32 dB below the fundamental. The peaks of the seventh and ninth harmonics result from the transient ringing exhibited in drain voltage waveforms in Figure 3.12. These peaks are also observed in the simulated spectrum, shown in Figure 3.17 (b). The accurate prediction of the transient ringing results from the appropriate modeling of transistor parasitics.

Figure 3.18 shows the measured voltage waveforms at two drain terminals in a push-pull pair. The two waveforms exhibit half-sinusoidal shapes and well-balanced characteristics, i.e., 180° out-of-phase and similar amplitude relative to each other. This confirms that the amplifier operates in Class-E/F_{odd} mode quite well, which leads to the high output power with high efficiency. The transient ringing can also be observed in the measured waveforms.

Finally, thermal characteristics are investigated when the amplifier operates in CW (continuous wave) for a long time. A thermal image of the amplifier is taken after it is driven at 1.5 kW output power for 30 seconds, as shown in Figure 3.19. The maximum temperature is exhibited at ATC 100E porcelain capacitors with 140 °C. The temperature of

transistor packages is well-suppressed to 73 °C max, which indicates that the water-cooled heatsink works in high performance to extract the heat generated inside the packages. Note that most of power dissipation and resulting heat generation occur in the transistor packages; 7.7 % out of 13 % total power dissipation in simulation. Also, a similar temperature between the two transistor packages verifies the balanced operation of each push-pull pair.

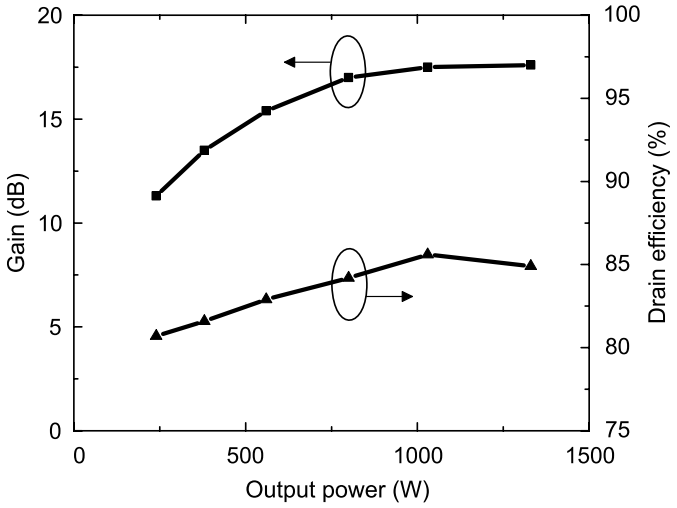
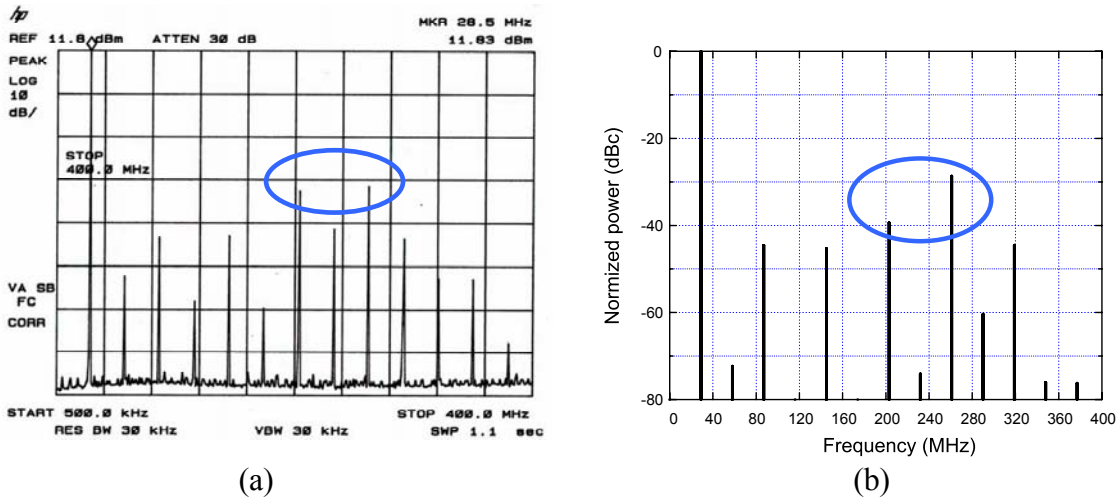


Figure 3.16: Measured gain and drain efficiency versus output power at 29 MHz.



(a) (b)

Figure 3.17: Output power spectrum for 1.5 kW. (a) Measured, (b) Simulated.

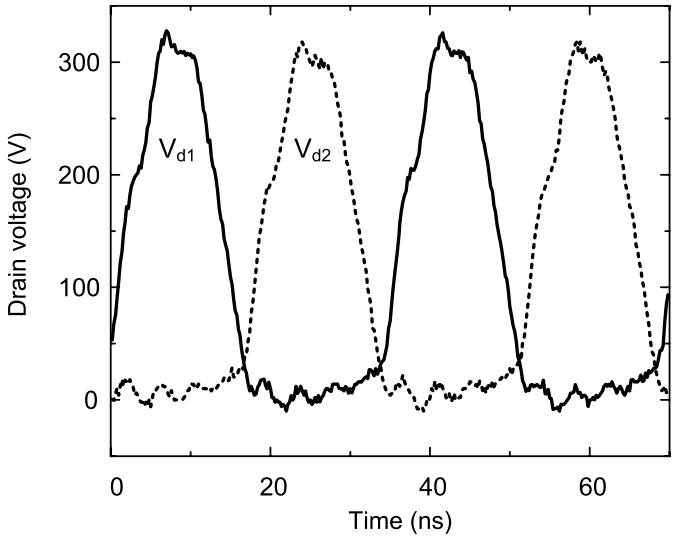


Figure 3.18: Measured drain voltage waveforms for 1.5 kW. Two drain terminals in the same push-pull pair are taken.

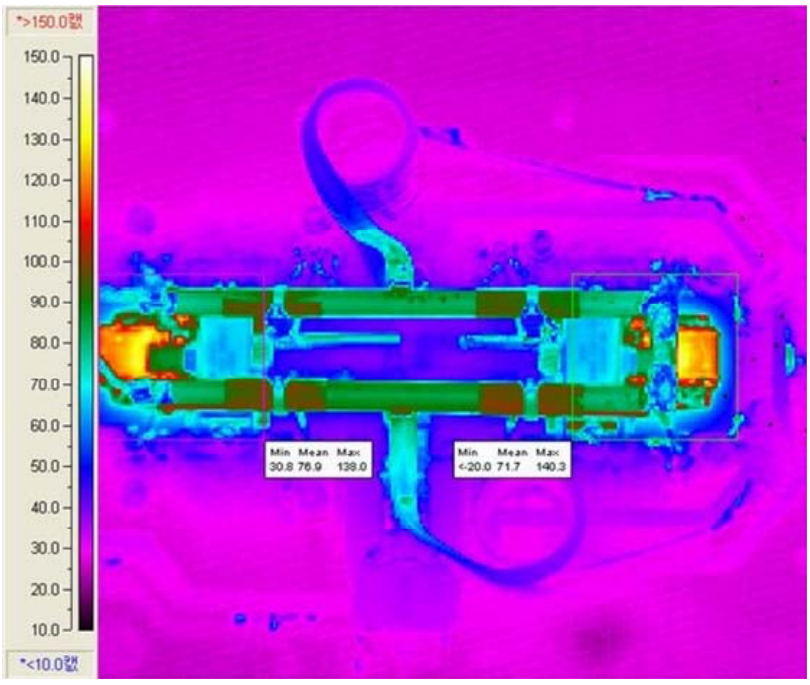


Figure 3.19: Thermal image of the amplifier driven at 1.5 kW for 30 seconds.

3.4 2.7-kW, 29-MHz Class-E/F$_{odd}$ Amplifier with a DAT

The design technique for the 1.5-kW power amplifier has been extended to obtain higher output power. For a 2.7-kW amplifier, four push-pull pairs are combined by a DAT instead of two. Each push-pull pair is independently tuned to Class-E/F$_{odd}$ as in the 1.5-kW amplifier. Also, the same models of the DAT and the active device are used for simulation. The complete schematic is shown in Figure 3.20, and each component value is listed in Table 3.2. The input-power distribution network is modeled in a multi-layered board and simulated in Sonnet, as in Section 3.3.2.

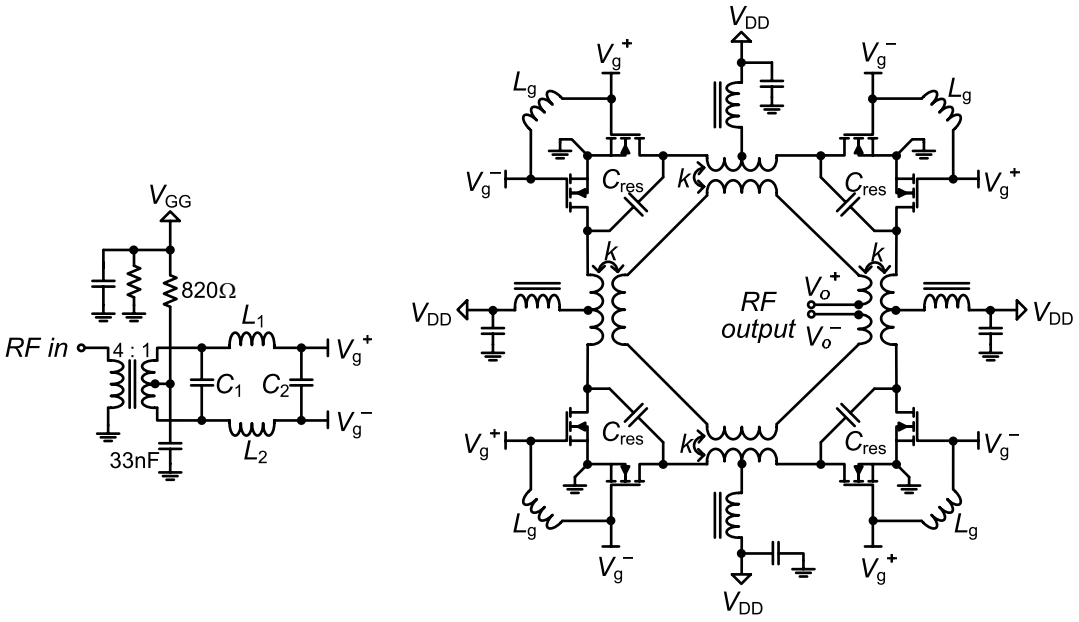


Figure 3.20: Complete schematic of a 2.7-kW, 29-MHz power amplifier.

Table 3.2: Component values of the power amplifier.

C_{res}	L_g	C_1	C_2	L_1, L_2
470 pF	48 nH	1770 pF	3300 pF	5 nH

3.4.1 Performance Simulation and Implementation

In the simulation, the value of C_{res} and the length of the output slab transformer are optimized to provide not only a parallel resonant tank at the operating frequency, but also the appropriate susceptance given in equation (3.1) for the ZVS condition. The simulation predicts a drain efficiency of 83 % at an output power of 2.7 kW. This includes a transistor loss of 13 %, a capacitor loss of 2 %, and an inductor loss in the slab transformers and the RF chokes of 2 %. In addition, an external output balun from Radioworks has a measured loss of 7 %, which means that the predicted overall drain efficiency will be 76 %.

The amplifier is built on an FR-4 board that is mounted on a water-cooled heatsink. Figure 3.21 shows a photo of the amplifier. The DAT forms a square structure of copper slabs and combines four transistor packages. Signal traces for the input-power distribution network stretch in a star shape, from the center point of the DAT to each gate of the transistors. Other circuit components are same as those of the 1.5-kW amplifier.

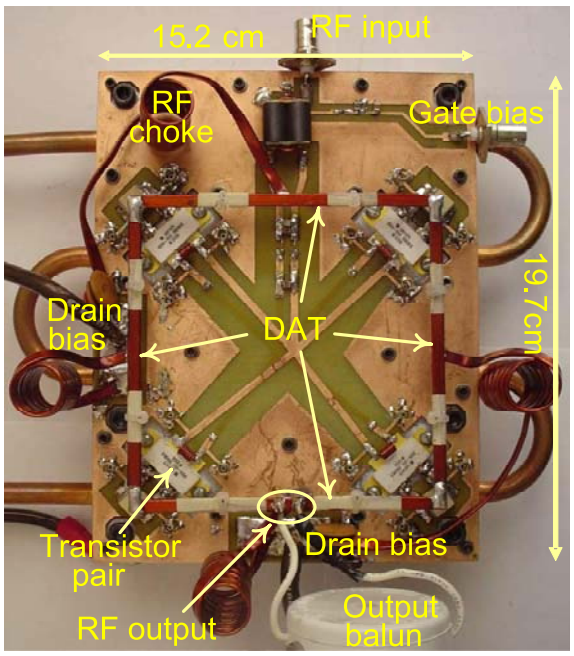


Figure 3.21: Photo of the 2.7-kW, 29-MHz power amplifier.

3.4.2 Experimental Results

The measured drain voltage waveforms of the eight transistors for 2.7 kW output power are shown in Figure 3.22, where the simulated waveforms of two transistors are superimposed. Good agreement can be seen between them. The visible good balance among the measured waveforms leads to high drain efficiency. The transient ringing observed in the waveforms results from the parasitic resonance among the transistor package inductance, the transistor output capacitance, and the capacitance in the resonant tank.

Figure 3.23 shows the gain and the drain efficiency versus the output power at 29 MHz. The drain efficiency stays above 80 % up to 2 kW output power. The gain increases with the output power, as expected in a switching amplifier. At a drain voltage of 83 V, an output power of 2.7 kW is obtained with 79 % drain efficiency and 18 dB gain. This compares with 76 % predicted drain efficiency. The input drive is 37 W and the input VSWR is 1.3.

The measured output power and input VSWR at a drain voltage of 72 V are shown as a function of input frequency in Figure 3.24. The output power exhibits a peak at the center frequency of 29 MHz, and the VSWR is better than 2:1 over a bandwidth of 1 MHz.

The measured output power spectrum of the amplifier for 2.7 kW is shown in Figure 3.25. The largest harmonic is the fifth, at 34 dB below the fundamental. Even harmonics are much lower than odd harmonics due to the push-pull operation of the amplifier.

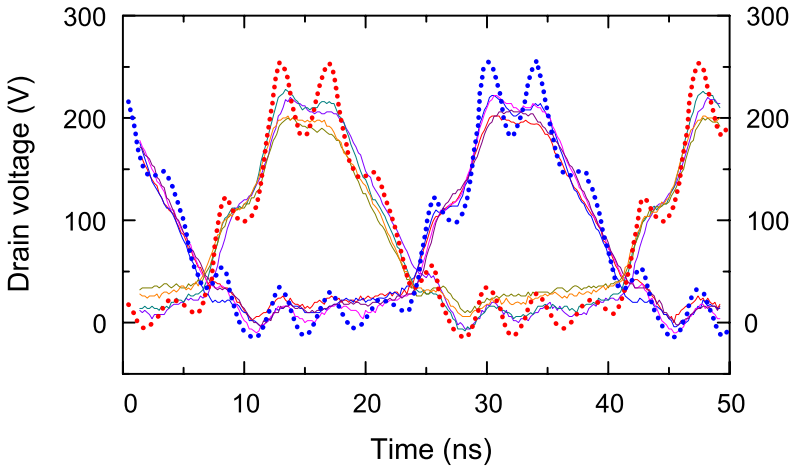


Figure 3.22: Measured (solid lines) drain voltage waveforms of eight transistors for 2.7 kW output power. Simulated (dotted lines) waveforms of two transistors are superimposed.

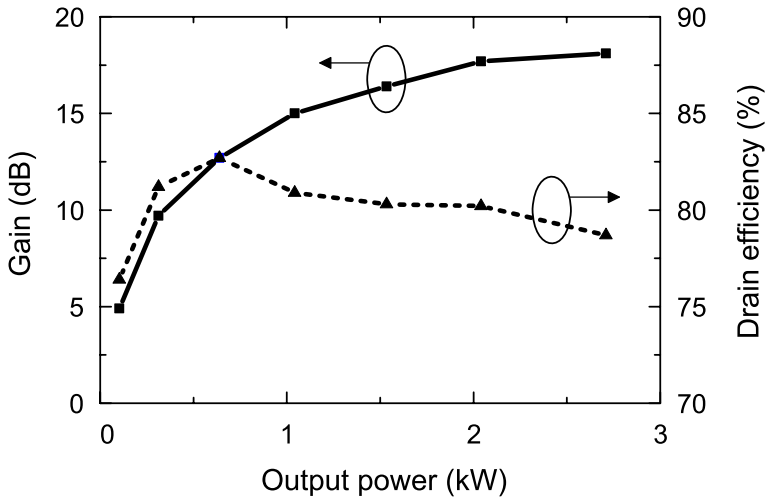


Figure 3.23: Measured gain and drain efficiency versus output power at 29 MHz.

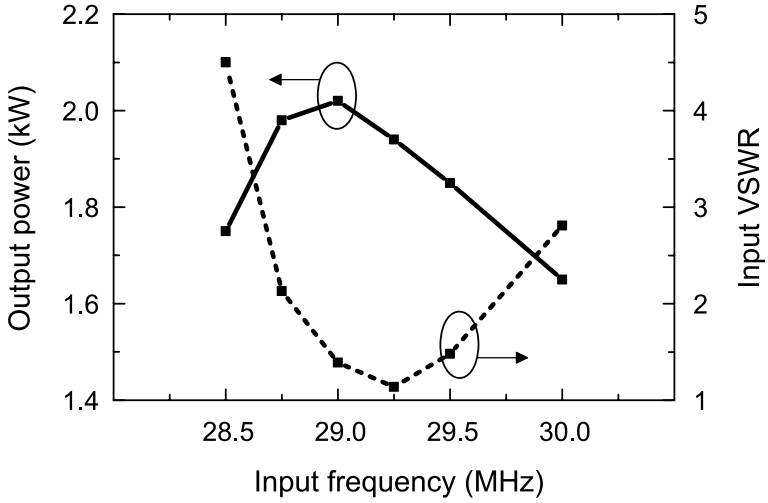


Figure 3.24: Measured output power and input VSWR vs. input frequency for a drain voltage of 72 V.

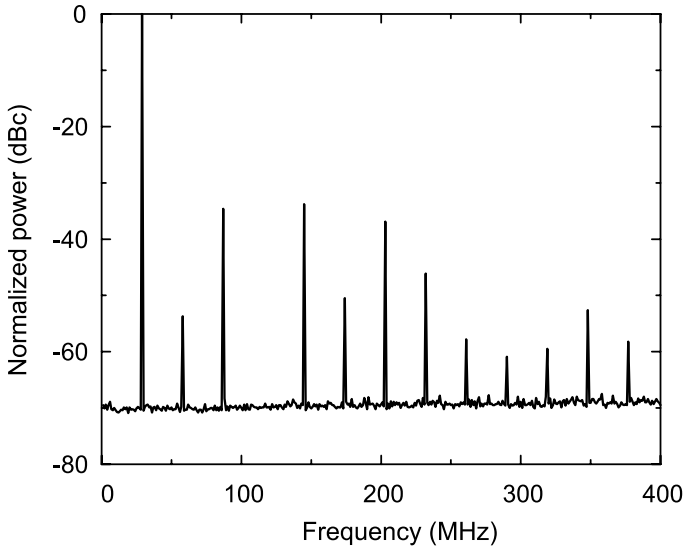


Figure 3.25: Measured output power spectrum for 2.7 kW. The harmonics power level is normalized by the fundamental.

Chapter 4

Nonlinear Stability Analysis Techniques

This chapter presents stability analysis techniques that are effectively applicable to predict and analyze the instabilities of power amplifiers. Since most of the instabilities shown in power amplifiers come from parametric oscillations [48], the instabilities are not presented when the amplifiers are only DC biased without any input-drive signal. On the other hand, when the input signal drives amplifiers, the large-signal periodic solution triggers instabilities. For this reason, the linear stability analysis is not appropriate for power amplifiers and nonlinear techniques are required instead. In this chapter, the conventional linear techniques and their limitations are briefly described first, and then, the nonlinear techniques are introduced.

4.1 Linear Stability Analysis Techniques

The conventional and widely used way to examine the stability is to investigate *k*- and Δ-factors of a two-port represented network of the circuit. The *k*-Δ factors are calculated as [49]:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{4.1}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \ , \tag{4.2}$$

where S_{ij} are linear S-parameters of the two-port network. Usually, the two-port network represents a transistor employed in the circuit. The unconditional stability, which means that

the circuit is stable no matter what passive terminations are presented in the input and output of the two-port network, is achieved when

$$k > 1 \tag{4.3}$$

and

$$|\Delta| < 1 \ . \tag{4.4}$$

On the other hand, in the case of a conditionally stable condition, the stability circles are useful to determine the stable range of input and output termination impedances for the two-port network. The center and radius of the input and output stability circles are also calculated as functions of linear S-parameters of the two-port network [49].

Although simple and powerful for checking the stability only with S-parameters, these linear stability analysis techniques have limitations when applied to nonlinear circuits like power amplifiers. Since the techniques are based on linear S-parameters given at a single bias condition, only the instabilities raised from the DC solution are detected. In other words, the linear techniques are unable to accurately predict the instabilities that originate from the large-signal periodic solution at input-drive frequency. Actually, when the circuit is pumped by a strong RF signal, the linear S-parameters at one bias point make no sense anymore in stability analysis. The RF signal will change the parameters of nonlinear circuit components, so that the S-parameters will also be varied periodically at the RF frequency. Hence, even with the conditions of (4.3) and (4.4) satisfied at a given bias point, power amplifiers may have instabilities in the large-signal periodic regime.

One might ask the question: What if the linear techniques are applied to multiple bias conditions that cover the whole range of the RF large-signal solution? Is this approach enough to check the stability of power amplifiers, taking into account the large pumping signal? Unfortunately, it is not true because of the parametric oscillation that is often shown in power amplifiers. The nonlinear reactance (mostly nonlinear capacitance) pumped by the large RF signal, exhibits negative resistance that gives rise to oscillation [48]. This parametric

oscillation is not predicted by the linear analysis techniques, because its analysis requires the inclusion of nonlinearity of the reactance components.

4.2 Nonlinear Stability Analysis Techniques

In order to overcome the limitation of linear techniques when applying to the stability analysis of power amplifiers, this section introduces nonlinear techniques that analyze the stability of the large-signal periodic solution obtained from harmonic balance simulation. Harmonic balance is an efficient method to approach the steady-state solution of nonlinear RF and microwave circuits in the frequency domain. Since state variables of the simulated circuit are expressed by the Fourier series, all of the frequency bases involved with the circuit operation must be pre-assigned before the simulation. The problem of harmonic balance, however, is that it may lead to a coexisting unstable solution to which the circuit never evolves. For example, when an amplifier has an oscillation at a different frequency than the input-drive, harmonic balance is unable to simulate the oscillating solution because the frequency basis of the oscillation is unknown and cannot be pre-assigned during the simulation. The solution obtained by harmonic balance will be an amplifier periodic solution without an oscillation, which is an unstable solution coexisting with the stable oscillating solution. Therefore, complementary techniques are required to check the stability of harmonic balance solutions and to obtain the stable one.

The important concept for the stability analysis is bifurcation that is defined as qualitative stability change when one or more circuit parameters are varied. At the bifurcations, a real pole or a pair of complex-conjugate poles of the system transfer function crosses the imaginary axis of the complex plane [37], [38]. There are plenty of types of bifurcation, but three bifurcations commonly observed in power amplifiers are shown in Figure 4.1: Hopf bifurcation, flip bifurcation, and D-type bifurcation. In Hopf bifurcation <Figure 4.1 (a)>, a conjugate pole pair crosses the imaginary axis at the frequency f_a that is not related with the input frequency f_{in}. So, the oscillation at f_a and its

intermodulation with f_{in} are presented in the circuit, as in Figure 2.17 (b). In flip bifurcation <Figure 4.1 (b)>, a conjugate pole pair crosses the axis at $f_{in}/2$ and frequency division by two occurs, as in Figure 2.17 (a). D-type bifurcation <Figure 4.1 (c)> has a real pole crossing the axis, so that no frequency variation is involved in this type. Instead, hysteresis and jump of solutions are shown in the circuit like Figure 2.17 (e). The nonlinear stability analyses in this section are based on detection of these bifurcations from the large-signal periodic solution of power amplifiers.

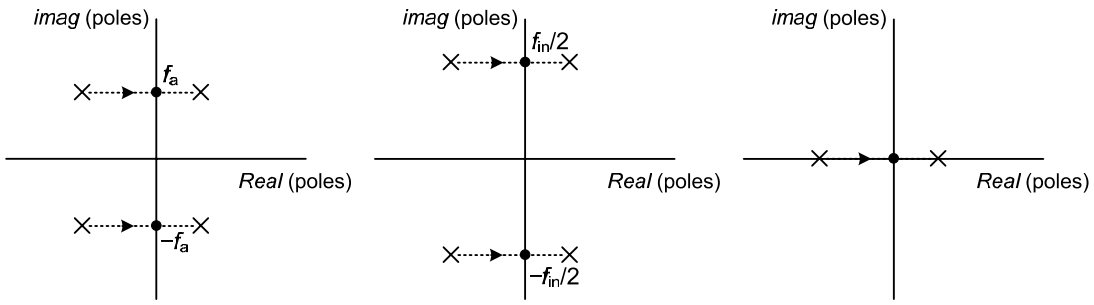


Figure 4.1: Three common types of bifurcation. (a) Hopf bifurcation. (b) Flip bifurcation. (c) D-type bifurcation.

4.2.1 Pole-Zero Identification

The first technique used for the bifurcation detection is pole-zero identification. The system poles and zeros are identified by fitting the single-input, single-output transfer function of the circuit, which is obtained from the large-signal periodic solution. When a series of identifications is carried out with some circuit parameters varied, it is possible not only to determine the stability of the solution at each of the parameter values, but also to find the value that leads to the bifurcation. Any circuit parameters can be chosen for the stability

analysis depending on designers' interest: input-drive power, input-drive frequency, bias voltages, circuit element values, etc. Figure 4.2 shows a representative example of identification results for a power amplifier when input-drive power is varied. In this example, Hopf bifurcation occurs at $P_{in} = 3$ W, from which a spurious oscillation is presented at f_{osc} in the output spectrum.

The question that arises now is how to calculate the single-input, single-output transfer function from the large-signal periodic solution. In [50], it has been proven that the impedance function, calculated at any circuit node looking into the circuit, serves as the closed-loop transfer function to which pole-zero identification is performed. Note that this impedance function has to be calculated under the large-signal periodic solution presented in the circuit. Figure 4.3 shows how to obtain the impedance function in harmonic balance simulators. A small-signal current source is connected to a node of the nonlinear circuit driven by input signal at f_{in}. Using the conversion-matrix approach [51], [52], the nonlinear components in the circuit are linearized around the large-signal harmonic balance solution at f_{in}. Then, the impedance function defined by

$$Z_{in}(\omega) = \frac{I_s}{V_s} \tag{4.5}$$

is calculated on the linearized circuit elements. V_s and I_s are the voltage and current of the current source, respectively. By sweeping frequency f_s of the current source, the impedance function is obtained as a function of frequency, which is used for pole-zero identification. In this dissertation work, STAN [53] has been employed for the identification process once the impedance function is at hand. Finally, it should be noted that judicious choice of the circuit node where the current source is connected is of importance to obtain a proper closed-loop transfer function. In principle, any node of the circuit provides a transfer function that has the same denominator, which means the same pole system [52], [54]. However, the circuit nodes close to active devices, such as gate or drain terminals, are sensitive to stability, so that they are the optimum nodes to probe the current source empirically.

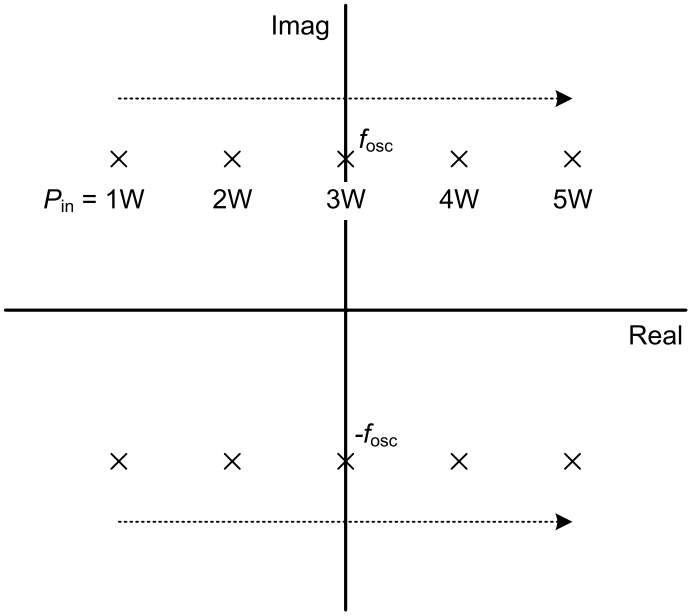


Figure 4.2: Example of pole-zero identification result.

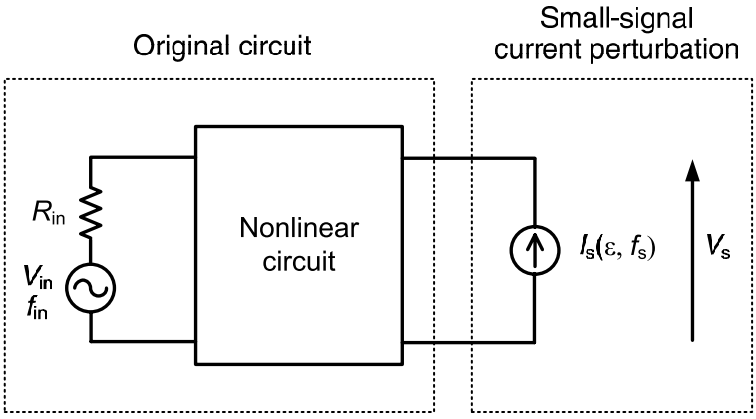


Figure 4.3: Schematic for obtaining the impedance function calculated from a large-signal harmonic balance solution.

4.2.2 Auxiliary Generator

An auxiliary generator (AG) is another versatile method to analyze the stability of steady-state solutions obtained from harmonic balance simulation. As mentioned earlier,

harmonic balance has difficulty in predicting an oscillation at unknown frequency due to the failure to provide the frequency basis of the oscillation. So, harmonic balance simulation converges to an amplifier periodic solution that is unstable and so unobservable in real. The auxiliary generator is a technique to circumvent this difficulty by assigning the oscillation frequency and amplitude to harmonic balance simulation. The implementation of the auxiliary generator is shown in Figure 4.4. A nonlinear circuit is driven by an input signal of f_{in} and V_{in}, and is assumed to give an oscillation at a different frequency. The auxiliary generator consists of an ideal voltage source and an ideal bandpass filter in series [38]. The amplitude V_{AG} and frequency f_{AG} of the voltage source correspond to those of the oscillation signal. The ideal bandpass filter passes only the oscillation signal at f_{AG} and prevents the other signals from flowing into the original nonlinear circuit. By connecting this auxiliary generator to a circuit node in shunt, the frequency basis and amplitude of the oscillation can be loaded into harmonic balance simulation.

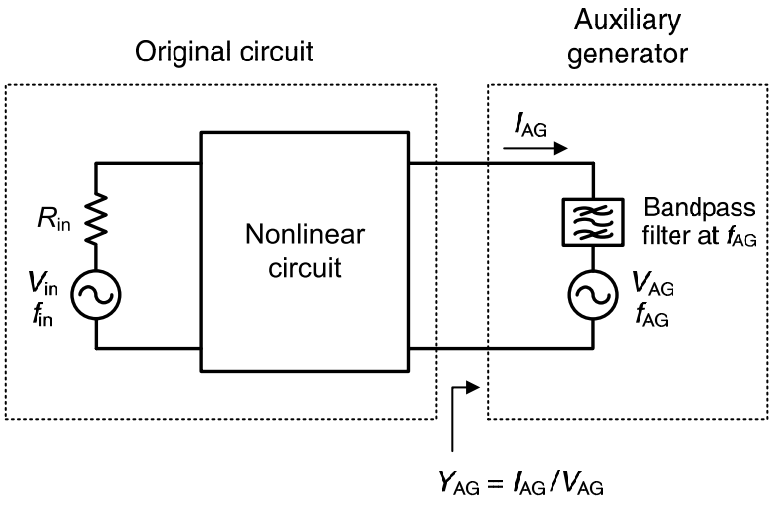


Figure 4.4: Implementation of an auxiliary generator in harmonic balance simulation. A nonlinear circuit is driven by a large input signal of V_{in} and f_{in}.

The next step is to determine the oscillation parameters, V_{AG} and f_{AG}, because they are still unknowns. Since the auxiliary generator is an artificial source added into the original circuit, it must not perturb the original harmonic balance solution that exists before connecting the auxiliary generator. This *non-perturbation condition* is fulfilled when the input admittance looking into the auxiliary generator is zero at f_{AG}:

$$Y_{AG} = \frac{I_{AG}}{V_{AG}} = 0 \ , \tag{4.6}$$

where I_{AG} is current flowing into the auxiliary generator. The equation (4.6) is solved in combination with harmonic balance equations of

$$\overline{H}(\overline{X}) = 0 \ , \tag{4.7}$$

where $\overline{X}$ is a vector of state variables. Since equation (4.7) is a complete system of equations, which means the number of real variables is the same as that of real equations, two more real variables are needed to solve the simultaneous equations of (4.6) and (4.7). The auxiliary generator parameters, V_{AG} and f_{AG}, serve as those two real variables, and can be determined. Note that the phase of the ideal voltage source is not a variable in case of non-synchronized circuits [38]. In commercial harmonic balance simulators, the non-perturbation condition is solved by optimization or error-minimization, in combination with harmonic balance as the inner loop.

Using an auxiliary generator, a bifurcation locus, which is a boundary of stability, can be traced in a plane of two circuit parameters η_1 and η_2. At a bifurcation point, an oscillation just starts up, so that the amplitude of oscillation V_{AG} will be very small. Hence, the non-perturbation condition is solved in terms of f_{AG}, η_1, and η_2, with fixed $V_{AG} = \varepsilon$ (tiny amplitude):

$$Y_{AG}(f_{AG}, \eta_1, \eta_2) = 0 \ . \tag{4.8}$$

Here, η_1 and η_2 can be any circuit parameters that designers are interested in: input-drive power, input-drive frequency, bias voltages, circuit elements, etc. By sweeping one of the variables in equation (4.8), a locus is traced in terms of the other two variables. When the locus has a turning point or an infinite-slope point, the sweep parameter is changed to another and the equation is solved for the other two as well [38], [55], so that a complete locus is traced. An illustrative bifurcation locus is shown in Figure 4.5. In this locus, there are two infinite-slope points in terms of η_1 (marked by two dots), so the sweep parameter has to be changed to f_{AG} or η_2 at those points.

An oscillating solution curve inside the unstable operating region of Figure 4.5 can also be traced through the auxiliary generator technique. The oscillating solution curve is necessary for investigating the oscillation characteristics such as oscillating mode or possible hysteresis phenomenon. In order to trace it, the non-perturbation is solved for V_{AG}, f_{AG}, and one circuit parameter η_1:

$$Y_{AG}(V_{AG}, f_{AG}, \eta_1) = 0 \ . \tag{4.9}$$

Note that the oscillation amplitude V_{AG} is not a tiny value any more and has to be considered as one of the variables in equation (4.9). A switching-parameter algorithm should also be applied when sweeping a parameter. Figure 4.6 shows an illustrative oscillating solution curve obtained by solving equation (4.9), in which two bifurcations, hysteresis, and resulting jumps of solution are presented. Oscillation is generated or extinguished at the values of η_1 corresponding to the two bifurcation points, when the circuit parameter is increased. However, when the circuit parameter is decreased, the value of η_1 at which the oscillation is extinguished by *Jump2* is lower than the bifurcation point, which suggests a hysteresis phenomenon. It is very important to figure out the oscillation characteristics in order to devise an efficient way to eliminate the oscillation.

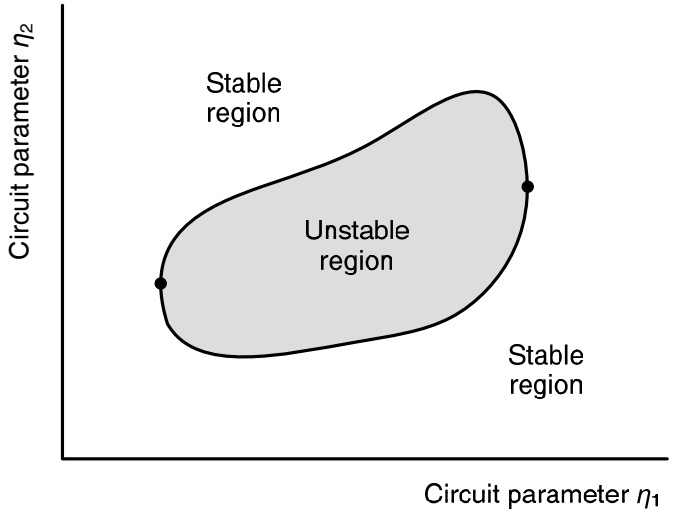


Figure 4.5: Illustrative bifurcation locus traced by the auxiliary generator technique.

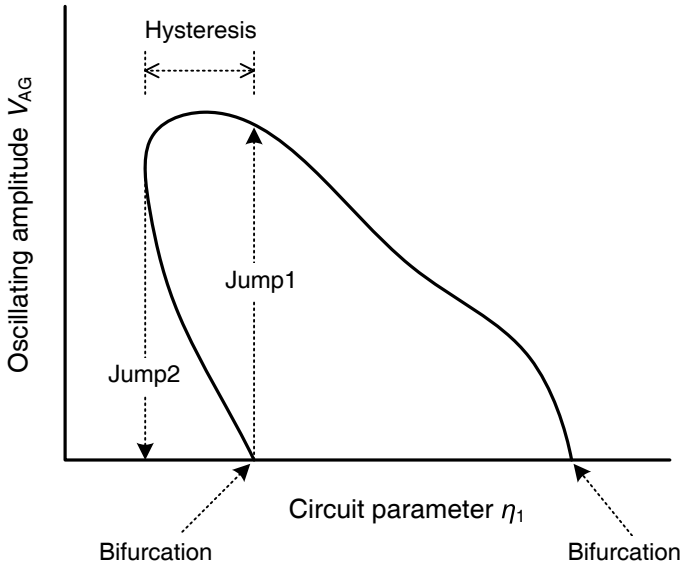


Figure 4.6: Illustrative oscillating solution curve traced by the auxiliary generator technique.

Chapter 5

Global Stability Analysis and Stabilization of a Class-E/F Amplifier with a DAT

During measurements of switching-mode amplifiers, several different operating behaviors can be observed. In particular, unstable behaviors are likely to be presented due to the strong nonlinearity, depending on input-drive level. Below a certain level of input power, the transistor is completely turned off and only leakage power from the input-drive source, passing through the feedforward capacitance of the transistor, is obtained at the output. For an intermediate input power range, the output power and drain efficiency of the amplifiers increase rapidly. However, it is also not unusual to observe spurious oscillations, sub-harmonic oscillations, or even chaos when the amplifiers are not completely stable [4], [35], [56]. As the input drive increases further to a high power level, the amplifiers show a typical switching amplifier operation with high drain efficiency.

In switching-mode amplifiers, the gain increase versus the input power for intermediate drive level, besides the negative resistance presented by nonlinear capacitances, may give rise to oscillations. These oscillations, observed from a certain level of input power, cannot be detected through a small-signal stability analysis of the circuit, such as the one based on the *k*-factor and the stability circles. Instead, a large-signal stability analysis must be performed through the techniques in [57], [58], [59] and (or) in Section 4.2. The qualitative changes in

the observed spectrum, when varying the input power, are the result of bifurcations, or qualitative stability variations [60], taking place in the circuit.

In previous work, large-signal analyses of the mechanisms leading single-ended or power-combining power amplifiers (PAs) to unstable behavior have been carried out [57], [58], [59], [61], [62]. As an example, the frequency division by 2, commonly observed in power-combining amplifiers, has been related to odd-mode instabilities, favored by the symmetries of the circuit topology. The analyzed amplifiers were operated in either Class-A or Class-AB. No similar study has ever been attempted in the case of switching amplifiers. To devise a proper stabilization procedure for these amplifiers, an understanding of the oscillation mechanism is necessary. This study will be carried out here through the use of accurate stability and bifurcation analysis tools presented in Section 4.2.

In particular, stability of the 1.5-kW, 29-MHz Class-E/F_{odd} PA designed in Section 3.3 will be analyzed in detail. The amplifier operates properly with high efficiency when the input-drive level is high enough to saturate the amplifier. However, when the input power is decreased, the amplifier shows interesting instabilities including self-oscillation, chaos, and hysteresis. In this chapter, the instabilities will be characterized with regard to the bias voltage and the input power. The instability contour, in terms of these two parameters, will be obtained through a bifurcation-detection technique. Then, a suitable stabilization network will be designed in order to globally suppress the instabilities and be verified experimentally.

5.1 Instabilities of a Class-E/F_{odd} Power Amplifier

The power amplifier in Section 3.3 shows various instabilities as a function of input-drive power. The variation of the measured output spectrum at a drain bias $V_{DD} = 72$ V with different input-drive power is presented in Figure 5.1. As shown in Figure 5.1 (a), for low input power, only a leakage signal is obtained at the amplifier output. When the input power P_{in} reaches $P_{in\_1} = 5.5$ W, the output spectrum turns into the one in Figure 5.1 (b). The

continuity of this spectrum suggests chaotic behavior. Two peaks can be seen on each side of the fundamental line at the input frequency of 29 MHz. The distance from each peak to this fundamental line is about 4 MHz. As the input power is further increased, this kind of spectrum continues to be observed until the input power reaches $P_{in\_2} = 13.0$ W. From this value on, the spectrum becomes the proper one, shown in Figure 5.1 (c). The amplifier behaves in the expected switching mode with high drain efficiency as in the measurements in Section 3.3.5.

The reverse sense of input power variation has also been considered and we have found a hysteresis phenomenon. If the input power is reduced, the chaotic spectrum is observed until the value $P_{in\_3} = 5.3$ W is reached and a mixer-like spectrum is obtained. Thus chaos is observed for the input power below the value $P_{in\_1} = 5.5$ W, at which it had originated when increasing the power. As we decrease the power further from $P_{in\_3} = 5.3$ W, the amplifier behaves in a self-oscillating mixer regime. The input signal at 29 MHz (f_{in}) mixes with a self-oscillation at about 4 MHz (f_a) and gives the output power spectrum of Figure 5.2. It is interesting to note that the intermodulation products with even orders at the oscillation frequency, $f_{in} \pm 2nf_a$ (n: positive integer), are stronger than those with odd orders at this frequency, $f_{in} \pm (2n-1)f_a$. This is attributed to the common-mode oscillation in each push-pull pair, which will be discussed in more detail in Section 5.3.3. If the input power continues to be reduced, the oscillation vanishes at the input power $P_{in\_4} = 5.0$ W.

To summarize, as the input power increases, the amplifier undergoes bifurcations at the values $P_{in\_1} = 5.5$ W (jump to chaotic solution) and $P_{in\_2} = 13.0$ W (extinction of oscillation). When the input power decreases, the amplifier undergoes bifurcations at the values $P_{in\_3} = 5.3$ W (extinction of chaotic solution) and $P_{in\_4} = 5.0$ W (extinction of oscillation).

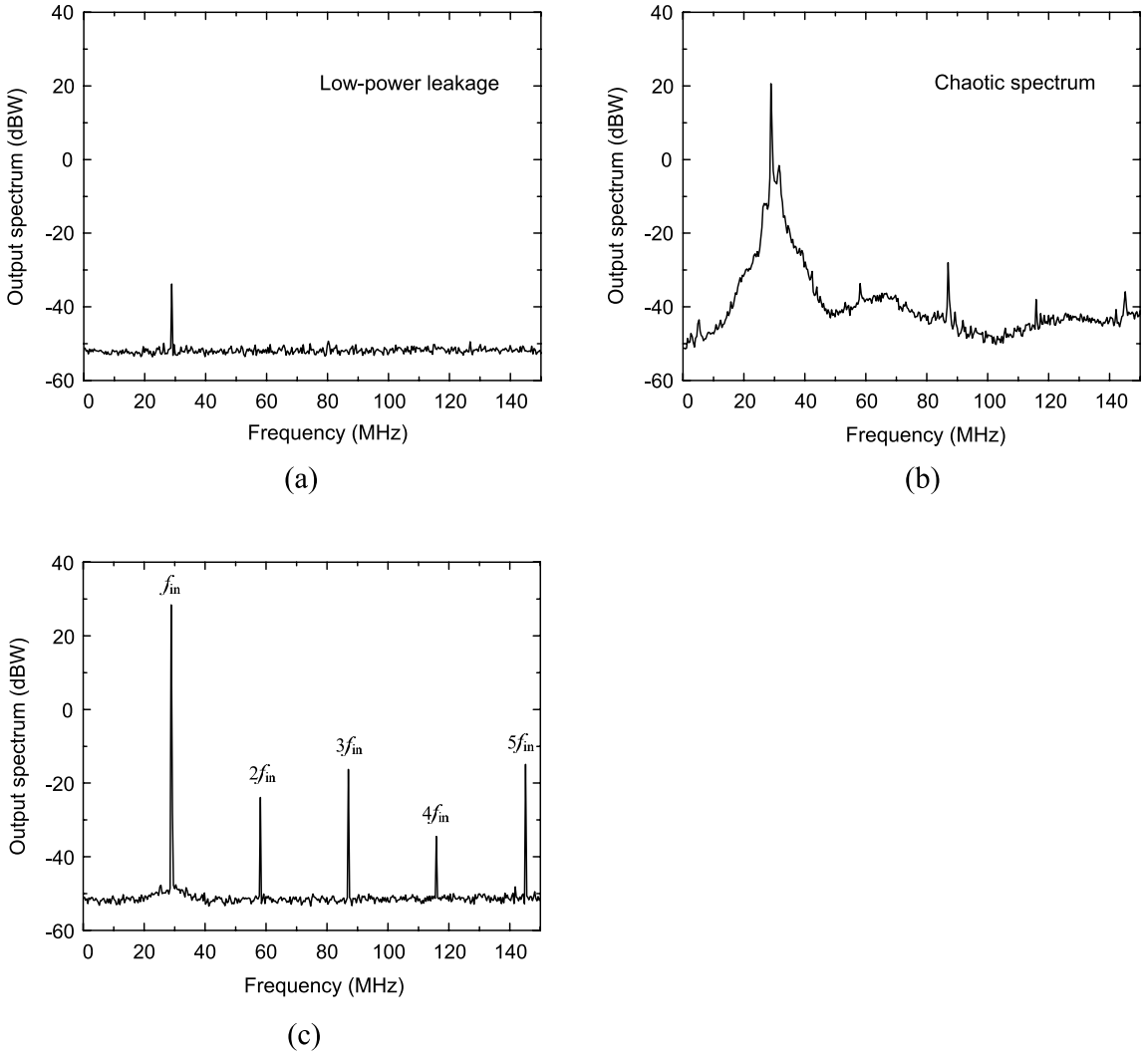


Figure 5.1: Variation of the output power spectrum when increasing the input power. (a) P_{in} = 4 W, showing leakage power at the input-drive frequency. (b) P_{in} = 10W, showing a chaotic spectrum. (c) P_{in} = 16.5 W, showing the proper spectrum in switching-mode operation.

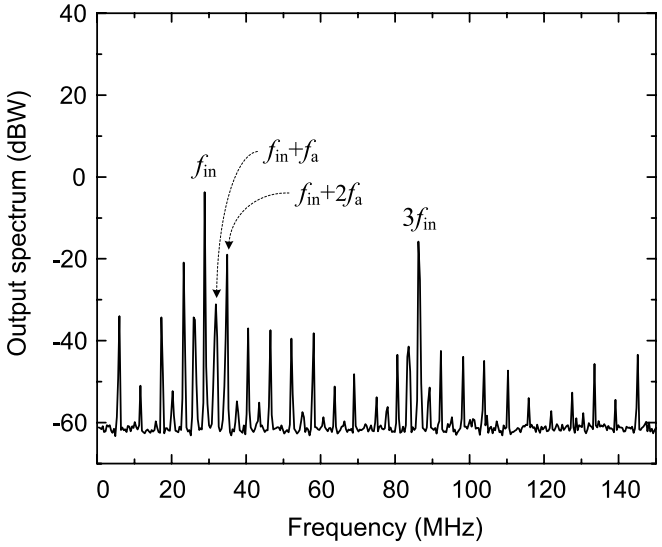


Figure 5.2: Quasi-periodic output power spectrum observed near the bifurcation boundary when the input power is decreased. The circuit behaves in a self-oscillating mixer regime, at the input-drive frequency f_{in} = 29 MHz and the oscillation frequency $f_a \approx 4$ MHz.

5.2 Transistor Modeling

One of the objectives of the work is to fully understand the different instability phenomena involving self-oscillation, chaos, and hysteresis that have been observed in the measurements. With this aim, stability and bifurcation analysis tools will be applied to the PA, in combination with harmonic balance. In order for the simulation tools to be successful, accurate models for the different linear and nonlinear elements will be necessary. Thus, special effort has been devoted to the transistor modeling.

The active device employed in the amplifier is the ARF473 VDMOS from Advanced Power Technology [45]. The transistor is modeled primarily as a voltage-controlled current source with two nonlinear capacitances [63], [64]. One is the drain-to-source capacitance C_{ds}. This is modeled as a reverse-biased diode, in which the parameters of the junction capacitance are fitted in order to match the measured capacitance as a function of the drain

bias voltage. The other is the feedback capacitance between the gate and the drain. The values of the feedback capacitance are extracted from the data sheet of the transistor, and a junction capacitance model is also used to fit the values. The gate-to-source capacitance is assumed to be constant as a first-order approximation [64]. The parasitic resistances and inductances at both gate and drain are also incorporated in the model as linear elements.

5.3 Stability Analysis

As shown in Section 5.1, different instability phenomena have been observed in the experimental characterization of the Class-E/F_{odd} amplifier, including self-oscillation, chaos, and hysteresis. Thus, the stability analysis of the amplifier will be a demanding one, involving different kinds of tools. The entire analysis procedure is presented in the following sub-sections.

5.3.1 Local Stability Analysis

The initial objective is to analyze the stability of the amplifier solution for several values of drain bias voltage and input power at which unstable behavior had been experimentally observed. Pole-zero identification presented in Section 4.2.1 is employed. This analysis is based on the linearization of the amplifier circuit about its large-signal steady-state regime at the input-drive frequency f_{in}, calculated with harmonic balance and 15 harmonic components. To obtain this linearization, a small-signal current generator is connected to a particular circuit node. Due to the complex topology of the amplifier circuit, different observation nodes must be considered. The generator operates at a frequency f, non-rationally related to f_{in}. The purpose of the generator is to enable the determination of the total impedance function Z_{in} at the frequency f, at the observation node. This is obtained by taking the ratio of the node voltage to the injected current, using the conversion-matrix approach [50], [52]. In this way, a

single-input, single-output transfer function is calculated, to which pole-zero identification will later be applied.

Initially, the operation conditions of $V_{DD} = 72$ V and $P_{in} = 10$ W, for which instability had experimentally been observed, were considered. By sweeping f and representing the real and imaginary parts of the admittance function $Y_{in} = 1 / Z_{in}$, a critical resonance at 5.6 MHz was found at the drain terminal of any of the four transistors. Negative conductance and a zero crossing of the susceptance with positive slope were obtained, which are the start-up conditions for an oscillation at that frequency [65].

For a more rigorous stability analysis, pole-zero identification was applied to Z_{in} [50]. Since all circuit nodes share the same denominator of the characteristic equation [54], the pole values are independent of the particular location of the current generator. However, exact pole-zero cancellations may occur at some current-generator locations. Thus, the need for the initial consideration of different observation nodes arises. Applying this technique, a pair of conjugate poles are found on the right-hand side of the complex plane, for the considered conditions of $V_{DD} = 72$ V and $P_{in} = 10$ W, confirming the unstable behavior (Figure 5.3).

Now the variation of the input power will be considered. When increasing the input power from a very small value, the critical poles evolve as shown in Figure 5.3. The amplifier solution is initially stable, with the poles located on the left-hand side of the complex plane. When increasing the input power, the critical poles cross the imaginary axis at $P_{in\_Hl} = 6.1$ W. From this power value, the amplifier periodic solution becomes unstable. At P_{in_Hl}, a Hopf bifurcation [37], [38] is obtained (the additional sub-index l means lower boundary). This Hopf bifurcation gives rise to the onset of an oscillation at the frequency 4.8 MHz, determined by the imaginary part of the poles. As the power continues to increase, the poles move further to the right, turn, and cross the imaginary axis again, to the left-hand side, at the input power value $P_{in\_Hu} = 13.5$ W (the sub-index u means upper boundary). At this power

value, the oscillation vanishes. This corresponds to an inverse Hopf bifurcation, occurring at P_{in_Hu}.

The above stability analysis provides the input-power range for which the amplifier periodic solution is unstable and thus unobservable. At P_{in_Hl}, an oscillation is generated, giving rise to a self-oscillating mixer regime. At P_{in_Hu}, the oscillation is extinguished and the amplifier recovers stability. Note that the stability analysis of the amplifier periodic solution does not enable, by itself, the prediction of the experimentally observed hysteresis phenomenon. Actually, in experiment, chaotic and mixer-like spectra had been found for the input power below P_{in_Hl} as well, which is not explained by the previous analysis. Hysteresis is associated with Hopf bifurcations of the subcritical type [38]. The determination of the bifurcation type requires higher-order derivatives of the circuit equations about the bifurcation point [66], which is beyond the scope of the paper. A different technique will be used in this work, to be shown in Section 5.3.4.

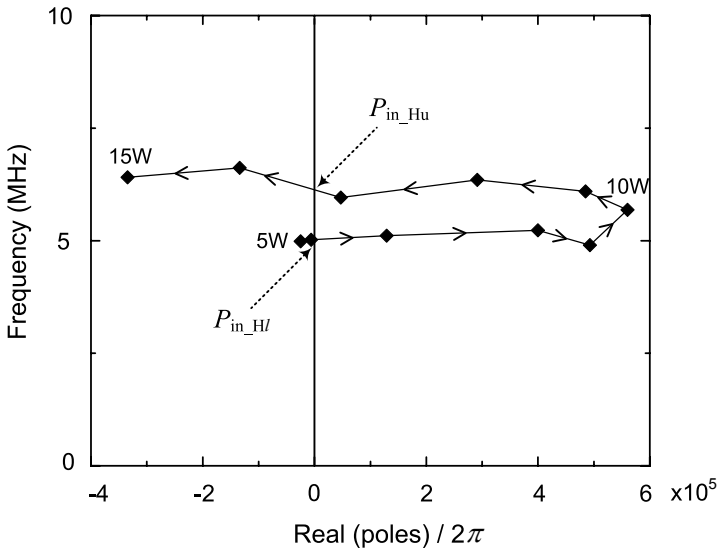


Figure 5.3: Evolution of the critical poles with increasing input power for V_{DD} = 72V. For simplicity, only poles in the upper half of the complex plane have been represented. The input power has been increased from 5 W to 15 W by 1-W steps.

5.3.2 Instability Contour

The amplifier circuits generally have one or more parameters, susceptible to variation in the different applications. The designer will be interested in knowing the parameter ranges that give rise to unstable operation of the amplifier. In the case of this amplifier, the parameters are the drain bias voltage V_{DD} and the input power P_{in}. Thus, the objective will be the determination of the set of (V_{DD}, P_{in}) values with unstable behavior. The set will be delimited by the Hopf-bifurcation locus, containing the points at which the oscillation is generated or extinguished, depending on the variation sense of the parameters [38].

To obtain this locus, the continuity of local bifurcations is taken into account, according to which the oscillation amplitude tends to zero at the Hopf bifurcation. Unlike previous work [58], the small-signal current generator, introduced in Section 5.3.1, will be used here to obtain the input-admittance function Y_{in} at the observation node. This generator operates at a frequency f, non-rationally related with f_{in}. The admittance Y_{in} is calculated as the ratio between the delivered current and the node voltage by means of the conversion-matrix approach. At the bifurcation point, occurring for $f = f_a$, both the real and imaginary parts of the input admittance vanish. This oscillation condition is fulfilled for oscillation amplitude tending to zero, as expected at the Hopf-bifurcation point. Thus, the Hopf-bifurcation locus, which delimits the unstable behavior region in terms of V_{DD} and P_{in}, is obtained by solving the following system:

$$Y_{in}(f_a, V_{DD}, P_{in}) = 0 \ , \tag{5.1}$$

with f_a being the oscillation frequency. The above system (5.1) is solved through error minimization or optimization, using harmonic balance with 15 harmonic components and the conversion-matrix approach. The goals are $Real\,(Y_{in}) = 10^{-18}$ S and $Imag\,(Y_{in}) = 10^{-18}$ S. There exist three unknowns, f_a, V_{DD}, and P_{in}, in the two equations given by the real and imaginary parts of Y_{in}. This gives a curve in the plane defined by the bias voltage V_{DD} and the

input power P_{in}. Note that the oscillation frequency f_a must be included in the calculation, as the frequency is autonomous and thus varies along the locus.

The application of the above technique to the Class-E/F_{odd} PA has provided the instability contour of Figure 5.4. The dashed line shows the input power variation, at V_{DD} = 72 V, considered in the pole-zero identification of Figure 5.3. The consistency in the bifurcation points resulting from both analyses should be noted. Through several applications of the pole-zero identification technique, the unstable region is confirmed to be inside the locus. The locus exhibits three points of infinite slope. To pass through these points, we switch the sweep parameter between V_{DD} and P_{in}. Thus, the entire contour has been traced, enabling accuracy in the determination of the unstable operation region.

In Figure 5.4, experimental points have been superimposed. In the lower border, two different sets of experimental points are represented. The triangles correspond to the points at which the amplifier becomes unstable for increasing input power. A chaotic regime is immediately obtained at most of the represented points, as shown in the spectra of Figure 5.1. The stars correspond to the oscillation extinction for decreasing input power. The two sets of points show the hysteresis phenomenon discussed in Section 5.1. On the other hand, in the upper border, no hysteresis has been experimentally obtained and only one set of measured points has been represented by squares. This set of points shows good agreement with the upper section of the simulated locus.

The instability contour provides the set of points at which the amplifier periodic solution becomes unstable, i.e., at which a pair of complex-conjugate poles cross the imaginary axis to the right-hand side of the complex plane. Thus, in the lower border, the contour must agree with the set of experimental points providing the instability threshold for increasing input power. As can be seen in Figure 5.4, the obtained locus enables a good prediction of this set of values represented by triangles. The prediction of the hysteresis interval demands a different procedure to be presented in Section 5.3.4.

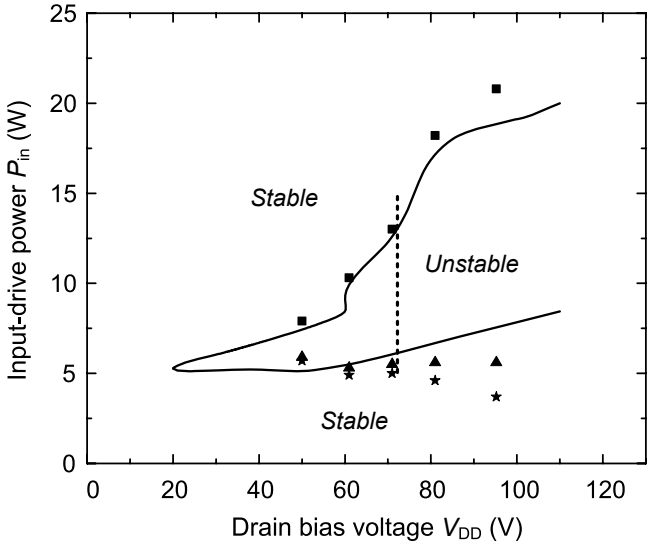


Figure 5.4: Instability contour (solid line). The Hopf-bifurcation locus delimits the V_{DD} and P_{in} values for which the amplifier periodic solution is unstable. Experimental points have been superimposed. Squares indicate the upper border. In the lower border, triangles indicate the onset of instability for increasing input power, whereas stars indicate recovering of stable behavior for decreasing power. The dashed line shows the input power variation in the pole-zero identification of Figure 5.3. Note that both analyses show good consistency in bifurcation points.

5.3.3 Analysis of the Self-Oscillating Mixer Regime

For understanding of the oscillation mechanism, a steady-state analysis of the circuit in its undesired self-oscillating mixer regime has been carried out. The oscillating solution will exist inside the instability contour of Figure 5.4. Due to the hysteresis phenomenon, it may also exist for input-power values below the lower border of the instability contour.

In order to obtain the oscillating solution in harmonic balance, a two-tone analysis must be carried out. One of the fundamentals is the input-drive frequency f_{in}. The other fundamental is the oscillation frequency f_a. By default, harmonic balance will converge to the amplifier periodic solution, with zeros at all spectral lines containing f_a. In order to avoid this,

an auxiliary generator (AG) is introduced into the circuit [38] for simulation purposes only. When choosing a voltage AG, this generator is connected in parallel at a circuit node. We will use the drain node, as in Section 5.3.1. The AG operates at the oscillation frequency, i.e., $f_{AG} \equiv f_a$, and must be an open circuit at all other frequencies. Thus, an ideal bandpass filter is used in series with the AG. Furthermore, the AG must not perturb the circuit steady-state solution. This is ensured by imposing a zero value to its current-to-voltage relationship $Y_{AG} = I_{AG} / V_{AG} = 0$, where I_{AG} and V_{AG} are the current and the voltage of the AG, respectively. For given V_{DD} and P_{in}, the amplitude V_{AG} and the frequency f_{AG} of the AG are calculated in order to fulfill the condition $Y_{AG}(V_{AG}, f_{AG}) = 0$. Even though the amplifier contains four transistors, only one AG, connected at one of the drain terminals, is necessary to determine the oscillating steady state.

To investigate the nature of the oscillation, the phase at each drain terminal of the four transistors has been analyzed at different harmonic frequencies (see Table 5.1). At the oscillation frequency f_a, the two transistors in the same pair are in phase, whereas the two pairs are 180º out of phase. However, at the input-drive frequency f_{in}, the original phase-shift relationships are maintained, i.e., 180º phase shift between the two transistors in the same pair and 180º phase shift between the two pairs as well. Other phase relationships exist at intermodulation products of the two frequencies. The oscillation can be understood as the result of the negative resistance exhibited by the transistor under relatively strong pumping signal and the resonant circuit formed with the equivalent capacitance and inductance seen from the drain terminals. This equivalent circuit will be discussed in detail in Section 5.4.

The two drain voltage waveforms in the same push-pull pair, V_{d1} and V_{d2}, are compared in Figure 5.5. It can be seen that the slowly varying envelopes at f_a are in phase whereas the fast-varying carriers at f_{in} show a 180º phase shift relative to each other.

Since the amplifier is operated in push-pull, the in-phase drain voltage waveforms at the oscillation frequency will ideally be cancelled, presenting no power in the output spectrum.

This explains why the intermodulation products of the form $f_{in} \pm (2n-1)f_a$, n: positive integer, are much more attenuated than those having the form $f_{in} \pm 2nf_a$, as can be seen in Figure 5.2. In a practical amplifier, however, no perfect cancellation can occur due to the imperfect symmetry.

Taking the above phase relationships into account, different virtual-ground and virtual-open planes can be considered in the circuit topology. At the input-drive frequency f_{in}, virtual-ground planes exist between any of two adjacent transistors. At the oscillation frequency f_a, two virtual-ground planes are located between the two push-pull pairs, as shown in Figure 5.6. In addition, two virtual-open planes develop at the symmetry planes of the pairs.

Considering these virtual-ground and virtual-open plane concepts, a simplified equivalent circuit at the oscillation frequency will be obtained in Section 5.4, which will be useful in efficiently finding the stabilization network.

Table 5.1: Phase of signals with different frequencies at each drain terminal of the four transistors ($V_{d1} \sim V_{d4}$ are defined in Figure 3.5).

Frequency	V_{d1}	V_{d2}	V_{d3}	V_{d4}
f_a	0°	0°	180°	180°
$f_{in}-f_a$	156°	−64°	−64°	156°
f_{in}	−71°	109°	−71°	109°
$f_{in}+f_a$	−86°	118°	118°	−86°

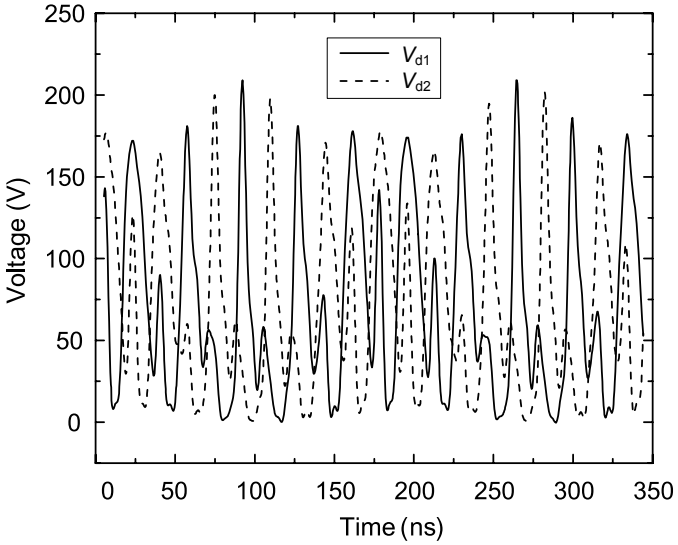


Figure 5.5: Comparison of two simulated drain voltage waveforms V_{d1} and V_{d2} in the same push-pull pair.

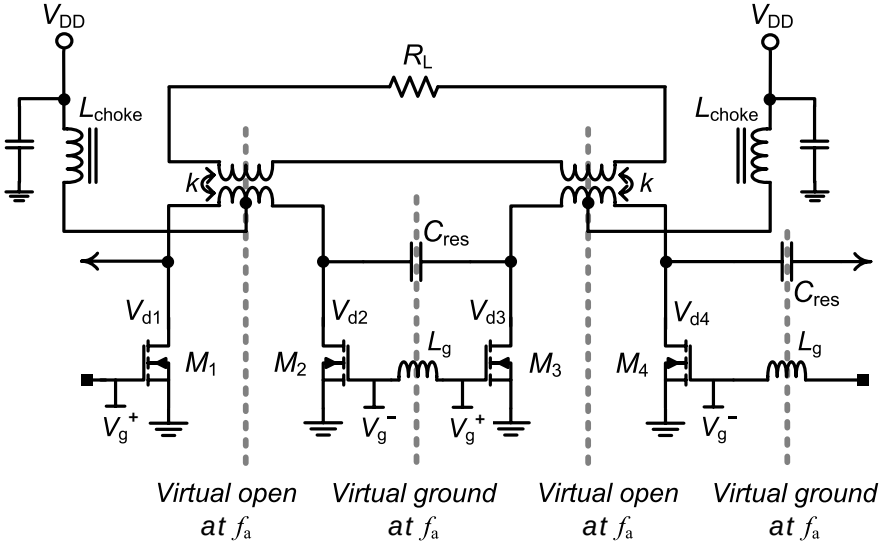


Figure 5.6: Schematic of the push-pull amplifier, showing the virtual-ground and the virtual-open planes at the oscillation frequency.

5.3.4 Hysteresis Prediction

To study the hysteresis phenomenon, the evolution of the self-oscillating mixer solution versus the input power will be analyzed. As in Section 5.3.3, an AG is connected to any drain terminal and the equation $Y_{AG}(V_{AG}, f_{AG}) = 0$ is solved versus P_{in}, in combination with harmonic balance. A two-fundamental frequency basis, at f_{in} and f_{AG}, the latter playing the role of the oscillation frequency f_a, must be considered in the harmonic balance simulation. The resulting variation of the oscillation amplitude at the drain terminal, agreeing with V_{AG}, is represented in Figure 5.7. A constant bias voltage $V_{DD} = 72$ V has been assumed. As can be seen, the curve exhibits an infinite-slope point or turning point *T*. To pass through this point, the sweep parameter has been switched to the oscillation amplitude V_{AG} in the neighborhood of the turning point, calculating the input power P_{in} and the oscillation frequency f_{AG} for each V_{AG} value.

The turning point is responsible for the hysteresis phenomenon. Actually, when the input power is increased, the transition from stable amplifier behavior to the self-oscillating mixer regime (J_1 in Figure 5.7) is due to a Hopf bifurcation H_l^1 occurring in the amplifier solution. When the input power is decreased, the transition back to stable amplifier behavior (J_2) is due to the turning point *T* in the self-oscillating mixer solution. Note that the simulated hysteresis interval, in terms of the input power, is in good correspondence with the experimental one shown in Figure 5.4. On the other hand, no hysteresis is obtained in the upper input-power range, delimited by H_u^1, which also agrees with the measurement results.

The hysteresis phenomenon is well-predicted by Figure 5.7. However, in the measurement, an abrupt transition from stable amplifier behavior to the chaotic regime occurred for most V_{DD} values, when the input power was increased. The study of this chaotic solution will require additional tools, to be presented in Section 5.3.5.

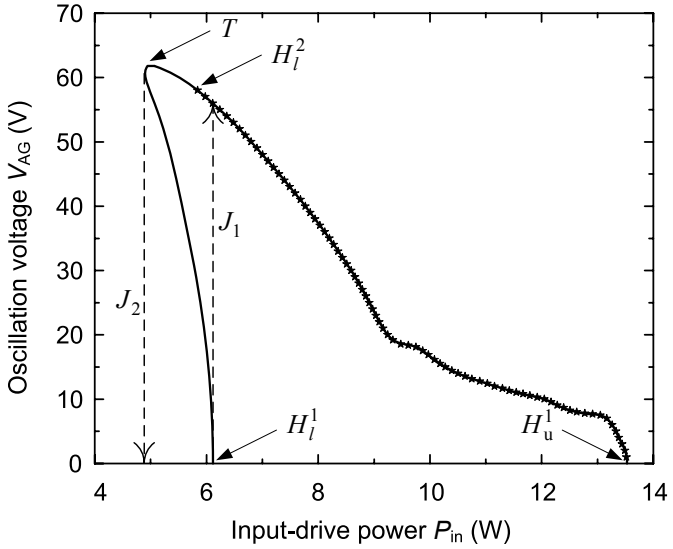


Figure 5.7: Simulation of the undesired self-oscillating mixer regime of the PA. Variation of the oscillation amplitude at the drain terminal is represented with the input-drive power. The points at which the different bifurcations occur are indicated. *H* stands for a Hopf bifurcation and *T* stands for a turning point. H_l^1 and H_u^1 are Hopf bifurcations from amplifier periodic regime. H_l^2 is a Hopf bifurcation from self-oscillating mixer regime. J_1 and J_2 indicate jumps of the solution. Chaotic solutions are observed from H_l^2, which is analyzed in Section 5.3.5.

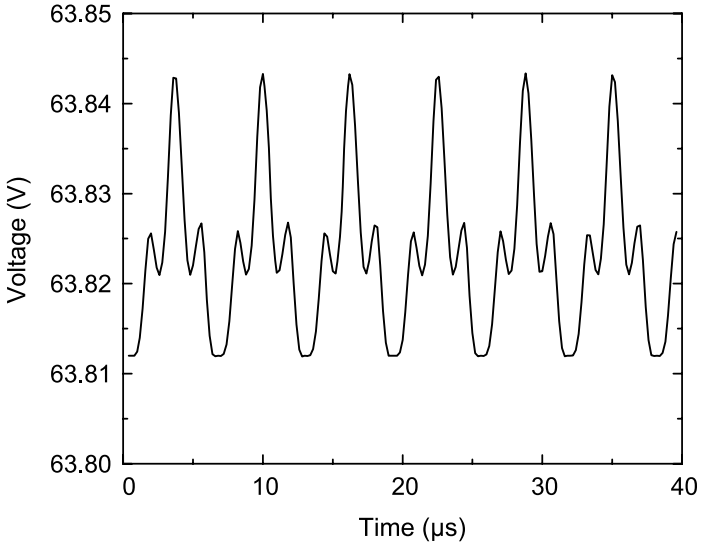
5.3.5 Envelope-Transient Analysis of the Oscillating Solution

The envelope-transient enables an efficient analysis of the regimes in which two different time scales may be distinguished. In this technique, the circuit variables are expressed in a Fourier series with time-varying coefficients and a differential-equation system is obtained in these coefficients [67], [68]. The technique is efficiently applied to forced circuits. However, when used for the simulation of an oscillating regime, like that of the unstable amplifier, it generally converges to the coexisting non-oscillating solution, in a similar manner to harmonic balance. To avoid this, the oscillation must be properly initialized [69]. This can be done through the connection of an AG to the circuit at the initial envelope time t_0. The amplitude and the frequency of the AG are determined through a

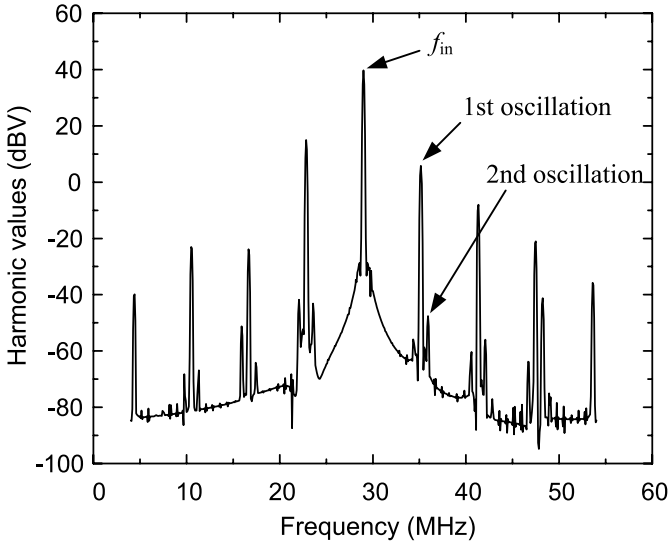
previous harmonic balance simulation. Since the AG is used for the initialization of the solution only, it must be disconnected from the circuit for time $t > t_0$. After this disconnection, the circuit will evolve according to its own dynamics. The AG disconnection from the circuit can be carried out with the aid of a time-varying resistor, in series with the AG [69], changing from zero to a very high value (ideally infinite).

The objective will be to analyze the circuit along the entire solution curve of Figure 5.7, corresponding to a self-oscillating mixer regime. Thus, the variables are represented here in a Fourier series, with f_{in} and f_{AG} as fundamentals, i.e., $\mathbf{x}(t) = \sum_{k,l} \mathbf{X}_{k,l}(t)\, e^{j2\pi(kf_{\text{in}} + lf_{\text{AG}})t}$. At each point, the AG amplitude V_{AG} and frequency f_{AG}, resulting from the harmonic balance analysis in Figure 5.7, are used for initialization purposes. From the point H_l^2 in Figure 5.7, the magnitude of the harmonic components $|\mathbf{X}_{k,l}(t)|$ becomes time-varying <Figure 5.8 (a)>. It oscillates at a few hundred kHz, the actual oscillation frequency depending on the input power. Thus, there is a second oscillation, in addition to the previous oscillation at about 4 MHz (f_{a}). Together with the input-drive frequency, this gives rise to a three-fundamental regime. The simulated spectrum is shown in Figure 5.8 (b). To verify this qualitatively, an expanded view of the experimental spectrum near the turning point T in Figure 5.7 is shown in Figure 5.9. This confirms the existence of the second oscillation at about 500 kHz, in agreement with the envelope-transient simulation, which has enabled the efficient detection of the second oscillation.

As has been shown, there are two autonomously generated fundamentals involved in the circuit solution, in addition to the input-drive frequency. According to the Ruelle-Takens theorem [60], this kind of solution is likely to give rise to chaos, which would explain the chaotic spectrum that was observed in the experiment <see Figure 5.1 (b)>. Actually, chaotic envelope variations have also been obtained in simulation for some values of input power. However, it should be noted that there is limited accuracy in the representation of these solutions using the two-tone basis f_{in} and f_{AG}.



(a)



(b)

Figure 5.8: Envelope-transient simulation of the amplifier. (a) Time-domain evolution of the magnitude of the f_{in} harmonic component of the drain voltage when a two-fundamental basis at f_{in} and f_a is considered. (b) Spectrum of the harmonic component, showing the presence of two oscillation frequencies.

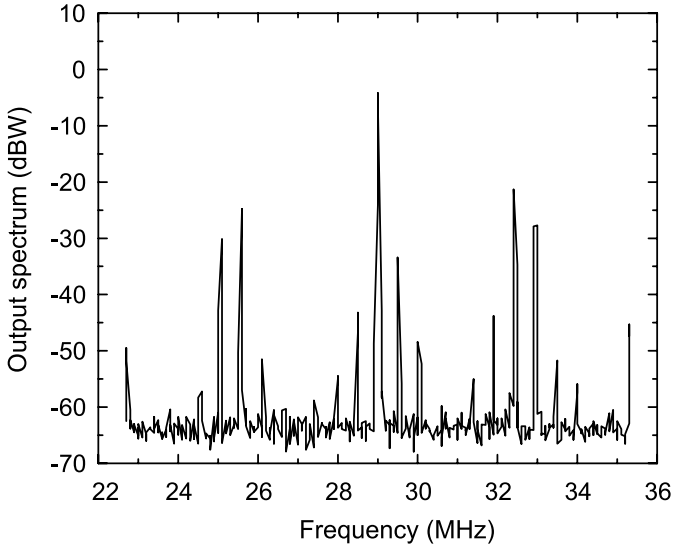


Figure 5.9: Expanded view of the experimental output power spectrum about the input-drive frequency. V_{DD} = 72 V and P_{in} = 5.15 W.

The interval in which the self-oscillating mixer solution at f_{in} and f_a is unstable has been indicated with stars in Figure 5.7. At the point H_l^2, the self-oscillating mixer solution becomes unstable, due to the generation of the second oscillation frequency. It is a Hopf bifurcation from the self-oscillating mixer regime. Thus, starting from very low input power, the amplifier periodic solution is initially stable, and as the input power is further increased, it suddenly becomes chaotic at the Hopf-bifurcation point H_l^1. This is because the input power for the bifurcation H_l^1 is larger than the input power for the bifurcation H_l^2, so the solution jumps from H_l^1 to the chaotic regime (see J_1 in Figure 5.7). The chaotic regime persists until the input power reaches the bifurcation point H_u^1, from which the amplifier periodic solution becomes stable.

When decreasing the input power, the second oscillation vanishes at H_l^2 and the self-oscillating mixer regime (at f_{in} and f_a) becomes stable for a very short input-power interval. At the turning point T, the system jumps to the stable amplifier periodic solution (J_2 in Figure 5.7).

In conclusion, the bifurcation diagram of Figure 5.7 gives a satisfactory explanation of the experimental observations of Figure 5.1. All the different phenomena observed in the measurements are associated with the occurrence of particular kinds of bifurcations.

5.4 Stabilization Technique

After understanding the different phenomena observed in the measurements, the objective will be the stabilization of the amplifier. For this purpose, a stabilization network will have to be added to the circuit. In order to efficiently obtain the optimum network, a simplified equivalent circuit will be derived here, taking into account the virtual-ground and virtual-open planes at the oscillation frequency, identified in Section 5.3.3.

Figure 5.10 shows the equivalent circuit, which corresponds to a quarter section of the amplifier at the oscillation frequency. It is a parallel resonance oscillator composed of the transistor exhibiting negative resistance and the equivalent capacitance, inductance and load resistance seen from the drain terminal. The output capacitance C_{res} connected between two transistor pairs is doubled due to the virtual-ground developed at the center of the capacitance, and the magnetization inductance L_{res} in the output transformer is divided by two due to the virtual-open at the center of the transformer. Note that the RF choke inductance L_{choke} is also a critical element included in the equivalent circuit. The resonance frequency is 5.3 MHz, which is quite close to the oscillation frequency obtained both in measurement and in simulation. This confirms the validity of the proposed equivalent circuit.

From the schematic of Figure 5.10, a simple means to stabilize the amplifier is the addition of a resistor at the node *N*. The value of this resistance must be small enough to avoid the oscillation for all the possible operation conditions, in terms of V_{DD} and P_{in}. It also must not affect the normal operation of the amplifier.

The node *N* corresponds to the center point of the primary circuit in the output transformers. The push-pull operation introduces a virtual ground at the node for the

operating frequency f_{in} and odd harmonics. Hence, the addition of the resistance at the node N will have little effect over these frequencies. However, the resistor will impose a finite impedance to even harmonics instead of an open circuit, which would be the right termination for the Class-E/F_{odd} operation. Thus, a second harmonic trap at $2f_{in}$ will be connected in series with the resistor to reduce the effect. This will provide an open circuit at the second harmonic frequency. The effect of higher even harmonics on the operation, expected to be small, will be analyzed through simulation. The schematic of the amplifier, with the stabilization network, is shown in Figure 5.11.

Once the topology and the location of the stabilization network have been determined, the next step will be the calculation of stabilization resistance value, in order to ensure stable amplifier operation for all the expected values of V_{DD} and P_{in}. An efficient technique will be applied for this purpose. The technique is based on the plot of the small-signal input admittance Y_{in}. This is calculated at the drain terminal using the small-amplitude current source and the conversion-matrix approach (see Section 5.3.1). Comparing the frequency variation of Y_{in} with pole-zero identification results, it has been possible to associate the instability with the existence of negative conductance and resonance at the oscillation frequency. Thus, the plot of Y_{in} will allow a fast verification of these oscillation conditions.

Three different values of the stabilization resistance have been considered: 100 Ω, 50 Ω, and 15 Ω. For each value, two nested sweeps are carried out in the two amplifier parameters V_{DD} and P_{in}. For each (V_{DD}, P_{in}) point, a harmonic balance calculation is performed, together with a sweep in the current-source frequency f, using conversion matrix. This yields the input admittance $Y_{in}(f)$ seen by the current source. Then, the imaginary part of $Y_{in}(f)$ is plotted versus the real part. The resulting plots, for the original amplifier and for the amplifier with the three indicated resistance values, are shown in Figure 5.12. Each admittance curve corresponds to a pair of values (V_{DD}, P_{in}). The same frequency-sweep range has been considered for each curve. In the representation, this range has been limited to 3−5.5 MHz, for the sake of clarity. For global stability, no crossing of the real axis with negative

conductance and positive increase of the susceptance must be obtained [65]. As expected, larger stability ranges are achieved as the stabilization resistance is reduced. For $R_{stab} = 15\ \Omega$, the amplifier becomes stable for all the operation values of V_{DD} and P_{in}. This has been rigorously verified by extending the range of the frequency sweep and applying pole-zero identification.

Through bifurcation detection, it is possible to directly calculate the stabilization resistance R_{stab}, for given V_{DD} and P_{in} values. To achieve this, the stabilization resistance R_{stab} and the oscillation frequency f_a will be determined in order to fulfill $Y_{in}(R_{stab}, f_a) = 0$. For each V_{DD} and P_{in}, the resulting resistance R^0_{stab} is the maximum value allowed for stable behavior. The resistance value R^0_{stab} is actually a bifurcation value: The amplifier is unstable for $R_{stab} > R^0_{stab}$ whereas it is stable for $R_{stab} < R^0_{stab}$.

In order to globally determine the variation of R^0_{stab}, a sweep of P_{in} is performed for several V_{DD} values covering the expected operation ranges. For each V_{DD}, the equation $Y_{in}(R_{stab}, f_a) = 0$ is solved to calculate R^0_{stab} versus P_{in}, which is shown in Figure 5.13. As can be observed, R^0_{stab} decreases with the bias voltage. On the other hand, as P_{in} approaches values for which the amplifier periodic solution is stable, this resistance tends to infinity. From Figure 5.13, a resistance value smaller than 17 Ω is required for global stabilization of the amplifier. The results are consistent with those obtained from the admittance plots of Figure 5.12.

In view of the results of Figure 5.12 and Figure 5.13, the resistance value $R_{stab} = 15\ \Omega$ has been chosen for the corrected design of the amplifier. As the final step, the influence of this resistance on the amplifier drain efficiency and output power has been analyzed. This is shown in Figure 5.14, where the drain efficiency and output power is traced versus the resistance value. As can be seen, the stabilization resistance has only small influence. This is due to the fact that the connection point is a virtual ground at the fundamental and the odd harmonics, and the second-harmonic trap has been used to maintain the connection point as

an open circuit at that frequency. The higher even harmonics turned out to have negligible influence.

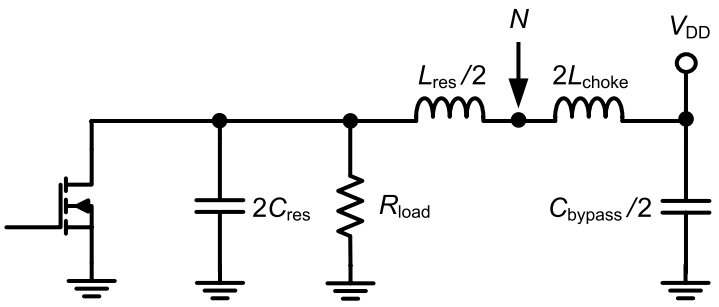


Figure 5.10: Simplified equivalent circuit of the PA at the oscillation frequency after considering the virtual-open and virtual-ground planes.

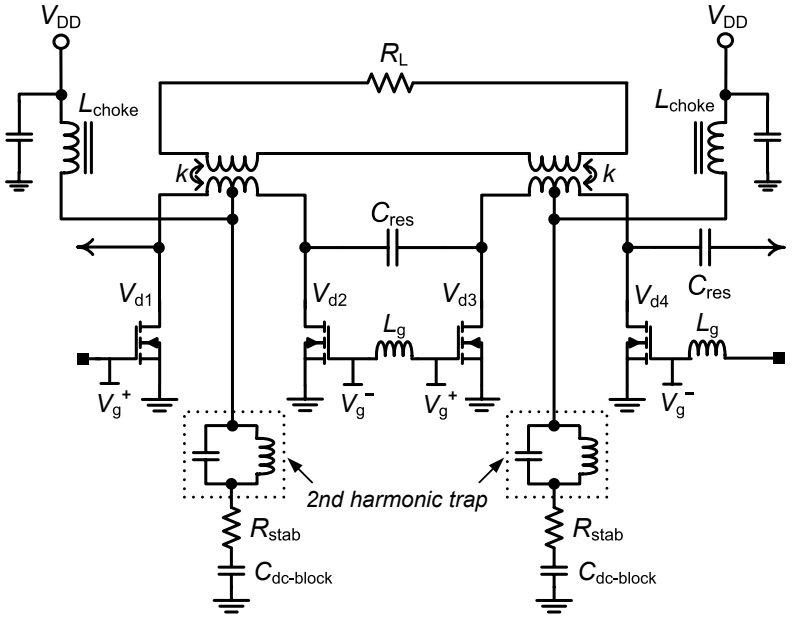


Figure 5.11: Amplifier schematic with stabilization network. The stabilization network consists of a stabilization resistor R_{stab}, a second harmonic trap, and a DC-blocking capacitor $C_{dc\text{-}block}$.

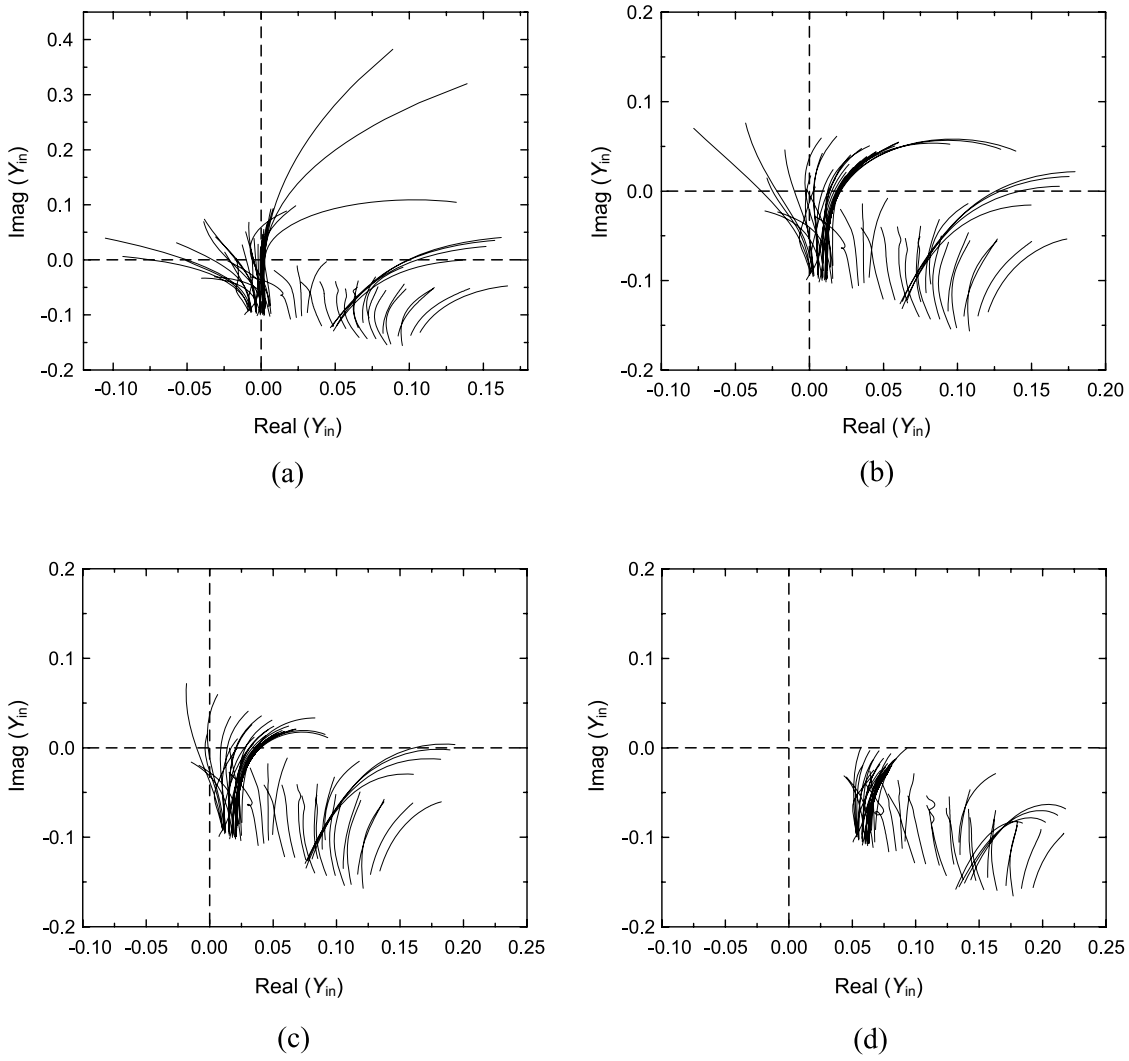


Figure 5.12: Stabilization action of the parallel resistance, analyzed by means of admittance plots. Three resistance values have been considered. (a) No stabilization resistor. (b) R_{stab} = 100 Ω. (c) R_{stab} = 50 Ω. (d) R_{stab} = 15 Ω. In (a), (b), and (c), the oscillation condition is satisfied for a certain parameter range, and thus the global stability is not achieved.

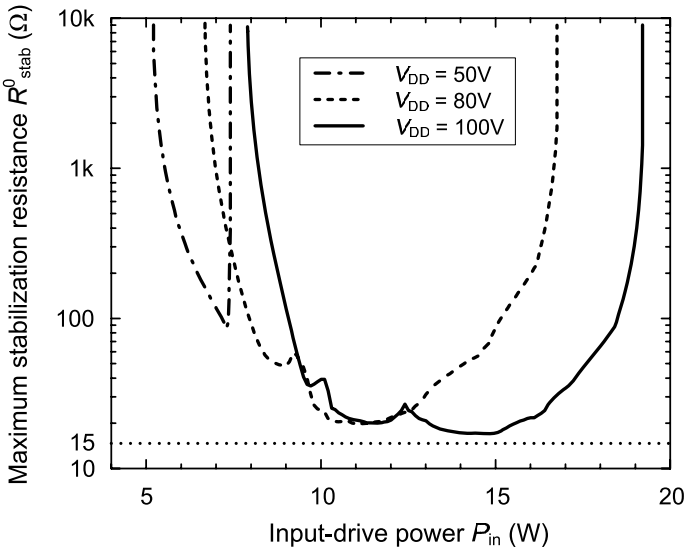


Figure 5.13: Variation of the maximum value of stabilization resistance R^0_{stab} versus the input-drive power P_{in}, obtained through bifurcation analysis. Three different drain bias voltages have been considered.

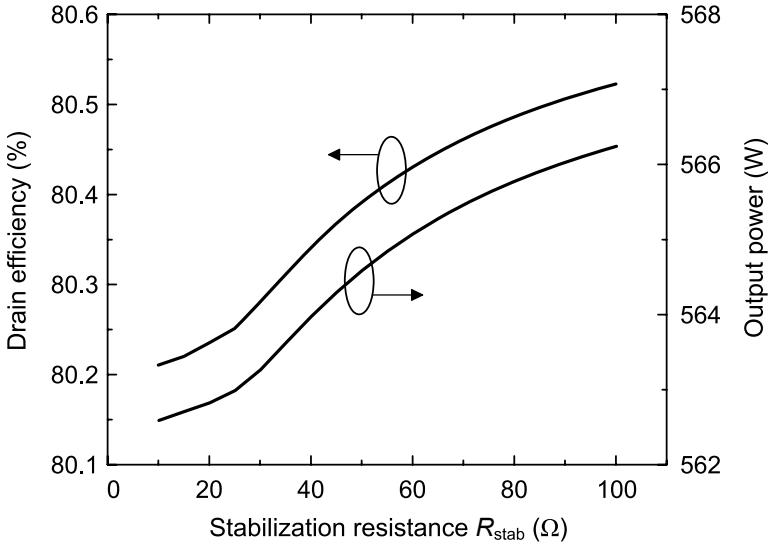


Figure 5.14: Variation of the amplifier drain efficiency and output power versus the value of the stabilization resistance. The drain bias voltage is assumed as V_{DD} = 72 V.

5.5 Measurements of the Stabilized Amplifier

The amplifier has been modified for globally stable behavior by introducing the stabilization network developed in Section 5.4. A stabilization resistor of 15 Ω in series with the second harmonic trap and a DC-blocking capacitor is simply connected to the center point of each output transformer. Power resistors with a 35-W rating are used in order to handle the simulated current of 0.7 A at even harmonics of the input-drive frequency. The Q-factor of the second harmonic trap is carefully chosen considering a trade-off between low impedance at the oscillation frequency and the feasibility of realizing each component. A mica capacitor and an air-core inductor with 14-AWG copper wire are used for the second harmonic trap.

This amplifier has shown global stability over the entire range of operating conditions of V_{DD} and P_{in}, as predicted in the simulation. We never observed any oscillation or chaotic regimes. The output power spectrum was similar to Figure 5.1 (c), whenever the input drive was sufficient to turn on the transistors. The drain efficiency of the amplifier has been measured, which is shown in Figure 5.15. Compared to the original PA, the drain efficiency is degraded by less than 0.4 % for all output power levels except for 240 W, which shows 1.3 % degradation.

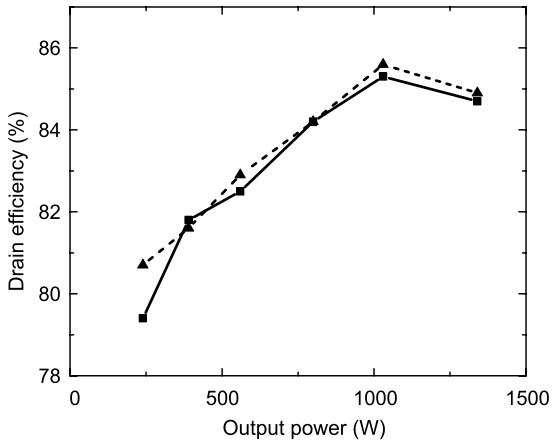


Figure 5.15: Measured drain efficiency versus the output power. Solid line: the stabilized PA, dashed line: the original PA.

Chapter 6

Analysis and Elimination of Hysteresis and Noisy Precursors in Power Amplifiers

Power amplifiers (PAs) often exhibit unstable behavior from a certain level of the input power [58], [61], [62], [70]. Frequency divisions by two and oscillations at incommensurate frequencies can be predicted through a large-signal stability analysis of the amplifier solution [36], [50], [59], [70]. In the stability analysis in Chapter 5, techniques were also presented for the efficient determination, through bifurcation detection, of the circuit parameters giving unstable behavior. Oscillatory and chaotic solutions were analyzed in detail, which enabled the derivation of a suitable stabilization technique. However, other phenomena, whose origins are difficult to identify, are also commonly observed in the measurement of PAs. The work in this chapter has been motivated by the anomalous behavior of a Class-E PA [35]. In the intermediate input-power range, this circuit exhibited pronounced noise bumps at frequencies different from the input-drive frequency, which degraded the amplifier performance. The bumps were observable for a relatively large input-power interval until an oscillation was suddenly obtained. The frequency of this oscillation f_a mixed with the input-drive frequency f_{in}, to give rise to sidebands whose frequencies were surprisingly different from the central frequencies of the previous noise bumps.

As will be shown, the observed phenomenon involves hysteresis in the power-transfer curve and sideband amplification [40], the latter giving rise to the spectrum bumps, also called noisy precursors [71]. These undesired phenomena may also be obtained in PAs for communications, in which linearity and spectral purity are essential. The hysteresis causes sudden spectral growth and disrupts the linearity of amplifiers. The noisy precursors degrade the spectral purity and, particularly, bumps around the input-drive frequency may give rise to interference with other channels.

The in-depth investigation of the undesired behavior of PAs requires the combination of different analysis techniques, some of which will be presented here for the first time. The hysteresis in the P_{in}-P_{out} curve is due to the existence of a multi-valued section in the solution curve traced versus P_{in}, as a result of infinite-slope points or turning points [38], [72] occurring in this curve. This is shown in the sketch of Figure 2.17 (e). Increasing P_{in} from the lower curve section, the jump J_1, from the point T_1, leads to the upper section. Decreasing P_{in} from this upper section, the jump J_2 leads to the lower one. When using harmonic balance (HB), the multi-valued solution curve can be traced by means of a suitable continuation technique like the switching-parameter algorithm [38], [55], [72]. Here a technique will be presented to obtain the multi-valued curve in commercial HB software, unable to pass through the tuning points. However, the actual goal of the designer is the suppression of the hysteresis phenomenon, which is generally carried out through a trial-and-error procedure. In order to improve the design efficiency, a new technique is proposed here allowing the removal of the turning points through a single simulation on commercial HB. It relies on the tracing of a turning-point locus on the plane defined by the input power and a suitable stabilization parameter.

As already discussed, high-power bumps were observed in the output power spectrum of the Class-E PA. In previous work, these bumps have been related to noise amplification, coming from a small stability margin [40]. The circuit resonant frequencies have low damping and, under the continuous noise perturbations, give rise to bumps in the output

power spectrum. If a circuit parameter, such as the input power, is varied and the near-critical poles approach the imaginary axis, the noise bumps become narrower and higher. If the poles cross the imaginary axis, a bifurcation occurs and, from this parameter value, the bumps become distinct spectral lines. One of the objectives of this work is the study of this phenomenon in power amplifiers.

The continuous pole displacement, approaching the imaginary axis, takes place in any circuit evolving to an unstable regime. However, the noisy precursors are not always observable. Another aspect that will be investigated here is the reason for the observation of this phenomenon in particular circuits only. Pole-zero identification will be applied to follow the evolution of the system poles, which will be related to the noise amplification. The output noise spectrum will be simulated with both the conversion-matrix approach [73] and the envelope-transient [67], [68]. The latter enables a prediction of nonlinear phenomena occurring for high-power bumps or in the immediate neighborhood of the bifurcation. A technique will also be presented for the elimination of noisy precursors from the amplifier output spectrum.

This chapter is organized as follows. In Section 6.1, the measurements of the Class-E power amplifier, with anomalous behavior, are presented. In Section 6.2, the amplifier solution and its stability are analyzed versus the input power. In Section 6.3, the noisy precursors are simulated with the conversion-matrix approach and the envelope-transient. In Section 6.4, a general technique for the elimination of hysteresis in the P_{in}-P_{out} curve of power amplifiers is presented and applied to the Class-E power amplifier. Experimental confirmation is also shown. In Section 6.5, a technique for the elimination of noisy precursors is presented and applied to the Class-E power amplifier with experimental verification.

6.1 Experimental Measurements on the Class-E Power Amplifier

The schematic of the Class-E power amplifier is shown in Figure 6.1. The output capacitance C_{out} and a resonant tank composed of C_{res} and L_{res} fulfill the Class-E tuning, together with the transistor driven as a switch [4], [7]. The resonant tank is slightly mistuned from the operating frequency f_{in} = 7.4 MHz to present a zero-voltage switching characteristic to the drain voltage. In order to suppress the second harmonic level below −40 dBc, a second harmonic trap (C_{2nd} and L_{2nd}) is used at the output. This also performs the output impedance transformation to 8 Ω, an appropriate load impedance for switching operation. In addition, a low-pass filter (C_{lpf} and L_{lpf}) is added to suppress VHF harmonic components from the output spectrum at least 40 dB below the fundamental. The amplifier achieves an output power of 360 W with a gain of 16.1 dB and a drain efficiency of 86.1 % at 7.4 MHz, when it is driven with sufficient input power for saturated operation. The input VSWR is 1.7.

We observe different phenomena in the measurements of the Class-E amplifier. As the input power increases from zero, only leakage output power at the input-drive frequency f_{in} is initially obtained. This is in good agreement with the fact that the transistor in the switching amplifier is not turned on below a certain level of input power. Then, from the input power P_{in} = 0.5 W, noise bumps of relatively high power arise in the spectrum. There are three bumps centered about f_c = 560 kHz and $f_{in} \pm f_c$, respectively <Figure 6.2 (a)>. As the input power is further increased, f_c decreases and the bumps about f_{in} become closer. The bump power also increases <Figure 6.2 (b)>, until, at P_{in} = 0.83W, an oscillation is obtained at the frequency f_a = 1MHz <Figure 6.2 (c)>, quite different from f_c. From this power value, the circuit operates in a self-oscillating mixer regime, at the two fundamentals f_{in} and f_a <Figure 6.2 (c)>. The high phase noise indicates a low quality factor of the oscillation. The oscillation frequency is close to f_{in} / 7, which gives rise to spectral lines at short frequency distance from the oscillation harmonics.

At the power value P_{in} = 0.89 W, a frequency division by 7 is obtained <Figure 6.2 (d)>. The synchronization at f_a / f_{in} = 1 / 7 is maintained for the input-power interval from 0.89 W to 0.92 W. The synchronization capability at this high-harmonic order also indicates a low

quality factor of the oscillation. When the power level is higher than $P_{in} = 0.92$ W, the circuit behaves again as a self-oscillating mixer. Finally, at $P_{in} = 1.7$ W, the oscillation is extinguished and, from this power value on, the amplifier operates in the desired periodic regime <Figure 6.2 (e)>. For reasons to be given later, we did not notice hysteresis in these initial measurements. When reducing the input power from power levels above 1.7 W, all the transitions between the different regimes seemed to occur for the same indicated P_{in} values.

As stated in the introduction, the noise bumps are due to noise amplification about the natural frequencies of the circuit when the stability margin is small. Thus, the spectral lines due to the oscillation should be generated at frequencies near $kf_{in} \pm f_c$, with k integer, which are the central bump frequencies. However, in the Class-E amplifier, there is a substantial difference between the bump frequency f_c and the oscillation frequency f_a. To give an explanation of this and other observed phenomena, several analysis techniques will be combined in the next section.

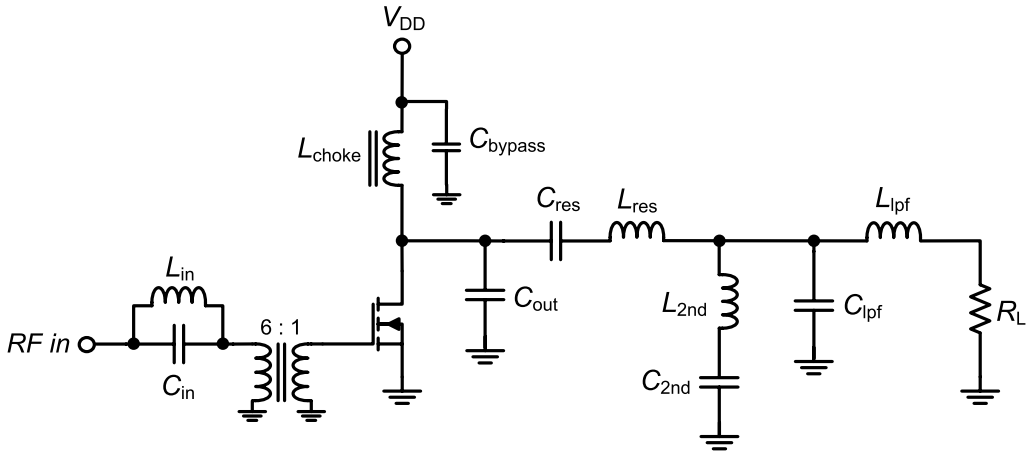


Figure 6.1: Schematic of the Class-E power amplifier at 7.4 MHz [35].

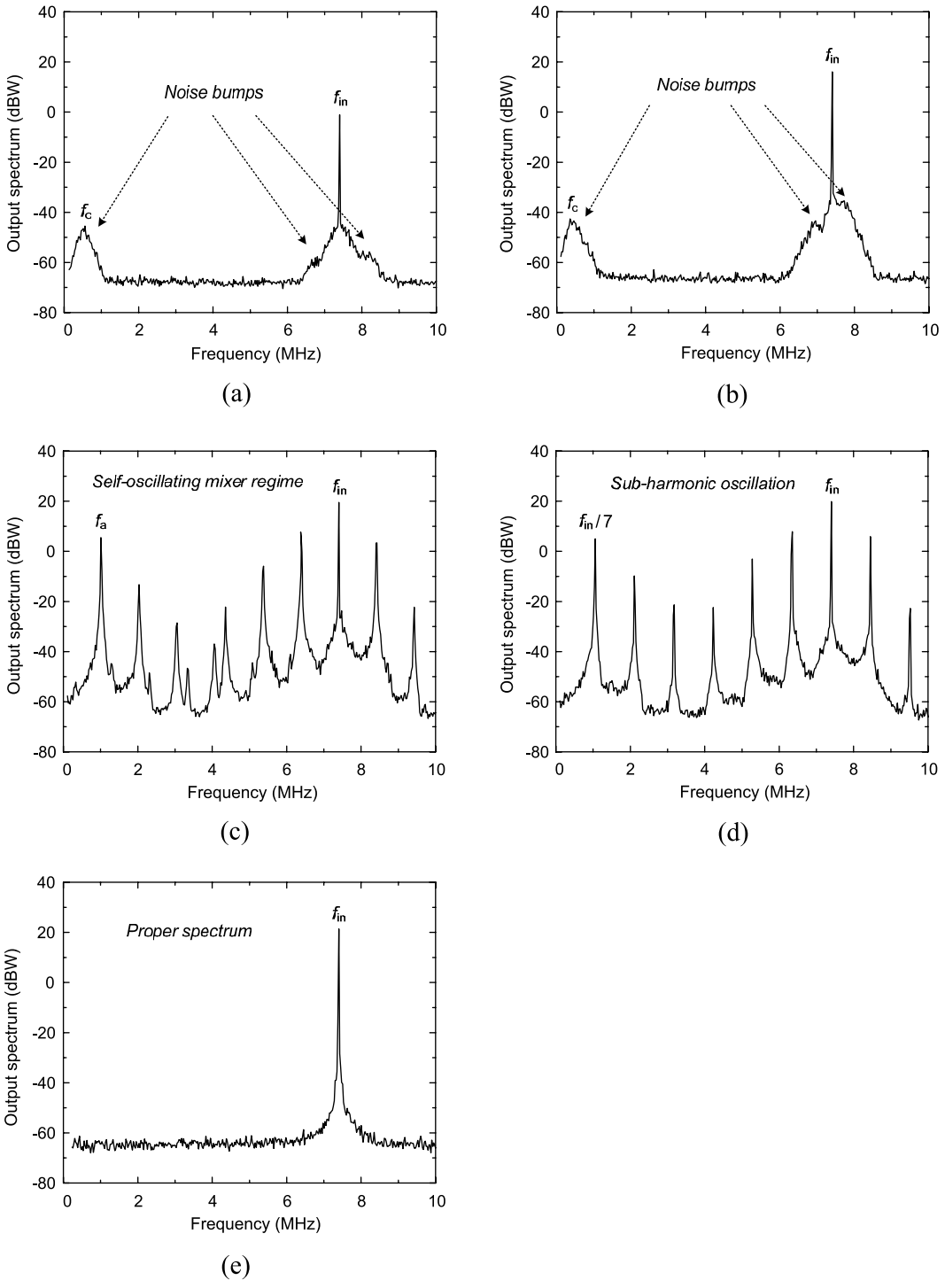


Figure 6.2: Measured output power spectrum of the Class-E power amplifier, for different input power values. Resolution bandwidth = 3 kHz. (a) P_{in} = 0.5 W.

Pronounced noise bumps are observed about the frequencies f_c = 560 kHz and $f_{in} \pm f_c$. (b) P_{in} = 0.8 W. The bump frequency f_c is lower and its power is higher. (c) P_{in} = 0.83 W. An oscillation suddenly arises at the frequency f_a = 1 MHz. (d) P_{in} = 0.89 W. Frequency division by 7. The seventh harmonic of the oscillation is synchronized to the input frequency. (e) P_{in} = 4.0 W. Proper operation of the amplifier.

6.2 Nonlinear Analysis of the Class-E Power Amplifier

The analysis of the Class-E amplifier will be carried out in three different steps. Initially, its power-transfer curve will be obtained through an HB continuation technique. In a second step, stability-analysis techniques will be applied to study the amplifier stability along the resulting solution curve. Finally, the oscillatory solution will be analyzed using two-tone HB.

6.2.1 Analysis of the Power-Transfer Curve

The initial step in the nonlinear analysis of the power amplifier is the determination of its power-transfer curve, using HB. However, a discontinuity was observed when sweeping the input power, which indicated a possible hysteresis phenomenon. This is caused by turning points or infinite-slope points of the solution curve, at which the Jacobian matrix of the HB system becomes singular [38]. The used commercial HB software is unable to pass through the turning points. This requires a suitable continuation technique [38], [55], [74]. In the switching-parameter algorithm, the sweep parameter is switched, near the turning point, to the HB variable with the largest increment, given by the real or imaginary part of one of the harmonic components of one of the circuit variables [38], [55]. Here, a different technique will be applied, based on the introduction of an auxiliary generator (AG) into the circuit. Unlike previous work [58], [38], [75], this AG will be used for the analysis of a non-oscillatory regime, corresponding to the amplifier periodic solution at the input-drive

frequency f_{in}. The AG will enable the implementation of a parameter-switching technique on the commercial HB software.

When using a voltage AG, this generator is connected in parallel at a sensitive circuit node, typically corresponding to a transistor terminal. The AG will operate at f_{AG} and must be an open circuit at all other frequencies. Thus, an ideal bandpass filter is introduced in series with this generator. Furthermore, the AG must not perturb the circuit steady-state solution. This is ensured by imposing a zero value to its current-voltage relationship $Y_{AG} = I_{AG} / V_{AG} = 0$, where I_{AG} and V_{AG} are the current and the voltage of the AG, respectively.

The AG will operate at the input-drive frequency $f_{AG} = f_{in}$. The variables to be determined, in order to fulfill $Y_{AG} = 0$, will be the AG amplitude $|V_{AG}|$ and its phase ϕ_{AG}. The requirement for the AG phase calculation comes from the fact that it is a non-autonomous regime [38]. The equation $Y_{AG} = 0$ is solved through error-minimization or optimization procedures, with the HB system as the inner loop. When the condition $Y_{AG} = 0$ is fulfilled, the AG amplitude agrees with that of the fundamental harmonic component of the voltage at the AG connection node. Thus, sweeping the AG amplitude will be equivalent to sweeping the amplitude of this fundamental component.

The continuation technique is applied as follows. In the curve sections with low slope with respect to the input power, this power is used as the sweep parameter. In the sections with high slope, the sweep parameter is switched to the AG amplitude $|V_{AG}|$. In the Class-E PA, the AG is connected to the transistor drain terminal. Using the described technique, it has been possible to obtain the multi-valued P_{in}-P_{out} curve of Figure 6.3.

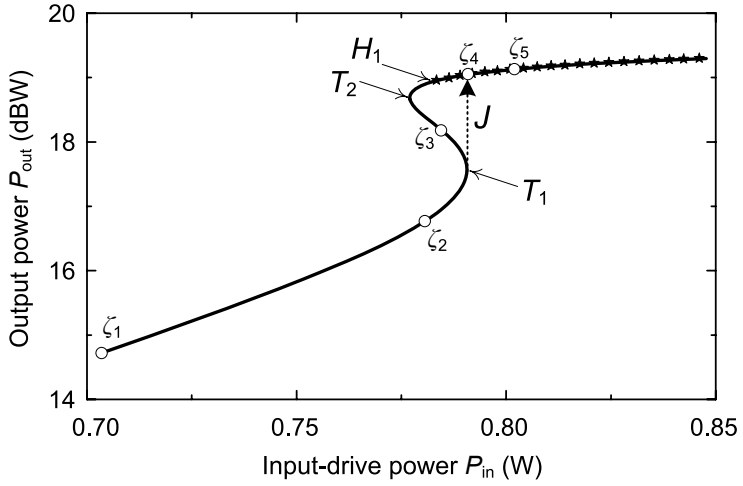


Figure 6.3: Multi-valued P_{in}-P_{out} curve of the Class-E power amplifier, obtained with the AG-based switching-parameter technique. The section in which the amplifier behaves in self-oscillating mixer regime is indicated by stars.

6.2.2 Stability Analysis

The next step will be the stability analysis of the amplifier periodic solution along the multi-valued curve of Figure 6.3, which will be carried out through a sequential application of the pole-zero identification technique presented in Section 4.2.1. This technique requires the linearization of the HB equations about the steady-state amplifier periodic solution, which is done through the introduction of a small-signal current generator i_s into the circuit, at a sensitive circuit node n. This generator operates at a frequency f, non-harmonically related to f_{in}. By using the conversion-matrix approach, the ratio between the node voltage $V_n(f)$ and the injected current $I_s(f)$ is calculated, which provides a single-input, single-output transfer function $Z_{in}(f)$. We will apply pole-zero identification to this function. Note that the poles of a periodic solution are non-univocally defined, because adding any integer multiple of $j2\pi f_{in}$ gives another pair of poles with the same real part. These extra poles provide no additional information, so only poles between $-j2\pi f_{in}$ and $j2\pi f_{in}$ will be considered here.

In the case of the Class-E amplifier, the small-signal current generator is connected at the transistor drain terminal. Initially, the input power is varied from $P_{in} = 0.70$ W to $P_{in} = 0.79$ W, in 0.01 W steps, following the section ζ_1-ζ_2-ζ_4 of Figure 6.3 with a jump between ζ_2 and ζ_4. The pole-zero identification technique is sequentially applied to each periodic solution obtained with HB. For the Z_{in} calculation, we consider the frequency interval from 1 kHz to 2 MHz. The resulting pole locus is shown in Figure 6.4 (a), where the two pairs of poles, $\sigma_1 \pm j2\pi f_1$ and $\sigma_2 \pm j2\pi f_2$, closest to the imaginary axis are represented. The pair $\sigma_1 \pm j2\pi f_1$ is initially much closer to this axis than $\sigma_2 \pm j2\pi f_2$.

As P_{in} increases, both $\sigma_1 \pm j2\pi f_1$ and $\sigma_2 \pm j2\pi f_2$ move rightwards at very different velocity $d\sigma / dP_{in}$. The displacement of $\sigma_2 \pm j2\pi f_2$ is faster than that of $\sigma_1 \pm j2\pi f_1$, which remains in the neighborhood of the axis for all the considered P_{in} values. For $P_{in} = 0.79$ W, due to the jump, there is a discontinuity in the pole locus and an anomalously large shift is obtained in $\sigma_2 \pm j2\pi f_2$, whereas the pair $\sigma_1 \pm j2\pi f_1$ is no longer present. From this power value, the pair $\sigma_2 \pm j2\pi f_2$ is located on the right-hand side of the complex plane. The amplifier periodic solution is unstable, as the pair of poles $\sigma_2 \pm j2\pi f_2$ gives rise to an oscillation at about $f_a = 1$ MHz.

For a detailed study of the pole variations, the sections around the turning points are also analyzed: ζ_2-T_1-ζ_3 and ζ_3-T_2-H_1-ζ_4-ζ_5 of Figure 6.3. Note that, unlike the case of Figure 6.4 (a), P_{in} does not increase monotonically along these sections. The pole-zero identification technique is applied to the solution curve obtained with the AG-based parameter switching technique.

Figure 6.4 (b) shows the pole evolution along the section ζ_2-T_1-ζ_3. The pair of complex-conjugate poles $\sigma_2 \pm j2\pi f_2$ approaches the imaginary axis without crossing it. For clarity, only the evolution of the poles $\sigma_1 \pm j2\pi f_1$ is presented. The considered frequency interval is 0 to 300 kHz. As the input power increases, the two complex-conjugate poles remain close to the imaginary axis and from 0.780 W to 0.789 W, move nearly vertically, approaching each

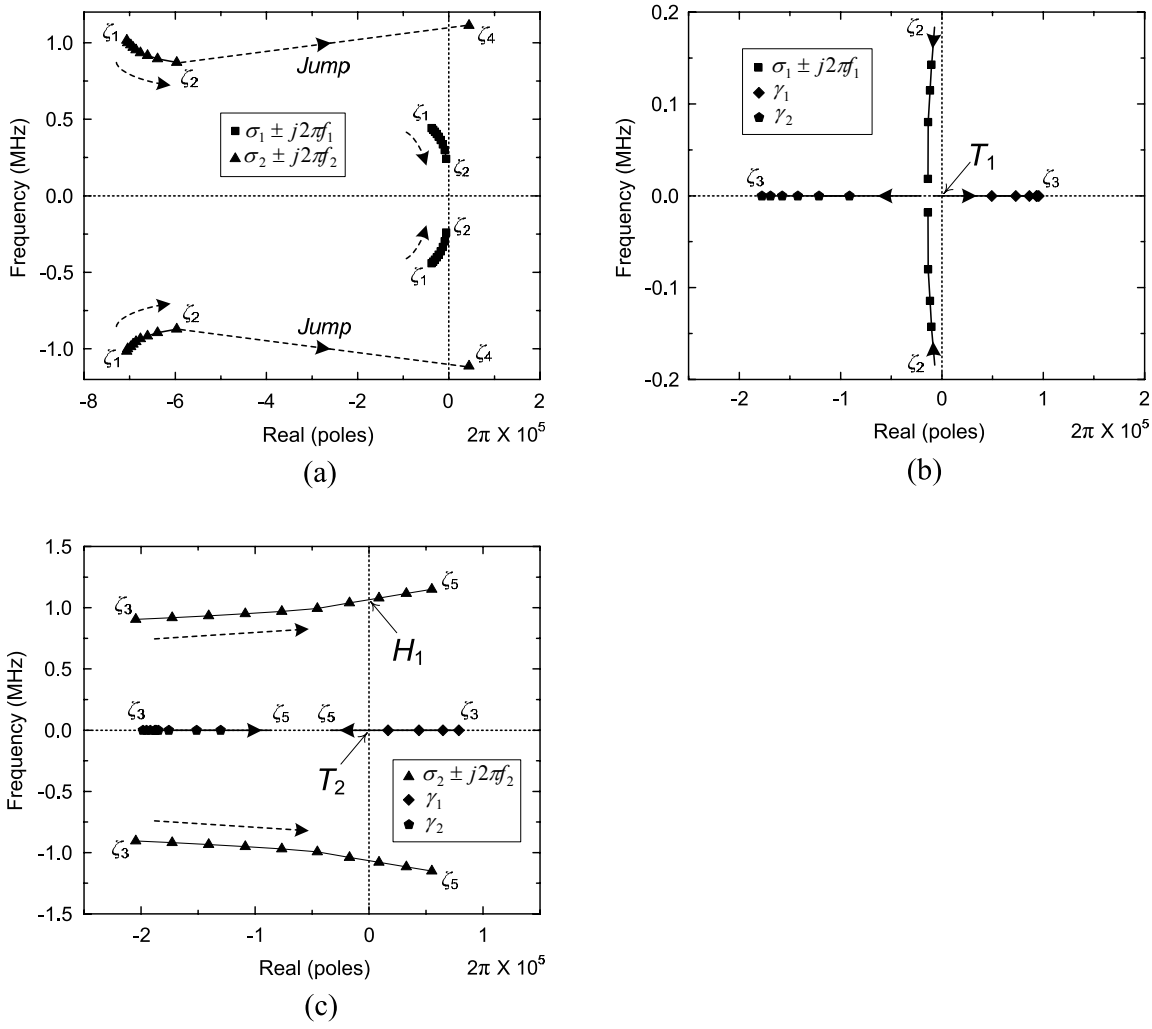


Figure 6.4: Pole evolution along the P_{in}-P_{out} curve of Figure 6.3. (a) Section ζ_1-ζ_2-ζ_4 of Figure 6.3. The two pairs of poles $\sigma_1 \pm j2\pi f_1$ and $\sigma_2 \pm j2\pi f_2$ closest to the imaginary axis are represented. (b) Section ζ_2-T_1-ζ_3. The complex-conjugate poles $\sigma_1 \pm j2\pi f_1$ approach each other and meet on the real axis. They become two different real poles, γ_1, γ_2 and, from that point, follow opposite directions. One of the real poles crosses the imaginary axis at $P_{in} = 0.790$ W, corresponding to the turning point T_1, and the solution becomes unstable. (c) Section ζ_3-T_2-H_1-ζ_4-ζ_5. The real pole γ_1 crosses the imaginary axis back to the left-hand side at $P_{in} = 0.777$ W, corresponding to the turning point T_2. The pair of complex-conjugate poles $\sigma_2 \pm j2\pi f_2$ crosses the imaginary axis to the right-hand side at the Hopf bifurcation H_1, obtained for $P_{in} = 0.781$ W.

other, until they meet on the real axis. This gives rise to a qualitative change in the pole configuration, as the two complex-conjugate poles become two real ones γ_1 and γ_2 from this power value. By further increasing the power, the two real poles move in opposite directions. The pole γ_1 moves to the right and crosses the imaginary axis at $P_{in} = 0.790$ W. This is the power value at which the turning point T_1 is obtained in the P_{in}-P_{out} curve of Figure 6.3, in correspondence with the fact that a pole at zero implies a singularity of the HB Jacobian matrix [38]. From this point, the amplifier periodic solution is unstable.

Figure 6.4 (c) shows the evolution of the two sets of poles $\sigma_2 \pm j2\pi f_2$ and γ_1, γ_2 along the section ζ_3-T_2-H_1-ζ_4-ζ_5 of the P_{in}-P_{out} curve. The considered frequency interval is 0 to 1.5 MHz. After passing through zero, γ_1 moves farther right, turns, and crosses the imaginary axis through zero again at $P_{in} = 0.777$ W, corresponding to the turning point T_2. The entire section between T_1 and T_2 of the P_{in}-P_{out} curve is unstable because the pole γ_1 is on the right-hand side of the complex plane for the section.

For the same section ζ_3-T_2-H_1-ζ_4-ζ_5 in Figure 6.4 (c), the poles $\sigma_2 \pm j2\pi f_2$ move to the right, approaching the imaginary axis. At $P_{in} = 0.781$ W, they cross to the right-hand side of the complex plane. A Hopf bifurcation H_1 [38], [60] is obtained, giving rise to an oscillation at about $f_a = 1$ MHz. As P_{in} is further increased, the poles move to the right, turn, and cross again the imaginary axis at $P_{in} = 1.45$ W. At this power value, a second Hopf bifurcation H_2 is obtained, which extinguishes the oscillation.

The analysis in Figure 6.4 is in correspondence with the measurements of Figure 6.2. For the input-power interval 0.5 W to 0.789 W, the first pair of complex-conjugate poles $\sigma_1 \pm j2\pi f_1$ is very close to the imaginary axis and the small stability margin explains, as will be shown in Section 6.3, the observation of the noisy precursors. Actually, the pole frequency f_1 agrees with the bump frequency f_c. As the input power increases, the pole frequency decreases, which explains the decrease of the bump frequency observed in the measurements. At $P_{in} = 0.790$ W, the turning point T_1 is encountered, which ordinarily would give rise to a

jump leading to the upper section of the periodic-solution curve. However, this periodic solution is already unstable when the jump takes place, because the second pair of complex-conjugate poles $\sigma_2 \pm j2\pi f_2$ with $f_2 = 1$ MHz is on the right-hand side of the complex plane (see the section indicated by stars in Figure 6.3). Thus, an oscillation at about $f_a = 1$ MHz is obtained from this power, in agreement with the measurement results.

In fact, this explains why the hysteresis of Figure 6.3 was not initially detected in the measurements. The sudden variation of the output power was attributed solely to the oscillation. In addition, the hysteresis interval was too small to actually observe the difference between the input power values at which the oscillation was generated and extinguished.

6.2.3 Analysis of the Oscillatory Solution

For the input-power interval from 0.781 W to 1.45 W, the amplifier operates in a self-oscillating mixer regime, with the signal at the drive frequency f_{in} mixing with the oscillation at f_a. For a more detailed study of the amplifier behavior, this solution has also been simulated by means of HB. The existence of two fundamental frequencies f_{in} and f_a requires a two-tone analysis. In order to prevent the HB convergence towards the unstable periodic solution at f_{in}, an AG at the oscillation frequency $f_{AG} = f_a$ has been used. Both the AG amplitude $|V_{AG}|$ and frequency f_{AG} must be calculated in order to fulfill the non-perturbation condition $Y_{AG} = 0$. This equation is solved through error-minimization or optimization procedures, with the HB system as the inner loop.

Using the AG technique, it has been possible to obtain the evolution of the oscillatory solution versus the input power, which is represented in Figure 6.5. Two different curves are traced. One provides the power variation at the oscillation frequency. Increasing the input power, this curve arises at the Hopf bifurcation H_1 and vanishes at the Hopf bifurcation H_2. The second curve provides the output power at the input-drive frequency, when the circuit is oscillating. This curve joins the amplifier periodic solution at the two input-power values

corresponding to H_1 and H_2. The dashed curve shows the unstable amplifier periodic solution, when the circuit is oscillating. As can be seen, the P_{in} value for the Hopf bifurcation H_1 is smaller than the P_{in} value for the turning point T_1. This is in correspondence with the pole diagrams of Figure 6.4 and with the measurements.

For the considered input frequency $f_{in} = 7.4$ MHz, no harmonic synchronization of the oscillation frequency f_a to the input-drive signal has been observed in simulation, which is attributed to modeling inaccuracies. However, for a somewhat higher frequency $f_{in} = 7.7$ MHz, a frequency division by 7, has been obtained versus P_{in}. For the simulation of this divided solution of high order, an AG is connected to the drain terminal in parallel. The AG frequency is determined by the input-drive source and given by $f_{AG} = f_{in} / 7$. Instead, the AG phase ϕ_{AG} has to be calculated, due to the harmonic relationship between f_a and f_{in}. The synchronization curves are generally closed and can be efficiently determined by a sweep of the AG phase [76]. To obtain the synchronization curve versus P_{in}, this power, together with the AG amplitude $|V_{AG}|$, is calculated at each phase step $\Delta\phi_{AG}$, in order to fulfill the condition $Y_{AG} = 0$.

The application of the above technique to the Class-E amplifier provides the closed curve S_1-T_1'-T_2'-S_2 of Figure 6.6, where the output power at $f_{in} / 7$ is represented versus P_{in}. The stability of the different sections of the closed curve has been analyzed with the pole-zero identification technique, with the results indicated in the figure. The turning points T_1' and T_2' give rise to jumps between the different stable sections. The output power at f_a, outside the synchronization range, is also represented. The resulting paths approach the closed curve near the synchronization points S_1 and S_2.

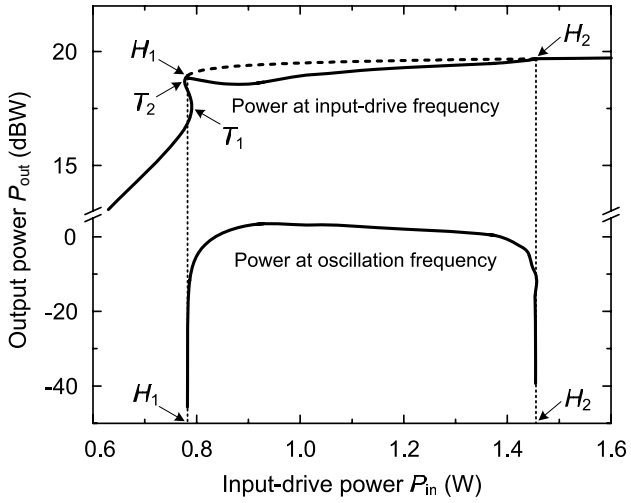


Figure 6.5: Bifurcation diagram of the Class-E power amplifier versus the input power P_{in}. The dashed curve represents the output power of the unstable periodic solution. For the self-oscillating mixer regime, the power variations at both the oscillation frequency and input-drive frequency are represented. The turning points and Hopf bifurcations are also indicated.

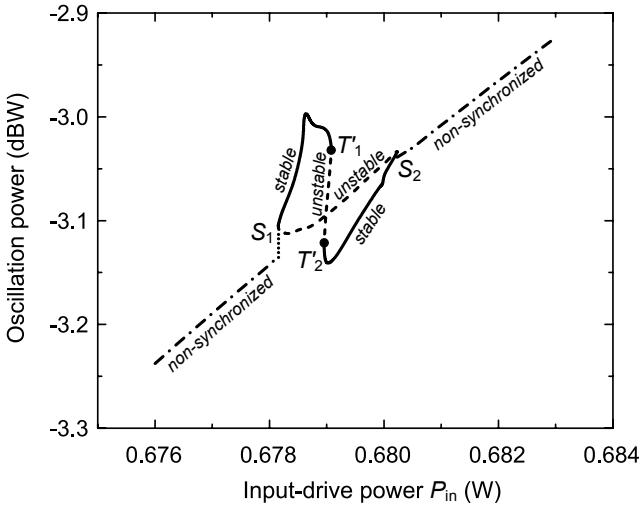


Figure 6.6: Synchronization diagram versus P_{in} for frequency division by 7. The closed curve with butterfly shape represents the synchronized solution. This solution is unstable in the dashed-line sections. The power at the oscillation frequency, outside the synchronization region, is also traced.

6.3 Analysis of Noisy Precursors

In this section, a simplified mathematical model is provided for the noisy precursors. The analysis techniques, based on the conversion matrix and envelope-transient, will also be discussed. These techniques will be applied in a detailed study of the noise bumps in the Class-E power amplifier.

6.3.1 Precursor Model and Analysis Techniques

Let the stable periodic solution $\mathbf{x}_0(t)$ at f_{in} be considered. If a small-amplitude perturbation is applied, an exponential transient will lead back to the original solution $\mathbf{x}_0(t)$. This transient will be dominated by the pole or a pair of complex-conjugate poles with the smallest real part, in absolute value [38]. Assuming the dominant poles are $\sigma_c \pm j2\pi f_c$, the smaller the $|\sigma_c|$, the longer the transient at the frequency f_c. Under continuous noise perturbations, bumps will appear in the spectrum about the frequencies $kf_{in} \pm f_c$ [77].

If a parameter η is varied and the near-critical poles $\sigma_c \pm j2\pi f_c$ approach the imaginary axis, the noise bumps will become higher and narrower. If the poles cross the axis, a bifurcation will be obtained, with the bumps turning into distinct spectral lines. Due to this fact, the bumps have been called noisy precursors [40], [71]. The phenomenon can also be explained as a result of negative-resistance parametric amplification [48]. Under the effect of the pumping signal, the nonlinear capacitances will exhibit negative resistance about the circuit resonance frequencies $kf_{in} \pm f_c$. Prior to the bifurcation, the absolute value of this negative resistance will be smaller than the positive resistance exhibited by the embedding circuit. At the bifurcation, the positive resistance equals the negative one. From this point on, the negative resistance will be dominant and the solution will be unstable [65]. In negative-resistance parametric amplifiers, the product $\sqrt{G}\Delta f$, where G and Δf are the maximum gain and the 3-dB bandwidth, respectively, increases for a lower Q-factor of the

resonant circuits at the input and idler frequencies [48]. In the case of the noisy precursors, larger total bump power should be expected for a lower Q-factor of the resonance at f_c.

Following [40] and [77], it is possible to relate the precursor power with the stability margin and the frequency detuning from the central values $kf_{in} \pm f_c$. Assuming white noise perturbations, the output noise spectrum can be approximately modeled:

$$S(f) \cong \sum_{k=-\infty}^{\infty} \left[\frac{\lambda_k^{lsb}}{\sigma_c^2 + 4\pi^2 (f - kf_{in} + f_c)^2} + \frac{\lambda_k^{usb}}{\sigma_c^2 + 4\pi^2 (f - kf_{in} - f_c)^2} \right], \tag{6.1}$$

where only the dominant poles $\sigma_c \pm j2\pi f_c + j2\pi k f_{in}$ are taken into account. The coefficients λ_k^{lsb} and λ_k^{usb} depend on the system linearization about the steady-state regime and the input noise sources. There are pairs of Lorentzian lines, centered about the resonance frequencies $kf_{in} \pm f_c$. The height of these lines increases for lower σ_c, which means a smaller distance from the critical poles to the imaginary axis. Higher power is also obtained as the frequency approaches the critical values, $kf_{in} \pm f_c$. It must also be noted that the linearization becomes invalid in the immediate neighborhood of the bifurcation.

When using HB, the noisy precursors can be analyzed with the conversion-matrix approach [73] or the envelope-transient [67], [68]. The applicability of the conversion matrix is limited to a relatively low precursor power, in order for the linearization about the noiseless solution to be valid. For higher power, the circuit nonlinearities will give rise to gain saturation and other effects [40]. The envelope transient should be used instead.

In the envelope transient, the circuit variables are expressed in a Fourier series at the harmonic components of the input-drive frequency, with time-varying coefficients: $\mathbf{x}(t) = \sum_k \mathbf{X}_k(t) e^{j2\pi k f_{in} t}$. Prior to the bifurcation, the time variation $\mathbf{X}_k(t)$ will be exclusively due to the noise perturbations. When these series expressions are introduced in the circuit

equations, a differential system is obtained in the harmonic components $\mathbf{X}_k(t)$, to be integrated in time. For the analysis to be accurate, the integration step must be small enough to cover the noisy precursor band about the near-critical frequency f_c. This integration step is typically much larger than the one that would be required for a full time-domain simulation. The power spectrum is calculated using a periodogram technique.

6.3.2 Application to the Class-E Amplifier

Both the conversion-matrix approach and the envelope transient will be applied to the analysis of the noisy precursors of the Class-E amplifier. The noise sources that will be taken into account correspond to the channel noise, the thermal noise from the resistive elements, and the noise from the input generator.

To validate our initial assumption of sideband amplification occurring in this circuit, the conversion-matrix approach will be applied to analyze the gain about the near-critical frequencies $f_1, f_{in} - f_1, f_{in} + f_1$, with f_1 corresponding to the imaginary part of the pair of poles $\sigma_1 \pm j2\pi f_1$ in Figure 6.4. The gain from the channel-noise source to the circuit output is initially considered. For this gain analysis, the noise source is replaced with a deterministic current source of small amplitude. Its frequency is swept about $f_1, f_{in} - f_1$, and $f_{in} + f_1$, in three different analyses, calculating the conversion gain at the three considered sidebands.

As a representative case, Figure 6.7 shows the gain variation about $f_1, f_{in} - f_1$ and $f_{in} + f_1$ when sweeping the current source about f_1. Three different P_{in} values are considered. Note that the conversion-matrix approach is applied about a different steady-state solution for each P_{in} value. Qualitatively, the gain curves have the Lorentzian shape of equation (6.1), except for the asymmetries about the central bump frequencies, which cannot be predicted with this model. The central frequency of the amplification bands changes with P_{in} due to the variation of f_1. Extremely high gains will not be physically observed because small changes in P_{in}

cause large gain variations. Furthermore, nonlinear effects occur in the immediate neighborhood of the bifurcation.

For $P_{in} = 0.65$ W, the gain curves are centered about 490 kHz, in agreement with the pole frequency f_1 at this particular power value. The highest gain corresponds to the upper sideband $f_{in} + f$. For the higher power values ($P_{in} = 0.70$ W and $P_{in} = 0.75$ W), the central frequency decreases in good correspondence with the pole displacement of Figure 6.4 (a) and also with the experimental observations in Figure 6.2 (a) and Figure 6.2 (b). The sideband gains increase more rapidly than the lower-frequency gain, also in agreement with Figure 6.2 (a) and Figure 6.2 (b). Similar qualitative behavior is obtained when sweeping the current source about $f_{in} - f_1$ or $f_{in} + f_1$: the gain increases and the bump frequency decreases with the input power, showing the highest gain at the upper sideband. The behavior is also similar when the gain analysis is applied to other noise sources. Note that the purpose of this gain analysis is just to validate our initial assumption of sideband amplification.

For the actual noise analysis, all the different noise sources must be simultaneously considered. The noise from the input-drive source has been modeled from experimental measurements. The available source providing the necessary power for the switching operation of the amplifier has high noise and constitutes the largest noise contribution. The results obtained with both the conversion-matrix approach and envelope transient are compared in Figure 6.8. The good agreement indicates that no relevant nonlinear effects are taking place in the system for these operation conditions. The power of the upper sideband about f_{in} is higher than that of the lower sideband, in correspondence with the gain analysis of Figure 6.7 and with the measurements. As has been verified in simulation, noisy precursors of lower power are still obtained when using an input-drive source of higher spectral purity. Although the power is lower, the noisy precursors are still quite noticeable in the spectrum, so their observation in measurements can also be expected.

The Class-E amplifier combines three characteristics that contribute to the practical observation of the precursors. The Q-factor associated with the self-oscillation is low, so a relatively large precursor power may be expected. The near-critical poles have small derivative $|d\sigma / dP_{in}|$, so they remain close to the imaginary axis for a relatively large P_{in} interval. Finally, the gain from the noise sources to the circuit output is high, as shown in Figure 6.7. This gain is critical in allowing the precursors to be observed. For other amplifiers operating close to instability, the gain is usually too low and the precursors are below the noise floor of the measurement system.

This analysis of the circuit characteristics contributing to the observation of the noisy precursors will be very helpful in order to devise a technique for their efficient elimination from the spectrum. This will be shown in Section 6.5.

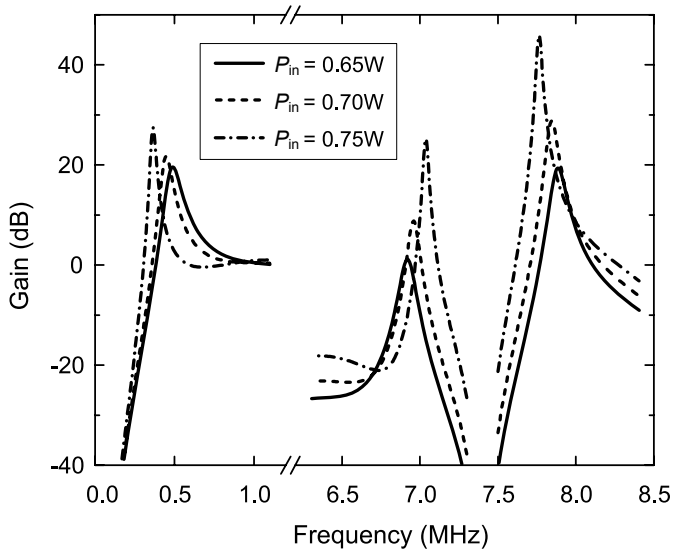


Figure 6.7: Validation of sideband amplification. Frequency variation of the current gain from the channel-noise current source to the amplifier output, calculated with the conversion matrix. Three different P_{in} values have been considered.

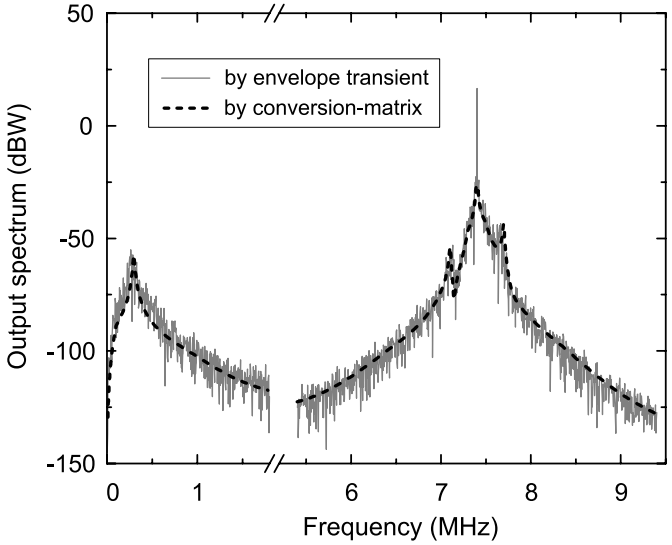


Figure 6.8: Analysis of noisy precursors. Comparison of the simulated output spectrum using the conversion-matrix and the envelope-transient methods. Higher power is obtained at the upper sideband, in agreement with the higher gain value obtained in Figure 6.7.

6.4 Elimination of the Hysteresis in the P_{in}-P_{out} Curve

Hysteresis is commonly observed in the P_{in}-P_{out} curve of power amplifiers. Its accurate prediction with a HB simulator requires the use of a suitable continuation technique, like the one that was proposed in Section 6.2.1. However, the actual design goal would be the total elimination of hysteresis from the P_{in}-P_{out} curve. To our knowledge, no technique has ever been presented for an efficient suppression of this phenomenon. Lengthy trial-and-error procedures are carried out instead. Here a new method will be shown, enabling the elimination of the hysteresis through a single simulation on HB software.

As already discussed, the hysteresis is due to the existence of turning points in the P_{in}-P_{out} curve. Thus, the hysteresis can be suppressed if we remove these turning points.

Taking the curve in Figure 6.3 as an example, the two turning points occur at $P_{in} = 0.790$ W and 0.777 W, with a difference of 0.013 W. These points can be removed by making them approach each other and eventually meet in a single point, corresponding to a "cusp" bifurcation, through the variation of a suitable circuit parameter μ. This parameter can be either an existing circuit component or an added one for the hysteresis elimination. At the "cusp" bifurcation [60], [66], the two turning points meet and, for a further variation of the parameter, disappear from the solution curve, due to the continuity of the system. This continuity also ensures a limited disturbance of the original amplifier response.

As already stated, the Jacobian matrix of the HB system becomes singular at the turning points, due to the existence of a real pole at zero $\gamma = 0$. In [38], it was shown that the Jacobian matrix associated to the non-perturbation equation $Y_{AG} = 0$ also becomes singular at these points. When simulating the amplifier periodic solution, this Jacobian matrix is given by

$$\left[JY_{AG}\right] = \begin{bmatrix} \dfrac{\partial Y_{AG}^{r}}{\partial |V_{AG}|} & \dfrac{\partial Y_{AG}^{r}}{\partial \phi_{AG}} \\ \dfrac{\partial Y_{AG}^{i}}{\partial |V_{AG}|} & \dfrac{\partial Y_{AG}^{i}}{\partial \phi_{AG}} \end{bmatrix}, \tag{6.2}$$

where Y_{AG}^{r} and Y_{AG}^{i} are the real and imaginary part of Y_{AG}, respectively. The derivatives are calculated through finite differences, using HB.

The cusp point is a co-dimension 2 bifurcation, requiring the fine tuning of two parameters [60]. One parameter will be P_{in} and the other, the stabilization element μ. In the plane defined by these two parameters, the locus of turning points is given by

$$\begin{aligned} & Y_{AG}\left(|V_{AG}|, \phi_{AG}, \mu, P_{in}\right) = 0 \\ & \det\left[JY_{AG}\left(|V_{AG}|, \phi_{AG}, \mu, P_{in}\right)\right] = 0 \end{aligned}. \tag{6.3}$$

The above system contains four real unknowns in three real equations, so a curve is obtained in the plane (μ , P_{in}). All the points in this curve have a real pole at zero $\gamma = 0$.

The curve defined by equation (6.3) will be traced from the initial value $\mu = \mu_0$, corresponding to the original circuit. In the case of a multi-valued curve like the one in Figure 6.3, for $\mu = \mu_0$, there will be two different turning points. Provided there is enough sensitivity to μ, the two turning points will vary versus μ and, at given $\mu = \mu_{cp}$, they will meet in a cusp point, obtained for the input power P_{in_cp}. At the cusp point, the two following conditions are satisfied:

$$\begin{aligned} &\gamma(\mu_{cp}, P_{in\_cp}) = 0 \\ &\frac{\partial \gamma}{\partial P_{in}}(\mu_{cp}, P_{in\_cp}) = 0 \end{aligned} \quad . \tag{6.4}$$

Note that all the rest of turning points, composing the locus defined by equation (6.3), fulfill $\partial\gamma / \partial P_{in} \neq 0$, as they give rise to a qualitative stability change in the solution curve. The second condition in equation (6.4) comes from the fact that the unstable section between the turning points does not exist anymore due to the merging of these points, so the real pole does not cross the imaginary axis. Instead, it is tangent to this axis at the origin. For a further μ variation (in the same sense), the solution curve will exhibit no turning points and the hysteresis will be eliminated.

We can implement this technique on a commercial HB simulator. It requires the consideration of the original circuit, plus two identical copies. An AG will be connected to each of the three circuits, with different values of the AG amplitude and phase in each of them. The two copies will enable the calculation of the derivatives that compose the Jacobian matrix of equation (6.2). The first of the three circuits operates at the nominal values $|V_{AG}|$ and ϕ_{AG} and must fulfill the equation (6.3). One of the copies operates at $|V_{AG}| + \Delta|V_{AG}|$ and ϕ_{AG}, and is used for the calculation of the derivative $\partial Y_{AG} / \partial |V_{AG}|$. The other copy operates at $|V_{AG}|$ and $\phi_{AG} + \Delta\phi_{AG}$, and is used for the calculation of the derivative $\partial Y_{AG} / \partial \phi_{AG}$. The three circuits are solved simultaneously in a single HB simulation. In order to obtain the turning-

point locus in the single simulation, the phase ϕ_{AG} is swept, optimizing $|V_{AG}|$, P_{in}, and μ in the nominal circuit, in order to fulfill the equation (6.3).

This approach has been applied here to eliminate the hysteresis phenomenon in our Class-E amplifier. After inspection of the circuit schematic, it was considered that the variation of the elements in the output low-pass filter, composed of L_{lpf} and C_{lpf}, should not strongly affect the drain efficiency and output power. Their possible influence on the turning points of the P_{in}-P_{out} curve was examined. The capacitance C_{lpf} was taken as a stabilization parameter $\mu = C_{lpf}$. The turning-point locus fulfilling equation (6.3) was traced in the plane defined by C_{lpf} and P_{in}, for three different L_{lpf} values.

The results are shown in Figure 6.9. The two P_{in} values obtained for each L_{lpf} and C_{lpf} are the ones corresponding to the turning points in the particular P_{in}-P_{out} curve. For the original amplifier, $L_{lpf} = 257$ nH and $C_{lpf} = 100$ pF, the turning points, indicated with dots in Figure 6.9, are the same as those in Figure 6.3. As can be seen, the range of C_{lpf} values for which the P_{in}-P_{out} curve exhibits turning points decreases with larger L_{lpf}. For each L_{lpf} value, as C_{lpf} decreases, the two turning points approach each other until they meet at the cusp point *CP*. For smaller C_{lpf}, no turning points exist, so no hysteresis phenomenon should be observed in the circuit.

The results of Figure 6.9 have been verified by tracing the P_{in}-P_{out} curves for $L_{lpf} = 257$ nH and different C_{lpf} values between 80 pF and 100 pF (Figure 6.10). For $C_{lpf} = 100$ pF, two turning points are obtained at the power values predicted by the locus of Figure 6.9, and a hysteresis phenomenon is observed. For $C_{lpf} = 90$ pF, the two turning points are closer, in agreement with Figure 6.9, and a narrower hysteresis interval is obtained. For $C_{lpf} = 85$ pF, the two turning points meet at the cusp point CP_2. For $C_{lpf} = 80$ pF, no hysteresis is observed. The small disturbance of the original P_{in}-P_{out} characteristic by the application of this technique should also be noted. Similarly small disturbance can be expected regardless of

the particular circuit. It is due to the continuity of the system, evolving smoothly when the stabilization parameter is varied.

To analyze the effect of the output-filter modification on the amplifier stability, the pole-zero identification technique has been sequentially applied along the solution curves in Figure 6.10. Figure 6.11 shows the variation of the real pole γ_1 versus P_{in}, for each of the considered curves. As can be seen, for C_{lpf} values giving hysteresis, the γ_1-curve crosses the horizontal axis $\gamma_1 = 0$ twice, at the turning points T_1 and T_2. At the cusp point, the γ_1-curve is tangent to the axis $\gamma_1 = 0$, in agreement with equation (6.4). For C_{lpf} values without hysteresis, there is no crossing of the axis $\gamma_1 = 0$.

The analysis of Figure 6.11 has been carried out in a P_{in} range for which the real pole γ_1 is in the neighborhood of the imaginary axis. For $C_{lpf} = 80$ pF, with no hysteresis, a wider P_{in} variation has also been considered. For low P_{in}, there are two pairs of complex-conjugate poles $\sigma_1 \pm j2\pi f_1$ and $\sigma_2 \pm j2\pi f_2$, as in the original circuit. As P_{in} increases, the poles $\sigma_1 \pm j2\pi f_1$ approach each other, merge, and split into two real poles at $P_{in} = 0.83$ W that never cross the imaginary axis to the right-hand side. Although the distance of $\sigma_1 \pm j2\pi f_1$ to the imaginary axis has increased, the precursors are still obtained in simulation. On the other hand, for C_{lpf} values below 50 pF, the instability at $f_a = 1$ MHz, due to the pair of complex-conjugate poles $\sigma_2 \pm j2\pi f_2$, is not observed. This is a beneficial effect of the modification of the output low-pass filter. Thus, in order to obtain a P_{in}-P_{out} curve without hysteresis and without oscillation, capacitor values below 50 pF must be chosen.

The validity of the new technique has also been experimentally verified. Maintaining $L_{lpf} = 257$ nH, the capacitor value C_{lpf} was changed to below 50 pF. The experimental P_{in}-P_{out} curves of the stabilized amplifier with $C_{lpf} = 20$ pF, 10 pF, and 0 pF are shown in Figure 6.12, where they can be compared with the original curve exhibiting a jump. Note that only the curves without oscillation are presented for the stabilized PA. The oscillation was suppressed for a capacitor value smaller than 30 pF. Although this value is lower than the one obtained in

simulation (50 pF), there is a good qualitative agreement with the predictions of Figure 6.10. The reduction of C_{lpf} value eliminates the hysteresis, with minimum disturbance of the power-transfer curve. As the capacitor value decreases, the intermediate range of the curve becomes smoother and shifts to the right in similar manner to Figure 6.10. For the chosen capacitor value $C_{lpf} = 20$ pF, all the output harmonic levels were suppressed more than 50 dB below the fundamental, so the low-pass filter still fulfills the original purpose. No oscillation was observed when varying the input power, but the bumps were still noticeable in the spectrum, both corresponding to the simulations. Thus, an additional technique is needed for the elimination of the noisy precursors. This will be presented in Section 6.5.

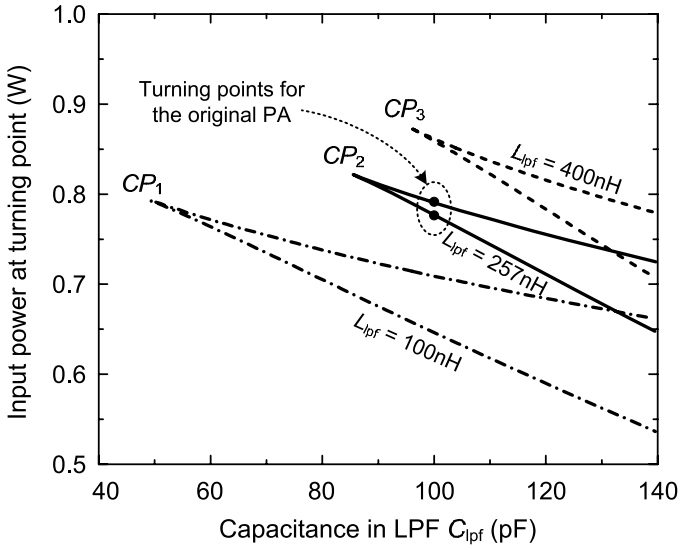


Figure 6.9: Locus of turning points in the plane defined by the stabilization parameter C_{lpf} and the input power P_{in}. The two power values obtained for each L_{lpf} and C_{lpf} correspond to the two turning points of P_{in}-P_{out} curves, like the ones in Figure 6.3. For C_{lpf} smaller than the value corresponding to the cusp point, no turning points are obtained and no hysteresis phenomenon is observed.

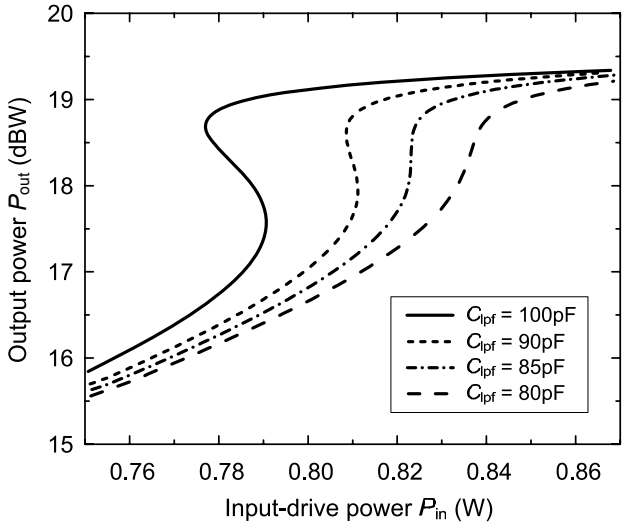


Figure 6.10: Elimination of the hysteresis phenomenon, with $L_{lpf} = 257$ nH. The hysteresis interval becomes narrower as the capacitance C_{lpf} is reduced, in agreement with the loci in Figure 6.9. For capacitor values smaller than $C_{lpf} = 85$ pF, corresponding to the cusp point of this locus, no hysteresis is observed.

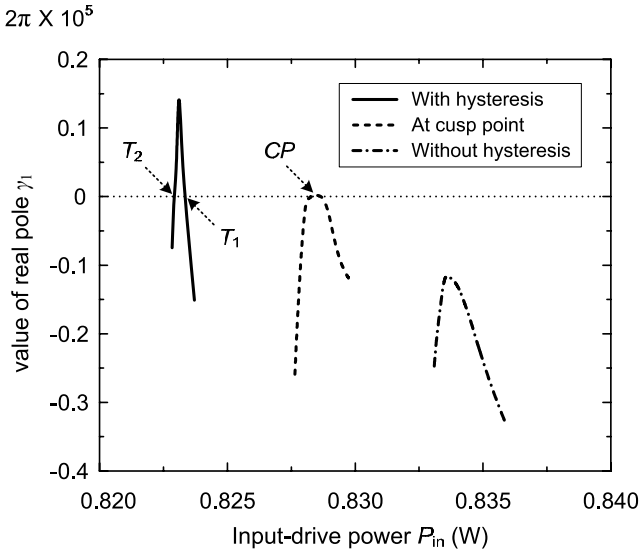


Figure 6.11: Variation of the real pole γ_1 versus the input-drive power for different values of the capacitance C_{lpf}. At the cusp point, the curve is tangent to the horizontal axis.

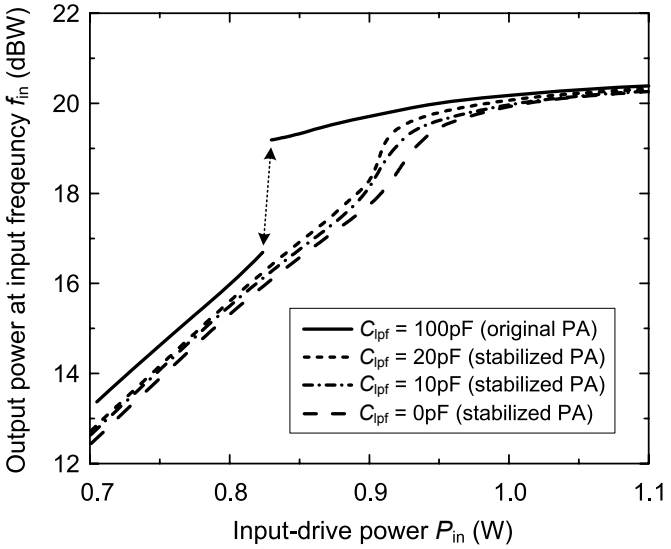


Figure 6.12: Measured P_{in}-P_{out} transfer characteristics before and after the elimination of the hysteresis. For the stabilized PA, only the curves without oscillation are presented.

6.5 Elimination of Noisy Precursors

As already stated, the noisy precursors are noise amplification due to the circuit operation under a small stability margin. Their practical observation is closely dependent on the gain functions from the different noise sources to the circuit output. In order to eliminate the precursors, both aspects must be considered.

From the analysis of Section 6.3, the precursors of the Class-E amplifier are due to the proximity of the pair of poles $\sigma_1 \pm j2\pi f_1$ to the imaginary axis, with $\sigma_1 < 0$ for all the P_{in} values. According to equation (6.1), for a reduction of the precursor power, we need to move σ_1 away from the axis. A possible technique is described in the following.

The same small-signal current source i_s, introduced for the stability analysis, is connected in parallel at the transistor drain terminal. The input admittance from this current source is calculated as the ratio between the delivered current and the node voltage. When traced

versus frequency, this admittance exhibits a clear resonance around 400 kHz, with positive slope of the imaginary part of Y_{in} and positive real part of Y_{in}, because the amplifier solution is stable [65]. The parallel connection of a resistance at the drain terminal will increase *Real* (Y_{in}). In the pole diagram, this will give rise to a leftward movement of the near-critical poles $\sigma_1 \pm j2\pi f_1$, increasing the stability margin. The pole shift will be larger for smaller value of the resistance in parallel. However, the resistance at the transistor output will substantially degrade the drain efficiency and output power of the amplifier. To avoid this degradation, an inductor of relatively high value is connected in series with the resistor. So the correction network is composed of a stabilization resistance of 33 Ω, an inductor of 4 μH and a DC-blocking capacitor of 80 nF in series. This network is connected in parallel at the drain terminal. With the addition of the inductor, the impedance exhibited at f_{in} will be large, and little current will flow at that frequency. However, due to the fact that the resonance frequency f_c is relatively close to f_{in}, the impedance of the inductor at f_c will affect the system poles. To analyze this influence, the pole locus versus P_{in} has been retraced.

In the lower P_{in} range, the introduction of the inductance changes the former complex-conjugate poles $\sigma_1 \pm j2\pi f_1$ into two real poles γ_1' and γ_2', the apostrophe referring to the modified circuit. As P_{in} increases, they approach each other, meet, and become a complex-conjugate pair $\sigma_1' \pm j2\pi f_1'$, with f_1' being significantly smaller than f_1 for the entire P_{in} range. On the other hand, the real part σ_1' is only slightly smaller than σ_1. However, the observation of the precursors is also strongly dependent on the gain from the noise sources to the amplifier output at the near-critical frequencies $f_1', f_{in} - f_1', f_{in} + f_1'$, … This gain has also been analyzed, with the results of Figure 6.13. Compared with Figure 6.7, there is a substantial gain decrease for all the P_{in} values. This is due to high attenuation of the embedding circuit at the much lower value f_1' of the near-critical frequency. The gain curves about the input-drive frequency maintain the Lorentzian shape. Similar low-gain values are obtained when sweeping the current source about $f_{in} - f_1'$ or $f_{in} + f_1'$. The output power

spectrum, simulated with the conversion-matrix and envelope-transient methods, is shown in Figure 6.14. No noise bumps are obtained, which shows the validity of the technique.

The elimination of the precursors has been experimentally confirmed. A separate heatsink is used for the resistor in order to handle the dissipated power at the input-drive frequency. No precursors or instability were obtained in the measurements for the entire range of input power and drain bias voltage, in agreement with the simulations. Figure 6.15 shows a representative measurement of the output power spectrum, corresponding to $P_{in} = 0.95$ W. The noise coming from the input-drive source is still present about f_{in} but, unlike the spectrum of Figure 6.2 (b), no noise bumps are observed about f_{in} or at low frequency. The measured gain and drain efficiency of the corrected amplifier is shown in Figure 6.16. Compared with the original amplifier, the degradation of the drain efficiency is below 1.5 % for all output power levels. The gain is almost same because of the saturated switching operation of the amplifier.

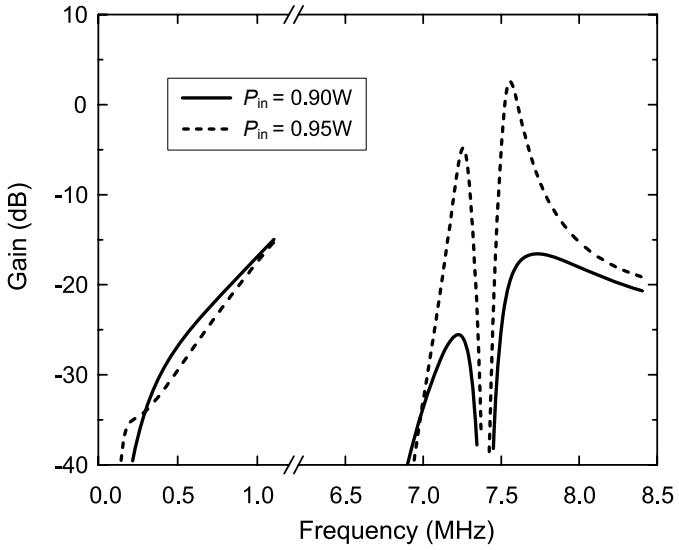


Figure 6.13: Corrected amplifier. Frequency variation of the current gain from the channel-noise current source to the circuit output, calculated with conversion matrix.

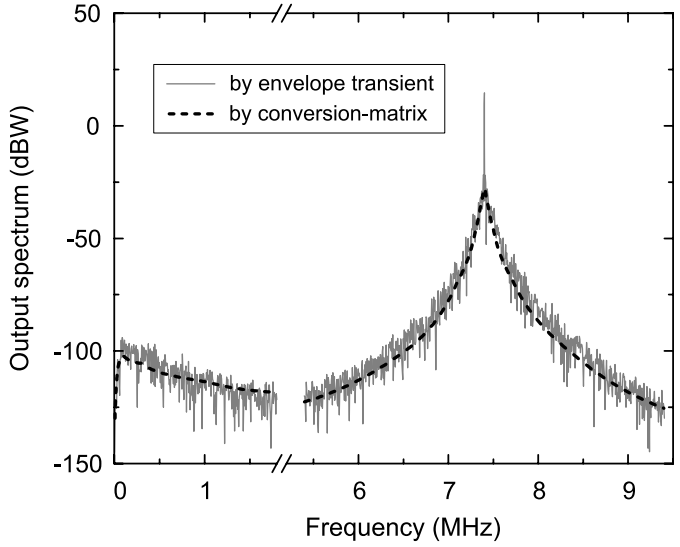


Figure 6.14: Simulated output power spectrum of the corrected amplifier, in which no noise bumps are observed.

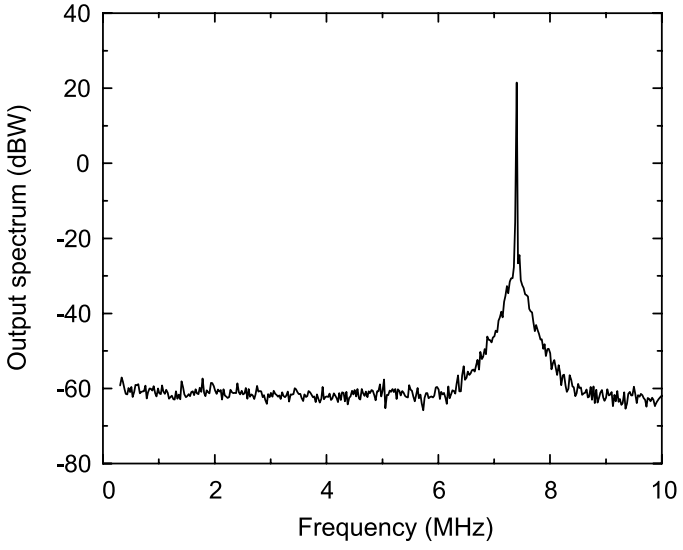


Figure 6.15: Measured output power spectrum of the corrected amplifier at P_{in} = 0.95 W. The noise from the input-drive source is still present about f_{in}. However, the noise bumps have disappeared, which validates the proposed correction technique.

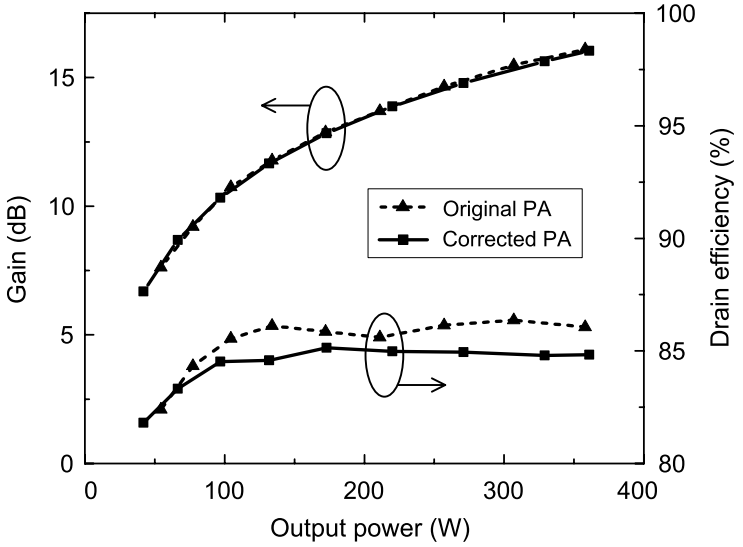


Figure 6.16: Comparison of the measured gain and drain efficiency versus the output power between the original and corrected amplifiers. The input power is 9 W for saturated switching operation in the entire measurements.

Chapter 7

Nonlinear Design Technique for High-Power Switching-Mode Oscillators

RF and microwave high-power sources have diverse applications in the industrial and scientific fields, including induction heating, electric welding, RF lighting, and plasma generation [41], [42], [78]. For power sources, the efficiency is an important aspect because high power loss and its resulting thermal stress will degrade the reliability of transistors and increase the cost for thermal management.

A number of works [79]−[85] have been devoted to improve the DC-to-rf conversion efficiency of oscillators by adopting the switching-mode amplifier concepts. In [79], [80], Class-E oscillators are designed by synthesizing the required phase shift with a feedback network. However, the assumption of lumped elements and the approximate calculation of the transistor phase shift make the technique difficult to apply to high-frequency oscillators. In [81], [82], an experimentally tunable feedback network is added to stand-alone Class-E and Class-F amplifiers, respectively, to give an oscillation at higher frequency. The small-signal circular function [81] and the required attenuation of the feedback network [82] are calculated to fulfill the oscillation condition, but no systematic nonlinear technique is proposed for the design. In [83], the design criterion is also linear and based on the calculation of a small-signal loop gain providing high efficiency in the high-power oscillator. On the other hand, [84] and [85] present systematic nonlinear-design procedures, based on the load-pull optimization of the transistor harmonic terminations. These load-pull techniques are versatile and powerful, since they are not constrained to a specific embedding topology.

However, the performance of the final design is closely dependent on the synthesis accuracy at the different harmonic frequencies.

In this chapter, a new systematic nonlinear technique to optimize the output power and efficiency of switching-mode oscillators is proposed. Although constrained to a specific feedback-network topology, the technique enables a simple and reliable design of high-efficiency oscillators, taking into account an arbitrary number of harmonic components. It combines existing quasi-nonlinear methods [86], [87] with the use of an auxiliary generator (AG) [38] in harmonic balance (HB). An AG is an ideal voltage generator introduced into the circuit only for simulation purposes. It operates at the oscillation frequency and fulfills a non-perturbation condition of the steady-state solution. In the optimization of the switching-mode oscillators, the AG has a twofold role. First, the AG is used to set the oscillation frequency to the desired steady-state value. Hence, circuit parameters can be optimized to maximize the output power and efficiency without affecting the oscillation frequency. Second, the AG with large voltage amplitude drives the transistor in deep saturation region, which leads to the switching-mode operation with high efficiency.

To achieve a robust convergence of the HB system including the AG, the provision of suitable initial values is of importance. Accordingly, a quasi-nonlinear design is initially performed using the techniques developed in previous works [86], [87]. This gives the proper circuit topology and the initial values for the circuit elements. Here, a nonlinear optimization of the amplifier is also carried out, tracing contour plots of the output power and drain efficiency versus critical circuit elements. Then the appropriate embedding network for the oscillator circuit is determined from the resulting terminal voltages and currents.

The oscillator optimization is performed with an AG, the amplitude of which is made equal to that of the input-terminal voltage in the former amplifier design. This ensures the switching-mode operation of the transistor. Using the AG, the circuit parameters are tuned to achieve high output power and efficiency at the specified oscillation frequency. Contour plots

are traced to determine the optimum element values. The oscillation start-up and steady-state stability are verified with the pole-zero identification technique. The influence of the gate bias on the oscillator output power, efficiency, and stability is analyzed, together with the causes for the common observation of hysteresis versus the gate bias in high-power oscillators. The techniques have been applied to the design of a Class-E oscillator, which showed an output power of 75 W from a single transistor and 67 % DC-to-rf conversion efficiency at 410 MHz.

This chapter is organized as follows. Section 7.1 presents the optimization of the initial Class-E amplifier and the synthesis of the embedding network. Section 7.2 presents the nonlinear optimization of the Class-E oscillator, the verification of the oscillation start-up, and the stability analysis of the steady-state solution. Section 7.3 presents the analysis of the influence of the gate bias on the oscillator output power and efficiency. Finally, Section 7.4 presents the experimental results.

7.1 Optimization of Class-E Amplifier and Synthesis of Embedding Network

The Class-E oscillator considered in this work consists of a transistor that operates in the saturation region, and an embedding network that includes the output load. The transistor in an oscillator operates in the same way as in an amplifier under the same set of terminal voltages and currents [86]. Thus, a Class-E amplifier with optimized performance is first designed. Then, the embedding network is synthesized, applying the substitution theorem to the optimized terminal voltages and currents [87]. It should be noted that this synthesis considers only the fundamental frequency, so the performance of the designed oscillator will be further investigated with the proposed fully nonlinear technique in Section 7.2.

7.1.1 Optimization of Class-E Amplifier

The schematic of the Class-E amplifier is shown in Figure 7.1. The active device is the MRF183 LDMOS from Freescale Semiconductor. The series LC tank resonates at the input-drive frequency f_{in}, which must be the same as the oscillation frequency, $f_o = 410$ MHz. Note that the detuning inductance L_{detune}, required for the zero voltage switching (ZVS) [4], is separated from the LC tank. The input-drive level (V_{in}) and the output circuit parameters (C_{out}, Q_{res}, L_{detune}, and R_L) are optimized so that the amplifier achieves a proper Class-E tuning, which leads to high drain efficiency.

The loaded Q-factor of the series resonator Q_{res} is set to 18. This is higher than usual in Class-E amplifiers, where the Q is usually below 10. The higher Q increases losses slightly, but helps to obtain a more stable oscillation. C_{out} and L_{detune} can be calculated using the well-known Class-E design equations [23]:

$$C_{out} = \frac{0.1836}{2\pi f_{in} R_L} , \tag{7.1}$$

$$L_{detune} = \frac{1.1525 R_L}{2\pi f_{in}} . \tag{7.2}$$

Assuming $2\,\Omega$ for R_L, the equations give $C_{out} = 36$ pF and $L_{detune} = 0.9$ nH. Since this transistor already has an output capacitance that is near 36 pF [88], C_{out} is completely absorbed into the transistor.

Starting from these initial values, an HB optimization is next performed, using the nonlinear transistor model provided by the vendor. The considered value of the input-drive amplitude is $V_{in} = 40$ V, for which the transistor operates in the saturated region. For the HB simulation, 11 harmonic components are taken into account. Contour plots of constant output power and constant drain efficiency are traced, respectively, as functions of L_{detune} and R_L, shown in Figure 7.2. As can be seen, the optimum element values to achieve the highest drain efficiency are not the same as the ones providing the highest output power. The output power

keeps increasing until L_{detune} becomes zero, whereas a small detuning inductance is required to satisfy the ZVS condition for the highest drain efficiency. This is due to the fact that the output power has its maximum value at the net resonance frequency of the output LC tank including L_{detune}. We choose $L_{detune} = 0.6$ nH and $R_L = 2.6\ \Omega$, which give the highest efficiency at the expense of some loss of output power.

After setting L_{detune} and R_L to the above optimum values obtained for $V_{in} = 40$ V, the influence of the input-drive level is analyzed. A sweep in V_{in} is carried out, with the results of Figure 7.3. As a compromise between the saturated operation and the maximum voltage rating of the transistor, the initially considered value $V_{in} = 40$ V is chosen. This provides an output power of 58 W and a drain efficiency of 73 %.

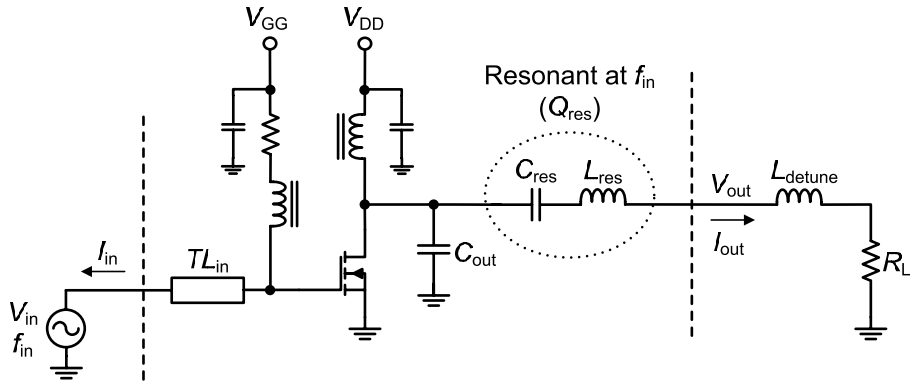


Figure 7.1: Schematic of the Class-E amplifier. The input-drive frequency is set to the oscillation frequency. TL_{in} is a transmission line added at the gate to facilitate the layout of the feedback network, which will be synthesized in Section 7.1.2. Dashed lines represent the reference planes for the synthesis.

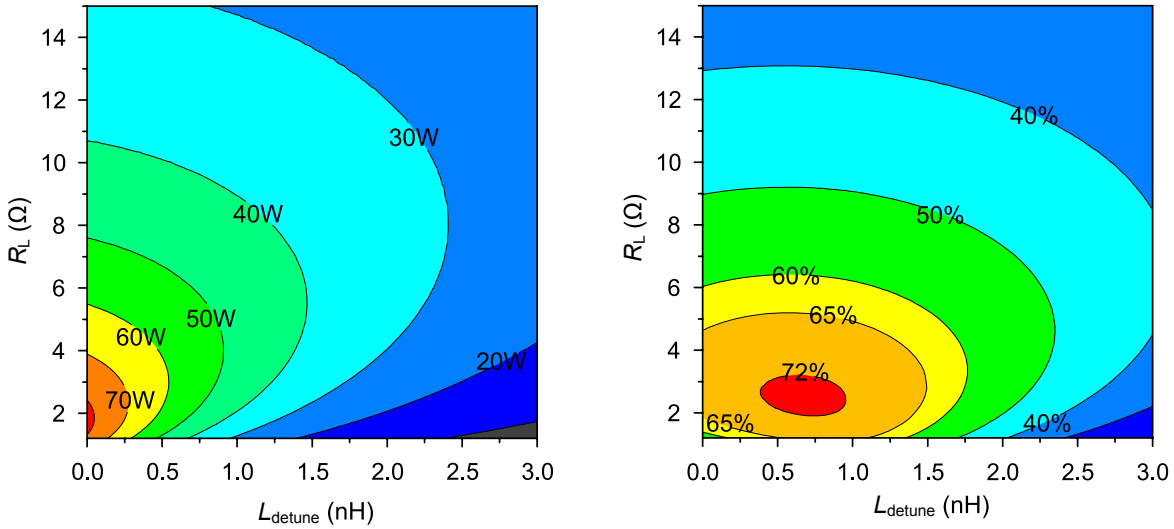


Figure 7.2: Simulated output power (a) and drain efficiency (b) of the Class-E amplifier as functions of detuning inductance and load resistance. The drain and gate bias voltages are 25 V and 4 V, respectively.

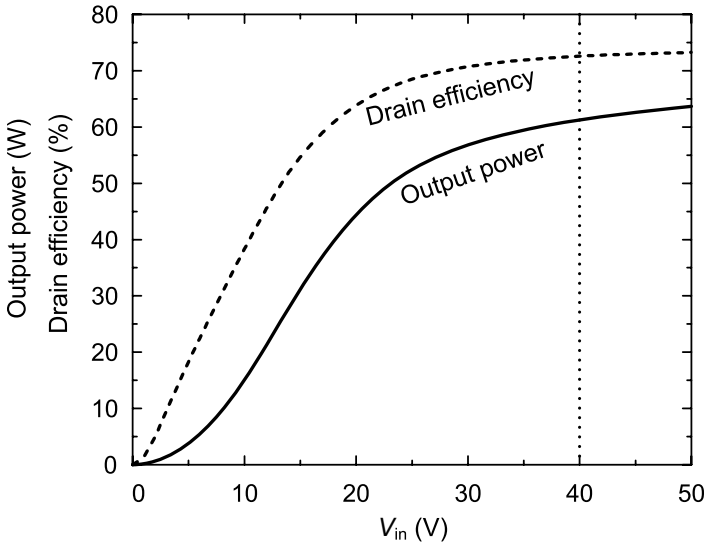


Figure 7.3: Simulated output power and drain efficiency as a function of the input-drive level V_{in}. L_{detune} and R_L are tuned to the maximum drain efficiency point. The dotted line at 40 V represents the determined input-drive level for the saturated operation.

7.1.2 Synthesis of Embedding Network

Once the HB optimization of the amplifier has been carried out, the next step is to synthesize the embedding network from the terminal voltages and currents at the reference planes of Figure 7.1 (indicated with dashed lines). For convenience, both the transmission line TL_{in} and the series LC tank are taken inside the reference planes. This choice of the output-reference plane facilitates the synthesis of the embedding network. Although the optimum terminal voltages and currents are calculated with 11 harmonic components, the strong bandpass-filtering action of the LC tank allows a synthesis of the embedding network at the fundamental frequency only, without substantial degradation of the design accuracy. At all other harmonic frequencies, the drain of the transistor will be terminated by a shunt capacitance or C_{out}, which is the proper harmonic loading for a Class-E oscillator.

The embedding network is usually configured as a T-network or Π-network [87]. In this work, a Π-network is chosen, as shown in Figure 7.4. It consists of three reactive elements (jB_1, jB_2, jB_3) and one resistive element (G_1) representing the load resistance. For this particular network, the 2-port Y-parameters relating the terminal currents, I_{in}, I_{out}, and voltages, V_{in}, V_{out}, are

$$\begin{bmatrix} I_{\text{in}} \\ I_{\text{out}} \end{bmatrix} = \begin{bmatrix} j(B_2 + B_3) & -jB_2 \\ -jB_2 & G_1 + j(B_1 + B_2) \end{bmatrix} \begin{bmatrix} V_{\text{in}} \\ V_{\text{out}} \end{bmatrix}. \tag{7.3}$$

Thus, the four element values are calculated in terms of the terminal voltages and currents, as follows:

$$\begin{bmatrix} B_2 \\ B_3 \end{bmatrix} = \begin{bmatrix} \text{Im}\{V_{\text{out}}\} - \text{Im}\{V_{\text{in}}\} & -\text{Im}\{V_{\text{in}}\} \\ \text{Re}\{V_{\text{in}}\} - \text{Re}\{V_{\text{out}}\} & \text{Re}\{V_{\text{in}}\} \end{bmatrix}^{-1} \begin{bmatrix} \text{Re}\{I_{\text{in}}\} \\ \text{Im}\{I_{\text{in}}\} \end{bmatrix}, \tag{7.4}$$

$$\begin{bmatrix} G_1 \\ B_1 \end{bmatrix} = \begin{bmatrix} \text{Re}\{V_{\text{out}}\} & -\text{Im}\{V_{\text{out}}\} \\ \text{Im}\{V_{\text{out}}\} & \text{Re}\{V_{\text{out}}\} \end{bmatrix}^{-1} \begin{bmatrix} \text{Re}\{I_{\text{in}} + I_{\text{out}}\} + B_3\,\text{Im}\{V_{\text{in}}\} \\ \text{Im}\{I_{\text{in}} + I_{\text{out}}\} - B_3\,\text{Re}\{V_{\text{in}}\} \end{bmatrix}. \tag{7.5}$$

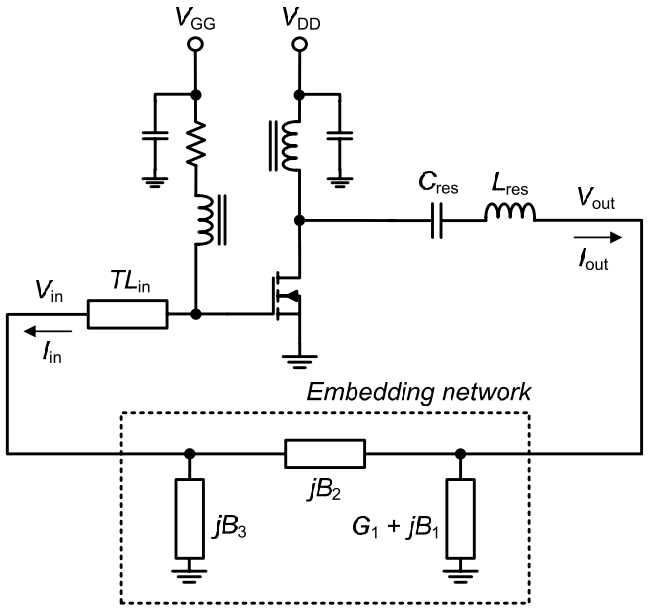


Figure 7.4: Basic structure of the Class-E oscillator, consisting of a transistor, a series LC tank, and an embedding network. The embedding network substitutes for the input-drive source and output load circuitry of the Class-E amplifier in Figure 7.1, keeping the same set of terminal voltages and currents.

In order for equations (7.4) and (7.5) to be solvable, the matrices on the right-hand side must be invertible (not singular). As derived in [87], this requires two conditions, easily fulfilled by the amplifier: V_{out} must not be zero and a phase difference between V_{in} and V_{out} must exist. The element values for the T-network could also be derived in a similar way.

The fundamental components of the terminal voltages and currents of the optimized amplifier in Section 7.1.1 are shown in Table 7.1. The phase of V_{in} is set to 0° without loss of generality. The element values of the embedding network, obtained from equations (7.4) and (7.5), are shown in Table 7.2. As can be seen, the network will be composed of two capacitors for B_2 and B_3, an inductor for B_1, and a resistive component transformed from the output load.

Table 7.1: Optimized terminal voltages and currents at fundamental frequency.

V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)
$40.0\, e^{j0°}$	$2.6\, e^{j\,91.3°}$	$19.9\, e^{-j\,25.8°}$	$6.9\, e^{-j\,52.1°}$

Table 7.2: Evaluated element values of embedding network and corresponding circuit elements.

Element	G_1	B_1	B_2	B_3
Evaluated value	302.9 mS	-147.5 mS	6.7 mS	60.6 mS
Circuit element	$R_1 = 3.3\ \Omega$	$L_1 = 2.6$ nH	$C_2 = 2.6$ pF	$C_3 = 23.5$pF

Figure 7.5 shows the complete schematic of the Class-E oscillator with the implemented embedding network. A shunt transmission line of 110 Ω characteristic impedance (TL_{ind}) is used for the implementation of L_1. The 50 Ω output load is transformed to R_1 by a simple L-section matching ($C_o = 28$ pF and a transmission line TL_o) [49]. This oscillator configuration with the determined element values will serve as the starting point for the new nonlinear optimization, to be presented in Section 7.2.

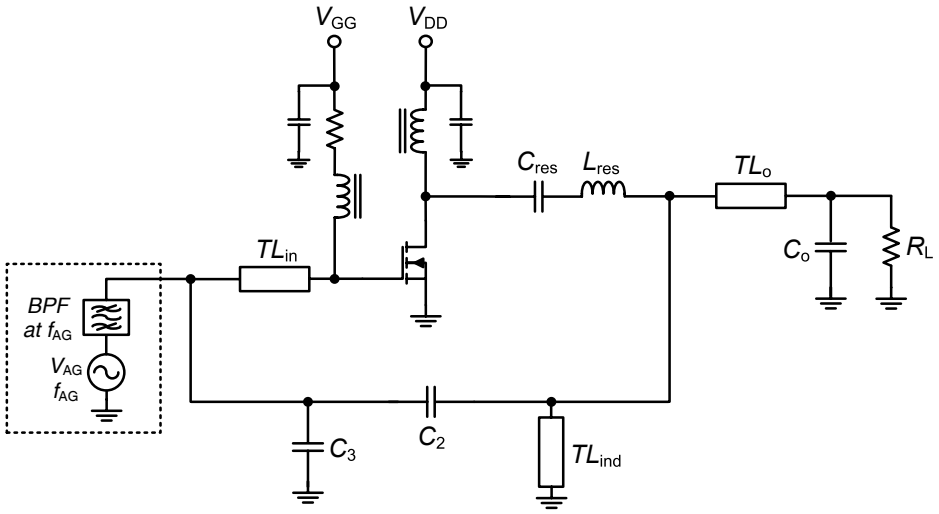


Figure 7.5: Complete schematic of the Class-E oscillator. The embedding network is implemented by capacitors (C_2, C_3, C_o), transmission lines (TL_{ind}, TL_o), and a 50 Ω load (R_L). The AG, consisting of a voltage source and an ideal bandpass filter inside the dashed box, is not a part of the oscillator, but will be used for the nonlinear simulation of oscillatory solutions in Section 7.2.

7.2 Nonlinear Optimization of the Oscillator Performance

In Section 7.1, the Class-E oscillator was optimized in terms of the output power and efficiency, taking into account the saturated operation of the transistor. However, the design has two intrinsic limitations. As already stated, the synthesis of the embedding network is carried out, considering only the fundamental frequency. In spite of the judicious choice of the output-reference plane to reduce the influence of the other harmonic components, the approach is not appropriate to accurately predict the performance of switching-mode oscillators in which many harmonics are strongly generated. Moreover, the onset of the oscillation from a small-signal level is not guaranteed by the steady-state oscillation condition. The oscillation start-up should be investigated separately to check whether or not the oscillation is triggered truly and growing to the designed power level.

To overcome those limitations, a new optimization technique taking into account all the generated harmonic components will be employed, together with the stability analysis based on pole-zero identification.

7.2.1 Nonlinear Optimization through the AG Technique

The AG technique was initially proposed to avoid trivial solutions in the HB simulation of autonomous circuits [38]. However, the AG can also be used for nonlinear oscillator design at a specific frequency, using HB. The AG, composed of a voltage source and a bandpass filter in series (Figure 7.5), is connected in parallel at a circuit node. The AG frequency is made equal to the oscillation frequency $f_{AG} = f_o$. The series bandpass filter is an ideal short circuit at f_{AG} and an open circuit at all the other frequencies. Thus, the AG amplitude V_{AG} agrees with the fundamental component of the voltage amplitude at the connection node. Since the AG is introduced only for simulation purposes, it should have no influence on the steady-state oscillatory solution. This is imposed by the following non-perturbation condition:

$$Y_{AG} = I_{AG} / V_{AG} = 0 \ , \tag{7.6}$$

where I_{AG} is the current through the AG at f_{AG}. The equation (7.6) is solved through error-minimization or optimization procedures, with the HB system as the inner loop. For the optimization of the power oscillator, the AG is connected to the same node considered in the definition of the input-reference plane in Figure 7.1. Thus, the AG amplitude V_{AG} is made equal to the input-drive amplitude $V_{in} = 40$ V obtained in Section 7.1, i.e., $V_{AG} = 40$ V. In this way, the transistor is in deep saturation during the nonlinear simulation, which leads to the switching-mode operation of the oscillator. The AG frequency, f_{AG} is set to the desired oscillation value, 410 MHz. With both the AG amplitude and frequency imposed by the designer, two circuit element values must be determined in order to fulfill the non-perturbation condition (7.6). In our oscillator, two capacitors in the feedback network, C_2

and C_3, are calculated. The rest of elements are set to the values obtained in Table 7.2. Equation (7.6) is solved through optimization in HB, considering 11 harmonic components. The simulation predicts 61 W output power with 71 % DC-to-rf conversion efficiency for the imposed V_{AG} value, $V_{AG} = 40$ V. This agrees well with the amplifier performance for the same input-drive voltage $V_{in} = 40$ V in Section 7.1.

To investigate the influence of the feedback-element values on the oscillator performance, two nested sweeps are carried out in C_2 and C_3. For each pair of capacitance values (C_2, C_3), the oscillation amplitude V_{AG} and the capacitance (or the inductance) in the series LC tank, i.e., C_{res} (or L_{res}) are optimized, in order to fulfill the non-perturbation condition $Y_{AG} = 0$. It is important to note that the oscillation frequency keeps the desired value during the entire double sweep, which is ensured by setting the AG frequency to $f_{AG} = 410$ MHz. In contrast, the oscillation amplitude is modified during the sweep, since V_{AG} is one of the considered optimization variables, together with C_{res} (or L_{res}).

The simulated contours of constant output power and constant efficiency in the plane of (C_2, C_3) are shown in Figure 7.6. The efficiency in Figure 7.6 (a) exhibits its maximum value near the point resulting from the quasi-nonlinear analysis, corresponding to 2.6 pF of C_2 and 23.5 pF of C_3 (marked by a star). It means that the effect of harmonic components on the efficiency is not too significant in this particular Class-E oscillator. This is mainly due to the series LC tank with high Q-factor, which prevents the harmonics generated at the drain from affecting the output load. This confirms the assumptions in the synthesis technique discussed in Section 7.1.2. It is also interesting to see that the contour plot in Figure 7.6 (a) has a narrow ridge of the efficiency along the dashed line. By changing (C_2, C_3) along this line, the oscillator output power could be optimized further, maintaining a high efficiency of more than 67 %.

As can be seen in Figure 7.6 (b), the output power does not show its peak at the point marked with a star but keeps increasing along the dashed line toward the point marked with a

square. Hence, the feedback elements can be modified from the original values determined in Section 7.1, in order to obtain a higher output power without impairing the efficiency significantly.

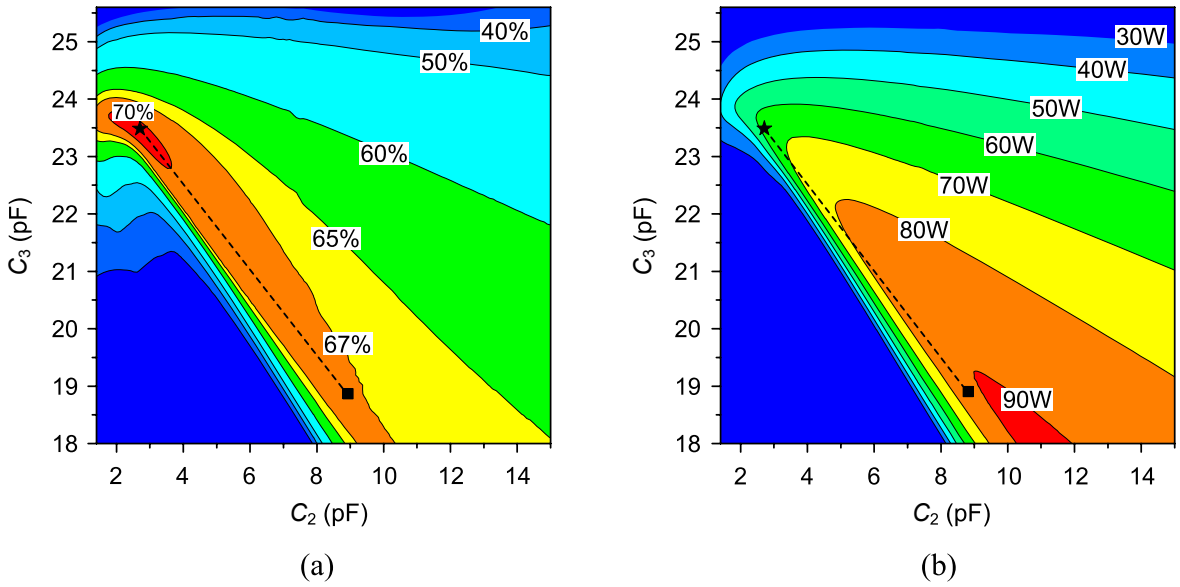


Figure 7.6: Contour plots of the simulated DC-to-rf conversion efficiency (a) and output power (b) in the plane of (C_2, C_3). For the entire solutions, the oscillation frequency is fixed to 410 MHz. The points of a star and a square represent, respectively, the original values of (C_2, C_3) obtained in Section 7.1 and the new values nonlinearly optimized in the output power and efficiency.

For the circuit-element values corresponding to the square point ($C_2 = 9.0$ pF, $C_3 = 18.7$ pF), the oscillation amplitude fulfilling the non-perturbation condition (7.6), at the imposed frequency $f_{AG0} = 410$ MHz, is $V_{AG0} = 97$ V. The predicted output power is 85W with 68 % DC-to-rf conversion efficiency. We did not want to further increase the output power because the transistor might become too hot. Figure 7.7 shows the simulated voltage and current waveforms at the extrinsic drain terminal. Due to the complete absorption of C_{out} into the transistor output capacitance, the drain current exhibits an almost sinusoidal waveform.

The above analysis and optimization are applied to the circuit in its steady-state oscillatory regime. However, even if the obtained solutions are accurate and valid, the oscillator might fail to start up from its DC solution with the optimized values of the circuit elements. The oscillation start-up from the DC regime is due to the instability of the DC solution at the oscillation frequency. Thus, the start-up condition depends on this DC solution and its stability properties. The stability of the DC solution and that of the steady-state oscillatory solution must be separately analyzed, as will be shown in Section 7.2.2.

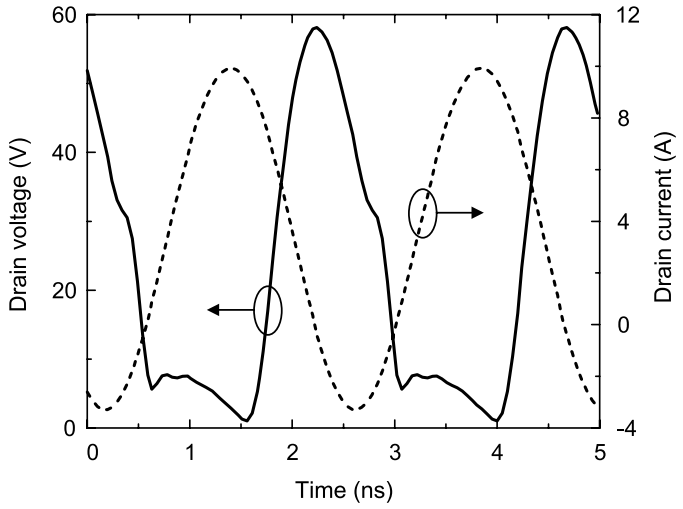


Figure 7.7: Simulated voltage and current waveforms at the extrinsic drain terminal, corresponding to the square point in Figure 7.6. The drain and gate bias voltages are 25 V and 4 V, respectively.

7.2.2 Stability Analysis

To verify the oscillation start-up, the stability of the DC solution, coexisting with this oscillation, must be analyzed. This is done with the pole-zero identification technique, which, in the case of a DC solution, requires the calculation of the input impedance function $Z_{in}(f)$ at a given circuit node through AC analysis. A sweep in the frequency f is carried out, applying

pole-zero identification to the resulting function $Z_{in}(f)$. In our Class-E oscillator, the considered observation port, at which $Z_{in}(f)$ is calculated, is defined between the gate node and ground.

For the stability analysis, the parameters C_2 and C_3 are varied along the dashed line in Figure 7.6 by changing C_2 in 1 pF steps and calculating the corresponding C_3 from the linear equation of the dashed line. Pole-zero identification is applied to the DC solution associated with each pair of values C_2 and C_3. For all the points in the line, a pair of complex-conjugate poles, with frequency close to the oscillation frequency, is located on the right-hand side of the complex plane. The evolution of this critical pair of poles along the dashed line is shown in Figure 7.8. All the pairs are located in the right-hand side of the plane with a nearly constant imaginary part. This implies that all the points along the dashed line satisfy the oscillation start-up condition around 410 MHz. The nearly constant value of this frequency is explained by the fact that the oscillation frequency was kept constant at the nonlinear design stage by setting $f_{AG} = 410$ MHz. However, the real part of the pole pair, indicating the instability margin for start-up, is very small at low values of C_2 and increases as (C_2, C_3) approaches the square point along the line. This means that the square point is less likely to be affected in start-up by inaccuracies of the circuit model.

The stability of the steady-state oscillation at this optimum point must also be analyzed, which will also be carried out using the pole-zero identification technique. For this analysis, the AG is maintained at the amplitude $V_{AG0} = 97$ V and frequency $f_{AG0} = 410$ MHz which fulfill $Y_{AG} = 0$ at the point marked with a square in Figure 7.6. Then, a small-signal current source at frequency f is added to the circuit. By the conversion-matrix approach, the impedance function $Z_{in}(f)$ is calculated as the ratio between the node voltage and the introduced current. Pole-zero identification is applied to this impedance function. For a rigorous analysis, several frequency intervals are considered in the range from 0 to f_{AG0}. When sweeping near f_{AG0}, a pair of complex-conjugate poles at this oscillation frequency is located on the imaginary axis, as expected in an oscillatory regime [38]. The rest of poles, for

all the different frequency sweeps, are located on the left-hand side of the complex plane, which indicates a stable oscillation.

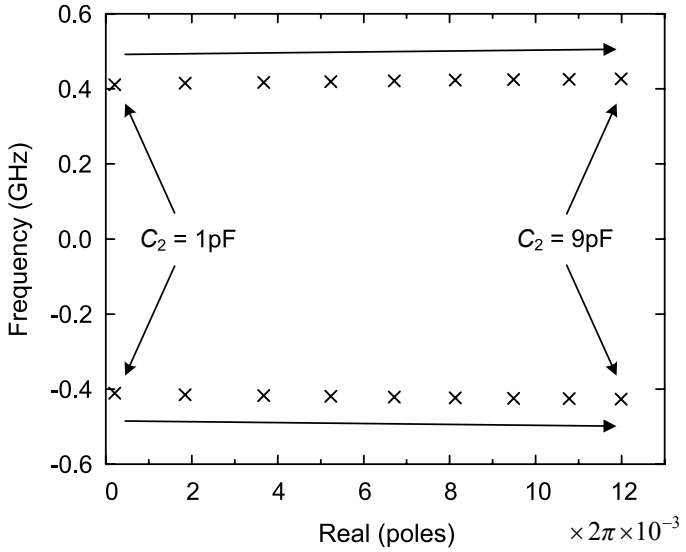


Figure 7.8: Evolution of the critical pole pair with the values of C_2 and C_3 varied along the dashed line in Figure 7.6. C_2 is varied from 1 pF to 9 pF in steps of 1 pF along the dashed line and the corresponding value of C_3 is calculated from the dashed-line equation. At each point of (C_2, C_3), pole-zero identification is carried out on the input impedance function, which is obtained from the linearized DC solution.

7.3 Analysis of the Oscillating Solution versus the Gate Bias

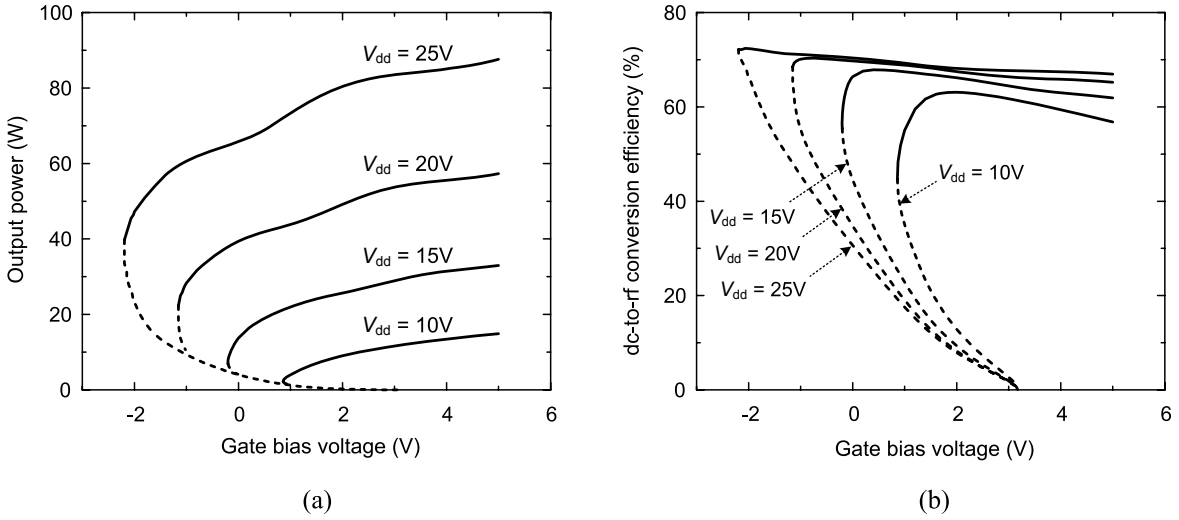
Typically, Class-E amplifiers and oscillators exhibit higher efficiency for gate bias below the threshold voltage. However, in the case of oscillators, the start-up does not occur for gate bias below this threshold because no actual gain is exhibited by the transistor and so the DC solution is stable. Nevertheless, after the oscillation build-up for gate bias above the threshold voltage, it might be possible to experimentally reduce this bias voltage below the threshold

while the oscillatory regime is still observed. This may lead to an oscillation with higher efficiency. As an example, a triggering signal is used in [89] to start up a high efficiency oscillation at low gate bias voltage. The requirement for this signal must be due to the coexistence of the desired oscillatory regime with a stable DC solution.

The evolution of the steady-state oscillation when reducing the gate bias is analyzed here, using an AG. For the simulation, the element values of the optimized design corresponding to the square point in Figure 7.6 are considered. The gate bias is reduced from $V_{gg} = 5$ V, calculating, at each sweep step, the oscillation amplitude V_{AG} and frequency f_{AG} in order to fulfill the non-perturbation condition $Y_{AG}(V_{AG}, f_{AG}) = 0$. When performing this gate-bias sweep, the bias can be reduced below the threshold voltage with the HB solution still converging to a steady-sate oscillation. A switching-parameter algorithm [38] must be applied to obtain the entire oscillation curve. Below a certain gate bias, the AG amplitude is swept instead of V_{gg} and reduced to zero, determining, at each sweep step, the bias voltage V_{gg} and oscillation frequency f_{AG} in order to fulfill the non-perturbation condition $Y_{AG}(V_{gg}, f_{AG}) = 0$.

In Figure 7.9, the oscillation curve has been traced for four different values of the drain bias voltage. Figure 7.9 (a) shows the output power variation and Figure 7.9 (b) shows the efficiency variation versus the gate bias. Each curve has a turning point that divides it into a stable and an unstable section. As will be shown later, the solid-line section corresponds to stable solutions, whereas the dashed-line section corresponds to unstable ones. All curves start from zero amplitude at the threshold voltage, $V_{gg} = 3.2$ V. At this voltage value, a Hopf bifurcation takes place in the DC solution [38], i.e., a pair of complex-conjugate poles at the oscillation frequency crosses the imaginary axis. The DC solution is unstable above the threshold voltage. The Hopf bifurcation is of subcritical type [38], [60]. Thus, after the bifurcation, no stable oscillation exists in the neighborhood of the DC solution, which gives rise to a jump to the upper section of the oscillation curve in Figure 7.9. On the other hand, when the gate bias is reduced from a voltage above the threshold, the oscillation persists until

it reaches the turning point, below which no oscillation is possible. Thus, a hysteresis phenomenon is obtained versus the gate bias.



(a) (b)

Figure 7.9: Simulated output power and DC-to-rf conversion efficiency in the oscillatory regime as a function of the gate bias voltage. Four drain bias voltages (V_{dd}) are considered. The solid-line and dashed-line sections represent the stable and unstable oscillating solutions, respectively, in each solution curve.

The stability of the oscillation curves in Figure 7.9 has been analyzed with pole-zero identification. A turning point in a periodic-solution curve corresponds to the Floquet multiplier crossing the unit circle through $1 + j0$ [60]. Due to the non-univocal relationship between poles and multipliers, this is equivalent to the simultaneous crossing of the imaginary axis by a real pole and infinite pairs of poles $\pm jkf_o$, with k positive integer and f_o the oscillation frequency [60]. For the pole-zero identification, a frequency sweep about f_o will be initially considered. Near the turning point, a pair of complex-conjugate poles $\sigma \pm jf_o$ is obtained at the oscillation frequency. This is an additional pair of poles different from the one located on the imaginary axis at $\pm jf_o$, which exists for all points in the curve due to the solution autonomy.

In the solid-line section of Figure 7.9, near the turning point, the pair of poles $\sigma \pm jf_o$ is located on the left-hand side of the complex plane. When varying the gate bias from the solid-line section to the dashed-line one around the turning point, the pair of poles approaches the imaginary axis and crosses it at the turning point. Then, the pair of poles $\sigma \pm jf_o$ stays on the right-hand side for all the entire dashed-line section, so this section is unstable. This is shown in the pole locus of Figure 7.10, corresponding to $V_{dd} = 25$ V. For all the considered solution points, another pair of poles at f_o, very close to the imaginary axis, is also obtained. This is represented by solid squares. It must be pointed out that, to clearly obtain the two distinct pairs of poles at $\pm jf_o$ and $\sigma \pm jf_o$, high accuracy is necessary in the HB calculation of the steady-state oscillating solution.

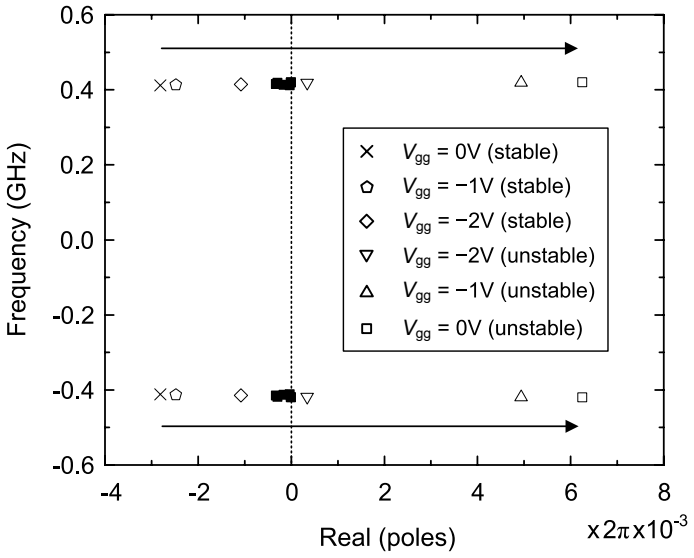


Figure 7.10: Evolution of the critical pole pair for the steady-state oscillating solution as the gate bias varies from the stable section to the unstable one near the turning point in Figure 7.9. The solid squares close to the imaginary axis represent another pair of complex-conjugate poles at each bias point, exhibited due to the singularity of the HB system for oscillating solutions.

The hysteresis in the oscillation curves of Figure 7.9 comes from the fact that a high power oscillation is built up when the gate bias reaches the threshold voltage. This is related to the high input-drive voltage considered in the initial amplifier design of Section 7.1, in order to ensure the switching-mode operation. In the oscillator design, the embedding network is synthesized from the terminal voltages and currents associated with this high-amplitude solution. Once the oscillation builds up at gate bias above the threshold, there exists a high-amplitude oscillating signal at the gate over the quiescent gate bias voltage. This signal turns the transistor on and off as in a switch, as shown in Figure 7.11 (the solid waveform). When the gate bias is reduced below the threshold voltage, this self-generated input-drive signal decreases in a continuous manner, so it is still large enough to make the transistor operate as a switch (see the dashed waveform in Figure 7.11). The situation is different when the gate bias is increased from a DC regime. In that case, no oscillation is possible until the threshold is reached, because there is no input-drive signal to the transistor.

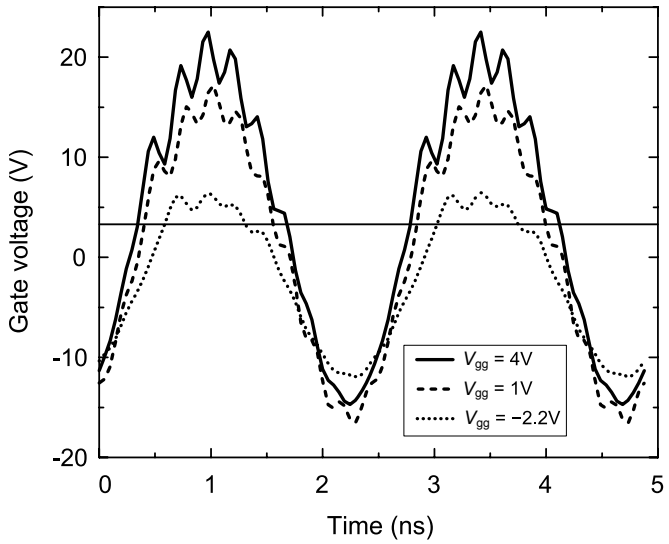


Figure 7.11: Gate voltage waveforms at different gate bias voltages. The threshold voltage is represented by a thin solid line. The considered drain bias is 25 V.

When the gate bias is decreased to the turning point, the self-generated input-drive signal becomes marginal to turn on the transistor and so to sustain the steady-state oscillation (see the dotted waveform in Figure 7.11). If the gate bias is further decreased, no oscillation is observed. As can be seen in Figure 7.9, and in agreement with the previous discussion, the gate bias voltage at the turning point decreases with the drain bias, because a larger swing is obtained in the gate voltage waveform.

In switching-mode amplifiers and oscillators, the output power is usually modified by varying the drain-bias voltage [4], [32], [81], [83], [85]. The reduction of output power, which might be required for some applications, is achieved by decreasing the drain bias, which generally gives rise to a severe degradation of the drain efficiency [32], [81], [83], [85]. This can be avoided by taking advantage of the possibility to maintain the oscillation at the gate bias below the threshold voltage. It enables the reduction of the output power without the efficiency degradation. As shown in Figure 7.9 (a), the output power decreases as the gate bias approaches the turning point. The efficiency, however, increases with lower gate bias <see Figure 7.9 (b)>, as expected in a Class-E oscillator. Hence, the output power can be varied by changing the gate bias down to the turning point, which provides higher efficiency. It must be noted, however, that the stable oscillation and the stable DC solution coexist in the interval comprised between the turning point and the Hopf bifurcation. Each of these two stable solutions has its own basin of attraction in the phase space [38]. Thus, the oscillatory solution will be robust under noise and small perturbations, but a big perturbation such as a high amplitude pulse may lead the system back to the stable DC solution.

For a rough test for the robustness of the oscillation below the threshold voltage, envelope-transient simulations [67], [68] are performed. A sweep is carried out in the gate bias, which is reduced from $V_{gg} = 4$ V to lower values. At each bias-sweep step, the HB solution corresponding to $V_{gg} = 4$ V is used as the initial value for the envelope-transient equations. Actually, an AG with the steady-state values $V_{AG0} = 97$ V and $f_{AG0} = 410$ MHz, corresponding to $V_{gg} = 4$ V, is connected to the circuit for a short initial time interval and

disconnected afterwards. This disconnection is carried out with a time-varying resistor [69]. Figure 7.12 shows the time variation of the first harmonic amplitude of the voltage at the AG connection node. At 0.1 μs, the AG is disconnected for all the V_{gg} values. After a certain transient time, each solution reaches the steady-state amplitude, which decreases with smaller V_{gg} as expected from Figure 7.9. When V_{gg} is reduced below the turning point, for example −2 V, the oscillation is extinguished.

The simulation of Figure 7.12 shows that, below the threshold voltage, the stable oscillation can be reached even when the initial conditions are not in the immediate neighborhood of the steady-state values. The robustness of the oscillation will actually depend on the size of the basin of attraction for this solution in the phase space [38], which would be extremely difficult to determine.

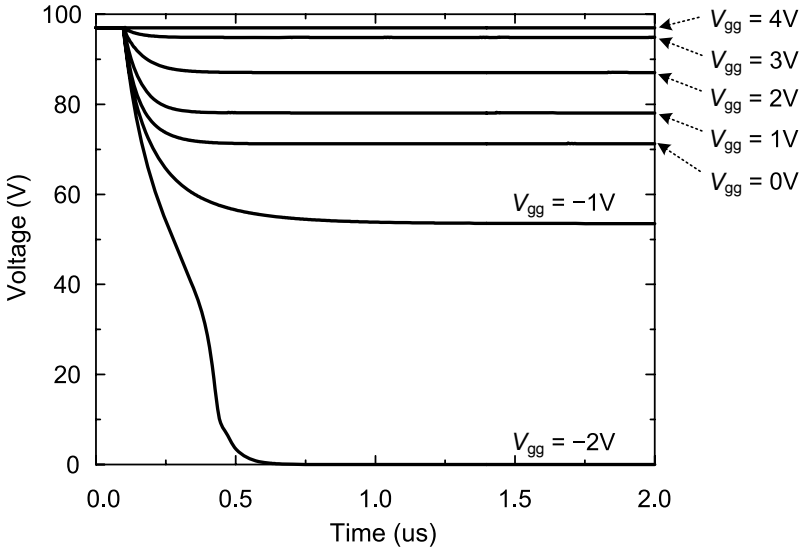


Figure 7.12: Simulated evolution of the oscillating solution as the gate bias changes from 4 V to different values. The fundamental component of the voltage at the AG connection node is represented. The AG is disconnected at 0.1 μs. The considered drain bias is 25 V.

7.4 Experimental Results

The Class-E oscillator designed following the proposed technique is fabricated on FR-4 board. Figure 7.13 shows the photo of the oscillator mounted on a heatsink. An air-core inductor from Coilcraft with a current rating of 7.2 A is used for the inductor in the output LC tank. For tuning purposes, Giga-Trim variable capacitors from Johanson are employed along with ATC multi-layer capacitors. The capacitors are tuned to the nonlinearly optimized values obtained in Section 7.2 (marked by the square in Figure 7.6), which are 9.0 pF for C_2 and 18.7 pF for C_3.

The output power is measured by a Bird 4022 power sensor and a 4421 power meter. Figure 7.14 shows the measured output power and DC-to-rf conversion efficiency versus the drain bias voltage at three different gate bias voltages. The gate biases are slightly above the threshold voltage of the transistor, to give a free running oscillation. The output power increases as the square of the drain bias, as expected in a switching-mode operation [4]. The efficiency increases rapidly at low drain bias and saturates at high drain bias. As the gate bias increases, the efficiency is reduced, but the oscillator exhibits higher output power. This is due to the fact that the Class-E tuning shows the highest efficiency with the gate bias below the threshold voltage. The oscillator achieves the highest efficiency of 69 % with 67 W output power, and 67 % efficiency with 75 W at higher bias voltage. These results are compared with those of other switching-mode oscillators of high efficiency in Table 7.3.

The hysteresis in terms of the gate bias is also experimentally verified. After the oscillation builds up at a gate bias of 4 V, the bias voltage is reduced gradually down to 0 V. The oscillation is sustained for all the gate bias voltages. Figure 7.15 shows the measured output power and efficiency versus the gate bias. The output power decreases when the gate bias is reduced, whereas the efficiency improves, in comparison with the values corresponding to the gate bias of V_{gg} = 4 V.

The output power spectrum, measured by an Agilent E4407B spectrum analyzer, is shown in Figure 7.16. The simulated spectrum is superimposed with square marks. The largest harmonic level is 46 dB below the fundamental, which corresponds to the second harmonic component. High-frequency ringing is observed at the fifth and sixth harmonics in the measured spectrum. It is due to a parasitic resonance when the transistor is turned on and off abruptly [46]. The phase noise is −117 dBc/Hz at a frequency offset of 100 kHz.

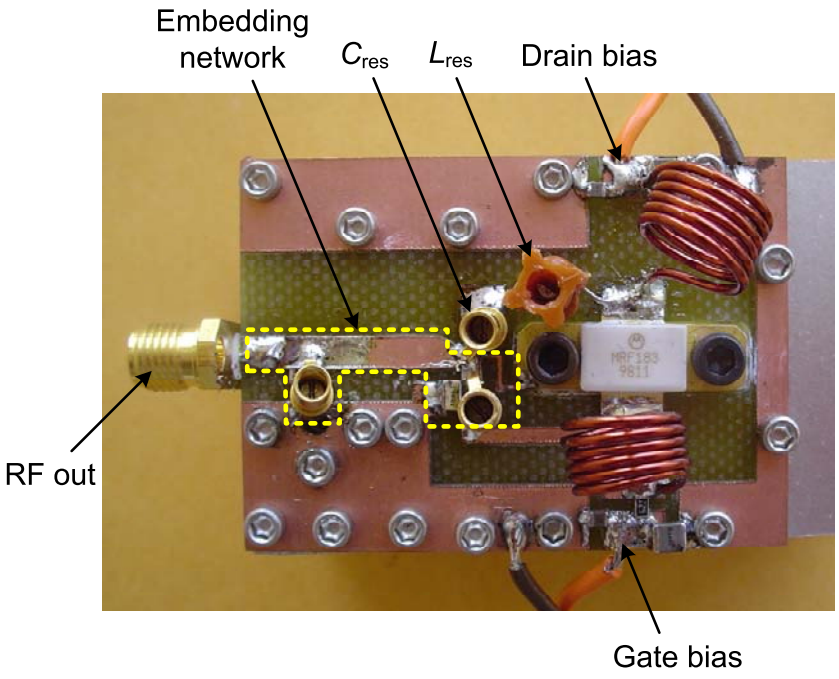


Figure 7.13: Photo of the Class-E oscillator built on FR-4 board. The transistor is mounted directly on a heatsink through a slot in the board. The circuit size is 49 mm x 35 mm.

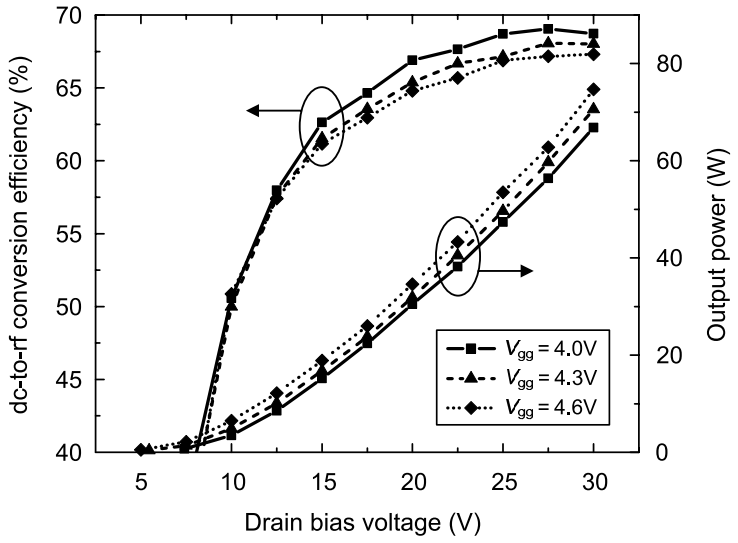


Figure 7.14: Measured output power and DC-to-rf conversion efficiency versus the drain bias voltage.

Table 7.3: Performance comparison of published switching-mode oscillators.

Oscillation frequency	Output power	Efficiency	Class	Reference
2 MHz	3 W	95 %	E	[79]
800 kHz	1.19 W	86 %	E	[80]
5 GHz	0.47 W	56 %	E	[81]
1.6 GHz	0.25 W	67 %	F	[82]
915 MHz	65 W	65 %	Not specified	[83]
1.86 GHz	< 0.03 W	61 %	Between B and F	[84]
6 GHz	Not specified	48 %	F	[85]
410 MHz	**75 W**	**67 %**	**E**	**This work**
410 MHz	**67 W**	**69 %**	**E**	**This work**

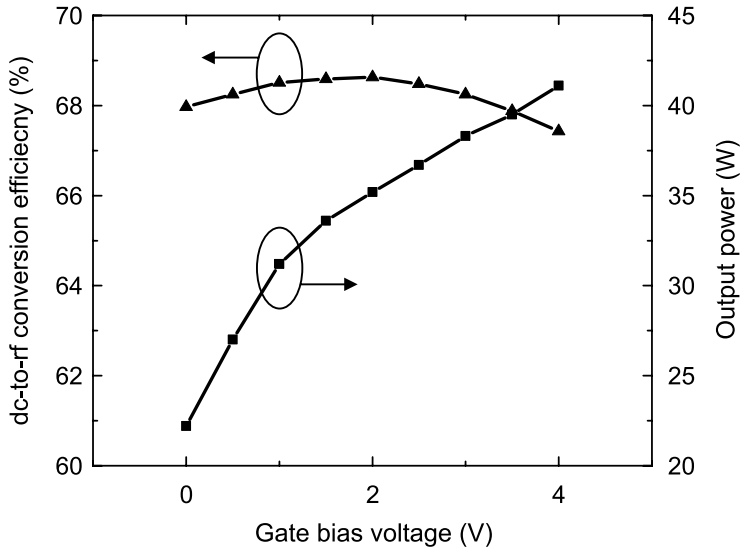


Figure 7.15: Measured output power and DC-to-rf conversion efficiency versus the gate bias voltage. The applied drain bias voltage is 23 V.

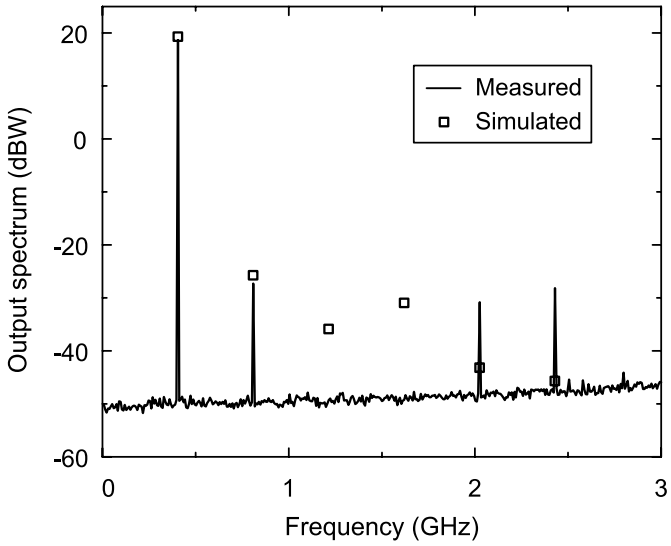


Figure 7.16: Measured and simulated output power spectrum. The largest harmonic is the second, at 46 dB below the fundamental.

Chapter 8

Suggestions for Future Investigations

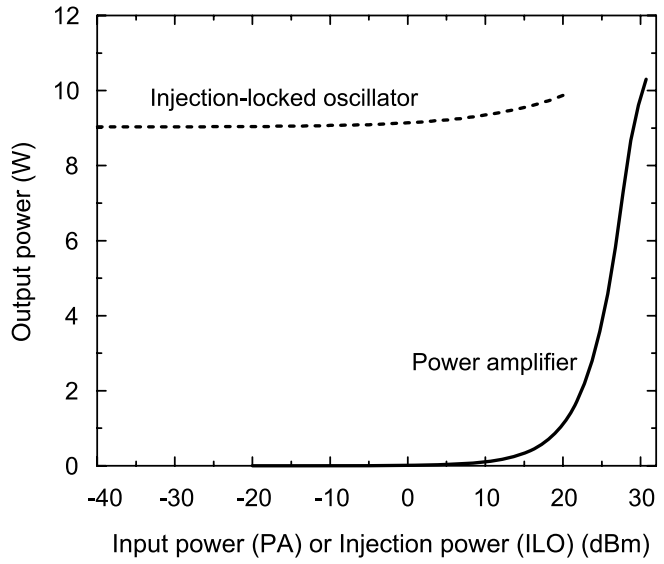
Due to ever-increasing demand for high-efficiency amplifiers in communication applications, nowadays the interest in high-performance switching-mode amplifiers rapidly grows. Suggestions can be made for the performance improvement of switching-mode power amplifiers at RF and microwave frequencies. First, special attention to the waveform shaping of input-drive signal can enhance the efficiency of power amplifiers significantly. Obviously, a sinusoid is not the optimum input drive to maximize the efficiency of switching-mode amplifiers. By imposing appropriate harmonic terminations at the input, e.g., short at the second harmonic, the input waveform can be shaped in such a way that the transistor operates as a switch more ideally. A substitution generator [90] in harmonic balance simulation can be employed to impose the appropriate harmonic components on the input waveforms as well as the output ones, required for the efficient waveform shaping. A technique for suppression of high-frequency transient ringing at the output waveform will also be worth investigating, in order to reduce loss and to improve the efficiency.

Additional progress will be achieved by employing wide-bandgap transistors such as SiC and GaN, recently released in commercial packages. These devices will make a marked impact on the switching-mode power amplifiers, which considerably extend the achievable output power level and the operating frequency limit.

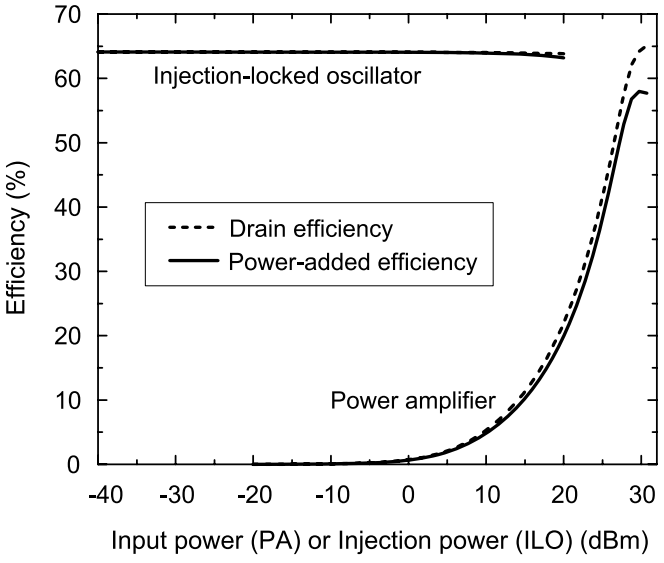
The nonlinear stability analysis techniques introduced in Chapter 4 are general-purpose and versatile. Although the techniques have been applied to predict and eliminate the instabilities exhibited in switching-mode amplifiers in Chapter 5 and Chapter 6, any type of amplifiers at any frequency are able to be analyzed by the techniques. Particularly, it will be

interesting to apply the techniques in detail to odd-mode oscillations in power-combined MMIC power amplifiers and commonly observed oscillations in Doherty amplifiers. In addition, a theoretical approach to the origin and the growing mechanism of instabilities exhibited from power amplifiers will be a good research issue. This study will be helpful to understand the instabilities more in general, so that a universal rule can be devised for the design of globally stable power amplifiers.

Finally, the stability analysis techniques can be employed to design other nonlinear circuits in addition to a free-running oscillator presented in Chapter 7. It includes frequency dividers/multipliers, injection-locked circuits, and self-oscillating mixers. As an example, an injection-locked oscillator (ILO) operated in a switching mode (Class-E) has been designed based on the auxiliary generator and pole-zero identification techniques at 1.8 GHz. This switching-mode ILO can be used as a substitute of a switching-mode amplifier, particularly in transmitter systems [91]. Since an ILO requires a very tiny injection signal to lock the power oscillation, it has substantially larger gain and larger power-added efficiency than an amplifier. Figure 8.1 shows the simulated output power and efficiency of the Class-E ILO and the comparison with those of the Class-E amplifier under the same transistor and bias conditions. It can be seen that the power-added efficiency of the ILO keeps a high value even with large input power, which is almost the same as the drain efficiency. On the other hand, the power-added efficiency of the amplifier decreases significantly from its drain efficiency (more than 7 % at the peak envelope power condition). Furthermore, even when the input power of the ILO is decreased to a very small value, the output power and efficiency keep an high value almost constantly until it loses the locking condition. These characteristics will make the ILO useful for many transmitter applications.



(a)



(b)

Figure 8.1: Comparison of simulated output power (a) and efficiency (b) between a Class-E injection-locked oscillator and a Class-E power amplifier. The transistor and bias conditions are identical between the two circuits.

Bibliography

[1] S. D. Kee, I. Aoki, A. Hajimiri, and D. B. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 51, no. 6, pp. 1677−1690, Jun. 2003.

[2] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer – a new power-combining and impedance-transformation technique," *IEEE Trans. Microwave Theory & Tech.*, vol. 50, no. 1, pp. 316−331, Jan. 2002.

[3] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[4] M. Albulet, *RF Power Amplifiers*. Atlanta, GA: Noble Publishing, 2001.

[5] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using Kahn EER technique," *IEEE Trans. Microwave Theory & Tech.*, vol. 46, no. 12, pp. 2220−2225, Dec. 1998.

[6] P. J. Baxandall, "Transistor sinewave oscillators," *Proc. IEE* (London), vol. 106, part B, suppl. 16, 748-758, May 1959.

[7] N. O. Sokal and A. D. Sokal, "Class-E: A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168−176, Jun. 1975.

[8] V. J. Tyler, "A new high-efficiency high power amplifier," *Marconi Review*, vol. 21, no. 130, pp. 96−109, Fall 1958.

[9] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163−1182, Sep. 1936.

[10] A. A. M. Saleh and D. C. Cox, "Improving the power-added efficiency of FET amplifiers operating with varying-envelope signals," *IEEE Trans. Microwave Theory & Tech.*, vol. 31, no. 1, pp. 51−55, Jan. 1983.

[11] T. Taniguchi, K. Potter, and D. Rutledge, "A 200 W power amplifier," *QEX*, pp. 3−6, Jan/Feb. 2004.

[12] P. Colantonio, F. Giannini, R. Giofrè, M. A. Yarleque Medina, D. Schreurs, and B. Nauwelaers, "High frequency class E design methodologies," *European Microwave Week – 13th GaAs Symposium*, Paris, France, Oct. 2005, pp. 329−332.

[13] M. M. El-Desouki, M. J. Deen, and Y. M. Haddara, "A low-power CMOS class-E power amplifier for biotelemetry applications," *European Microwave Week – 35th European Microwave Conference*, Paris, France, Oct. 2005, pp. 441−444.

[14] L. R. Kahn, "Single sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, pp. 803−806, Jul. 1952.

[15] F. H. Raab and D. J. Ruff, "High-efficiency single-sideband HF/VHF transmitter based upon envelope elimination and restoration," *Proc. Sixth International Conference HF Radio Systems and Techniques*, York, UK, Jul. 4−7, 1994, pp. 21−25.

[16] N. Wang, X. Peng, V. Yousefzadeh, D. Maksimovic, S. Pajic, and Z. Popovic, "Linearity of X-band class-E power amplifiers in EER operation," *IEEE Trans. Microwave Theory & Tech.*, vol. 53, no. 3, pp. 1092−1102, Mar. 2005.

[17] H. Chireix, "High power outphasing modulation," *Proc. IRE*, vol. 23, no. 11, pp. 1370−1392, Nov. 1935.

[18] G. M. Hegazi, T. T. Chu, and R. A. Groshong, "Improved LINC power transmission using a quadrature outphasing technique," *2005 IEEE MTT-S Int. Microwave Symp. Dig.*, Long Beach, CA, Jun. 2005, pp. 1923−1926.

[19] R. Langridge, T. Thornton, P. M. Asbeck, and L. E. Larson, "A power re-use technique for improving efficiency of outphasing microwave power amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 47, no. 8, pp. 1467−1470, Aug. 1999.

[20] Advanced Power Technology, Inc., Bend, OR, website: www.advancedpower.com.

[21] M. Kazimierczuk and K. Puczko, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle," *IEEE Trans. Circuits and Systems*, vol. 34, no. 2, pp. 149−159, Feb. 1987.

[22] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, New York: John Wiley & Sons, 1980.

[23] F. Raab, "Idealized operation of the Class E tuned power amplifier," *IEEE Trans. Circuits & Systems*, vol. 24, no. 12, pp. 725−735, Dec. 1977.

[24] S. Li, "UHF and X-band class-E amplifiers," *Ph.D. Thesis*, California Institute of Technology, Pasadena, CA, 1999.

[25] T.-P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, "Design of high-efficiency current-mode class-D amplifiers for wireless handsets," *IEEE Trans. Microwave Theory & Tech.*, vol. 53, no. 1, pp. 144−151, Jan. 2005.

[26] F. Bohn, S. Kee, and A. Hajimiri, "Demonstration of a switchless class E/F_{odd} dual-band power amplifier," *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, Jun. 2002, pp. 1631−1634.

[27] A. Grebennikov, "Simple design equations for broadband class E power amplifiers with reactance compensation," *2001 IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 2143−2146.

[28] V. S. R. Gudimetla and A. Z. Kain, "Design and validation of the load networks for broadband class E amplifiers using nonlinear device models," *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, Anaheim, CA, Jun. 1999, pp. 823−826.

[29] S. Jeon and D. B. Rutledge, "A 2.7-kW, 29-MHz class-E/F_{odd} amplifier with a distributed active transformer," *2005 IEEE MTT-S Int. Microwave Symp. Dig.*, Long Beach, CA, Jun. 2005, pp. 1927−1930.

[30] T. B. Mader and Z. Popovic, "The transmission-line high-efficiency class-E amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 5, no. 9, pp. 290−292, Sep. 1995.

[31] F. Lepine, A. Adahl, and H. Zirath, "L-band LDMOS power amplifiers based on an inverse class-F architecture," *IEEE Trans. Microwave Theory & Tech.*, vol. 53, no. 6, pp. 2007−2012, Jun. 2005.

[32] A. Adahl and H. Zirath, "An 1 GHz Class E LDMOS power amplifier," *European Microwave Week – 33rd European Microwave Conference*, Munich, Germany, Oct. 2003, pp. 285−288.

[33] S. Kee, "The Class E/F family of harmonic-tuned switching power amplifiers," *Ph.D. Thesis*, California Institute of Technology, Pasadena, CA, 2001.

[34] F. Wang and D. B. Rutledge, "A 60-W L-band Class-E/$F_{odd,2}$ LDMOS power amplifier using compact multilayered baluns," *IEEE Topical Workshop on Power Amplifiers for Wireless Communications, Tech. Dig.*, San Diego, CA, Sep. 2004.

[35] E. Lau, K.-W. Chiu, J. Qin, J. Davis, K. Potter, and D. Rutledge, "High-efficiency class-E power amplifiers – Part 1," *QST*, pp. 39−42, May 1997.

[36] A. Anakabe, J. M. Collantes, J. Portilla, J. Jugo, S. Mons, A. Mallet, and L. Lapierre, "Analysis of odd-mode parametric oscillations in HBT multi-stage power amplifiers," *European Microwave Week – 11th GaAs Symposium*, Munich, Germany, October 2003, pp. 533−536.

[37] S. H. Strogatz, *Nonlinear Dynamics and Chaos*, Cambridge, MA: Westview Press, 1994.

[38] A. Suárez and R. Queré, *Stability Analysis of Nonlinear Microwave Circuits*, Boston, MA: Artech House, 2003.

[39] C. P. Silva, "Chaotic oscillators and their applications to communications," *European Microwave Week – 35th European Microwave Conference*, *WSEuMC03 Workshop Dig.*, Paris, France, Oct. 2005.

[40] C. Jeffries and K. Wiesenfeld, "Observation of noisy precursors of dynamical instabilities," *Physical Review A*, vol. 31, no. 2, pp. 1077−1084, Feb. 1985.

[41] F. H. Raab, R. Caverly, R. Campbell, M. Eron, J. B. Hecht, A. Mediano, D. P. Myer, and J. L. B. Walker, "HF, VHF, and UHF systems and technology," *IEEE Trans. Microwave Theory & Tech*., vol. 50, no. 3, pp. 888−899, Mar. 2002.

[42] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovich, N. Pothecary, J. F. Sevic, and N. O. Sokal, "RF and microwave power amplifier and transmitter technologies – part 2," *High Frequency Electronics*, May 2003.

[43] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, " Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371−383, Mar. 2002.

[44] S. D. Kee, I. Aoki, and D. B. Rutledge, "7-MHz, 1.1-kW demonstration of the new $E/F_{2,odd}$ switching amplifier class," *2001 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1505-1508, May 2001.

[45] Advanced Power Technology VDMOS Data Sheet for ARF473, Advanced Power Technology Inc. http://www.advancedpower.com.

[46] J. F. Davis and D. B. Rutledge, "A low-cost class-E power amplifier with sine-wave drive," *1998 IEEE MTT-S Int. Microwave Symp. Dig*., vol. 2, pp. 1113−1116, Jun. 1998.

[47] Sonnet Suites Release 8: Sonnet, Syracuse, NY.

[48] R. E. Collin, *Foundations for Microwave Engineering*, 2nd Edition, New York, NY: IEEE Press, 2001.

[49] D. M. Pozar, *Microwave Engineering*, 2nd Edition, New York, NY: John Wiley & Sons, 1998.

[50] J. Jugo, J. Portilla, A. Anakabe, A. Suárez, and J. M. Collantes, "Closed-loop stability analysis of microwave amplifiers," *IEE Electronics Letters*, vol. 37, pp. 226−228, Feb. 2001.

[51] S. A. Maas, *Nonlinear Microwave Circuits*, Norwood, MA: Artech House, 1988.

[52] J. Jugo, A. Anakabe, and J. M. Collantes, "Control design in the harmonic domain for microwave and RF circuits," *IEE Proc. Control Theory and Applications*, vol. 150, no. 2, pp. 127−131, Mar. 2003.

[53] STAN (STability ANalysis), developed in Prof. Collantes' group at University of the Basque Country, Bilbao, Spain.

[54] J. M. Collantes, I. Lizarraga, A. Anakabe, and J. Jugo, "Stability verification of microwave circuits through floquet multiplier analysis," *2004 IEEE Asia-Pacific Conference on Circuits and Systems*, Tainan, Taiwan, Dec. 2004, pp. 997−1000.

[55] L. O. Chua, "A switching-parameter algorithm for finding multiple solutions of nonlinear resistive circuits," *International Journal of Circuit Theory and Applications*, vol. 4, no. 3, pp. 215-239, Jul. 1976.

[56] J. Vidkjaer, "Instabilities in RF-power amplifiers caused by a self-oscillation in the transistor bias network," *IEEE J. Solid-State Circuits*, vol. 11, no. 5, pp. 703−712, Oct. 1976.

[57] A. Anakabe, J. M. Collantes, J. Portilla, J. Jugo, S. Mons, A. Mallet, and L. Lapierre, "Analysis of odd-mode parametric oscillations in HBT multi-stage power amplifiers,"

European Microwave Week – 11th GAAS Symposium, Munich, October 2003, pp. 533−536.

[58] A. Collado, F. Ramírez, and A. Suárez, "Analysis and stabilization tools for microwave amplifiers," *2004 IEEE MTT-S Int. Microwave Symp. Dig.*, Fort Worth, TX, Jun. 2004, pp. 945−948.

[59] S. Mons, J.-C. Nallatamby, R. Queré, P. Savary, and J. Obregon, "A unified approach for the linear and nonlinear stability analysis of microwave circuits using commercially available tools," *IEEE Trans. Microwave Theory & Tech.*, vol. 47, no. 12, pp. 2403−2409, Dec. 1999.

[60] J. M. T. Thompson and H. B. Stewart, *Nonlinear Dynamics and Chaos*, John Wiley & Sons, 1986.

[61] D. Teeter, A. Platzker, and R. Bourque, "A compact network for eliminating parametric oscillations in high power MMIC amplifiers," *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, Anaheim, CA, Jun. 1999, pp. 967−970.

[62] M. Mochizuki, M. Nakayama, Y. Tarui, Y. Itoh, S. Tsuji, and T. Takagi, "Nonlinear analysis of $f_o/2$ loop oscillation of high power amplifiers," *1995 IEEE MTT-S Int. Microwave Symp. Dig.*, Orlando, FL, May 1995, pp. 709−712.

[63] *Spice model for TMOS power MOSFETs*, Application note, AN1043, Motorola Semiconductor Products Inc., Phoenix, AZ, 1989.

[64] Y.-S. Kim and J. G. Fossum, "Physical DMOST modeling for high-voltage IC CAD," *IEEE Trans. Electron Devices,* vol. 37, no. 3, pp. 797−803, Mar. 1990.

[65] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *Bell Syst. Tech. J.*, vol. 48, pp. 1937−1955, Jul.-Aug. 1969.

[66] J. Guckenheimer and P. Holmes, *Nonlinear Oscillations, Dynamical Systems and Bifurcations of Vector Fields*, Third printing, Springer-Verlag, 1990.

[67] E. Ngoya and R. Larcheveque, "Envelope transient analysis: a new method for the transient and steady state analysis of microwave communication circuits and systems," *1996 IEEE MTT-S Int. Microwave Symp. Dig.*, San Francisco, CA, Jun. 1996, pp. 1365−1368.

[68] J. C. Pedro and N. B. Carvalho, "Simulation of RF circuits driven by modulated signals without bandwidth constraints," *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, Jun. 2002, pp. 2173−2176.

[69] E. de Cos, A. Suárez, and S. Sancho, "Envelope transient analysis of self-oscillating mixers," *IEEE Trans. Microwave Theory & Tech.,* vol. 52, no. 4, pp. 1090−1100, Apr. 2004.

[70] S. Jeon, A. Suárez, and D. B. Rutledge, "Global stability analysis and stabilization of a Class-E/F amplifier," *IEEE Trans. Microwave Theory & Tech.,* vol. 53, no. 12, pp. 3712−3722, Dec. 2005.

[71] S. Ver Hoeye, A. Suárez, and S. Sancho, "Analysis of Noise Effects on the Nonlinear Dynamics of Synchronized Oscillators," *IEEE Microwave and Wireless Components Letters*, vol. 11, no. 9, pp. 376−378, Sep. 2001.

[72] V. Rizzoli and A. Neri, "State of the art and present trends in nonlinear microwave CAD techniques," *IEEE Trans. Microwave Theory & Tech.*, vol. 36, no.12, pp. 343−365, Feb. 1988.

[73] V. Rizzoli, F. Mastri, and D. Masotti, "General noise analysis of nonlinear microwave circuits by the piecewise harmonic-balance technique," *IEEE Trans. Microwave Theory & Tech.*, vol. 42, no. 5, pp. 807−819, May 1994.

[74] M. M. Green and R. C. Melville, "Sufficient conditions for finding multiple operating points of DC circuits using continuation methods," *1995 IEEE Int. Symp. Circuits and Syst., ISCAS '95*, May 1995, pp. 117−120.

[75] V. Iglesias, A. Suárez, and J. L. García, "New technique for the determination through commercial software of the stable-operation parameter ranges in nonlinear microwave circuits," *IEEE Microwave and Guided Wave Letters,* vol. 8, no. 12, pp. 424−426, Dec. 1998.

[76] F. Ramirez, M.E. de Cos, and A. Suárez, "Nonlinear analysis tools for the optimized design of harmonic-injection dividers," *IEEE Trans. Microwave Theory & Tech.*, vol. 51, no. 6, pp. 1752−1762, Jun. 2003.

[77] F. X. Kaertner, "Analysis of white and f^{α} noise in oscillators," *International Journal of Circuit Theory and Applications*, vol. 18, 1990, pp. 485−519.

[78] V. A. Godyak, "Radio frequency light sources," *IEEE Industry Applications Conference*, Oct. 8−12, 2000, vol. 5, pp. 3281−3288.

[79] J. Ebert and M. Kazimierczuk, "Class E high-efficiency tuned power oscillator," *IEEE J. Solid-State Circuits*, vol. 16, no. 2, pp. 62−66, Apr. 1981.

[80] D. V. Chernov, M. K. Kazimierczuk, and V. G. Krizhanovski, "Class-E MOSFET low-voltage power oscillator," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, Phoenix, AZ, May 2002, pp. 509−512.

[81] E. W. Bryerton, W. A. Shiroma, and Z. B. Popovic, "A 5-GHz high-efficiency Class-E oscillator," *IEEE Microwave Guided Wave Lett.*, vol. 6, no. 12, pp. 441−443, Dec. 1996.

[82] M. Prigent, M. Camiade, G. Pataut, D. Reffet, J. M. Nebus, and J. Obregon, "High efficiency free running Class F oscillator," *1995 IEEE MTT-S Int. Microwave Symp. Dig.*, Orlando, FL, May 1995, pp. 1317−1320.

[83] A. Gitsevich, D. Kirkpatrick, and L. Dymond, Jr., "Solid-state high power RF oscillator," *2001 IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 1423−1426.

[84] M.-Q. Lee, S.-J. Yi, S. Nam, Y. Kwon, and K.-W. Yeom, "High-efficiency harmonic loaded oscillator with low bias using a nonlinear design approach," *IEEE Trans. Microwave Theory & Tech.*, vol. 47, no. 9, pp. 1670−1679, Sep. 1999.

[85] S. V. Hoeye, F. Ramirez, A. Suarez, "Nonlinear optimization tools for the design of high-efficiency microwave oscillators," *IEEE Microwave Wireless Components Lett.*, vol. 14, no. 5, pp. 189−191, May 2004.

[86] K. L. Kotzebue, "A technique for the design of microwave transistor oscillators," *IEEE Trans. Microwave Theory & Tech.*, vol. 32, no. 7, pp. 719−721, Jul. 1984.

[87] Y. Xuan and C. M. Snowden, "A generalized approach to the design of microwave oscillators," *IEEE Trans. Microwave Theory & Tech.*, vol. 35, no. 12, pp. 1340−1347, Dec. 1987.

[88] *Freescale Semiconductor LDMOS Data Sheet* for MRF183, Freescale Semiconductor, Inc., http://www.freescale.com

[89] M. Matsuo, H. Sekiya, T. Suetsugu, K. Shinoda, and S. Mori, "Design of a high-efficiency class DE tuned power oscillator," *IEEE Trans. Circuits & Systems*, vol. 47, no. 11, pp. 1645−1649, Nov. 2000.

[90] D. Barataud, M. Campovecchio, and J. M. Nebus, "Optimum design of very high efficiency microwave power amplifiers based on time-domain harmonic load-pull measurements," *IEEE Trans. Microwave Theory & Tech.*, vol. 49, no. 6, pp. 943−950, Jun. 2001.

[91] Y.-S. Jeon, H.-S. Yang, and S. Nam, "A novel high-efficiency linear transmitter using injection-locked pulsed oscillator," *IEEE Microwave Wireless Components Lett.*, vol. 15, no. 4, pp. 214−216, Apr. 2005.