Incomplete Charge Transfer in Overlapping Gates Charge Coupled Devices

Thesis by

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ABSTRACT

We have developed a numerical simulation of the charge transfer in the overlapping gates charge coupled devices. The transport dynamics were analyzed in terms of thermal diffusion, self-induced fields and fringing fields under all the relevant electrodes and the interelectrode regions with time varying gate potentials. We have also developed a lumped circuit model of charge coupled devices. Using this model simple analytic expressions describing the charge transfer with various clocking waveforms are derived. This model can be used to study the charge transfer characteristics for other device structures, dimensions, clocking waveforms and voltages, thus providing practical charge coupled device and circuit design tools.

Using the numerical simulation and lumped circuit model, the influence of clocking waveforms and clocking schemes on CCD operation are studied. It is concluded that increasing the clocking scheme complexity allows a better control of the storage and transfer of the signal charge and hence improves the signal dynamic range and charge transfer characteristics. It is shown that the performance of charge coupled devices is better with push clocks (that push the charge from one storage site to another) than with drop clocks (that create deeper potential wells to transfer the charge). The performance of charge coupled devices is shown to be basically superior to the MOS bucket brigade.

We have also developed a simple model to study the incomplete charge transfer due to trapping in the interface states. Incomplete

charge transfer due to trapping in interface states is shown to limit the performance of CCDs at low frequencies. The most dominant effect is trapping in the interface states under the edges of the gates parallel to the active channel. The influence of the device parameters, dimensions and clocking waveforms on the signal degradation is discussed. Design features of CCD structures which would reduce the incomplete charge transfer due to interface states are presented. It is shown that increasing the clock voltages, increasing the signal charge or using dynamic push clock reduces the incomplete charge transfer due to interface states.

The contents of this thesis have been published under the following titles:

"Charge Transfer in Overlapping Gates Charge Coupled Devices" A. M. Mohsen, T. C. McGill and C. A. Mead, Journal of Solid State Circuits, SC-8, No. 3, June 1973.

"The Influence of Interface States on Incomplete Charge Transfer in Overlapping Gates Charge Coupled Devices", A. M. Mohsen, T. C. McGill, Y. Daimon and C. A. Mead, Journal of Solid State Circuits, SC-8, No. 2, April 1973.

"Push Clocks: A new approach to charge coupled device clocking", A. M. Mohsen, T. C. McGill, M. Anthony and C. A. Mead, Appl. Phys. Letters, 22, 4, February 15, 1973, pp. 172-175.

"Charge Transfer in Charge Coupled Devices", A. M. Mohsen, T. C. McGill and C. A. Mead, ISSCC Digest of Technical Papers 15, 1972, pp. 248-249.

The contents of this thesis have also been presented in the following conferences:

"Physics of Charge Coupled Devices", Invited Review Talk given at the Gordon Research Conference, Meriden, New Hampshire, August 1972.

"The Influence of Clocking Waveforms on CCD Operation", presented at the International Device Research Conference at Edmonton, Canada, June 1972.

"Charge Transfer in Charge Coupled Devices", presented at the International Solid State Circuits Conference, Philadelphia, Pa., February 1972.

A motion picture simulation of the various stages of the charge transfer process with two-phase and four-phase clocking schemes was produced directly from the results of the numerical simulation developed in this thesis. The CCD movie has been presented in the conferences mentioned above and is included in the "Semiconductor Memory Course" prepared by Texas Instruments on video tapes. The CCD movie is published in the Journal of Solid State Circuits (June 1973) as three sequences of page-flip movie.

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Chapter 1

INTRODUCTION

The idea of making a shift register for analog signals and using it as a delay line dates back to the beginning of the fifties.[1] Sampled values of the analog signal can be stored in the form of charges on a series of capacitors. The transfer of charge between these storage capacitors can be controlled by switches driven by clock pulses. By analogy with the old fire-fighting method, in which buckets of water are passed along the line, circuits of this type were called "bucket brigade delay lines". However, these delay lines have not come into general use because of the inevitable complexity and bulk of the switches. In 1969, Sangster[2] proposed an integrated circuit version of the bucket brigade delay line with the advantages of low cost, high packing density and compatibility with the existing semiconductor technology. Figure (1) shows a two-phase MOS bucket brigade. Each stage consists of a MOS transistor and a storage capacitor. The signal charge is stored in the p-diffusion islands and the transfer of charge is controlled by the clock pulses, ϕ_1 and ϕ_2.

In 1970, Boyle and Smith[3] showed that the signal charge packets could be stored and transferred in potential wells at the semiconductor-insulator interface under electrodes without using p-diffusion islands as in the MOS bucket brigade. For efficient coupling of the potential wells at the interface the electrodes should be closely spaced. The resulting structure is commonly known as the charge coupled device and

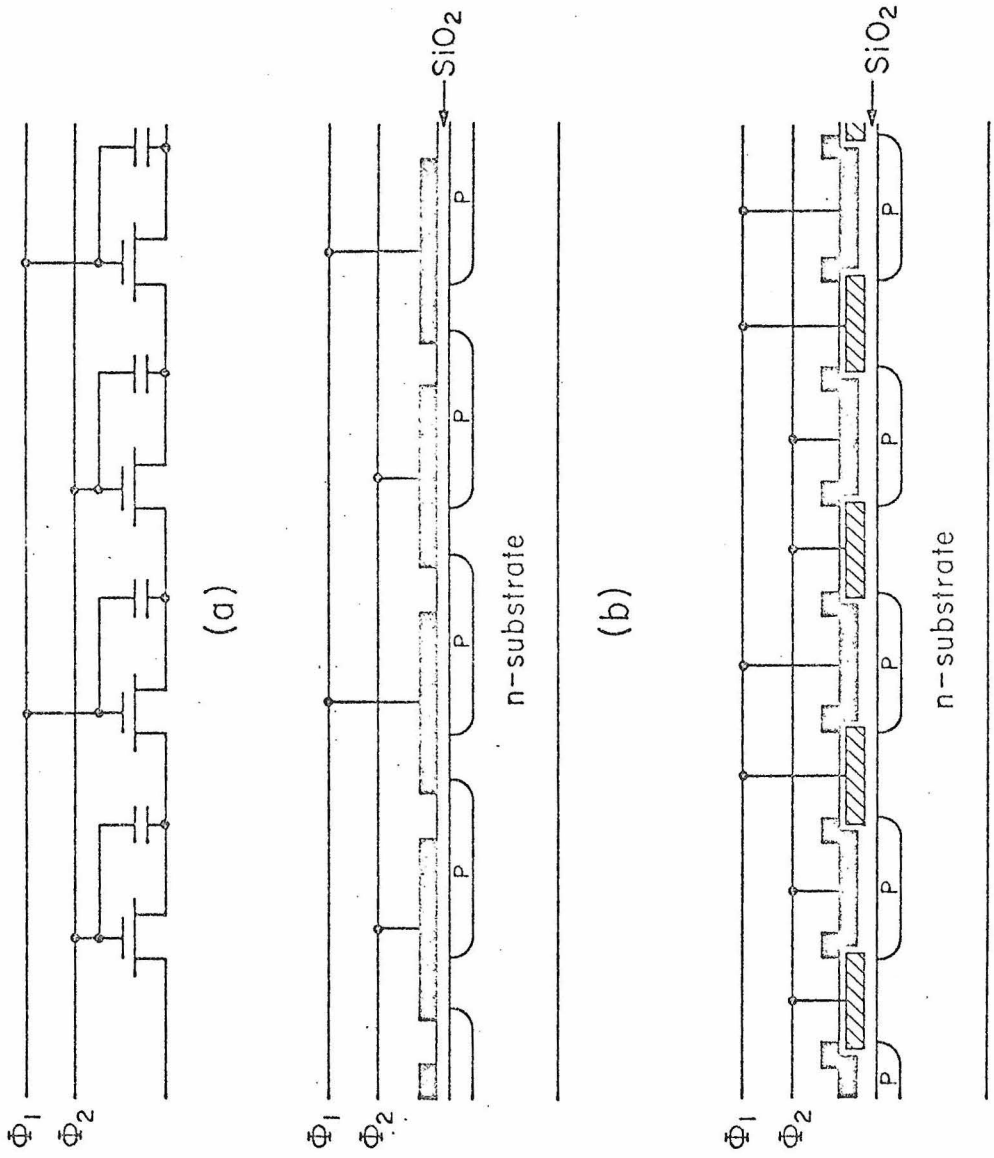
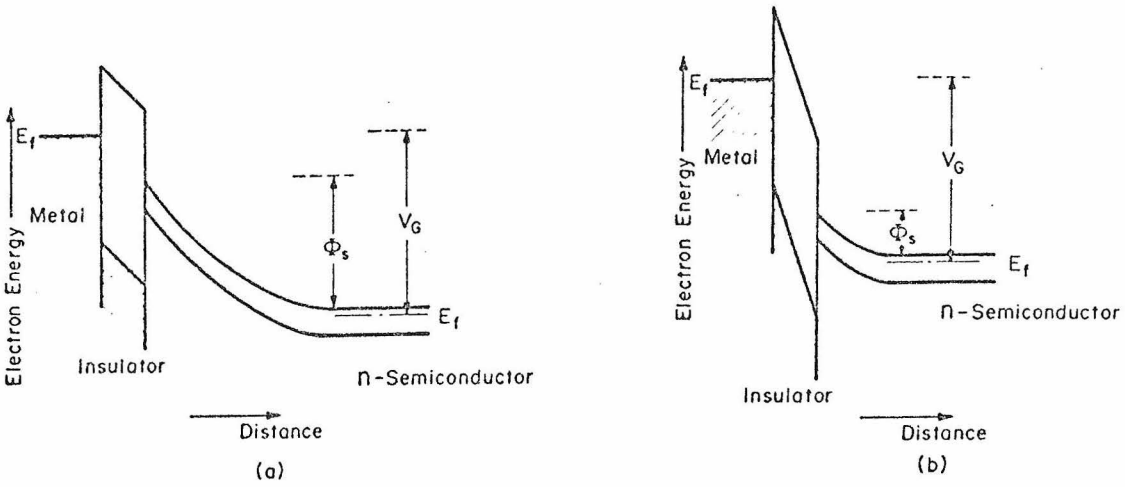


Figure 1.

is shown in Fig. (2c). In Fig. (2a) and (2b) the band diagram of a metal-insulator-n semiconductor is shown to illustrate the creation of potential wells at the interface when a voltage pulse is applied to the metal electrode. Minority carriers injected in reponse to a digital or analog signal or generated by photons could be stored as charge packets in these potential wells resulting in a decrease in depth of the potential well. The storage and transfer of the charge packets are controlled by the clocking pulses driving the closely spaced electrodes as shown in Fig. (2c,d,e) where a three phase clocking scheme is used.

So charge coupled devices (CCDs) are a new class of semiconductor structure operating in nonequilibrium. In essence CCDs are analog, dynamic, passive shift register that permits the design of complex functional devices. Currently there is a great interest in these devices as they have important applications for digital memories, self-scanned imagers and analog signal processing. In order to design and properly operate charge coupled devices with optimum performance an understanding of the physical limitations on the performance of these devices is essential.

From the operation of charge coupled devices, it is clear that the main limitations on the performance of these devices are due to the incomplete transfer of the signal charge; trapping of the signal charge in the interface states; thermal generation currents from the generation centers at the interface, the depletion regions, and the substrate and the noise generated during the storage and transfer of the signal charge along the interface.


Electron Energy
E_f
Metal
Insulator
Φ_s
V_G
E_f
n-Semiconductor
Distance
(a)
Electron Energy
E_f
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n-Semiconductor
Insulator
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(b)

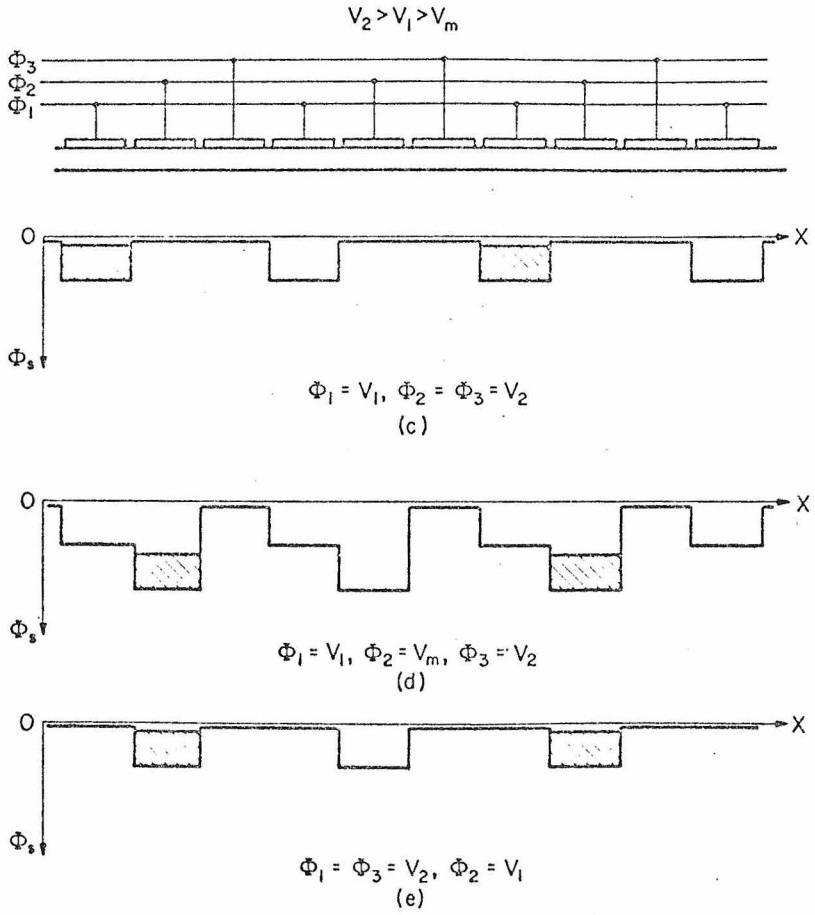
$V_2 > V_1 > V_m$
Φ_3
Φ_2
Φ_1
0
X
Φ_s
$\Phi_1 = V_1$, $\Phi_2 = \Phi_3 = V_2$
(c)
0
X
Φ_s
$\Phi_1 = V_1$, $\Phi_2 = V_m$, $\Phi_3 = V_2$
(d)
0
X
Φ_s
$\Phi_1 = \Phi_3 = V_2$, $\Phi_2 = V_1$
(e)

Figure 2.

In this thesis, we present a detailed study of the limitations on the performance of charge coupled devices due to incomplete free charge transfer and trapping in the interface states and their dependence on the device parameters and clocking waveforms. In our work we have considered the overlapping gate structure (shown in Fig. (3)) as it is presently the most technically promising structure for the large scale application of the devices. Compared to the simplicity of the three-phase metal gate CCD[3,4] and the resistive gate CCD[5], the inter-electrode spacing in the overlapping gate structure is reduced to an oxide thickness and the overlapping electrodes provide good control of the surface potential in the entire channel region, seal the active channel from any external contaminations, shield out the charge repulsion,[1] and thus enhance the charge transfer. Overlapped gate CCDs can be easily manufactured with two levels of metalization technology such as silicon gate and refractory gate technology.[6,7] The two levels of metalization also simplifies the layout of large CCD arrays.

We have developed a detailed numerical simulation of the charge transfer process in the overlapping gate charge coupled devices. With some assumptions and approximations, which are shown to be well satisfied, we have solved the nonlinear nonlocal equations describing the transfer dynamics, under all the relevant gate electrodes and interelectrode regions with time varying gate potentials using a new finite difference scheme, the Box scheme.[8] We have developed a simple lumped circuit model of charge coupled devices. This model can

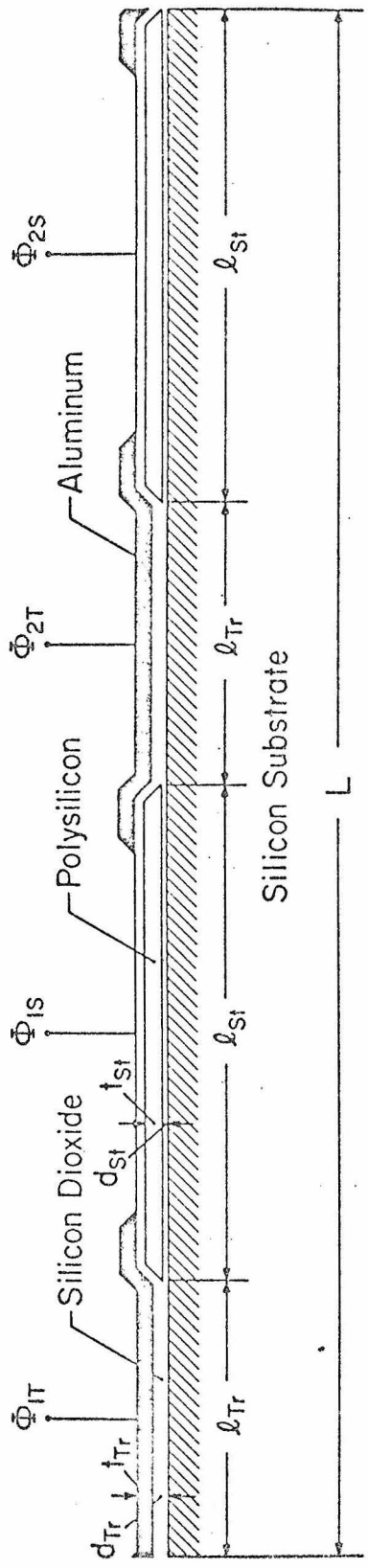
Φ_{2S}
Φ_{2T}
Φ_{1S}
Φ_{1T}
Aluminum
Polysilicon
Silicon Dioxide
Silicon Substrate
t_{St}
d_{St}
t_{Tr}
d_{Tr}
ℓ_{St}
ℓ_{Tr}
L

Figure 3.

be used to study the charge transfer characteristics for other device structures, dimensions, clocking waveforms, and voltages, thus providing practical charge coupled device and circuit design tools. Using the numerical simulation and the lumped circuit model we have studied the influence of clocking waveforms and clocking schemes on the performance of charge coupled devices and we present a fundamental comparison of the performance of bucket brigade and charge coupled devices. Finally, we have developed a simple model to study the influence of trapping in the interface states on the incomplete charge transfer and present design features of CCD structures to reduce it.

Chapter 2

THEORETICAL MODEL

In this chapter we present the equations that describe the storage and transfer of charge in charge coupled devices. We also discuss the assumptions and approximations that we have used to reduce the nonlinear-nonlocal transport equations to nonlinear diffusion equations.

In the calculations presented below we have considered p-channel[2] devices with dimensions consistent with typical layout tolerances of silicon gate technology. One unit cell of the overlapping gate structure using silicon gate technology is shown in Fig. (3).

2.1 Transport Equations

The storage and transfer of charge along the insulator-semiconductor interface is described by the continuity equation:

$$\frac{\partial q}{\partial t} = \frac{-\partial}{\partial x} J_x - \left.\frac{\partial q}{\partial t}\right|_{\text{Trapping}} + \left.\frac{\partial q}{\partial t}\right|_{\text{Th. Generation}} , \qquad (1)$$

where

$$J_x = -D \frac{\partial q}{\partial x} - \mu q \frac{\partial \phi_s}{\partial x} . \qquad (2)$$

q is the surface charge density of the free minority carrier, J_x is the sheet current density, and ϕ_s is the surface potential. D and μ are the minority carrier diffusion and mobility at the interface respectively. x is the distance along the interface in the direction

of charge transfer. $\left.\frac{\partial q}{\partial t}\right|_{\text{Th. Generation}}$ is the rate of generation of surface charge due to thermal generation currents from generation centers at the interface, the depletion regions and the substrate. For a total delay time from the input to the output of the device much smaller than the storage time of the interface, the effect of thermal generation can be neglected.[3] $\left.\frac{\partial q}{\partial t}\right|_{\text{Trapping}}$ is the total rate of capture of the mobile carriers due to their interaction with the interface states in the band gap. Since the mobile carriers interact with interface states within an energy range of the order of thermal voltage and for the low interface state density obtainable with the present thermally grown silicon oxide, the rate of capture or emission of the mobile carriers by the interface states is smaller than the divergence of the sheet current density in Eq. (1). Thus one can obtain the free charge transfer characteristics by neglecting $\left.\frac{\partial q}{\partial t}\right|_{\text{Trapping}}$ in Eq. (1) and solving the continuity equation. The effects of trapping on the incomplete charge transfer can then be calculated by studying the interaction of the mobile carriers with the interface states from the Shockley-Read-Hall equations together with the surface charge density profiles $q(x,t)$ under the gates. Thus the free charge transfer continuity equation reduces to

$$\frac{\partial q}{\partial t} = \frac{\partial}{\partial x}\left[D\,\frac{\partial q}{\partial x} + \mu q\,\frac{\partial \Phi_s}{\partial x}\right] \quad . \qquad (3)$$

The surface potential gradient $\frac{\partial \Phi_s}{\partial x}$ is due to the variable

surface charge density and the two-dimensional nature of the CCD structure. For given electrode potentials, device geometry, and charge density profile, the surface potential gradient is obtained from the solution of the two-dimensional Poisson equation. Thus a rigorous treatment of the free charge transfer problem would require the simultaneous solution of Eq. (3) and the two-dimensional Poisson equation. While this rigorous approach is conceptually possible, the cost of such an analysis leads us to seek some valid approximation to simplify the solution.

2.2 Approximations

The surface potential gradient due to variations in the surface charge density (self-induced fields) can be obtained, according to the standard gradual channel approximation.[9] In this approximation, we take the gradient of the surface potential Φ_s obtained from the one-dimensional solution of the Poisson equation with the parameters of the solutions chosen to correspond to the one-dimensional cut through the structure. In Appendix I, we show, using a Green's function solution of the two-dimensional Poisson equation for an arbitrary minority charge density profile, that the gradual channel approximation is reasonably accurate when the lateral variation of the various charges over a distance on the order of the depletion layer width is small.

The surface potential gradient under the electrodes due to the adjacent electrodes (fringing fields) are obtained by solving the two-dimensional Poisson equation of the CCD structure. In Fig. (4) we have plotted the surface potential and surface potential gradient

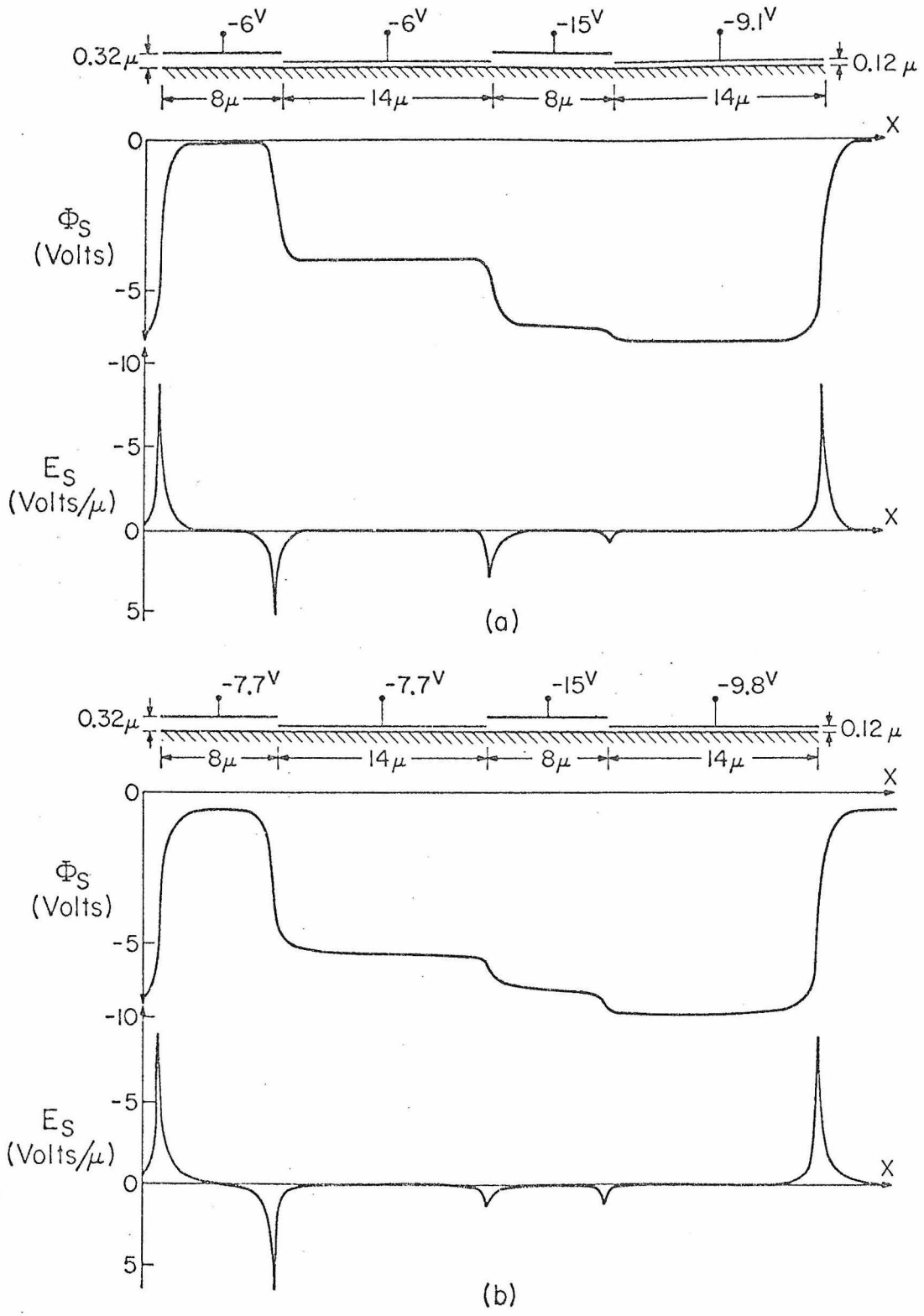
-6V
-6V
-15V
-9.1V
0.32μ
0.12 μ
8μ
14μ
8μ
14μ
X
0
ΦS
(Volts)
-5
-10
-5
ES
(Volts/μ)
0
X
5
(a)
-7.7V
-7.7V
-15V
-9.8V
0.32μ
0.12 μ
8μ
14μ
8μ
14μ
X
0
ΦS
(Volts)
-5
-10
-5
ES
(Volts/μ)
0
X
5
(b)

Figure 4.

along the semiconductor insulator interface. These plots were obtained from the solution of the two-dimensional Poisson equation[10] of an overlapping gate CCD with the electode voltages corresponding to the last stages of the charge transfer and with most of the signal charge in the receiving storage electrode. The fringing fields in devices with dimensions consistent with typical layout tolerances of MOS technology are of the order of a few hundreds volts/cm. During the first stages of the charge transfer process the self-induced fields are typically few thousands volts/cm, therefore, the fringing fields are only important at the last stages of the charge transfer when the self-induced fields become very small. Accordingly the fringing field profile under the electrodes obtained from a two-dimensional solution of the Poisson equation of the CCD structure with the gate voltages corresponding to the last stages of the charge transfer and with most of the signal charge in the receiving electrode can be used during the entire charge transfer process.

The two-dimensional solution of the Poisson equation for the overlapping gate structure shown in Fig. (4) illustrates that the surface potential under the interelectrode regions varies quite smoothly for different gate electrode potentials. Therefore we have used a smooth interpolating polynomial to approximate the surface potential in these regions. We have also assumed a constant surface mobility to simplify the transport equations. The dependence of the surface mobility on the normal surface field and the surface potential gradient along the interface introduce negligibly small

error on the charge transfer characteristics of typical minimum geometry devices.[4]

2.3 Nonlinear Diffusion Equation

In Appendix II, we show that according to the above assumptions the surface potential gradient under the gates or in the inter-electrode regions can be written in the form

$$\frac{\partial \Phi_s}{\partial x} = L(x,t) + M(x,t)\, q + N(x,t)\, \frac{\partial q}{\partial x} \quad . \qquad (4)$$

Substituting in Eqs. (3), the continuity equation reduces to the non-linear diffusion equation:

$$\frac{\partial q}{\partial t} = \frac{\partial}{\partial x}\left[D\, \frac{\partial q}{\partial x} + \mu q\left(L + Mq + N\, \frac{\partial q}{\partial x} \right) \right] \quad . \qquad (5)$$

If fringing fields under the gate electrodes are negligible then $L = M = 0$.

The dynamics of the charge transport in each bit is thus described by equations similar to Eq. (5) with the appropriate functions, L, M, and N under the storage and transfer electrodes and the interelectrode regions. At the junction points between the different regions, the surface potential and surface charge density must be continuous and the current must be conserved.

We have solved the set of nonlinear equations with the appropriate boundary conditions using a new finite difference scheme, the Box scheme.[8] The numerical formulation of the problem[5] and its accuracy is treated in detail in Appendix III.

Chapter 3

FREE CHARGE TRANSFER

We have shown in Chapter 2 that the charge transfer dynamics in each bit of the charge coupled device can be described by a nonlinear diffusion equation. In this chapter we will present the results of the numerical solutions of these nonlinear equations when the device is operated with different clocking schemes and waveforms. A comparison of the charge transfer characteristics obtained from the lumped circuit model of the device developed in Appendix IV and V with the numerical results is also presented.

3.1 Push and Drop Clocks

The closely spaced electrodes of the charge coupled device can be driven by clocking pulses that may have various shapes and waveforms to control the storage and transfer of the charge along the interface. In general clocking pulse waveforms could be classified into two basically different types: drop clocks and push clocks. With drop clock the signal charge is stored below a gate at a holding voltage V_1 which is a fraction of the largest clock voltage V_m that the MOS structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates, and the charge flows to the potential minimum thus created. With push clocks the charge is stored under a gate held at V_m, and transferred to a nearby gate, also at V_m, by raising the potential of the gate where the charge has been residing and thus "pushing" the charge to the next gate. Charge coupled devices

can be operated with two-phase, three-phase, or four-phase clocking schemes by push clocks, drop clocks, or a combination of push and drop clocks. With three-phase and four-phase clocking schemes the electrodes of the overlapping gate structure are equal in size so that charge may be stored under each gate during the transfer process. Alternatively the upper electrodes may be made smaller and used to control the transfer of charge between the buried storage electrodes. In this case, four-phase, two-phase, and single-phase clocking schemes may be used to control the storage and transfer of charge for both serpentine and parallel signal flow.

A detailed explanation of push clock operation and comparison with drop clocks can be made with the aid of Figs. (5), (6), and (7). These figures depict charge storage and transfer in three-phase, four-phase, and two-phase CCD's respectively with both drop and push clocks. The particular clock voltages shown apply to the case of p-channel devices, in which all clock voltages are negative. V_m is the minimum (most negative) clock voltage that can be used, as determined by some constraint such as field oxide threshold; V_1 is the holding voltage (in the drop clock case); and V_2 is a resting (gate-off) voltage; thus $V_2 > V_1 > V_m$.

The drop clock case is shown first; the signal charge is stored under a gate at potential V_1 (Figs. 5a, 6a, and 7a). To effect charge transfer, the voltage of the next gates is lowered to V_m (Figs. 5b, 6b, and 7b); the charge flows to the local potential minimum thus created. In the push clock case, the signal

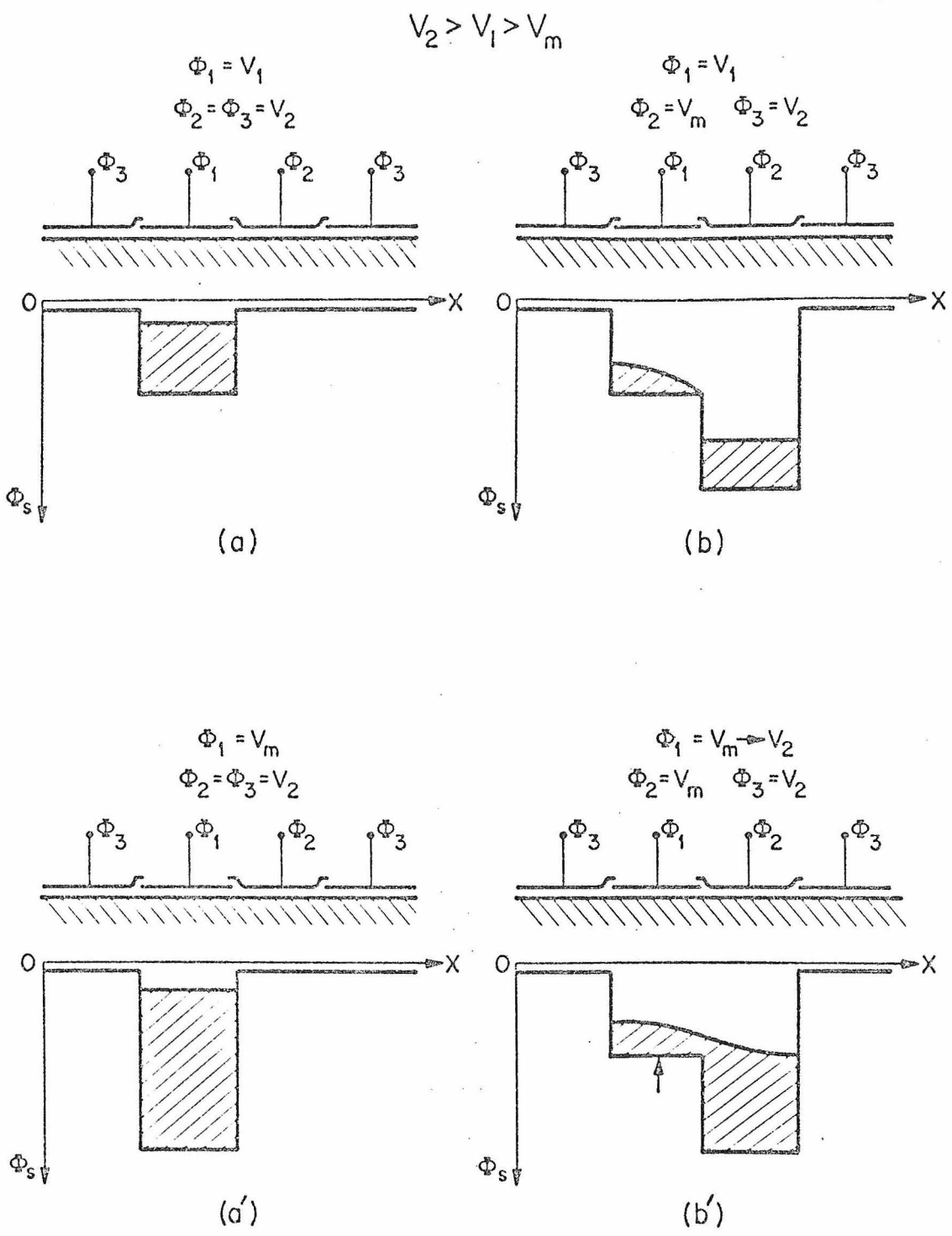
$V_2 > V_1 > V_m$
$\Phi_1 = V_1$
$\Phi_2 = \Phi_3 = V_2$
Φ_3 Φ_1 Φ_2 Φ_3
O
X
Φ_s
(a)
$\Phi_1 = V_1$
$\Phi_2 = V_m$ $\Phi_3 = V_2$
Φ_3 Φ_1 Φ_2 Φ_3
O
X
Φ_s
(b)
$\Phi_1 = V_m$
$\Phi_2 = \Phi_3 = V_2$
Φ_3 Φ_1 Φ_2 Φ_3
O
X
Φ_s
(a′)
$\Phi_1 = V_m \rightarrow V_2$
$\Phi_2 = V_m$ $\Phi_3 = V_2$
Φ_3 Φ_1 Φ_2 Φ_3
O
X
Φ_s
(b′)

Figure 5.

$V_2 > V_1 > V_m$

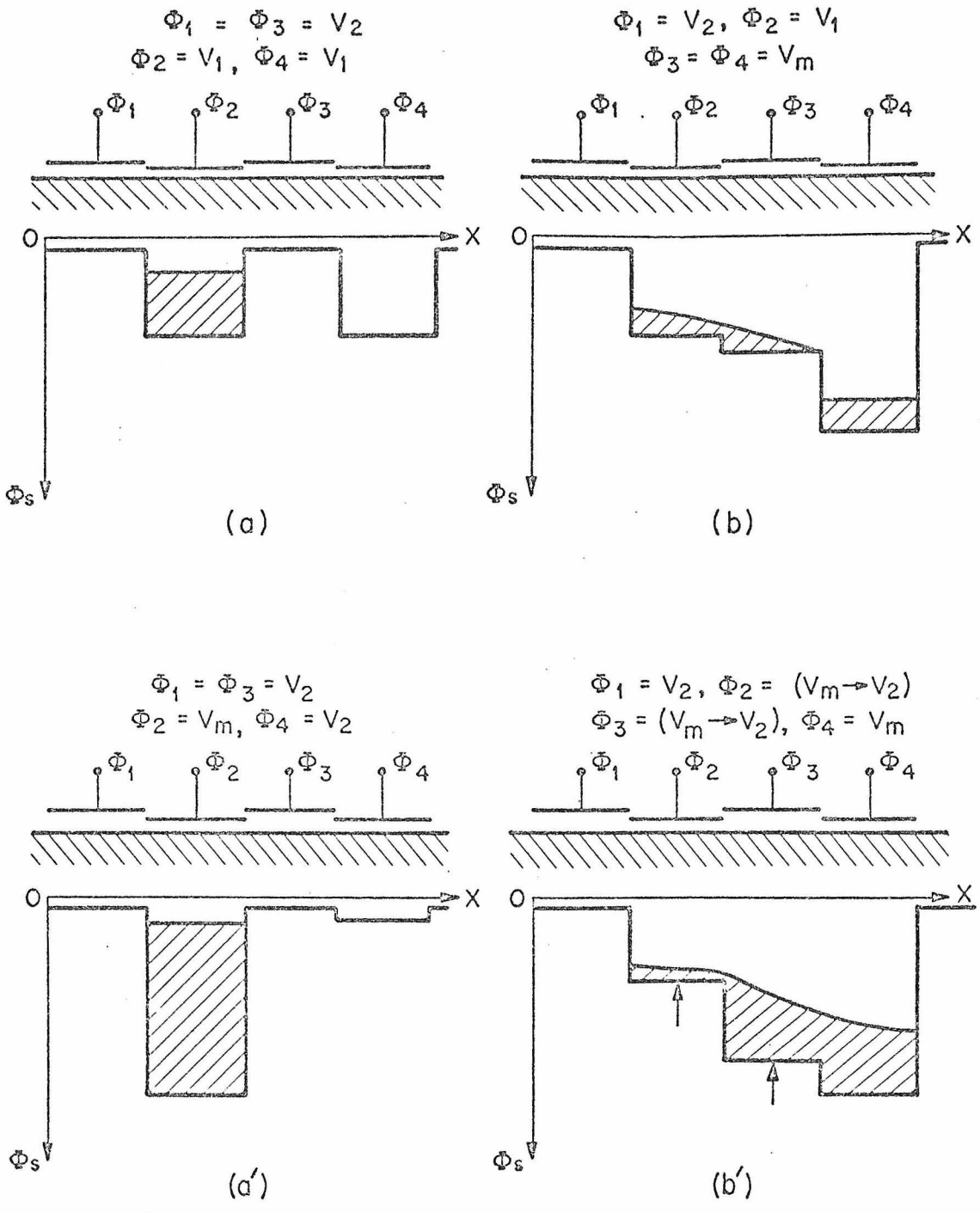

Figure 6.

$V_2 > V_1 > V_m$

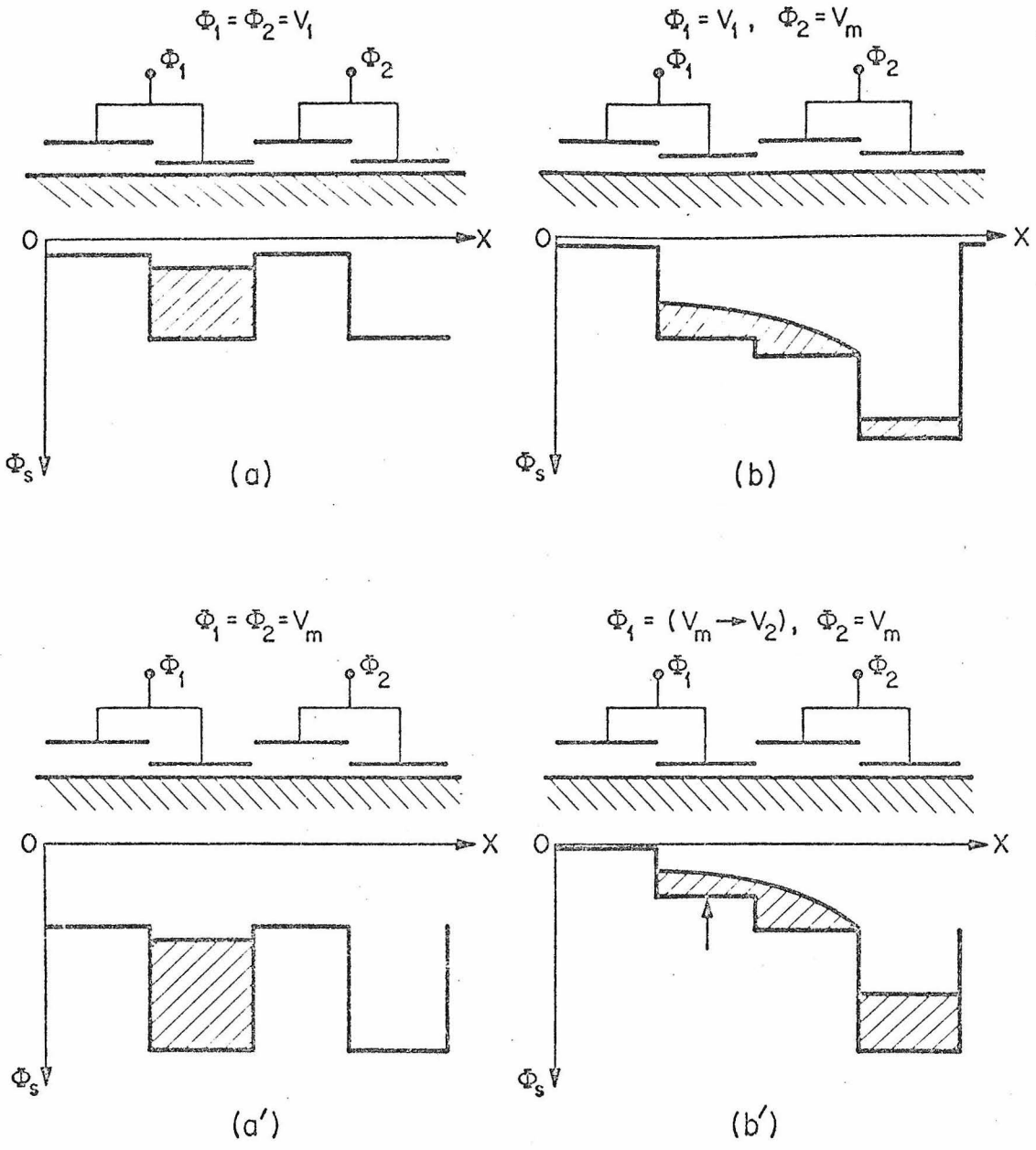

Figure 7.

charge is initially held under a storage gate which is at V_m (Figs. 5a', 6a', and 7a'). At the beginning of the charge-transfer operation, the voltages of the next gates are lowered to V_m . The potential of the original storage gate is then gradually raised, and the charge stored there is pushed to the area under the next storage gate (Figs. 5b', 6b', and 7b'). As the potential of the original storage gate continues to rise, more of the charge under it is brought to a potential higher than that under the transfer gate, and so is able to flow to the next storage gate. Finally the original storage gate reaches its resting potential, V_2.

It can be seen from the preceding discussion that the push clocks allow a greater fraction of V_m to be used in storing the signal charge, and thus provide a greater dynamic range and signal to noise ratio than drop clocks. Also as will be shown in the next sections, the push clock scheme yields better charge-transfer efficiency at both high and low frequencies, and allows a definite advantage in high-speed operation to be obtained from the use of a four-phase clock. In Figs. (6) and (7), it is clear that the charge transfer for the two-phase drop clock and four-phase drop clock are similar, therefore increasing the clock complexity from two-phase to four-phase with drop clocks does not improve the performance of the device. However the push clock takes full advantage of the more flexible control of the surface potential under the different electrodes. For example in Fig. (6a') during storage times the transfer gates can be turned off by the resting voltage V_2 and the storage gates can be

heavily turned on by the minimum voltage V_m. The maximum signal charge which may be stored under the storage gate is thus almost a full bucket.[6] Also, since the transfer gates are controlled independently, they can be turned on heavily during the first stages of the transfer process, as shown in Figs. (6b') to enhance the rate of charge transfer. Thus increasing the clocking scheme complexity with push clock allows better control of the storage and transfer of the signal charge and hence provides larger signal dynamic range, larger signal to noise ratio and better performance, especially at high frequency.

The waveforms of the different phases of the dynamic push clocks must be overlapping. Since the rate of charge transport along the interface is finite the rise times T_r of the clocking pulse have minimum permissible values. If these values are exceeded the surface potential under the gates exceeds $2\phi_F$ and some of the signal charge will be injected into the substrate where it is lost by recombination. For example, the minimum rise time of the two-phase push clock is given by (as shown in Eq. (20) below)

$$T_{r_{min}} \sim 2 \frac{\ell_{St}\ell_{Tr}}{\mu} \frac{C_{St}}{C_{Tr}} \cdot \frac{1}{V_c}$$

where ℓ_{Tr} and ℓ_{St} are the lengths of transfer gate and storage gate. μ is the surface mobility. C_{St} and C_{Tr} are the effective oxide and depletion layer capacity under the storage and transfer gates respectively. V_c is equivalent to the clocking voltage amplitude. For minimum geometry electrodes ($\sim$10 microns) and reasonable clock voltage amplitudes ($\sim$5 volts), $T_{r_{min}}$ is much smaller than the finite

rise and fall times which are unavoidable in practical clock drivers ($\sim$tens of nanosecond). Hence, the finite rise and fall times that would delay the charge transfer with drop clocks are advantageously used with push clocks to push the charge from one storage site to another.

A single clocking phase could be used to operate the device as shown in Fig. (8). In this case the same two-phase structure of Fig. (7) is used, and one of the clocking phases ϕ_2 is kept at a constant voltage V_1, while the other phase ϕ_1 is changed between V_m and V_2. When ϕ_1 changes from V_m to V_2 the signal charge is pushed from under ϕ_1 to under ϕ_2 in one half cycle. In the other half cycle when ϕ_1 changes from V_2 to V_m the signal charge flows to the deeper potential well under ϕ_1. Instead of applying a bias voltage V_1 on ϕ_1, ion implantation or the charge storage properties of double dielectric structure could be used. As compared with the two-phase and four-phase clocking scheme, the signal phase clocking scheme utilizes a smaller fraction of the surface potential swing to store the signal charge and, therefore, the device will have smaller signal dynamic range, signal to noise ratio, and transfer efficiencies.

3.2 Two-Phase Clocking Scheme

In the two-phase clocking scheme only two clock phases are used to control the storage and transfer of charge along the interface. The asymmetry in the surface potential needed to provide the directionality of the signal charge transfer can be achieved by using

$V_2 > V_1 > V_m$

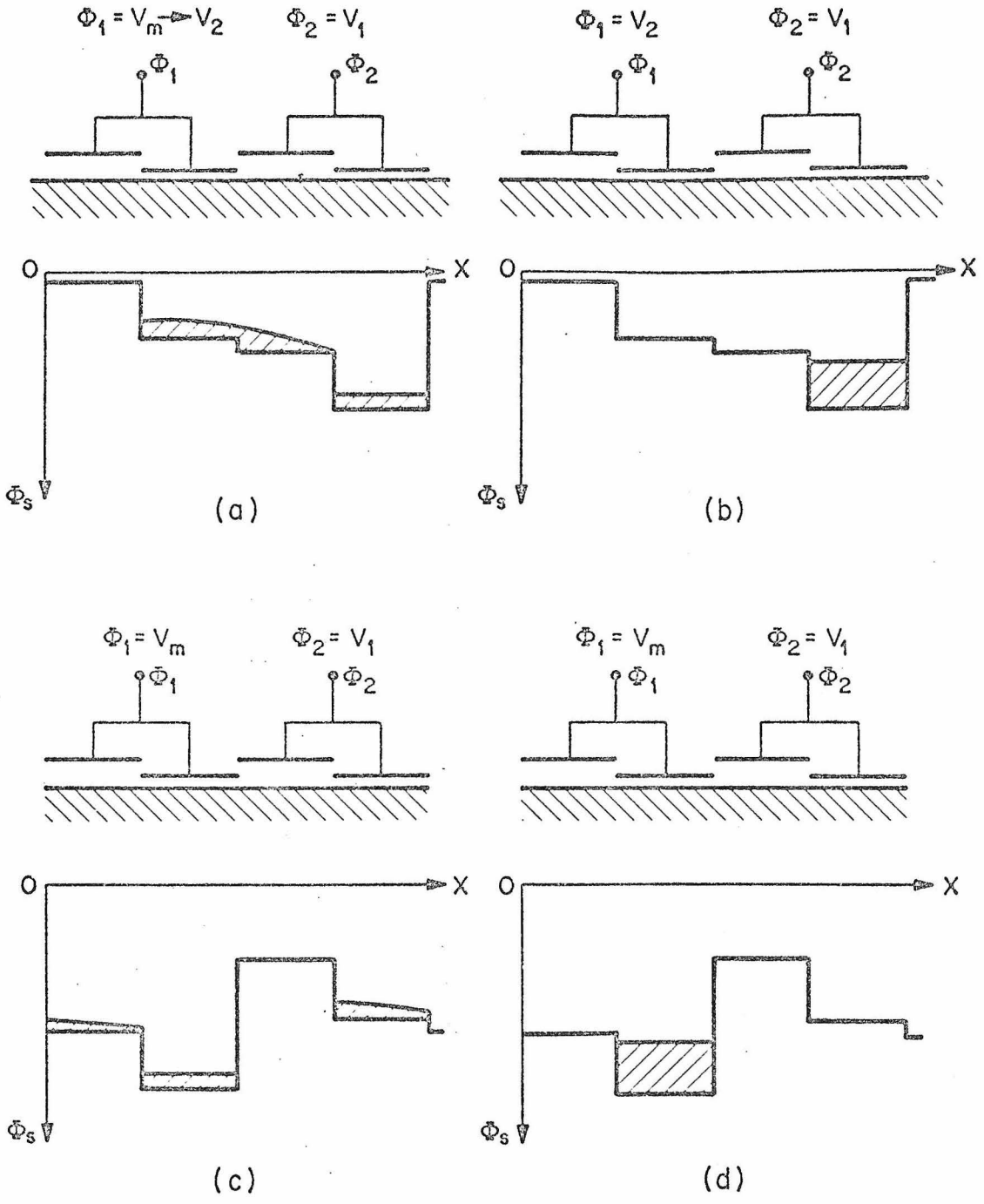

Figure 8.

a step in the channel oxide[7] or an ion implanted barrier[13] or the charge storage properties of double dielectric structures.[14] In this section we present some of the calculations of the charge transfer characteristics of two-phase overlapping gates CCDs where the asymmetry of the structure is achieved by a step in the channel oxide. However our results can be applied to all other structures with the appropriate modifications.

3.2.1 Complete Charge Transfer Mode

In the complete charge transfer modes the charge under the storage gate is transferred to the following gates; none is deliberately retained.

(A) Drop Clock: With drop clock the signal charge is stored below a gate at a holding voltage V_1 which is a fraction of the largest clock voltage V_m that the MOS structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates and the charge flows to the potential minimum thus created.

In Fig. (9) we have plotted the one-dimensional relation between the surface potential and the gate voltage for a polysilicon gate with 1200 Å oxide and for an aluminum gate with different oxide thickness for a substrate doping of 8×10^{14} donors/cm^3. Since in the two-phase clocking scheme the surface potential under each successive set of transfer and storage gates is controlled by a single clocking voltage, the maximum amount of charge that can be stored under the storage gate without spill over and the fringing fields under it depend on the silicon oxide thickness under the transfer and storage gates.

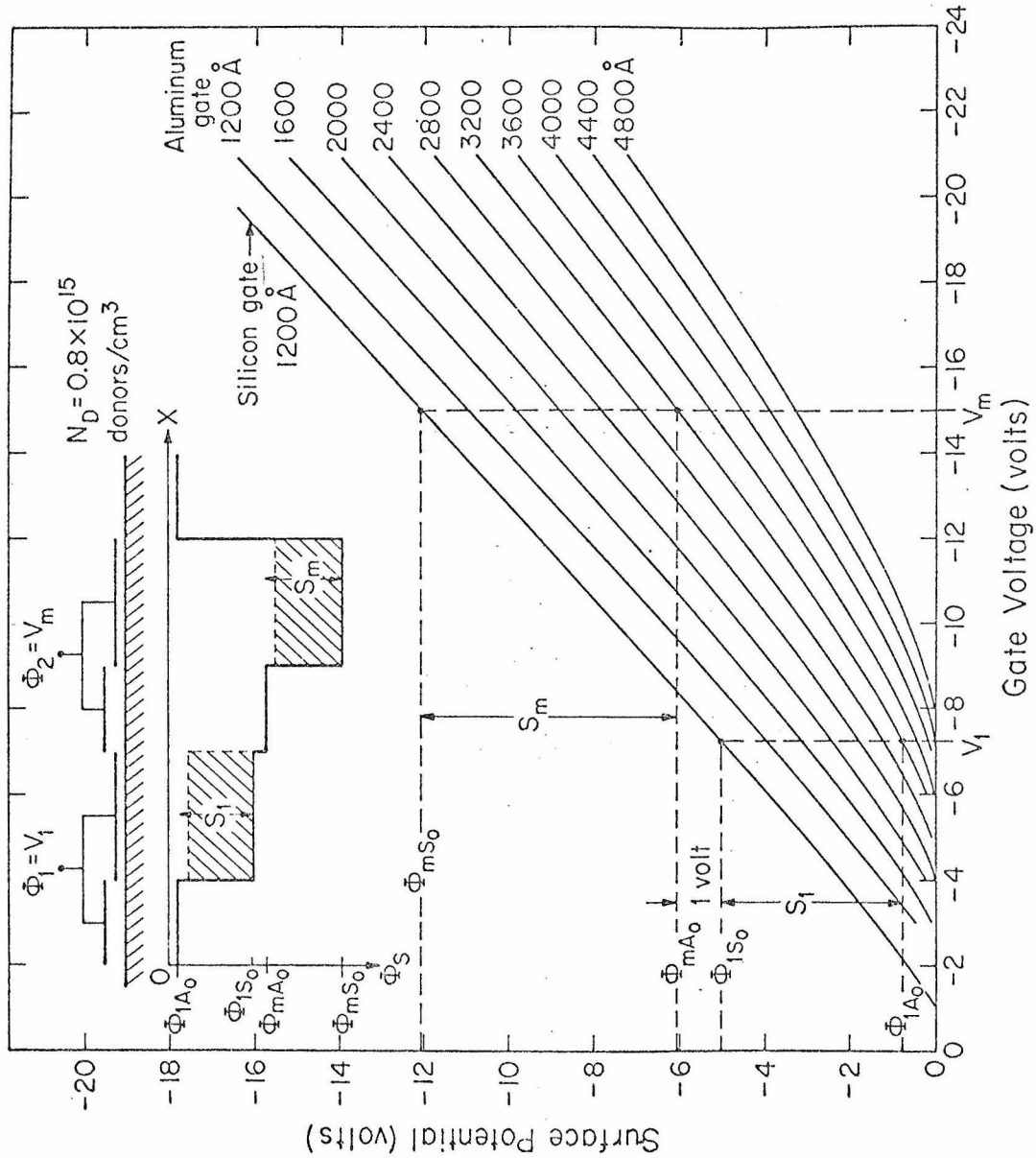
Surface Potential (volts)
Gate Voltage (volts)
Aluminum gate
1200 Å
1600
2000
2400
2800
3200
3600
4000
4400
4800 Å
Silicon gate
1200 Å
$N_D = 0.8 \times 10^{15}$ donors/cm^3
X
$\Phi_1 = V_1$
$\Phi_2 = V_m$
S_1
S_m
Φ_{1A_o}
Φ_{1S_o}
Φ_{mA_o}
Φ_{mS_o}
Φ_S
1 volt
V_1
V_m

Figure 9.

Therefore, for optimum operation of the device, the oxide thickness under the storage and transfer gates should be properly chosen. [7]

We have simulated numerically the charge transfer characteristics for the device shown at the top of Fig. (10) clocked by square wave drop clocks with zero fall and rise times. [8] The transient currents at the beginning and end of the aluminum transfer gate and the net current charging it are shown in Fig. (10). Zero time corresponds to the instant when ϕ_2 decreases to V_m starting the charge transfer. The current at the beginning of the gate increases from zero sharply to about 60 μamp and then decreases rapidly. The surface charge takes about 0.3 nanoseconds propagating under the transfer gate to reach its end. The transfer gate is charged rapidly during the first nanosecond and then is discharged slowly. In Fig. (11) a few frames are shown to illustrate the details of the charge transfer at its initial stages. A perfect sink at the end of the storage gate being discharged is formed after about 13 nanoseconds. The large surface potential gradient in the interelectrode regions between the transfer gate and the receiving storage gate sweeps out the minority carriers fast enough to create an almost perfect sink of charge there during all stages of the transfer. In Fig. (12) we have plotted the residual charge under the source storage gate as a percentage of a full bucket for two different initial charges equivalent to about 3 volts and 1 volt with a substrate doping of 8×10^{14} donors/cm^3 and 10^{14} donors/cm^3. Consideration of the transient currents at the ends of the transfer gate and the surface charge and surface potential profiles under the

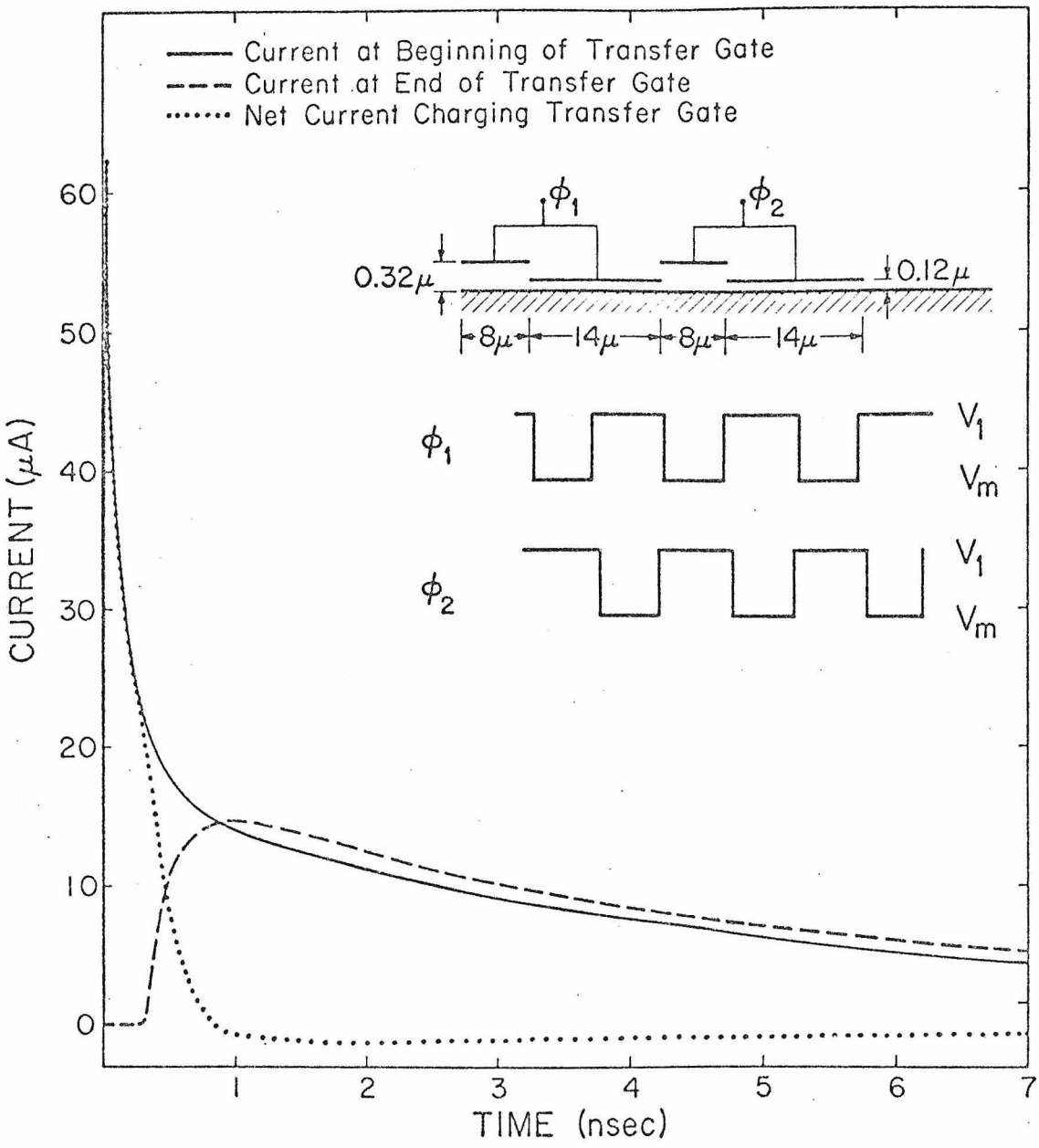
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
ϕ_1
ϕ_2
0.32μ
0.12μ
8μ
14μ
8μ
14μ
ϕ_1
V_1
V_m
ϕ_2
V_1
V_m
CURRENT (μA)
60
50
40
30
20
10
0
1
2
3
4
5
6
7
TIME (nsec)

Figure 10.

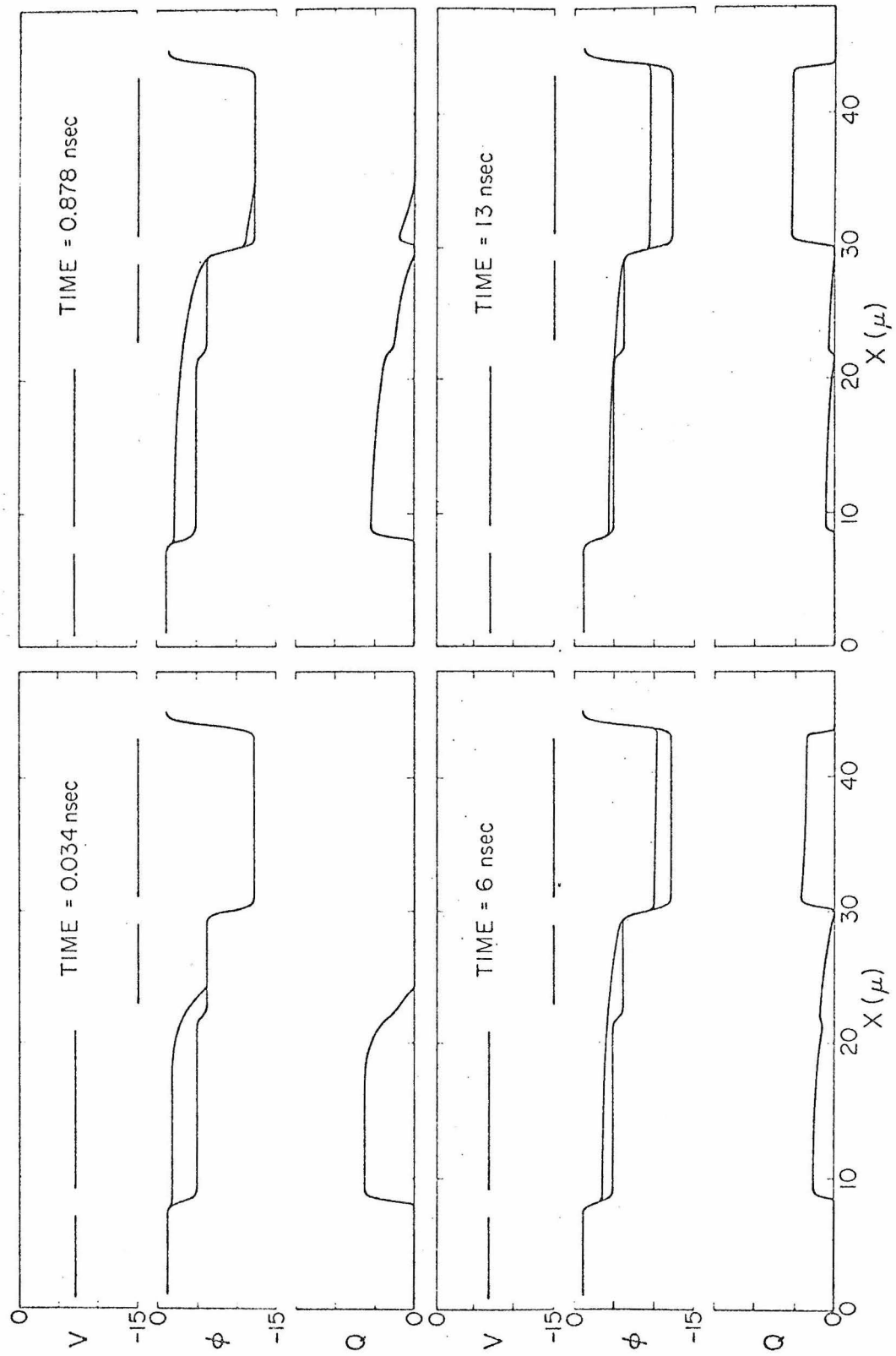
TIME = 0.034 nsec
TIME = 0.878 nsec
TIME = 6 nsec
TIME = 13 nsec
V
φ
Q
0
-15
10
20
30
40
X (μ)

Figure 11.

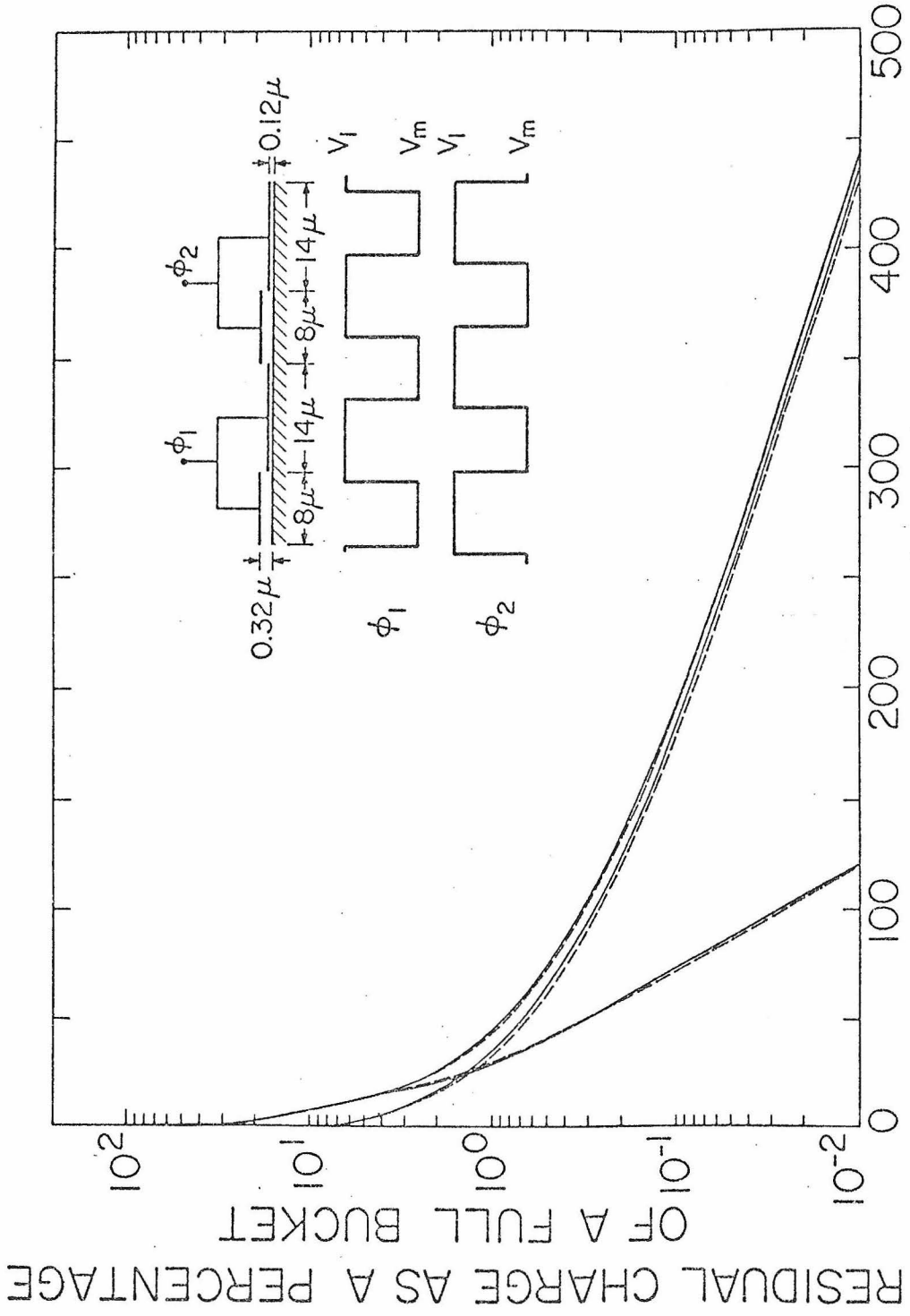
RESIDUAL CHARGE AS A PERCENTAGE OF A FULL BUCKET
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
0
100
200
300
400
500
TIME (nsecs)
ϕ_1
ϕ_2
V_1
V_m
V_1
V_m
ϕ_1
ϕ_2
0.32μ
0.12μ
8μ
14μ
8μ
14μ

Figure 12.

gates during the charge transfer show that the charge transfer divides naturally into several distinct stages.

(i) In the first stage, the charge initially confined under the source storage gate spreads to charge up the adjacent transfer gate for a fraction of a nanosecond.

(ii) In the second stage, the charge transfer is limited by the transport of charge across the transfer gate to the next storage gate. The transfer gate acts as a MOS transistor at pinch off with the storage gates as its source and drain. Thus the source and receiving storage gates are capacitors charged and discharged through the transfer channel.

According to the lumped circuit model discussed in Appendix V the decay of the residual charge under the gates is described by

$$\frac{d}{dt}(Q_{St} + Q_{Tr}) = \frac{-\mu C_{Tr} W}{2\ell_{Tr}} \left[2KT(\phi_{mT} - \phi_{mTo}) + (\phi_{mT} - \phi_{mTo})^2 \right] \tag{6a}$$

$$Q_{St} = w\ell_{St}\, C_{St}(\phi_{1s} - \phi_{1so}) \quad , \tag{6b}$$

$$Q_{Tr} = \frac{2}{3} w\ell_{Tr}\, C_{Tr}(\phi_{mT} - \phi_{mTo}) \quad , \tag{6c}$$

$$\phi_{mT} \cong \phi_{1s} \quad ; \quad \phi_{mT}' = \phi_{mTo} \quad , \tag{6d}$$

where Q_{St} and Q_{Tr} are the total charges under the source storage gates and transfer gates. ϕ_{1s} and ϕ_{1so} are the surface potential under the source storage gate with and without surface charge when its voltage is equal to V_1. ϕ_{mT} and ϕ_{mT}' are the surface potential

with charge at the beginning and at the end of the transfer gate respectively, and ϕ_{mTo} is the surface potential under the transfer gate without charge when its voltage is equal to V_m. C_{St} and C_{Tr} are the effective oxide and depletion layer capacity under the storage and transfer gates. ℓ_{St} and ℓ_{Tr} are the lengths of the storage and transfer gates, W is the active channel width, and KT is the thermal voltage. Since in this stage $(\phi_{mT} - \phi_{mTo}) >> KT$, then for an initial total charge Q_o the residual charge under the storage gate decreases hyperbolically and is given by:

$$Q = \frac{Q_o + Q'}{1 + \left(\frac{t - t_1}{\tau_2}\right)} - Q' \quad , \qquad (7)$$

where $Q' = W\ell_{St}C_{St}(\phi_{1so} - \phi_{mTo})$, t_1 is the time at which the second stage starts and τ_2 is given by

$$\tau_2 = 2\,\frac{\ell_{Tr}\ell_{St}}{\mu}\,\frac{C_{St}}{C_{Tr}}\,\frac{R}{\frac{(Q_o + Q')}{W\ell_{St}\,C_{St}}} \quad , \qquad (8)$$

where

$$R = 1 + \frac{2}{3}\,\frac{\ell_{Tr}C_{Tr}}{\ell_{St}C_{St}} \quad . \qquad (9)$$

When the charge under the storage gate decreases to a small value Q_o', the discharge current becomes so small that the electric field in the transitional region between the source storage gate and the next transfer gate can sweep out the carriers fast enough to form an almost perfect sink of charge there. [9] This brings the second stage to an

end at a time t_2 given by

$$t_2 = t_1 + \tau_2 \frac{Q_o - Q_o'}{Q_o' + Q'}$$

For the device parameters given below:

$$\left.\begin{aligned} \ell_{St} &= 13.5 \text{ microns} & \ell_{Tr} &= 7 \text{ microns} \\ C_{St} &= 3.5 \times 10^{-8} \text{ Farad/cm}^2 & C_{Tr} &= 1.45 \times 10^{-8} \text{ Farad/cm}^2 \\ \mu &= 200 \text{ cm}^2/\text{sec}\cdot\text{volt} \\ \frac{Q'}{W\ell_{St}C_{St}} &= 0.8 \text{ volts} & \frac{Q_o'}{W\ell_{St}C_{St}} &= 0.48 \text{ volts} \end{aligned}\right\} \qquad (10)$$

and for a signal charge equivalent to about 3 volts we obtain $\tau_2 \cong 6.9$ nsec and $t_2 = 13$ nsec. For a signal charge equivalent to about 1 volt, we obtain $\tau_2 \cong 14.6$ nsec and $t_2 = 5.9$ nsec.

(iii) In the third stage the charge transfer is limited by the transport of charge out of the storage gate with an almost perfect sink at its end. The storage gate can be considered in this stage also as a capacitor discharged through a transfer channel which is the same storage gate. Thus according to the lumped circuit model it can be easily shown (or by expanding the denominator in Eq. (A5-6)) that the residual charge under the storage during the first part of this stage (when $\frac{Q(t)}{W\ell_{St}C_{St}} \gg KT$) decreases almost hyperbolically with a time constant τ_3. So,

$$Q(t) = \frac{Q_o'}{1 + \frac{(t - t_2)}{\tau_3}} \qquad t > t_2 \quad , \qquad (11)$$

$$\tau_3 = \frac{\ell_{St}^2}{\alpha \frac{Q_o'}{C_{St}\ell_{St}W}\mu} \quad . \qquad (12)$$

where α is a constant of the order of unity (about 1.2). During this stage the charge is spread over the entire gate even if fringing fields are appreciable.

(iv) In the last stage of the charge transfer, the self-induced fields become negligible. The residual charge decreases exponentially with a time constant that depends on thermal diffusion and the fringing fields under the storage gate.

For the device we have considered here and for a substrate doping of 8×10^{14} donors/cm^3 and larger, fringing fields under the storage gate are negligible. For $t > t_3$ the residual charge under the storage gate decreases exponentially with the thermal diffusion time constant $\tau_d = \frac{\ell_{St}^2}{2.5\ D}$, where

$$Q(t_3) \sim W\ell_{St}C_{St}KT \qquad t_3 \cong t_2 + \frac{\pi}{2}\tau_d \quad . \qquad (13)$$

For the device we have considered and for substrate doping equal to 10^{14}donors/cm^3, solutions of the two-dimensional Poisson equation at the end of the charge transfer show a minimum fringing field E_{min} under the storage gate of about 70 volt/cm and an average value $\bar{E}$ of about 140 volt/cm. The fringing fields considerably enhance the

rate of charge transfer. The single carrier transit time across the storage gate t_{tr} due to fringing fields is given by

$$t_{tr} = \int_{\substack{\text{over storage} \\ \text{gate length}}} \frac{dy}{\mu E(y)} = \frac{\ell_{St}}{\mu \bar{E}} = \frac{\ell_{St}^2}{\mu \Delta\phi} \quad , \qquad (14)$$

where $\bar{E}$ is the average fringing field under the storage gate, $\Delta\phi$ is equal to $\bar{E}\ell_{St}$ and is related to the voltage drop across the storage gate due to fringing fields.

Under the influence of the fringing fields, the charge profile under the storage gate starts to drift after a time $t_3 \simeq t_2 + t_{tr}$ for about one single carrier transit time and then becomes stationary at a position that depends on the minimum fringing field E_{min}. The residual charge then decreases exponentially with a final decay time constant given approximately by

$$\frac{1}{\tau_f} \simeq 4\left(\frac{\pi^2 D}{4\ell_{St}^2}\right) + \frac{\left(\mu E_{min}\right)^2}{4D} \quad . \qquad (15)$$

The factor 4 in the second term is due to the large fields at the edges of the gate. For negligible fringing fields this factor takes a value of unity. The exponential decay is due to the diffusion at the tail end of the residual charge packet under the storage gate irrespective of the fringing field profile. Fringing fields alone, without diffusion and self-induced fields, will sweep out the residual charge under the storage gate in a single carrier transit time.

The transition between the hyperbolic regime of the third stage and the exponential regime of the last stage of the charge is rather

broad and is best described by Eq. (A5-9) in Appendix V

$$\frac{Q_{st}}{Q_o'} \approx \frac{\exp\left(-(t-t_2)/\tau_f\right)}{1 + \frac{Q_o'}{\frac{2}{3} C_{St} \ell_{St} W} \cdot \frac{1}{2KT} \cdot \frac{\tau_f}{\tau_d} \left[1 - \exp\left(-(t-t_2)/\tau_f\right)\right]} \tag{16}$$

The dashed lines [10] in Fig. (12) are obtained from Eq. (7) and (16) with the device parameters given in Eq. (10).

(B) Push Clocks: With push clocks the charge is stored under a gate held at V_m which is the largest clock voltage the MOS structure can tolerate. The charge is transferred to a nearby gate also at V_m by raising the potential of the gate where the charge has been residing and thus pushing the charge to the next gate.

For optimum operation of the device with two phase push in the complete charge transfer mode, the oxide thickness under the storage and transfer gates should be properly chosen. [11]

We have simulated numerically the charge transfer characteristics for several devices with various clocking waveforms. In Figs. (13) and (17) we show the transient currents at the beginning and end of the transfer gate, as well as the net current charging the region under the gate. The clock voltages and rise time as well as the oxide thickness under the transfer gates of the device are shown for each case at the top of the figures. Zero time coincides with the instant the clock voltage starts to increase to push the charge and starts the transfer. The currents are zero for the first few nanoseconds until the charge initially confined under the silicon storage gate can flow

to the next gates. This time delay depends on the clock rise time and the initial charge under the storage gate. In Fig. (13) we have plotted the transient currents for a device with 4400 Å oxide under the transfer gate and with a clock rise time equal to 40 nanoseconds and a minimum voltage V_m equal to -15 volts. The currents at the beginning of the transfer gate starts to increase at about 4.5 nanoseconds reaching a maximum value of about 8 micro amperes, then it drops rapidly to zero at about 40 nanoseconds. The current at the end of the transfer gate has the same waveform but is delayed by 2.5 nanoseconds due to the charge propagation under the gate. From Fig. (13), it is obvious that the transfer gate is charged up rapidly during the first few nanoseconds. After this period, the charge under it remains almost constant. It is discharged at about 40 nanoseconds. In Fig. (14) we have plotted the transient currents for the same device with a similar clocking waveform but the rise time is equal to 50 nanoseconds. In this case the potential of the first phase of the clock ϕ_1, changes from the resting voltage V_2 to the minimum voltage V_m ending the transfer at about 90 nanoseconds. The currents in this case have almost the same waveform but they drop rapidly to zero at about 49 nanoseconds. The small negative spike at about 90 nanoseconds is due to the flow of the charge in the transfer gate back to the preceding storage gate when the voltage of the first phase of the clock drops to V_m ending the transfer.

In Figs. (15), (16), and (17) we have plotted the transients current for a device with 3200 Å oxide under the transfer gate using a

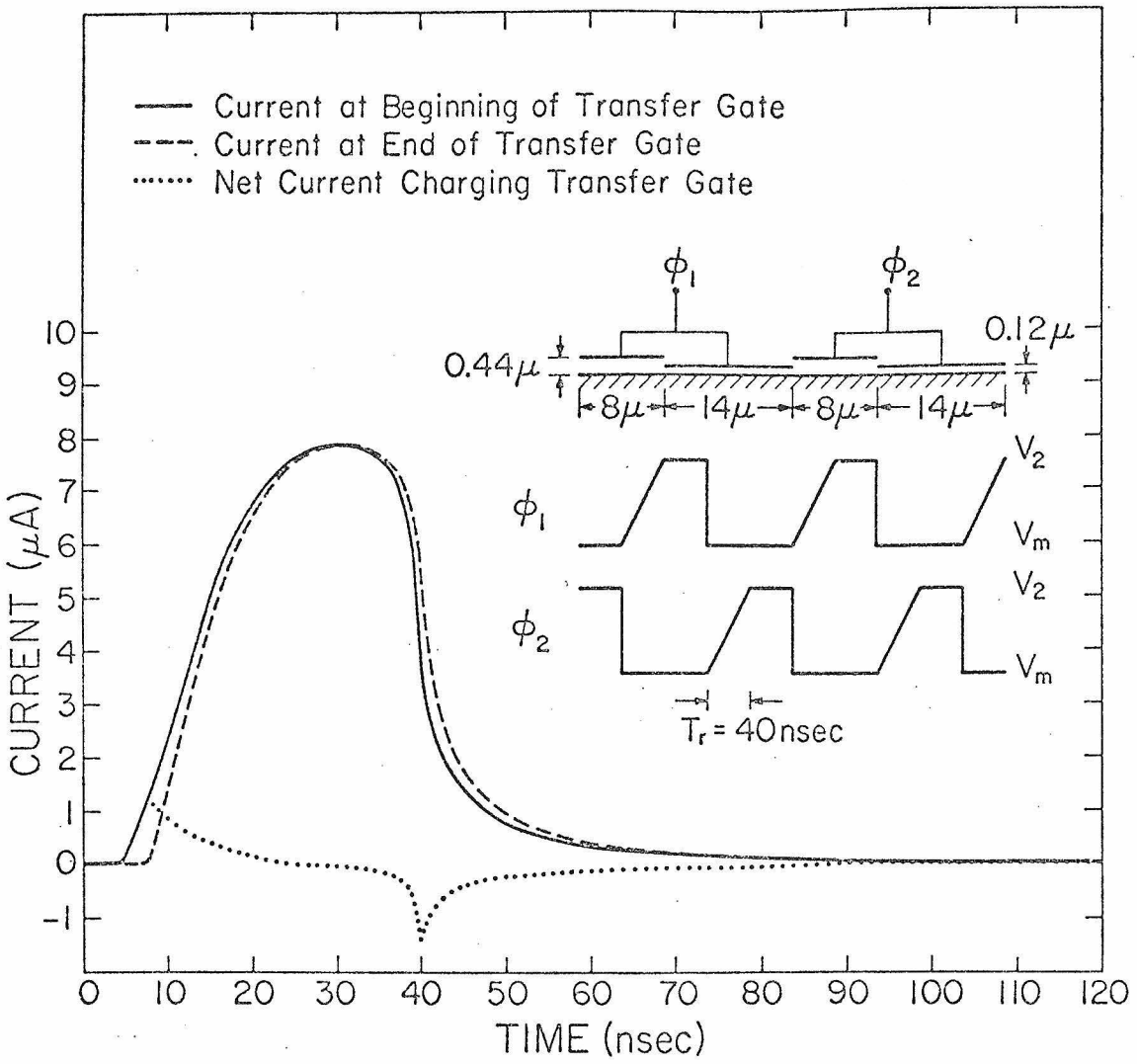
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
ϕ_1
ϕ_2
0.44μ
0.12μ
8μ
14μ
8μ
14μ
V_2
V_m
ϕ_1
V_2
ϕ_2
V_m
T_r = 40nsec
CURRENT (μA)
TIME (nsec)
10
9
8
7
6
5
4
3
2
1
0
-1
0
10
20
30
40
50
60
70
80
90
100
110
120

Figure 13.

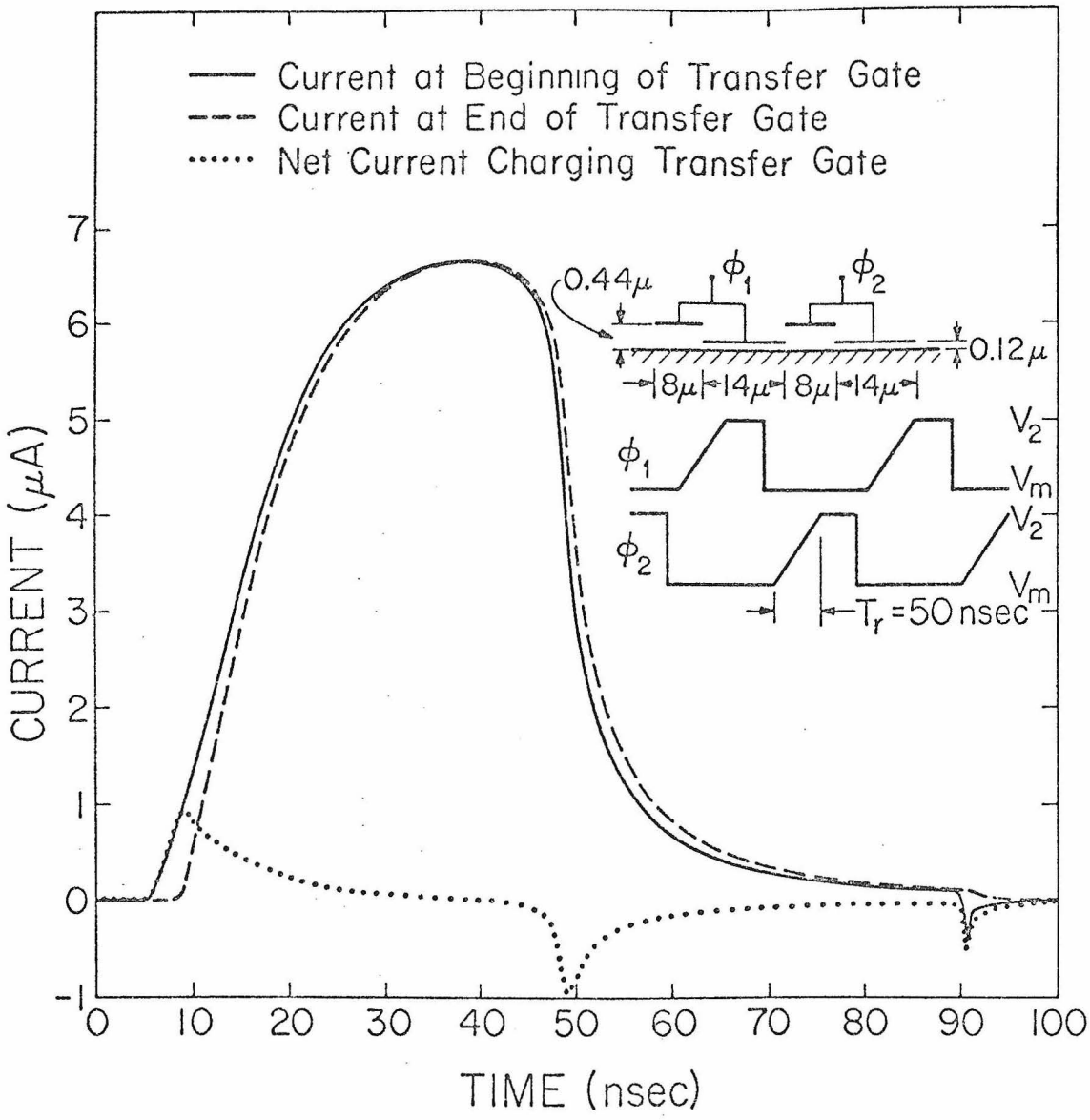
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
CURRENT (μA)
TIME (nsec)
0.44μ
φ1
φ2
0.12μ
8μ 14μ 8μ 14μ
V2
Vm
Tr=50 nsec

Figure 14.

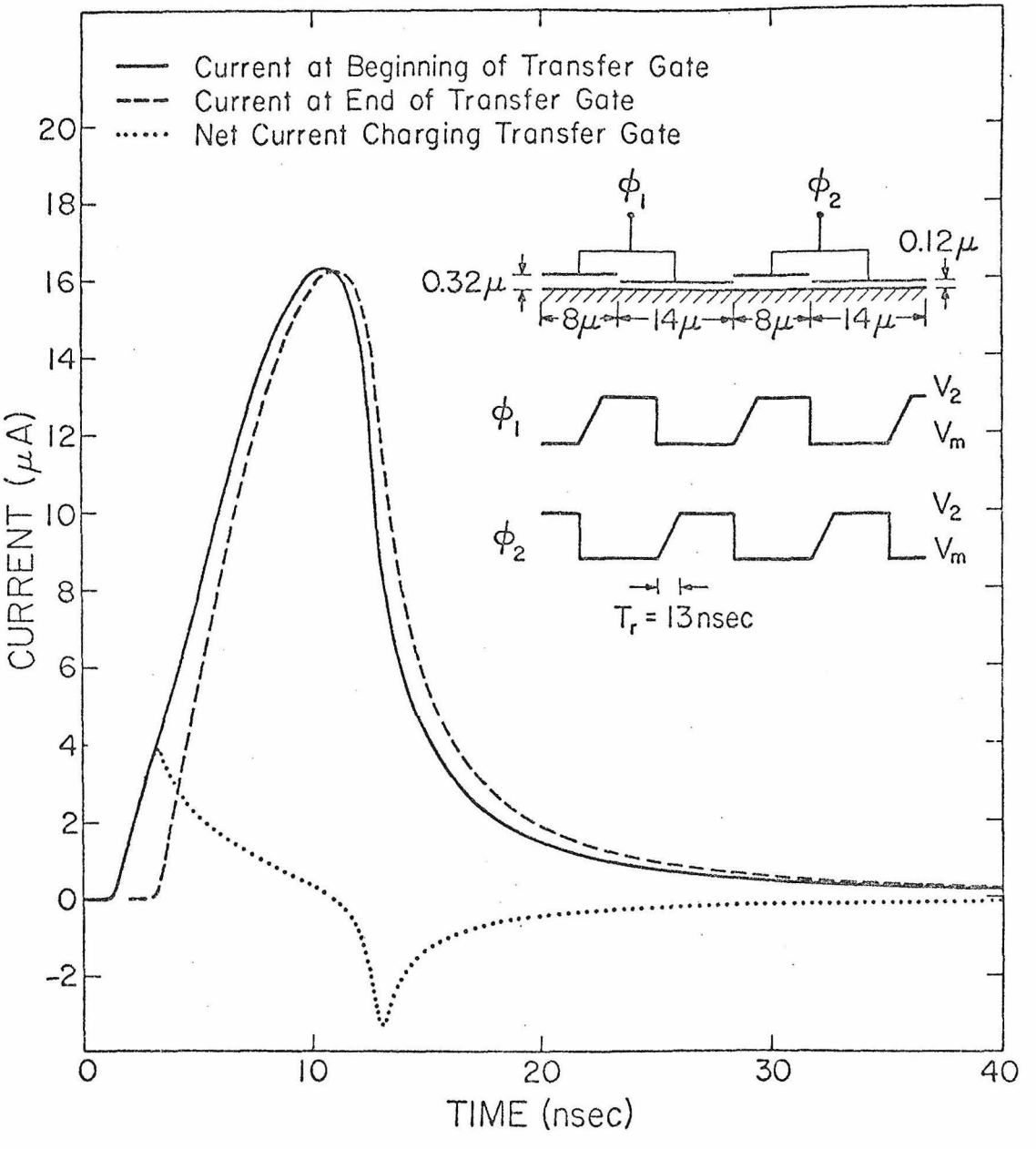
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
ϕ_1
ϕ_2
0.12μ
0.32μ
8μ
14μ
8μ
14μ
V_2
V_m
ϕ_1
V_2
V_m
ϕ_2
T_r = 13nsec
CURRENT (μA)
TIME (nsec)
20
18
16
14
12
10
8
6
4
2
0
-2
0
10
20
30
40

Figure 15.

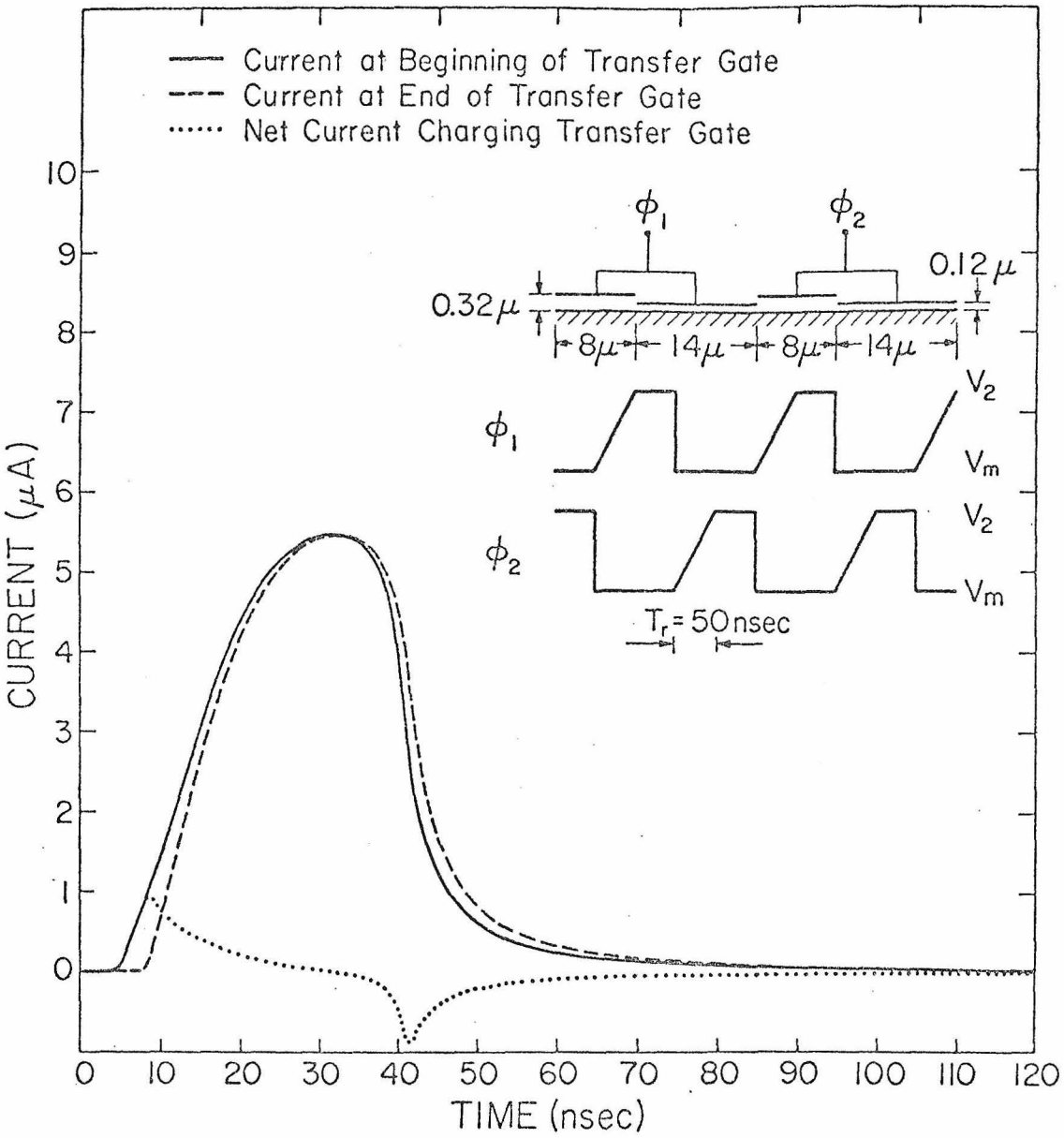
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
ϕ_1
ϕ_2
0.32μ
0.12μ
8μ
14μ
8μ
14μ
V_2
V_m
T_r = 50nsec
CURRENT (μA)
TIME (nsec)
0
10
20
30
40
50
60
70
80
90
100
110
120
1
2
3
4
5
6
7
8
9
10

Figure 16.

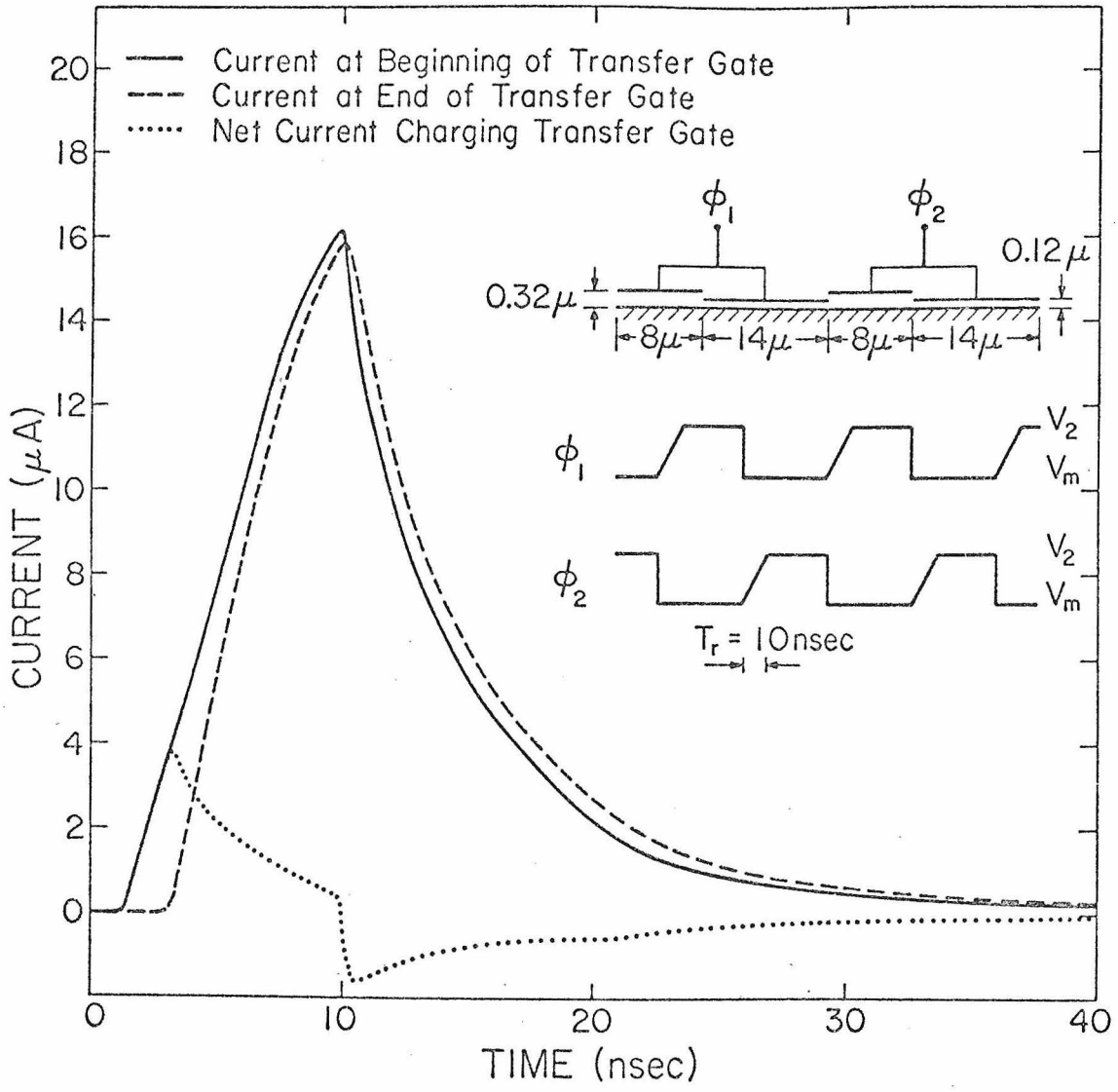
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
CURRENT (μA)
TIME (nsec)
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
ϕ_1
ϕ_2
0.32μ
0.12μ
8μ
14μ
8μ
14μ
V_2
V_m
T_r = 10nsec

Figure 17.

similar clocking waveform but the resting voltage is about -6 volts in the first two cases and -7 volts in the third case and the rise time is 13 nsec, 50 nsec, and 10 nsec, respectively. The current waveforms have essentially the same behavior except that they reach a maximum value of about 16 μamp then drop rapidly at 13 nsec in the first case, and in the second case they reach a maximum value of 5.5 μamp and drop rapidly at about 42 nsec. In the third case they reach a maximum value of 16 μamp and then drop rather slowly at about 10 nsec.

In Figs. (18) and (19), we have plotted a few frames of the surface potential and surface charge density profile for the cases shown in Fig. (14) and (17) respectively. In Fig. (20) and (21) we have plotted the residual charges under the source storage gate versus transfer time.for the cases shown in Fig. (13) and (15) respectively.

From the plots of the transient currents at the end of the transfer gate and the residual charges versus time and the surface charge and surface potential profiles under the gates one can identify several distinct stages of the charge transfer.

(i) In the first stage, the surface potential under the storage gate containing charge increases as the storage gate voltage is increasing, until it becomes equal or less than the surface potential under the next transfer gate by (KT). Then the charge initially confined under the storage gate spreads to charge up the next transfer gate. The time interval of the first part of this stage depends on the amount of initial charge and the clock rise time as given below in Eq. (19).

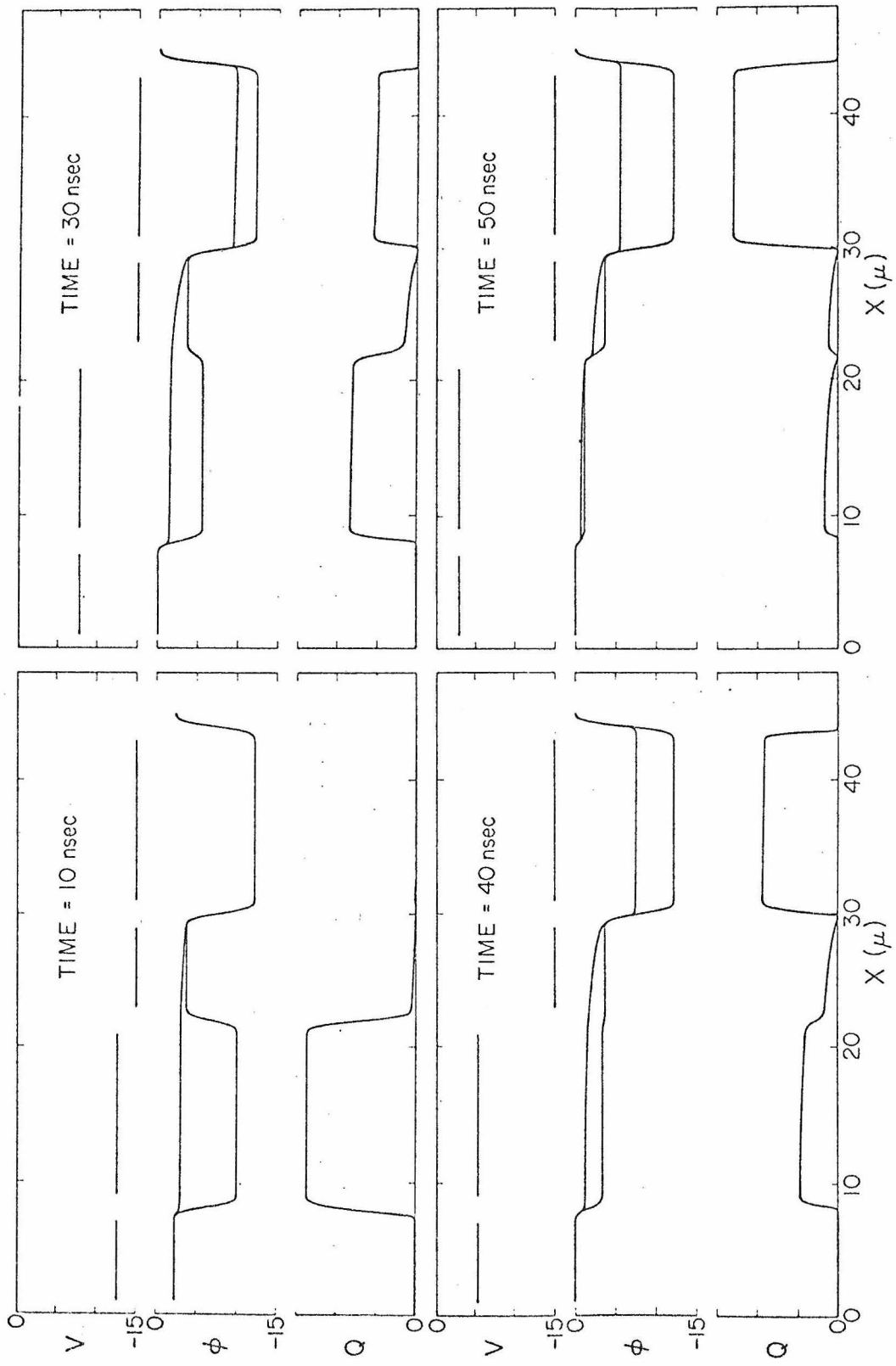
TIME = 10 nsec
TIME = 30 nsec
TIME = 40 nsec
TIME = 50 nsec
V
φ
Q
0
-15
10
20
30
40
X (μ)

Figure 18.

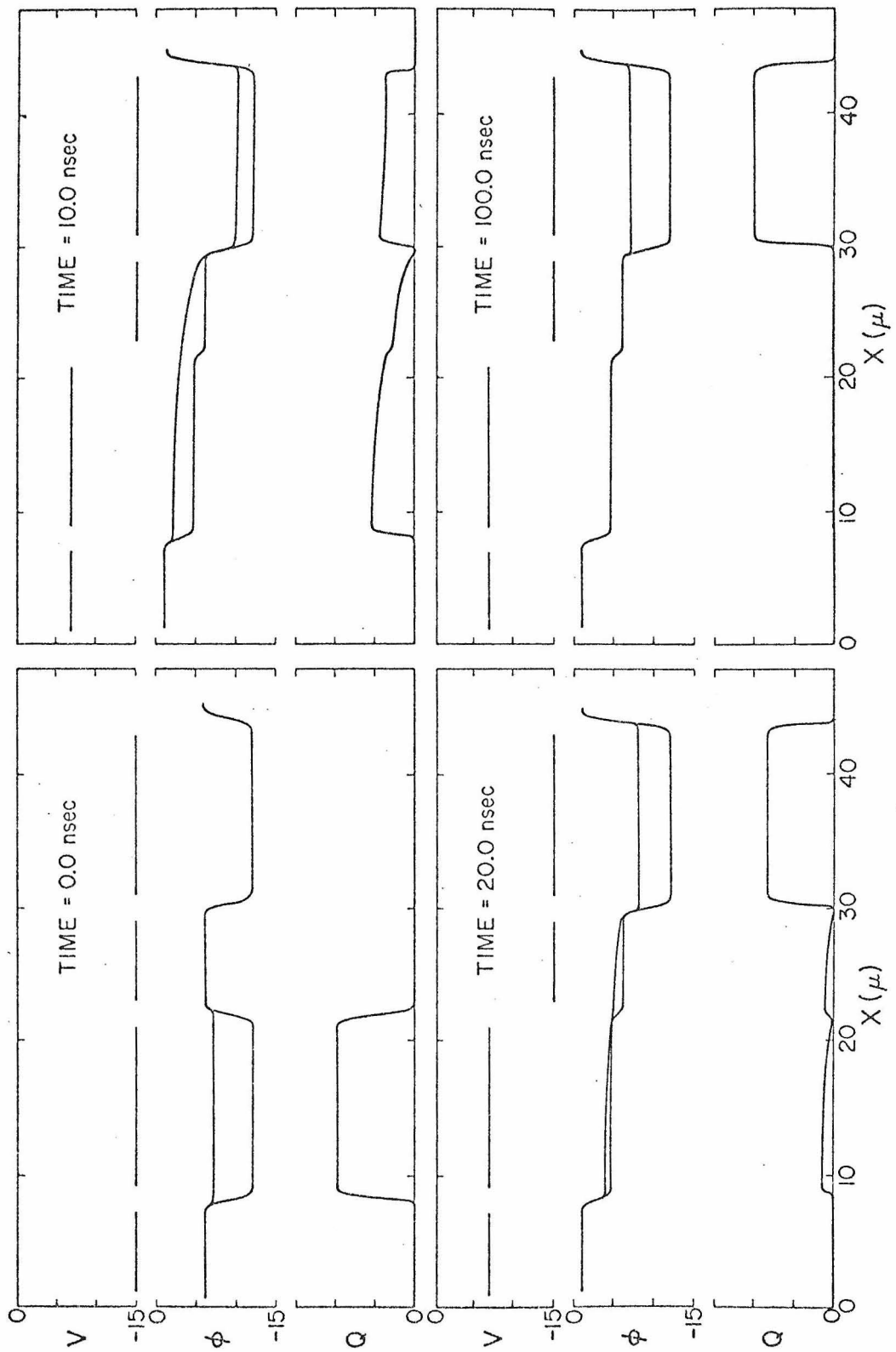
TIME = 0.0 nsec
TIME = 10.0 nsec
TIME = 20.0 nsec
TIME = 100.0 nsec
V
φ
Q
0
-15
10
20
30
40
X (μ)

Figure 19.

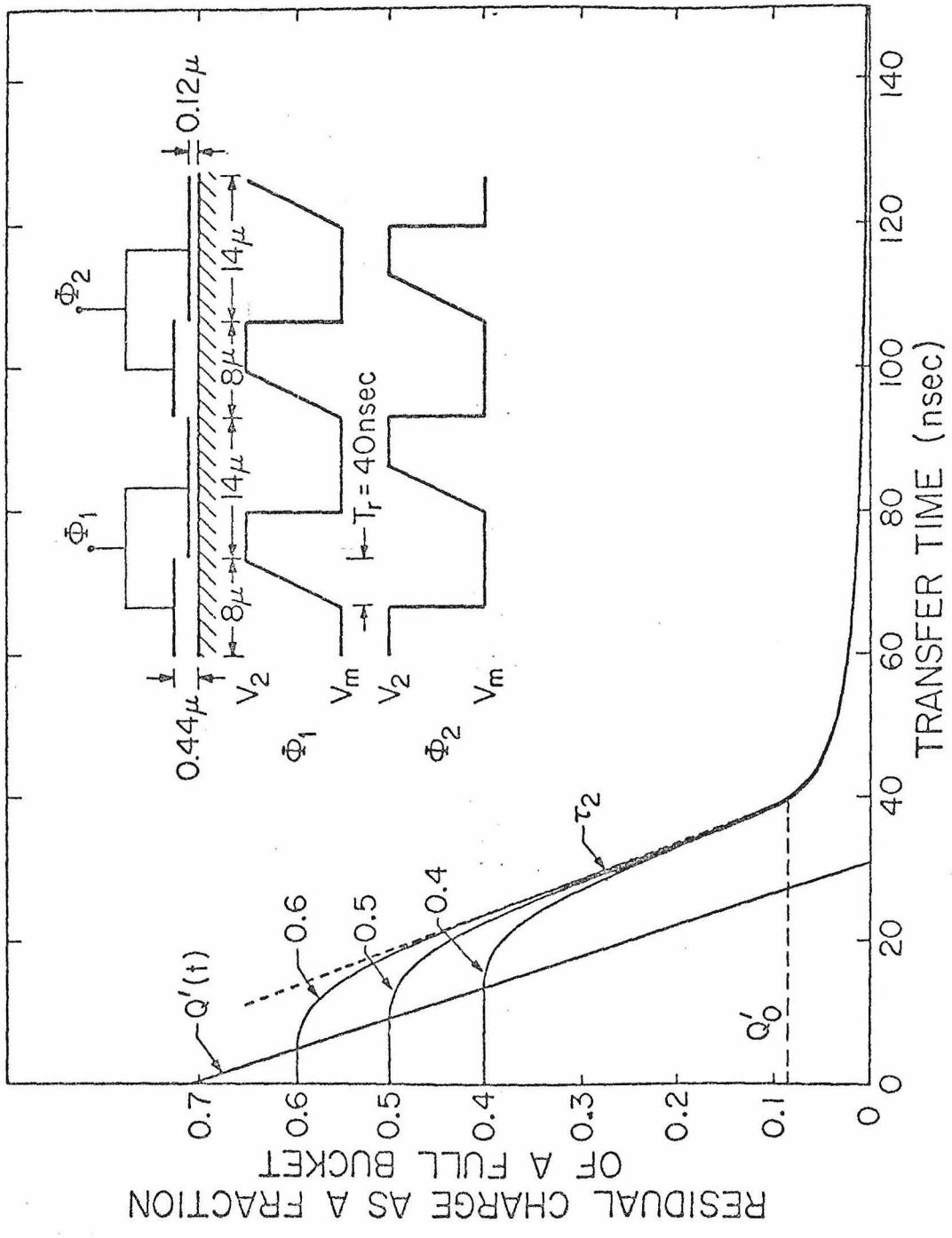
RESIDUAL CHARGE AS A FRACTION OF A FULL BUCKET
TRANSFER TIME (nsec)
Q'(t)
Q'o
τ2
0.6
0.5
0.4
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
20
40
60
80
100
120
140
Φ1
Φ2
0.44μ
0.12μ
8μ
14μ
V2
Vm
Tr = 40nsec

Figure 20.

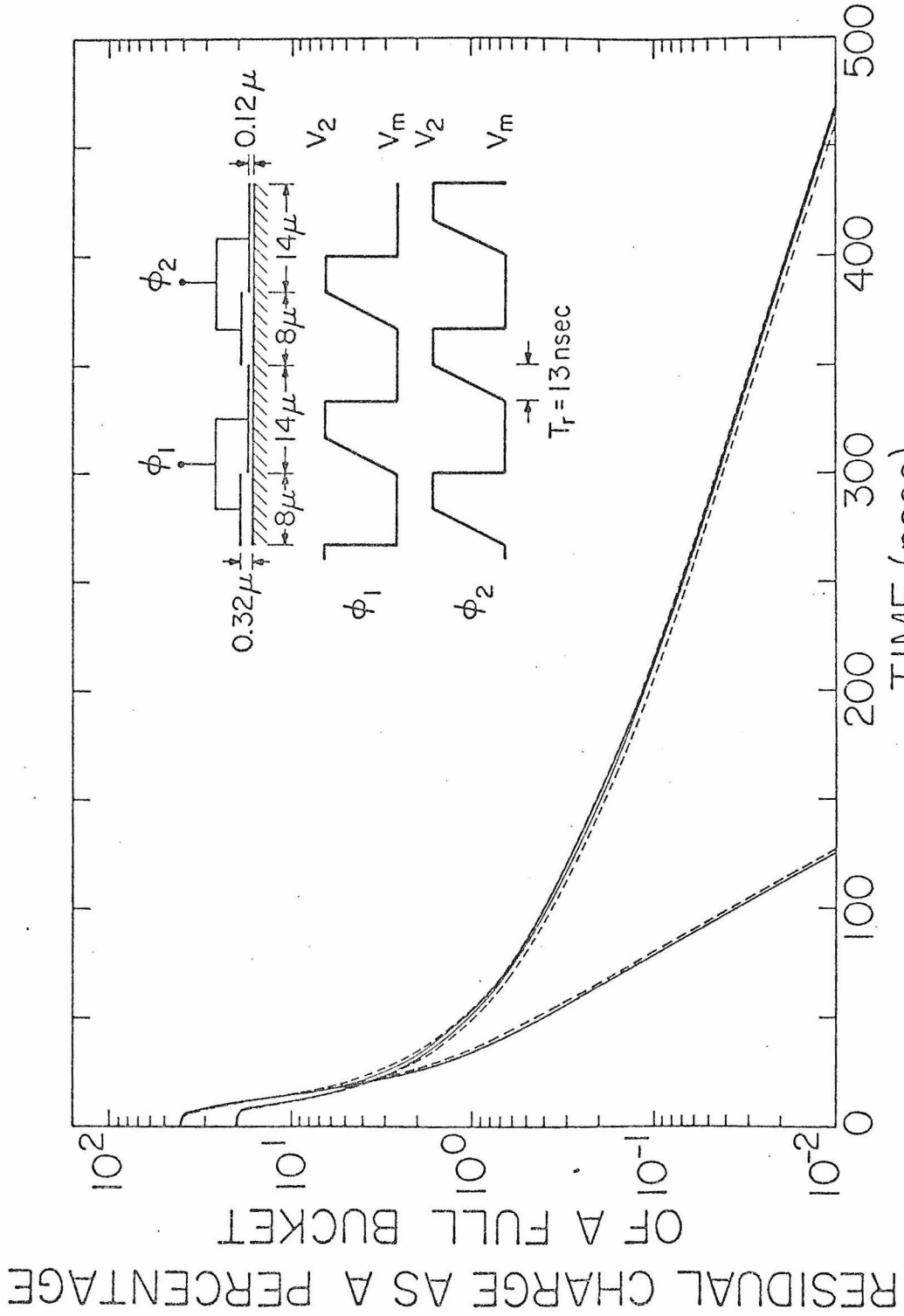
RESIDUAL CHARGE AS A PERCENTAGE OF A FULL BUCKET
10^2
10^1
10^0
10^{-1}
10^{-2}
0
100
200
300
400
500
TIME (nsec)
ϕ_1
ϕ_2
V_2
V_m
V_2
V_m
$T_r = 13$ nsec
0.32μ
8μ
14μ
8μ
14μ
0.12μ

Figure 21.

(ii) The second stage of the charge transfer is limited by the transport of charge across the transfer gate to the next storage gate. The transfer gate acts as a MOS transistor at pinch off, and the storage gate as its source and drain. For maximum rate of discharge in this stage, the gate voltage should be rising with a rate that keeps the surface potential under the storage gate at a value that does not exceed $2\phi_F$ to avoid injection of the signal charge into the substrate where ϕ_F is the Fermi potential of the substrate. Since the surface potential under the gate varies almost linearly with the stored charge and the gate voltage, the maximum rate of charge transfer can be achieved by clocking waveforms with ramps of a slope that matches the saturation current of the transfer gate.

According to the lumped circuit model discussed in Appendix V the decay of the residual charge under the storage gate in this stage can be described by the following equations:

$$\frac{d}{dt}(Q_{St} + Q_{Tr}) = - \frac{\mu C_{Tr} W}{2\ell_{Tr}} \left[2KT(\phi_{mT} - \phi_{mTo}) + (\phi_{mT} - \phi_{mTo})^2 \right] \quad (17a)$$

$$Q_{St} = W\ell_{St} C_{St} (\phi_s - \phi_{so}) \quad , \quad (17b)$$

$$Q_{Tr} = \frac{2}{3} W\ell_{Tr} C_{Tr} (\phi_{mT} - \phi_{mTo}) \quad , \quad (17c)$$

$$\phi_{mT} \cong \phi_s \quad ; \quad \phi_{mT}' \cong \phi_{mTo} \quad , \quad (17d)$$

$$\phi_{so} = B_{1s} V + B_{2s} \quad \text{and} \quad \phi_{mTo} = B_{1T} V_m + B_{2T} \quad , \quad (17e)$$

where V and V_m are the voltages of the first and second phases, driving the source storage gate and transfer gate respectively. B_{1s},

B_{2s}, B_{1T}, and B_{2T} are constants chosen to give the best linear fitting to the relation of the surface potential under the storage and transfer gates to the voltage applied to them. The rest of the notation is similar to that in Eq. (6). For clocking waveforms with ramps or with sufficiently smooth driving functions [12] and for an initial charge Q_o the residual charge under the storage gate is given by

$$Q = Q'(t) + Q''\tanh\left((t-t_1)/\tau_2\right) \quad , \qquad (18a)$$

where

$$Q'(t) = W\ell_{St}C_{St}(\phi_{mTo} - \phi_{so}) \quad , \qquad (18b)$$

$$Q'' = W\ell_{St}C_{St}\sqrt{\frac{2\ell_{Tr}\ell_{St}}{\mu}\frac{C_{St}}{C_{Tr}}\frac{d}{dt}(\phi_{so} - \phi_{mTo})} \quad , \qquad (18c)$$

$$\tau_2 = R\sqrt{\frac{2\ell_{Tr}\ell_{St}}{\mu}\frac{C_{St}}{C_{Tr}}\frac{1}{\frac{d}{dt}(\phi_{so} - \phi_{mTo})}} \quad , \qquad (18d)$$

$$R = 1 + \frac{2}{3}\frac{\ell_{Tr}C_{Tr}}{\ell_{St}C_{St}} \quad . \qquad (18e)$$

t_1 is the time at which the discharge current I starts to flow. The value of $Q'(t)$ is the minimum initial charge under the source storage gate which causes the discharge current I to start at time t. Hence, for a given initial charge Q_o, t_1 is given by

$$Q'(t_1) = Q_o \quad . \qquad (19)$$

It follows directly from Eqs.(18) that for a ramp clocking waveform

the minimum rise time $T_r|_{min}$ of the clocking voltage to prevent injection of the signal charge in the substrate is given by

$$T_r|_{min} = \frac{2\ell_{Tr}\ell_{St}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{B_{ls}(V_2 - V_m)}{(2\phi_F - \phi_{mAo})^2} \quad , \qquad (20)$$

where V_2 and V_m are the resting and minimum voltages of the clock. For $(t-t_1) > \tau_2$ the residual charge under the storage gate decreases according to the waveform of $V(t)$.

The parameters of the device used in the numerical simulation are given below:

$$\left.\begin{array}{ll} \ell_{St} = 13.5 \text{ microns}, & \ell_{Tr} = 7 \text{ microns}, \\ C_{St} = 3.14 \times 10^{-8} \text{F/cm}^2, & B_{ls} = 0.9162, \\ V_m = -15 \text{ volts} & \mu = 200 \text{ cm}^2/\text{volt sec}. \end{array}\right\} \qquad (21)$$

If the oxide thickness under the transfer gate is 3200 Å and $V_2 = -6$ volts and $T_r = 13$ nsec, then $C_{Tr} = 1.45 \times 10^{-8} \text{F/cm}^2$, $T_r|_{min} \cong 5.5$ nsec, and $\tau_2 \cong 6.5$ nsec. If the oxide thickness under the transfer gate is 4400Å and $V_2 = -3$ volts and $T_r = 40$ nsec then $C_{Tr} = 1.32 \times 10^{-8} \text{F/cm}^2$, $T_r|_{min} \cong 21$ nsec and $\tau_2 = 11.5$ nsec.

(iii) In the third stage the clock voltages are nonchanging and the charge transfer is limited by the transport of charge out of the storage gate with an almost perfect sink at its end. The storage gate in this stage is discharged through itself as in the case of the drop clock. The residual charge under the storage gate $Q(t)$ decreases during the first part of this stage hyperbolically with a time constant τ_3.

$$Q(t) = \frac{Q_o'}{1 + \frac{t-t_2}{\tau_3}} \qquad t > t_2 \qquad , \qquad (22)$$

where $\tau_3 = \frac{\ell_{St}^2}{\alpha \frac{Q_o'}{C_{St}\ell_{St}W}\mu}$ and Q_o' is the total charge under the source storage gate when the perfect sink at its end is formed at time t_2. t_2 is approximately [13] equal to T_r and Q_o' is obtained from Eq. (18) with $t = t_2$.

(iv) In the last stage the residual charge decreases exponentially with a time constant that depends on thermal diffusion and fringing fields under the storage gate as discussed above in Eqs. (13), (14), (15), and (16).

3.2.2 Incomplete Charge Transfer Mode:

In the incomplete (or residual) charge transfer mode, a bias charge is deliberately retained under the storage gates at each transfer. This can be achieved by controlling the resting surface potential under the storage gate relative to that under the next transfer gate at the end of the charge transfer process. In the two phase clocking scheme, for a given substrate doping and minimum voltage V_m the oxide thickness under the storage and transfer gates should also be properly chosen for optimum device operation in this mode.

We have simulated numerically the charge transfer for the device shown at the top of Fig. (22) clocked by a two-phase push clock in the incomplete charge transfer mode with a bias charge equivalent to

about one volt. In Fig. (22) we have plotted the transient currents at the beginning and end of the transfer gate and the net current charging the region under the gate. The current at the beginning of the transfer gate starts to increase at about 4.5 nsec reaching a maximum value of about 8 μamp when the clock voltage stops, then the current decreases slowly. The current at the end of the gate has a similar waveform except it is delayed by about 2.5 nsec due to the charge propagation under the gate. We have plotted in Fig. (23) the residual charge under the source storage gate as a fraction of a full bucket versus transfer time for two different initial charges 0.6 and 0.4 of a full bucket. From the plots of the currents at the ends of the gates and the residual charges versus time and the surface charge and surface potential profiles under the gates one can easily identify distinct stages of the charge transfer. The first two stages are similar to the first two stages of the two-phase push clock case described above. The third stage starts when the clock voltage stops at time $t_2 = T_r$ with a residual charge under the source storage gate equal to Q_o'. The charge transfer in the first part of this stage $\left(\frac{Q(t) - Q'}{W\ell_{St}C_{St}} > 2KT\right)$ is similar to the charge transfer in the second stage of the two-phase drop clock discussed above in Eqs. (7), (8), and (9). The residual charge is thus given by

$$Q(t) = \frac{Q_o' - Q'}{1 + \frac{(t-t_2)}{\tau_3}} + Q' \quad , \qquad (23a)$$

where

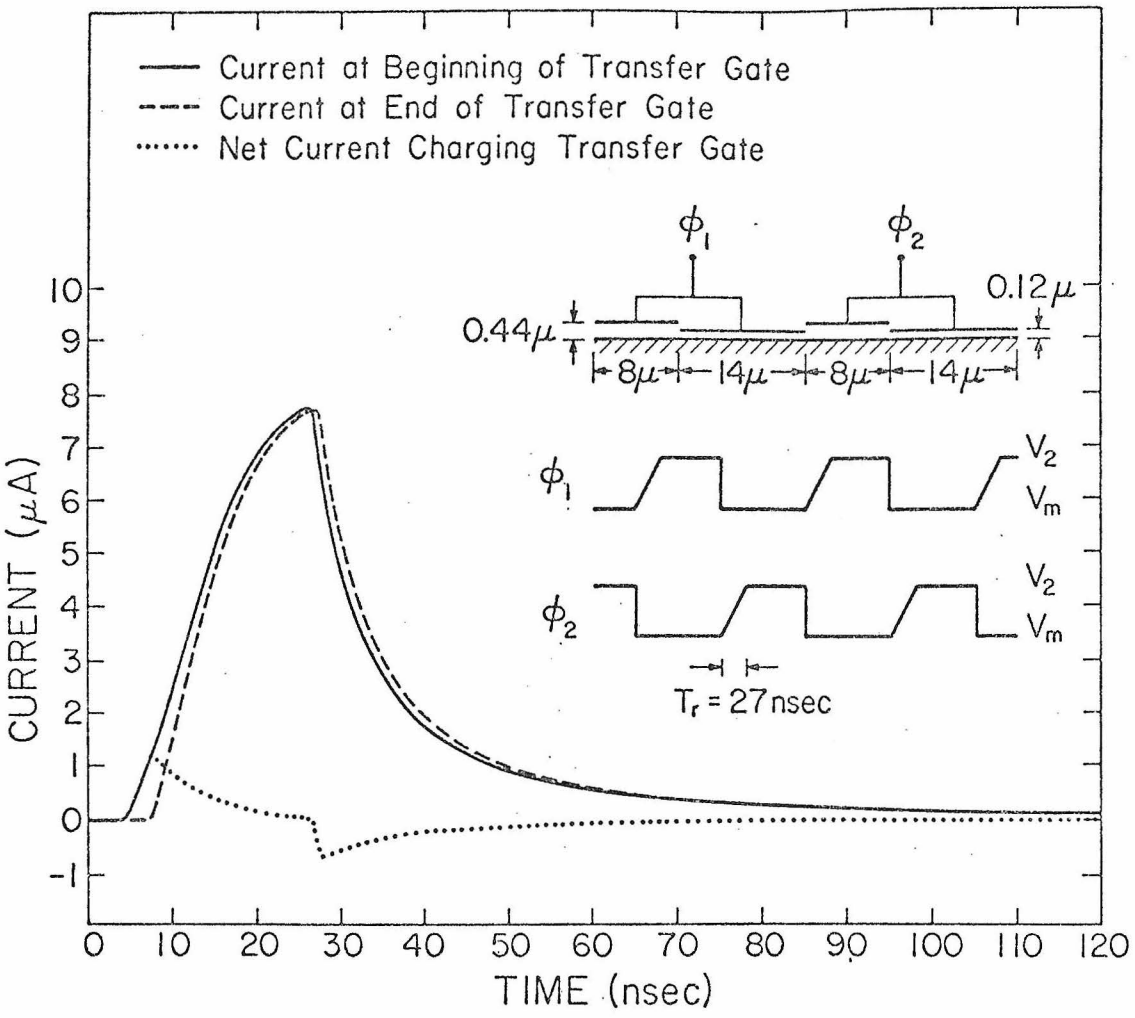
Current at Beginning of Transfer Gate
Current at End of Transfer Gate
Net Current Charging Transfer Gate
ϕ_1
ϕ_2
0.44μ
0.12μ
8μ
14μ
8μ
14μ
ϕ_1
V_2
V_m
ϕ_2
V_2
V_m
T_r = 27nsec
CURRENT (μA)
TIME (nsec)
10
9
8
7
6
5
4
3
2
1
0
-1
0
10
20
30
40
50
60
70
80
90
100
110
120

Figure 22.

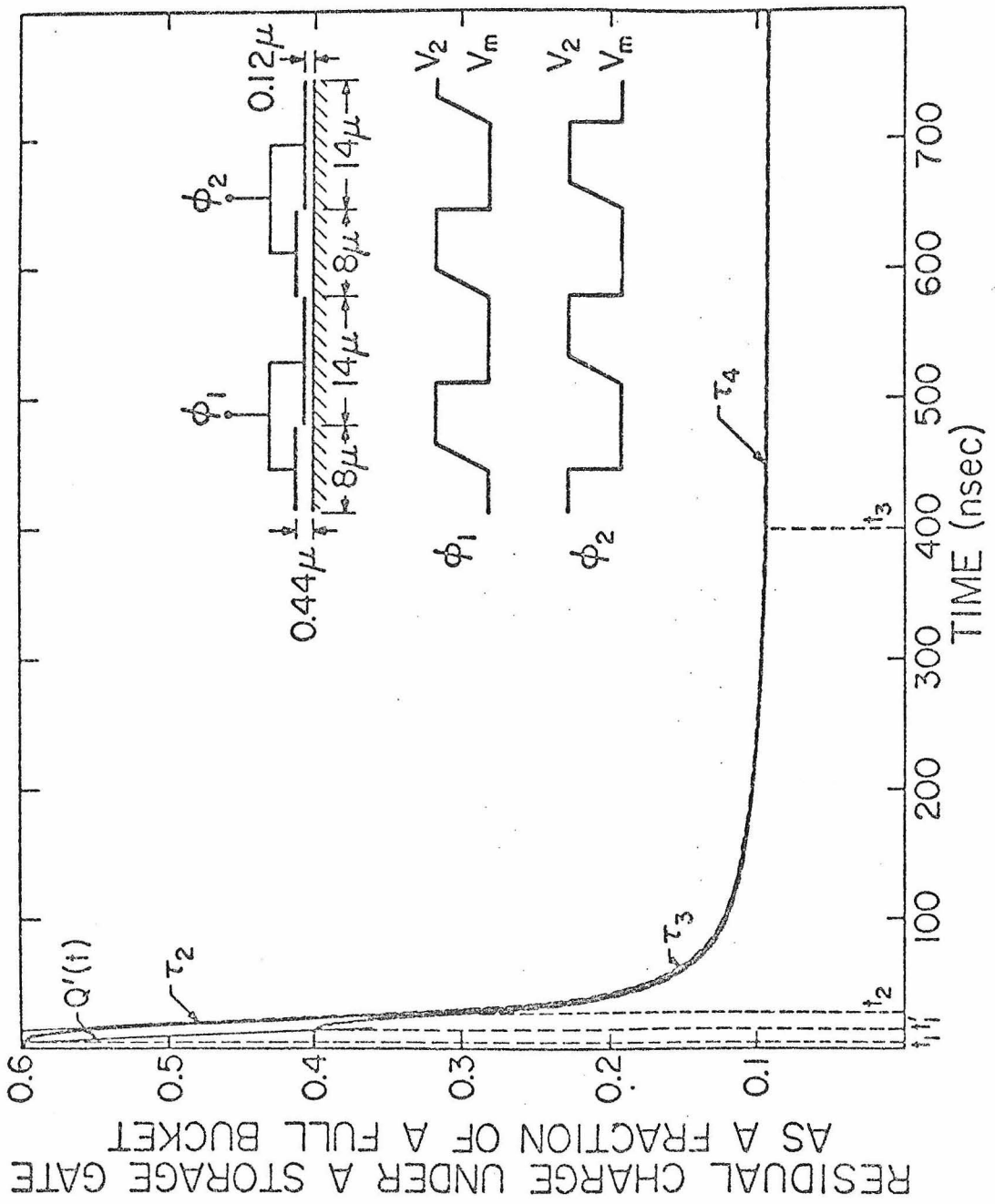
RESIDUAL CHARGE UNDER A STORAGE GATE
AS A FRACTION OF A FULL BUCKET
0.6
0.5
0.4
0.3
0.2
0.1
Q'(t)
τ2
τ3
τ4
t1'
t2
t3
100
200
300
400
500
600
700
TIME (nsec)
φ1
φ2
Vm
V2
0.44μ
0.12μ
8μ
14μ

Figure 23.

$$\tau_3 = \frac{2\ell_{St}\ell_{Tr}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{R}{\frac{Q_o' - Q'}{WC_{St}\ell_{St}}} \quad . \qquad (23b)$$

Q' is the bias charge and is equal to $W\ell_{St}C_{St}(\phi_{mTo} - \phi_{1so})$. This stage ends at time t_3 when

$$Q(t_3) - Q' \simeq WC_{St}\ell_{St} \cdot 2KT \longrightarrow t_3 = t_2 + \frac{\ell_{St}\ell_{Tr}}{D} \frac{C_{St}}{C_{Tr}} \cdot R. \qquad (24)$$

In the last stage of the charge transfer, the surface potential under the storage gate drops below that under the transfer gate. However, the discharge current still continues to flow due to the thermal emission of the carriers under the storage gate over the potential barrier. The mobile charge under the transfer gate also becomes so small that thermal diffusion becomes dominant. Fringing fields under the transfer gate are usually small because the surface potential under the transfer gate and the preceding storage gate are almost equal. The residual charge under the storage gate in this stage decreases logarithmically with time. Using the lumped circuit described in Appendix V the charge transfer in the incomplete charge transfer mode is described by the following equations:

$$\frac{d}{dt}(Q_{St} + Q_{Tr}) = -\frac{\mu C_{Tr} W}{2\ell_{Tr}} \left[2KT(\phi_{mT} - \phi_{mTo}) + (\phi_{mT} - \phi_{mTo})^2\right] \qquad (25a)$$

$$Q_{St} = W\ell_{St}C_{St}(\phi_{1s} - \phi_{1so}) \qquad (25b)$$

$$Q_{Tr} = \frac{2}{3} W\ell_{Tr}C_{Tr}(\phi_{mT} - \phi_{mTo}) \frac{\left[(\phi_{mT} - \phi_{mTo}) + \frac{3}{2} KT\right]}{\left[(\phi_{mT} - \phi_{mTo}) + 2KT\right]} \qquad (25c)$$

$$C_{Tr}(\phi_{mT} - \phi_{mTo}) = C_{St}(\phi_{ls} - \phi_{lso}) \exp -(\phi_{mT} - \phi_{ls})/KT); \; \phi_{mT}' = \phi_{mTo} \tag{25d}$$

$$\left[1 + \frac{KT}{\phi_{mT} - \phi_{mTo}}\right] \cdot \frac{d}{dt}(\phi_{mT} - \phi_{mTo}) = \left[1 + \frac{KT}{\phi_{ls} - \phi_{lso}}\right] + \frac{d}{dt}(\phi_{ls} - \phi_{lso}) + \frac{d}{dt}(\phi_{lso} - \phi_{mTo}) \tag{25e}$$

Assuming a sufficiently large bias charge $(Q' >> KT\ W\ell_{St}C_{St})$ and taking $(\phi_{mT} + KT)(\phi_{mT} + 3KT) \cong (\phi_{mT} + 2KT)^2$, then the above equations reduce to

$$-\frac{\mu C_{Tr} W}{2}\left[(\phi_{mT} - \phi_{mTo})^2 + 2KT(\phi_{mT} - \phi_{mTo})\right] = \left[W\ell_{St}C_{St}\left(1 + \frac{KT}{\phi_{mT} - \phi_{mTo}}\right) + \frac{2}{3} W\ell_{Tr}C_{Tr}\right] \frac{d}{dt}(\phi_{mT} - \phi_{mTo}) . \tag{26}$$

For $(\phi_{mT} - \phi_{mTo}) < KT$ the residual charge under the source storage gate is given by [14]

$$Q(t) = Q' - KT\ W\ell_{St}C_{St}\ \ell n\left[1 + (t-t_3)/\tau_4\right] \tag{27a}$$

where

$$\tau_4 = \frac{\ell_{Tr}\ell_{St}}{2D}\frac{C_{St}}{C_{Tr}} . \tag{27b}$$

If $t > t_4 = t_3 + \tau_4 \exp(Q'/C_{St}\, W\ell_{St}\, KT)$, Eq. (25) reduces to

$$Q(t) \sim C_{St}\, W\ell_{St}\, KT \exp -\left((t-t_4)/\tau_5\right) \quad , \qquad (28a)$$

where

$$\tau_5 = \frac{\ell_{Tr}\ell_{St}}{D} \exp\left((\phi_{mTo} - \phi_{1so})/KT\right) \quad . \qquad (28b)$$

However for a bias charge equivalent to one volt t_4 and τ_5 are larger than the interface storage time[19] of the best thermally grown oxide and hence that stage will never be reached practically. If fringing fields under the transfer gate are appreciable for a closer spacing device or a lower substrate doping, then the above relations still hold except $\frac{D}{\ell_{Tr}}$ is replaced by $\left(\frac{D}{\ell_{Tr}} + \mu\bar{E}\right)$ where $\bar{E}$ is the average fringing field under the transfer gate.

When a static two-phase clock is used to operate the device in the incomplete charge transfer, the two first stages of the charge transfer are similar to the two first stages of the static drop clock in the complete charge transfer mode. However in the last stage, the residual charge in the incomplete charge transfer mode decreases logarithmically according to Eq. (27).

3.3 Four-Phase Clocking Scheme

In the overlapped gates charge coupled devices, four-phases may be used to control the storage and transfer of charge along the interface. Since each gate electrode is driven by a separate phase, more flexibility in operating the device is expected. With four clocking phases the

polysilicon electrodes can be used to store the signal charge and the aluminum electrodes to control the transfer and storage process, or both the polysilicon and aluminum gates can be used as storage sites. The latter method requires four transfers per bit and the aluminum electrode should have the same areas as the polysilicon electrodes, but the former method requires two transfers per bit and the aluminum electrodes can have a smaller area. We will consider the first method as it requires less area per bit and results in less signal degradation due to incomplete free charge transfer.

3.3.1 Complete Charge Transfer Mode:

(A) Drop Clock. With the four-phase drop clock, the minimum and resting voltages (V_m' and V_2') of the clock phases driving the transfer gates can be independently controlled whatever is the oxide thickness under the transfer electrodes for operation in the complete charge transfer mode. The stages of the charge transfer process are similar to the two-phase drop clocks. So increasing the complexity of the clock from two-phases to four-phases with drop clock does not improve the performance of the device.

(B) Push Clock. Push clocks take full advantage of the more flexible control of the storage and transfer of charge with the four-phases of the clock. At the top of Fig. (24), we show the device dimensions and the clocking waveforms we have used in our computer simulation of the four-phase push clock. In Fig. (25) we have plotted the surface potential and surface charge density profiles during the charge transfer process.

Since with four clocking phases the preceding transfer gate can be turned off by the resting voltage V_2', the maximum signal charge that can be stored under the storage gate with its voltage equal to V_m can be almost a full bucket. In the two-phase clocking scheme, each set of transfer and storage gates is driven by the same phase of the clock so the preceding transfer gate is turned on when the storage gate is turned on. Hence the maximum charge that can be stored with four-phase clock is larger than with two-phase clock for the same clock voltage amplitude. To transfer the charge for example, from under the first storage gate to the second one, ϕ_{2A} and ϕ_{2S} drops to V_m to turn on heavily the second transfer and storage gates. Then ϕ_{1S} increases to push the charge from under the first storage gate to the adjacent gates. Then ϕ_{2A} increases to push the charge to the next storage gate. As ϕ_{2A} reaches the resting voltage, V_2', the charge transfer ends and some of the residual charge under the transfer gate spills back to the preceding storage gate. The rate of rise of ϕ_{2A} should be sufficiently slow so that the amount of charge under the transfer gate which spills back to the preceding storage gate is small. Therefore, the rise time T_r of the transfer gate clock should increase with the increase of the clock bit time.

In Fig. (24) we have plotted the transient currents at the beginning and end of the transfer gate. The current at the beginning of the transfer gate increases very rapidly with a rate that depends on the fall time of the clock. It reaches a maximum value of about 70 μamps, at 5 nsec when the transfer gate is completely on. Then it drops

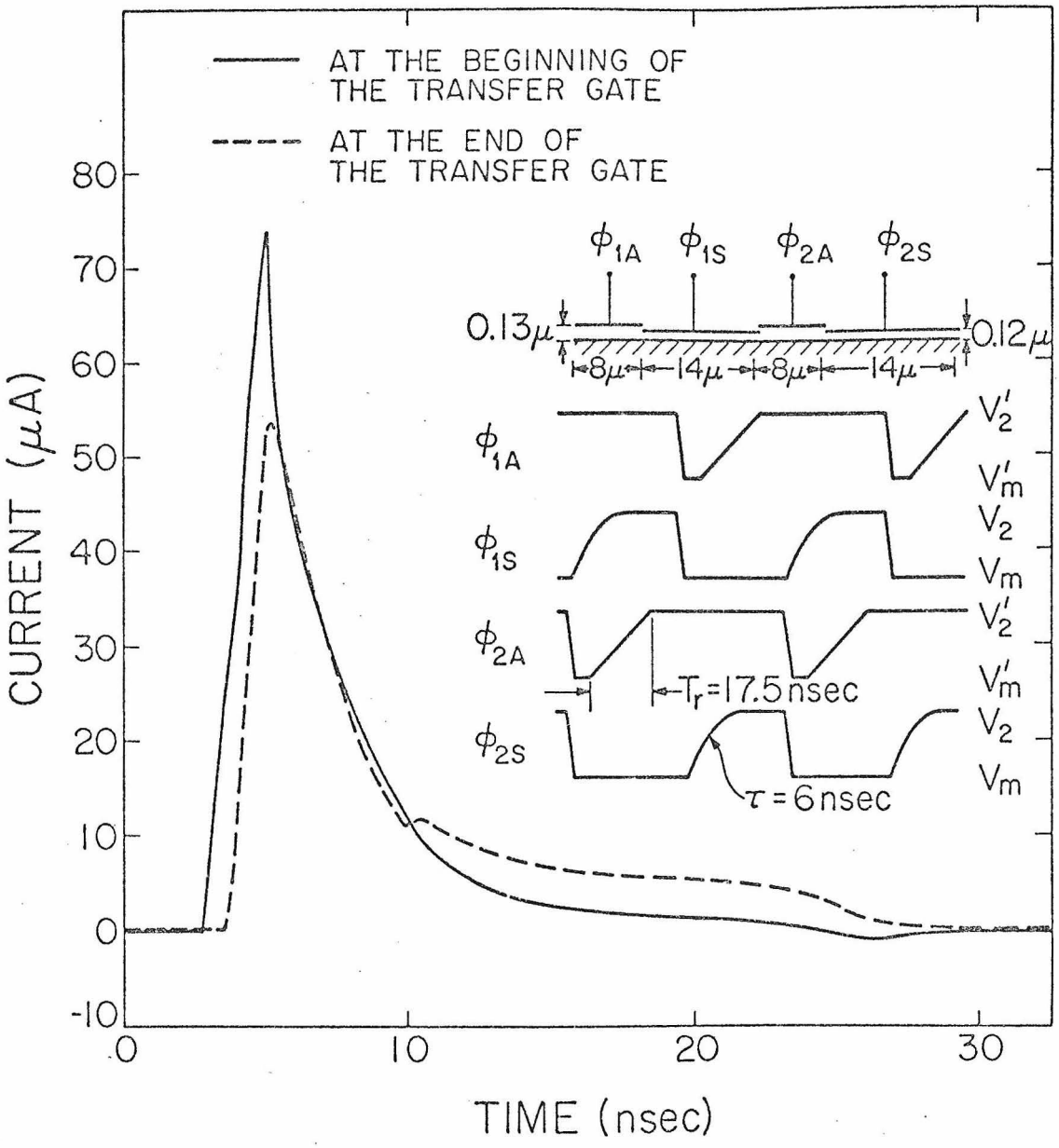
AT THE BEGINNING OF
THE TRANSFER GATE
AT THE END OF
THE TRANSFER GATE
CURRENT (μA)
TIME (nsec)
80
70
60
50
40
30
20
10
0
-10
0
10
20
30
ϕ_{1A} ϕ_{1S} ϕ_{2A} ϕ_{2S}
0.13μ
0.12μ
8μ 14μ 8μ 14μ
V_2'
V_m'
V_2
V_m
T_r=17.5nsec
τ = 6nsec

Figure 24.

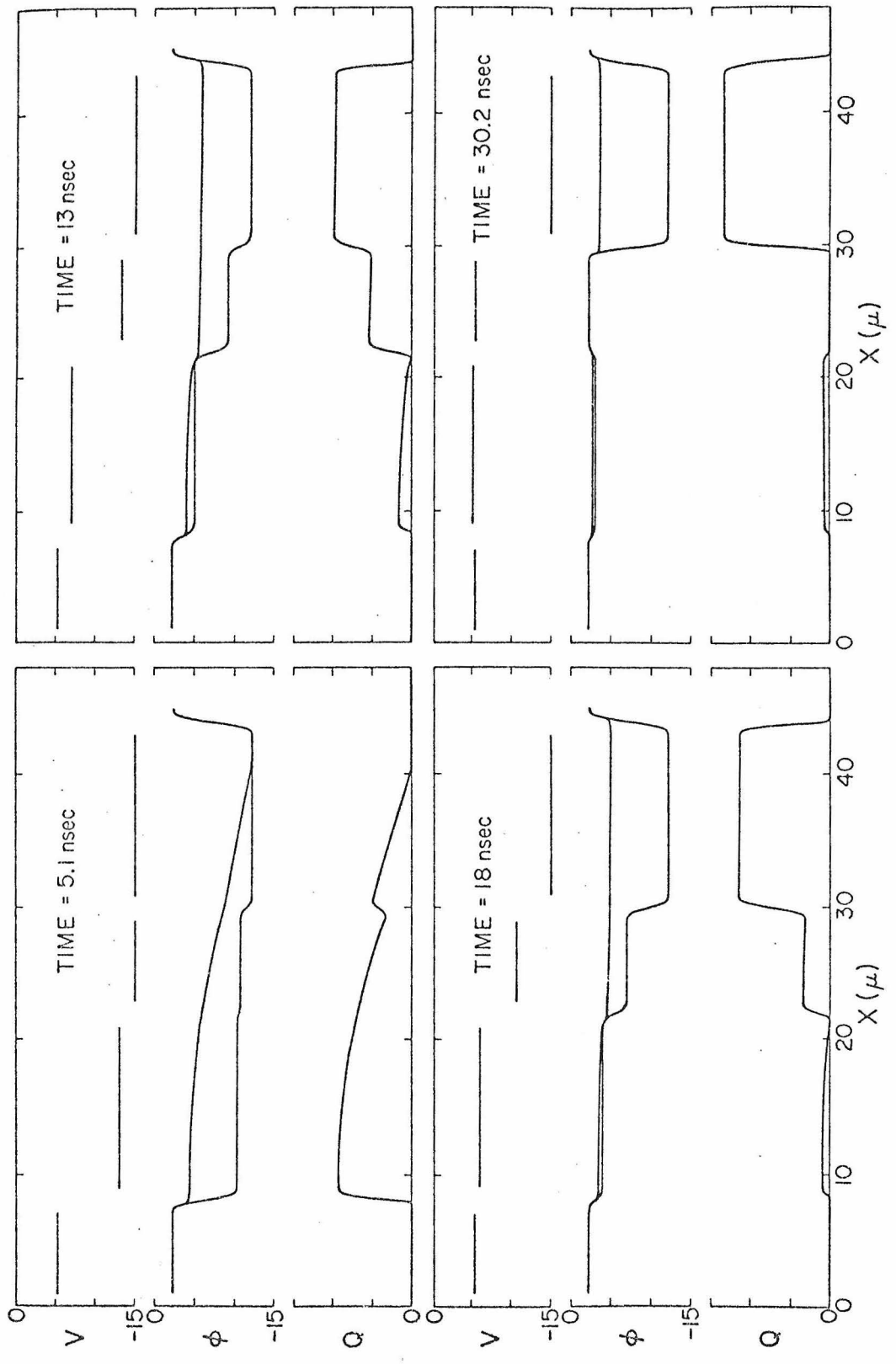
TIME = 5.1 nsec
TIME = 13 nsec
TIME = 18 nsec
TIME = 30.2 nsec
V
φ
Q
0
-15
10
20
30
40
X (μ)

Figure 25.

rapidly reversing its sign when some of the residual charge under the transfer gate spills back to the preceding storage gate. The current at the end of the transfer gate has a similar waveform except it is delayed by 1 nsec due to charge propagation across the transfer gate. The second small peak at 10 nsec occurs when the transfer gate voltage starts to increase to push the charge to the next storage gate. In Fig. (26) we have plotted the residual charge under the storage gate for two different initial charges 0.75 and 0.35 of a full bucket. With the four-phase push clock, more charge can be stored and much faster rates of charge transfer in the first stages of the transfer process can be achieved since the transfer gates can be controlled independently. However, in the last stages of the charge transfer process, the residual charge decreases exponentially with a time constant that depends on thermal diffusion and fringing fields as with the two-phase clocks.

3.3.2 Incomplete Charge Transfer Mode:

In the incomplete charge transfer mode, a bias charge is left under the storage gate at each transfer. Whether push or drop four-phase clocks are used, the first stages of the charge transfer will be similar to those in the complete charge transfer mode. But in the last stage of the charge transfer, the residual charge under the storage gate does not decrease exponentially as in the complete charge transfer mode, but it decreases logarithmically with a much slower rate.

3.4 Signal Degradation

Due to the incomplete transfer of charge from one storage site to

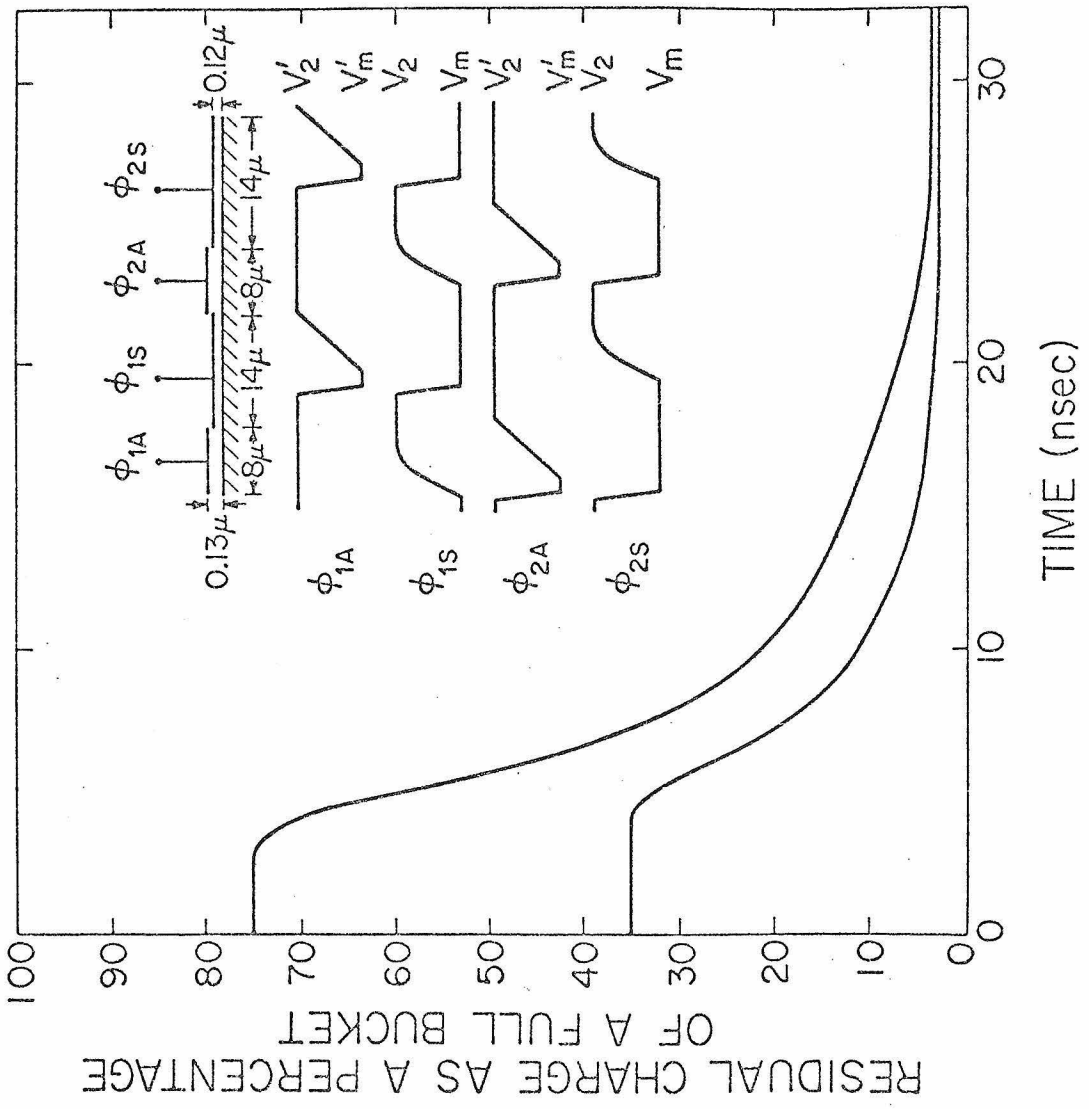
RESIDUAL CHARGE AS A PERCENTAGE
OF A FULL BUCKET
TIME (nsec)
0
10
20
30
40
50
60
70
80
90
100
ϕ_{1A}
ϕ_{1S}
ϕ_{2A}
ϕ_{2S}
V_2'
V_m'
V_2
V_m
0.13μ
8μ
14μ
0.12μ

Figure 26.

another the signal stored and transferred along the device will be degraded.[15] The charge transfer characteristics presented above show that for any finite transfer time there is a finite residual charge under the original storage gate. In Fig. (27) we have plotted the residual charge Q_r due to incomplete free charge transfer versus the initial charge Q_i at various transfer times. The saturation characteristics of these plots are due to the strong nonlinearity inherent in the transport dynamics. The plots of the net residual charge due to trapping in interface states versus the initial charge show also the same saturation shape as will be shown in Chapter 4. For larger charge the residual charge tends to be less dependent on the initial charge. This saturation characteristic indicates that the signal degradation due to incomplete free charge transfer and trapping in interface states can be considerably reduced by using a circulating background charge or a "fat zero" to represent the zero signal.

The net charge loss from a charge packet in one transfer event is the difference between the residual charge it lost in the original storage site and the residual charge it gained from the preceding charge packet. From Fig. (27), it is clear that for digital signals the worst bit pattern is when a "one bit" follows a long series of "zero bits" or when a "zero bit" follows a long series of "one bits". Let ΔQ be the difference in the residual charge due to a "one bit" and a "zero bit" resulting from incomplete free charge transfer and trapping in the interface states. If $Q_{in}^{(1)}$ and $Q_{in}^{(o)}$ are the input charges which represent the one and zero bit, then the worst case output charges

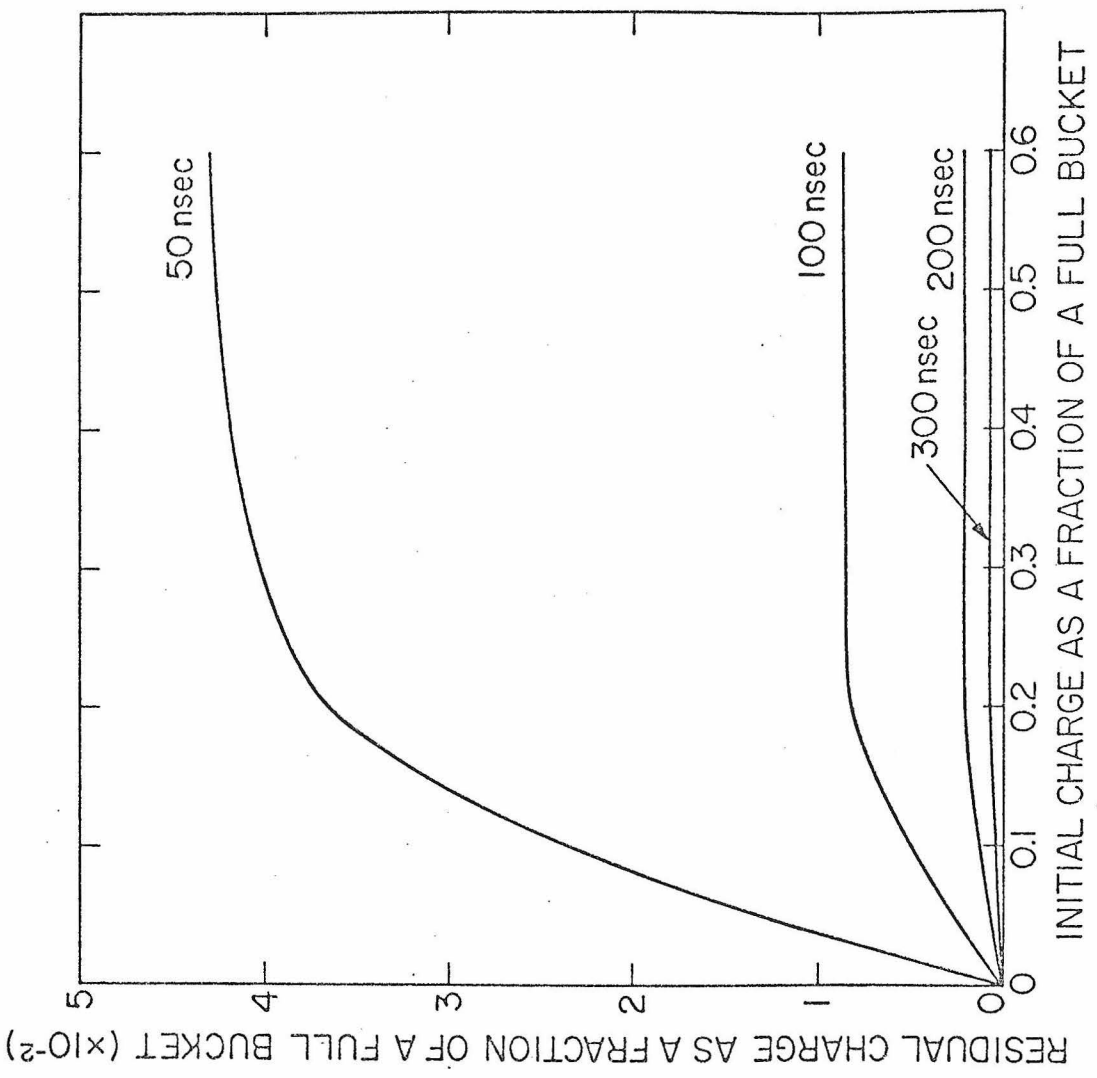
RESIDUAL CHARGE AS A FRACTION OF A FULL BUCKET (×10-2)
INITIAL CHARGE AS A FRACTION OF A FULL BUCKET
50 nsec
100 nsec
200 nsec
300 nsec
0
1
2
3
4
5
0
0.1
0.2
0.3
0.4
0.5
0.6

Figure 27.

after n transfer are given approximately by

$$Q_{out}^{(1)} = Q_{in}^{(1)} - n\Delta Q \quad ,$$
$$Q_{out}^{(o)} = Q_{in}^{(o)} - n\Delta Q \quad , \tag{29}$$

and the output signal is given by

$$Q_{out}^{(1)} - Q_{out}^{(o)} = Q_{in}^{(1)} - Q_{in}^{(o)} - 2\, n\Delta Q \quad . \tag{30}$$

Due to the saturation characteristics in Fig. (27), there exists an optimum fat zero charge $Q_{in}^{(o)}\Big|_{opt}$ which results in maximum output signal and is defined by

$$2n \frac{d}{dQ_{in}^{(o)}} (\Delta Q) + 1 = 0 \quad . \tag{31}$$

The shape of the saturation characteristics in Fig. (27) indicates that the optimum fat zero charge $Q_{in}^{(o)}\Big|_{opt}$ increases by increasing the clock frequency and the number of stages n of the charge coupled register and is independent of the size of the one bit.

The signal degradation due to incomplete charge transfer is best described by the signal degradation factor ε which is defined by

$$\varepsilon = \frac{\Delta Q_r}{\Delta Q_i} \quad . \tag{32}$$

where ΔQ_r is the difference in the residual charge Q_r due to a difference ΔQ_i in the initial charge Q_i. For small ΔQ_i, ε tends to its small signal value α, where

$$\alpha = \frac{dQ_r}{dQ_i} \quad . \tag{33}$$

In Figs. (28), (39), and (30) we have plotted the signal degradation factor due to incomplete free charge transfer versus transfer time for the drop and push two-phase clock in the complete charge transfer mode and for the two-phase push clock in the incomplete (or residual) charge transfer mode respectively. The signal degradation of the incomplete free charge transfer is due to an intrinsic transfer rate and due to the modulation of the device parameters by the signal charge being transferred. The intrinsic transfer rate is due to the finite carrier mobility and finite transfer time. The modulation effects are due to the dependence of the effective lengths of the gates, the effective capacitances per unit area and fringing fields under the storage and transfer gates on the signal charge being transferred. In Fig. (28), (29), and (30) the full line curves are the signal degradation due to the intrinsic transfer rate and the device parameters modulations, and the dashed line curves are the signal degradation due to the intrinsic transfer rate only. In the complete charge transfer mode (or CCD mode) the signal degradation due to incomplete free charge transfer decreases exponentially with time. But in the incomplete transfer mode (or bucket brigade mode), the signal degradation tends to a constant value at low clock frequency due to transfer gate length modulation and barrier height modulation (which modulates the residual or bias charge under the storage gates).

In order to compare the performance of charge coupled devices with push and drop clocks, we have plotted in Fig. (31) the signal degradation versus bit time for a two-phase push and drop clock. The device

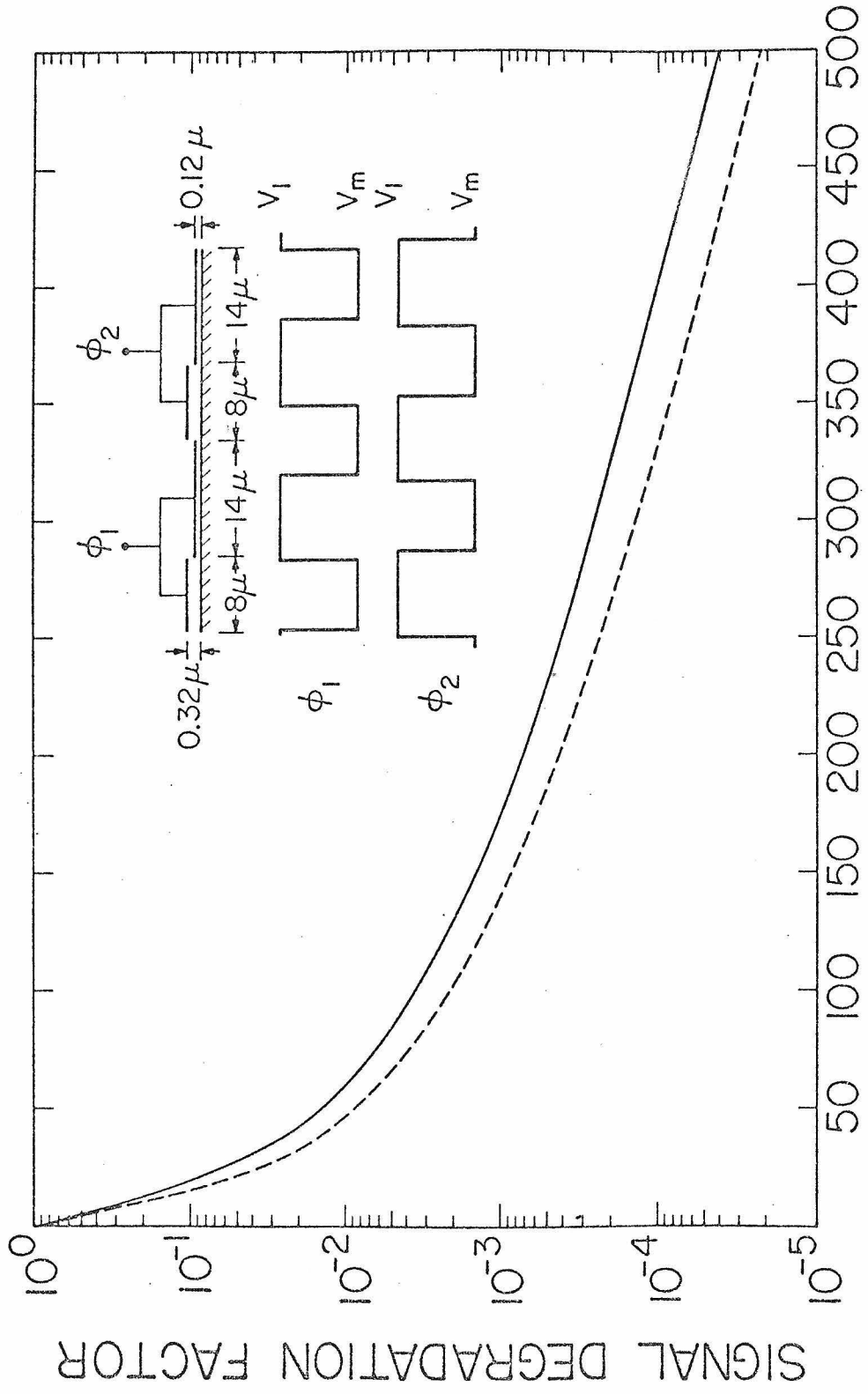
SIGNAL DEGRADATION FACTOR
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
50 100 150 200 250 300 350 400 450 500
TRANSFER TIME (nsec)
ϕ_1
ϕ_2
V_1
V_m
V_1
V_m
0.32μ
8μ
14μ
8μ
14μ
0.12μ

Figure 28.

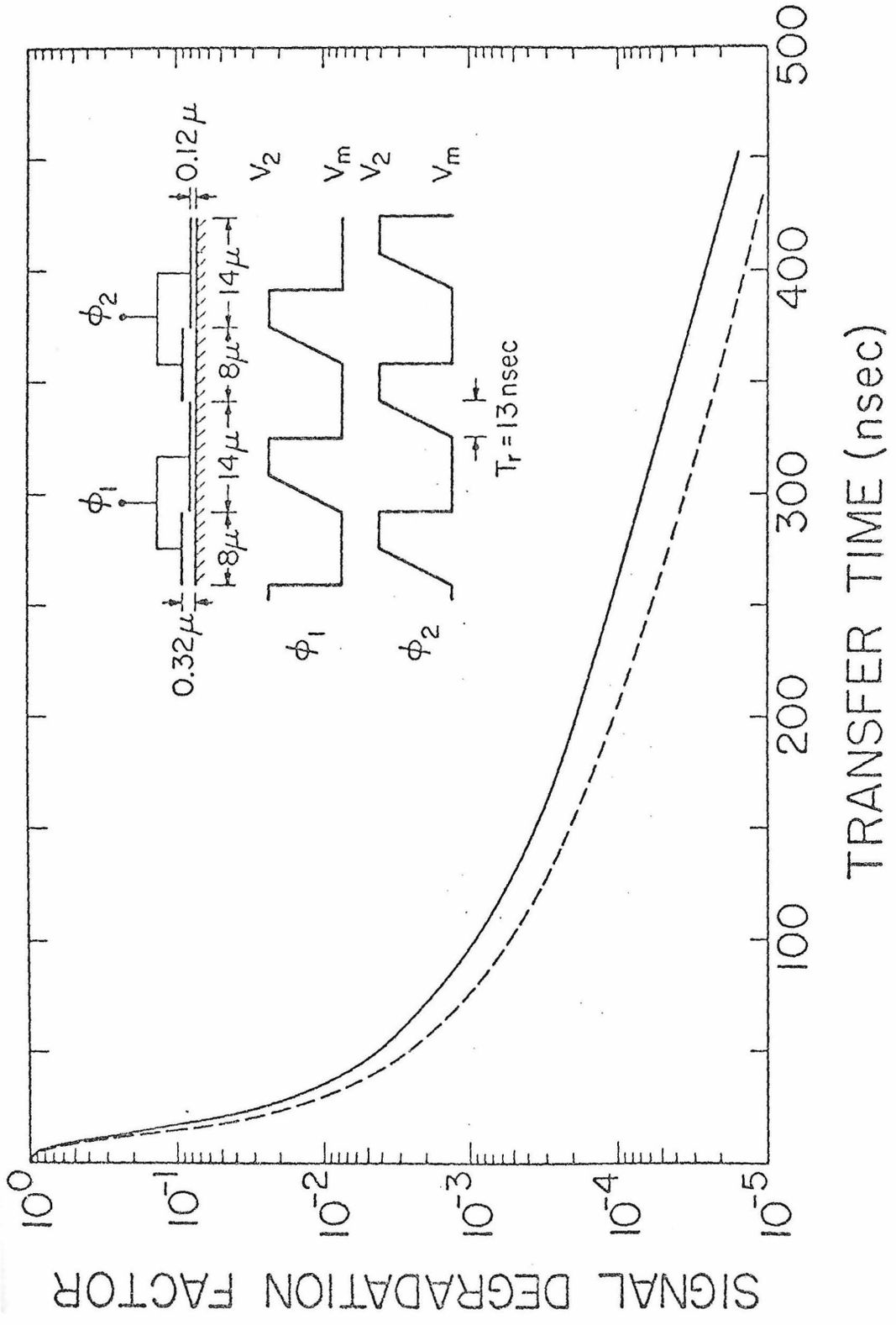
SIGNAL DEGRADATION FACTOR
TRANSFER TIME (nsec)
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
100
200
300
400
500
ϕ_1
ϕ_2
0.32μ
8μ
14μ
8μ
14μ
0.12μ
V_2
V_m
V_2
V_m
T_r = 13 nsec

Figure 29.

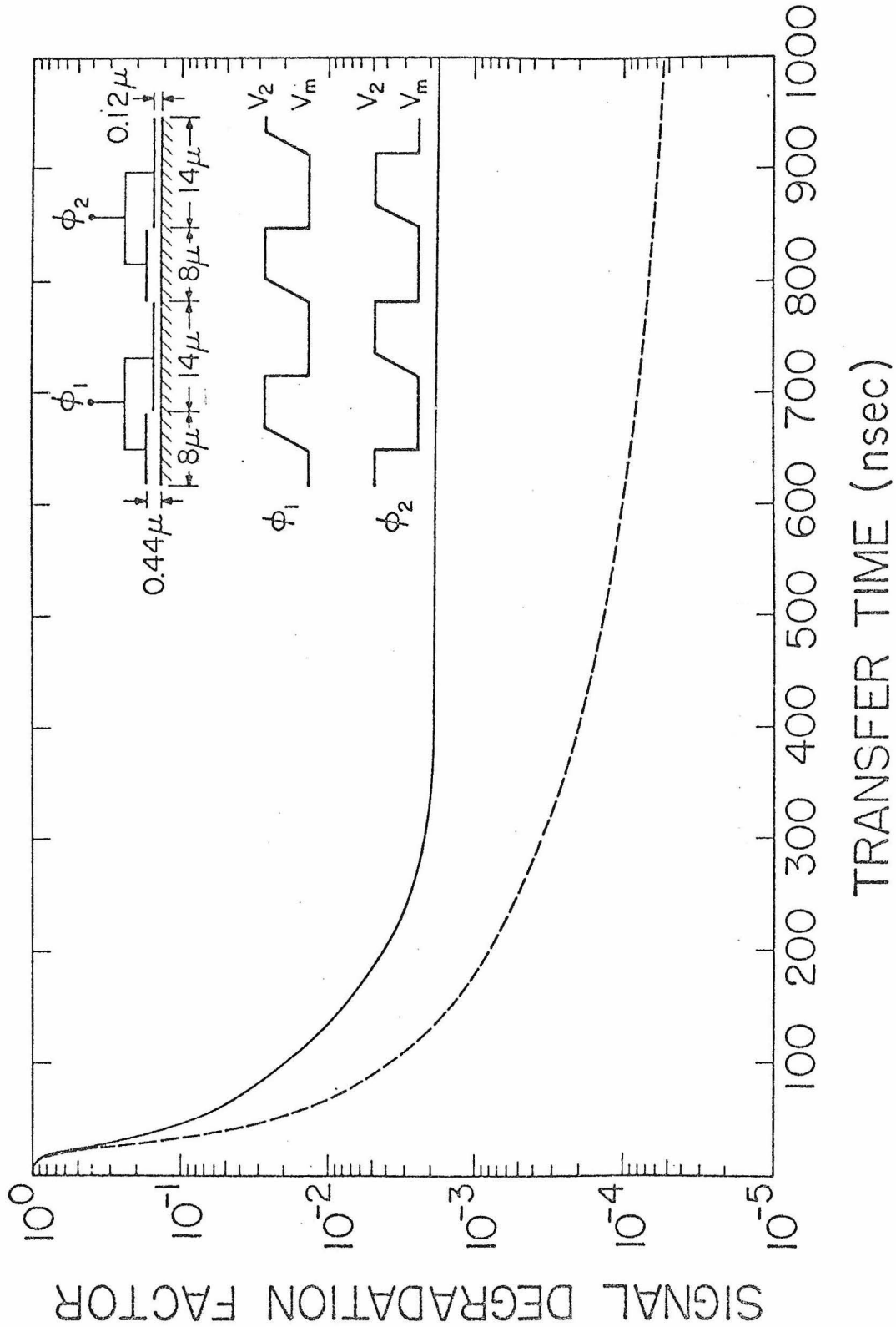
SIGNAL DEGRADATION FACTOR
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
100 200 300 400 500 600 700 800 900 1000
TRANSFER TIME (nsec)
ϕ_1
ϕ_2
V_2
V_m
V_2
V_m
ϕ_1
ϕ_2
0.44μ
8μ
14μ
8μ
14μ
0.12μ

Figure 30.

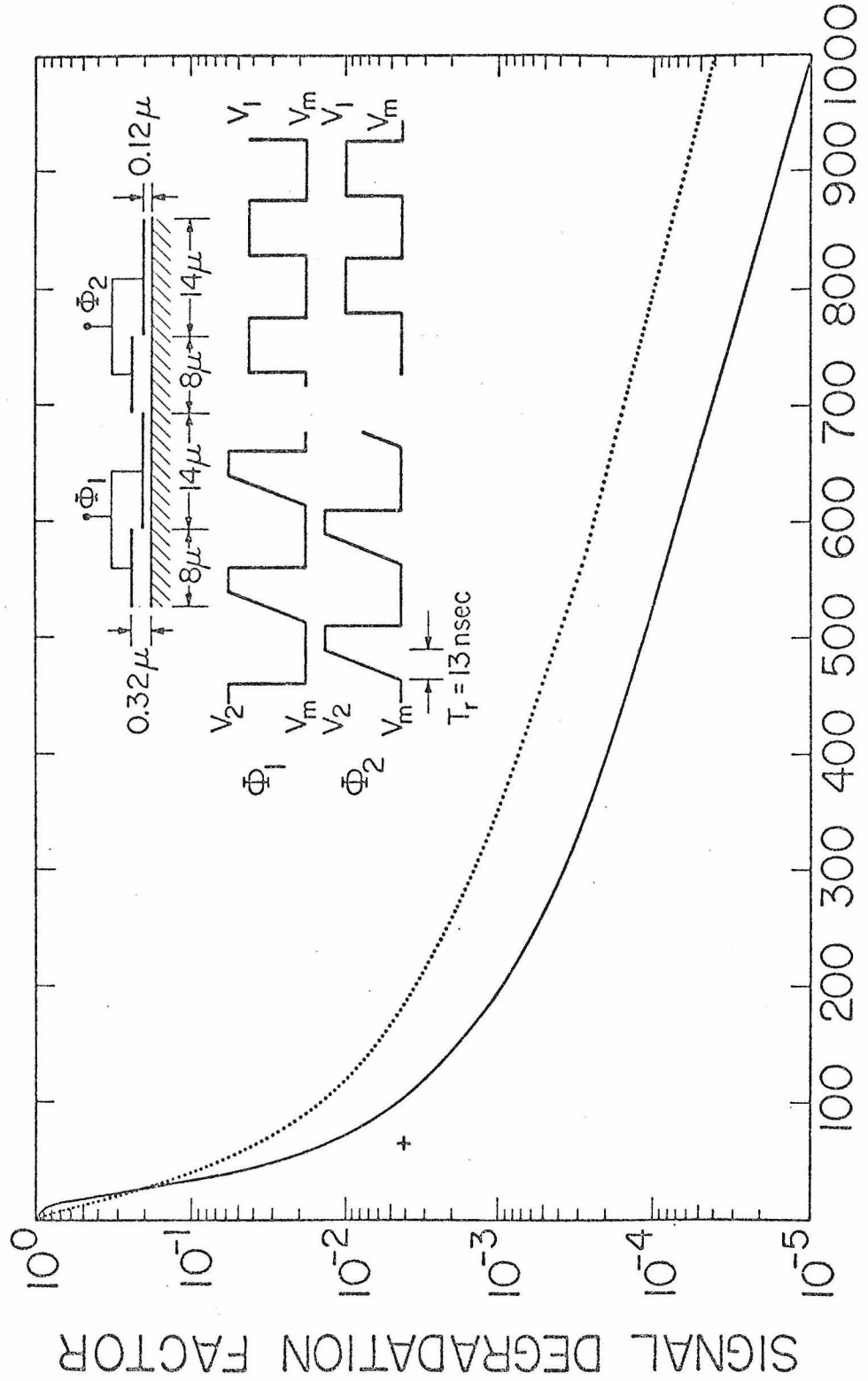
SIGNAL DEGRADATION FACTOR
BIT TIME (nsec)
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
100 200 300 400 500 600 700 800 900 1000
Φ_1
Φ_2
V_1
V_m
V_2
$T_r = 13$ nsec
0.32μ
0.12μ
8μ
14μ

Figure 31.

dimensions and the clocking waveforms are shown at the top of Fig. (31). We have chosen a suitable background charge q_o to represent a "fat zero" and a larger charge q_s to represent the signal or one bit, as would be used for example to represent the zero and one bit in a digital serial memory. It is clear that the transfer efficiency is higher for the push clock. The improvement in transfer efficiency is due mainly to an important property of push clocks: The differences in the charge transfer characteristics and the mobile charge profiles under the CCD gates depending on whether a large or small charge is being transferred are minimized with push clocks. With a push clock the transfer of charge does not start until the surface potential under the initial storage gate is larger than that under the next transfer gate. This condition occurs earlier or later in the transfer cycle depending on whether more or less charge was originally stored. Thus provided the zero signal or zero bit is represented by a background charge, the charge profiles under the gates during the remainder of the transfer cycle are almost independent of when the actual movement of charge began: That is they are independent of the initial charge to be transferred. Hence the residual chargesafter each transfer with push clocks are almost independent of the initial charges. Therefore the signal degradation due to incomplete free charge transfer at high frequency is less when the device is operated with push clocks than when it is operated with drop clocks.[16] In Chapter 5, we will show that the signal degradation due to trapping in the interface states, which is dominant at low and moderate clock frequency, is also reduced by using push clocks instead of drop clocks.

In Fig. (31) we show also the signal degradation for the four-phase push described in section (3.3.1 B). It is clear that increasing the clocking scheme complexity from two-phase to four-phase improves the performance of the device at high frequency. This is because increasing the clocking scheme complexity allows a better control of the storage and transfer of the signal charge. This results also in a larger signal dynamic range and larger signal to noise ratio.

Chapter 4

TRAPPING IN THE INTERFACE STATES

The incomplete charge transfer due to trapping in interface states at the semiconductor-oxide interface imposes limitations on the performance of charge coupled devices at moderate and low frequencies, where the incomplete free charge transfer is very small as shown in the previous chapter. In this chapter we use a simple and accurate model to study the incomplete charge transfer due to trapping in interface states and show its dependence on frequency, device parameters, dimensions, and clocking waveforms.

4.1 Incomplete Charge Transfer Due to Trapping in Interface States

If a voltage is applied to one of the storage electrodes of the charge couple device, a potential well is created at the interface, where signal charge can be stored. Some of this charge will be trapped in interface states. During the first stages of the transfer of charge to the next storage site, some carriers will also be trapped in interface states under the transfer gates. In the last stages of the transfer process, the relatively large fringing fields under the transfer gates sweep out the mobile carriers very rapidly and the interface states then start to emit the captured carriers. According to the Shockley-Read-Hall rate equations,[21] the emission time constant τ_e of the interface states varies exponentially with their energy level relative to the band edge. If the emission time constant of the interface states in a given energy range is smaller than the transfer

time, then most of the trapped carriers in these states are emitted and can join the main packet. Interface states with an emission time constant equal or larger than the transfer time will emit only a fraction of the trapped carriers. Since the storage gate is longer and has a thinner oxide than the transfer gate, the fringing fields under it are much smaller than under the transfer gate. The residual charge under the storage gate, in the last stages of the charge transfer process, decreases exponentially with a time constant that depends on thermal diffusion and the small fringing fields. Interface states continue to capture carriers from the residual signal charge until the residual charge becomes so small that emission from the traps becomes dominant. The non-emitted trapped carriers under the storage gate and the transfer gate are thus lost from the signal charge and will be emitted in the succeeding packets. If the next signal samples do not contain any charge, the interface states continue to emit the captured carriers until a signal sample containing charge passes. Then the empty interface state fill by capturing carriers from that signal sample. After its transfer, the trapped carriers are emitted and so on.

The charge captured by interface states from a large charge packet passing through the device is larger than the charge emitted into that packet, unless it has been preceded by an equal or larger charge packet. But the charge captured by interface states from a small charge packet passing through the device is smaller than the charge emitted into that packet, unless it has been preceded by an equal or smaller charge packet. Thus the interaction of the signal charge with the

interface states results in incomplete transfer of charge from one storage site to another and imposes limitations on the performance of the overlapping gates charge coupled devices.

The signal degradation due to the trapping of carriers in the interface states can be considerably reduced by using the fat zero scheme. In this scheme the zero signal is represented by a small background charge or "fat zero", so that charge packets are always flowing across the device. Hence the interface states under the storage and transfer electrodes are filled every cycle. The net charge trapped from a signal charge packet will then be the difference between the captured charge it lost at each transfer and the charge emitted into that packet, by the interface states under the storage and transfer gates, which was trapped from the preceding charge packets. Since for a sufficiently large fat zero charge the capture time constant of the interface state is very small (as discussed below) the interface states will be almost completely filled during each cycle and similar net trapping occurs during every cycle. The incomplete transfer due to trapping in interface states is consequently reduced by orders of magnitude.

4.2 Model and Approximations

The interface states at the semiconductor-oxide interface are characterized by their density $N_{ss}(E)$ and capture cross-section $\sigma_h(E)$. The capture and release of charge from these states is described by the Shockley-Read-Hall equation.[21] Assuming a p-channel 17 device and assuming that the interface is always kept under depletion to exclude the majority carrier and suppress any recombination

between the trapped holes and electrons, the rate equation describing the occupation of the interface states at an energy E above the valence band is given by

$$\frac{dn_{ss}}{dt} = K_1(N_{ss}-n_{ss})\ p-K_2 n_{ss}\ \exp(-E/KT) \qquad (34a)$$

$$K_1 = \sigma_h V_{th}/d \qquad (34b)$$

$$K_2 = \sigma_h V_{th} N_v \quad , \qquad (34c)$$

where N_{ss} is the interface state density (states/cm^2 - eV), n_{ss} is the density of filled interface (states/cm^2 - eV), and p is the density per unit area of the mobile holes in the valence band at the interface. σ_h is the trap capture cross-section for holes and V_{th} is the average thermal velocity of the mobile carriers. d is the average thickness of the inversion layer at the interface, N_v is the density of states in the valence band, and KT is the electron-volt equivalent of temperature.

The first term describes the rate of capture of the mobile carrier and is proportional to the density p of the available mobile carriers and the density of the empty traps $(N_{ss}-n_{ss})$. The second term describes the rate of emission of the trapped carrier. This term is proportional to the density of the filled interface states and decreases exponentially as the trap energy increases.

The total rate of capture of the mobile carrier is then given by

$$\text{Rate of Capture} = -\left.\frac{dp}{dt}\right|_{\text{capture}} = \int_{o}^{E_g} \frac{dn_{ss}}{dt}\, dE \,, \qquad (35)$$

where E_g is the energy gap. The mobile carrier continuity equation which describes the performance of the device is then given by (neglecting thermal generation currents)

$$\frac{\partial q}{\partial t} = -\frac{\partial}{\partial x} J_x - e \left.\frac{dp}{dt}\right|_{\text{capture}} \,, \qquad (36)$$

where q is the surface charge density of the mobile carrier, e is the electronic charge, J_x is the sheet current density, and x is the distance along the interface.

Thus, from the rigorous standpoint, the continuity Eq. (36) should be solved simultaneously with the nonequilibrium rate Eq. (34) and (35) in the regions under the source and receiving storage gates and transfer gate. While a rigorous treatment is conceptually possible, the uncertainty in the parameters characterizing the interface states makes such an elaborate calculation unwarranted. However, with suitable approximations one can make calculations which give qualitatively reliable and quantitatively suggestive estimates of the incomplete transfer due to interface state trapping.

When charge coupled devices are operated with the circulating background charge, interface states having an emission time constant larger than the cycle time remain almost completely filled all the time. These states capture carriers every cycle and do not get a chance to re-emit an appreciable fraction of the captured carriers during the cycle time. Interface states with an emission time constant much less

than the cycle time will be emptying and filling every cycle. These interface states have an energy of a few KT above the valence band edge (as shown below). Hence the interface states which make a substantial contribution to the incomplete transfer will be those with a time constant of the order of the clock cycle period and will lie within an energy range of the order of the thermal voltage. For the low interface state density obtainable with the present thermally grown oxide,[22-24] the rate of capture or emission is quite small compared to the other terms in Eq. (36). Thus, one can obtain an accurate solution by the following procedure. First, the term in Eq. (36) due to trapping is neglected and the continuity equation is solved to obtain the free charge transfer characteristics. The surface charge density profiles $q(x,t)$ are then used with the rate Eqs. (34) and (35) to calculate the incomplete charge transfer due to trapping in interface states.

The precise values of the interface state density N_{ss} and capture cross-section σ_h of the interface states; their distribution in energy over the band gap; and their dependence on temperature, normal and tangential surface fields are not well known, and vary strongly with the type and preparation of the oxide over the active channel of the device.[22-24] For our purposes here, we will take N_{ss} and σ_h independent of all the above parameters. However, if the exact energy dependence of N_{ss} and σ_h in the relevant part of the band gap is accurately known, it can be easily incorporated in this model. Consistent with the same order of accuracy of the above assumptions, we can also use average values of the mobile carrier concentration and

neglect the effect of their spatial distribution under the electrodes, to further simplify the numerical calculation.

4.3 Trap Occupation in Steady State and Transient

In steady state, the trap occupation can be obtained from Eq. (33a) and is given by

$$n_{ss} = \frac{N_{ss}}{\left(1 + \frac{K_2 \exp(-E/KT)}{K_1 p}\right)} \quad . \qquad (37)$$

The interface states are in equilibrium with the mobile carriers. Their occupation is described by the same quasi-fermi level as the mobile carriers.

$$E_f = KT \, \ell n \frac{K_2}{K_1 p} = KT \, \ell n \frac{N_v \cdot d}{p} \quad . \qquad (38)$$

Following a sudden abrupt change in the mobile carrier concentration, say p_0 to p_1, the trap occupation changes to the new steady state value corresponding to the new mobile carrier concentration p_1 with an effective time constant given by

$$\tau_{eff} = \frac{1}{K_1 p_1 + K_2 \exp(-E/KT)} \quad . \qquad (39)$$

If the effective time constant of the interface states τ_{eff} is smaller than the time constant τ measuring the variation of the mobile carrier density then the trap occupation reaches steady state very rapidly and effectively equilibrates with the varying carrier density. That is, if $\tau > \tau_{eff}$, then

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2 e^{-E/KT}}{K_1 p(t)}} \quad . \qquad (40)$$

Thus, the quasi-fermi levels of the traps follows the quasi-fermi level of the mobile carriers.

$$E_f(t) = KT \ln \frac{N_v \cdot d}{p(t)} \quad . \qquad (41)$$

On the other hand, if $\tau < \tau_{eff}$, then the trap occupation fails to follow the variation of the mobile carrier. If we let $K_1 p(t) >>> K_2 \exp(-E/KT)$, then this occurs when the mobile carrier density falls to a level such that

$$K_1 \tau p(t) < 1 \quad . \qquad (42)$$

For charge transfer from under a gate, we can define two regimes. First, when $K_1 p(t)\tau > 1$, the mobile charge is in effective equilibrium with the trapped charge. The total number of trapped carriers p_{tr} is given by

$$p_{tr}(t) = N_{ss} \left[E_g - KT \ln \frac{K_2}{K_1 p(t)} \right] \quad . \qquad (43)$$

Second, when $K_1 p(t)\tau < 1$, the mobile charge is no longer in equilibrium with the trapped charge. If we let t_4 be the time the emission mechanism becomes dominant, then for $t > t_4$ the trap occupation is given by

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t_4)}} \cdot \exp\left(-(t-t_4) K_2 \exp(-E/KT)\right) \qquad (44)$$

and the interface states start to empty with a time constant that increases exponentially with the trap energy. The total number of trapped carriers is given by

$$p_{tr}(t) = N_{ss}\left[E_g - KT\ \ell n\ K_2(t-t_4) - \frac{KT}{(t-t_4)K_1 p(t_4)}\right] \qquad t > t_4 \tag{45}$$

So in this case the interface states above $E_f = KT\ \ell n\ K_2(t-t_4)$ are almost full and those below it are nearly empty. The last terms in Eqs. (43) and (45) shows the dependence of the interface state occupation on the mobile carrier density. .

4.4 Trapping in Interface States Under the Storage Gates

When a signal charge packet is stored under the storage gate, all the interface states trap carriers and are filled very rapidly down to a quasi-fermi level given by Eq. (38). As the charge transfers to the next storage site, the residual charge decreases. In the complete charge transfer mode the transfer of charge at the end of the charge transfer process (say after a time t_3) becomes limited by thermal diffusion and fringing fields. The residual charge under the storage gate is then given by

$$p(t) = p(t_3)\ \exp\left(-(t-t_3)/\tau\right) \qquad t > t_3 \qquad , \tag{46}$$

where the characteristic time constant τ depends on diffusion and fringing fields.

Since the fringing fields under the storage gate are relatively small giving a rather large value of τ, and since the charge $p(t_3)$

is relatively large, the inequality

$$\tau K_1 p(t_3) > 1 \quad , \qquad (47)$$

is satisfied at the beginning of this time interval. Hence, the mobile charge is in equilibrium with the trapped charge. However, at later times the free carrier density may fall to such a value that the interface states are no longer in equilibrium with the free carriers and the interface states begin to simply emit the charge trapped in them. This state pertains for times t such that

$$t > t_4 = t_3 + \tau \, \ell n \left(K_1 p(t_3) \tau \right) \quad . \qquad (48)$$

If the clock frequency f_o is such that the charge transfer ends at a time t less than t_4, then the interface states will remain filled down to an energy defined by Eq. (41). When the next charge packet arrives, it fills all the interface states, and after it transfers the total number of trapped carriers is given by Eq. (43) with the proper value of $p(t)$. So, when the device is operated with a circulating background charge, or "fat zero", the net charge trapped from a signal charge packet is maximum when it is preceded by a fat zero and is given by:

$$\Delta q_{st} = e \, A_{st} \, N_{ss} \, KT \, \ell n \frac{p_s(t)}{p_o(t)} \quad . \qquad (49)$$

where Δq_{st} is the net charge trapped per transfer, A_{st} is the area of the storage gate, $p_o(t)$ and $p_s(t)$ are the residual charge under the storage gate at the end of the transfer time t for the fat zero

charge and the signal charge, respectively. When the difference between $p_s(t)$ and $p_o(t)$, is relatively small, then

$$\Delta q_{st} = e\, A_{st}\, N_{ss}\, KT\, \frac{\left(p_s(t) - p_o(t)\right)}{p_o(t)} \quad . \qquad (50)$$

It follows from Eqs. (46) and (50) that the net charge trapped is almost independent of frequency. In addition all the interface states above an energy E_1, where

$$E_1 = KT\, \ell n\, \frac{K_2}{K_1 p(1/2\, f_o)} \quad , \qquad (51)$$

will always be filled with captured holes. If the charge transfer ends after a time $t > t_4$, then in the complete charge transfer the interface states under the original storage gate continue to emit the trapped charge for one whole transfer (or $(m-1)$ transfer times for m transfers per cycle). This released charge is added to the next packet transferred into this storage bucket. When the next charge packet comes along, all the interface states are filled again. After this charge packet transfers, the interface states start to emit and so on. So when the device is operated with a circulating background charge, the net charge trapped from a signal charge packet at each transfer, for transfer time $t > t_4 + \tau$, is also maximum when preceded by a fat zero and can be obtained directly from Eq. (45).

$$\Delta q_{st} = e\, R\, A_{st}\, N_{ss}\, KT\, \frac{1}{(t-t_4)K_1} \left[\frac{1}{p_o(t_4)} - \frac{1}{p_s(t_4)}\right] , \qquad (52)$$

where $p_o(t_4)$ and $p_s(t_4)$ are the residual charge under the storage gate after a time t_4 (as defined in Eq. (48)) for the fat zero charge

and the signal charge, respectively, and R is a fraction given by

$$R = \frac{(m-1)t}{mt - t_4} = \frac{m-1}{m} \cdot \frac{1}{1-f_o t_4} \quad . \qquad (53)$$

m is the number of transfers per bit. If t_4 is smaller than the cycle time, then $t_4 f_o < 1$ and for $m = 2, R \cong \frac{1}{2}$. If the difference between $p_s(t_4)$ and $p_o(t_4)$ is relatively small, then

$$\Delta q_{st} = \frac{1}{2} e A_{st} N_{ss} KT \frac{\tau}{(t-t_4)} \cdot \frac{\left(p_s(t_4) - p_o(t_4)\right)}{p_o(t_4)} \quad . \qquad (54)$$

Thus, for transfer times $t > t_4 + \tau$, the net charge trapped per transfer decreases almost directly with the clock frequency. Also, all the interface states above an energy E_1 are filled with captured holes, E_1 is almost independent of the signal charge and is given by

$$E_1 = KT \, \text{ℓn} \, K_2(mt - t_4) \quad . \qquad (55)$$

4.5 Trapping in Interface States Under the Transfer Gates

The surface potential and the surface potential gradient under the gates of an overlapping gate charge coupled device along the silicon-silicon oxide interface are plotted in Fig. (4). These plots are obtained from a solution of the two-dimensional Poisson equation for substrate doping of $8 \times 10^{14}/cm^3$ and $10^{14}/cm^3$. The electrode voltages correspond to the last stages of the charge transfer with a signal charge in the receiving storage gate. Since the transfer gate is shorter and has a thicker oxide than the storage gate, the fringing fields under it are much larger than under the storage gate. Typical

values of single carriers transit time under the transfer gate are of the order of a few nanoseconds.

When a signal charge packet transfers from one storage site to the next, interface states under the transfer gate trap some of the charge during the first stages of the transfer process. Since fringing fields under the transfer gates are relatively large, the mobile carriers are swept out very rapidly and the emptying of the interface states begins earlier in the transfer process. Thus for all transfer times t of interest

$$t > t_{4_{tr}} \quad . \qquad (56)$$

The trapped carriers emitted before the transfer ends will join the main packet. During the last times of the cycle, a larger fraction γ of the emitted carrier will drift backwards to join the succeeding packet of charge, and a smaller fraction $(1-\gamma)$ will drift forward to join the original packet of charge. Because of the asymmetrical surface potential distribution γ is greater than one half. Then in the next cycle, during the transfer of the next packet of charge, the interface states under the transfer gate capture some charge, and so on. From the plots of the average mobile carrier concentration under the transfer gates for a two-phase overlapping gate CCD in Figs. (32) and (34), it is clear that the interface states will capture carriers for a time interval Δt. During that time interval an average carrier concentration p_{av} may be defined. The traps fill with an effective time constant τ_{eff} given by

$$\tau_{eff} = \frac{1}{K_1 p_{av} + K_2 e^{-E/KT}} \simeq \frac{1}{K_1 p_{av}} \quad . \qquad (57)$$

The filling probability or the fill factor F of the traps is given by

$$F = (1 - e^{-\Delta t/\tau_{eff}}) \quad . \qquad (58)$$

For transfer times $t > t_{4tr}$ the interface states empty according to Eq. (44) and the total trapped carriers is given by Eq. (45). When the device is operated with a circulating background charge or fat zero, the net charge trapped from the signal charge in interface states under the transfer gates is maximum when it is preceded by a fat zero and is given by

$$\Delta q_{tr} = \gamma e A_{tr} N_{ss} KT \left\{ \left(F_s \ell n \frac{\left(\frac{1}{f_o} - t_{4_{trs}}\right)}{\left(\frac{1}{mf_o} - t_{4_{trs}}\right)} - F_o \ell n \frac{\left(\frac{1}{f_o} - t_{4_{tro}}\right)}{\left(\frac{1}{mf_o} - t_{4_{tro}}\right)} \right) + \frac{R}{\left(\frac{1}{mf_o} - t_{4_{tr}}\right)} \left(\frac{F_o}{K_1 p_{avo}} - \frac{F_s}{K_1 p_{avs}} \right) \right\} \quad , \qquad (59)$$

where R is a fraction given by Eq. (53). p_{avo}, p_{avs} are the average mobile carrier concentration under the transfer gate during the interval Δt for a background charge and a signal charge respectively. F_o, F_s are the filling probability as defined by Eq. (58) for a background charge and a signal charge respectively. A_{tr} is the area under the transfer electrodes and $t_{4_{tro}}$, $t_{4_{trs}}$ are the times at which the emptying of the interface states start for the background charge and the signal charge.

Two special cases are of interest. First, if the fill factors F_s and F_o are less than one and unequal, then the first two terms dominate. For $\gamma = 1$ and $t_{4_{tro}} \approx t_{4_{trs}}$ Eq. (59) reduces to

$$\Delta q_{tr} = eA_{tr} N_{ss} KT(F_s - F_o) \ell n \, m \frac{\left(1 - f_o t_{4_{tr}}\right)}{\left(1 - mf_o t_{4_{tr}}\right)} \quad .$$

For $f_o t_{4_{tr}} << 1$ and $m = 2$,

$$\Delta q_{tr} \cong eA_{tr} N_{ss} KT(F_s - F_o) \ell n \, 2 \quad . \qquad (60)$$

Second, if the fill factors are equal to one $\left(\frac{\Delta t}{\tau_{eff}} >> 1\right)$, then Eq. (59) reduces to:

$$\Delta q_{tr} = eA_{tr} N_{ss} KT \left\{ \frac{\delta(t_4)}{(t - t_{4_{tr}})} R + \frac{R}{(t - t_{4_{tr}})} \left(\frac{1}{K_1 p_{avo}} - \frac{1}{K_1 p_{avs}} \right) \right\}$$

For $f_o t_4 << 1$, $m = 2$, $R \approx 1/2$

$$\Delta q_{tr} = eA_{tr} N_{ss} KT \left\{ f_o \, \delta(t_4) + f_o \left(\frac{1}{K_1 p_{avo}} - \frac{1}{K_1 p_{avs}} \right) \right\} \qquad (61)$$

where $\delta(t_4)$ is the difference in the time t_4 at which the emptying of the interface states start for the signal charge and the background charge.

In the first case, the net charge trapped is almost frequency independent. While in the second case it increases almost linearly with frequency.

All the interface states under the transfer gate above an energy E_1 are filled with captured holes. E_1 is almost independent of the

signal charge but depends on the clock frequency and is given by

$$E_1 = KT \ln K_2 \left(\frac{1}{f_o} - t_4\right) \cong KT \ln \frac{K_2}{f_o} \quad . \qquad (62)$$

4.6 Trapping in the Interface States Under the Edges of the Gates

Trapping in the interface states under the edges of the storage and transfer gates also add to the incomplete charge transfer. Since the precise area covered by the charge being transferred at the interface depends upon the surface potential profiles under the gates which in turn depends on the surface charge density, the number of interface states at the edges which come in contact with the charge is dependent upon the amount of surface charge. The surface potential profile for a given surface charge density and sequence of potentials applied to the gate electrodes is obtained by solving the two dimensional Poisson equation for the CCD structure. Solutions to this equation along and perpendicular to the active channel show that fringing fields penetrate under the edges of the gates for a distance of approximately a depletion layer thickness. The onset of these fringing fields define the spatial extent of the mobile charge. For fixed voltages applied to the gates, the depletion layer thickness and the penetration of fringing fields increase with decreasing surface charge. Hence a small surface charge is confined to a smaller area at the interface than a larger charge.

In the treatment of trapping and release of charge by these interface states, we must distinguish between the interface states at the gate edges parallel to the channel from those at the gate edges

perpendicular to the channel.

In the case of the interface states at the edges perpendicular to the channel, the signal charge or the background charge flows over the interface state during every cycle. Thus the interface state can capture carriers from both the signal charge and background charge. Hence, the filling and emptying of these interface states is similar to that under the transfer gates.[18]

The net charge trapped from a signal charge in the interface state under the perpendicular edges when the device is operated with fat zeros is maximum when it is preceded by a fat zero. If the probability of filling of the interface states by the background charge is less than unity, then from Eq. (60)

$$\Delta q_{e_\perp} = eA_{e_\perp} N_{ss} KT(1 - F_o) \ln 2 \quad , \qquad (63)$$

where $A_{e_\perp}$ is the area under the perpendicular edges and F_o is the fill factor for the background charge defined by Eq. (58). In the case F_o is almost equal to unity, then from Eq. (61):

$$\Delta q_{e_\perp} = eA_{e_\perp} N_{ss} KT \left\{ f_o \, \delta(t_4) + f_o \left(\frac{1}{K_1 p_{avo}} - \frac{1}{K_1 p_{av\ edge}} \right) \right\} \quad . \qquad (64)$$

In the case of the interface states parallel to the edges we must distinguish between the drop clock and the push clock. With drop clocks the signal charge is stored below a gate at a holding voltage V_1 which is a fraction of the largest clock voltage V_m that the MOS

structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates, and the charge flows to the potential minimum thus created. With push clocks the charge is stored under a gate held at V_m, and transferred to a nearby gate, also at V_m, by raising the potential of the gate where the charge has been residing and thus "pushing" the charge to the next gate. Charge coupled devices can be operated with two-phase, three-phase, or four-phase clocking schemes by push clocks, drop clocks, or a combination of push and drop clocks.

So with drop clocks, the charge transfer is effected by creating deeper potential wells under the next gates; and the background charge does not flow over the edges of the gates parallel to the channel. Thus the interface states under the parallel edges capture carriers from the signal charge but do not trap any carriers from the background charge; and the parallel edges are residual areas of the active channel that the background charges cannot reach. For example, after a signal charge is transferred from under the storage gate, the interface states under the parallel edges of this gate continue to emit the trapped carriers until the next signal charge passes, then the interface states fill again. The net charge trapped from the signal charge in the interface states under the parallel edges of the storage and transfer gates increases with increasing the number of fat zeros preceding it. This is unlike the net trapped charge in interface states under the storage gates, transfer gates, and the perpendicular edges which is almost independent of the number of fat zeros preceding the signal charge.

The net charge trapped in the interface states under the parallel edges increases logarithmically with the clock frequency (similar to the charge trapped when no fat zeros are used as shown below). For digital signals, the net trapped charge per transfer in the interface states under the parallel edges from the first "one bit" preceded by n_{zero} "zero bits" can be easily obtained from Eq. (45).

$$\Delta q_{e_{\parallel}} = e\,KT(N_{ss}\,A_{ste_{\parallel}} + N_{ss}F_s A_{tr_{\parallel}})\,\ell n\left[\left(\frac{n_{zero}+1/m}{f_o} - t_{4e_{\parallel}}\right)\Big/\left(\frac{1}{mf_o} - t_{4e_{\parallel}}\right)\right] \quad , \qquad (65)$$

where $A_{st_{\parallel}}$ and $A_{tr_{\parallel}}$ are the area of the edges parallel to the channel under the storage and transfer gates respectively. $t_{4e_{\parallel}}$ is the time at which the emptying of the interface states under the parallel edges start. For $f_o t_{4e_{\parallel}} \ll 1$ and $m = 2$ Eq. (65) reduces to

$$\Delta q_{e_{\parallel}} = eKT(N_{ss}A_{ste_{\parallel}} + N_{ss}F_s A_{tre_{\parallel}})\,\ell n(2n_{zero}+1) \quad . \qquad (66)$$

In this case, all the interface states under the parallel edges above an energy E_1, where for $n_{zero} \gg 1$

$$E_1 = KT\,\ell n\,K_2\left((n_{zero}+1)\frac{1}{f_o} - t_{4e_{\parallel}}\right) \quad , \qquad (67)$$

are filled with the captured holes.

But with push clocks, the trapping effects under the parallel edges are reduced. The charge transfer characteristics and the charge profiles

under the gates for the signal charge and the fat zero charge tend to be more similar with push clocks, hence the interaction of the traps with the mobile carriers of both charges is almost the same. For example, with the two-phase push clock, the charge transfer does not start until the surface potential under the storage gate is larger than that under the next transfer gate for both the fat zero charge and the signal charge. Hence the fat zero charge covers almost the same area covered by the signal charge at the interface under the storage gates before the charge transfer begins. Thus with push clocks, the behavior of most of the parallel edge area of the storage gates is similar to the behavior of the perpendicular edges and hence is described by Eqs. (63) and (64). So the effective area of the parallel edges under the gates that interact with the mobile carriers according to Eqs. (65) and (66) is much smaller with push clocks than with drop clocks.

4.7 Numerical Results

When the device is operated with a circulating background charge the total net charge trapped from a large charge packet in interface states at each transfer is obtained by summing the different contributions obtained above

$$\Delta q = \Delta q_{st} + \Delta q_{tr} + \Delta q_{e_\perp} + \Delta q_{e_\parallel} \quad . \qquad (68)$$

The same net charge Δq is emitted to the background charge by the interface states when it is preceded by a large signal charge. The

influence of this incomplete charge transfer due to trapping in interface states on the signal degradation is best described by the signal degradation factor ε,

$$\varepsilon = \frac{\Delta q}{q_s - q_o} = \varepsilon_{st} + \varepsilon_{tr} + \varepsilon_{e\perp} + \varepsilon_{e\parallel} \quad . \qquad (69)$$

Where q_s is the signal charge and q_o is the background charge, so $q_s = eA_{st}p_s$ and $q_o = eA_{at}p_o$. ε_{st}, ε_{tr}, $\varepsilon_{e\perp}$, $\varepsilon_{e\parallel}$ are the signal degradation factors due to trapping in interface states under the storage gate, transfer gate and the perpendicular and parallel edges of the gates respectively. p_s and p_o are the mobile carrier density for the signal charge and the background charge respectively.

We have evaluated the relative magnitudes of the signal degradation factors for an overlapping gate charge coupled device with dimensions consistent with typical layout tolerances of silicon gate technology. The storage polysilicon gates are 14μ long and 8μ apart. The channel width is 8μ. The results in Figs. (32), (33), (34), and (35) are taken from a detailed numerical solution of the transport dynamics in p-channel devices with a substrate doping of $0.8 \times 10^{15}/cm^3$ and minimum geometry dimensions operated in the complete charge transfer modes described in Section 3.1. In Figs. (32) and (33) the average mobile carrier concentration under the storage and transfer gates are plotted versus time when a two-phase drop clock is used. The same plots for a two-phase dynamic push clock are shown in Figs. (35) and (36).

In Table I, we have listed the values of the quantities used to

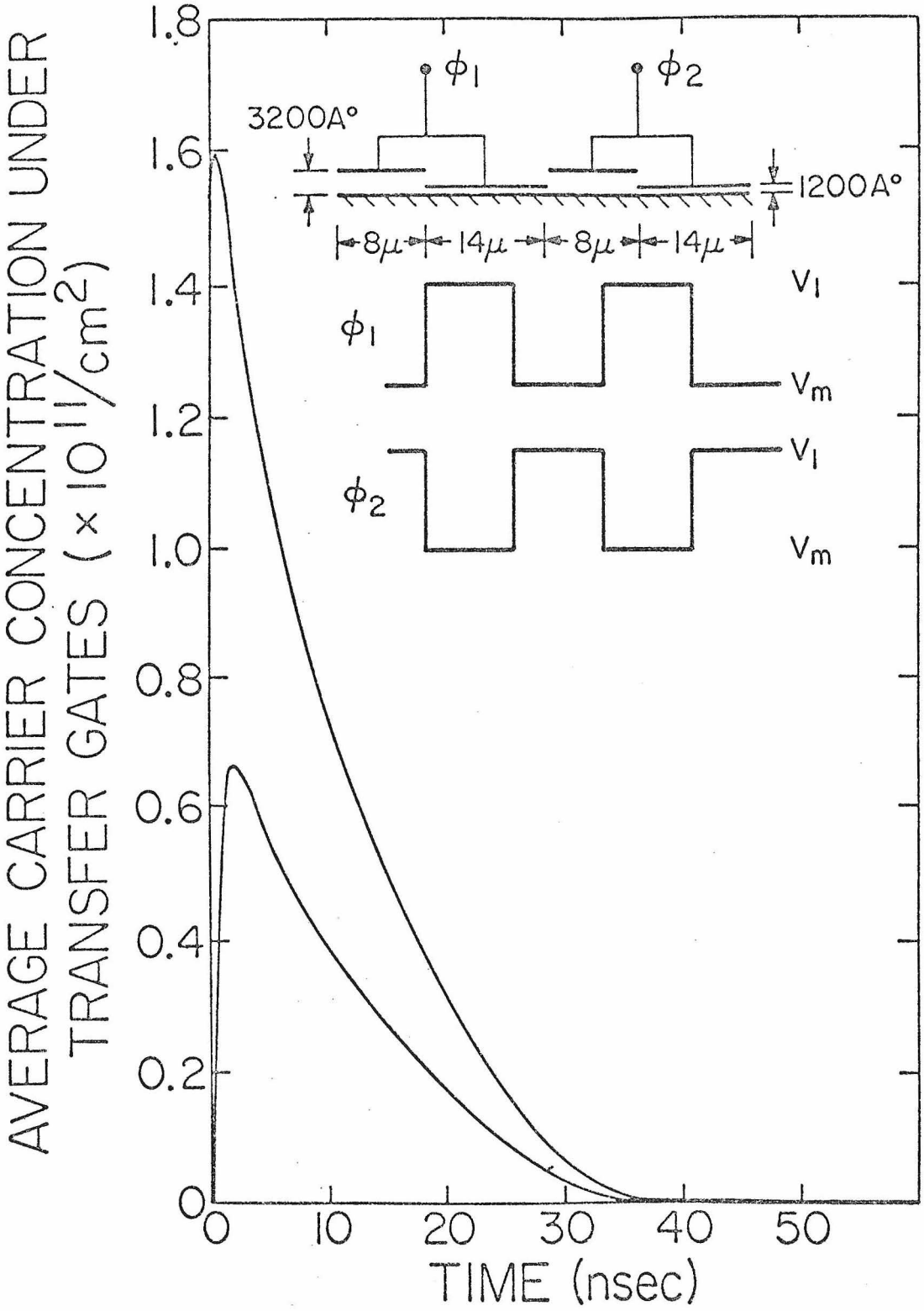
AVERAGE CARRIER CONCENTRATION UNDER TRANSFER GATES (× 10^11/cm^2)
TIME (nsec)
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
0
10
20
30
40
50
φ1
φ2
3200A°
1200A°
8μ
14μ
8μ
14μ
V1
Vm
φ1
V1
Vm
φ2

Figure 32.

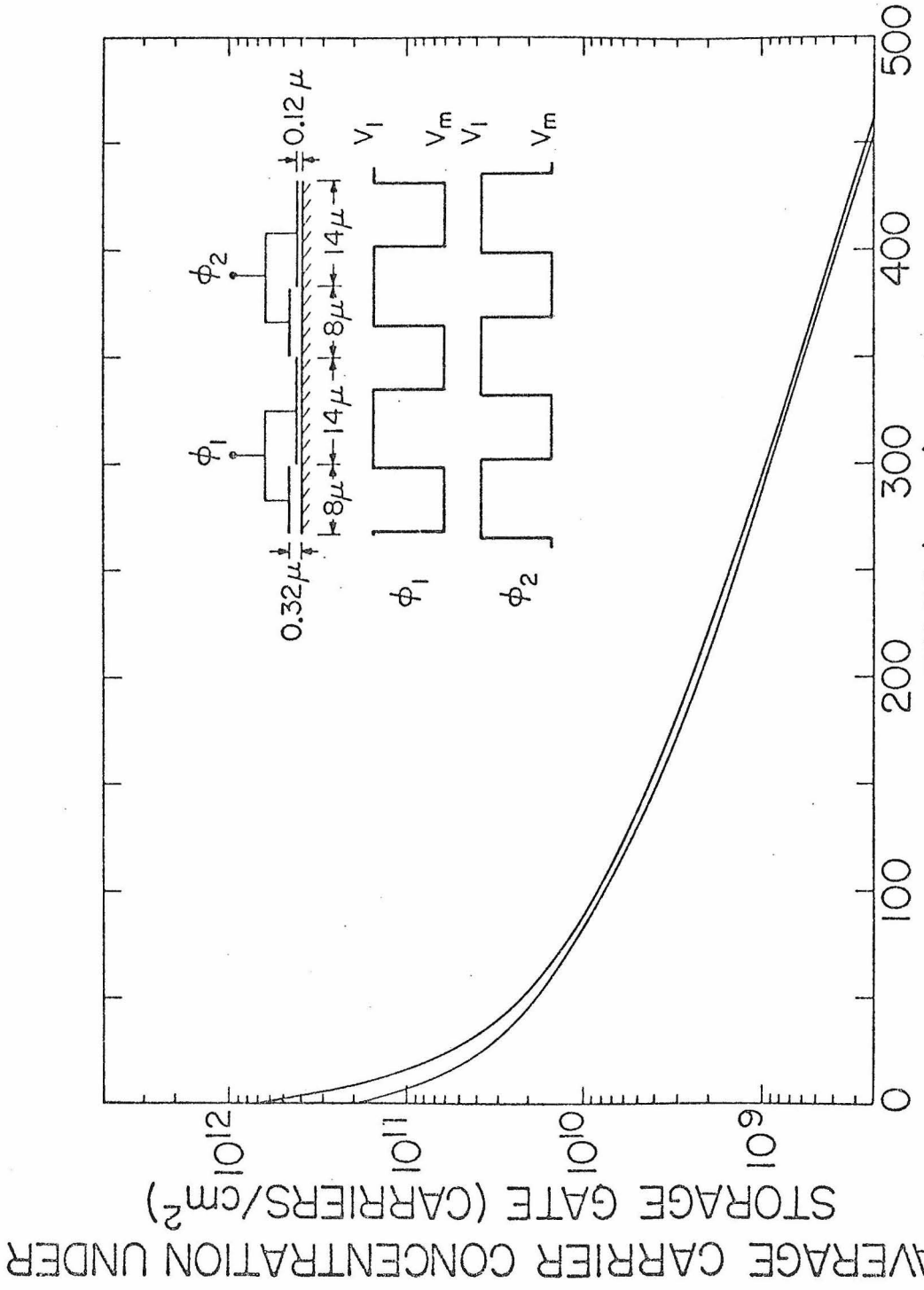
AVERAGE CARRIER CONCENTRATION UNDER STORAGE GATE (CARRIERS/cm²)
10¹²
10¹¹
10¹⁰
10⁹
0
100
200
300
400
500
TIME (nsec)
0.32μ
8μ
14μ
8μ
14μ
0.12 μ
φ1
φ2
V1
Vm
V1
Vm
φ1
φ2

Figure 33.

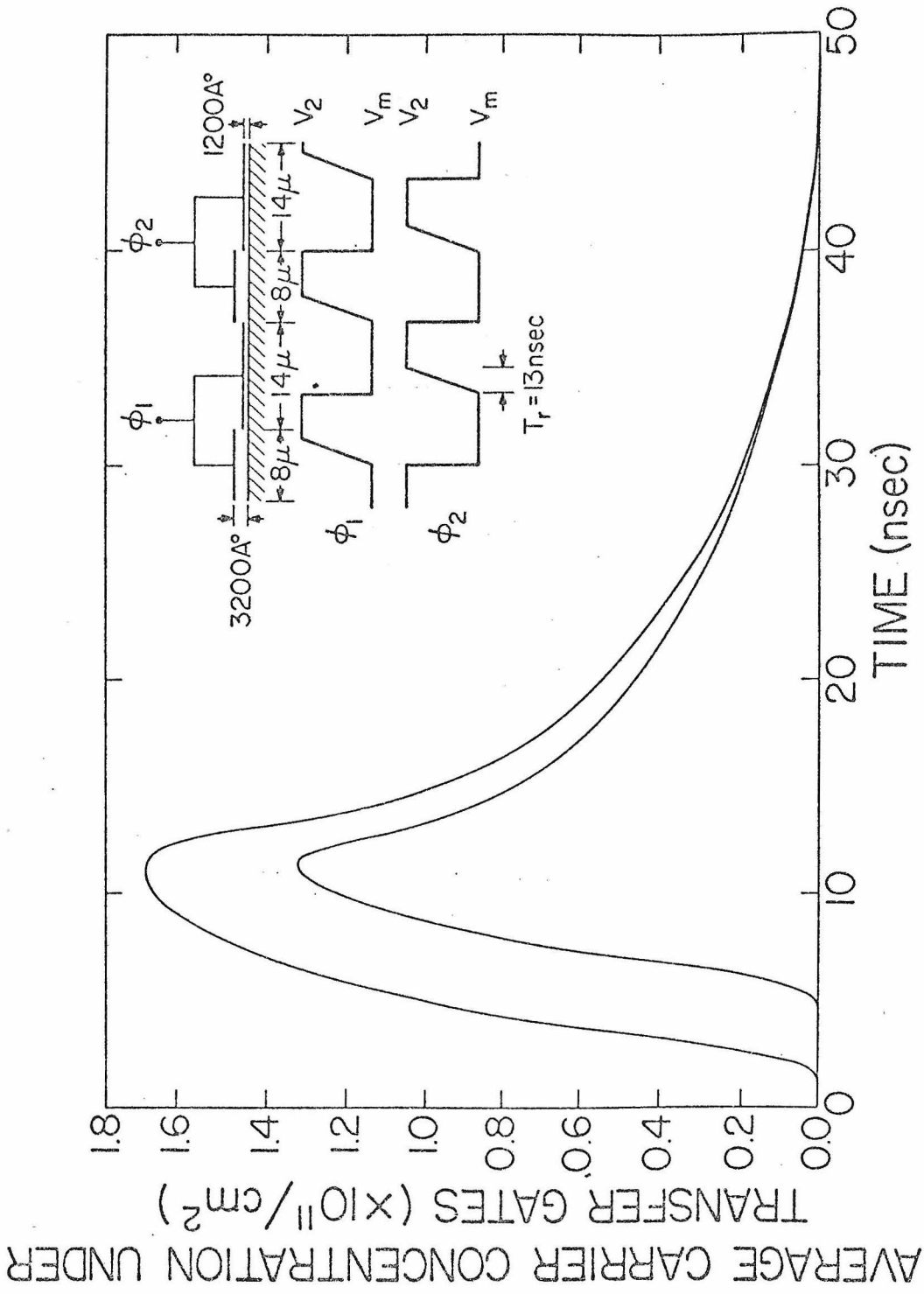
AVERAGE CARRIER CONCENTRATION UNDER TRANSFER GATES (x10¹¹/cm²)
TIME (nsec)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
10
20
30
40
50
3200A°
1200A°
8μ
14μ
8μ
14μ
φ1
φ2
V2
Vm
V2
Vm
φ1
φ2
Tr=13nsec

Figure 34.

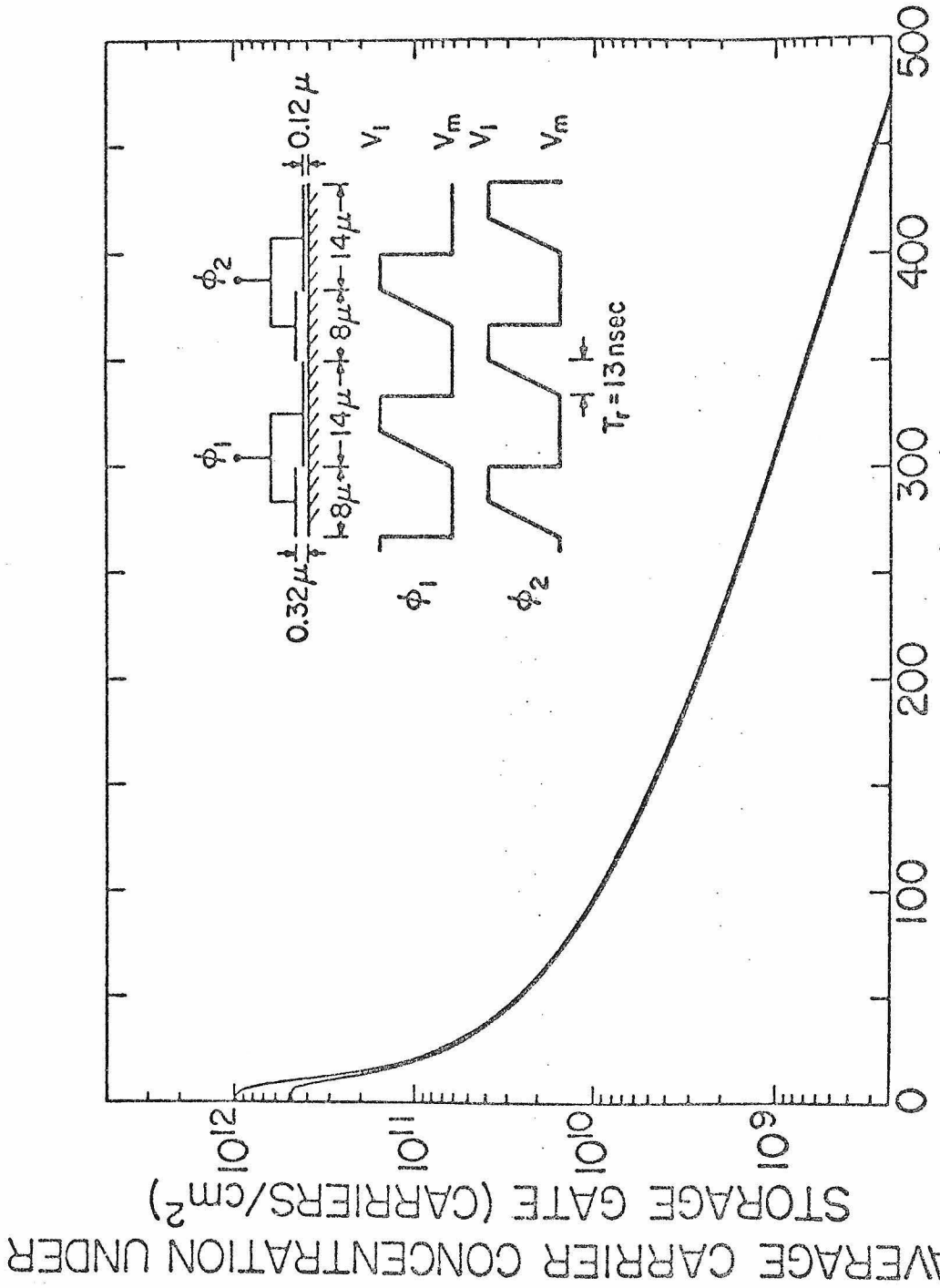
AVERAGE CARRIER CONCENTRATION UNDER STORAGE GATE (CARRIERS/cm²)
10¹²
10¹¹
10¹⁰
10⁹
0
100
200
300
400
500
TIME (nsec)
0.32μ
8μ
14μ
8μ
14μ
0.12μ
φ1
φ2
V1
Vm
V1
Vm
φ1
φ2
Tr = 13 nsec

Figure 35.

evaluate the signal degradation from the above equations. An average value of N_{ss} and σ_h was taken in agreement with the published values in the literature.[22-24] With a substrate doping of $0.8 \times 10^{15}/cm^3$ and for the minimum geometry dimensions, fringing fields under the storage electrodes are negligible.[10] Hence the time constant of the exponential decrease of the residual carrier under the storage gate is the thermal diffusion time constant $\tau_d = \ell_{Si}^2/2.5\ D$. The time intervals Δt (which are the times the carriers spend under the transfer gates and the perpendicular edges) are taken from Figs. (32) and (34). Zero fall and rise time for the two-phase drop clock and zero fall time and 13 nsec rise time for the two-phase push clock were used in the numerical simulation of the charge transfer characteristics shown in Fig. (33) to (35). For larger rise and fall times, the values of Δt are larger. The fill factors F_o and F_s are then calculated using an average carrier density under the transfer gates during the time intervals Δt from Figs. (32) and (34). They are almost unity for the drop and push clocks. Hence Eqs. (61) and (64) should be used to estimate Δq_{tr} and $\Delta q_{e\perp}$. The value of n_{zero} in Eq. (66) was taken unity to give the minimum value of $\varepsilon_{e_{\parallel}}$. The ratio of the area of the edges to the storage gate area depends on the width of the channel W, the lengths of the storage and transfer gates, and the substrate doping concentration. The values of $A_{st_{\parallel}}/A_{st}$, $A_{tre_{\parallel}}/A_{st}$ and $A_{e\perp}/A_{st}$ are taken from surface potential plots of the solutions of the two-dimensional Poisson equation of the device similar to those in Fig. (4). With push clocks, the effective area of the parallel edges under the

storage gates that interacts with the mobile carriers according to Eqs. (65) and (66) was taken one-tenth of the total parallel edge area under the storage gates. Actually a smaller value is expected because of the neutralization effect mentioned above during the pushing of the charge.

In Table II we have listed the values of ε_{st}, ε_{tr}, $\varepsilon_{e_{\parallel}}$, $\varepsilon_{e_{\perp}}$ and ε for the static drop and dynamic push two-phase clock at a frequency of one megacycle for the minimum geometry device. In our calculations, we chose a suitable background charge to represent a fat zero (ep_0) and a large charge to represent the signal charge (ep_s) as would be used for example to represent the zero and the one bit in a digital serial memory. In Figs. (36) and (37) we have plotted the signal degradation factor due to incomplete free charge transfer and due to trapping in interface state versus frequency. Several conclusions become apparent for this particular device. Trapping effects due to the interface states under the storage gate are larger than those under the transfer gate and under the perpendicular edges of the storage gate.[19] Trapping in interface states under the parallel edges of the gates is dominant at low frequencies. Also the incomplete charge transfer due to trapping in interface states when the device is operated with push clock is much less than when it is operated with drop clock. At low clock frequencies the signal degradation due to trapping interface states is larger than that due to incomplete free charge transfer. But at high frequency, the device performance is limited by the free charge transfer process,

TABLE I

Values of Parameters and Constants Used in the Calculation

$N_{ss} = 2 \times 10^{10}/cm^2$ - e.v.

$\sigma_h = 10^{-15} cm^2$

$K_1 = 1/25\ cm^2/sec.$

$K_2 = 10^{11}\ sec^{-1}$

$V_{th} = 10^7$ cm/sec.

$d = 25$ Å

$C_o = 2.86 \times 10^{-8}\ F/cm^2$

$p(t_3) = 4.5 \times 10^9/cm^2$

$A_{ei}/A_{st} = 0.156$

$t_3 \sim 150$ nsec

$t_4|_{st} \sim 500$ nsec

$\tau = 117$ nsec

$A_{tr}/A_{st} = 0.58$

Static Drop Clock

$p_s = 6.25 \times 10^{11}/cm^2$

$p_o = 1.79 \times 10^{11}/cm^2$

$p_{av\ s} = 0.5 \times 10^{11}/cm^2$

$p_{av\ o} = 0.27 \times 10^{11}/cm^2$

$p_{av\ edge} = 1.57 \times 10^{11}/cm^2$

$\frac{p_s(t_4)-P_o(t_4)}{p_o(t_4)} = 1.75 \times 10^{-2}$

$\delta(t_4) = 6$ nsec.

$\Delta t_{tr} \cong 35$ nsec.

$\Delta t_{eo} \cong 7$ nsec.

$t_4|_{tr} \cong 35$ nsec

$F_s = 1 - e^{-76} = 1$

$F_o = 1 - e^{-41} = 1$

$\left.\frac{A_{tre\,u} + A_{ste\,u}}{A_{st}}\right|_{W = 8\mu} = \frac{1}{10}$

Dynamic Push Clock

$p_s = 9.8 \times 10^{11}/cm^2$

$p_o = 4.6 \times 10^{11}/cm^2$

$p_{av}|_s = 0.6 \times 10^{11}/cm^2$

$p_{av}|_o = 0.4 \times 10^{11}/cm^2$

$p_{av}|_{edge} = 2.45 \times 10^{11}/cm^2$

$\frac{p_s(t_4)-P_o(t_4)}{P_o(t_4)} = 1.75 \times 10^{-2}$

$\delta(t_4) = 1.5$ nsec

$\Delta t_{tr}|_s \cong 44$ nsec

$\Delta t_{tr}|_o \cong 40$ nsec

$t_4|_{tr} \cong 45$ nsec

$F_s = 1 - e^{-118} = 1$

$F_o = 1 - e^{-72} = 1$

$\Delta t_{eo} \cong 13$ nsec

$$\left.\frac{A_{tre\,u} + A_{ste\,u}|_{effective}}{A_{st}}\right|_{W = 8\mu} = \frac{1}{200}$$

TABLE II

Numerical Values of Signal Degradation Factors for a p-channel

Minimum Geometry Two-phase CCD at one Megacycle Clock Frequency

Signal Degradation Factor Due to Trapping in Interface States Under:	Equation	Value for Static Drop Clock	Value for Dynamic Push Clock
The storage gate ε_{st}	(49)	8.4×10^{-5}	1.7×10^{-5}
The transfer gate ε_{tr}	(61)	3.62×10^{-6}	$.975 \times 10^{-6}$
The perpendicular edges $\varepsilon_{e\perp}$	(64)	1.33×10^{-6}	0.464×10^{-6}
The parallel edges $\varepsilon_{e\parallel}$	(66)	1.64×10^{-4}	7.0×10^{-6}
Total ε	(69)	2.53×10^{-4}	2.54×10^{-5}

It should be emphasized that the results shown in Figs. (36) and (37) are for a minimum geometry overlapping gate charge coupled devices under a specific set of operation conditions. The specific values of the signal degradation due to trapping in interface states depend on the device geometry and the operating conditions. So care should be taken in extrapolating the specific values of the signal degradation factors in Figs. (36) and (37) to other CCD structures with other dimensions under other operating conditions. The equations derived in the above Sections should be used with the device and model parameters appropriate to each case.

4.8 Discussion

The analysis and results given in the above Sections reveal some important and general features of the incomplete charge transfer due to trapping in interface states in charge coupled devices. In this Section we discuss some of these important features: Such as the relative contribution to the signal degradation of the interface states under the storage and transfer gates and their edges; the influence of clocking waveforms and voltages, device dimensions and parameters on the incomplete charge transfer due to trapping in interface states, and design features of CCD structures to reduce it.

When charge coupled devices are operated with fat zeros trapping in interface states under the edges of the gates parallel to the channel is the dominant effect at low frequencies. The parallel edges are the areas parallel to the channel at the interface under the storage and transfer gates which are covered by the signal charge and are not

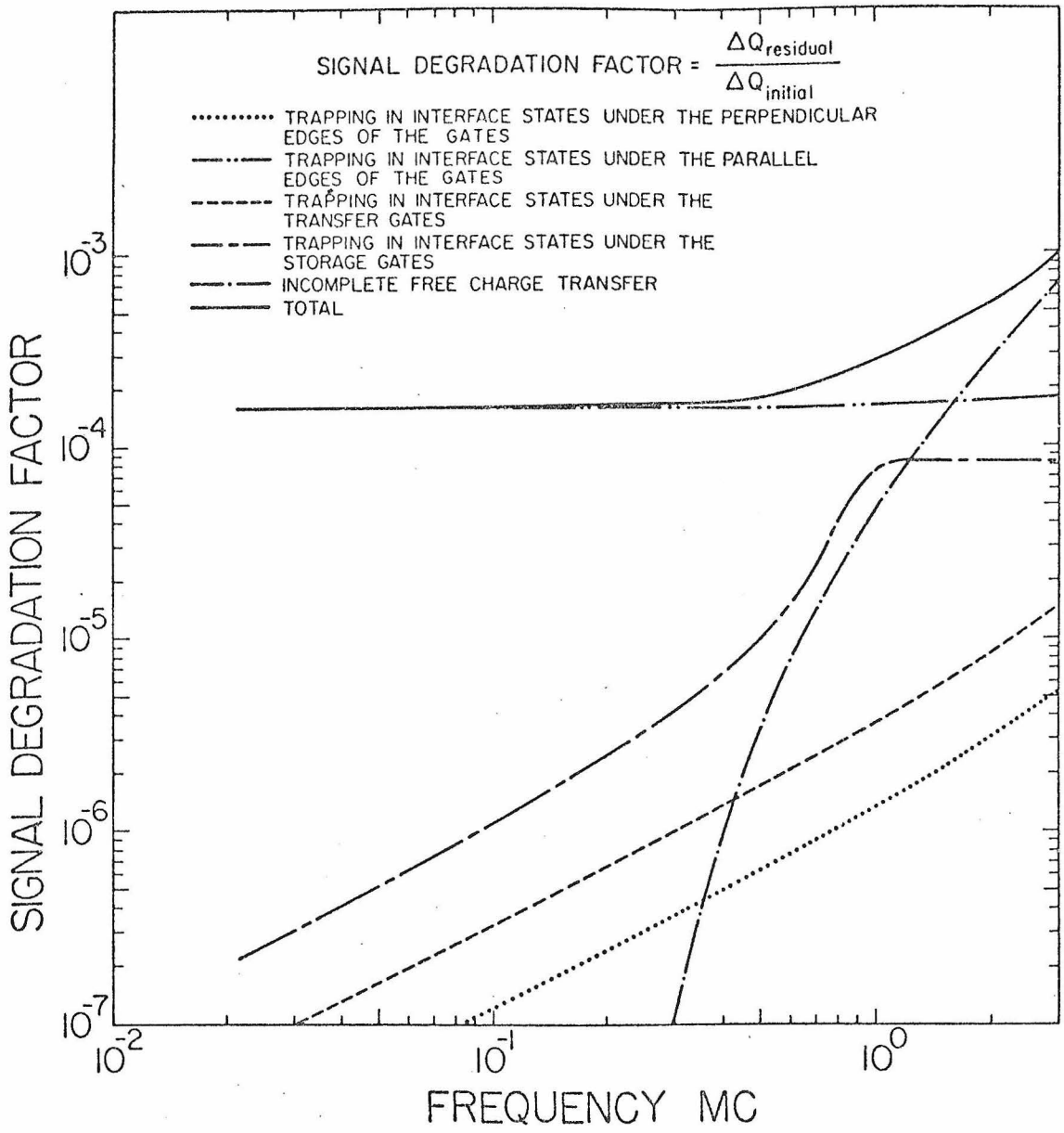
SIGNAL DEGRADATION FACTOR = $\frac{\Delta Q_{residual}}{\Delta Q_{initial}}$
TRAPPING IN INTERFACE STATES UNDER THE PERPENDICULAR EDGES OF THE GATES
TRAPPING IN INTERFACE STATES UNDER THE PARALLEL EDGES OF THE GATES
TRAPPING IN INTERFACE STATES UNDER THE TRANSFER GATES
TRAPPING IN INTERFACE STATES UNDER THE STORAGE GATES
INCOMPLETE FREE CHARGE TRANSFER
TOTAL
SIGNAL DEGRADATION FACTOR
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-2}
10^{-1}
10^{0}
FREQUENCY MC

Figure 36.

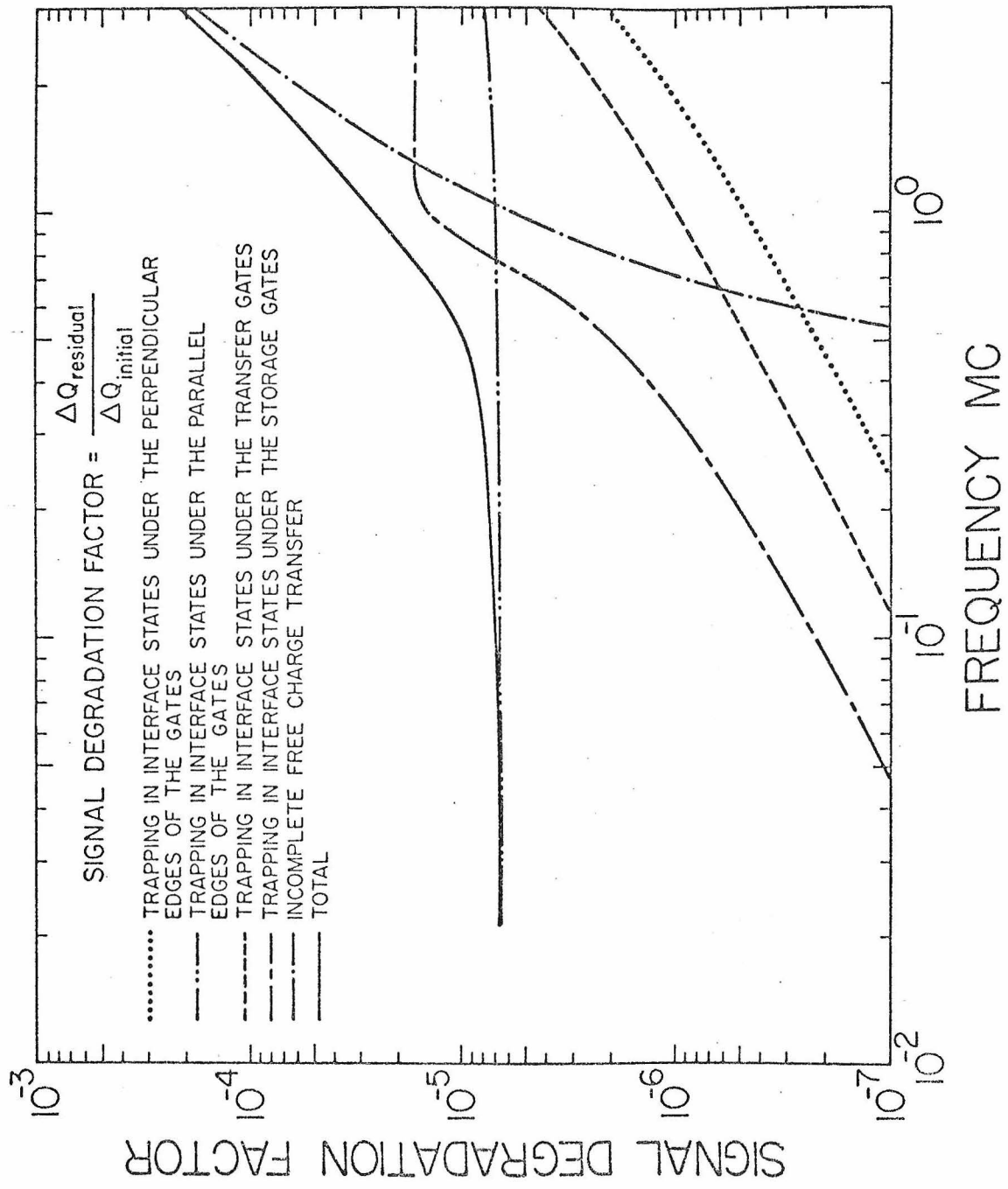
SIGNAL DEGRADATION FACTOR
FREQUENCY MC
SIGNAL DEGRADATION FACTOR = ΔQ residual / ΔQ initial
TRAPPING IN INTERFACE STATES UNDER THE PERPENDICULAR EDGES OF THE GATES
TRAPPING IN INTERFACE STATES UNDER THE PARALLEL EDGES OF THE GATES
TRAPPING IN INTERFACE STATES UNDER THE TRANSFER GATES
TRAPPING IN INTERFACE STATES UNDER THE STORAGE GATES
INCOMPLETE FREE CHARGE TRANSFER
TOTAL
10^-3
10^-4
10^-5
10^-6
10^-7
10^-2
10^-1
10^0

Figure 37.

covered by the background charge. The interface states under the parallel edges capture charge from the signal charge only. The resulting signal degradation is almost frequency independent, varies inversely with the channel width, and depends on the information content of the signal. At low frequency the signal degradation due to trapping in the interface states under the storage gates, the transfer gates and the perpendicular edges is relatively smaller. These interface states capture charge from both the signal charge and the background charge. Hence the background charge is effective in reducing the effect of trapping in these interface states on the incomplete charge transfer. For a sufficiently large background charge the effective time constant of the interface states is typically a fraction of a nanosecond. With the finite rise and fall times obtained with the practical clock drivers, and for the minimum geometry CCD devices we have considered, these interface states can equilibrate with both the signal charge and background charge. This leads to a small signal degradation which is directly proportional to frequency.

From the equations derived in Sections 4.4, 4.5 and 4.6 and Chapter 3, we may conclude that increasing the clock voltage amplitude and the signal charge reduces the incomplete transfer due to trapping in interface states and the incomplete free charge transfer. Clocking waveforms that tend to reduce the incomplete free charge transfer by making the charge transfer for large and small charge similar will also reduce the incomplete charge transfer due to trapping in interface states because the effective parallel edge area is reduced and the

charges under the storage and transfer gates, and the time at which emptying of the interface states begins tend to be less dependent on the initial charge. For example when the device is operated with a two-phase push clock, the incomplete charge transfer due to interface state is reduced by over an order of magnitude over that when it is operated with static drop clock. If the device is operated in the complete charge transfer mode the other details of the clocking waveforms such as its rise time and waveshape affect mainly the time interval Δt the charge spends under the transfer gate and the time t_4 at which the interface states starts to empty. For example if the rise time increases Δt and t_4 increase and the signal degradation ε_{st} due to the interface states under the storage gate increases slightly. The signal degradation due to interface states under the transfer gates and the perpendicular edges ε_{tr} and $\varepsilon_{e\perp}$ also increase very slightly if $\frac{\Delta t}{\tau_{eff}} >> 1$, but decrease if the fill factor F_s and F_o are less than unity.

Certain design features of CCD structures may reduce the incomplete charge transfer due to the interface states. A wide active channel increases the signal charge relative to the net charge trapped in the parallel edges and hence reduces the signal degradation factor at low frequencies.[20] Thinner oxide over the active channel increases the oxide capacity and the signal charge density. Thus, the net charge trapped under the storage gates, transfer gates, and the perpendicular edges decreases, and the area of the edges is reduced. A higher

substrate doping reduces the edges area, but also reduces the fringing fields under the storage gates and hence decreases the rate of free charge transfer. A structure with a high substrate doping (or channel stop diffusion) and a low doping under the active channel reduces the parallel edge area and increases the fringing fields at the same time. The large fringing fields reduce the incomplete free charge transfer at high frequency. The net charge trapped under the transfer and storage gates is also reduced as the interface states start to empty earlier in the transfer process. The perpendicular edge area is increased in this structure, but since in the overlapping gate CCD the effect of the perpendicular edges is relatively small, the overall effect of interface states on incomplete transfer is reduced at low frequencies. Such a structure can be easily achieved with ion implantation or otherwise. Reduction of the signal degradation due to trapping in interface states can be also achieved by decreasing the interface state density N_{ss} for example by using (100) instead of (111) substrate. Moving the charge packets in potential wells in the bulk rather than at the interface as in buried channel CCD[27] eliminates the incomplete charge transfer and fluctuation noise due to trapping of the signal charge in the interface states. Since trapping in the defect states of the buried channel is expected to be much smaller than interface state trapping, the signal degradation in buried channel charge coupled devices is much smaller than in surface channel CCD.

The signal degradation due to trapping in interface states limits the performance of CCD devices at low frequency, but at high frequency

the signal degradation due to incomplete free charge transfer is dominant. According to the simple model we have considered, the capture cross-section σ_h and the interface state density N_{ss} were taken constant for simplicity. Actually the variation of N_{ss} and σ_h with energy will change the frequency dependence of the signal degradation due to trapping in interface states from that plotted in Figs. (36) and (37). However the frequency dependence of the signal degradation factor due to the interface states will still be weaker than that due to incomplete free charge transfer. The latter changes very rapidly with frequency, for example in Fig. (37) it changes by more than four orders of magnitude over only one decade of frequency.

So far, we have assumed that the background charge and the signal charge are sufficiently large that the interface states under the transfer gates, and the perpendicular edges can effectively equilibrate with the mobile carriers. However, if the background charge, or, the capture cross-section σ_h, or the time interval Δt the carriers spend under the transfer gates and the perpendicular edges is too small, then these interface states cannot equilibrate with the mobile carriers in transit. The fill factor F_s and F_o are thus less than unity, and the first two terms in Eq. (59) dominates at sufficiently low frequency. In this case the contribution to the signal degradation from the interface states under the perpendicular edges and the transfer gates tends to a constant value at low frequency given by Eq. (60) and (63). This contribution is due to the difference in the filling probabilities of the interface states for the background charge and the signal charge.

The contribution to the signal degradation from the interface states under the parallel edges and the storage gates increases also by decreasing the background charge. However the trapping in the interface states under the parallel edges still remain the dominant effect especially from minimum geometry devices.

If the storage and transfer gate lengths are reduced, the time interval Δt that the charge spends under the transfer gate decreases and the relative area of the perpendicular edges increases. Also the time t_4 at which the emptying of the interface states starts to decrease. Thus ε_{st} slightly decreases but $\varepsilon_{e\perp}$ increases, ε_{tr} decreases very slightly in the case $\Delta t/\tau_{eff} >> 1$, but increases considerably if the filling probabilities F_s and F_o are less than unity. The signal degradation due to the parallel edges $\varepsilon_{e\parallel}$ which is the dominant effect decreases also very slightly.

The interface states under the storage gates, the transfer gates and the perpendicular edges can capture carriers every cycle from the signal charge and the fat zero charge. Hence the interface states with energy levels above E_1 (given by Eqs. (51), (55), (62), and (67)) do not get a chance to re-emit the captured carriers and are filled all the time. The interface states with energy between the valence band edge and the energy E_1 will be emptying and filling every cycle.[21] For example for digital signals, the net trapped charge from the first "one bit" in the interface states under the storage and transfer gates and the perpendicular edges is almost independent of the number of preceding "zero bits". But the net

trapped charge from the first "one bit" in the interface states under the parallel edges, increases logarithmically with the number of preceding "zero bits". If a two-phase device is operated with no fat zeros, then the net trapped charge per transfer from the first "one bit" preceded by n_{zero} "zero bits" can be easily obtained from Eq. (45).

$$\Delta q = eA_{st}\, KT\, N_{ss}\, \ell n \left(\frac{n_{zero} + 1/2}{f_o} - t_{4st} \right) \Bigg/ \left(\frac{1}{2f_o} - t_{4st} \right)$$

$$+ eA_{tr}\, KT\, N_{ss}\, P_s\, \ell n \left(\frac{n_{zero} + 1/2}{f_o} - t_{4tr} \right) \Bigg/ \left(\frac{1}{2f_o} - t_{4tr} \right)$$

$$+ eA_e\, KT\, N_{ss}\, \ell n \left(\frac{n_{zero} + 1/2}{f_o} - t_{4tr} \right) \Bigg/ \left(\frac{1}{2f_o} - t_{4e} \right)$$

and for $t_{4st} < \frac{1}{2f_o}$ and $t_{4tr} << \frac{1}{2f_o}$

$$\Delta q = e\, KT\, N_{ss}(A_{tr} + A_{st}P_s + A_e)\, \ell n(2\, n_{zero} + 1) \quad . \tag{70}$$

The above result could be used to measure N_{ss} by measuring the slope of the charge loss versus $\ell n\, n_{zero}$. However, Eq. (70) shows that the so measured value of N_{ss} is some average value of N_{ss} under the transfer and storage gate. A typical value of the signal degradation factor ε at each transfer in this case is about 10^{-3}, if n_{zero} is equal to unity.

Measurements of the signal degradation factor in charge coupled devices are difficult and require long register strings for a good accuracy. The signal degradation factor due to incomplete free charge

transfer at high frequencies were measured by J. E. Carnes and W. F. Kosonocky[28] using a 64 bits two-phase overlapping gate shift register. They measured a signal degradation factor of 10^{-4} at one megacycle. Using feedback to increase the effective number of transfers, P. A. Levine[29] measured a signal degradation of 3×10^{-5} at 200 Kilocycles and 9×10^{-6} at 10 Kilocycles. Presently, the experimental data of the signal degradation factor in the overlapping gate charge coupled devices are relatively sparce. So experimentally, the precise values of the signal degradation due to trapping in the interface states at low frequencies and its frequency dependence are not presently well known.

Chapter 5

CONCLUSION

We have developed a detailed numerical simulation of the transport dynamics in terms of charge motion due to thermal diffusion, self-induced fields and fringing fields under all the relevant electrodes and inter-electrodes regions of charge coupled devices. This numerical simulation is a simple mathematical model that can be used to study the free charge transfer characteristics of different device structures with various clocking schemes and waveforms. We have also presented the charge transfer characteristics of overlapping gate charge coupled devices clocked with two and four-phase clocks and various waveforms.

The charge transfer with three-phase and single-phase clocking schemes can be readily understood from the results of the numerical simulation of the charge transfer with two and four-phase clocking schemes. The charge transfer with a single-phase clocking scheme can be easily deduced from the charge transfer with the push and drop two-phase clocks. The charge transfer with dynamic three-phase push clock also follows from the charge transfer with the four-phase push clock.

We have shown that the charge transfer in the overlapping gate structure divides naturally into several distinct stages. In the first stages, the storage gates are like capacitors charged and discharged by the transfer gates which limit the transfer rate. The overlapping transfer gate shields out the repulsive forces of the surface charge in transit and enhances the rate of charge transfer. The nonlinearity due

to the self-induced fields is dominant in these stages and the charge transfer depends on the clocking waveforms. In the two-phase clocking scheme the transfer gates are like MOS transistors at pinch off, and the storage gates are the sources and the drains. In these stages the transferred charge increases according to the portion of the clock voltage waveform that pushes the charge from one storage site to another for the push clocks, or according to the portion of the clock voltage waveform that creates the deeper potential well for the drop clocks.

The last stages of the charge transfer process depend on whether the device is operated in the complete charge transfer mode or in the incomplete charge transfer mode. During the last stages of the complete charge transfer mode the rate of charge transfer in the overlapping gate structure depends on how fast the storage gates can be discharged. The transfer gates in this structure are usually shorter and have larger fringing fields, and the charge transfer across the transfer gates is much faster than the charge transfer out of the storage gate. In the last stage, the residual charge under the storage gates decreases exponentially with a time constant that depends on fringing fields and thermal diffusion. For strong fringing fields, the final decay time constant τ_f is a fraction of the single carrier transit time across the storage gate. In this case the exponential decay is due to the diffusion at the tail end of the residual charge packet under the storage gate. In the incomplete charge transfer mode, the charge transfer is very similar to the charge transfer in the MOS bucket

brigade.[30] In this case, the charge transfer in the last stage is dependent on the transfer gate length. The residual charge under the storage gate decreases logarithmically, due to the thermally emitted carriers from the residual charge that diffuses across the transfer gate to the next storage gate.

The time constants of all stages of the charge transfer are proportional to the product of the storage gate and transfer gate lengths or the storage gate length squared, and the inverse of the surface mobility. In the first stages, the time constants are proportional to the inverse of the portion of the clock voltage used to store the signal charge. In the last stages the time constants are proportional to the inverse of the thermal voltage or the voltage drop across the gates due to fringing fields.

We have shown also that the charge transfer characteristics calculated from a lumped circuit model of the overlapping gate charge coupled devices agree with the results of the numerical simulation. According to this model, the charge transfer dynamics could be described by the charging and discharging of lumped capacitors through lumped transfer channels. This is possible because the charge redistribution time of the surface charges under the CCD gates is orders of magnitude smaller than the transfer times of interest and therefore the surface charge profiles under the gates reach rapidly steady state. The lumped circuit model can be used to derive the charge transfer characteristics for other device structures and dimensions with various clocking waveforms and voltages, thus providing practical charge coupled device and

circuit design tools.

We have also calculated the signal degradation due to incomplete free charge transfer from the charge transfer characteristics obtained from the numerical simulation or the lumped circuit model of the free charge transfer process. These calculations show that the signal degradation of the incomplete free charge is due to an intrinsic transfer rate and due to the modulation of the device parameters by the signal charge being transferred. The intrinsic transfer rate is due to the finite carrier mobility and finite transfer time. The modulation effects are due to the dependence of the effective lengths of the gates, the effective capacitances per unit area and fringing fields under the storage and transfer gates on the signal charge being transferred.

Calculation of the signal degradation due to incomplete charge transfer shows also that the performance of the overlapping gate charge coupled devices is better than the MOS bucket brigade. At very high clock frequency the signal degradation due to incomplete free charge transfer in the MOS bucket brigade is almost the same as in the overlapping gate CCD. But at moderate and low clock frequency the signal degradation in the MOS bucket brigade is larger than in the overlapping gate CCD. The MOS bucket brigade always operates in the incomplete charge transfer mode; the p islands are storage buckets with undefined bottoms that always contain residual charge. So the residual charge decreases logarithmically with time and the signal degradation tends to a constant value at low clock frequency due to transfer gate length and barrier height modulation. But the overlapping gate charge coupled

devices can be operated in the complete charge transfer mode. So the residual charge decreases exponentially and the signal degradation due to incomplete free charge transfer (intrinsic transfer rate and device parameters modulation) also decreases exponentially with time. The signal degradation due to trapping in the interface states, which is the dominant effect in the overlapping gate CCD at low clock frequency, is also less than the signal degradation in the MOS bucket brigade at low clock frequency.

Using a simple model we have estimated the signal degradation to interface states trapping in overlapping gates charge coupled devices operated with a background charge taking into account the re-filling of the interface states during transfer. The incomplete charge transfer due to interface states limits the performance of these devices at low frequencies. The most dominant effect is trapping in the interface states under the parallel edges (the areas parallel to the active channel at the interface under the storage and transfer gates which are covered by the signal charge and are not covered by the background charge). For a sufficiently large background charge the interface states under the storage gates, transfer gates, and the perpendicular edges of the gates can effectively equilibrate with both the signal and background charge. Hence the incomplete charge transfer due to trapping in these interface states varies almost directly with frequency and becomes very small at sufficiently low frequency. Some design features of CCD structures were shown to reduce the incomplete charge transfer due to interface state trapping. We have

shown also that increasing the clock voltages or increasing the signal charge or using push clock instead of drop clocks reduces the incomplete charge transfer due to interface states trapping.

We have shown also that the key features of the push clocks are that a larger portion of the clocking voltage is used to store the signal charge; hence larger signal charges can be transferred resulting in larger signal dynamic range and signal to noise ratio. Also with push clocks the characteristics of the charge transfer are almost independent of the value of the signal charge than with drop clocks. Hence the residual charges after each transfer are much less dependent on the initial charges, and the interaction of the different charges with the interface states is more similar. This results in better performance at both high and low frequencies. The pushing of the charge from one storage site to another is easily achieved by the finite fall and rise times which are unavoidable in practical clock drivers.

In addition we have shown that increasing the clocking scheme complexity, from single-phase to two-phase to four-phase clocking scheme, allows a better control of the storage and transfer of the signal charge and better device performance. Increasing the clocking scheme complexity is important in applications requiring larger signal dynamic range, larger signal to noise ratio, and higher frequency range.

APPENDIX I

Green Function Solution of the Potential in a MIS Structure

Consider a MIS structure as shown in Fig. 38. The insulator-semiconductor interface, and the insulator-metal interface are parallel to the y-z planes. It is desired to estimate the surface potential and the surface potential gradient at the semiconductor-insulator interface, for an arbitrary surface charge density profile $q(y)$ and a voltage V_G on the metal electrode. Although the Poisson equation for this problem is nonlinear in the semiconductor region, we may still solve it as a linear equation using the depletion approximation. First, let us calculate the potential and electric field at any point (x,y) in the semiconductor region due to a linear charge of unit strength, i.e. one Coulomb/cm, at a point (x', y') parallel to the z-axis. The semiconductor region, in this case, is treated as a dielectric of permittivity ε_1. The resulting potential function $G(x,y,x',y')$ is the Green function solution of the two-dimensional Poisson equation of the structure. Assuming the metal plane is at ground potential, the desired potential function can be calculated by the method of images. Since the boundary conditions at both the insulator-semiconductor interface and insulator-metal interface should be satisfied, an infinite series of image line charges are required to calculate the potential function in each region. It can be shown that the Green function in the semiconductor region is given[31] by

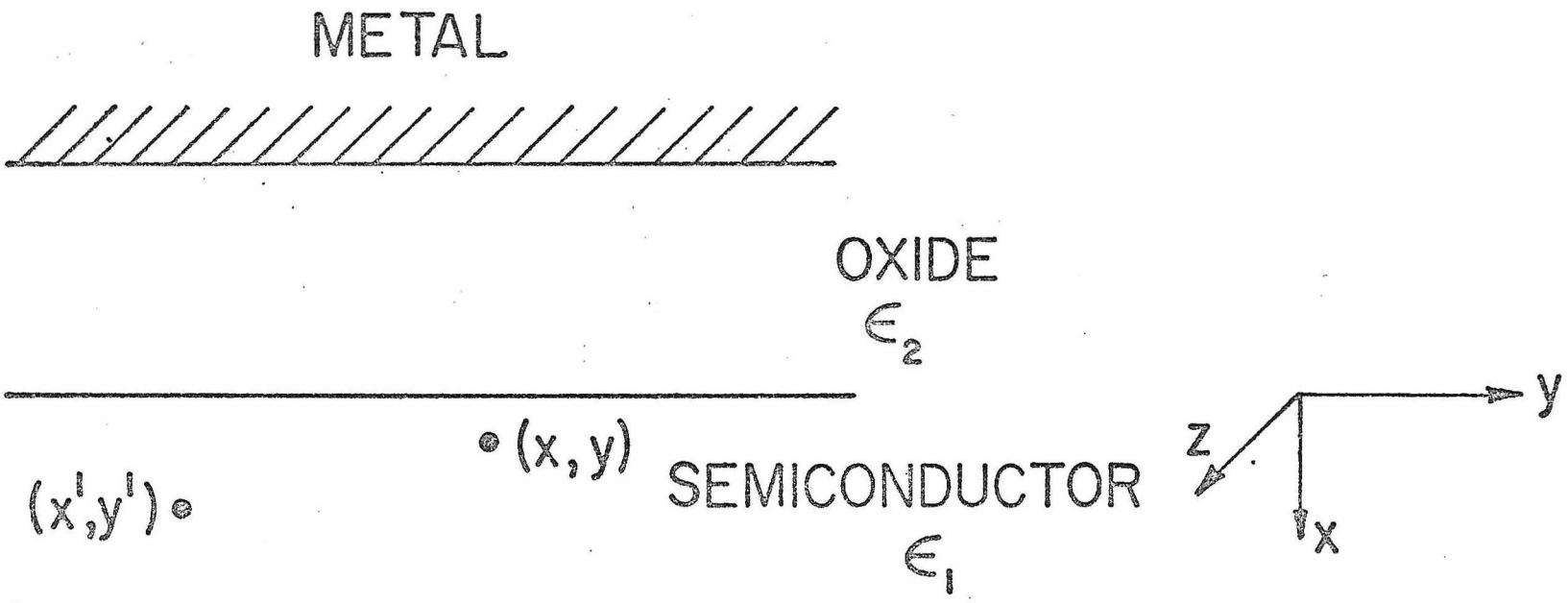

Figure 38.

$$G(x,y,x',y') = \frac{-1}{4\pi\varepsilon_1}\{\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2} \ln [(y - y')^2 + (x + x')^2]$$

$$+ \ln[(y - y')^2 + (x - x')^2]$$

$$- \frac{4\varepsilon_1\varepsilon_2}{(\varepsilon_1 + \varepsilon_2)^2} \sum_{m=1}^{\infty} (\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2})^{m-1} \ln[(y-y')^2$$

$$+ (x + x' + 2md_o)^2]\} \qquad \text{(A1-1)}$$

Where d_o is the insulator thickness.

If the point (x,y) lies at the semiconductor-insulator interface, then substituting in Eq. (A1-1) we get:

$$G(o,y,x',y') = \{\frac{-1}{2\pi(\varepsilon_1 + \varepsilon_2)} \ln[(y - y')^2 + x'^2]$$

$$- \frac{\varepsilon_2}{\varepsilon_1 + \varepsilon_2} \sum_{m=1}^{\infty} (\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2})^{m-1} \ln[(y - y')^2 + (x' + 2md_o)^2]\} \qquad \text{(A1-2)}$$

The Green function of the surface potential gradient along the semiconductor-insulator interface is given by

$$\frac{\partial}{\partial y} G(o,y,x',y') = \frac{-1}{\pi(\varepsilon_1 + \varepsilon_2)}\{\frac{y - y'}{(y - y')^2 + x'^2} - \frac{2\varepsilon_2}{\varepsilon_1 + \varepsilon_2} \sum_{m=1}^{\infty}$$

$$(\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2})^{m-1} \frac{(y - y')}{(y - y')^2 + (x' + 2md_o)^2}\} \qquad \text{(A1-3)}$$

The surface potential for a surface charge density profile q(y') and a gate voltage V_G is given by (neglecting the fixed insulator-semiconductor interface charge q_{ss}, and the difference in the metal and

semiconductor work functions)

$$\Phi_s(y) = \Phi(o,y) = V_G + \int_{-\infty}^{+\infty} G(o,y,o,y')q(y')dy' +$$

$$+ \int_{-\infty}^{+\infty} dy \int_{o}^{X_D(y')} dx' \; G(o,y,x',y') \; eN_D \qquad \text{(A1-4)}$$

where N_D is the donor concentration for n-semiconductor. $X_D(y)$ is the depletion layer thickness defined by the implicit relation:

$$\Phi(x_D,y) = V_G + \int_{-\infty}^{+\infty} G(x_D,y,o,y') \; q(y')dy'$$

$$+ \int_{-\infty}^{+\infty} dy' \int_{0}^{X_D(y')} G(x_D,y,x',y')eN_D dy' = 0 \qquad \text{(A1-5)}$$

It can be shown from (A1-1) and (A1-2) that

$$G(x,y,x',y') = G(x-x',\; y-x') \qquad \text{(A1-6a)}$$

$$\int_{-\infty}^{+\infty} G(x,y,o,y')dy' = \frac{d_o}{\varepsilon_2} = \frac{1}{C_o} \qquad \text{(A1-6b)}$$

$$\int_{-\infty}^{+\infty} G(o,y,x',y')dy' = \frac{d_o}{\varepsilon_2} = \frac{1}{C_o} \qquad \text{(A1-6c)}$$

$$\int_{-\infty}^{+\infty} \frac{\partial G}{\partial y}(x,y,x',y')dy' = 0 \qquad \text{(A1-6d)}$$

where C_o is the insulator capacity per unit area. In the case when q(y) is a constant, using Eqs. (A1-4), (A1-5), and (A1-6), the surface potential is given by

$$\Phi_s = V_G + \frac{q}{C_o} + \frac{eN_D X_D}{C_o} \tag{A1-7a}$$

$$V_G + \frac{q}{C_o} + \frac{eN_D X_D}{C_o} - \frac{eN_D X_D^2}{2\varepsilon_1} = 0 \tag{A1-7b}$$

Equations (A1-7a and b) are the one-dimensional solutions of the Poisson equation using the depletion approximation for the MIS structure.[32] For a given surface charge density profile, the surface potential gradient can be obtained according to the gradual channel approximation by differentiating (A1-7a)

$$\frac{\partial \Phi_s}{\partial y} = \frac{1}{C_o}\frac{\partial q}{\partial y} + \frac{eN_D}{C_o}\frac{\partial X_D}{\partial y} \tag{A1-8}$$

A more accurate estimation of the surface potential gradient can be obtained from Eqs. (A1-4) and (A1-6).

$$\frac{\partial \Phi_s}{\partial y} = \int_{-\infty}^{+\infty} \frac{\partial G}{\partial y}(o,y,o,y')q(y')dy' + \int_{-\infty}^{+\infty} dy' \int_{0}^{X_D(y')} \frac{\partial G}{\partial y}(o,y,x',y')eN_D dx' \tag{A1-9}$$

The first term in the above equation represents the repulsive force due to the nonuniform surface charge q(y), screened by the metal electrode. The second term represents the repulsive force from the ionized fixed impurity atoms due to the nonuniform depeletion region thickness. Let us consider the first term, from Eq. (A1-3)

$$\frac{\partial G}{\partial y}(o,y,o,y') = \frac{-1}{\pi(\varepsilon_1+\varepsilon_2)}\left\{\frac{1}{y-y'} - \frac{2\varepsilon_2}{(\varepsilon_1+\varepsilon_2)}\sum_{m=1}^{\infty}\left(\frac{\varepsilon_1-\varepsilon_2}{\varepsilon_1+\varepsilon_2}\right)^{m-1}\frac{(y-y')}{(y-y')^2+(2md_o)^2}\right\} \qquad (A1\text{-}10)$$

For the silicon oxide, silicon substrate

$$\frac{2\varepsilon_2}{\varepsilon_1+\varepsilon_2} \simeq \frac{1}{2} \qquad \text{and} \quad \frac{\varepsilon_1-\varepsilon_2}{\varepsilon_1+\varepsilon_2} \simeq \frac{1}{2} \quad .$$

Thus the successive terms in the above series decrease rapidly. So the Green function $(\partial G/\partial y)$ decreases rapidly within a region of a few d_o from y, however not as rapid as it would be if $\varepsilon_2 = \varepsilon_1$. Hence, we may expand $q(y')$ as a Taylor series about y. Since $(\partial G/\partial y)$ is odd, all even terms in the expansion vanish. If the variation of the surface charge $q(y)$ is small over a distance on the order of a few oxide thicknesses d_o, $(\partial^3 q(y')/\partial y'^3)$ and higher derivations may be neglected. Hence.

$$\int_{-\infty}^{+\infty}\frac{\partial G}{\partial y}(o,y,o,y')q(y')dy' = +\frac{\partial q}{\partial y}\int_{-\infty}^{+\infty}G(o,y,o,y')dy' = \frac{\frac{\partial q}{\partial y}}{C_o} \qquad (A1\text{-}11)$$

This is the result obtained in the first term of the one-dimensional solution in Eq. (A1-8). So if the variation of the depletion layer width is neglected, the surface potential gradient obtained by differentiating the one-dimensional solution in Eq. (A1-7a) includes the charge repulsion effect, and gives a reasonably accurate estimate of the self-induced fields when the lateral variation of the surface charge density over a distance on the order of several oxide thickness is small. The error in this estimate depends upon the charge

profile and may be positive or negative.

Similarly the contribution of the second term in Eq. (A1-9) can be shown to be almost equal to the value obtained from the second term of the one-dimensional solution in Eq. (A1-8) when the lateral variation of the charge over a distance on the order of the depletion region thickness is small.

The surface charge density profiles under the CCD gates show that, during the charge transfer, the surface charge density varies slowly under the electrodes but rapidly in the interelectrode regions. So the gradual channel approximation gives accurate estimates of the self-induced fields under the electrode. As discussed in Chapter 3 and IV, the charge transfer in all stages is limited by the transfer of charge across the transfer gates or out of the storage gate. Hence, the error in estimating the self-induced fields in the interelectrode regions has a negligible effect on the overall charge transfer characteristics.

APPENDIX II

Derivation of the Surface Potential Gradient under the Gate Electrodes and in the Interelectrodes Regions

The one-dimensional solution of the Poisson equation using the depletion approximation gives the following relation between the surface potential ϕ_s and the surface charge density[3] q :

$$\Phi_s = V_G - V_{FB} + \frac{q}{C_o} + \frac{B}{C_o}\left[\sqrt{1 - 2\frac{C_o}{B}\left(V_G - V_{FB} + \frac{q}{C_o}\right)} - 1\right] \qquad (A2\text{-}1)$$

where $B = \frac{\varepsilon_s}{\varepsilon_{ox}} eN_D d_o$. V_G is the voltage applied to the electrode, V_{FB} is the flat band voltage, C_o is the oxide capacitance per unit area, e is the electronic charge, N_D is the donor concentration, d_o is the oxide thickness and X_d is the width of the depletion region. ε_s and ε_{ox} are the dielectric constants of silicon and silicon oxide respectively. The equilibrium surface charge density q_o is equal to $C_o(V_{Th} - V_G)$ where V_{Th} is the threshold voltage. If the surface charge profile q is not uniform then according to the gradual channel approximation, the surface potential gradient is given approximately by

$$\frac{\partial \Phi_s}{\partial x} = \frac{\partial \Phi_s}{\partial q}\frac{\partial q}{\partial x} = \frac{\partial q/\partial x}{C_o + C_D} = \frac{1}{C_o}\left[1 - \frac{1}{\sqrt{1 - 2\frac{C_o}{B}\left(V_G - V_{FB} + \frac{q}{C_o}\right)}}\right]\frac{\partial q}{\partial x} \qquad (A2\text{-}2)$$

where C_D is the depletion layer capacity. For typical oxide thickness ($\sim$1000 - 4500A), substrate doping ($\sim 10^{14}$-$10^{16}/cm^3$) and electrode voltages the above relations can be simplified to

$$\Phi_S = \Phi_{So} + \frac{q}{C} \quad \text{and} \quad \frac{\partial \Phi_S}{\partial x} = \frac{1}{C}\frac{\partial q}{\partial x} \tag{A2-3}$$

where Φ_{So} is the surface potential with no charge. C is an effective capacity given by

$$C = \frac{q_o F}{(2\Phi_F - \Phi_{So})} \tag{A2-4}$$

where $2\Phi_F$ is the surface potential at equilibrium and F is a factor less than unity to reduce the error in this approximation to less than a few percent. Numerical calculations using values of the self-induced fields given in Eqs. (A2-2) and (A2-3) show almost no difference in the charge transfer characteristics. Since the latter expression is simpler, we will use it below.

If fringing fields under the electrodes are appreciable, then Φ_{So} and q_o are functions of time and the spatial coordinate x and are given by

$$\Phi_{so}(x,t) = \Phi_{so}(t) - \int_x E_{fr}(y)\, dy \tag{A2-5}$$

$$q_o(x,t) = C_o\{[2\Phi_F - \Phi_{so}(x,t)] + \sqrt{2\varepsilon_s e N_D}\,[\sqrt{|\Phi_{so}(x,t)|} - \sqrt{|2\Phi_F|}\}} \tag{A2-6}$$

where $E_{fr}(y)$ is the fringing field profile obtained from the solution of the two dimensional Poisson equation and $\Phi_{so}(t)$ is given by Eq. (A2-1) with $q = 0$. The surface potential under the electrode

is thus given by

$$\Phi_s(x,t,q) = \Phi_{so}(x,t) + \frac{(2\Phi_F - \Phi_{so}(x,t))q}{q_o(x,t)\ F} \qquad \text{(A2-7)}$$

In the interelectrode regions the surface potential is also given by

$$\Phi_S(x,t,q) = P(x,t) + \frac{(2\Phi_F - P(x,t))q}{C(x,t)} \qquad \text{(A2-8)}$$

where $P(x,t)$ and $C(x,t)$ are the surface potential with no charge and the equilibrium surface charge density respectively, both approximated by a smooth interpolating polynomial. From Eqs. (A2-7) and (A2-8) the surface potential gradient under the electrodes and in the interelectrode regions can be written in the following form

$$\frac{\partial \Phi_S}{\partial x}(x,t,q) = L(x,t) + M(x,t)q + N(x,t)\frac{\partial q}{\partial x} \qquad \text{(A2-9)}$$

APPENDIX III

Numerical Solution

We have shown that the continuity equation describing the dynamics of the charge transport in charge coupled devices under the electrodes and the interelectrode regions could be reduced to the nonlinear diffusion equation

$$\frac{\partial q'}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial q'}{\partial x} + \mu q'(L(x,t) + M(x,t)q' + N(x,t)\frac{\partial q'}{\partial x})\right] \quad \text{(A3-1)}$$

where q' is the surface charge density. Before proceeding with the numerical formulation and solution of the problem, it is convenient to scale the variables according to the following definitions

$$y = \frac{x}{L_o}\ , \qquad \phi = \frac{\Phi}{V_o}\ , \qquad q = \frac{q'}{q_o} \qquad \text{and} \quad \tau = \frac{t}{t_o} \qquad \text{(A3-2)}$$

The units L_o, V_o, q_o and t_o are chosen to be as natural to the problem as possible

$$\left.\begin{aligned} L_o &= 1 \text{ micron}\ , & V_o &= 1 \text{ Volt}\ , \\ q_o &= 10^{-8} \text{ Coulomb/cm}^2 & \text{and } t_o &= \frac{L_o^2}{\mu V_o} \end{aligned}\right\} \qquad \text{(A3-3)}$$

The nonlinear diffusion equation in (A3-1) scales to:

$$\frac{\partial q}{\partial \tau} = \frac{\partial}{\partial y}\left[a\ \frac{\partial q}{\partial y} + q(l(y,\tau) + m(y,\tau)\ q + k(y,\tau)\ \frac{\partial q}{\partial y})\right] \qquad \text{(A3-4)}$$

where

$$a = KT/V_o \quad , \qquad m(y,\tau) = M(x,t)\frac{L_o q_o}{V_o}$$

$$l(y,\tau) = L(x,t)\frac{L_o}{V_o} \quad , \qquad k(y,\tau) = N(x,t)\frac{q_o}{V_o} \tag{A3-5}$$

Thus the dynamics of the charge transfer in each bit of the charge coupled device is described by equations similar to Eq. (A3-4) with the appropriate functions l, m and k under the storage and transfer electrodes. In the interelectrode regions the nonlinear diffusion equation can be written in the following form

$$\frac{\partial q}{\partial} = \frac{\partial}{\partial y}[a\,\frac{\partial q}{\partial y} + q(\alpha(y,\tau) + \beta(y,\tau)\,q + \gamma(y,\tau)\,\frac{\partial q}{\partial y})] \tag{A3-6}$$

At the junction points between the different regions, the surface potential and surface charge density must be continuous and the current must be conserved. From the details of the charge storage and charge transfer shown in Figs. (11),(18),(19) and (25) for the problem of charge transfer inside one bit of the device continuity conditions between the left end of the first transfer gate and the right end of the second storage gate could be used. But for the problem of charge transfer from the first storage gate to the second storage gate in the first half cycle, boundary conditions that describe the fact that the current at the left end of the first storage gate being discharged and the right end of the second storage being charged are zero, should be used. In this case the boundary conditions are

$$\left[a\frac{\partial q}{\partial y} + q(\alpha_1 + \beta_1 q + \gamma_1 \frac{\partial q}{\partial y})\right] = 0 \quad \text{at } y = y_1$$

$$\left[a\frac{\partial q}{\partial y} + q(\alpha_4 + \beta_4 q + \gamma_4 \frac{\partial q}{\partial y})\right] = 0 \quad \text{at } y = y_{J+1} \qquad \text{(A3-7)}$$

for all times. The charge transfer in the second half cycle can be handled in a similar way.

We have used a new finite difference scheme, the Box scheme,[8] to solve the above set of nonlinear equations. One of the basic ideas of this scheme is to write the system of the nonlinear partial differential equations in the form of a first order system. Thus derivatives of the surface charge density, which is the function we are solving for, with respect to the spatial coordinate must be introduced as a new unknown function. With the resulting first order system and on an arbitrary rectangular net, simple centered difference quotients and averages at the midpoints of the net rectangles and the net segments are used to get accurate finite difference equations of order $O(h^2) + O(\Delta t^2)$. The resulting difference equations are highly implicit and nonlinear. Newton's method is employed to solve them using a block-tridiagonal factorization technique. This scheme has a number of very desirable features that made it very suitable for solving the system for nonlinear diffusion equations describing the charge transport dynamics of CCD. These features are

(i) it is simple, easy to program, efficient and stable,

(ii) it has second order accuracy with nonuniform nets. This is especially important, as small net spacing can be used in the interelectrode regions, where the surface charge density is changing

rapidly, while large net spacing can be used in the other regions where the surface charge density gradient is small.

(ii) Both the surface charge density and surface charge density gradient are approximated with the same accuracy. This is again especially important since the current continuity at the boundaries between the different regions involves the surface charge density and its gradient.

Numerical Formulation

A crucial step in the numerical procedure is to reformulate the problem in terms of a first order system of partial differential equations. For this purpose we introduce a new dependent variable $v(y,\tau)$ so that Eqs. (A5-6) or (A5-7) can be written as:

$$v(y,\tau) = \frac{\partial}{\partial y} q(y,\tau) \qquad \text{(A3-8a)}$$

$$\frac{\partial q}{\partial \tau} = \frac{\partial}{\partial y} [a\, v + q(1 + mq + kv)] \qquad \text{(A3-8b)}$$

Let the net points be given by

$$y_1 = 0\ ,\quad y_j = y_{j-1} + h_j\ ,\quad j = 2,3 \text{ --- } J+1$$
$$\tau_1 = 0\ ,\quad \tau_n = \tau_{n-1} + (\Delta\tau)_n\ ,\quad n = 2,3 \text{ --- } N+1 \qquad \text{(A3-9)}$$

The net spacings, h_j and $(\Delta\tau)_n$, are completely arbitrary and may have large variations. This is especially important in the charge transfer problem. In the interelectrode regions, where the surface charge density changes rapidly, the spatial net spacing can be small while in the other regions, where the surface charge density gradient is small, the spatial net spacing may be large.

The quantities (q,v) will be approximated at points (y_j, τ_n) of the net by net functions denoted by (q_j^n, v_j^n). We also employ the following notation, for points and quantities midway between net points and for any net function (1_j^n)

$$\text{(a)}\quad \tau_{n-\frac{1}{2}} \equiv \frac{1}{2}(\tau_n + \tau_{n-1}) \ , \quad y_{j-\frac{1}{2}} \equiv \frac{1}{2}(y_j + y_{j-1})$$

$$\text{(b)}\quad 1_j^{n-\frac{1}{2}} \equiv \frac{1}{2}(1_j^n + 1_j^{n-1}) \ , \quad 1_{j-\frac{1}{2}}^n \equiv \frac{1}{2}(1_j^n + 1_{j-1}^n) \qquad \text{(A3-10)}$$

$$\text{(c)}\quad D_t^- 1_j^n = (\Delta\tau_n)^{-1}(1_j^n - 1_j^{n-1}), \ D_y^- 1_j^n = (h_j)^{-1}(1_j^n - 1_{j-1}^n)$$

The difference equations which are to approximate (A3-8) are now easily formulated by considering one mesh rectangle as in Fig. (39). We simply approximate (A3-8a) using centered difference quotients and averages about the mid-point $(y_{j-\frac{1}{2}}, \tau_n)$ of the segment p_2p_3. Similarly (A3-8b) is approximated by centering about the mid-point $(y_{j-\frac{1}{2}}, \tau_{n-\frac{1}{2}})$ of the rectangle $p_1p_2p_3p_4$. The only ambiguity or choice in the above indicated approximations concerns the nonlinear terms. We may take averages of products, as in $q\,v \simeq (qv)_{j-\frac{1}{2}}^{n-\frac{1}{2}}$, or products of averages, as in $qv \approx q_{j-\frac{1}{2}}^{n-\frac{1}{2}}\, v_{j-\frac{1}{2}}^{n-\frac{1}{2}}$. Since the former is simpler, in the computations reported here we have used it. Thus the difference approximations to (A3-8) are:

$$\text{(a)}\quad v_{j-\frac{1}{2}}^n = D_y^- q_j^n$$

$$\text{(b)}\quad D_\tau^- q_{j-\frac{1}{2}}^n = D_y^-[a\,v + 1q + mq^2 + kqv)_y^{n-\frac{1}{2}} \qquad \text{(A3-11)}$$

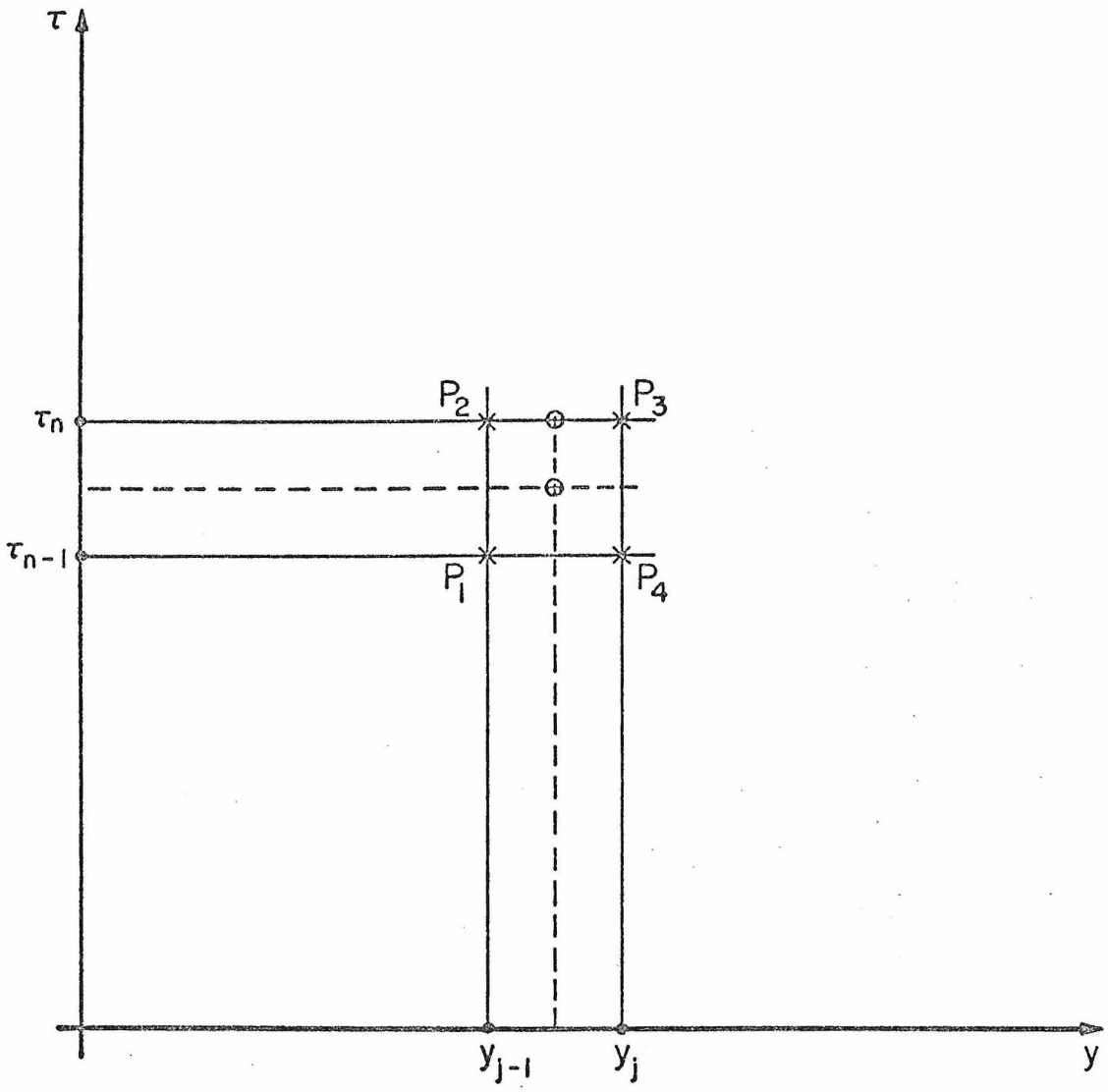

Figure 39.

Using the notation defined in Eqs. (A3-10 and (A3-11) can be re-written:

$$(a)\quad \tfrac{1}{2}(v_j^n + v_{j-1}^n) = (h_j)^{-1}(q_j^n - q_{j-1}^n)$$

$$(b)\quad (\Delta\tau_n)^{-1}[\tfrac{1}{2}(q_j^n + q_{j-1}^n) - \tfrac{1}{2}(q_j^{n-1} + q_{j-1}^{n-1})] =$$

$$(h_j)^{-1}\{\tfrac{1}{2}[a\ v_j^n + l_j^n\ q_j^n + m_j^n(q_j^n)^2 + k_j^n(q_j^n\ v_j^n)]$$

$$+ \tfrac{1}{2}[a\ v_j^{n-1} + l_j^{n-1}\ q_j^{n-1} + m_j^{n-1}(q_j^{n-1})^2 + k_j^{n-1}(qv)_{j-1}^n]$$

$$- \tfrac{1}{2}[a\ v_{j-1}^n + l_{j-1}^n\ q_{j-1}^n + m_{j-1}^n(q^2)_{j-1}^n + k_{j-1}^n(qv)_{j-1}^n]$$

$$- \tfrac{1}{2}[a\ v_{j-1}^{n-1} + l_{j-1}^{n-1}\ q_{j-1}^{n-1} + m_{j-1}^{n-1}\ (q^2)_{j-1}^{n-1} + k_{j-1}^{n-1}(qv)_{j-1}^{n-1}]\} \qquad \text{(A3-12)}$$

Eqs. (A3-11) and (A3-12) are imposed for $j = 2,3, \text{---} J + 1$ (except at the junction points between the different regions). Since we assume (q_j^{n-1}, v_j^{n-1}) to be known for $1 \le j \le J + 1$ and (q_j^n, v_j^n) to be unknown for $1 \le j \le J + 1$, we rewrite Eq. (A3-12)

$$(a)\quad \frac{h_j}{2}(v_j^n + v_{j-1}^n) = (q_n^n - q_{j-1}^n)$$

$$(b)\quad [a\ v_j^n + l_j^n\ q_j^n + m_n^n(q_j^n)^2 + k_j^n(q_j^n\ v_j^n)]/$$

$$h_j - [a\ v_{j-1}^n + l_{j-1}^n\ q_{j-1}^n + m_{j-1}^n(q_{j-1}^n)^2 + k_{j-1}^n(q_{j-1}^n\ v_{j-1}^n)]/$$

$$h_j - \frac{1}{(\Delta\tau_n)}[q_j^n + q_{j-1}^n] = T_j^{n-\frac{1}{2}} \qquad \text{(A3-13)}$$

where

$$T_{j-\frac{1}{2}}^{n-1} = -[a\ v_j^{n-1} + l_j^{n-1}\ q_j^{n-1} + m_j^{n-1}(q_j^{n-1})^2 + k_j^{n-1}(q_j^{n-1}\ v_j^{n-1})]/$$

$$h_j + [a\ v_{j-1}^{n-1} + l_{j-1}^{n-1}\ q_{j-1}^{n-1} + m_{j-1}^{n-1}(q_{j-1}^{n-1})^2 + k_{j-1}^{n-1}(q_{j-1}^{n-1}\ v_{j-1}^{n-1})]/$$

$$h_j - \frac{1}{(\Delta\tau_n)}[q_j^{n-1} + q_{j-1}^{n-1}] \qquad \text{(A3-14)}$$

The boundary conditions at the extreme ends y_1 and y_{J+1} can be similarly written

$$\text{(a)}\quad a\ v_1^n + (\alpha_1)_1^n\ q_1^n + (\beta_1)_1^n\ (q_1^n)^2 + (\gamma_1)_1^n\ (q_1^n\ v_1^n) = 0 \text{ at } y = y_1$$

$$\text{(b)}\quad a\ v_{J+1}^n + (\alpha_4)_{J+1}^n\ q_{J+1}^n + (\beta_4)_{J+1}^n\ (q_{J+1}^n)^2$$

$$+ \gamma_{J+1}^n\ (q_{J+1}^n\ v_{J+1}^n) = 0 \quad \text{at } y = y_{J+1} \qquad \text{(A3-15)}$$

At the junctions between the different regions, the spatial net is chosen such that two net points coincide there, e.g. $y_i = y_{i-1}$ where y_i denotes the net points at the different junctions. Since the interpolating function $P_s(x,t)$ and $C(x,t)$ in Eq. (A2-14) were chosen to approximate the surface potential with no charge and the equilibrium surface charge density smoothly, the continuity of the surface potential and surface charge density at the junction point requires:

$$q_i^n = q_{i-1}^n \quad , \quad h_i = 0 \qquad \text{(A3-16)}$$

The conservation of charge across the junction point requires

$$[a\ v_i^n + l_i^n\ q_i^n + m_i^n\ (q_i^n)^2 + k_i^n\ (q_i^n\ v_i^n)] =$$

$$[a\ v_{i-1}^n + \alpha_{i-1}^n\ q_{i-1}^n + \beta_{i-1}^n (q_{i-1}^n)^2 + \gamma_{i-1}^n (q_{i-1}^n\ v_{i-1}^n)] \quad \text{(A3-17)}$$

where the appropriate functions (l,m,k) and (α,β,γ) have to be used according to the junction point under consideration. Eqs. (A3-16) and (A3-17) describe the continuity and charge conservation to the same order of accuracy of the finite difference equations in (A3-14).

Solutions of the Finite Difference Equations

If we assume (q_j^{n-1}, v_j^{n-1}) to be known for $1 \le j \le J + 1$ then Eqs. (A3-13), (A3-15), (A3-16) and (A3-17) are a system of $(2J + 2)$ nonlinear equations for the determinations of $(2J + 2)$ unknowns (q_j^n, v_j^n), $1 \le j \le J + 1$. We shall solve this nonlinear system by means of Newton's method. For simplicity of notation we shall write the unknowns at $t = \tau_n$ as $(q_j^n, v_j^n) \equiv (q_j, v_j)$. Then the system of Eqs. (A3-13), (A3-16) and (A3-17) can be written as:

$$\text{(a)}\quad q_j - q_{j-1} - \frac{h_j}{2}(v_j + v_{j-1}) = 0$$

$$\text{(b)}\quad [a\ v_j + l_j q_j + m_j q_j^2 + k_j q_j v_j]/h_j - [a\ v_{j-1} + l_j\ q_{j-1} +$$

$$m_{j-1}\ q_{j-1}^2 + k_{j-1}\ q_{j-1}\ v_{j-1}]/$$

$$h_j - \frac{1}{(\Delta\tau)_n}\ [q_j + q_{j-1}] = T_j^{n-1} - \tfrac{1}{2}$$

(c) $q_i = q_{i-1}, \quad h_i = 0$

(d) $a\, v_i + l_i q_i + m_i q_i^2 + k_i q_i v_i = a\, v_{i-1} + \alpha_{i-1} q_{i-1} + \beta_{i-1}(q_{i-1})^2$

$+ \gamma_{i-1}(q_{i-1}\, v_{i-1})$ (A3-18)

where (a) and (b) apply for $j = 2,3, \text{---} J + 1$ except at the junction points. (c) and (d) apply at the junction points between the different regions only. Similarly the boundary conditions in (A3-15) can be written as

(a) $a\, v_1 + (\alpha_1)_1\, q_1 + (\beta_1)_1\, q_1^2 + (\gamma_1)_1\, q_1\, v_1 = 0$

(b) $a\, v_{J+1} + (\alpha_4)_{J+1}\, q_{J+1} + (\beta_4)_{J+1}\, q_{J+1}^2 + (\gamma_4)_{J+L}\, q_{J+1}\, v_{J+1} = 0$

(A3-19)

We note that $T_{J-\frac{1}{2}}^{n-1}$ involves only known quantities if we assume the solution is known at $\tau = \tau_{n-1}$. To solve (A3-18) and (A3-19) by Newton's method we introduce the iterates $q_j^{(i)}$, $v_j^{(i)}$ $i = 0,1,2,\ldots$ with initial values; say:

$$q_j^{(o)} = q_j^{n-1}, \quad v_j^{(o)} = v_j^{n-1} \text{ for } 1 \le j \le J + 1 \qquad \text{(A3-20)}$$

For higher order iterates we set

$$q_j^{(i+1)} = q_j^{(i)} + \delta q_j^{(i)}, \quad v_j^{(i+1)} = v_j^{(i)} + \delta v_j^{(i)} \text{ for } 1 \le j \le J + 1 \qquad \text{(A3-21)}$$

Then we insert these expressions in place of (q_j, v_j) in equation

Eqs. (A3-18) and, drop the terms that are quadratic in $\delta q_j^{(i)}$, $\delta v_j^{(i)}$. This procedure yields the following linear system:

$$\text{(a)}\quad (\delta q_j^{(i)} - \delta q_{j-1}^{(i)}) - \frac{h_j}{2}(\delta v_j^{(i)} + \delta v_{j-1}^{(i)}) = r_{j-\frac{1}{2}}^{(i)}$$

$$\text{(b)}\quad \delta q_j^{(i)}\,\theta_j^{(i)} + \delta v_j^{(i)}\,\phi_j^{(i)} - \delta q_{j-1}^{(i)}\,\bar{\theta}_j^{(i)} - \delta v_{j-1}^{(i)}\,\bar{\phi}_j^{(i)} = t_{j-\frac{1}{2}}^{(i)}$$

$$\text{(c)}\quad \delta q_i - \delta q_{i-1} = 0; \quad h_i = 0$$

$$\text{(d)}\quad \delta q_i^{(i)}\,\theta_i^{(i)} + \delta v_i^{(i)}\,\phi_i^{(i)} - \delta q_{i-1}\,\bar{\theta}_i^{(i)} - \delta v_{i-1}^{(i)}\,\bar{\phi}_i^{(i)} = t_{i-\frac{1}{2}}^{(i)}$$

(A3-22)

where (a) and (b) hold for j = 2,3, --- J + 1 except at the junction points while (c) and (d) hold only at the junction points between the different regions. Here we have introduced:

$$\text{(a)}\quad r_{j-\frac{1}{2}}^{(i)} = q_{j-1}^{(i)} - q_j^{(i)} + h_j\,v_{j-\frac{1}{2}}^{(i)}$$

$$\text{(b)}\quad \theta_j^{(i)} = [2\,q_j^{(i)}\,m_j + v_j^{(i)}k_j + 1_j]/h_j - (\Delta\tau_n)^{-1}$$

$$\text{(c)}\quad \Phi_j^{(i)} = [a + q_j^{(i)}\,k_j]/h_j$$

$$\text{(d)}\quad \bar{\theta}_j^{(i)} = [2\,q_{j-1}^{(i)}\,m_{j-1} + v_{j-1}^{(i)}\,k_{j-1} + 1_{j-1}]/h_j + (\Delta\tau_n)^{-1}$$

$$\text{(e)}\quad \bar{\phi}_j^{(i)} = [a + q_{j-1}^{(i)}\,k_{j-1}]/h_j$$

$$(f)\quad t_{j-\frac{1}{2}}^{(i)} = T_{j-\frac{1}{2}}^{(i)} - [a\, v_j^{(i)} + l_j q_j^{(i)} + m_j (q_j^{(i)})^2 + k_j q_j^{(i)}\, v_j^{(i)}]/h_j$$

$$+ [a\, v_{j-1}^{(i)} + l_{j-1}\, q_{j-1}^{(i)} + m_j (q_{j-1}^{(i)})^2 + k_{j-1}\, q_{j-1}^{(i)}\, v_{j-1}^{(i)}]/h_j$$

$$+ (\Delta\tau_n)^{-1}\, (q_j^{(i)} + q_{j-1}^{(i)})$$

$$(g)\quad \theta_i^{(i)} = [l_i + 2\, m_i q_i^{(i)} + k_i\, v_i^{(i)}]$$

$$\phi_i^{(i)} = [a + k_i\, q_i^{(i)}]$$

$$\overline{\theta}_i^{(i)} = [\alpha_{i-1} + 2\, \beta_{i-1}\, q_{i-1}^{(i)} + \gamma_{i-1}\, v_{i-1}^{(i)}]$$

$$\overline{\phi}_i^{(i)} = [a + \gamma_{i-1}\, q_{i-1}^{(i)}]$$

$$t_{i-\frac{1}{2}}^{(i)} = - [a\, v_i^{(i)} + l_i q_i^{(i)} + m_i (q_i^{(i)})^2 + k_i\, q_i^{(i)}\, v_i^{(i)}]$$

$$+ [a\, v_{i-1}^{(i)} + \alpha_{i-1}\, q_{i-1}^{(i)} + \beta_{i-1} (q_{i-1}^{(i)})^2 + \gamma_{i-1}\, q_{i-1}^{(i)}\, v_{i-1}^{(i)}]$$

$$r_{i-\frac{1}{2}}^{(i)} = 0 \qquad \text{(A3-23)}$$

Following the same procedure for the boundary conditions in (A3-19), we get:

$$(a)\quad \delta q_1^{(i)}\, \theta_0^{(i)} + \delta u_1^{(i)}\, \phi_0^{(i)} = t_0^{(i)}$$

$$(b)\quad \delta q_{J+1}^{(i)}\, \theta_{J+2}^{(i)} + \delta u_{J+1}^{(i)}\, \phi_{J+2}^{(i)} = t_{J+2}^{(i)} \qquad \text{(A3-24)}$$

$$(a)\quad \theta_o^{(i)} = (\alpha_1)_1 + 2(\beta_1)_1\, q_1^{(i)} + (\gamma_1)_1\, v_1^{(i)}$$

$$(b)\quad \phi_o^{(i)} = a + (\gamma_1)_1\, q_1^{(i)}$$

$$(c)\quad t_o^{(i)} = -\left[a\, v_1^{(i)} + (\alpha_1)_1\, q_1^{(i)} + (\beta_1)_1\, (q_1^{(i)})^2 + (\gamma_1)_1\, q_1^{(i)}\, v_1^{(i)}\right]$$

$$(d)\quad \theta_{J+2}^{(i)} = (\alpha_4)_{J+1} + 2(\beta_4)_{J+1}\, q_{J+1}^{(i)} + (\gamma_4)_{J+1}\, v_{J+1}^{(i)}$$

$$(e)\quad \phi_{J+2}^{(i)} = a + (\gamma_4)_{J+1}\, q_{J+1}$$

$$(f)\quad t_{J+2}^{(i)} = -\left[a\, v_{J+1}^{(i)} + (\alpha_4)_{J+1}\, q_{J+1}^{(i)} + (\beta_4)_{J+1}\, (q_{J+1}^{(i)})^2 + (\gamma_4)_{J+1}\, q_{J+1}^{(i)}\, v_{J+1}^{(i)}\right] \qquad \text{(A3-25)}$$

The linear system in (A3-22) and (A3-24) can be solved in an extremely efficient manner since it has a block tri-diagonal structure. To clarify the solution procedure we write our system in matrix-vector form. There are many ways in which this can be done. They are all equivalent and merely amount to different permutations of the equations or the unknowns or both. We will describe here the formulation and procedure we employed in our calculations.

We define the two dimensional vectors $\underset{\sim}{\delta}_j^{(i)}$ and $\underset{\sim}{\tau}_j^{(i)}$ and the 2 X 2 matrices $L_j^{(i)}$ and $R_j^{(i)}$ by:

$$(a)\quad \underset{\sim}{\delta}_j^{(i)} = \begin{pmatrix} \delta q_j^{(i)} \\ \delta v_j^{(i)} \end{pmatrix} \qquad \underset{\sim}{\tau}_j^{(i)} = \begin{pmatrix} t_{j-\frac{1}{2}}^{(i)} \\ r_{j-\frac{1}{2}}^{(i)} \end{pmatrix}$$

$$(b)\quad R_j^{(i)} = \begin{pmatrix} \theta_j^{(i)} & \phi_j^{(i)} \\ 1 - \frac{h_j}{2} & \end{pmatrix}, \quad L_j^{(i)} = \begin{pmatrix} \overline{\theta}_j^{(i)} & \overline{\phi}_j^{(i)} \\ 1 & \frac{h_j}{2} \end{pmatrix} \qquad \text{(A3-26)}$$

In terms of these quantities the system (A3-22) can be simply written as:

$$R_j^{(i)} \underset{\sim}{\delta}_j^{(i)} - L_j^{(i)} \underset{\sim}{\delta}_{j-1}^{(i)} = \underset{\sim}{\tau}_j^{(i)}$$

$$j = 2,3, \text{---} J + 1 \qquad \text{(A3-27)}$$

We also write the boundary conditions in (A3-24) in a matrix-vector form

$$M_o \underset{\sim}{\delta}_1^{(i)} = t_o^{(i)}, \qquad N_{J+1} \underset{\sim}{\delta}_{J+1}^{(i)} = t_{J+2}^{(i)} \qquad \text{(A3-28)}$$

where we have introduced the row matrices .

$$M_o = (\theta_o^{(i)} \ \phi_o^{(i)})$$

$$N_{J+1} = (\theta_{J+2}^{(i)} \ \phi_{J+2}^{(i)}) \qquad \text{(A3-29)}$$

Now the complete linear system in Eqs. (A3-27) and (A3-28) which is just (A3-22) and (A3-24) in compact form, can be written in compound block-matrix-vector notation as

$$(a)\quad W^{(i)} \underset{\sim}{\delta}^{(i)} = S^{(i)}$$

where

$$(b)\quad W^{(i)} = \begin{pmatrix} M_o^{(i)} & & & 0 \\ -L_2^{(i)} & R_2^{(i)} & & \\ & & -L_{J+1}^{(i)} & R_{J+1}^{(i)} \\ 0 & & & N_{J+1} \end{pmatrix} \qquad \text{(A3-30)}$$

$$\underset{\sim}{\delta}^{(i)} = \begin{pmatrix} \underset{\sim}{\delta}_1^{(i)} \\ \underset{\sim}{\delta}_2^{(i)} \\ \\ \underset{\sim}{\delta}_{J+1}^{(i)} \end{pmatrix} \qquad \underset{\sim}{S}^{(i)} = \begin{pmatrix} t_o^{(i)} \\ \underset{\sim}{\tau}_2^{(i)} \\ \underset{\sim}{\tau}_{J+1}^{(i)} \\ t_{J+2}^{(i)} \end{pmatrix}$$

It is now clear that the non-zero elements in the coefficient matrix above are clustered about the diagonal. We have used a block-tridiagonal factorization scheme to solve the system (A3-30).

The coefficient matrix $W^{(i)}$ is of order 2J+2 and the vectors $\underset{\sim}{\delta}^{(i)}$ and $\underset{\sim}{S}^{(i)}$ have also this dimension. We decompose $W^{(i)}$ into 2 X 2 blocks starting with the upper left hand corner. We also write $S^{(i)}$ in terms of (J+1) vectors of dimensions 2; this is already done for $\underset{\sim}{\delta}^{(i)}$. Thus we rewrite (A5-30b) as:

$$(a)\quad W^{(i)} = \begin{pmatrix} A_1^{(i)} & C_1^{(i)} & & & & & 0 \\ B_2^{(i)} & A_2^{(i)} & C_2^{(i)} & & & & \\ & & & B_j^{(i)} & A_j^{(i)} & C_j^{(i)} & \\ 0 & & & & & B_{J+1}^{(i)} & A_{J+1}^{(i)} \end{pmatrix}$$

where:

$$(b)\quad A_o^{(i)} = \begin{pmatrix} \theta_o^{(i)} & \phi_o^{(i)} \\ -\bar{\theta}_2^{(i)} & -\bar{\phi}_2^{(i)} \end{pmatrix} \qquad A_j^{(i)} = \begin{pmatrix} 1 & -\frac{h_j}{2} \\ -\theta_{J+1}^{(i)} & -\bar{\phi}_{J+1}^{(i)} \end{pmatrix}$$

$$2 \le j \le J$$

$$A_{J+1}^{(i)} = \begin{pmatrix} 1 & -\frac{h_{J+1}}{2} \\ \theta_{J+2}^{(i)} & \phi_{J+2}^{(i)} \end{pmatrix}$$

$$(c)\quad B_j^{(i)} = \begin{pmatrix} -1 & -\frac{h_j}{2} \\ 0 & 0 \end{pmatrix} \qquad \text{for } 2 \le j \le J$$

$$B_{J+1}^{(i)} = \begin{pmatrix} -1 & -\frac{h_{J+1}}{2} \\ 0 & 0 \end{pmatrix}$$

$$\text{(d)}\quad C_1^{(i)} = \begin{pmatrix} 0 & 0 \\ \theta_2^{(i)} & \phi_2^{(i)} \end{pmatrix} \qquad C_j^{(i)} = \begin{pmatrix} 0 & 0 \\ \theta_{J+1}^{(i)} & \phi_{J+1}^{(i)} \end{pmatrix}$$

$$2 \le j \le J$$

$$\text{(e)}\quad S^{(i)} = \begin{pmatrix} \underset{\sim}{S}_1^{(i)} \\ \underset{\sim}{S}_2^{(i)} \\ S_{J+1}^{(i)} \end{pmatrix} \qquad \underset{\sim}{S}_1^{(i)} = \begin{pmatrix} t_0^{(i)} \\ t_{2\ -\ \frac{1}{2}}^{(i)} \end{pmatrix}$$

$$\underset{\sim}{S}_j^{(i)} = \begin{pmatrix} r_{j\ -\ \frac{1}{2}}^{(i)} \\ t_{j\ +\ \frac{1}{2}}^{(i)} \end{pmatrix} \qquad S_{J+1}^{(i)} = \begin{pmatrix} r_{J\cdot +\ \frac{1}{2}}^{(i)} \\ t_{J\ +\ 2}^{(i)} \end{pmatrix} \qquad \text{(A3-31)}$$

$$2 \le j \le J$$

The system (A3-30) using the structure (A3-31) can be solved by a standard block tri-diagonal factorization procedure.[33] For completeness we include here the relevant recursions. We determine 2 X 2 matrices $D_j^{(i)}$ and $E_j^{(i)}$ from the relation

$$\text{(a)}\quad D_1^{(i)} = A_1^{(i)}; \quad E_j^{(i)} = (D_j^{(i)})^{-1}\, C_j^{(i)} \qquad 1 \le j \le J$$

$$\text{(b)}\quad D_j^{(i)} = A_j^{(i)} - B_j^{(i)}\, E_{j-1}^{(i)} \qquad 2 \le j \le J+1 \qquad \text{(A3-32)}$$

As these matrices are computed the matrices $A_j^{(i)}$ and $C_j^{(i)}$ can be eliminated from the computer storage as they will no longer be required. Next we compute the intermediate vectors $Z_j^{(i)}$ from the

forward recursion:

$$\underset{\sim}{Z}_1^{(i)} = [D_1^{(i)}]^{-1}\ \underset{\sim}{S}_1^{(i)}\ ;$$

$$\underset{\sim}{Z}_j^{(i)} = [D_j^{(i)}]^{-1}\ [\underset{\sim}{S}_j^{(i)} - B_j^{(i)}\ \underset{\sim}{Z}_{j-1}^{(i)}] \quad 2 \le j \le J+1 \qquad \text{(A3-33)}$$

Finally the solution components $\delta_j^{(i)}$ are obtained from the backward recursion:

$$\underset{\sim}{\delta}_{J+1}^{(i)} = \underset{\sim}{Z}_{J+1}^{(i)}\ ;$$

$$\underset{\sim}{\delta}_j^{(i)} = \underset{\sim}{Z}_j^{(i)} - E_j^{(i)}\ \underset{\sim}{\delta}_{j+1}^{(i)} \quad J \ge j \ge 1 \qquad \text{(A3-34)}$$

It is to be noticed that (A3-32a) requires $A_1^{(i)}$ to be nonsingular.

To summarize, one iteration step of Newton's method is carried out as follows:

(i) The $T_{J-\frac{1}{2}}^{n-1}$ are computed from Eq. (A3-14) only once for all of the interations

(ii) Using the latest iterate, the quantities $\{r_{j-\frac{1}{2}}^{(i)}, t_{j-\frac{1}{2}}^{(i)}\}$ and $\{t_o^{(i)}, t_{J\pm2}^{(i)}\}$ are calculated from Eqs. (A3-23) and (A3-25). This determines the inhomogeneous terms $\underset{\sim}{S}_j^{(i)}$ in Eq. (A3-31).

(iii) The matrix elements for $\{A_j^{(i)}, B_j^{(i)}, C_j^{(i)}\}$ are next determined from Eqs. (A3-31) and (A3-23).

(iv) The factorization procedure can now be carried as outlined in Eqs. (A3-32), (A3-33) and (A3-34) to determine $\{q_j^{(i+1)}, v_j^{(i+1)}\}$ as in (A3-21).

These calculations are repeated till some convergence criterion is satisfied. In most of cour calculations we have used

the surface charge density as the confergence criterion. Iterations were stopped when

$$\text{Max}|\delta q_j| < \varepsilon_1 \qquad 1 \le j \le J+1 \tag{A3-35}$$

It should be noted that Newton's method converges quadratically if the initial guess is not too far from the solution. Actually three or four iterates were sufficient in most of our calculations to achieve the required accuracy.

For the charge transfer problem, within one bit of the CCD structure shown in Fig. (4) four hundred net points were enough to solve the nonlinear set of equations under all the electrodes. The net spacing varied widely from 10^{-4} microns to ½ micron. In this way the surface charge density change from one net point to the next is about the same. With this nonuniform net a high accuracy is obtained with great economy by using the box scheme as mentioned before. The time steps were automatically adjusted by the program such that convergence is achieved after three or four iteration steps at most.

Finally it is possible to estimate the error of the numerical solution. Actually there are several kinds of error to consider.

(i) The truncation error arises from the replacement of the continuous differential equations by finite difference equations. The exact numerical solution of the difference equations in (A3-11) has second order accuracy, i.e. $O(h^2) + O(\Delta\tau^2)$ for both the surface charge density and its gradient even with the nonuniform net spacing used. The easiest method to check the accuracy of the solutions is to reduce the net spacing and compare the resulting solutions. Agreement

down to the sixth digit was observed with the chosen net spacing. Although Richardson extrapolation could have been used to reduce the number of mesh points for the same accuracy, we didn't use it in most of our calculation to keep the problem simple.

(ii) The round off error arises from representing the numbers in the computer by finite number of digits. To reduce the round off error, most of the arithmetical operations and computations were done in double precision. Using single precision variables affected the iteration convergence at the latter stages of the charge transfer due probably to the accumulation of the round off error.

(iii) Iteration error results from the fact that our iteration procedure is terminated after a finite number of iteration steps. Note that the order of accuracy mentioned in (i) assumes that exact solutions of the difference equations are achieved. Accumulation of the iteration error may considerably degrade the charge conservation implied behind the set of nonlinear diffusion equations or their finite difference approximations. However, one of the virtues of Newton's method is that with quadratic convergence, the iteration error can easily be reduced to the same order of magnitude as the truncation error. If the initial error in the iteration scheme (i.e., in the initial guess) is such that $|q_j - q_j^{(o)}| = O(\Delta\tau)$ and $|v_j - v_j^{(o)}| = O(\Delta\tau)$, which is obvious from Eq. (A3-20), then by quadratic convergence of Newton's method it follows that $|q_j - q_j^{(i)}| = O[(\Delta\tau)^{2^{(i)}}]$. Thus if the tolerated errors are to be $(\Delta\tau^{2m})$, it requires only $i = 1 + \frac{\ln m}{\ln 2}$ iterations to be consistent. In practice we seldom required more than three iterations.

APPENDIX IV

Steady State Current and Charge under the Transfer Gate

Assuming that the charge redistribution time under the transfer gate is much smaller than the transfer times of interest, then the current across it and the charge under it can be approximately derived by a steady state approach.

The relation between the surface potential and surface charge density under the transfer gate according to the gradual channel approximation is given by

$$\Phi_T = \Phi_{To} + \frac{q}{C_{tr}} \qquad \text{(A4-1)}$$

where Φ_T and Φ_{To} are the surface potential under the transfer gate with charge and with no charge respectively, q is the mobile surface charge density, C_{Tr} is the effective oxide and depletion layer capacity under the transfer gate. The current I under the transfer gate is given by

$$I = W(-D \frac{\partial q}{\partial x} - \mu q \frac{\partial \Phi_T}{\partial x}) \qquad \text{(A4-2)}$$

where D and μ are the surface diffusion constant and mobility respectively, and W is the channel width. If fringing fields under the transfer gate are negligible Eq. (A4-2) may be rewritten as:

$$I = -W\mu C_{Tr}[KT \frac{\partial \Phi_T}{\partial x} + (\Phi_T - \Phi_{To}) \frac{\partial \Phi_T}{\partial x}] \quad , \qquad \text{(A4-3)}$$

where KT is the thermal voltage. If we let the surface potential at the beginning and end of the transfer be Φ_T and Φ_T', then

assuming the current I across the gate constant and integrating Eq. (A4-3) we get

$$I = \frac{\mu C_{Tr} W}{2\ell_{Tr}} [2KT(\Phi_T - \Phi_T') + (\Phi_T - \Phi_T')(\Phi_T + \Phi_T' - 2\Phi_{To})] \qquad (A4\text{-}4)$$

and

$$Q_{Tr} = \frac{2}{3} \ell_{Tr} W C_{Tr} (\Phi_T - \Phi_{To}) \frac{\{(\Phi_T - \Phi_{To}) + \frac{3}{2} KT + (\Phi_T' - \Phi_{To})[1 + \frac{3/2\ KT}{(\Phi_T - \Phi_{To})} + \frac{(\Phi_T' - \Phi_{To})}{(\Phi_T - \Phi_{To})}]\}}{\{(\Phi_T - \Phi_{To}) + (\Phi_T' - \Phi_{To}) + 2KT\}} \qquad (A4\text{-}5)$$

where ℓ_{Tr} is the length of the transfer gate and Q_{Tr} is the total charge under the transfer gate.[18] In the case the surface charge density at the end of the transfer gate is very small (as in the two-phase clocking scheme) then $\Phi_T' \approx \Phi_{To}$ and the above equations reduce to

$$I = \frac{\mu C_{Tr} W}{2\ell_{Tr}} [(\Phi_T - \Phi_{To})^2 + 2KT\ (\Phi_T - \Phi_{To})] \qquad (A4\text{-}6)$$

$$Q_{Tr} = \frac{2}{3} \ell_{Tr} W C_{Tr} (\Phi_T - \Phi_{To}) \frac{[(\Phi_T - \Phi_{To}) + \frac{3}{2} KT)]}{[(\Phi_T - \Phi_{To}) + 2KT]} \qquad (A4\text{-}7)$$

If $(\Phi_T - \Phi_{To}) >> KT$, the above equations reduce further to:

$$I = \frac{\mu C_{Tr} W}{2\ell_{Tr}} (\Phi_T - \Phi_{To})^2 \qquad \text{(A4-8)}$$

$$Q_{Tr} = \frac{2}{3} \ell_{Tr} W C_{Tr} (\Phi_T - \Phi_{To}) \qquad \text{(A4-9)}$$

The current formula in Eq. (A4-8) is the quadratic relation of the MOS transistor at pinch off, and the factor (2/3) in Eq. (A4-9) is due to the square root dependence of the surface charge density q on the distance from the end of the transfer gate.

If $(\Phi_T - \Phi_{To}) < (2KT)$, then the charge transport under the transfer gate is mainly by diffusion, and the above equations reduce to

$$I = \frac{\mu C_{Tr} W}{\ell_{Tr}} (KT)(\Phi_T - \Phi_{To}) = \frac{C_{Tr} WD}{\ell_{Tr}} (\Phi_T - \Phi_{To}) \qquad \text{(A4-10)}$$

$$Q_{Tr} = \frac{1}{2} \ell_{Tr} W C_{Tr} (\Phi_T - \Phi_{To}) \qquad \text{(A4-11)}$$

The factor (1/2) in Eq. (A4-10) is due to the linear dependence of the surface charge density q on the distance from the end of the transfer gate.

If the fringing fields under the transfer gates are appreciable then the above current relations still hold approximately after replacing (KT) and (D/ℓ_{Tr}) by $(KT + \ell_{Tr}\bar{E})$ and $(D/\ell_{Tr} + \mu\bar{E})$ respectively, where $\bar{E}$ is the average fringing field weighted by the surface charge density profile under the transfer gate.

APPENDIX V

Lumped Circuit Model of Charge Coupled Devices

The detailed numerical solution of the transport dynamics with various clocking waveforms show that during the different stages of the charge transfer process the surface charge profiles under the gates take almost a steady shape. The response time of the charge distribution under the gates is of the order of the dielectric relaxation time of the surface minority carrier.[34] During all the stages of the charge transfer the surface charge density is sufficiently large that the response time is orders of magnitude smaller than the transfer times of interest. Hence it is possible to describe approximately the details of the charge transfer dynamics with various clocking waveforms by means of a lumped circuit model which consists of lumped capacitors charged and discharged through lumped transfer channels (MOS transistors).

As discussed in Section 3.2 and 3.3 in the first stages of the charge transfer process, the rate of charge transfer is limited by the transport of charge across the transfer gate and depends strongly on the clocking waveforms. Due to the relatively large carrier concentration under the storage gates, a very small gradient in the quasi-fermi level E_f under the storage gates is sufficient to balance the discharge current. Thus the surface potential and the mobile carrier concentration under the storage gates are almost constant. So the total charge under the source and receiving storage gate Q_{St} and Q'_{St} are given by $W\ell_{St}C_{St}(\Phi_S - \Phi_{So})$ and $W\ell_{St}C_{St}(\Phi'_S - \Phi'_{So})$

respectively, where the surface potential with and without charge under the source storage gate are Φ_S and Φ_{So} and under the receiving storage gate are Φ'_S and Φ'_{So} respectively. The transfer gate acts as a MOS transistor with the source and receiving storage gates as its source and drain. The quasi-fermi level may be assumed constant across the transitional region between the source storage gate and the transfer gate during the first stages of the charge transfer process as this region extends over several times the mean carrier free path and the mobile carrier concentration there is relatively large. Therefore the surface potential at the end of the source storage gate Φ_S is related to the surface potential at the beginning of the transfer gate Φ_T by

$$C_{Tr}(\Phi_T - \Phi_{To}) = C_{St}(\Phi_S - \Phi_{So}) \exp(-(\Phi_T - \Phi_S)/KT) \qquad \text{(A5-1)}$$

and

$$\left[1 + \frac{KT}{\Phi_T - \Phi_{To}}\right] \frac{d}{dt}(\Phi_T - \Phi_{To}) = \left[1 + \frac{KT}{\Phi_S - \Phi_{So}}\right] \frac{d}{dt}(\Phi_S - \Phi_{So}) + \frac{d}{dt}(\Phi_{So} - \Phi_{To}) \qquad \text{(A5-2)}$$

Φ_T and Φ_{To} are the surface potential under the beginning of the transfer gate with and without charge. For $(\Phi_T - \Phi_{To}) >> KT$ and $(\Phi_S - \Phi_{So}) >> KT$ the above equations reduce to:

$$\Phi_T \cong \Phi_S \qquad \text{(A5-3)}$$

and

$$\frac{d}{dt}(\Phi_T - \Phi_{To}) = \frac{d}{dt}(\Phi_S - \Phi_{So}) + \frac{d}{dt}(\Phi_{So} - \Phi_{To}) \qquad \text{(A5-4)}$$

If the mobile carrier concentration in the transitional region between the transfer gate and the receiving storage gate is also relatively large (as in the four phase clocking scheme) then the surface potential at the end of the transfer gate Φ_T' is related to the surface potential at the beginning of the receiving storage gate Φ_S' by similar relations. The total charge under the transfer gate Q_{Tr} and the current I across it are given by Eq. (A4-5) and (A4-4). So, according to this lumped circuit model the total charges under the storage and transfer gates are related to the surface potentials by lumped capacitors, of almost constant values, which are charged and discharged through lumped transfer channels with discharge current that depend mainly on the difference between the surface potential at the ends of the transfer channels. The charge transfer dynamics could be simply described by a first order nonlinear differential equation given by:

$$\frac{d}{dt}(Q_{St} + Q_{Tr}) = - I(\Phi_T, \Phi_T', \Phi_{To}) \qquad \text{(A5-5a)}$$

$$Q_{St} \cong W\ell_{St}C_{St}(\Phi_S - \Phi_{So}) \qquad \text{(A5-5b)}$$

$$Q_{St}' \cong W\ell_{St}C_{St}(\Phi_S' - \Phi_{So}') = Q_o - Q_{St} - Q_{Tr} \qquad \text{(A5-5c)}$$

$$Q_{Tr} \cong \frac{2}{3} W\ell_{Tr}C_{Tr}(\Phi_T - \Phi_{To}) \qquad \text{(A5-5d)}$$

$$\Phi_T \cong \Phi_S, \quad \Phi_T' \cong \Phi_S' \qquad \text{(A5-5e)}$$

$$I(\Phi_T, \Phi_T', \Phi_{To}) = \frac{\mu C_{Tr} W}{2\ell_{Tr}} [2KT(\Phi_T - \Phi_T') + (\Phi_T - \Phi_T')(\Phi_T + \Phi_T' - 2\Phi_{To})] \qquad \text{(A5-5f)}$$

where KT is the thermal voltage and Q_o is the initial total charge. Φ_{To}, Φ_{So} and Φ'_{So} depend on the clock voltage waveforms. In the two-phase clocking scheme, there is usually a large surface potential gradient between the transfer gate and the receiving storage gate. The transfer gate thus acts as an MOS transistor at pinch off and $\Phi'_T = \Phi_{To}$. In this case the current I and the total charge under the transfer gate Q_{Tr} are given by Eqs. (A4-6) and (A4-7). The solutions of the charge transfer characteristics using the lumped circuit model for a two phase drop clock and push clock discussed in Section 3.2 give good agreement with the numberical solution of the transport equations given in Eq. (A-5).

During the last stages of the charge transfer, when the device is operated in the complete charge transfer mode, the charge transfer is limited by the transport of charge out of the storage gate with an almost perfect sink at its end. In this case also the storage gate can be considered as a capacitor discharged through a transfer channel which is the same storage gate. Assuming a constant steady current across the storage gate, the total charge under it Q_{St} and the discharge current I are given by Eqs. (A4-6) and (A4-7) respectively. Solving the discharge equation $I = -(d/dt)Q_{St}$ gives approximately:

$$\frac{Q_{St}}{Q_o} = \frac{\exp(-(t-t_3)/\tau)}{1 + \frac{Q_o}{\frac{2}{3} C_{St} \ell_{St} W} \frac{1}{2KT} [1 - \exp(-(t-t_3)/\tau)]} \qquad \text{(A5-6)}$$

where $\tau = \ell_{St}^2/2D$ and Q_o is the initial total charge under the gate when this stage of the charge transfer process starts at time t_3.

The assumption of a constant steady current across the storage gate is expected to be reasonably good when the nonlinear terms due to the self-induced fields are dominant. But since the effects of the boundary conditions, the fringing fields, the shape of the mobile carrier concentration profile under the gates are not properly considered in the above derivation, the time constant τ of the exponential decay of the charge should be modified. Analytic solutions of the charge transport dynamics including thermal diffusion and fringing-field drift only with the appropriate boundary conditions show that the final decay time constant τ is given approximately[10] by

$$\frac{1}{\tau_f} = \frac{4}{\tau_d} + \frac{(\mu E_{min})^2}{4D} \qquad \text{(A5-7)}$$

where E_{min} is the minimum fringing field under the storage gate, τ_d is the thermal diffusion time constant and is equal to $(4\ell_{St}^2/\pi D)$. The factor 4 in front of the second term is due to the large fields at the edges of the gate, and for zero fringing field this factor takes a value of unity. Accordingly Eq. (A5-6) could be modified to:

$$\frac{Q_{St}}{Q_o} = \frac{\exp(-(t-t_3)/\tau_f)}{1 + \dfrac{Q_o}{\frac{2}{3} C_{St}\ell_{St}W} \cdot \dfrac{1}{2KT} \cdot \dfrac{\tau_f}{\tau_d}\left[1 - \exp(-(t-t_3)/\tau_f)\right]} \qquad \text{(A5-8)}$$

The factor τ_f/τ_d in the denominator is included in order not to modify the original equation for $(t-t_3) < \tau_f$, as the effect of the fringing-field drift is expected to be smaller than the self-induced drift in this period.

Using Eq. (A4-6) and (A4-7) the charge under the transfer gate is described approximately by

$$\frac{dQ_{Tr}}{dt} + \frac{\mu C_{Tr} W}{2\ell_{Tr}} \frac{Q_{Tr}}{\frac{1}{2} C_{Tr} \ell_{Tr} W} [2(\ell \bar{E} + KT) + \frac{Q_{Tr}}{\frac{1}{2} C_{Tr} \ell_{Tr} W}] = - \frac{dQ_{St}}{dt} \qquad (A5\text{-}9)$$

where $\bar{E}$ is the average fringing field weighted by the surface charge density profile under the transfer gate. Using Ricatti's substitution, this equation could be solved by the WKB method.[16] However, an approximate solution can be obtained in the overlapping gates structures as the transfer gates are usually shorter and have larger fringing fields than the storage gates. So the carriers are swept rapidly from under the transfer gate and for transfer time of practical interest, the solution simplifies to

$$Q_{Tr} \cong \tau_{Tr} \left(- \frac{dQ_{st}}{dt} \right) \qquad (A5\text{-}10)$$

where τ_{Tr} is the single carrier transit time under the transfer gate and is given by $\tau_{Tr} = (\ell_{Tr}^2/2\mu(KT + \bar{E}\ell_{Tr}))$.

APPENDIX VI

Transient Occupation of the Interface States

If the mobile carrier concentration $p(t)$ is varying with time, then the transient average occupation of the interface states at an energy E above the valence band is obtained by integrating the rate Eq. (1). Assuming $p(t) >> KT \cdot N_{ss}$ then we get:

$$n_{ss} = K_1 N_{ss} \exp\left[-\int_o^t (K_1 p(t') + K_2 \exp(-E/KT))\, dt'\right] \cdot \int_o^t p(t') \exp\left[\int_o^{t'} (K_1 p(v) + K_2 \exp(-E/KT))\, dv\right] dt' + \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(o)}} \exp\left[-\int_o^t (K_1 p(t') + K_2 \exp(-E/KT))\, dt'\right]$$

for $t > o$ (A6-1)

If $p(t) = p(t_3) \exp(-(t-t_3)/\tau)$ for $t > t_3$, then

$$n_{ss}(t) = K_1 N_{ss} \exp\left[-K_1 p(t_3) \tau(1 - \exp(-(t-t_3)/\tau)) - K_2(t-t_3) \exp(-E/KT)\right] \int_{t_3}^t p(t') \exp\left[K_1 p(t_3) \tau(1 - \exp(-(t'-t_3)/\tau) + K_2(t'-t_3) \exp(-E/KT)\right] dt' + \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t_3)}} \exp\left[-K_1 p(t_3) \tau(1 - \exp(-(t-t_3)/\tau)) - K_2(t-t_3) \exp(-E/KT)\right]$$

for $t > t_3$ (A6-2)

his can be easily reduced to

$$N_{ss}(t) = N_{ss}K_1\tau \exp\left[K_1\tau p(t) - K_2(t-t_3) \exp(-E/KT)\right]$$

$$\cdot\left[p(t) \exp(K_2 \exp(-E/KT)) E_c(K_1\tau p(t)) - p(t_3) E_c(K_1\tau p(t_3))\right]$$

$$+ \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1 p(t_3)}} \exp\left[-K_1 p(t_3) \tau(1-\exp-(t-t_3)/\tau) + K_2(t-t_3)\exp(-E/KT)\right.$$

for $t \geq t_3$ (A6-3)

where $E_c(x)$ is the exponential integral of order c defined by

$$E_c = \int_1^\infty \frac{\exp(-xv)}{V} dv \quad , \qquad \text{(A6-4)}$$

and

$$c = \tau K_2 e^{-E/KT} \quad . \qquad \text{(A6-5)}$$

If $K_1\tau p(t) > 1$, then the asymptotic expansion of $E_c(x)$ can be used:

$$E_c(x) = \frac{e^{-x}}{x + c} \quad . \qquad \text{(A6-6)}$$

For $t > t_3 + \frac{1}{K_1 p(t_3)}$, Eq. (A6-3) reduces to

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1 p(t)}} + \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1 p(t_3)}} \exp\left[-K_1 p(t_3)\tau(1-\exp(-(t-t_3)/\tau))\right.$$

$$\left. - K_2 \cdot (t-t_3) \exp(-E/KT)\right] \quad . \qquad \text{(A6-7)}$$

Two special cases are of interest. First, if $K_1 p(t_3)\tau > 1$, then the second term is negligible for $t > t_3 + \tau$, and Eq. (A6-7) reduces to

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t)}} \quad . \qquad \text{(A6-8)}$$

Thus the interface states have a small effective time constant τ_{eff} and can equilibrate very rapidly with the mobile carrier. Assuming a constant interface state density N_{ss} states/cm^2 eV and a constant capture cross-section $\sigma_h$cm^2, the total density of trapped carriers P_{tr} is given by

$$P_{tr} = \int_0^{E_g} n_{ss}(t)\, dE$$

$$= N_{ss}\, KT\, \ell n \frac{(\exp(E_g/KT) + \frac{K_2}{K_1 p(t)})}{(1 + \frac{K_2}{K_1 p(t)})}$$

If $\frac{1}{K_2} < \frac{1}{K_1 p(t)} < \frac{1}{K_2} \exp(E_g/KT)$, then

$$P_{tr} = N_{ss}(E_g - KT\, \ell n \frac{K_2}{K_1 p(t)}) \quad . \qquad \text{(A6-9)}$$

Second, if $K_1 p(t)\tau \leq 1$ Eq. (A6-7) reduces to

$$n_{ss} = \frac{N_{ss}}{1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t_4)}} \cdot \exp(-K_2(t-t_4) \exp(-E/KT)$$

$$t > t_4 \qquad \text{(A6-10)}$$

where t_4 is the time the emission of carriers becomes dominant and the refilling of the traps becomes negligible. It is given by

$$K_1 p(t_4) \tau = 1 \qquad \text{(A6-11)}$$

Similarly integrating Eq. (A6-10), we get

$$P_{tr} = N_{ss}\, KT \Big[E_1(K_2(t-t_4)\, \exp(-E_g/KT)) - E_1(K_2(t-t_4)) - E_1(K_2(t-t_4)\, \exp(-E_g/KT) + K_1(t-t_4)\, p(t_4)) + E_1(K_2(t-t_4) + K_1(t-t_4)\, p(t_4)) \Big] .$$

If $\frac{1}{K_2} < t-t_4 < \frac{1}{K_2} \exp(E_g/KT)$ and $t-t_4 > \frac{1}{K_1 p(t_4)}$, then we may use the asymptotic expansion of the exponential integral for small and large arguments to get

$$P_{tr} = N_{ss} \left[E_g - KT\, \ell n\, K_2(t-t_4) - \frac{KT}{(t-t_4) K_1 p(t_4)} \right] \qquad \text{(A6-12)}$$

FOOTNOTES

1. The maximum current that can be transferred across an inversion layer produced by a metal gate of length ℓ and width W is given approximately by (as shown in Appendix IV)

$$I \cong \frac{\mu C W}{2\ell} \Phi_o^2$$

where C is the oxide capacity μ is the surface mobility and Φ_o is the surface potential without charge. If an inversion layer is produced by a constant normal field in a gap of length ℓ and width W on a substrate of doping N_D then the relation between the surface potential Φ_S and surface charge q is given by

$$q = \sqrt{2\varepsilon_S e N_D}\,(\sqrt{|\Phi_o|} - \sqrt{|\Phi_S|})$$

where Φ_o is the surface potential without charge, ε_S is the semiconductor dielectric constant and e is the electronic charge. Then using the gradual channel approximation, it can be shown that the maximum current that can be transferred by the inversion layer under the gap is approximately given by:

$$I' = \frac{2}{3}\frac{\mu C_D W}{\ell} \Phi_o^2$$

where C_D is the depletion layer capacity under the gap with no surface charge. Thus the presence of a metal gate over the inversion layer shields out the charge repulsion and increases the maximum rate of transfer of charge by the ratio of the oxide to the depletion layer capacity which is typically about an order of magnitude.

2. The calculations and results presented here can be applied to n-channel devices after the proper scaling of the transfer times by the surface mobility ratio of the electrons and holes and the use of the appropriate values of the threshold and flatband voltages.
3. Thermal generation and leakage currents impose a limit on the maximum delay time and the minimum clock frequency of the device.
4. Carrier mobilities at the Si-SiO_2 interface are approximately constant up to a normal surface field of 1.5×10^5 Volt/cm corresponding to a surface carrier concentration of $10^{12}/cm^2$.[11] Therefore, for mobile carrier concentration equal or less than $10^{12}/cm^2$, the reduction in the surface mobility due to the normal surface field is small. The carrier velocity in silicon saturates at a critical field around 5 volts/micron.[12] During the charge transfer, the surface potential gradient usually does not exceed one volt/micron except in the interelectrode region between the transfer gate and the receiving storage gate, where it may reach about 10 volts/micron. Since the maximum sheet current density is about few μamp/micron, and the mobile carrier concentration in this region is smaller by more than an order of magnitude than that under the gate electrodes, the changes in the mobile carrier concentration in this region due to velocity saturation has negligible effects on the charge transfer characteristics.
5. The box scheme has very desirable features that made it suitable for solving the set of nonlinear diffusion equations describing the charge transport dynamics in CCD. For example, second order accuracy can be achieved with nonuniform nets. Thus small net

spacing can be used in the interelectrode regions where the surface charge density is changing rapidly, while a large net spacing can be used in the other regions where the surface charge density gradient is small. Also both the surface charge density and its gradient are approximated with the same accuracy. Thus the charge flow across the boundaries between the different regions is conserved to the same order of accuracy of the surface charge under the electrodes.

6. A full bucket is the equilibrium surface charge density under the storage gate electrode with its voltage equal to V_m.
7. For example, in applications requiring maximum charge to be transferred along the device (such as digital serial memories and analog delay lines) and if the oxide thickness under the storage gate is 1200Å, then to operate the device in the complete charge transfer mode with two-phase drop clock the optimum oxide thickness under the transfer gate is about 3200Å for V_m = -15 volts and a substrate doping of $8 \times 10^{14}/cm^3$. In other applications such as low level injection CCD imagers it may be more important to maximize the fringing fields under the storage gate. In this case thicker silicon oxides under the storage and transfer gates with a low substrate doping may optimize the performance of the device.
8. For rise and fall time comparable or larger than the transfer times of interest the same equations given with the push clocks below in Eqs. (17) and (18) could be used.
9. The value of Q_o' at which the perfect sink at the end of the storage gate becomes a good approximation unfortunately cannot be defined

precisely. It can be estimated approximately by assuming that the almost perfect sink is formed, when the surface charge density in the transitional region is about a fifth of its value under the storage gate. Assuming the average surface potential gradient in the transitional region is $\Delta\Phi/\Delta x$ where $\Delta\Phi$ is the difference in surface potential with no charge under the source storage gate and transfer gate and Δx is the spatial extent of the transitional region (which is equal to about a depletion layer thickness), then Q_o' is given by solving

$$W\mu \frac{\Delta\Phi}{\Delta x} \frac{Q_o'}{W\ell_{St}C_{St}} \frac{1}{5} = \frac{(Q_o' + Q')^2}{(Q_o + Q')} \frac{1}{\tau_2} \rightarrow \frac{(Q_o'+Q')^2}{Q_o'Q'} \simeq \frac{1}{5} \cdot \frac{2\ell_{Tr}}{\Delta x} \cdot \frac{C_{St}}{C_{Tr}} \cdot R$$

Although the approximate values of Q_o' and t_2 may lead to about 15% error in defining the onset of the last two stages, this is a much better approximation than using the perfect sink assumption at the end of the storage gate from the beginning of the charge transfer process.

10. The good fitting in Fig. 12 to the numerical solution is partly because the precise values of Q_o' and t_2 could be obtained from the time evolution of the numerically calculated surface potential profiles under the gates.

11. Note that in the overlapping gate two phase structure, the asymmetry is obtained by the step in the oxide under the two electrodes connected to the same phase, therefore a larger signal charge could be stored under the storage gate with push clock than with

drop clocks. Also the maximum signal charge increases as the oxide thickness increases. The limits on the oxide thickness under the transfer gates are imposed by the following two factors: First, as the oxide thickness under the transfer gates increases the maximum current that can be transferred across it, which is the saturation current of a similar MOS transistor, decreases. Thus the rate of charge transfer during the first stages of the transfer process decreases. Second, if the oxide is too thick the regions under the transfer gates will go into majority carrier accumulation, when its phase voltage is at the resting potential V_2. Thus the majority carriers fill the traps and recombination centers at the interface and may recombine with the signal minority carriers during the charge transfer. The charge loss in this case is not as severe as the case when the regions under the storage gates are driven into accumulation,[15] because the signal charge does not spend as much time under the transfer gates as it spends under the storage gate. This phenomena does not impose severe limitations, but it is preferable to keep the regions under the transfer gates always depleted to avoid the second order effects of charge loss especially for long registers.

12. For arbitrarily smooth waveforms solution of Eq. 18 can be easily obtained analytically using Ricatti's substitution and the WKBJ method.[16] The final solutions are similar to the results reporeted by K.K. Thornber[17] for the MOS Bucket Brigade. For sinusoidal drive functions the solutions can be written in terms of Mathieu functions. We mean by sufficiently smooth drive

function that the time dependence of

$$\frac{2\ell_{Tr}\ell_{St}}{\mu}\frac{C_{St}}{C_{Tr}}\frac{d}{dt}(\Phi_{so} - \Phi_{mTo})$$

is much smaller than that of $(\Phi_{mT} - \Phi_{mTo})^2$.

13. Actually the perfect sink may be formed before or after the clock voltage stops changing. The value of t_2 unfortunately cannot be evaluated precisely and this may lead to about 10% error in locating the exponential tail of the last stage of the charge transfer. If $t_2 > T_r$, then after the clock voltage stops the residual charge under the storage gate decreases hyperbolically with a time constant τ_2 as given by Eqs. (7),(8) and (9). If $t_2 < T_r$ then the perfect sink is formed before the clock voltage stops. In Fig. (21) the good fitting to the numerical solution is because the precise values of t_2 could be obtained from the numerically calculated surface charge profiles under the gates.

14. The residual charge under the source storage gate during the last two stages (after the clock voltage stop) given by Eqs. (23) and (27) can be approximately described by one equation if we assume that

$$\frac{[(W\ell_{St}C_{St} + \frac{2}{3}W\ell_{Tr}C_{Tr})(\Phi_{mT} - \Phi_{mTo}) + W\ell_{St}C_{St}KT]}{[(\Phi_{mT} - \Phi_{mTo}) + 2kT]} \simeq W\ell_{St}C_{St}$$

Then Eq. (27) can be solved to give:

$$Q(t) \simeq Q' + \frac{Q_o' - Q'}{1 + \frac{(t - t_2)}{\tau}} - KTW\ell_{St}C_{St}\ell n(1 + \frac{(t - t_2)}{\tau})$$

where

$$\tau = \frac{2\ell_{St}\ell_{Tr}}{\mu}\frac{C_{St}}{C_{Tr}}\frac{1}{\frac{Q_o' - Q'}{W\ell_{St}C_{St}}}$$

15. For example at the end of the device the amplitude of the output of digital signals will decrease with increasing clock frequency and the output of analog signals will have frequency and phase distortion.(18)

16. Note that the two-phase drop clock used in Fig. (31) has zero rise and fall times. Any finite rise and fall times of the pulses of the drop clock will delay the charge transfer, hence the shown results actually over-estimate the performance of the device with drop clocks at high frequency. But with push clocks, the finite rise times are advantageously used to push the charge from one site to another.

17. The same discussion and analysis given below holds for n-channel devices. In this case the mobile electrons interact mostly with interface states near the conduction band edge.

18. Note that in this case, since the signal charge reamins under the storage electrode for one whole transfer time, the probability of filling the interface states by the signal charge F_s is equal to unity. As discussed in Section 4.5, we may also obtain the average mobile charge density under the edges $p_{av,edge}$ and p_{avo} and the time interval Δt_{eo} for which the background charge is in contact with the edges from the charge transfer dynamics and the surface charge density profile of the signal charge under the electrodes.

19. This is actually due to the following reasons. First, for a

sufficiently large background charge, the mobile carriers during the first stages of the charge transfer process effectively equilibrate with the interface states under the transfer gates and the perpendicular edges. Second the area under the transfer gates and the perpendicular edges in the overlapping gate structure is usually smaller than the area under the storage gates. Third, because of the larger fringing fields under the transfer gates and the perpendicular edges, the mobile carriers are swept out very rapidly and the emptying of the interface state begin earlier in the transfer process. But under the storage gate the residual charge decreases with a relatively large time constant. The interface states under it continue to capture carriers from the residual charge and the quasi-fermi level follows the quasi-fermi level of the residual charge. When the residual charge becomes small enough, emission from the traps becomes dominant. This results in a change of the slope of the signal degradation due to trapping in interface states under the storage gates versus clock frequency as shown in Figs. (36) and (37).

20. Increasing the active channel width increases also the signal to noise ratio and dynamic range of the CCD. The noise introduced to the signal charge in the storage process through the leakage and thermal generation current is proportional to the square root of the gates area. The noise introduced during the transfer process through the fluctuations of the carriers trapped in the interface states and through thermal noise (suppressed transfer loss fluctuations) is also proportional to the square root of the gates

area.[25,26] But the signal charge is directly proportional to the gate area. Hence the dynamic range and signal to noise ratio can be increased by increasing the active channel width of the device without degrading its high frequency performance.

21. Thus the incomplete charge transfer due to trapping in interface states under the storage and transfer gates and the perpendicular edges is due to the variable mean occupation of the state with energy close to E_1. Therefore the values of N_{ss} and σ_h at the energy E_1 should be used to estimate the trapping effects in these states.

22. Note that the last term in Eq. (A4-5) is a very slowly varying function taking a value between 3/4 and 3/2 depending on the value of $(\Phi_{mT} - \Phi_{mTo})$ and $(\Phi'_{mT} - \Phi_{mTo})$. So, taking the value of this term unity is a good approximation to simplify the solution of the differential equation (A5-5) for any clocking waveforms.

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FIGURE CAPTIONS

Figure 1. (a) An equivalent circuit of a two-phase MOS bucket brigade device. Storage utilizes the gate to drain capacitance which is enlarged in the bucket brigade structure. The two phases ϕ_1 and ϕ_2 control the transfer of charge from one storage capacitor to another.

(b) and (c) Structure of a two-phase bucket brigade device built with p-MOS technology and silicon gate technology respectively.

Figure 2. Energy level diagram of a metal-insulator-n semiconductor

(a) when a voltage pulse has just been applied to the metal electrode

(b) after the accumulation of some minority carrier at the insulator-semiconductor interface

(c) schematic cross section of a three-phase charge coupled device structure. The electrodes are pulsed in the sequence $\phi_1\phi_2\phi_3$.

Figure 3. One unit cell of the overlapping gate structure using the silicon gate technology.

Figure 4. Plots of the surface potential and surface potential gradient along the silicon-silicon oxide interface obtained from the solution of the two-dimensional Poisson equation of the structure in Fig. 3 with minimum geometry dimensions.

The thickness of the polysilicon and the aluminum electrodes is 0.5 micron. The electrode voltages correspond to the latter stages of the charge transfer. A signal charge of about 5.5 volts is in the receiving storage electrode. The substrate doping is 8×10^{14} donors/cm^3 in Fig. 2a and 10^{14} donors/cm^3 in Fig. 2b.

Figure 5. Storage and transfer of charge in three-phase overlapping gates charge coupled devices. Surface potential ϕ_s with and without charges are plotted along the interface. (a) and (b) are for three phase drop clocks, (a') and (b') are for three phase push clocks.

Figure 6. Storage and transfer of charge in four phase overlapping gates charge coupled devices. Surface potentials ϕ_s with and without charge are plotted along the interface. (a) and (b) are for four phase drop clocks, (a') and (b') are for four phase push clocks.

Figure 7. Storage and transfer of charge in two phase overlapping gates charge coupled devices. Surface potentials ϕ_s with and without charges are plotted along the interface. (a) and (b) are for two phase drop clocks, (a') and (b') are for two phase push clocks.

Figure 8. Storage and transfer of charge in an overlapping gates charge coupled device using single phase clocking scheme.

Figure 9. Plots of the one-dimensional relation between the surface potential ϕ_s and the gate voltage for a polysilicon gate with 1200Å and aluminum gates with different oxide thickness. The substrate doping is 0.8×10^{15}donors/cm^2, $Q_{ss} = 3.1\times10^{11}/cm^3$.

Figure 10. Transient currents at the beginning and end of the transfer gate and the net current charging the region under the gate. The device shown at the top of the figure is operated with drop two-phase clocks V_m=- 15 volts, V_1 = -7 volts. Signal charge equivalent to about 3 volts. Channel width W = 8 microns.

Figure 11. Frames to illustrate the charge transfer at its initial stages for the device shown in Fig. 10 operated with drop two-phase clock. The horizontal axis represents the distance along the interface. The vertical axis at the bottom of each frame represents the surface charge density of the mobile carrier Q in normalized units. The vertical axis at the top of each frame represents the gate voltage V from 0 to -15 volts. The vertical axis at the middle of each frame represents the surface potential ϕ from 0 to -15 volts. The upper line represents the surface potential with charge; the lower line represents the surface potential without charge, so the difference between the two lines is proportional to the surface charge density. Zero time corresponds to the instant when ϕ_2 decreases to V_m starting the charge transfer. The time of each frame is shown at its upper corner.

Figure 12. The residual charge under the storage gate as a percentage of a full bucket for two different initial charges equivalent to about 3 volts and one volt versus transfer time. The full line curves are for a substrate doping of 8×10^{15} donors/cm^3 and 10^{14} donors/cm^3. The dashed line curves are obtained from Eqs. (7) and (16) according to the lumped circuit model. V_m = -15 volts.

Figure 13. Transient currents at the beginning and end of the transfer gate as well as the net current charging the region under the gate for the device shown at the top of the figure operated with two-phase push clock. Zero time coincides with the instant the clock voltage starts to increase to push the charge. V_m = -15 volts. Signal charge is equivalent to about 7 volts, channel width W = 8 microns.

Figure 14. Transient currents for the device shown at the top of the figure operated with push two-phase clock. V_m = -15 volts. Signal charge is equivalent to about 7 volts, channel width W = 8 microns.

Figure 15. Transient currents for the device shown at the top of the figure. Two-phase push clock is used. T_r = 13 nsec. V_m = -15 volts, V_1 = -6 volts, W = 8 microns.

Figure 16. Transient current for the device shown at the top of the figure operated with two-phase push clock. T_r = 10 nsec., V_m = -15 volts, V_1 = -6 volts, channel width W = 8 microns.

Figure 17. Transient currents for the device shown at the top of the figure operated with two-phase push clock. T_r = 10 nsec., V_m = -15 volts, V_1 = -7 volts, channel width W = 8 microns.

Figure 18. Frames to illustrate the charge transfer for the device with 4400Å oxide under the transfer gate operated with two-phase push clock and rise time T_r = 50 nsec. The frame format is the same as that of Fig. 11.

Figure 19. Frames to illustrate the charge transfer for the device with 3200Å oxide under the transfer gate operated with two-phase push clock. T_r = 10 nsec. The frame format is the same as that of Fig. 11.

Figure 20. Residual charge under the storage gate as a fraction of a full bucket for different initial charges versus transfer time, using two-phase push clocks with a rise time T_r = 40 nsec. The dimensions of the device used are shown at the top of the figure.

Figure 21. The residual charge under the storage gate as a percentage of a full bucket for a device with 3200Å under the transfer gate. The full line curves are for a substrate doping of 8×10^{14} donors/cm^3, and 10^{14} donors/cm^3. The dashed line curves are obtained from Eqs. (16) and (18) according to the lumped circuit model. V_m = -15 volts, T_r = 13 nsec.

Figure 22. Transient currents for a two-phase push clock in the incomplete charge transfer mode. T_r = 27 nsec. V_m = -15 volts, V_1 = -7 volts, channel width W=8 microns.

Figure 23. The residual charge as a fraction of a full bucket for two different initial charge 0.6 and 0.4 of a full bucket versus transfer time. The device is operated with two-phase push clock in the incomplete charge transfer mode. The dimensions of the device used are shown at the top of the figure. The dashed line curves are obtained from Eqs. (18), (23) and (27) according to the lumped circuit model.

Figure 24. Transient currents at the beginning (full line curve) and end (dotted line curve) of the transfer gate for the four-phase push clock shown. The dimensions of the device used are shown at the top of the figure.

Figure 25. Frames illustrating the charge transfer with four-phase push clock. The frame format is the same as that of Fig. 11.

Figure 26. The residual charge under the storage gate for two different initial charges 0.75 and 0.35 of a full bucket versus transfer time with the four-phase push clock. The dimensions of the device and the clocking waveforms used are shown at the top of the figure.

Figure 27. Residual charge versus initial charge at different transfer times for two-phase push clock.

Figure 28. Signal degradation factor due to incomplete free charge transfer versus transfer time for a two-phase drop clock. The device dimensions and clocking waveforms are shown at the top of the figure. The substrate doping is 8×10^{14} donors/cm^3. The dashed line curve is the signal degradation due to intrinsic transfer rate. The full line curve is the signal degradation due to the intrinsic transfer rate and the device parameters modulation.

Figure 29. Signal degradation due to incomplete free charge transfer versus transfer time for a two-phase push clock. The device dimensions and clocking waveforms are shown at the top of the figure. The substrate doping is 8×10^{14} donors/cm^3. The dashed line curve is the signal degradation due to the intrinsic transfer rate. The full line curve is the signal degradation due to the intrinsic transfer rate and the device parameters modulation.

Figure 30. Signal degradation due to incomplete free charge transfer versus transfer time for a two-phase push clock in the incomplete or residual charge transfer mode. The device dimensions and clocking waveforms are shown at the top of the figure. The substrate doping is 8×10^{14} donors/cm^3. The dashed line curve is the signal degradation due to the

intrinsic transfer rate. The full line curve is the signal degradation due to the intrinsic transfer rate and the device parameters modulations.

Figure 31. Signal degradation due to incomplete free charge transfer versus bit time for a two-phase drop and push clock. The device dimensions and clocking waveforms are shown at the top of the figure, the substrate doping is 8×10^{14} donors/cm^3. The full line curve is the signal degradation with push clock and the dotted line curve is the signal degradation with drop clocks. The signal degradation with the four-phase push clock at 15 Megahertz shown in Fig. 26 is indicated by the cross point in the figure.

Figure 32. Average carrier concentration under the transfer gates versus transfer time for the fat zero and signal charges. A two-phase drop clock with zero fall and rise time is used. V_m = -15 volts, V_1 = -7 volts.

Figure 33. Average carrier concentration under the storage gates versus transfer time for the fat zero and signal charges. A two-phase drop clock with zero fall and rise times is used. V_m = -15 volts, V_1 = -7 volts.

Figure 34. Average carrier concentration under the transfer gates versus transfer time for the fat zero and signal charges. A two-phase push clock with zero fall time and 13 nsec rise time is used. V_m = -15 volts, V_2 = -6 volts.

Figure 35. Average carrier concentration under the storage gates versus transfer time for the fat zero and signal charge. A two-phase push clock is used. T_r = 13 nsec, V_m = -15 volts, V_2 = -6 volts.

Figure 36. Signal degradation factors versus clock frequency for the minimum geometry device operated with a two-phase drop clock.

Figure 37. Signal degradation factors versus clock frequency for the minimum geometry device operated with a two-phase push clock.

Figure 38. Metal-insulator semiconductor system. The potential at any point in the semiconductor (x,y) due to a line charge parallel to the z axis at (x',y') is calculated using the method of images.

Figure 39. Net rectangle for difference approximations.