Nanoscale Field Emission Devices

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ABSTRACT

This thesis outlines work done to produce in-plane nanoscale field emission devices. Field emission, the process of quantum tunneling electrons from a conductor into a vacuum, has been theorized as a device concept for almost as long as integrated circuits have existed. This is because the micro- and nanoscale dimensions of integrated circuits make field emission possible at modest voltages, and because the physics of field emission and conduction in a vacuum channel suggest that field emission devices can operate at extremely high frequencies and in harsh environments where CMOS devices face challenges. Yet despite many attempts to make practical field emission devices none have risen to the level of commercial products. These attempts were stymied by short lifetimes, high operating voltages, and the necessity for vacuum enclosure. In this thesis work, I outline how new fabrication technologies like high resolution electron beam lithography, atomic layer deposition, and refinement in reactive ion etching make lateral field emission devices with extremely short vacuum channels practical. The demonstrated devices can operate at near CMOS voltages and at atmospheric pressures, and are robust to emitting tip destruction. These devices are prime candidates for integration into demonstration circuits.

The second part of this thesis outlines work done in an emerging field to combine field emission with plasmonics for practical devices. The tunneling process in field emission depends exponentially on the magnitude of the instantaneous electric field, either static or time-varying, at the emitting surface. While it has long been known that using extremely powerful pulsed lasers one can field emit electrons from a metallic surface, the combination of plasmonics into a field emitting device has the potential to dramatically lower the incident optical power needed to produce field emission. This could enable extremely fast opto-electronic devices. This thesis presents work in progress to realize a plasmonically enhanced field emission opto-electronic modulator that is designed to operate at 1550 nm and is integratable with existing silicon photonics platforms.

PUBLISHED CONTENT AND CONTRIBUTIONS

Chen, Yu et al. (2013). "Ultrasensitive gas-phase chemical sensing based on functionalized photonic crystal nanobeam cavities". In: *ACS Nano* 8.1, pp. 522–527. DOI: 10.1021/nn4050547. URL: http://pubs.acs.org/doi/abs/10.1021/nn4050547.

The author of this thesis assisted in optically testing the devices described in this publication.

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The author of this thesis led the project, fabricated and tested the published devices, and wrote the manuscript.

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The author of this thesis fabricated and tested the devices that this patent application was based on, in addition to writing and editing parts of the application.

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Chapter 1

INTRODUCTION

To understand the context in which the enclosed thesis work takes place it is important to understand the field of micro and nanoscale cold field emission and its relationship to the more mature field of semiconductor devices. Micro and nanoscale cold field emission was conceived during the rapid rise of semiconductor devices. Integrated circuits built on solid-state devices had been demonstrated only two years before Ken Shoulders suggested cold field emission as a physical mechanism for a microscale device (Shoulders, 1961). Throughout the development of cold field emitting devices, they were always compared unfavorably to their more mature solid-state cousins. The only applications that they were considered for were those where a solid-state equivalent could not operate as well. These included microwave amplifiers, miniaturized and parallelized cathode ray displays, and for applications in high temperature or high radiation environments. Where solid-state devices were later developed for some of these applications, notably for displays, the field emission devices were quickly supplanted. From this perspective, it may seem strange to further refine this device concept, but it is the author's opinion that technology has ripened to a point that this device deserves further consideration. It may be possible now, using the same tools developed to miniaturize solid-state devices, to overcome the difficulties that plagued field emission devices in the past. Additionally, the development of solid-state transistors has unquestionably hit a bottleneck that field emission devices may be able to overcome. Finally, field emission devices may be uniquely suited to take advantage of the advances in plasmonics to create new, hybrid electronic/optical devices. In this introductory chapter we will lay out the history of field emitting devices, motivate our work by discussing briefly the state of the integrated circuit industry, and introduce plasmonics and its application to field emission.

1.1 The state of the integrated circuit industry

For the past 35 years the semiconductor industry has been dominated by geometric scaling of MOSFET parameters, termed Dennard scaling (Dennard et al., 1974). The Dennard scaling paradigm was predicated on reducing the channel length, width, and gate oxide thickness of successive generations of MOSFETs by a factor

$1/\kappa$ and simultaneously increasing the doping concentration of the channel by a factor κ. This scaling ensures that the operating voltage, operating current, and device capacitance will all scale by a factor of $1/\kappa$ as well, providing an increase in maximum operating frequency of κ. The density of devices would increase by a factor κ^2 but the power dissipation of a single device, $V \times I$, would scale by a factor of $1/\kappa^2$ so that the power density of the integrated circuit would remain constant. The assumptions that Dennard's scaling paradigm were built on have begun to break down as dimensions have shrunk. For example, shrinking the gate thickness past 1.2 nm, which occurs for the Intel 65 nm node, produces prohibitive gate leakage current (Bohr, 2007). Additionally, Dennard ignored sub-threshhold leakage current, which has become a significant part of each individual MOSFETs power budget as the threshold voltage has dropped. Both of these additional sources of leakage have combined, along with other effects, to limit the decrease in power density with each successive generation. To abate this issue, operating frequencies have been throttled to prevent overheating. This is shown in Figure 1.1 (Rupp, 2017). From the figure we can see that performance increases in the late 2000s were driven strongly by multi-core architectures and parallelization.

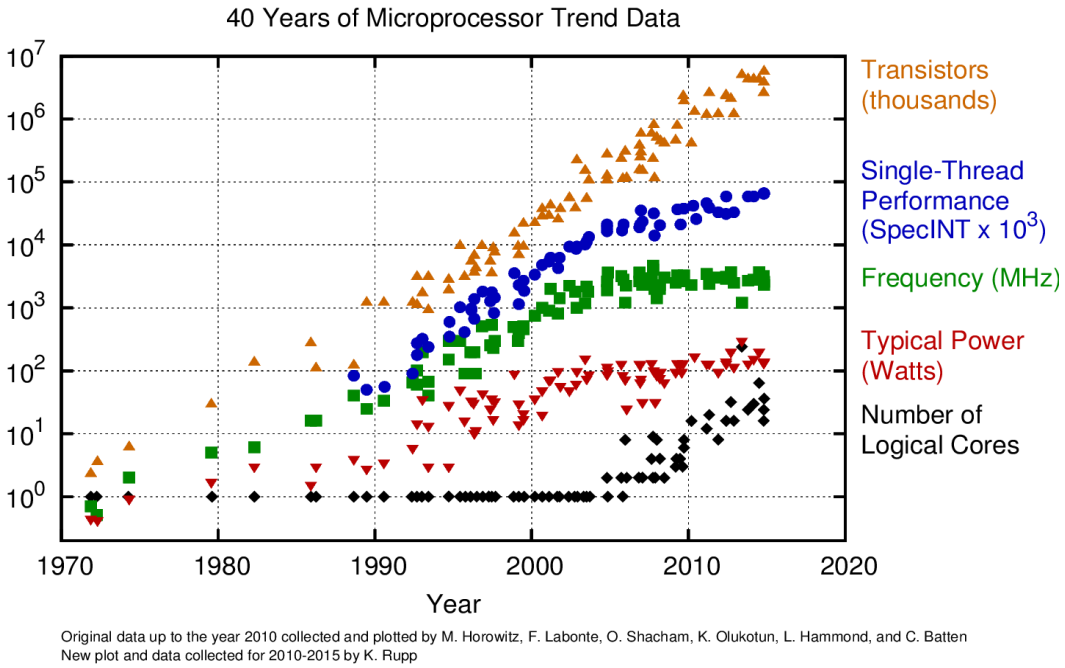

Figure 1.1: 40 year processor trend demonstrating the failure of Dennard Scaling in the early 2000s. Image curtesy of Karl Rupp.

The failure of Dennard scaling has been partial since transistor sizes have continued

to scale but supply voltages have scaled down less quickly. This has led to the rise of so-called dark silicon. Succinctly, the power density of modern processors is so high that powering all transistors simultaneously would quickly exceed the thermal power budget for the chip and would result in diminished performance, decreased lifetime, and/or permanent device failure. Dark-silicon (and dim silicon) are strategies to combat overheating by powering off (or operating in sub-threshold) transistors on a single chip dynamically to prevent overheating (Shafique et al., 2014). According to the International Technology Roadmap for Semiconductors (the ITRS report) approximately 50% of the 22 nm node will be dark at any instant. The necessity of dark or dim silicon provides huge technical challenges to overcome with each successive technology node.

This mounting difficulty has led to dramatic innovation. For example, in 2011 Intel introduced its 22 nm node technology with so-called tri-gate transistors (Bohr and Mistry, 2011). Unlike traditional metal oxide semiconductor transistors (MOSFETs), tri-gate transistors and similar technologies like FinFETs use a thin vertical silicon "fin" as the conduction channel. Surrounding the conducting channel on two sides and also on top are gates separated from the channel by high-κ dielectric. This design allows for a larger operating current by providing a larger conducting interface since three of the four sides of the channel are close enough to the gate to be depleted. Still, these innovations have not been sufficient to maintain technological growth rate dictated by Moore's law. Since 1985, major entities in the semiconductor manufacturing world have compiled industry wide reports, first as the National Technology Roadmap for Semiconductors (NTRS) and in 1998, with the addition of international partners, as the International Technology Roadmap for Semiconductors (ITRS). The purpose of the roadmap is to coordinate suppliers of equipment and raw materials with the needs of the industry for a 15 year period into the future. For example, the ITRS will project the critical feature size of technology nodes many years in advance, giving makers of photolithography equipment the ability to reliably plan their introduction of new technologies (smaller wavelength light sources, gray scale photomasks, etc) to align with the industry need. In light of the failure of Moore's law and facing the uncertainty of industries future the ITRS issued its last roadmap in 2015. This final report predicts that past 2021 it will no longer be economically feasible to shrink device dimensions. As the semiconductor industry searches for the next generation of devices, there is an opportunity for dark horse candidates, including field emission devices, to become accepted by the industry. Initially, field emission devices could enter markets where silicon devices

do not operate well. One such market is in high temperature electronics. Solid-state transistors fail at high temperatures when electrons in p-doped regions are thermally excited to such a degree that the region has the same conduction electron concentration as an n-doped region. This eliminates p-n junctions and the device becomes resistive. This phenomenon sets the maximum operating temperature for silicon MOSFETs to approximately 300 °C (P. G. Neudeck, Okojie, and Chen, 2002), and for high temperature silicon carbide (SiC) transistors to 600 °C (P. Neudeck, Krasowski, and Prokop, 2011). High temperature operation of field emission devices is fundamentally less problematic, as the current remains exponentially dependent on the field until thermionic emission dominates, which occurs at higher temperatures. Indeed, SiC nanoneedle arrays have been operated at 500 °C (Wang et al., 2015). The advantages of field emitting transistors and the rising challenges to continued MOSFET usage, particularly in many niche fields, is the motivator for much of our work in field emission devices.

1.2 A brief history of vacuum tubes

At the dawn of the twentieth century the technology to create vacuum in enclosed vessels began to mature rapidly. The technology had already made possible mass production of Edison's incandescent lightbulbs in the 1870's (Redhead, 1999). The innovation of the mercury rotary vane pump and eventually the mercury diffusion pump as well as improvements in sealing technology eventually made it possible to vacuum seal vessels at pressures of 10^{-3} Torr or better with isolated electrical contacts to the atmosphere side. In 1904 John Ambrose Fleming used these innovations to make the first vacuum tube device, a vacuum diode. The device worked by heating an an electrical conductor (called the cathode) in vacuum until it began to emit electrons through thermionic emission. The emitted electrons would follow the gradient of the electric field to an appropriately biased electrical terminal called the anode. Because heating occurred on only one terminal electrical conduction was only possible in a single direction between the two terminals. This provided rectification, which found ready use in the demodulation of radio signals. Vacuum tubes were a significant improvement on so-called cat's whiskers diodes which were based on Schottky junctions as because vacuum tubes were not sensitive to surface oxidation and vibration.

Vacuum packaging was a critical precursor to vacuum tube devices for two reasons. Firstly, thermionic emission for most materials occurs at temperatures of 1000 °C. Without vacuum packaging, convective cooling of the cathode would make devices

very power inefficient. Secondly, the distance between the emitting cathode and the anode was typically on the order of a centimeter so vacuum was necessary to extend the mean free path of electrons to this length. This principle is used today to transduce vacuum pressure to electronic signals in Bayard-Alpert vacuum ion gauges (Bayard and Alpert, 1950).

Vacuum tubes were refined and miniaturized between their invention and the middle of the 1900s. A transistor, termed a triode, was constructed by inserted a metallic grid between the cathode and the anode. A bias on the grid would serve to modulate the number of electrons that reached the anode. Later refinements included adding a second gate (termed the screen) between the gate and the anode to reduce the input impedance of the triode due to the Miller effect, and after that the addition of suppressor grid between the screen grid and the anode to prevent secondary electrons generated at the cathode from being collected by the screen.

Despite these refinements vacuum tubes suffered from serious drawbacks. Lifetimes were limited, and because of the necessity to heat the cathode, packing densities were limited by heat dissipation. In 1947 the first solid state transistor (the bipolar point contact transistor) was invented by John Bardeen, Walter Brattain, and William Shockley at Bell Labs. In 1959 Dawon Kahng and Martin Attala, also at Bell Labs, demonstrated the first metal oxide semiconductor field effect transistor (MOSFET), a device that has become ubiqutous in modern computers (Dawon, 1963). In both these devices, conduction took place inside the semiconductor, obviating the need for vacuum packaging. Additionally, no heating was necessary so device densities could be increased. A rapid changing of the guard took place as less reliable vacuum tubes were replaced by their solid state equivalents. Advances in semiconductor processing technology like zone melting for semiconductor purification and the ability to integrate active and passive devices onto a single wafer, patented by Jack Kilby of Texas Instruments in 1959 (Kilby, 1964), cemented the dominant status of solid-state devices for nearly all applications.

1.3 Microscale field emission devices

In 1961, a scientist working at Stanford Research Institute named Ken Shoulders proposed using the methods being developed for microscale semiconductor circuits to fabricate microscale vacuum tunneling devices (Shoulders, 1961). He envisioned a device that looked very similar to the vacuum tubes of a decade prior with an electron emitting cathode, an electrostatic gate, and an electron collecting anode all

machined with nascent microfabrication techniques and with dimensions and distances that were order's of magnitude smaller than their mascroscopic counterparts. Critically, his device would not operate via thermionic emission but would instead operate on the principle of Fowler-Nordheim tunneling (also called cold-field emission). Instead of giving electrons in a conductor sufficient energy to overcome the work function barrier by heating, this process involves applying a large electric field to the surface of a conductor. At field strengths of 1 GV/m the electrons in the conductor can tunnel into the surrounding medium. Assuming that medium is not an insulator the electron can proceed along the electric field gradient to a collector. Gating of emission could occur through several mechanisms: electrostatic deflection similarly to macroscopic vacuum tubes, modulation of the field at the emitter surface via a biased gate terminal, depletion of the supply of emitting electrons in the case of a semicondutor emitter, etc. Shoulder's critical insight was to realize that at micron scales or smaller the voltage difference between each terminal needed to cause field emission could be reduced to an attainable number, less than 1000 V. If the electron emitting surface were sharpened so that static field enhancement could take place, devices could operate at potential differences as low as 50 V. He postulated that such a device would be capable of switching times as fast as 10^{-10} s, be insensitive to ionizing radiation, be insensitive to temperature effects up to 1000 °C, and "have a useful lifetime of many hundreds of years."

Researchers following in Ken Shoulders footsteps developed the one of the first practical microscale field emission devices, the Spindt field emitter, in 1968 (Spindt, 1968). These devices were fabricated by simultaneously angle evaporating a dielectric and normal angle evaporating a low work function metal into a pre-defined microscale hole in a dielectric film on top of a metal layer. The angle evaporated dielectric gradually closed the hole through which the low work function metal was being evaporated, leading to a sharp field emitting tip. This technique has been refined to make high brightness vertical field emission arrays (FEAs). The vertical field emitter technology reached its peak during the 1990's as arrays of vertical field emitters were used in an effort to manufacture thin form-factor displays (Talin, Dean, and Jaskie, 2001). Despite some advantages, and even some commercial production, the field emission displays eventually lost out to LCD technology. In the past twenty years, refinement of vertical field emission devices has been focused on niche applications. For example, high brightness vertical field emitter arrays have been used for x-ray spectroscopy (Cheng, Hill, and Heubel, 2013), (Basu et al., 2015).

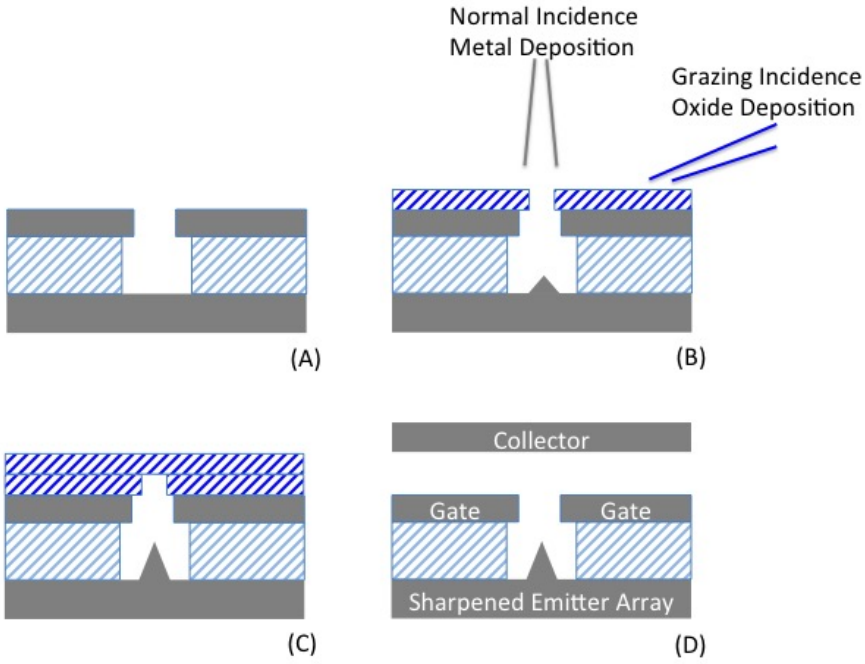

Figure 1.2: Fabrication process of Spindt Triode. In (A), shadow masking is used to make micron scale holes in top metal film, which later serves as the gate layer. Wet etching of gate dielectric layer (shown in light blue hatching) produces a cavity. In (B) the simultaneous deposition of a removable oxide at a grazing angle and a low work function metal at a normal angle produces an aligned tip at the base of the cavity. In (C), the oxide deposition eventually closes the aperture, producing a sharp tip. Finally in (D) the removable oxide is etched away and a collector is placed above the substrate.

A revolution in field emission devices came about in the early 2000s when CMOS technology became sufficiently refined to fabricate practical lateral field emission devices Driskill-Smith, Hasko, and Ahmed, 1997. Vertical field emitter arrays typically operated with electrode spacings as small as several hundred nanometers to several microns (Guerrera and Akinwande, 2016). These devices can obtain field emission, but only at greater than 50 Volts, and then only by oxide sharpening field emission tips to sub 10 nm radii. Sharp field emission tips are extremely susceptible to Joule heating and energetic ion bombardment, particularly when the device must be operated at voltages well above the ionization potential of residual gases. Lateral field emission devices can take advantage of modern lithography, thin film deposition, and etching techniques to produce emitter collector gaps that

are truly on the nanoscale. Nanoscale field emission devices may be operated at atmospheric pressures, since the mean free path of electrons in air is less than 200 nm, and at sub-10 Volts (Pescini et al., 2001). Furthermore, because the low operating voltages are due to the small emitter-to-collector gaps as opposed to static field enhancement from a small radii tips, these devices are potentially less susceptible to emitter damage from Joule heating or ion bombardment. Finally, if field emission transistors can be fabricated out of CMOS compatible materials and with CMOS compatible processes, lateral field emitters can be integrated with traditional MOSFETs to achieve combined functionality.

1.4 Plasmonics and field emission

A plasmon is the collective oscillation of electronic density in a conductor relative to the fixed, positive ionic background. At the interface of a conductor and a dielectric, these collective oscillations can interact with light to form surface plasmons, a coherent combination of oscillating electronic density in the conductor and the electromagnetic radiation in the dielectric that is produced by the oscillating electronic charge density (Maier, 2007). Surface plasmons have been an area of intense study for more than two decades, with applications including surface enhanced raman spectroscopy (Nie and Emory, 1997), photodectors Knight et al., 2011,

Recent work highlights the ability to combine plasmonics and field emission. We broadly split the issue into two: the production of plasmons via ballistic electron impact and the use of plasmons to generate enhanced field emission. Beginning with the first we highlight a number of experiments that demonstrate the generation of plasmons from ballistic electrons. One of the first experimental observations of surface plasmons was via electron energy loss spectroscopy of aluminum and magnesium (Powell and Swan, 1960). It was already experimentally demonstrated that electrons would excite the bulk plasmon mode with a corresponding energy loss of $\hbar\omega_p$ but Powell and Swan wanted to investigate theoretical predications that electrons could also excite a surface plamon mode. They reasoned that this surface plasmon mode would depend strongly on surface cleanliness and the presence of an oxide layer on aluminum and magnesium samples. They noticed an energy loss corresponding to $\hbar\omega_p/2$ on freshly deposited samples that gradually disappeared with time to be replaced by an energy loss corresponding to a lower energy mode, which matches a theory that includes oxide thickness. Recent work has extended this concept to nanoplasmonic structures. In 2009, Kuttge, Vesseur, and Polman were able to map the nodes and anti-nodes of a plasmonic Fabry-Perot cavity fabricated

by milling two grooves into gold film (Kuttge, E. J. R. Vesseur, and Polman, 2009). The grooves formed parallel mirrors and the electron beam acts as a point source for plasmons of wide range of frequencies. If the beam is placed on an anti-node of a resonant mode, the mode is excited and the generated light travels back and forth between the two mirrors. Some of this light is eventually scattered into free space by the groove mirrors or by surface roughness. This light is captured by a parabolic mirror and sent to a spectrometer. By varying the position of the electron beam and monitoring intensity changes for different wavelengths, the authors were able to map the nodes and anti-nodes of different plasmonic modes. Similar work has been done with Au nanowires (Ernst Jan R. Vesseur et al., 2007).

The reverse mechanism is also an area of active research. The use of metallic nano-tips stimulated to field emit by femto-second optical pulses to produce ultra-fast electronic pulses is an area of active research (Hommelhoff et al., 2006). Silicon field emitter arrays, like those used decades earlier have also been employed as high brightness, ultra-fast photocathodes (Swanwick et al., 2014). In both cases, the sharpened emitter tip serves to focus optically induced and electrostatic fields. This work has been recently been extended to plasmonic resonators in several studies (Forati et al., 2016) (Putnam et al., 2017). Forati, Dill, Tao, and Sievenpiper fabricated a three-dimensional structure consisting of closely spaced gold "mushrooms" that were connected by alternating finger electrodes to two separate electrical contacts (Forati et al., 2016). The gold mushroom structures act as coupled plasmonic resonators and adjacent mushrooms could be electrostatically biased. This combination of field due to electrostatic biasing and the time-varying electric field induced by the incident light served to produce the necessary field strength for emission to occur. Putnam, Hobbs, Keithley, Berggren, and Kartner demonstrated an on-chip device based on photoemission induced from plasmonic nanostructures. The authors fabricated arrays of gold resonators, either nanotriangles or nanorods, on indium tin oxide (ITO), a conducting dielectric. By irradiating the plasmonic arrays with a femtosecond laser source, the authors induced electrons to be field emitted into the surrounding air to be collected by ITO contact pad several microns away. At low pulse energies ($<$ .1 nJ) the emission process is governed by multi-photon absorption. At high powers, the authors demonstrate that there is direct tunneling via Fowler-Nordheim field emission induced by the instantaneous electric field.

The combination of plasmonics and field emission is very promising. As previously discussed, field emission devices have the potential to operate at extremely

high speeds. This is because Fowler-Nordheim tunneling is an intrinsically fast phenomenon, electrons traveling ballistically through vacuum have a very short transit time under the high fields involved, and capacitance can be engineered to be very small because the gating mechanism doesn't rely on depleting a semiconductor channel. The intrinsic capacitance of individual nanoscale devices suggests that they could operate at frequencies of 0.5 Thz (Han, Sub Oh, and Meyyappan, 2012). With individual devices capable of switching this quickly, it will be the capacitance of the metal contact lines connecting devices that will limit the operating frequency. If nanoscale field emission devices can be modulated by (and modulate) light, it raises the possibility that field emission transistors (FEmTs) can be integrated with on-chip light sources to create electro-optic circuits. This would by-pass the metal contact line all together. Plasmonics provides a mechanism to increase the interaction of light with field emission devices so that the intensities common to on-chip silicon photonics are sufficient to make electro-optic devices.

1.5 Objective of this thesis

The objective of this thesis work is to demonstrate, experimentally and theoretically, design paradigms for field emission devices that could compliment or replace existing solid state equivalents. We will provide a theoretical underpinning for Fowler-Nordheim emission, as well as the closely relevant Frenkel-Poole conduction. We will then discuss our early attempts to make field emission devices as well as our successful paradigm for field emission transistors. We will also discuss our work on combining field emission and plasmonics into a single, telecommunications wavelength device. Finally we will close with an addenda on nanofabrication tips, provided for the benefit of future students, that contains recipes and tips for successfully fabricating devices like those seen here.

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Chapter 2

THEORETICAL DISCUSSION OF FOWLER-NORDHEIM EMISSION, FRENKEL-POOLE EMISSION AND LIGHT ENHANCED EMISSION

The devices in this thesis operate on physical principles familiar to different disciplines. Fowler-Nordheim field emission is of course the operative principle for micro- and nanoscale field emission, Frenkel-Poole tunneling is familiar to those working on semiconductor devices, and light induced tunnel ionization has been studied extensively for THz electronics. Since the devices in this thesis build upon each of these process it is convenient to describe them in brief detail in a single source.

2.1 Fowler-Nordheim emission: electron tunneling through a triangular barrier

The triangular barrier Fowler-Nordheim problem is one used in many undergraduate and graduate texts to demonstrate the Wentzel, Kramers, Brillouin (WKB) approximation (Shankar, 2012). Under this approximation, one solves for the wave-function of an electron in a space varying potential by assuming that the potential changes slowly in comparison to the de-Broglie wavelength so that the wave function is plane-wave like:

$$\phi(x) = A \exp\left(\frac{iS(x)}{\hbar}\right)$$

with a time-varying phase $S(x)$ that is Taylor expanded in powers of $\hbar$.

$$S(x) = S_0(x) + \hbar S_1(x) + \frac{\hbar^2}{2} S_2(x) + \ldots$$

Substituting of $\phi(x)$ into the time-independent Schrödinger equation equation and demanding that the coefficient of each power of $\hbar$ separately cancels gives

$$\begin{aligned} S_0 &= \pm \int_{x_0}^{x_1} p(x)dx \\ S_1 &= \frac{i}{2} \ln\left(\frac{p(x)}{\hbar}\right) \end{aligned}$$

where $p(x) = \sqrt{2m[E - V(x)]}$ is the momentum. In the WKB approximation, we ignore all powers of $\hbar$ that are higher than one. The wave function has both right

traveling and left traveling solutions as

$$\phi_{\pm}(x) = \frac{\phi(x_0)p(x_0)^{1/2}}{p(x)^{1/2}} \exp\left(\pm\frac{i}{\hbar}\int_{x_0}^{x} p(x)dx\right)$$

From this, it can be shown (Liboff, 2003) that the transmission coefficient across a finite potential extending from x_0 to x_1 is

$$\begin{aligned} T(E) &= \exp\left(-\frac{2}{\hbar}\int_{x_0}^{x_1} p(x)dx\right) \\ &= \exp\left(-\frac{2}{\hbar}\int_{x_0}^{x_1} \sqrt{2m[V(x)-E]}dx\right) \end{aligned}$$

We now seek to apply this formulation to the triangular barrier Fowler-Nordheim problem to solve for the field emission current. Here the potential is given by $V(x) = E_F + \Phi - eE_{es}x$, where E_F is the Fermi energy, Φ is the work function of the emitting material, and E_{es} is the applied electrostatic field. The conductor-vacuum surface is at $x = 0$ as shown in 2.1 From Figure 2.1 we see that that x_1,

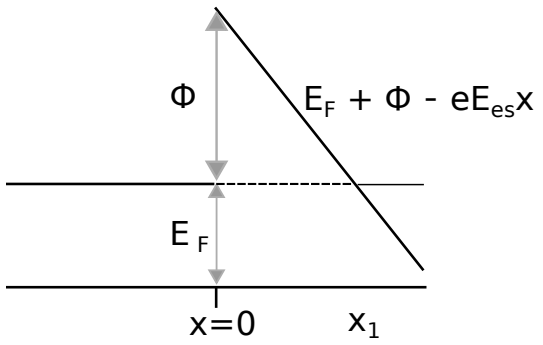

Figure 2.1: Triangular potential barrier in elementary Fowler-Nordheim problem

the point in vacuum where the potential energy is equal to the energy E is given by $x_1 = \frac{(\Phi+E_F)-E}{eE_{es}}$. Inserting the Fowler-Nordheim potential into the transmission coefficient equation, we have

$$\begin{aligned} T(E) &= \exp\left(-\frac{2}{\hbar}\int_{0}^{\frac{(\Phi+E_F)-E}{eE_{es}}} \sqrt{2m[(E_F+\Phi-eE_{es}x)-E]}dx\right) \\ &= \exp\left(-\frac{2}{\hbar}\int_{0}^{\frac{(\Phi+E_F)-E}{eE_{es}}} \sqrt{2m[((E_F+\Phi)-E)-eE_{es}x]}dx\right) \end{aligned}$$

We make the substitution

$$y = \frac{eE_s}{(E_F+\Phi)-E}x$$

And our expression becomes

$$\begin{aligned} T(E) &= \exp\left(-\frac{2}{\hbar}\frac{((\Phi+E_F)-E)}{eE_{es}}\int_0^1 \sqrt{2m[((E_F+\Phi)-E)-((E_F+\Phi)-E)\,y]}dy\right) \\ &= \exp\left(-\frac{2}{\hbar}\frac{((\Phi+E_F)-E)^{3/2}}{eE_{es}}\int_0^1 \sqrt{2m[1-y]}dy\right) \\ &= \exp\left(-\frac{2}{\hbar}\frac{((\Phi+E_F)-E)^{3/2}}{eE_{es}}\left(\frac{-2}{3}\sqrt{2m}\,(1-y)^{3/2}\Big|_{y=0}^{y=1}\right)\right) \\ &= \exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{((\Phi+E_F)-E)^{3/2}}{eE_{es}}\right) \end{aligned}$$

The expression $T(E)$ already has many of the familiar characteristics of the Fowler-Nordheim result including the exponential dependence on $-\frac{\Phi^{3/2}}{eE_{es}}$. To determine the current we integrate the product of the electronic charge, the electron velocity, the distribution function, and the transmission coefficient in k-space. We note the relationship $E_i = E(k_i) = \frac{(\hbar k_i)^2}{2m}$ for later use. The expression for the tunneled current is

$$J(E_{es}) = \frac{e}{2\pi}\int_0^\infty \frac{\hbar k_x}{m} f(k_x)T(E_x(k_x))dk_x$$

We have heretofore ignored the three-dimensional nature of the problem but we now evaluate the integral in all three dimensions, assuming the x-direction is perpendicular to the interface. Then the electron velocity, perpendicular to the interface, is $\frac{\hbar k_x}{m}$ seen in the expression for $J(E_{es})$. Here $f(k_x)$ is the Fermi-Dirac distribution as a function of the perpendicular momenta obtained by integrating the Fermi-Distribution in cylindrical coordinates, denoting the magnitude of the wavevector that is parallel to the interface as $k_\parallel$,

$$\begin{aligned} f(k_x) &= \frac{2}{(2\pi)^2}\int_0^\infty \frac{2\pi k_\parallel dk_\parallel}{\exp\left(\beta[E_\parallel + E(k_x) - E_F]\right)+1} \\ &= \frac{2}{(2\pi)^2}\int_0^\infty \frac{2\pi k_\parallel dk_\parallel}{\exp\left(\beta[\frac{(\hbar k_\parallel)^2}{2m} + E(k_x) - E_F]\right)+1} \end{aligned}$$

substituting

$$y = \hbar\sqrt{\frac{\beta}{2m}}k_\parallel$$

we have

$$f(k_x) = \frac{2}{(2\pi)}\frac{2m}{\beta\hbar^2}\int_0^\infty \frac{ydy}{\exp\left(\beta[E(k_x)-E_F]\right)\exp(y^2)+1}$$

The solution to the indefinite integral can be found using Wolfram Mathematica as

$$\begin{aligned} f(k_x) &= \frac{2}{(2\pi)}\frac{2m}{\beta\hbar^2}\frac{1}{2}\left(y^2 - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\exp(y^2) + 1\right]\right)\Bigg]_{y=0}^{y\to\infty} \\ &= \frac{m}{\pi\beta\hbar^2}\left(y^2 - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\exp(y^2) + 1\right]\right)\Big]_{y=0}^{y\to\infty} \end{aligned}$$

We evaluate the inner expression in the limit to infinity

$$\begin{aligned} &\lim_{y\to\infty}\left(y^2 - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\exp(y^2) + 1\right]\right) \\ =\ &\lim_{y\to\infty}\left(y^2 - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\exp(y^2)\right]\right) \\ =\ &\lim_{y\to\infty}\left(y^2 - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\right] - \log\left[\exp(y^2)\right]\right) \\ =\ &\lim_{y\to\infty}\left(y^2 - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\right] - y^2\right) \\ =\ &-\log\left[\exp\left(\beta[E(k_x) - E_F]\right)\right] \end{aligned}$$

We then have the expression for the Fermi-Dirac distribution

$$\begin{aligned} f(k_x) &= \frac{m}{\pi\beta\hbar^2}\left(\log\left[\left(\exp\left(\beta[E(k_x) - E_F]\right)\right] + 1\right) - \log\left[\exp\left(\beta[E(k_x) - E_F]\right)\right]\right) \\ &= \frac{m}{\pi\beta\hbar^2}\left(\log\left[\left(\exp\left(\beta[E(k_x) - E_F]\right)\right] + 1\right)\right) \end{aligned}$$

Near $T = 0$, this expression simplifies to

$$\begin{aligned} f(k_x) &= \frac{m}{\pi\beta\hbar^2}\left(\beta[E_F - E(k_x)]\right) \\ &= \frac{m}{\pi\hbar^2}\left(E_F - E(k_x)\right) \end{aligned}$$

for $E(k_x) \leq E_F$ and 0 otherwise. We now insert expressions for $f(E(k_x))$ and $T(E(k_x))$. We will solve the remainder in energy-space where $dE_x = \frac{\hbar^2 k_x}{m} dk_x$.

$$\begin{aligned} J(E_{es}) &= \frac{e}{2\pi}\int_0^\infty \frac{\hbar k_x}{m} f(k_x) T(E(k_x)) dk_x \\ &= \frac{e}{2\pi\hbar}\int_0^\infty f(E_x) T(E_x) dE_x \end{aligned}$$

We insert our $T = 0$ approximation for $f(E_x)$ and obtain

$$\begin{aligned} J(E_{es}) &= \frac{em}{2\pi^2\hbar^3}\int_0^{E_F} \left(E_F - E_x\right) T(E_x) dE_x \\ J(E_{es}) &= \frac{em}{2\pi^2\hbar^3}\int_0^{E_F} \left(E_F - E_x\right) \exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{\left((\Phi + E_F) - E_x\right)^{3/2}}{eE_{es}}\right) dE_x \end{aligned}$$

We set $y = E_F - E_x$ and obtain

$$J(E_{es}) = \frac{em}{2\pi^2\hbar^3}\int_0^{E_F} y \exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{(\Phi+y)^{3/2}}{eE_{es}}\right)dy$$

We Taylor expand the term inside the exponential to first order in y to obtain

$$\exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{(\Phi+y)^{3/2}}{eE_{es}}\right) \approx \exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{\Phi^{3/2}}{eE_{es}}\right)\exp\left(-\frac{2\sqrt{2m}}{\hbar}\frac{\Phi^{3/4}y}{eE_{es}}\right)$$

We can now pull out the constant exponential factor

$$J(E_{es}) = \frac{em}{2\pi^2\hbar^3}\exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{\Phi^{3/2}}{eE_{es}}\right)\int_0^{E_F} y \exp\left(-\frac{2\sqrt{2m}}{\hbar}\frac{\Phi^{3/4}y}{eE_{es}}\right)dy$$

We use the Wolfram Mathematica to solve the indefinite integral as

$$\begin{aligned} J(E_{es}) &= \frac{em}{2\pi^2\hbar^3}\exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{\Phi^{3/2}}{eE_{es}}\right)\left(\frac{\hbar eE_{es}}{2\sqrt{2m}\Phi^{3/4}}\right)^2 \times \\ &\quad \left[-\exp\left(-\frac{2\sqrt{2m}}{\hbar}\frac{\Phi^{3/4}y}{eE_{es}}\right)\left(\frac{2\sqrt{2m}}{\hbar}\frac{\Phi^{3/4}y}{eE_{es}}+1\right)\right]_{y=0}^{y=E_F} \\ &= \frac{e}{16\pi^2\hbar}\frac{F^2}{\Phi^{3/2}}\exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{\Phi^{3/2}}{F}\right) \end{aligned}$$

where we assumed the that the exponential evaluated at $y = E_F$ is very small. We have also made the typical substitution $F = eE_{es}$. This is the Fowler-Nordheim equation, though the exact form of the constant multiple varies depending on the assumptions made during the derivation. Regardless, all variations of the Fowler-Nordheim current vary as

$$J(F) = \propto F^2 \exp\left(-\frac{4\sqrt{2m}}{3\hbar}\frac{\Phi^{3/2}}{F}\right)$$

This dependency is the basis for the common technique of plotting suspected field emission current in so-called Fowler-Nordheim coordinates. That is, the x-coordinate is plotted as $\frac{1}{F}$ (or more commonly as $\frac{1}{V}$ where V is the macroscopically applied voltage, including contact resistances). The y-coordinate is plotted as $\log\left(\frac{J}{F^2}\right)$ (or more commonly as $\log\left(\frac{I}{V^2}\right)$ where I is the macroscopically measured current). In these coordinates, the characteristic of field emission is a straight line. To illustrate this we have generated an example plot of field emission current in standard coordinates in Figure 2.2 using illustrative values for the constants in the

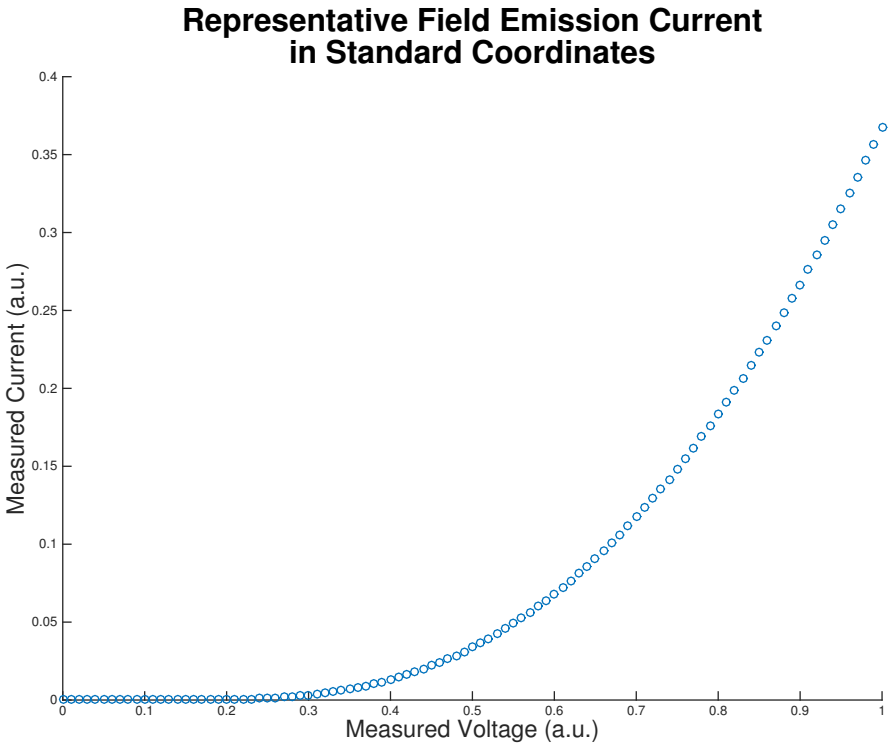

Figure 2.2: Representative Fowler-Nordheim current/voltage data plotted in standard coordinates.

Fowler-Nordheim equation and we have plotted the same data in Fowler-Nordheim coordinates in Figure 2.3. The assumptions made during the above derivation of field emission current are numerous. The triangular barrier above does not take into account the image charge potential caused by an electron that is a distance x from the surface of a conductor. The Schottky-Nordheim barrier given in (Zhu, 2004)

$$\begin{aligned} V(x) &= E_F + \Phi - eE_{es}x - V_{Image}(x) \\ &= E_F + \Phi - eE_{es}x - \int_x^\infty -\frac{e^2}{16\pi\epsilon_0 y^2}dy \\ &= E_F + \Phi - eE_{es}x - \frac{e^2}{16\pi\epsilon_0 x} \end{aligned}$$

The Schottky-Nordheim barrier is the simplest realistic model for field emission, as the formula above using the triangular Fowler-Nordheim barrier typically under predicts the current density by a factor of 100-500 (Forbes, n.d.). Additionally, during the above derivation the Fermi-Dirac distribution was simplified by assuming that $\beta E_F \approx 0$, an assumption that is only generally true for either $T = 0$ or for metals where the Fermi energies are 1-10 eV(Ashcroft and Mermin, 2005). More accurate

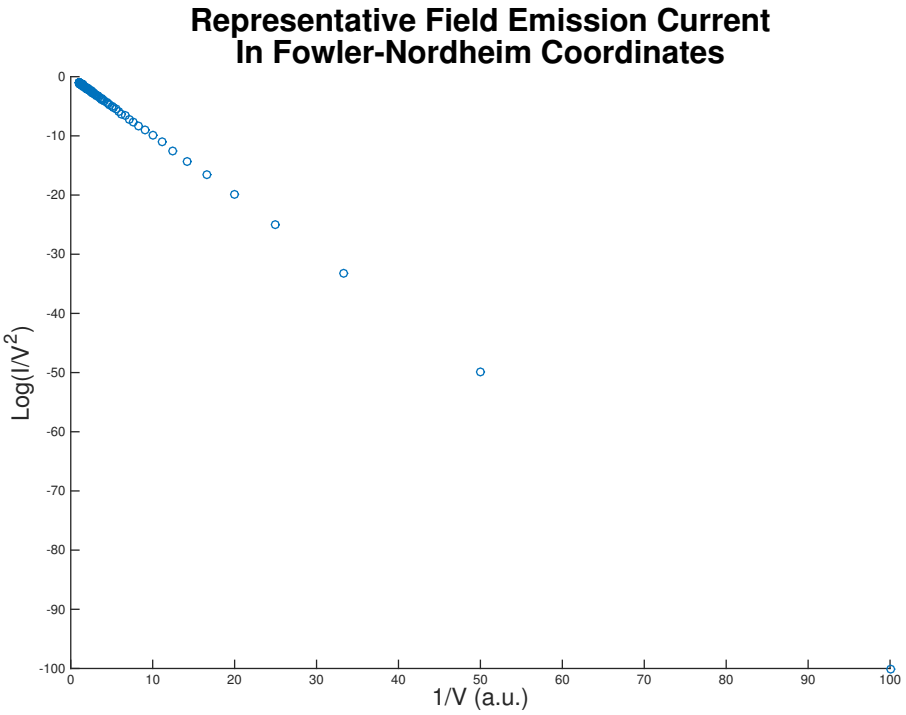

Figure 2.3: Representative Fowler-Nordheim current/voltage data plotted in Fowler-Nordheim coordinates.

formulations of the Fowler-Nordheim equation due to Murphy and Good (Murphy and Good, 1956) but in practice they are invariably simplified for experimental situations to retain the usual dependencies on voltage.

2.2 Frenkel-Poole emission

In 1938 Frenkel attempted to to explain pre-breakdown current in insulators by appealing to a simple model based on assuming that an insulator consisted of neutral atoms (Frenkel, 1938). Conduction in the insulator would then consist of two parts: thermal ionization of bound electron and then that electron traveling under the influence of the combination of the field of the now ionized donor atom and any external field. The electron in absence of the electric field is modeled as experiencing a standard Coulomb potential, seen in Figure 2.4(A)

$$V_i(r) = E_c - \frac{e^2}{\epsilon r}$$

where the atom is located at $r = 0$ and E_c is the conduction band energy of an electron traveling freely far away from its donor atom. The emission rate depends on the ionization energy in a standard Arrhenius fashion (Mitrofanov and Manfra,

2004)

$$e(T) = AT^2 \exp\left(-\frac{E_i}{kT}\right)$$

where E_i is the ionization energy to move the electron from radius r_0 to in $r = \infty$. An applied electric field E_{es} lowers the barrier, as seen in Figure 2.4(B) by changing the potential experienced by the electron to

$$V_f(r) = E_c - \frac{e^2}{\epsilon r} - eE_{es}r$$

From the figure we see that in the forward direction there is a maximum potential

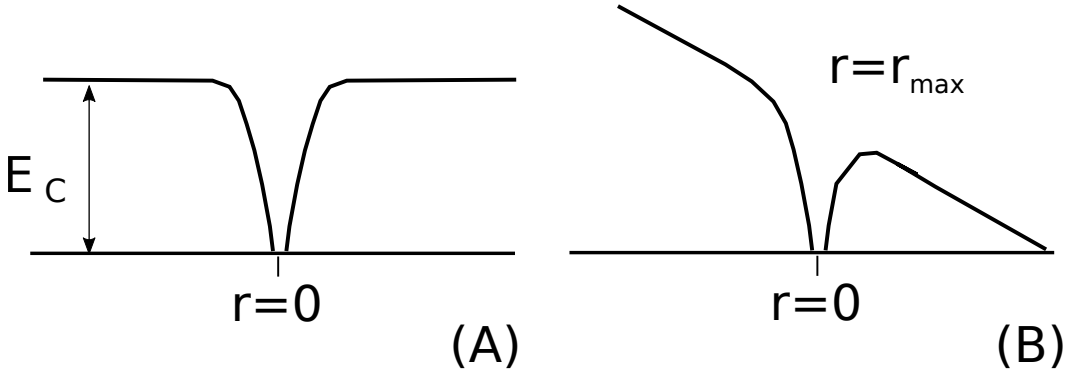

Figure 2.4: Diagram of potential electron experiences in insulator as modeled by J. Frenkel in the absence of an applied electric field (A) and in the presence of an applied electric field (B)

energy, which is reduced from the original barrier energy. The maximum is located at $r_{\max}$, which can be found by setting $V'(r) = 0$ and solving for r:

$$\begin{aligned} 0 &= V'(r_{\max}) \\ &= -eE_{es} + \frac{e^2}{\epsilon r_{\max}^2} \\ r_{\max} &= \sqrt{\frac{e}{\epsilon E_{es}}} \end{aligned}$$

Then, we see that the potential barrier faced by an electron at r_0 to escaping is reduced by an amount ΔV equal to

$$\begin{aligned} \Delta(V) &= V_f(r_{\max}) - V_i(r_{\max}) \\ &= -eE_{es}r_{\max} \\ &= -\sqrt{\frac{e^3}{\epsilon}}\sqrt{E_{es}} \\ &= -\beta\sqrt{E_{es}} \end{aligned}$$

We see that the emission probability is now modified by an additional factor

$$e(T) \quad = \quad e_0 \exp\left(\frac{\beta\sqrt{E_{es}}}{kT}\right)$$

The conductivity in the insulator is proportional to the emission probability, and the current density $J(E_{es})$ is proportional to the applied field multiplied by the conductivity so that

$$J(E_{es}) \quad \propto \quad E_{es} \exp\left(\frac{\beta\sqrt{E_{es}}}{kT}\right)$$

This is the phenomenological expression for Frenkel-Poole current. If the lattice of the insulator contains defects or if the path is along the surface of an insulator, which necessitates the existence of dangling bonds conduction via Frenkel-Poole emission becomes easier, since the potential well of each trap state will be shallower. Importantly though, the dependencies of Frenkel-Poole emission on the electric field are not the same as the dependencies of Fowler-Nordheim emission on the electric field, so the two phenomena can be distinquished by plotting suspect current-voltage data in Fowler-Nordheim coordinates and looking for linearity.

2.3 Light induced field emission

The emission of electrons into free space due the interaction with a strong time-varying electromagnetic field has been studied for more than a hundred years. Famously, Albert Einstein described the photoelectric effect by appealing to the then unknown quantum nature of light (Einstein, 1905). By foregoing the classical description of light as an electromagnetic wave, he was able to describe a slew of photoelectric results (Stoletow, 1888). The typical photoelectric experiments took place in vacuum and consisted of irradiating a cathode metal with light. The cathode would be biased relative to an anode (also in vacuum) and by changing the relative biases, the current leaving the cathode and entering the anode could be modulated. The frequency and intensity of the incident light could also effect the measured current. Einstein's model was able to explain the following items:

- Particular metals irradiated with light in vacuum and under constant bias showed no photoemission as the frequency of the incident light was increased from a low value until a particular frequency ω_{pe} was reached. Above ω_{pe} the photoemitted current increased with increasing frequency for fixed incident light intensity.

- For frequencies of incident light at or above the critical frequency, the photoemitted current increased with increasing intensity.
- Applying a negative bias to the anode (relative to the cathode) while keeping the frequency and intensity of incident light fixed could decrease the current measured at the anode. At some voltage V_{cutoff} the current would stop completely.
- The magnitude of V_{cutoff} increased as the frequency of light increased and was independent of the intensity of the incident light.

The items could be explained by assuming that each photon had an energy $E_{ph} = \hbar\omega$ that could be transferred to a conduction electron. If $E_{ph} > \Phi$, the work function of the material, then it was possible for a single photon to give a single electron enough energy to leave the metal surface and enter vacuum. Once in vacuum, the electron can have a maximum energy of $E_{ph} - \Phi$ and traveling against a repelling voltage V_{cutoff} on an anode placed a distance d from the emitting surface will be able to reach the anode if $E_{ph} - \Phi > dqV_{\text{cuttoff}}$.

More recently, the in-detail mechanics of light absorption in atoms and also in solids was laid out by Keldysh in 1965 (Keldysh, 1965). Keldysh identified two regimes for photon absorption. The first regime is multi-photon absorption where the dominant energy transfer mechanism is consecutive absorption of photons by an electron until it has enough energy to reach the conduction band (in the case of ionization) or to leave the solid entirely in the case case of emission to vacuum The photoelectric effect described by Einstein is the limiting case where only a single photon is needed to overcome the work function. Multi-photon absorption dominates at high frequencies where each photon can impart a significant fraction of the work function energy to an electron. At very high intensities, Keldysh identified the possibility of light induced field emission. In this so-called 'strong field' regime, electrons can tunnel across the instantaneous barrier directly. These two regimes are shown in Figures 2.5 and 2.6.

The delineation between the two regimes is determined by the tunneling time of an electron through the instantaneous barrier generated by the incident light's electric field F. If Φ is the work function of the emitting material, then the barrier width is

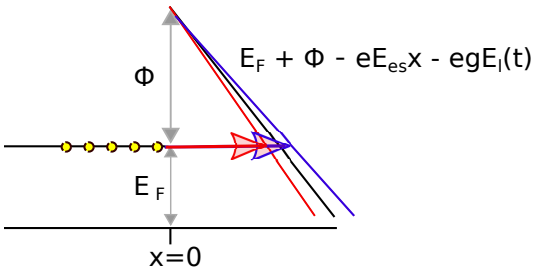

Figure 2.5: Diagram of the light induced field emission process for $\gamma \ll 1$ regime. In this model, electrons can tunnel during the red part of the cycle.

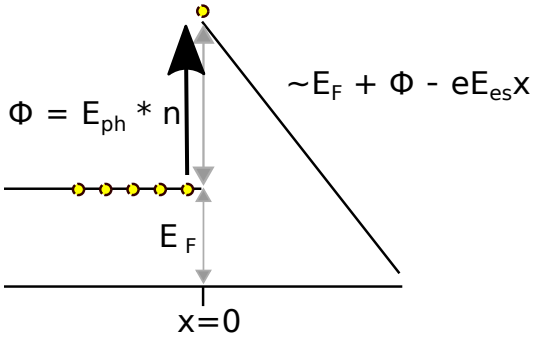

Figure 2.6: Diagram of the multi-photon induced field emission process for $\gamma \gg 1$ regime

$\frac{\Phi}{eF}$. The electron velocity is of order $\sqrt{\frac{\Phi}{2m}}$. Therefore the approximate transit time

$$\begin{aligned} T &= \frac{\sqrt{2m}\Phi}{eF\sqrt{\Phi}} \\ &= \frac{\sqrt{2m\Phi}}{eF} \end{aligned}$$

Keldysh states that light induced field emission will occur when $\omega_T = \frac{eF}{\sqrt{2m\Phi}}$ is large compared to the incident light frequency ω so that the electron has sufficient time to tunnel through the barrier before an optical half-cycle elapses and the instantaneous electric field reverses direction. This leads to the definition of the so-called Keldysh parameter

$$\begin{aligned} \gamma &= \frac{\omega}{\omega_T} \\ &= \omega\frac{\sqrt{2m\Phi}}{eF} \end{aligned}$$

The order of magnitude nature of the Keldysh parameter belies its usefulness as a convenient metric for determining the governing physics for light induced electronic emission. For $\gamma \ll 1$ a quasi-static Fowler-Nordheim model has accurately modeled

the emitted current from plasmonic nano-structures (Putnam et al., 2017). This model assumes that field emitted current obeys the Fowler-Nordheim Law $J_{FN}(E)$ with the field given by the sum of the electrostatic field and the instantaneous light field $E = E_{es} + gE_l(t)$. Here g accounts for any plasmonic enhancement. For $\gamma \gg 1$ multi-photon absorption dominates and the emitted current obeys a multi-photon Beer's law $J \propto I^n$ (Nathan, Guenther, and Mitra, 1985). This regime has also been extensively studied in nanostructures and metallic tips (Bormann et al., 2010).

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Chapter 3

EARLY ATTEMPTS AT FIELD EMISSION DEVICES

Part of the work that appears in this chapter was published in the conference proceedings of the International Vacuum Nanoeelectronics Conference 2016 (Jones, Lukin, and Scherer, 2016). It is included here with the permission of the publisher.

3.1 In-plane emission devices

Our initial attempts to make field emission devices focused on using silicon on insulator (SOI) substrates to make completely in-plane gated field emission devices. This concept built upon the work of Pescini et al. (Pescini et al., 2001) in which the authors patterned doped silicon on insulator into a four terminal device as shown in Figure 3.1.Two gate electrodes (G1 and G2) were symmetrically placed around the axis of the emitter (E) and collector (C) so that the non-axial component of the field caused by voltage difference between the emitter and collector is cancelled out.

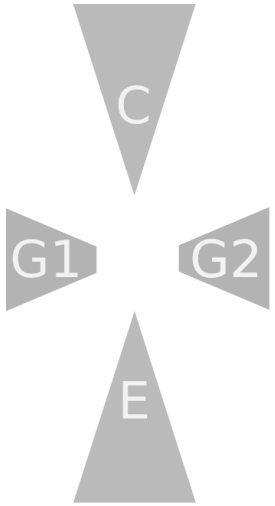

Figure 3.1: Diagram of doped SOI field emitter geometry used in Pescini et al.

3.2 In-plane emission devices via shadow deposition

Our initial work focused on patterning un-doped SOI, taking advantage of improved resolution from electron beam lithography to make smaller emitter-collector and emitter-gate gaps then was possible before. After patterning, an alumina hard mask was deposited and lifted off in hot Remover PG. The hard mask protected the tip

regions during a reactive ICP SF_6/C_4F_8 etch. The etched structure was undercut with dilute hydrofluoric acid. Then low work function metals could be deposited directly onto the undercut structure. The undercut acted as a shadow mask to separate the metal on top of the silicon scaffolding from the metal on the oxide underneath. In this manner we hoped to improve on the total emitted current found in (Pescini et al., 2001), since metals have significantly more conduction electrons than silicon. In addition, the metals in general have higher thermal conductivities, which should help prevent tip destruction via Joule heating. Finally, the procedure is agnostic to the deposited metal so that low work function metals, like zirconium alloyed with tungsten, could be used.

Initially, the devices were tested using a probe station in atmosphere. The in-plane field emitters demonstrated very poor emission characteristics. Despite the 30 nm emitter-to-collector gap which would suggest that field emission should begin at approximately 30 volt bias (assuming as a worst-case no static field enhancement due to sharp emitter tips), most devices never emitted even at 100 V bias. We attributed this failure to contamination of our emitting tips by adsorbed molecules (Zhu, 2004).

3.3 Vacuum Testing with Automated Setup

To ensure that the tips of the partially suspended field emitting diodes were clean, my undergraduate researchers and I built a custom vacuum chamber with a heated sample stage. Because the testing would take place inside vacuum, the testing setup incorporated an automated stage to move the heated stage (and the chip sitting on top of it) underneath a set of fixed probes. Software was developed to automate the entire testing process by first calibrating the measured position of particular devices on a chip with their designed positions from the CAD file. The software could then move the chip to underneath the probes to place the large contact pads (250 μm×250 μm) underneath the probe tips. The probes were then brought into contact with the device and the source meters (Keithley series) turned on and instructed to perform the required testing.

The chamber was constructed by glueing 1" thick acrylic sheets to each other to form five sides of a cubic chamber approximately 1.5 feet along each side. The base is a metal plate with a square o-ring that contains feed throughs for electrical testing and for USB feedthroughs to run the automated stage. The heavy acrylic top of the chamber is lifted up to open the chamber and gently lowered to close the chamber by

an industrial pulley. The system is evacuated by a combination of a turbo-molecular pump backed by an oil rotary vane pump. Initially, the acrylic chamber contains solvent that outgasses over several days. After outgassing, the acrylic chamber could be pumped to approximately 10^{-5} torr after four hours and could eventually reach a pressure of 10^{-6} torr after several days. The entire system is shown closed in Figure 3.2 and in detail in Figures 3.3, 3.4, 3.5, 3.6, 3.7, and 3.8.

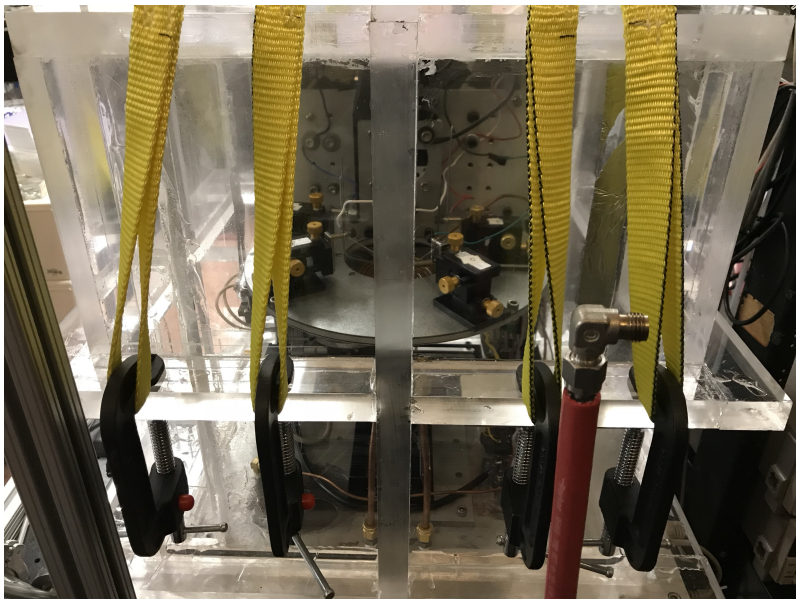

Figure 3.2: Custom vacuum system shown here with the acrylic lid lowered. The yellow straps connect to a pulley system for lifting and lowering the acrylic lid.

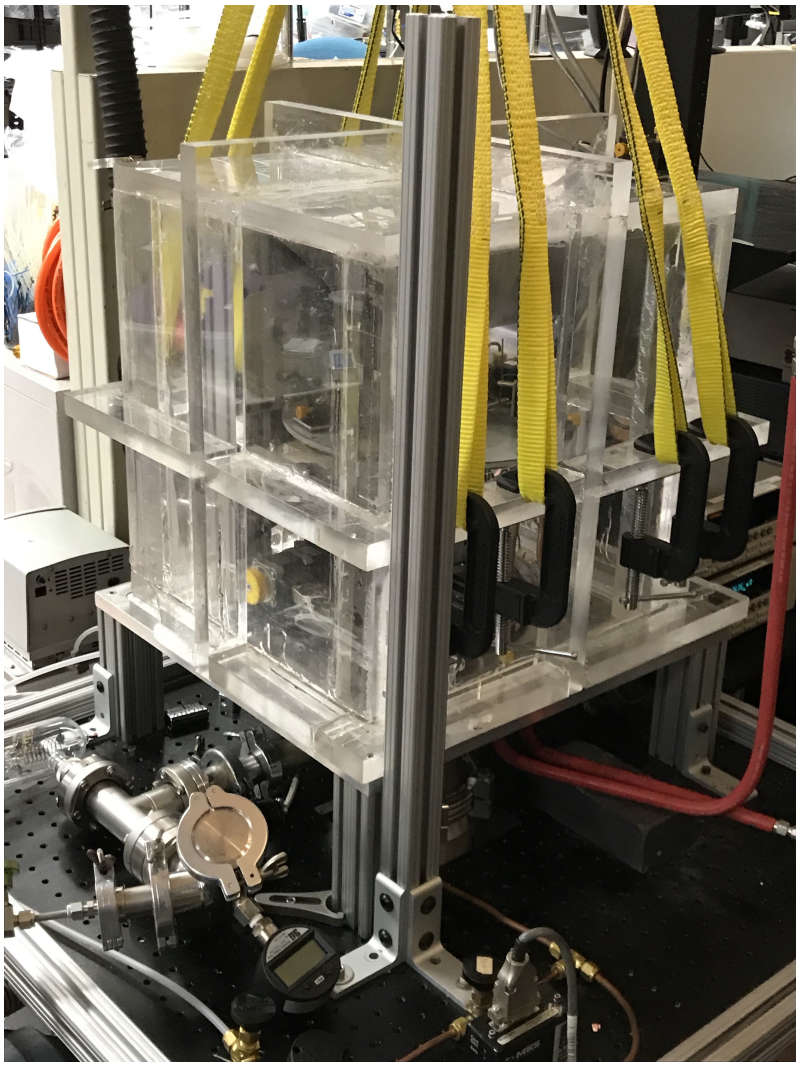

Figure 3.3: Custom vacuum system shown here with the acrylic lid lowered. The metallic base contains feed-throughs for electronics to run the stage and to connect each probe to sourcemeters. The base also contains vacuum feed-throughs for pressure gauges and for the turbo-molecular and rotary vane pumps.

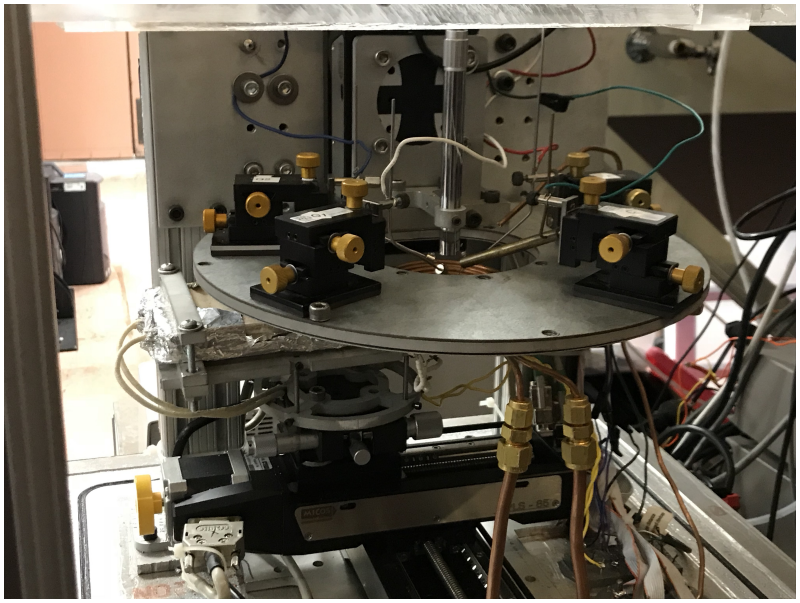

Figure 3.4: Custom vacuum system shown here with the acrylic lid raised. The probes sit on a machined probe stand that is stationary in the horizontal directions but moves in the vertical direction. The stage consists of an industrial heater with a two-inch heating surface and is moved in the horizontal plane by the automated stage.

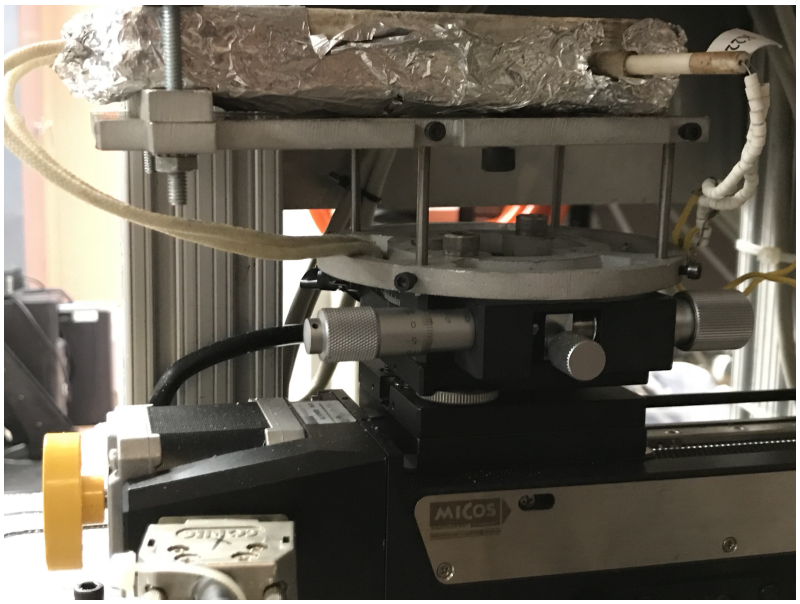

Figure 3.5: The heated stage shown here is capable of heating the sample in excess of 600 °C, while in vacuum. A copper plate with screws to hold the chip in place is used to uniformly conduct heat across the sample. At low pressures the radiative heating from the stage at high temperatures does not compromise the integrity of the acrylic cover.

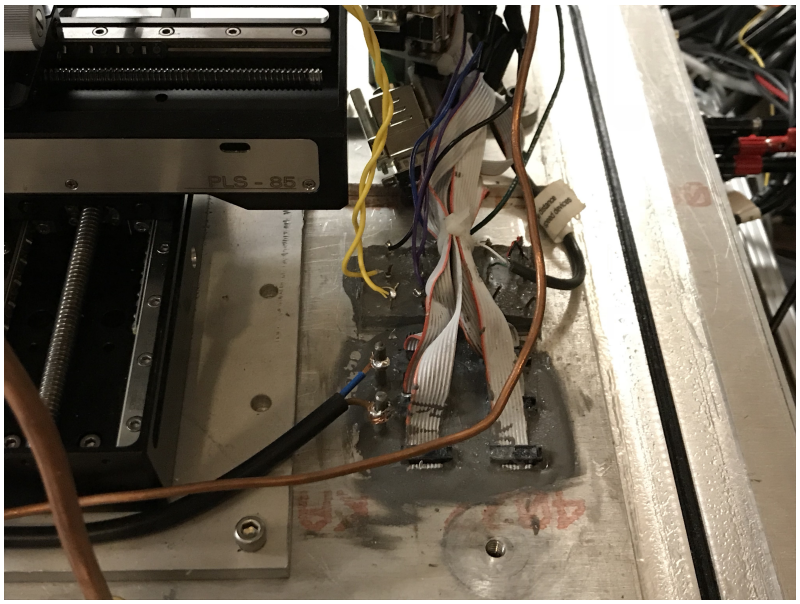

Figure 3.6: Electrical feedthroughs to connect the probes, stage heater, and stage thermocouple to stage controllers, sources, and controlling computers outside the vacuum.

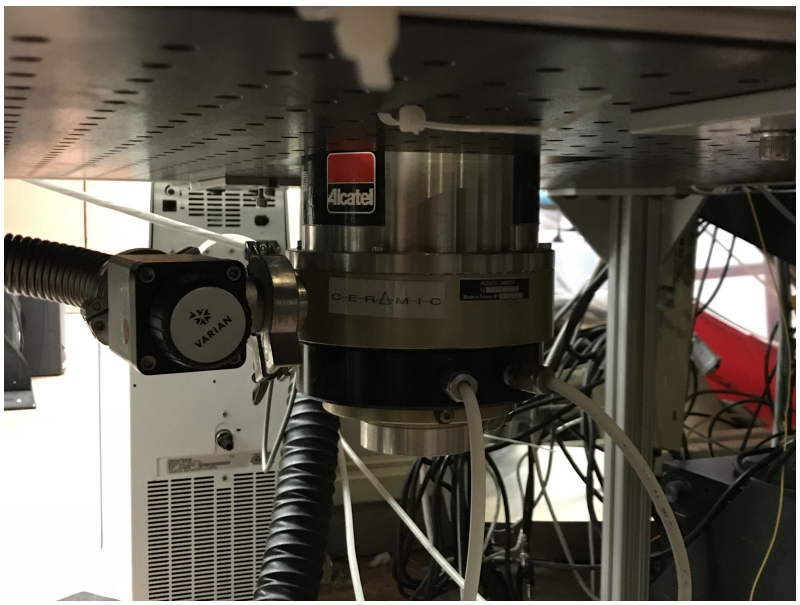

Figure 3.7: Water cooled turbo-molecular pump allows the sealed chamber to reach 5×10^{-5} torr in 3 hours. The turbo-molecular pump is backed by an oil rotary vane pump. The chamber is roughed through the turbo-molecular pump which is turned on when the chamber pressure reaches 5×10^{-2} torr.

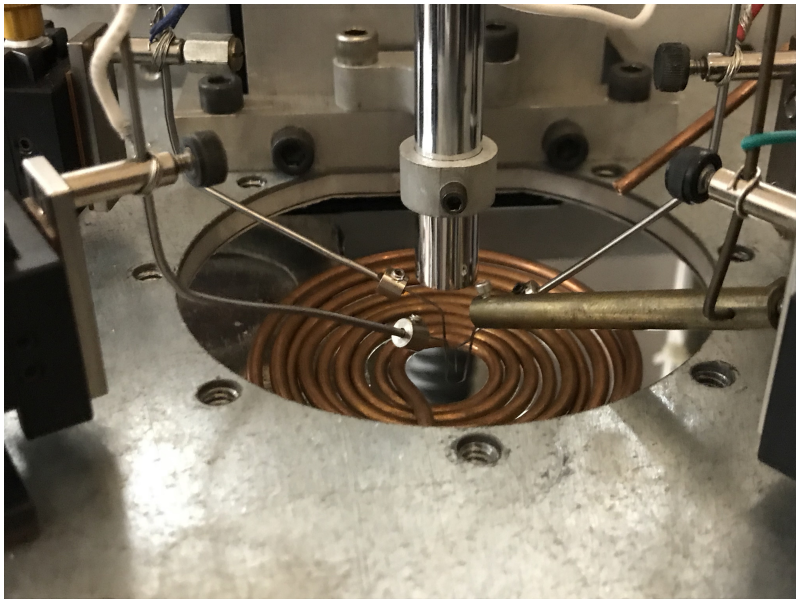

Figure 3.8: Four electrical probes on vertically moving stage allows for automated testing of gated devices.

3.4 In-plane two terminal devices fabricated on silicon dioxide/silicon scaffolding

In addition to improving the measurement setup by incorporating heating and vacuum desorption we implemented several device design changes. The emitter-to-collector gap dimensions that were manufacturable via the previously discussed process were 30 nm. As stated before, one would expect to see field emission at approximately 30 V from these devices, ignoring static field enhancement. If the emitter-to-collector dimension could be manufactured even smaller, it was reasoned, field emission could occur at less than 10 volts, which would be easier to integrate with modern CMOS. A new fabrication procedure was developed to accomplish this goal, and is shown in Figure 3.9. The initial substrate, shown in (a) is undoped silicon on insulator wafers (SOI, 220 nm device layer /2000 nm buried oxide layer). Nanoscale field emission tips and contacts are patterned using electron beam lithography (using PMMA A2 950 diluted 1:1 with anisole) in (b). The pattern was then transferred to an alumina hardmask by electron beam evaporating Al_2O_3 onto the substrate and performing liftoff in hot Remover PG, shown in (c) and (d). Beam blur in the electron beam patterning step combined with hard mask liftoff effectively sets the resolution limit at 24 nm. A mixed mode SF_6/C_4F_8 reactive ion etch removes the unprotected silicon, defining our tips, connecting lines, and contact pads in silicon in (e). Then, 1:10 water:hydrofluoric acid is used to etch the exposed silicon dioxide layer to partially undercut the devices by several microns and leave the silicon tips suspended in (f). To shrink the emitter-to-collector gap, a dry oxide growth step is performed at 975 °C for 45 minutes to partially oxidize the silicon tips. As silicon is consumed, the formed oxide has a larger crystal spacing and so shrinks the gap size controllably from either direction, shown in (g). This is the critical step that allows the manufacture of a hybrid silicon/silicon dioxide scaffold with a much smaller emitter-to-collector gap as small as 7 nm. Finally, metal is deposited everywhere, using the undercut as a shadow mask to prevent shorting via the substrate, shown in (h). A representative example of a device fabricated in this manner is shown in Figure 3.10. The produced field emission devices were tested in the custom vacuum chamber with automatic probing, clean argon purging and a heated stage. The devices are heated in excess of 200 °C at a pressure of 5×10^{-6} Torr to facilitate desorption of water and adsorbed organic molecules. The devices are then probed automatically. Promising devices are subjected to repeated IV sweeps, a process which prior reports indicate promotes de-adsorption from the emitting surfaces (Zhu, 2004). For atmospheric operation the pressure is raised

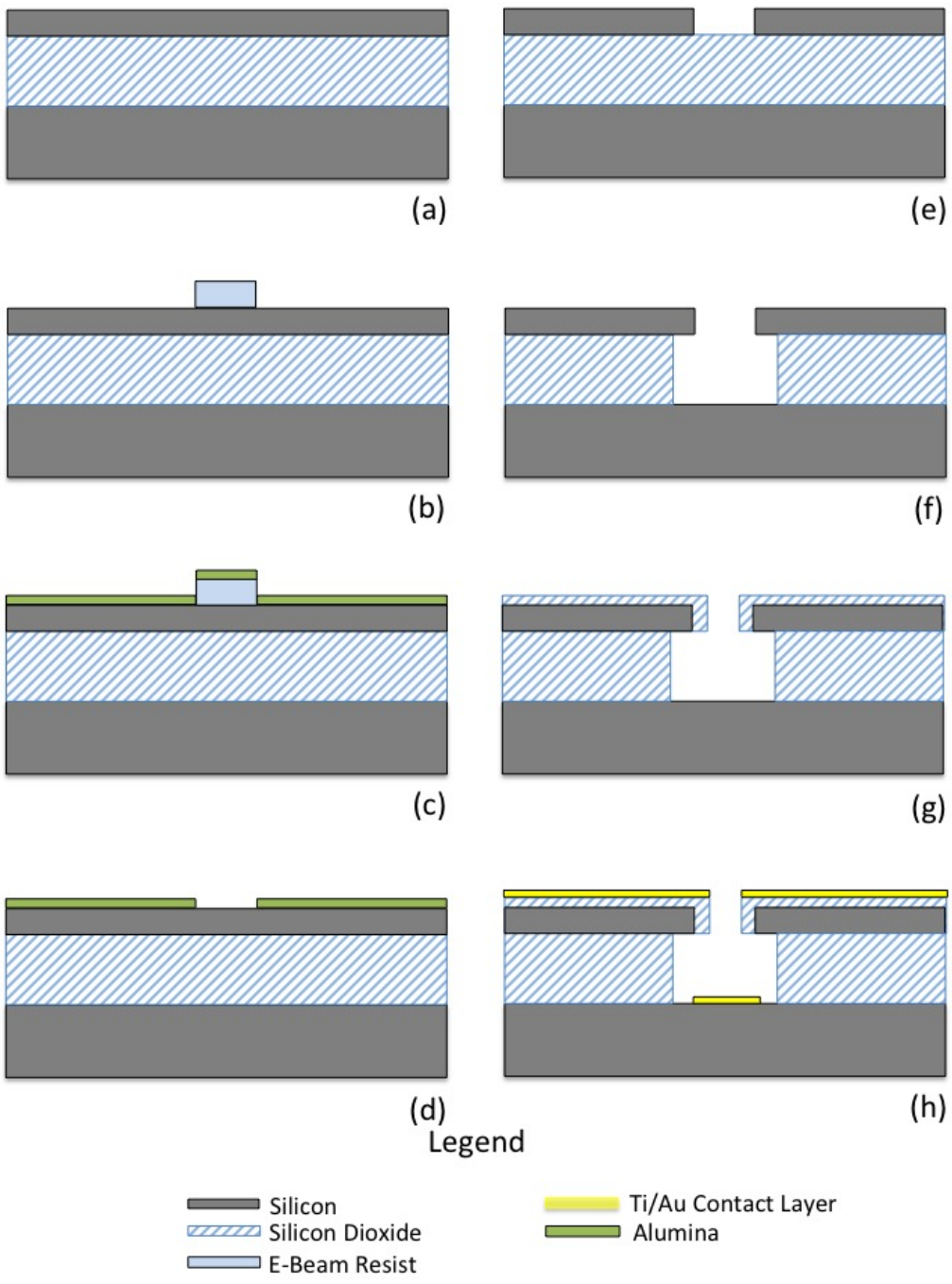

Figure 3.9: Diagram of the fabrication of field emitting diodes using oxide growth to create nanoscale gaps.

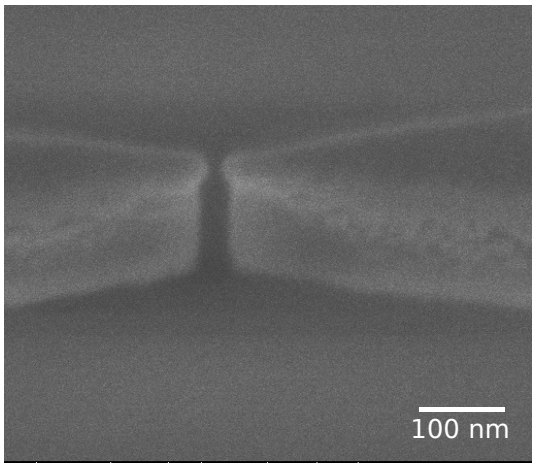

Figure 3.10: Fabricated field emitting diode composed of a gold layer on top of a hybrid silicon dioxide/silicon scaffolding shown here at a tilt of 30 degrees. The measured emitter-to-collector gap is 15 nm.

inside the chamber by backfilling with research grade argon gas. This prevents contamination of the device surface with water. High temperature testing operation occurs at pressures of approximately 5×10^{-6} Torr to prevent oxidation of emitter material.

Devices consisting of 25 nm of electron beam evaporated gold with a 5 nm titanium adhesion layer were deposited on a hybrid silicon dioxide/silicon scaffold and tested at different pressures. The results are shown in Figure 3.11. The devices displayed turn-on voltages in the sub-10 Volt range despite the high work function of gold. Low turn-ons are a critical component to atmospheric integration, as the emitted electrons won't have sufficient energy to ionize atoms in transit and cause ion bombardment of the tips. This is especially important for soft metals like gold which are interesting for their chemical inertness and plasmonic properties.

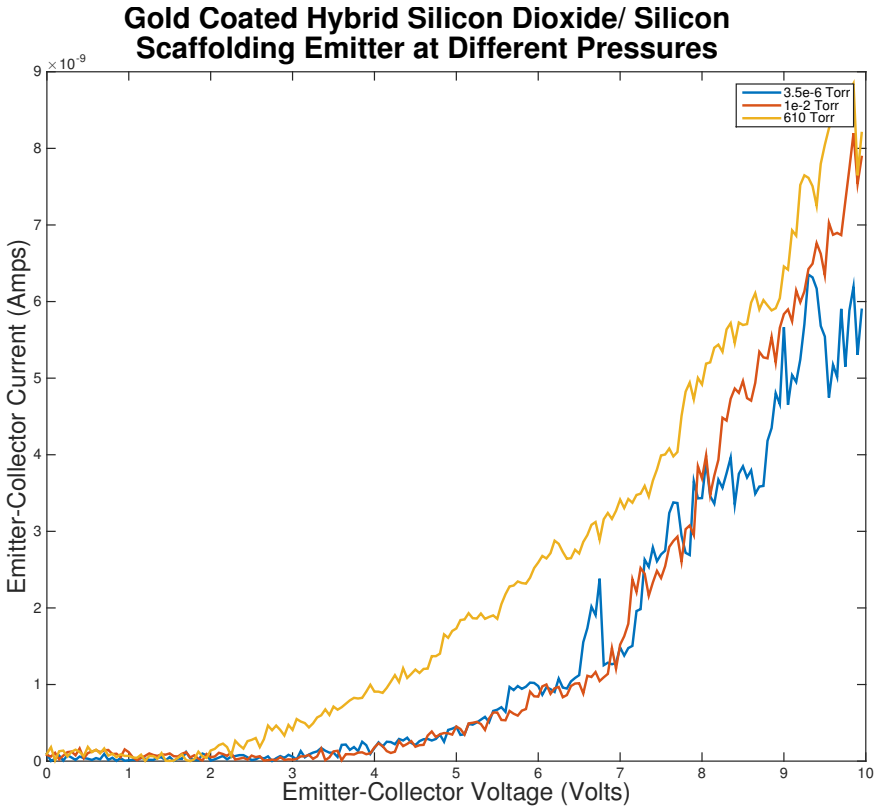

Figure 3.11: Current-voltage characteristics of a gold coated hybrid silicon dioxide/silicon scaffolding field emission device at different pressures.

3.5 Evaluation of the Feasibility of Gating in In-Plane Triode

Using the fabrication processes outlined above it is possible to produce four terminal devices similar to the geometries used in Pescini et al (Pescini et al., 2001) with dimensions as small as 7 nm. Such a device is shown in two views in Figures 3.12 and 3.13. Despite the precision of the fabrication process, a substantial challenge remained. Essentially, if emitter-to-collector gaps of 10-30 nm are necessary for sub 10-Volt operation, and if the radius of curvature of the emitter or collector tip was 25 nm (measured via scanning electron microscopy) the gate terminals, also with the same radius of curvature, cannot effectively change the field between the emitter and collector. This is illustrated via a 2D finite element model made using COMSOL Multiphysics. The modeled geometry is a simplification of the geometry demonstrated in Figure 3.12. This is shown in Figure 3.14. Each of the terminals is labeled and we have fixed the emitter-to-collector distance at 15 nm. The gate-to-gate distance is parameterized to vary between 100 nm and 160 nm. Each terminal has a fixed radius of curvature of 20 nm, which is the feature size obtainable following the

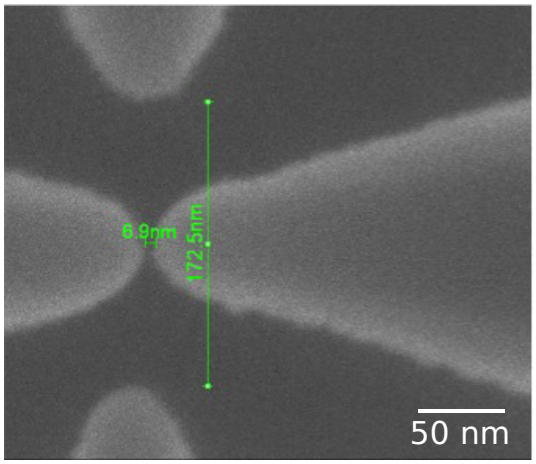

Figure 3.12: Fabricated field emitting triode composed of a tungsten layer on top of a hybrid silicon dioxide/silicon scaffolding.

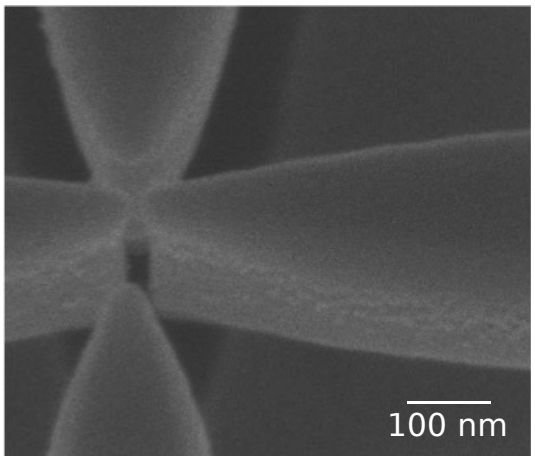

Figure 3.13: Fabricated field emitting triode composed of a tungsten layer on top of a hybrid silicon dioxide/silicon scaffolding shown here at a tilt of 30 degrees.

silicon dioxide/silicon hybrid scaffolding process as measured via SEM. The region between the two tips is separately bounded to allow for a finer mesh at the region of interest, as shown in an example mesh diagram in Figure 3.15. To simulate the electrostatic gating of field emission by the gate terminals, one begins by assigning a voltage of 1 V to the emitter surface, a voltage of 0 V to the collector surface. One then varies the voltage on the surface of each of the gate terminals. In this simulation, both gates are biased identically. From Figure 3.16 we see that the field values for 1 volt emitter bias are approximately 7×10^7 Volts/meter. This suggests that field emission should occur in the low tens of volts since all fields will scale linearly with voltage. To examine how effective gate biasing is in this geometry, we evaluate the maximum field on the emitter tip surface as a function of the gate-to-gate distance

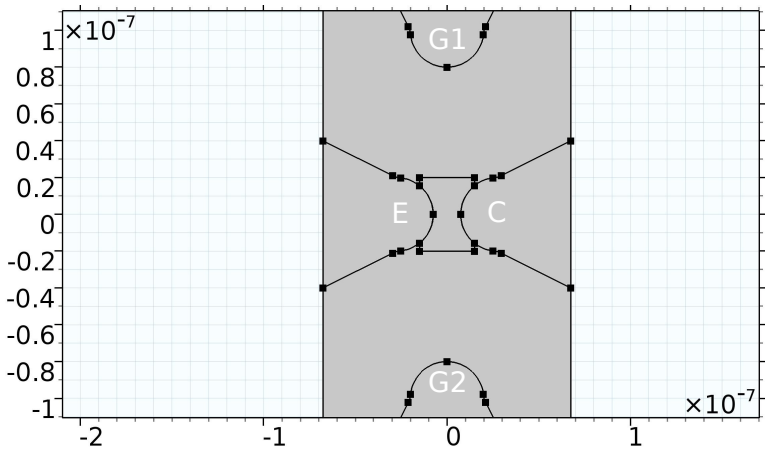

Figure 3.14: FEM simulation of in-plane triode fabricated using silicon dioxide/silicon hybrid scaffolding to achieve very small gaps.

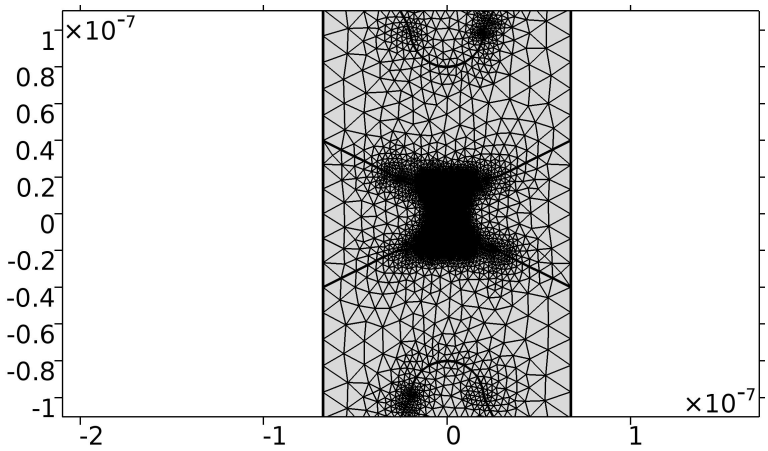

Figure 3.15: Meshing of FEM simulation of in-plane triode fabricated using silicon dioxide /silicon hybrid scaffolding to achieve very small gaps.

and the gate bias. This is shown in 3.16 . We evaluate how effective the gate is in changing the field on the surface of the emitter by examining the fraction change of the maximum electric field magnitude on the surface of the emitter at gate voltages from V_g = -V_e (in this case -1) to +V_e (in this case 1) relative to the maximum field magnitude on the emitter surface when the gate is biased at V_g = 0. We see that at the closest extent simulated (100 nm gate-to-gate distance), the gate is only able to change the maximum field norm on the emitter surface by 5% when V_g = ± V_e. This value implies very poor transconductance characteristics, since the maximum electric field due to the biases on the emitter and collector is at least twenty times the field due to the gate bias. Consistent with the finite element simulations, when these in-plane four terminal devices were tested there was no appreciable gating for

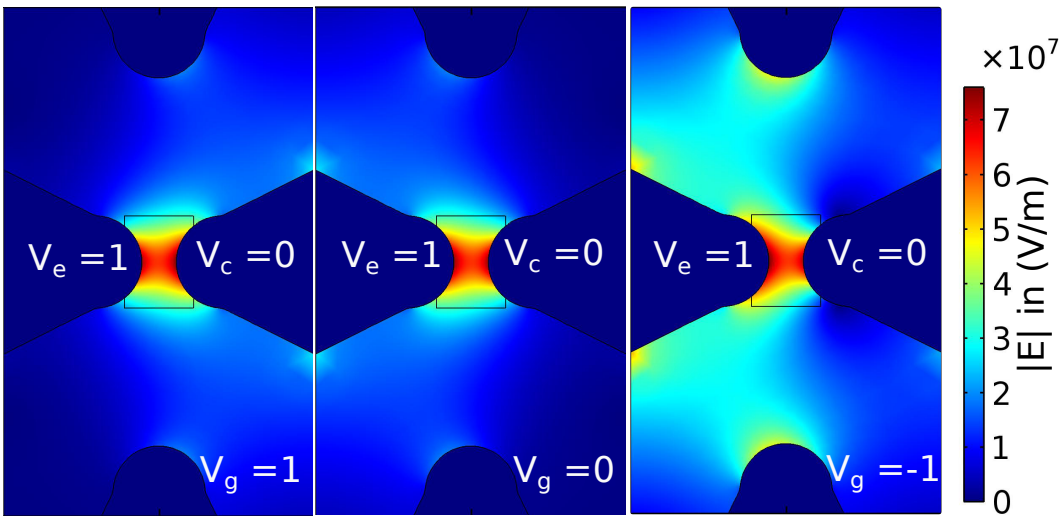

Figure 3.16: FEM simulation of |E| produced by biasing in-plane triode fabricated using silicon dioxide /silicon hybrid scaffolding.

gate biases below 100 V.

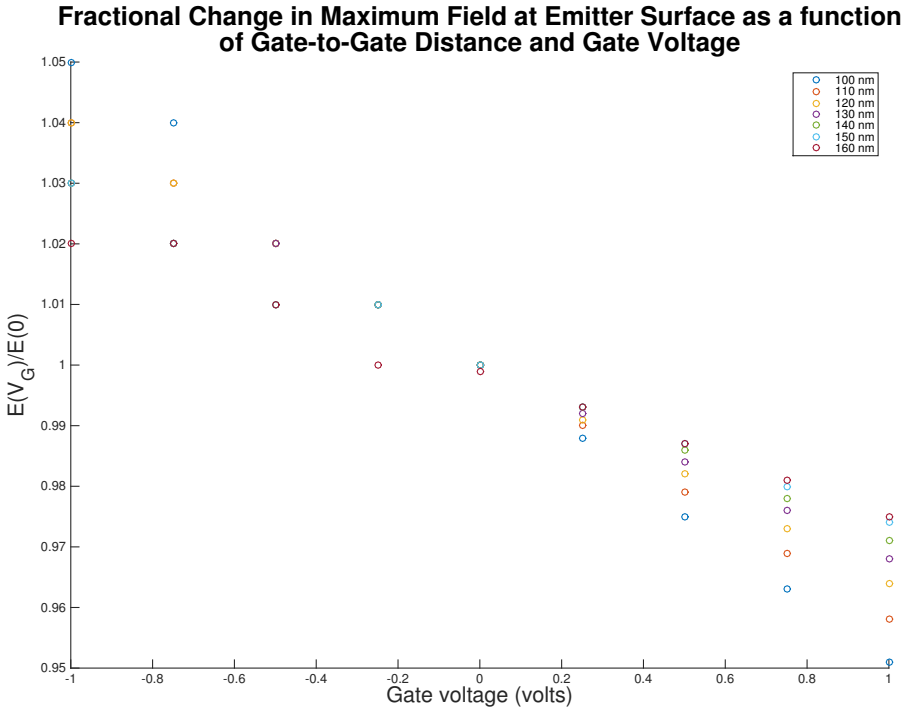

Figure 3.17: Results of FEM simulation showing the relative change of the maximum |E| on the emitter surface as a function of gate voltage relative to the maximum |E| when the gate is biased at 0 V. The date is displayed for different values of gate-to-gate distance.

3.6 Nanoelectromechanical Motion

During testing of the two and four terminal devices with very small emitter-to-collector distances several devices displayed very sharp on-off characteristics, transitioning from current at the noise floor (10^{-10} A) to current at the compliance limit of the measurement system (105 μA) in the span of 0.1 V. Noting that the devices were suspended with a distance of several microns from emitting tip to base of the silicon dioxide support, we considered the possibility that the extremely small emitter-to-collector gap devices could experience nanoelectromechanical motion. From literature reviews, it appears that the suspended small gap devices share similar dimensions and operating voltages to existing nanoelectromechanical switches (Loh and Espinosa, 2012) (Feng et al., 2010).

3.7 Conclusions

The difficulty involved in gating in-plane field emitters, combined with the possibility of nanoelectromechanical motion ultimately forced us to consider different avenues to realizing on chip, gated field emission devices.

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Jones, W Max, Daniil Lukin, and Axel Scherer (2016). "Ultra-low turn-on field emission devices characterized at atmospheric pressures and high temperatures". In: *Vacuum Nanoelectronics Conference (IVNC), 2016 29th International*. IEEE, pp. 1–2. DOI: 10.1109/IVNC.2016.7551459. URL: http://ieeexplore.ieee.org/document/7551459/.

Loh, Owen Y and Horacio D Espinosa (2012). "Nanoelectromechanical contact switches". In: *Nature nanotechnology* 7.5, pp. 283–295.

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Chapter 4

MULTILAYERED FIELD EMITTING DEVICES

Following our work with suspended nanoscale field emitters, which saw ambiguous results that we attributed to nanoelectromechanical motion of our suspended structures, we pursued a strategy that avoided the need to undercut our structures. Instead, electrodes were placed directly on insulating substrate and leakage currents were reduced by anisotropic reactive ion etching to increase the resistance of the leakage pathway. Noting the aforementioned difficulty of gating strictly in-plane device, we embarked on strategy to make multilayer devices. Using atomic layer deposition (ALD) technology, we made high quality gate oxides to isolate a thin metallic gate layer from a field emitting layer. This strategy was ultimately successful and much of the following section is an expanded version of work taken from publication in Applied Physics Letters (Jones, Lukin, and Scherer, 2017), in accordance with the policy of the publisher.

We focused on shrinking device dimensions below 200 nm to allow our field-emitting devices to operate at atmospheric pressure, since the mean free path of electrons at these pressures exceeds this distance (Driskill-Smith, Hasko, and Ahmed, 1997; Pescini et al., 2001). Field emitters can be made in SOI as shown by Han et al.and gated by applying a potential to the handle, but this design makes implementing multi-transistor circuits on a wafer difficult (Han, Sub Oh, and M. Meyyappan, 2012). We demonstrate a paradigm for CMOS compatible, low voltage, robust devices, which are operational at atmospheric pressures, and can be independently gated on a single integrated chip. We achieve the high fields necessary for field emission at low voltages by creating short emitter-collector gaps via electron beam lithography, as opposed to relying on atomic protrusions to create low voltage turn-ons as in Pescini et al. (Pescini et al., 2001). This strategy provides the reproducibility needed to make many robust devices on a single chip. Cold field emission involves the tunneling of electrons from a conductor into the vacuum under the presence of an intense surface electric field. The applied electric field bends the vacuum level outside of the conductor, causing the energy of the vacuum state to drop to the energy of the conduction electrons in the metal. This allows the electrons to tunnel to free space. The phenomenon is governed by a Fowler-Nordheim type equation (Fursey, 2007). For emission from a non-flat metallic surface, also from

Pescini:

$$
\begin{aligned}
I &= \lambda A a \frac{1}{\phi} E^2 \exp\left(\frac{-b\phi^{3/2}}{E}\right) \\
a &\approx 1.54 * 10^{-6} \frac{\text{Amps*eV}^2}{\text{V}} \\
b &\approx 6.83 * 10^9 (\text{eV})^{-3/2}\ \text{V/m}
\end{aligned}
$$

where A is the field emission area, $E = kV$ is the electric field at the point of emission for a voltage V, and λ is a factor that depends on the geometry of the emitter. The factor k is the static field enhancement and also depends on the device geometry. Designs including silicon oxide sharpening or atomic protrusions experience a higher field enhancement, which can partially compensate for larger emitter-collector gaps. To distinguish cold cathode field emission from other conduction mechanisms, current-voltage data is typically plotted in so-called Fowler-Nordheim coordinates, where the x-axis is plotted in units of $1/V$ and the y-axis in units of $\log(I/V^2)$. True cold cathode field emission should be linear in these coordinates (Chung and Yoon, 2003).

4.1 Fabrication of two-terminal field emitting devices

To demonstrate our design paradigm, we first fabricate two-terminal devices. As shown in Figure 4.1 (a), we begin with a silicon-on-insulator substrate (SOI, 220 nm Si/2000 nm SiO_2). The single-crystal silicon device layer is n-doped with phosphorus to a surface conductivity of approximately 5 kΩ using Desert Silicon P-260 spin-on dopant. We then spin coat a layer of diluted Microchem poly(methyl methacrylate) (PMMA) A2 950 and pattern this resist with 100 keV electron beam lithography, as shown in (b). We deposit 12 nm of Al_2O_3 over the silicon layer by electron beam evaporation and perform liftoff, shown in (c) and (d). Using the Al_2O_3 as a hardmask, the device and contact pads are etched into the silicon device layer, shown in (e). To etch the silicon layer we use a mixed-mode Bosch etch consisting of SF_6 as an etch gas and C_4F_8 as a passivation layer. Contact pads to each terminal are made using photolithography followed by a wet etch step in 5% tetramethylammonium hydroxide (TMAH) to remove the Al_2O_3 layer over the contacts (shown in (f)), followed by gold contact metal deposition and liftoff (shown in (g) and (h)). Shown in 4.2 is a scanning electron micrograph of a representative two-terminal field emission device.

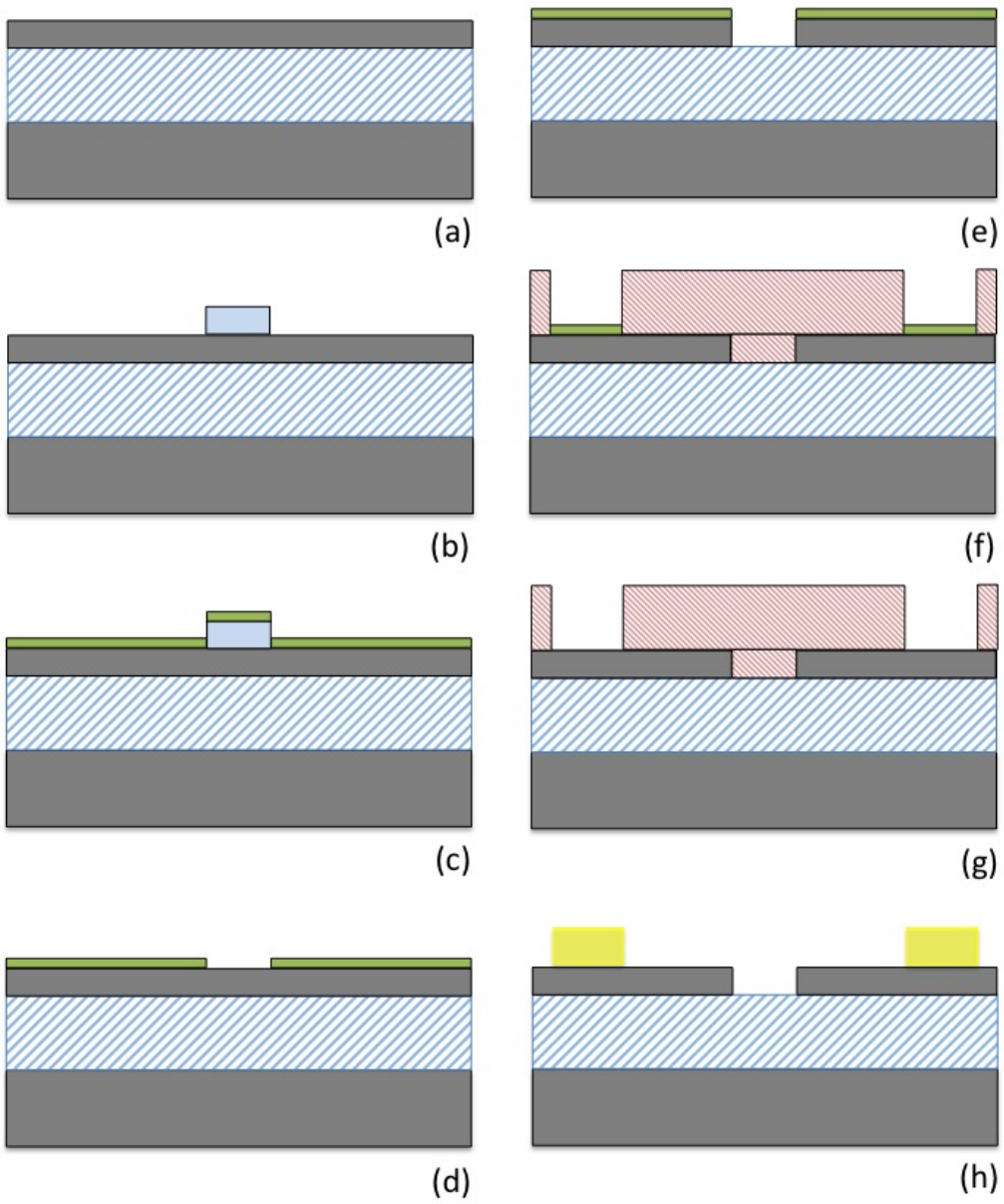


Figure 4.1: Fabrication diagram for field emission diode.

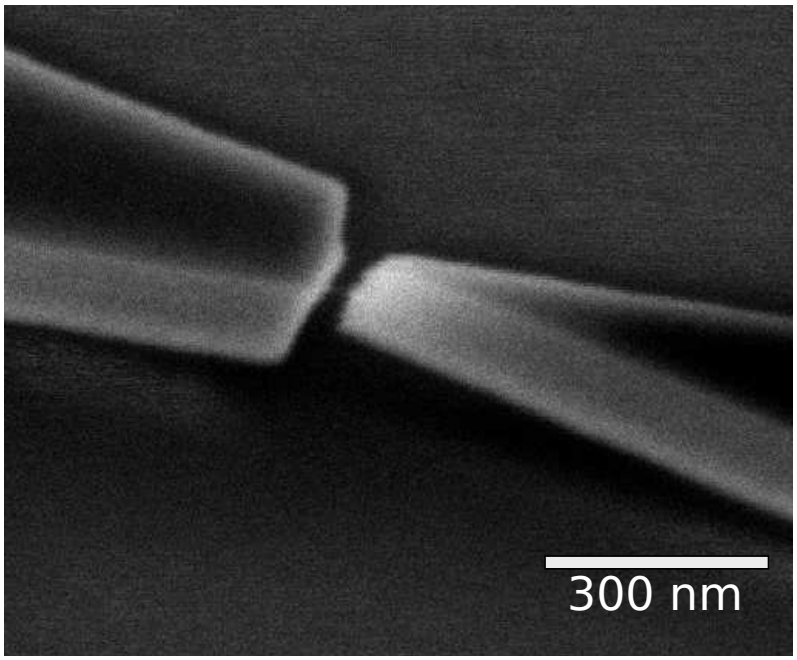


Figure 4.2: A representative diode fabricated by the indicated method.

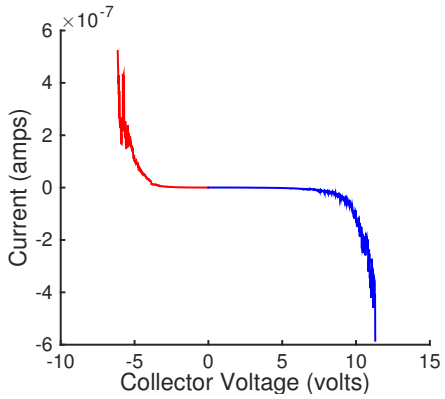
4.2 Measurement of two-terminal field emitting devices

Devices are pumped to a pressure of 10^{-5} Torr for several hours prior to testing to allow desorption of water and other contaminants from the emitting surfaces. The devices are then measured in-situ using a custom-built probe station. A heated stage and attached thermocouple allows the temperature of the devices during testing to be varied from near room temperature to over 500°C. To test the devices at different pressures, the chamber is backfilled with argon gas to a desired pressure.

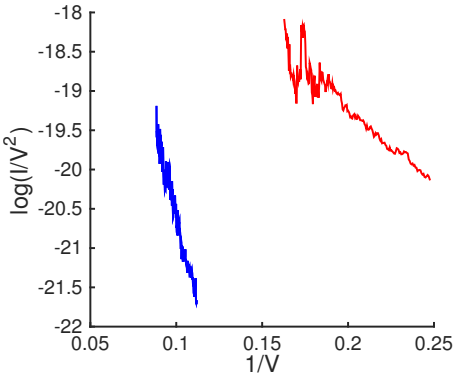
By designing the relative sharpness of each tip, as seen in 4.2, we can create an asymmetric current-voltage characteristic, shown in Figure 4.3a. When biased to emit electrons from the sharp tip (shown in the red portion of the graph and hereafter referred to as the forward direction), emission occurs at a lower voltage. This is because the sharp tip experiences greater static field enhancement than the dull tip. This asymmetric behavior for lateral devices is important for replicating the rectification behavior of existing solid-state diodes.

Figure 4.3b shows the current-voltage characteristic of the same device in Fowler-Nordheim coordinates, ignoring currents below 30 nA. We see from the linear nature of the plot that the currents above 30 nA are due to Fowler-Nordheim emission. The instability observed in the forward direction at higher voltages is likely caused by changes in the emitter, probably as a result of current-induced heating. We also performed time series operations of the two terminal device, shown in 4.4. Over the course of 1 hour while held at a constant potential the emitter produced a constant current of 250 nA in the forward direction with fluctuations of approximately 40%. Single tip field emitter current instabilities are often attributed to field induced atomic motion at the tip (Zhu, 2004). Lower current fluctuations can be achieved by adding more field emission tips at the cost of increased device capacitance (Temple et al., 1998).

We calculate the work function of the above device using a combination of measured current-voltage data, and COMSOL simulations derived from SEMS of the specific device. We can fit the plotted Fowler-Nordheim data to obtain a straight line with a slope equal to $\frac{-b\phi^{3/2}}{k}$, where$k$ is the static field enhancement relating the applied voltage to the generated surface field $E = k \times V$. We obtain device dimensions from scanning electron micrographs of each specific device and build 2D COMSOL simulations to estimate the static field enhancement factor, k. In COMSOL we build a electrostatic model of the same device using the overview SEM shown in Figure 4.5. For this particular device, we see that the blunt collector has a minor



(a) Assymetric current voltage characteristic of field emitting diode.



(b) Fowler-Nordheim plot of same diode demonstrating the presence of field emission.

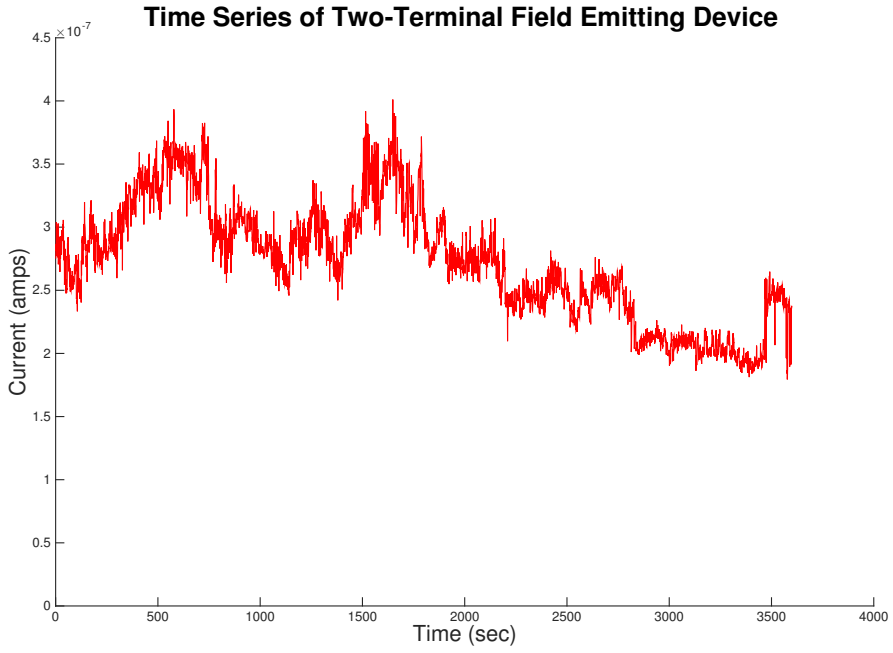


Figure 4.4: Time series of emission current from a two-terminal device in the forward direction. The emitter- collector voltage was -5.0 volts. The plateau behavior of the time sweep is characteristic of single tip field emission.

protrusion that reduces field enhancement experienced by the emitting tip. We build a comparable geometry in COMSOL, a FEM software, as shown in Figure 4.6(a). The box region between the emitter and collector allows us to highly mesh this middle region as shown in (b). We simulate the field profile for the x-component of the electric field under the condition that there is a 1 volt potential difference between the emitting terminal and the collecting terminal. This is the component

along the emission direction. Finally in (d) we have have plotted the derivative of the voltage with respect to x along a cut line through the center of the emitter tip. This is equivalent to the electric field in the x-direction. The red line in (d) represents the expected field for the given bias in the case of two capacitor plates spaced the same distance from each other as the emitter and collector. From these simulations we calculate the static field enhancement to be $k = 5.69 \times 10^7$ 1/m in the forward direction and $k = 4.376 \times 10^7$ 1/m in the reverse direction. Using MATLAB, we fit the slope of the FN devices as $s = -19.302$ in the forward direction and $s = -91.713$ in the reverse direction. From this we can attempt to calculate a work function for the emitting material as $\phi = 0.2957$ in the forward direction and $\phi = 0.7015$ in the reverse direction. The accepted value for the work function of bulk silicon is 4.05 eV (S.M. Sze, 2007), but strong phosphorus doping can produce work functions as low as 2 eV (Plekhanov and Tan, 2000), and finally the presence of adsorbed molecules at the emission site can change the work function even further. The large discrepancy between our extracted work function and literature is probably due to uncertainty about the exact geometry of the emitting area combined with the presence of adsorbates. Even in a scanning electron microscope, it may not be possible to image the emitting tip well enough to accurately model its static field enhancement. Furthermore, strongly adsorbed surface molecules may modify the local work function further making this type of analysis difficult.

Single tip field emission devices are particularly susceptible to surface contamination and tip destruction. Surface adsorbates can alter the local work function upon which the current exponentially depends (Delchar and Ehrlich, 1965). Additionally, the emitted current can ionize atoms that can then collide with the tip, blunting or destroying the devices. By shrinking the emitter-collector gap, we reduce the need to have a sharp tip to produce low voltage emission. This minimizes the effect of surface changes, either by contamination or by ion impact. Additionally, by operating at potentials lower than 12 volts, emitted electrons don't have sufficient energy to ionize common gas species (Wong and Ingram, 1993), which further reduces tip degradation.

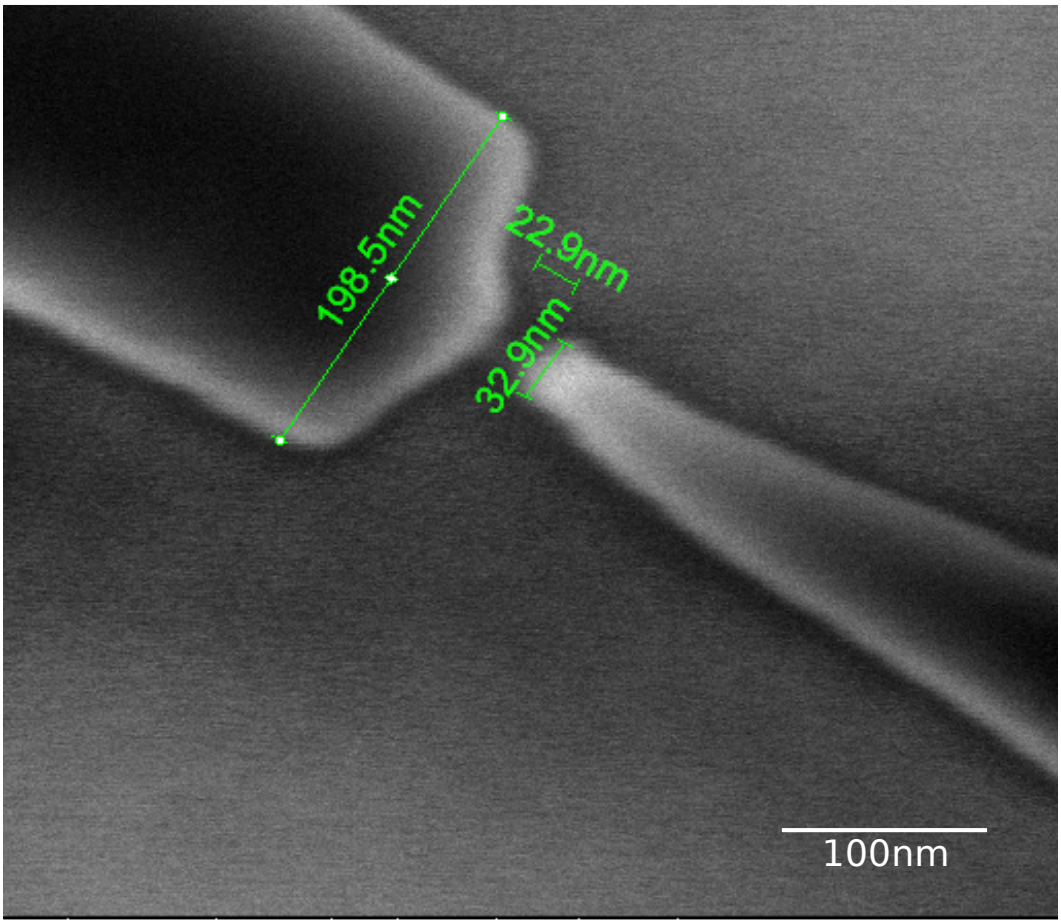


Figure 4.5: Overview SEM of field emitting diode used as the basis for 2D simulation of field emission characteristics.

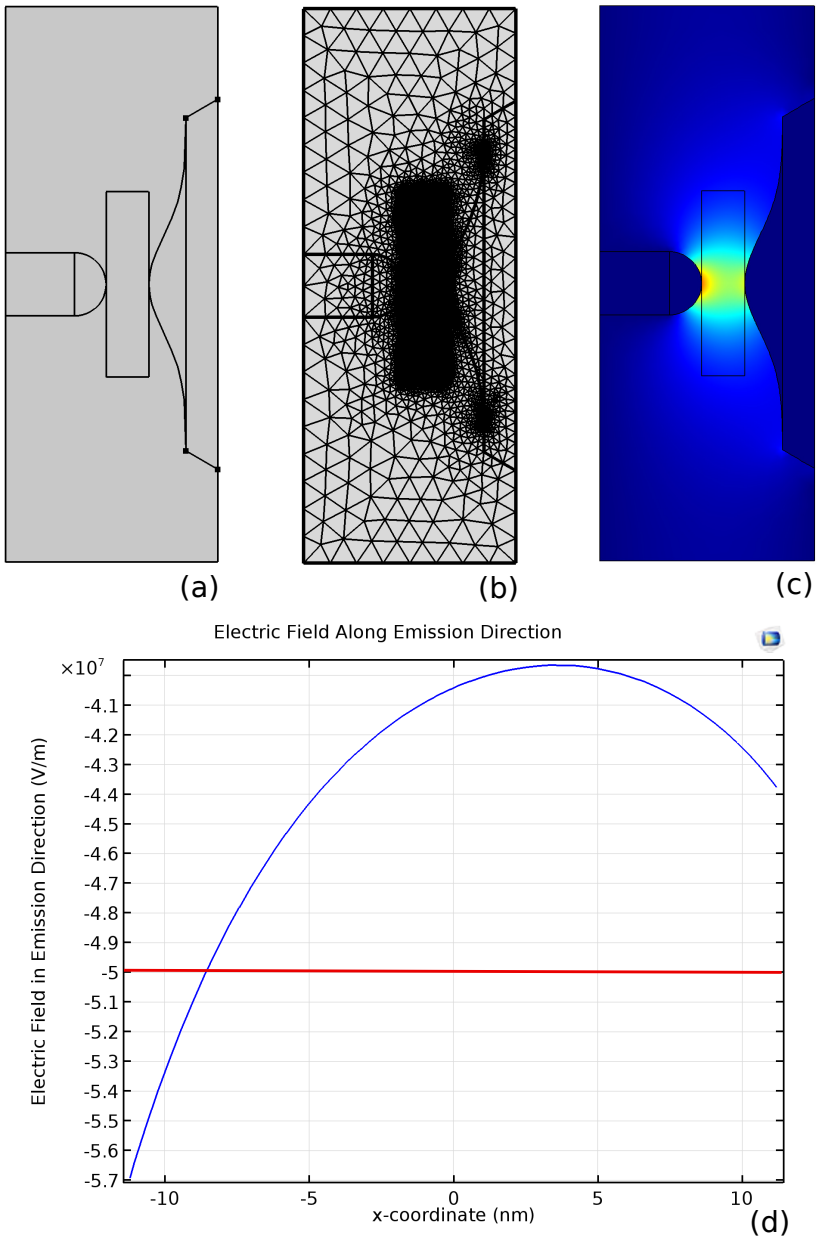


Figure 4.6: 2D FEM simulation of field emitting diode. In (a) we have the modeled geometry. In (b) we show the simulated mesh. In (c) we show the field profile for the x-component of the electric field. In (d) we show the x-component of the electric field along a cut line connecting the tip of the emitter to the tip of the collector.

4.3 Gated multi-layer field emission devices

Following our work with two-terminal devices, we extended our geometry to produce a multi-layer gated three-terminal device. This was done by combining the layered approach of Srisonphan et al. (Srisonphan, Jung, and Kim, 2012) with the design of our two-terminal devices as shown in Figure 4.7. As with the diode case, the bottom layer consists of a doped silicon emitter and collector. A high quality dielectric Al_2O_3 layer, deposited by atomic layer deposition (ALD), separates the silicon layer from a metallic gate layer. Application of a bias voltage to the gate layer modifies the field at the emitter tip, modulating the current between the emitter and collector. By combining a high work function gate material with a high dielectric strength oxide, one can limit the leakage current either through field emission from the gate or from oxide leakage. For this study, chrome with a work function of 4.5 eV16 was used as the gate material to facilitate fabrication since it is compatible with later etching processes. A critical improvement in this design over the use of backplane gating is that these devices can be gated separately, a necessity for the integration of many devices on a single wafer.

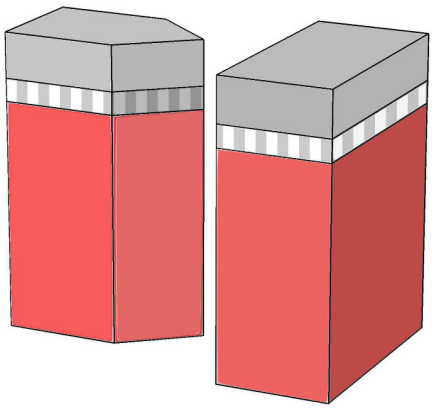


Figure 4.7: Diagram of the respective layers of gated field emission device. The red layer is a doped silicon layer, the striped gray layer is an ALD Al_2O_3, and the gray layer is a chromium layer that serves as the gate.

To fabricate the gated field emission device, we begin with the same SOI substrate (220 nm/2000 nm) as was used for the two-terminal devices, as shown in Figure 4.8 (a). The device layer is again doped with phosphorus via spin-on dopant. A 20 nm layer of Al_2O_3 is deposited via ALD, shown in (b). We perform electron beam lithography, using Microchem PMMA A2 950 with an additional anti-charging layer (Mitsubishi Rayon Aquasave 53za). Following development, we sequentially

deposit 5 nm ofAl_2O_3, 30 nm of chromium, and finally 40 nm of Al_2O_3 all using electron beam evaporation and perform a liftoff of this layered stack shown in (c) and (d). Using the top layer of Al_2O_3 as a hardmask, we etch through the ALD Al2O3 layer using a Cl_2, CH_4, H_2 plasma etch. We then etch through the silicon device layer using a mixed-mode Bosch etch, as shown in (e). This process aligns the chromium gate layer with the silicon layer without a second lithography step. Finally, we use successive photolithography steps followed by wet chemical etching to create vias through the mask to electrically contact the chromium gate layer on either side of the emitter-collector gap and to the silicon device layers serving as the emitter and collector, shown in (f) and (g). Etching through the ALD Al_2O_3 layer requires a thicker hardmask, and reduces the minimum achievable emitter to collector gap to approximately 60 nm. A representative fabricated device is shown in

The current-voltage characterization of the field-emission triode is shown in Figure 4.10. The chromium layer over the blunt collector is referred to as gate 1. As the voltage on gate 1 is decreased, the electric field at the emitter tip is reduced in turn, reducing the Fowler-Nordheim current. The emitter emits electrons into both the collector and the gate, with a ratio of approximately 1.75:1. The second gate over the emitter is partially etched during fabrication, and so is ineffective at gating field emission. It is expected that the emitter-side gate could serve as a suppressor for field emission current by depleting the doped silicon emitter of free charges. Increasing the thickness of the ALD Al_2O_3 layer could further reduce gate leakage by reducing the possibility of pin-holes as well as reducing the likelihood that emitted electrons would travel to the gate rather than the emitter.

In Figure 4.11, we show a plot of the currents in Fowler-Nordheim coordinates, for currents greater than 50 nA. The y-intercept of each Fowler-Nordheim line increases in magnitude with gate voltage. This corresponds to either an increasing emission area at high gate voltages or a decrease in work function, or both (Forbes, 1999). The slope of the Fowler-Nordheim line is dependent on the work function of the emission site. We perform a second set of 2D COMSOL simulations to obtain an estimate of the field enhancement factor $k = 3.22 \times 10^7$ (where we remind the reader that $E = kV$. Using this value and the slope of each Fowler-Nordheim line we estimate the work function of the emitting material, shown in table 4.1. As gate voltage increases, the absolute value of the slope of the Fowler-Nordheim line increases, corresponding to a decrease in the calculated work function of the emitter

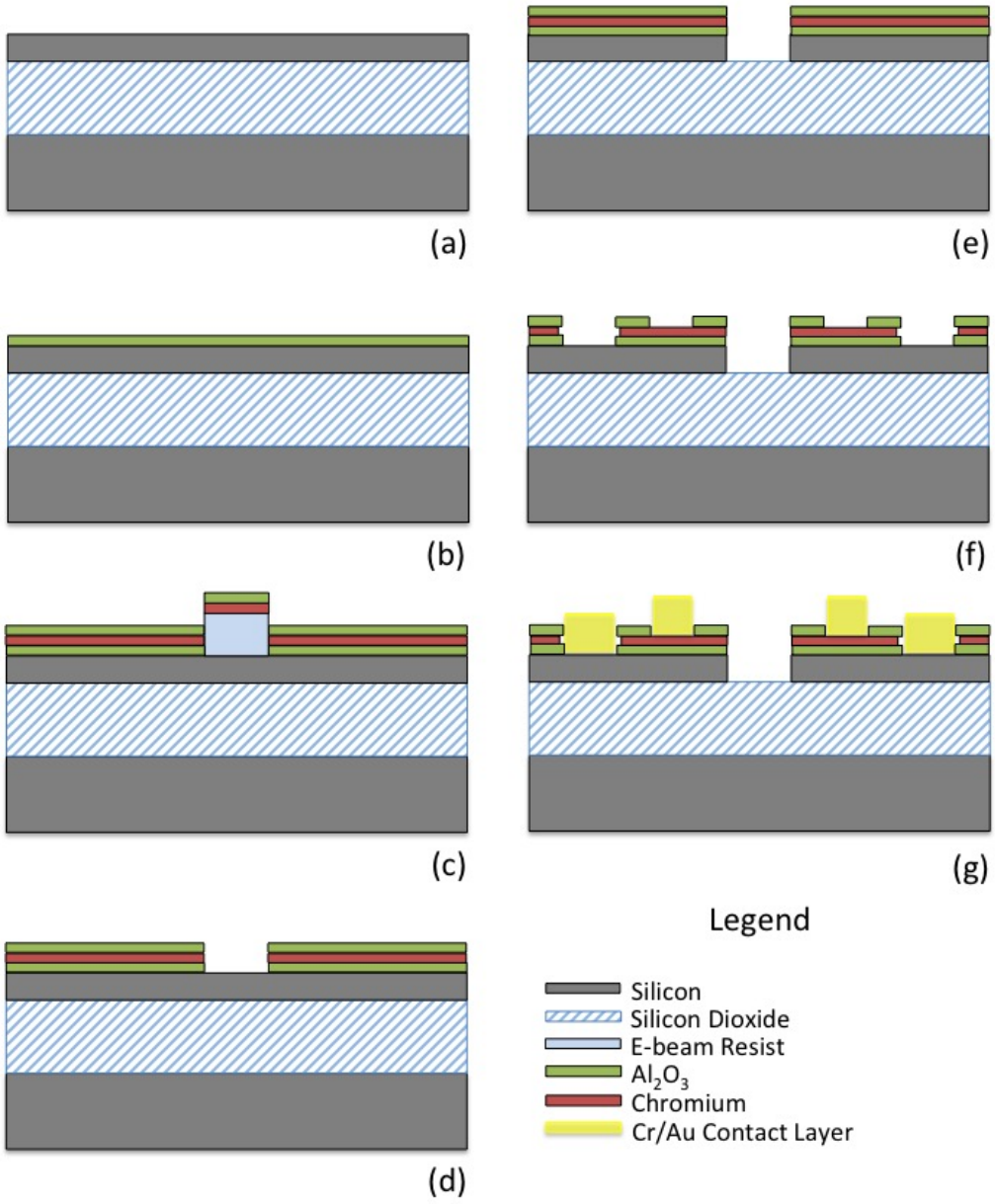


Figure 4.8: Fabrication diagram for field emission Triode.

towards a limiting value. Again, we attribute the large discrepancy between our extracted work function and literature is probably due to uncertainty about the exact geometry of the emitting area combined with the presence of adsorbates.

The operation of field emitting devices at different pressures is an important metric

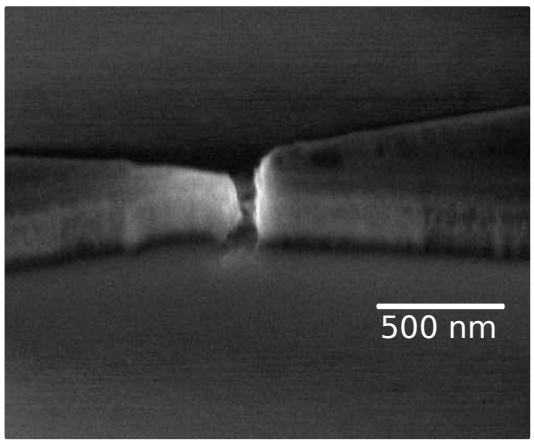


Figure 4.9: Scanning electron micrograph of fabricated gated field emission device.

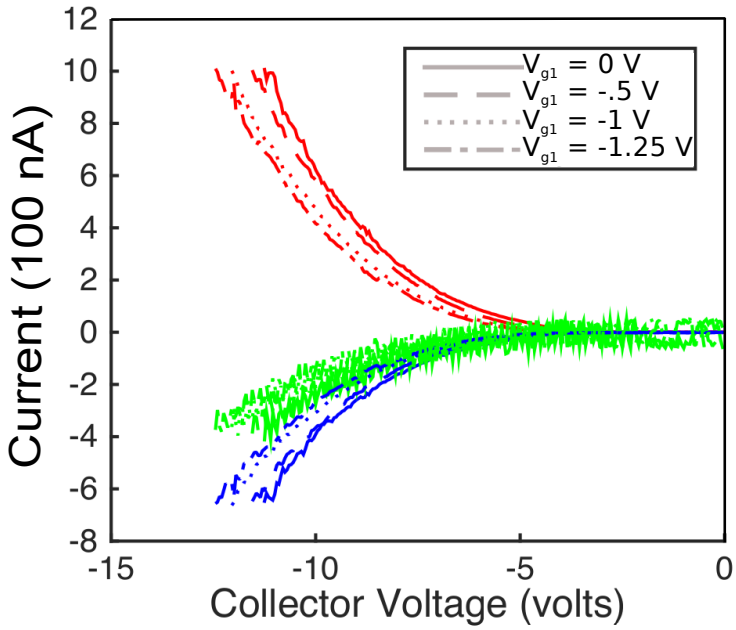


Figure 4.10: The current-voltage characteristic for the three-terminal field emission device. The red portion is the emitter current, the blue portion is the collector current, and the green portion is the gate leakage current.

for future packaging and practical use. In Figure 4.12 we plot the current-voltage characteristics of a three-terminal field-emitting device with fixed gate voltages at different pressures. We determine the pressure dependence by backfilling our testing chamber with 99.99% pure argon gas and controlling the chip temperature via a heater and thermocouple to 110°C ± 10°C. The device was stabilized at each pressure for 5-10 minutes before the measurement was taken. As expected, even as the pressure is increased by several orders of magnitude, there is no systematic

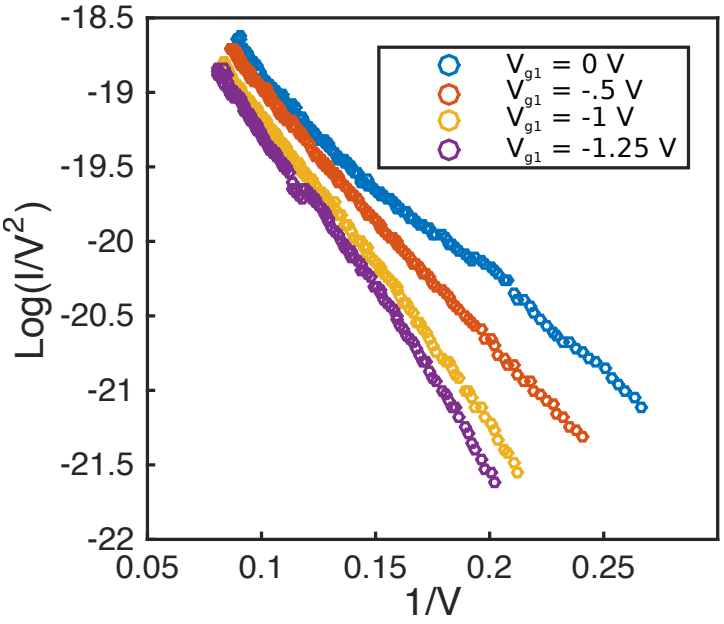


Figure 4.11: The three-terminal Fowler-Nordheim characteristic, plotted for currents greater than 50 nA, confirms that the gate modifies field emission

Gate Voltage	Slope of FN Line	Calculated ϕ
0	-13.32	.1580
.25	-18.26	.1950
.5	-17.04	.1862
.75	-18.54	.1970
1	-20.35	.2096
1.25	-21.74	.2190

Table 4.1: Table of calculated FN slope data and work functions.

change to the current voltage characteristic greater than the change expected of a single emitter in the same amount of time, as indicated by our earlier time series measurements.

In this section, we have demonstrated practical field emission devices that operate below 10 volts and that are CMOS compatible. Our devices represent a promising start toward matching the performance of existing solid-state devices and integrated circuits in terms of current and turn-on voltages. Current CMOS devices operate at in the sub 5-volt regime and switch milliamps of current. By choosing low work function materials, such as tungsten or very highly doped silicon (Plekhanov and Tan, 2000), and by using thicker emitting layers that can sustain higher current it is

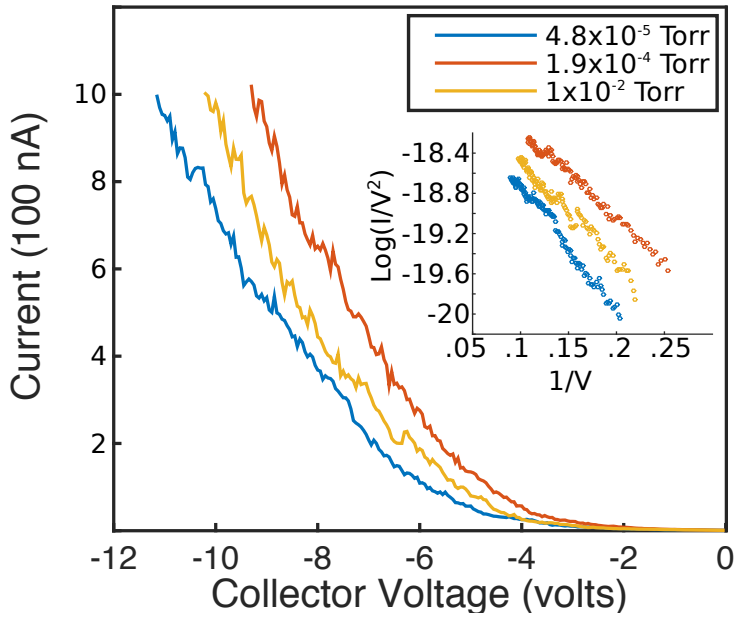


Figure 4.12: The current-voltage characteristic of a three-terminal field-emitting device with fixed gate voltages plotted at different pressures of argon gas.

possible that nanoscale field emitting devices can achieve these operating conditions.

4.4 High temperature testing of multi-layer device

Following demonstration of successful gating in the multilayer field emitting devices, the next goal was to demonstrate operation at high temperatures. Unfortunately, as the temperature was increased from 25 °C to 100 °C, exponential Fowler-Nordheim current was accompanied by a second resistive current that decreased in resistance as the temperature increased. The effect was reversible; the device was restored to normal operation if the temperature was lowered. This is likely the result of a decrease in the resistance of the surface leakage pathway as temperature increases. One strategy to combat this is to increase the length (and therefore the resistance) of the parasitic leakage pathway via deep anisotropic etching. This strategy builds on the experience described in the third chapter of this thesis wherein devices that were dramatically undercut could experience anomalous nanoelectromechanical effects. By not significantly undercutting the electrodes, nanoelectromechanical effects can be mitigated.

To demonstrate this strategy, an asymmetric two terminal device was fabricated, similar to the devices under consideration in earlier sections of this chapter. After etching the doped silicon layer and before deposition of contact pads, a C_4F_8/O_2 ICP/RIE etch was used to continue the anisotropic etch into the silicon dioxide layer underneath. The selectivity for the C_4F_8/O_2 etch between the alumina hard mask and the silicon dioxide layer to be etched was low and so only an additional 250 nm of silicon dioxide could be etched before the silicon tip began to erode. A representative field emitting diode is shown in Figure 4.13. One can see the erosion of the Al_2O_3 layer (bright uppermost layer) near the tip. This tip erosion sets a limit on the amount of undercut possible. Deeper etching necessitates a thicker mask which limits the resolution of the emitter-to-collector gap. The current-voltage characteristic of a device undercut by 250nm is shown in Figure 4.14. The resistive, parasitic pathway becomes less resistive at higher temperatures, eventually making diode-like operation impossible at temperatures above 350 C. Examining the current-voltage data plotted Fowler-Nordheim coordinates in Figure 4.15 makes this even clearer. As temperature rises, the contribution to the current from parasitic leakage is greater and Fowler-Nordheim behavior doesn't dominate until higher voltages.

One can imagine decreasing the emitter-to-collector leakage by increasing the length of the emitter-to-collector leakage pathway by etching even deeper into the substrate. This would necessitate clever materials selection and improved fabrication techniques to avoid top erosion but is not inconceivable. Unfortunately, in a multilayer

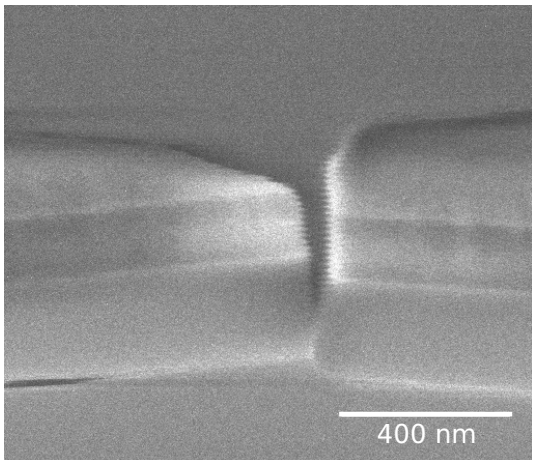


Figure 4.13: High temperature field emitting device manufactured by anisotropically etching silicon dioxide layer underneath the device.

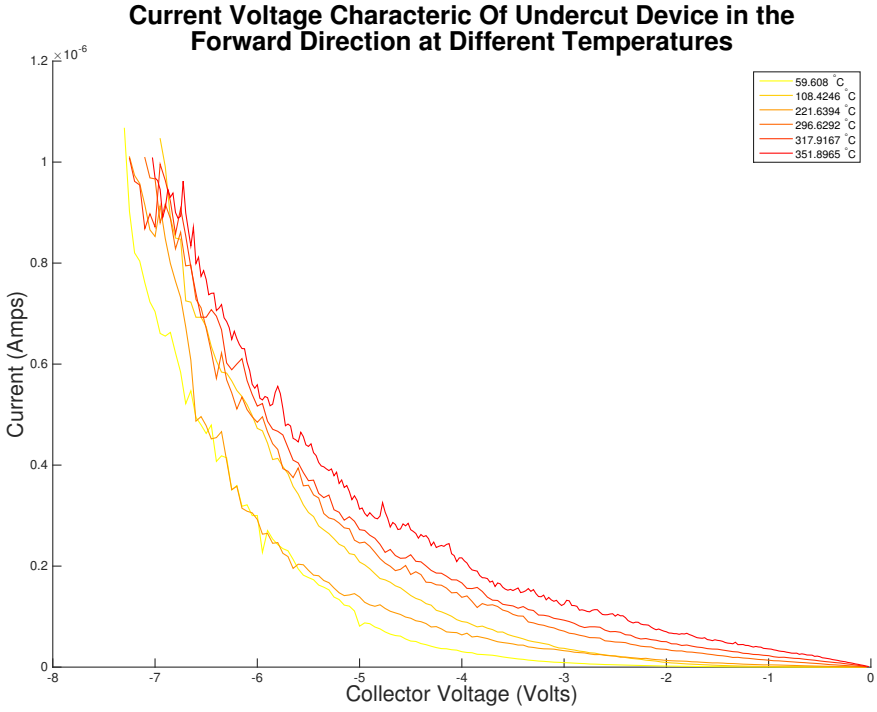


Figure 4.14: Current-voltage characteristic of field emitting diode with 250nm anisotropically etched silicon dioxide layer.

field emitting device like those in the previous section, the gate oxide presents a pathway where leakage current and the possibility of failure will always increase with temperature. Therefore, a new paradigm is needed to build gated, high temperature field emission devices.

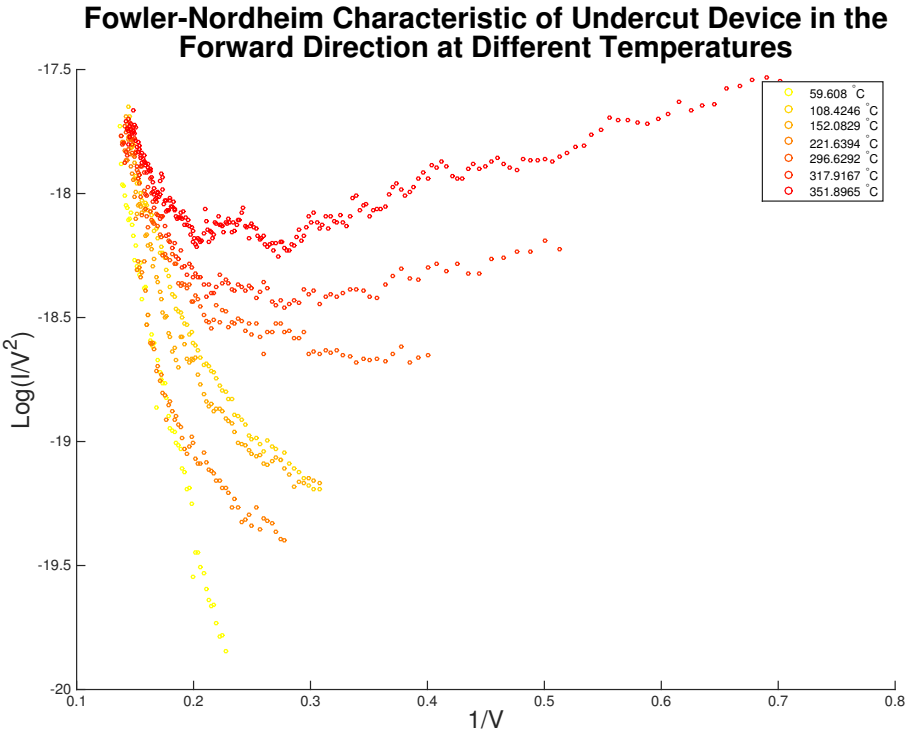


Figure 4.15: Fowler-Nordheim characteristic of field emitting diode with 250nm anisotropically etched silicon dioxide layer.

4.5 Preliminary work on three-dimensional field emission devices for radiation hard, high temperature transistors

As discussed in the introduction, one promising avenue for immediate implementation of field emission devices is for implementing circuits in extreme environments that feature high levels of radiation and/or high temperatures, and currently pose a significant challenge to circuit designers. Traditional CMOS devices are susceptible to radiation damage through a number of avenues: ionizing radiation can produce anomalous carriers in the depletion region of semiconductor transistors and photodiodes, causing temporary upsets; heavy particle radiation can produce lattice displacements and decrease minority carrier lifetimes in bipolar junction transistors; heavy particle radiation may also damage sensitive gate oxides, permanently destroying MOSFET devices (Radiation Effects Group at Nasa JPL, n.d.). Many of the effects only become more dramatic as device dimensions are shrunk, which imperils the ability of space missions to use the latest CMOS node.

Electronics used on space based missions Low earth orbit spacecraft experience low levels of radiation 20 krad(Si) over long time periods. Interplanetary missions

can experience high levels of radiation from solar flares and from intense trapped radiation belts around other planets (Radiation Effects Group at Nasa JPL, n.d.). These sources of radiation impact mission success. For example, the solid-state recorder on the Cassini-Huygens mission to Saturn experienced an anomalous surge of multiple bit error rates due to a solar flare event (Swift and Guertin, 2000). Shielding for these issues is possible but only with a concomitant increase in launch weight. In the case of Cassini, for instance, a half-inch aluminum shield was used to protect the solid-state recorders, though the device still experienced upsets

Demonstrations of radiation-hard field emission devices surviving high radiation are numerous, most recently a silicon on insulator field emission transistor showed uncompromised operation after exposure to 100 krad radiation (Han, Moon, and M Meyyappan, 2017). The fundamental device physics of field emission transistors that directly modulate the field on the emitter surface are insensitive to many radiation effects; they are not minority carrier devices and are routinely manufactured from amorphous metals so defects induced by heavy ion radiation will not significantly diminish device operation. Indeed, even the threat to the gate oxide can be eliminated using side or wrap-around gates that are vacuum separated from the emitter and collector

The multilayer devices demonstrated so far in this chapter are not ideal candidates for high temperature and radiation hard operation. Surface leakage currents across the gate oxide layer and across the surface of the oxide between the emitter and collector terminals will increase with temperature. Breakdown of the dielectric gate oxide also becomes more likely at higher temperatures. Finally, the gate oxide will likely suffer from the same issues that the oxide separating the emitter and collector electrodes. An avenue for achieving high temperature and radiation hard environments is to continue the strategy described in the previous section by using nanoscale anisotropic etching to increase the surface leakage pathway. This can be readily done in silicon nitride, which can be etched using a standard mixed mode C_4F_8/SF_6 etch. To remove the possibility of temperature or heavy ion radiation induced breakdown of the gate oxide, the gate must be isolated from both the emitter and the collector by vacuum. The earlier work on in-plane field emission devices indicates that a completely in-plane geometry won't provide adequate gating at these dimensions. Instead, one can remake the multi-layer design by using a wrap-around gate, separated by vacuum from the emitter and collector.

A proposed fabrication design is shown in Figure 4.16. The starting substrate is either

single crystal sapphire or silicon dioxide on silicon. Tungsten in sputter deposited onto the substrate in (b). Sputter deposition takes place in an argon atmosphere at 7 mTorr and with RF power of 200 Watts. Following sputter deposition, electron beam lithography is performed to define a the emitter, the collector, and the two gate supports. Alumina is electron beam deposited onto the patterned substrate and lifted off in hot Remover PG, as seen in (c). The alumina pattern, as seen from above is shown in figure 4.17, has a narrow emitter separated from a broad collector and two gate supports on either side of the collector. The cross-section in figure 4.16 is specifically the cross-section intersecting the gate supports and the collector. The alumina pattern is transferred into the tungsten and silicon nitride by a mixed mode C_4F_8/SF_6 etch (as shown in (d)). The alumina hard mask is removed with a wet etch in 5% Tetramethylammonium Hydroxide (TMAH) afterwards. An aligned electron beam lithography step is performed to mask everything but the region encompassing the gate-collector-gate region. Electron beam evaporated silicon dioxide is deposited at a steep angle onto the patterned substrate and lifted off to make a silicon dioxide bridge between the two gate terminals and across the collector as shown in (e) and (f). The silicon dioxide will be removed as the final step so the thickness of deposited silicon dioxide will determine the thickness of the vacuum layer. A third aligned electron beam lithography step is performed to mask everything but the gates and the bridged region. Electron beam evaporated tungsten is deposited at normal incidence onto the patterned substrate and lifted off in hot Remover PG as shown in (g). This creates a tungsten bridge to act as a gate connected to the gate supports and separated from the collector by the silicon dioxide layer. Finally the silicon dioxide is removed in vapor phase HF acid, leaving only a vacuum gap between the tungsten bridge gate as shown in (h). Preliminary work in this direction has already been done to demonstrate the ability to etch nanoscale gaps in stacks of sputtered tungsten on silicon nitride, as shown in Figure 4.18. The gap between the gate supports and the collector is 30 nm, the tungsten layer thickness is 200 nm and the silicon nitride layer thickness is also 200 nm. This work will be continued by myself as a post-doctoral scholar at the Jet Propulsion Laboratory in collaboration with the Axel Scherer Group.

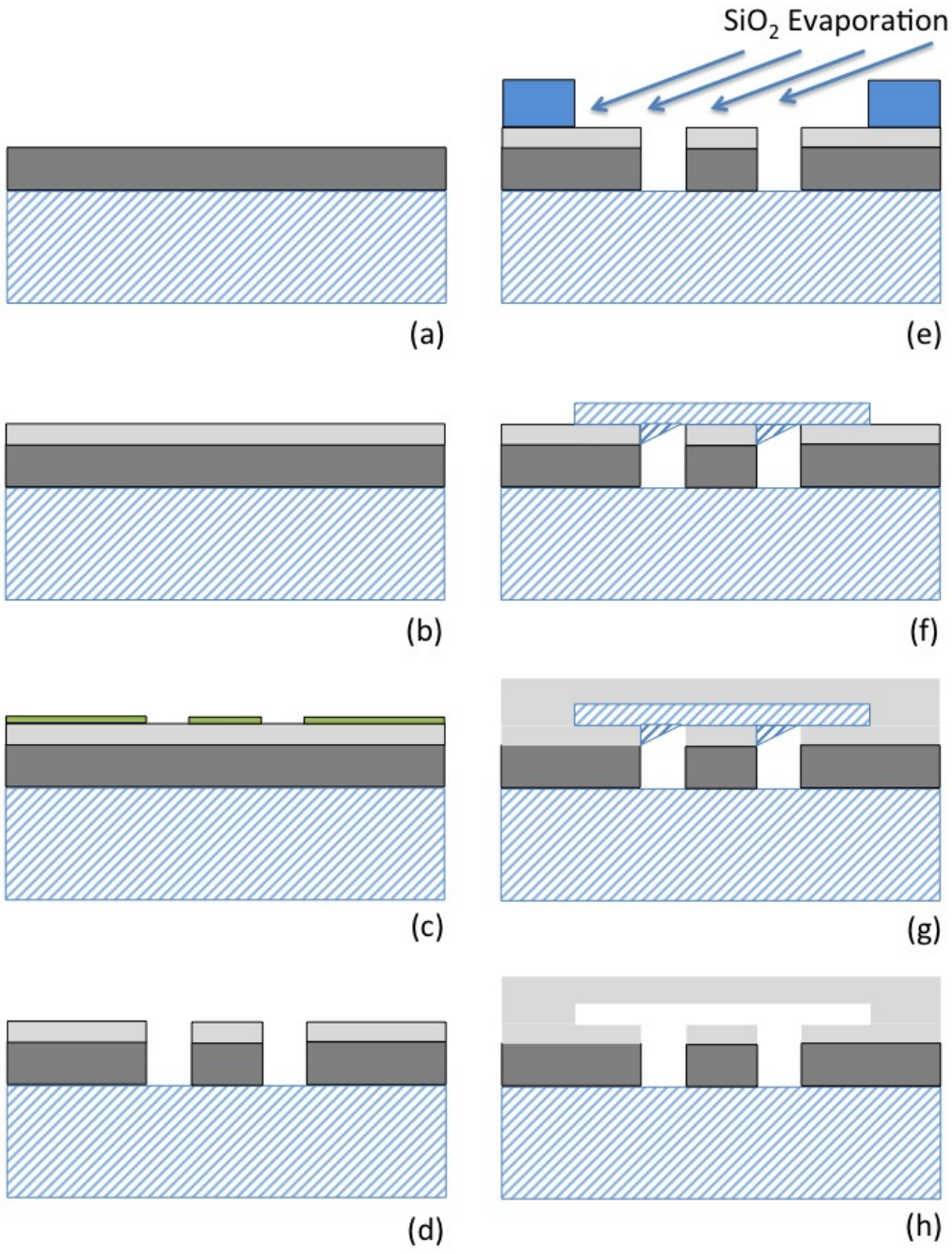


Figure 4.16: Fabrication procedure for tungsten high temperature triode. All terminals are separated from each other by vacuum gaps and long vertical silicon nitride pillars.

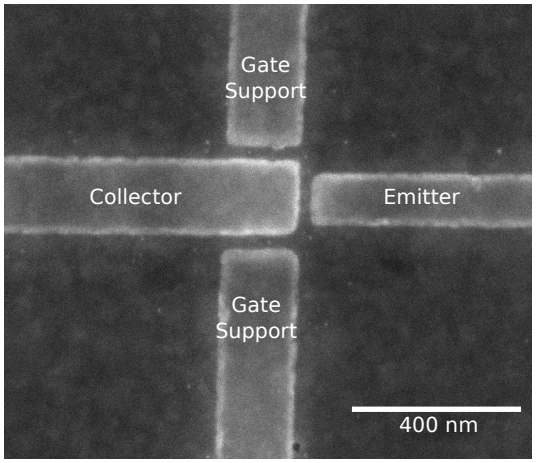


Figure 4.17: Alumina hard mask of tip region of tungsten high temperature triode with electrodes labeled.

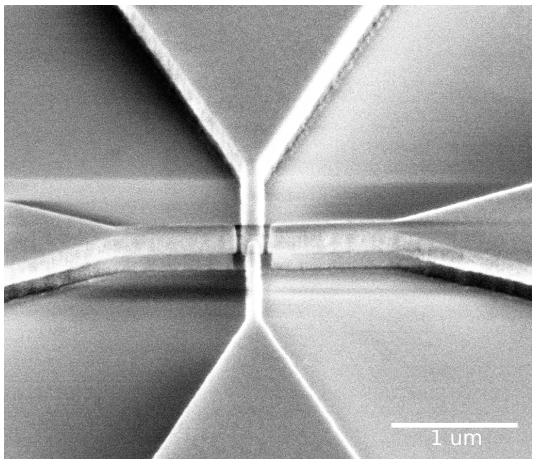


Figure 4.18: Preliminary demonstration of etched tungsten/silicon nitride stacks. The gap between the gate supports and the collector is 30 nm, the tungsten layer thickness is 200 nm, and the silicon nitride layer thickness is also 200 nm.

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Chapter 5

PLASMONICALLY ENHANCED FIELD EMISSION

Building on our previous experience with nanoscale field emitters, we seek to combine on-chip field emission and plasmonics. Earlier devices built on the concept of combining field emission with plasmonics focused on used field enhancement from metallic tip (Hommelhoff et al., 2006) or have used resonant plasmonic structures have lately been used to modulate field emission (Putnam et al., 2017). Here we take the approach of using nanofocusing in a waveguide to create very large optically induced electric fields inside a structure which is already a gated field emitter. We hope to use these large optical fields as an alternative gate, hopefully capable of ultrafast opto-electric modulation. Furthermore, we seek to demonstrate this device in a on-chip, and integratabtle fashion and operating at a wavelength that is commercially viable.

5.1 Simulation of Hybrid Plasmonic Nanocoupler

To achieve nanofocusing of our incident light we have adapted a scheme for adiabatic focusing of 1550 nm light that was theoretically describe by Lafone et al. (Lafone, Sidiropoulos, and Oulton, 2014) and experimentally demonstrated by Nielson et al. (Nielsen et al., 2016). In the work due to Nielson et al, the authors couple free space light into a silicon slab waveguide mode via an un-optimized gold grating. The silicon slab waveguide is laterally confined on either side by a metal loaded silicon slab waveguide consisting of gold/silicon dioxide/silicon layers. After the grating, the width of the silicon slab waveguide is reduced along a taper region as shown in overview of the structure in Figure 5.1 (a). The taper adiabatically couples light from the silicon slab mode into a hybrid plasmonic mode that exists primarily inside the gap in the gold layer, as shown in Figure 5.1 (b) . In the work of Nielsen et al. the entire device was clad in a layer of silicon dioxide and thus the gap was filled with silicon dioxide. The authors measure the field enhancement of the hybrid plasmonic mode by evaluating the photoluminescence enhancement for quantum dots placed inside the silicon dioxide inside gap. From this they calculate a maximum experimental field enhancement factor of 167 ± 26 for a 24 nm gap device. The authors suggest that this high field enhancement could be used to make modulators by placing a non-linear material in the high field region inside the gaps.

For our device, we intend to leave the gap un-filled and apply a sufficient voltage to field emit electrons. This will allows us to study the relationship between field emission and plasmonics.

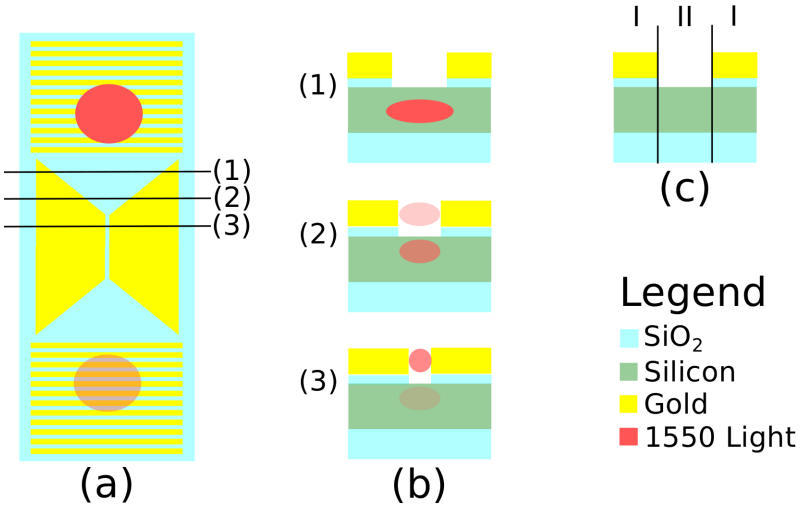

Figure 5.1: Diagram of adiabatic coupler as used in our experiment. In (a) is a top-down view of the device. Light is coupled into and out of the device via gold gratings. The taper regions convert light adiabatically between a silicon slab waveguide mode at large gaps to a hybrid silicon/plasmonic mode with significant energy in air as the gap width decreases, shown in (b). Unlike in previous works, there is no top oxide cladding. In (c) we label the three different multi-layer slab waveguides.

The operating principle of the hybrid nanofocusing structure can be explained phenomenologically, following an analysis due to Lafone et al. (Lafone, Sidiropoulos, and Oulton, 2014). The structure may be viewed as three multilayer waveguides as shown in Figure 5.1 (c). Region II consists of a silicon slab waveguide clad with oxide below and, in our case, vacuum above. The identical regions on either side (labeled I) consist of the same silicon slab waveguide, bound below by a silicon dioxide layer, and above by a spacer oxide layer and above that, a 50 nm thick layer of gold. At 1550 nm, gold has a refractive index of n = .52406 (Johnson and Christy, 1972). The low index gold layer lowers the refractive index of the metal loaded slab waveguide relative to the unloaded slab waveguide. The silicon slab waveguide in region II is therefore higher index and light can be guided inside it between the metal loaded regions. As the width of region II decreases to less than 100 nm, the TE silicon slab waveguide mode hybridizes with a plasmonic mode. This hybridized mode has significant field energy in the gapped region. As the gap width becomes

smaller, a larger percentage of the field energy is concentrated in the gapped region and additionally the effective index of refraction of the hybrid mode rises.

A first step to designing our proposed structure is to remove the oxide cladding found in previous works, and to remove the oxide in the gap. We use COMSOL finite element analysis to simulate the slab waveguide in each region. For material properties we use Johnson et al. for gold (Johnson and Christy, 1972), an extrapolation of Gao et al. for silicon dioxide (Gao, Lemarchand, and Lequime, 2013) , and Li for silicon at 293 K (Li, 1980). In Figure 5.2 we simulate the effective refractive index for the oxide-clad and bare silicon slab waveguide mode as well as the metal loaded modes without oxide cladding, with different spacer oxide thickness. For the metal-loaded waveguide modes, we plot both the TE and TM modes since the bound TE-like mode will couple to both. From this data we extract the difference in the real part of the refractive index between the bound TE mode (the TE mode of the silicon slab waveguide without oxide cladding) and the largest of either the TE metal-loaded refractive index or the TM metal-loaded refractive index for each spacer thickness as a function of the silicon slab waveguide thickness and plot it in Figure 5.3. The hybrid mode will be guided easier for larger refractive index differences. We see, somewhat surprisingly, that for a 20 nm SiO_2 spacer layer the refractive index difference is low regardless of the thickness of the silicon slab. This is because the refractive index of the TM mode of the silicon slab increases dramatically with decreasing spacer thickness.

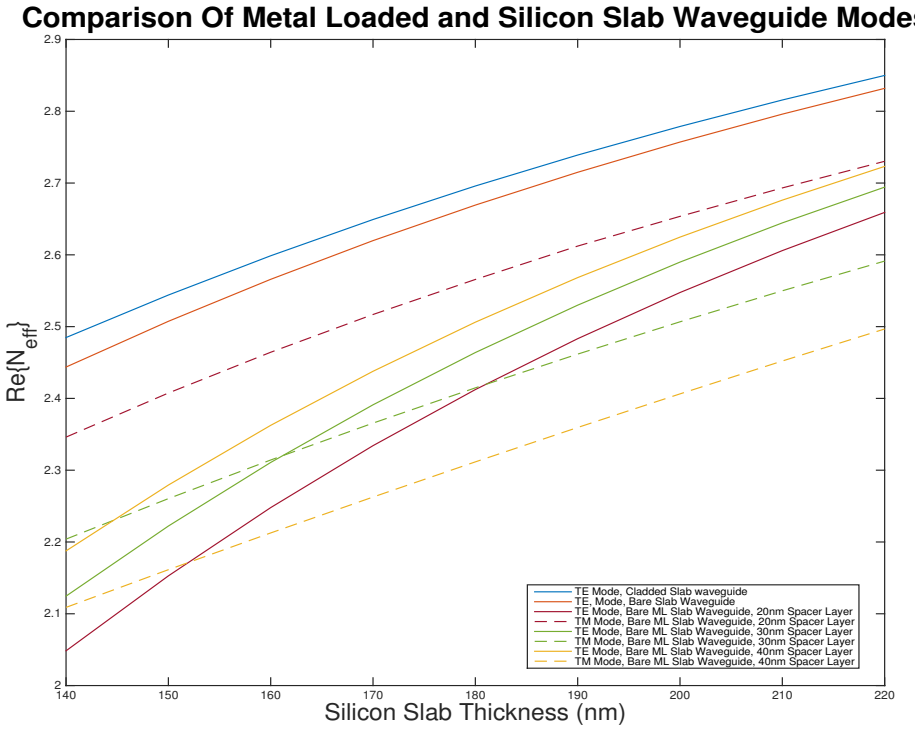

Figure 5.2: Comparison of the effective refractive index for the TE modes of the oxide clad and bare silicon slab waveguides with the real part of the effective refractive indices of the bare metal loaded slab waveguides. Both the TE and TM modes of the metal loaded (ML) slab waveguides are diagramed as the nanofocused mode can couple to either.

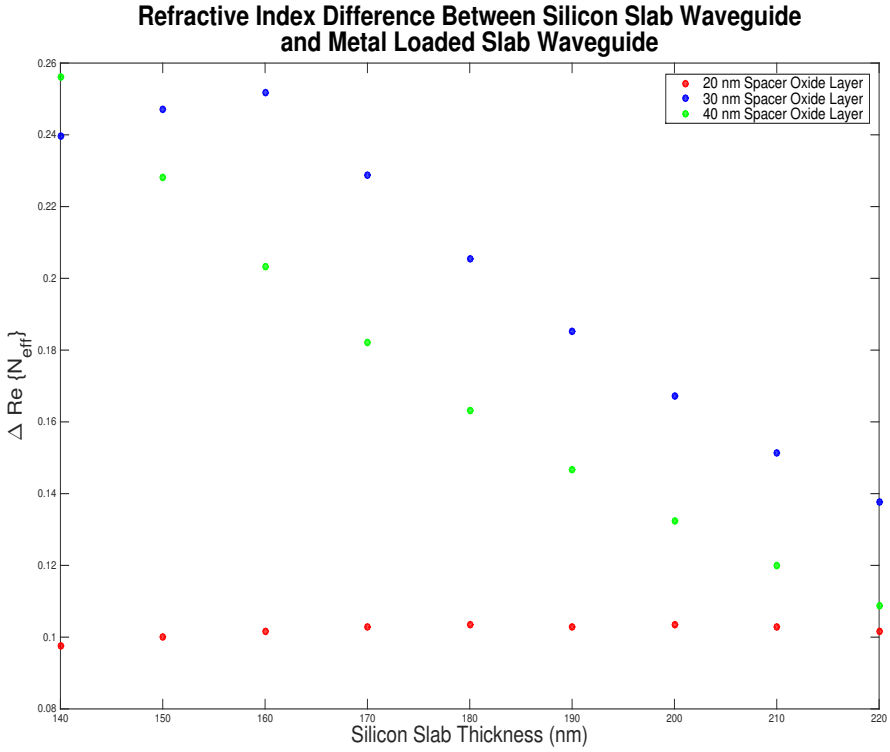

Figure 5.3: Difference between the effective refractive index of the bare silicon slab waveguide TE mode and the larger of either the TE or TM mode of the metal loaded slab waveguide modes. This indicates the parameters for maximum confinement.

5.2 Mode analysis of oxide-clad structure as model verification

With guidance from our mode analysis we may now use COMSOL finite element analysis we build a 2D model of the cross-section of our proposed device. We filet the corners of the gold layer to prevent unphysical hotspots. We include an additional rectangle to define an area of interest that surrounds the gap and an additional 10 nm on each side, horizontally and vertically. This rectangle defines our area of interest for evaluating the ratio of electromagnetic energy in the gap versus electromagnetic energy in the mode. This evaluation is given by

$$R = \frac{\int_{\text{gap}} \langle W \rangle}{\int_{\text{waveguide}} \langle W \rangle} \tag{5.1}$$

$$\langle W \rangle = \frac{1}{2} \left\langle \vec{E} \cdot \vec{D} + \vec{B} \cdot \vec{H} \right\rangle \tag{5.2}$$

where $\langle W \rangle$ is the time average energy density of the electromagnetic wave. We first evaluate the geometry demonstrated by Nielsen et al. (with oxide cladding atop the structure) to verify our finite element model. From the data in Table 5.1 we see several features which are indicative of nanofocusing. We see the real part of the refractive index rising with decreasing gap size. This is because a higher proportion of mode energy now resides in the high index region formed by the vertical silicon dioxide/silicon stack as opposed to the surrounding regions formed by the vertical silicon dioxide/gold/silicon dioxide/silicon stack. We also see the imaginary part of the refractive index, the extinction coefficient, rise with decreasing gap size. This high loss is characteristic of plasmonic waves. We further plot the mode diagrams in Figure 5.4 for the nanofocused mode at each gap width and with the same intensity scale. As the gap narrows, the mode energy that resided in the silicon sub layer is transferred to the gapped region.

Gap (nm)	Effective Mode Index	% of Mode in Gap	% of Mode in Metal
20	$2.84\text{-i}4.15\times10^{-2}$	25.14 %	5.58 %
30	$2.76\text{-i}1.44\times10^{-2}$	7.23 %	1.62 %
40	$2.74\text{-i}8.94\times10^{-3}$	3.84 %	0.85 %
50	$2.74\text{-i}7.18\times10^{-3}$	2.80 %	0.61 %
60	$2.74\text{-i}6.35\times10^{-3}$	2.36 %	0.50 %
70	$2.74\text{-i}5.86\times10^{-3}$	2.14 %	0.44 %

Table 5.1: FEM cross-section analysis of mode in Nielson et al. Gold thickness is 50 nm, oxide spacer layer is 40 nm, silicon device layer is 220 nm silicon and the device includes oxide in the gap as well as an oxide cladding layer of thickness 250 nm.

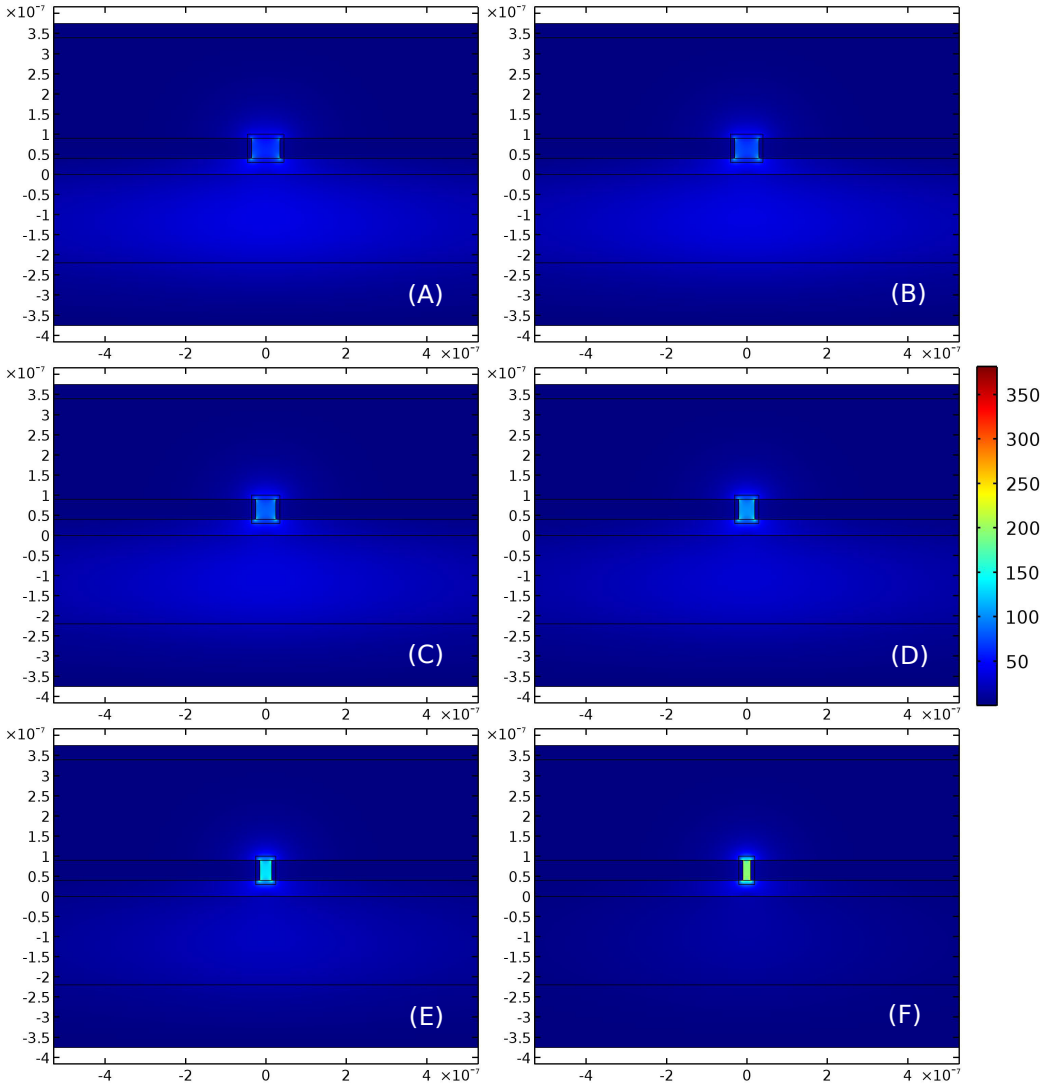

Figure 5.4: Mode diagram showing the evolution of hybrid plasmonic modes for gap sizes (a) 70 nm (b) 60 nm (c) 50 nm (d) 40 nm (e) 30 nm (f) 20 nm. Dimensions are taken from Neilsen et. al, Gold thickness is 50 nm, oxide spacer layer is 40 nm, silicon device layer is 220 nm silicon and the device includes oxide in the gap as well as an oxide cladding layer of thickness 250 nm. All figures are adjusted to the same intensity scale.

5.3 Mode analysis of undercut structure

This result matches the analysis in Nielson et al. With newfound confidence in the accuracy of our 2D mode simulations, we can proceed to modify the simulated structure to match a structure that is manufacturable and consistent with field emission. Firstly, we would like to be able to remove the oxide cladding and the oxide in the gap. This effectively lowers the refractive index of the middle waveguide reducing our confinement but allows us to field emit into the vacuum. Our gap is manufactured via neon focused ion beam. To ensure electrical isolation and limit leakage currents across the damaged oxide between the metal layers, we would also like to remove the spacer oxide in the gap region. This geometry has the added advantage of forcing the leakage pathway between the gold emitter and the gold collector to of necessity pass along the surface of the doped silicon layer. In the final device, the doped silicon layer will be electrically active as a gate so that we will be able to monitor directly the leakage current through the substrate. We also produce a small undercut of the oxide spacer layer to further limit the possibility of Frenkel-Poole surface leakage across the oxide, and to reduce the chance of oxide breakdown to the doped silicon layer by removing the oxide from the high field region between the emitter and collector. From experimentation, we have learned that the wet etch procedure used to produce an undercut in the oxide layer partially etches the silicon layer, probably because the silicon layer is damaged by the focused ion beam and thus becomes easier to etch. This is seen in Figure 5.5. We incorporate this silicon undercut in our simulations. For parameters, we choose a 30 nm silicon dioxide spacer layer, a 160 nm silicon layer, with a 30 nm deep silicon undercut as shown in Figure 5.6. To adequately capture the physics involved, we restrict the mesh to a maximum size of 5 nm in the gap region as shown Figure 5.7 In our phenomenological model of nanofocusing, the undercut lowers the effective refractive index of the middle waveguide region. Nevertheless, nano-focusing is still observed, as evidenced by the mode diagram shown in Figure 5.8. Additionally, a plot of the real and imaginary parts of the refractive index, shown in Figure5.9, shows a rise in the real part of the refractive index as the gap is reduced.

We would finally like to examine the proportion of mode energy that is focused into the gap region, as well as the mode energy that is focused into the emitter and collector tips specifically, shown in Figure5.10. This is the proportion of the mode energy that we expect to modulate field emission, either by multi-photon absorption or by tunnel ionization. From the cross-section of the fabricated structure, we see that the neon beam is not capable of producing a perfectly straight cross-section

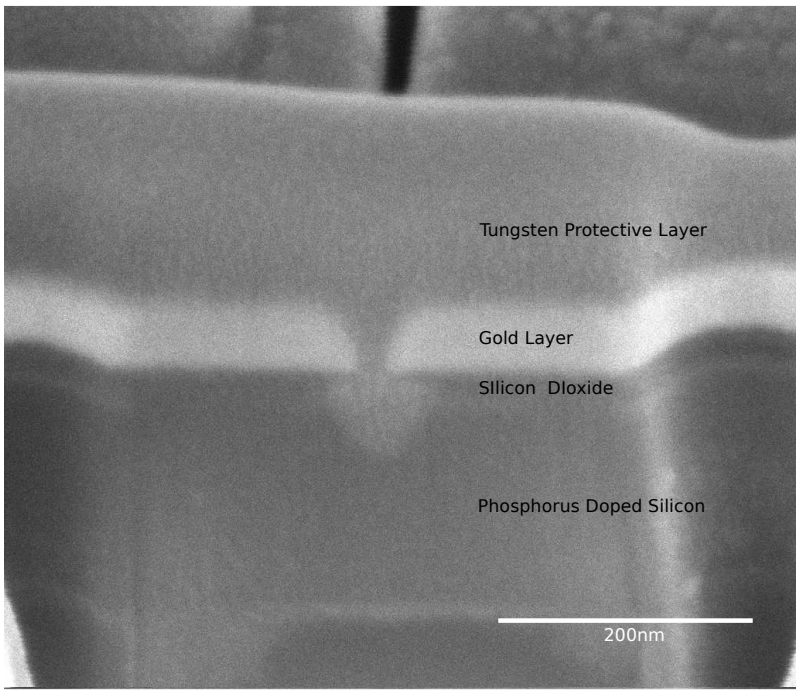

Figure 5.5: Cross section of nanogap device produced with neon ion FIB followed by 2 minutes of isotropic etching in 50:1 hydroflouric acid with buffer. A tungsten protective layer has been deposited in-situ by electron beam induced deposition to preserve the layers during cross section

in the gold layer. We examine the effect of angled sidewalls via simulation by considering the hybrid plasmonic mode for a undercut structure as in the study above. The undercut in the oxide spacer layer is 30 nm in the undercut in the silicon layer is 30 nm in depth. A mode diagram for this hybrid plasmonic mode is shown in Figure 5.11. In this case, the gap width is the distance of closest approach and is fixed at 20 nm. From the mode profile, we see that the point of nearest approach is now a hot spot, but that the confined mode continues to exist. We again examine the real and imaginary parts of the refractive index of the hybrid plasmonic mode, now as a function of angle, in Figure 5.12. The real part of the refractive index varies slightly with angle, while paradoxically the extinction coefficient is reduced with increasing angle. We also examine the mode energy confinement as a function of sidewall angle in Figure 5.13.

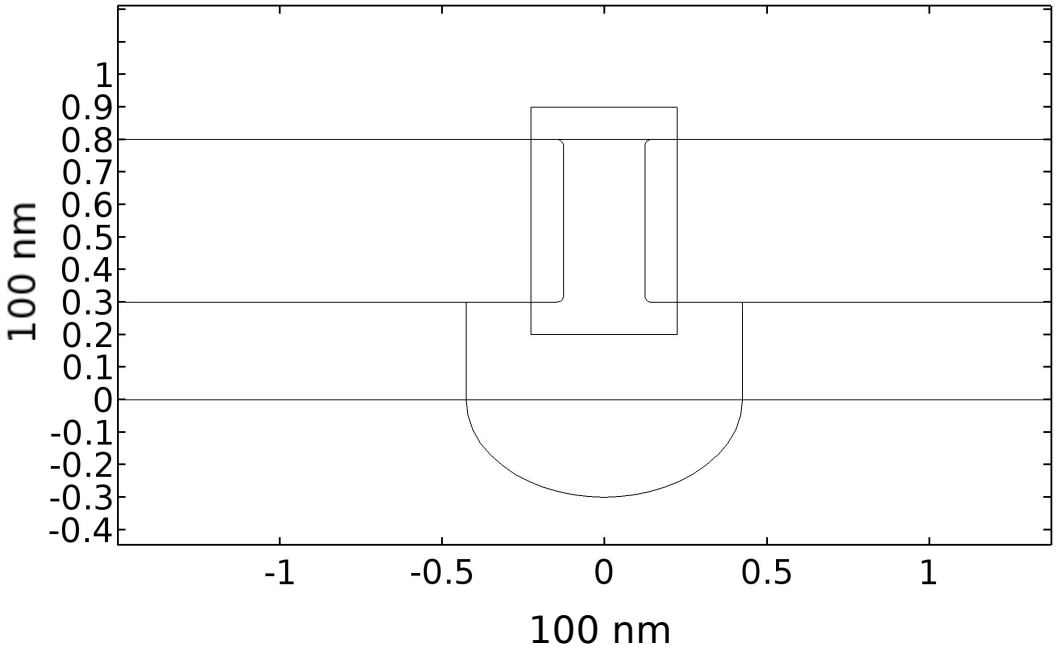

Figure 5.6: Simulated undercut structure. The boxed region allows the the definition of a high resolution mesh area, as well as the calculation of mode power in the gap region.

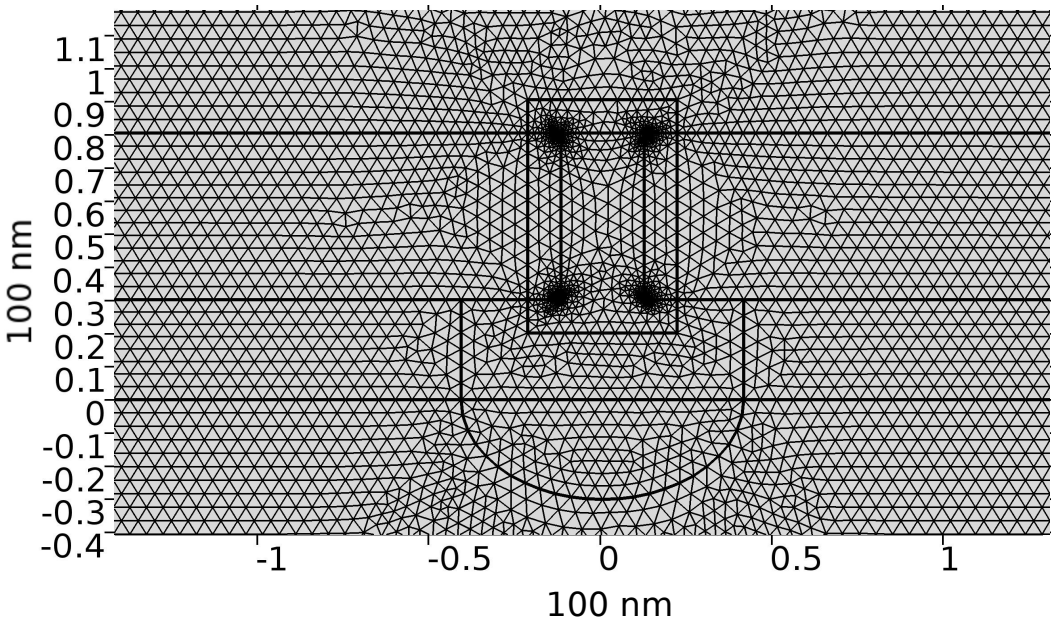

Figure 5.7: Meshing of simulated undercut structure. Mesh size inside the gap region defined by the box is restricted to be a maximum of 5 nm in either x or y direction.

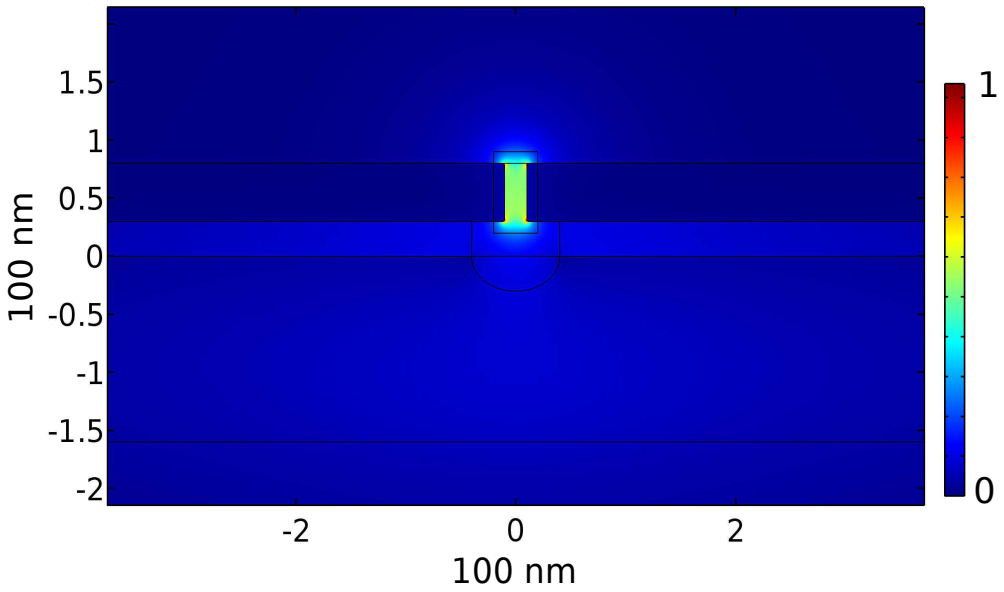

Figure 5.8: Mode diagram (zoomed) of nanofocused mode in undercut structure. The undercut is 30 nm and the gap is 20 nm.

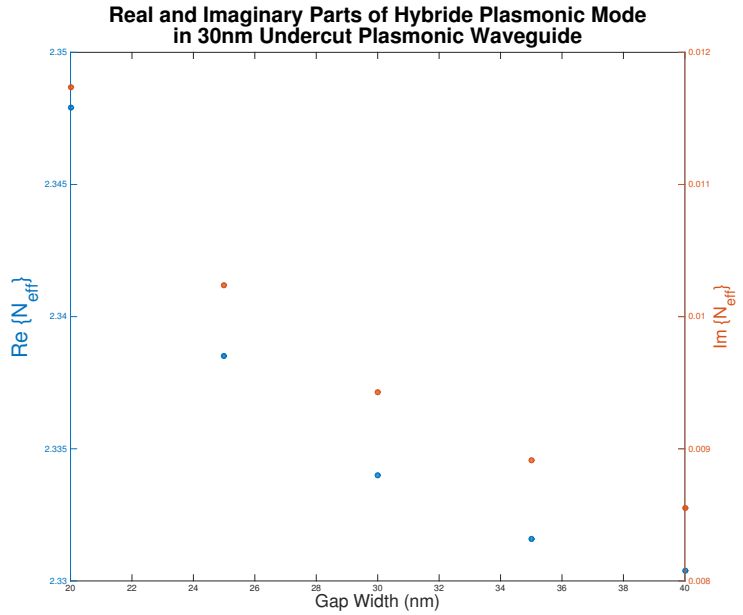

Figure 5.9: Real and imaginary part of the refractive index for mode in undercut structure with 30 nm silicon dioxide undercut and varying gap width

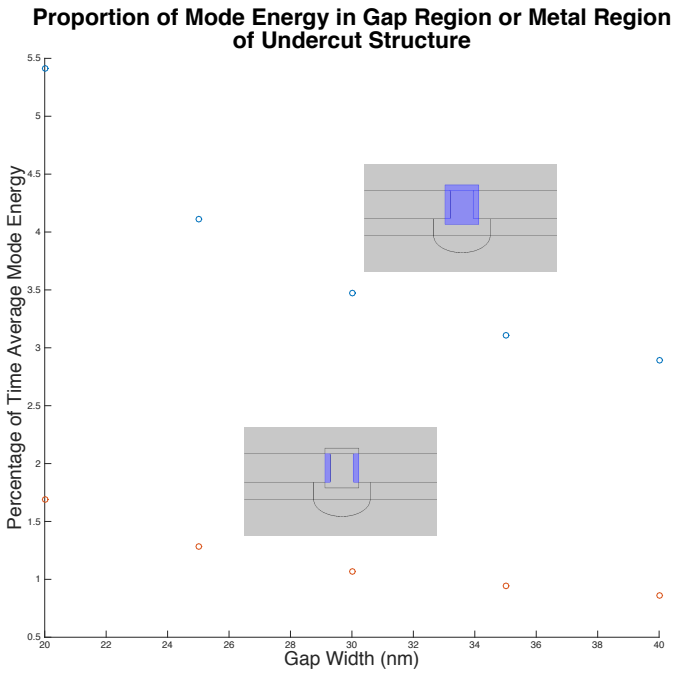

Figure 5.10: Evaluation of mode energies in nanogap and emitter and collector tips as a function of gap width undercut structure with 30 nm silicon dioxide undercut and varying gap width.

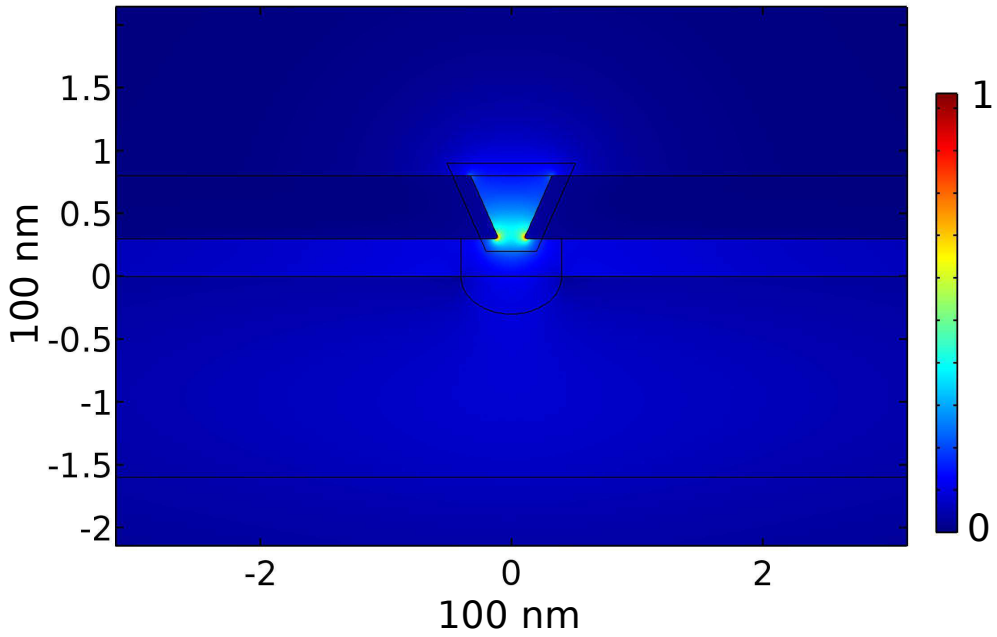

Figure 5.11: Mode diagram (zoomed) of nanofocused mode in undercut structure with 24° angled sidewall. The silicon dioxide undercut is 30 nm and the gap is 20 nm.

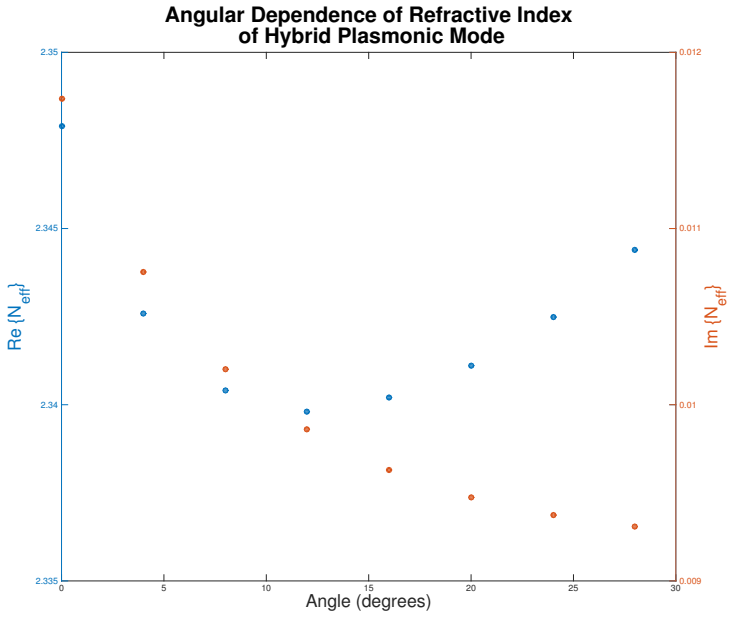

Figure 5.12: Real and imaginary part of the refractive index for mode in undercut structure with 30 nm silicon dioxide undercut and 20 nm gap with varying angled sidewalls.

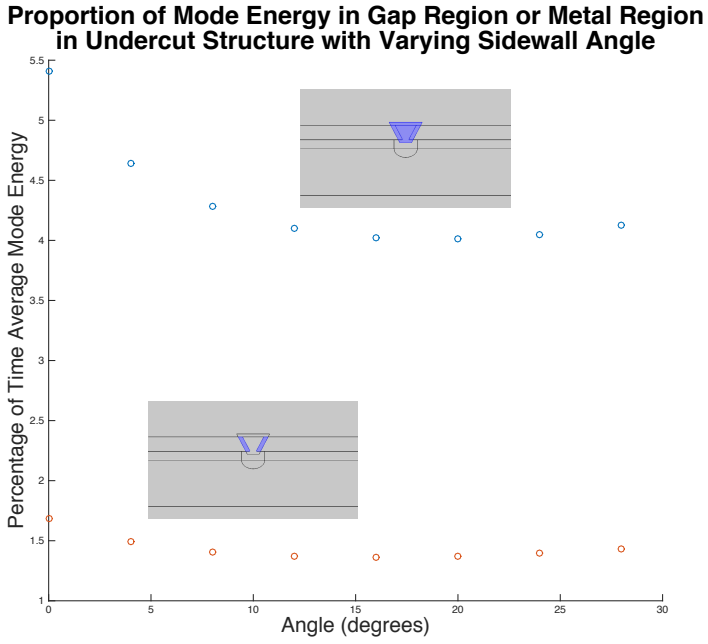

Figure 5.13: Evaluation of mode energies in nanogap and emitter and collector tips as a function of gap width undercut structure with 30 nm silicon dioxide undercut and varying gap width.

5.4 Simulation of electrical properties

In addition to simulating the confinement of the hybrid plasmonic mode, one must also simulate the electrostatic properties of the proposed structure to ensure that field emission and gating at these dimensions are possible. Unlike in the case of the multilayered field emitters in chapter 4, the gold emitter and collector in this device are symmetric. They are also relatively blunt, with a width of 50 nm which is large relative to the gap between the emitter and collector. This limits the static (to distinguish from the plasmonic) field enhancement. Ignoring the angled sidewalls and the oxide undercut for a moment, we calculate the field enhancement as a function of the emitter and collector gap width in Figure 5.16. From the results of the simulation of the hybrid plasmonic mode, we fix the thickness of the silicon dioxide spacer layer as 30 nm, the silicon layer as 160 nm, and the gold layer as 50 nm. We set a surface voltage of -1 Volt on the emitter and 0 Volts on the collector as well as the gate as shown in Figure 5.14. The simulated normalized electric field for a 20 nm gap is shown in Figure 5.15. The field magnitude is approximately a tenth of the necessary field for field emission which corresponds to a 10 Volt turn-on, although the possibility of nanoscale protrusions that experience higher field enhancements may lower the observed turn-on voltages. This is indicative of the small static field enhancement experienced by the blunt tips as the gap width is decreased.

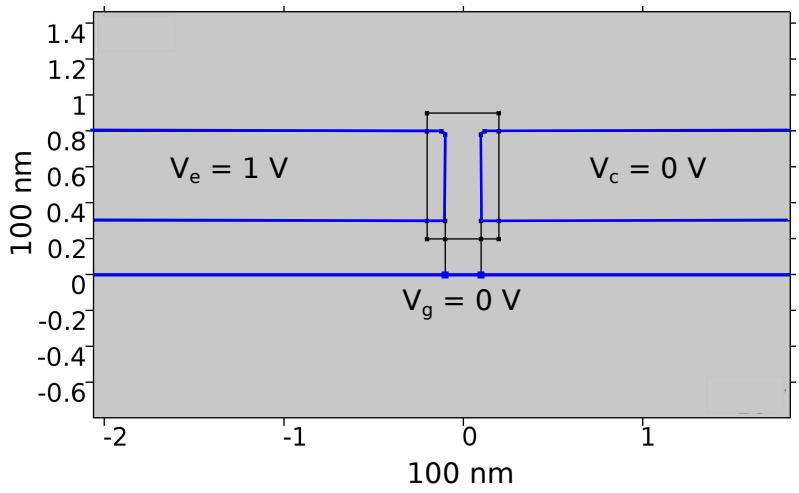

Figure 5.14: Location of surface voltages in electrostatics simulations of plasmonically enhanced field emission device. The small center rectangle is a virtual area to enforce a more refined mesh and for the evaluation of maximum field area.

Gating of field emission in the plasmonically enhanced field-emitting structure

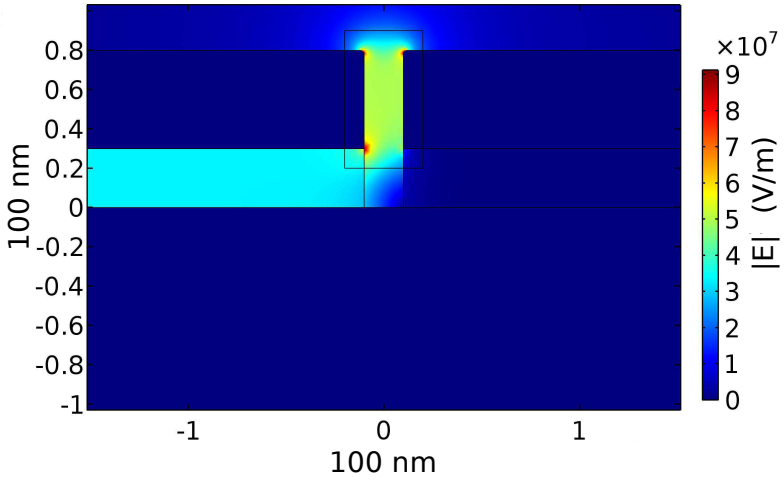

Figure 5.15: Field diagram of biased plasmonically enhanced device with 20nm gap width. Without an undercut, the oxide separating the emitter and collector experience a significant hotspot.

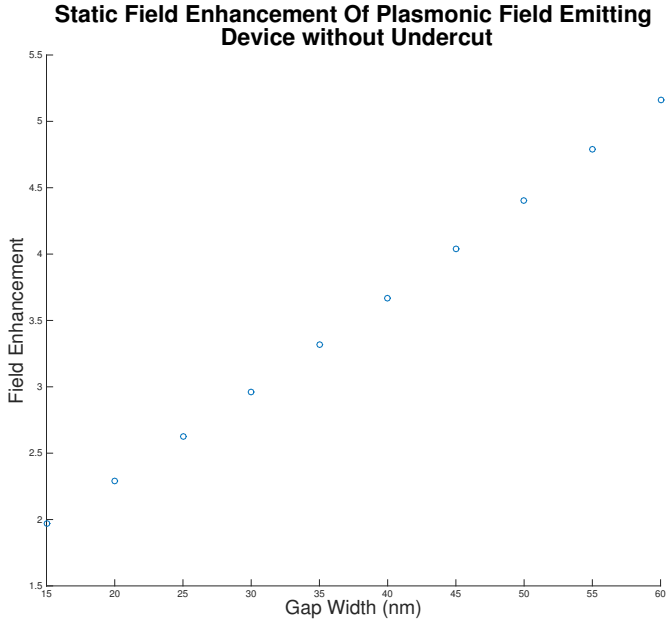

Figure 5.16: Field enhancement of biased plasmonically enhanced device with varying gap width and with no undercut and without angled sidewalls.

competes with spacer oxide breakdown. The dielectric strength δ_{BD} of thin film thermal silicon dioxide can be between 1-10 MV/cm or 0.1-1 V/nm (Klein and Gafni, 1966). The biasing scheme that allows the largest difference between the emitter and collector voltages (and thus the largest modulated current) is to have the gate modulated around a bias which is half the difference between the emitter

and collector (for now we'll assume the collector is biased at 0 V). This allows the emitter to be biased to a maximum of twice the breakdown voltage of the gate dielectric. Let T be the thickness of gate oxide and W be the gap width and ρ_{FE} be the field enhancement experienced by the tips

$$\begin{aligned} V_{BK} &> V_{FE} \\ \delta_{BD} * T &> \frac{1\text{V/nm} \times W}{\rho_{FE}} \end{aligned}$$

Here we have used 1 V/nm as an estimate for the field strength to cause field emission. We see that a major priority is to maximize field enhancement and to minimize gap width to minimize the right-hand side of the equation while maximizing the left-hand side of the equation by increasing the breakdown voltage. The thickness of the oxide layer is fixed by the optical design to 30 nm. To this end, we implement an undercut of the oxide. This also prevents the formation of hot-spots at the metal-dielectric interface as shown as shown in Figure 5.17. The should reduce the probability of oxide breakdown. As Figure 5.18 shows, the static field enhancement slightly increases with any amount of undercut compared to the device with no undercut, though additional undercut doesn't confer increased static field enhancement.

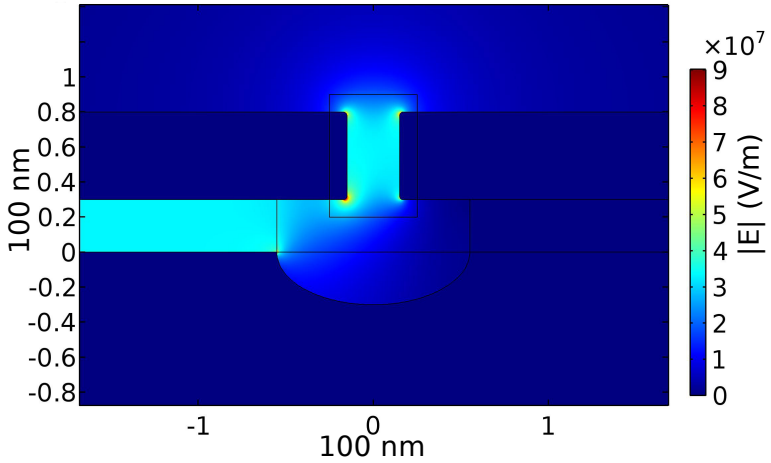

Figure 5.17: Field diagram of biased plasmonically enhanced device with 20 nm gap width and 40 nm undercut. The hot spot from the non-undercut structure has disappeared.

A final question to consider is whether and how much the angled sidewalls of the structure as produced by neon focused ion beam affect the static field enhancement. We simulate the electrostatic problem with angled sidewalls. From the mode diagram in Figure 5.19, we see that emission will occur at the bottom edge of the gold

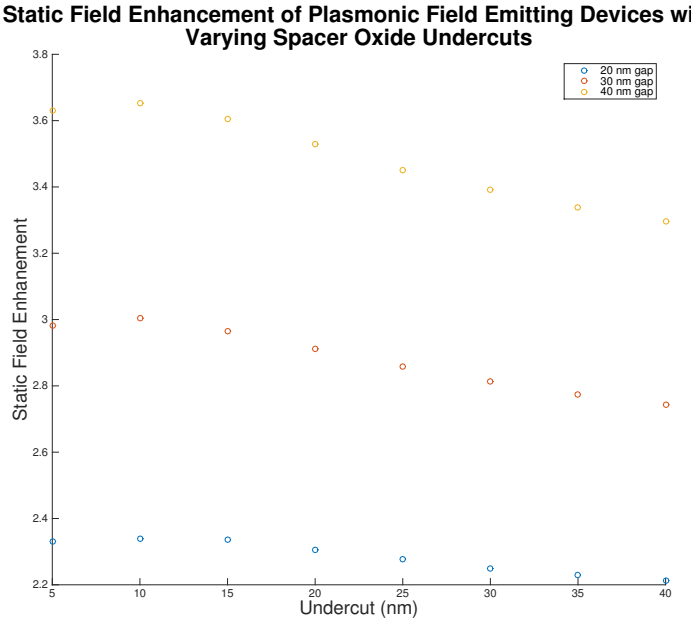

Figure 5.18: Static field enhancement of plasmonically enhanced field emission structure as a function of silicon dioxide undercut gap width. The spacer oxide thickness is 30 nm.

layer. We plot the field enhancement for a device with a 20 nm gap, a 30 nm spacer oxide layer and a 30 nm undercut in Figure 5.20. From these studies we see that the field enhancement of the angled undercut structure is slightly higher than the non-angled undercut structure for the same gap width but is relatively insensitive to the specific angle and/or the specific undercut amount. This is advantageous from a fabrication perspective because controlling these two variables with any precision is difficult.

With the incorporation of spacer oxide undercut and angled sidewalls the simulated device is now similar to the fabricated cross-section shown in Figure 5.5. Gating of the current between the emitter and collector will be done by applying a voltage to the doped silicon layer. The gold emitter and the gold collector each form a capacitor with the underlying doped silicon layer so it is reasonable to expect that the added field will be very similar to the fringing field of a parallel plate capacitor. From a well known result of undergraduate electromagnetism, the magnitude of this fringing field of a parallel plate capacitor is approximately $\frac{1}{2}$ the magnitude of field in the middle of the capacitor. This fact implies that for devices with emitter to collector lengths similar to the spacer oxide thickness, we need to modulate the potential difference of the emitter and the gate, ΔV_{EG} at approximately twice the

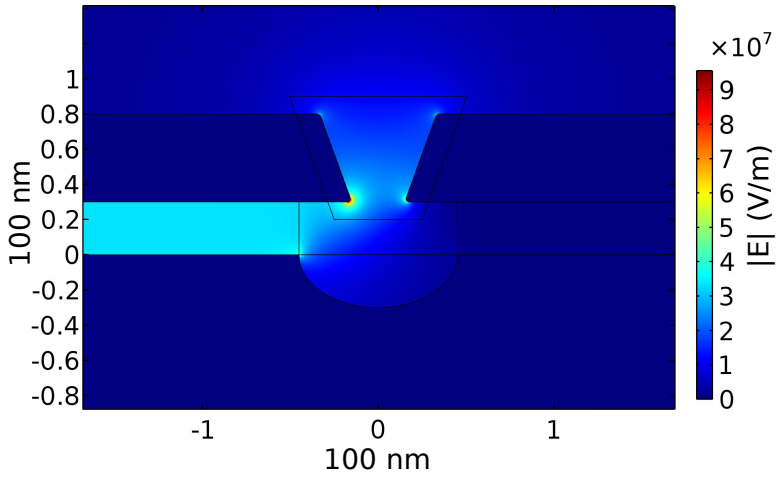

Figure 5.19: Field diagram of biased plasmonically enhanced device with angled sidewall and with 40 nm gap width and 30 nm undercut.

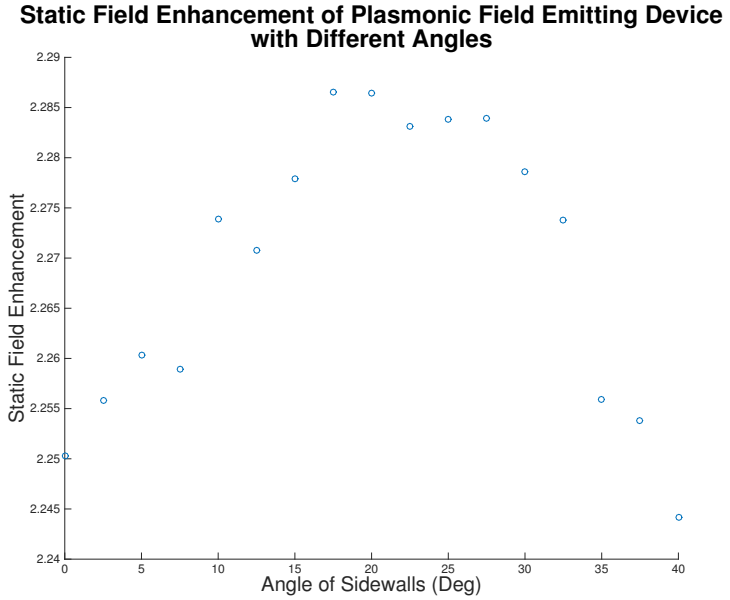

Figure 5.20: Static field enhancement of plasmonically enhanced field emission structure as a function of sidewall angle. The spacer oxide thickness is 30 nm, the gap width is 20 nm and the silicon dioxide undercut is 30 nm.

magnitude of the emitter to collector potential difference, ΔV_{EC}, to produce the same electromagnetic field. To more quantitatively analyze gating, we simulate the electrostatic problem using COMSOL FEM for a representative structure with different gating potentials with the emitter held at -1 Volts and the collector held at 0 Volts: 30 nm oxide spacer, 20 degree angled sidewalls, and various gap widths. We evaluate the maximum electromagnetic field along the surface of the emitter tip,

identified in Figure 5.21, for each set of voltages and gap widths. We plot the results in Figure5.22 . From this plot it becomes apparent that the gate voltage acts to

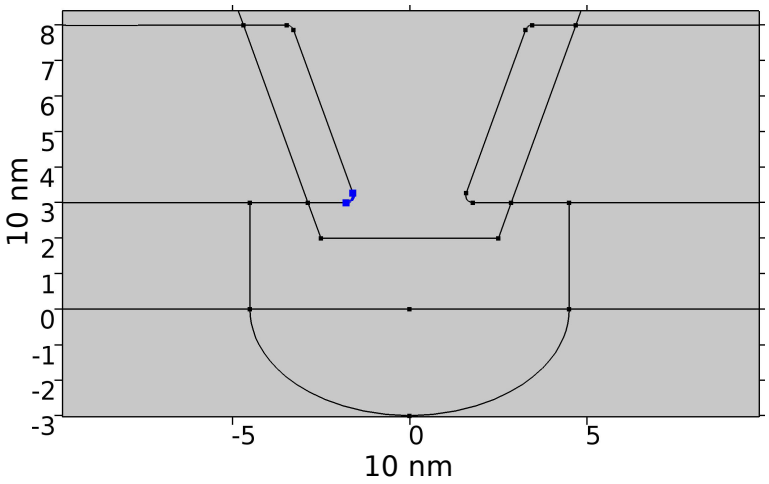

Figure 5.21: Diagram showing the emitting surface in blue for the evaluation of maximum electric field and gradient vector streamlines for different gap widths and biases.

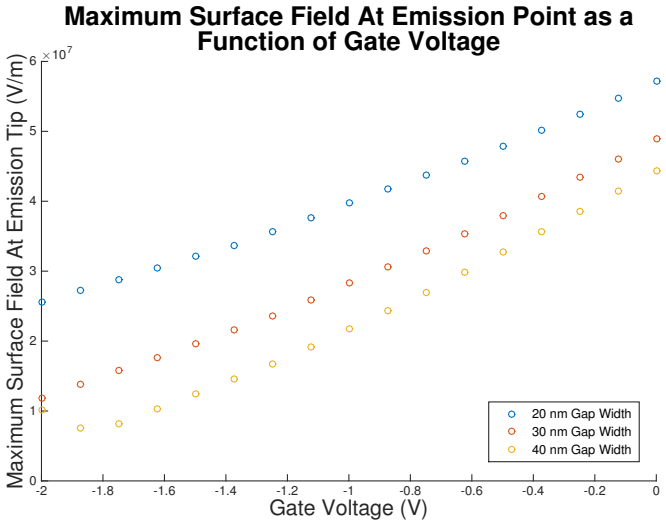

Figure 5.22: Electrostatic field for fixed emitter and collector voltages. As the gap widens for fixed spacer oxide thickness, the gate becomes more effective at modulating the maximum surface field, though the overall field is decreased.

lower the maximum field on the emitting tip as the gate voltage is lowered from the collector voltage (ground) to the emitter voltage (-1 Volts in this model) and beyond. The field on the emitter tip is a linear sum of the fields produced by ΔV_{EG} and ΔV_{EC}, and as the gate voltage is lowered to the emitter voltage the fringing field produced

by the emitter/gate capacitor decreases to zero. As the gate voltage is lowered still further, the magnitude of the fringing field increases, but the direction opposes field emission from the tip. Additionally, the field produced by a fixed ΔV_{EC} decreases with increasing gap width so that for larger gap width devices the modulating field between the emitter and gate is a larger proportion of the total field. This allows the same $\Delta V_{EG} = 2$ V to modulate the maximum emitter field by a factor of 4.37 in a device with a 40 nm gap width compared to only a factor of 2.24 in a 20 nm gap width device. Given similarly spaced and biased collector and gate it must be checked that electrons leaving the emitter tip do indeed go to the collector. We plot the vector gradient streamlines of the electric potential for the 30 nm gap width device in Figure 5.23. The vector gradient streamlines are plotted by starting at the emitting surface defined in Figure 5.21 and following the gradient $\nabla V = E$ in small steps. The force on emitted electrons is $F = qE = q\nabla V$ and the momenta of the electrons are small so we may use the streamlines as an approximation for the path that emitted electrons follow. This approximation ignores uncertainty in the precise emission location, space charge effects, and momenta effects. From Figure 5.23 we see that when the gate and collector are at the same bias both have the potential to collector electrons. As the bias on the gate decreases, electrons are less attracted to the gate, though the magnitude of the emitting field is smaller for the same ΔV_{EC}. The lack of a sharp emitting point on the gate serves to keep the gate from field emitting even when biased to twice the emitter bias, $\Delta V_{GC} = 2\times\Delta V_{EC}$. The practical lower limit to the gate bias is set by the breakdown voltage of the capacitor formed by either the gate and collector or the gate and emitter. Since field emission requires fields on the order of 1 GV/m, we expect that the fabricated devices should begin to emit at approximately 2-10 volts. This depends on the presence of microprotusions and surface contaminants, which would tend to lower the work function.

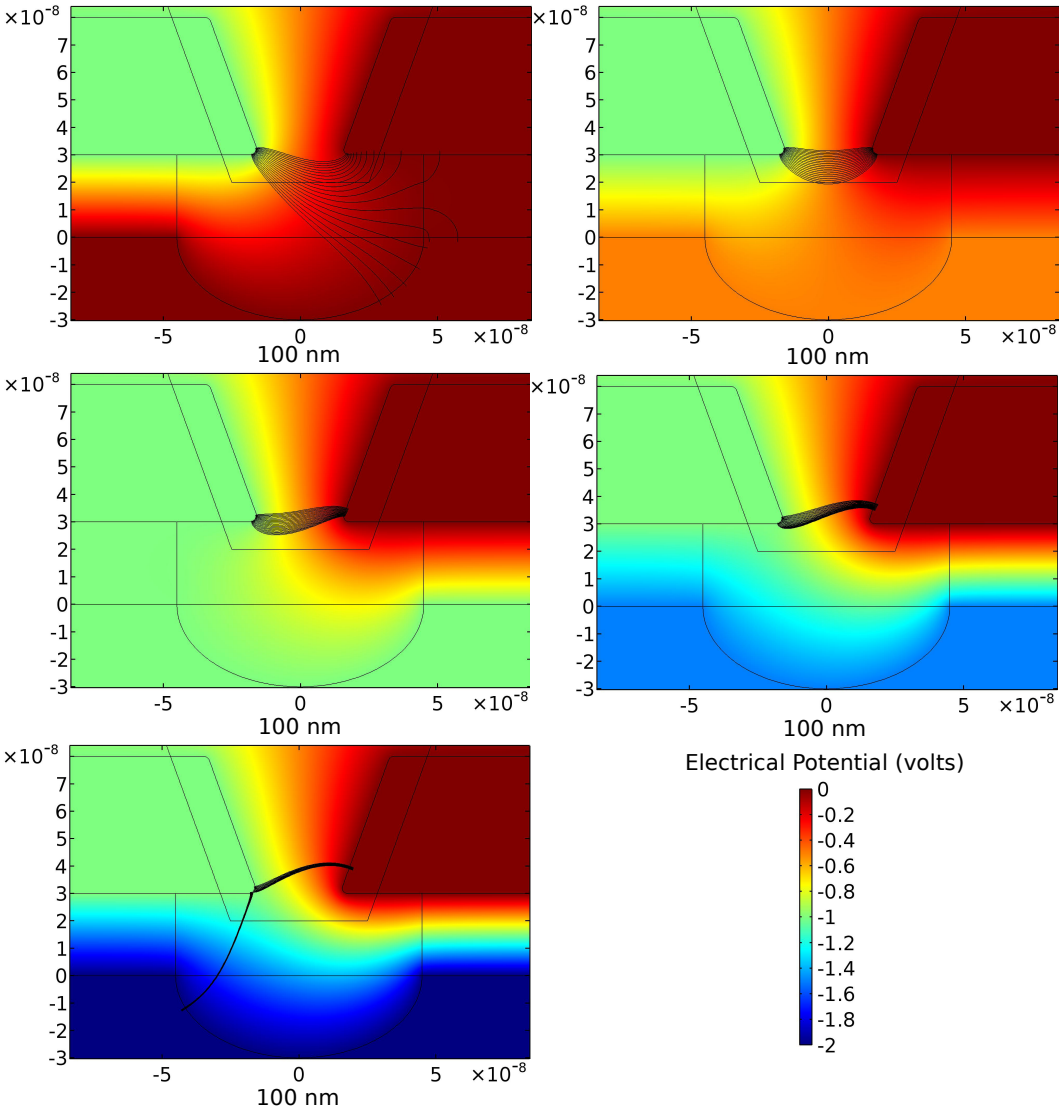

Figure 5.23: Potential field of plasmonically enhanced field emission structure as a function of gate bias. The black lines represent electric field streamline curves as a stand-in for the path of emitted electrons. The spacer oxide thickness is 30 nm, the gap width is 30 nm, and the silicon dioxide undercut is 30 nm.

5.5 Fabrication of plasmonically enhanced field emitting structure

We begin similarly to our work in multi-layer field emitting devices in chapter 4 by doping silicon on insulator with phosphorus via spin-on dopant. Our starting substrate is 220 nm silicon on 2000 nm silicon dioxide. We perform a native oxide etch using 6:1 buffered hydroflouric acid for 3 minutes, followed by spinning Desert Silicon P-260 dopant (500 rpm/3500 rpm for 5 seconds/ 35 seconds) followed by baking on a hotplate at 200 °C for 5 minutes. We then perform pre-deposition in a 1 inch tube furnace in nitrogen atmosphere for 30 minutes at 600 °C. We then

strip the spin on dopant in 6:1 buffered hydroflouric acid for 5 minutes, checking for hydrophobicity following the etch. Finally we perform drive-in for 30 minutes in a 1 inch tube furnace in an oxygen atmosphere. We perform a final hydrofluoric acid etch to removed the oxide grown during drive-in. The device layer is now doped and has been thinned to 200 nm.

To produce the desired combination of silicon and silicon dioxide thicknesses we have two methods. The first method is to grow dry thermal oxide in a 1 inch dry furnace at 1050 °C and then hydroflouric acid etch the sample in successive steps to thin the silicon layer from the initial 200 nm to 180 nm. We then grow a final layer of dry thermal oxide and anneal the sample in nitrogen gas to produce a silicon dioxide layer that is 20-30 nm thick on top of a silicon layer that is 160 nm thick. Throughout this process we use filmetrics to monitor the growth of oxide and the thickness of the silicon layer. The annealed silicon dioxide makes a high dielectric strength barrier to gate leakage. We've successfully applied a field of 8 Volts across a device with a 26 nm thermally grown silicon dioxide layer with leakage current of 1 nA (though repeated operations at these high voltages eventually caused breakdown). This implies a dielectric strength of 3 MV/cm. Literature suggests that the dielectric strength can be improved by at least a factor of three (Klein and Gafni, 1966) though those values were recorded for significantly thicker films and thinner dielectric films are known to be of higher dielectric strength. The downside to thermal oxide growth is the practical difficulty of simultaneously controlling the thickness of the silicon and silicon dioxide layers. An alternative to this, which is our second method, is the use of atomic layer deposition of silicon dioxide films. With atomic layer deposition we first etch the doped silicon layer from 200 nm via plasma etching to 160 nm and then we grow silicon dioxide via thermal or ozone atomic layer deposition. The quality of ALD grown thermal silicon dioxide layers depends on the temperature of deposition. Literature indicates that breakdown fields of 5-10 MV/cm can be expected for ALD films grown with ozone at 300 °C (Han and Chen, 2013). Additionally, literature also indicates that many of the properties, such as etch rate in hydroflouric acid, of silicon dioxide films grown by thermal ALD can be improved to more closely match thermal SiO_2 by annealing at high temperatures (Hiller et al., 2010). We ourselves have observed that the dielectric strength of thermal ALD (specifically low temperature thermal ALD deposited at 120 °C) is improved by a factor of 2-3 by annealing in a nitrogen furnace at 1000 °C.

After obtaining the desired thickness for the oxide spacer layer and the doped silicon device layer we cleave the substrate into individual chips that are each approximately 10 mm×20 mm. We then deposit 400 nm of silicon dioxide via PECVD along 3 mm wide strips on each of the long sides of the chip. To do this, we put an appropriately sized chip in the middle of the substrate before loading the sample into the PECVD. The second chip acts as a shadow mask to prevent additional silicon dioxide deposition in the middle of the substrate. The contact pads will be placed on the thicker oxide portion of the chip to prevent shorting the emitter and/or collector to the substrate during ultrasonic wirebonding. This was an issue with early designs. Contact lines will connect contact pads to junctions on the chip.

We then use e-beam lithography to pattern junction region, the contact lines and the emitter/collector contact pads, optical gratings, and small circles near the junction that will be later used during He/Ne FIB milling as focusing features. At this step, there is no gap between emitter and collector. That will be produced later via He/Ne FIB milling. For the e-beam lithography process we use PMMA A8 950 electron beam resist spin coated for 5 seconds/30 seconds at 500 rpm/4000 rpm and then baked on a hotplate at 180 °C for 4 minutes. We develop the sample for 30 seconds in 1:3 MIBK:IPA at room temperature. We then deposit 3 nm/50 nm of Ti/Au using electron beam evaporation at a rate of 0.5 Å/s / 1 Å/s. We then perform liftoff in heated Remover PG because we have noticed significant difficulties during metal removal that we attribute to resist burning. A representative junction region is shown in Figure 5.24.

After fabricating the unseparated junctions and contact lines, we use a photomask (produced here at Caltech using a process found in the addenda) to define gate contact regions several millimeters from the junction on the thin spacer oxide. We immerse the patterned device in a 6:1 buffered hydroflouric acid to etch the gate contact region so that we may later contact the gate. We use a second photolithography step to define regions to deposit thick Au for contact pads, both on top of the bare silicon to serve as the gate contact pads and also on top thick oxide region and connected to the emitter and collector contact lines. We use e-beam evaporation followed by liftoff to deposit a thick 10 nm/400 nm Ti/Au layer onto the defined regions. The thick contact pads connecting the emitter/collector layer works in concert with thick PECVD oxide rails to prevent punch-through during ultrasonic wire bonding. Following the deposition of the contact pads, we quickly check the dielectric strength of our oxide films by wirebonding a small number of gapless

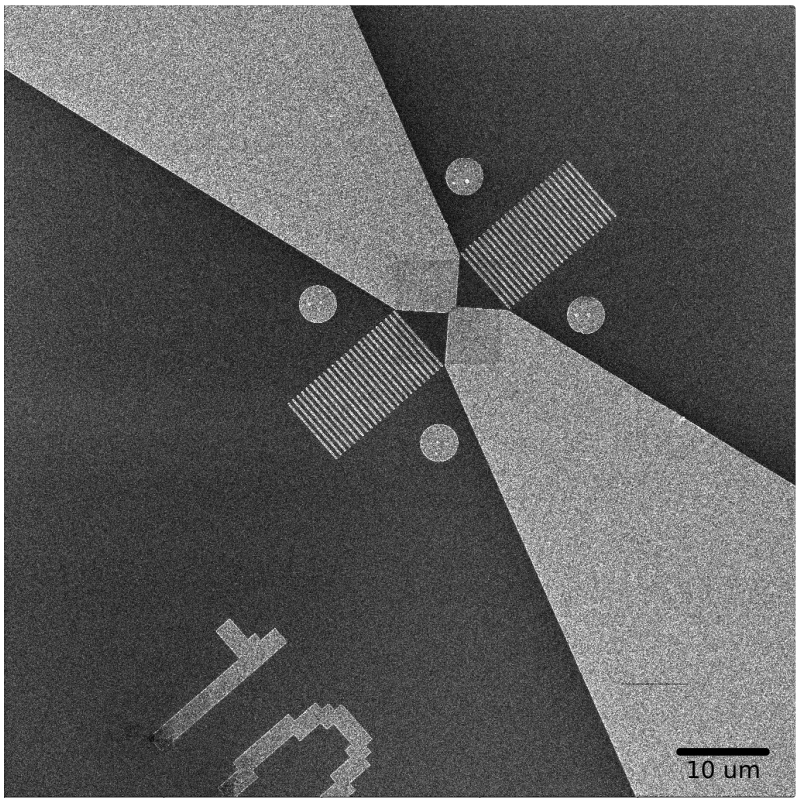

Figure 5.24: Overview SEM of fabricated plasmonically enhanced field emittion device

devices and a gate contact and examining leakage current and dielectric strength.

Following this qualification testing, the gap is formed using neon focused ion beam (FIB) lithography in a Carl Zeiss Orion NanoFab. The objective is to produce the narrowest complete gap in the metal layer as well as in the silicon dioxide spacer layer underneath. The silicon dioxide gap allows the elimination of an unmonitored leakage pathway through the oxide. For complete oxide gaps, all surface leakage will go into the gate contact, which is separately monitored. This allows further verification that any current leaving the emitter and entering the collector is indeed Fowler-Nordheim field emission. After significant testing, which is elaborated on in the addenda, the parameters used to produce the junction were a focused Neon beam at 10 keV making single pass lines with step resolution of .5 nm, a dwell time of 1 μs. The dose to clear the gold and silicon dioxide from the junction, chosen via dose arrays, is 0.015 nC/μm. The single pass line is oriented to be 41° relative to the positive x-axis in the field of view of the microscope. This is the machine specific angle between the two split neon beams, caused by the different focus of two common isotopes ^{22}Ne (90% of neon atoms) and ^{20}Ne (9% of neon

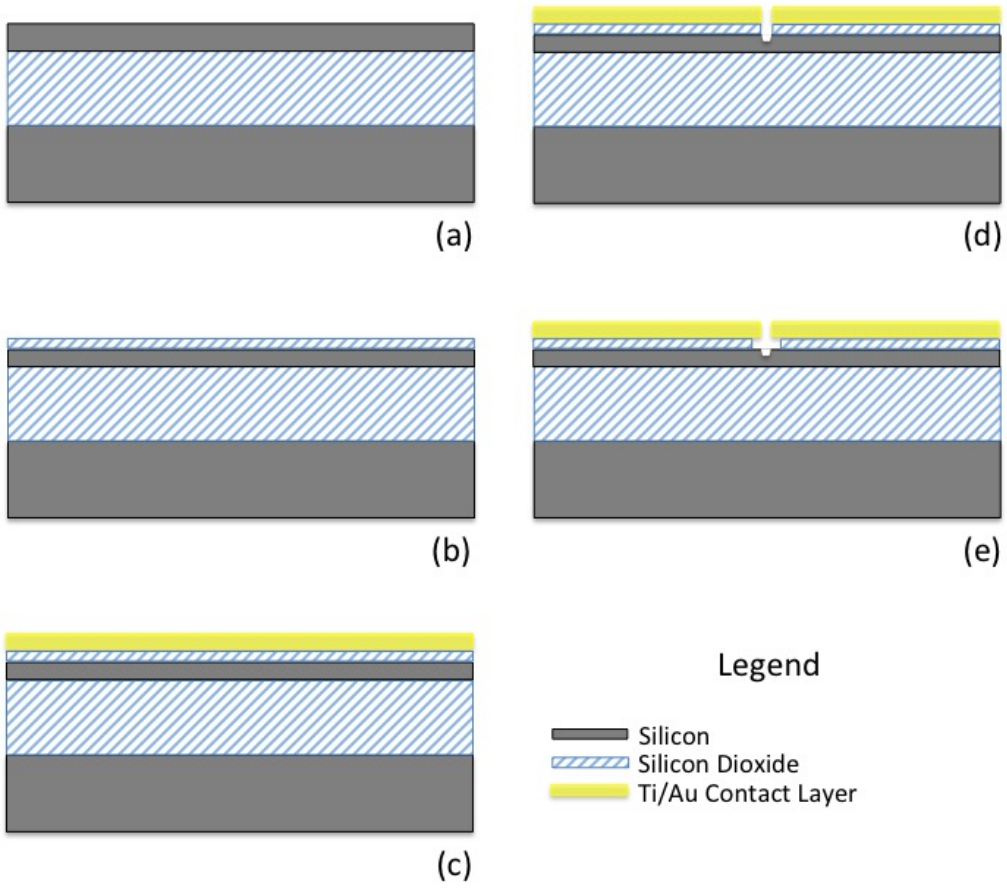

Figure 5.25: Fabrication Procedure for the gap region of plasmonically enhanced field emission device

atoms). Following the FIB lithography, hydroflouric acid is used to undercut the gap by 20-30 nm. This small undercut, as elaborated on in the simulation section, is a strategy to remove the oxide from the high field junction region and so lower

the possibility of dielectric breakdown. First a custom made photomask is used in a negative tone AZ 5214 process to protect the chip, minus 10 μm×10 μm squares at the junctions, from the acid. The chip is then immersed in dilute 50:1 buffered hydroflouric acid for 1 minute, followed by water rinse, and then immersion in solvent to remove the photoresist. This produces waveguide cross-sections similar to the ones seen in Figure 5.5. An additional oxygen plasma clean serves to remove any organic residue.

Finally, the device is ultrasonically wirebonded to a chip carrier. An emphasis here is placed on using the minimal ultrasonic power (typically less than 25% of maximum power) to avoid punch through and oxide damage. Additionally, experience has taught that repeatedly wirebonding a device often leads to punch through at the bond pad.

5.6 Measured field emission from plasmonically enhanced field emitting structure

Purely electrical testing of these devices initially took place at atmosphere, since the mean free path of electrons is much greater than the manufactured gaps. The collector was attached to common ground, while the emitter and collector were both attached to Keithley sourcemeters. Before neon ion milling, tests of gate oxide failure were performed on gapless devices to determine the maximum allowable voltage difference between the gate electrode and the emitter or collector electrode. A representative example of one such test is shown in Figure 5.26. Several devices per chip would be sacrificed to quantify safe testing voltages.

Following gate oxide failure analysis, the remaining devices were milled using the neon focused ion beam, and then cleaned and wirebonded. Initial testing took place by performing emitter voltage sweeps while biasing the gate at an intermediate voltage between the maximum expected emitter voltage and the collector voltage (ground in this case). One such example is shown in Figure5.27. The current was limited to 100 nA. We attribute the low turn-on voltage to surface contamination. The considerable width of the emitting surface made contamination induced lowering of the work function more possible by providing more sites of approximately equal electric field for contaminants to land on. This results in lowering the work function barrier to field emission. Similarly to our earlier work on multilayered field emission devices, we plot the current voltage characteristics of this device in Fowler-Nordheim coordinates in Figure 5.28 . That is, we plot the data using $1/V$ as the x-axis and

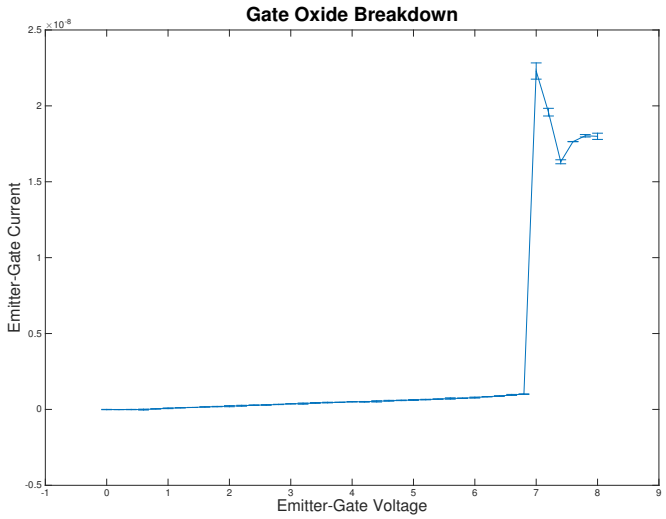

Figure 5.26: Breakdown of gate oxide on un-milled device as determined by decreasing the emitter voltage while holding the gate at ground.

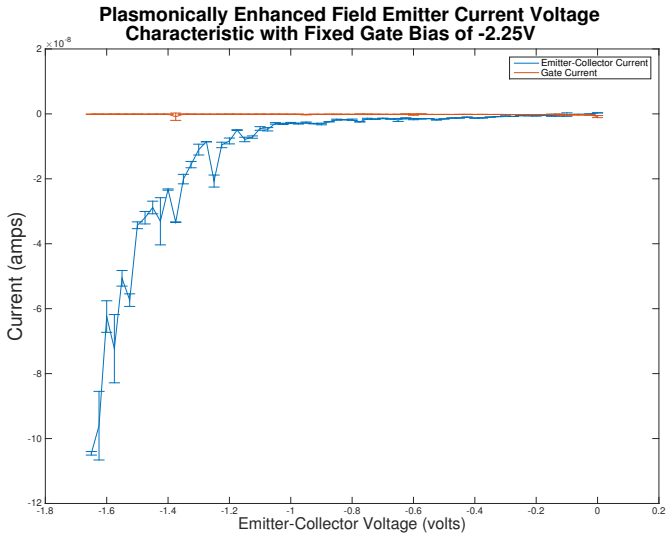

Figure 5.27: Current voltage characteristic for plasmonically enhanced field emitting device generated by sweeping the emitter voltage with fixed gate bias of -2.25 V and collector held at ground.

$\log(I/V^2)$ as the y-axis. Here the current I is in units of Amperes and the voltage V is in units of Volts. Finally, we gate the device by applying a voltage to the doped silicon gate layer in Figure 5.29. As outlined previously, for gate bias levels between the emitter bias and collector bias (ground), for all gaps, decreasing the voltage on the gate decreases the fringing field produced by the emitter and gate capacitor. The result of this is that as the gate bias is lowered, a lower emitter voltage

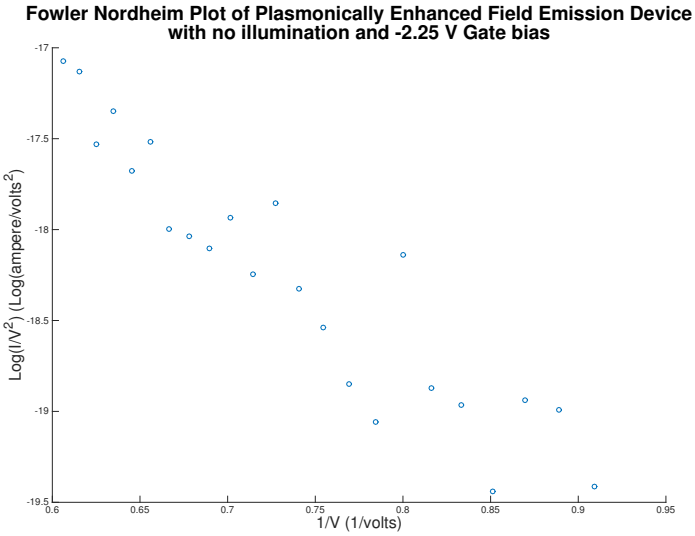

Figure 5.28: Fowler-Nordheim characteristic for plasmonically enhanced field emitting device with fixed gate bias of -2.25 V and collector held at ground. Data is plotted for voltages after turn-on, in this case approximately 1.1 V.

(higher emitter-to-collector differential) is required to induce field emission. As a

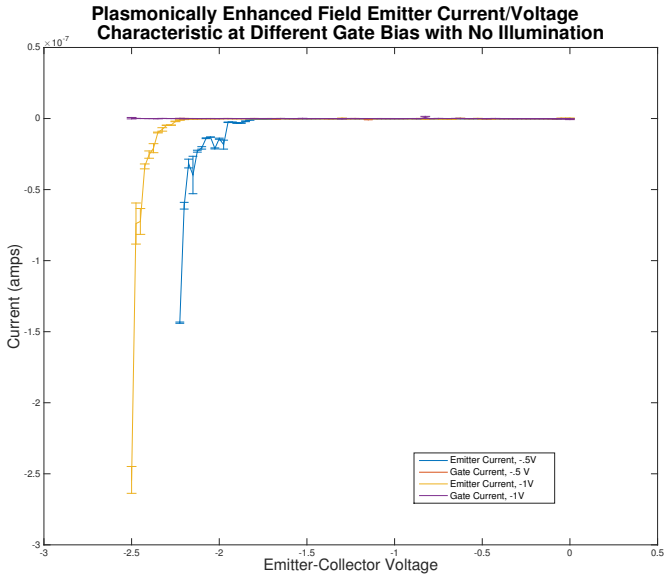

Figure 5.29: IV for plasmonically enhanced field emitting device with generated by sweeping the emitter voltage with different gate biases at collector held at ground.

final caveat, working devices experienced degradation over time in atmosphere. We attributed this to surface contamination, and began using a nitrogen box to store our devices between testing sessions. Furthermore, for electrical and later optical

testing we fabricated a small gas enclosure into which we flowed dry nitrogen gas. In this way we limited surface contamination while maintaining flexibility to select different wire-bonded devices for electrical and optical testing.

5.7 Kelydish parameter

The transition to the strong-field emission regime is indicated by the Keldysh parameter.

$$\begin{aligned} \gamma &= \frac{\tau_t}{\tau_{\text{cyc}}} \\ &= \omega \frac{\sqrt{2mW_F}}{eF_P} \end{aligned}$$

where $\omega = 2\pi f$ is the frequency of input light in radians, W_F is the work function of emitting material (in this case 5.1eV for gold), m is the mass of the electron and e is the charge of the electron. F_P is the total field, the sum of the time-varying field from the incident light and the static field due to the fixed biases. If we insert $F_P = 1V/nm$, the estimated field required for field emission we calculate $\gamma = 9.25$. This value of γ corresponds to the multi-photon absorption regime; however, the field F_p can be increased by increasing the bias ten fold, which should allow the device to operate in the tunnel-ionization regime without having to increase the incident optical power. This is an advantage of incorporating plasmonic focusing into a design that is already a low-voltage nanoscale field emission device.

5.8 Optical testing setup

Following the successful demonstration of gated field emission by the the plasmonically enhanced field emitting device, we manufactured a free space optical setup to simultaneously probe the optical and electrical properties of our device. The initial experiment will be to test the optical response of the plasmonically enhanced field emission device. Telecommunications wavelength light will be coupled into the hybrid plasmonic waveguide via the grating shown in Figure 5.24. The optical grating is an un-optimized 25% duty cycle, with 629.5 nm grating period.

The optical setup is shown in Figure 5.30. Light from a tunable, telecommunications band, polarized laser (Keysight Technologies 81689A, maximum power 153 mW) is guided through free space to a beam splitter and an into a NIR objective (Mitutoyo 100X NIR M-Plan Apo). The NIR input beam beam path shown in red in Figure 5.30. A 1550 nm centered half-wave plate is inserted before the beam splitter to allow the polarization angle of the NIR laser light to be rotated to be maximally coupled

into the device. The light reflected off the sample as well as the light out-coupled by the output grating is re-collected by the NIR objective and directed to a NIR camera (Merlin Indigo) by the beam-splitter. The return beam line is shown in green. A second in-line beam splitter allows free-space white illumination light to be inserted in the beam line. This allows the sample to be illuminated for coarse navigation. The second in-line beam splitter is on a flip mount so that during data acquisition it can be removed from the beam line and the position of the NIR laser and the angle of the half wave plate re-adjusted to maximize output coupled light. The sample is mounted on a three axis stage to allow sample navigation and the sample and stage are enclosed within a partially enclosed nitrogen gas testing chamber shown in Figure 5.31. The testing chamber allows the reduction of the amount of water vapor in the environment, which can precipitate early dielectric breakdown. A fiber electro-optic modulator (Lucent Technologies Model: X-2623Y), driven by an RF source (Rhode and Schwarz SMC 100A) allows amplitude modulation of the tunable NIR laser source.

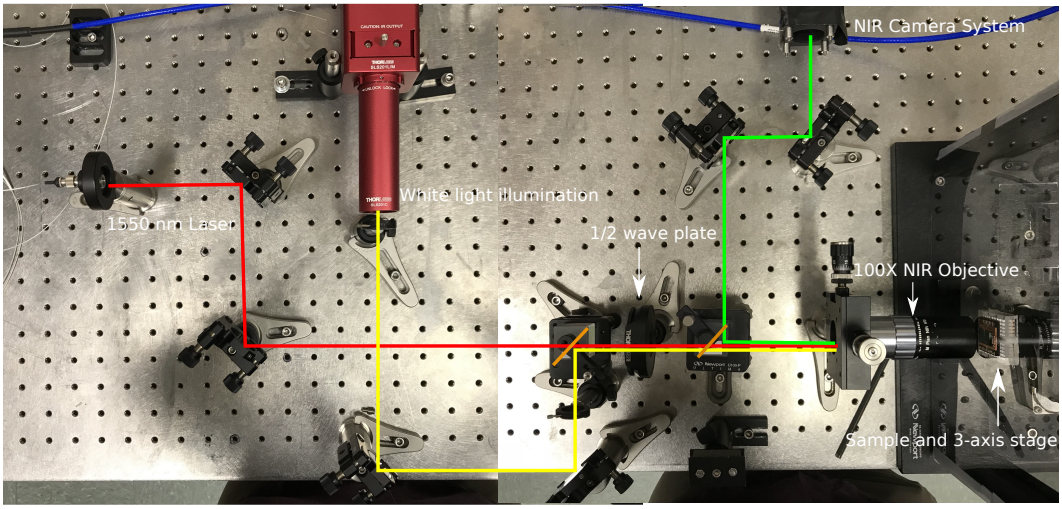

Figure 5.30: Free-space optical setup for testing optical response of plasmonically enhanced field emission device. The red beam path represents the path taken by polarized telecommunications wavelength laser light, the yellow path represents the the path taken by white illumination light, and the green path represents the return path from the sample.

As stated before, the NIR camera combined with the polarized source and the half-wave plate, allows the maximization of coupled light into hybrid plasmonic waveguide. Rotating through the polarizer, we can visually see the intensity of the output coupled light changes, as shown in Figure 5.32. Coupling light though the

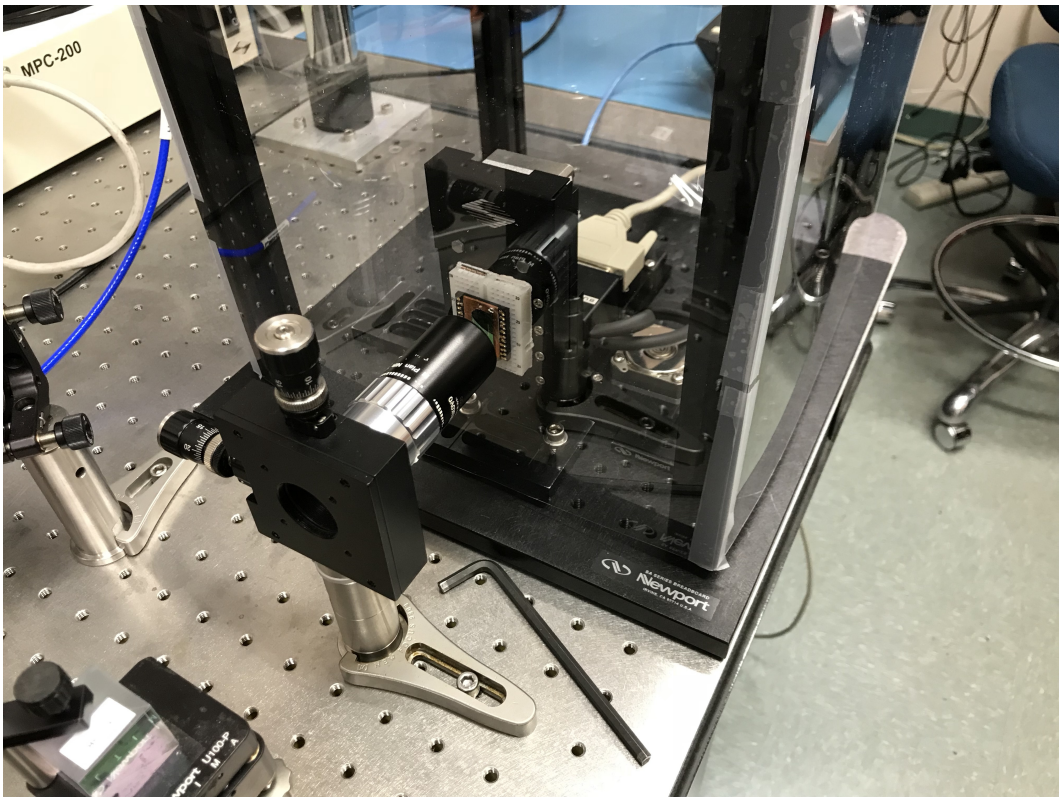

Figure 5.31: Partially enclosed sample test chamber. During testing, the sample chamber is continuously purged with dry nitrogen.

grating, as opposed to the direct illumination in previous experiments, eliminates the possibility of direct heating from normal incidence light. Observing polarization dependent signal from the output grating insures that light is being coupled into the plasmonic waveguide.

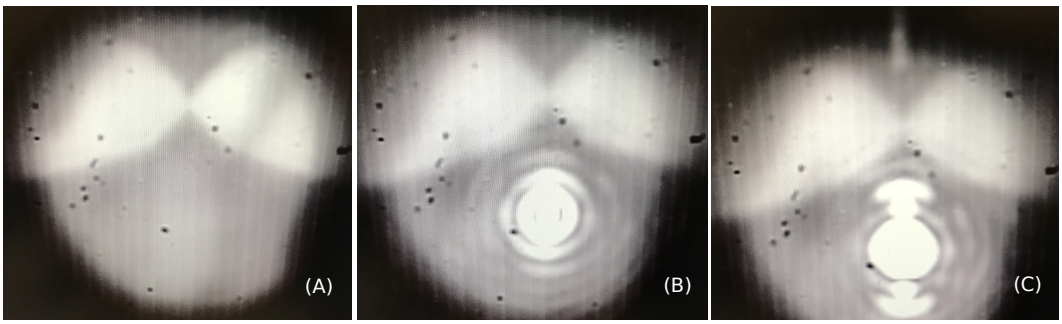

Figure 5.32: NIR camera image of PLFE device active region in (A). In (B) and (C) the tunable telecommunications wavelength laser is turned on. Between (B) and (C) the half-wave plate is rotated by 90 degrees. In (C) the half wave plate is rotated to maximize the light entering the hybrid plasmonic waveguide and exiting the output grating.

For optical testing, the emitter and gate of the plasmonically enhanced field emitting device are connected to sourcemeters (Keithley 2400 attached to the emitter and Keithley 2410 attached to the doped silicon gate). The collector is connected through a resistor R of modest voltage (50 kOhm) to ground. An oscilloscope, triggered by the RF source driving the electro-optic modulator is connected across the resistor R. The input impedance of the oscilloscope is 1 MOhm so that very little current flows into the oscilloscope when it is connected in parallel to the resistor, R. The circuit diagram is shown in Figure 5.33. For currents of 100 nA, the voltage measured across R = 50 kOhms will be 5 mV, which is well within the range of the oscilloscope.

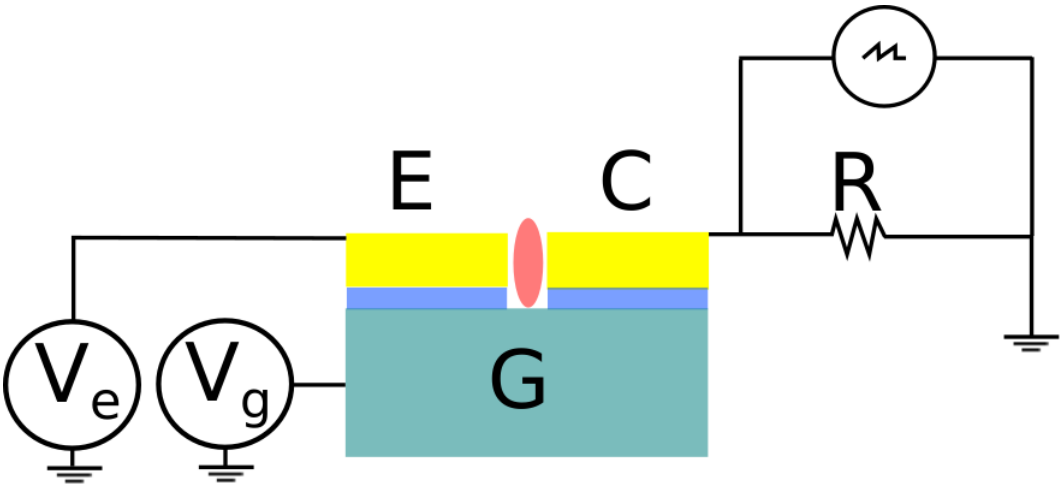

Figure 5.33: Diagram of testing circuit for plasmonically enhanced field emitting device. The coupled light (shown in red) is intensity modulated via an electro-optic modulator that also triggers the oscilloscope.

5.9 Future work

This experiment is on-going in the Axel Scherer group. Having demonstrated that the fabricated devices operate as nanoscale field emitters, and having built an optical testing testing setup, we hope to shortly provide data on the efficacy of this device as an opto-electric modulator.

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Chapter 6

CONCLUDING THOUGHTS

In 1947, William Shockley, Walter Brattain, and John Bardeen demonstrated the first solid-state transistor, a point contact transistor (Gertner, 2012). For this invention they won the 1956 Nobel Prize in Physics and also heralded the end of the age of the vacuum tube transistor (n.d.). The bipolar junction transistor (BJT) and later the metal oxide semiconductor field effect transistor (MOSFET), developed soon thereafter, eventually supplanted the vacuum tube transistor in almost all electronics. The reasons for this were simple: vacuum tube devices were fragile and couldn't be miniaturized further or easily integrated. In contrast, improvements to solid state transistors came quickly: techniques to purify semiconductors reduced scattering in the channel (Theuerer, 1963), photolithography allowed devices to be patterned en-masse, and improvements to fabrication technology reduced manufacturing errors at an even faster clip than device scaling. With the invention of the integrated circuit by Jack Kilby in 1958 (Kilby, 1964), solid-state devices were off to the races. With each generation, dimensions shrunk and virtually every metric of a MOSFET improved (a model pointed out by Dennard (Dennard et al., 1974)).

The solid-state transistor has undoubtedly changed the world. In his seminal 1965 paper, Gordon Moore wrote "Integrated circuits will lead to such wonders as home computers - or at least terminals connected to a central computer - automatic controls for automobiles, and personal portable communications equipment" (Moore, 1998). The paper also included a comic, meant to invoke the ridiculousness of the claim, of a man selling "Handy Home Computers" to a bevy of eager department store customers next to the cosmetics section. Time has shown Moore to be remarkably prescient. Today we enjoy immensely powerful personal computers, cell phones that connect anyone to anyone else, and cars that automatically and seamlessly adjust their internal mechanics to operate better. All this was made possible by the irresistible march of the semiconductor industry. Now that this march has slowed, there is cause to examine if other devices are positioned to supplant the solid-state transistor as the solid-state transistor supplanted vacuum tube transistor.

In this thesis, I have demonstrated a paradigm to produce practical nanoscale field emitting transistors (FEmTs) that can operate in atmospheric pressures, and at

CMOS compatible voltages. The proposed design is within the capability of modern foundries to produce and is on the cusp of readiness for integration in small circuits. I have described an on-going project to make field emitting transistors that deliver on the promise on high temperature operation and radiation hard operation. Finally, I have demonstrated a paradigm for integrating field emission with a hybrid plasmonic waveguide operating at telecommunications wavelengths on a silicon platform.

It is my belief that the nanoscale FEmT is a device whose time has come. Building on the same integrated circuit technology that doomed the vacuum tube transistor, nanoscale FEmTs can finally scale to dimensions that can mitigate their earlier flaws. They can fill a niche role, at least in the beginning, by operating in harsh environments that modern CMOS is unable to fill. And finally, modern advances in plasmonics can be uniquely harnessed by field emission devices to potentially make faster transistors than ever before possible.

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Chapter 7

ADDENDUM

In my time at Caltech, I have had the privilege to explore many different types of nanofabricated structures. What follows is a set unconnected process notes serving as a facility specific guide to identifying and mitigating various fabrication problems.

7.1 Helium/Neon/Gallium Ion FIB

Focused beam lithography is a promising direct write technique to make to fabricate small, anisotropic structures. The process can be done without a mask, which allows rapid prototyping of designs and usually enables higher resolution than traditional photo- or electron-beam lithography followed by etching or liftoff. This is because the thickness of the resist limits the resolution of the feature patterned in the resist and the thickness of the resist is constrained by the minimum necessary to to survive the etch step and/or to adequately liftoff deposited materials. For example, in the case of material liftoff the rule of thumb is that the resist should be at least three times the final film thickness. The thickness must be even greater if the goal is to create a small gap in the deposited material. Focused ion beam lithography is also a useful tool when the material to be removed is not susceptible to reactive ion etching. Materials like gold, silver, and platinum fall in this category. It is for this combination of reasons that I chose to use focused ion beam lithography to produce the narrow gaps in the earlier discussed plasmonically enhanced field emission devices.

Having established the usefulness of focused ion beam lithography, particularly for the plasmonic structures in the later part of this work, there are several practical considerations. During this work, I used a Carl Zeiss Orion Nanofab with helium, neon, and gallium source capabilities. Focused ion beam technology has been an industry tool for more than 20 years. Gallium ion beam lithography is used to edit photomasks, cross-section finished devices, and thin samples for transmission electron microscopy. Gallium liquid metal sources produce ion emission from a heated liquid gallium metal surface under an applied electromagnetic field. In the past decade, gas field ion sources have come to commercial prominence. In the case of the Orion Nanofab, a noble gas is injected near an atomically sharp tip with a large applied electromagnetic field to produce ion current through field ionization

(*Orion Nanofab Product Specification* n.d.). The ionized atoms are directed and focused using electromagnetic optics to the sample where they sputter material. The sharp tip creates a point source for ions and allows smaller beam sizes than possible from liquid metal ion sources used in gallium FIB.

An excellent study of the comparative benefits of helium, neon, and gallium ion beam etching is found in Tan, Livengood, Shima, Notte, and McVey (Tan et al., 2010). In that study, the authors point out that two extremely important parameters for focused ion milling are sputter yield and subsurface damage. Sputter yield is defined as

$$\frac{\text{Number of sputtered atoms}}{\text{Number of incident ions}}$$

and depends on the accelerating voltage and ion species. Sputter yield scales as ion mass with light ions like helium having sputter yields of .1 atoms/ion on silicon substrates, heavier neon atoms having sputter yields of 1 atoms/ion on silicon substrate, and gallium having sputter yields of 2 atoms/ion on silicon substrates. Sputter yield determines the dose clear a given feature. Subsurface damage occurs whenever the ion beam is rastered over an object to be imaged or patterned. The incident ion beam can amorphize the substrate and can introduce vacancies that can damage electrical properties. Highly mobile gas ions can even create nanoscale bubbles inside the substrate with diameters ranging from 1-2nm to 20nm. The penetrating depth of the incident ions depends strongly on ion mass. Light ions can penetrate very far into the substrate, and in the case of helium up to 100 nm at modest voltages of 5 keV. Heavier ions penetrate to shallower depths. My initial attempts to produce the nanogap feature in the plasmonically enhanced were using the helium ion beam to achieve the smallest beam focus. Unfortunately, the low sputter yield combined with deep subsurface damage resulted in significant pattern defects due to helium beam induced swelling. This phenomena is on display in images of a helium beam dose array on a substrate consisting of 30nm SiO_2/Si produced for our plasmonically enhanced field emitters (see 7.1). The discoloration of the metal near the lines as well as the taper of the lines near the ends is indicative of silicon swelling. In cross-section in 7.2 , the higher doses clearly show swelling induced mis-alignment. The increased subsurface damage of helium FIB is compounded by the lower sputter yield, making higher doses necessary. Helium induced swelling ultimately prevented me from using helium FIB patterning to fabricate the nanogap in the plasmonically enhanced field emitting structure. Moving to neon FIB patterning immediately increased the sputter yield, reducing the dosage to .015 nC/um @ 10

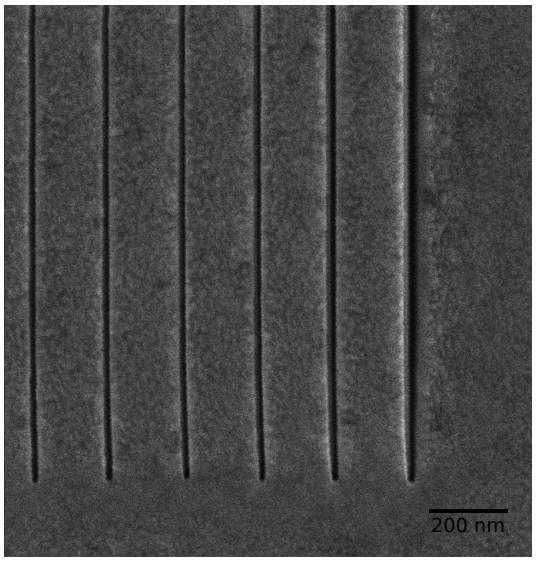

Figure 7.1: Dose array with helium ion FIB.

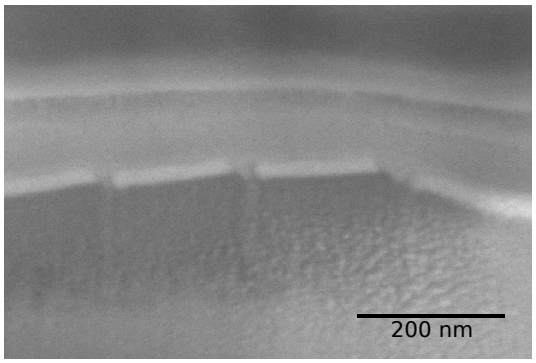

Figure 7.2: Dose array with helium ion FIB.

keV acceleration voltage, and decreased the subsurface damage because of smaller dose and lower substrate penetration. By limiting the acceleration voltage of neon atoms to 10 keV, I hope to limit the implant depth to the silicon dioxide layer directly underneath the removed portion of the metal. This damaged oxide is then removed with a dilute hydroflouric acid solution. This prevents the damaged oxide from causing premature dielectric breakdown between the gold emitter/collector layer and the doped silicon gating layer.

A challenge presented by neon focused ion beam milling arises from the fact that neon has two isotopes of significant abundance. ^{20}Ne accounts for 90.5% of the isotopic composition in air while ^{22}Ne accounts for 9.3% (Laeter et al., 2003). Both ions are therefore present in the feed gas supplied to the gas field ion source and the electromagnetic optics of the Orion Nanofab subsequently focuses each isotope to

a different spot in the x-y plane. This means that Neon FIB single pass lines are comprised of a primary line and an offset line as shown in 7.4. The double line is shown in cross-section in Work done by Matt Sullivan (Kavli Nanoscience Institute

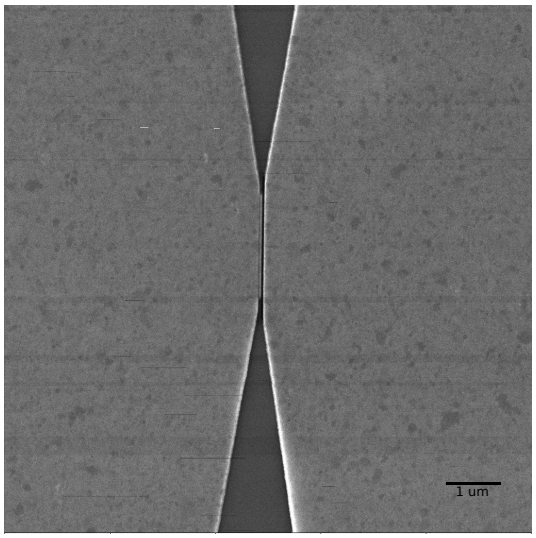

Figure 7.3: Nanoscale gap produced by neon focused ion beam milling. The single pass line has a primary and secondary line due to the high abundance of ^{22}Ne.

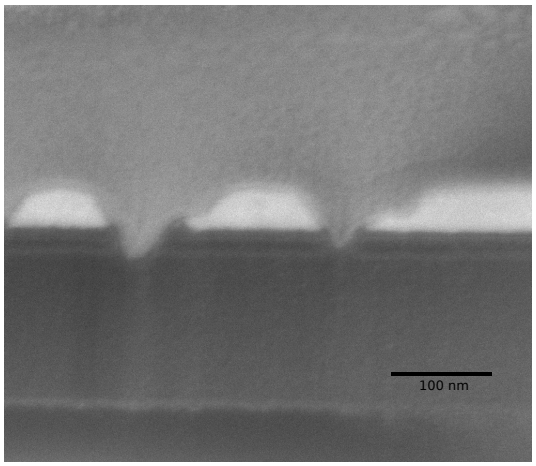

Figure 7.4: Cross-section of nanoscale gap produced by neon focused ion beam milling. The single pass line has a primary and secondary line due to the high abundance of ^{22}Ne.

Staff) and Steven Wood (Kavli Nanoscience Institute SURF student) identified the machine specific angle that the secondary beam makes relative to the primary beam as 41 degrees (Wood, Hunt, and Painter, 2017). This is demonstrated by drawing a circle using the neon focused ion beam. The two beams will converge at some absolute angle (and the mirror opposite location) shown in 7.5. For isolated single

pass lines, as in the plasmonically enhanced field emitting structure from before, we can avoid the second beam artifact by aligning the cut-line with the convergence angle, in this case 41 degrees. A final concern is redeposition of milled material and

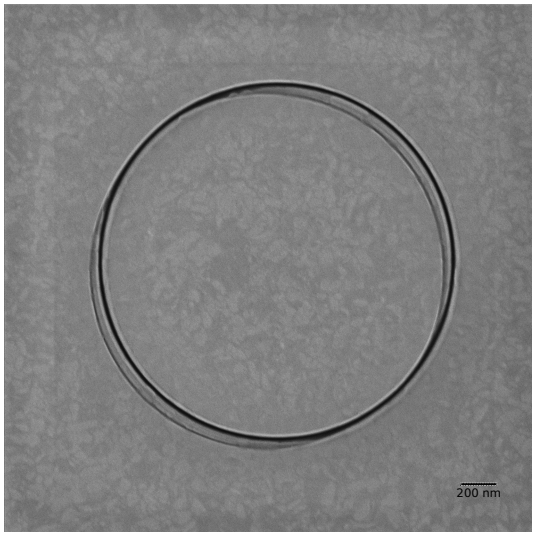

Figure 7.5: Image identifying the angle and position offset of two neon beams in the Orion Nanofab in the Kavli Nanoscience Institute. Courtesy of Steven Wood, Matt Sullivan, and Oskar Painter

surface contaminants. Carbon in the chamber or on the sample can be redeposited on the surface of a milled feature. This often occurs near points where the beam executes a turn, since the beam effectively dwells in the area for a longer than usual time. The problem can be mitigated by cleaning the sample in oxygen plasma before focused ion beam, or failing that, minimizing the number of turns needed to generate the desired pattern.

7.2 Electromigration in Thin Metals

Metals are a promising candidate for use in nanoscale field emission for a number of reasons. They have higher numbers of conducting electrons than semiconductors so field emission in metals isn't supply limited. Generally speaking, metals exhibit improved thermal conduction which should lessen the possibility of tip degradation from overheating. And finally, noble metals in particular may serve as good field emitters and collectors because of their lack of native oxides though they have relatively high work functions (Au has a work function of 4.3 eV as does Ag) (Ashcroft and Mermin, 2005). Despite these advantages, we have found that thin metal films are challenging as field emitters because of electromigration induced failure. In this process conducting electrons transfer momentum during collisions

with metal ions. At high current densities this momentum transfer is enough to push metal ions along the length of the wire creating voids where the metal ion previously was and hillocks where the metal ions motion is arrested. Void formation further concentrates current at that point, leading to more electromigration which exacerbates the problem in a vicious cycle until the wire is destroyed by joule heating (Lienig, 2013). Crystalline materials, like the doped silicon used for our multilayered field emitters don't experience electromigration, which was a primary reason we initially went with these materials. Additionally, because current density is higher at grain boundaries metal ions there exhibit more susceptibility to electromigration.

The narrow gaps in field emission devices combined with the high fields and the the thin, amorphous nature of the films deposited, make metallic field emission devices particularly prone to failure via electromigration. A prime example is shown in Figures 7.6 and 7.7. Through hard-won experience, there are several strategies one can pursue to reduce electromigration induced failure. The most successful is to induce a modest undercut like the one shown in 5.5. Then electromigration doesn't necessarily short the emitter to the collector. A second strategy is to use metallic layers that are as thick as possible to mitigate the effect of Joule heating. The challenge for that strategy is to produce narrow gaps, which necessitates careful choice of the material system and fabrication procedure.

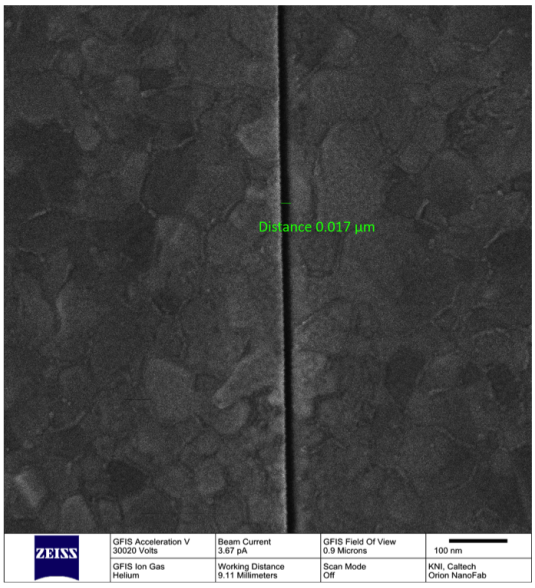

Figure 7.6: Nanoscale gap produced by helium focused ion beam milling before electrical testing.

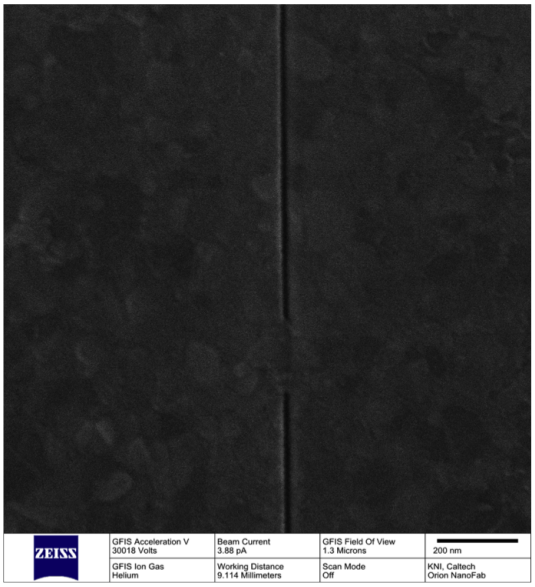

Figure 7.7: Electromigrated nanoscale gap after electromigration induced shorting.

7.3 Photomask Production and Use

A useful technique in the rapid prototyping common in research labs is the production of custom photomasks. Electron beam lithography using high beam currents allows same-day, high quality photomask production. I have produced countless photomasks for use in defining metal contact pads, oxide etch regions, and other large features. To produce these photomasks, we use the following procedure to electron beam pattern the chrome masks and then transfer the pattern to the chrome layer:

- Clean chrome mask in solvent (acetone/IPA/Remove PG) for 5 minutes.
- Spin coat MAN 2403 on oxidized side (colored red) of chrome mask. Spin parameters are 5s/30s at 500 rpm/3000 rpm. Acceleration 100rpm/s / 1000 rpm/s.
- Dose 275 uC/cm^2 with resolution 25 nm.
- Beam current > 50 nA acceptable.
- Develop for 90" in MF-319.
- Water rinse, including spraying the sample with water for at least 10 seconds. This is to completely remove the significant amount of unexposed resist. Dry with nitrogen.

- Remove unmasked chrome in bath of CR-7S. It should take 5-7 minutes to clear un-masked areas.
- Rinse with water and dry with nitrogen.
- Clean resist mask in solven (acetone/IPA/Remove PG) for 5 minutes.

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