Localization and Stimulation Techniques for Implantable Medical Electronics

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To my family and my new family

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ABSTRACT

Implantable medical devices (IMDs) are emerging as one of the keystones of tomorrow's medical technology. Although they have enabled a revolution in medicine, from research to diagnosis to treatment, most of today's devices have critical limitations. They are bulky, have low resolution, and, in some cases, are limited to basic functionality. Miniaturization of IMDs will have an enormous impact not only on the technology itself and the medical procedures they enable, but also on the lives of patients, who will be more comfortable, have greater confidence in their medical treatments, and enjoy an overall improvement in their quality of life. The path towards miniaturized bioelectronic devices requires a reevaluation of existing paradigms to reach a seamless integration of electronics and biology. Miniaturization of medical electronics then involves an exploration of advanced integrated circuit processes and novel circuit and system level architectures. In this dissertation, we provide an overview of implantable medical devices and present novel circuit and system level techniques for the miniaturization of medical electronics.

The function of wireless miniaturized medical devices such as capsule endoscopes, biosensors, and drug delivery systems depends critically on their location inside the body. However, existing electromagnetic, acoustic, and imaging-based methods for localizing and communicating with such devices with spatial selectivity are limited by the physical properties of tissue or imaging modality performance. In the first part of this dissertation, we introduce a new approach for microscale device localization by embodying the principles of nuclear magnetic resonance in a silicon integrated circuit. By analogy to the behavior of nuclear spins, we engineer miniaturized RF transmitters that encode their location in space by shifting their output frequency in proportion to the local magnetic field. The application of external field gradients then allows each device's location to be determined precisely from the frequency of its signal. We demonstrate the core capabilities of these devices, which we call addressable transmitters operated as magnetic spins (ATOMS), in an integrated circuit smaller than 0.7 mm^3, manufactured through a standard 180 nm complementary metal-oxide-semiconductor (CMOS) process. We show that ATOMS are capable of sub-millimeter localization *in vitro* and *in vivo*. As a technology that is inherently robust to tissue properties and scalable to multiple devices, ATOMS localization provides an enabling capability for the development of microscale devices to monitor and treat disease.

In neuroprosthetics, retinal prostheses aim to restore vision in patients suffering from advanced stages of retinal degeneration (e.g., retinitis pigmentosa) by bypassing the damaged photoreceptors and directly stimulating the remaining healthy neurons. In the second part of this dissertation, we describe a fully intraocular self-calibrating epiretinal prosthesis that reduces area and power consumption, and increases the functionality and resolution of traditional implementations. We introduce a novel novel digital calibration technique that matches the biphasic stimulation currents of each channel independently while sharing the calibration circuitry among every 4 channels. The system-on-chip presents dual-band telemetry for power and data with on-chip rectifier and clock recovery. These techniques reduce the number of off-chip components and achieve a power conversion efficiency >80% and supporting data rates up to 20 Mb/s. The system occupies an area of 4.5×3.1 mm^2 and is implemented in 65 nm CMOS . It features 512 independent channels with a pixel size of 0.0169 mm^2 and arbitrary waveform generation per channel. The chip is integrated with flexible MEMS origami coils and parylene substrate to provide a fully intraocular implant.

PUBLISHED CONTENT AND CONTRIBUTIONS

[1] M. Monge and A. Emami, "Design considerations for high-density fully intraocular epiretinal prostheses," in *IEEE 2014 Biomedical Circuits and Systems Conference, BioCAS 2014 - Proceedings*, 2014, pp. 224–227, ISBN: 9781479923465. DOI: 10.1109/BioCAS.2014.6981703,
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M.M. participated in the conception of the project, was the lead designer of the system-on-chip, designed the stimulator array, performed system integration, performed all the experiments, analyzed the data and simulations, and co-wrote the manuscript.

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M.M. participated in the conception of the project, was the lead designer of the system-on-chip, designed the stimulator array, performed system integration, performed all the experiments, analyzed the data, and co-wrote the manuscript.

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Chapter 1

INTRODUCTION

It can be said that in December 1959 a new field emerged, a field whose incredible results have defined us over the last years, and yet is still in its beginning. *"Manipulating and controlling things on a small scale,"* as Richard Feynman would say, or Nanotechnology, as it has become known, has its roots in Feynman's plenary talk *"Plenty of Room at the Bottom."* In this talk, Feynman offered a vision of exploring the *"unknown world of the small,"* which led to numerous and fascinating applications. He also envisioned how patients would eventually *"swallow the surgeon,"* paving the path for small medical robots to diagnose and treat diseases from inside the body, addressing localized malfunction in neurological disorders, cardiovascular diseases, autoimmune disorders, cancer, and other diseases [1]–[5].

A few years after Feynman's speech in 1965, Gordon Moore presented his seminal paper [6] predicting an increase in the number of components per integrated circuit by a factor of two every year — which he modified in 1975 to double the number of transistors in an IC every two years — driven by miniaturization. The impact of what is now know as Moore's Law can be seen in any aspect of our society, including biology and medicine. Since then, the field of electronics for biology and medicine — bioelectronics — has produced remarkable advances ranging from visual prostheses to powerful imaging modalities such as magnetic resonance imaging (MRI), which have evolved to be widely used in medical-device technology. An example of this symbiosis can be seen in the evolution of pacemaker technology. As shown in Figure 1.1, miniaturization of technology has enabled the development of advanced devices, from external pacemakers in 1958 to smaller implantable devices in the following years. The latest generation device (2013) features a size of 0.8 cc, a mass of 1.75 g, and a transcatheter delivery system that enables implantation using minimally invasive surgery through the vasculature.

1.1 Implantable Medical Devices and Miniaturization of Medical Electronics

Implantable medical devices (IMDs) are emerging as one of the keystones of tomorrow's medical technology. Applications of these devices involve deep-brain stimulators for treatment of several neurological conditions such as Parkinson's disease or chronic pain, neural interfaces for recording and monitoring of brain activity,

Figure 1.1: Evolution of pacemaker technology (images courtesy of Medtronics).

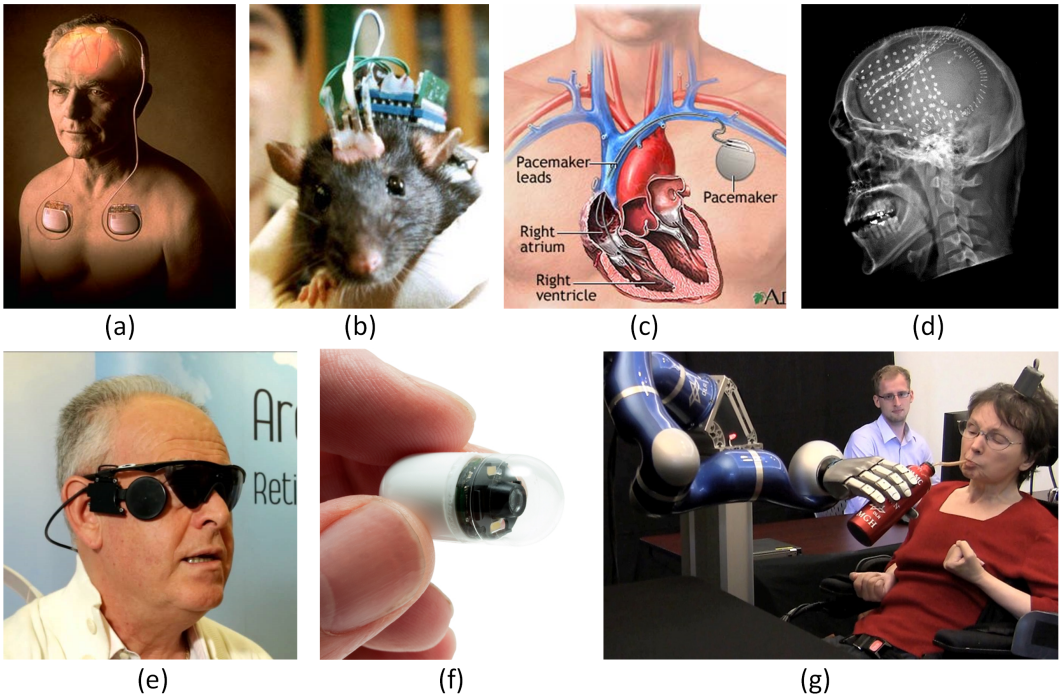


Figure 1.2: Biomedical applications of Implantable Medical Electronics. (a) Deep-Brain Stimulation, (b) Neural Interfaces, (c) Pacemakers, (d) ECoG, (e) Retinal Prostheses, (f) Capsule Endoscopy, (g) Motor prostheses.

cardiac pacemakers to regulate the heart's beating, prosthetics for the visual, hearing and motor impaired, capsule endoscopy for recording images of the gastrointestinal tract, and others (Figure 1.2).

The system architecture of a general IMD consists of three main layers: sensing and actuation layer, electronics layer, and energy harvesting layer (Figure 1.3). The sensing and actuation layer comprises transducers capable of acquiring biological information and/or manipulating biological media. Sensing technologies include

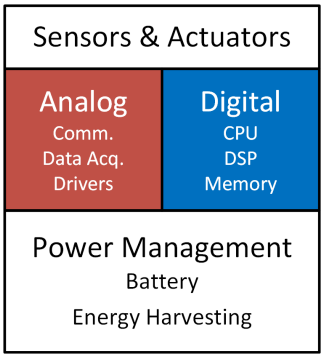


Figure 1.3: System architecture of Implantable Medical Devices.

electrochemical sensors with on-chip electrodes [7] or external electrodes or micro-electrode arrays [8], [9], photoluminescence-based sensors [10], [11], magnetic-based sensors [12], and micro-cameras for video recording [3], [4]. Actuation technologies include electrical stimulation [13]–[16], optogenetics [17], light emission [18], drug delivery [1], [2], and surgical procedures [5], [19]. The electronics layer includes all the circuit and systems required for interfacing with adjacent layers (sensing and actuation, and energy harvesting) as well as for signal processing, data storage, and communication [20]. The energy harvesting layer extracts and transforms energy from available or supplied sources ranging from radio-frequency (RF) [7], [21], [22] to ultrasound [23], [24] to chemical [25]. In recent years, power transfer to IMDs has increased relevance by trying to solve the problem of powering even smaller devices efficiently, with current solutions explained in [22], [26]–[28].

Although IMDs have enabled a revolution in medicine, from research to diagnosis to treatment, most of today's available devices have critical limitations. They are bulky, heavy, have low resolution, and, in some cases, are limited to basic functionality. Miniaturization of these devices will have an enormous impact not only on the technology itself and the medical procedures they enable, but also on the lives of patients, who will be more comfortable, have greater confidence in their medical treatments, and enjoy an overall improvement in their quality of life. Thus, miniaturization will continue to lead the efforts for future medical devices and this trend can be observed in the state-of-the-art (Figure 1.4). Such implants are evolving from low-resolution systems with big external components to high-resolution fully implantable devices.

The path towards miniaturized bioelectronic devices requires a reevaluation of existing paradigms to reach a seamless integration of electronics and biology. Thus,

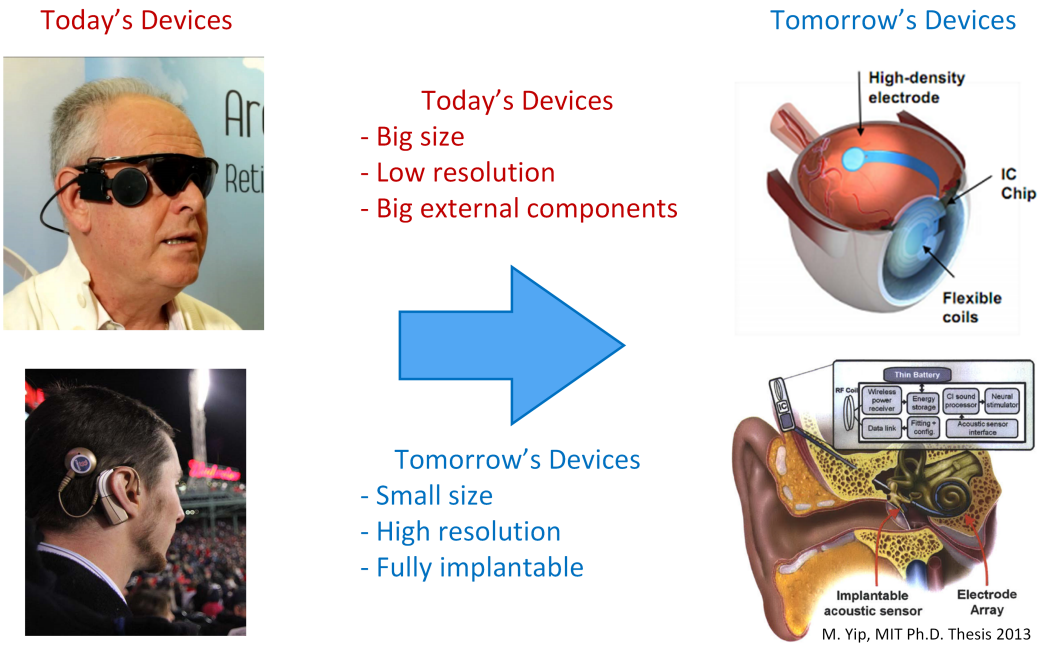


Figure 1.4: Future medical implants.

the miniaturization of medical electronics involves an exploration of advanced integrated circuit (IC) processes and the hybrid integration of ICs with new materials, micro-electro-mechanical systems (MEMS) technology, and biological and chemical sensors and actuators. The transition to nanometer processes leverages all the benefits of scaling in the digital domain but imposes new constraints for the design of analog circuits, such as lower supply voltages, lower intrinsic gain, and higher process variation [29], in applications that require a low-power solution in a small form-factor. Figure 1.5 shows the implications of technology scaling for medical electronics. Through a span of 48 years, IC technology has moved from analog-dominant to digital-driven processes. Although these highly scaled technologies improve significantly the capabilities for signal processing and data storage, biology is analog by nature[1] and requires analog interfaces. The performance reduction in the analog domain affects dramatically the traditional implementation of signal acquisition systems, as they typically rely on higher supply voltage and intrinsic gain. However, novel circuit techniques that take advantage of the increase speed and small size of transistors are emerging as alternative solutions for the design of IMDs. Some examples of such techniques include digitally assisted analog circuits, self-healing systems, time-based analog design, and 3D integration [30].

[1] At scales larger than quantum mechanics.

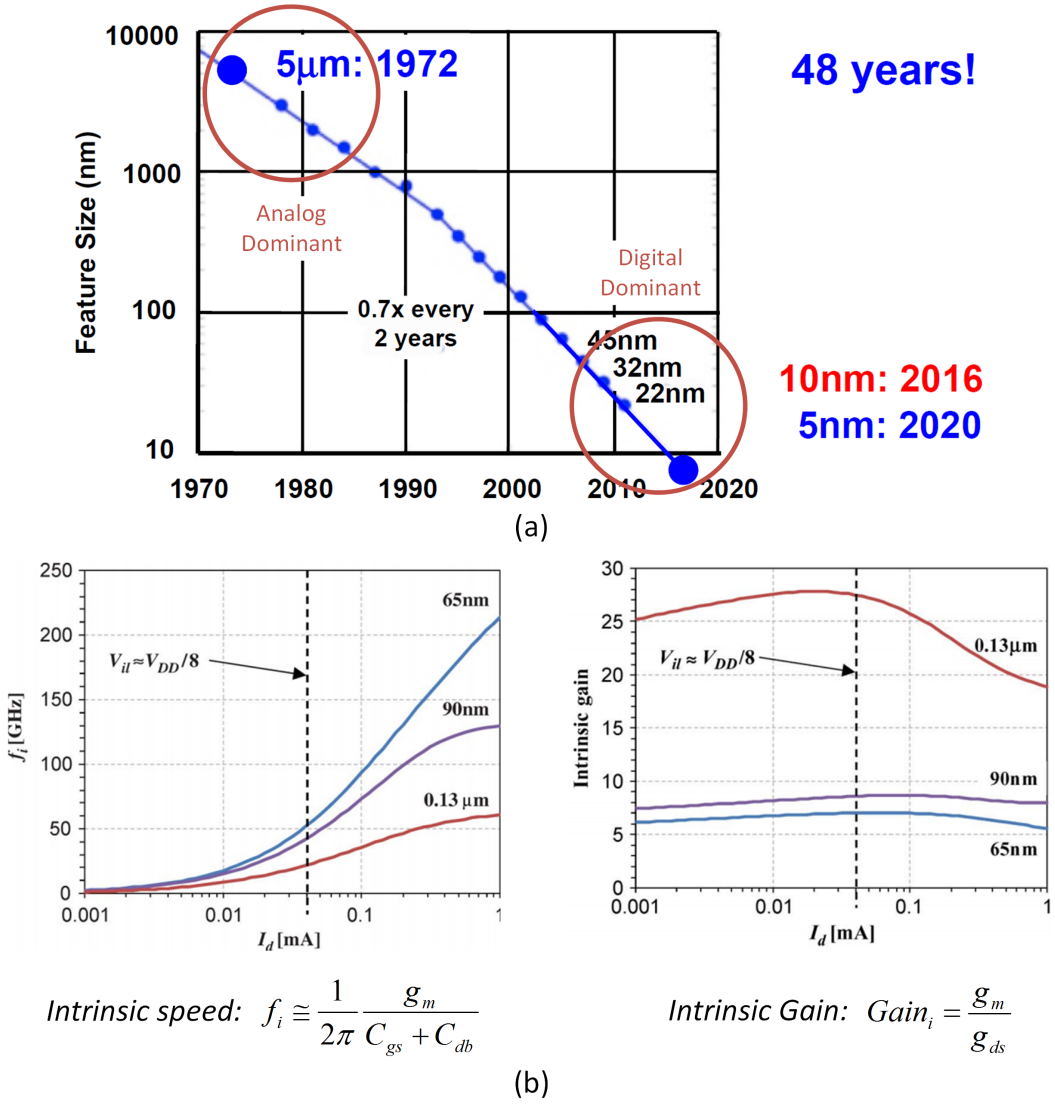


Figure 1.5: Technology scaling and implications. (a) Moore's law showing initial analog dominant and current digital dominant processes (modified from [30]). (b) Effects of scaling in analog circuit design (modified from [29]).

1.2 Stimulation of Biological Media

Stimulation of biological tissue dates back to the first explorations of electrical stimulation in the 18th century. As mentioned in [31], [32], LeRoy created sensations of light by passing electrical currents through the head, Wesley showed electric shock-induced pain relief, and Galvani demonstrated muscle contraction in the legs of dead frogs via electrical stimulation. Significant advances over the past two centuries have shown not only the versatility of electrical stimulation but also its potential to restore biological functions as electrical stimulators have evolved to

be highly complex bioelectronic systems. Table 1.1 shows the most important milestones achieved using electrical stimulation. Some of the current applications include visual prosthesis, cochlear prosthesis, motor prosthesis, pacemaker for the heart, and deep-brain stimulation for treatment of epilepsy and Parkinson's disease.

Today's devices are exploring new methods to improve upon recent achievements of electrical stimulator technology. At the interface between electronics and biology, new materials, fabrication processes, and surgical techniques are being studied to improve placement of electrodes, increase electrode density, reduce the impedance of the electrode-tissue interface, and prolong chronic implantation [9], [31], [33]–[35]. Alternative actuation methods using light are also being explored, including: thermal, mechanical, chemical, and biological responses to photons for use in surgery and therapy [10]. Application of optogenetics to neural implants is also being studied, and current efforts include the development of optoprobes and implantable photonic and optoelectronic devices [10], [17]. Future approaches for actuation of biological media for therapeutic purposes in the context of stimulation include: genetically engineered acoustic protein nanostructures for molecular targeting using ultrasound [36], neural activity control using orthogonal pharmacogenetics [37], ultrasound control of tunable thermal bioswitches [38], and electronic control of gene expression and cell behavior via redox signaling [39].

In this thesis, we explore novel techniques in the electronics for high-density low-power neural stimulators targeting a fully intraocular retinal prosthesis. In addition, our approaches and results can be easily extended to other applications of electrical stimulation for future high-resolution neural interfaces such as high-density close-loop cortical interfaces [8], [9], [40], [41] and brain-spine interfaces [42].

Stimulation purpose	Organ/area	Author
Light sensations	Head	LeRoy
Pain treatment	Head/Neck/Eye	Wesley
Muscle contractions	Leg	Galvani
Organ movement	Brain	Fritsch
Movement and sensation	Brain	Penfield and Boldrey
Understanding membrane physics	Axon/Nerve	Hodgkin and Huxley
Cardiac pacing	Heart	Zoll 1952
Hearing	Cochlea	Djourno and Eyries
Vision	Visual Cortex	Brindley and Lewin

Table 1.1: Milestones in Electrical Stimulation through history (from [31], [32]).

1.3 Localization of Implantable Devices

The miniaturization of medical devices has enabled the development of new approaches to the diagnosis and treatment of human diseases [1], [5]. For instance, smart pills are being used to image the gastrointestinal tract [3], [4], [19], distributed sensors are being developed to map the function of the brain [24], [43], and microscale robots are being designed to access organs through the bloodstream [44]. Although substantial progress has been made in endowing microscale devices with the capability of sensing their environment, performing biopsies, and releasing drugs [1], [2], [19], [45], a major challenge remains in the way these devices communicate with the outside world.

Existing technologies are limited in their ability to precisely determine the location of microscale devices inside the body and communicate with them in a location-specific manner. For example, current techniques based on RF signals [2], [46]–[50] are limited in their resolution and ability to localize multiple devices due to the strong dependence of signal propagation on tissue properties and the necessary close proximity of RF receivers to the implant. Meanwhile, approaches based on direct detection of magnetic fields generated by devices bearing permanent magnets or coils have limited detection range [46], involve millimeter-sized architectures [51]–[58], and have not been applied at the microscale. Alternatively, device imaging using methods such as X-ray computed tomography [59]–[61], positron emission tomography [62], magnetic resonance imaging (MRI) [46], [62]–[64] and ultrasound [2], [46], [62], [65]–[68] are limited by the properties of each modality – such as the presence of background contrast or the use of ionizing radiation – and provide limited opportunity for information transfer to and from the device.

Here, we present an alternative approach to microscale device localization based on concepts from nuclear magnetic resonance. Specifically, the magnetic field-dependent precession frequency of nuclear spins allows their location in space to be encoded through the application of magnetic field gradients. This allows MRI to visualize signals from nuclear spins located throughout a specimen with $\sim$100 μm resolution. We hypothesized that by designing microscale devices whose output frequency could shift with the magnetic field, they too could be localized, read out and controlled with MRI-like precision. Details on the design, implementation, and measurements are discussed in chapters 3, 4, and 5.

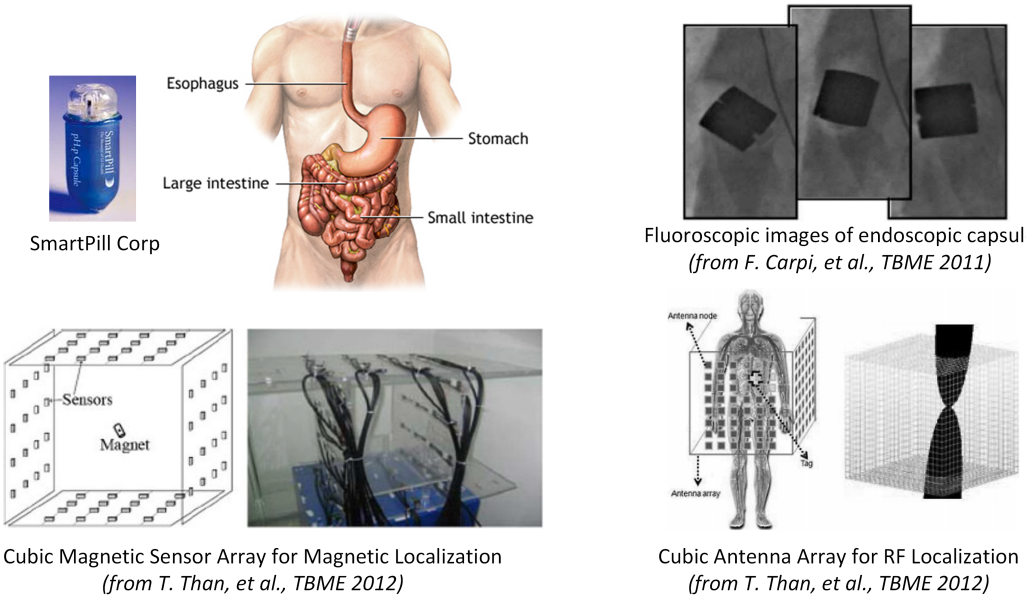


Figure 1.6: Current methods for localization of devices inside the body, showing magnetic, RF, and X-ray based methods.

1.4 Contributions

In this dissertation, we propose novel techniques for the miniaturization of implantable medical electronics while improving system performance in two important pillars: localization of medical devices and electrical stimulation.

In localization, we introduce a new approach for microscale device location by embodying the principles of nuclear magnetic resonance in an integrated circuit. By analogy to the behavior of nuclear spins, we engineer miniaturized RF transmitters that can encode their location in space by shifting their output frequency in proportion to the local magnetic field. The application of external magnetic fields then allows each device's location to be determined precisely from the frequency of its signal, similar to pulse sequences in MRI. We call this technology Addressable Transmitters Operated as Magnetic Spins (ATOMS). In addition, ATOMS technology decouples the dependence of RF methods from body composition and time-sensitive parameters such as time-of-arrival and received-signal-strength. As a result, it combines the benefits of frequency encoding using magnetic field gradients with those of highly sensitive RF receivers. We demonstrate the core capabilities of these devices in an integrated circuit smaller than 0.7 mm^3, implemented in 180 nm CMOS, achieving sub-millimeter localization resolution *in vitro* and *in vivo*.

In stimulation, we present a fully intraocular high-density self-calibrating epiretinal

prosthesis that minimizes the area of the integrated circuit and reduces the number of off-chip components. The system-on-chip features dual-band telemetry for power and data, on-chip rectifier, and clock recovery, and a 512-channel stimulator array in an area of 4.5×3.1 mm^2. By using circuit techniques such as dynamic biasing, stacking, and sharing, we implement a neural stimulator with high output voltage compliance and self-calibration with state-of-the-art performance in a highly scaled low-voltage process. We introduce a novel robust digital calibration technique that matches biphasic currents with minimal area overhead, ensuring charge-balance stimulation. We demonstrate a fully intraocular system achieving a pixel size of 0.0169 mm^2 and arbitrary waveform generation per channel in 65 nm CMOS. The chip is integrated with flexible MEMS origami coils and parylene substrate to provide a fully intraocular implant.

1.5 Organization

This thesis is organized as follows. Chapter 2 provides a review of important concepts related to this work. The basics of MRI are introduced, as well as performance metrics of oscillators such as phase noise and jitter. The behavior of RF signals in the human body and the electrode-electrolyte interface are also discussed.

Chapter 3 introduces the concept of ATOMS as a novel technique for the localization of microscale devices inside the body. A brief overview of existing methods is also discussed. The theoretical analysis of ATOMS technology is presented and discussed, including future scenarios ranging from phase encoding to 3D localization schemes. The design and implementation of our prototype device is described in Chapter 4. Concepts and design insights are discussed, covering several aspects of the electronic design space: from sensing of magnetic fields and signal conditioning to mixed-signal and RF interface elements to logic design. Analysis, modeling, and simulation results are given. Chapter 5 presents the measurement results of the fabricated ATOMS chip including electrical characterization and localization experiments. An *in vivo* model using a small mouse shows a localization resolution of less than 500 μm on a device smaller than 0.7 mm^3 and consuming an average power of less than 340 μW.

We move from localization to stimulation, to discuss a fully intraocular epiretinal prosthesis in Chapter 6. The concept of a retinal prosthesis and its progress over recent years are presented. Details of the overall system architecture are shown, including previous calibration methods applied to neural stimulators. The chapter

concludes showing measurement results in an *in vitro* scenario. Chapter 7 presents design challenges of the electronics considering the biology of the eye and discusses new approaches for future high-density fully intraocular prostheses.

Conclusions of the work and future directions are given in Chapter 8.

Chapter 2

BACKGROUND

In this chapter, we discuss the key concepts upon which this work has been developed. We start with a quick review of the basics of nuclear magnetic resonance and MRI, which are the fundamental concepts of ATOMS technology. Then, we take a look at the nature of the frequency instabilities in oscillators by describing phase noise and jitter, which play an important role in the resolution of ATOMS. We conclude the chapter by discussing the modeling of the electrode-electrolyte interface in neural stimulators.

2.1 Basics of Magnetic Resonance Imaging

MRI, one of the most successful imaging medical technologies of recent years, allows us to *see* the inside of the living organisms with great detail while using non-ionizing radiation. It is vastly used in research and diagnosis, with applications including neuroimaging, soft tissue imaging, musculoskeletal imaging, brain activity studies, biomarker imaging, and cancer studies, among others. Figure 2.1 illustrates the fundamentals of MRI. We observe a patient inside an MRI scanner, which comprises three main magnetic fields: the strong polarizing magnetic field B_0 generated by a super-conductive magnet, the excitation RF field B_1 generated by an RF coil, and the magnetic field gradients (G_X, G_Y, and G_Z) generated by gradient coils. Zooming-in to the target area, all three magnetic fields interact with nuclei according to the principle of magnetic resonance (which is explained below), exciting them. Then, we measure their responses. As an example, two nuclear spins at two different locations transmit two different signals based on the applied field gradient. After scanning the entire anatomical region and gathering all the data, an image can be formed in which both nuclear spins are *visualized* according to their anatomical locations.

Particles possess a spin that characterizes them. Individual unpaired protons, neutrons and electrons are spin-1/2 particles. For example, in the deuterium atom ^{2}H, with one proton, one neutron, and one electron, the total electronic spin is 1/2 and the total nuclear spin is 1 [69]. In the case of the hydrogen atom ^{1}H, the total electronic spin is 1/2 and the total nuclear spin is 1/2. For our discussion of nuclear magnetic resonance, we use the hydrogen atom (or proton) as a study case.

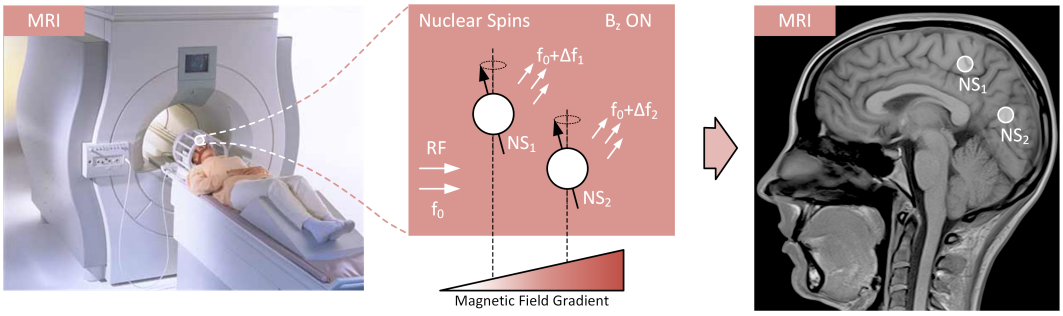


Figure 2.1: Illustration of Magnetic Resonance Imaging.

Since ^{1}H has a spin and a positive charge, its constant spinning produces a magnetic moment which makes the proton behave like a very tiny magnet. When these nuclei are placed inside a magnetic field B_0, they start precessing. This spontaneous behavior occurs even with weak magnetic fields such as the Earth's magnetic field. The precessing frequency is known as the *Larmor frequency* [70] and is defined as

$$\omega = 2\pi\nu = \gamma B_0\,, \tag{2.1}$$

where γ is the gyromagnetic ratio of the nuclei. Table 2.1 shows the gyromagnetic ratios of selective nuclei. There are two possible spin states for a proton when it is inside a magnetic field. Known as the *Zeeman splitting* (Figure 2.2), the energy difference between the two states is proportional to the applied magnetic field B_0 [70] and defined as

$$\Delta E = \hbar\nu = \hbar\gamma B_0\,. \tag{2.2}$$

Nuclei	Net Spin	Gyromagnetic ratio γ (MHz/T)
^{1}H	1/2	42.58
^{2}H	1	6.54
^{13}C	1/2	10.71
^{14}N	1	3.08
^{15}N	1/2	-4.31
^{17}O	5/2	-5.77
^{19}F	1/2	40.08
^{31}P	1/2	17.25
^{23}Na	3/2	11.27
^{129}Xe	1/2	-7.441
electron	1/2	28024.95

Table 2.1: Net spin and gyromagnetic ratio of nuclei (from [69], [70]).

An interesting property of nuclei in a magnetic field is that they can absorb a photon of frequency ν. A particle can then transition from the lower energy state to the higher energy state by absorbing an RF photon whose frequency provides the exact amount of energy needed for the transition (the energy difference between the two states) [69], [70]. Figure 2.3 illustrates the original nuclear magnetic resonance (NMR) experiments consisting of a *continuous wave* RF experiment. In one of the experiments, the absorbed energy is measured while the magnetic field B_0 is swept, keeping constant the frequency of the RF signal. Since the RF is fixed, the energy of the signal is also fixed. By changing the magnetic field, the energy of the signal is moved from left to right at a constant height as shown in Figure 2.3a. In the other experiment, the magnetic field is kept constant and the frequency of the RF signal is swept. The energy of the RF signal increases as the frequency increases, and it is represented as a bigger and darker line in Figure 2.3b. In both cases, the absorbed energy reaches a maximum when the energy of the RF signal is equal to the difference between energy states. This condition is called *resonance*, and gives the name to NMR.

Let's discuss now the process of interacting with nuclear spins and the localization mechanism. Consider an ensemble of nuclei as shown in Figure 2.4a. The spins are randomly oriented, producing a zero net magnetization. When a polarizing magnetic field B_0 is applied, they start precessing at f_0 and align with B_0, producing a net magnetization M. Then, by applying an RF signal at the resonance or Larmor frequency f_0, nuclei absorb this energy and the net magnetization of the ensemble M starts rotating. The angle of the rotation depends on the duration of the RF pulse. When the excitation RF pulse ends, nuclei start relaxing, emitting a signal at the same frequency f_0 until they return to the resting state. This signal is known as the free induction decay (FID). This interactive process is shown in Figure 2.4b. To enable localization, a magnetic field gradient is applied after the RF pulse to expose nuclei at different locations to different magnetic fields, changing the frequency of their FID. The location information encoded in the oscillation frequency or frequency shift is then used to map the location of nuclei back in space (Figure 2.4c).

Moving to three dimensions, MRI uses pulse sequences that involve slice selection, phase encoding, and frequency encoding to image the target area of a patient. Figure 2.5 illustrates a simple pulse sequence for 3D imaging. Slice selection is achieved by sending a *soft* RF pulse and applying the field gradient G_Z simultaneously to *selectively* excite only the nuclei from the target 2D slice. Phase encoding is then

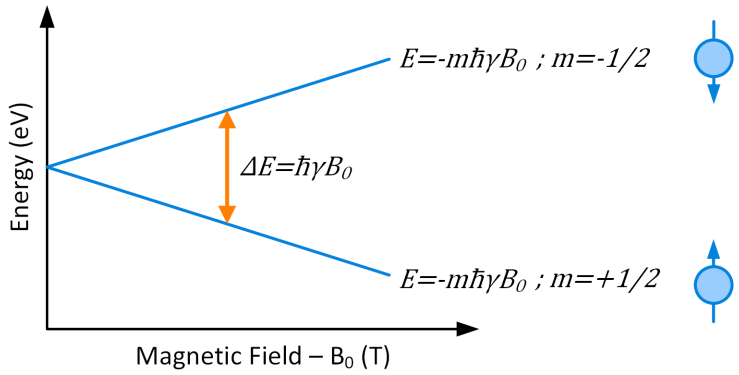


Figure 2.2: Energy levels of spin-1/2 particles in a magnetic field (modified from [69]).

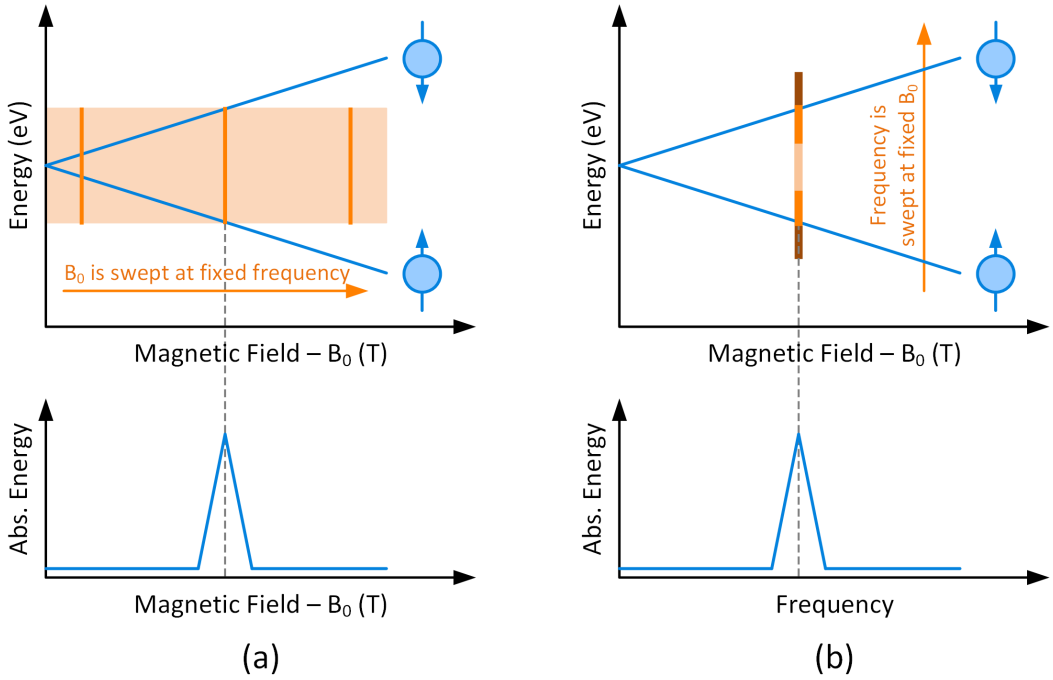


Figure 2.3: Illustration of the original NMR experiments using a CW RF signal. (a) With a fixed frequency, the magnetic field is swept while measuring the absorbed energy. The orange line represents the energy of the signal changing from left to rigth. (b) With a fixed magnetic field, the frequency is swept while measuring the absorbed energy. The orange line represents the energy of the signal changing from small (clear) to big (dark). In both cases, when the energy is equal to the difference between energy states, the absorbed energy reaches a maximum (modified from [69]).

achieved by applying the field gradient G_Y to temporarily change the precessing frequency and *dephase* nuclei at different locations. Finally, the field gradient G_X

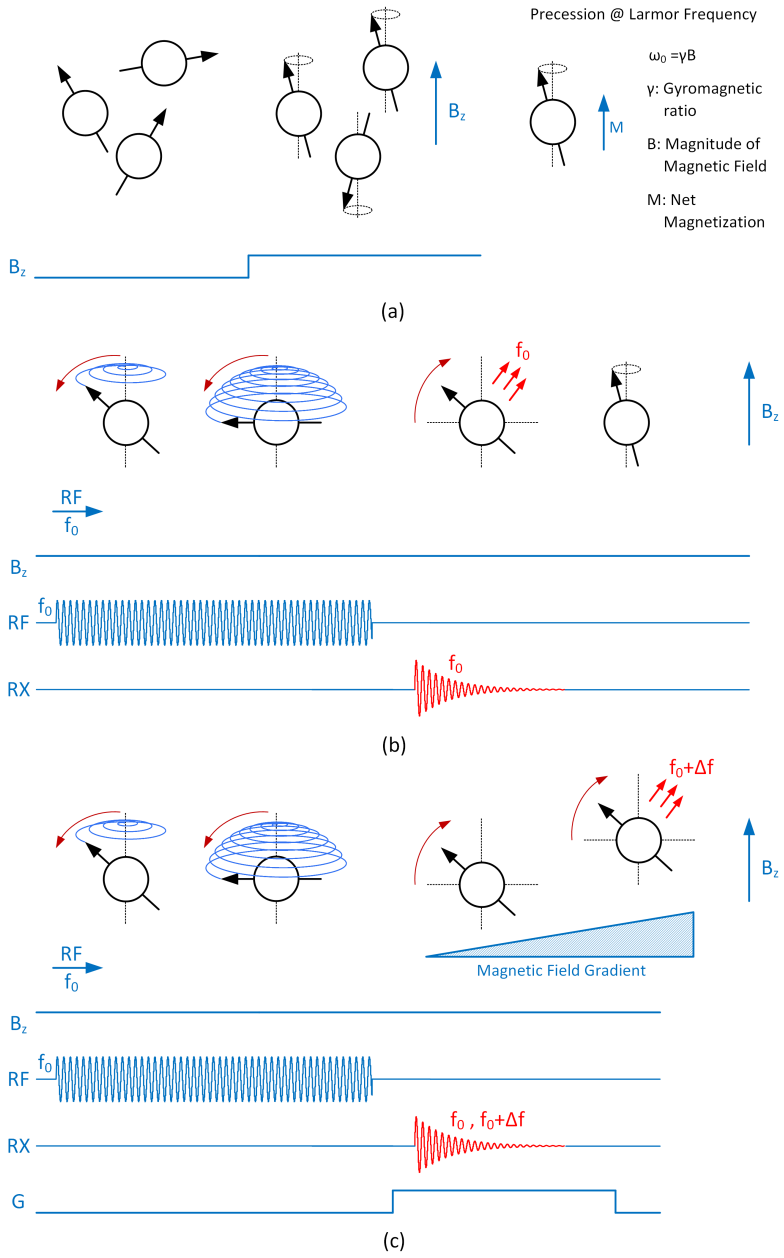


Figure 2.4: (a) Randomly oriented nuclei aligned to the applied magnetic field B_0. (b) When an RF field B_1 at the resonance frequency (Larmor frequency) is applied, nuclei absorb this energy, and the net magnetization starts rotating. When the RF field stops, nuclei start relaxing, rotating back to the resting state along B_0. (c) If a gradient field is applied after RF excitation, nuclei at different locations will radiate back signals with distinctively different frequencies proportinal to the total magnetic field at their locations. These frequency shifts are then used to map their location back into space.

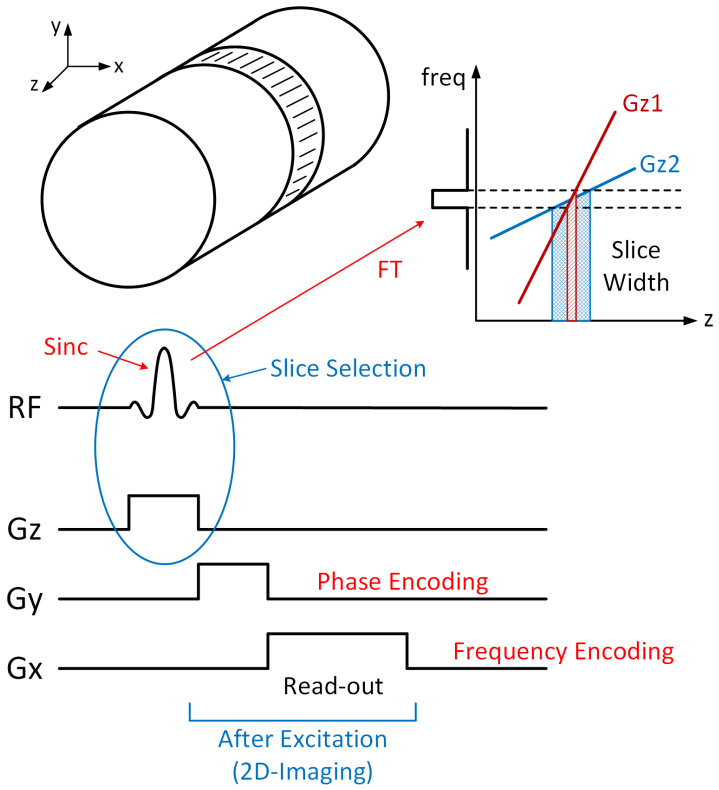


Figure 2.5: Illustration of a MRI pulse sequence for 3D imaging.

is applied during read-out to achieve frequency encoding.

2.2 Phase Noise and Jitter in Oscillators

Phase Noise

Phase noise represents the short term instabilities of an oscillator in the frequency domain and is typically described in terms of the single sideband noise spectral density at a frequency offset f_{offset} from the center frequency as shown in Figure 2.6 [71]. It is defined by

$$\mathcal{L}(f_{\text{offset}}) = 10\log\left[\frac{P_{\text{sideband}}(f_0 + f_{\text{offset}},\ 1\text{Hz})}{P_{\text{carrier}}}\right], \tag{2.3}$$

where $P_{\text{sideband}}(f_0 + f_{\text{offset}},\ 1\text{Hz})$ is the single sideband power at a frequency offset $\Delta\omega$ from the center frequency in a measuring bandwidth of 1Hz, and P_{carrier} is the total power under the power spectrum. Note that this definition includes both amplitude and phase fluctuations [71]. We observe that the phase noise has different regions. At large frequency offsets, the phase noise is flat, representing the noise floor of the oscillator. As the frequency offset decreases, the phase noise increases. We first

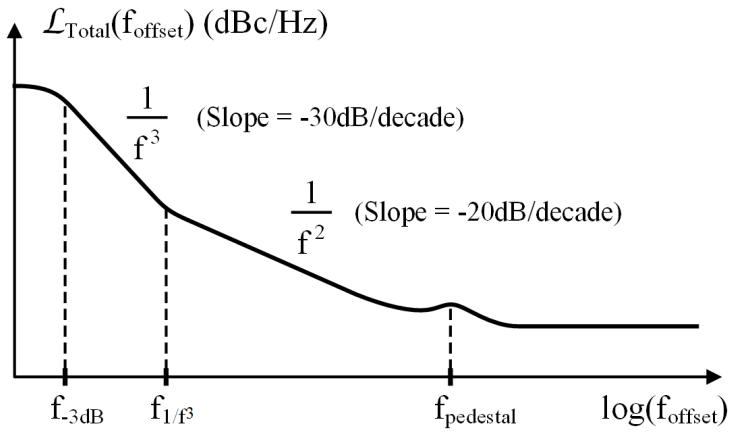


Figure 2.6: Phase noise profile of a typical oscillator [71].

notice a small "bump", which may arise from the effect of amplitude fluctuations. Then, we enter into the $1/f^2$ region that shows a -20 dB/dec slope, which is the result of the up-conversion of thermal (white) noise. At lower offset frequencies, a $1/f^3$ region with -30 dB/dec slope is noticed, which is mainly due to the up-conversion of flicker noise. Close to the center frequency, the phase noise flattens to a maximum value.

When localizing ATOMS devices, it is important to know the in-band noise around the oscillation frequency of any device, specifically the self-generated noise and interference noise to an adjacent device. This is illustrated in Figure 2.7, where the in-band noise of Δf bandwidth is determined around f_0 or between f_1 and f_2 for self-generated and interference noise, respectively.

The in-band noise relative to the carrier is determined as

$$P_{\text{noise}} = \int_{f_{\text{offset}_{\text{min}}}}^{f_{\text{offset}_{\text{max}}}} \mathcal{L}(f_{\text{offset}}) d(f_{\text{offset}}), \tag{2.4}$$

where the integration boundaries for each case are 0 and $\Delta f/2$, and $\Delta f/2$ and $3\Delta f/2$, respectively.

Let's consider initially the contributions due to white noise. In this case, the phase noise can be described as

$$\mathcal{L}(f_{\text{offset}}) = \frac{1}{\pi} \frac{2 f_B}{f_B^2 + f_{\text{offset}}^2}, \tag{2.5}$$

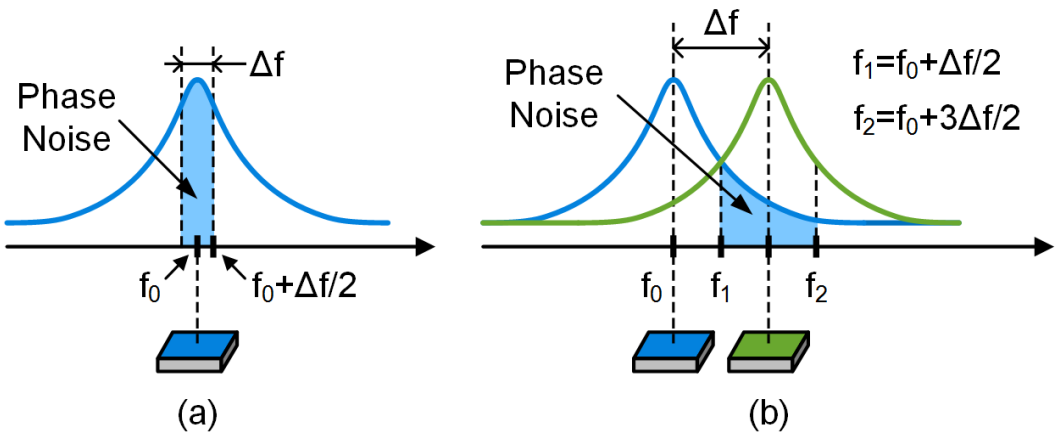


Figure 2.7: Phase noise implications when localizing ATOMS devices. (a) Self-generated noise. (b) Interference noise to adjacent device.

which has a Lorentzian spectrum, where $2f_B$ is the 3-dB bandwidth of the oscillator. In the $1/f^2$ region, the phase noise can be approximated by

$$\mathcal{L}(f_{\text{offset}}) = \frac{c}{f_{\text{offset}}^2}, \tag{2.6}$$

where $c = 2f_B/\pi$ is a proportionality constant.

We can calculate the in-band noise around f_0 as

$$P_{\text{noise}} = \int_0^{\Delta f/2} \frac{c}{(\pi c/2)^2 + f^2} df = \frac{2}{\pi} \tan^{-1}\left(\frac{\Delta f}{\pi c}\right). \tag{2.7}$$

The in-band noise between f_1 and f_2 is calculated as

$$P_{\text{noise}} = \int_{\Delta f/2}^{3\Delta f/2} \frac{c}{f^2} df = \frac{c\,(\Delta f)}{\left(\sqrt{\frac{3\Delta f}{2}\frac{\Delta f}{2}}\right)^2} = \mathcal{L}\left(\frac{\sqrt{3}}{2}\Delta f\right)(\Delta f) \tag{2.8}$$

$$P_{\text{noise}} = P_{\text{PN}}\left(\frac{\sqrt{3}}{2}\Delta f\right)\Delta f\,, \tag{2.9}$$

where $P_{\text{PN}}(\sqrt{3}\Delta f/2)$ or just P_{PN} is the constant phase noise between f_1 and f_2 at a frequency offset $\sqrt{3}\Delta f/2$. The phase noise at a reference frequency offset f_{ref} can then be calculated as

$$P_{\text{PN}}\,(f_{\text{ref}}) = P_{\text{PN}}\left(\frac{\sqrt{3}}{2}\Delta f\right) + 20\log\left(\frac{\sqrt{3}\Delta f/2}{f_{\text{ref}}}\right). \tag{2.10}$$

When considering flicker noise, the phase noise does not follow a Lorentzian spectrum anymore. Different publications have focused on modeling phase noise in this scenario. Herzel [72] decomposes the model into a Lorentzian spectrum for the white noise sources and a Gaussian spectrum for the flicker noise sources. The final spectrum is then the convolution of both spectrums, which is called a Voigt line profile. This profile conserves the overall power of the oscillator and has a finite value at very small frequency offsets. The spectrum follows a Gaussian profile at small offsets when dominated by flicker noise, followed by $1/f^3$ and $1/f^2$ behaviors at larger offsets. In another work, Navid et al.[73] arrive at a similar conclusion, modeling the phase noise as a Voigt line profile, with a Gaussian profile close to the oscillation frequency. Chorti and Brookes [74] model the phase noise using a power-law expression and also find that the phase noise close to the oscillation frequency to can be modeled as a Gaussian when dominated by flicker noise.

To calculate the phase noise in the presence of flicker noise, the expressions developed in [72]–[74] need to be evaluated numerically. However, when calculating the phase noise around the oscillation frequency, we can use the oscillator bandwidth as a measure of phase noise. If the dominant noise source is flicker noise, the phase noise profile $S_\phi(\omega)$ can be approximated by a Gaussian profile and its standard deviation can be estimated from its 3-dB bandwidth by $\sigma_{\mathrm{PN}} \approx BW_{S_\phi,3dB}/2.355$.

Timing Jitter

Timing jitter represents the uncertainties in the transition instants of a periodic signal [71]. In electronics, random jitter is the result of the noise inherent to any electrical device and typically exhibits a Gaussian distribution. This is because random jitter is the result of the aggregate effect of many uncorrelated noise sources (central limit theorem).

For a free-running oscillator, the jitter increases with the time delay between the reference and the measurement interval τ, as shown in Figure 2.8. The region with a slope of 1/2 corresponds to uncertainties caused by white noise, while the region with a slope of 1 corresponds to uncertainties due to both white noise and the additional effect of flicker noise at longer τ. The increment in variance occurs because any variation in an earlier transition affects all subsequent transitions, persisting indefinitely [71]. Therefore, the uncertainty in the transition after τ seconds includes the cumulative effect of all transitions. This is known as *jitter accumulation* and it is shown in Figure 2.9.

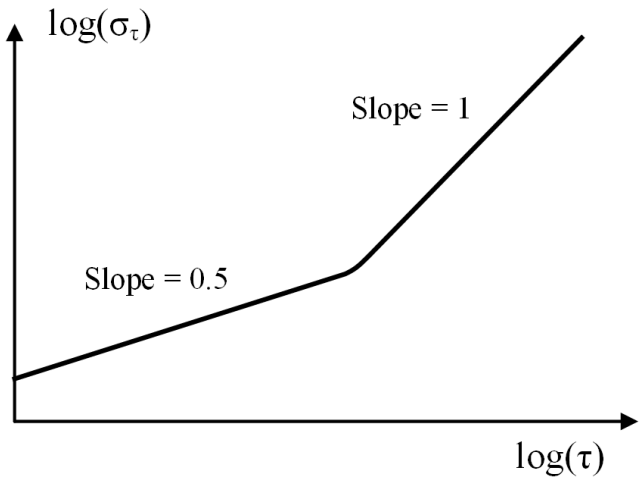


Figure 2.8: Timing jitter profile of a typical oscillator (modified from [71]).

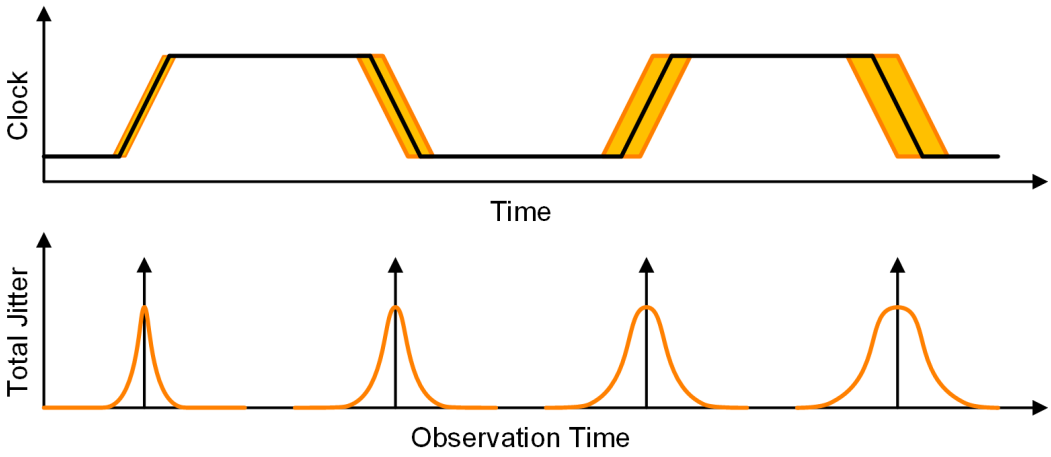


Figure 2.9: Illustration of *jitter accumulation* (modified from [71]).

The standard deviation of the jitter after τ seconds can be expressed as

$$\sigma_\tau = \kappa\sqrt{\tau}\,, \text{ in the region with slope = 1/2} \tag{2.11}$$

$$\sigma_\tau = \zeta\tau\,, \text{ in the region with slope = 1}\,, \tag{2.12}$$

where κ and ζ are proportionality constants determined by circuit parameters [71].

It is useful to relate timing jitter to phase noise. This relationship can be obtained by noticing that jitter is the standard deviation of the timing uncertainty. As shown in [71], jitter and phase noise relate to each other according to the following expression:

$$\sigma_\tau^2 = \frac{4}{\pi\omega_0^2}\int_0^\infty S_\phi(\omega)\sin^2\left(\frac{\omega\tau}{2}\right)d\omega\,, \tag{2.13}$$

where $S_\phi(\omega)$ is the phase noise profile.

In the case where phase noise is dominated by white noise ($1/f^2$ region), κ can be calculated from phase noise by

$$\kappa = \left(\frac{f_{\text{offset}}}{f_0}\right) 10^{\mathcal{L}(f_{\text{offset}})/20}, \tag{2.14}$$

where $\mathcal{L}(f_{\text{offset}})$ is the phase noise at a frequency offset f_{offset} and f_0 is the oscillation frequency.

As we will discuss in the next chapter, phase noise and timing jitter directly affect the resolution of ATOMS when frequency encoding or phase encoding are used because they determine the minimum detectable frequency shift Δf_{min} and phase shift $\Delta\phi_{\text{min}}$, respectively.

2.3 Electrode-Electrolyte Interface

When a metal (electrode) is introduced in a solution (electrolyte), a redistribution of charges occurs at the interface involving ions, electrons, dipoles, and neutral molecules. Similar to the well-known Metal-Oxide-Semiconductor (MOS) structure, a potential is formed between both phases (metal and liquid) due to charge redistribution, creating a *double layer* at the interface. The accumulation and distribution of charges vary with the distance from the electrode surface due to the interaction of different forces and thermal fields [75], as shown in Figure 2.10.

We observe three main regions in the electrolyte side: a compact layer, a diffusive layer, and the bulk solution (Stern Model). Near the surface of the electrode, ions are considered to be immobilized, forming the Helmholtz layer. After this layer, ions are diffusely spread-out across the Gouy-Chapman layer (diffusive layer) according to electrical and thermal fields following Maxwell-Boltzmann statistics [75]. The bulk solution, as its name suggests, is the region that shows the original charge distribution of the solution before electrode insertion. The *double layer* is then modeled as a capacitor C_{DL} following the expression

$$\frac{1}{C_{DL}} = \frac{1}{C_H} + \frac{1}{C_G}, \tag{2.15}$$

where C_H and C_G are the capacitances of the Helmholtz and Gouy-Chapman layers. More information about the Helmholtz model, Gouy-Chapman model, and Stern model can be found in [75], [76] and in electrochemistry literature.

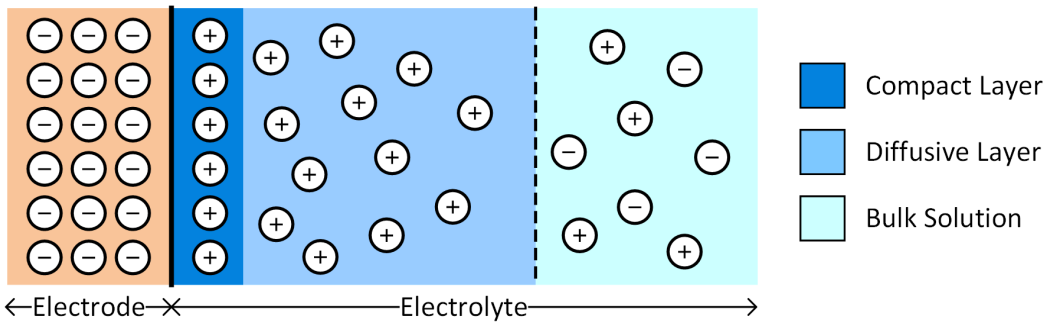


Figure 2.10: Illustration of the electrode-electrolyte interface, showing the different accumulation regions in the solution.

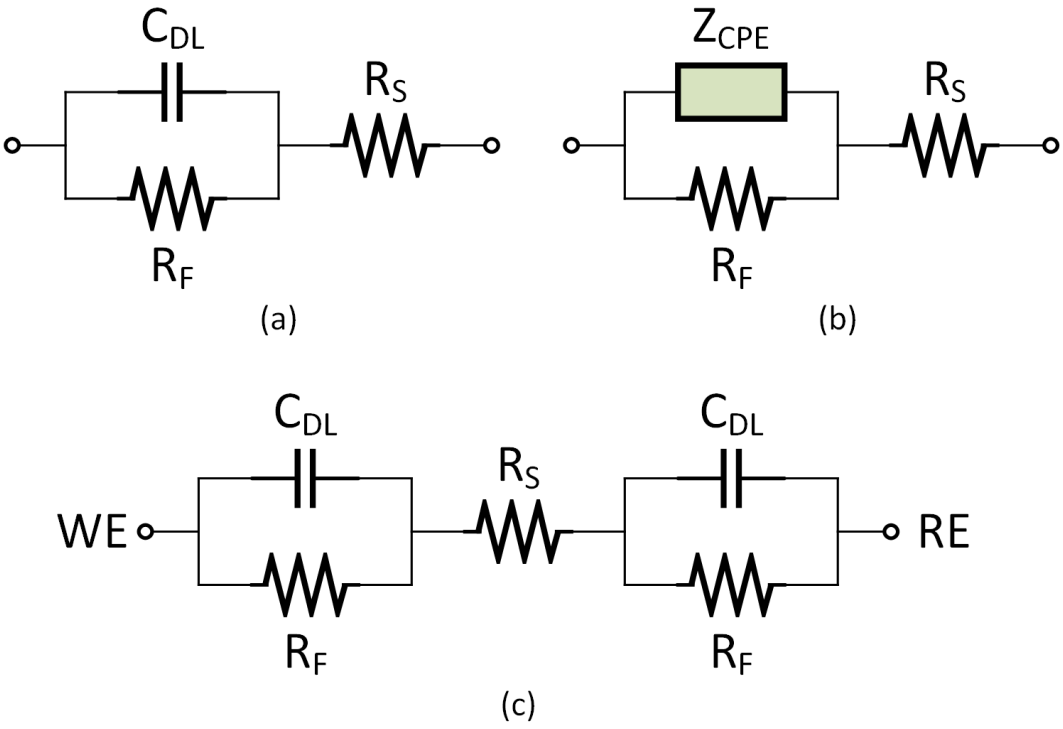


Figure 2.11: Simplified electrical model of the electrode-electrolyte interface. (a) Electrical model. (b) Constant-phase element (CPE) replaces the double-layer capacitor to model the interface when the electrode is roughened. (c) Simplified electrical model of two electrodes (working and counter electrodes) in a solution.

The electrode-electrolyte interface can be electrically modeled using the three-element model shown in Figure 2.11, a-b [77]. In stimulation, charge injection can take place via charging and discharging of the *double layer* or through electrochemical reactions across the interface. The first injection mechanism is modeled by

the double-layer capacitance C_{DL} and the second by the faradaic resistor R_F [77]–[79]. The electrolyte is modeled by the series resistance R_S. When the electrode is roughened [77], [80], a constant phase element (CPE), which represents an R-C network, replaces the parallel capacitor to model the roughness. The CPE has an impedance of $Z_{CPE} = Y_0(j\omega)^{-n}$, where a value of n close to 1 indicates that the CPE is primarily capacitive, and a value of n close to 0 indicates the CPE is primarily resistive. Figure 2.11 shows the electrical model of two electrodes (working and counter electrode) in a solution. In the epiretinal prosthesis developed in this thesis, the counter electrode provides a large surface area, and can be modeled solely as a capacitor [79]. Additionally, since the value of this capacitance is large (in comparison with the working electrode), its impedance is very small and can be neglected. As a result, the simplified model reduces to the electrical model shown in Figure 2.11a.

Chapter 3

LOCALIZATION OF MICROSCALE DEVICES USING ADDRESSABLE TRANSMITTERS OPERATED AS MAGNETIC SPINS

The function of wireless miniaturized medical devices such as capsule endoscopes, biosensors, and drug delivery systems depends critically on their location inside the body. However, existing electromagnetic, acoustic, and imaging-based methods for localizing and communicating with such devices with spatial selectivity are limited by the physical properties of tissue or imaging modality performance. Here, we introduce a new approach for microscale device localization by embodying the principles of nuclear magnetic resonance in a silicon integrated circuit. By analogy to the behavior of nuclear spins, we engineer miniaturized RF transmitters that encode their location in space by shifting their output frequency in proportion to the local magnetic field. The application of external field gradients then allows each device's location to be determined precisely from the frequency of its signal. Because these devices operate analogously to magnetic spins, we call this technology Addressable Transmitters Operated as Magnetic Spins (ATOMS).

3.1 Localization of devices inside the body

Current methods are unable to precisely determine the location of microscale devices inside the body and communicate with them in a location-specific manner. Existing techniques based on radio-frequency (RF) interactions are limited in their ability to localize and communicate with individual implants [2], [46]–[50]. The strong dependence of RF signals on tissue properties (i.e., body composition) and the proximity of RF receivers to the implant drastically reduce the spatial resolution of these methods and their capacity to interface with multiple devices at once. This is because they rely on time-sensitive parameters such as time-of-arrival, time-of-flight or received-signal-strength. Arrays of multiple sensors have also been used but they require sub-nanosecond synchronization. The best reported resolution in the literature is limited to ~5 mm using *a priori* knowledge of body composition by means of a full-body MRI or CT-scan.

On the other hand, magnetic approaches have desirable features such as very low attenuation through and low dependence on human tissue [51], non-line-of-sight

detection [81], and good accuracy [57], [58], [82], [83]. Current methods show resolutions of few millimeters or even sub-millimeter. However, available magnetic techniques have limited coverage [46], have typically used millimeter-sized permanent magnets and coils [51]–[58], and have not been studied for microscale devices.

Imaging methods such as magnetic resonance imaging (MRI) [63], [64] and ultrasound [65], [66] have also been used for localization. Even though MRI techniques could enable high accuracy tracking of medical devices, the need for a full MRI scanner and custom-programmed pulse sequences elevates the cost and complexity of the system [46], [62]. Although ultrasound techniques provide high speed, safety and low cost [2], [67], they are limited to soft tissue and their implementation could be challenging due to possible acoustic impedance mismatches [46], [62], [68].

Localization using other imaging procedures such as X-ray computed tomography (CT-scan) [59]–[61] or positron emission technology [62] expose patients to ionizing radiation and can only visualize and not transmit information to and from devices at specific locations in the body.

3.2 ATOMS concept

MRI measures signals from ensembles of nuclear spins, each of which can be thought of as an atom-sized transmitter resonating at a magnetic field-dependent frequency. The operating principle of MRI discussed in Section 2.1 is summarized in Figure 3.1. When a polarizing magnetic field (B_0) is applied, randomly oriented nuclear spins align to B_0 and start precessing at a known frequency f_0 (Larmor frequency). They are excited by an RF signal at their resonance frequency (f_0) and start rotating. When the excitation is removed, the nuclear spins relax and radiate back a signal with a shifted frequency proportional to the applied magnetic field gradient. Using this principle, MRI can distinguish the locations of more than 10^{26} spins in the body with $\sim$ 100 μm precision by encoding the location of nuclei in the frequency at which they absorb and emit signals. A magnetic field gradient is applied such that spins in one location resonate at a predictably different frequency from spins at another location. Applying gradients while receiving signal from the full ensemble of nuclei allows the use of frequency shifts to assign signals to specific locations in space. Conversely, one can excite spins selectively by applying field gradients during frequency-specific transmission.

We reasoned that by creating silicon ATOMS circuits that mimic the behavior of

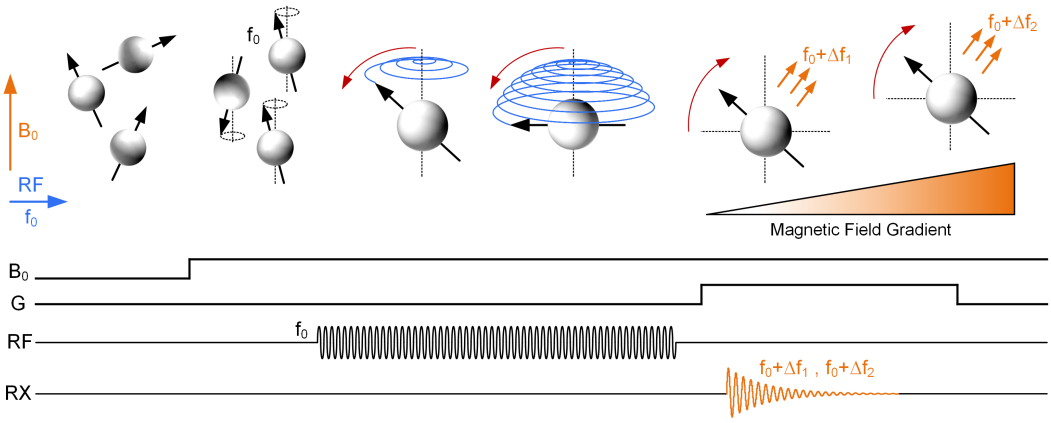


Figure 3.1: Operating principle of MRI. Nuclear spins interact with a polarizing magnetic field B_0 and precess at their Larmor frequency f_0. They absorb and emit energy when an excitation RF signal is pulsed at the same resonance frequency f_0. By applying a magnetic field gradient during radiation, the location of spins are encoded in frequency shifts.

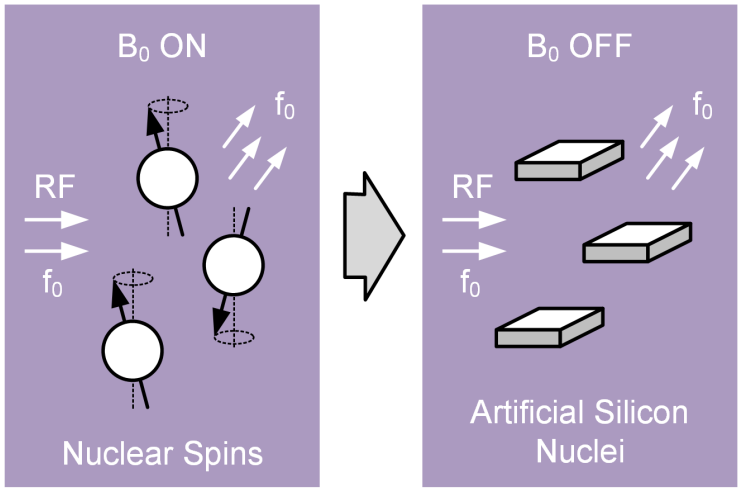


Figure 3.2: Bio-inspired design: Artificial Silicon Nuclei mimic the behavior of nuclear spins in an MRI. It is important to note that B_0 is not required.

nuclear spins, we would be able to localize devices containing such circuits in space using magnetic field gradients (Figure 3.2). This would allow the devices to transmit information or receive commands via RF signals in a spatially specific manner (Figure 3.3). Like nuclear spins in MRI, this approach could allow multiple identical devices at different locations to be addressed in parallel. Importantly, unlike MRI, a strong static polarizing magnetic field is not required, since ATOMS oscillations can be powered by internal or external energy sources. Also, unlike

other RF localization methods, the spatial resolution of this approach would not be limited by RF wavelengths or tissue parameters.

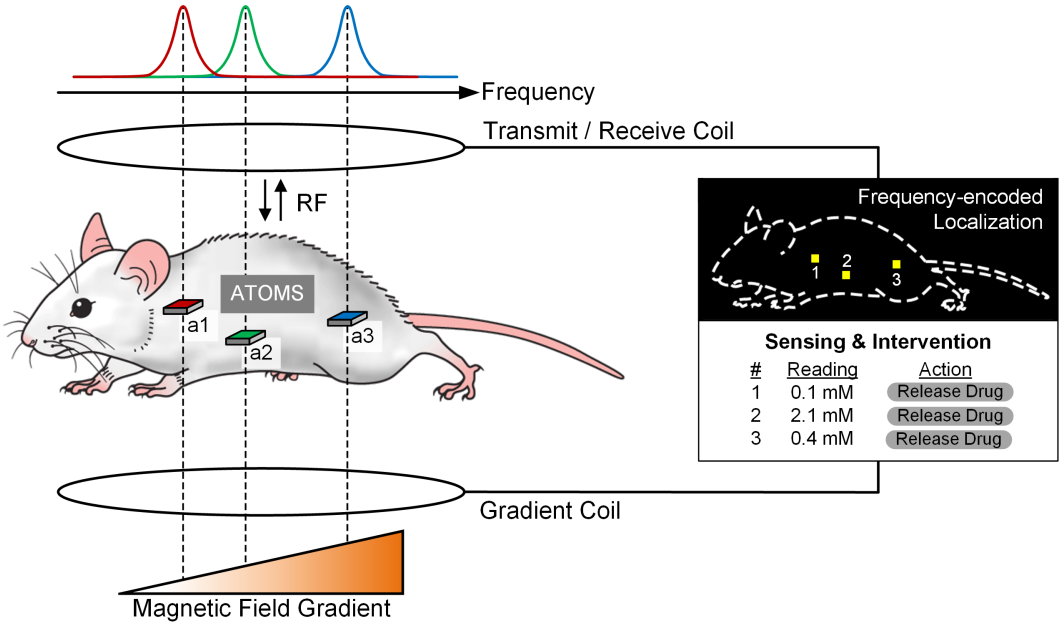


Figure 3.3: ATOMS concept. Addressable Transmitters Operated as Magnetic Spins are microscale devices capable of power harvesting and communication at magnetic field-dependent frequency. When multiple ATOMS are in an animal or a patient, their locations are discerened by applying a magnetic field gradient.

The basic operation of ATOMS consists of three phases: magnetic phase, excitation phase, and transmission phase (Figure 3.4). During the magnetic phase, ATOMS devices sense, process, and store the applied magnetic field at each of their locations. The excitation phase starts when the RF pulse is applied. The frequency of the RF pulse f_0 is acquired and the devices start oscillating at the same frequency. The transmission phase follows, during which each device emits a signal with a shifted frequency proportional to the measured magnetic field.

As a general-purpose platform, ATOMS has the potential to be the enabling technology for *in vivo* monitoring and tracking of biological processes with precise localization. The integration of ATOMS with microscale biological sensing and actuation technologies will enhance the development of a wide range of biomedical applications, from distributed localized monitoring of biologically relevant biomarkers to targeted release of therapeutic agents and tissue imaging for disease diagnosis.

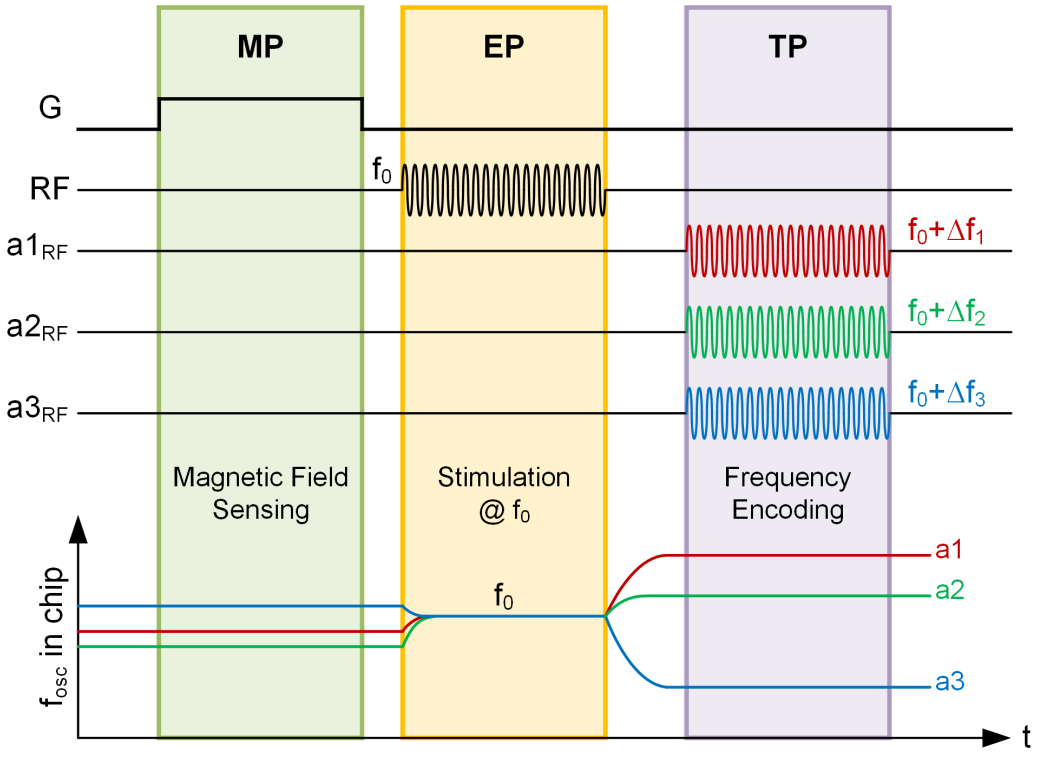


Figure 3.4: Operation of ATOMS devices. During MP, ATOMS sense and store the applied magnetic field at each of their locations prior to excitation. During EP, they acquire the frequency of the excitation RF signal f_0 and start oscillating at the same frequency. During TP, they emit a signal with a shifted frequency proportional to the measured magnetic field. MP, magnetic field sensing phase; EP, excitation phase; TP, transmission phase.

3.3 Theoretical Analysis

ATOMS devices encode their location in the frequency and phase of their emitting signal according to two proportionality constants that reflect the responsivity of the chip. Since these devices are designed analogous to nuclear spins, we name these constants as the gyromagnetic ratios $\gamma_{\text{ATOMS,f}}$ in MHz/T and $\gamma_{\text{ATOMS},\phi}$ in rad/T for frequency and phase, respectively.

Localization

Consider an ATOMS device inside a body in a magnetic field profile **B** as shown in Figure 3.5. For the selected slice, the magnetic field profile orthogonal to the plane $B_Z = g(r, \theta)$ determines the response of the chip. For a fixed $\theta = \theta_0$, the location of ATOMS can be estimated by mapping the magnetic field back in space:

$$\hat{r} = g^{-1}(\hat{B}_Z), \tag{3.1}$$

with

$$\hat{B}_Z = \frac{\Delta f + \Delta f_0}{\gamma_{\text{ATOMS,f}}}, \tag{3.2}$$

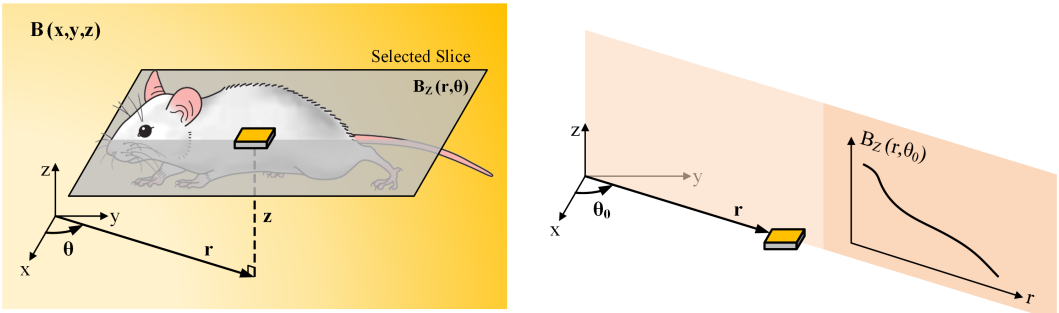


Figure 3.5: Illustration of the localization process for an ATOMS device inside the body of an animal or patient. (a) ATOMS device is located based on the cylindrical coordinates (r, θ, z) using a selected slice at position z. (b) Magnetic field B_Z in the selected slice as a function of r for a given θ_0.

where g^{-1} is the inverse function of B_Z, $\hat{B}_Z$ is the estimated magnetic field at the location of the chip, Δf is the frequency shift, and Δf_0 is the frequency shift offset.

To calculate the spatial resolution Δr for frequency encoding, we first take the derivative of Equation 3.1:

$$\frac{d\hat{r}}{d\hat{B}_Z} = \frac{d}{d\hat{B}_Z}\left(g^{-1}(\hat{B}_Z)\right). \tag{3.3}$$

Using the inverse function theorem, the expression reduces to

$$\frac{d\hat{r}}{d\hat{B}_Z} = \frac{1}{\frac{d}{dr}\left(g(r,\theta_0)\right)} = \frac{1}{G_{Z,\theta_0}}, \tag{3.4}$$

where

$$G_{Z,\theta_0} = \frac{d}{dr}\left(g(r,\theta_0)\right) \tag{3.5}$$

is the magnetic field gradient of B_Z at θ_0.

The spatial resolution is then given by

$$\Delta r = \frac{\Delta f_{\text{min}}}{\gamma_{\text{ATOMS,f}}\, G_{Z,\theta_0}}, \tag{3.6}$$

where we define $\Delta f_{\text{min}} = 2\sigma_f$ as the minimum detectable frequency shift, and σ_f is the standard deviatino of the oscillation frequency.

In the case of a constant magnetic field gradient G_X in one dimension, as used in MRI, the spatial resolution reduces to

$$\Delta x = \frac{\Delta f_{\text{min}}}{\gamma_{\text{ATOMS,f}}\, G_X}. \tag{3.7}$$

Similarly, for phase encoding, the spatial resolution can also be given by

$$\Delta r = \frac{\Delta \phi_{\text{min}}}{\gamma_{\text{ATOMS},\phi}\, G_{Z,\theta_0}}, \tag{3.8}$$

where we define $\Delta\phi_{\text{min}} = 2\sigma_p$ as the minimum detectable phase shift, and σ_p is the standard deviation of the phase. For a constant magnetic field gradient G_Y in one dimension, it reduces to

$$\Delta y = \frac{\Delta \phi_{\text{min}}}{\gamma_{\text{ATOMS},\phi}\, G_Y}. \tag{3.9}$$

Phase Noise and Timing Jitter Analysis

Consider an ATOMS devices that has an oscillator with the phase noise and jitter profiles shown in Figure 3.6. The phase noise and timing jitter of the chip's internal oscillator affect Δf_{min} and $\Delta\phi_{\text{min}}$. As we mentioned in Section 2.2, phase noise represents the oscillator's short term instabilities in the frequency domain and is typically described in terms of the single sideband noise spectral density at a frequency offset f_{offset} from the center frequency [71]. Timing jitter represents the uncertainties in the transition instants of a periodic signal [71]. For a free-running oscillator, the jitter increases with the time delay between the reference and the measurement interval τ, i.e., the reading time t_{TP}. We are going to look into each of these phenomenons below.

Phase Noise in Frequency Encoding

As mentioned before in Section 2.2, the in-band noise around the oscillation frequency of any ATOMS device affects the localization performance. Considering a single device (Figure 3.7), the phase noise of the ATOMS's oscillator broadens the spectral profile and increases the uncertainty region around the center frequency. For an external receiver requiring a specific SNR, the spectral resolution is determined by Δf according to

$$10\log(\text{SNR}) = 10\log(P_{a_1}) - 10\log(P_{\text{noise}}), \tag{3.10}$$

where P_{a_1} is the power of the signal from the device a_1, and P_{noise} is given by

$$P_{\text{noise}} = \int_0^{\Delta f/2} \mathcal{L}(f)df. \tag{3.11}$$

When the dominant noise source is white noise, P_{noise} is equal to Equation 2.7

$$P_{\text{noise}} = \frac{2}{\pi}\tan^{-1}\left(\frac{\Delta f}{\pi c}\right). \tag{3.12}$$

When dominated by flicker noise, P_{noise} needs to be evaluated numerically because $\mathcal{L}(f)$ follows a Voigt line profile [72]–[74]. However, Δf can be simply approximated by considering the oscillator's bandwidth as a measure of phase noise. Since, $S_\phi(\omega)$ can be approximated by a Gaussian profile close to the center frequency, the standard deviation of the frequency σ_f can be approximated by $\sigma_f \approx BW_{S_\phi,3dB}/2.355$.

In the presence of a second ATOMS device at a different location, a difference in the received power of each signal can appeared if, for example, the devices are located at different depths (Figure 3.8) or if the signals are passing through different tissues. This additional noise reduces the SNR of the received signal when the devices are close, where the overlap range is between $f_0 + \Delta f/2$ and $f_0 + 3\Delta f/2$ (i.e., the devices are at different depths and/or the signals are passing through tissues of different composition).

The Δf_{min} required to detect the signal of one ATOMS (a_1) in the presence of another (a_2) can be derived as

$$10\log(\text{SNR}) = 10\log(P_{a_1}) - 10\log(P_{a_2}) - 10\log(P_{\text{noise}}), \tag{3.13}$$

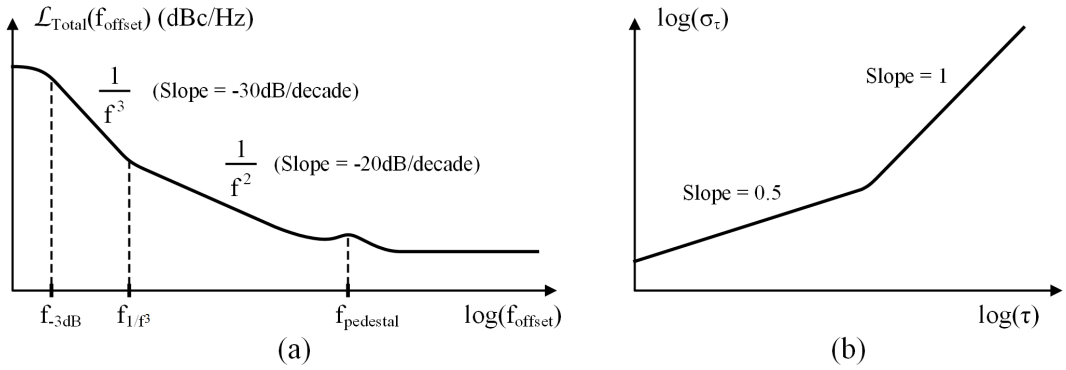


Figure 3.6: (a) Phase noise and (b) timing jitter of a typical oscillator (modified from [71]).

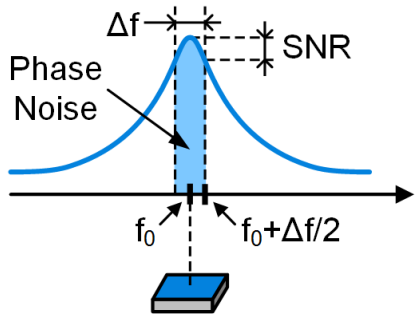


Figure 3.7: Effects of phase noise in frequency uncertainty for a target SNR.

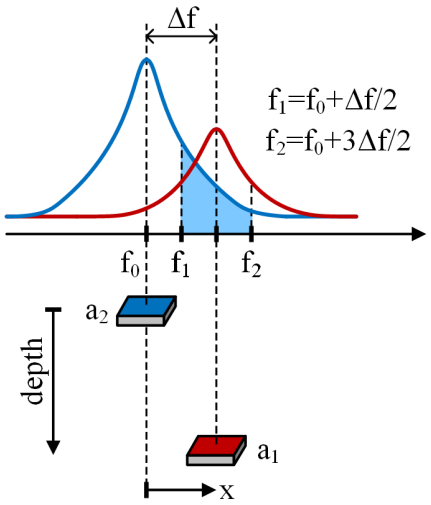


Figure 3.8: Illustration of the effect of two ATOMS devices close to each other at different depths on Δf. The device a_2 acts as an interferer and degrades the SNR of a_1 due to its phase noise in the band between f_1 and f_2.

$$10\log(\text{SNR}) = 10\log\left(\frac{P_{a_1}}{P_{a_2}}\right) - 10\log(P_{noise}), \tag{3.14}$$

where P_{a_1} and P_{a_2} are the power levels of the received signals, SNR is the target signal-to-noise ratio at the receiver, and P_{noise} is given by

$$P_{\text{noise}} = \int_{\Delta f/2}^{3\Delta f/2} \mathcal{L}(f)df. \tag{3.15}$$

Since P_{noise} follows a Voigt line profile, it needs to be evaluated numerically. In addition, time averaging can improve the resolution by increasing the recording time. We define n as the ratio between the reading time t_{TP} and the minimum reading time

$t_{TP_{\min}}$ required at the receiver to detect a signal. Then, Equation 3.14 becomes

$$10\log(P_{\text{noise}}) = 10\log\left(\frac{P_{a_1}}{P_{a_2}}\right) - 10\log(\text{SNR}) + 10\log\left(\sqrt{n}\right). \tag{3.16}$$

If the overlap falls in the $1/f^2$ region, we can replace P_{noise} by Equation 2.9. We obtain

$$10\log(\Delta f_{\min}) = 10\log\left(\frac{P_{a_1}}{P_{a_2}}\right) - 10\log(P_{PN}) - 10\log(\text{SNR}) + 10\log\left(\sqrt{n}\right). \tag{3.17}$$

Equations 3.16 and 3.17 tell us that $\Delta f_{\min}$ depends on the interference level, phase noise of the oscillator, and the characteristics of the external receiver SNR and n.

Timing Jitter in Phase Encoding

For phase encoding, the $\phi_{\min}$ required to distinguish an ATOMS device at two different locations is limited by jitter. We can model the jitter as a normal random variable $\eta \sim \mathcal{N}(0, \sigma_\tau)$, where σ_τ is expressed in radians for frequency f_0.

In the absence of jitter and assuming a sinusoidal waveform - due to the bandwidth of the transmitter and the receiver -, the received signal $r(t)$ is

$$r(t) = Re\left[Ae^{j\Delta\phi(m-1)}e^{j2\pi f_0 t}\right],\ m = 1, 2, ..., M;\ \Delta\phi = 2\pi/M, \tag{3.18}$$

where M is the maximum number of positions for a given $\Delta\phi$.

In the presence of jitter, the received signal is

$$r(t) = Re\left[Ae^{j\Delta\phi(m-1)}e^{j2\pi f_0 t}e^{j\eta}\right],\ m = 1, 2, ..., M;\ \Delta\phi = 2\pi/M, \tag{3.19}$$

$$r(t) = A\cos\left(2\pi f_0 t + \Delta\phi(m-1) + \eta\right)$$

$$r(t) = A\cos(\Delta\phi(m-1) + \eta)\cos(2\pi f_0 t) - A\sin(\Delta\phi(m-1) + \eta)\sin(s\pi f_0 t).$$

For a quadrature receiver, the orthogonal signals used for expansion can be defined as

$$\phi_1(t) = \cos(2\pi f_0 t), \tag{3.20}$$

$$\phi_2(t) = -\sin(2\pi f_0 t). \tag{3.21}$$

Then

$$r(t) = A\cos(\Delta\phi(m-1) + \eta)\phi_1(t) + A\sin(\Delta\phi(m-1) + \eta)\phi_2(t),$$

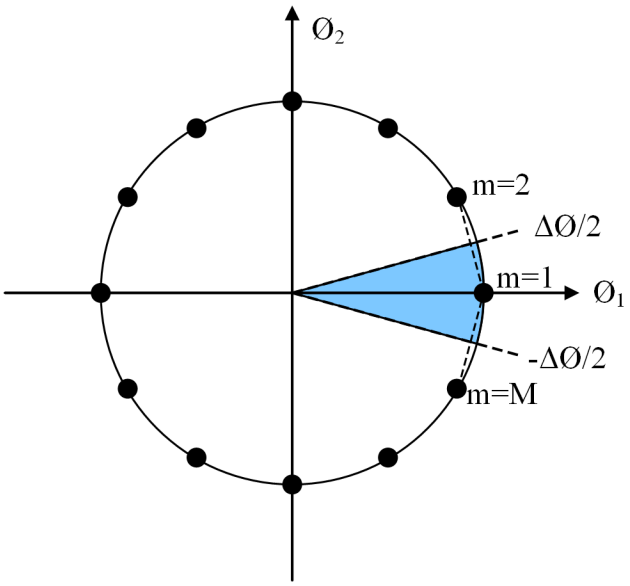


Figure 3.9: Constellation of possible locations using phase encoding. Φ_1 and Φ_2 are the orthogonal signals used for expansion.

and as a vector

$$\mathbf{r} = (A\cos(\Delta\phi(m-1)+\eta),\ A\sin(\Delta\phi(m-1)+\eta)). \tag{3.22}$$

Figure 3.9 shows the constellation of the location encoding using the orthogonal signals described in equations 3.20 and 3.21.

Given the symmetry of the constellation, the error probability of the system can be determined by calculating the case when $m = 1$ [84]:

$$\mathbf{r} = (A\cos\eta,\ A\sin\eta). \tag{3.23}$$

Applying polar transformations

$$V = \sqrt{r_1^2 + r_2^2}$$

$$\Theta = \arctan\left(\frac{r_2}{r_1}\right)$$

we get

$$\mathbf{r}_{v,\theta} = (A,\ \eta). \tag{3.24}$$

The probability density function of Θ is then

$$p_\Theta(\theta) = \frac{1}{\sqrt{2\pi\sigma_\tau^2}} e^{-\frac{\theta^2}{2\sigma_\tau^2}}. \tag{3.25}$$

Therefore, the error probability of the decision region between $-\Delta\phi/2$ and $\Delta\phi/2$ is

$$P_e = P\left(|\theta| > \frac{\Delta\phi}{2}\right) = 1 - \int_{-\Delta\phi/2}^{\Delta\phi/2} p_\theta(\theta)d\theta = 2Q\left(\frac{\Delta\phi}{2\sigma_\tau}\right), \tag{3.26}$$

where Q is the tail probability of the standard normal distribution and σ_τ was defined in equations 2.11 and 2.12, depending on the observation time τ.

The resolution of phase encoding is therefore directly dependent on the jitter, and more importantly jitter accumulation. Several methods have been proposed for reduction of jitter accumulation, most of them can be reviewed in PLL literature. One example that relates directly to biosensors is the work presented in [85]. Here, the effect of noise is minimized by finding the best observation time for minimum normalized accumulated jitter. Another approach is the use of time-multiplexing, where the phase shifted signal is interleaved with a non-phase shifted or reference signal. The use of the reference signal synchronizes the receiver and resets the jitter, in a fashion similar to a multiplying PLL.

Magnetic Sensor Noise

As mentioned before, ATOMS devices measure, digitize and store the applied magnetic field prior to transmission. Thus the measured magnetic field is unchanging during TP, and therefore contributes to neither the phase noise nor the jitter. However, the noise of the magnetic field does affect the estimated localization and reduces the accuracy of the system. For an input referred noise with standard deviation σ_{MS}, the effects of the sensor noise in the frequency and phase shifts are

$$\sigma_{f_{\mathrm{MS}}} = \gamma_{\mathrm{ATOMS,f}}\,\sigma_{\mathrm{MS}}, \tag{3.27}$$

$$\sigma_{\phi_{\mathrm{MS}}} = \gamma_{\mathrm{ATOMS},\phi}\,\sigma_{\mathrm{MS}}, \tag{3.28}$$

where $\sigma_{f_{\mathrm{MS}}}$ and $\sigma_{\phi_{\mathrm{MS}}}$ are the standard deviation of Δf and $\Delta\phi$ due to the magnetic sensor noise, respectively. The net effect is an increase in the effective Δf_{min} and $\Delta\phi_{\mathrm{min}}$. Time averaging can also be used here to reduce the noise of the device. By repeating the measurements N times, the standard deviation decreases to $\sigma_{\mathrm{MS}}/\sqrt{N}$.

Resolution

The spatial resolutions Δx and Δy defined in equations 3.6 and 3.8 depend on the standard deviation of the oscillation frequency (σ_f) and phase (σ_ϕ) of the ATOMS

device. Based on our previous discussion, we can define σ_f and σ_ϕ as

$$\sigma_f = \sqrt{\sigma_{f_{\text{MS}}}^2 + \sigma_{PN}^2} \tag{3.29}$$

$$\sigma_\phi = \sqrt{\sigma_{\phi_{\text{MS}}}^2 + \sigma_{TJ}^2}, \tag{3.30}$$

where σ_{PN} is the standard deviation of the oscillator's phase noise and σ_{TJ} is the standard deviation of the timing jitter.

3.4 Angular Misalignment

The previous analysis comprises the case when B_Z is orthogonal to the chip. In the case of an angular misalignment of θ° degrees between B_Z and an ATOMS device (Figure 3.10), the measured magnetic field will be proportional to the projection of B_Z into the plane orthogonal to the device (i.e., $B_Z \cos\theta$), and can reduce the accuracy of the system. The polar angle η, in contrast, will not affect the resolution because the device only measures the orthogonal magnetic field.

To overcome this limitation, we devise the following method which can be applied to frequency and phase encoding. We add an extra step in the pulse sequence where a uniform magnetic field B_C (i.e., no field gradient) is applied to measure a correction factor and correctly estimate B_{G_Z}, the local magnetic field at the device's location generated by the field gradient G_Z. For simplicity, we only consider the case of frequency encoding. The same derivation can be applied to phase encoding.

Figure 3.11 shows the pulse sequence for localization of a single ATOMS device with angular misalignment. We first apply the known field B_C. In this case, the ATOMS device measures

$$B_{MC} = B_C \cos\theta, \tag{3.31}$$

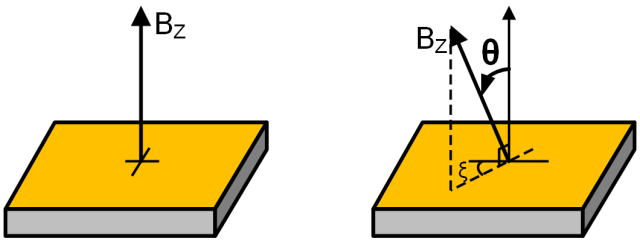


Figure 3.10: Illustration of angular misalignment, where θ is the azimutal angle and ξ is the polar angle. In the case of misalignment, the chip measures $B_Z \cos\theta$.

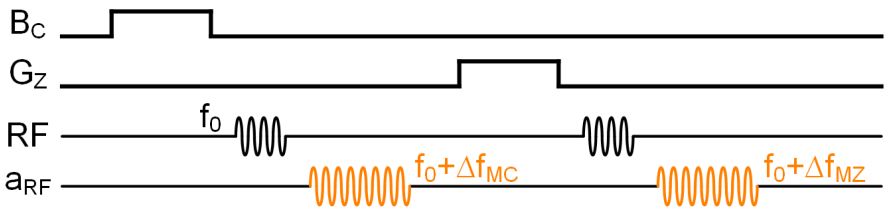


Figure 3.11: Pulse sequence for localization of a single device with angular misalignment. An extra step in the pulse sequence is added where a uniform magnetic field B_C is applied to measure a correction factor. This factor is used to estimate the local magnetic field generated by G_Z (B_{G_Z}) from measured frequency shifts Δf_{MC} and Δf_{MZ}, and the known field B_C.

which is estimated from the measured frequency shift by

$$B_{MC} = \frac{\Delta f_{MC}}{\gamma_{\text{ATOMS,f}}}, \tag{3.32}$$

where Δf_{MC} is the frequency shift due to B_{MC}. Then, the angular misalignment can be estimated by

$$\theta = \cos^{-1}\left(\frac{B_{MC}}{B_C}\right). \tag{3.33}$$

Second, we apply G_Z and the chip measures

$$B_{MZ} = B_{G_Z}\cos\theta. \tag{3.34}$$

Similarly, B_{MZ} is estimated by

$$B_{MZ} = \frac{\Delta f_{MZ}}{\gamma_{\text{ATOMS,f}}}, \tag{3.35}$$

where Δf_{MZ} is the frequency shift due to B_{MZ}. Finally, combining the device's measurements B_{MC} and B_{MZ} with equations 3.32 and 3.35 gives

$$\frac{B_{MZ}}{B_{MC}} = \frac{B_{G_Z}\cos\theta}{B_C\cos\theta} = \frac{\Delta f_{MZ}/\gamma_{\text{ATOMS,f}}}{\Delta f_{MC}/\gamma_{\text{ATOMS,f}}},$$

$$B_{G_Z} = B_C\frac{\Delta f_{MZ}}{\Delta f_{MC}}. \tag{3.36}$$

This approach allows the correct estimation of the ATOMS device's location and also enables the estimation of its orientation as long as the local magnetic fields B_{MC} and B_{MZ} are above the noise floor of the magnetic sensor. This means

$$B_C\cos\theta \text{ or } B_{G_Z}\cos\theta > B_{\text{min}}, \tag{3.37}$$

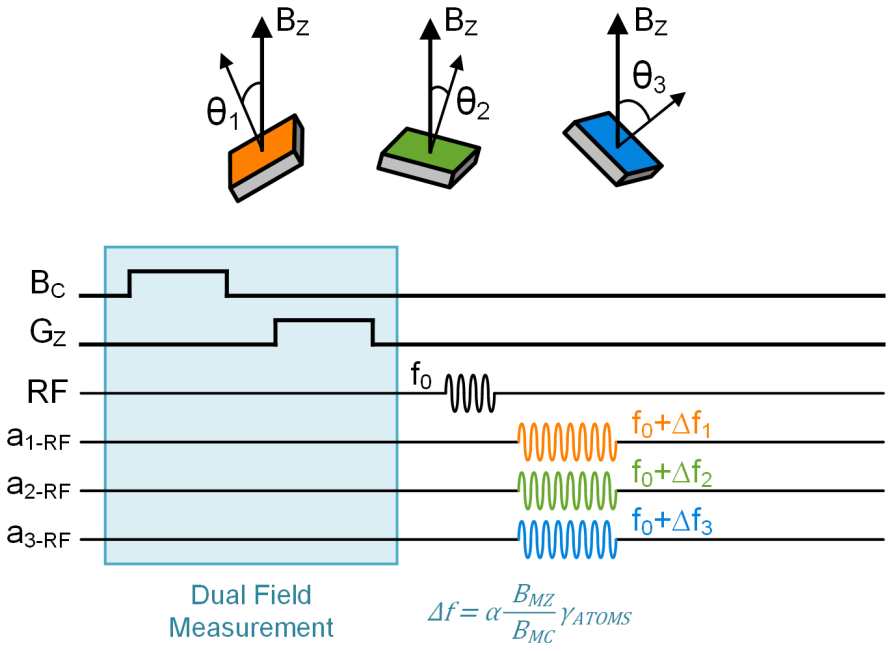


Figure 3.12: Pulse sequence for localization of multiple arbitrarily aligned ATOMS devices. In this case, each device calculates the ratio of measured fields B_{MZ} and B_{MC}, and shifts its oscillation frequency in proportion to this ratio, γ_{ATOMS}, and the bandwidth utilization constant α.

where B_{min} is the resolution of the magnetic sensor. Therefore, the maximum angular misalignment θ_{max} is given by

$$\theta_{\text{max}} = \cos^{-1}\left(\frac{B_{\text{min}}}{B_{G_Z\text{min}}}\right), \text{ with } B_{G_Z\text{min}} < B_C, \tag{3.38}$$

where $B_{G_Z\text{min}}$ is the minimum magnetic field generated by the field gradient G_Z.

For a single device, Δf_{MC} and Δf_{MZ} can be obtained in two successive acquisitions. For localization of multiple arbitrarily arranged ATOMS devices (Figure 3.12), the device can calculate the alignment correction internally (on-chip). In this scenario, both B_C and G_Z are applied consecutively so that the devices measure B_{MC} and B_{MZ}. Then, each device calculates the ratio of B_{MC} and B_{MZ} and shifts its oscillation frequency according to

$$\Delta f = \alpha \frac{B_{MZ}}{B_{MC}} \gamma_{ATOMS}, \tag{3.39}$$

where α is a constant pre-programmed into the device which is set by the target bandwidth utilization. Thus, the location of each device is estimated as described above.

Another approach is to use a 3D magnetic sensor in the chip. Here, B_{G_Z} can be calculated by measuring all 3 components of the magnetic field and performing frequency encoding using the total field $B_M = \sqrt{B_{MX}^2 + B_{MY}^2 + B_{MZ}^2}$, where B_M, B_{MX}, B_{MY}, and B_{MZ} are the measured total magnetic field and magnetic field components in x, y, and z, respectively. In this case, the resolution will be limited by noise.

3.5 3D Localization Schemes

Depending on the target application, a single of multiple ATOMS devices can be found inside a patient or an animal as shown in Figure 3.13. Similar to MRI, three magnetic field gradients with different directions can be used to locate these devices.

For a single ATOMS device, we achieve 3D localization by performing frequency encoding in each dimension as shown in figure 3.14. For the device shown in

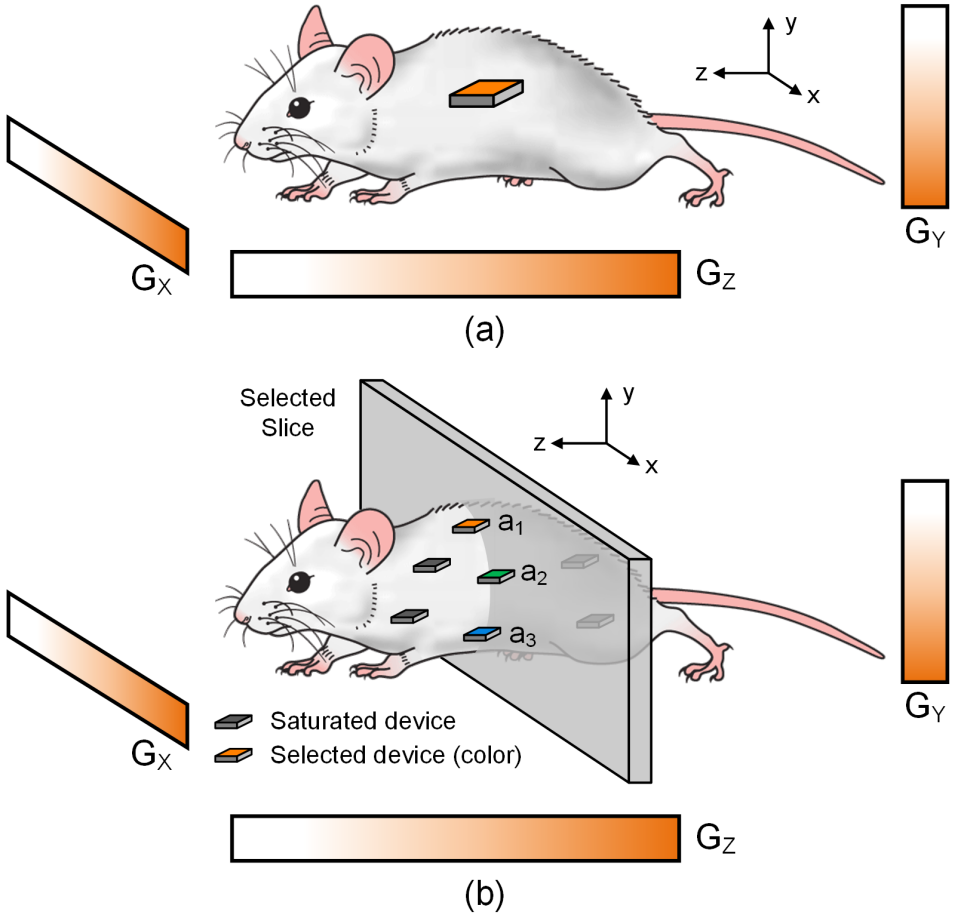


Figure 3.13: Illustration of 3D localization of (a) a single and (b) multiple ATOMS devices. G_X, G_Y, and G_Z are the magnetic field gradients.

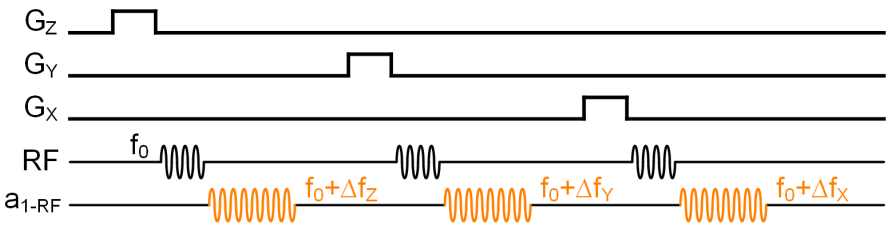


Figure 3.14: Pulse sequence for 3D localization of a single ATOMS device using only frequency encoding.

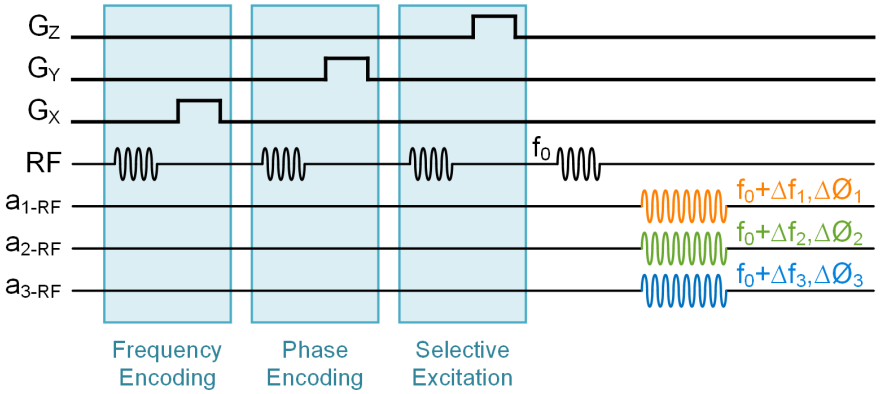


Figure 3.15: Pulse sequence for 3D localization of multiple ATOMS devices using frequency encoding, phase encoding, and selective excitation.

Figure 3.13a, the frequency shifts after each RF excitation Δf_X, Δf_Y, and Δf_Z are proportional to the local magnetic field generated by G_X, G_Y, and G_Z, respectively. By mapping these frequency shifts back in space, the location can be determined.

For multiple devices (Figure 3.13b), we achieve 3D localization using frequency encoding, phase encoding and selective excitation according to the pulse sequence shown in Figure 3.15. ATOMS devices can be designed to expect four RF pulses before transmitting their responds. The first two pulses trigger the chips to sense the magnetic field generated by G_X and G_Y, and set Δf and $\Delta\phi$, respectively. The third pulse tells the devices to sense the field generated by G_Z and become silent during transmission if they experience a field magnitude above a certain threshold (outside the slice of interest). The final RF pulse is then used for frequency acquisition and synchronization, and to indicate devices not saturated by G_Z (selected devices a_1, a_2 and a_3) to start transmitting according to their frequency and phase shifts (Δf_1, Δf_2, Δf_3, and $\Delta\phi_1$, $\Delta\phi_2$, $\Delta\phi_3$, respectively). These frequency and phase shifts are then mapped back in space to estimate the location of selected devices.

Chapter 4

ATOMS: DESIGN AND IMPLEMENTATION

In this chapter, we focus on the description of the design and implementation of the electronics targeting an ATOMS device. We cover design concepts and insights from the system architecture down to the single block level. Analysis and simulations are given and explained to understand the reasoning behind our assumptions and decisions.

4.1 System Architecture

The proposed system architecture for a fully wireless and autonomous device is shown in Figure 4.1 and consists of a magnetic sensor, a data acquisition unit, a phase-locked loop (PLL),a power amplifier (PA), a control logic with digital signal processing (DSP), a power management unit, and dual RF coils for power and data transfer. The data acquisition unit consists of a low-noise amplifier (LNA), a variable gain amplifier (VGA) and a buffer to interface with the analog-to-digital converter (ADC). The power management consists of a on-chip rectifier, a dual low-dropout regulator for analog and digital circuitry, a bandgap and a bias generator. To interface with RF fields, an on-chip micro-coil is designed. The power management unit harvest energy either from RF fields via a power coil or from a local battery to

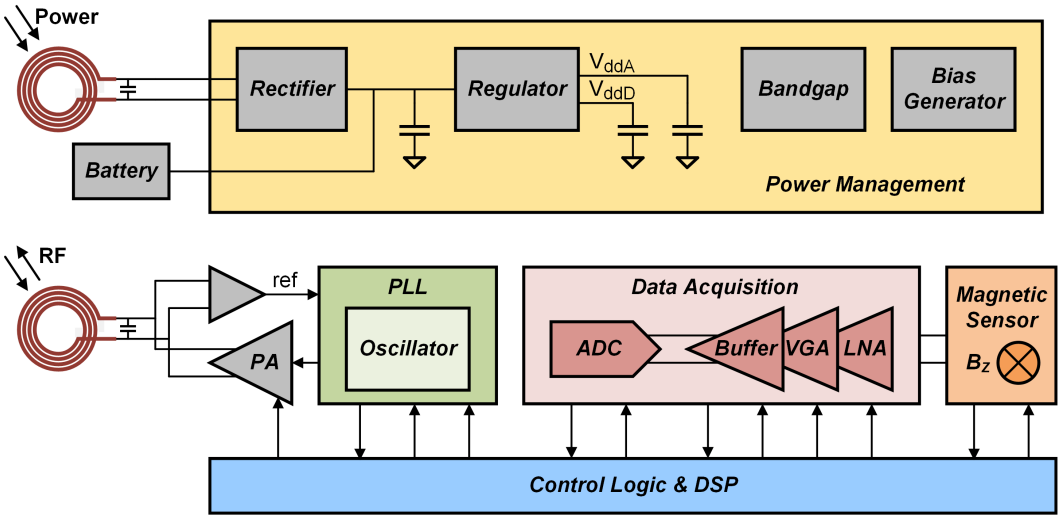


Figure 4.1: System architecture of the proposed fully wireless system.

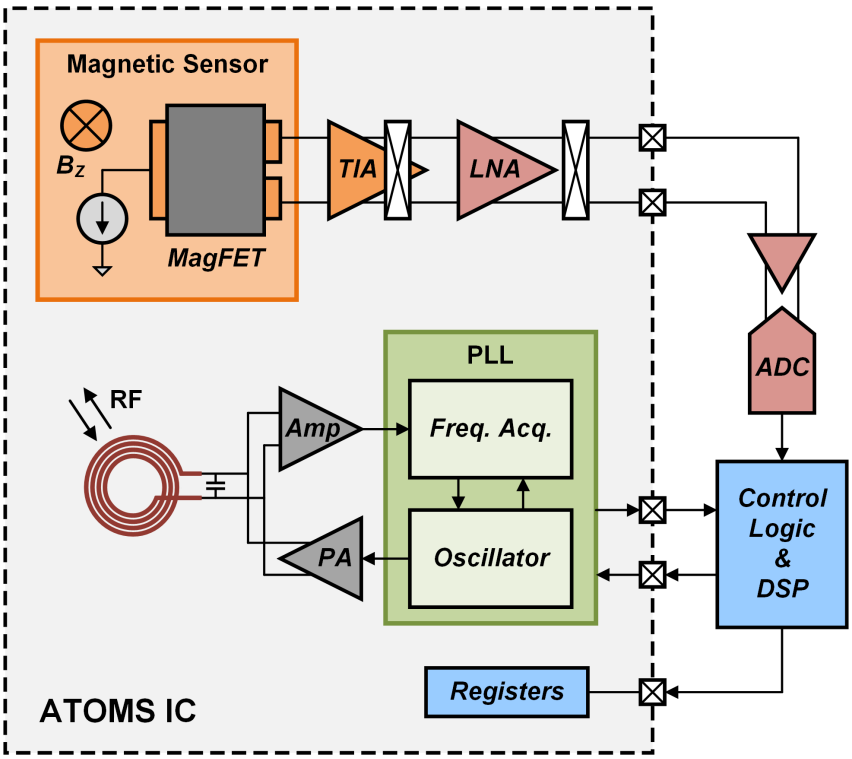


Figure 4.2: System architecture of our ATOMS prototype. In this work, the magnetic sensor, amplifiers, PLL, PA, and the on-chip coil are integrated in the same chip. The ADC, control logic, and DSP are implemented externally.

power all the chip's functions, including future sensing and actuation of biological processes. The PLL is used to synchronize multiple ATOMS to the same RF excitation signal. An on-chip magnetic sensor is used to measure the magnetic field generated by the applied field gradient. Then, this measurement is used to shift the oscillation frequency of the internal (on-chip) oscillator proportionally.

In this work, we focused on integrating the critical components of the system in a single chip: the magnetic sensor, amplifiers, PLL, PA, and the on-chip coil for frequency locking and radiation. The ADC and control logic have more relaxed requirements due to the low processing speed (up to few kHz) and can be integrated into the system in future versions.

As a first proof-of-concept, we targeted a resonance frequency (f_0) of 500 MHz to emulate a small 11.7 T MRI system, and utilized frequency encoding as the localization method. The system architecture of our ATOMS prototype consists of a magnetic sensor, a two-stage chopper amplifier, an ADC, a PLL, a PA, an on-chip coil and a control logic with DSP (Fig. 4.2). The magnetic sensor is an on-chip

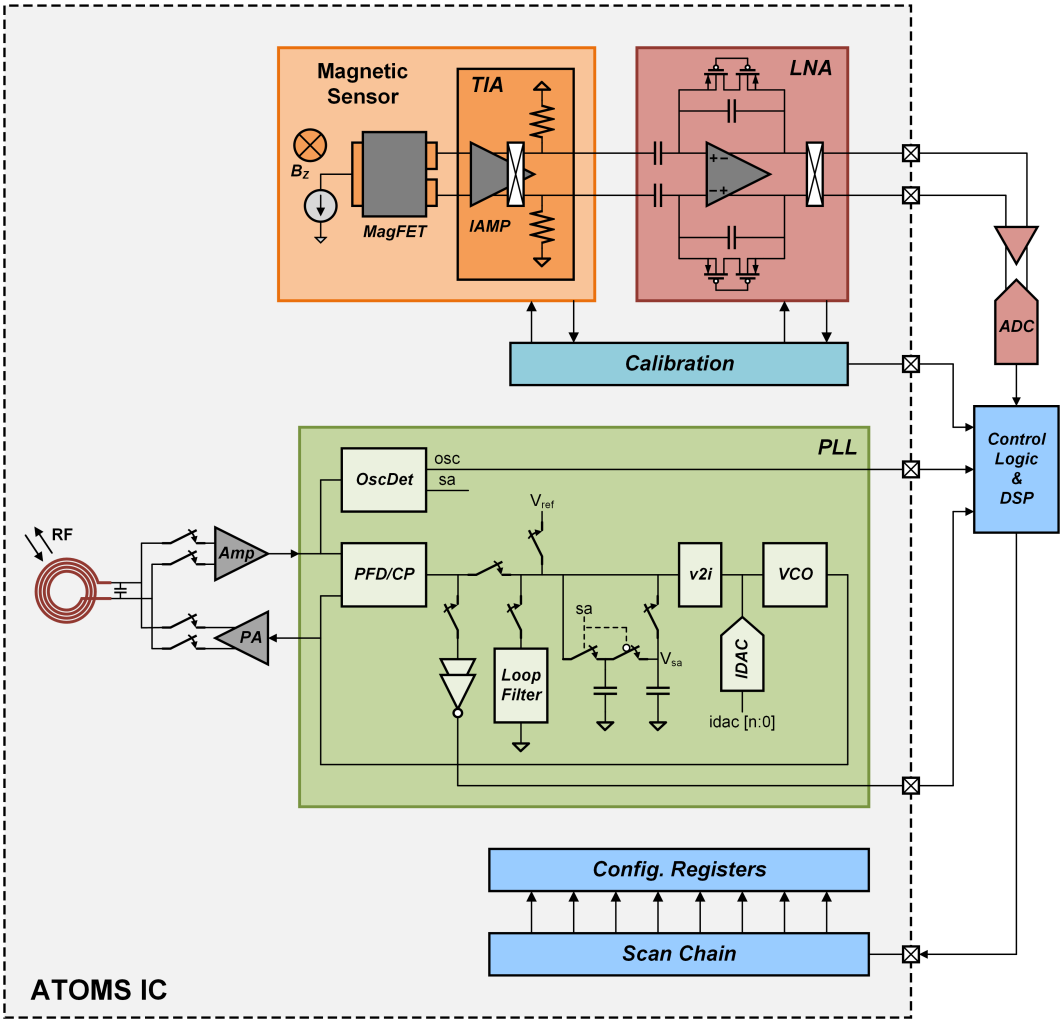


Figure 4.3: Detailed schematic of our ATOMS prototype.

split-drain magnetic field-sensitive field-effect transistor (MagFET) that measures the applied magnetic field orthogonal to the chip (B_Z). This Hall-effect device generates a differential current between both drains by deflecting the carriers across the transistor's channel proportional to B_Z and its bias current [86]. The output current of the MagFET is amplified by a trans-impedance amplifier (TIA) and a LNA. To minimize the noise of the readout circuitry at low frequencies, a chopper amplifier is formed by adding chopper modulators in the TIA and at the output of the LNA. The output of the amplifier is then digitized for processing (e.g., averaging) and storage. The on-chip coil is resonated at f_0 using an on-chip capacitor. The coil acquires the excitation RF signal and emits the response of the chip. The PLL locks the internal oscillator to the RF pulse during the excitation phase. During the transmission phase, the frequency of the internal oscillator (f_0 immediately after

excitation) is shifted proportionally to the measured magnetic field and is fed to the PA for transmission. The control logic manages the whole operation of the chip and processes the measured magnetic field. Figure 4.3 shows details of the system architecture of our current prototype.

4.2 Magnetic Field-Sensitive Field-Effect Transistor - MagFET

To measure the magnetic field we use a Hall-effect device based on current deflection. The split-drain magnetic field-effect transistor (MagFET) uses the inversion channel under the transistor's gate as the Hall plate [86]. Since we bias this device in strong-inversion, the main carrier transport is drift.

Considering the transistor's channel as an extrinsic silicon sheet and an applied magnetic field B orthogonal to its surface, the Lorentz force F in a carrier is expressed as

$$F = qE + qv \times B\,, \tag{4.1}$$

where q is the carrier charge, E is the electric field, and v is the carrier velocity.

The drift current densities in the inversion channel for holes and electrons, J_{p_B} and J_{n_B}, are defined as

$$J_{p_B} = J_{p_0} + \mu_p \left(J_{p_B} \times B\right) \tag{4.2}$$

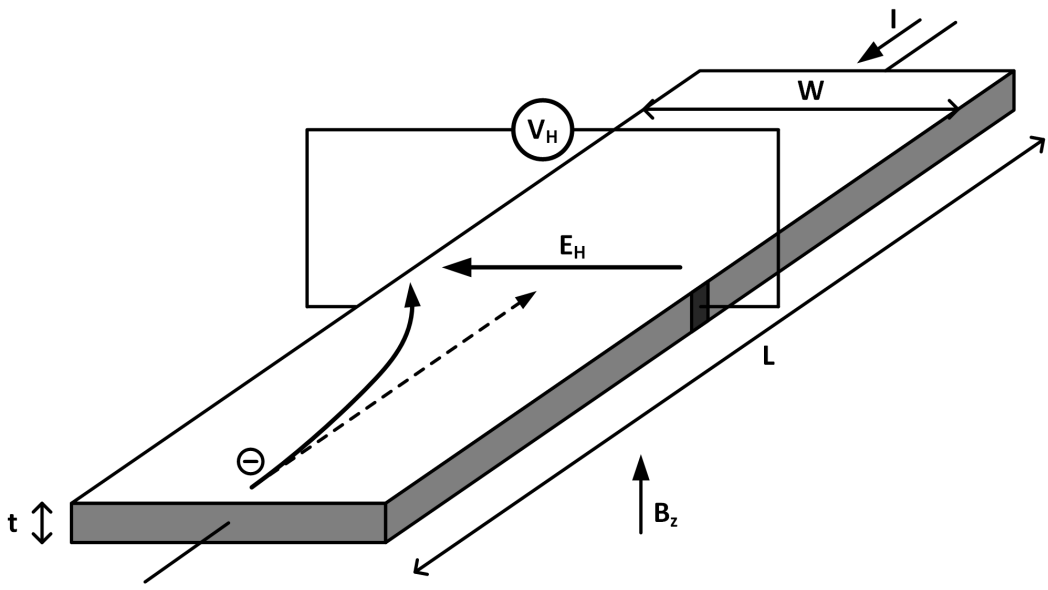


Figure 4.4: Illustration of the Hall effect in a conductive media with a length L and a width W. An electric field E_H is generated by the carrier deflection and produces a maximum potential call the Hall voltage V_H.

$$J_{n_B} = J_{n_0} + \mu_n (J_{n_B} \times B), \tag{4.3}$$

where J_{p_0} and J_{n_0} are the current densities for holes and electrons at zero field, and μ_p and μ_n are the mobilities for holes and electrons, respectively. Solving the previous equations, we obtain

$$J_{p_B} = \sigma_{p_B} E + \sigma_{p_B} \mu_{H_p} (E \times B) \tag{4.4}$$

$$J_{n_B} = \sigma_{n_B} E - \sigma_{n_B} \mu_{H_n} (E \times B) \tag{4.5}$$

with

$$\sigma_{p_B} = \frac{\sigma_{p_0}}{1 + (\mu_{H_p} B)^2} \tag{4.6}$$

$$\sigma_{n_B} = \frac{\sigma_{n_0}}{1 + (\mu_{H_n} B)^2}, \tag{4.7}$$

where σ_{p_B} and σ_{n_B} are the conductivities for holes and electrons at field B, respectively; σ_{p_0} and σ_{n_0} are the conductivities at zero field; and μ_{H_p} and μ_{H_n} are the Hall mobilities for holes and electrons, respectively. The Hall coefficient R_H is defined as

$$R_H = -\frac{r_H}{qn} = \frac{r_H}{qp}, \tag{4.8}$$

where r_H is the Hall factor and$p$ and n are the carrier densities for holes and electrons, respectively.

The conductivity at zero field is defined as

$$\sigma_{p_0} = q \mu_p p \tag{4.9}$$

$$\sigma_{n_0} = q \mu_n n \,. \tag{4.10}$$

Then the conductivities for holes and electrons at a field B are defined as

$$\sigma_{p_B} = \frac{\sigma_{p_0}}{1 + (\sigma_{p_0} R_H B)^2}, \tag{4.11}$$

$$\sigma_{n_B} = \frac{\sigma_{n_0}}{1 + (\sigma_{n_0} R_H B)^2}. \tag{4.12}$$

MagFET Modeling

We model the Hall effect in the transistor's channel by using an anisotropic conductivity model. We can think of the Hall effect as a change in the effective local resistivity or conductivity of the channel due to the effect of carrier deflection caused by the applied magnetic field. This effect implies that the accumulation of carriers in one side of the channel at a particular distance from the source (conductive media) is due to a lower effective resistivity compared to the opposite side.

For a current density $J_B = \sigma_B E + \sigma_B \mu_H B_Z (E \times B)$, the anisotropic conductivity is defined as

$$\sigma_{\text{anisotropic}} = \begin{bmatrix} \sigma_{11} & \sigma_{12} \\ \sigma_{21} & \sigma_{22} \end{bmatrix}, \tag{4.13}$$

where

$$\sigma_{11} = \sigma_{22} = \sigma_B = \frac{\sigma_0}{1 + (\sigma_0 R_H B_Z)^2} \tag{4.14}$$

$$\sigma_{12} = -\sigma_{21} = \mu_H B_Z \sigma_B = \sigma_0 R_H B_Z \sigma_B \,. \tag{4.15}$$

In a split-drain MagFET, the Hall current is defined as

$$I_H = I_{D_2} - I_{D_1} = \mu_H B_Z \left(\frac{L}{W}\right) I_D G_H \,, \tag{4.16}$$

where G_H is the geometry factor which takes values from 0 to 1. The sensitivity of the devices is then defined as

$$S_I = \frac{I_H}{I_D B_Z} = \mu_H \left(\frac{L}{W}\right) G_H. \tag{4.17}$$

Figure 4.5a shows the geometrical model of the MagFET, where the single source S_1, split drain D_1 and D_2, form factor W/L and sensor current I_D are highlighted. Figure 4.5b shows the equivelent electrical model of the MagFET based on the sensitivity S_I of the device. It can be seen that it reseembles a differential pair which output current ΔI is proportional to S_I and the orthogonal magnetic field B_Z.

Therefore, the response of the sensor ΔI in the equivalent electrical model is given by

$$\Delta I = \frac{1}{2} S_I B_Z I_D. \tag{4.18}$$

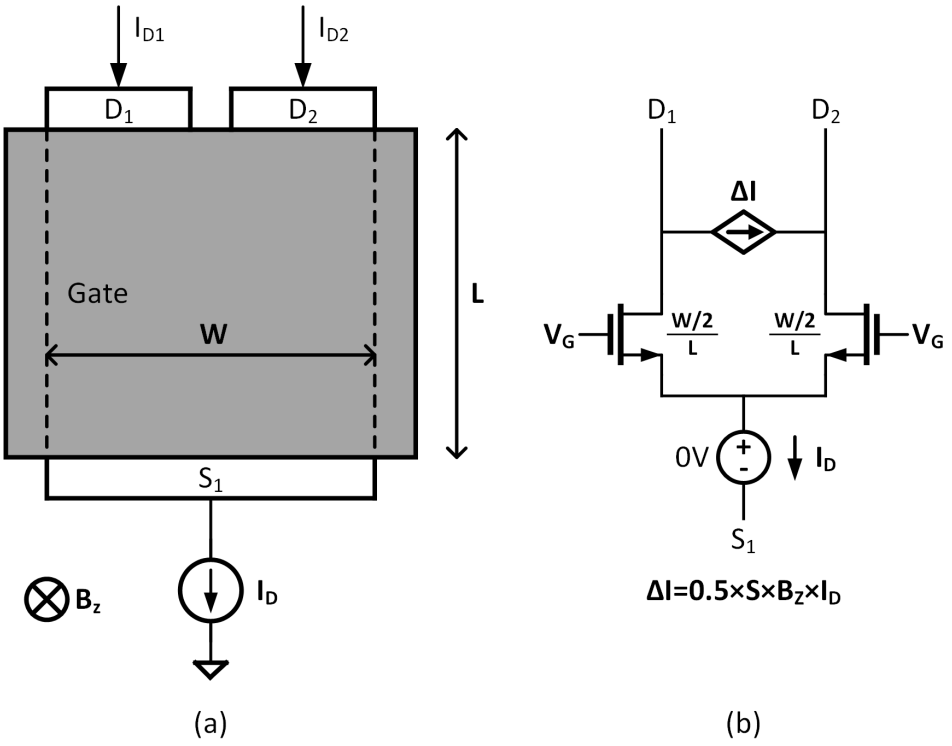


Figure 4.5: (a) Geometrical model of the MagFET. (b) Equivalent electrical model of the MagFET based on the sensitivity S_I of the device.

MagFET Design

Because the sensitivity of the MagFET is directly related to the Hall mobility, we choose a n-type transistor (NMOS) as the base of our sensor. We model the transistor's channel in strong inversion as a sheet resistance with the following parameters:

- Carrier mobility in the channel: μ_n
- Carrier concentration in the channel - Doping: N_D

Usually, these parameters are not given explicitly by the manufacturer, and need to be extracted via simulations. To do so, we realized that usually split-drain MagFETs are long channel devices. Thus, we can use the following simple approximation for its behavior:

$$I_D = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2 \tag{4.19}$$

$$\frac{\partial^2 I_D}{\partial V_{GS}^2} = \mu_n C_{OX}\left(\frac{W}{L}\right), \tag{4.20}$$

where C_{OX} is given by the technology.

An important note is that this approximation is better suited for technologies bigger than 90 nm. Short-channel effect such as high vertical electric field and strained silicon might cause a significant deviation in highly scaled technologies. Although this method can still be used for such technologies as an initial approximation in the design, further considerations need to be taken into account for an accurate model.

We extract the previous parameters by means of a simple DC simulation. The extracted parameters are:

- $\mu_n C_{OX}$ = 230 μA/V^2 - From simulations
- $C_{OX} \approx$ 8.22 mF/m^2 - From PDK
- $\mu_n \approx$ 280 cm^2/V/s - From simulations
- $N_D \approx$ 6e17 cm^{-3} - From PDK

Using the extracted parameters from the technology, we use COMSOL Multiphysics to design the Magfet. We use a 2-D conductive media to model the channel of the transistor, and perform an analysis using SPICE integration for better accuracy with the front-end design (Figure 4.6). We set W to 10 μm and sweep L for 5, 8, 10, and 20 μm. The separation between the drains is minimized to reduce the *insulator effect* that reduces the sensitivity of the device [86]. In this technology, it is set to 0.28 μm. The orthogonal magnetic field B_Z is swept from 0 to 1 mT.

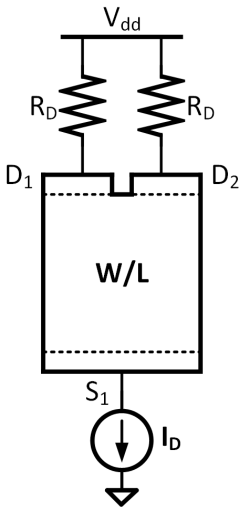
As important as finding the best geometry for peak sensitivity, the impedance of the transistor between drain and source also plays an important role in the design of the sensor. From the simulation results, a longer device will have a higher sensitivity and will also have a higher resistance. This implies that the voltage drop between drain and source will increase for a given current. Thus, if we have a limited supply (e.g., in low power applications or low-supply applications as is the trend in modern technologies), focusing only on the sensitivity doesn't guarantee the best responsivity of the sensor.

Another important factor is the input impedance of the read-out circuitry. Ideally, this impedance should be zero, so that the voltage across each of the drains and source is equal and symmetric. Due to the principle of current deflection, when a magnetic field is applied, one of the drains will carry more current. Since the

```
Id 1 0 50e-6
Vdd 2 0 1
Rd1 2 3 1e3
Rd2 2 4 1e3
X1 3 4 1 sdmagfet

.SUBCKT sdmagfet d1 d2 s COMSOL:
"../sdmagfet_model.mph"
.ENDS
```

(a)



(b)

Figure 4.6: (a) SPICE script and (b) schematic representation for MagFET simulation.

impedance of the read-out circuitry is non-zero, there will be an imbalance of potential at the drains. The drain that carriers more current will have a lower voltage than the other drain. This means that V_{DS} for this drain reduces, which reduces the drain current I_{D1} due to channel length modulation. Conversely, the other drain experiences a higher V_{DS} which increases its drain current I_{D2}. The overall effect is a reduction in the sensitivity of the sensor.

Therefore, we focus on the output current of the sensor, which is defined as

$$\Delta I = S_I I_{bmax}\,, \tag{4.21}$$

where the maximum bias current I_{bmax} is defined by the headroom of the bias circuits of the sensor. For a given form factor (W/L), the sensitivity and I_{bmax} is found. This is shown in Figure 4.7 for a supply of 1V.

The simulations show that a high sensitivity is achieved for low W/L, with a peak of ~1.6 %/T. Given the power budget constrain, for a bias current I_B of 18 μA, the best performance is achieved with W/L of 0.7 with a sensitivity of 1.54 %/T and ΔI of 0.28 nA/mT.

The final size of the device will depend on noise. A bigger device will reduce flicker noise significantly. We can see this behavior in Figure 4.8. A final W/L of 20 μm / 28 μm is chosen.

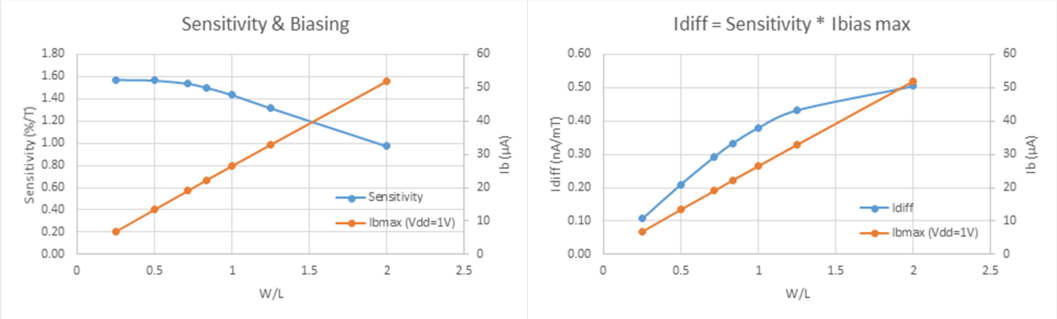


Figure 4.7: (a) Sensitivity and sensor current as a function of aspect ratio W/L. (b) MagFET output (ΔI) as a function of aspect ratio.

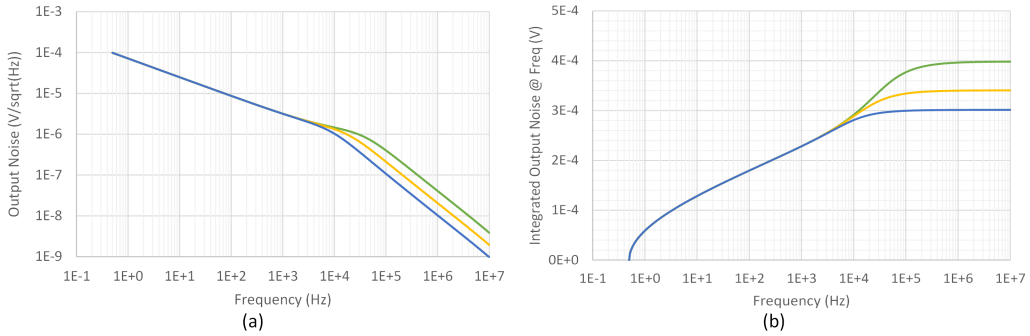


Figure 4.8: (a) Output referred noise of the MagFET. (b) Integrated noise as a function of frequency.

4.3 Trans-Impedance Amplifier

We use a trans-impedance amplifier to convert the output current of the MagFET to voltage. The topology of the TIA is shown in Figure 4.9. As mentioned before, the output of the MagFET is a differential current which requires a low input impedance and good matching for the differential stage. A low-voltage cascode current mirror with high W/L ratio and a gain of 1 provide low input impedance with good matching and relative high output impedance. This is a trade-off between input and output impedance in this topology. However, this limitation is not of concern because the output load is not significantly high. Having a current gain greater than 1 implies higher TIA gain but also higher power consumption and higher process variation. Given that we have other gain stages and a limited power budget, a gain of 1 gives the best performance.

Because of the relative low sensitivity of the MagFET, the input current to the TIA is a very small DC signal on top of a very high DC bias current. In order to amplify

the signal and not saturate the output stage of the TIA, we remove the majority of the DC input current via 2 additional current sources (I_{bp} and I_{bn}). The bias circuitry for the MagFET is also included in the TIA and keeps a fixed ratio between the MagFET current and $I_{bp,n}$. The output current consists of a residual DC current with the very small DC signal. This current is then converted to voltage via a resistor. The value of the resistor and the residual DC current are chosen to set the common-mode voltage of the output stage, which is ensured by the common-mode feedback (CMFB) stage. Any offset in the sensor and TIA is reduced via two current DACs I_{calp} and I_{caln}, explained in section 4.5.

In order to sense the output common-mode, we use a pmos source follower as a level shifter and a resistor network as the sensing element. The output of the resistor network is then fed to a nmos differential pair to be compared with the desired common-mode V_{CM}. The output of the CMFB circuit is injected into the output stage of the TIA by means of a pair of nmos cascode current sources. The capacitors C_C are used to stabilize the feedback network.

Because we are measuring DC or very low frequency signals, flicker noise is of great importance. Chopper amplifiers have proven to be a successful choice for such a signals [REFs]. They modulate the target signals to a higher frequency so that they can be amplified and filtered away from the low frequency noise of the amplifier. Because of the target low supply (1V) and mismatch considerations, the chopper modulator was placed at the output of the cascode current mirror to allow

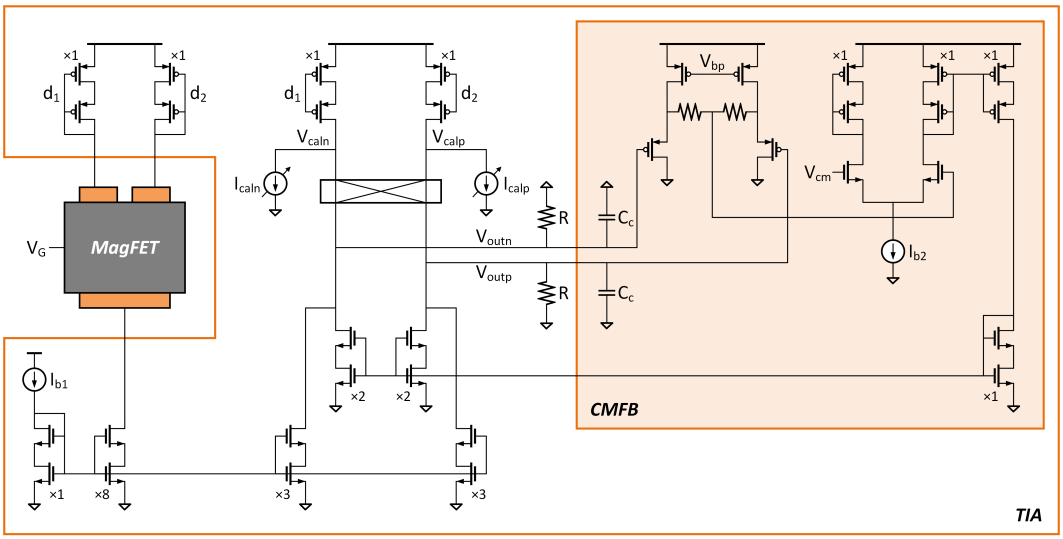


Figure 4.9: Schematic of the Trans-Impedance Amplifier (TIA) and MagFET.

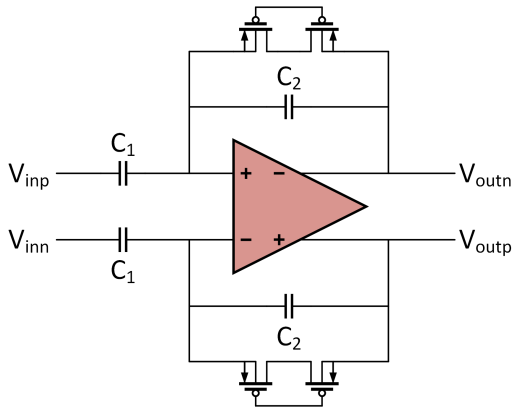


Figure 4.10: Top level schematic of the LNA.

the maximum possible voltage across the MagFET, as shown in Figure 4.9. Even though the noise of the input's transistors will not be reduced, this choice allows for a more sensitive MagFET due to the higher V_{DS} and better symmetry. In applications with higher supplies, the chopper modulator can be placed right at the output of the MagFET. It is important to note that the inherent flicker noise of the sensor cannot be reduced with this approach. This is a fundamental limitation of the current geometry of MagFETs. Other Hall effect devices based on Hall plates can used flicker noise removal techniques such as *spinning current* [REFs] at the expense of lower sensitivity due to the use of a Hall plate instead of a transistor's channel. Recently, [REF] show that a modification in the structure of the traditional MagFET can allow the use of the previously mentioned techniques to reduce the flicker noise of the device. Nevertheless, the techniques developed in this work can be applied to other Hall effect sensor. Another approach to reduce the flicker noise of the sensor is to use a low frequency alternating magnetic field as the signal instead of a DC magnetic field.

4.4 Low-Noise Amplifier

The LNA is a capacitive-feedback amplifier with a fully differential folded-cascode amplifier at its core (Figure 4.10). It has a gain of

$$A_{LNA} \approx \frac{C_1}{C_2}. \tag{4.22}$$

By changing the value of C_1, the gain of the LNA can be modified. Our topology has a 2-bit gain variation feature. These values are 25 dB, 28 dB, 31 dB, and 37 dB.

Figure 4.11 shows the schematic of the fully differential folded-cascode amaplifier. This topology is chosen because it provides high gain and good noise performance

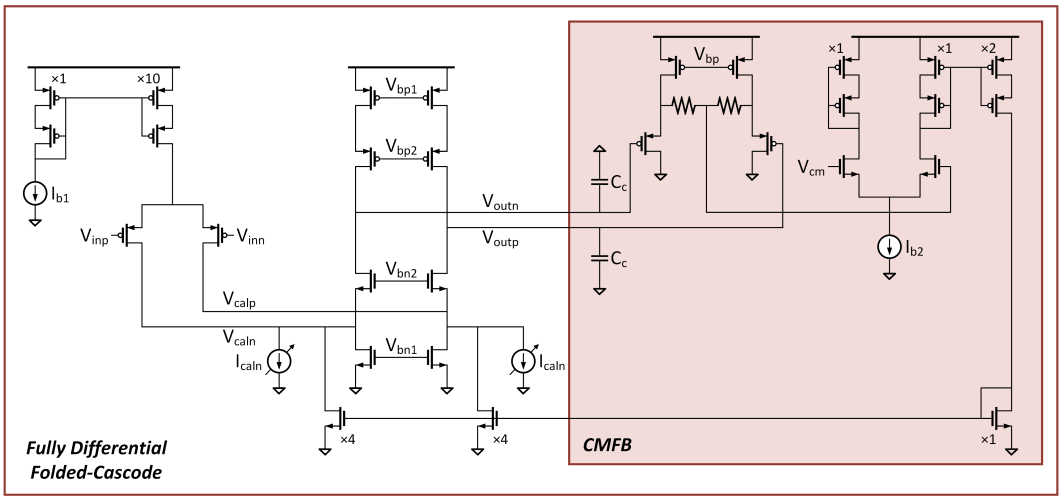


Figure 4.11: Schematic of the LNA core: Fully Differential Folded-Cascode.

at low supplies. A pmos differential pair topology is chosen to minimize noise. They are biased in weak inversion to maximize the g_m/I_D and thus the gain, noise and power performance. A cascode stage provides a high output impedance and high gain given the low supply. A CMFB stage is used to set the output common-mode. The CMFB stage is similar to the one described above for the TIA and sets the common-mode V_{CM}. Current sources I_{calp} and I_{caln} at nodes V_{calp} and V_{caln}, respectively, reduce the offset of the amplifier. More details about the calibration are explained in section 4.5.

Noise analysis of this stage shows that the main noise contributors are the transistors in the differential pair. Hence, their bias current is set by the noise requirement, and it is usually in the low μA range. Given the target bias current, the noise of the amplifier is minimized as follows. Thermal noise of the differential pair is minimized by biasing them in weak inversion. Flicker noise is minimized by increasing their area. The flicker noise in the current mirrors is minimized by biasing transistors in strong inversion and making them long (i.e., high value of L).

Simulation results showing frequency response, stability analysis, noise analysis, and timing response are shown in Figure 4.12.

4.5 Two-stage Chopper Amplifier

The analog front-end consists of the two-stage chopper amplifier conformed by the TIA and the LNA as shown in Figure 4.13. The frequency response of the amplifier is shown in Figure 4.14, where we can observe the gain of each stage as well as the

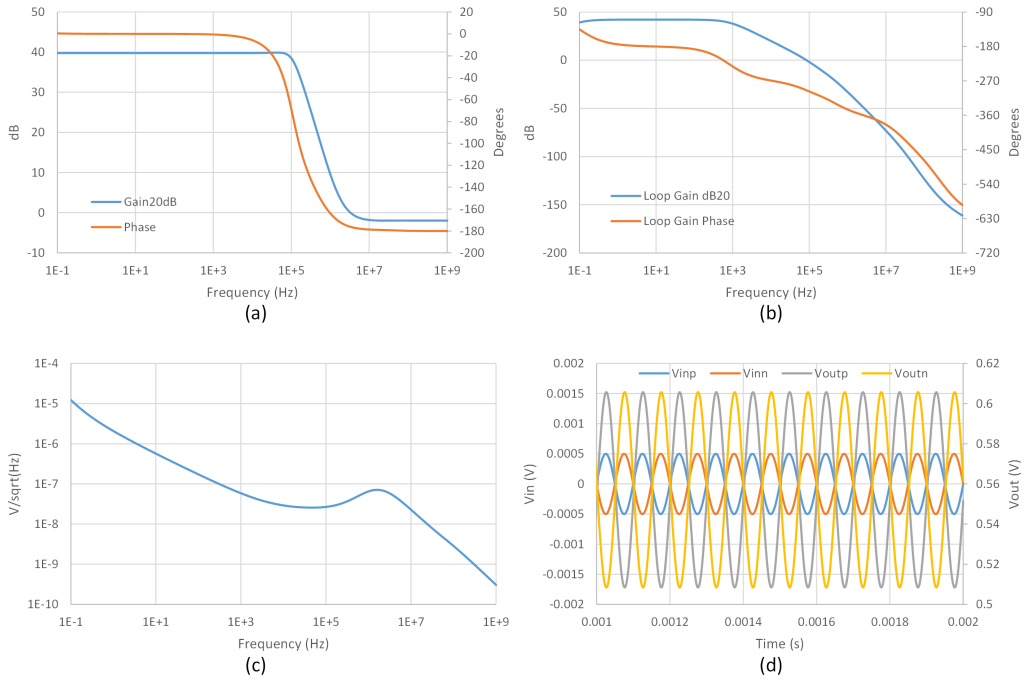


Figure 4.12: LNA simulations. (a) Frequency response. (b) Stability analysis. (c) Input referred noise. (d) Timing simulation.

total gain. The high bandwidth of the LNA allows for a high chopper frequency. However, it also increases the effective total noise. This bandwidth can be reduced in the buffers before the ADC, as it is the case in this work. Simulation results showing the timing response and noise analysis are shown in Figures 4.15 and 4.16.

The calibration of the amplifier is performed by 6 dual current DACs. A pair of 4-bit DACs is used instead of a single 7-bit or 8-bit DAC to reduce area. This is extremely important in an implant, where area is limited. For example, if the area of a unit cell is A_{UC}, a 7-bit DAC requires $128A_{UC}$ whereas two 4-bit DACs occupy a total of $32A_{UC}$. If we consider that the same unit cell is used as part of the current divider and assuming a division by 16, the total area would be $49A_{UC}$. In practice, the division factor is chosen to be 10 or 12, which increases the savings. Overall, this configuration achieves significant area savings with a minimum reduction of 61% for an equivalent ENOB.

Two pair of DACs are used for calibration of the TIA while four pair of DACs are used for the LNA. Due to the low supply, an additional set of current mirrors are used to inject the calibrating currents. These currents are injected at the nodes msV_{calp} and msV_{caln} in the TIA, and at $lnaV_{calp}$ and $lnaV_{caln}$ in the LNA. The calibrating

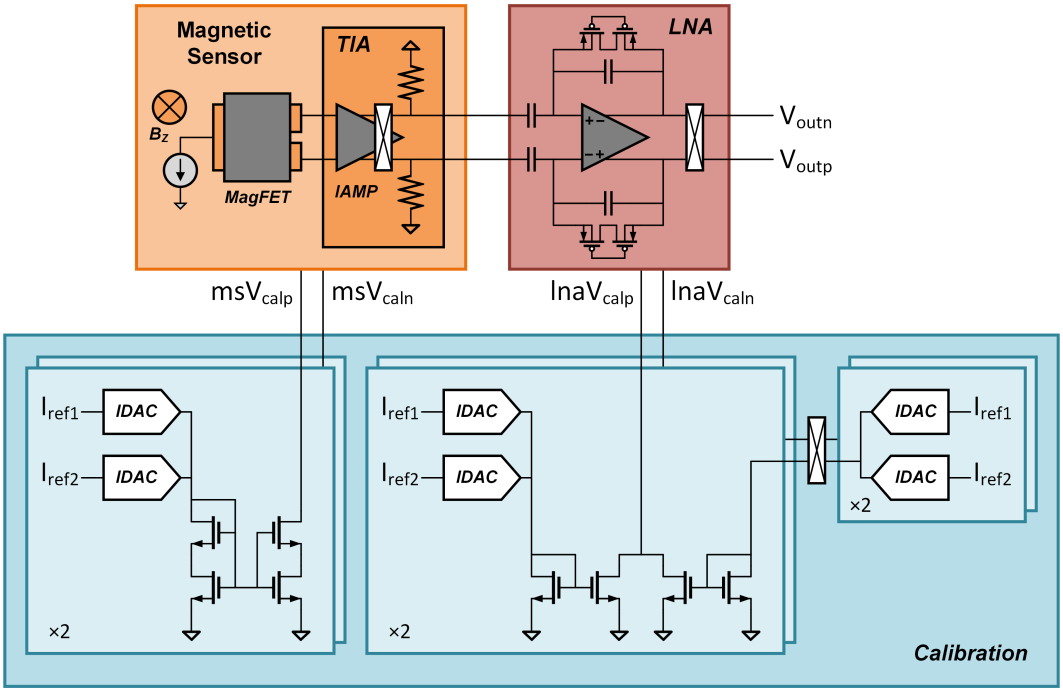


Figure 4.13: Schematic of the two-stage Chopper Amplifier.

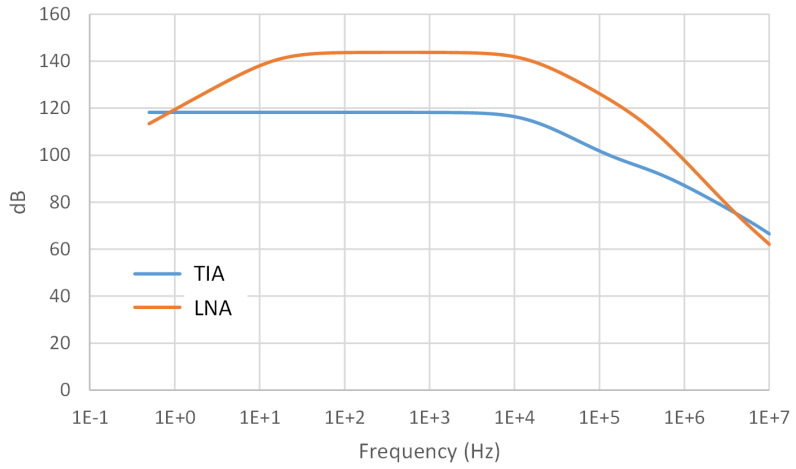


Figure 4.14: Frequency Response of the chopper amplifier after each stage.

currents in the TIA reduce the offset of the MagFET and are injected before the chopper modulator. In the LNA, there are two sets of calibrating currents. One of them reduces the inherent offset of the amplifier, while the second one, which is modulated, reduces the offset generated by the chopper modulators and any residual MagFET's offset.

Our current implementation calibrates the amplifier manually, but it can be easily in-

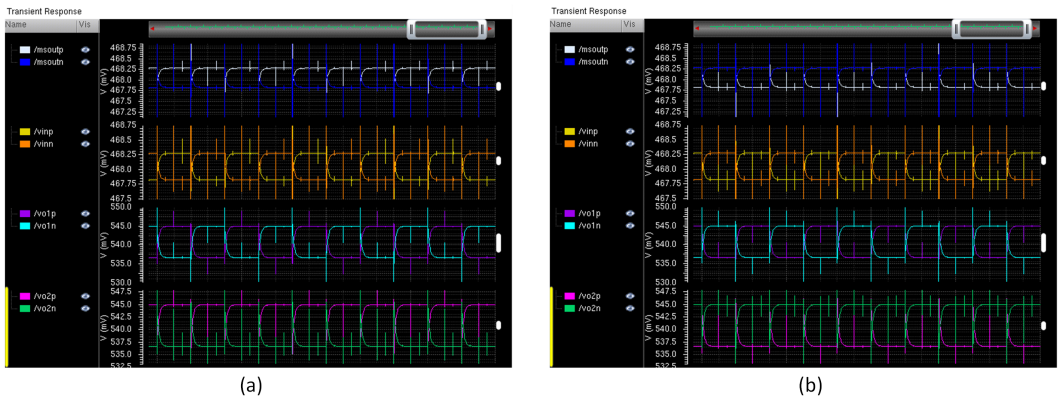


Figure 4.15: Timing simulations of the Chopper Amplifier.

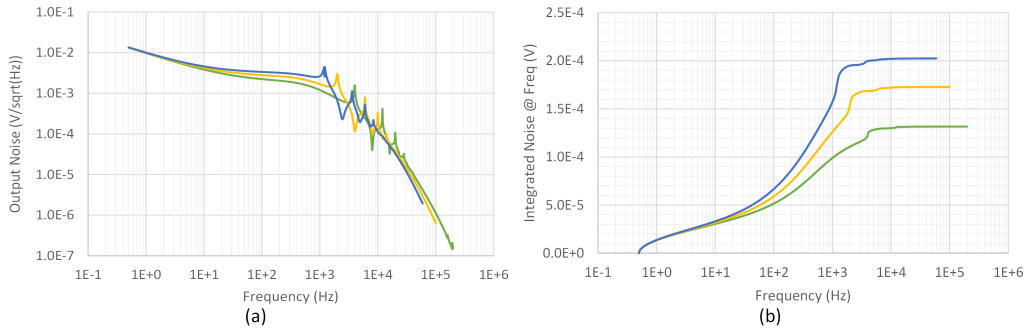


Figure 4.16: (a) Output referred noise. (b) Integrated noise as a function of frequency.

tegrated in a future version following a SAR-like process to achieve a self-calibrating stage. This would be of great impact in a fully wireless implant, where manual calibration becomes significantly more difficult.

4.6 Phase-Locked Loop

One of the main requirements of an ATOMS devices is the interface with the RF excitation signal. For a collection of devices, each of them needs to not only oscillate at the same frequency of the excitation signal f_0 but also synchronize with each other. Frequency acquisition allows the use of frequency encoding for localization purposes, while phase synchronization allows for phase encoding. In addition, the oscillation frequency needs to be sustained after the RF excitation is removed, in other words, in the absence of a reference signal. This implies that f_0 needs to be acquired and stored to be used during transmission. Furthermore, the oscillation frequency needs to be shifted based on the previously measured local

magnetic field.

The architecture of the proposed PLL is shown in Figure 4.17. An oscillator detector is designed to sense the presence and absence of the reference signal, allowing control of the PLL loop. In the presence of the reference signal, the loop is closed and the PLL locks to input signal. The oscillation frequency of the VCO f_{osc} is then measured by sampling V_{ctrl} using a switch capacitor network. In the absence of reference signal, the PLL loop is opened to avoid any miscorrection in the oscillation frequency. Since the PLL needs to keep the oscillation frequency of the VCO without a reference, a low K_{VCO} architecture is chosen so that the VCO oscillation frequency is less sensitive to variations in V_{ctrl}. The low K_{VCO} will produce *gaps* in the f_{osc} vs V_{ctrl} curve since they will not overlap in the presence of process variation as shown in Figure 4.18. A digital coarse tuning following a SAR-like process corrects for process variations and brings the oscillation frequency within the PLL locking range, so that the *PLL action* locks the PLL in a fine tuning fashion. The digital coarse tuning uses three 4-bit current DACs to calibrate the VCO in a similar structure to the DACs described above for the amplifiers.

The proposed architecture presents three modes of operation: calibration mode, normal mode and transmission mode. They are described in the following paragraphs.

The PLL enters the calibration mode after powering up to calibrate the oscillation frequency of the VCO (Figure 4.19a). The PLL loop is opened, the loop filter is disconnected, the input of the $V2I$ block is connected to a reference voltage V_{ref},

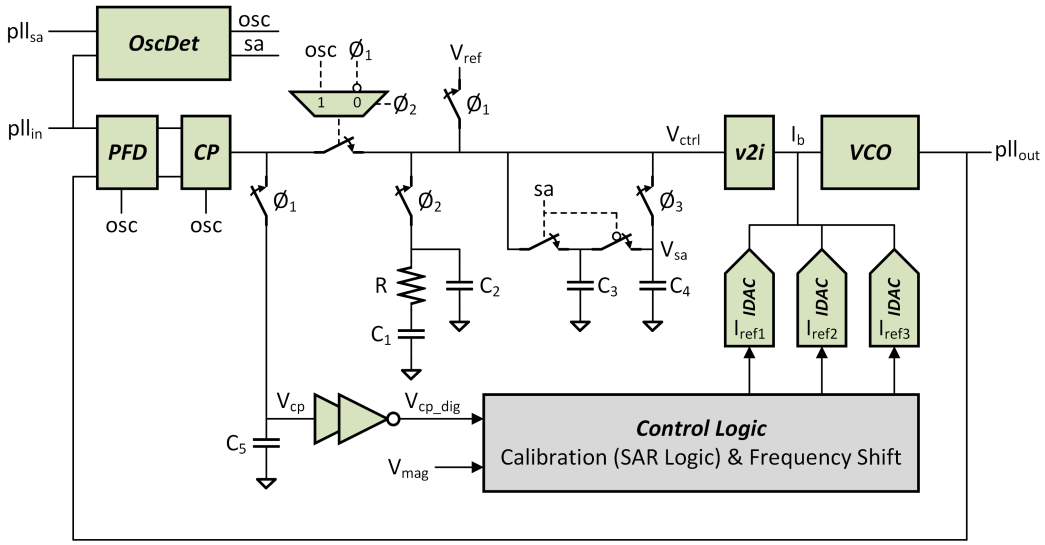


Figure 4.17: Top level schematic of the PLL.

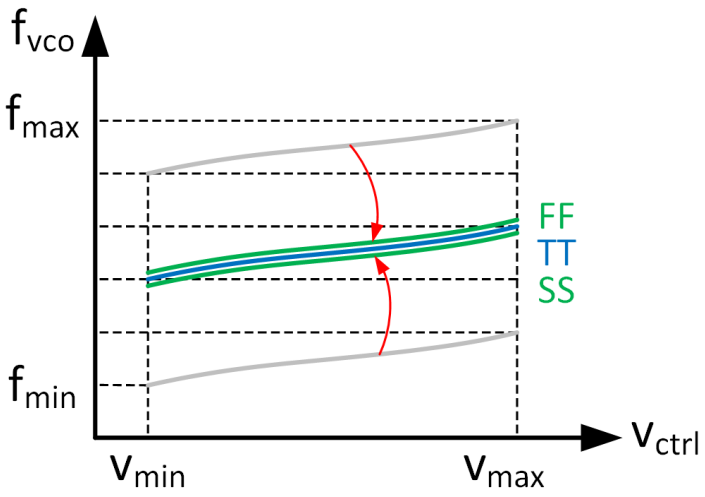


Figure 4.18: Effect of low K_{VCO} in the oscillation frequency of the VCO under process variation.

and the output of the charge-pump is connected to a capacitor and a digital buffer to form a frequency detector. By taking advantage of the behavior of the PFD, we integrate the output of the charge pump using a capacitor to obtain the frequency difference information in a digital fashion (Figure 4.20). The ability to re-use the available circuitry of the PLL for the calibration loop enables the use of this method with minimal area penalty. The control logic follows a SAR-like process to set all 12 bits of the current DACs according to the output of the frequency difference detector. The output of the calibration is stored in an internal register to be used as the reference for the frequency shifts.

The oscillator detector determines the other two operation modes. When the RF excitation signal is detected, the PLL switches to normal mode (Figure 4.19b). Here, the PLL loop is closed, the control logic is turned off, and V_{ref} and V_{CP} are disconnected. To avoid altering the PLL dynamics, the sampling capacitors C_3 and C_4 are initially disconnected from V_{ctrl} ($sa = 0$ and $\phi_3 = 0$). The global controller waits for ~20 μs for locking. Then, the signal pll_{sa} activates and enables the sampling of V_{ctrl}. To reduce the impact of the sampling capacitors to the PLL dynamics, C_3 is sized much smaller than the bigger capacitor of the loop filter C_1, while C_4 is sized to minimize variations in V_{ctrl} due to leakage. The switch-capacitor network samples charge from V_{ctrl} in C_3 during $sa = 1$ and dumps this charge to C_4 when $sa = 0$. This operation converges when the voltage across C_4 (V_{sa}) is equal to V_{ctrl}.

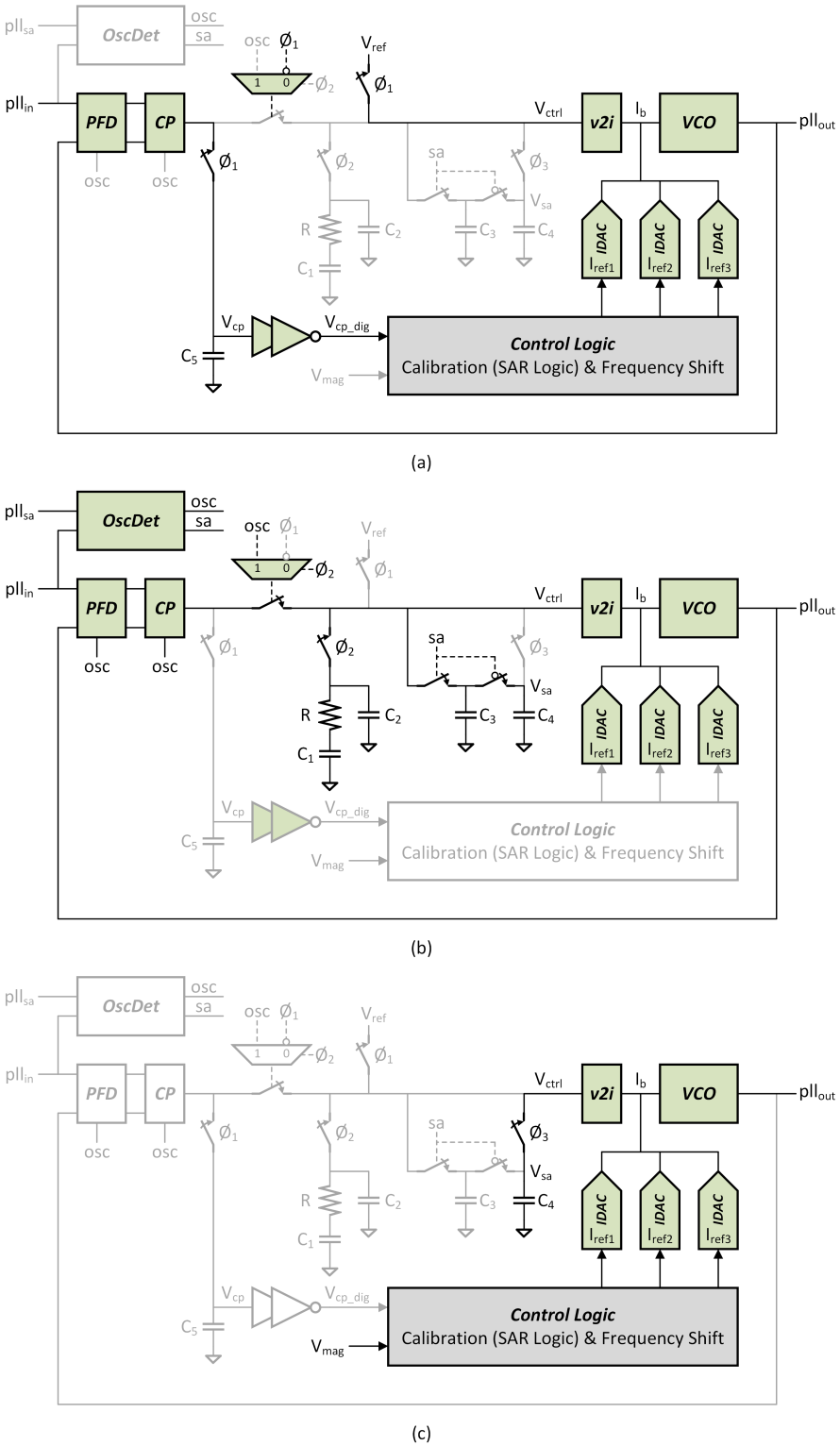


Figure 4.19: PLL operation modes. (a) Calibration mode. (b) Normal mode (c) Transmission mode.

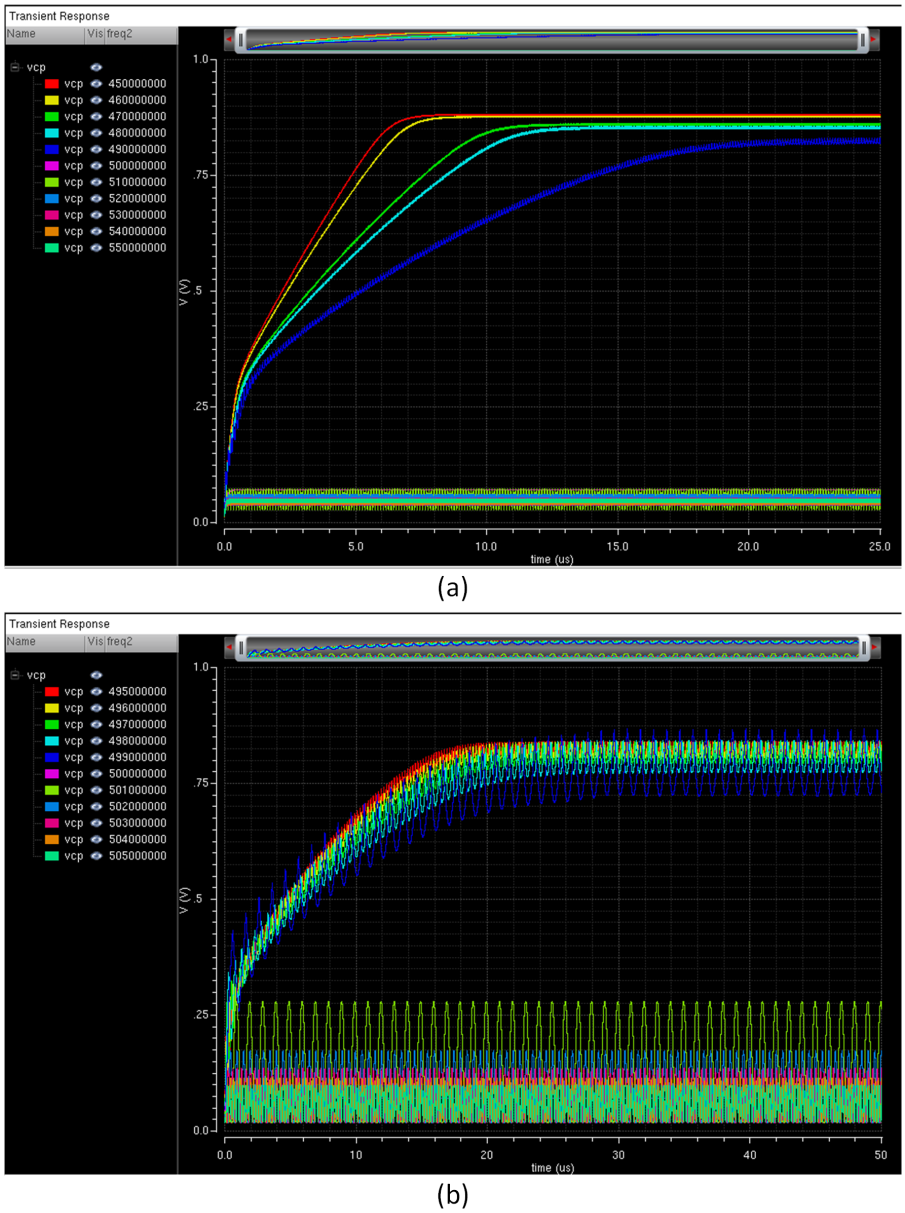


Figure 4.20: Simulation of the frequency detector with reference frequency set at 500 MHz. The figure shows the signal before the digital inverters. (a) Input frequency swept from 450 MHz to 550 MHz at 10 MHz steps. (b) Input frequency swept from 495 MHz to 505 MHz at 1 MHz steps.

When the RF excitation pulse ends, the oscillation detector senses this transition and the PLL switches to transmission mode (Figure 4.19c). All the components of the PLL are turned off except for the control logic, current DACs, $V2I$, and VCO. In addition, V_{sa} is connected to V_{ctrl}. During this mode, the VCO will be a free-running oscillator with a central frequency determined by V_{sa}. The frequency shift

is realized by shifting the digital values of the calibration DACs proportional to the measured magnetic field V_{mag}. The global controller keeps the PLL in this mode during a fixed time window (e.g., 1 ms) and then changes modes to wait for the next pulse. It is important to note that in this mode, the phase noise of the VCO plays an important role in determining the resolution of the localization in both frequency and phase encoding, as it has been discussed in the previous chapter.

The dynamics of the PLL are shown in Figure 4.21. The PLL has a bandwidth ω_n = 3.4 MHz and a damping ratio of ~0.71. Figure 4.22 shows simulation results of PLL locking from two different initial conditions. The PLL has a locking time of ~5 μs with a single overshoot. Figure 4.23 shows the simulation results of the behavior of the PLL when the reference signal is turned off. We can see how a traditional PLL locks to the RF excitation pulse and, when the pulse ends, it tries to follow the input and reduces its oscillation frequency. This is indicated by V_{ctrl} reducing to 0 V. In the second case, we enable the Oscillation Detector circuit. Here, V_{ctrl} does not decrease to zero, but because of the delay in the oscillation detector circuit (as we will see below) it does jump to an undesired value. Finally, once the oscillation

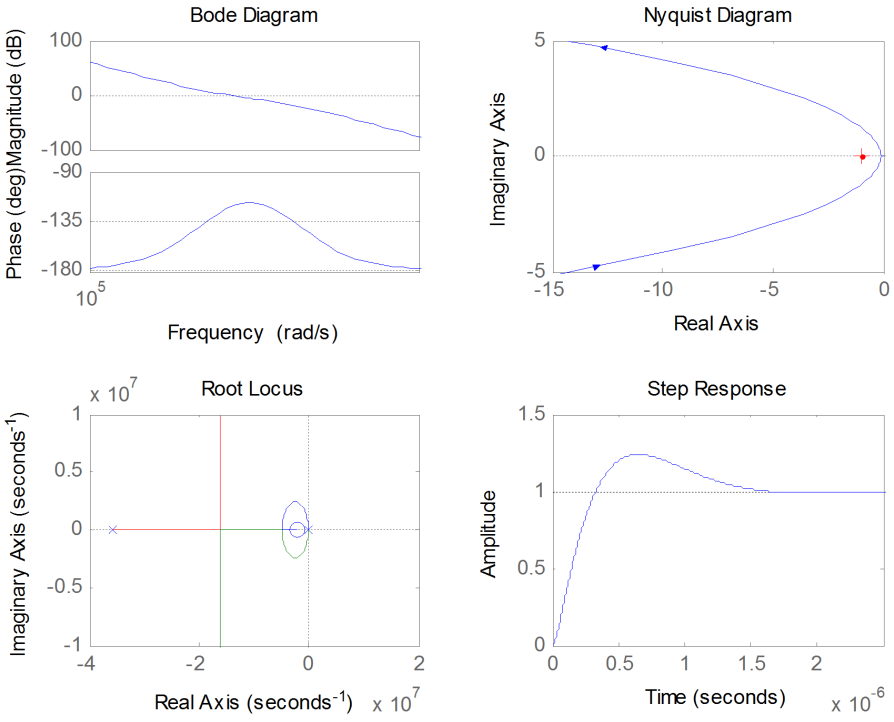


Figure 4.21: PLL dynamics using a MATLAB model.

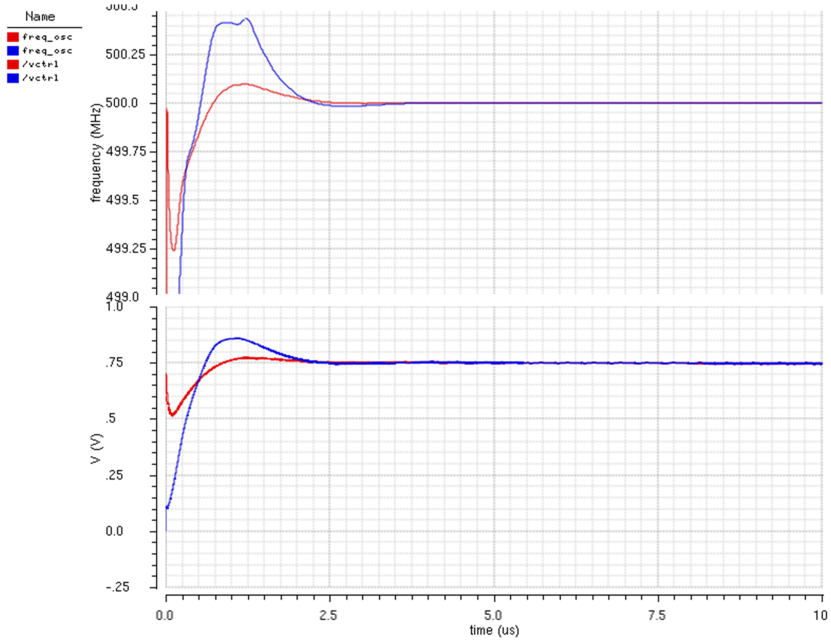


Figure 4.22: PLL locking from two different initial conditions.

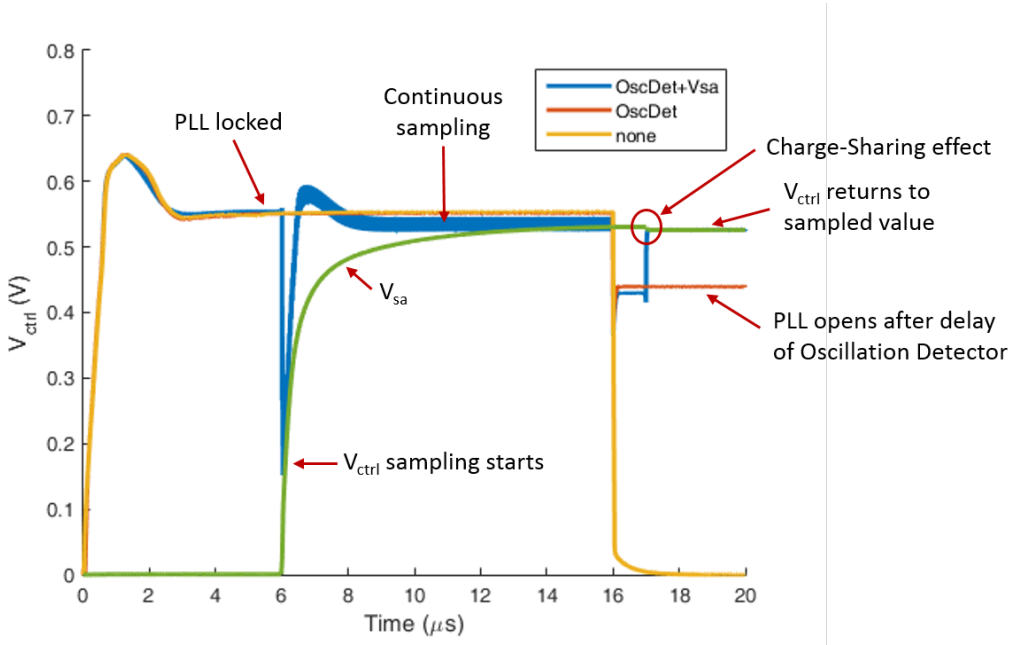


Figure 4.23: PLL behavior when reference signal is turned off and comparison with a traditional implementation.

detector and the sampling of V_{ctrl} are enabled, we notice that the value of V_{ctrl} is restored to its original value except for a minor difference due to charge-sharing.

After describing the behavior of the PLL as a system, we now describe the design

of its different components below.

Oscillation Detector

In order to sense the presence of the reference signal, we detect the presence of an oscillating signal. Given that the reference is a square signal, the detector can be accomplished by detecting the edges or transitions. Next, we convert the narrow pulses to a digital signal using an asymmetrical charging stage. The schematic of the proposed oscillation detector is shown in Figure 4.24. The edge detector is realized by connecting the input and a delayed version of it to a XOR gate. The asymmetrical charging stage is implemented by connecting a capacitor to an inverter with a weak pmos and a strong nmos. This configuration allows for a long charge and a fast discharge of the capacitor.

The current implementation of the detector is shown in Figure 4.25. Since we are pushing the limits of the technology by targeting a 1 V supply with 1.8 V devices, the parasitics and speed are limited in the design of this block. To reduce power consumption, we minimize the load of the delay stage by simplifying the implementation of the XOR gate while keeping its functionality. The charging capacitor is implemented by the parasitic capacitance of the asymmetric inverter and the following buffer (node d). In addition to the oscillation detector, we take advantage of the fact that we are detecting the edges of the reference signal to generate the sampling signal sa which is used to sample V_{ctrl}. This signal is generated by buffering the output of the XOR gate (node c) and adding an enable gate for the gating signal pll_{sa}. The simulation results can be seen in Figure 4.26. We can see that the reference signal is detected correctly. The difference in the detection delay of the presence (begging of the pulse) and absence (end of pulse) is due to the asymmetrical charge of the capacitor.

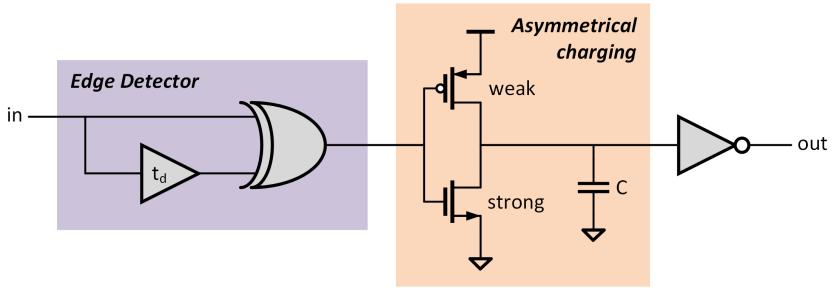


Figure 4.24: Oscdet model.

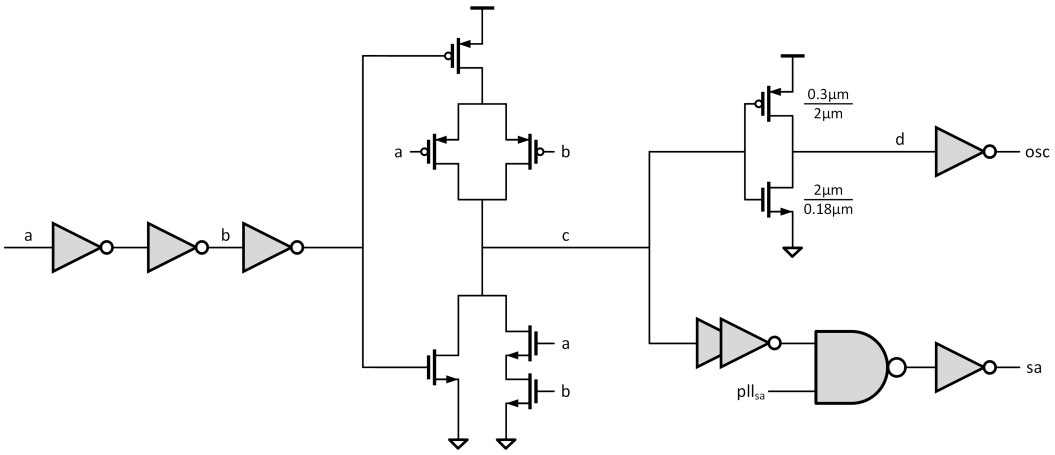


Figure 4.25: Oscdet PulseGen schematic.

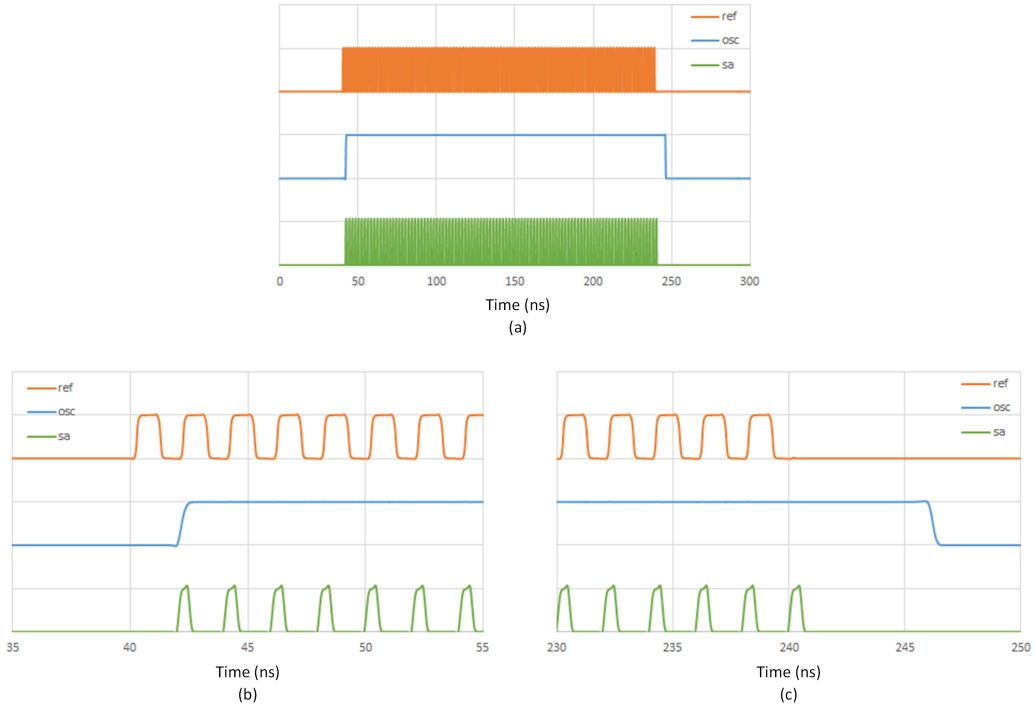


Figure 4.26: Simulation results of the Oscillation Detector. (a) Response to a 500 MHz pulse of 200 μs. (b) Zoom-in to the beginning and (c) end of the pulse.

Phase-Frequency Detector

The design of the PFD is based on the traditional PFD architecture with a minor modification to allow control of its behavior by the oscillation detector (*osc* signal). The model of the proposed PFD is shown in Figure 4.27. We add a multiplexer to control the reset of the flip-flops. When there is a reference signal, $osc = 1$ and

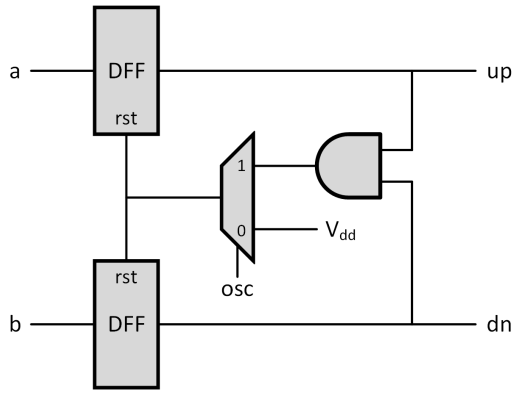


Figure 4.27: PFD model.

the PFD operates normally. In the absence of a reference signal, $osc = 0$, the reset of the flip-flops are activated and both outputs *up* and *dn* are set to 0, canceling any further action of the PFD. Figure 4.28 shows the schematic of the PFD. This topology is based on the pass-transistor logic presented in [REFs], which is derived from the model in 4.27 by simplifying the architecture using true single-phase clock (TSPC) flip-flops. To save power, the multiplexer is incorporated directly in the NAND gate.

Figure 4.29 shows the simulation results of the PFD. As shown in Figure 4.29a, the PFD range is severely reduced when *svt* devices are used, while the range is restored when *lvt* devices are used. To achieve correct operation under low supplies, we decide to use *lvt* devices at the expense of higher power consumption compared to *svt* devices (Figure 4.29b).

Charge-Pump

The schematic of the charge-pump is shown in Figure 4.30. It is based on a traditional cascode topology where *up* and *dn* switches are placed next to the supplies to minimize charge-injection into the output. This stage has a gain of 8 to reduce power consumption. Two transistors are added to the output stage to turn off the charge-pump output in the absence of a reference signal ($osc = 0$).

In addition, we also designed a differential topology that can be used if the outputs of the PFD are differential (Figure 4.31). This topology is based on current-steering, and further reduces the charge-injection effects at the output of the charge-pump. Similar to the previous design, two transistors are added to turn off the output stage in the absence of a reference signal.

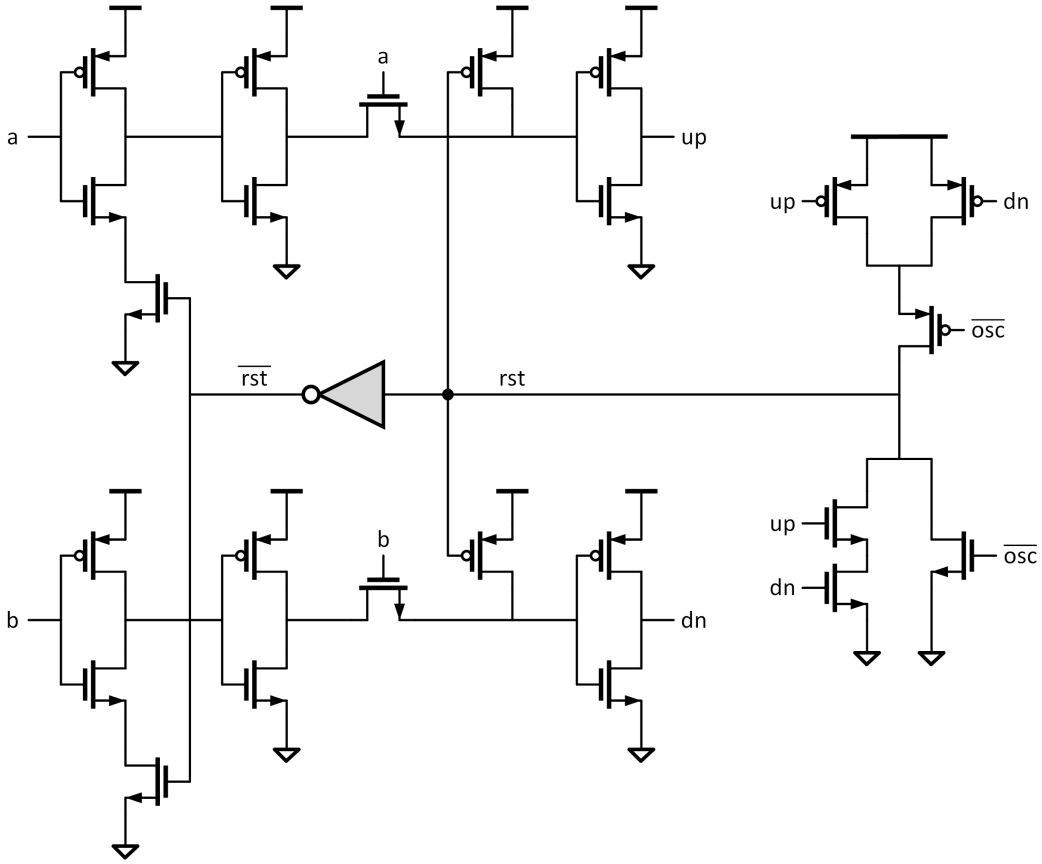


Figure 4.28: PFD schematic.

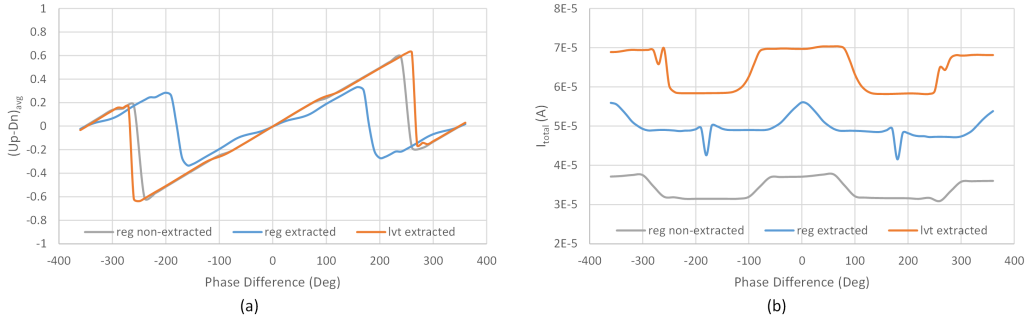


Figure 4.29: (a) Output response and (b) power consumption of the PFD for three different cases. We can notice the performance degration due to parasitics.

Voltage-Controlled Oscillator

We use a current-controlled ring oscillator and a voltage-to-current (*v2i*) stage as the VCO (see Figure 4.17). We choose a ring oscillator instead of an LC oscillator because of its small area and lower power consumption. Although ring oscillators have higher phase noise compared to LC oscillators, the phase noise requirements

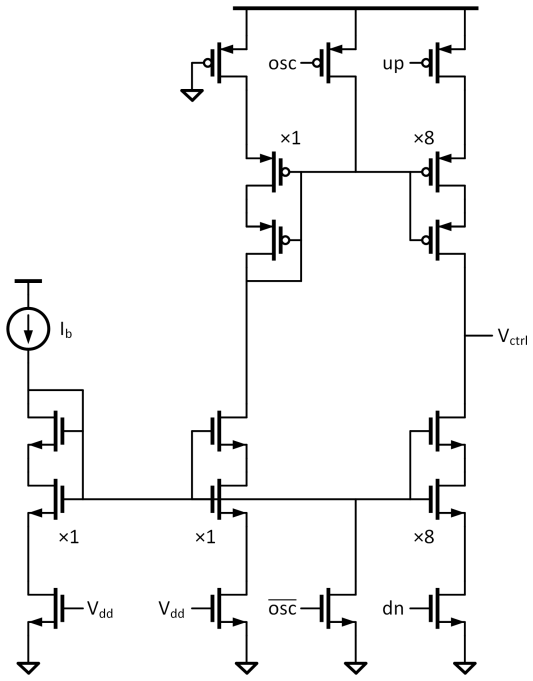


Figure 4.30: Schematic of the Charge-Pump.

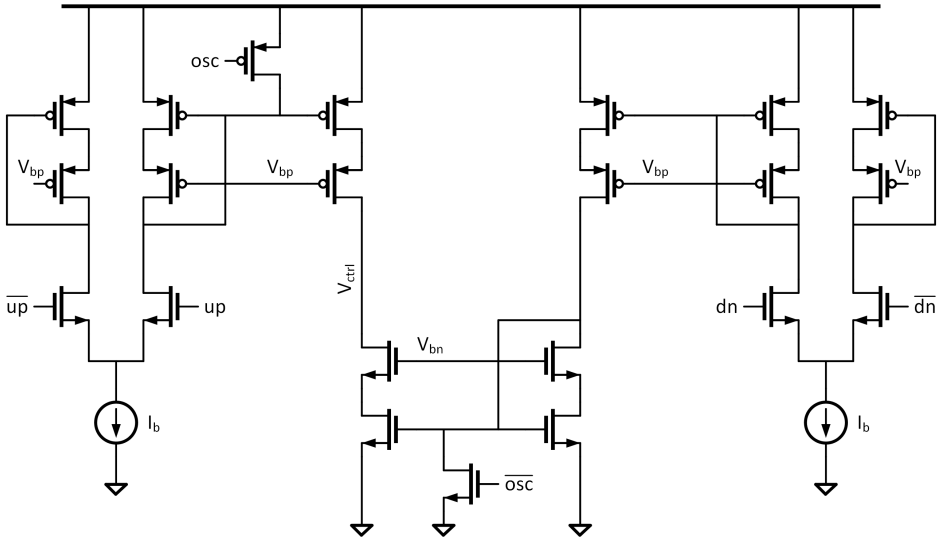


Figure 4.31: Schematic of a differential Charge-Pump.

can be relaxed by adjusting the bandwidth of the external receiver.

The schematic of the differential two-stage ring oscillator is shown in Figure 4.32. Current-starved inverters are used as the delay elements. Varactor-based delay elements can also be used but the available varactors in this technology were limited in area (the smallest available varactor was too big). Although we could design a

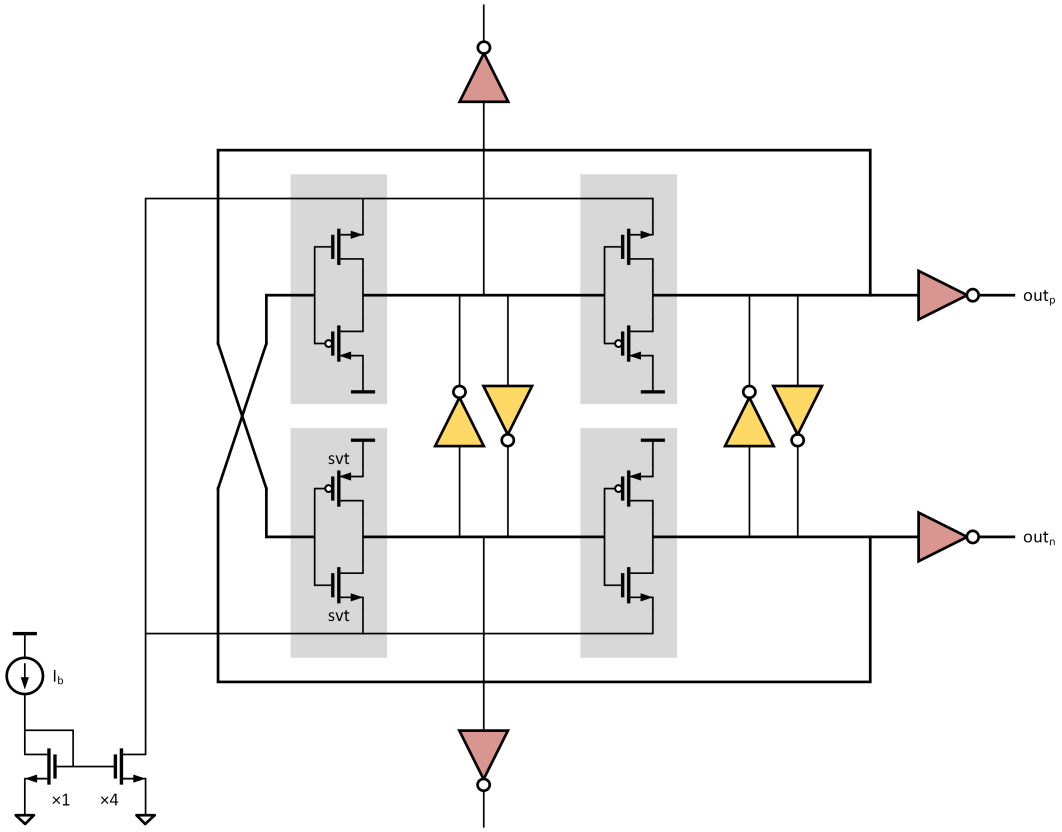


Figure 4.32: Schematic of the VCO.

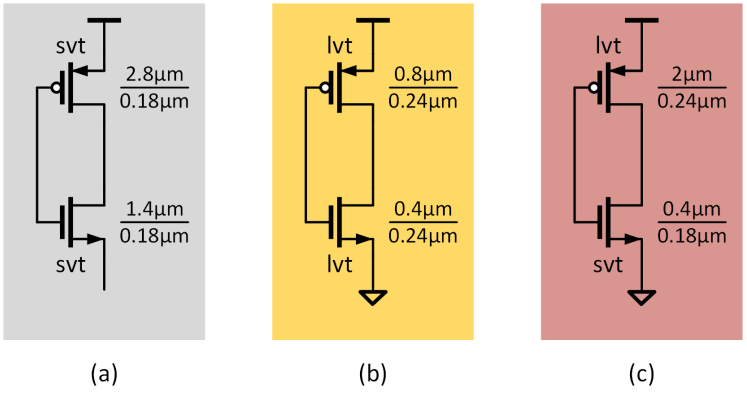


Figure 4.33: VCO inverters.

custom varactor, we decided to use instead a current-starved inverter as the delay element.

The oscillation frequency of the ring oscillator is controlled by the input current I_b, as the delay in each delay element changes in inverse proportion to I_b. As such, the oscillation frequency increases in proportion to I_b. To minimize power consumption,

we design this stage with a supply voltage of 1 V. Since we are using 1.8V devices, this constraint creates many challenges in the design of the oscillator. Due to the low supply, only NMOS current starvation is used. This creates an asymmetry in the rising and falling times which is corrected in the sizing of the output stage, as described below. We use standard-Vt (svt) transistors in the delay elements because they provide a good balance between power consumption and area. Cross-coupled inverters are used to reduced duty-cycle distorsion, and are implemented using low-vt (lvt) devices to reduce power consumption at lower supplies. The output stage (buffers) are designed to correct for the asymmetrical transition times. These inverters are designed using a svt nmos and a lvt pmos. The svt nmos ensures a slower transition when the output of the current-starved inverters transitions from 0 to 1 (fast rising time), while the lvt pmos creates a faster transition in the opposite case (slow falling time). This technique compensates for the asymmetrical transition times in the delay elements and provides a 50% duty-cycle output. The final sizing of all the inverters in the ring oscillator is shown in Figure 4.33.

To connect the output of the charge-pump to the ring oscillator, we use a voltage-to-current stage as shown in Figure 4.34. A rail-to-rail input stage of a svt nmos (MN) and a svt pmos (MP) are used. The other transistors in this stage are lvt transistors. Current mirrors are used to copy the current of the input stage to the output. An

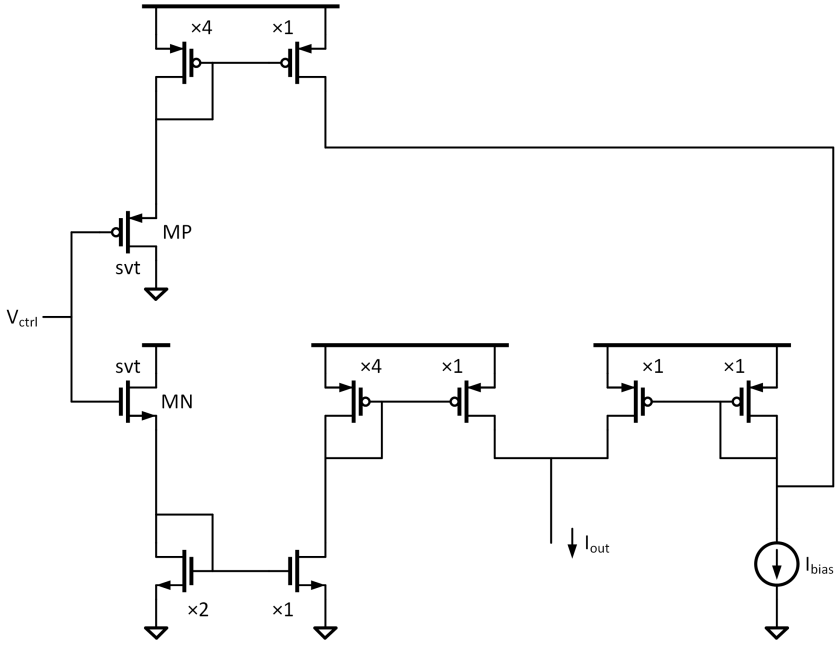


Figure 4.34: Schematic of the voltage-to-current stage (v2i).

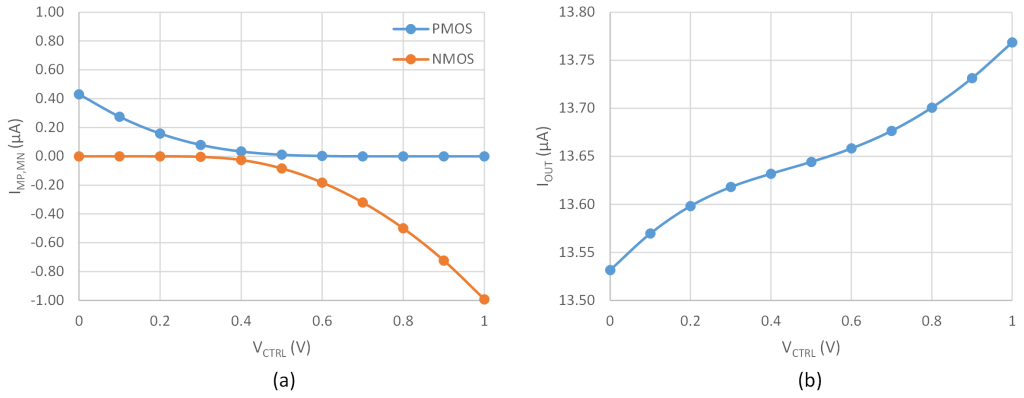


Figure 4.35: (a) Drain current of transistors of the input stage as a function of the control voltage V_{ctrl}. (b) Output current as a function of V_{ctrl}.

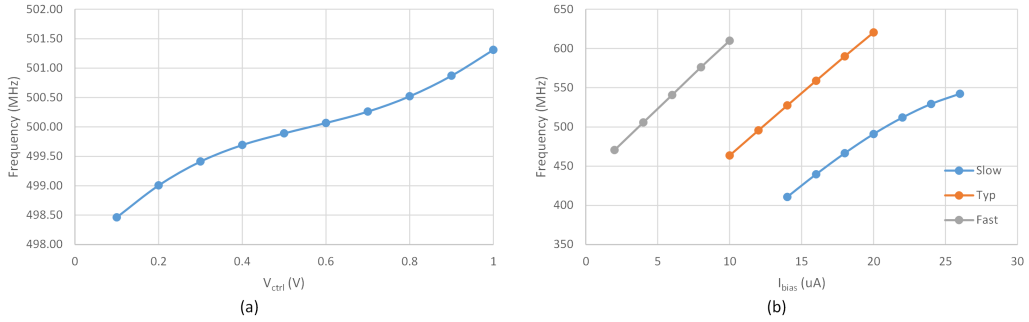


Figure 4.36: (a) Oscillation frequency of the VCO as a function of the control voltage V_{ctrl}. (b) Corner simulations as a function of bias current I_{bias}.

additional current source is used to set the bias point of the output. Since the strength of the nmos is close to twice of the pmos, the net gain of the current mirros for the MN branch is half as of the one for the MP. The final sizes of MN and MP match the strengths of each branch from input to output. Figure 4.35 shows the simulation results of this stage.

Simulation results of the VCO are shown in Figure 4.36. The oscillation frequency changes proportional to V_{ctrl}, and shows a K_{VCO} of 3 MHz/V. Corner simulations are also shown in the figure. The VCO can oscillate at the desired frequency of 500 MHz in all cases. However, it is necessary to add a calibration stage to change the bias current I_b accordingly. The bias current needs to change between 2 μA to 25 μA to cover slow and fast corners. Since K_{VCO} is 3 MHz/V, the calibration resolution needs to be less than $K_{VCO}/2$. Thus, for a Δf of ~1 MHz, a ΔI_b of ~64 nA is required. We set the LSB of the calibration to be 50 nA. To cover the whole

range, a 10-bit DAC is needed. We implement this DAC by using three 4-bit current DACs, which uses less area than a full 10-bit DAC. The calibration method follows a SAR-like process, as explained before, and ensures an oscillation frequency between ±1 LSB around the target frequency.

4.7 Power Amplifier and RF Receiver

The power amplifier (PA) and RF receiver directly interface with the RF coil to either transmit the response of the chip (shifted frequency signal) or receive the incoming RF pulse. The schematic of this stage is shown in Figure 4.37. It has two modes of operation depending on the value of coil_{sel}: transmitter (TX, $\text{coil}_{\text{sel}} = 1$) or receiver (RX, $\text{coil}_{\text{sel}} = 0$).

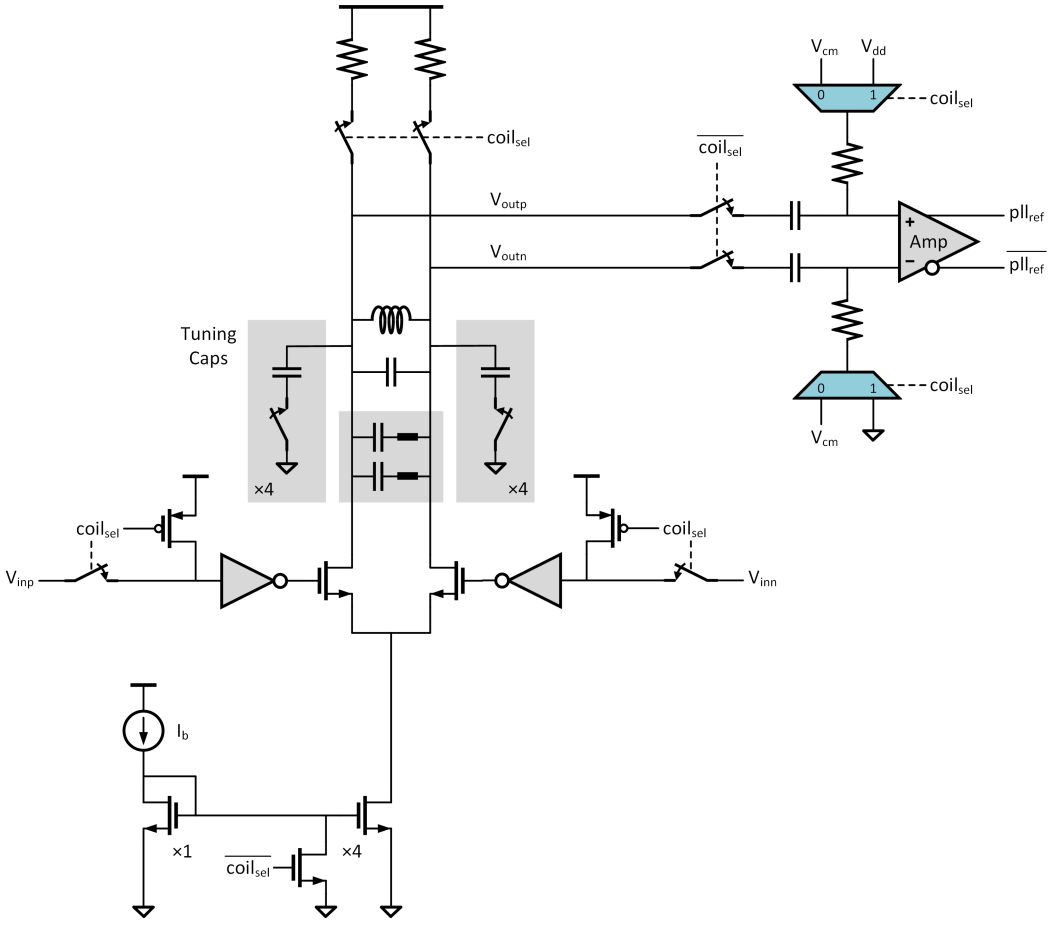


Figure 4.37: Schematic of the power amplifier and RF receiver.

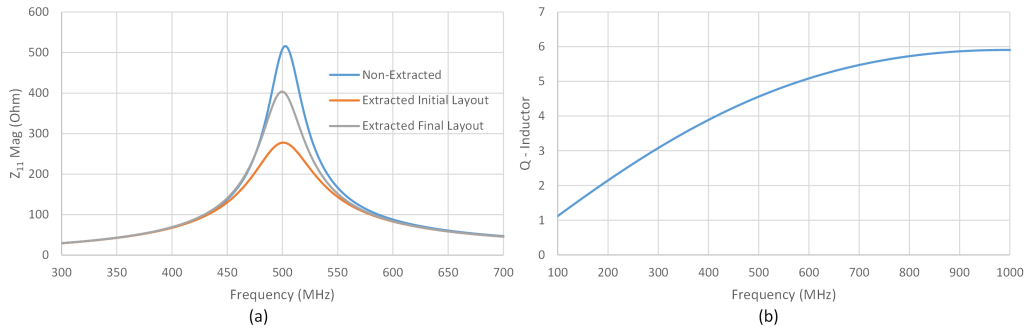


Figure 4.38: (a) Magnitude of the impedance of the on-chip coil before and after layout. (b) Q of the inductor as a function of frequency.

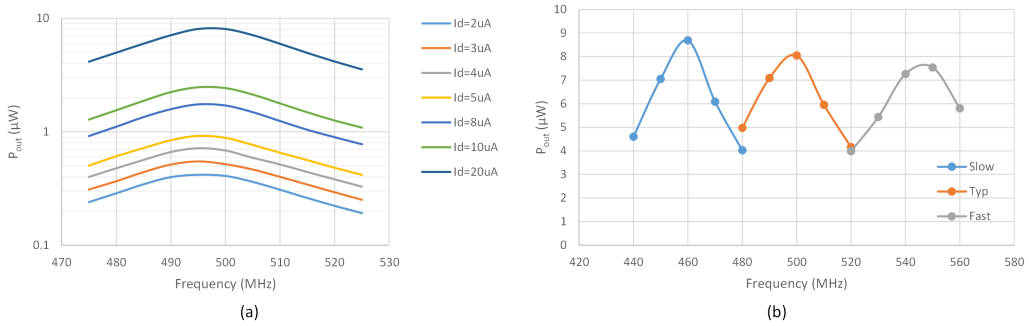


Figure 4.39: (a) PA output power as a function of frequency for different bias current. (b) Corner simulations of PA output power.

Power Amplifier and on-chip RF Coil

The design of the PA and the on-chip RF coil was optimized for near-field interactions due to the target operating frequency of 500 MHz. In this frequency ranges, the main source of interaction between the on-chip coil and the external reader is in the near-field regime ($\lambda << d_{\text{separation}}$). We maximize the quality factor (Q) of the coil at 500 MHz while utilizing the maximum area allocated for the coil. In this designed, the on-chip coil has a size of 420 μm $\times$ 420 μm. Figure 4.38a shows the impedance of the resonated coil before and after layout. We see that our initial layout reduces the Q of the inductor significantly due to thinner connecting traces. We modified the layout, increasing the width of these traces and therefore reducing the overall coil resistance. The final layout improves upon the initial one, increasing the impedance by a factor of ~40%. A numerical simulation using a 3D field solver shows a quality factor of 4.6 at 500 MHz (Figure 4.38b). The PA is a differential common-source stage with resistive load. Two inverters are added to drive the differential pair. The value of the resistor is chosen so that the current through the inductor is maximized.

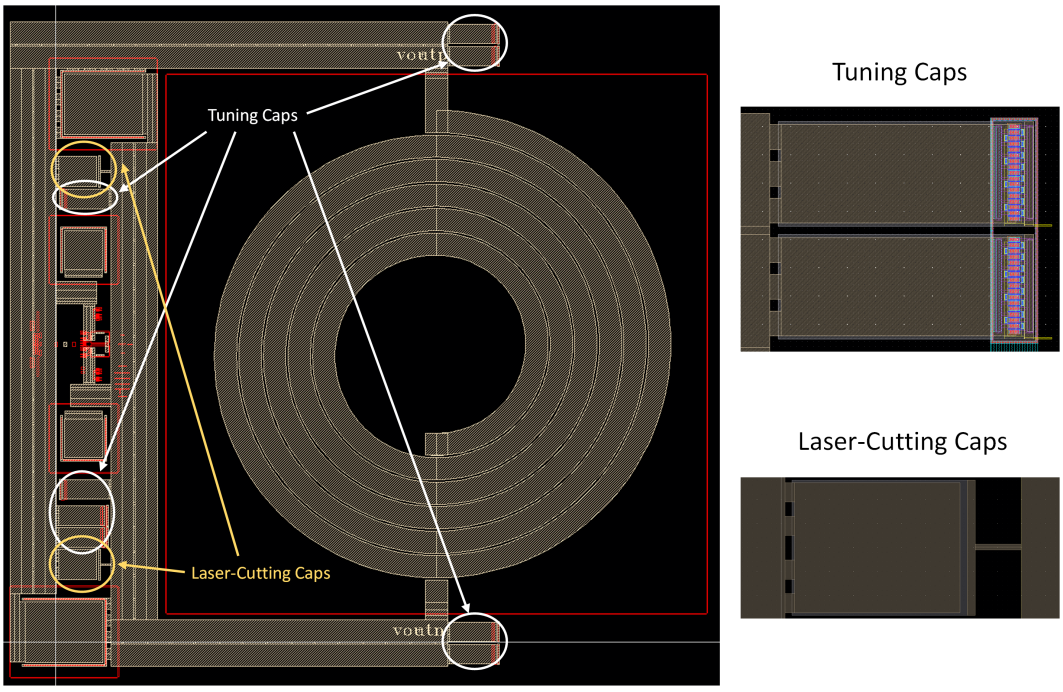


Figure 4.40: On-chip coil layout with tuning capacitors for process variation correction.

The output of the PA (drains of the differential pair) is connected to the coil, which is resonated by a capacitor. Figure 4.39a shows simulation results of the output power of the PA as a function of frequency. As expected, the output power increases as the bias current of the PA increases, allowing control of the output power. Figure 4.39b shows corner simulations for a fixed bias current as a function of frequency. We can see that the resonance frequency of the LC tank changes significantly from the target frequency and needs to be compensated. Additional capacitors are added to the LC tank to provide calibration in two ways: by laser cutting and by tuning capacitors. The implementation of both techniques is shown in Figure 4.40.

Simulation results of the resonance frequency tuning are shown in Figures 4.41-4.43. An initial corner analysis of the resonance frequency of the LC tank shows a variation of ~100 MHz around the center frequency. Trimming of the laser-cutting capacitors moves the resonance frequency of the typical case to 525 MHz and 554 MHz, respectively. The tuning capacitors reduce the resonance frequency of each case by ~10 MHz per step, with a total of four steps.

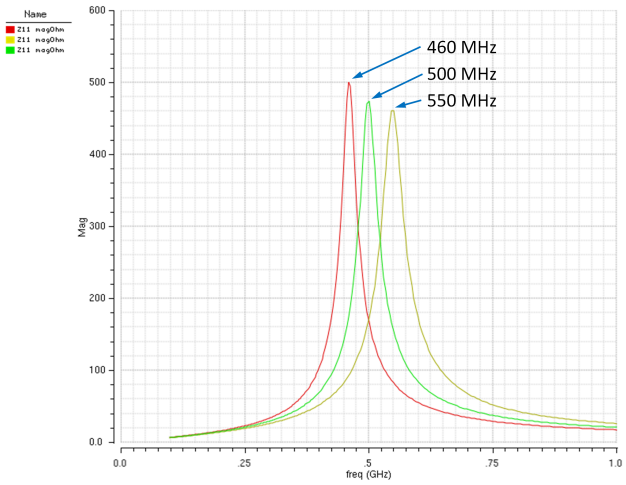


Figure 4.41: Corner simulation of the on-chip coil impedance.

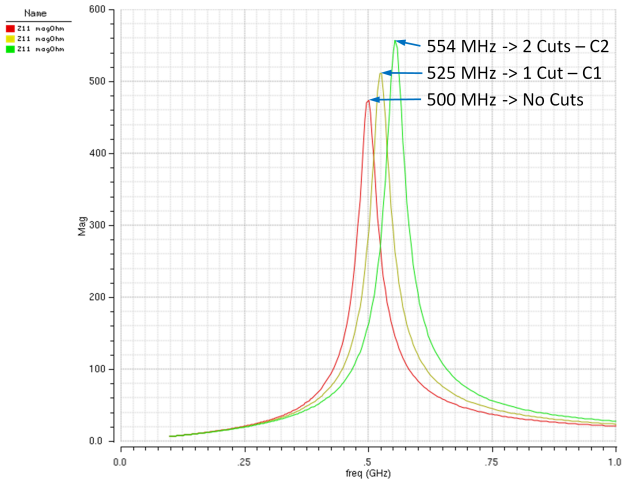


Figure 4.42: Tuning of on-chip coil resonance frequency due to laser-cut capacitors.

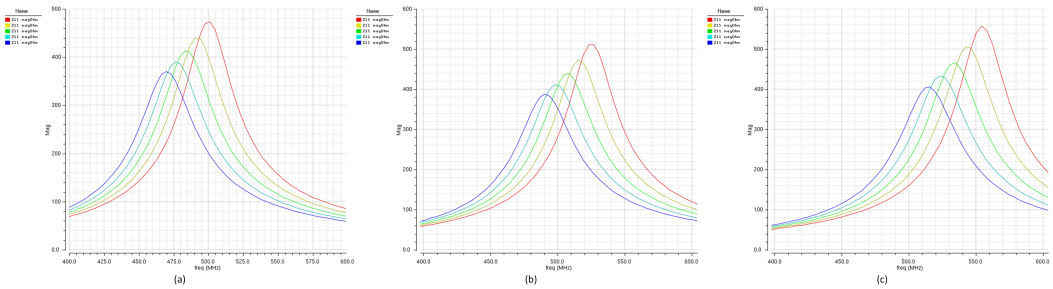


Figure 4.43: Tuning of on-chip coil resonance frequency due to tuning capacitors. (a) No cuts. (b) One cut. (c) Two cuts.

RX Amplifier

The excitation RF pulse gets captured by the on-chip coil and amplified by the RX amplifier. This signal needs to be amplified to CMOS levels to be used as the

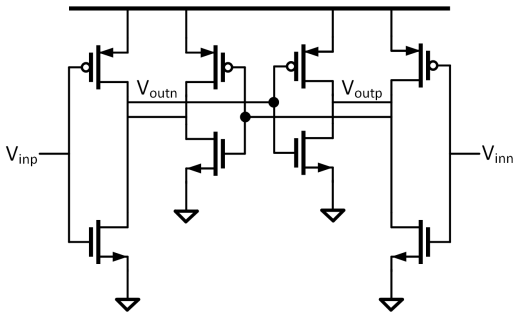


Figure 4.44: PA amplifier 1.

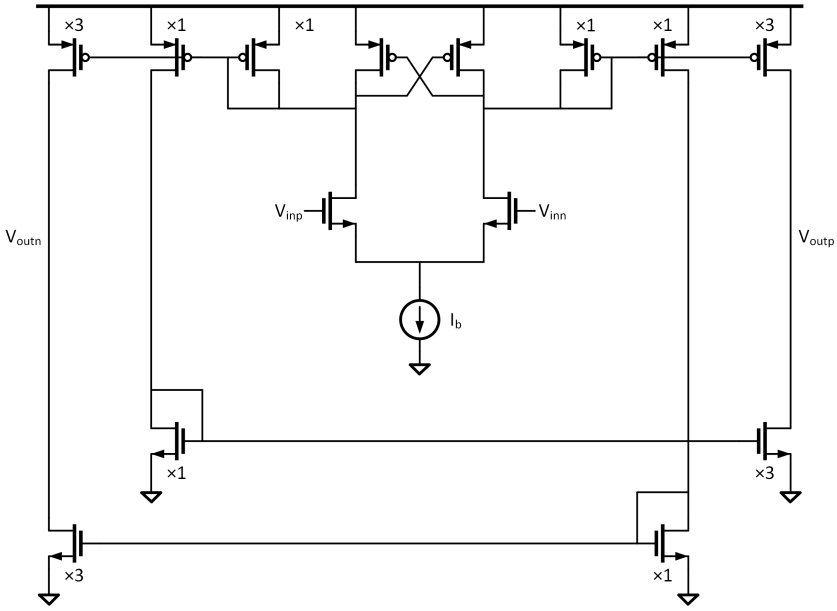


Figure 4.45: PA amplifier 2.

reference signal for the PLL. As shown in Figure 4.37, the amplifier is biased using to resistors that connect the input common mode V_{cm}. The gain of this stage depends on the coupling between the on-chip coil and the coil of the external reader. As such, we explore two different designs.

Figure 4.44 shows the schematic of the RX amplifier used in this design. The gain of this stage is defined by the size of the input inverters. The advantage of this stage is its compatibility with low supplies due to the stack of only two transistors. However, once the transistors are sized, the gain is set and it can only be changed by a change in the supply voltage. The cross-couple inverters provide positive feedback which increases the overall gain of the input stage. The output inverters (not shown in the figure) set the CMOS levels and drive the output load.

Another approach is to use the differential amplifier shown in Figure 4.45. Similar to the previous case, the cross-couple transistors provide positive-feedback which increases the gain of the first-stage. The addition of a second gain-stage increases the overall gain of the amplifier in comparison with the previous case at the expense of extra power consumption. The output needs to be converted to CMOS levels by adding a couple of buffers. One advantage of this topology is that the gain of the amplifier can be changed by changing the bias current.

Chapter 5

ATOMS: MEASUREMENT RESULTS

In this chapter, we present the characterization of the internal blocks as well as the system level performance. After we describe the electrical test bench results, we focus on localization experiments both *in vitro* and *in vivo*. We develop an algorithm to estimate the location of ATOMS devices in 1D and 2D experiments using frequency encoding. Finally, we test our device *in vivo* in an animal model, achieving sub-millimeter localization resolution.

As a first proof-of-concept, we targeted a resonance frequency (f_0) of 500 MHz to emulate a small 11.7 T MRI system, and utilized frequency encoding as the localization method. As we discussed in the previous chapter, the system architecture

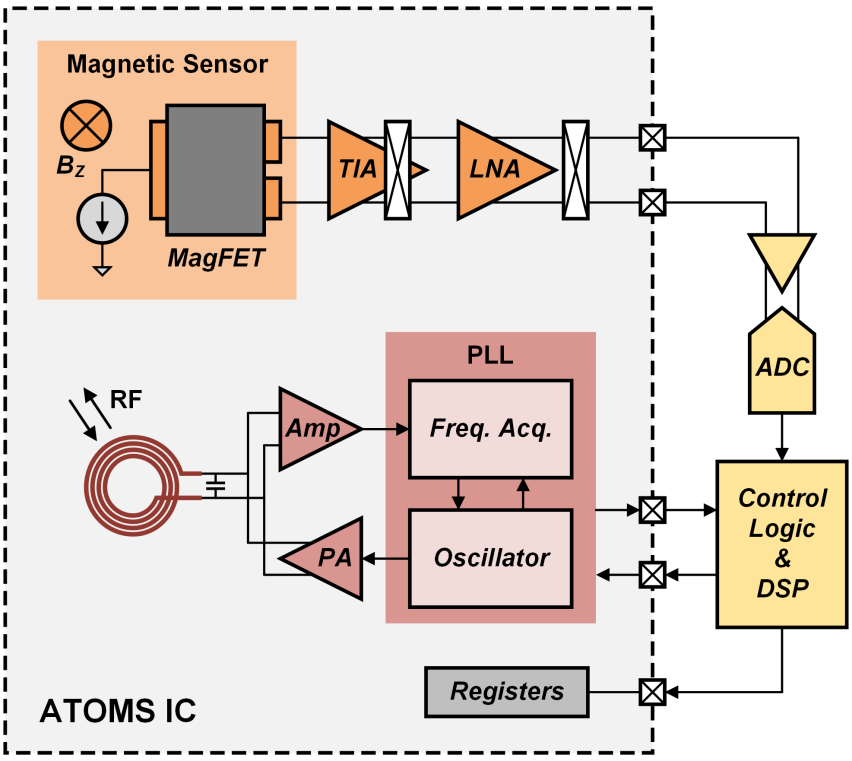
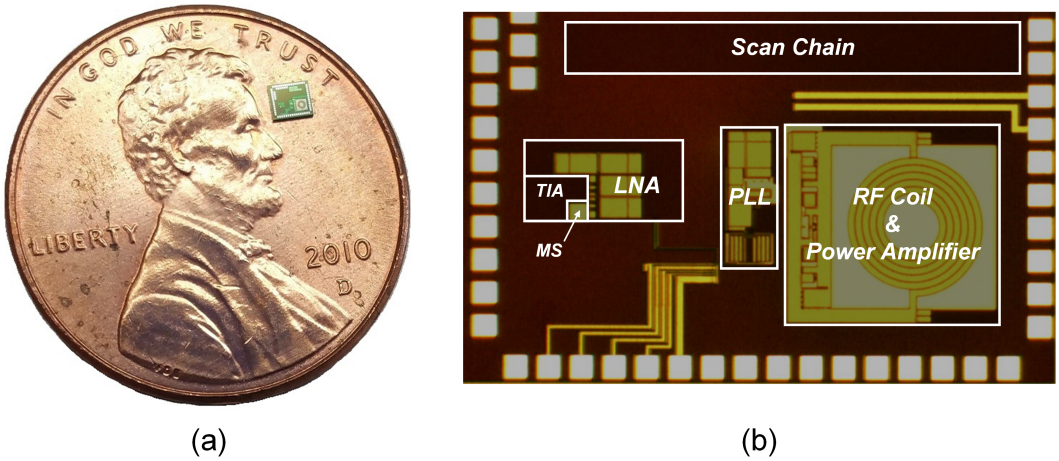


Figure 5.1: System architecture of the current ATOMS device, featuring an on-chip magnetic field-sensitive field-effect transistor (MagFET), TIA, LNA, an on-chip RF coil, PLL, and PA. The ADC and Control Logic with DSP are implemented externally.



(a) (b)

Figure 5.2: (a) ATOMS microchip compared with a US penny and (b) die micrograph. The chip has a size of 1.8 mm × 1.2 mm.

of the chip consists of a magnetic sensor, a two-stage chopper amplifier, an ADC, a PLL, a PA, an on-chip coil, and a control logic with DSP (Figure 5.1). The magnetic sensor is an on-chip MagFET that measures the applied magnetic field orthogonal to the chip (B_Z). The output current of the MagFET is amplified by a two-stage chopper amplifier, which is formed by the TIA and LNA. The output of the amplifier is then digitized for processing (e.g., averaging) and storage. The on-chip coil is resonated at f_0 using an on-chip capacitor. The coil acquires the excitation RF signal and emits the response of the chip. The PLL locks the internal oscillator to the RF pulse during the excitation phase. During the transmission phase, the frequency of the internal oscillator is shifted proportionally to the measured magnetic field and is fed to the PA for transmission. The control logic manages the whole operation of the chip and processes the measured magnetic field. It was implemented externally in an FPGA, where the controller run at 1 MHz due to the serial communication of 150 bits, and the DSP run at 763 Hz. The chip was fabricated in a standard 180 nm CMOS process and occupies an area of 1.8 mm × 1.2 mm (Figure 5.2).

5.1 Test Setup for Bench and *In Vitro* Experiments

An illustration of the test setup used for bench experiments and *in vitro* experiments is shown in Figure 5.3. Pictures are shown in Figures 5.4 and 5.5. The ATOMS chip was placed in a small daughter PCB and connected using wirebonds. This PCB was connected to a mother PCB which interfaces with the ADC, FPGA, and voltage and current sources. The PCBs were fabricated on a standard 4-layer 0.062" FR4 substrate. The outputs of the chip's LNA were buffered using an

AD8512 dual amplifier from Analog Devices in a voltage-follower configuration. The buffered outputs of the chip were digitized by an AD7450 12-bit ADC from Analog Devices. The ADC interfaces directly with the FPGA. The FPGA was a Cyclone IV EP4CE115F29C7 from Altera, and was integrated in a DE2-115 development board from Terasic. The FPGA interfaced directly with the ADC, processed the digitized data and controlled the operation of the chip. The FPGA code was written in Verilog HDL. A MSO7104B mixed-signal oscilloscope from Keysight was used to visualize the output of the chip and other control signals.

The RF pulse was applied via a 4-turn coil which was connected to a matching network. The coil had a diameter of 5 mm and was manually wounded using copper wire with a diameter of 320 μm. The coil was aligned with the chip and placed at ~3 mm distance from it. The RF signal was generated by a MG3694B signal generator from Anritsu and was amplified by a ZHL-20W-13SW+ power amplifier from MiniCircuits. Semirigid coaxial cables were used to connect the coil and matching network to the output of the power amplifier. The RX channel used a second coil which is similar to the transmit coil. A similar matching network was also used. The signal from the chip was picked up by the coil and amplified by a chain of 3 ZX60-P33ULN+ low-noise amplifier from MiniCircuits. The output of the amplifier is sent to a DSA90804A real-time oscilloscope and an E4440A spectrum analyzer,

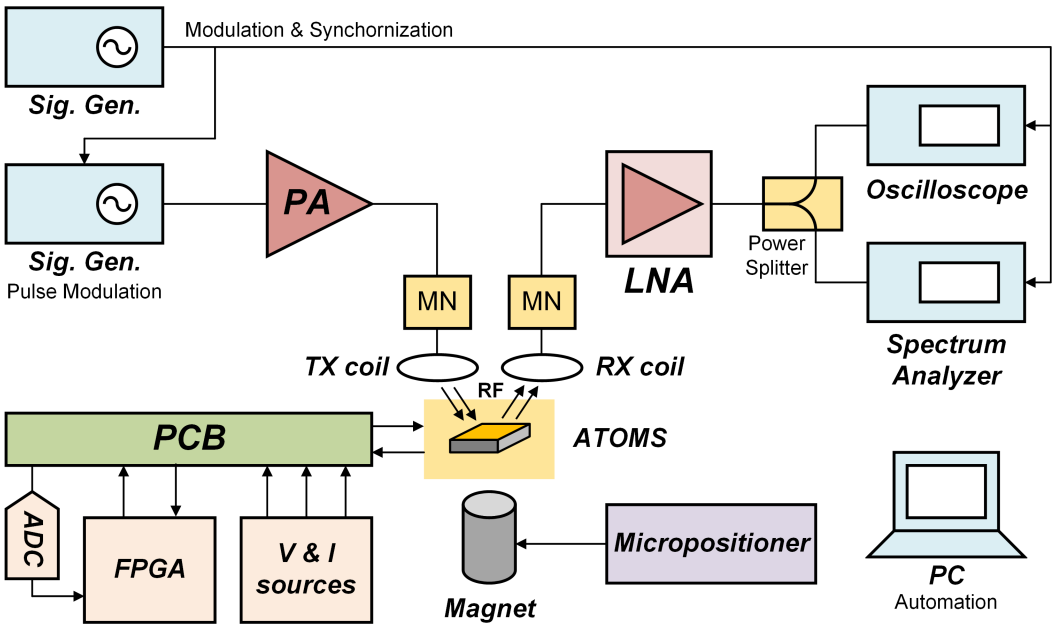
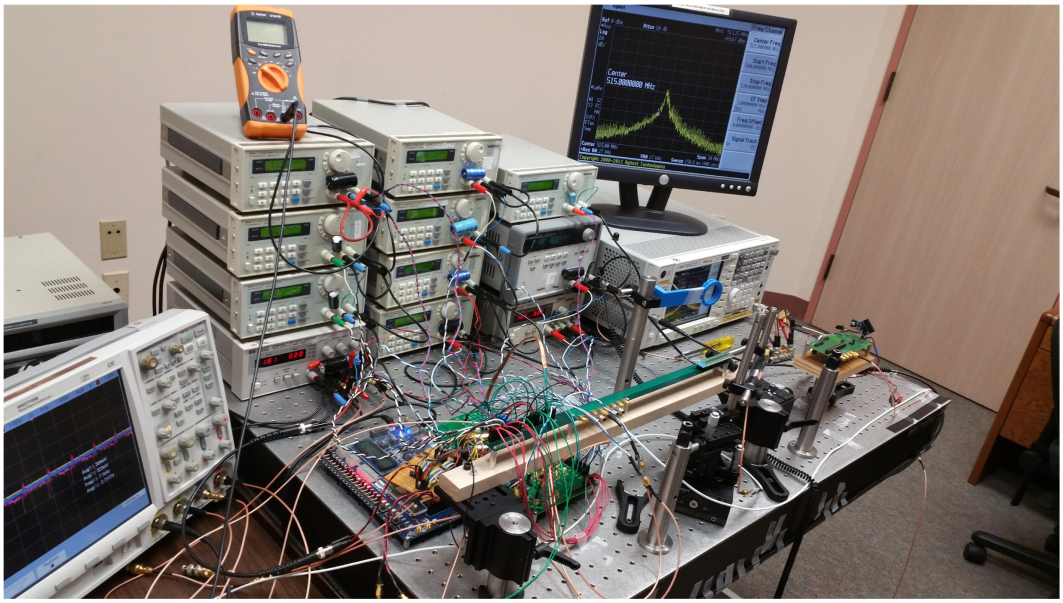
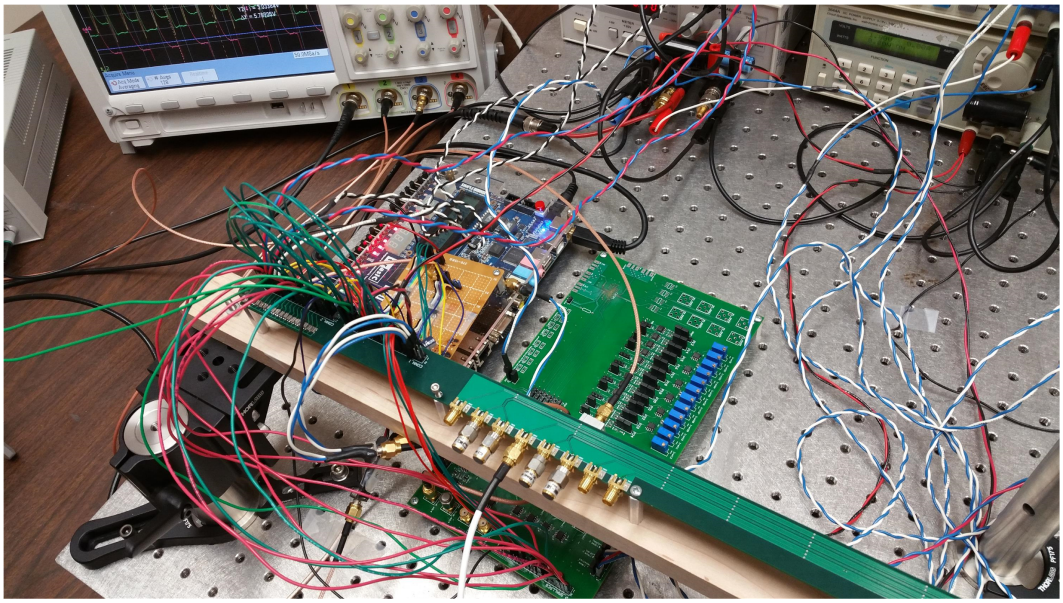


Figure 5.3: Illustration of the Test Setup for bench and *in vitro* experiments.



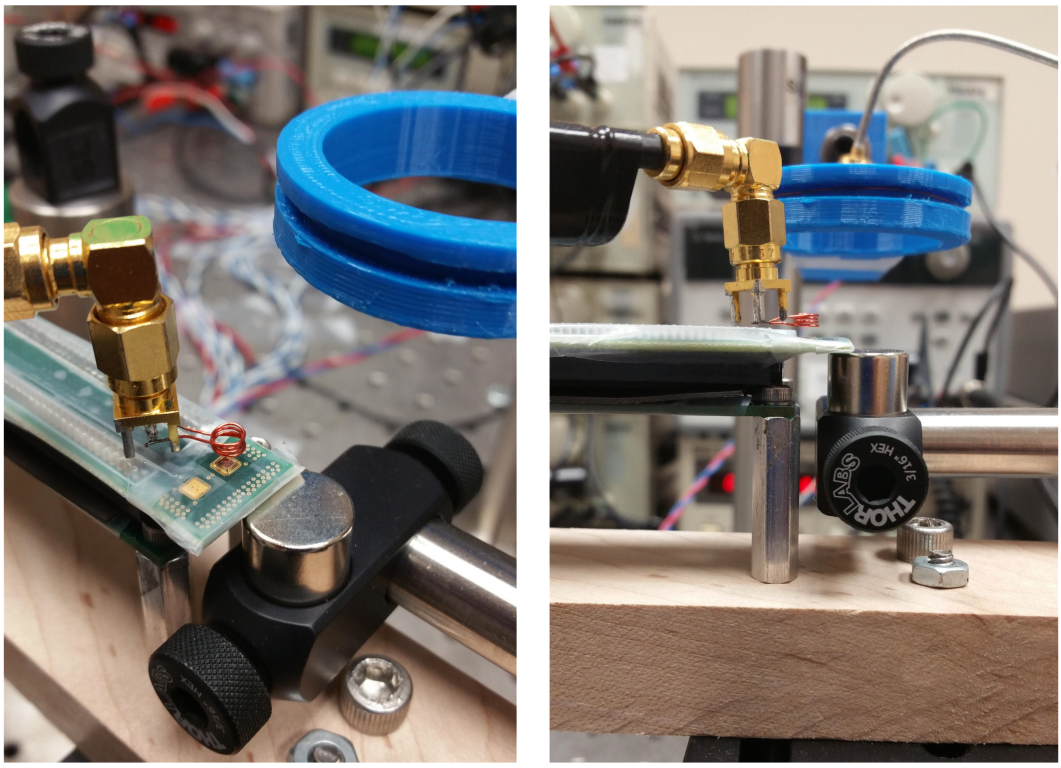
(a)



(b)

Figure 5.4: Pictures of the Test Setup for bench and *in vitro* experiments. (a) Test setup and (b) PCBs and FPGA board.

both from Keysight. Pulse modulation of RF signal and synchronization between TX and RX channels was performed using a 33522B waveform generator from Keysight. The whole test setup was automated and controlled by a custom script written in MATLAB. The magnetic field was generated using an NdFeB grade N40



(a) (b)

Figure 5.5: Zoomed picture of the chip, transmit coil and receive coil. (a) Angled and (b) side views.

magnet from MAGCRAFT, with a size of 0.5" diameter × 1" length. The distance between the chip and the magnet was controlled by moving the magnet using a micropositioner.

Magnet Characterization

We first characterized the magnetic profile generated by the permanent magnet. We aligned the chip with the magnet in the same axis and placed the sensor probe in close proximity to the chip. Then, we moved the magnet along this axis and measured the magnetic field using a 3-axis gaussmeter. Figure 5.6 shows pictures of the characterization process.

The measurement results are shown in Figure 5.7. The total magnetic field decays as a function of distance, with a maximum field value of ~200 mT. Similarly, the field orthogonal to the probe (and the chip) B_Z decays as the distance increases. The other two components have a different behavior, with a peak around a distance of 2 mm. For our purposes, we are interested in the field orthogonal to the chip. Figure

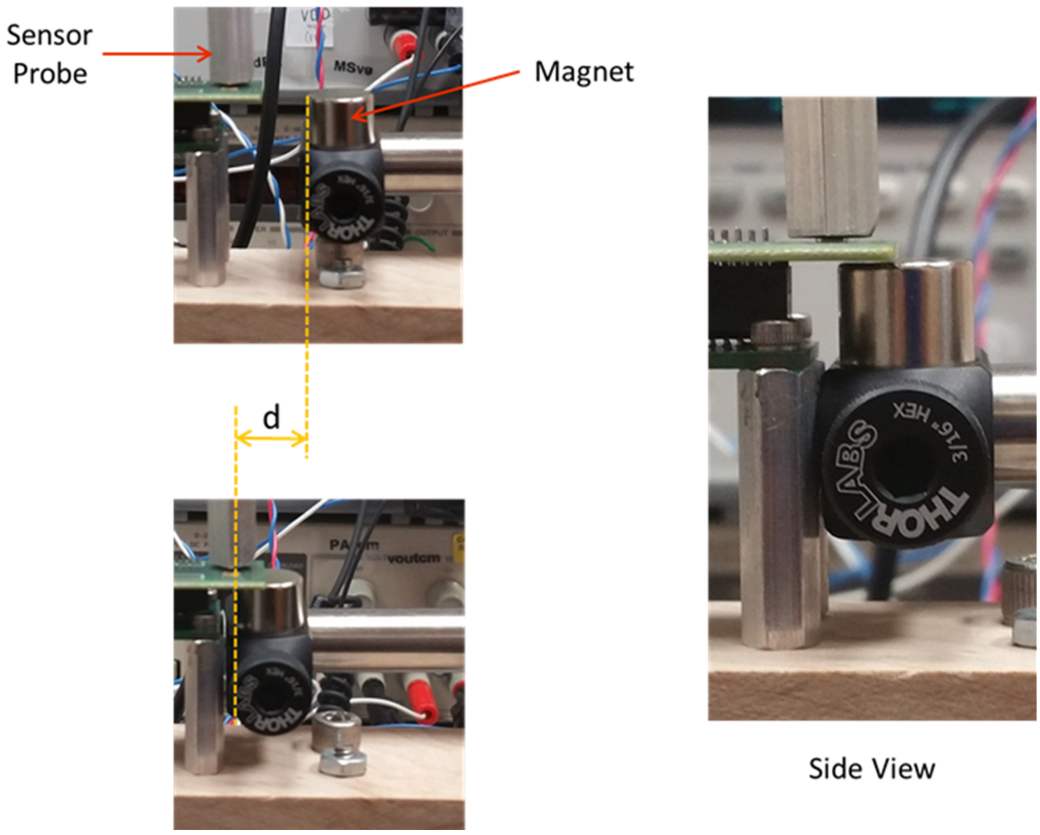


Figure 5.6: Magnet characterization.

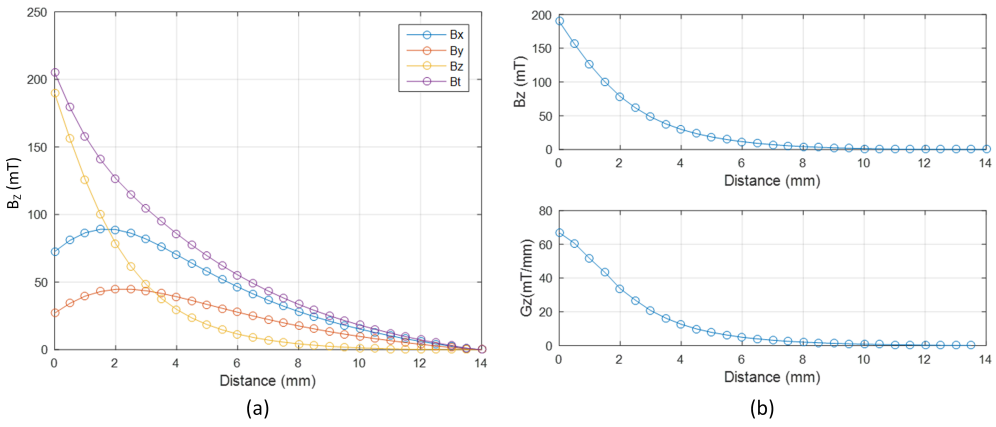


Figure 5.7: Magnetic profile generated by the permanent magnet.

5.7b shows the magnetic field B_Z and the field gradient G_Z as a function of distance. It is important to note that the permanent magnet generates a peak field gradient of ~60 T/m, decaying to ~17 T/m at a distance of 4 mm.

5.2 Magnetic Sensor and LNA Characterization

To characterize the magnetic sensor and LNA, we measured the output of the TIA and LNA as we moved the permanent magnet away from the chip. The measurement results are shown in Figure 5.8. The supply voltage was set to 1 V, the MagFET's gate voltage to 1 V, the sensor current to 16 μA, and the chopper frequency to 763 Hz. The overall bandwidth of the amplifier is 1 kHz. The LNA has an output range of ~400 mV with a gain of 26.3 dB, and shows good linearity with the magnetic field. The TIA has an output range of ~20 mV with a gain of 408.09 kΩ, and also shows good linearity with the magnetic field. The magnetic sensor (MagFET + TIA) has a sensitivity of 100.8 mV/T. Based on these results, the MagFET has an estimeted sensitivity of 1.54 %/T in good agreement with our simulation results. The power consumption of the magnetic sensor was measured to be 36.4 μW.

After these initial results, we optimized the sensitivity and noise performance of the sensor. We increased the supply voltage to 1.2 V, the MagFET's gate voltage to 1.2 V, and the sensor current to 29.52 μA. Since we moved the chip to accommodate the slightly different arrangement in the setup, we measured again the magnetic profile generated by the magnet. This profile is shown in Figure 5.9, which is very similar to the previous one (Figure 5.7). Measurement results are shown in Figure 5.10. In this case, the LNA has an output range of ~600 mV with a gain of 25 dB. The TIA has an output range of ~30 mV with a gain of 317.38 kΩ. The magnetic sensor has a sensitivity of 5.48 V/T while consuming 75.96 μW. In this configuration, the

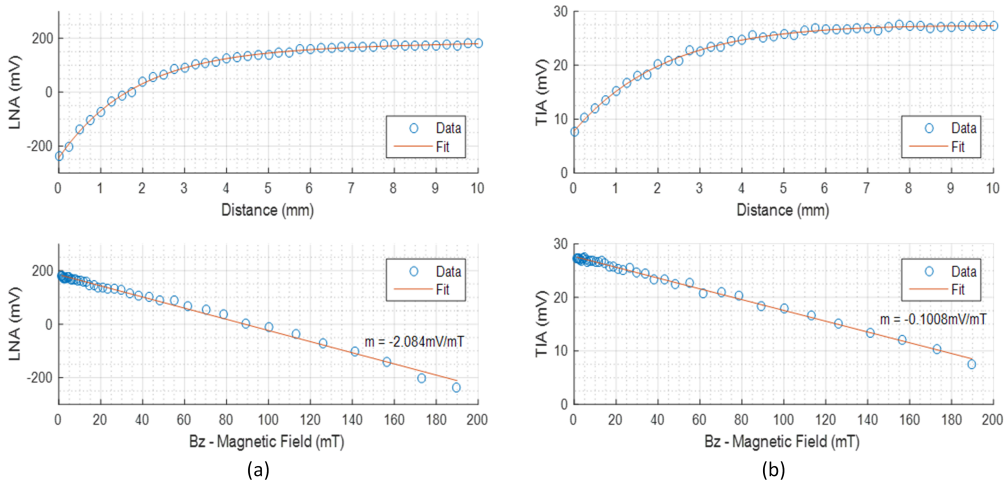


Figure 5.8: Measurement results of the Magnetic Sensor and LNA. (a) Output of the LNA and (b) TIA as a function of distance (top) and magnetic field (bottom).

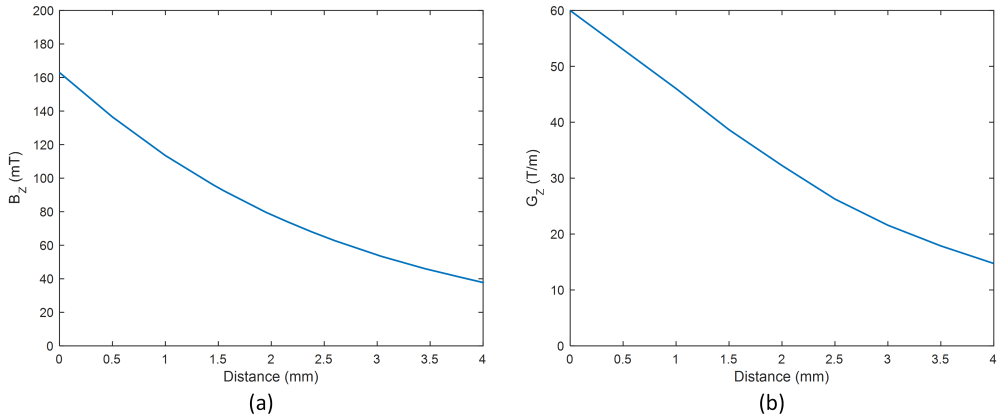


Figure 5.9: Magnetic profile generated by the magnet after optimization. (a) Magnetic field and (b) field gradient as a function of distance.

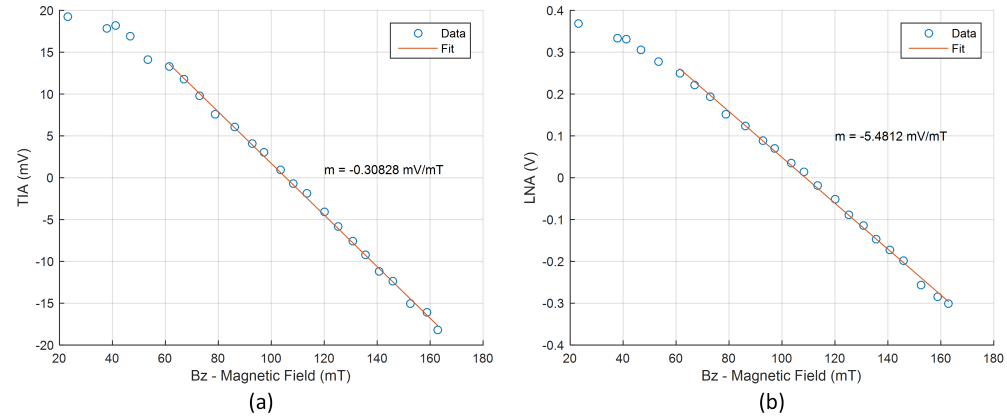


Figure 5.10: Output of the (a) TIA and (b) LNA as a function of magnetic field after optimization.

MagFET has an estimated sensitivity of 3.29 %/T. The measured total input referred noise of the sensor is 625.48 μT between 2 Hz and 100 kHz, as shown in Figure 5.11.

5.3 Ring Oscillator characterization

The oscillation frequency of the ring oscillator is set by the bias current of the ring oscillator, the digital input of the three 4-bit current DACs, and its supply voltage. For this characterization, the supply voltage of the oscillator was set to 1 V. The input of each DAC was swept independently and the oscillation frequency of the oscillator was measured. The results are shown in Figures 5.12 and 5.13. The ring oscillator presents good linearity between 350 MHz to 600 MHz. Beyond this frequency,

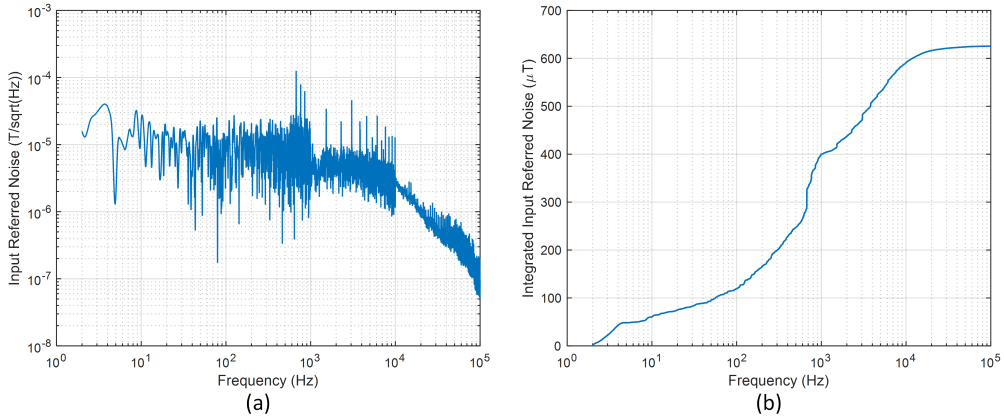


Figure 5.11: Noise measurements. (a) Input referred noise and (b) integrated noise of the magnetic sensor.

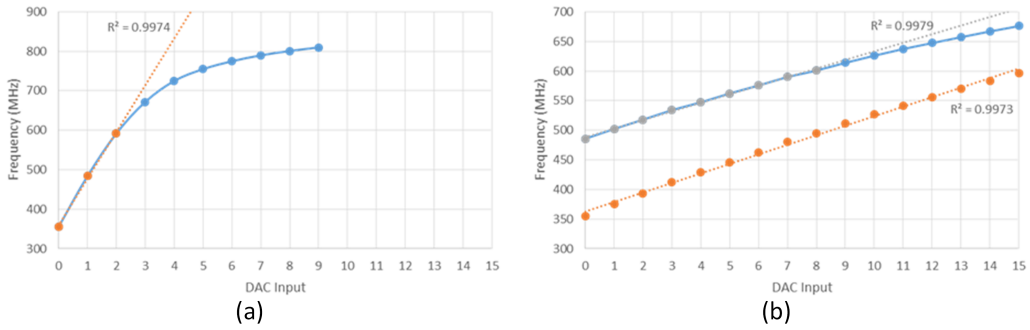


Figure 5.12: Oscillation frequency of the Ring Oscillator as a function of the DAC input. (a) Sweep of DAC_1 with others at zero. (b) Sweep of DAC_2 for two values of DAC_1 with DAC_3 at zero.

the oscillator loses its linear behavior due to non-linearities in the inverters at this low supply voltage. Higher frequencies are supported with a higher supply. The LSB for DACs 1, 2, and 3 are measured to be ~100 MHz, ~16.67 MHz and ~1.4 MHz, respectively. Based on these measurements, we formed a digitally controlled oscillator (DCO) with 6-bit resolution by selecting the desired frequencies from the outputs of the DACs. This DCO has a LSB of 1.4 MHz and a oscillation frequency from 448.17 MHz to 536.67 MHz. The DNL and INL of the DCO are shown in Figure 5.14. A maximum DNL and INL of 0.4 LSB and 1.45 LSB were measured. The DCO consumes an average power of 236.37 μW.

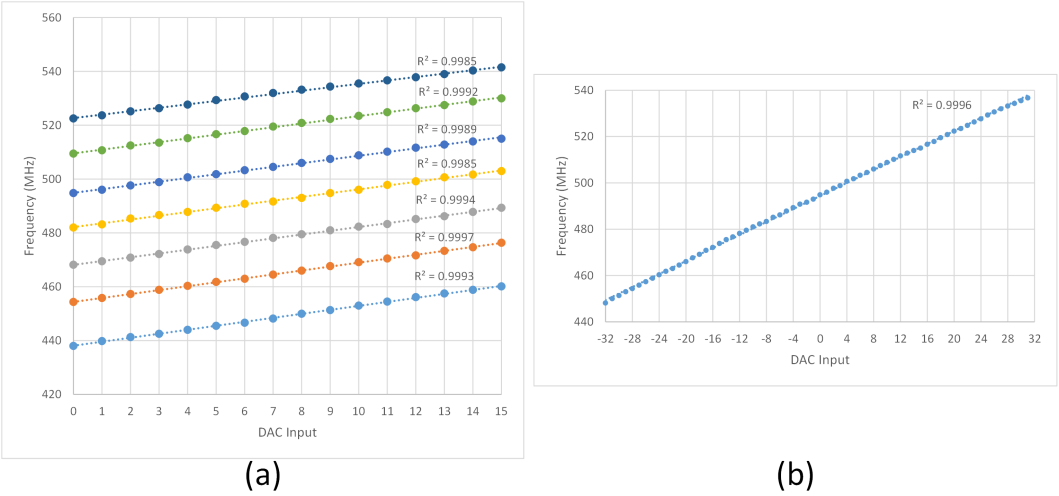


Figure 5.13: (a) Sweep of DAC_3 for a fixed DAC_1 and seven values of DAC_2. (b) 6-bit DCO formed by a selection of desired output frequencies from all DACs.

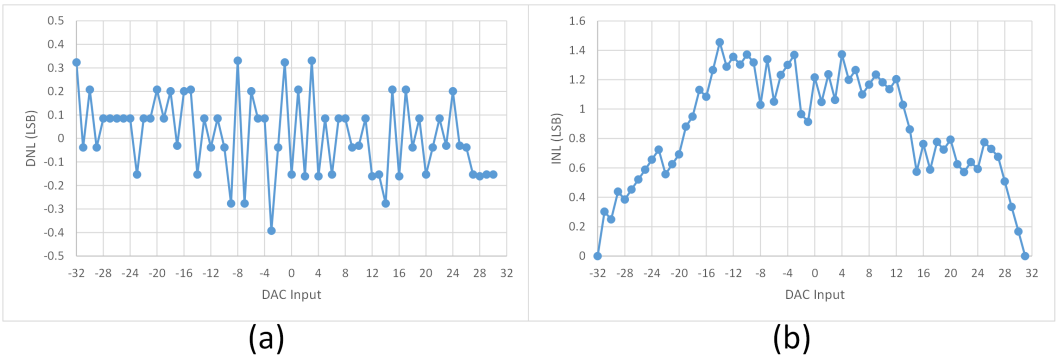


Figure 5.14: (a) DNL and (b) INL of the 6-bit DCO.

5.4 PLL Characterization

PLL wireless locking

The PLL was measured by sending the reference signal wirelessly and recording its output either via a wire or wirelessly via a receiver coil. We have only used the wired output to measure the PLL response in experiments involving the excitation phase. All other measurements were done wirelessly.

As a first experiment we send an RF pulse at 500 MHz wirelessly to the chip. This pulse has a pulse width of 400 μs. The output of the PLL is measured using a real-time oscilloscope at 10 GSa/s. Figure 5.15 shows the spectrogram and the oscillation frequency of the PLL's response to the excitation signal. Initially, the PLL is opened and it oscillates at its natural frequency. When the RF pulse initiates, the PLL detects

its presences by *osc* = 1, closes its loop, locks its oscillation frequency to the RF pulse, and samples V_{ctrl} to a capacitor. The straight line at 500 MHz in Figure 5.15 indicates the locking state. When the RF pulse ends, the PLL senses this transition by *osc* = 0 and opens its loop to avoid any miscorrection to the measured oscillation frequency (i.e., sampled V_{ctrl}) that could occur due to the reference signal's absence. At this point, the control logic (in the FPGA) receives the signal *osc* = 1, and sends a command to the chip to connect the sampled V_{ctrl} to the input of the VCO. The latency in communication between the chip and the external controller (FPGA) causes a delay of 35 μs before the command is executed. During this time, the PLL is opened and its oscillation frequency returns to its initial value. After the delay, the sampled V_{ctrl} is connected and the oscillation frequency changes to the sampled frequency of 500 MHz. During this phase, the VCO is a free-running oscillator (PLL is opened). It is important to note that the oscillation frequency stays at the sampled value in average for a duration of ~1 ms.

We increased the recording time to 5 ms, and changed the RF pulse frequency to 504 MHz. Figure 5.16 shows the results of this experiment. The PLL locks to the RF pulse, going from an initial frequency of ~501.5 MHz to the pulse frequency of 504 MHz. After the 1 ms pulse, the PLL keeps the oscillation frequency for 3.5 ms. To determine how the oscillation frequency of the ring oscillator changes with time, we repeated the experiment with a frequency of 500 MHz (Figure 5.17). We notice a drop of approximately 1 MHz after 4 ms, which indicates a decay of 250 kHz/ms. The PLL locking range was measured to be 2.5 MHz.

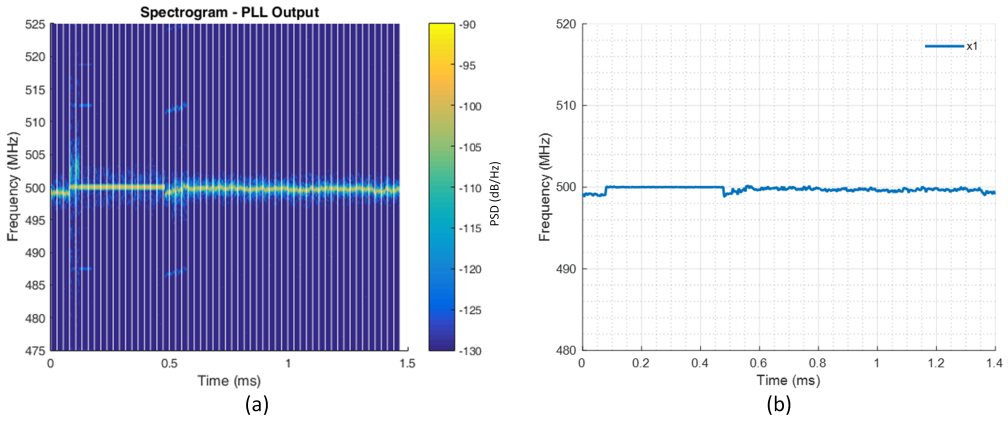


Figure 5.15: (a) Spectrogram and (b) oscillation frequency of the response of the PLL to a wireless RF pulse of 400 μs.

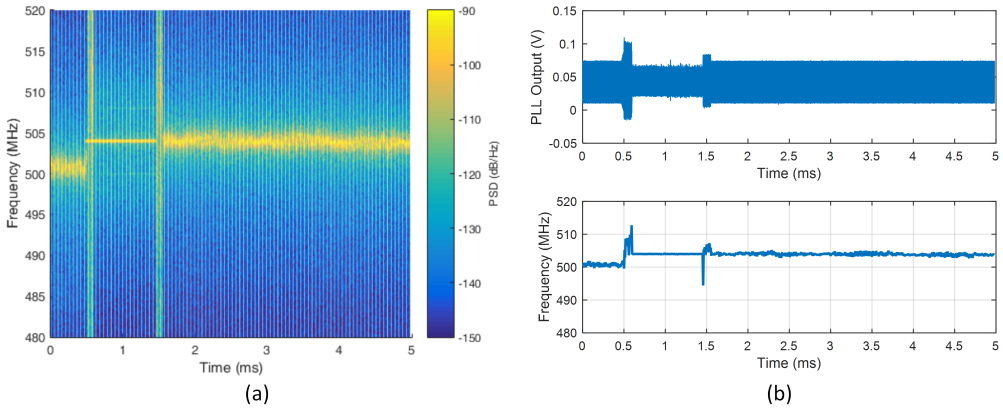


Figure 5.16: (a) Spectrogram, (b) time-domain signal, and (c) oscillation frequency of the response of the PLL to a wireless RF pulse of 1 ms. Note the duration of the recording time of 5 ms.

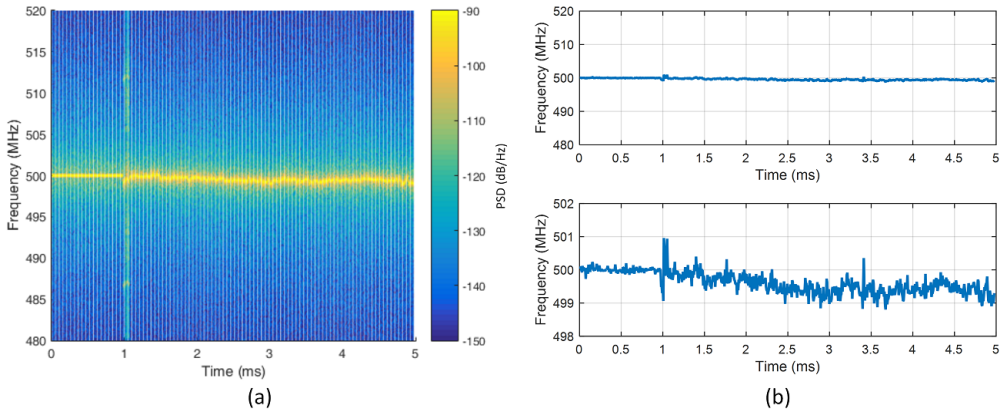


Figure 5.17: (a) Spectrogram and (b) oscillation frequency of the response of the PLL to a wireless RF pulse of 1 ms. Note the duration of the recording time of 5 ms. The zoomed figure (b, bottom) shows a decay of 250 kHz/ms.

Next, we tested the functionality of *sampling* V_{ctrl} in keeping the oscillation frequency. We sent a wireless pulse of ~2 ms and observed the output of the free-running ring oscillator for ~8 ms while connecting or not connecting the sampled V_{ctrl}. The oscillation detector frequency was kept ON, which means that in both cases the PLL opened when the reference signal was turned off. Figure 5.18 shows the measurement results. When the sampled V_{ctrl} was left unconnected, the oscillation frequency jumped by ~2 MHz and started to decay from ~505 MHz to ~499 ms after ~8 ms. When the sampled V_{ctrl} was connected, the oscillation frequency returned rapidly to the RF pulse frequency of 503 MHz and stayed approximately

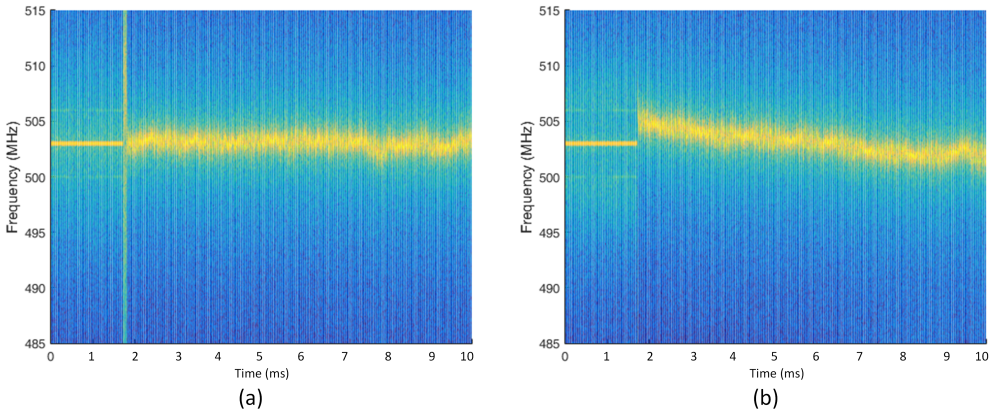


Figure 5.18: Spectrogram of the response of the PLL to a ~2 ms RF pulse at 503 MHz when sampled V_{ctrl} is (a)connected or (b)left unconnected. Note the duration of the recording time of 10 ms.

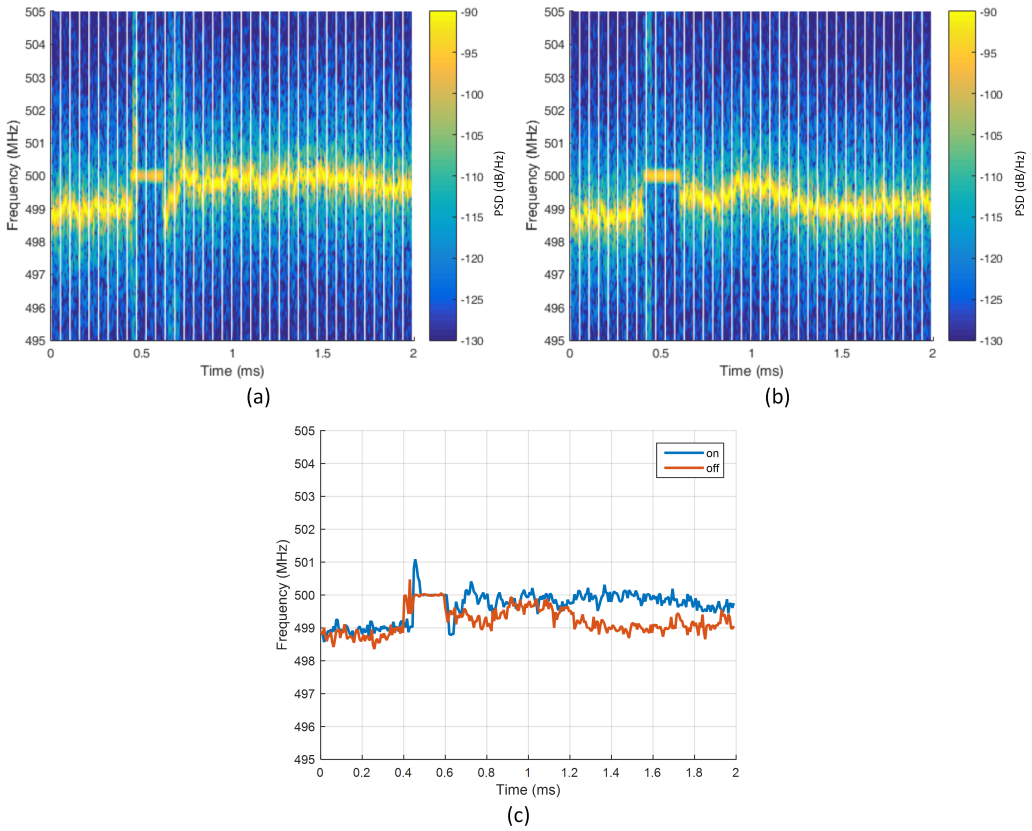


Figure 5.19: PLL response to a wireless RF pulse of 200 μs at 500 MHz when the sampled V_{ctrl} is (a)connected or (b)left unconnected. (c) Comparison of both cases.

constant for ~8 ms.

Another example is shown in Figure 5.19, with an RF frequency of 500 MHz, a pulse of 200 μs and a recording time of 2 ms. Here we can see how the free-running behavior of the ring oscillator continues after a short pulse when the sampled V_{ctrl} is left unconnected. Contrary, the oscillation frequency returns to 500 MHz when the sampled V_{ctrl} is connected.

The measured phase noise of the PLL is shown in Figure 5.20. The PLL has an integrated rms jitter (10 kHz - 10 MHz) of 60 ps when it is locked and 308 ps when it is unlocked. In addition, we observed a dominant *1/f* noise behavior, showing a -30dB/dec slope. This is due to the small size transistors in the ring oscillator targeting a low-power PLL.

PLL calibration

We first measured the response of the frequency detector (FD) as the oscillation frequency of the ring oscillator is swept around the reference signal. The average of the output of the sensor as a function of the frequency difference is shown in

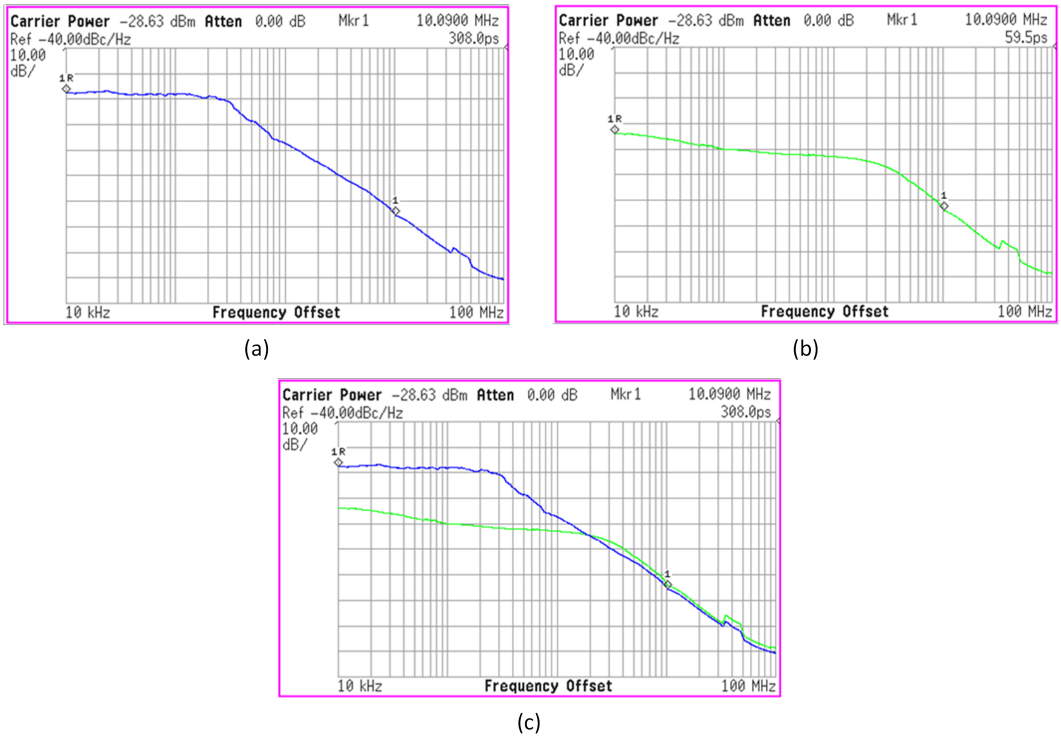


Figure 5.20: Phase noise of the PLL when it is (a) unlocked and (b) locked. (c) Comparison of both cases.

Figure 5.21. We observed a transition period of ±1 MHz when the average output goes from 0 to 1. This output is then used by the calibration algorithm to correct for this difference. The calibration logic is implemented in the FPGA and used an integration time of 100 μs. The output of the PLL was recorded and analyzed, and the results are shown in Figure 5.22. The spectrogram of the PLL output shows the correct calibration of the oscillation frequency following a SAR-like process. The end of the calibration is indicated by the end-of-calibration (EOC) signal.

5.5 System Characterization

To characterize the behavior of the system, we first produced a positive and negative shift artificially. We sent a command to the chip to shift its oscillation frequency by +1 LSB, 0 LSB and -1 LSB after the RF pulse is received. For this experiment, the RF pulse was set to 500 MHz with a duration of 200 μs (Figure 5.23). The response of the chip was observed for 2 ms. We can see that the chip correctly locks to the

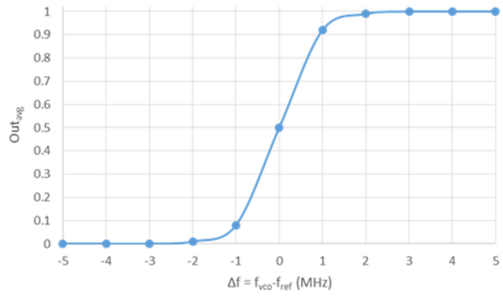


Figure 5.21: Averaged output of the FD as a function of frequency difference.

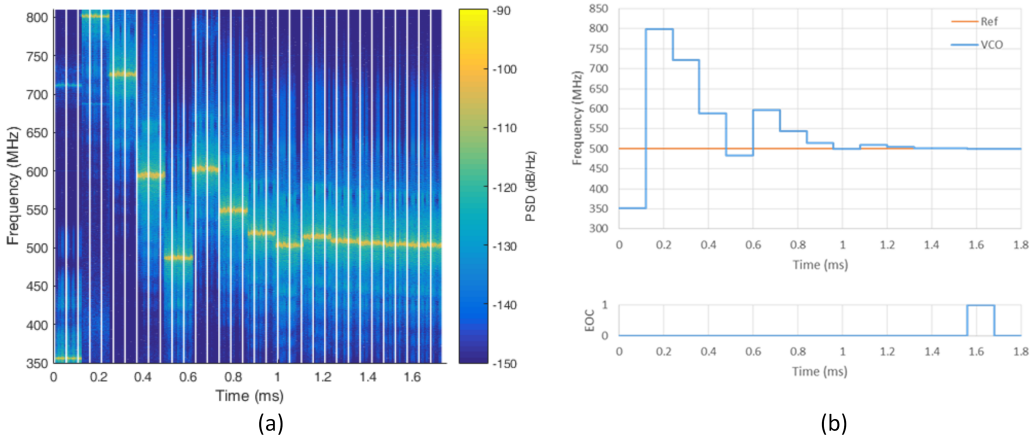


Figure 5.22: PLL calibration results. (a) Spectrogram. (b) Oscillation frequency as a function of time.

RF pulse and shifts its oscillation frequency according to the command sent. This oscillation frequency is kept approximately constant for ~1.4 ms.

At this point, we decided to test our first proof-of-concept by placing the chip at 13 different locations at 0.5 mm steps (Figure 5.24). We observe that the chip correctly locks to the desired frequency (500 MHz) and generates a frequency shift that changes with distance. After mapping the response of the chip in space, we observe that the generated frequency shifts are proportional to the magnetic field.

We then optimized the test setup and the system, and characterized the response of the chip as an artificial nuclear spin. The ATOMS chip first measured the magnetic field and used a moving-average filter of 128 samples at 763 Hz (implemented in the FPGA) to reduce noise. Then, it detected the excitation RF pulse (400 μs pulse width), locked the internal oscillator to this signal, and waited until the pulse ended to transmit the shifted-frequency response. For this experiment, the output of the chip was measured for 800 μs at 31 different positions.

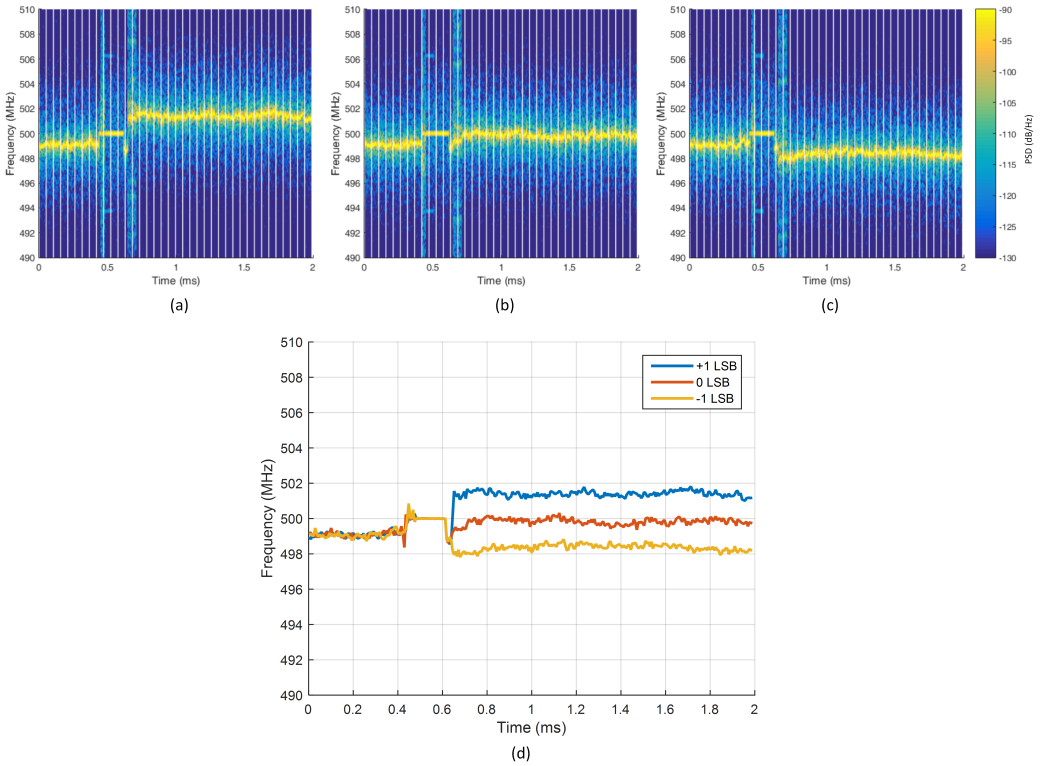


Figure 5.23: Response of the chip to an excitation RF pulse of 200 μs at 500 MHz when the pre-programmed shifts are (a)+1 LSB, (b)0 LSB, and (c) -1 LSB. (d) Comparison of all 3 cases.

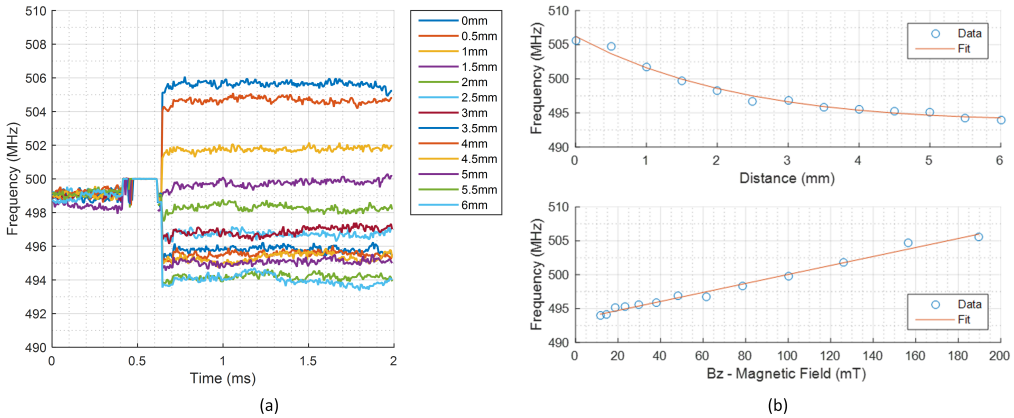


Figure 5.24: First proof-of-concept experiment of ATOMS technology. (a) Oscillation frequency of the chip to 13 different locations. (b) Oscillation frequency during transmission phase as a function of distance (top) and magnetic field (bottom).

The spectral profile of the chip for all 31 positions is shown in Figures 5.25 and 5.26. As expected, the oscillation frequency of the chip changes proportional to its distance from the magnet, with higher frequencys (positive shifts) when the chip is close to lower frequencies (negative shifts) when it is far. It shows a 3dB-bandwidth of 600 kHz, which allows accurate location estimation. After mapping the magnetic field in space, a linear relationship between oscillation frequency and magnetic field

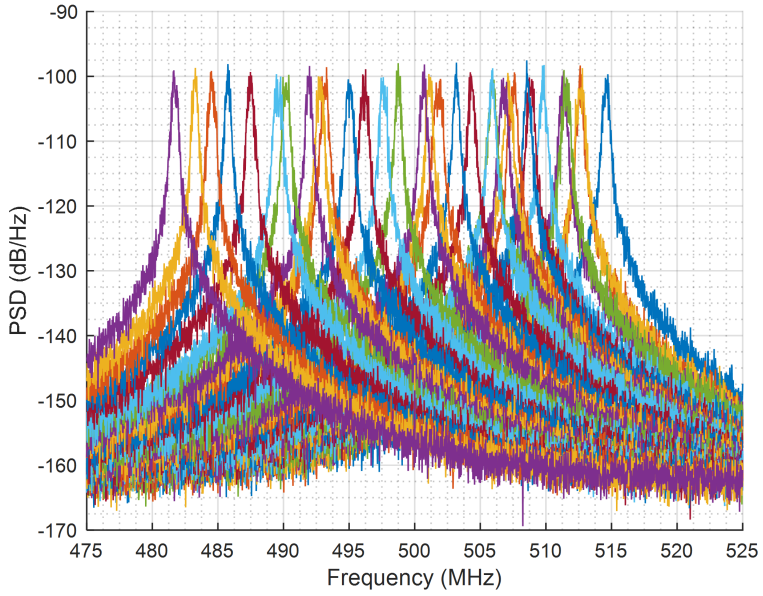


Figure 5.25: Spectrum of the response of the chip for all 31 position.

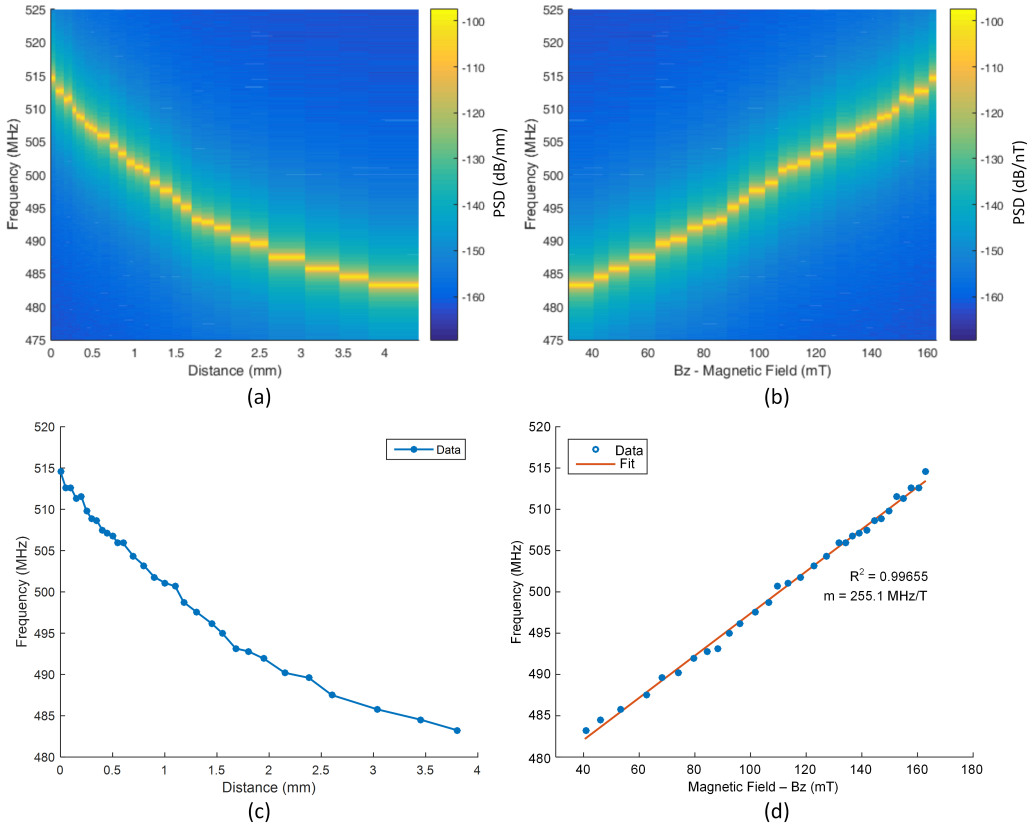


Figure 5.26: Spectral profile of the ATOMS chip for 31 different positions as a function of (a) distance and (b) magnetic field. Oscillation frequency of the chip during transmission phase as a function of (c) distance and (d) magnetic field. A responsivity $\gamma_{ATOMS,f}$ of 255.1 MHz/T is measured.

is revealed in the range of 480-520 MHz and 40-170 mT. For each position, the oscillation frequency was estimated by calculating the center frequency of the peak of the power spectral density (PSD); then a linear fit was calculated (Figure 5.26d). The ATOMS chip has a measured responsivity $\gamma_{ATOMS,f}$ of 255.1 MHz/T.

5.6 1D Localization

To verify the behavior of ATOMS, we first performed a 1D localization experiment using the test setup described above and placed the chip at 3 different positions along the same axis (Figure 5.28). In this experiment, we also used an RF pulse of 400 μs at 500 MHz and a receiver reading window of 800 μs. We only used the wired output of the chip to capture the response of the system during the excitation phase. All other measurements were taken from the wireless signal picked up by the receiver coil. Figure 5.29 shows the frequency response during the excitation phase

and transmission phase, showing frequency acquisition and frequency encoding. Initially, the chip measured the magnetic field. The internal oscillator, during this phase, oscillated at its natural frequency. When the RF pulse was applied, the chip detected its presence, locked the internal oscillator, and measured its frequency. When the RF pulse was removed, the chip sensed this transition and performed frequency encoding according to the previously measured magnetic field. The latency in communication between the chip and the external control logic (FPGA) caused a delay of ~35 μs in frequency encoding due to the use of a serial interface for data transfer. During this time, the PLL was opened and the oscillation frequency returned to its initial value.

We measured the chip's response wirelessly, and calculated the PSD. The chip generated different frequency shifts for all three positions (Figure 5.29). We estimated the distance from the magnet according to Equations 3.1 and 3.2. It is interesting to note that the spectrum response from each position either narrows (x_1) or widens (x_2 and x_3) (Figure 5.29c) depending on the distance from the magnet. This behavior is caused by the nonlinear magnetic field of the magnet, which translates into a non-constant magnetic field gradient and reduces the accuracy of the system when the chip is far from the magnet. The position of the chip was estimated by taking the center value of the peak of the PSD in space. Interference at the center frequency (500 MHz) due to harmonics of electronics' clock signal is filtered out during processing. Figure 5.30 shows the true and estimated positions for all three locations, and the FWHM as a function of the magnetic field gradient. The estimation error and standard deviation of the estimated location σ_x were also measured. Both quantities increased in inverse proportion to the magnetic field gradient at each location, from 50.44 μm and 59.17 μm when the gradient is 51.46 T/m to 115.4 μm

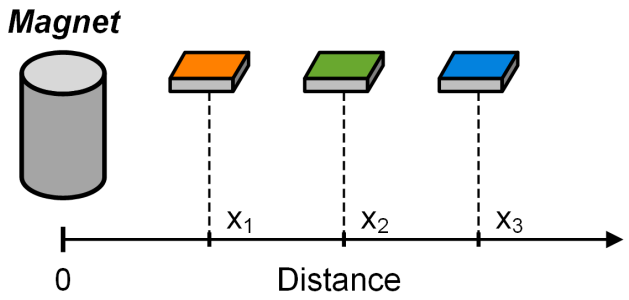


Figure 5.27: Illustration of the 1D localization experiment with three different positions for the ATOMS chip.

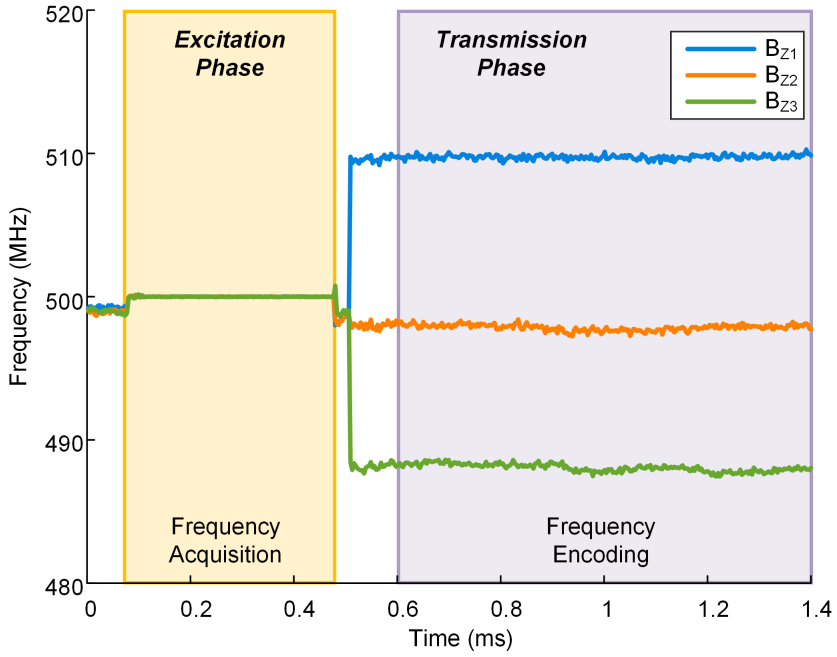


Figure 5.28: Frequency response during excitation phase and transmission phase, showing frequency acquisition and frequency encoding.

and 125.7 μm when it is 32.14 T/m, respectively

To explore the widening effect of the spatial PSD, we measured the response of the chip to 31 different locations (Figure 5.31). The FWHM of the chip's response follows the magnetic field trend, varying from ~140 μm at 12 T/m down to ~35 μm, at ~60 T/m. The FWHM is a measure of the phase noise of the oscillator, and indicates the uncertainty region of the localization for a given SNR at the receiver. Although it is not as important for the localization of a single device, it is of high relevance for the localization of multiple devices, because it determines the spectral separation between devices and, therefore, the resolution.

5.7 2D Localization

Next, we performed a 2D localization experiment using the test setup shown in Figure 5.32. We used two magnets (M_1 and M_2) to generate two magnetic field gradients in different directions and moved the ATOMS chip relative to their positions. At each location, we estimated the distance from the chip to each magnet using one magnet at a time. Here, the response of the chip to each measurement defined a curve of possible positions that aligned with the magnetic field line of the estimated magnetic field magnitude (B_{Z_1} and B_{Z_2} in Figure 5.32). We defined the functions

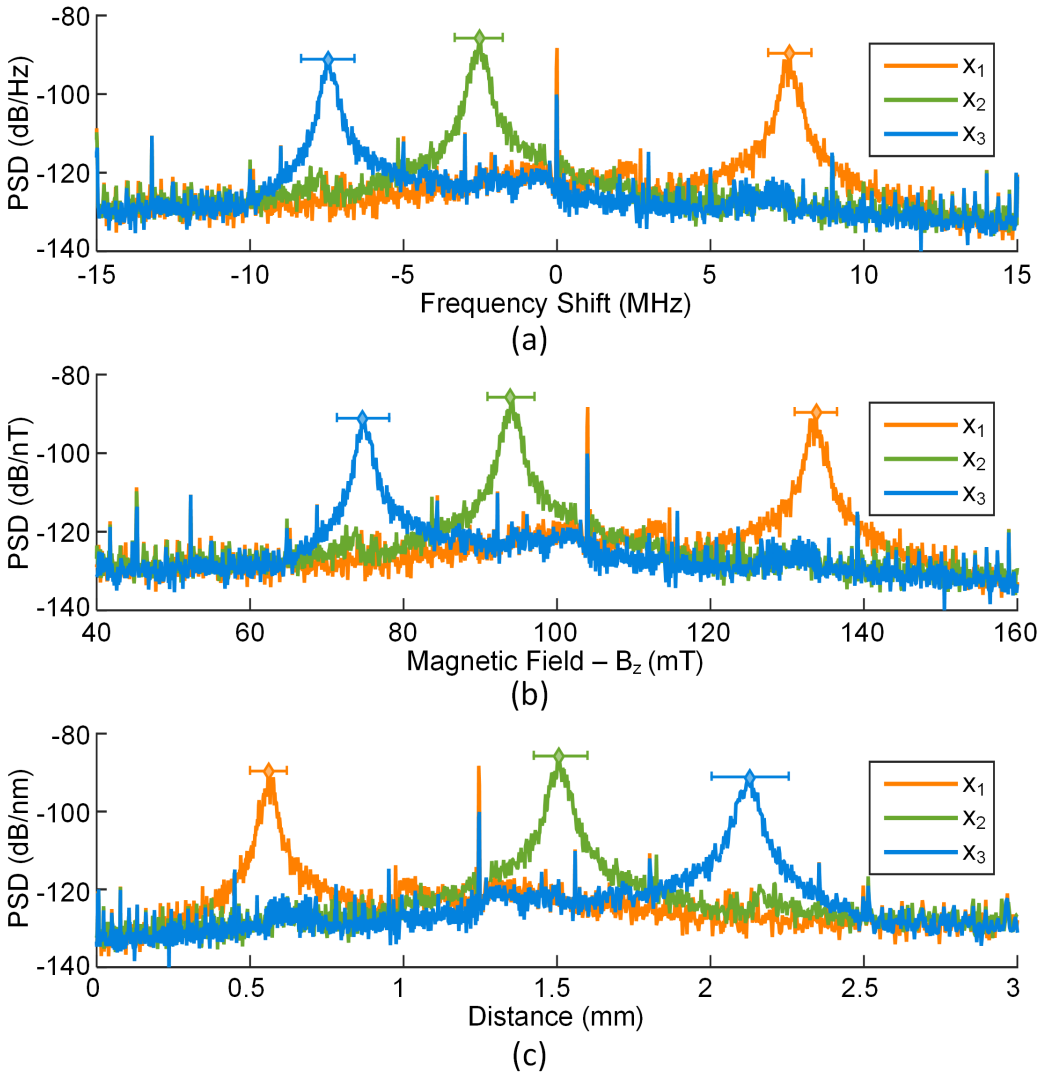


Figure 5.29: Frequency Shift - Magnetic Field - Location estimation. The figure shows the PSD of the received signal as a function of (a) frequency shifts, (b) magnetic field and (c) distance.

$P_{M_1}(x, y)$ and $P_{M_2}(x, y)$ as the mapping of the PSD of the chip's response into the 2D magnetic field space of M_1 and M_2, respectively. Then, we estimated the 2D position by calculating the center value of the peak of the cost function

$$P_{M_{12}}(x, y) = \left(\frac{P_{M_1}}{P_{M_1,\max}}\right) \cdot \left(\frac{P_{M_2}}{P_{M_2,\max}}\right), \tag{5.1}$$

which is the product of the normalized P_{M_1} and P_{M_2} (i.e. the point where they intersect). Prior to the experiment, we measured the magnetic field of the magnets in the region of interest and calculated the magnetic field gradients, with magnets

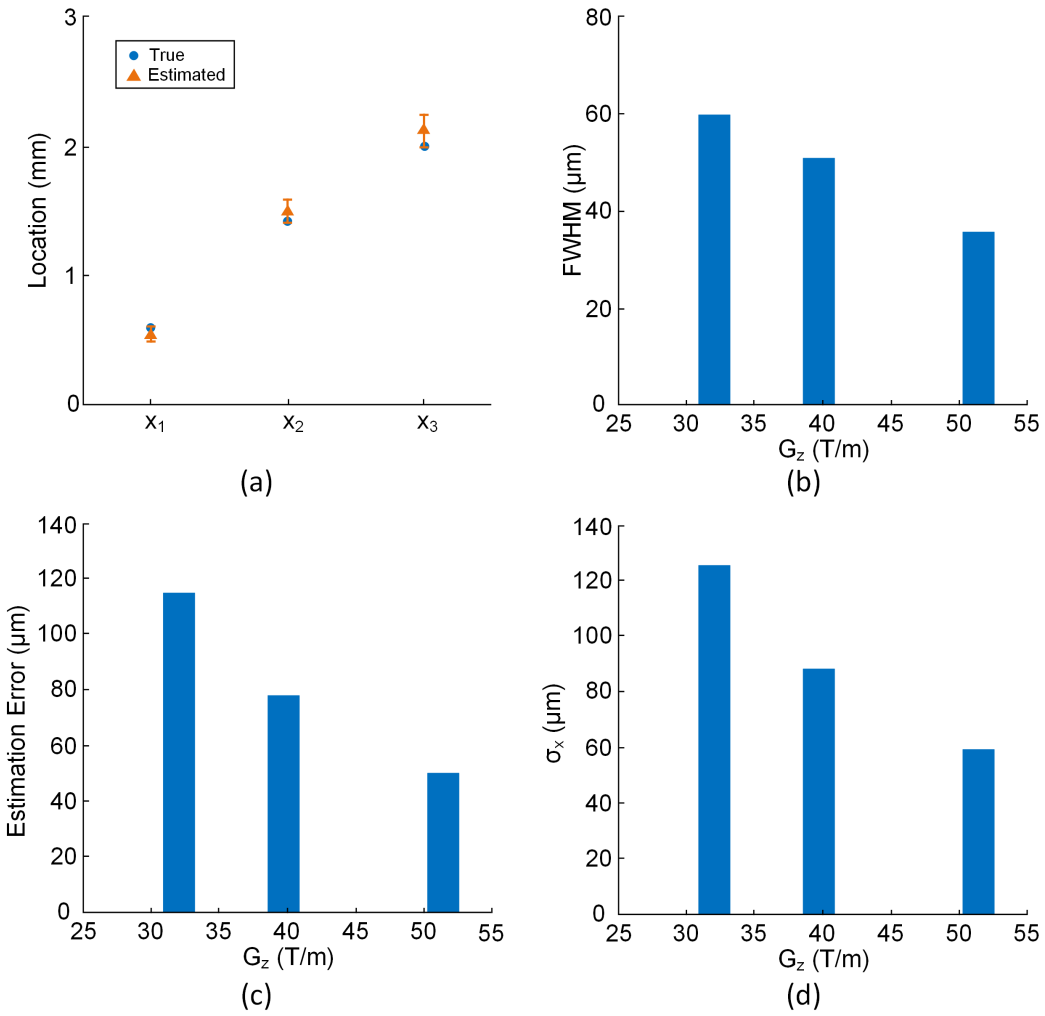


Figure 5.30: Localization results. (a) Estimated and true positions of all 3 cases. (b) FWHM or 3-dB bandwidth of the spatial PSD as a function of G_Z. (c) Localization error as a function of G_Z. (d) Standard deviation of the experiment σ_x as a function of G_Z. Horizontal error bars indicate standard deviation.

at positions (0 mm, 0 mm) for M_1 and (0 mm, 2.6 mm) for M_2, (Figure 5.32). Only M_1 is shown since both magnets are of the same kind.

We first localized the ATOMS chip at a single position. This experiment can be seen in Figure 5.34. The cost function $P_{M_{12}}$ in (5.1) is shown in the figure in dB and linear scales. We observe the location of the chip clearly, as well as the lines of equal magnetic field generated by M_1 and M_2.

Then, we perfomed a 2D experiment were the chip was placed at 5 different positions along a straight line in a 2D plane. The response of a single sample for each position is shown in Figure 5.35. Both dB and linear scales of $P_{M_{12}}$ show the localization

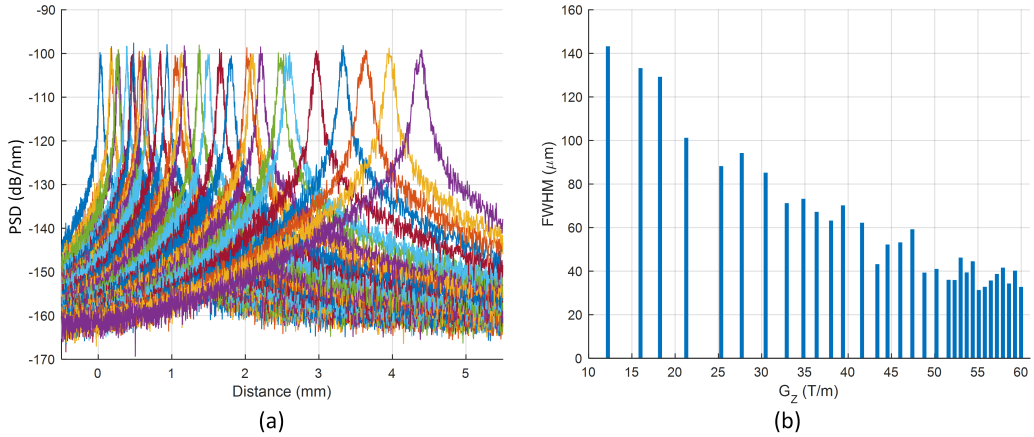


Figure 5.31: Widening effect of the spatial PSD generated by the non-linear magnetic field. (a) Spatial PSD of the chip for 31 different positions. (b) FWHM as a function of G_Z.

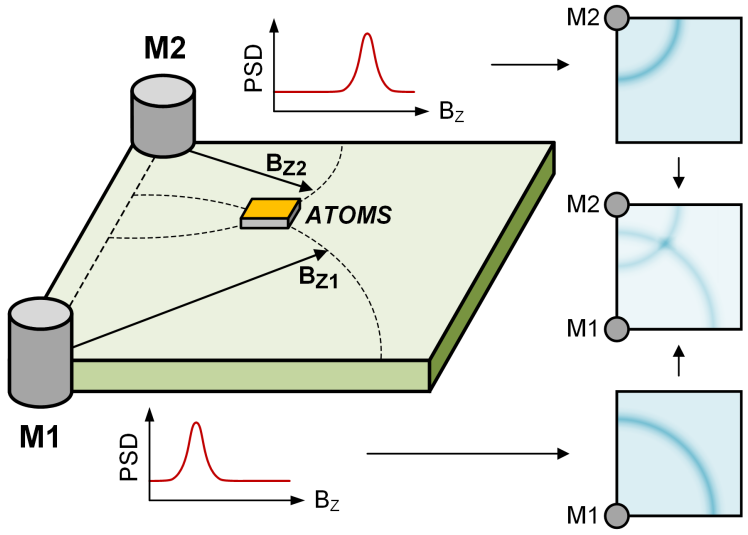


Figure 5.32: Illustration of the 2D localization experiment, in which two magnets are used to generate two magnetic field gradients in different directions. The ATOMS chip is moved relative to the position of both magnets. At each location, the distance to each magnet is estimated using a single magnet at a time. The 2D location is then determined by combining both estimated distances.

of the chip at each location. An estimation error of less than 350 μm is measured. It is important to note that the high estimation error is due to the fact that we have performed a single sample at each position. Thus, since we have digitized the output of the magnetic sensor, the error is determined by the random nature of the noise. In other words, the error will be bounded by $\pm 3\sigma$ around the mean.

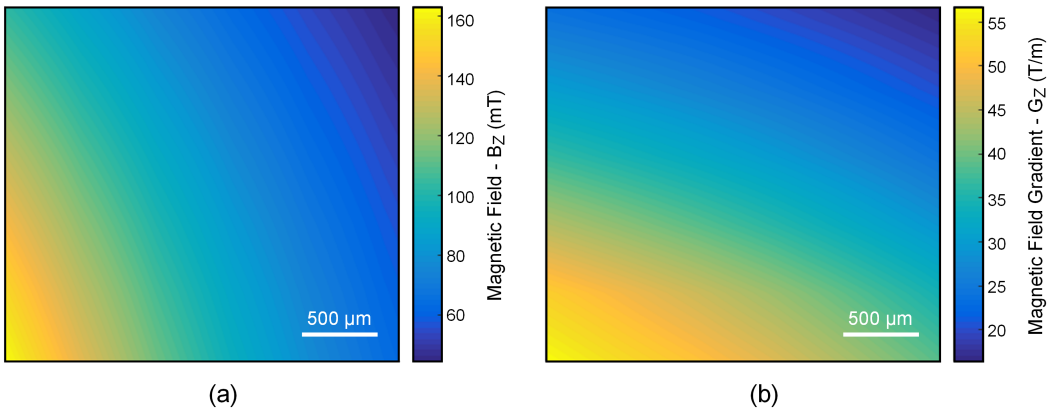


Figure 5.33: 2D mapping of (a) the magnetic field and (b) magnetic field gradient generated by the magnets. The magnet is placed at the bottom left corner. Colorbars indicate the magnetic field in mT and the field gradient in T/m.

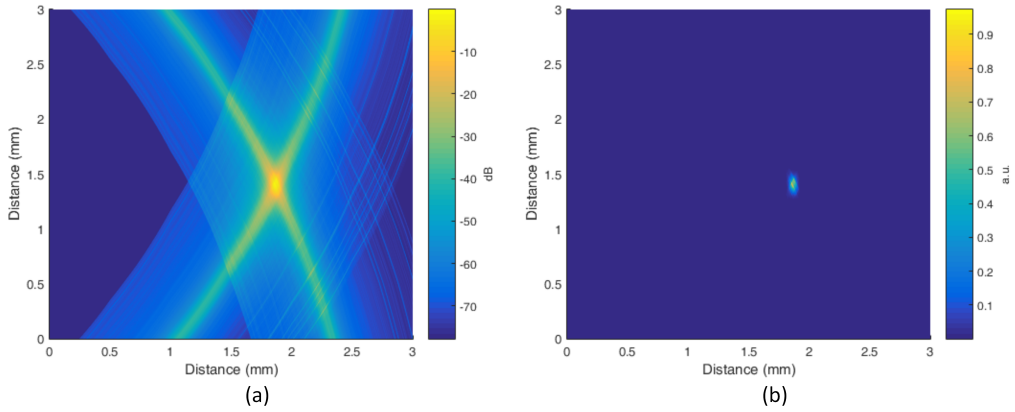


Figure 5.34: 2D localization of a single position showing the intensity of the chip's response in (a) dB and (b) linear scales.

Finally, we performed three experiments where the ATOMS chip was placed at different positions to form the letters C, I, and T. For each measurement, we used the same 1D localization method and took 32 samples at each position. In this case, the spectral information (i.e. Fourier transform) was calculated directly in the oscilloscope to reduce localization time. As expected, the three letters can be clearly identified, and the positions can be easily discerned (Figure 5.36a). The estimated and true positions of each experiment are shown in Figure 5.36b. An estimation error of less than 250 μm was measured for all cases (Figure 5.36c). Similar to the previous experiment, the estimation error depends on the magnitude of the magnetic field gradient, with lower errors and variations at locations closer to the magnets

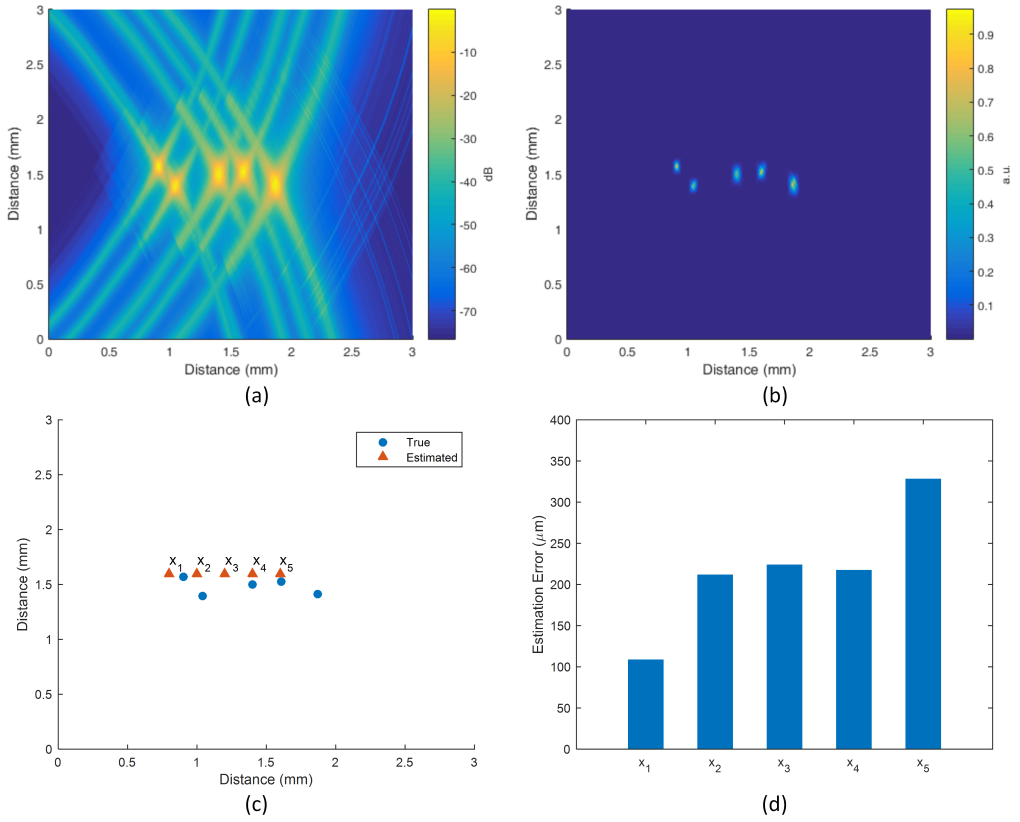


Figure 5.35: 2D localization of a five position in a straight line showing the intensity of the chip's response in (a) dB and (b) linear scales.

where the gradient is high.

5.8 Test Setup for *In Vivo* Experiments

For the *in vivo* experiment, the interface with the chip was modified as follows. A small PCB with a shaft on a standard 4-layer 0.062" FR4 substrate was designed to hold the chip for insertion. The shaft had a length of 32 mm and a width of 3.55 mm before encapsulation. The chip was placed in the tip of the PCB's shaft and both were encapsulated using a silicon elastomer. The total width of the shaft after encapsulation was 4 mm. The PCB with the chip was inserted into the mouse and moved to target locations using a micropositioner. A shielded cable was used to connect this small PCB to the mother board and the rest of the test setup. The magnetic field was generated using an NdFeB grade N52 magnet from K&J Magnetics, with a size of 2" diameter × 2" length. The magnet was placed above the mouse. A transmit/receive coil was used to send the RF pulse and to pick up the response of the chip. Custom 3D-printed structures were designed to hold and

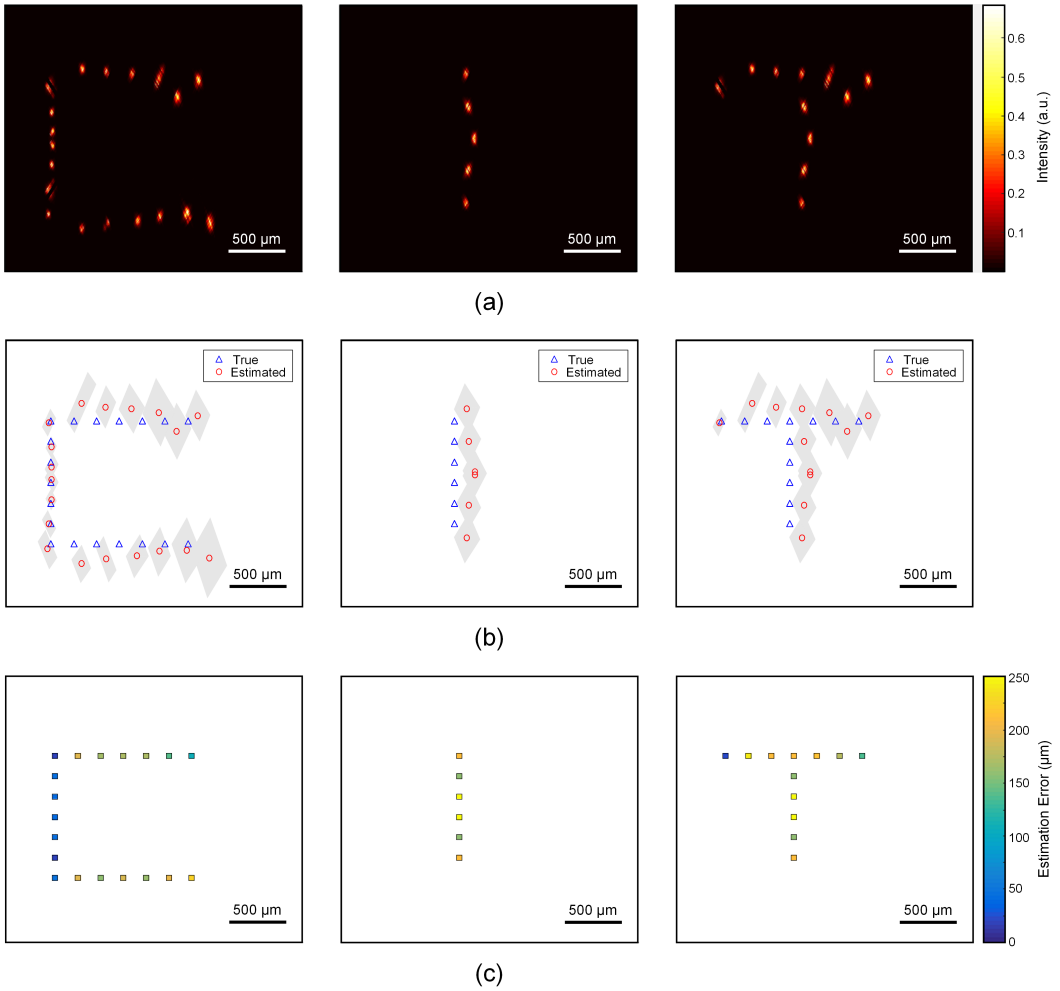


Figure 5.36: (a) Localization results of three different experiments where the ATOMS chip was placed at positions to form the letters C, I, T. Colorbar indicates intensity. (b) Estimated and true position of each experiment. The blue triangles show the true location and the red circles the estimated position. The shaded region indicates the standard deviation. N = 32. (c) Estimation errors of each experiments. Each square in the figure shows the error of its corresponding position in space. Colorbar indicates the estimation error in μm.

position the small PCB, magnet, and animal in place. A picture of the modified test setup is shown in Figure 5.37.

Chip Silicon Encapsulation

First, a layer of Sylgard-184 was applied on top of the chip to cover and protect the wirebonds, and it was cured at 75° C for 60 min. Then, Silastic MDX4-4210 was used for encapsulation. Dip-coating was performed on the PCB's shaft with the chip, and it was cured at 75° C for 60 min.

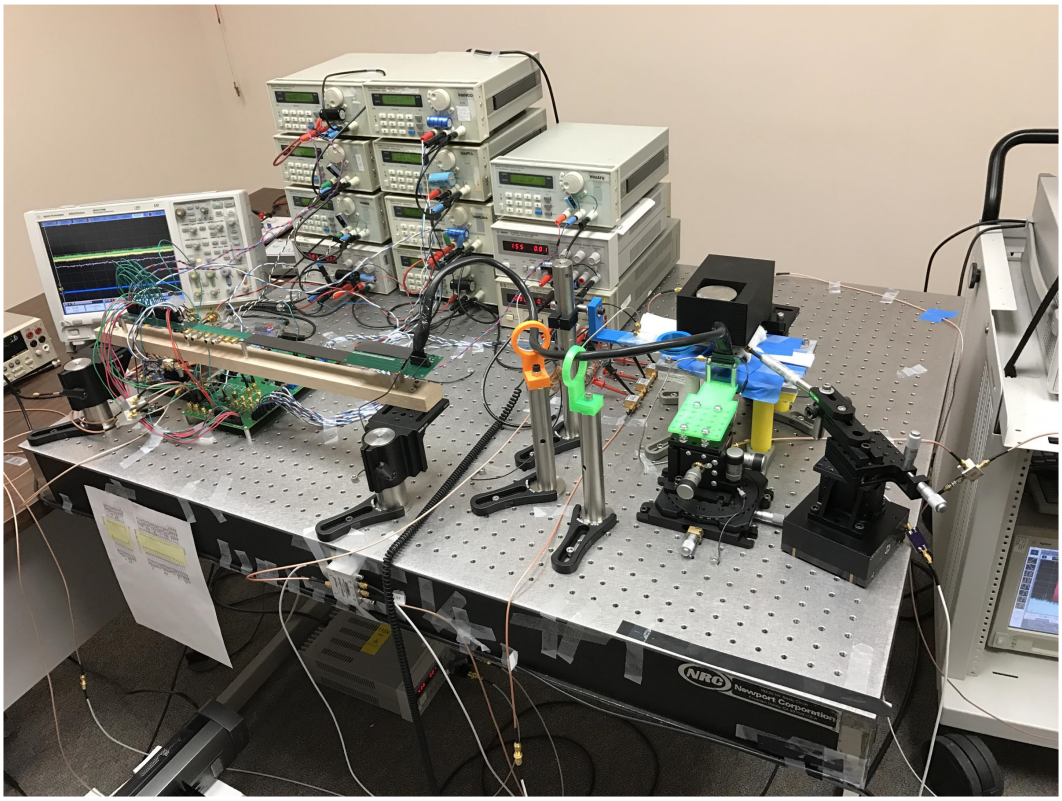


Figure 5.37: Picture of the test setup for *in vivo* experiments.

5.9 *In Vivo* Localization

To establish the feasibility of ATOMS technology *in vivo*, we performed a localization experiment where the ATOMS chip was inserted subcutaneously in the back of a mouse (Figure 5.38). We moved the chip to four different locations in the same axis using a micropositioner (Figure 5.39). We used a stronger magnet to increase the FOV to more than 12 mm. This magnet was placed above the mouse and generated the magnetic field profile shown in Figure 5.40. Due to this new profile, we recalibrated the chip to accommodate the new magnetic field range. In this case, $\gamma_{\text{ATOMS,f}}$ was measured to be 170.7 MHz/T. A transmit/receive coil was used for RF excitation and signal reception. The PSD of the received signals exhibited four different peaks corresponding to the target locations (Figure 5.41). An estimation error of less than 500 μm was measured for all cases (Figure 5.42). We observe that the estimation errors are similar to each other, which agrees with a more linear magnetic field. In addition, the variation of the location of x_1 is the highest, which corresponds to the region with the lowest field gradient of $\sim$ 9 T/m.

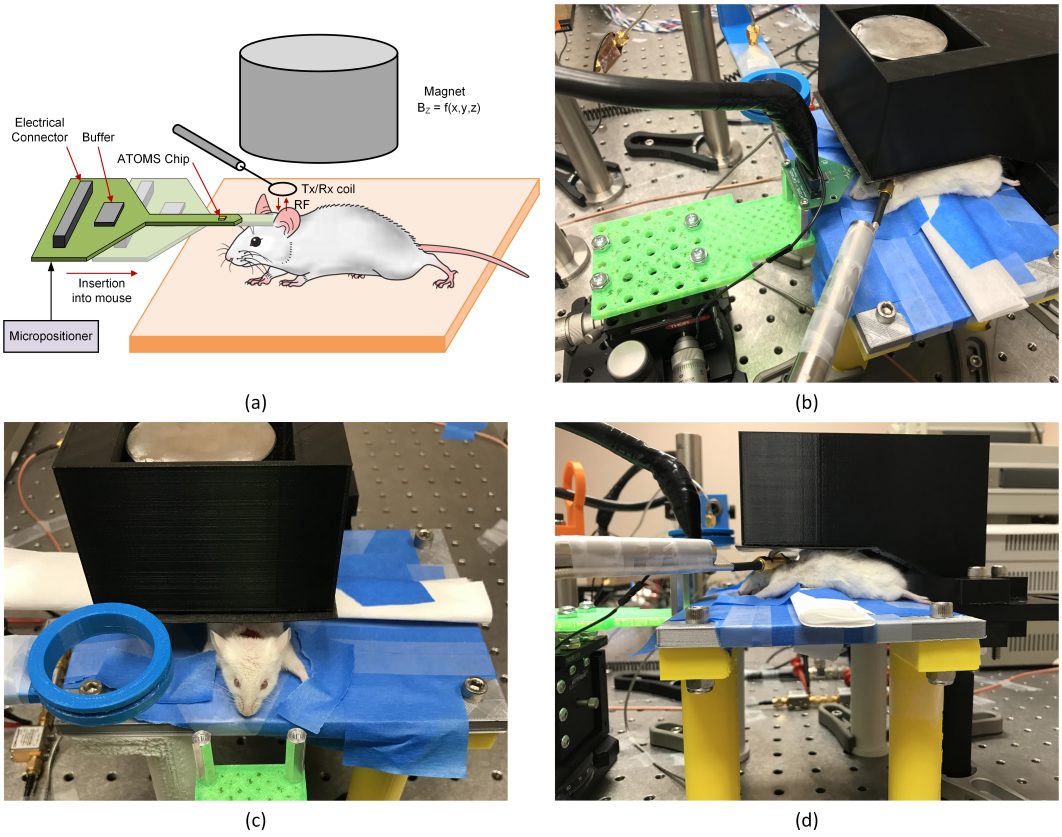


Figure 5.38: (a) Illustration and (b-d) pictures of the *in vivo* localization experiment. The ATOMS chip is placed in the shaft of a small PCB. The total width of the shaft after silicon encapsulation is 4 mm. A permanent magnet placed above the mouse generates the magnetic field profile. A transmit/receive coil is used for RF excitation and signal reception. The PCB is inserted into the mouse and moved to target locations using a micropositioner.

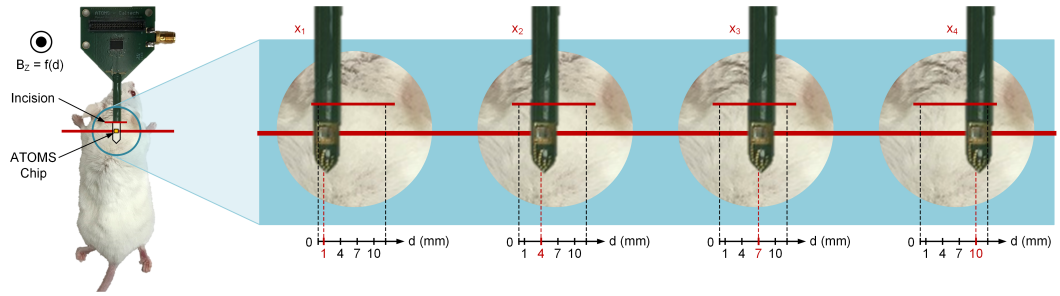


Figure 5.39: Illustration of the ATOMS chip placement. A small incision of 1.5 cm is performed into the skin of the shoulder are of the mouse for subcutaneous insertion. The chip is placed at four different locations in the same axis.

5.10 Power Consumption

The power consumption of each block per phase was measured and is shown in Table 5.1. It is interesting to note that the on-chip magnetic sensor consumes less than

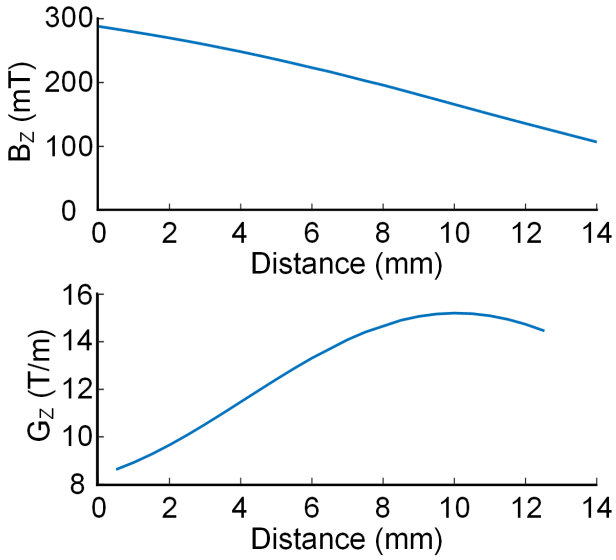


Figure 5.40: Magnetic field and magnetic field gradient produced by the magnet.

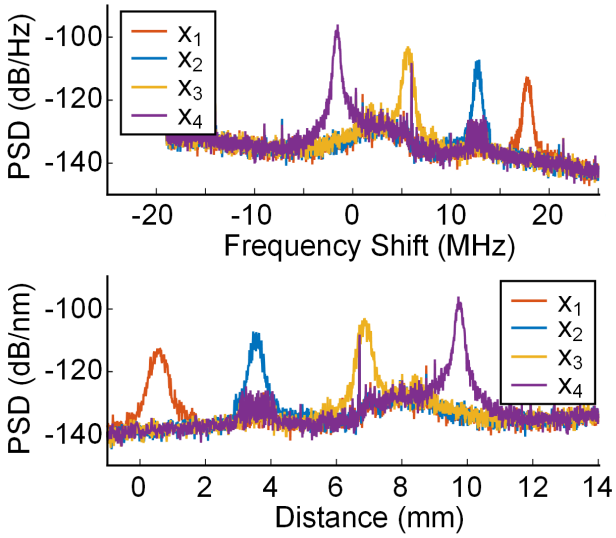


Figure 5.41: Frequency Shift-Location mapping. The figure shows the PSD of the received signal as a function of frequency shift (top) and distance (bottom).

100 μW, which is encouraging for future developments. Additionally, the power consumption of the VCO was kept low at 236.37 μW. But, the power consumption of the PA during excitation phase (RX) and transmission phase (TX) is high, reaching more than 1 mW in the case of TX. However, we have been able to reduce the duration of both phases to the sub-ms range, reducing the impact in the total average power consumption. This is shown in Table 5.2, where the power consumption and

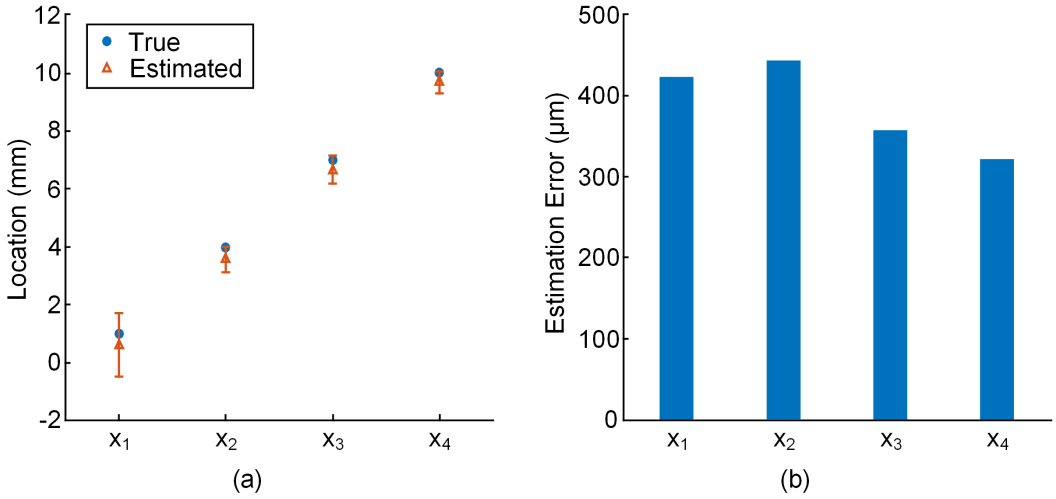


Figure 5.42: (a) Estimated and true positions of all 4 cases. N = 32. Error bars represent ± standard deviation. (b) Estimation error of the experiment.

duration of each phase are compared. Figure 5.43 shows the power consumption of the device as a function of time.

The total average power consumption of the ATOMS device is 339 μW. While in this design power is provided externally, such low power consumption allows wireless power delivery in future versions. In addition, although in this design the VCO is kept on at all times, we can easily add a lower power oscillator for the analog front-end and control logic and turn the VCO off during the magnetic phase. This minor modification can further reduce the power consumption of the device.

5.11 Discussion

In this study, we introduced the concept of ATOMS – microscale devices that mimic the behavior of nuclear spins to enable their spatial localization using the principles of MRI – and demonstrated the core element of this concept *in vitro* and *in vivo*.

Block	Power (μW)	Phase
Magnetic Sensor	75.96	MP
LNA	18.48	MP
VCO	236.37	MP, EP, TP
PLL wo/ VCO	120.48	EP
PA (RX)	690	EP
PA (TX)	1200	TP

Table 5.1: Power consumption and Activity per block.

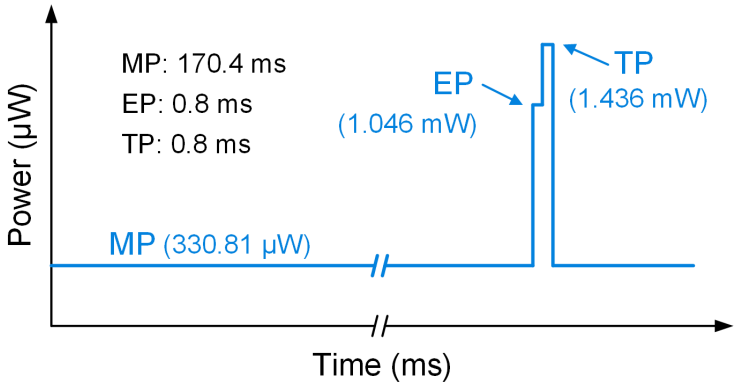


Figure 5.43: Power consumption of the ATOMS chip as a function of time, showing the power and duration of each phase.

The ATOMS technology provides an elegant solution to the problem of locating and interfacing with microscale in vivo biosensors by decoupling the dependence of RF methods from body composition and time-sensitive parameters (e.g., time-of-arrival or received-signal strength). As a result, it combines the benefits of frequency encoding using magnetic field gradients and highly sensitive RF receivers. Because ATOMS technology does not require a superconductive magnet, it offers a more affordable and simpler alternative compared to actual MRI methods that image nuclear spin precession.

The methods developed in this work can be extended to 3-D localization of microscale devices using techniques similar to MRI pulse sequences (see Chapter 3). For a single ATOMS device inside a patient, 3-D localization can be achieved by using a sequence of three magnetic field gradients in different directions (G_X, G_Y and G_Z) and performing frequency encoding in each dimension. For multiple ATOMS devices, 3-D localization can be accomplished by using selective excitation, phase encoding and frequency encoding prior to excitation. For instance, selective excitation can be performed by applying G_Z such that devices outside the slice of interest become inactivated for transmission by experiencing field magnitudes above a cer-

Phase	Power (μW)	Duration (ms)
Magnetic Phase	330.81	170.4
Excitation Phase	1046	0.8
Transmission Phase	1436.37	0.8
Total Average	339	172

Table 5.2: Power consumption and duration of each phase.

tain threshold. Phase encoding can be achieved by producing a phase shift (using a digitally controlled phase shifter) proportional to the magnetic field generated by G_Y. Finally, frequency encoding can be performed by applying G_X as described in the previous sections.

In the case of an angular misalignment of θ° between B_Z and the ATOMS device, the accuracy of the system can reduce because the magnetic sensor measures the magnetic field orthogonal to its surface (i.e., $B_Z \cos\theta$). To overcome this limitation, we can add an extra step in the pulse sequence where a uniform magnetic field B_C is applied to measure a correction factor and correctly estimate B_{G_Z}, the magnetic field generated by G_Z at the location of the chip (Chapter 3). It can be shown that $B_{G_Z} = B_C \Delta f_{MZ}/\Delta f_{MC}$, where Δf_{MZ} is the frequency shift due to $B_{MZ} = B_{G_Z} \cos\theta$, and Δf_{MC} is the frequency shift due to $B_{MC} = B_C \cos\theta$ (see Chapter 2 for detailed derivation). This approach allows the correct estimation of the chip's location and enables the estimation of its orientation as long as the local magnetic fields B_{MC} and B_{MZ} are above the noise floor of the magnetic sensor. In addition, this method can be applied to phase encoding as well.

The noise of the magnetic sensor and the phase noise of the oscillator are the main factors that affect the minimum detectable frequency shift $\Delta f_{\min}$ and, therefore, the resolution of the system. As we have shown, for frequency encoding, the theoretical spatial resolution is given by

$$\Delta x = \frac{\Delta f_{\min}}{\gamma_{ATOMS}\, G_Z}, \tag{5.2}$$

where $\Delta f_{\min} = 2\sigma_f$, and σ_f is the standard deviation of the oscillation frequency (see Chapter 3 for detailed derivation). For an ATOMS device with a magnetic sensor noise of σ_{MS} and an oscillator phase noise profile of $S_\phi(\omega)$, σ_f is defined as $\sqrt{(\gamma_{ATOMS}\,\sigma_{MS})^2 + \sigma_{PN}^2}$, where σ_{PN} is the standard deviation of the oscillator's phase noise. Since the dominant noise source close to the oscillation frequency is flicker noise, $S_\phi(\omega)$ can be approximated by a Gaussian profile in this region [72]–[74], and its standard deviation can be estimated by $\sigma_{PN} \approx FWHM_{S_\phi}/2.355$. For example, according to Equation 5.2, the resolution of our current *in vivo* system would be limited to 360 μm (γ_{ATOMS} = 170.7 MHz/T, G_Z = 9 T/m). It is important to note that, in this design, the magnetic sensor noise and oscillator's phase noise are limited by the budgeted power consumption targeting a wirelessly powered implantable device. Other applications such as capsule endoscopy or minimally invasive surgery [1], [3], [4] are usually powered via batteries and present higher

power budgets that, if applied to our approach, can boost the performance of the sensor and oscillator, and therefore the resolution of the system.

The strength of the magnetic field gradient also impacts the localization resolution. Our experiments show an *in vivo* accuracy of ~500 μm when the field gradient is ~10 T/m. Therefore, in our current implementation, a magnetic field gradient of ~5 T/m is required to design a system with 1 mm resolution. High field gradients are already in use in the field of magnetic particle imaging with values as high as 7 T/m [87]. Thus, the generation of high field gradients for a high-accuracy ATOMS system is feasible. A potential limitation of such a system is the relatively small range of high field gradients in space, because they decay with the distance from the source and thus limit the localization area. However, we can use multiple magnetic field sources to enhance the coverage and expand the FOV. Although using multiple sources creates an underdetermined mathematical framework, the position can still be estimated with high accuracy by prioritizing the readings from sources closer to the ATOMS device.

With precise localization *in vivo*, ATOMS-enabled devices can act as real-time sensors and actuators for diagnosis and therapy. For sensors, information about the measured quantity can be encoded in the device's transmitted output via amplitude or time modulation. For actuators, slice selection in three dimensions can activate a therapeutic event for ATOMS-enabled devices located only at a specific spot in the body.

5.12 Methods

Animal Procedures

A small incision of 1.5 cm was done into the skin of the shoulder area of a female wild-type mouse to insert the microchip. The mouse was anesthetized during the entire experiment with an IP injection of ketamine/xylazine (100 and 10 mg/kg of BW respectively). The incision area was shaved and cleaned before insertion of the microchip. An RF signal and a magnetic field was applied using a small antenna and a permanent magnet. The chip measured these signals and then radiated an RF signal back. This signal was picked up by the antenna to be analyzed. The signal was measured for 5 min per location. A total of four locations were measured. This animal procedure was approved by the Institutional Animal Care and Use Committee of the California Institute of Technology.

Data Analysis

The detection algorithm, fits and measurement figures were written and generated in MATLAB running on a standard workstation.

Chapter 6

A FULLY INTRAOCULAR HIGH-DENSITY SELF-CALIBRATING EPIRETINAL PROSTHESIS

6.1 Introduction

Retinal degenerative diseases such as retinitis pigmentosa (RP) and age-related macular degeneration (AMD) are the leading causes of blindness [18], affecting millions worldwide. RP and AMD damage the photoreceptor cells (rods and cones), resulting in profound vision loss, but leave the inner retinal cells (bipolar, horizontal and ganglion cells) functional [88]–[90]. Retinal prostheses (Fig. 6.1) aim to restore vision in these patients by bypassing the damaged photoreceptors and directly stimulating the remaining healthy neurons. There are three main approaches in retinal prostheses which are based on the location of the electrode array: epiretinal, subretinal, and suprachoroidal approaches. In an epiretinal prosthesis the electrode array is placed in front of the retina, in a subretinal prosthesis it is placed between the retina and the retinal pigment epithelium, and in a suprachoroidal prosthesis it is placed between the choroidal and the sclera. Each method presents different requirements in terms of space, medical procedures, and electrode-tissue interface [91], and each has its own advantages and disadvantages. Further discussions on these techniques are well summarized in [18], [91]–[106].

The prosthesis stimulates the retina using electrical stimulation. Fig. 6.2(a) shows a model of the stimulator array and the electrode-retina interface. This interface presents a high impedance as a result of the small size of the electrode (100μm diameter). The stimulator, which can be modeled as a charge-pump, generates a biphasic current waveform to stimulate the retina (Fig. 6.2(b)). During the first phase, charge is injected into the tissue, which changes the membrane potential of adjacent cells and makes them fire. In the second phase, this charge is removed from the tissue, reducing the residual charge close to zero. This is important because any remaining charge beyond tolerable limits can cause electrolysis that may result in tissue damage and electrode corrosion. Therefore, charge-balanced stimulation is essential and requires anodic and cathodic currents to be equal. Another significant characteristic is the stimulation waveform. The shape and duration of each phase, as well as the interphase delay and the period, are important stimulation

parameters. Several studies have shown that more sophisticated waveforms such as high-frequency pulse trains, asymmetric biphasic pulses, or non-rectangular shapes (Gaussian, linear and exponential), present advantages over biphasic pulses [107]–[110]. A recent publication [111] has proved that flexible stimulation such as step-down current pulse shape can potentially reduce the required voltage compliance by 10%-15%. Thus, having a highly flexible stimulation waveform is desirable and allows further studies in stimulation efficiency, color perception, and multi-channel stimulation [14], [91], [108].

Recent work on retinal prostheses has shown significant progress over the past decade. Clinical trials have proven to successfully provide visual restoration with an acuity on the order of 20/1200 to blind patients suffering from retinal degeneration [18]. Simulation studies in normally sighted subjects have predicted that hundreds of channels are needed to restore functional visual perception to a degree that will enable tasks such as reading and face recognition [102]. In recent epiretinal prostheses, the number of electrodes has increased considerably, achieving up to 1024 channels [16] using a 1:4 demux scheme and limiting the functionality of the system to biphasic pulses. However, previous work has used extraocular implants with a trans-sclera trans-choroid cable to connect the electrode array to the retina [93], [94], [99], [112]. Although this method results in a less invasive surgery [94], this cable can cause infection and low intraocular pressure (hypotony) in the long term. To avoid the use of such a cable, a fully intraocular implant is desired. Intraocular coils as well as low power and small size electronics are needed. The former requires the development of high-Q flexible intraocular coils. For the latter, it is essential to reduce off-chip components such as crystal oscillators and diodes, and to make the chip smaller and low power.

Initial designs targeted current levels up to 1mA to ensure stimulation of retinal cells. For such designs, an output compliance of >10V was required [108], [112] due to the high impedance of the electrode-retina interface (Fig. 6.2(a)). Therefore, high-voltage (HV) technologies were used at the expense of area and power consumption [91], [108], [112]–[114]. Human clinical trials have recently shown that implanted electrodes present a stimulus threshold as low as 20μA for a 260μm diameter electrode implanted in the macular region [102], [115]. In addition, advances in implant technology promise close placement of the electrode array and retinal tissue, which can further decrease the required current. This opens a window for highly scaled technologies to reduce area and power, and to support hundreds of flexible

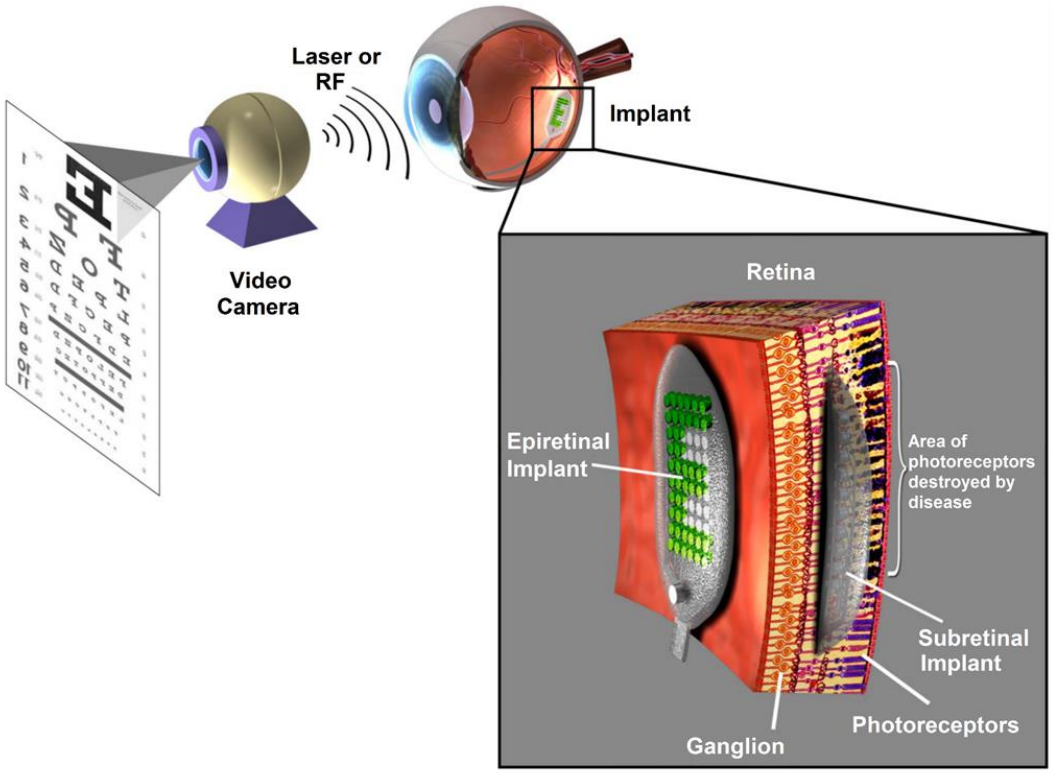


Figure 6.1: Retinal Prosthesis (Image courtesy of [97]).

channels for fully intraocular implants.

In this work, a fully intraocular high-density self-calibrating epiretinal prosthesis implemented in 65nm CMOS is presented. It provides charge-balanced stimulation with highly flexible waveforms. It features dual-band telemetry for power and data, on-chip rectifier and clock recovery, a digital calibration technique to match biphasic stimulation currents, and 512 independent channels capable of arbitrary waveform generation.

6.2 System Architecture

The system architecture of the fully intraocular implant is shown in Fig. 6.3. It consists of two intraocular coils, the 65nm IC, off-chip capacitors, electrode array, and the biocompatible flexible parylene substrate. Power and data are wirelessly transmitted to the implant using dual-band telemetry via a pair of inductively coupled coils. The power telemetry operates at 10MHz and produces 4 different supplies: ±2Vdd for stimulation and ±Vdd for the rest of the system. The data telemetry recovers the clock from the power signal and produces 160MHz and 20MHz clocks. These signals are used by the phase-shift keying (PSK) receiver to demodulate the

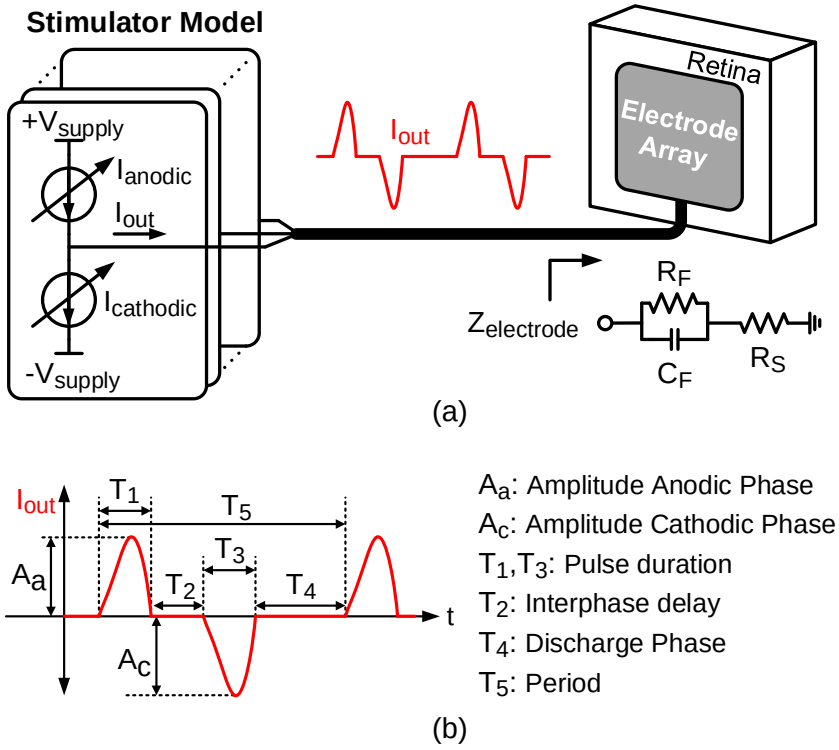


Figure 6.2: (a) Model of the stimulator array and electrode-retina interface, where C_F represents the double-layer capacitance, R_F the faradaic charge transfer, and R_S the solution impedance. (b) Stimulation current waveform.

20Mb/s data. The stimulator array presents 512 independent channels which are grouped into 8 blocks of 16 4-channel stimulators. The global logic receives and demultiplexes the data to each block, running at 20MHz.

3-coil Power Transmission

Fig. 6.4 shows the 3-coil power transmission scheme [116]. The transmitter coil (L1) has an outer diameter (OD) of 42mm and is placed on external eye-glasses. The buffer coil (L2) is smaller (20mm OD) and is placed inside contact lenses. The intraocular receiver coil (L3) is a flexible MEMS origami foil coil. It is placed in the anterior chamber of the eye after the crystalline lens is removed. This imposes hard constrains on its size (<10mm OD) and weight (<46mg in saline). The intraocular coil presents a Q of 24 at 10MHz in air, 10mg of mass in saline, and a size of 10mm OD and 1mm thickness. The distance between L1 and L3 and the small size and weight of the latter reduces the coupling coefficient κ_{13} drastically. The insertion of the buffer coil enhances coupling coefficients κ_{12} and κ_{23} due to its high Q and close proximity to the eye. This scheme achieves an efficiency of 36% with 1 inch

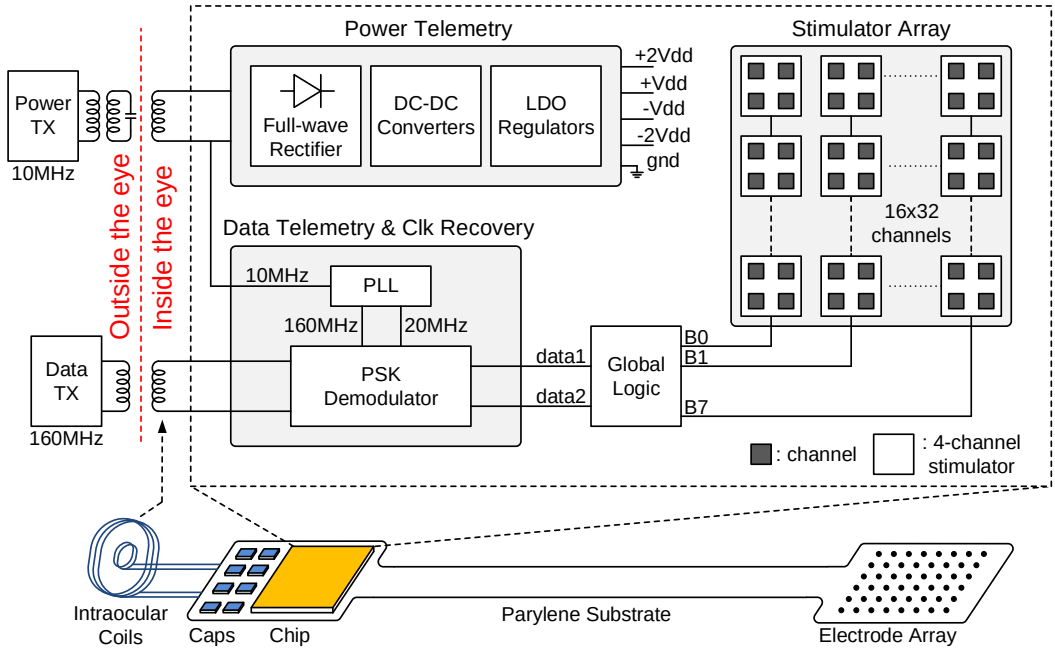


Figure 6.3: Fully intraocular epiretinal prosthesis system architecture (modified from [14]).

separation in saline, showing a 5x improvement over the 2-coil scheme [116]. It is comparable to the 40% efficiency of the extraocular 2-coil scheme with 18mm separation presented in [15]. Capacitors C1, C2, and C3 resonate coils L1, L2, and L3, respectively. Further information about the 3-coil power transmission scheme can be found in [116].

Power Telemetry

The power telemetry (Fig. 6.5) operates at 10MHz. It consists of a full-wave rectifier, a positive and a negative bandgap reference, three DC-DC converters and four low-dropout (LDO) regulators. To reduce the number of off-chip components, an on-chip rectifier was implemented to replace the external diodes used in previous designs [91], [93], [99], [112]. It rectifies the incoming power signal to output V_{rec} which is then used by the DC-DC converters to generate $-V_{rec}$ and $\pm 2V_{rec}$. These signals are used by the LDO regulators to produce the supplies ±Vdd and ±2Vdd. Reference voltages for the LDO regulators are generated by the bandgaps. The rectifier, DC-DC converters and LDO regulators are optimized for efficiency achieving >80%, >90%, and >85%, respectively, for a total combine efficiency of 65%.

The schematic of the proposed full-wave rectifier is shown in Fig. 6.6(a). In

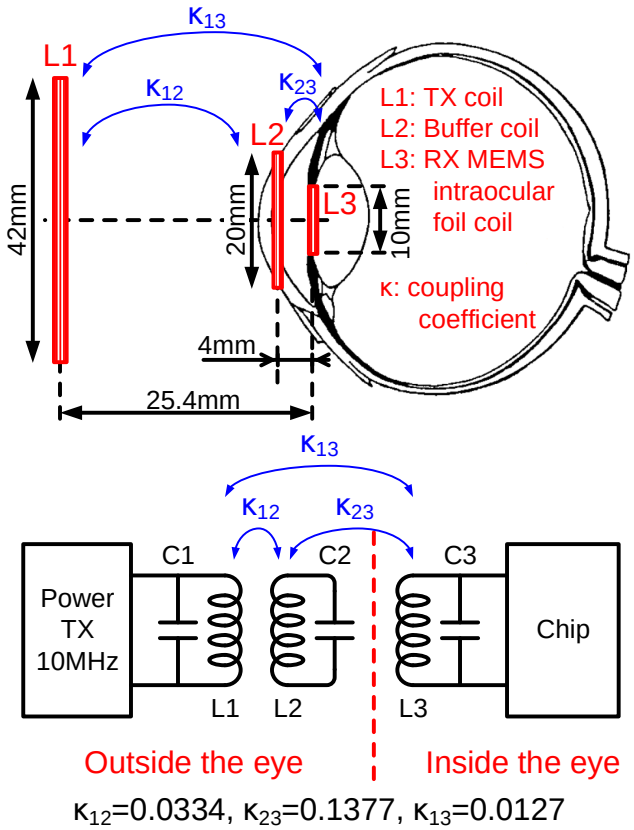


Figure 6.4: Three-coil inductive power transmission (modified from [14]).

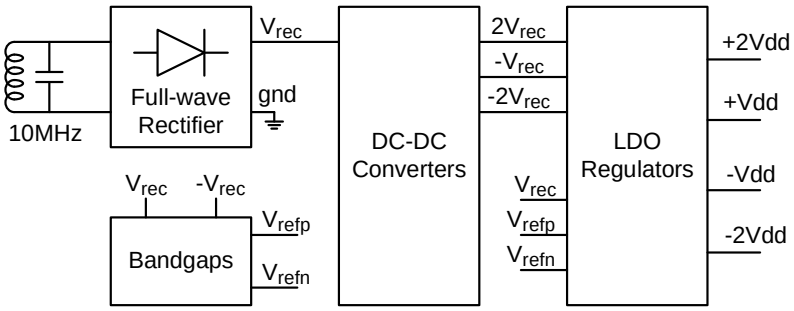


Figure 6.5: Schematic of the power telemetry. DC-DC conversion sequence: $V_{rec} \rightarrow 2V_{rec}$, $V_{rec} \rightarrow -V_{rec}$, $-V_{rec} \rightarrow -2V_{rec}$ (modified from [14]).

order to increase the efficiency of this stage, two unidirectional switches are used to prevent reverse conduction loss in the power transistors. A comparison between a pass transistor switch and the proposed unidirectional switch (Fig. 6.6(b)) shows the advantages of the latter over a traditional implementation. In a pass transistor switch, when $V_{inn}<V_{rec}<V_{inp}$, the transistor M0 is in forward conduction and power is transferred from the input to the output. However, when V_{inp} decreases lower

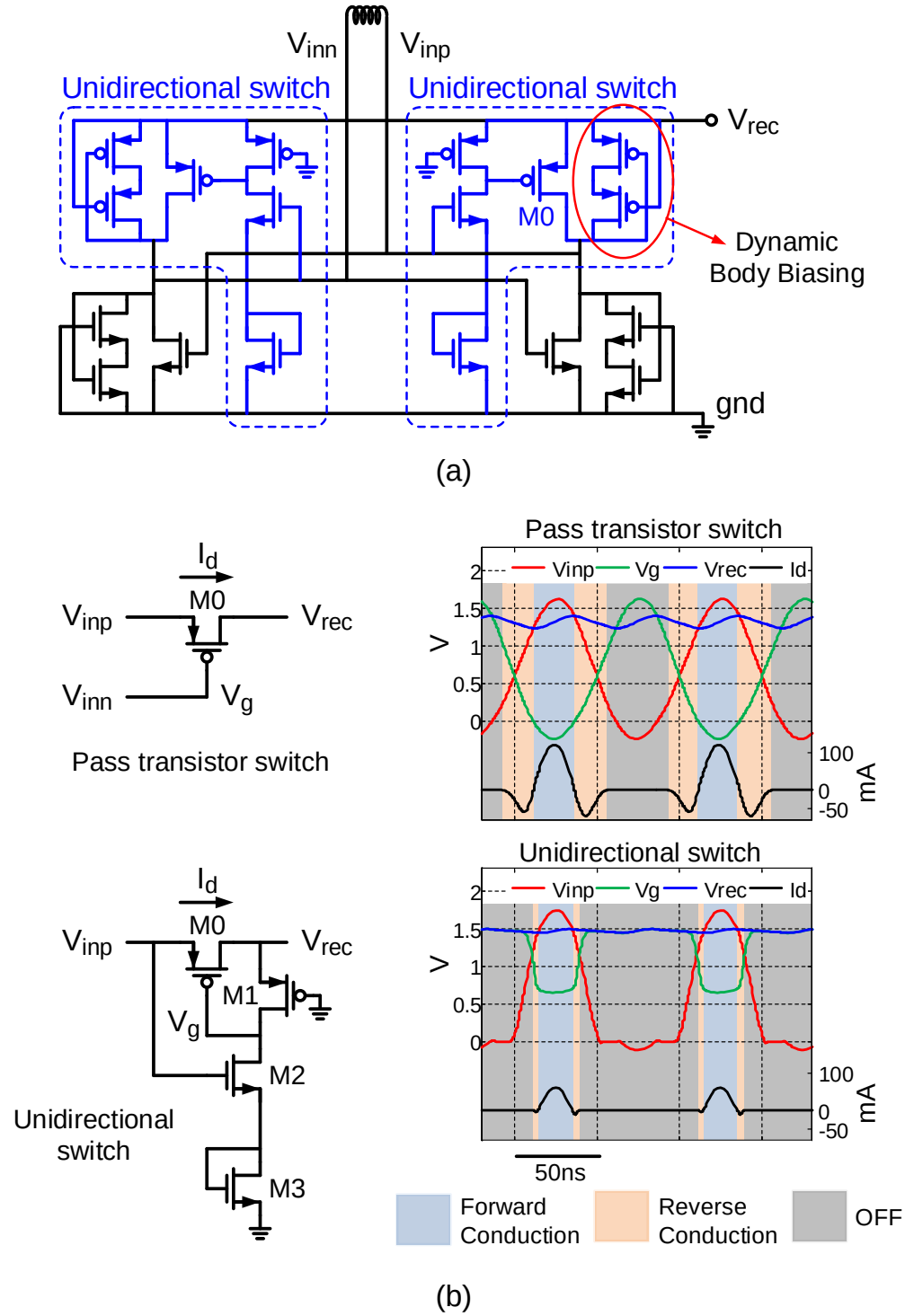


Figure 6.6: (a) Transistor-level schematic of the proposed full-wave rectifier (modified from [14]). (b) Comparison between the pass transistor switch and the unidirectional switch showing the reduction in reverse conduction loss.

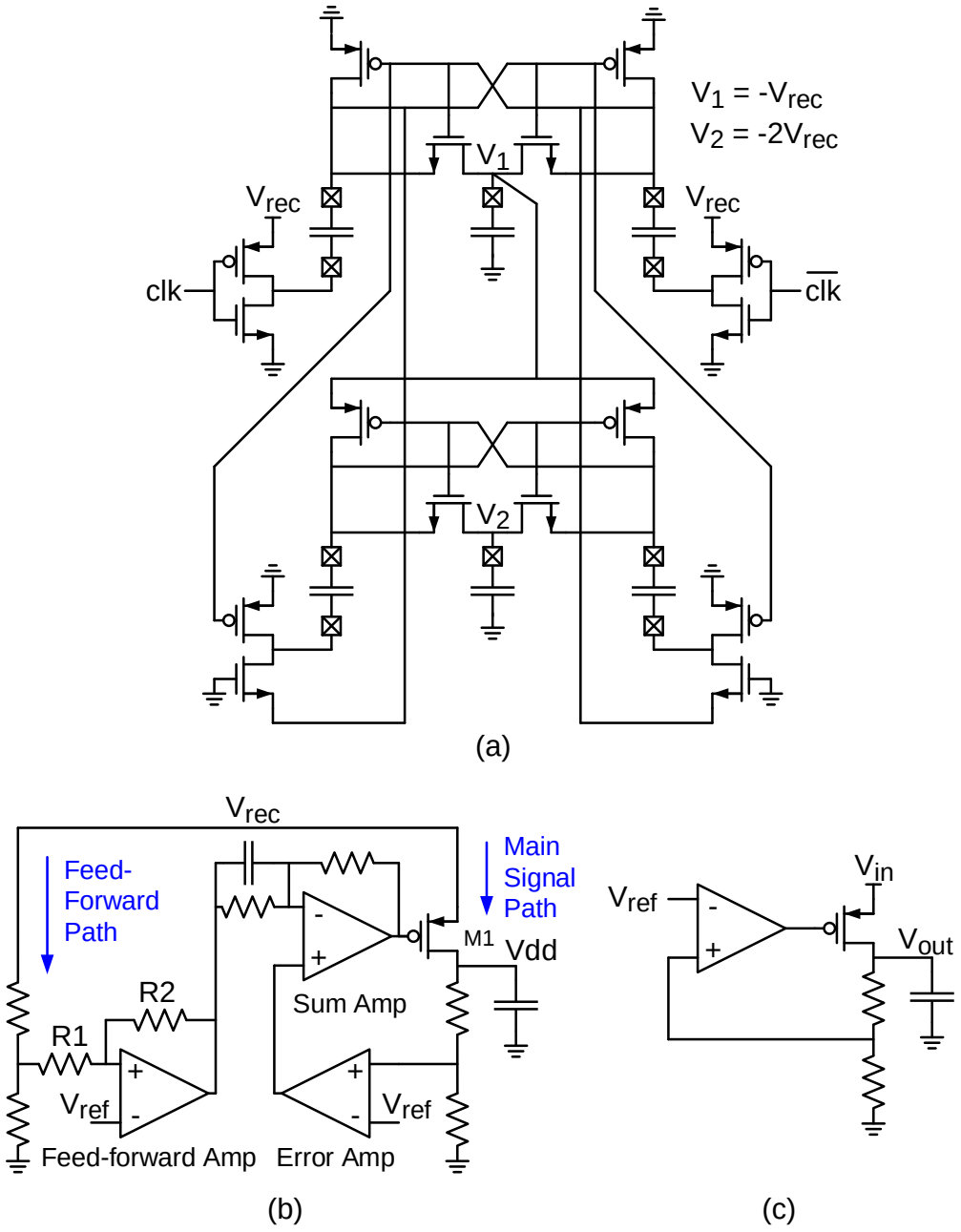


Figure 6.7: Schematics of the (a) charge-pump DC-DC converter that generates $-V_{rec}$ and $-2V_{rec}$, (b) feed-forward ripple cancellation LDO regulator that generates Vdd (modified from [14]), and (c) LDO regulator that generates -Vdd and ±2Vdd.

than V_{rec} while V_{inn} is still low ($V_{inn}<V_{inp}<V_{rec}$), reverse conduction occurs. This is not desired and reduces the efficiency of the stage considerably. In the proposed switch, reverse conduction is minimized by the addition of transistors M1-M3. When $V_{inp}<2V_{th}$, transistors M2 and M3 are off and leave transistor M1 on. This transistor shorts the gate of the power transistor M0 to V_{rec} and turns it off. When

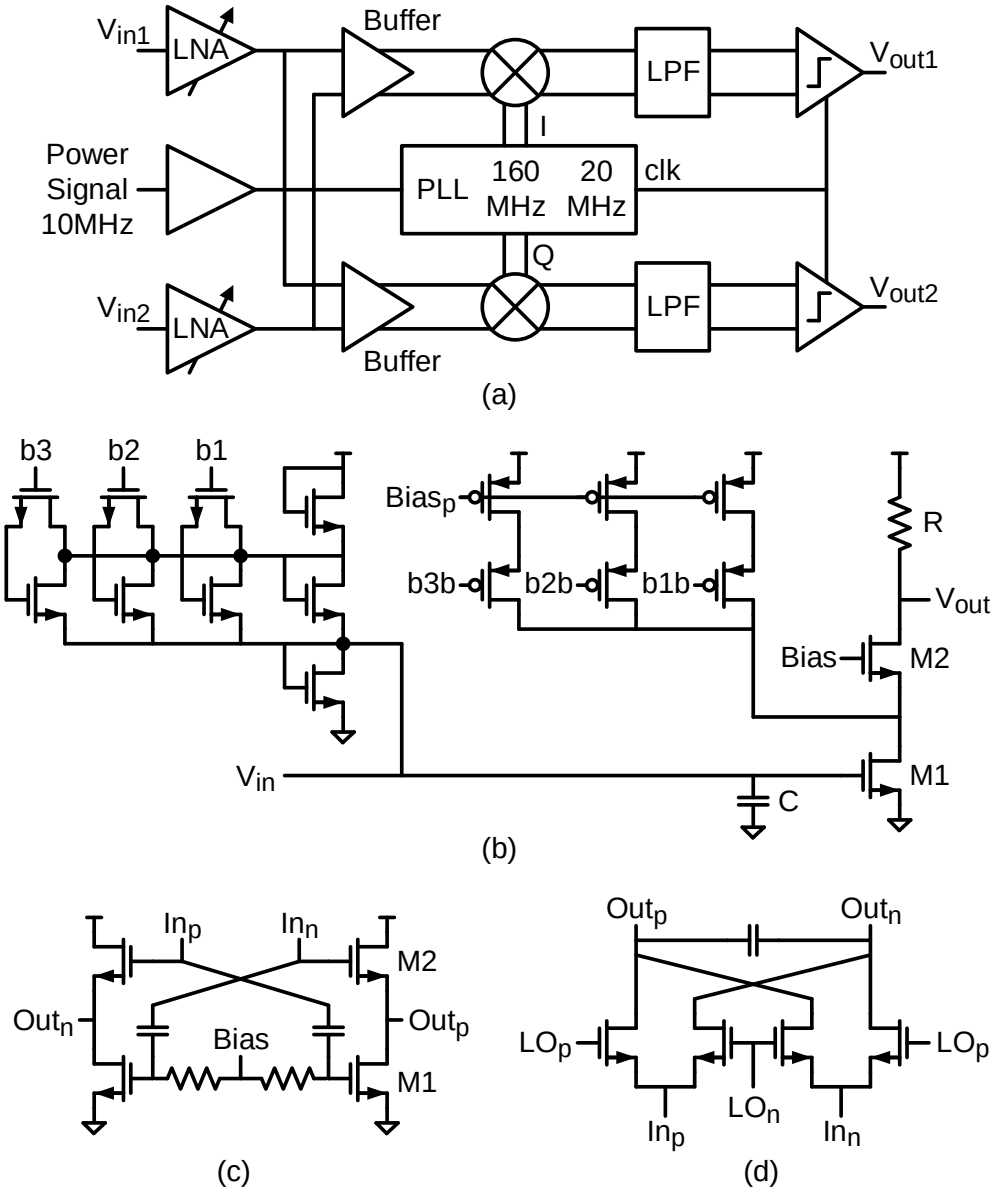


Figure 6.8: Schematic of the (a) data telemetry and clock recovery [14], (b) LNA with gain control, (c) differential buffer, and (d) passive-mixer.

$V_{inp}>2V_{th}$, transistors M2 and M3 turn on, turning M0 on by reducing its gate voltage. Therefore, forward conduction occurs when $V_{inp}>V_{rec}>2V_{th}$ while reverse conduction is limited to $V_{rec}>V_{inp}>2V_{th}$. Simulation results are also shown in Fig. 6.6(b). A color scheme shows the three regions of operation of the switch: forward conduction, reverse conduction and cut-off. It can be seen that the reverse conduction region is minimized when the unidirectional switches are used. This technique improves the efficiency of the stage to more than 80% while delivering

≈25mW.

The DC-DC converters are implemented using charge-pump circuits. A single stage charge-pump circuit is used to generate +2V_{rec} while two stages of charge-pump are cascaded to generate -V_{rec} and -2V_{rec} from the output of the rectifier. This last charge-pump circuit is shown in Fig. 6.7(a).

The regulator that generates Vdd employs a feed-forward ripple cancellation scheme and is shown in Fig. 6.7(b). This technique filters out the input ripples by replicating the same ripples at the gate of transistor M1 through the feed-forward path. Resistors R1 and R2 set the feed-forward gain to cancel the noise from the main signal path. In addition, due to the inherent high bandwidth of the feed-forward configuration, significant PSRR is achieved at high frequencies [117]. To further enhance the PSRR bandwidth, a zero is introduced in the summing amplifier to cancel the dominant pole of the system. Three additional regulators, as shown in Fig. 6.7(c), are employed to generate -Vdd and ±2Vdd for the stimulation circuitry.

Data Telemetry

The schematic of the data telemetry is shown in Fig. 6.8(a). It implements a pseudo-differential PSK demodulator with gain control and a PLL for clock recovery. The multiplication factor in the PLL allows for the use of the 10MHz power signal as a reference to generate I/Q 160MHz clocks for down-conversion and a 20MHz clock for the data slicers. This alleviates the need for an external reference which, in previous designs, was provided by an external crystal oscillator [16], [112]. The LNA (Fig. 6.8(b)) is a single-ended cascode amplifier with gain control. The gain control is obtained by a 3-bit programmable bias scheme. These bits modify the transconductance of M1 by changing its bias voltage and drain current, providing a minimum gain of 10. The LNA presents a narrow-band 50Ω input impedance at 160MHz set by the capacitor C, the transistor M1, the bias network, and the external coil. The buffer (Fig. 6.8(c)) is a hybrid differential common-source/common-drain amplifier which improves the voltage-gain to $A_v \approx -(g_{m1} + g_{m2})/g_{m2}$. The output of each buffer is then mixed by a passive-mixer with the I/Q 160MHz clocks, respectively. Passive-mixers (Fig. 6.8(d)) were chosen to reduce power consumption. The size of the mixer switches is optimized to minimize the voltage drop and non-linearity effects. The low-pass filter is added at the output of the mixer and is implemented by a passive RC-filter. The low-power sense amplifier is a standard Strong-Arm latch followed by a SR latch.

Given the following input signals:

$$V_{in1}(t) = A\sin(\omega t + \phi_1) \tag{6.1}$$

$$V_{in2}(t) = A\cos(\omega t + \phi_2), \tag{6.2}$$

where A is the amplitude of the received signal and $\phi_1, \phi_2 \in \{0°, 180°\}$, the datapath produces 2 data streams:

$$V_{out1}(t) = \frac{AA_T}{2}\cos(\phi_1) = \pm\frac{AA_T}{2} \tag{6.3}$$

$$V_{out2}(t) = -\frac{AA_T}{2}\cos(\phi_2) = \mp\frac{AA_T}{2}, \tag{6.4}$$

where $A_T = A_{\text{LNA}} \cdot A_{\text{Buffer}}$. Each data stream supports data rates up to 20Mb/s, for a combine data rate of 40Mb/s, although only 20Mb/s is required for single-chip operation. The datapath and PLL consume 2.3mA and 350μA, respectively.

Stimulator Array

The stimulator array, shown in Fig. 6.9(a), is composed of 512 independent channels grouped into 8 blocks. Each block consists of 16 4-channel stimulators, which are explained in detail in section III and section IV. The input of each stimulator is serialized and connected to all stimulators in the same block. This makes a 256-bit scan chain per block (4-bit per channel). The 8 scan chains are connected to the outputs of the global logic. The global logic receives the demodulated data, processes it and demultiplexes it into 8 bit streams running at 20MHz. It implements the communication protocol shown in Fig. 6.9(b). In case of communication error, the whole package is discarded, the scan chains are reset, and all the stimulators receive a zero input.

In this work a high resolution current-based stimulation scheme has been utilized. The voltage-based stimulation technique reported in [118] promises high energy-efficiency, but it is more suitable for relatively long stimulation pulses (more than 8ms). A global reference current, generated by the bandgap, is distributed to each stimulator using a tree structure. Cascode current mirrors with transistors biased in strong inversion are used to minimize current variations. Simulation results showed that the reference current at each 4-channel stimulator has a σ=21.7nA while distributing 1.3μA.

Multi-chip configuration

An additional feature of the system is its capability for 2-chip configuration in a Master/Slave fashion. In this case, both coils (power and data) are connected to the

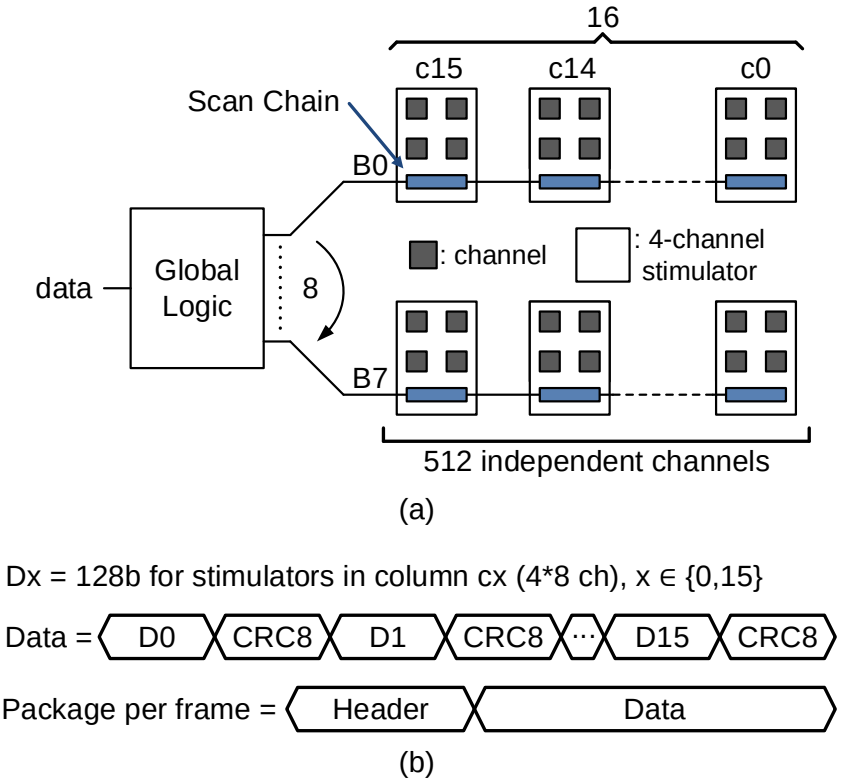


Figure 6.9: (a) Schematic of the global logic and stimulator array showing scan chain connections. (b) Communication protocol for data transmission.

master chip which generates the supplies and demodulates the data. In particular, it produces two data streams, V_{out1} and V_{out2} (Fig. 6.8(a)), according to equations 6.3 and 6.4. One of them is used in the master chip while the other is sent to the slave chip. The power and data telemetry circuits in the slave chip are shut down, since it receives the supplies and data stream from the master chip. Thus, both chips can be integrated in parylene to support 1024 independent channels. As the number of required electrodes for retinal prosthesis continues to increase, this technique will allow the use of multiple chips to configure a network to scale up the number of channels of the design with only minor modifications.

6.3 Calibration Methods for Neural Stimulators

Matching the current or charge of biphasic stimulation is an important design consideration in neural implants. Previous studies in cochlear implants have shown that a residual DC current of more than 100nA is highly correlated with neural tissue damage [119] and that this value has been suggested as a safety limit [120]–[122]. However, a safety limit for retinal prosthesis has not been established yet and it de-

pends on electrode material, and electrode size and shape, as well as charge density [33], [123].

A large DC blocking capacitor in series with the electrode can reduce the residual DC current to minimal levels (<1nA) [114], but hundreds of capacitors in the nF range are not realizable for retinal prostheses [124]. Simple passive charge-balancing techniques rely on shorting the stimulation electrode to the counter electrode. The effectiveness of this technique depends on the initial charge imbalance, the time constant associated with the electrode-tissue interface, and the available time for the discharge phase [114]. The charge error after stimulation Q_{error} is caused by the mismatch between anodic and cathodic currents, and the difference between the duration of each phase. For example, a 5μA mismatch between stimulation currents in a 2ms 100Hz biphasic pulse with 1ms duration at each phase (i.e. pulse duration difference is negligible) generates a Q_{error}=5μA×1ms=5nC. Assuming there is no interface delay, the discharge phase is $\tau_{discharge}$=10ms-2ms=8ms. For a stimulation period T and a time constant τ=(R_{SW}+R_S)×C_F=3ms, where R_{SW} is the shorting switch resistance, R_S is the tissue resistance, and C_F represents the double-layer capacitance of the interface, the net DC current error is defined as:

$$I_{\mathrm{DCerror}} = \frac{Q_{\mathrm{remained}}}{T} = \frac{Q_{\mathrm{error}} \cdot e^{-\tau_{\mathrm{discharge}}/\tau}}{T}, \tag{6.5}$$

which is equal to 34.74nA. Although this value is less than 100nA, for reasons of patient safety, it is desirable to achieve a more precise charge balance with a DC current error close to the level produced by DC blocking capacitors [114]. Therefore, it is important to reduce the initial charge imbalance by matching anodic and cathodic currents with high precision [91], [108].

Previous work

Several methods to achieve charge-balanced stimulation have been reported in the literature. An analog negative feedback technique to sample and hold a correction current to improve current matching has been used in [113]. A similar technique, dynamic current matching, is used in [114]. Here, a single DAC generates the cathodic current which is sampled by a pmos transistor to produce the anodic current. These schemes require the use of large capacitors to store the sampled voltage for the duration of both phases. This increases the area of the stimulator considerably, making them not suitable for a multi-channel implant. They also need to run for every stimulation, which increases the power consumption. Furthermore, they rely on constant output current that limits them to biphasic pulses.

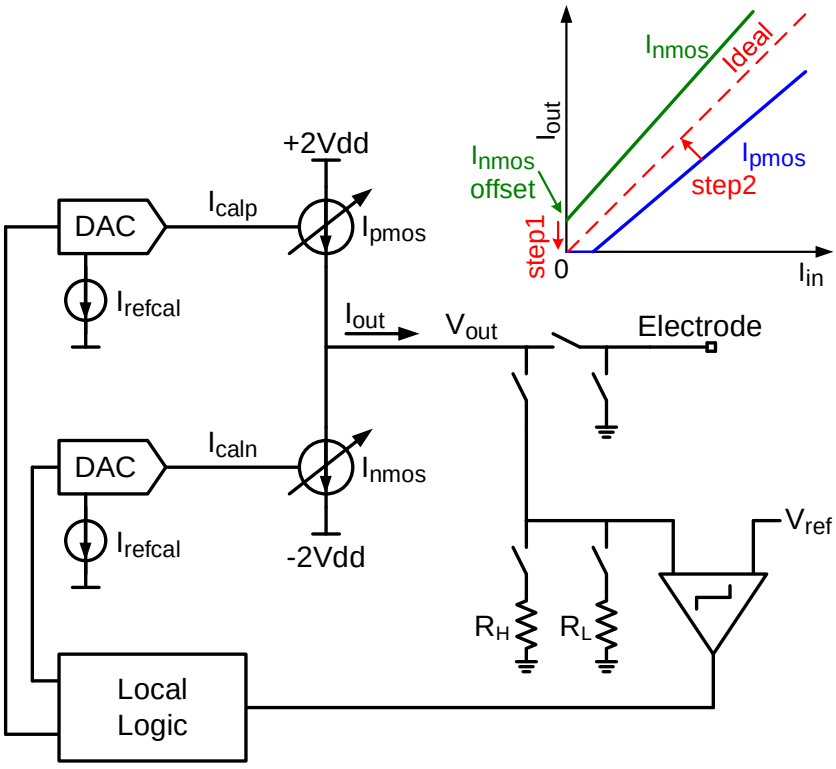


Figure 6.10: Model of the proposed calibration scheme and illustration of the non-ideal initial characteristics of I_{nmos} and I_{pmos} due to process variation.

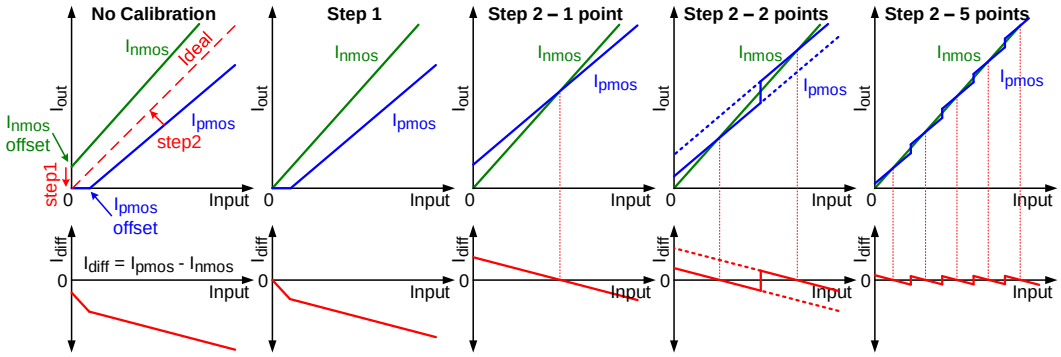


Figure 6.11: Conceptual model of the two-step multi-point calibration scheme [14].

Active charge balancers [91], [108] monitor any residual charge in the tissue after every stimulation and keep this charge within a safety window of $\approx \pm 100$mV. Two different approaches have been presented: active charge balancers based on pulse insertion and based on offset regulation. The former cancels the remaining charge instantaneously via short current pulses [91], while the latter cancels the remaining charge in the long-term by adjusting the offset of the stimulation currents

[108], [125]. The precision of charge balance in this technique is a function of the capacitance of the electrode-tissue interface [114]. In addition, this compensation depends on the output waveform and changes for different wave shapes.

In this work, we propose a digital calibration technique to match anodic (I_{pmos}) and cathodic (I_{nmos}) currents, and to reduce area and power consumption. The calibration needs to run only once when the implant is turned on (e.g. daily).

Two-step digital calibration scheme

A model of the stimulator connected to the calibration circuitry is shown in Fig. 6.10. Two switched resistors are used to sense the output current I_{out} during calibration. The high resistor R_H increases the conversion gain when I_{out} is low, while the low resistor R_L ensures voltage compliance when I_{out} is high. This measured voltage (V_{out}) is then compared to V_{ref} to produce a digital output that is sent to the local logic. Based on this result, the local logic adjusts two current DACs to calibrate the stimulation currents. As illustrated in the same figure, anodic and cathodic currents differ from an ideal behavior due to process variation. To compensate for this difference, a two-step digital calibration scheme is proposed. During the first step, the offset of I_{nmos}, which is the current value at zero input, is cancelled. In the second step, I_{pmos} is matched to I_{nmos} by reducing their difference (I_{diff}).

Step 1

To measure the offset of I_{nmos}, R_H is connected to the output, a zero input is set, and the I_{nmos} current source is turned on. As a result, the offset of I_{nmos} flows to R_H. The voltage across this resistor (V_{out}) is then compared to V_{ref}. Based on this, the calibration current I_{caln} is changed to adjust I_{nmos} until the comparator switches. Finally, the value of the calibration DAC is stored in a local register. For this step, V_{ref} is set to -ΔV to account for the fact that the offset of I_{nmos} flows from R_H to the current source making V_{out} always negative. In order to switch the comparator, V_{out} is compared to a small negative voltage so that, when the offset gets reduced, the comparator switches.

Step 2

To measure I_{diff}, R_L is connected to the output and both currents are turned on so that I_{diff} flows to R_L. Using the same method as the previous case with V_{ref} set to

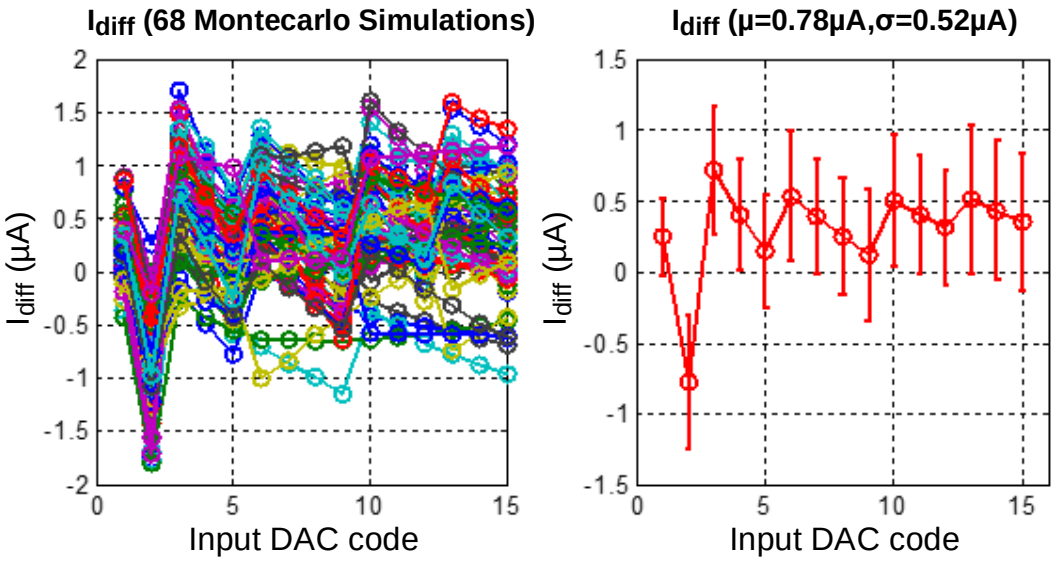


Figure 6.12: Montecarlo simulation of the two-step calibration scheme showing a current mismatch with μ=0.78μA and σ=0.52μA.

0V (since I_{diff} can flow in both directions), the calibration current I_{calp} is adjusted to reduce I_{diff}. Then, the calibration value is also stored in a local register.

Multi-point calibration

Since the slope of the two currents can vary, reducing I_{diff} at one point does not guarantee to match them over the entire range. To overcome this issue, the output current range is split into regions and a distinct calibration is performed for each region. By increasing the number of calibration points, the overall difference of the currents I_{diff} gets reduced over the entire range. In this design, for the target mismatch of <5% that correspond to 2.5μA, a 5-point calibration scheme was chosen.

Fig. 6.11 illustrates the conceptual model of the calibration scheme. Simulation results from a Montecarlo simulation are shown in Fig. 6.12. The calibration scheme was able to adjust the currents in all cases and achieve significant improvement in matching. The current mismatch after calibration has a mean (μ) of 0.78μA and standard deviation (σ) of 0.52μA. Details of the implementation and analysis of the effects of process variation in the calibration scheme are explained in section IV.B.

6.4 Self-Calibrating 4-Channel Stimulator

The circuit level implementation of the proposed stimulator is shown in Fig. 6.13. It consists of four independent current drivers, which share calibration circuitry and

local logic. Each current driver presents a 5V output stage and produces an arbitrary output waveform with 4 bits of resolution at 109.2μs time-steps. A 4-bit input signal determines the input current I_{in}. This current is mirrored to the output stage to produce either the anodic current I_{pmos} or the cathodic current I_{nmos}, depending on the stimulation phase. The local logic controls the stimulation and the calibration. It has a serial interface that enables the use of simple cascade connections to build the array. It is important to mention that while the calibration circuitry is shared among every four channels, each channel is calibrated independently.

Current Driver

The schematic of the current driver is shown in Fig. 6.13. To enable robust operation with high output voltage, low-headroom current mirrors and protection transistors have been used. Low-voltage (LV) transistors are used extensively, and high voltage transistors are used only for protection. A 5V output stage is designed using 1.2V core and 2.5V I/O transistors, and is limited by the nwell-substrate junction breakdown voltage (6V in this process).

Low-headroom current mirrors are used at the output stage to increase the voltage compliance. The current mirror is a variation of [126] and presents a high output resistance with low headroom (Fig. 6.14(a)). Two current sources bias transistors M4 and M5 and reduce the drain voltage of M1 and M2 for low-headroom operation. M3 increases the loop gain, which increases the output resistance. The circuit is optimized for low headroom at the expense of higher mismatch. However, this mismatch is compensated by the calibration scheme. Transistors M6 and M7 are added to either increase or decrease I_{out} according to the calibration by mirroring the calibration current I_{cal}.

In order to connect the electrode or the calibration circuit to the current driver, the switches have to tolerate voltages in the range of $V_{out} \in [-2Vdd+V_h, +2Vdd-V_h]$, where V_h is the headroom of the current mirror. A traditional complimentary switch implemented with I/O transitors cannot be used because it will present >2.5V between its terminals. To overcome this, a HV switch that limits the voltage between transistor terminals to <2.5V has been designed (Fig. 6.14(b)). V_{p1} and V_{n1} bias transistors MP1 and MN1 to withstand the input voltage swing, while V_{p2} and V_{n2} open or close the switch. Transistors MN3 and MP3 are used to reduce the voltage at middle nodes (V_1 and V_2) when leakage current flows through the switch. The HV switch has two modes of operation when it is turned on, depending on the

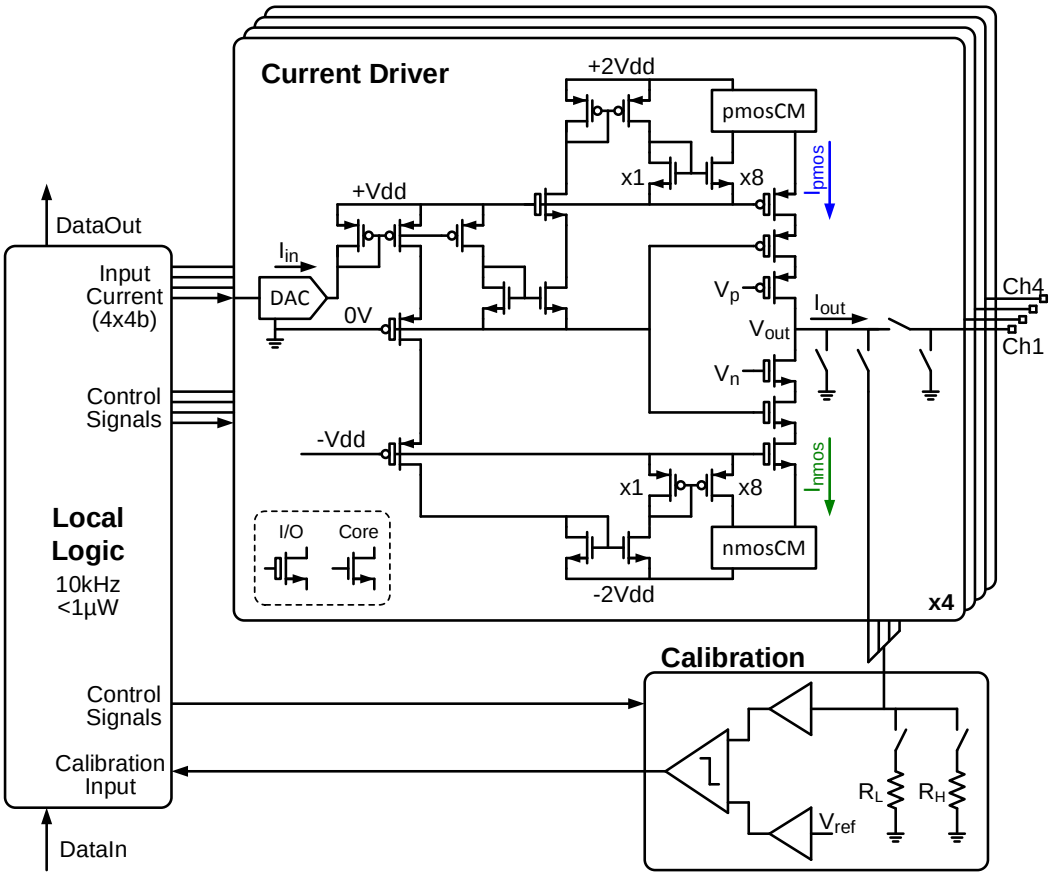


Figure 6.13: Detailed schematic of the self-calibrating 4-channel stimulator (modified from [14]).

required input voltage swing. For a low swing of ±Vdd (i.e. calibration phase, discharge phase), V_{p1} and V_{p2} are set to -Vdd while V_{n1} and V_{n2} are set to +Vdd. For a higher swing (i.e. stimulation phase), V_{p1}, V_{p2}, V_{n1} and V_{n2} are set to 0V to withstand the voltage swing. It is important to mention that in this last mode V_{in} $\neq V_{out}$ for $|V_{out}| < |V_{th}|$; nevertheless, $I_{out}=I_{in}$ for all cases.

Fig. 6.15(a) shows the output stage of the current driver. It is implemented using a stack of 6 I/O transistors. Since the current mirrors are implemented with core transistors, the voltage across them has to be ≤Vdd. To achieve that, the gate voltage of transistors M1 and M6 are set to +Vdd and -Vdd, respectively. To avoid stressing the transistors, the gate voltage of M3 and M4 are dynamically biased according to the stimulation phase, while V_{G2} and V_{G5} are set to 0V. During anodic phase (I_{pmos} is on and V_{out}> 0V), V_{G3} is set to 0V turning M3 on. During cathodic phase (I_{pmos} is off and V_{out}<0V), V_{G3} is set to -Vdd to distribute the almost 5V (4Vdd) across transistors M1, M2, and M3, keeping the voltage across the current mirror ≤Vdd.

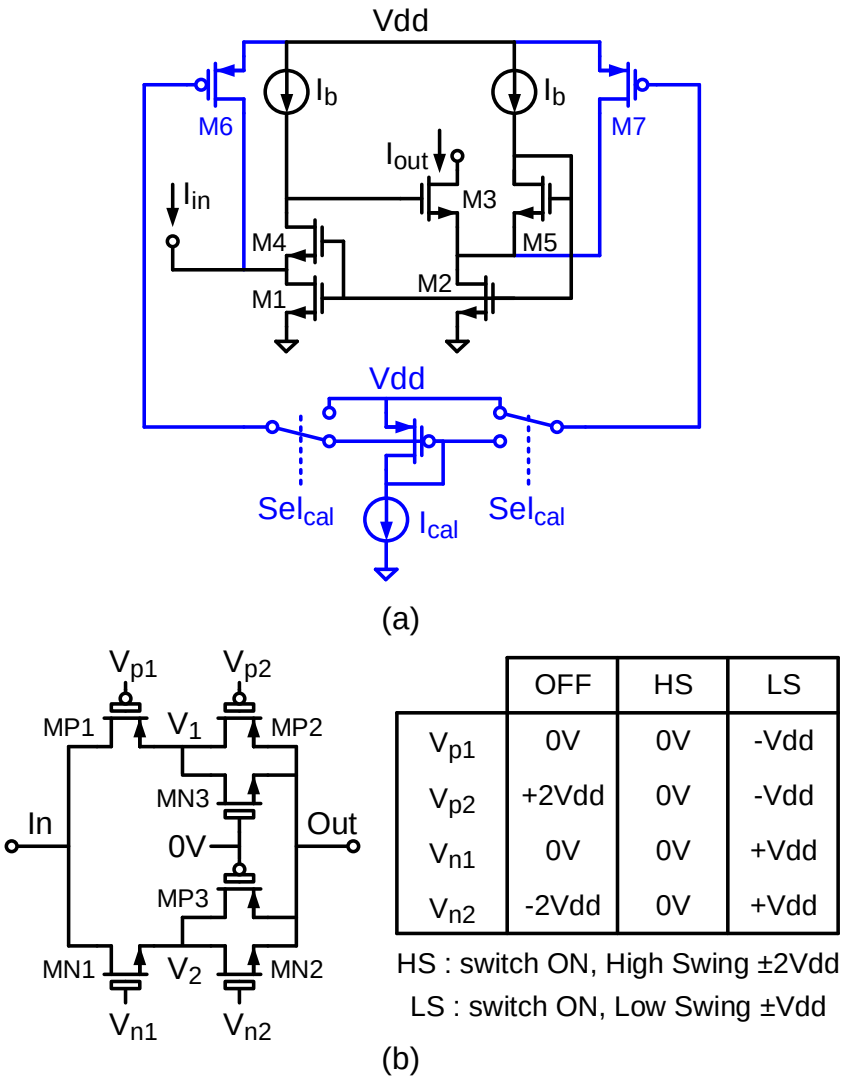


Figure 6.14: Schematics of (a) current mirror (modified from [14]) and (b) high-voltage switch.

A similar analysis can be done for the I_{nmos} current, setting the values for V_{G4} to be +Vdd and 0V during anodic and cathodic phase, respectively.

Between stimulation phases (interphase delay and discharge phase), the current driver is disconnected from the electrode and both stimulation currents (I_{pmos} and I_{nmos}) are turned off. In this state, protection transistors in the output stage of the current driver (M1-M6) accumulate charge due to the body effect. Since these transistors share the same substrate (p-well for nmos and n-well for pmos), each transistor accumulates different amount of charge proportional to its V_{GB}. This is shown in Fig. 6.15(b) for transistors M4-M6, where V_{GB4}, V_{GB5}, and V_{GB6} are

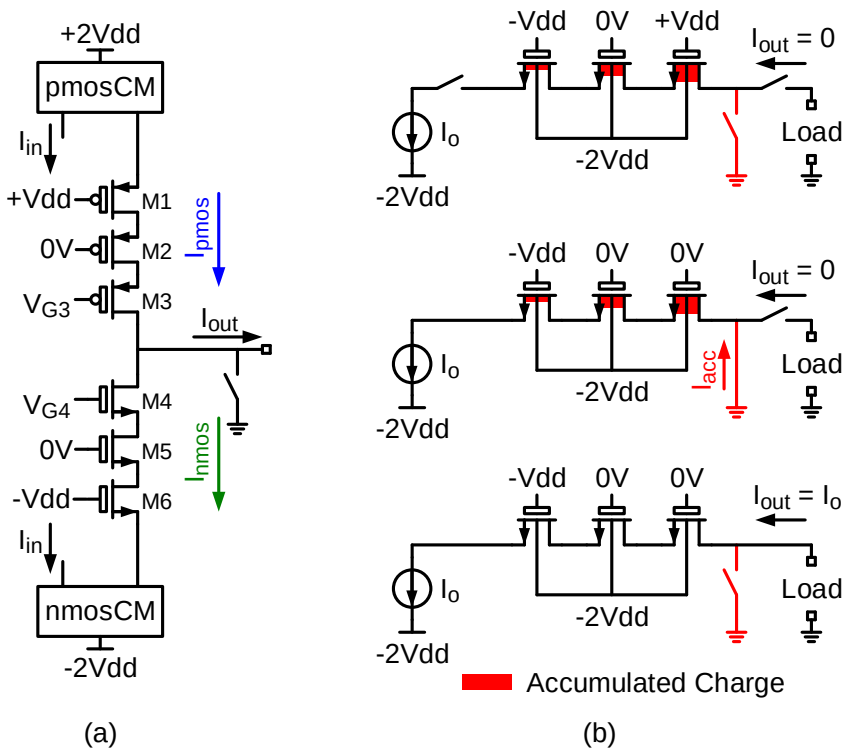


Figure 6.15: (a) Schematic of the output stage of the current driver. V_{G3} and V_{G4} are dynamically biased to avoid stressing the transistors. (b) Model of the protection transistors M4-M6 showing how accumulated charge is removed prior to stimulation.

3Vdd, 2Vdd, and Vdd, respectively. The red bar in the figure represents the accumulated charge. In order to guarantee charge-balanced stimulation based on calibrated stimulation currents, this charge is removed via a switch prior to stimulation.

Calibration

Fig. 6.16 shows the schematic of the calibration circuitry connected to the local logic and a simple model of the current driver. R_H and R_L sense the output current I_{out}. A self-biased pmos common-source amplifier with pmos load, implemented with I/O transistors, is used as a pre-amplifier to provide gain with good linearity and to bias and protect the comparator. A strong-arm sense amplifier is used as the calibration comparator and is implemented using core transistors. In this design, R_H=75kΩ, R_L=15kΩ, V_{ref}= -35mV (step 1), or 0V (step 2), and the calibration DACs have 5-bit resolution with I_{refcal} set to 1μA.

The resolution of the calibration is set by the minimum detectable voltage V_{LSB},

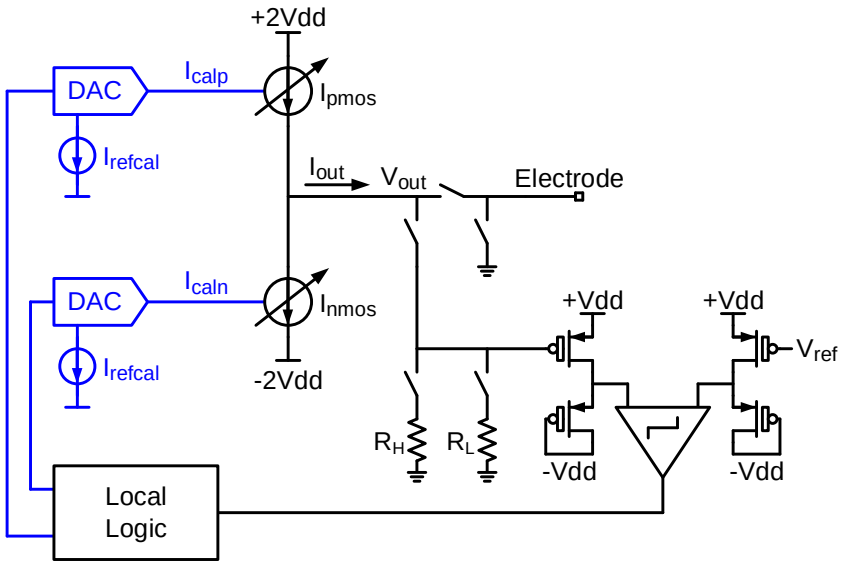


Figure 6.16: Schematic of the calibration circuitry.

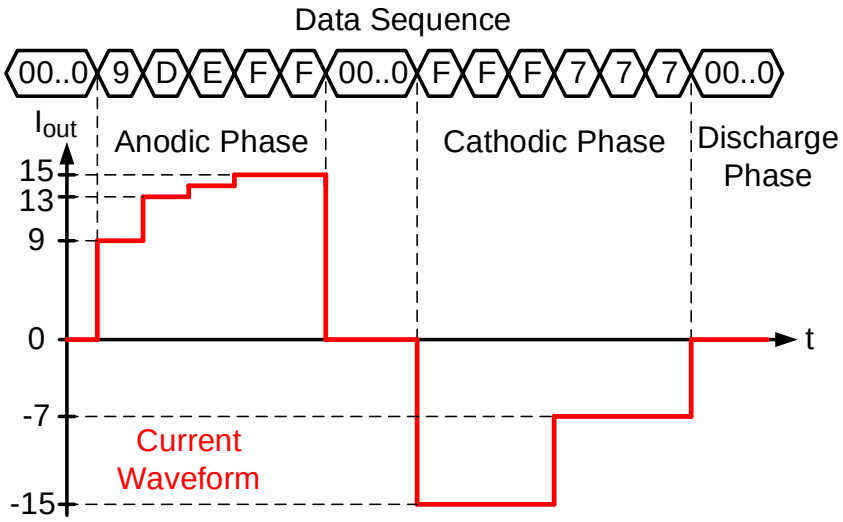


Figure 6.17: Arbitrary waveform generation.

which is defined as:

$$V_{\mathrm{LSB}} = I_{\mathrm{refcal}} \cdot R_{\mathrm{H/L}}\,, \tag{6.6}$$

where $\mathrm{I_{refcal}}$ is the reference current of the calibration DACs and $R_{\mathrm{H/L}}$ is R_H or R_L, depending on the calibration step. To maximize current matching, $\mathrm{V_{LSB}}$ is designed according to the following expression:

$$V_{\mathrm{LSBmin}} > |V_{\mathrm{ref}}|_{\mathrm{max}} + \sum V_{\mathrm{offset}}\,, \tag{6.7}$$

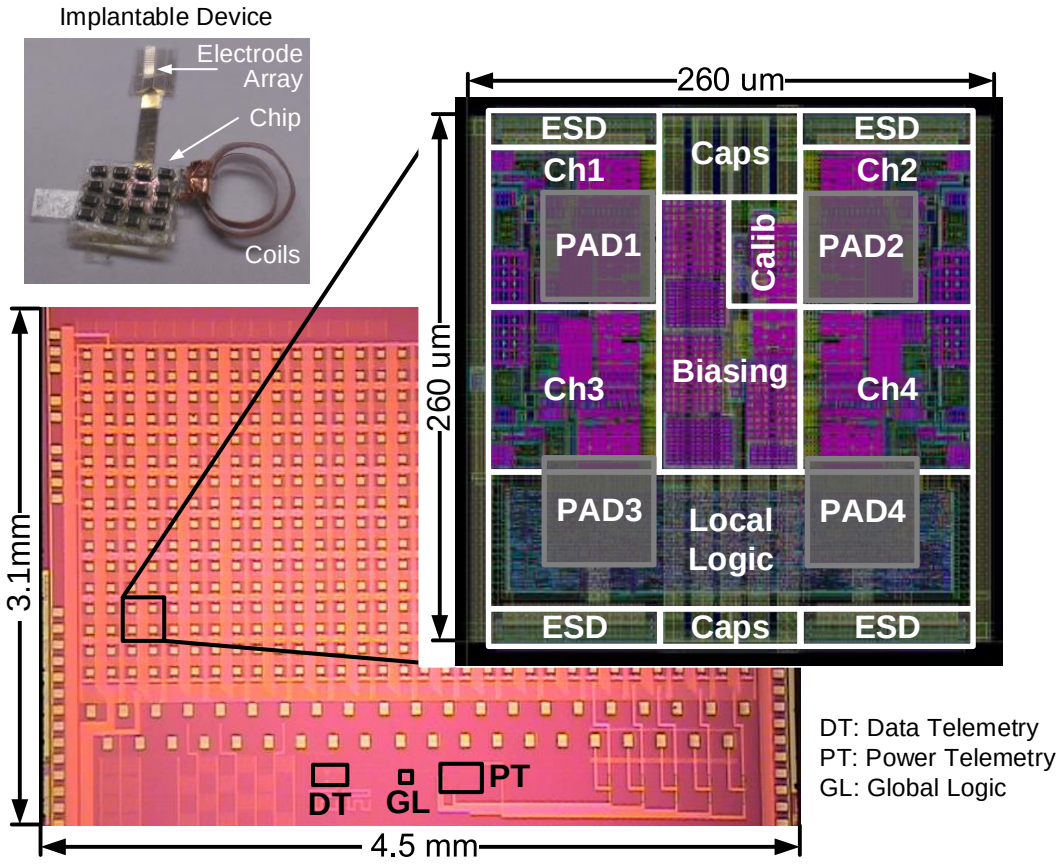


Figure 6.18: Die micrograph of the epiretinal prosthesis, layout of the 4-channel stimulator (4 independent channels sharing local logic and calibration circuitry), and picture of the prototype of the implantable system (modified from [14]).

where

$$\sum V_{\text{offset}} = V_{\text{offset-PreAmps}} + V_{\text{offset-Comparator}} \,. \tag{6.8}$$

Thus, the variation of I_{refcal} becomes the dominant factor. This variation is minimized by increasing the size of the transistors in the bias network and by distributing a current that bias these transistors in strong inversion. The drawback is a slightly higher power consumption.

Local Logic

The local logic controls the calibration and the stimulation, and stores the calibration values. It runs at a low frequency clock of 10kHz to save power and consumes <1uW, which is mostly due to leakage. It implements six finite state machines (FSM). Four identical FSMs control the current drivers and produce independent channels. A separate FSM controls the calibration of each channel, which is performed in a serial

fashion. Finally, an arbiter controls the global operation of the local logic.

Fig. 6.17 shows how the arbitrary output waveform is generated. A data sequence with 4 bits of resolution defines the amplitude of the waveform every 109.2μs. The first non-zero values correspond to the first phase. Then, a group of zeros sets the interphase delay. The next group of non-zero values defines the second phase. Finally, after both phases, the last group of zeros (discharge phase) ends the biphasic stimulation and shorts the electrode to ground. Any remaining charge imbalance is then removed during this phase.

6.5 Measurement Results

The prototype was fabricated in a 65nm LP bulk CMOS process. The die micrograph and stimulator details are presented in Fig. 6.18. The chip occupies an area of 4.5x3.1mm^2, including the extra area needed for parylene integration (0.4mm on the bottom, 0.2mm on the sides and top). The 4-channel stimulator occupies an area of 260x260μm^2 including pads, ESD structures and bypass capacitors, for a pixel size of 0.0169mm^2. A picture of the prototype of the implantable device is also shown in the same figure.

The functionality of the system was verified using a 75μm/300μm inner/outer diameter Pt/Ir flat concentric bipolar electrode in 1X PBS solution as a load while the implant receives power and data wirelessly. An arbitrary waveform generator was used to generate the PSK modulated data, and a signal generator was used to generate the 10MHz power signal. The impedance of the electrode-solution interface was measured and fitted to a simple linear model. It shows a solution resistance R_S of 20kΩ in series with a faraday capacitance C_F of 160nF. This impedance is close to the impedance expected from a 100μm diameter Pt electrode implanted in the retina, which is 100nF in series with 30kΩ [77].

Fig. 6.19 shows measurements of power telemetry operating at 10MHz. The rectified voltage (V_{rec}) and the generated supplies ($\pm$Vdd, $\pm$2Vdd) were measured to be $\approx$1.97V, $\approx \pm$1.3V and $\approx \pm$2.5V, respectively. Fig. 6.20 shows measurements of data telemetry. A 20Mb/s 160MHz PSK data was sent to the system and was correctly demodulated. Fig. 6.20(a) shows 35ms of the measured transmitted signal (TXdata), received signal (RXdata) and demultiplexed signal (Demuxed_data, output of global logic). Fig. 6.20(b) shows details of these signals.

Measurements of arbitrary output waveforms are shown in Fig. 6.21. The measured voltages show the integrated version of the current due to the capacitive effect of

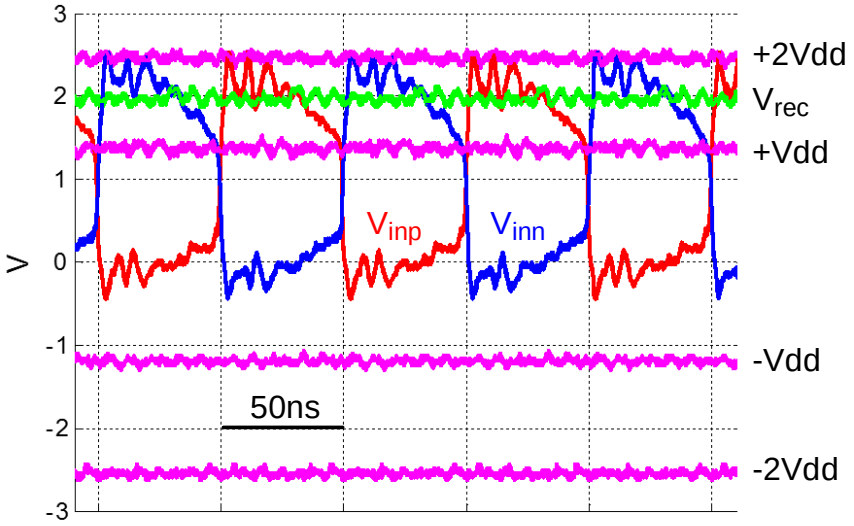


Figure 6.19: Measurement of generated supply voltages.

the electrode-solution interface. First, a biphasic pulse at 60Hz is generated. Then, three different arbitrary waveforms were sent to the implant using the same setup. A piecewise-constant pulse (Waveform A), a pseudo-exponential pulse followed by a constant pulse (Waveform B), and an asymmetric biphasic pulse (Waveform C) were tested. Measurements show that the chip is capable of arbitrary output waveform generation. The charge error after stimulation Q_{error} has been estimated by calculating the integral of the stimulation current over the duration of the pulse. The biphasic pulse, waveform A, B and C have an estimated Q_{error} of 0.7nC, 1.09nC, 0.23nC and 1.2nC, respectively.

Fig. 6.22(a) shows the performance of the calibration technique on a single channel. I_{pmos} and I_{nmos} currents were measured for each value of the input DAC with the calibration turned on and off. The figure shows that both currents are monotonic and that the matching of the currents is improved by a factor of 10 when the calibration is turned on (mismatch decreased from 10μA to 1μA). A statistical measurement over 40 channels from 5 different chips was performed and is shown in Fig. 6.22(b). All 40 channels were correctly calibrated and present a current mismatch with μ=1.12μA and σ=0.53μA. This measurement shows good alignment with the simulation results shown in Fig. 6.12. Differences are mainly caused by the variation of I_{refcal} due to the bias network, which was not considered in the simulation.

The power consumption of the system depends on the stimulation waveform and the number of active channels (activity factor). The system is one of the most power efficient designs, consuming 15mW for a 10% duty cycle, with a 50μA

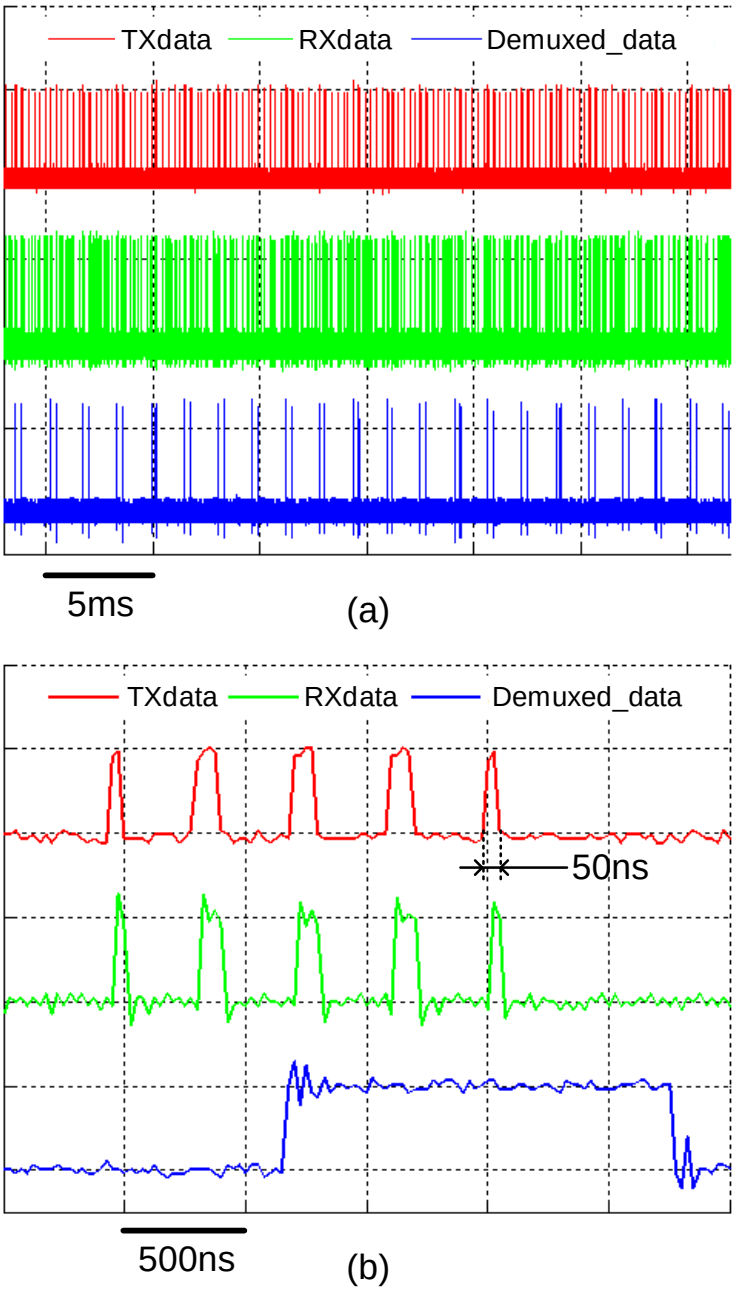


Figure 6.20: (a) Measured data telemetry digital signals at 20Mb/s. (b) Details of the measured signals.

biphasic pulse at 50% activity factor. The output voltage range was also measured after replacing the electrode-solution load by a resistive load. The maximum and minimum output voltage, voltage headroom, and output impedance were measured to be ±2.4V, 0.1V, and greater than 1MΩ, respectively.

Table 6.1 summarizes the performance of the proposed epiretinal prosthesis and

compares it with the state of the art. The self-calibrating 4-channel stimulator is also compared with the state of the art neural stimulators in Table 6.2. The system achieves a reduction of 35% in pixel size. It is important to note that none of the previous work in the literature has reported statistical measurements for current matching.

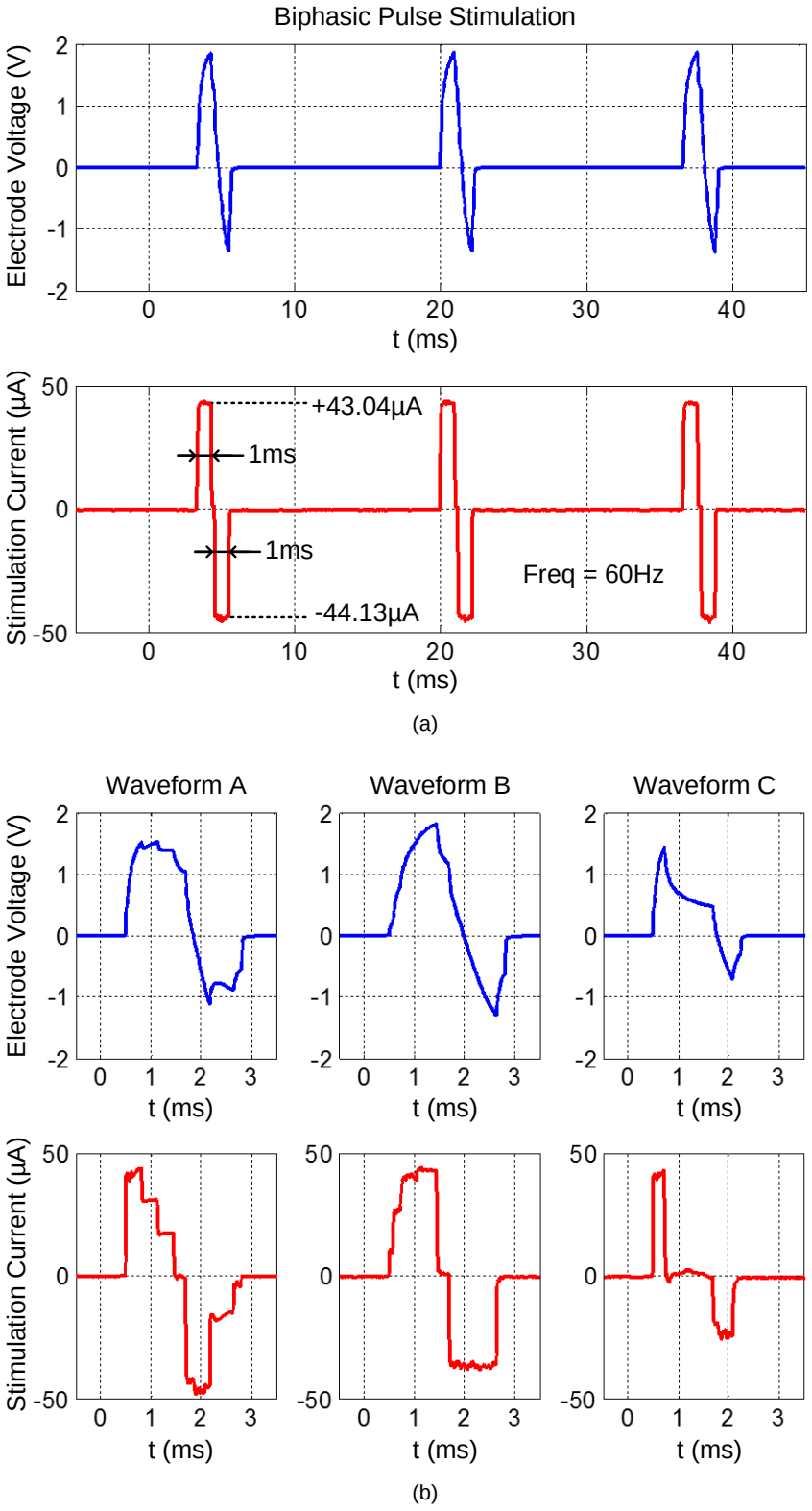


Figure 6.21: Measured arbitrary output waveforms using a Pt/Ir flat concentric bipolar electrode in 1X PBS solution as a load while power and data are delivered wirelessly. (a) Biphasic pulse at 60Hz with a current mismatch of 1.09μA. (b) 3 different arbitrary waveforms.

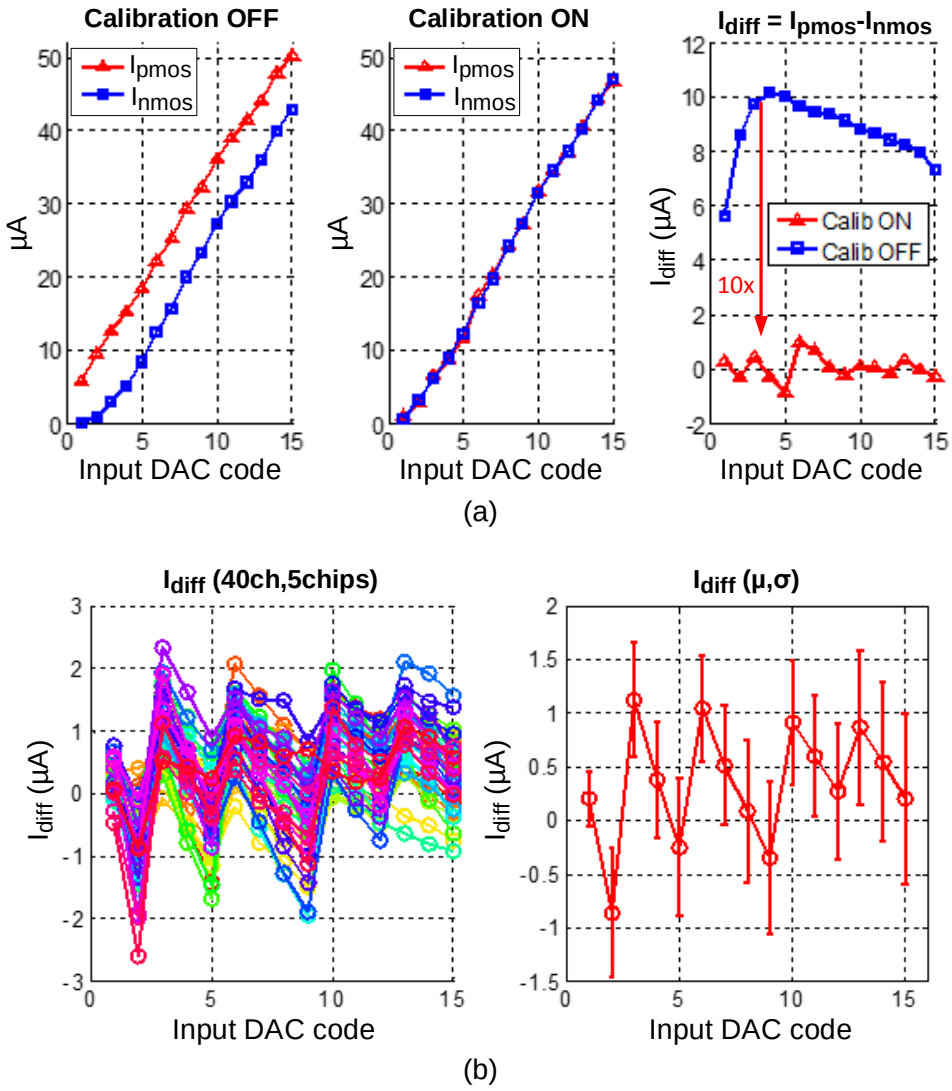


Figure 6.22: (a) Measurements of current matching from a single channel showing a 10x improvement when calibration is turned on. (b) Statistical measurement over 40 channels from 5 different chips showing a current mismatch with μ=1.12μA and σ=0.53μA [14].

	JSSC07 [91]	JSSC10 [112]	ISSCC13 [16]	This Work
Technology	HV 0.35μm	HV 0.18μm	HV 0.18μm	65nm 1.2V/2.5V
Modulation	Photodiode	DPSK @ 22MHz	DPSK	PSK @ 160MHz
Data Rate	968kb/s	2Mb/s	2Mb/s	Up to 20Mbps
Power Carrier	N.A.	2MHz	2MHz	10MHz
On-Chip Supplies (V)	3.3, 11.25, 22.5	±1.8, ±12	±1.8, ±12	±1.3, ±2.5
Number of Channels	232	256	1024	512
I_{out} max (μA)	1000	500	500	50
V_{out} range (V)	>20 (1.25, 21.25)	-10, +10	-10, +10	-2.4, +2.4
Pixel Size (mm^2)	≈0.0718	0.08034	0.026	0.0169
Shared Channels	2*	1	4*	1**
Mismatch	<50μA, charge balancers 5%	<14.5μA <2.9%	N.A.	μ=1.12μA, σ=0.53μA† 2.24%
Load model	10kΩ+100nF	10kΩ+100nF	30kΩ	30kΩ+100nF
Total Area (mm^2)	4.9x4.5	5.3x5.1	5.7x6.6	4.5x3.1††

* no independent channels ** every 4 independent channels share local logic and calibration circuitry

† Statistical measurement (μ: mean, σ: standard deviation)

†† including extra area for placement in parylene (0.4mm on the bottom, 0.2mm on the sides and top)

Table 6.1: Performance Comparison - Epiretinal Prosthesis

	ISCAS07 [113]	TBCAS07 [114]	JSSC10 [112]	EMBC11†† [127]	JSSC12 [108]	ISSCC13 [16]	TBCAS13†† [128]	This Work
Technology	HV 0.5μm	HV 0.7μm	HV 0.18μm	65nm	HV 0.35μm	HV 0.18μm	HV 0.35μm	65nm 1.2V/2.5V
Supplies (V)	±3, ±8	-9, +6	±1.8, ±12	+1 ,+3.3	3.3,10,17,20	±1.8, ±12	3, 12, 15	±1.3, ±2.5
V_{out} range (V)	-7.45, +7.45	-8, 5	-10, +10	-1.5, +1.5	0.3, 19.7	-10, +10	0.8, 14.2	-2.4, +2.4
Pixel Size (mm^2)	0.51	1.44	0.08034	0.04	0.05875	0.026	0.1	0.0169
Shared Channels	1	1	1	1	4*	4*	1	1**
I_{out} max	3.2mA	1mA	500μA	N.A.	1mA	500μA	1mA	50μA
Mismatch	1.8μA 0.05625%	4μA 0.4%	<14.5μA <2.9%	N.A.	charge balancers	N.A.	<1μA <0.3%	μ=1.12μA, σ=0.53μA† 2.24%
Load model	N.A.	3.9kΩ +10nF	10kΩ +100nF	N.A.	10kΩ +100nF	30kΩ	10kΩ +100nF	30kΩ +100nF

* no independent channels ** every 4 independent channels share local logic and calibration circuitry

† Statistical measurement (μ: mean, σ: standard deviation) †† two electrodes per stimulation point

Table 6.2: Performance Comparison - Stimulator IC

Chapter 7

DESIGN CONSIDERATIONS FOR HIGH-DENSITY FULLY INTRAOCULAR EPIRETINAL PROSTHESES

7.1 Introduction

Retinal degenerative diseases such as retinitis pigmentosa (RP) and age-related macular degeneration (AMD) affect primarily the photoreceptor cells (rods and cones) and damage the ability of the retina to sense light, resulting in severe vision loss. However, the majority of inner neurons in the retina remain functional and can be electrically activated [35], [102]. Retinal prostheses (Fig. 7.1) aim to partially restore vision in such patients by bypassing the damaged photoreceptors and directly stimulating the remaining healthy neurons.

Recent work on retinal prostheses has shown significant progress over the past years and has led to the development of commercialized products. One of them is the FDA-approved Argus II retinal prosthesis system which features 60 electrodes and a visual acuity of up to 20/1260 [35]. However, similar to previous work, it uses an extraocular implant with a trans-sclera trans-choroid cable to connect the electrode array to the retina [108], [112]. Not only does having a cable across the eye wall increase the risk of infection and lower the normal eye pressure, but it also leads to unpredictable and difficult to control forces on the electrode array that result in malpositioning of the electrodes relative to the retina.

To avoid the use of such a cable, a fully intraocular implant is desired. In this chapter we discuss design challenges of the electronics and our proposed solutions for future fully intraocular epiretinal implant. Implementation of such device is extremely difficult due to the limitations imposed by the anatomy and biology of the eye as well as desired features such as waveform programmability and a large number of electrodes. In order to have a minimally invasive surgery and guarantee self-healing, the intraocul1ar device needs to be implanted through a small incision of less than 5 mm. We will discuss the possibility of using multiple chips instead of a single chip to reduce the size of the implant while achieving high performance. To enhance the efficiency of the stimulation it is also crucial that all the electrodes be placed uniformly close to the retina without damaging the tissue. In current implants [35], a single surgical tack at one end of the electrode array is used to fix

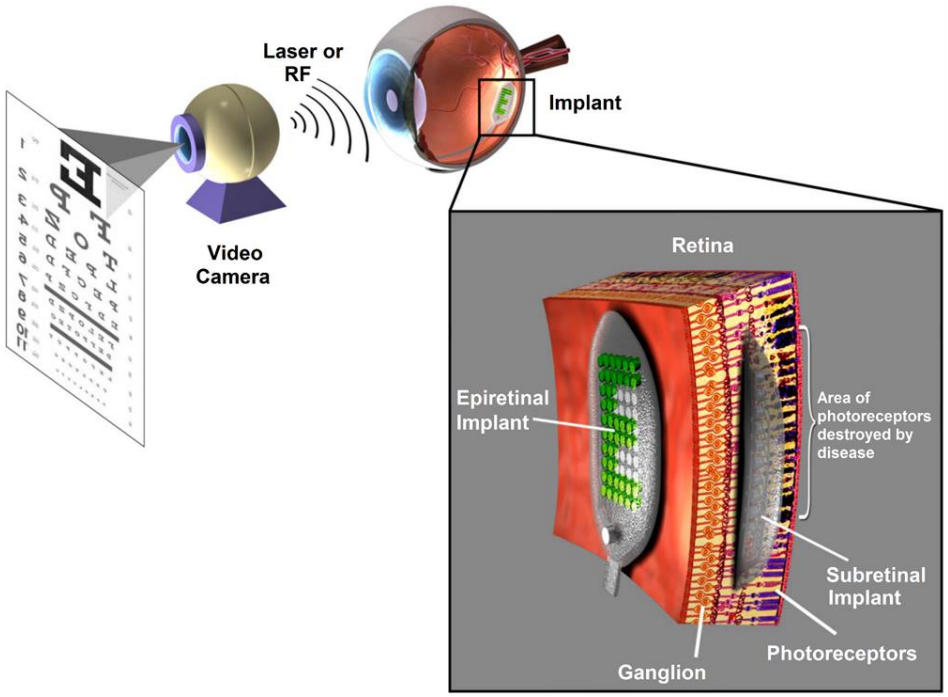


Figure 7.1: Retinal Prosthesis (Image courtesy of annual review of biomed. eng).

the position of the electrodes. However, this approach does not guarantee a uniform placement, and the other end of the array can lift. A new approach that can alleviate this problem and thus reduce the stimulation current and total power consumption of the implant will also be discussed.

7.2 Electrical Stimulation in Epiretinal Prosthesis

In an epiretinal implant, the prosthesis stimulates the retina via an electrode array placed in front of it as shown in Fig. 7.1. The electric charge is then delivered to the tissue in a precisely controlled fashion to initiate a functional response (i.e. action potential) by depolarization of the membrane of retinal neurons. The electrode-retina interface, shown in Fig. 7.2(a)-(b), presents an impedance that depends on the electrode size and the distance from the retinal tissue [77], [108]. This impedance is relatively large due to the small size of the electrodes and properties of retinal tissue.

Of special interest is the perceptual threshold in the retina, since this stimulus threshold together with the electrical properties of the electrode-retina interface will define the output load and voltage compliance of the implant. To ensure stimulation of retinal cells, initial designs targeted current levels up to 1 mA. For those designs, an output compliance of >10V was required, and high-voltage (HV) technologies

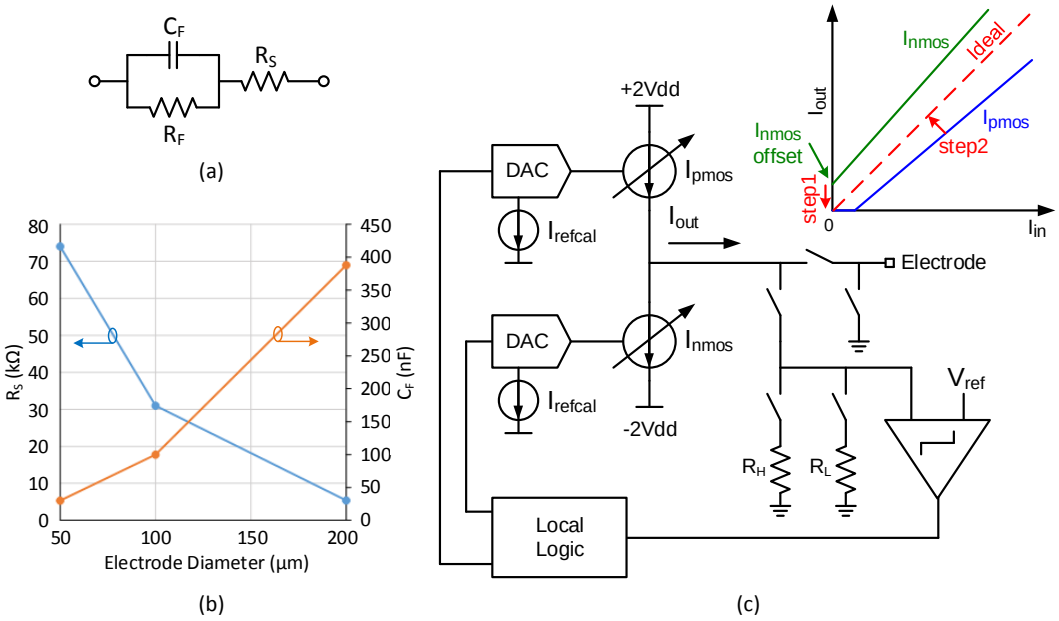


Figure 7.2: (a) Simplified model of the electrode-retina interface, where C_F represents the double-layer capacitance, R_F the Faradaic charge transfer, and R_S the solution impedance. (b) Estimated values for R_S and C_F based on measurements of Pt electrodes implanted in cadeveric porcine eye (from [77]). (c) Model of calibration scheme proposed in [13].

were used at the expense of area and power consumption [108], [112]. Human clinical trials have recently revealed that the stimulus threshold of a single biphasic pulse with 1 ms duration at each phase can be as low as 20 μA for a 260 μm diameter electrode implanted in the macular region [115]. In addition, advances in implant technology promise close placement of the electrode array and retinal tissue, which can further decrease the required current. This creates an opportunity for highly scaled low-voltage (LV) technologies to reduce area and power, and to support hundreds of flexible channels for fully intraocular implants.

It is important to note that recent studies suggest that near term retinal implants must be able to deliver higher currents, but future implants, with advanced electrode array technology, may be able to use lower stimulus and still elicit perception [35]. In section 7.5, we present a promising approach that can pave the way to achieve this important goal.

Waveform Programmability and Biphasic Stimulation

Several studies have shown that more complicated stimulation waveforms such as high-frequency pulse trains, asymmetric biphasic pulses, or non-rectangular shapes

(Gaussian, linear and exponential) present advantages over biphasic pulses [108], [111]. A recent work [111] has proved that the required voltage compliance can potentially be reduced by 10%-15% if a step-down current pulse shape is used. Thus, having a highly flexible stimulation waveform is desired and allows for further studies in stimulation efficiency, color perception, and parallel stimulation [108]. In order to achieve this flexibility, our chip is designed to produce independent arbitrary waveforms with 4 bits of resolution at about 100 μs time-steps.

Another important design consideration in retinal prosthesis is matching the current or charge of biphasic stimulation, since any remaining charge beyond tolerable limits can result in tissue damage and electrode corrosion. Analog techniques to sample correction currents require large area and have to run for every stimulation. In addition, they rely on a constant output current that limits them to biphasic pulses. Instead, as shown in Fig. 7.2(c), we have proposed a digital calibration method to match biphasic currents that reduces area and power. It needs to run only once when the implant is turned on (e.g. daily), and is compatible with arbitrary output waveforms. This technique achieves a current mismatch with μ=1.12 μA and σ=0.53 μA (2.24%).

Number of Channels

Clinical trials have proven to successfully provide visual restoration to blind patients suffering from retinal degeneration [35]. To restore functional visual perception to a degree that will enable reading and face recognition, simulation studies in normally sighted subjects have predicted that hundreds of channels are required [102]. Although the number of channels has increased considerably, most of the previous work have used extraocular implants due to their large size and high power consumption [108], [112]. In order to have a fully intraocular design, the area of the chip, and therefore the area of the stimulator, should be minimized. In our design, control logic and calibration circuitry are shared among several channels to reduce the chip size and power consumption. To further reduce the area of the stimulator, circuit-under-pad technique has been used. This design achieves a pixel size of 0.0169 mm^2, improving the state-of-the-art by 35%.

7.3 Dual-Band Telemetry

Power Telemetry

Fully intraocular implants require the use of coils that can fit inside the eye. Such an intraocular coil is placed in the anterior chamber of the eye after the crystalline

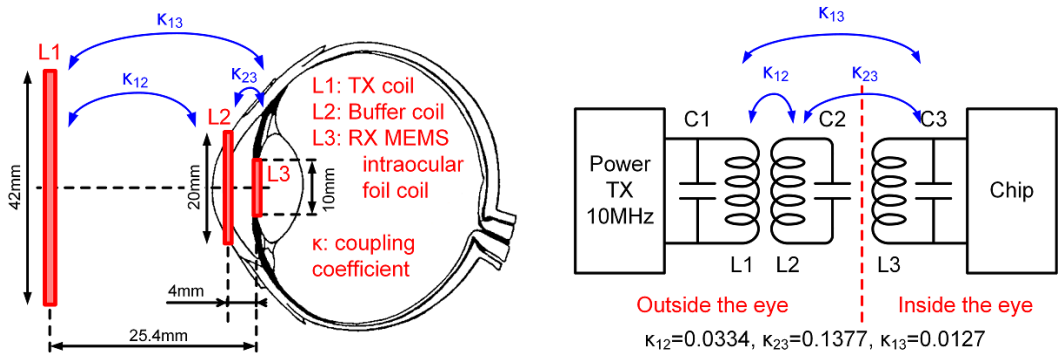


Figure 7.3: Three-coil inductive power transmission [13].

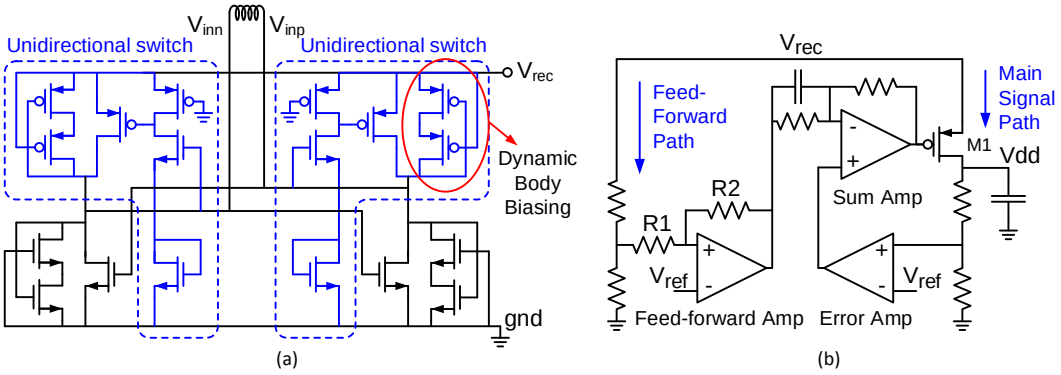


Figure 7.4: (a) Full-wave rectifier and (b) feed-forward ripple cancellation LDO regulator [13].

lens is removed. This imposes hard constraints on its size (<10 mm outer diameter) and weight (<46 mg in saline). Due to these limitations, the efficiency of traditional 2-coil inductive link reduces drastically (≈7% with 1 inch separation). By using a high-efficiency MEMS foil coil and a 3-coil power transmission scheme as shown in Fig. 7.3, our power delivery link achieves 36% of efficiency at 10 MHz [116].

The power management circuitry also needs to have very high efficiency and should be optimized for the frequency at which the coil has its maximum quality factor (Q). In order to reduce the number of off-chip components, an on-chip rectifier is desired to avoid external diodes used in previous work [112]. Our rectifier design utilizes transistor-based diodes and unidirectional switches to prevent reverse conduction loss in the power transistors, improving its efficiency to more than 80% while delivering ≈ 25 mW. A feed-forward ripple cancellation LDO regulator is also used to generate the analog supply, enhancing its PSRR. Both circuits are shown in Fig. 7.4. The power management achieves a total combine efficiency of 65%.

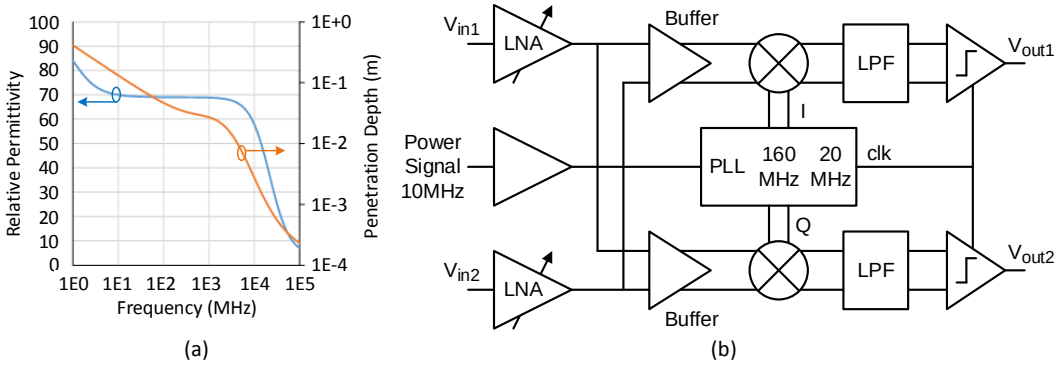


Figure 7.5: (a) Electrical characteristics of the vitreous humor [130]. (b) Schematic of the data telemetry and clock recovery [13].

Data Telemetry

As mentioned in the previous section, hundreds of channels are required to restore functional visual perception, and arbitrary stimulation waveforms present advantages over traditional biphasic pulses. Thus, high-data rate communication is required in order to have independent channels that generate high-resolution waveforms. As an example, for a 1000-channel retinal implant with a resolution of 4-bit at 100 μs time-steps, a data rate of 40 Mb/s is required. Such data rates need a carrier frequency in the order of hundreds of MHz. A PSK modulation scheme and a communication protocol with error-detection capabilities can be used to provide robust data transmission while minimizing the interference from the power telemetry.

Fig. 7.5(a) shows the electrical characteristics of the vitreous humor. It can be seen that the optimal frequency range is located between 100 MHz to 1 GHz because of the approximately constant relative permittivity (i.e., low distortion) and low tissue absorption. Our design implements a PSK demodulator at 160 MHz as shown in Fig. 7.5(b). The on-chip PLL synthesizes the clock from the power signal and removes the need for an external crystal oscillator used in previous designs [112], [129].

7.4 Multiple-Chip Approaches

Recent developments in retinal prosthesis design have increased the number of electrodes achieving more than 1000 channels [129]. As discussed before, the prosthesis should have a number of extra features such as programmable stimulation waveforms, current calibration and charge balancing [13], [108]. Such an increase in capabilities requires the development of specialized system-on-chip designs. In a conventional approach, a single chip manages all major tasks of the implant

(wireless power and data telemetry, power management, digital processing, and electrical stimulation) and gets connected to the electrode array via a dense cable. Even with a highly integrated solution, the size of such system can be around 8×8 mm^2 [108] requiring a large incision, which can pose an implantation challenge in a small and delicate organ like the eye.

Retinal prostheses can be implemented using either HV or LV process. HV technologies allow us to have a high output voltage compliance, but increases the size and power consumption of the chip and limits its functionality. On the other hand, LV technologies reduce the area and power consumption and offer advantages for digital design, data telemetry, and waveform programmability. However, the output current of such systems may be limited depending on the impedance of the electrode-retina interface.

A possible approach involves a hybrid 2-chip solution using HV and LV technologies. In such a scheme, stimulator array and part of power management are designed in the HV process while data telemetry, clocking, synchronization and control logic are designed using a LV process. A possible design strategy to minimize the area and power consumption of the implant for a 2-chip system is as follow:

HV Chip

Simplify the architecture of the stimulator array by extensive use of digitally-assisted analog design and time-multiplexing of electrodes (i.e., only anodic and cathodic current DACs, muxes, level shifters, and registers).

LV Chip

It includes a low-power high-data rate data telemetry, a frequency synthesizer with adjustable phase, and control logic for self-calibration and adaptation of both chips. The size and power of this chip will be extremely small.

Another possible but completely different approach that can alleviate the size problem of implants involves miniaturization through folding and unfolding. Not only folding offers an efficient technological solution for size reduction and minimal surgical cut, but novel origami designs can improve mechanical matching with retinal tissue enhancing the overall performance of the implant.

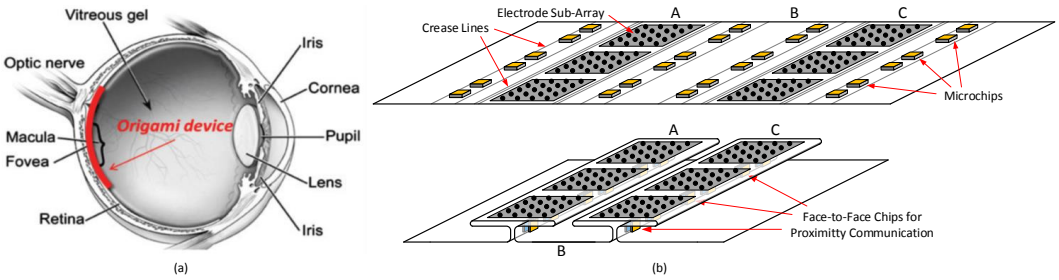


Figure 7.6: Origami retinal prosthesis: (a) position in the eye and (b) Configuration of microchips and electrode sub-arrays before (top) and after (bottom) folding.

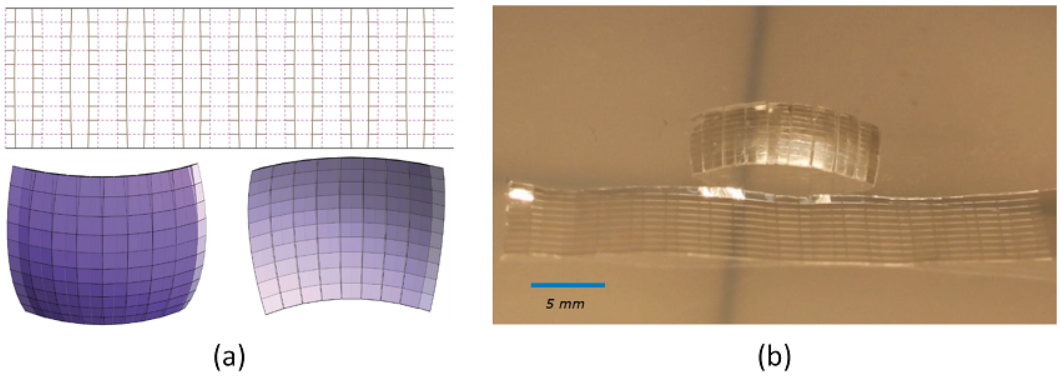


Figure 7.7: (a) Crease pattern (top) and outer and inner views of curved surface (bottom). (b) Fabricated origami structure [131].

7.5 Origami Implants with Distributed Electronics

Our proposed origami design is a 3D integration technique that addresses the size and cost constraints of biomedical implants. Large systems can be split into many smaller chips and connected using 3D integration techniques to be folded compactly for implantation, and then deployed inside the body.

Retinal prostheses can particularly benefit from this approach given their challenging requirements. Instead of a single large chip, many micro-size low-cost chips are distributed over a flexible biocompatible thin film substrate along with the electrodes. Electrodes can be micro-manufactured on the top surface of the film in a sub-array fashion. Each sub-array can be connected to a microchip by parallel micro-manufactured electrical wires on the film. Power and ground will be distributed via such wires, avoiding sharp folds. The origami design will place chips facing each other across the fold and wireless (proximity) chip-to-chip communication can be used to reduce reliance on electrical wires [132]. As shown in Fig. 7.6(a), when inside the eye, the origami implant will take a curved shape to conform to

the shape of the retina improving electrode contact for effective stimulation [131]. The location of the chips and electrodes can be optimized through the design of the origami structure. This high-performance system will achieve the following goals: allow minimally invasive surgery, closely appose electrodes to the retina, place all components within the eye, reduce the interconnect cable density, and enhance the yield and reliability of the system.

Chapter 8

CONCLUSIONS

The impact of Feynman's and Moore's visions has driven not only the development of nanotechnology and electronics, but medicine as well. Over the past decades, remarkable advances toward miniaturized bioelectronic devices have been made. Yet, most of today's biomedical devices present critical limitations regarding size, power consumption, and functionality. Furthermore, several medical conditions could be dramatically improved if even smaller bioelectronic devices were to exist. Although advances in battery and packaging technologies can provide significant progress, the fundamental challenge is the *miniaturization of medical electronics*. The transition to nanometer processes leverages all the benefits of scaling in the digital domain but imposes new constraints for the design of analog circuits, such as lower supply voltages, lower intrinsic gain and higher process variation [29], in applications that require a low-power solution in a small form-factor. In this dissertation, we investigated how novel circuit and system level techniques improve the performance of biomedical devices in two specific areas with a wide range of applications: localization of medical devices inside the body and neural stimulators for epiretinal prosthesis.

In localization of medical devices, our results establish the concept of microscale silicon devices mimicking the physical behavior of nuclear spins to enable their localization inside the body, and demonstrate sub-millimeter resolution of a device smaller than 0.7 mm^3 *in vivo*. The ATOMS technology combines the benefits of RF communication with the simple spatial encoding offered by magnetic field gradients. In addition, it enables external control and adaptation of the spatial resolution by programming of γ_{ATOMS} and G_Z. As a general-purpose platform, ATOMS has the potential to be the enabling technology for *in vivo* monitoring and tracking of biological processes with precise localization. The integration of ATOMS with microscale biological sensing and actuation technologies will enhance the development of a wide range of biomedical applications, from distributed localized monitoring of biologically relevant biomarkers to targeted release of therapeutic agents and tissue imaging for disease diagnosis.

The low-power, on-chip magnetic sensor used in this design provides the required

sensitivity for the implementation of ATOMS in silicon. In addition, it is fully compatible with CMOS technology and requires no extra steps in the fabrication process. Together with a low-power PLL capable of wireless locking and frequency storage provide an effective means to incorporate the physical principles of nuclear magnetic resonance into a microscale silicon chip. Moreover, the ability to integrate RF coils on-chip allows the interaction with RF fields without the need of an external antenna. As a result, the monolithic integration of all magnetic and RF interfacing elements using a commercially available CMOS process provides a desirable and affordable solution that minimizes the number of off-chip components and reduces the complexity of integration. It also enables further developments of ATOMS technology in the same device by taking advantage of the progress of CMOS electronics in communications, signal processing, power management and memory.

In neuroprosthetics, although retinal prostheses have successfully restored vision in patients suffering from advanced stages of retinal degeneration, their traditional implementation presents critical limitations that need to be solved for future generation devices. Fully intraocular implants are emerging as promising solutions to reduce area and power consumption and to avoid the use of a trans-sclera cable. In the second part of this disertation, we presented a high-density 512-channel self-calibrating epiretinal prosthesis system-on-chip fabricated in 65 nm CMOS. The complete system includes high-data rate data telemetry, low-power clock recovery, and high-efficiency power telemetry. The addition of the on-chip rectifier and clock recovery reduces off-chip components such as diodes and crystal oscillator. We also introduced a novel digital calibration technique that matches stimulation currents and is shown to be robust against process variation. The local logic and calibration circuitry are shared among every 4 channels to reduce power and area. The chip features a pixel size of 0.0169 mm^2 resulting in a total area of 4.5×3.1 mm^2. It also supports a master/slave configuration which extends the design to 1024 channels. The system is integrated with MEMS origami coils and off-chip capacitors using a biocompatible flexible parylene substrate. All components fit inside the eye, providing a fully intraocular implant. *In vitro* measurement results were conducted on a Pt/Ir concentric bipolar electrode in PBS solution.

In summary, miniaturization of implantable medical devices will continue to lead the efforts for future medical devices. As smaller and smaller devices are developed, previously inaccessible locations within the body would be reached. These

novel devices will emerge as alternatives to traditional medical approaches, opening up new opportunities to treat and diagnose disease. The devices and techniques presented in this dissertation are examples of this trend. Future advances in the integration of electronics with new materials, MEMS, and biological and chemical sensors and actuators will further enhance this vision.

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