Chapter 3

Strategies for the Fabrication of Silicon Wire Arrays

3.1 Introduction

Although the Cd(Se, Te) nanorod cell of Chapter 2 was a logical initial experiment to test the radial junction concept, the results of that work indicate this is not an ideal material for realizing the benefits of a radial junction, wire array solar cell. One of the key limitations of the cell was its reduced open-circuit voltage, V_{oc}, relative to the planar cell due in part to increased recombination and the fully-depleted nature of the wires. Better control over the doping, materials properties, and surface conditions will be necessary to improve the V_{oc} and produce a wire array that can meet the theoretical expectations.

Silicon seems an ideal material for making these advancements in wire array performance. Being an indirect gap absorber with a long optical absorption depth (100 – 200 μm), low-quality Si is generally minority-carrier collection limited and could potentially benefit from the radial junction architecture. As the dominant semiconductor in the PV industry, there is a wealth of knowledge about how to controllably dope Si and affect its materials properties. Even though reports of Si nanowires have shown the

possibility of one-dimensional growth, the challenge remains to assemble Si wires into a uniform, controllable array that can eventually be doped and contacted to produce a high-efficiency solar cell.

3.2 Silicon Properties

At present, Si is by far the most commonly used semiconductor in the terrestrial photovoltaics industry, accounting for ~ 90% of the PV market.[20, 21] The success of Si is due to several beneficial attributes. It has a band gap energy of 1.12 eV, well matched to the terrestrial solar spectrum.[21, 29] Si is, however, an indirect gap semiconductor and consequently requires > 100 μm of material to absorb most of the incident light. Due to its abundance, this is not an overwhelming design constraint. In fact, Si is the second most common element in the Earth's crust (Figure 3.1).[95] Considering the enormous areas that will need to be covered with photovoltaics to approach 10 TW of carbon-free energy (see Section 1.2), it will be essential that the dominant semiconductor in PV technology be extremely abundant. In contrast, the promising thin film technologies CdTe and $CuInSe_2$ (and its alloys) employ elements that may not be useable at this scale. Indium (In) and selenium (Se) are approximately as common as silver (Ag), while tellurium (Te) is only slightly more common than gold (Au) (Figure 3.1). Although these films can be made inexpensively at their present scale due to the lack of competition for materials like Te, they would likely suffer from scarcity issues upon scaling up to the TW range. Si has a further advantage over competing technologies like CdTe and GaAs in that it is nontoxic. Cd and As are both highly toxic and are known carcinogens.

Covering the land with square miles of these materials with only glass encapsulation to prevent them from leaching into the groundwater has significant potential health risks.

Silicon is also the benefactor of decades of research by the microelectronics industry. A great deal is known about the crystal structure and surface planes, isotropic and anisotropic etch techniques, controllable doping of both n- and p-types, surface passivation methods, effects of impurities, etc.[29, 96, 97] The semiconductor industry prefers Si over materials such as Ge because its oxide can be easily grown and etched and is water-stable. With all of these advantages, Si is likely to play a leading role in the PV industry for years to come.

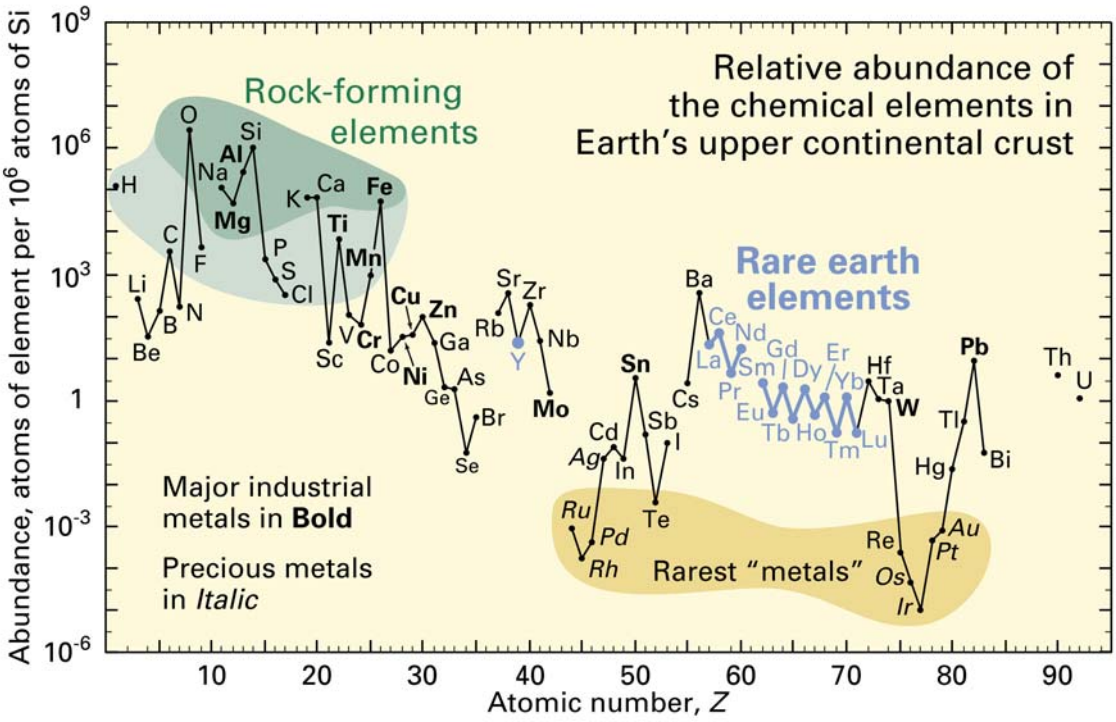

Figure 3.1. Abundance (atom fraction) of the chemical elements in Earth's upper continental crust as a function of atomic number. Many of the elements are classified into (partially overlapping) categories: (1) rock-forming elements (major elements in green field and minor elements in light green field); (2) rare earth elements (lanthanides, La-Lu, and Y; labeled in blue); (3) major industrial metals (global production ≥ 3 x 10^7 kg/year; labeled in bold); (4) precious metals (italic); and (5) the nine rarest "metals" – the six platinum group elements plus Au, Re, and Te (a metalloid). (credit: U.S. Geological Survey).[95]

3.3 Silicon Deposition Methods

3.3.1 Electrodeposition of Silicon

It is possible to fabricate silicon layers via electrodeposition from nonaqueous solvents.[98, 99] The negative electrode potential of Si would result in hydrogen emission in an aqueous medium, so its electrodeposition must be carried out in electrolytes such as

propylene carbonate or tetrahydrofuran under an inert gas. These solutions typically use silicon halide precursors (e.g., $SiCl_4$ or $SiBr_4$) and are nonconducting without the addition of a supporting electrolyte such as tetrabutylammonium chloride or lithium chloride. The electrodeposit can be doped by adding to the electrolyte bath small amounts of PCl_3 or PCl_5 for n-Si or $AlCl_3$ for p-Si.[99] All the materials must be rigorously dried to exclude water.

The electrodeposition of Si could be combined with porous anodic aluminum oxide (AAO) templates to make nanowire arrays in a nearly identical process to that described for Cd(Se, Te) in Chapter 2. Si could even be sputtered from n- or p-type targets to create a shunt-preventing layer at the base of the wires. However, to date, electrodeposited Si has had a microscopic honeycombed structure that has led to significant oxidation throughout the material. The semiconductor properties of these deposits have been quite poor and fundamental research on improving the electrodeposition process is still needed.

3.3.2 Chemical Vapor Deposition of Silicon

Silicon can also be deposited by the decomposition of gas phase precursors. Among vapor-based methods, chemical vapor deposition (CVD) through the vapor-liquid-solid (VLS) process is the most successful for producing Si wires.[42, 100] The many benefits of the VLS mechanism include its tendency to form single-crystal wires,[101] the high growth rates that are achievable (up to several μm/s),[102] the availability of in situ doping

techniques,[103] and the ability to influence the wire diameter by controlling the catalyst size.[104]

In the VLS mechanism (Figure 3.2), a solid impurity metal acts as a preferred site for the deposition of Si from a gas precursor such as SiH_4 or $SiCl_4$, allowing for a very selective growth location as well as accelerated growth rates relative to uncatalyzed deposition under similar conditions.[100] The metal alloys with the Si, forming a liquid eutectic mixture at the reaction temperature (400 – 1100 ºC). As the metal droplet continues to uptake Si from the vapor phase, the concentration increases until the droplet is supersaturated with Si. Crystalline Si then precipitates from the alloy droplet, aided by the low activation energy for nucleation at the crystal-melt interface.[105] The metal droplet rises with the Si precipitate, resulting in the one-dimensional growth of Si wires. Under most conditions, the wire grows in the <111> crystal direction with the side facets usually having a {211} orientation.[42] If the catalyst metal has a low solubility in solid Si, the wire will not taper appreciably and will have a diameter approximately equal to the metal droplet diameter. Although Au has predominantly been used for VLS Si wire growth, several metals including Cu, Ni, Pt, and others are predicted to meet the necessary catalyst criteria.[105]

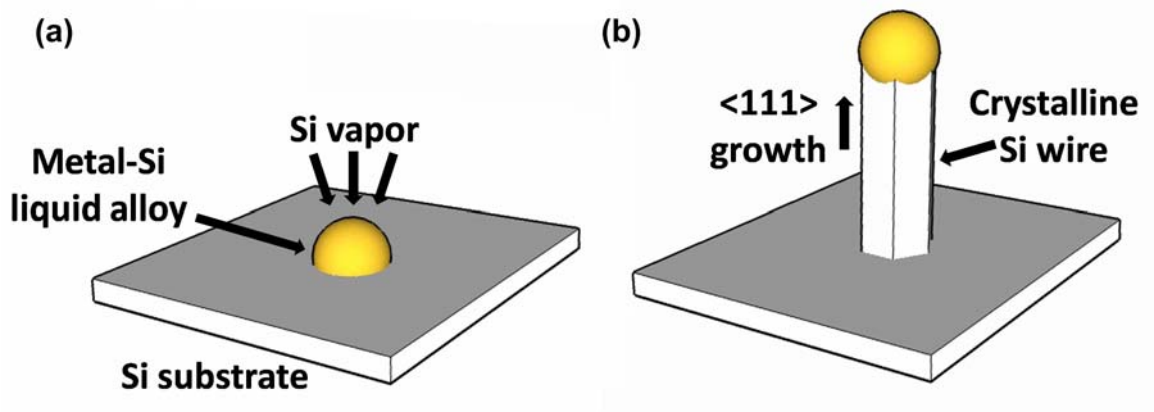

Figure 3.2. Schematic of the vapor-liquid-solid (VLS) mechanism of Si wire growth. **(a)** A solid metal catalyst forms a liquid eutectic alloy upon uptake of Si from the vapor phase. **(b)** When the metal becomes supersaturated, Si crystallizes out (typically in the <111> direction) and forms a one-dimensional wire with the catalyst droplet at the tip.

3.4 VLS-Grown Si Nanowires in Porous Alumina Templates

3.4.1 Benefits of a Template with the VLS Method

Despite the many advantages of the VLS technique for Si wire growth, it has a few key drawbacks. The growth of a high-quality Si wire array typically relies on a single-crystal Si wafer to produce aligned, crystalline wires epitaxially attached to the substrate.[106-110] The use of an expensive wafer detracts from the mission of the radial junction solar cell to be a low-cost photovoltaic. Also, it can be difficult to control the pattern and diameter uniformity of the wires due to the tendency of the catalyst metal to migrate on the substrate surface at reaction temperatures.

The use of AAO templates to guide and control the VLS process addresses both of these drawbacks. The pores should be able to confine both the catalyst metal and the Si deposition so that aligned wires of uniform dimensions are fabricated. Redwing et al.

have demonstrated that this can be done by electrodepositing metal into the pores and then exposing the template to SiH_4.[111-113] While we are not aware of any AAO-fabricated Si nanowires left as a freestanding array after the dissolution of the template, it should be possible to achieve by the deposition of a low-cost substrate onto one side of the membrane. Such a scheme would enable the fabrication of crystalline, aligned Si wires of uniform dimensions assembled into an array without the need for an expensive substrate. We report herein freestanding Si wire arrays grown with an AAO template-assisted VLS mechanism[114] and discuss the shortcomings of this approach.

3.4.2 Fabrication of Si Wire Arrays with AAO Templates

Nanowire arrays were fabricated using commercially available, 60 μm thick, 200 nm pore diameter, AAO membranes (Whatman Scientific) as templates. A 100 nm thick layer of Au was thermally evaporated onto one side of the AAO to cover the bottoms of the pores with catalyst and to make that side of the template conductive. The other side of the AAO was then covered in a layer of mounting wax to prevent deposition of metal onto the bottoms of the pores in subsequent processing steps. The template was then made into a working electrode by attaching a Cu wire and applying conductive Ag paint around the edge of the membrane. The wire was encased in a glass tube, and the wire contact area was sealed with epoxy.

To provide mechanical stability and support for the nanowire array after the removal of the template, > 10 μm of Ni metal was electrodeposited onto the back of the Au. The Ni substrate was galvanostatically electrodeposited at room temperature, under stirring,

from an aqueous solution of 0.8 M nickel (II) sulfamate ($Ni(SO_3NH_2)_2$) and 0.6 M boric acid (H_3BO_3). In this process, a current density of 25 mA cm^{-2} was maintained for 1 hr between the working electrode and a Pt gauze counter electrode. The mounting wax was then thoroughly removed by several washes in acetone. The AAO template was mechanically removed from the electrode assembly.

To grow Si wires, the AAO with a Ni substrate and Au at the bottom of the pores was inserted into a reactor at ~ 500 ºC and exposed to 5% SiH_4 in Ar at a flow rate of 100 sccm and a total pressure of 1 Torr. The reaction was allowed to proceed for 1 hr or more before removing the sample and allowing it to cool under vacuum. After growth of the nanowires, the AAO template was removed by submersing the array in 1 M NaOH(aq) for 20 min.

Figure 3.3 shows SEM images of a typical Si nanowire array that resulted from the templated VLS growth method. Si nanowires of 200 nm diameter, conforming to the AAO pore size, were regularly fabricated as freestanding arrays on the electrodeposited Ni substrate. Si wires up to ~ 5 μm long were produced after a grow time of 1 hr.

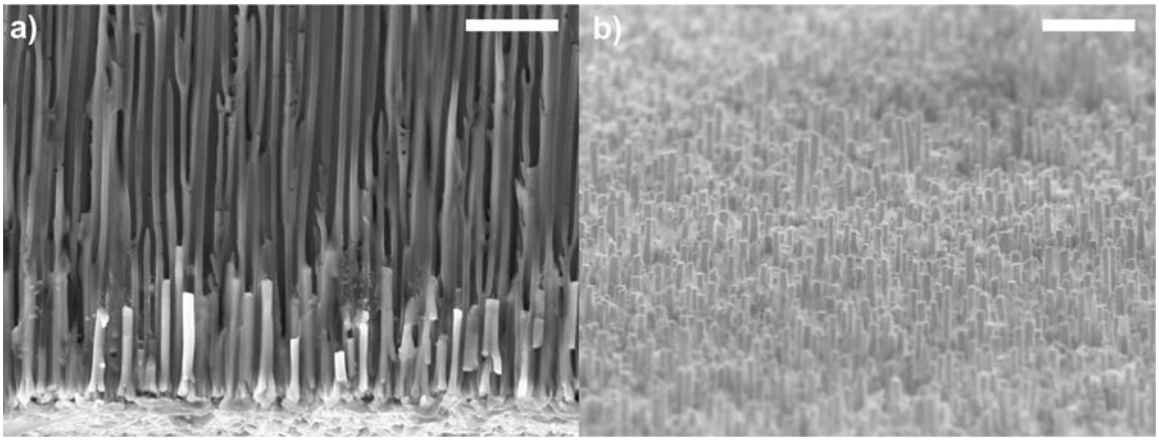

Figure 3.3. Si nanowire arrays grown with AAO templates. (a) Cross-sectional view SEM image of an AAO template with Si wires at the bottom of the pores. **(b)** Tilted-view SEM image of a freestanding Si nanowire array on a Ni substrate after the removal of the template. The scale bar for **(a,b)** is 2 μm.

3.4.3 Shortcomings of Templated VLS Growth

The gradual conformal deposition of Si onto the porous alumina template eventually accumulated until it blocked the pores on the top surface of the membrane (Figure 3.4). This conformal Si deposit made the selective chemical removal of the AAO difficult and limited the length of nanowires attainable. One approach to mitigate the conformal deposition problem would be to switch the carrier gas from Ar to H_2. By Le Chatlier's principle, the presence of excess H_2 would shift the equilibrium of the silane decomposition reaction so that less conformal Si would deposit on the template. This should promote the selectivity of the VLS-catalyzed Si deposition at the bottom of the pores. This approach was not pursued, however, as research began to focus on other Si wire growth strategies.

The difference in thermal expansion coefficients between Ni and alumina (α_{Ni} = 16.8, α_{Al2O3} = 8.8 mm/(mm ºC) x 10^6 at ~ 500 ºC)[115] presented another difficulty with this Si

nanowire array fabrication route. It was commonly observed that thermal stresses induced by heating and cooling the Ni-backed AAO template warped the sample and often resulted in pieces of the brittle alumina chipping away from the metal substrate, which could be a serious problem in any attempt to scale up this fabrication procedure. An alternative route was pursued with some success, wherein a conductive Ag layer was deposited on one side of the AAO followed by selective electrodeposition of Au catalyst at the bottom of the pores. The Ag layer was chemically removed in 8 M HNO_3, and then a thin (< 10 μm) layer of either p- or n-Si was sputtered over the bottom of the AAO to serve as a substrate. This type of sample was put in the reactor to grow Si wires, and as long as the heating and cooling steps were conducted slowly, minimal warping and no chipping were observed. After wire growth, an ohmic metal back contact followed by a thicker metal support layer was applied to the sputtered Si and then the template was removed. Technical difficulties with the silane reactor halted progress on this fabrication scheme, however, and it was not pursued further because an alternative VLS growth approach showed more promise for producing high-quality Si wire arrays.

Although it was demonstrated that vertically aligned, densely packed Si nanowire arrays of highly uniform diameters could be fabricated without expensive substrates via this technique, the limitations of the AAO-templated VLS growth of Si wires make this method less than ideal for producing parallelized radial junction Si solar cells. In addition to conformal Si deposition and AAO warping issues, templating the VLS Si growth is known to introduce polycrystallinity to the wires that is likely to result in lower quality electronic properties than if they were grown without confinement.[35, 116] Radial junction modeling[33] along with the experimental results on Cd(Se, Te) nanowire array

photoelectrodes (see Chapter 2) indicate that very high surface area electrodes will have a significantly reduced open-circuit voltage. At 200 nm, the AAO templates used in this work are already near the upper limit achievable for pore diameter size.[44] It will therefore be difficult to transition to larger diameter, and hence lower surface area, wire arrays by this technique. While the AAO template method can produce Si nanowire arrays that may be useful in other applications that require high surface areas, it is not the best route to fabricate Si wire arrays that are optimized for solar energy conversion.

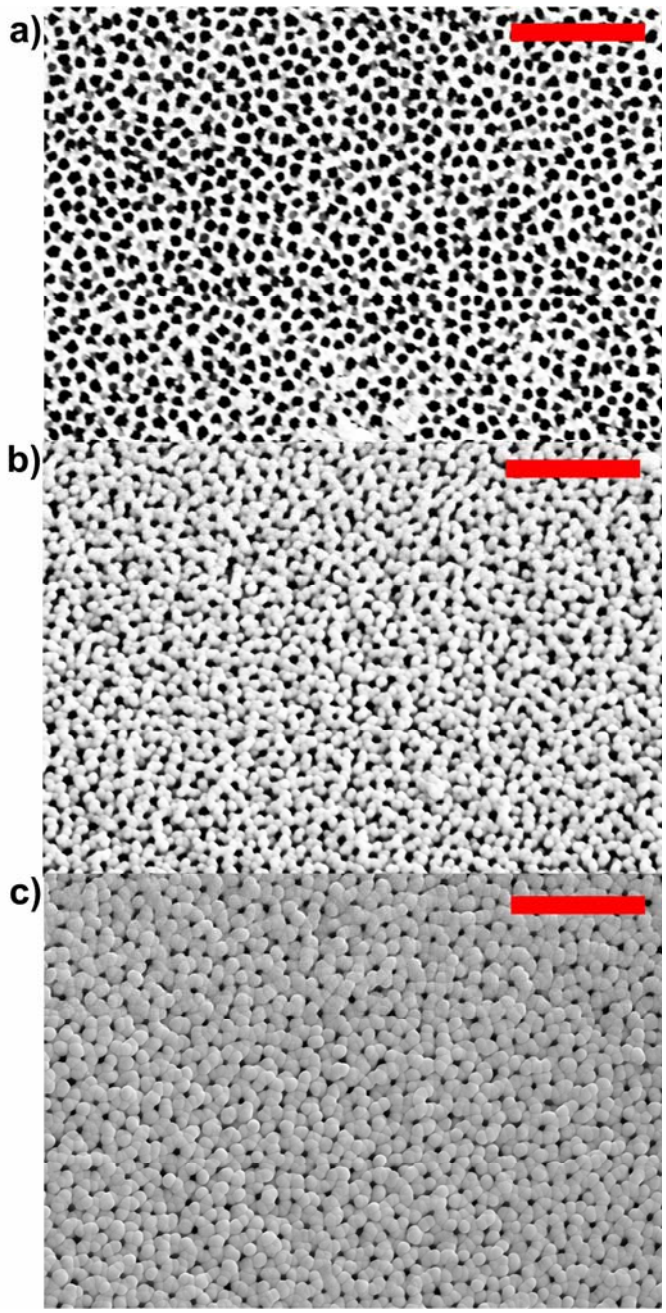

Figure 3.4. AAO template surface after SiH_4 chemical vapor deposition. Top-down view SEM images of an AAO template used to grow Si nanowires after **(a)** < 1 hr, **(b)** ~ 2 hr, and **(c)** ~ 3 hr in 5% SiH_4 in Ar at a flow rate of 100 sccm, a total pressure of 1 Torr, and a growth temperature of ~ 500 ºC . The scale bar for **(a-c)** is 2 μm.

3.5 VLS-Grown Si Microwire Arrays on Si(111) Substrates

3.5.1 Growth of Optimal Si Wire Array Geometry

The best approach for producing Si wire arrays that can be optimized for solar energy conversion is one that allows for the growth of wires with dimensions that are tunable within a wide range and also highly uniform from wire to wire. Control over the dimensions and spacing of the wires within an array is necessary to be able to individually change parameters such as radius, length, or pitch and interpret the effect that each variable has on the experimental results. As previously mentioned, theoretical modeling on radial junction Si solar cells indicates that larger diameter wires will result in a higher V_{oc} and efficiency as long as the minority-carrier collection length is at least equal to the wire radius.[33, 34] Unlike AAO-templated wires, VLS-grown Si wires on a Si wafer substrate are not prevented from having diameters > 200 nm. Therefore, if catalyst placement and growth conditions can be controlled such that uniform wire arrays can be produced, guiding VLS growth with a high-quality Si substrate may be the best way to study the optimal Si wire array geometry.

3.5.2 Growth from SiH_4

Initial attempts to grow Si wire arrays on single-crystal wafers employed a SiH_4 gas precursor. A Si(111) wafer was etched in 10% aq. HF for > 10 s immediately prior to the thermal evaporation of ~ 10 nm of Au onto the surface. The wafer was then put into a silane CVD reactor at ~ 500 ºC and exposed to 5% SiH_4 in Ar at a flow rate of 100 sccm

and a total pressure of 1 Torr to grow Si wires. Upon heating the wafer, the thin Au film broke up and agglomerated into larger pools of catalyst metal (Figure 3.5a). The resulting Si wires were arranged randomly and had widely varying diameters, mostly 100 – 2000 nm (Figure 3.5b). Even after 3 hr of growth under these reaction conditions, wire lengths were generally < 20 μm. Although straight, vertically oriented wires were sometimes achieved, wires were commonly kinked and at angles to the substrate (Figure 3.5b). Kinking occurs when the wire spontaneously switches from its initial [111] direction to one of the other equivalent {111} directions. It is known to occur in VLS growth at lower temperatures and SiH_4 partial pressures.[117] The silane reactor used in this work was not capable of reaching temperatures significantly > 500 ºC, limiting the ability to prevent kinking in this system. Greater control over catalyst size and placement, faster growth rates, and the more consistent growth of straight, aligned wires is needed to produce an ideal Si wire array.

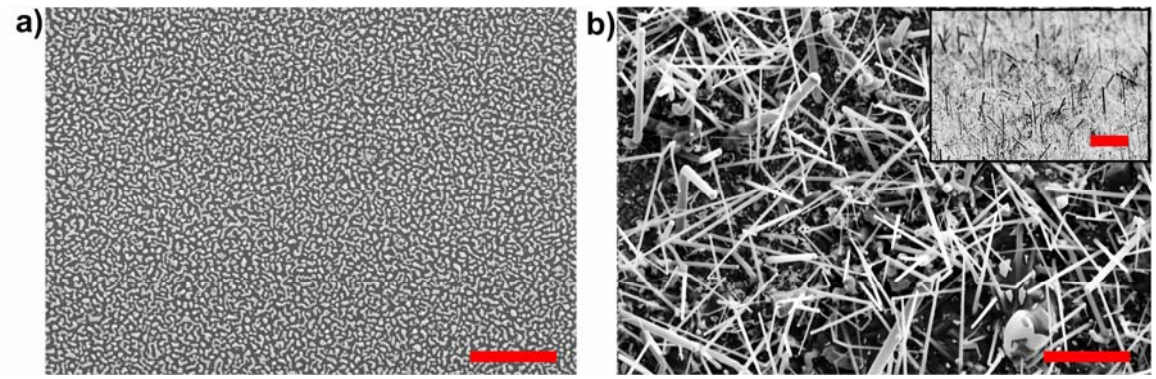

Figure 3.5. VLS Si wire growth from SiH_4 without patterning the catalyst. Top-down view SEM images of **(a)** a Si(111) wafer with ~ 10 nm of Au thermally evaporated on the surface and then annealed under vacuum at ~ 500 ºC for 5 min and **(b)** the same sample after exposure to a 100 sccm flow of 5% SiH_4 in Ar at 1 Torr total pressure and ~ 500 ºC for 3 hr. Scale bar for **(a,b)** is 2 μm. The inset shows a tilted-view SEM image of the Si wires shown in **(b)**. Scale bar for the inset is 10 μm.

3.5.3 Growth from $SiCl_4$

To pursue a better fabrication route for Si wire arrays, a reactor capable of employing $SiCl_4$ as the gas precursor at temperatures above 1000 ºC was built. $SiCl_4$ has several notable advantages over SiH_4 as the VLS gas precursor. At ~ 1000 ºC, wires can be grown at rates > 3 μm min^{-1} with no kinking, allowing the production of wires longer than the optical thickness of Si in < 1 hr. The $SiCl_4$ VLS reaction can be conducted at atmospheric pressure, decreasing the expense of the process by eliminating the need for vacuum technology. In the presence of H_2, HCl is formed in situ that can etch the native oxide from the Si growth substrate, promoting the epitaxial growth of Si wires normal to a [111] surface so that essentially all the wires are in vertical alignment.[106] Finally, as noted earlier (see Section 1.3), $SiCl_4$ is a byproduct of the current process used to produce solar grade Si.[25] In fact $SiCl_4$ is inexpensive enough that some polysilicon producers

have dumped it as a waste product.[118] These factors make $SiCl_4$ VLS growth appealing as a method to produce an ideal Si wire array architecture in a potentially cost-effective, scalable process.

To precisely form the desired wire array geometry, a method is still required to pattern the catalyst metal and control its location and size during Si wire growth. Our research group solved this problem by utilizing conventional photolithography on the Si substrate surface in combination with thermal evaporation to deposit patterns of catalyst metal islands.[119] At reaction temperatures, however, the catalyst pattern fidelity was lost due to metal migration and agglomeration on the Si(111) surface, leading to a low fidelity wire array. This issue was solved by using a thermal oxide buffer layer to confine the VLS catalyst to the patterned areas on the substrate surface. To do this, a buffered HF etch was performed before metal evaporation to remove the oxide from the exposed portion of the photoresist pattern so that the catalyst was deposited on Si but surrounded by SiO_2.

Specifically, a Si(111) wafer with 300 nm of a thermally grown silicon oxide was photolithographically patterned with S1813 photoresist (Microchem), followed by immersion for 4 min in buffered HF(aq) (Transene, Inc., 9% HF, 32% NH_4F) to remove the oxide in the holes formed by exposure of the photoresist. 300 nm of Au was then thermally evaporated onto the wafer, followed by lift-off of the remaining resist. Lithographic patterning resulted in a square array of 3 μm diameter Au islands, having a center-to-center pitch of 7 μm, separated by the SiO_2 layer (Figure 3.6a). The wafers were then annealed in a tube furnace at 1000 ^oC for 20 min under 1 atm of H_2 at a flow rate of 500 sccm, and then wire growth proceeded during a subsequent 30 min step by

addition of a flow of 10 sccm of $SiCl_4$ while maintaining the same pressure, temperature, and H_2 flow rate. This process produced highly uniform, vertically aligned, crystalline Si wires of ~ 1.5 μm diameter over large areas (Figures 3.6b and 3.6c). Uniform arrays > 1 cm^2 were produced, with the area limited only by the size of the reactor tube diameter. Equivalent wire array structures were grown under the same conditions using Cu or Ni as the VLS catalyst.

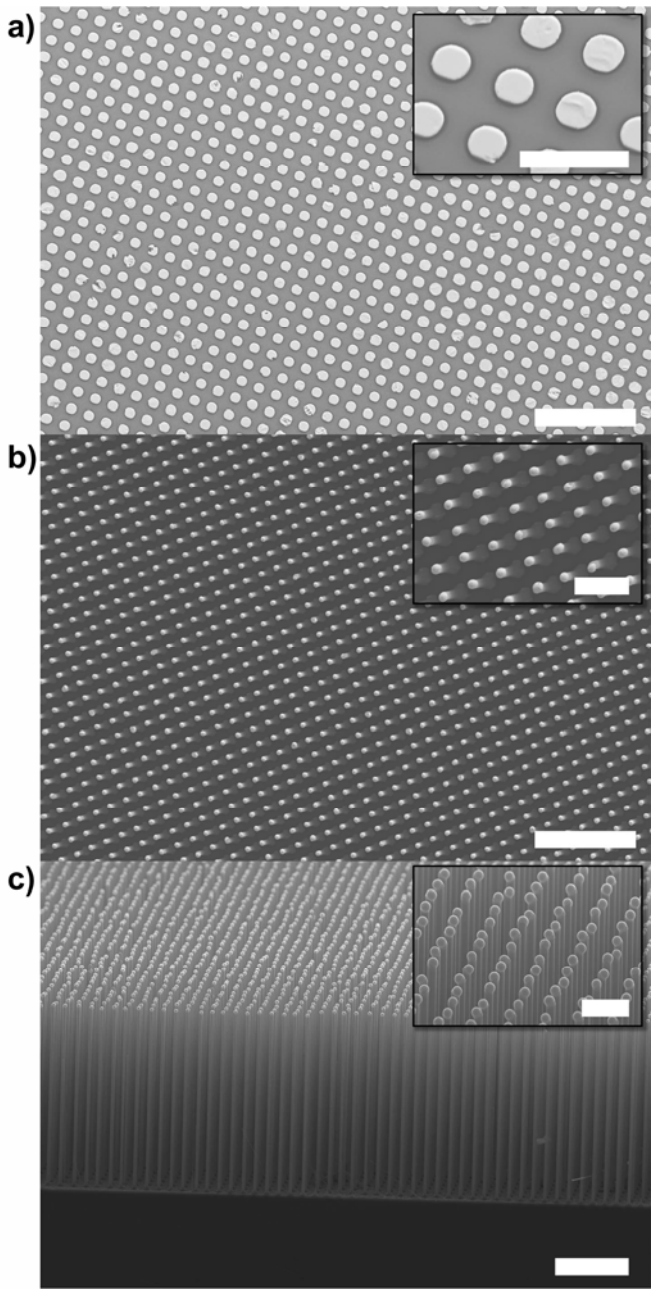

Figure 3.6. VLS Si wire growth from $SiCl_4$ with photolithographically defined catalyst. (a) Top-down view SEM image of a Si(111) wafer photolithographically patterned with 3 μm diameter Au catalyst islands in a square arrangement of 7 μm pitch. **(b)** Top-down view and **(c)** tilted-view SEM images of Si wires grown from 500:10 sccm H_2:$SiCl_4$ at 1 atm and 1000 ºC for 30 min. Scale bar is 40 μm for **(a-c)**, and 10 μm for each inset.

3.6 Effect of Substrate Surface Orientation on Wire Growth

While the primary role of the oxide buffer layer was to constrain the catalyst metal to its patterned location, there was also the possibility that the oxide side walls were helping to guide the nucleation and initial wire formation to grow normally to the substrate surface. To test this, a 300 nm thermal oxide was grown on the surface of Si substrates of (111), (110), and (100) orientation, patterned with 300 nm Au catalyst, and exposed to $SiCl_4$ under the reaction conditions described above (~ 20 min of growth time). Figure 3.7 shows cross-sectional SEM images of the resulting Si wire arrays. As expected, the wires on the Si(111) wafer grew normal to the substrate. However, the wires grew at a ~ 35 º angle to the Si(110) surface and a ~ 55 º angle to the Si(100) surface, indicating wire growth in the [111] direction despite the presence of the thermal oxide buffer layer. Therefore, a single-crystal Si(111) surface appears to be necessary in this process to fabricate vertically aligned epitaxial wire growth.

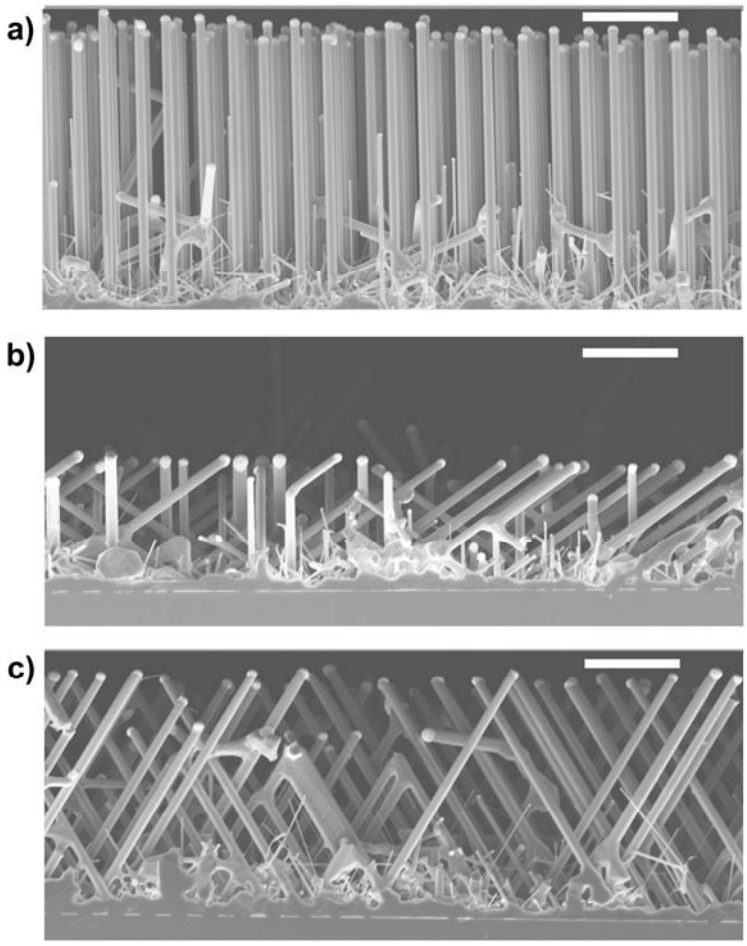

Figure 3.7. VLS Si wire growth from $SiCl_4$ on Si substrates of different crystal orientations. Cross-sectional SEM images of Si wire arrays produced after ~ 20 min of growth on a Si surface of **(a)** (111), **(b)** (110), and **(c)** (100) orientations. Scale bar for **(a-c)** is 20 μm.

3.7 Moving Toward Larger Diameter, Denser Wire Arrays

3.7.1 Motivation and Approach

According to the radial junction theory,[33] larger diameter wires will need to be grown to optimize the energy-conversion efficiency based on the minority-carrier collection length

of the Si wires. Arrays of smaller diameter wires have higher surface area, which increases overall surface recombination and lowers the V_{oc} because of the increased dark current (Equation 2.2). Therefore, without accounting for optical effects, the ideal Si wire array cell would have wires with the largest diameter that could be tolerated based on its minority-carrier collection length. Using e-beam lithography to create contacts to individual wires, four-point probe measurements to Au-catalyzed VLS-grown Si wires indicated minority-carrier diffusion lengths > 2 μm.[120] Similar studies later concluded that both Ni-catalyzed[34] and Cu-catalyzed[121] wires had minority-carrier diffusion lengths ≥ 10 μm. Optimized geometries are therefore likely to have wire diameters significantly larger than the ~ 1.5 μm initially reported.[119]

The photocurrent generated by a Si wire array cell should be optimized by maximizing the light absorption within the wires. In addition to standard industry techniques such as back reflectors and antireflection coatings that could potentially be added to a finalized array, absorption could be improved by increasing the packing density of the wires. The high-fidelity $SiCl_4$ VLS-grown wire arrays reported, with diameters of ~ 1.5 μm in a square arrangement of 7 μm pitch, have a packing fraction (percentage of the cross-sectional device area occupied by wires) of only ~ 4%.[119] Optical absorption studies conducted by our group on these wire arrays indicated that very high absorption is possible with an increased packing fraction, with even relatively sparse arrays (packing fraction ~ 10%) able to absorb nearly 80% of above band gap solar illumination.[122]

With an emphasis on larger diameter, more closely spaced wires, the ability to grow arrays with thermally evaporated catalyst metal becomes limited. As the patterned photoresist holes get closer together and the overlying metal layer gets thicker,

performing the lift-off procedure becomes increasingly difficult. It should be possible to avoid this issue by switching to electrodeposition as the method to selectively place catalyst metal in the holes of the patterned oxide buffer layer. This technique is particularly beneficial because the insulating properties of the oxide layer prevent metal from depositing on the entire surface, resulting in much less catalyst metal that must be recycled or wasted.

3.7.2 Designing for Arrays of a Specific Wire Size

To use electrodeposition to grow larger diameter wires, it should be helpful to have a decent initial estimation of the amount of charge to pass per sample area in order to deposit catalyst plugs that will result in wires of a predetermined radius. The following analysis attempts to provide that estimation. More details are available in the appendix.

The wire radius, r_w, can be related to the catalyst tip volume, V_{cattip}, by considering the contact angle, θ_c, that the specific metal forms with the silicon wire (Figure 3.8a). $\theta_c = 90° + \varphi$, where φ is the angle between the liquid-vapor interface and the direction of wire growth. From this, and assuming no tapering of the wire, it can be determined that:

$$r_w = r_{cat} \cos\varphi \tag{3.1}$$

$$V_{cattip} = \frac{4}{3}\pi r_{cat}^3 \left[1 - \frac{1}{8}\left(3\cos^2\varphi + (1-\sin\varphi)^2\right)(1-\sin\varphi)\right] \tag{3.2}$$

where r_{cat} is the radius of the spherically shaped catalyst tip. The contact angles of the relevant catalyst metals with Si{111} faces are known,[105] and Table 3.1 uses this information with Equations 3.1 and 3.2 to show V_{cattip} in terms of r_w.

The volume in Equation 3.2 is the same volume of catalyst (perhaps multiplied by a factor to account for any volumetric expansion upon saturation with Si and conversion to a eutectic alloy, which will be neglected here) that must be present on each patterned site on the substrate during growth. However, if a pure wafer is being used as the substrate, a fraction of the deposited catalyst metal will dissolve into the wafer during the annealing stage up to its solid solubility at 1000 ºC. The volume of the catalyst plug, $V_{catplug}$, that must be deposited on the substrate is therefore equal to the wire catalyst tip volume, V_{cattip}, plus the volume per plug of pure catalyst metal that is dissolved into the wafer at the reaction temperature, $V_{catwafer}$:

$$V_{catplug} = V_{cattip} + V_{catwafer} \tag{3.3}$$

The volume of metal per catalyst plug that would be dissolved into a pure Si wafer, assuming sufficient annealing time to reach saturation and a substrate with a fully patterned front surface, is:

$$V_{catwafer} = \frac{C_{s,cat} M_{cat} t_{wafer}}{N_A \rho_{cat} \rho_{elec}} \tag{3.4}$$

where $C_{s,cat}$ is the solid solubility of the catalyst metal in Si at 1000 ºC (values in Table 3.1), t_{wafer} is the thickness of the wafer (excluding oxide thickness), N_A is Avogadro's number (6.022 x 10^{23} atoms/mol), M_{cat} is the molecular weight of the catalyst metal, ρ_{cat} is the mass density of the catalyst metal, and ρ_{elec} is the number of catalyst plugs per unit of projected electrode surface area. For a square arrangement and hexagonal arrangement, respectively:

$$\rho_{elec,square} = \frac{1}{p^2} \tag{3.5}$$

$$\rho_{elec,hex} = \frac{2\sqrt{3}}{3p^2} \tag{3.6}$$

where p is the pitch, or center-to-center distance, of the catalyst particles. If the substrate is being reused for wire growth (see Section 4.3), $V_{catwafer}$ should be near zero, unless the wafer has been gettered to lower the impurity concentration. In that case, Equation 3.4 should be adjusted accordingly for the concentration of catalyst metal left in the wafer after gettering.

The thickness of the deposited catalyst plug can also be determined. The hole within the thermal oxide layer where the catalyst is deposited is actually a truncated cone (Figure 3.8b) rather than a cylindrical shape because buffered HF etches SiO_2 isotropically and thus undercuts the photoresist at approximately the same rate it etches downward.[96] Note that this means the center-to-center pitch must be greater than twice the oxide thickness plus the patterned hole diameter or else the holes will begin to etch into each other. The minimum pitch could possibly be changed in a future processing scheme by using an anisotropic dry etch such as reactive ion etching, in which case a cylindrical hole should be used instead. The radius of the oxide holes, r_h, is set by the photolithography mask but can be made larger by extended etching. When designing a mask, r_h should be > r_w, and most likely $r_h \geq r_{cat}$. It is unclear what minimum oxide thickness is necessary to confine the catalyst metal on the Si surface during the reaction. However, an oxide thickness, $t_{ox} \geq t_{cat}$, where t_{cat} is the deposited catalyst thickness, should prevent the catalyst from migrating and lowering the pattern fidelity. Assuming then that the deposited catalyst layer is not thicker than the oxide, and that the oxide etch

is well calibrated so that the bottom of the hole is the expected size, the volume of catalyst in the patterned hole is:

$$V_{catplug} = \frac{1}{3}\pi\left[t_{cat}^3 + 3t_{cat}^2 r_h + 3t_{cat} r_h^2\right] \tag{3.7}$$

Knowing r_h and determining $V_{catplug}$ from Equations 3.2 – 3.4 and Table 3.1, t_{cat} may be calculated to estimate the necessary t_{ox} for a given wire radius.

The total charge that must be passed in an electrodeposition process can be determined from the volume of each catalyst plug along with the pattern arrangement and pitch:

$$Q = \frac{nF\rho_{cat} V_{catplug} A_{elec} \rho_{elec}}{M_{cat}} \tag{3.8}$$

where Q is the total charge passed, n is the number of electrons required to deposit one atom of catalyst metal, F is Faraday's constant, A_{elec} is the projected surface area of the electrode exposed to electrodeposition conditions, and the other variables have the meanings defined above.

The preceding analysis does not account for volume expansion or contact angle differences due to changes in the surface tension when the catalyst droplet is saturated with Si at reaction temperatures. However, these formulas should enable a reasonable first estimate to be made for the total charge that must be passed to electrodeposit the proper amount of catalyst that will yield a desired Si wire diameter. Correction factors could be determined by experiment.

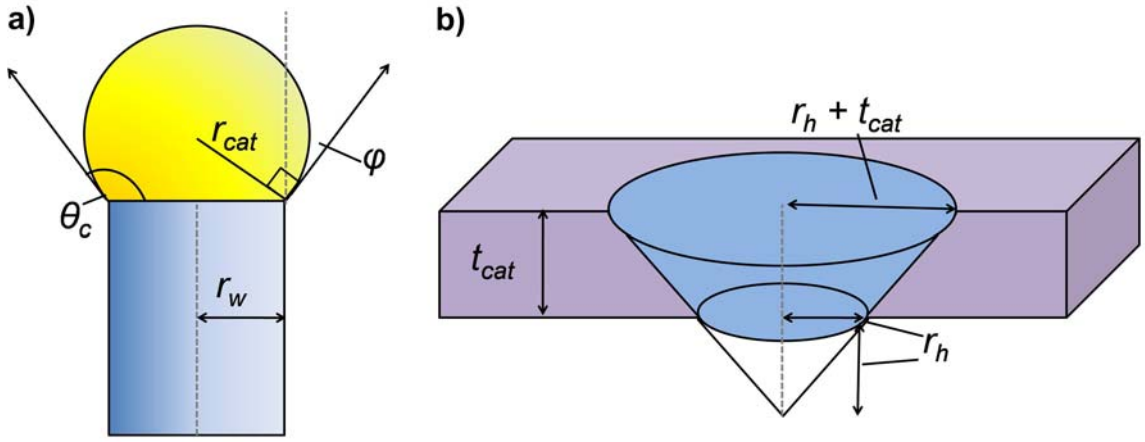

Figure 3.8. Schematics for relating wire size to catalyst deposition. **(a)** Schematic of a Si wire tip showing the relation between wire radius, r_w, catalyst tip radius, r_{cat}, and the contact angle between the catalyst metal and the Si(111) surface, θ_c, where $\theta_c = 90° + \varphi$. **(b)** Schematic of the truncated-cone-shaped hole that results from etching the oxide surface with buffered HF. The radius of any circle through the cone is equal to the hole radius at the bottom, r_h, plus the height of the circle from the bottom, so that a deposited catalyst plug has a top surface radius of $r_h + t_{cat}$ as long as it is not thicker than the oxide.

Table 3.1. VLS catalyst properties.

Catalyst	Au	Cu	Ni
θ_c (°)[105]	110	135	120
φ (°)	20	45	30
r_{cat}	$1.06r_w$	$1.41r_w$	$1.15r_w$
V_{cattip}	$1.20\pi r_w^3$	$3.55\pi r_w^3$	$1.73\pi r_w^3$
$C_{s,cat}$ (atoms cm^{-3})[123, 124]	~ 8 x 10^{15}	~ 3 x 10^{17}	~ 1 x 10^{17}
M_{cat} (g/mol)	196.97	63.55	58.69
ρ_{cat} (g/cm^3)	19.32	8.96	8.91

3.7.3 Hexagonally Packed, 3 – 4 μm Diameter Wire Arrays

Au was used to demonstrate the premise of growing larger diameter, more densely packed wires through the electrodeposition of catalyst metal. A Si(111) wafer (330 - 430 μm thick n-type Si, doped with Sb to a resistivity of 0.005 – 0.02 Ω-cm, International Wafer Service, Inc.) was heated at 1000 ºC under a flow of fully hydrated O_2 at 1 atm for 3.5 h, resulting in a thermal oxide surface layer of ~ 900 nm thickness as verified by ellipsometry. The wafer was photolithographically patterned with S1813 photoresist (Microchem) using a mask with circles of 5 μm diameter hexagonally packed with a pitch of 7 μm, followed by immersion for 10 min in buffered HF(aq) (Transene, Inc., 9% HF, 32% NH_4F) to remove the oxide in the holes formed by exposure of the photoresist (Figures 3.9a-c). The photoresist was subsequently removed with acetone.

Electrodeposition was then used to deposit the Au VLS catalyst into the holes in the oxide. The oxide was removed from the back surface of the Si by etching the back for > 10 min with buffered HF(aq), and care was taken during this step to avoid any contact of the HF(aq) with the front surface of the wafer. A piece of two-sided, conductive Cu tape was then attached to the back of the wafer, and the assembly was made into an electrode by connecting the other side of the Cu tape to a Cu wire that was sealed in a glass tube. Mounting wax was used to seal the tube and cover the wafer, so that only the patterned oxide on the front of the wafer was exposed. This electrode was then dipped in 10% (by volume) HF(aq) for 10 s to remove the native oxide at the bottom of the patterned holes. The electrode was rinsed thoroughly in H_2O and then immediately transferred to a Au electrodeposition bath (Orotemp 24 from Technic Inc.). Relatively low current densities (0.4 to 0.8 mA cm^{-2} of exposed wafer area between the Si working electrode and the Pt

gauze counter electrode) and Si wafers of high conductivity were required to electrodeposit uniform layers of Au selectively inside the oxide pattern (Figure 3.9d). The deposition was allowed to proceed galvanostatically until 0.2 – 0.4 C cm^{-2} of charge had been passed. The wafer, with metal catalyst deposits in the patterned holes in the oxide layer, was then recovered from the electrode by thoroughly dissolving the mounting wax in acetone. The patterned sample was then put into the CVD reactor, and Si wires were grown using the conditions described in Section 3.5.3 with 30 min of growth time.

The resulting Si wire array was significantly denser than the previously published array.[119] The earlier array, with 1.5 μm diameter wires in a square arrangement of 7 μm pitch, had a packing fraction of only ~ 4%, while the hexagonally packed arrays had wire diameters of 3 – 4 μm with a 7 μm pitch, resulting in packing fractions of ~ 17 – 30% (Figure 3.10). The fidelity was high for these electrodeposited arrays but became poor if wire diameters > 4 μm were attempted with this pattern and oxide thickness. After 30 min of growth, these wires were ~ 60 μm long. In the earlier square arrangement array, the wires were ~ 100 μm long after the same growth period. The slower growth of the larger diameter, more densely packed array under the same conditions suggests that the growth rate may have been limited by the flux of $SiCl_4$ to the sample. The successful fabrication of larger diameter wires of fairly high packing density using electrodeposition of the catalyst demonstrates that arrays of optimal geometry can be produced using a low-cost metal deposition technique.

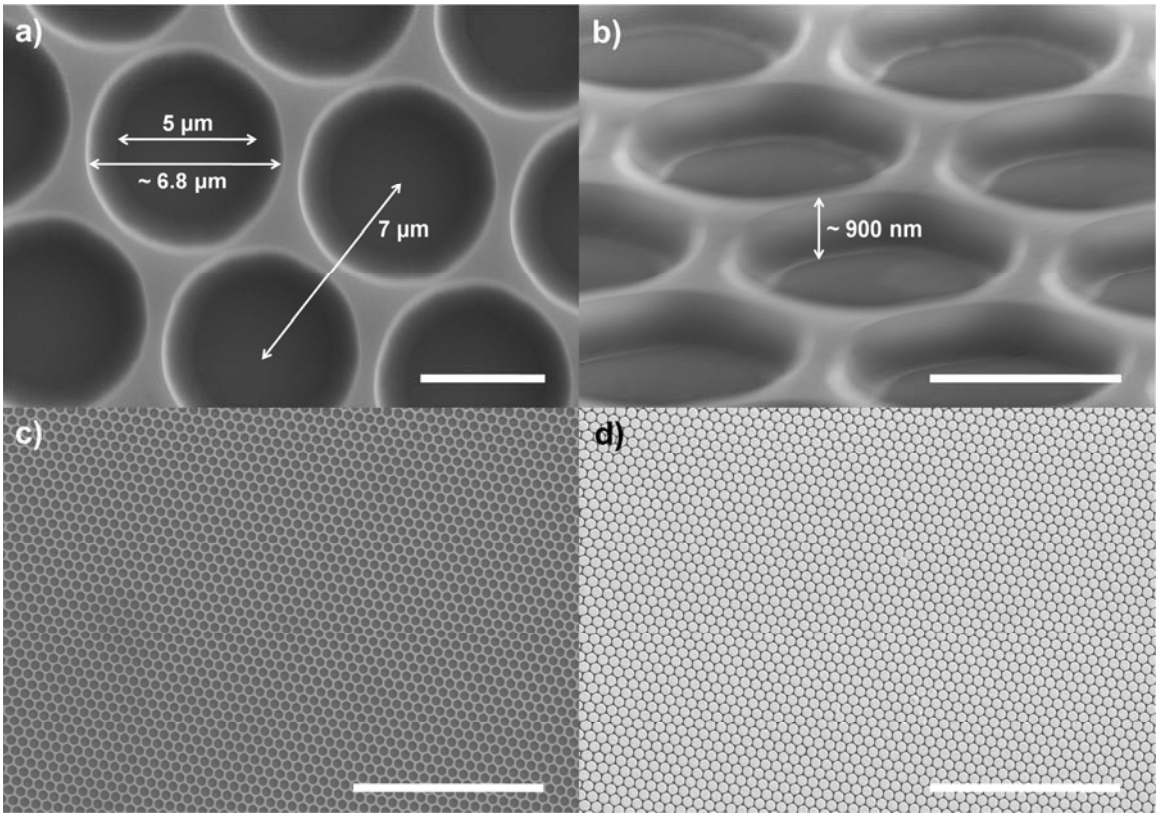

Figure 3.9. Oxide patterning and electrodeposition of a hexagonally packed array. **(a)** Top-down view and **(b)** tilted-view SEM images of a 5 µm hole diameter, 7 µm pitch pattern etched into a ~ 900 nm thick thermal oxide on Si(111). Scale bar for **(a,b)** is 4 µm. Top-down view SEM images of the hexagonally packed pattern **(c)** before and **(d)** after electrodeposition of Au catalyst. Scale bar for **(c,d)** is 100 µm.

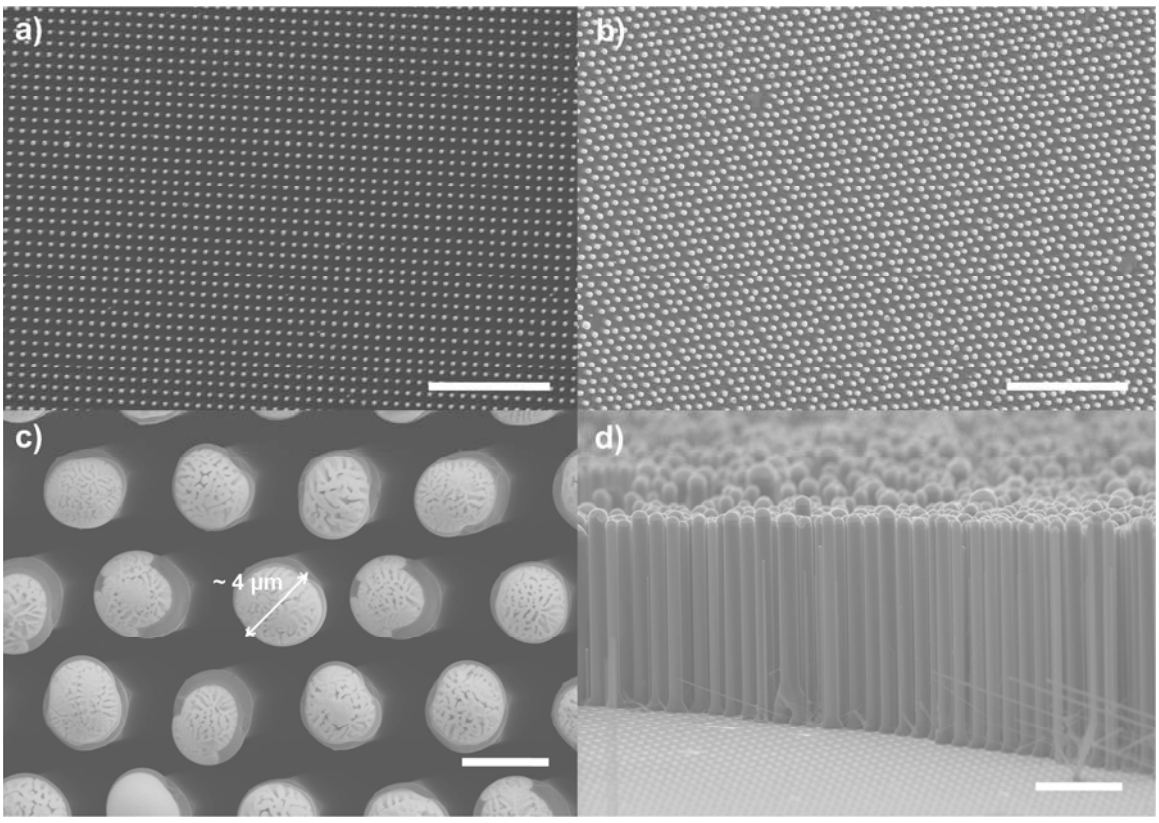

Figure 3.10. Hexagonally packed wire array grown from electrodeposited Au. Top-down view SEM images of **(a)** the original 3 µm diameter hole, 7 µm pitch, square packed wire array and **(b)** the 5 µm diameter hole, 7 µm pitch, hexagonally packed wire array. Scale bar in **(a,b)** is 50 µm. SEM images of the hexagonally packed array from the **(c)** top-down view, showing wires with diameters up to ~ 4 µm, and **(d)** tilted-view, showing wires ~ 60 µm long. Scale bar is 4 µm for **(c)** and 20 µm for **(d)**.

3.8 Conclusion

Si, as the predominant semiconductor of the photovoltaics industry and an indirect gap absorber easily limited by its minority-carrier diffusion length, is a logical material to be applied in the radial junction architecture. The vapor-liquid-solid mechanism is a convenient route to the fabrication of one-dimensional Si structures that, when guided by patterned catalysts, can produce highly uniform wire arrays of tunable dimensions.

Electrodeposition, rather than thermal evaporation, of catalyst allows larger diameter, more densely packed wire arrays to be produced while minimizing wasted metal. These techniques should permit the fabrication of uniform Si wire arrays of nearly any diameter, length, or spacing within the regime of interest, which makes possible the careful study of the solar energy-conversion properties of Si using radial junctions.