Chapter 1

Thesis Overview

1.1 Introduction to nanoelectronics

Nanoelectronics is an emerging field whose goal is to surpass existing ultra-large-scale integration (ULSI) technology in device size, density, and performance. This is indeed a challenge, as current silicon ULSI technology has been improving at an aggressive rate since the manufacture of the first integrated circuit (IC) in 1959.[1, 2] In 1965, the co-founder of Intel, Gordon Moore, made the famous prediction that the number of transistors in an IC would double approximately every 24 months.[3] This prediction has astonishingly held true for the past 40 years. IC technology has rapidly progressed from small scale integration (SSI) in the 1960s, with less than 30 transistors per chip, to the current technology, ULSI, with over 1,000,000 transistors per chip.

The success of Moore's law has been due to three factors.[4] First, the size of the transistor, the active element in ICs, has steadily decreased. The Intel Corporation's

current 45 nm technology contains transistors with a physical gate length of ~ 22 nm. In contrast, the gate length of the state-of-the-art transistors in 2001 was ~ 5.5 times larger. Also, the area on which the transistor sits has decreased by a factor of 30.[5] Second, the size of ICs has also increased. This has been due to both increasing the size of Si wafers and improving the capabilities of the fabrication tools. Lastly, the architecture of ICs has improved and fewer transistors are required to perform a specific function.

However, the conventional lithography techniques used to produce modern ICs will not be able to indefinitely shrink transistor size or increase density. The United States Semiconductor Industry Association, a nonprofit organization that assesses the future semiconductor industry's technology requirements and publishes the International Technology Roadmap for Semiconductors (ITRS), has stated it will be a "difficult challenge" to progress complementary metal oxide semiconductor (CMOS) technology beyond the 22 nm technology generation.[6] This challenge has stimulated intense research for alternatives to conventional, planar Si transistors.

The next-generation devices will most likely be based on non-planar structures such as double-gate FETs[7, 8] and fin-FETs,[9, 10] as well as on non-Si electronic materials, such as III-V compound semiconductors.[11–13] However, both of these technologies rely on an enhancement of individual device performance (such as increased mobility, lower leakage current, or higher drive current)[9, 14] and do not solve the issues of the size and density limitations.

To directly address these challenges, novel nanoscale transistor channel materials, such as semiconducting nanowires (NWs)[15–18] and carbon nanotubes (CNTs)[19–25] are also being explored. These materials are attractive because they have very narrow diameters

and have no density limitations since they are not fabricated using conventional lithography techniques. NWs and CNTs can also exhibit enhanced electronic behavior due to their highly confined nature, such as a high intrinsic mobility[17, 26] and enhanced phonon drag.[27] Additionally, these materials possess other interesting properties due to quantum confinement effects and their high surface area-to-volume ratios, which can be exploited in other fields, such as chemical and biological sensing,[28, 29] superconductivity,[30] and thermoelectrics.[27, 31]

Another class of nano-materials that will become increasingly more important for electronics applications are molecules. Individual molecules represent the ultimate scaling of electronic components and are fabricated using a bottom-up approach. Single molecules and monolayers can be used as the active electronic element or they can be used to enhance the properties of other nanoscale materials. For instance, molecules have been exploited as an active element for high-density logic and memory circuits.[32, 33] Examples of ways that molecular films can enhance other devices include passivating NW surfaces,[34] acting as gate dielectrics,[35, 36] and being the capture agents in sensors.[28, 37]

NWs, CNTs, and molecular films for electronics are still in the development stage and have not yet been fully utilized for any commercial application. The major problems associated with using these materials include difficulty in placing and aligning devices, controlling surface properties, and reducing variability in performance. For instance, the synthesis of single-walled CNTs will produce a distribution of diameters and chirality, which has profound affects on their electrical properties.[26, 38] Even if a synthetic approach yielded identical tubes, it is still prohibitively difficult to align these devices into a working circuit that is competitive, in terms of density or number of devices, with

CMOS technology. To fully utilize these nanoscale materials, the ITRS has summarized several challenges that must be addressed (Table 1.1):[6]

Table 1.1. Summary of nanoscale material challenges. Table adapted from Ref [6], Table ITWG6. Issues highlighted in blue are specifically addressed in this thesis.

Difficult Challenges ≤ 22 nm	*Summary of Issues*
Control of nanostructures and properties	Ability to pattern sub-20-nm structures in resist or other manufacturing related patterning materials (resist, imprint, self-assembled materials, etc.) (Chapter 2)
	Control of surfaces and interfaces (Chapter 2)
	Control of CNT properties, bandgap distribution, and metallic fraction
	Control of stoichiometry and vacancy composition in complex metal oxides
	Control and identification of nanoscale phase segregation in spin materials
	Control of growth and heterointerface strain
	Ability to predict nanocomposite properties based on a "rule of mixtures"
	Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability (Chapter 4)
	Control of interface properties (e.g., electromigration)
Control of self assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components (Chapter 3)
	Control of line width of self-assembled patterning materials (Chapter 5)
	Control of registration and defects in self-assembled materials
Compatibility with CMOS processing	Integration for device extensibility (Chapter 2)
	Material compatibility and process temperature compatibility (Chapters 2, 3)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures (Chapter 5)
	Device structure-related properties, such as ferromagnetic spin and defects
	Dopant location and device variability (Chapters 2, 3)

The goal of this thesis is to provide solutions to several of the challenges associated with working with nanoscale materials. The specific challenges that were addressed in this work are highlighted in blue in Table 1.1. In Chapter 2, a method is described that generates silicon nanowires (Si NWs) with a high control over their

placement, alignment, and doping and surface properties. Field-effect transistors (FETs) utilizing the NWs as the channel material were found to have high performance metrics and consistent behavior. In Chapter 3, the NW FETs were utilized for complementary symmetry logic circuits, which required precise alignment of devices and interconnects. In Chapter 4, these circuits were optimized by utilizing a strategy that coupled prototype devices with device and circuit simulations. Lastly, in Chapter 5, the silicon/molecular interface was manipulated by microcontact printing methods for molecular electronics applications. These advancements show that nanoscale materials *can* be highly controllable and that nanoscale electronics is a realizable technology.

1.2 Organization of the thesis

This thesis is organized into four main chapters. Each chapter was written to be largely self-contained and complete. To avoid excessive redundancy, lengthy information that is required in a later chapter of the thesis was occasionally referenced to an earlier chapter.

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1.2.1 Summary of Chapter 2

Chapter 2, titled "High-performance nanowire field-effect transistors", discusses the development of high-performance n- and p-type field effect transistors (FETs) from Si NWs generated from the superlattice nanowire pattern transfer (SNAP) process.[17, 18] The SNAP process produces ultra-dense arrays of metal or Si NWs at 33 nm pitch with virtually no defects using a template-mediated approach.[39] The NWs are doped by using conventional diffusion doping on the substrates prior to the NW formation.[40] The development of the SNAP process and the diffusion doping technique are introduced in the chapter. These technologies were the key behind the fabrication of NW FETs with consistent behavior and strong performance metrics, such as high on/off ratios, high mobilities, and small subthreshold swings.

Another important aspect to generating successful NW FETs was exploring methods to control the properties of the NW surface. A comparison of NW and microwire (μW) FET performance revealed that the NW FET performance is dominated by the properties of the surface. Reducing the amount of surface states increased the performance of the NW FETs significantly. This laid the foundation for developing complementary symmetry (CS) logic circuits from these devices.

1.2.2 Summary of Chapter 3

Once NW FETs were developed, their integration into CS circuits was explored in Chapter 3, titled "Fabrication and characterization of complementary nanowire logic circuits".[18] To achieve side-by-side p- and n-FETs on a single substrate, two technologies were developed: a patterned doping technique that allowed for spatial control of doped regions, and a SNAP master alignment system that facilitated the precise placement of NWs on the substrate. These technologies allowed the n- and p-FETs to be fabricated with precise control over location and alignment on a single substrate. The pattern doping technique was characterized using electrostatic force microscopy and by testing fabricated pn diodes. The inverter circuit, which represents the most basic Boolean logic function and consists of 1 p-FET and 1 n-FET,[41] was fabricated and tested. A gain of ~ 5 was consistently measured from 7 working inverter circuits. This demonstration provided the foundation for the eventual fabrication and characterization of the other Boolean logic functions.

1.2.3 Summary of Chapter 4

In Chapter 4, "In silico design optimization of nanowire circuits", a methodology is described that optimizes the design of high-performance logic circuits constructed from Si NW p- and n-type FETs.[42] Although NW circuits were demonstrated in the previous chapter, improving their performance is difficult and time consuming. In this methodology, circuit performance can be predicted from individual fabricated NW FETs before prototype circuits are manufactured, resulting in a faster and more efficient design process. NW FETs are fabricated and electrically characterized, the results of which are

placed into a circuit simulation environment. Next, a variety of DC and transient analyses can be performed for various circuit designs, and various circuit metrics can be optimized in silico. These results suggest design options for fabricating high performance NW circuits, which can then be implemented experimentally. The effectiveness of this methodology is shown by optimizing the gain of Si NW complementary symmetry inverter from an initially measured value of 8 to a gain of 45.

1.2.4 Summary of Chapter 5

Chapter 5, "Microcontact printing methods for molecular electronic applications", discusses efforts to develop methods to covalently attach electronically interesting molecules onto gold and silicon substrates. These methods utilized an elastomer stamp coated with reactive molecules. Pressing the stamp to a monolayer-covered substrate encourages the covalent attachment of the reactive molecules to the monolayer due to the highly concentrated environment. In these studies, the Cu^{I}-catalyzed azide-alkyne cycloaddition (CuAAC) reaction was used to form the covalent attachment. It was observed that the reaction would proceed readily by replacing the Cu catalyst in the stamp ink (the homogeneous catalyst) by a Cu coating on the stamp directly (the heterogeneous catalyst). Kinetics were monitored using ferrocene as the attached species and electrochemical measurements, and it was shown that the heterogeneous catalyst proceeded almost as quickly as the homogeneous catalyst (30 minutes versus 60 minutes). This reaction proceeded quickly on both azide-terminated monolayers on Au and Si(111) substrates.

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