Chapter 5

Covalent modification and electrical characterization of silicon (111)-on-insulator devices

5.1 Introduction

5.1.1 Electrical properties of silicon surfaces

As the dimensions of silicon (Si) devices are scaled to the nanometer regime, the properties of the surface play an increasingly prominent role in determining the overall device characteristics. This has presented significant challenges, and opportunities, to the nanoelectronic community, where surface effects manifest over a range of applications. Recent examples include substantial increases in the quality factor of electromechanical resonators through covalent modification of the surface[1], and the demonstration that electrical transport in ultra-thin (< 20 nm) silicon-on-insulator epilayers can be completely dominated by the electronic properties of the surface[3]. Silicon-on-insulator, or SOI, consists of a thin layer of single-crystal Si on a SiO_2 support, and is rapidly becoming the preferred platform for high-speed microelectronics, nanoelectronics, and sensor applications. However, surface effects such as interface roughness[6, 7], surface

optical[8-13] (SO) phonons, film stress[14], and coulombic interactions with electrically active surface states[15] (also called interface or trap states) scatter charge carriers in thin-film SOI devices, resulting in degradation of charge-carrier mobility. Additionally, surface states introduce localized energy levels continuously distributed in energy throughout the silicon bandgap that function as recombination-generation (R-G) centers catalyzing the annihilation and/or creation of charge carriers (Figure 5-1.A). Such states facilitate indirect recombination of electron-hole pairs by capturing an electron (or hole) within a bound-state orbit about the R-G center site until recombination occurs. This significantly increases the probability of electron-hole recombination, since an electron and hole no longer have to interact simultaneously in space and time[16, 17]. The technological implication of charge-carrier annihilation and creation due to electrically active surface states is the introduction of a significant amount of randomness into the operational behavior of the device. This is because the character, density, and energy distribution of surface states are exquisitely sensitive to very small fabrication details, and thus vary considerably from device to device[18].

The most egregious effect of surface states is their introduction of significant non-idealities into the behavior of metal-oxide-silicon (MOS) field-effect devices, the workhorse of modern information-processing technology, and the operational basis for the demultiplexer architecture described in Chapter 3. Figure 5-1.B shows how surface states influence the electrical characteristics of field-effect devices. To a good approximation, all surface states below the Fermi energy, E_F, are full and those above it are empty. These states continuously fill and empty as the Fermi energy moves upward in the bandgap with positive gate voltages and downward with negative gate voltages,

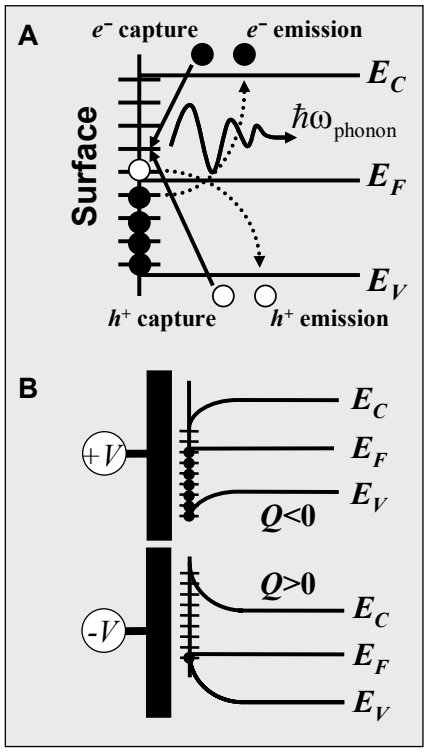

Figure 5-1. Surface states at a silicon interface. A. Surface states are distributed throughout the bandgap and can capture (solid arrows) or emit (dotted arrows) charge carriers. Carrier capture can result in electron-hole recombination with emission of lattice phonons. **B.** Surface states charge and discharge as a function of gate bias producing a net charge Q at the surface (see text).

respectively. Surface states roughly above the middle of the bandgap are believed to be acceptor-like (that is, neutral when empty and negative when filled with an electron), while those below midgap are believed to be donor-like (that is, positively charged when empty and neutral when filled with an electron)[19]. Thus, the application of a gate voltage produces a net charge per unit area, Q, at the Si/oxide interface of a MOS device. Since the surface states always remain fixed in energy relative to the conduction and valence band edges, a voltage more positive than the flat-band voltage, V_{FB}, (the voltage in which there is no band bending at the surface) draws electrons into the upper, acceptor-like surface states, making $Q < 0$, while negative voltages less than V_{FB} empties those states, making $Q > 0$. The point is that surface states can charge and discharge as a function of gate voltage, resulting in understandable, but generally unpredictable, behavior from field-effect devices.

To see this more quantitatively, consider a simple metal-oxide-silicon (MOS) capacitor (where the oxide is unspecified). Taking the direction from the metal/oxide interface into the Si layer as the positive x-direction (with $x = 0$ at the metal/oxide

interface), the potential applied to the metal gate, V_G, is dropped partly across the oxide, $\Delta\phi_{ox}$, and partly across the Si bulk, $\Delta\phi_{Si}$, or

$$V_G = \Delta\phi_{ox} + \Delta\phi_{Si} = \Delta\phi_{ox} + \phi_S \,, \tag{1}$$

where ϕ_S is the potential at the Si/oxide interface (since the potential goes to zero within the Si bulk). Poisson's equation can be used to relate the voltage dropped across the oxide to the potential at the Si surface as

$$\nabla^2\phi = -\frac{\rho_{ox}(x)}{\kappa_{ox}\varepsilon_0} = -\frac{dE_{ox}}{dx}, \tag{2}$$

where $\rho_{ox}(x)$ is the charge density distribution across the oxide layer, E_{ox} is the electric field across the oxide layer, and κ_{ox} is the oxide dielectric constant. Two integrations of equation (2) across the oxide layer of thickness t_{ox} then gives

$$\Delta\phi_{ox} = t_{ox}E_{ox}(t_{ox}) - \frac{1}{\kappa_{ox}\varepsilon_0}\int_0^{t_{ox}}\int_x^{t_{ox}} \rho_{ox}(x')dx'\,dx \,. \tag{3}$$

Invoking the electrostatic boundary condition relating the normal components of the electric displacement fields on either side of the Si/oxide interface, and assuming there is no charge at the interface other than that possibly included in ρ_{ox} gives

$$E_{ox}(t_{ox}) = \frac{\kappa_{Si}}{\kappa_{ox}}E_S(\phi_S) \,, \tag{4}$$

where κ_{Si} is the Si dielectric constant, and E_S is the electric field at the Si/oxide interface (which, of course, is a function of ϕ_S). The oxide charge density due to charged surface states resides right at the Si/oxide interface, and thus can be modeled as a delta function. Substituting $\rho_{ox}(x) = \pm Q(\phi_S)\,\delta(x - t_{ox})$ and equation (4) into equation (3) then gives

$$\Delta\phi_{ox} = \frac{\kappa_{Si}}{\kappa_{ox}}t_{ox}E_S - \frac{t_{ox}Q}{\kappa_{ox}\varepsilon_0} = \frac{\kappa_{Si}}{\kappa_{ox}}t_{ox}E_S(\phi_S) \pm \frac{Q(\phi_S)}{C_{ox}} \,, \tag{5}$$

where C_{ox} is the oxide capacitance per unit area. Substituting equation (5) into equation (1) gives

$$V_G = \phi_S + \frac{\kappa_{Si}}{\kappa_{ox}} t_{ox} E_S(\phi_S) \pm \frac{Q(\phi_S)}{C_{ox}}. \quad (6)$$

Equation (6) relates the voltage applied to the gate of a field-effect device, V_G, to the voltage 'seen' by the Si surface, ϕ_S. The effect of charged surface states is accounted for by the last term, which shows that the required gate voltage to obtain a given surface potential (the operational voltage of the device) will vary from device to device due to the presence of Q in equation (6).

Intensive experimental investigation of the Si surface and the Si/oxide interface (especially the Si/SiO_2 interface) has identified unsatisfied or 'dangling' Si bonds at the Si surface as the primary physical origin of surface states. When the Si lattice is cleaved along a particular plane to form a surface, one of the four Si–Si bonds is broken, thus leaving a dangling bond pointing in the direction perpendicular to the surface plane. The density of these dangling bonds per unit area of surface depends on the surface orientation and whatever reconstruction the surface might undergo[18]. Growth of a SiO_2 layer at the Si surface satisfies many of these dangling bonds (with the number critically dependent on the quality of the SiO_2 and thus the growth conditions), but not all, and the remaining dangling bonds are believed to result in electrically active surface states[20].

While the density of surface states and their energy distribution can vary considerably from one device to the next, the vast amount of experimental research on the electrical properties of Si surfaces has revealed some general trends[19]. For one, the density of surface states (states per unit area per unit energy) is about an order of magnitude greater on (111) surfaces than on (100) surfaces. This observation is correlated

with the number of dangling bonds per unit area at the Si surface. A (111) surface has roughly 15 percent more dangling bonds, which results in a faster oxidation rate of the (111) surface than the (100) surface during SiO_2 growth, a higher percentage of Si sub-oxides (SiO_x with $x \leq 2$), and thus a larger density of surface states[21]. It is primarily for this reason that the Si(100) surface has been used almost exclusively in the microelectronics industry.

5.1.2 Covalent modification of silicon (111) surfaces

Despite the less-than-ideal Si(111)/SiO_2 interface, the Si(111) surface has a number of attractive qualities for scientific and technological applications. The majority of these applications stem from the fact that a (111) surface can be made atomically smooth with nearly perfect hydrogen termination through simple bench-top aqueous NH_4F etching[22, 23]. In addition, dangling bonds on a (111) surface point in a direction normal to the surface plane, resulting in a structurally and chemically simple surface ideal for ultra-high vacuum (UHV) surface studies, such as scanning tunneling microscopy (STM)[24, 25] and small molecule adsorption[26], in addition to providing a convenient handle for covalent functionalization of the surface using a variety of techniques[27].

The hydrogen-terminated Si(111) surface obtained after aqueous fluorine-based etching has been well documented to have a low number of structural defect sites and electrically active surface states. This was first demonstrated by Yablonovich *et al.* through surface recombination measurements of hydrogen-terminated Si(111) surfaces[28] and has since been corroborated by a number of researchers[2, 27, 29]. The number of electrically active states on Si(111) surfaces has been reduced to very low levels (less

than one electrically active state per 10^8 surface atoms) through complete hydrogen passivation[28]. This is about two orders of magnitude less than the number of surface states measured from optimally-processed Si(100)/SiO_2 interfaces.

However, the electronic quality of hydrogen-terminated Si(111) surfaces rapidly degrades in air due to surface oxidation[29-31]. Consequently, several methods have been developed to achieve robust oxide-free alkyl passivation of crystalline Si surfaces[27]. These methods feature direct carbon-silicon bonding (as opposed to more labile Si–O–C linkages) and offer the advantage of a well ordered monolayer via kinetically inert covalent bonds that are stable up to 650° C in UHV[32].

Directly bonded alkyl monolayers have been demonstrated to be of much higher quality on Si(111) surfaces than on Si(100) surfaces[33]. This is because the top-most atoms of a Si(111) surface are characterized by a single dangling bond pointing perpendicular to the surface plane, while each Si(100) surface atom has two dangling bonds that point towards neighboring Si(100) surface atoms in adjacent rows. Steric interference thus prevents full alkyl passivation of Si(100) surfaces, even with the smallest hydrocarbon species, *e.g.*, methyl groups.

This is in contrast to Si(111) surfaces in which molecular modeling and cryogenic STM experiments by Yu *et al.*[24] have confirmed that complete methyl termination of every (top-most) surface Si atom on an unreconstructed (1×1) surface is possible. It is believed that surface functionalization with longer-chain alkyl groups (C_nH_{2n+1} with $n \geq 2$) results in incomplete coverage of the Si(111) surface due to steric interactions, with non-alkyl passivated surface sites being terminated primarily by hydrogen[4, 34].

The surface functionalization chemistry employed in studies by Yu *et al*. to obtain high-quality methyl-terminated Si(111) surfaces was developed within the Lewis group at Caltech[35], and consists of a simple two-step chlorination/methylation procedure. This method has been demonstrated from numerous studies to produce high-quality methyl passivated Si(111) surfaces[2, 5] that are robust to oxidation[36], and are characterized by low numbers of electrically active surface states[29]. Beyond STM studies, molecular-level control over the interfacial chemistry of Si surfaces is expected to find applications in molecular electronics[37] and nanoelectronics[38, 39]. A specific example of the latter is described below.

5.1.3 Application to FET-based nanowire demultiplexers

Methyl passivation of Si surfaces could have important applications in nanoelectronics where control of the surface is paramount. For instance, the nanowire (NW) demultiplexer described in Chapter 3 was hindered in its ability to selectively address a given NW from within an ultra-dense array by the presence of a thin native oxide coating the NWs. Figure 5-2 shows a schematic cross section of a portion of the demultiplexer structure with four NWs coming out of the plane of the page. The ability of the demultiplexer to reduce the conductivity of NW_G relative to that of NW_I is determined by the how much of the

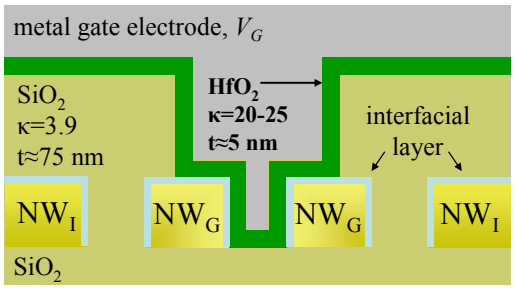

Figure 5-2. Schematic cross-section of a nanowire (NW) demultiplexer. The demultiplexer architecture selects a given NW by field-effect gating all the rest of the NWs in the array. Gated and isolated nanowires, NW_G and NW_I, respectively, are shown coming out of the page.

applied gate voltage, V_G, is seen at NW_G. This is given by the voltage dropped across the HfO_2/interfacial layer shown in the figure, and which equation (5) gives as (ignoring the surface-state term and modifying the second term to account for the added layers of dielectric material)

$$\Delta\phi_{ox} = V_G - \phi_S = \kappa_{Si}\left(\frac{t_i}{\kappa_i} + \frac{t_{HfO_2}}{\kappa_{HfO_2}}\right)E_S(\phi_S), \tag{7}$$

where t_i and κ_i are the thickness and dielectric constant of the interfacial layer (SiO_2 or CH_3). Equation (7) clearly shows that the selective gating of NW_G can be enhanced by replacing the NW native SiO_2 at the interface ($t_i \approx 1.5$ nm, $\kappa_i = 3.9$) by a covalently bonded methyl monolayer ($t_i \approx 0.2$ nm, $\kappa_i \approx 2$). Plugging these numbers into equation (7) predicts a 100 percent increase in the gating of NW_G, and, thus, a 100 percent increase in the demultiplexer selectivity (isolated NW current/gated NW current).

Additionally, CH_3-passivated NWs eliminate the electrically active native SiO_2/Si interface that has been present in previous-generation demultiplexer devices. Due to their chaotic mode of formation, native oxides are highly defective and do not successfully passivate surface states[21, 40]. Conversely, a well-ordered CH_3-Si(111) interface reduces the number of surface states by many orders of magnitude and should translate into more-efficient and -reliable FET-based devices. This could be particularly important for use with high-κ dielectrics, which generally form a significantly more-defective interface than does Si/SiO_2.

The majority of work with alkyl-passivated Si(111) surfaces has utilized bulk wafers. While such wafers are convenient for obtaining high-quality, atomically flat surfaces, and are compatible with a variety of surface characterization techniques, they

are less useful for nanoelectronic applications, where silicon-on-insulator (SOI) structures are generally required. This was the motivation for the work described below. The next two sections of this chapter will first describe the passivation and surface characterization of ultra-thin SOI, followed by electrical measurements employing variable temperature Hall effect measurements.

5.2 Fabrication and methyl passivation of SOI devices

This section describes the fabrication of Si(111)-on-insulator Hall bar devices and their functionalization using a modified two-step chlorination/methylation procedure.

5.2.1 Si(111)-on-insulator wafer fabrication

An unexpected challenge proved to be obtaining the appropriate SOI starting material. This is because the overwhelmingly dominant SOI material is Si(100), which can be purchased commercially. Additionally, (100)-oriented SOI wafers are available with Si epilayer thicknesses in the low tens of nanometers by fabrication techniques such as *separation by implanted oxygen* or SIMOX. This is in contrast to (111)-oriented SOI wafers, which are usually custom fabricated using a bonding process. This involves the oxidation of two bulk Si(111) wafers that are bonded together on their oxidized side through a high-temperature process. While this produces a Si(111)-on-insulator structure, the Si epilayer is very thick and must be subsequently thinned.

This led us to a collaboration with Isonics Corp. to develop a (111)-oriented, bonded SOI wafer (buried oxide thickness of 0.9–2 μm) with an epilayer thickness of less than 100 nm. A feedback loop was set up between our lab and Isonics to determine the processing parameters that consistently gave the highest quality Si(111) epilayer surface. Isonics' processing consisted of bonding the SOI wafer, grinding and lapping to thin it down, and applying a final (proprietary) touch polish to further reduce the Si epilayer thickness and smoothen out thickness inhomogeneities introduced during the grinding and lapping procedure. This set of procedures reduced the bonded SOI epilayer thickness to 100–200 nm. Our post-processing then consisted of thinning the wafers by growing a high-quality sacrificial oxide under dry conditions (*e.g.*, $Si + O_2 \rightarrow SiO_2$) at temperatures ranging from 1050° to 1100°. The exact growth time and temperature was obtained from calculations employing the Deal-Grove model[18] of thermal oxidation on a Si(111) surface, taking into account that 44 percent of the total thermal oxide thickness was due to consumed Si. The sacrificial oxide was then removed by wet etching in buffered oxide etch (BOE) (6:1 40% NH_4F to 49% HF; Gallade) and the thickness was measured using optical reflectance or ellipsometry. After a couple of SOI generations, the optimal starting thickness to begin thermal oxidation thinning was determined to be about 180 nm. Wafers that were polished to be thinner before the thermal oxidation step were found to produce poorer surfaces. Although these wafers were found to be locally homogeneous by atomic force microscopy (AFM) measurements, they were quite inhomogeneous over centimeter length scales. The data below shows pooled standard deviations of Si epilayer thicknesses for representative wafers. (Each row represents averages from three wafers.)

Average Si(111) epilayer thickness (nm)	Pooled standard deviation from 35 measurements on each of three samples (± nm)
20	6
34	3
45	9
50	6

5.2.2 Hall bar fabrication

Si(111)-on-insulator wafers were cleaved into approximately 1-cm squares, and doped using the spin-on doping protocol described in Chapter 2. Briefly, the wafers were sonicated in methanol and swabbed using a Texwipe CleanTip swab to remove particulates. After ensuring the wafer was clean, a 1:10 diluted (dopant to methanol) spin-on dopant solution was spin-coated (at 4000 RPM) onto the wafer surface and subsequently baked at 200° C for 10 min to drive off excess solvent. Emulsitone (Whippany, NJ) Phosphorosilicafilm and Borosilicafilm were used for n-type and p-type doping, respectively. The dopant-film-coated wafer was then annealed under nitrogen in a rapid thermal annealer for the appropriate time and temperature to achieve a given doping concentration. After annealing, the dopant film was removed by swirling in BOE until the surface was hydrophobic (usually less than 10 seconds). At this point, four-point-probe surface-resistivity measurements were used to measure the doping level, which ranged from $1\times10^{18} - 1\times10^{20}$ P or B atoms/cm^3. The measured dopant distribution

as a function of depth into n- and p-doped (111)-oriented SOI epilayers is shown in Figure 5-3.

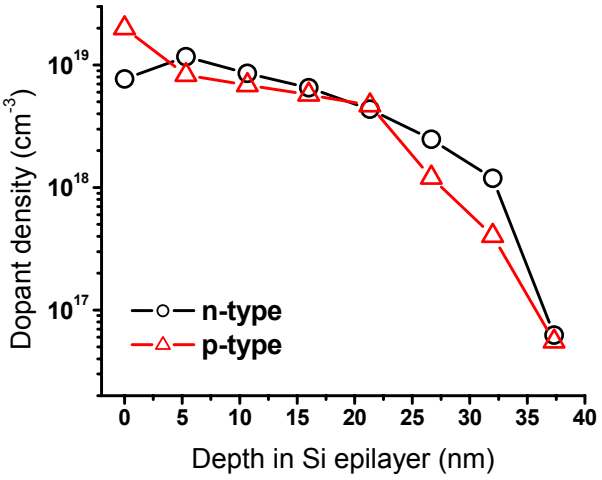

Figure 5-3. Dopant density vs. depth for 40-nm-thick diffusion-doped Si(111) epilayers. The n-type wafer was annealed for 5 min at 950° C; the p-type wafer was annealed for 5 min at 1050 ° C.

Photolithography was used to define rectangular Hall bars (described in more detail below) to facilitate resistivity and Hall mobility measurements. Specifically, AZ-5214 (Clariant) was spin-coated onto the wafer at 4000 RPM, baked at 105° C for 5 minutes, and exposed (λ = 405 nm, area dose ≈ 20 mW/cm^2) using a Karl Suss MA-6 mask aligner through a Cr mask. The exposed pattern was then developed in AZ-400k developer (pH ≈ 13, Clariant). The Cr mask exposed four Hall bar patterns into the photoresist (spaced by 1 mm along the perimeter of a square). Additionally, the mask exposed a large 2-mm square to facilitate x-ray photoelectron spectroscopy (XPS) measurements from the same chip from which the devices were fabricated. Electron-beam evaporation followed by lift-off was used to deposit 100 nm of Al onto the wafer surface to act as an etch mask. The Al Hall bar patterns were transferred into the underlying Si(111) epilayer using fluorine-based (CF_4 to He 20:30, 5 mTorr, 40 W) reactive-ion etching. The endpoint was determined via interferometric detection. The Al was then removed by 5 minutes in a ~ 50° C solution of 80% H_3PO_4 + 5% HNO_3 + 5% glacial acetic acid + 10% H_2O (18 MΩ Millipore),

revealing four Si Hall bars and a 2-mm square sitting on top of an oxide surface. Note that devices were fabricated, as much as possible, before surface passivation. This strategy avoided exposing CH_3-SOI surfaces to the harsh procedures described above (particularly AZ-400k, which is strongly basic, and the H_3PO_4/HNO_3 step).

5.2.3 Methyl passivation of SOI devices

With bulk Si(111) wafers, the various wet-chemical procedures can be allowed to continue for arbitrarily long periods without regard to over-etching the Si surface. In contrast, all of the wet chemical steps described here had to be optimized to obtain high-quality methyl passivation without over-etching the SOI surface or significantly etching the supporting SiO_2 in contact with solution. For small devices and nanowires, this caused significant undercutting which occasionally resulted in lifting-off of the SOI device (or nanowires).

Figure 5-4 shows the chlorination/methylation reaction protocol adapted from the Lewis group at Caltech[2]. Before functionalization, the wafers were rigorously cleaned to remove photoresist and fluoropolymeric by-products that may have been deposited on the surface from the previous photolithographic and etching steps. (For consistency, these steps were also followed for wafers that were not patterned into Hall bars, *i.e.*, surfaces intended for XPS analysis only.) This was accomplished with an aggressive piranha-clean

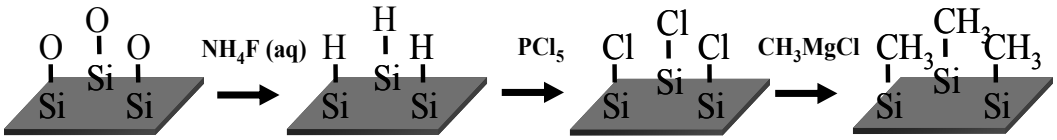

Figure 5-4. SOI chlorination/methylation reaction protocol.

step (1:2 concentrated H_2SO_4 to 30% H_2O_2 at 120º C for 5 minutes followed by a ~10 minute soak in H_2O). The wafer was etched for 5 seconds in diluted BOE (1:10 BOE to H_2O) to strip the native oxide, and rinsed in H_2O. The wafer was immediately immersed in a 1:1:5 NH_4OH:H_2O_2:H_2O solution for 15 minutes at 80º C, followed by an H_2O rinse and another 5 second dip in diluted BOE, and dried under a stream of N_2.

To obtain a flat Si(111) surface, the wafer was then etched for 5 minutes at room temperature in de-oxygenated 40% NH_4F (pH ≈ 7.8; Transene Inc.). The NH_4F was de-oxygenated by bubbling Ar into the solution with occasionally stirring for at least 40 minutes. The wafer was rinsed in water, dried under N_2, and immediately loaded into a N_2-purged glovebox for the chlorination and methylation steps. The surfaces were chlorinated using a saturated solution of PCl_5 in chlorobenzene with a few grains of benzoyl peroxide for radical initiation. The reaction time ranged from 10 to 45 minutes at 80–90º C, with the optimal reaction time discussed in Section 5.3. (It is worth noting that the chlorination reaction can also be carried out using Cl_2 gas in a Schlenk line[2] which has been demonstrated to result in less pitting of the Si surface[41].) The PCl_5 method was used here primarily because of convenience; however, it is worth noting that the PCl_5 method is compatible with batch-manufacturing protocols making this reaction protocol more relevant for technical applications.

The wafers were removed from the PCl_5 solution, rinsed with tetrahydrofuran (THF) followed by CH_3OH, and dried under N_2. The chlorine-terminated surfaces were methylated by refluxing in 3.0 M CH_3MgCl in THF (Aldrich) for 2.5–3 hours at 70–80º C. After the reaction, the wafers were rinsed in THF followed by CH_3OH, dried under N_2, and removed from the glovebox. The samples were additionally sonicated for 5 minutes in CH_3OH, followed by CH_3CN to remove any Mg from the methyl-Grignard reagent.

5.2.4 Making electrical contact to methyl-passivated devices

Electrical contacts to Hall bar structures had to be deposited following the methylation reaction since typical contact metals react with the various wet-chemical procedures (NH_4F, PCl_5, and CH_3MgCl). This constraint can be alleviated by masking the metal contacts with Si_2N_3 (which is not etched in NH_4F) before the functionalization reaction; however, as I will show in the next section this is not required since the methyl monolayer is robust to the microelectronic fabrication protocols used here.

Positive-tone photoresists such as AZ-5214 result in significant carbon contamination[18] of the CH_3–Si(111) surface, is difficult to remove without using harsh treatments (such as acidic piranha), that, as will be shown below, oxidize the CH_3–passivated surface. Thus, the surface was protected by spin-coating it with a layer of either 3% poly-methyl methacrylate (PMMA) or 5.5% methyl methacrylate (MMA) before spin-coating the photoresist on top. An optical mask was used to expose the contact electrode pattern followed by development in AZ-400k. To obtain good electrical contacts, the methyl-passivation and the PMMA or MMA layer protecting the methyl

surface (which is not removed during the basic AZ-400k development) had to be removed before depositing contacting metals. This was accomplished by an aggressive O_2 plasma etch (4 min, 20 mTorr, 100 W) followed by a five-second dip in undiluted BOE. Contact angle measurements on similarly processed methyl-passivated wafers were performed before and after this treatment to confirm removal of the organic layer as shown in the table below. Note that the surface was allowed to sit in air for a couple of hours to oxidize after the BOE step. Rapid re-growth of surface oxide confirmed removal of the methyl monolayer.

Treatment on CH_3-Si(111) surface	Water contact angle
Before O_2 + BOE	70 ± 3°
After O_2 + BOE + sitting in air	32 ± 3°

Following the O_2 + BOE step, the wafer was immediately loaded into an electron-beam metal evaporator and a tri-layer stack of Ti/Pt/Au (10 nm/10 nm/150 nm) was deposited at rates of 0.25 Å s^{-1}, 0.25 Å s^{-1}, and 1 Å s^{-1}, respectively. The temperature was monitored during the metal deposition on a separate Si(111) surface using a thermocouple lead in contact with the wafer surface. The highest recorded temperature was ~30° C and occurred during the Pt deposition. The capping Au layer was deposited to facilitate (Au) wire bonding in a subsequent step. The Pt layer was required to prevent Au from diffusing into the Si during a subsequent contact anneal, which was observed to result in a significant reduction of the device conductivity (note that Au impurities in Si introduce efficient mid-bandgap R-G centers[19]).

Lift-off was accomplished in acetone with brief sonication. After lift-off, the wafer was immersed in fresh acetone, sonicated for 5 minutes, and allowed to soak for ~20 minutes at 50° C. To gently remove excess organic residue, the wafer was soaked for over an hour in anisole heated to 150° C. The wafer was then annealed for 5 minutes at 425° C under a N_2 ambient to promote ohmic contact formation. Before proceeding, room temperature current-voltage (*I–V*) scans were performed to confirm the quality of the device contacts. Last, the chip was protected with a thick spin-coated layer of PMMA and cleaved to separate the four wired-up Hall bar patterns and the large 2-mm square. The PMMA was removed from the five (now individual) pieces by sonication in acetone followed by soaking in 150° C anisole. Note that the diagnostic 2-mm square underwent the exact same treatment as the Hall bar devices (*i.e.*, lithography → methylation → more lithography → cleaning and separation).

At this point, the 2-mm square surface was characterized via x-ray photoelectron spectroscopy to (1) confirm complete surface passivation and (2) check for gross carbon contamination following the device fabrication work-up. If the surface was contaminated (from photoresist or CF_4 plasma etch residue), more aggressive cleaning procedures were used, such as Aleg-310 positive photoresist/residue stripper (n-methyl-2-pyrrolidone, amine, and catechol in solvent; 55° C, 10–20 min) (Mallinckrodt Baker, Phillipsburg, NJ) or 1:1:5 $NH_4OH:H_2O_2:H_2O$ (75° C, 10 min). Note that adventitious carbon was always present due to solvent, wafer handling, etc.

5.3 Spectroscopic characterization of methyl-passivated SOI devices

5.3.1 Measurement description

X-ray photoelectron spectroscopy (XPS) data were collected at room temperature in a UHV (10^{-9}–10^{-10} Torr) chamber described in detail elsewhere[2, 42]. X-rays from an Al Kα line at energy $h\nu$ = 1486.6 eV were incident to the wafer surface at 35° from the surface plane. Ejected photoelectrons were collected with a hemispherical electron energy analyzer at a take-off angle of 35° from the sample surface. Data was collected using M-probe ESCA Software version S-Probe 1.36.00. Survey scans were always taken in the energy range 0–1000 BeV (binding electron volts, or, $h\nu$ minus the photoelectron energy) to confirm the presence of only Si, C, and O (except possibly Mg from the methyl-Grignard reaction). High-resolution XP spectra of the Si 2p region from approximately 97–106 BeV were used to identify any surface oxidation as indicated by the formation of a broad SiO_x peak at ~103.4 BeV. Additionally, high-resolution scans of the C 1s region from approximately 282–289 BeV were used to identify direct C–Si bonding, if possible (dependent on the amount of adventitious carbon adsorbed to the surface). All peak fitting was done using the M-probe software. Si 2p fitting employed a 95% Gaussian and 5% Lorentzian line shape, with a 15% asymmetry. The $2p_{1/2}$ and $2p_{3/2}$ peak separation was fixed at 0.6 eV with a $2p_{1/2}$:$2p_{3/2}$ area ratio of 0.51[2, 42]. C 1s peaks were roughly fit by manually specifying the approximate peak positions and allowing the software to freely adjust all remaining parameters.

For chips used to fabricate Hall bar structures, XP spectra were collected from the photolithographically-defined 2-mm square described above. Before each scan, the x-ray spot was centered in the 2-mm square. This was made possible through the use of a fluorescent screen to identify the location of the x-ray spot relative to the square. Once the spot was located, the sample stage was translated accordingly.

5.3.2 Surface characterization data

Figure 5-5 shows a representative AFM image of a ~40-nm bonded Si(111) SOI epilayer ($n = 1\times10^{19}$ cm^{-3}) that was etched for 15 minutes in de-oxygenated NH_4F at room temperature, and Figure 5-5 shows XPS data from this surface immediately after functionalization, and after 108 hours of air exposure. The AFM image of Figure 5-5 shows triangular etch pits pointing in the $[11\bar{2}]$ direction[43] can be resolved and used to assign lattice directions as shown. The terrace width was measured to be ≈ 20 nm. For very thin (≤ 30 nm) Si devices on top of a 1–2 μm supporting SiO_2 layer, 15 minutes of NH_4F etching frequently resulted in severe thinning of the device, despite NH_4F being a very slow Si(111)

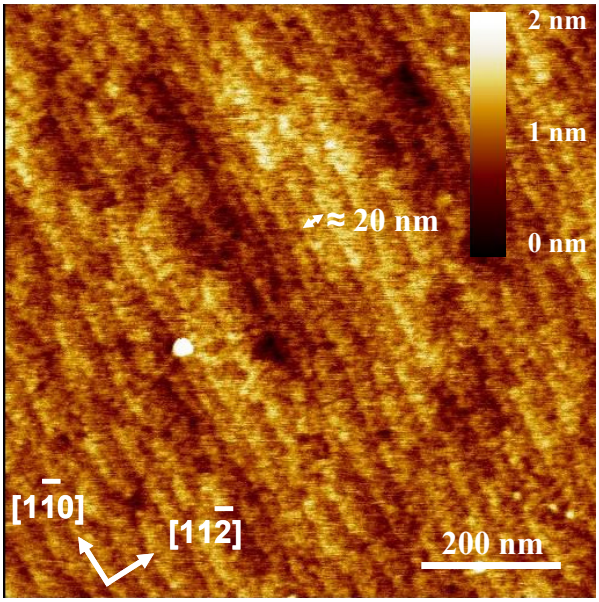

Figure 5-5. Atomic force microscopy (AFM) image of a 40-nm Si(111) epilayer etched in NH_4F.

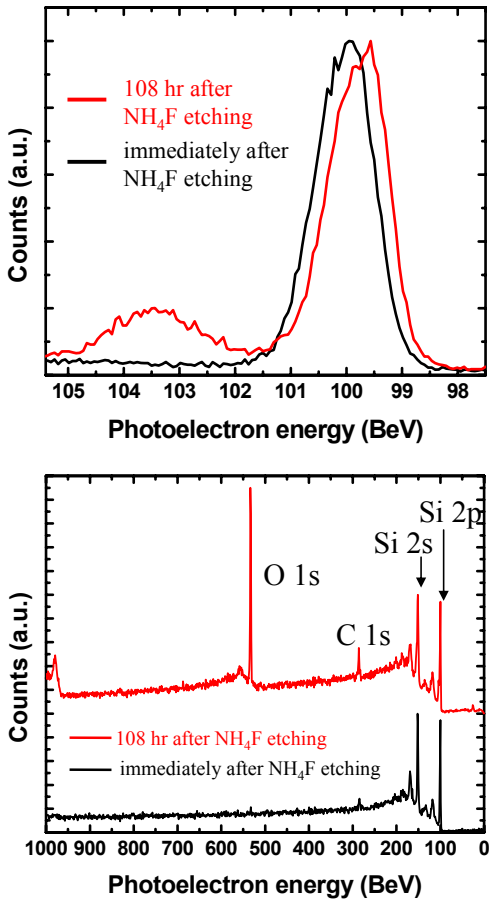

Figure 5-6 XP spectra of an H-terminated silicon epilayer. (Top) Si 2p region immediately after (black) and 108 hr after (red) NH_4F etching. Note the dramatic re-growth of surface oxide. (Bottom) Survey scans showing the presence of only O, C, and Si. The satellite peaks at lower binding energy to the Si 2s and 2p peaks are due to surface plasmon excitation. The peak at 970 BeV is characteristic of oxygen $K_1L_{23}L_{23}$ Auger emission.

etchant (etch rate ≈ 2 Å/min)[44]. A possible explanation for the enhanced etch rate may be excess dissolved oxygen in the NH_4F solution originating from the SOI SiO_2 layer. Transport of O_2 to the reactive, bare Si surface would result in rapid oxidation, followed by subsequent etching by F^- in the solution[45, 46]. Additionally, the presence of dissolved O_2 in the NH_4F solution may cause roughening of Si(111) surfaces[45], the extent of which requires further study using STM measurements. Nevertheless, a five-second 1:10 BOE:H_2O dip to remove the native oxide followed by a 4–5 minute NH_4F etch resulted in complete hydrogen termination, and robust methyl passivation of SOI surfaces was obtained with the chlorination/methylation steps described above.

To ascertain the quality of this passivation, high-resolution XP spectra of the Si 2p region were taken as a function of exposure time to air, and oxidation-resistance was taken as the figure of merit. The results of this study are presented in Figures 5-7.A and 5-7.B. Methyl-passivated SOI surfaces showed little re-growth of surface oxide, even after 108 hours (4.5 days) of exposure to ambient

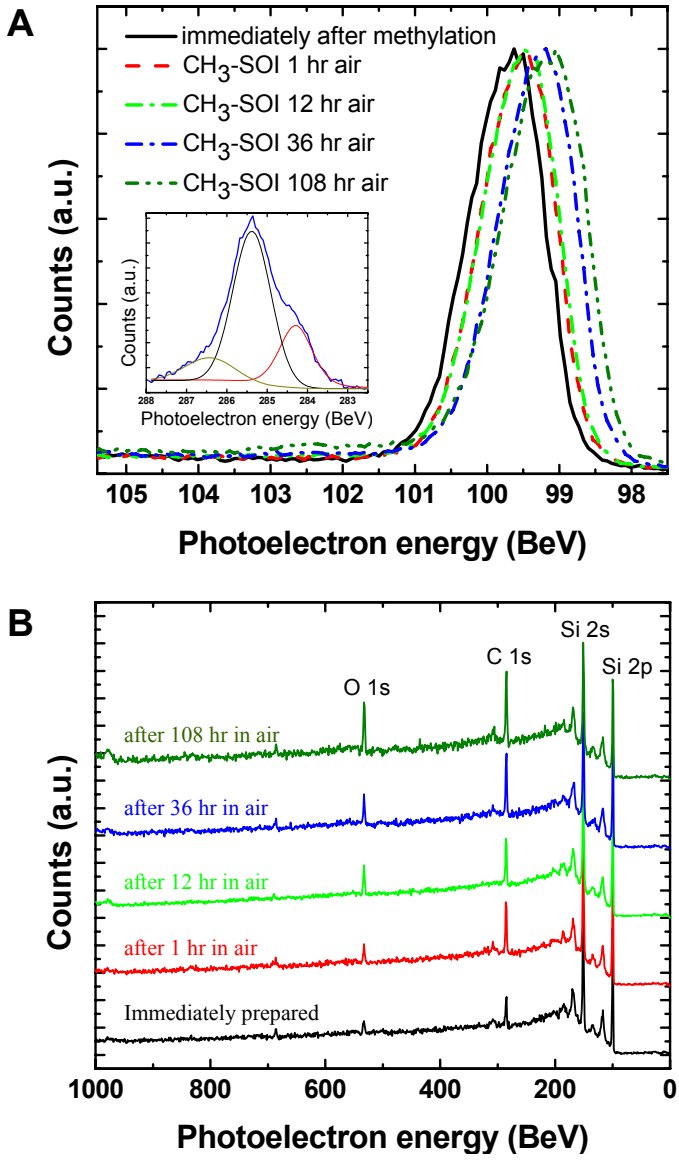

Figure 5-7. XP spectra of a 30 nm methyl-terminated SOI surface as a function of time in air. A. High-resolution scans of the Si 2p region showing very little oxidation after 108 hours in air. The noticeable shifting of the Si 2p peak to lower binding energy as a function of time may or may not be physical. This shift is seen in reported XPS data from the same instrument[2], but not for a different instrument[4]. If physical, the mechanism may be due to surface band bending and surface dipole effects[5] caused by the slow oxidation of unpassivated regions[4]. Inset. High-resolution scan of the C 1s region. Direct C–Si bonding is evidenced by the presence a side-peak shifted from the C 1s peak by 1.1 BeV to lower binding energy. **B.** Survey scans from 0–1000 BeV confirm only C, O, and Si. The growth of the O 1s peak is primarily due to adsorbed H_2O or adventitious C. This is verified by the Si 2p scan in **A**, which shows no significant surface oxidation.

air. Furthermore, follow-up XP scans on these surfaces after many months showed no significant further oxidation (not shown). This is in contrast to the H-terminated SOI surface shown in Figure 5-6, where surface oxidation is clearly evident by the presence of a broad peak at 103.4 BeV (due to formation of Si^{+}, Si^{2+}, Si^{2+} and Si^{4+} [4] species). The data of Figure 5-7.A does reveal some surface oxidation after 108 hours of air exposure, which is also observed with methylated bulk wafers. Recent work by Webb *et al*. has found this to result from the slow oxidation of isolated, inhomogeneous patches on the Si(111) surface[4]. Significantly, this study also found that slight oxidation of alkylated surfaces after prolonged air exposure resulted in no noticeable degradation of the surface's remarkable electronic properties.

The inset of Figure 5-7.A shows a high-resolution scan of the C 1s region. Although partially obscured by a ubiquitous aliphatic C 1s peak at 285.4 BeV, a shifted C 1s peak can be seen at 284.3 BeV. This shift to lower binding energy is due to direct C–Si bonding, and results from the carbon atom being negatively charged in its bond polarity, as expected from the electronegativities of C and Si (2.55 and 1.90, respectively)[5, 34].

For application to nanoelectronics, methyl-passivated SOI devices must be resistant to common microelectronic fabrication protocols and chemicals. To that end, 2-mm-square CH_3–Si(111) surfaces on SiO_2 were subjected to a host of fabrication chemicals, lithography procedures, and metal-deposition steps. XP spectra were collected before and after such treatments with re-growth of surface oxide once again taken as the figure of merit. As expected, immersion in a wide variety of solvents[47] heated to their boiling point (for 20–30 min) did not affect the passivation by any discernable amount.

Additionally, photolithography and metal deposition procedures* employing common positive-tone photoresists such as AZ-5214 (Clariant) and S-1813 (Shipley), and electron-beam lithography using PMMA did not result in appreciable oxidation of CH_3-SOI surfaces. An XP spectrum of the Si 2p region following photolithography and metal deposition (and lift-off in acetone) is shown in Figure 5-8.A for both a methyl-passivated (black trace) and untreated surface (red trace).

As expected, Figure 5-8.B (black trace) shows that one minute of diluted piranha-clean (2:1:10 H_2SO_4:H_2O_2:H_2O, ~ 100° C) resulted in oxidation of the methylated SOI surface, albeit to a significantly lesser extent than for an untreated Si surface (red trace). Aqua Regia (2:1 HCl:HNO_3, 1 min, ~100° C) treatment also resulted in significant oxidation (Figure 5-8.C). On the other hand, Figure 5-8.D shows that the popular RCA-I cleaning step (1:1:5 NH_4OH:H_2O_2:H_2O, 75° C, 10 min) did not result in appreciable oxidation of the CH_3-SOI surface. Methylated SOI was also resistant to oxidation from Aleg-310, a common photoresist stripper (n-methyl-2-pyrrolidone, amine, and catechol in solvent; 55° C, 10 min) (Figure 5-8.E).

Lithographic procedures frequently resulted in significant contamination of CH_3-SOI surfaces after metal lift-off in acetone. The signature of carbon contamination from photoresist was the presence of a shifted C 1s peak to ~ 290 BeV from the aliphatic carbon peak at 284.5 BeV, attributed to the presence of ester-bonded C atoms in photoresists and PMMA. This is clearly seen in the C 1s XP spectrum shown in Figure 5-8.F (top panel). Prolonged immersion (~1 hour) in anisole at 150° C significantly improved the surface in most cases (Figure 5-8.F, middle panel), but occasionally more-

* Note that, as described above, methyl-terminated surfaces do not come into contact with developers except where photo- or e-beam-resists are exposed.

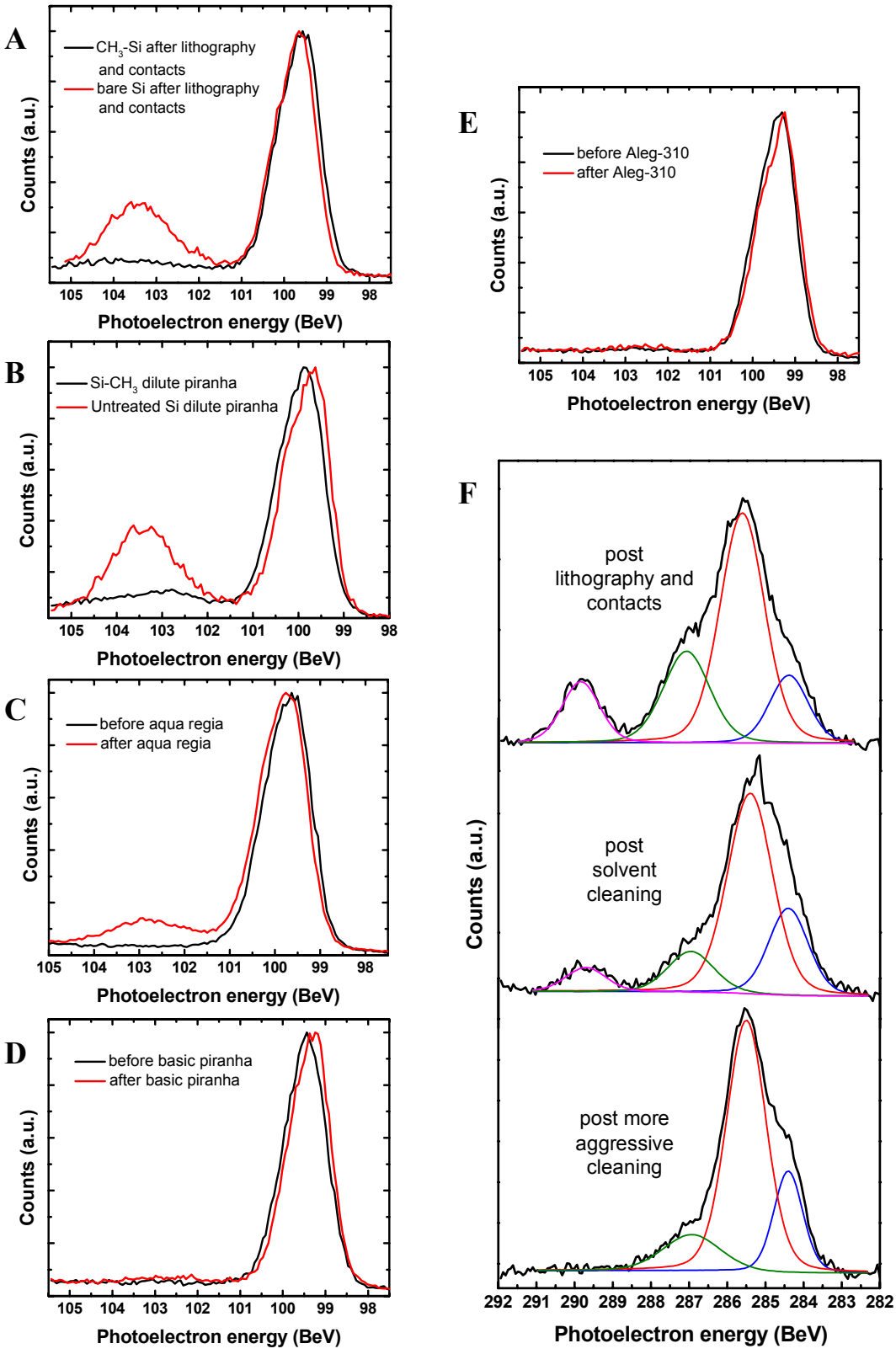

Figure 5-8. High-resolution XP spectra of Si 2p (A-E) and C 1s (F) regions from ~20-30 –nm-thick CH_3-SOI surfaces after various chemical treatments described in the text.

aggressive cleaning techniques were needed such as treatment with either RCA-I (basic piranha) or Aleg-310 (Figure 5-8.F, bottom panel).

The data in Figures 5-8.A–F show that CH_3-terminated SOI surfaces are resistant to oxidation from common micro/nanofabrication chemicals and lithographic protocols, and that devices fabricated from such surfaces should retain the excellent electrical properties of a CH_3-terminated surface.

5.4 Electrical characterization of methyl-passivated SOI devices

The previous section showed that methyl-passivated ultra-thin SOI devices remained passivated with little surface oxidation after complete microelectronic device fabrication. The studies described in this section aimed to directly measure the electronic transport parameters in such devices using variable-temperature magneto-transport measurements. By measuring electrical transport parameters, such as mobility at various temperatures, insight can be gained into the constituent scattering mechanisms.

5.4.1 Introduction to low-field Hall measurements

Measurements of the magnetoresistivity tensor in a weak magnetic field is a basic material characterization technique that enables the measurement of the Hall mobility, μ, and carrier concentration, n, separately, as opposed to zero-field resistivity measurements that only determine the product of the two. To see this, consider an n-doped rectangular

thin-film with a magnetic field, B, perpendicular to the surface. At steady state, the average rate in which an electron loses momentum due to the scattering forces within a crystal lattice is equal to rate at which it is accelerated by the external field, or, in equation form:

$$\left\langle \frac{d\mathbf{p}}{dt} \right\rangle_{lattice} = \left\langle \frac{d\mathbf{p}}{dt} \right\rangle_{field} . \tag{i}$$

In the low-field, single-carrier Drude model[48], a velocity-independent average momentum relaxation time, τ_m (the mean time between scattering events), is defined such that equation (i) can be simplified to

$$\frac{m^* \mathbf{v}}{\tau_m} = e\mathbf{E} + \mathbf{v} \times \mathbf{B} , \tag{ii}$$

where $\mathbf{v}$ is the drift velocity and m^* the effective mass. Taking the electric field, $\mathbf{E}$, to be in the plane of the thin-film (the x-y plane), equation (ii) can be simplified to

$$\begin{pmatrix} m^*/e\tau_m & -B \\ B & m^*/e\tau_m \end{pmatrix} \begin{pmatrix} J_x/en \\ J_y/en \end{pmatrix} = \begin{pmatrix} E_x \\ E_y \end{pmatrix} , \tag{iii}$$

where $\mathbf{J} = e\,\mathbf{v}\,n$ is the in-plane current density per unit cross-sectional area (= film thickness, t, × Hall bar width, w). The conductivity is given by $\sigma = en\mu$ and the Hall mobility by $\mu = e\tau_m / m^*$; thus, equation (iii) can put into the form of the magnetoresistivity tensor, $\mathbf{E} = \vec{\rho} \cdot \mathbf{J}$, with

$$\vec{\rho} = \begin{pmatrix} \rho_{xx} & \rho_{xy} \\ \rho_{yx} & \rho_{yy} \end{pmatrix} = \begin{pmatrix} 1/\sigma & -\mu B/\sigma \\ \mu B/\sigma & 1/\sigma \end{pmatrix} \tag{iv}$$

or

$$\rho_{xx} = \rho_{yy} = 1/en\mu \qquad \text{and} \qquad \rho_{xy} = -\rho_{yx} = B/en\,. \tag{v}$$

Equations (v) show that the Drude model predicts a field-independent longitudinal resistivity and a transverse resistivity that increases linearly with the applied magnetic field.

An eight-contact Hall bar geometry, shown in Figure 5-9 (on page 166), was utilized for this study because it enabled two independent four-point longitudinal voltage measurements, V_x, and a transverse (Hall) voltage measurement, V_H, at the center of the Hall bar structure. The remaining two measurement arms were not used, but were nonetheless patterned to keep the Hall bar as symmetrical as possible. From these measurements and the known dimensions of the device, the magnetoresistivity tensor components of the thin film can be calculated. This in turn enables the calculation of the Hall mobility, μ (cm^2/V s), resistivity, ρ (Ω cm), and carrier concentration, n (cm^{-3}), from equations (v).

Experimentally, a low-frequency AC or DC current was driven through the Hall bar structure and the longitudinal voltage, V_x, and Hall voltage, V_H, were synchronously measured. This enabled the calculation of ρ_{xx} and ρ_{yx} from

$$\rho_{xx} = \frac{E_x}{J_x} = \frac{V_x}{I}\frac{w}{l}t \qquad \text{and} \qquad \rho_{yx} = \frac{E_y}{J_x} = \frac{V_H}{I}t\,, \tag{vi}$$

where l is the distance between the same-side voltage measurement arms in Figure 5-9 (page 166), and I is the current. From equations (v) and (vi), the Hall mobility and carrier density were calculated from

$$\mu = \frac{|R_H|}{\rho_{xx}} \qquad \text{and} \qquad n, p = \frac{1}{e|R_H|}; \quad R_H = \frac{t}{I}\frac{V_H}{B}\,, \tag{vii}$$

where R_H is the Hall factor (= E_y / IJ_x); which was calculated by suitably averaging V_H measurements at different field and current polarities (described in the next section). The mobility (and carrier concentration) measured using this technique is qualified with the word 'Hall' because it differs from the true mobility by a scattering factor, r. The absence of this factor in the derivation above is due to the assumption of a velocity-independent mean time between collisions, τ_m. In reality, τ_m depends on the scattering mechanism (ionized impurity, phonon, etc.), and must be averaged over energy in addition to time. Further considerations give $r = \langle \tau_m^2 \rangle / \langle \tau_m \rangle^2$ where $\langle \ldots \rangle$ denotes an average over energy[49]. Fortunately, the scattering factor is close to unity ($\approx$ 0.95–1.2)[49] for the doping levels considered herein and was ignored.

5.4.2 Measurement description

Following fabrication, the Hall bar structures described in Section 5.2 were wired-bonded to a Au/plastic chip carrier and loaded into a Quantum Design Magnetic Property Measurements System (MPMS) cryostat with temperature control from 1.5 K to 400 K, and field capability of –50,000 to +50,000 Oersted. Independent longitudinal voltage measurements at two different locations of the Hall bar shown in Figure 7-8 allowed the homogeneity of the sample to be checked by comparing the two calculated resistivity values. I generally found the two resistivity measurements to agree to within ±10 percent unless there were poor Si-metal contacts, in which case I discarded the sample. It is desirable to measure the Hall voltage in the center of the Hall bar structure, as shown in Figure 5-9, because the measurement is then as far as possible from the end contacts of

the Hall bar. The proximity of the Hall bar end contacts can cause shorting of the transverse voltage, which can lead to an underestimate of the Hall coefficient. Theoretical analysis shows that if the contacts are in the middle of the Hall bar sample, and the aspect ratio of Hall bar length to width is $l/w > 3$, then the error from the contacts will be less than one percent [50]. For all the Hall bar structures tested $l/w > 7$, thus edge contacting errors should be negligible. Perturbations to the current flow and electric field pattern caused by voltage contacts were also reduced by using monolithic contact arms and making metal-Si contact at the ends of the arms[51].

Two sets of three equally-spaced contacts lie on opposite sides of the Hall bar. The distance between contacting arms is 150 μm and the distance from an end contact to a Hall voltage probe is nominally 220 μm. The Hall bar is 800 μm long and 100 μm wide, although after making electrical contacts the Hall bar length is effectively reduced to 750 μm.

5.4.2.1 DC measurements

For most of the measurements described herein, the Hall voltage signal, V_H, was three orders of magnitude smaller than the longitudinal voltage signal, V_x. Furthermore, the Hall voltage was usually offset by 'misalignment' voltage[49]. The misalignment voltage is caused by a voltage gradient parallel to the excitation current flow and is usually present even in the absence of a field, and for perfectly aligned Hall voltage probes. However, this voltage is (to a good approximation) independent of field, and was cancelled by measuring the Hall voltage at opposite field polarities and subtracting the two measurements. Likewise, thermoelectric and smaller magnetothermal-electric voltages

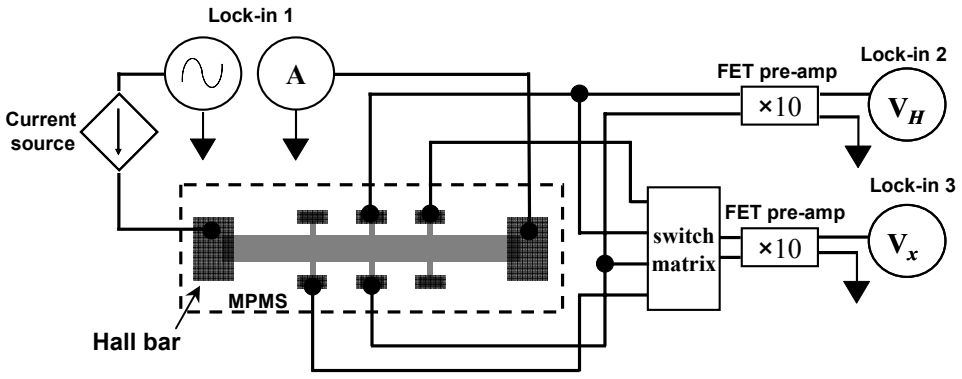

Figure 5-9. Hall measurement circuit. **For AC measurements**, an AC voltage output from Lock-in 1 (Stanford Research Systems SR-830 DSP) was used to control a current source consisting of either an operational amplifier operated in feedback or a precision resistor. For the resistor current source, the excitation current was monitored using the same lock-in. For an Op Amp current source, the excitation current was measured indirectly by using lock-in 1 to measure the voltage across a small precision resistor in series with the current (not shown). FET pre-amplifiers (100 MΩ) with a voltage gain of 10 amplified the voltage signals before they were measured by lock-in's 2 and 3. A switching matrix (Keithley 707A) was used to measure two longitudinal voltages with one pre-amplifier and lock-in. Note that the signal from V_H was much smaller than V_x, so an additional lock-in was dedicated for measuring V_H to avoid noise from the additional wiring of the switching matrix. **For DC measurements** lock-in 1 was replaced by a Keithley 2400 SourceMeasure unit and lock-in 3 was replaced by a Keithley 2182A Nanovoltmeter.

(Ettingshausen and Righi-Leduc effects)[52] were eliminated by reversing the current polarity and subtracting the measured Hall voltages. The resistivity was measured at zero-field on opposite sides on the bar and averaged. The equations for calculating transport parameters using the DC method are as follows:

Resistivity $$\rho_{1,2} = \frac{V_x(+I) - V_x(-I)}{2I}\frac{w \times t}{l} \quad , \qquad \rho_{avg} = \frac{\rho_1 + \rho_2}{2}$$

Hall factor $$R_H = \frac{\left(V_H(+B;+I) - V_H(+B;-I)\right) - \left(V_H(-B;+I) - V_H(-B;-I)\right)}{4I}\frac{t}{B}$$

Mobility $$\mu = \frac{|R_H|}{\rho_{avg}}$$

Carrier concentration $$n, p = \frac{1}{e|R_H|}$$

A constant current of 100 nA to 1 μA was used for DC measurements, and was adjusted with temperature to avoid sample heating and nonlinearities in the current-voltage response. (This was tested by doubling and/or halving the current and ensuring the voltage followed accordingly.) The applied magnetic field magnitude ranged from 3–5 T, depending on the Hall voltage signal level and the sourced current. (See Figure 5-9.)

5.4.2.2 AC measurements

DC measurements from samples doped below ~4×10^{18} cm^{-3} often became unreliable at lower temperatures due to decreased signal-to-noise from the need to use low current levels (which were required to avoid joule-heating of resistive samples[*]). Thus, many of the Hall measurements were made using low-frequency (≤ 13 Hz) and low current (1–10 nA) AC measurements with the measurement circuit shown in Figure 5-9. (The figure caption describes the electrical measurement in more detail.) The advantages of the AC technique for Hall measurements are: (1) Increased signal-to-noise via synchronous detection, and (2) elimination of thermal and magnetothermal voltage offsets. However, AC measurements create their own spurious effects, which are much more difficult to diagnose than are DC measurements, due to the involvement of phase. Accordingly, AC measurements were checked where possible with DC measurements. From 100 K to 400 K, AC measurements were found to differ from DC measurements in most cases by less than approximately five percent.

[*] Near this doping the Si:P alloy system undergoes a semiconductor-to-metal transition[49]

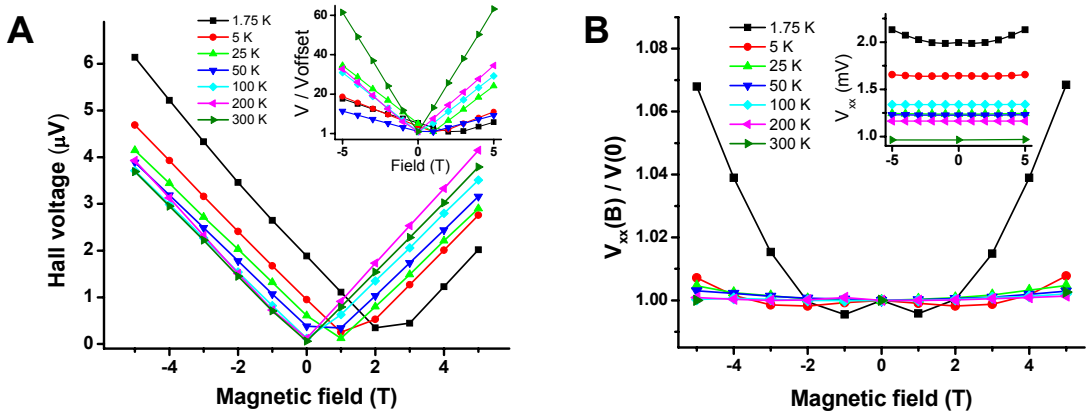

Figure 5-10. Hall and longitudinal voltages versus magnetic field from a 30-nm Hall bar. A. Hall voltage magnitude vs. field at various temperatures down to 1.75 K. The misalignment voltage is the residual voltage of the lowest point on the V_H vs. B plots and becomes smaller as the temperature increases and the device becomes less resistive. The inset shows the Hall voltage normalized by the offset voltage. **B**. Longitudinal voltage normalized by the zero-field value. The voltage is nearly independent of field down to ~5 K where characteristic B^2 behavior emerges due to departures from the single-carrier Drude model of magnetoresistance. Inset shows absolute voltage levels.

To eliminate the misalignment voltage, which is synchronous with the source current, V_H was calculated from the slope of V_H vs. B using two field points at each temperature. This eliminated the misalignment voltage as long as V_H was linear in B and the misalignment voltage was not field dependent. (This is also an implicit requirement for the validity of the single-carrier Drude model described above.) To that end, V_H and V_x vs. B scans were initially taken at a relatively small number of temperature points to establish the temperatures and field strengths where this is true. Figure 5-10 shows typical data down to 1.75 K.

Although a rather large field of 5 T was frequently used to increase the Hall voltage signal with respect to background (which was important for DC measurements), such fields were still within the low-field regime for the devices measured herein since

the measured mobilities were generally less than 300 cm^2/V-s, giving the low-field criterion* as $B < 1/\mu \approx 1/(300\ cm^2/V\text{-}s) \approx 30$ T.

5.4.3 Electrical characterization data

In this section, I will present preliminary data from methyl-passivated ultra-thin SOI devices. The majority of these devices are characterized by Si epilayers of approximately 10–25 nm thick. Figure 5-11 shows data from very highly doped ~20-nm thick CH_3-passivated SOI devices that were measured using DC techniques. This was possible because the samples were very highly-doped, resulting in metallic behavior down to 1.75 K. The observed metallic behavior is caused by the formation of phosphorus impurity banding, resulting in a vanishing dopant ionization energy[53, 54]. This behavior is clearly evident from the resistivity-vs.-temperature plot of Figure 5-11.A. (Although not shown, the measured carrier concentration displayed little temperature dependence, as expected.) The temperature dependence of the mobility shown in Figure 5-11.B is indicative of weak phonon scattering with a power-law temperature dependence, $\mu \sim T^s$, with temperature exponent $s = 0.34 \pm 0.03$ for the n-type CH_3 SOI device from 100–300 K, and $s = 0.24 \pm 0.04$ for the p-type CH_3 SOI device from 77–300.

For moderately-doped devices (approximately l–4×10^{18} cm^{-3}), the amount of time the device remained in the PCl_5 solution during the chlorination reaction was found to be an important parameter determining device mobility. This is most likely the result of

* The low-field criterion amounts to the requirement of non-closing cyclotron orbits. The frequency of a cyclotron orbit is $\omega_c = eB/m^*$, and an electron will be scattered before completing an orbit provided $\omega_c \langle \tau_m \rangle < 1$ radian, or $B < 1/\mu$.

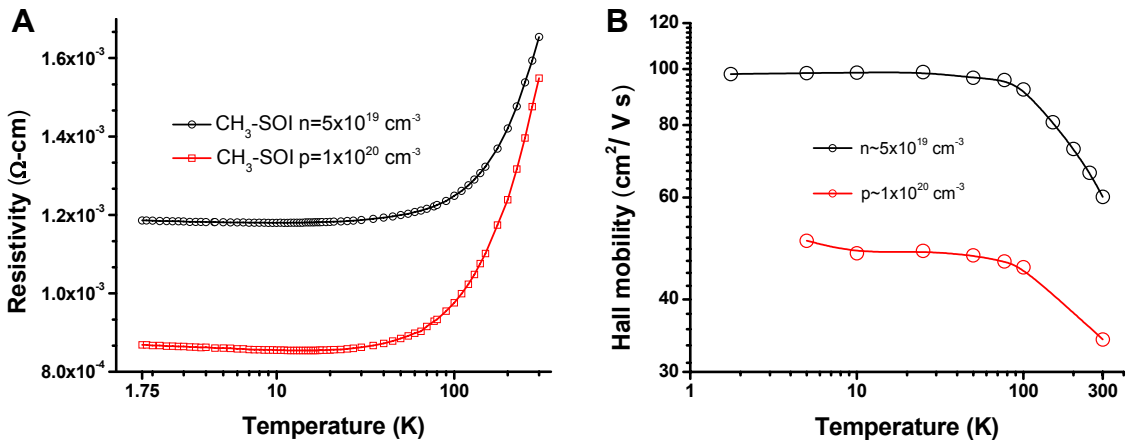

Figure 5-11 Resistivity and Hall mobility of highly-doped CH_3–SOI devices. **A**. Resistivity vs. temperature data showing clear metallic-like behavior due to high doping and impurity band formation. **B**. The mobility characteristics of n- and p-type CH_3 SOI devices indicating phonon scattering of charge carriers in impurity bands as the dominant scattering mechanism. As expected, the p-type doped sample mobility is roughly half the n-type sample mobility. Both devices were chlorinated via 30 minutes in PCl_5.

significant device thinning[1, 55] and etch-pit formation from the PCl_5 chlorination reaction, which is expected to have an enhanced effect on very thin epilayers, such as those studied here. This is in accord with recent work by Cao *et al.*[56], where STM measurements determined that wet-chemical chlorination of bulk Si(111) surfaces with PCl_5 resulted in significant etch-pit formation.

Supporting this hypothesis is the data of Figure 5-12, which displays the measured mobility of ~20-nm-thick CH_3-SOI devices as a function of PCl_5 chlorination time with the reaction temperature at ~90° C. Because the devices had different doping levels (from roughly $1–4\times10^{18}$ cm^{-3}), the measured mobility was normalized by the bulk mobility. The data suggests that short PCl_5 chlorination times are required to achieve good electrical properties from CH_3-terminated SOI devices using PCl_5 as the chlorination reagent. (Lower reaction temperatures and longer reaction times are expected to yield similar results). To verify that the surfaces used to obtain the data

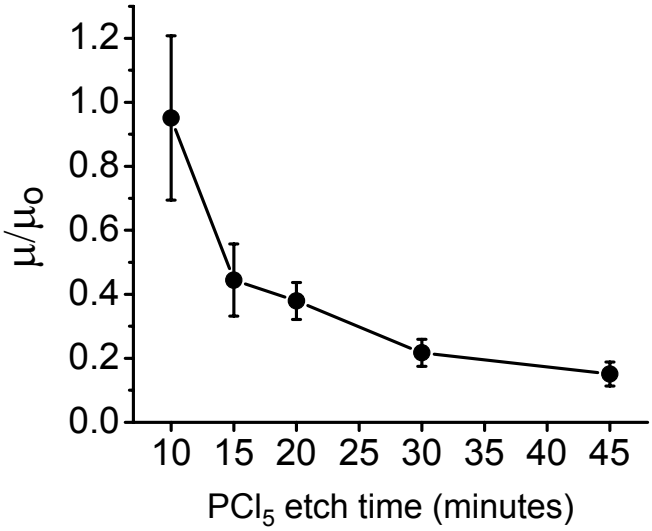

Figure 5-12. Normalized mobility as a function of PCl_5 chlorination time. The normalization constant, μ_o, is the bulk mobility for the device doping, which ranged from n=1–6×10^{18}. The uncertainty in these measurements is primarily due to uncertainty in the device thickness after functionalization, which in turn leads to uncertainty in the normalization factor. The PCl_5 reaction temperature was ~90° C.

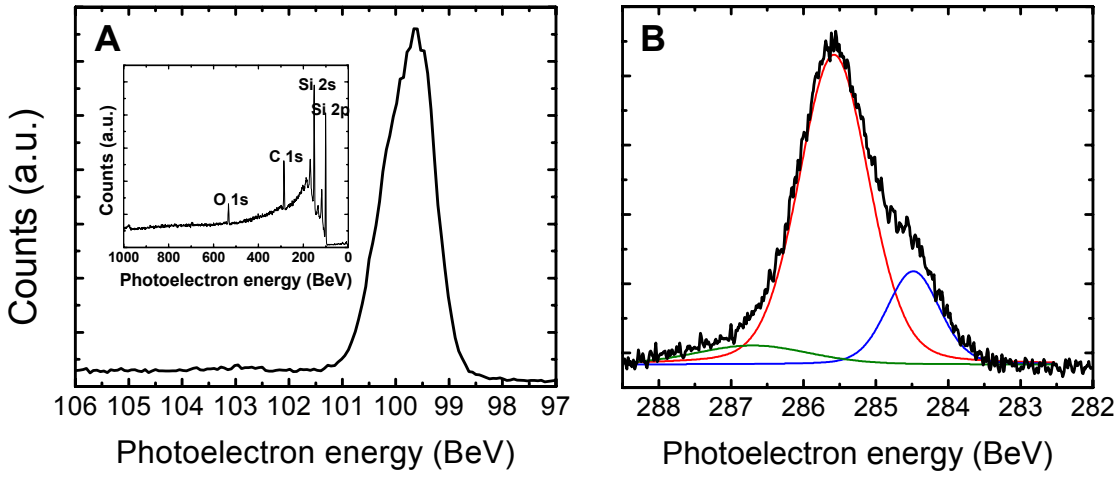

Figure 5-13. XP spectra of an approximately 20-nm-thick CH_3-SOI device chlorinated by a 10-minute immersion PCl_5. A. High-resolution scan of the Si 2p region showing little oxidation after ~24 hours of air exposure. Inset, survey scan showing only C, O, and Si. **B**. High-resolution scan of the C 1s region showing direct C–Si bonding evidenced by a chemical shift of the C 1s peak to lower binding energy (blue trace). The PCl_5 reaction temperature was ~90° C.

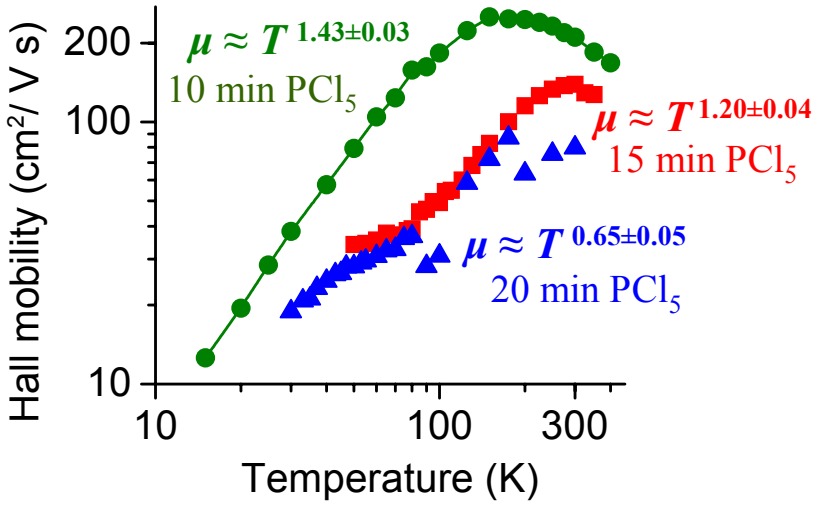

Figure 5-14. Hall mobility vs. temperature. Black circles: ~20 nm CH_3–SOI, n=2×10^{18} cm^{-3}, 10 min PCl_5. Red squares: ~20 nm CH_3–SOI, n=1×10^{18} cm^{-3}, 15 min PCl_5. Blue triangles: ~20 nm CH_3–SOI, n=2×10^{18} cm^{-3}, 20 min PCl_5.

shown in Figure 5-12 were methyl passivated, XP spectra were collected from the same chips on which the devices were fabricated. Figure 5-13 shows XP spectra from a device chlorinated from 10 minutes in PCl_5 at ~ 90° C.

Figure 5-14 shows the measured mobility vs. temperature characteristics from three moderately-doped devices (n = 1–2×10^{18} cm^{-3}) after 10, 15, and 20 minutes in PCl_5 solution at ~90° C. The data shows the mobility is dominated by lattice interactions, such as ionized impurity scattering at low temperature, and phonon scattering at high temperature, as expected for non-degenerately doped Si[19]. The device chlorinated with a ten-minute immersion in PCl_5 (black circles) displayed the highest mobility value (~210 cm^2/Vs at 300 K), which is slightly better than the bulk value for comparable doping. The low-temperature mobility of this device displays a temperature exponent of s = 1.43 ± 0.03 indicating that ionized impurity scattering (which theoretical considerations predict depends on temperature as $\mu \sim T^{3/2}$) is the dominant mobility reduction mechanism in

this device[57]. Thus, the mobility of this device displays bulk-like behavior, where ionized impurity scattering is the dominant contribution to the temperature dependence of the mobility * (at low temperature). The other two devices show lower temperature exponents: $s = 1.20 \pm 0.04$ (red squares, 15 min PCl_5) and $s = 0.65 \pm 0.05$ (blue triangles, 20 min PCl_5). This may be due to increased contributions from other scattering mechanisms, perhaps related to the surface, such as surface roughness scattering[14] due to increased etch pit density, and/or neutral impurity scattering. The latter has been observed to be important at low temperatures with a temperature exponent of $s = 0.5$ in bulk samples[57].

5.5 Concluding remarks

This chapter presented research directed towards chemically controlling the surface of Si(111)-on-insulator epilayers using a modified chlorination/methylation protocol. The surface characterization data is fairly complete, and shows that electronic devices with oxide-free surfaces can be prepared from ultra-thin SOI epilayers using standard microelectronic fabrication protocols. The electronic measurements suggest the various wet-chemical processing steps employed to alkylate the surface of thin-film devices

* The total mobility, μ_T, due to an assortment of independent scattering mechanisms, can be written as $1/\mu_T = \sum_s 1/\mu_s$, where $\mu_s \sim T^s$. Thus, the presence of surface scattering mechanisms (and/or other possible scattering mechanisms), each with a different temperature exponent, s, alters the measured temperature-dependence of the mobility from $\mu \sim T^{1.5}$ (the expected temperature-dependence for moderately-doped bulk devices).

should be used with caution to avoid degrading the overall electronic properties of the device.

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