Design and Characterization of Layered Tunnel Barriers for Nonvolatile Memory Applications

Thesis by

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This thesis is dedicated to my parents,
Lee and Susan Casperson
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-Julie Casperson
Abstract

The main limitations of all floating gate devices are the long program (~ $\mu$s) and erase times (~ 1 ms) inherent to charging floating gates using Fowler-Nordheim tunneling. An interesting alternative to the homogeneous dielectric tunnel barriers present in conventional floating gate devices is to use silicon compatible “layered” tunnel barrier heterostructures. The advantage of a multi-layer tunnel barrier is that the barrier height decreases with an applied voltage, greatly increasing the tunneling probability of electrons to the gate, while simultaneously exerting a large barrier to electron tunneling in the off state. The result would be short write/erase times and long retention times. This concept of integrating layered tunnel barriers into standard nonvolatile memory devices (Flash memory) is what motivates the work presented in this thesis.

To assess the performance of layered tunnel barriers, tunneling probability simulations for layered tunnel barriers were performed using an effective-mass model. By numerically integrating over all angles and energies, we naturally include a wide range of possible transport mechanisms such as thermionic emission, Fowler-Nordheim tunneling, and tunneling through the Schottky barrier of the silicon. Using this model we calculated the current-voltage (I-V) characteristics so that we can optimize the layered tunnel barrier structure. Based on the results of these simulations, we have correlated dielectric constants and band-offsets with respect to silicon in order to help identify possible materials from which to construct these layered barriers. This survey has allowed us to determine that some of the most promising high-k materials heterostructures are Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ and HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ and we have fabricated these structures.
We performed a series of physical and electrical characterization experiments on single-layer as well as two- and three-layer structures of Si$_3$N$_4$, Al$_2$O$_3$, and HfO$_2$. Transmission electron microscopy (TEM) was used to verify the thicknesses of the layers as well as the microstructure and effects of high-temperature annealing. I-V measurements determined the electrical ramifications of high-temperature annealing and other processing parameters. These experiments were useful in order to define the ideal processing conditions for optimal dielectric quality, with minimal interfacial layer growth. Using our effective mass model, we fit the experimental I-V results to determine the effective barrier heights and thicknesses of our films. However, due to a convolution in the effective mass model of these two parameters (barrier heights and film thicknesses), it was difficult to obtain quantitative barrier height measurements. A better method for determining the effective barrier heights (and to demonstrate barrier lowering behavior) was to construct Fowler-Nordheim plots from our data. By plotting the correct relationships between the electric field and tunneling currents in a given film, we were able to determine the symmetry of the barrier and confirm the existence of barrier lowering.

We have developed a bias-dependent internal photoemission technique for quantitative determination of the band-offsets between silicon and our dielectric barriers. By shining light from a tunable arc lamp onto our sample and by measuring the resulting photocurrent, we can extract an accurate value of the dielectric material conduction band-offset from silicon as a function of voltage applied across the high-k stack. The band-offsets show a strong dependence on applied bias, demonstrating the necessity to report applied voltages when measuring semiconductor/dielectric or metal/dielectric band-offsets. For SiO$_2$ (and other single-layer materials), image potential barrier lowering simulations
correctly predict the barrier profile as a function of voltage, allowing us to report the band-offsets for these materials in a more complete way than was previously possible.

The bias-dependent internal photoemission technique is also valuable for the demonstration of barrier lowering in dielectric heterostructures. By characterizing a number of multi-layer structures of HfO₂ and Al₂O₃, we have been able to measure the barrier height of these structures over a wide range of biases. Using an electrostatic model, we have analyzed this data and have been able to correctly simulate the barrier lowering results over all voltage ranges.

In order to capitalize on the barrier lowering behavior that we have confirmed using standard electrical characterization and bias-dependent internal photoemission measurements, we have done some preliminary measurements on metal-oxide-semiconductor (MOS) capacitors that integrate layered tunnel barriers. We have also outlined a complete procedure for the fabrication of transistors that incorporate a number of single-layer and multi-layer tunnel barriers for comparison of transistor performance. Additionally, we have introduced a new application for these layered dielectric stacks – a voltage-tunable photodetector that utilizes the barrier lowering behavior to act as a high-pass optical filter.
Table of Contents

Thesis Committee ............................................................................................................ ii

Acknowledgements ........................................................................................................ iii

Abstract .......................................................................................................................... xi

Table of Contents ............................................................................................................ xiv

List of Table and Figures ............................................................................................... xix

Chapter 1 Introduction .................................................................................................... 1

1.1 Overview of storage technology .............................................................................. 1

1.2 Nonvolatile memory ................................................................................................ 3

1.3 Basic physics of Flash memory .............................................................................. 4

1.4 Charge storage mechanism: tunneling ................................................................. 6

1.5 High-κ dielectrics ...................................................................................................... 7

1.6 Outline of thesis ........................................................................................................ 8

1.6.1 Layered tunnel barriers: simulation and materials identification ................... 9

1.6.2 Analysis of single-layer dielectrics: Bias-dependent internal photoemission and materials characterization ................................................................. 10

1.6.3 Optical and electrical characterization of layered dielectric barriers ................ 12

1.6.4 Device measurements and design ...................................................................... 13
3.4.1 Current-voltage measurements ........................................................... 49
  3.4.1.1 ALD HfO₂, Si₃N₄, and Al₂O₃ from Agere Systems ......................... 49
  3.4.1.2 Temperature dependence of I-V measurements ............................ 56
  3.4.1.3 I-V results for Harvard samples.................................................. 59
3.4.2 Internal photoemission ....................................................................... 60
  3.4.2.1 Theory of internal photoemission .................................................. 60
  3.4.2.2 Image potential barrier lowering theory ......................................... 63
  3.4.2.3 Experimental setup ..................................................................... 64
  3.4.2.4 Internal photoemission experiments for single-layer dielectrics ...... 65
    3.4.2.4.1 Photon energy vs. current for thermally grown SiO₂............... 65
    3.4.2.4.2 Extracting the band-offsets of SiO₂ – comparison of models....... 67
    3.4.2.4.3 Band-offset profile vs. photon energy for thermally grown SiO₂ 68
    3.4.2.4.4 Internal photoemission results for Agere samples............... 69
    3.4.2.4.5 Internal photoemission results for Harvard samples ............. 70
3.5 Conclusion .......................................................................................... 75

Chapter 4 Optical and electrical characterization of layered tunnel barriers
79

4.1 Introduction ......................................................................................... 79
4.2 Characterization of heterostructures by TEM ..................................... 80
  4.2.1 TEM analysis of Si₃N₄ / Al₂O₃ / Si₃N₄ from Agere ...................... 80
  4.2.2 TEM analysis of HfO₂ / Al₂O₃ / HfO₂ from Agere ............... 81
  4.2.3 TEM analysis of HfO₂ / Al₂O₃ / Si and Al₂O₃ / HfO₂ / Si from Harvard 82
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.3  Fowler-Nordheim analysis of layered barriers</td>
<td>83</td>
</tr>
<tr>
<td>4.3.1 Theory of Fowler-Nordheim tunneling</td>
<td>83</td>
</tr>
<tr>
<td>4.3.2 Fowler-Nordheim plots</td>
<td>85</td>
</tr>
<tr>
<td>4.3.2.1 Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ samples from Agere</td>
<td>86</td>
</tr>
<tr>
<td>4.3.2.2 HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ samples from Agere</td>
<td>90</td>
</tr>
<tr>
<td>4.3.2.3 Conclusions from I-V characterization</td>
<td>92</td>
</tr>
<tr>
<td>4.4  Internal photoemission analysis of layered barriers</td>
<td>93</td>
</tr>
<tr>
<td>4.4.1 Background</td>
<td>93</td>
</tr>
<tr>
<td>4.4.2 Analysis of HfO$_2$ and Al$_2$O$_3$ heterostructures from Harvard</td>
<td>93</td>
</tr>
<tr>
<td>4.4.2.1 HfO$_2$ / Al$_2$O$_3$ and Al$_2$O$_3$ / HfO$_2$ structures</td>
<td>93</td>
</tr>
<tr>
<td>4.4.2.1.1 Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si from Harvard</td>
<td>94</td>
</tr>
<tr>
<td>4.4.2.1.2 HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si from Harvard</td>
<td>98</td>
</tr>
<tr>
<td>4.4.2.1.3 Summary of two-layer samples from Harvard University</td>
<td>101</td>
</tr>
<tr>
<td>4.4.2.2 HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ and Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ structures</td>
<td>101</td>
</tr>
<tr>
<td>4.4.2.2.1 Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si from Harvard University</td>
<td>102</td>
</tr>
<tr>
<td>4.4.2.2.2 HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si from Harvard University</td>
<td>105</td>
</tr>
<tr>
<td>4.4.2.2.3 Summary of three-layer samples from Harvard University</td>
<td>107</td>
</tr>
<tr>
<td>4.4.3 Analysis of Si$_3$N$_4$ samples from Agere</td>
<td>108</td>
</tr>
<tr>
<td>4.5  Potential application: voltage tunable photodetector</td>
<td>110</td>
</tr>
<tr>
<td>4.6  Conclusion</td>
<td>111</td>
</tr>
</tbody>
</table>

Chapter 5 Conclusion

5.1 Layered tunnel barriers: simulation and materials identification
5.2 Analysis of single-layer dielectrics: Bias-dependent internal photoemission and materials characterization .......................................................... 117

5.3 Optical and electrical characterization of layered dielectric barriers ...... 119

5.4 Device measurements and design ........................................................................ 120

5.5 Future steps to be taken .................................................................................. 120

Appendix A Device measurements and design.................................................. 121

A.1 Introduction ........................................................................................................ 121

A.2 Fabrication and design of MOS transistors from Agere samples.......... 121
    A.2.1 Description of gate stack ........................................................................... 121
    A.2.2 Materials processing details ...................................................................... 122

A.3 Device characterization .................................................................................... 123
    A.3.1 MOS capacitor measurements: SiO₂ tunnel oxide ................................. 124
    A.3.2 MOS capacitor measurements: HfO₂ / Al₂O₃ / HfO₂ tunnel oxide 129

A.3.3 MOS capacitor result summary .................................................................. 133

A.4 ALD HfO₂ and Al₂O₃ gate stacks to be fabricated at IBM ..................... 133
    A.4.1 Description of samples obtained from IBM ............................................ 133
    A.4.2 Transistor design for IBM samples .......................................................... 137
    A.4.3 Mask design details .................................................................................. 139

A.5 Conclusion ........................................................................................................ 141
List of Table and Figures

Chapter 1

Table 1.1. Summary of important memory technologies throughout history. Adapted by permission of John Wiley & Sons. .................................................................1

Figure 1.1 (color). Schematic representation of a floating gate memory. When a voltage is applied to the control gate and a bias between the source (S) and drain (D), the channel opens to let a current flow. Some electrons also tunnel through the tunnel barrier and are stored on the silicon floating gate. ........................................4

Figure 1.2 (color). Influence of charge in the gate dielectric on the threshold of a p-channel transistor. ..........................................................5

Chapter 2

Figure 2.1. Schematic representation of a floating gate memory. When a voltage is applied to the control gate and a bias between the source (S) and drain (D), the channel opens to let a current flow. Some electrons also tunnel through the tunnel barrier and are stored on the silicon floating gate. The threshold voltage gives a measure of the amount of charge stored. Parts (a), (b), and (c) show conduction band edge diagrams of various types of tunnel barriers: (a) a typical uniform barrier; (b) idealized crested symmetric barrier; (c) three-layer structure. Dotted lines show the barrier tilting caused by applied voltage $V$. Part (d) illustrates the three-layer capacitor structure that is referred to in (c). The left-hand electrode is silicon and the right-hand electrode is a metal contact and dielectric constants $\varepsilon$, electric fields $E$, and applied voltage $V$ are indicated. Through calculation, it is found that the amount of charge trapped in the triangular well that is formed at the interface of layer 1 and 2 is negligible. .......................................................17

Table 2.1. Values for dielectric constant, band gap, conduction and valence band-offsets for various dielectric materials. .................................................................24

Figure 2.2. Shows the relationship between the dielectric constant and band-offset from Si for various materials. The upper panel shows the conduction band-offsets and the lower panel shows the valence band-offsets. They are separated by a silicon band gap of 1.1 eV. Squares indicate theoretical band-offset values and triangles indicate experimental band-offset values. The dielectric constants given are from recent journal articles and vary slightly according to deposition method or other factors. The values used in this figure are indicated by an asterisk in Table 2.1. ...26
Figure 2.3. Tunneling current per unit energy (A / cm² / eV) as a function of $E_x - E_F$ (eV). The solid line in part (a) is for a 4 nm square barrier and the dotted line indicates a 3 eV, 15 nm square barrier at a bias of 0.1 V. Part (b) shows the analogous situation for a bias of 2.0 V, while part (c) shows the transport of electrons through three different three-layer tunnel barriers at 2.0 V as well. The solid curve indicates Si₃N₄ / Al₂O₃ / Si₃N₄. The dotted curve indicates ZrSiOₓ / Al₂O₃ / ZrSiOₓ. The dashed curve indicates an ‘ideal structure’ with barrier heights 1.0 / 3.0 / 1.0 eV and dielectric constants 7.5 / 9.0 / 7.5. The thickness of each individual dielectric layer is 6 nm. Part (d) shows the analogous cases for the tunneling of holes at 2.0 V.

Figure 2.4 (color). Simulated current-voltage (I-V) curves for various tunnel barriers. The black line shows an I-V curve for a continuously graded triangular barrier (2.5 eV band-offset and 20 nm thick). The pink line represents a theoretical five-layer structure with band-offsets of 1.0 / 1.6 / 2.5 / 1.6 / 1.0 eV and 4 nm individual thicknesses. The blue line is a theoretical three-layer structure with band-offsets 1.4 / 2.5 / 1.4 eV and thicknesses 7 / 5 / 7 nm. The red line represents a square barrier with a 2.5 eV band-offset that is 8 nm thick.

Figure 2.5 (color). Simulated I-V curves for structures of Al₂O₃ and Si₃N₄. Part (a) shows I-V curves for electrons, where the solid curve shows tunneling through 6 nm Al₂O₃, the dotted curve is for Si₃N₄ / Al₂O₃ / Si₃N₄ (6 nm each), the dashed curve is for ZrSiOₓ / Al₂O₃ / ZrSiOₓ (6 nm each), and the curve with squares is for 9 nm Al₂O₃. Part (b) shows I-V curves for holes, where the solid curve is for 6 nm Al₂O₃, the dotted curve is for Si₃N₄ / Al₂O₃ / Si₃N₄ (6 nm each), the dashed curve is for ZrSiOₓ / Al₂O₃ / ZrSiOₓ (3 nm each), and the curve with squares is for 7.7 nm Al₂O₃.

Figure 2.6 (color). Conduction band diagram showing nonidealities for transport through of Metal / Si₃N₄ / Al₂O₃ / Si₃N₄ / n-Si.

Chapter 3

Table 3.1. First batch of Agere samples (Si₃N₄ and Al₂O₃).

Table 3.2. Second batch of Agere samples (HfO₂ and Al₂O₃).

Figure 3.1 (color). Band-structure schematics for three-layer structures. (a) shows Si / Si₃N₄ / Al₂O₃ / Si₃N₄ / metal and (b) shows Si / HfO₂ / Al₂O₃ / HfO₂ / metal. The conduction band-offsets (electron barriers) are indicated by $\Delta CB$ and the valence band-offsets (hole barriers) are indicated by $\Delta VB$. 
Figure 3.2. TEM images of nominally 6 nm CVD Si$_3$N$_4$ from Agere. (a) the film before any annealing steps are taken. (b) the Si$_3$N$_4$ after a 15 minute anneal in Ar + 2000 ppm O$_2$ at 1000°C.

Figure 3.3. Thin ALD Al$_2$O$_3$ film from Agere before any annealing steps. Nominally 6 nm film is found to be amorphous and 6.2 nm thick with no interfacial layer. Silicon substrate is somewhat rough.

Figure 3.4. Thin Al$_2$O$_3$ films (~6 nm) after annealing steps have been taken. (a) shows the film after a 15 minute, 600°C in Ar + 2000 ppm O$_2$. The film appears to have increased slightly in thickness to 6.7 nm, and has a very thin visible interfacial layer (~1 nm). The film appears to have remained amorphous. (b) shows the Al$_2$O$_3$ film after a similar anneal at 1000°C. The film has developed a thick interfacial layer (~3.4 nm). The film has not become crystalline, but appears to have developed striated layers. Both samples have a 500 Å Al cap layer.

Figure 3.5. Unannealed HfO$_2$ sample from Agere. The silicon / HfO$_2$ interface is found to be rather rough. The sample is semi-crystalline and ranges from 5.6 – 6.5 nm thick. A possible interfacial layer is < 3 nm thick.

Figure 3.6. Annealed ~6 nm HfO$_2$ films from Agere. (a) shows the film after a 15 minute, 600°C in Ar + 2000 ppm O$_2$. The film appears to have increased slightly in thickness to 6.5 nm, become more crystalline, and has a visible interfacial layer. (b) shows the HfO$_2$ film after a similar anneal at 1000°C. The film has changed dramatically, becoming polycrystalline, more uneven, and having grown a thick interfacial layer (~4 nm). It is possible that this “interfacial layer” is due to differential milling due to the large difference in Z for Hf and Si. Both samples had a 500 Å Al cap layer.

Figure 3.7. TEM images of single-dielectric layers from Harvard. (a) shows a nominally 15 nm Al$_2$O$_3$ film to be continuous, amorphous, and 15.7 nm thick. A thin interfacial layer can be seen and measures 2.2 nm thick. (b) shows a nominally 15 nm HfO$_2$ film to be slightly discontinuous, somewhat crystalline, and 16.7 nm thick. A 2.2 nm interfacial layer is observed. Each sample was annealed in Ar + 2000 ppm O$_2$ for 35 minutes at 600°C.

Figure 3.8 (color). Electrical characterization of 6 nm CVD Si$_3$N$_4$ from Agere. (a) shows I-V curves after various annealing temperatures. Anneals were done in N$_2$ / 10% H$_2$ for 30 min. (b) shows C-V curves for the film with an anneal at 850°C in Ar + 2000 ppm O$_2$ for 15 min.
Figure 3.9 (color). I-V data for 6 nm Si₃N₄ (blue curve) with effect mass model fit (red curve). Annealing conditions were 400°C in N₂ / 10% H₂ for 30 min. The best fit to the data was found to correspond to a 4.2 eV barrier that is 4.3 nm thick. ..........51

Figure 3.10 (color). Electrical characterization of 6 nm ALD Al₂O₃ from Agere. (a) shows I-V curves at various annealing temperatures. Anneals were done in Ar + 2000 ppm O₂ for 30 min. (b) shows C-V curves for the film with an anneal at 850°C in Ar + 2000 ppm O₂ for 15 min. ........................................52

Figure 3.11 (color). Annealing of 6 nm ALD Al₂O₃ from Agere at different annealing conditions. The black solid curve shows a film that has been annealed for 15 minutes at 850°C in Ar + 2000 ppm O₂. The red dashed curve shows a film that has been annealed at annealed for 15 minutes at 850°C in Ar + 2000 ppm O₂ with a subsequent anneal for 15 minutes at 1000°C in N₂. .................................53

Figure 3.12 (color). (a) I-V characterization and simulation of 6 nm ALD Al₂O₃. This film was annealed for 15 minutes at 700°C in Ar + 2000 ppm O₂ with a subsequent anneal for 15 minutes at 1000°C in N₂. The best fit to this data corresponds to a simulated two-layer barrier of 6.6 eV that is 2 nm thick on a barrier that is 2.9 eV and 2 nm thick as is shown schematically in (b) under both negative and positive bias. .................................................................54

Figure 3.13 (color). I-V characterization and simulation for 6 nm HfO₂. The film was annealed at various temperatures in Ar + 2000 ppm O₂ for 15 minutes as can be seen by the dotted lines. Simulated curves are shown by the solid lines and represent a barrier that is 2.5 eV tall and 3.7 nm thick and one that is 4.0 eV and 3.0 nm thick. .................................................................55

Figure 3.14. Plot of temperature vs. current density for Si₃N₄. Three distinct regions of transport can be seen. From Ref. 3.5. Reprinted by permission of S. M. Sze and the American Institute of Physics. .................................................................57

Figure 3.15 (color). I-V curves of ALD films from Agere at room temperature and 77 K. (a) shows the result for 6 nm Al₂O₃. (b) shows the result for 4 nm Si₃N₄. No significant difference (or suppression) in transport is observed. ....................59

Figure 3.16 (color). I-V results for Al₂O₃ and HfO₂ films grown at Harvard. (a) shows I-V curves for 6 nm Al₂O₃ on n⁺-Si. (b) shows I-V curves for 6 nm HfO₂ on n⁺-Si. Both samples were annealed at 800°C for 15 minutes in Ar + 2000 ppm O₂. ........60

Figure 3.17 (color). Plot of the square root of the quantum yield versus photon energy. Squares (blue line) and circles (red line) represent data obtained in this work for p- and n-type silicon specimens, respectively. The x-intercepts of each curve represent
the barrier height. The triangles are data for photoemission from silicon into vacuum, and are shown to permit comparison of the thresholds for photoemission into vacuum and photoemission into SiO$_2$. From Ref. 3.13. *Used with permission.* Reprinted by permission of the American Physical Society.

Figure 3.18 (color). Energy-band diagram between a metal surface and a dielectric. The effective barrier height is lowered (from black line to dotted blue line) when an electric field is applied to the structure. The lowering is due to the combined effects of the field and the image force (solid blue line).

Figure 3.19 (color). Sample structure used in internal photoemission measurements. The dielectric film is grown on n$^+$-Si. The light from a Hg-Xe lamp is shined on a thin gold film (deposited by evaporation). The front contact is a thicker gold pad, while the back contact is made to indium. A Keithley 6430 voltage source/ammeter is used to apply voltages across the sample and to measure the current.

Figure 3.20 (color). Current through 15 nm SiO$_2$ film as a function of incident photon energy. Inset: output spectrum of Hg-Xe light source.

Figure 3.21 (color). Yield to the 1/3, 2/5, and 1/2 power vs. photon energy. A linear fit to these curves is extrapolated to the x-axis to provide the barrier height.

Figure 3.22 (color). Barrier height profile as function of voltage for 15 nm SiO$_2$ on n-Si. The dotted line indicates the voltage at which the current switches sign. The square dots are extracted from the $Y^{1/2}$ ($Y =$ yield) curves and indicate the barrier for electrons from the metal. The triangles the barrier heights extracted from the $Y^{2/5}$ curves. The circles are from the $Y^{1/3}$ curves. The triangles or circles indicate the barrier for electrons coming from the silicon substrate.

Figure 3.23 (color). Photocurrent spectra for Al$_2$O$_3$ from Harvard.

Figure 3.24 (color). Curves showing the square root of the yield vs. photon energy for 15 nm Al$_2$O$_3$ from Harvard.

Figure 3.25 (color). Photocurrent spectra for 15 nm HfO$_2$ from Harvard.

Figure 3.26 (color). Curves showing the square root of the yield vs. photon energy for 15 nm HfO$_2$ from Harvard.

Figure 3.27 (color). Barrier height profile for HfO$_2$ and Al$_2$O$_3$ on n$^+$-Si. The data and image potential barrier lowering simulation curves on the left-hand side of the vertical dashed line represent negative photocurrents. The data and simulation curves on the right-hand side represent positive photocurrents. The open symbols and dashed lines are for HfO$_2$ while the solid symbols and solid lines are for Al$_2$O$_3$. 
Squares indicate data extracted from $Y^{1/2}$ vs. energy curves (where $Y = \text{yield}$). Triangles correspond to $Y^{2/5}$ data while circles correspond to $Y^{1/3}$ data. ………….74

Chapter 4

Figure 4.1. TEM images for Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ heterostructures. (a) The film with no high-temperature anneal. (b) The film after a 1000°C anneal in Ar + 2000 ppm O$_2$ for 15 minutes. ……………………………………………………………………………………………….80

Figure 4.2. TEM image for Al$_2$O$_3$ / Si$_3$N$_4$ / Si grown at Agere Systems. The film has been annealed for 15 minutes in Ar + 2000 ppm O$_2$ at 1000°C. An Al layer was added after the anneal. ………………………………………………………………………………………81

Figure 4.3. TEM image for HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / n$^+$-Si grown at Agere. The film has been annealed for 15 minutes in Ar + 2000 ppm O$_2$ at 1000°C. ………………….82

Figure 4.4. TEM images for heterostructures of HfO$_2$ and Al$_2$O$_3$. (a) shows Al$_2$O$_3$ / HfO$_2$ / Si. (b) shows HfO$_2$ / Al$_2$O$_3$ / Si. Each sample was annealed in Ar +2000 ppm O$_2$ at 600°C for 35 minutes. An interfacial SiO$_2$ layer was observed in both samples. ………………………………………………………………………………………83

Figure 4.5 (color). Conduction band diagram demonstrating Fowler-Nordheim tunneling. The black line represents the effective energy barrier for an electron with no bias applied. The blue dashed line represents the effective energy barrier for an electron with voltage V applied. In this case, the electron encounters a triangular barrier, the definition of Fowler-Nordheim tunneling. …………………………………….83

Figure 4.6 (color). Fowler-Nordheim plot for Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ / n$^+$-Si after a 15 min anneal in Ar + O$_2$ at 850°C. This plot shows the structure under negative bias. …86

Figure 4.7 (color). Summary of results from Fowler-Nordheim plots for Si$_3$N$_4$, Al$_2$O$_3$, and the three-layer heterostructure grown at Agere. The values of slope $E_c$ are listed for positive and negative bias for each instance. ………………………………..87

Figure 4.8 (color). Current-voltage curves for the three-layer structure 4 nm Si$_3$N$_4$ / 4 nm Al$_2$O$_3$ / 4 nm Si$_3$N$_4$. Each curve represents a sample that has been annealed for 30 minutes in N$_2$ + 10% H$_2$ at a different temperature (200, 600, 800°C). …………..89

Figure 4.9 (color). Current-voltage curve for 4 nm Si$_3$N$_4$ / 4 nm Al$_2$O$_3$ / 4 nm Si$_3$N$_4$ / n$^+$-Si. The heterostructure was annealed at 850°C for 15 minutes in Ar + 2000 ppm O$_2$. (a) is the I-V curve from the specified heterostructure with the best fit from the effective mass model overlaid. (b) is a schematic of the structure’s best fit to an effective mass model under negative bias. (c) is a schematic of the structure’s best fit to an effective mass model under positive bias. ………………………………..90
Figure 4.10 (color). Summary of results from Fowler-Nordheim plots for HfO$_2$, Al$_2$O$_3$, and the three-layer heterostructure grown at Agere. The values of slope $E_c$ are listed for positive and negative bias for each instance. ........................................92

Figure 4.11 (color). Barrier height profile as a function of voltage for Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / n$^+$-Si. The dashed vertical line indicates the voltage at which the sign of the photocurrent switches sign. On the left of this line, the electrons originate in the metal. On the right of this line, the electrons originate in the silicon substrate. The squares indicate the valence band of the silicon. The circles indicate the case in which the electrons come from the conduction band of the silicon. Blue symbols are barrier heights extracted from yield$^{1/3}$. Green symbols are barrier heights extracted from yield$^{2/3}$ .................................................................95

Figure 4.12 (color). Barrier height simulations for Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). Each barrier height profile is for the indicated voltage. The overall voltage profile assumes that the highest point in the barrier limits the electron transport. ..........96

Figure 4.13 (color). Current vs. photon energy curves for Al$_2$O$_3$ / HfO$_2$ / Si. .............97

Figure 4.14 (color). Square root of the yield vs. incident photon energy for Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si. Each curve represents a different voltage. Barrier heights are extracted from these curves by extrapolating the linear portion to the x-axis. ...............98

Figure 4.15 (color). Barrier height profile as a function of voltage for HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / n$^+$-Si. .................................................................99

Figure 4.16 (color). Barrier height simulations for HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). ..............99

Figure 4.17 (color). Current vs. incident photon energy curves for HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / n$^+$-Si. .................................................................100

Figure 4.18 (color). Barrier height profile as a function of voltage for Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / n$^+$-Si. Symbols are measurements from internal photoemission, the line is from an electrostatic simulation. The two sets of squares represent data extracted from two thresholds shown in Fig. 4.19. ..............................................102

Figure 4.19 (color). Square root of yield vs. photon energy for Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si. The dashed oval indicates the region used for fitting the lower threshold, and the dotted oval indicates the region used for fitting the upper threshold that is visible in the curve for -2 V. .................................................................103
Figure 4.20 (color). Barrier height simulations for Al₂O₃ / HfO₂ / Al₂O₃ / SiO₂ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). ........104

Figure 4.21 (color). Current vs. voltage curves for Al₂O₃ / HfO₂ / Al₂O₃ / Si grown at Harvard University. .............................................................. 105

Figure 4.22 (color). Barrier height profile as a function of voltage for HfO₂ / Al₂O₃ / HfO₂ / SiO₂ / n⁺-Si. .................................................................106

Figure 4.23 (color). Barrier height simulations for HfO₂ / Al₂O₃ / HfO₂ / SiO₂ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). ........107

Figure 4.24 (color). Barrier height profile as a function of voltage for Al₂O₃ / Si₃N₄ / n⁺-Si. .........................................................................................109

Figure 4.25 (color). Barrier height simulations for HfO₂ / Al₂O₃ / HfO₂ / SiO₂ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). The Schottky barrier height is 0.4 eV. .................................................................109

Figure 4.32 (color). Schematic demonstrating voltage tunable detector. (a) shows the barrier with no voltage applied. Neither high-energy (blue) nor low-energy (red) photons provide enough energy to the electrons in the metal for them to be transported over the barrier. (b) shows the barrier with a voltage applied, so that the overall barrier height is lowered. In this case, the high-energy photons transfer enough energy to the electrons so that a photocurrent can be measured. The low-energy photons do not. .................111

Appendix A

Figure A.1 (color). Structure of an MOS capacitor. The tunnel oxide is typically an SiO₂ layer, but a layered tunnel barrier can also be integrated. .........................122

Figure A.2 (color). Mask for deposition of silicon floating gate. .......................123

Figure A.3 (color). Capacitance-voltage (C-V) characteristics based on program voltages for MOS capacitor with SiO₂ tunnel oxide. (a) shows the C-V data at different voltages, held for 20 seconds. The black curve represents an erased device (-3.2 V for 20 seconds). (b) shows the flat-band voltage shift as a function of applied voltage. .................................................................125

Figure A.4 (color). Capacitance-voltage (C-V) characteristics based on program times for MOS capacitor with SiO₂ tunnel oxide. (a) shows the C-V data at different programming times at 3.0 V. The black curve represents an erased device (-3.2 V
Figure A.5 (color). Capacitance-voltage (C-V) characteristics based on program times for MOS capacitor with SiO₂ tunnel oxide. (a) shows the C-V data at different times after an initial program voltage of 3.0 V for 20 seconds (shown by the black curve). (b) shows the flat-band voltage shift as a function of the amount of time after the initial program pulse.

Figure A.6 (color). Description of capacitor structure in both physical and electrical terms. (a) shows a schematic of capacitor structure. (b) shows an electrical diagram of the series capacitance across the deposited layer (excluding silicon substrate). \( C_C \) represents the capacitance across the control oxide. \( C_t \) represents the capacitance across the tunnel oxide.

Figure A.7 (color). Capacitance-voltage (C-V) characteristics based on program voltages for MOS capacitor with an HfO₂ / Al₂O₃ / HfO₂ tunnel oxide. (a) shows the C-V data after 20 second voltage pulses at different voltages. The black curve represents an erased device (-3.2 V for 20 seconds). (b) shows the flat-band voltage shift as a function of program voltage.

Figure A.8 (color). Capacitance-voltage (C-V) characteristics based on program voltages for MOS capacitor with an HfO₂ / Al₂O₃ / HfO₂ tunnel oxide. (a) shows the C-V data after 20 second voltage pulses at different voltages. The black curve represents an erased device (-3.2 V for 20 seconds). (b) shows the flat-band voltage shift as a function of program voltage.

Figure A.9 (color). Capacitance-voltage (C-V) characteristics based on erase times for MOS capacitor with an HfO₂ / Al₂O₃ / HfO₂ tunnel oxide. (a) shows the C-V data for a device which has been erased at -3.2 V for varying times. The black curve represents a programmed device (3.0 V for 20 seconds). (b) shows the flat-band voltage shift as a function of erase time.

Figure A.10 (color). Capacitance-voltage (C-V) characteristics based on times after a full erase for a MOS capacitor with an HfO₂ / Al₂O₃ / HfO₂ tunnel oxide. (a) shows the C-V data at different times after a device has been fully erased. The black curve represents an erased device (-3.2 V for 100 seconds). (b) shows the flat-band voltage shift as a function of time after the erase.

Figure A.11 (color). Simulation of tunnel current and the resulting volume charge density in a complete MOS structure with a 3 nm HfO₂ / 3 nm Al₂O₃ tunnel barrier. The conduction band throughout the structure at 0 V is shown by the solid black line. The pink dotted line indicates the conduction band under 4.0 V bias. The complete structure consists of a silicon substrate (below 900 Å, 3 nm HfO₂, 3 nm Al₂O₃, 5 nm undoped silicon floating gate, and 12 nm SiO₂ control oxide, and an
aluminum gate contact. The blue solid line shows the charge density (left axis) at 0 V. The purple dotted line shows the charge density (left axis) at 4.0 V. ………..135

Table A.1. Samples from IBM – MOS devices with HfO₂ / Al₂O₃ tunnel barriers. …..136

Figure A.12 (color). Gate stack after deposition of films at IBM. ……………………..137

Figure A.13 (color). Gate stack after devices have been defined by etching. ……..138

Figure A.14 (color). Gate stack after implantation of phosphorous. The implant makes the poly-silicon control gate conductive while defining the source and drain. …..138

Figure A.15 (color). General schematics showing the transistors to be fabricated. (a) shows an embedded gate transistor. (b) shows an offset gate ring transistor. Blue represents the “active” channel regions under the poly-silicon control gate. Red represents the source region. Yellow represents the drain region. Green represents the “inactive” channel regions under the polysilicon control gate. ………………139

Table A.2. Dimensions for embedded transistors. ………………………………..140

Table A.3. Dimensions for offset contact transistors. ……………………………..140
Chapter 1  

Introduction

1.1 Overview of storage technology

Finding efficient methods for storing information has been a continuing challenge for much of human history. For example, we have archaeological records of this in the hieroglyphics of Egyptian tombs from more than 2000 years B.C. which show complex stories using a language with over 2000 characters and include methods for writing large numbers and fractions. These written methods for storing information are long lasting (nonvolatile) but the speed by which the authors could carve into stone is obviously very slow. The first precursors to modern calculation were the mechanical calculators of the 1600’s, invented by Schickard and later Pascal. In 1812, Jacquard invented his ‘weaving loom,’ the first mechanical calculator that could store information, in this case in the form of punched cards.

However, the rapid transition toward modern-day computers with high speed memories (see Table 1.1, adapted and updated from Ref. 1) occurred mostly in the 1940s, beginning perhaps with University of Pennsylvania’s ENIAC – the first instrument capable of large-scale electronic storage, utilizing vacuum tube flip-flop arrays. The birth of semiconductor-based computing occurred soon after the invention of the transistor in 1947, by Bardeen, Brattain, and Shockley.

<table>
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<th>Date</th>
<th>Storage technology</th>
<th>System Identification</th>
<th>Module size</th>
<th>Speed</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC</td>
<td>Mud or stone tablets; ink on papyrus</td>
<td>Malaysians and Egyptians; Greeks</td>
<td>Minutes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1623</td>
<td>Mechanical positions; cogs on wheels</td>
<td>Schickard's semiautomatic calculator</td>
<td></td>
<td></td>
<td>Probably first mechanical calculator; not</td>
</tr>
<tr>
<td>Date</td>
<td>Storage technology</td>
<td>System Identification</td>
<td>Module size</td>
<td>Speed</td>
<td>Comments</td>
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<td>---------------------------------------------------------</td>
<td>-------------------------------------</td>
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<td>---------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1642</td>
<td>Mechanical positions; cogs on wheels</td>
<td>Pascal's calculator</td>
<td>10 digits/wheel, 8 wheels</td>
<td>Seconds</td>
<td>First mechanical calculator still extant</td>
</tr>
<tr>
<td>1812</td>
<td>Punched cards</td>
<td>Jacquard weaving loom</td>
<td></td>
<td></td>
<td>First use of punched card storage</td>
</tr>
<tr>
<td>1890</td>
<td>Electromechanical dials, punched cards</td>
<td>Hollerith census machine</td>
<td>40 dials, 10K decimal digits per dial</td>
<td>Seconds per card (operator dependent)</td>
<td>First electrical calculator; mechanical storage electrically activated</td>
</tr>
<tr>
<td>1940</td>
<td>Capacitors on rotating drum</td>
<td>Atanasoff</td>
<td></td>
<td>1 rev/sec</td>
<td>Precursor to other circulating types of memory</td>
</tr>
<tr>
<td>1942</td>
<td>Electrical resistance on cards (analog)</td>
<td>Western Electric electrical director</td>
<td></td>
<td></td>
<td>Analog storage of functions</td>
</tr>
<tr>
<td>1943,1944</td>
<td>Electromechanical relays, punched tapes (papers)</td>
<td>Mark I (IBM - Harvard)</td>
<td>Internal counter, 2204 positions</td>
<td></td>
<td>First fully automatic calculator</td>
</tr>
<tr>
<td>1946</td>
<td>Vacuum tube flip-flop array</td>
<td>ENIAC (U. Penn)</td>
<td>20, 10 decimal digit numbers</td>
<td></td>
<td>First large-scale electronic storage</td>
</tr>
<tr>
<td>1948</td>
<td>Cathode ray (Williams) tube, magnetic drum</td>
<td>Manchester Univ. miniature machine</td>
<td>4K bits (100 numbers)</td>
<td></td>
<td>First CRT storage; one of the earliest operational drums</td>
</tr>
<tr>
<td>1949</td>
<td>Mercury delay lines</td>
<td>EDSAC (Cambridge University, England)</td>
<td>CRT (1) 1024 bits (2) 1280 bits; drum 120K bits</td>
<td>1.1 msec circulation time</td>
<td>First fully operational delay line memory</td>
</tr>
<tr>
<td>1951</td>
<td>Magnetic tape (commercial)</td>
<td>UNIVAC I</td>
<td>576 bits/tube, 18K bits total</td>
<td>100 in./sec</td>
<td>First commercial tape (and computer)</td>
</tr>
<tr>
<td>1953</td>
<td>Magnetic cores (coincident selection)</td>
<td>MIT memory test computer</td>
<td>1.44M bits max, 1500 ft, 128 char./in.</td>
<td>20 µsec access</td>
<td>First operational core memory</td>
</tr>
<tr>
<td>1955</td>
<td>Magnetic cores (coincident selection)</td>
<td>RCA BIZMAC</td>
<td></td>
<td></td>
<td>First commercial core memory</td>
</tr>
<tr>
<td>1956</td>
<td>Magnetic disk, movable heads</td>
<td>IBM 350 RAMAC</td>
<td>40M bits on 100 surfaces</td>
<td>0.5 sec access</td>
<td>First commercial movable head system</td>
</tr>
<tr>
<td>1962</td>
<td>Thin magnetic films</td>
<td>UNIVAC 1107</td>
<td>128 words, 36 bits/word (scratch-pad memory)</td>
<td>0.3 µsec</td>
<td>First commercial thin film memory</td>
</tr>
<tr>
<td>1965</td>
<td>Plated rods</td>
<td>NCR 315</td>
<td></td>
<td></td>
<td>First commercial system</td>
</tr>
<tr>
<td>1968</td>
<td>Transistor (bipolar), integrated circuits</td>
<td>IBM buffer memory S360/M85, M25</td>
<td>512 words, 18 bits/word, 64 bits/chip</td>
<td>60 nsec cycle</td>
<td>First mass-produced integrated circuit memory</td>
</tr>
<tr>
<td>1971</td>
<td>Transistor (bipolar)</td>
<td>IBM main</td>
<td>128 bits/chip</td>
<td>0.54 µsec</td>
<td>First integrated</td>
</tr>
</tbody>
</table>
Table 1.1. Summary of important memory technologies throughout history. Adapted by permission of John Wiley & Sons.

1.2 Nonvolatile memory

Since the advent of metal-oxide semiconductor (MOS) technology in the 1960s, chip designers have been working to overcome its main drawback, its intrinsic volatility. The ultimate memory technology achievement would be a genuine random access memory (RAM) that retains data without external power, can be read from or written like static or dynamic RAM (SRAM or DRAM), and can still achieve high-speed, high-density, and low-power consumption at a reasonable cost.²

One type of rewritable nonvolatile memory is electrically erasable programmable read-only memory (EEPROM) which can be subcategorized to Flash EEPROM (or simply Flash memory), where the term Flash refers to the fact that the contents of the whole memory array, or of a memory block, is erased in one step. At the moment, Flash memory is the fastest growing segment of the memory market, and it is expected that it will eventually become the third largest segment behind DRAM and SRAM.²
memory has found a niche as a portable memory and is used as the main data storage element in such products as cellular telephones and digital cameras. Its main advantage is its nonvolatility, or its ability to store charge indefinitely without the need for an electrical refresh of the data. Flash memory’s main drawback is its slow program and erase speeds (µs and ms, respectively).

1.3 Basic physics of Flash memory

Flash memory’s basic operating principle is the storage of charge in the floating gate of a metal-oxide semiconductor field effect transistor (MOSFET), as illustrated in Fig. 1.1. By applying appropriate voltages to the control gate, source, and drain, charge carriers travel through the tunnel oxide and are stored on the floating gate even after voltages are removed. The amount of charge stored on the floating gate of the MOSFET can be modified to alternate between two distinct values, usually defined as the “0” erased state and the “1” programmed state, as illustrated in Fig. 1.2.

Fig. 1.1. Schematic representation of a floating gate memory. When a voltage is applied to the control gate and a bias between the source (S) and drain (D), the channel opens to let a current flow. Some electrons also tunnel through the tunnel barrier and are stored on the silicon floating gate.
From the basic theory of a MOS transistor, the threshold voltage can be written

\[ V_{TH} = 2\phi_F + \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_D}{\varepsilon_i} d_i \]  

(1.1)

where \( \phi_{ms} \) = the workfunction difference between the gate and bulk material

\( \phi_F \) = the Fermi potential of the semiconductor at the surface

\( Q_i \) = the fixed charge at the substrate / tunnel oxide interface

\( Q_D \) = the charge in the silicon depletion layer

\( Q_T \) = the charged stored in the control oxide at a distance \( d_i \) from the gate

\( C_i \) = the capacitance between the gate and the substrate

\( \varepsilon_i \) = the dielectric constant of the oxide.

The threshold shift caused by the storage of charge \( Q_T \) is given by

\[ \Delta V_{TH} = -\frac{Q_T}{\varepsilon_i} d_i. \]  

(1.2)
The state of a Flash memory device is detected by applying a gate voltage $V_{\text{read}}$ with a value between the two possible threshold voltages. In one state, the transistor conducts current, while in the other, no current flows. Even if the power supply is interrupted, the stored charge will keep the requested memory state for later use.

1.4 Charge storage mechanism: tunneling

As illustrated in Fig. 1.1, charge is stored on the floating gate of Flash memory after electrons are transported through the tunnel oxide from the channel generated in the silicon substrate. The tunnel oxide, typically SiO$_2$, must be sufficiently thin for high electric fields to induce tunneling of electrons toward the floating gate, but still thick enough to “trap” the electrons in the conduction band of the floating gate when no voltage is applied. When the gate voltage is removed, the field in the tunnel barrier should be small to prevent charge from tunneling back to the substrate. There is a tradeoff between charge retention and the overall speed of the device and this tradeoff is a function of the tunnel oxide thickness. With a thin tunnel oxide, speed of programming and erasing is high while charge retention is low due to the greater difficulty in achieving electrically perfect thin oxide layers with no pinholes or leakage paths. While higher charge retention is achievable with thicker tunnel oxides, the speed of programming and erasing is low. This tradeoff is very significant in evaluating the overall performance of a Flash device.
1.5 High-$\kappa$ dielectrics

It can be argued that the key consideration limiting the scaling of the silicon-based MOSFET concerns the electrical properties associated with the SiO$_2$ dielectric that has been used for decades to isolate the transistor gate from the silicon channel in complementary metal-oxide-semiconductor (CMOS) devices.$^3$ The ability to grow an amorphous SiO$_2$ layer as a gate dielectric offers several key advantages in CMOS processing, including a stable high-quality silicon-SiO$_2$ interface as well as excellent electrical isolation properties.

Industry continually demands greater integrated circuit functionality at a lower cost. A requirement for this is increased circuit density, which translates into a higher density of transistors on a wafer. This requirement in turn has resulted in a rapid shrinking of transistor size and has forced the channel length and gate dielectric thicknesses to decrease to the point that the materials are near their physical limitations. Until recently, SiO$_2$ films have performed adequately as the gate dielectric material in CMOS devices, however, as the thickness of this layer drops to less than 1 nm, the electrical properties of the material become significantly degraded. For this reason, it is of interest to find alternative materials that have good electrical properties, but are still electrically thin enough to maintain good control of the channel of CMOS devices.

Performance of the dielectric gate materials is directly proportional to its capacitance. To increase transistor speed, industry continually decreases the area of the transistor. However, based on the equation for a parallel plate capacitor

$$C = \frac{\kappa \varepsilon_0 A}{t}$$  \hspace{1cm} (1.3)
where $\kappa$ is the dielectric constant of the material, $\varepsilon_0$ is the permittivity of free space ($8.85 \times 10^{-12} \text{ F} / \mu\text{m}$), $A$ is the area of the capacitor, and $t$ is the thickness of the dielectric layer, we can see that the capacitance will decrease in direct proportion to the area. To maintain the required capacitance in the gate dielectric, until recently, the semiconductor has continued to decrease the dielectric thickness $t$. However, as can be seen in Eq. (1.3), an alternative to decreasing the thickness of an SiO$_2$ tunnel oxide could be to increase the dielectric constant of the layer. Research relating to so-called high-$\kappa$ dielectrics has become a huge area of interest, and hundreds of groups around the world have been working to develop alternative gate dielectrics for CMOS devices.

1.6 Outline of thesis

The work of thesis draws on the wealth of new knowledge in the field of high-$\kappa$ dielectrics and describes both new techniques for measuring the properties of these materials as well as new applications. The main motivation for our work was to demonstrate how the integration of a careful choice of a stack of high-$\kappa$ materials can allow for improved Flash memory characteristics. Through simulation and thorough literature searches, we have identified the important parameters in optimizing a layered tunnel barrier in Flash Memory. We have demonstrated a valuable optical technique for determining band-offsets of dielectric materials, bias-dependent internal photoemission, and have used this technique to confirm the effect of barrier lowering in multi-layer samples. The observation of barrier lowering leads to the viability of improved memory characteristics using these structures.
The outline of this thesis begins with the design of layered tunnel barriers and follows the development of our capability to fully characterize these structures, and their individual components.

### 1.6.1 Layered tunnel barriers: simulation and materials identification

Chapter 2 motivates our study of layered dielectric barriers and describes our efforts in understanding and creating an ideal structure. In the context of improved memory characteristics, the concept of conduction band diagrams is introduced in order to intuitively compare layered barriers with homogenous ones and the intrinsic advantages of creating layered tunnel barriers. By choosing materials with appropriate varying band-offsets and dielectric constants, the overall barrier height seen by tunneling electrons across a tunnel barrier (see Fig. 1.1) will be reduced by the applied voltage, improving both the program and erase speed of floating gate memory devices without sacrificing their retention time.\(^4\)

Using an effective mass barrier transport model, we have calculated the current-voltage (I-V) characteristics that would optimize the layered tunnel barrier structure. Tunneling currents are calculated by numerical integration over energy and carrier angle of incidence and thus naturally include the transport mechanisms of thermionic emission, Fowler-Nordheim tunneling, direct tunneling, and tunneling through the Schottky barrier of silicon. An additional mathematical tool for studying the effects of layering dielectric materials and for an understanding of the amount of barrier lowering in an effective triangular tunnel barrier is to analyze the electrostatics of the structure.

The two mathematical methods that are described give us some guidelines for picking appropriate materials to optimize barrier lowering. Namely, for a three-layer
structure, we would like the center layer material to have a high dielectric constant and a relatively high band-offset relative to silicon (2.5 to 3.5 eV). We would like the material in the outer two layers to have a lower band-offset relative to silicon (1.0 to 1.5 eV) and a lower dielectric constant.

Though the number of measurements of band-offsets of high-κ materials in the literature is small, after a thorough literature search of both theoretical and experimental work, we were able to compile a complete list of high-k materials, their band-offsets, and their dielectric constants. This list enabled us to choose materials structures to study in more detail using our mathematical tools. The structures we chose to analyze in detail are: Si₃N₄ / Al₂O₃ / Si₃N₄, ZrSiOₓ / Al₂O₃ / ZrSiOₓ, and HfO₂ / Al₂O₃ / HfO₂.

Through the simulations and literature searches in this chapter, we have confirmed the potential advantages of layered barriers and have identified the structures that will result in the most improved characteristics in terms of a memory device.

1.6.2 Analysis of single-layer dielectrics: Bias-dependent internal photoemission and materials characterization

In Chapter 3, we use the knowledge gained from simulations presented in Chapter 2 to design and fabricate multi-layer dielectric samples. There are two main sets of samples. From Agere Systems, we obtained Si₃N₄ / Al₂O₃ and HfO₂ / Al₂O₃ heterostructures on silicon. From Harvard University, we obtained HfO₂ / Al₂O₃ heterostructures on silicon. The samples were grown on highly doped silicon to decrease the silicon depletion layer and enable easy electrical analysis. Though multi-layer sample
design is described in this chapter, only the single-layer samples are characterized. The characterization of the multi-layer samples will be presented in Chapter 4.

A series of annealing studies were performed on single-layer with the purpose of decreasing the defect density and decrease leakage currents. Transmission electron microscopy (TEM) was used to study the materials structure as a function of the annealing conditions. In the single-layer Al₂O₃ and HfO₂ films, the annealing temperature was found to be highly correlated with the growth of interfacial layers between the dielectric and the silicon substrate.

Next, current-voltage (I-V) measurements were used to investigate the electrical characteristics of the dielectric films on processing conditions. These I-V curves could be fit by the effective mass model described in Chapter 2, allowing for the extraction of thicknesses and barrier heights of the materials. Because of the non-idealities observed in the film (also shown by TEM), it was difficult to deconvolute the effects of the high-k layer, possible interfacial layers, and the nonidealities caused by leakage currents, charging, and defects in the sample.

The difficulties in quantifying the properties of the dielectric barrier by I-V characterization led us to develop the technique called bias-dependent internal photoemission. Internal photoemission spectroscopy is a simple optical method that can be used to gain information about barrier heights of dielectric materials. In this method, a bias is applied across a dielectric structure, while tunable monochromatic light shines on the sample. At a threshold photon energy, electrons from the substrate (or metal gate) are excited by internal photoemission over the dielectric barrier. This threshold energy corresponds to the barrier height of the dielectric. We developed bias-dependent internal
photoemission spectroscopy, a technique which enables us to determine a barrier height profile as a function of voltage. By measuring the barrier height at both positive and negative voltages, band-offsets with respect to silicon (and also the metal gate) can be found in addition to the flat-band voltage and barrier asymmetry at 0 V. In Chapter 3, the results of our internal photoemission measurements are presented for SiO₂, Al₂O₃, and HfO₂.

1.6.3 Optical and electrical characterization of layered dielectric barriers

In Chapter 4, we bring together what we have learned about layered tunnel barrier design in Chapter 2 with what we have learned about characterization of band-offsets with respect to silicon in Chapter 3. We will present materials characterization results for Si₃N₄ / Al₂O₃ and HfO₂ / Al₂O₃ heterostructures. We utilize TEM and I-V characterization to analyze these samples. Additionally, we use Fowler-Nordheim plots based on I-V data to compare about the positive and negative bias-dependence within a single sample, giving us information on the barrier height and asymmetry. This analysis shows good evidence that barrier-lowering is indeed occurring within our multi-layer samples. It also enables us to understand the effects the interfacial layers at the Si surface have on both the single-layer dielectrics and the multi-layer samples.

Finally, we utilize bias-dependent internal photoemission to construct a barrier profile for our multi-layer samples. Using this method, we will demonstrate the barrier lowering effect in a number of samples grown at Harvard University and Agere Systems. Additionally, we develop a consistent model for the barrier height as a function of
voltage for each heterostructure and find that our results agree with our experimental data, most notably for the HfO₂ / Al₂O₃ and Al₂O₃ / HfO₂ structures.

Barrier lowering in these heterostructures can be used in Flash memory devices, as has been discussed. In Chapter 4, we will introduce a new application called a voltage-tunable detector that will utilize these layered dielectric barriers as a high-pass filter and will detect the energies of photons that are incident on a sample.

### 1.6.4 Device measurements and design

In Appendix A, we describe how to design and measure devices that integrate layered tunnel barriers. Capacitor structures that incorporate poly-silicon floating gates and layered tunnel barriers were fabricated and the characteristics analyzed. The results, however, are somewhat inconclusive without a more thorough study of devices with both single-layer, double-layer, and triple-layer dielectrics. To this end, we describe a complete method for fabricating a set of ring-gate transistors (and other devices) that can be used to easily compare the characteristics of standard Flash memory with memory devices that integrate layered tunnel barriers.

### References


Chapter 2  Layered tunnel barriers: simulation and materials identification

2.1 Introduction

As was described in Sec. 1.4, there is a distinct tradeoff between charge storage and retention in standard Flash memory devices, based on the thickness of the SiO₂ tunnel barrier. The goal of my thesis work has been to demonstrate the capabilities of a new type of tunnel barrier. This alternative tunnel barrier utilizes high dielectric constant (high-κ) materials heterostructures and can increase the write/erase speed of a Flash memory device while maintaining good retention times.

In Fig. 2.1, three conduction band diagrams are shown. The outer flat lines represent the conduction bands of the silicon channel and floating gate, while the inner ones represent the conduction band of a dielectric gate oxide. The dotted line is an approximation of the effective band-offset when a voltage \( V \) is applied.

In Fig. 2.1(a), a homogeneous or "square" barrier is represented, as would be found in a conventional floating gate memory device. When a voltage is applied, electrons travel through an effective triangular barrier. This type of tunneling is defined as Fowler-Nordheim tunneling, as will be discussed in more detail in Sec. 4.3.

A perfectly graded triangular barrier is drawn in Fig. 2.1(b). This structure could be fabricated from a dielectric gate with a continually changing composition and dielectric constant across its thickness. In this case, when a voltage is applied, the overall barrier height that the electrons encounter is shorter (and effectively thinner for tunneling electrons) than when the voltage is removed. Since the tunneling rate depends on both the height and the thickness of the barrier, this lowering enables much faster electron
transport than with a conventional barrier (see Fig. 2.1(a)). Longer retention times should also be achievable because the taller barrier height is restored after voltages are removed. However, it isn't yet possible to make such graded barriers that are compatible with silicon due to industry's difficulty in depositing high-quality materials with graded compositions.

In Fig. 2.1(c), a layered dielectric barrier is shown, fabricated by stacking three layers of dielectric materials with appropriate dielectric constants. It was suggested by Likharev that the advantage of graded dielectric barriers could be emulated by layering dielectric materials. By choosing materials with appropriately varying band-offsets and dielectric constants, the overall barrier height seen by the tunneling electrons will be reduced by the applied voltage, improving both the program and erase speed of floating gate memory devices without sacrificing their retention time.
Fig. 2.1. Schematic representation of a floating gate memory. When a voltage is applied to the control gate and a bias between the source (S) and drain (D), the channel opens to let a current flow. Some electrons also tunnel through the tunnel barrier and are stored on the silicon floating gate. The threshold voltage gives a measure of the amount of charge stored (after Ref. 1). Parts (a), (b), and (c) show conduction band edge diagrams of various types of tunnel barriers: (a) a typical uniform barrier; (b) idealized crested symmetric barrier; (c) three-layer structure. Dotted lines show the barrier tilting caused by applied voltage \( V \) (after Ref. 3). Part (d) illustrates the three-layer capacitor structure that is referred to in (c). The left-hand electrode is silicon and the right-hand electrode is a metal contact and dielectric constants \( \varepsilon \), electric fields \( E \), and applied voltage \( V \) are indicated. Through calculation, it is found that the amount of charge trapped in the triangular well that is formed at the interface of layer 1 and 2 is negligible.
2.2 Simulation methods

2.2.1 Effective mass model

2.2.1.1 General functionality of the effective mass model

Using a barrier transport model, we have calculated the current-voltage (I-V) characteristics that would optimize the layered tunnel barrier structure. To correspond with a long retention time as well as a fast program/erase speed, the ideal I-V curves show that the ratio of the current density at some maximum voltage $J_{\text{max}}$ to the current density at some minimum voltage $J_{\text{min}}$ should be at least as large as

$$\frac{J_{\text{max}}}{J_{\text{min}}(V = 0)} = \frac{\tau_{\text{ret}}}{\tau_{\text{prog}}} = \frac{30 \text{ years}}{1 \text{ ns}} \approx 10^{18}. \quad (2.1)$$

This value is based on an ideal retention time $\tau_{\text{ret}}$ for a device of at least 30 years and a programming time $\tau_{\text{prog}}$ of at most 1 nanosecond yielding an overall current ratio of at least $10^{18}$. This current ratio should occur between voltages of approximately 0 and 4 V to be compatible with current device technology. While it is important to obtain large current ratios, the absolute currents are also important because the nonvolatility and speed in data storage devices are affected by off-state and on-state currents, respectively. A reasonable off-state current for a gate of area 0.01 $\mu$m$^2$ would be 1 electron per 30 years, or about $1.7 \times 10^{-18}$ A/cm$^2$. The on-state current could be 100 electrons per nanosecond, or about 160 A/cm$^2$.

The tunneling current for any given bias is determined by the thermal distribution of electrons, Fermi functions, and the shape of the barrier. We have developed a barrier tunneling transport model to analyze possible barrier structures that incorporate the layered dielectrics on silicon with a metal contact. Because the dielectrics will be grown
on silicon, our simulations include the effects of band bending due to the depletion region of the silicon. For this case, the values for band bending in a metal-semiconductor (MS) contact are used.\textsuperscript{3} The model assumes the effective mass approximation and a plane-wave basis. The barrier layers and electrodes are treated as continuous media, which is a reasonable approximation for amorphous materials.\textsuperscript{4} Tunneling current is calculated by numerical integration over energy and carrier angle of incidence and thus naturally includes the transport mechanisms of thermionic emission, Fowler-Nordheim tunneling, direct tunneling, and tunneling through the Schottky barrier of the silicon. The barrier transmission probability is calculated using numerical methods, which allows for analysis of resonant tunneling effects and localized charge densities trapped in potential minima. The current density includes the carrier transport (either electrons or holes) in both directions between the metal and semiconductor contact:

\[
J = J_{S-M} - J_{M-S} = \frac{4m^*e}{h^3} \int \int \pi(\epsilon, \Omega)[f_s(\epsilon) - f_m(\epsilon)]\cos \theta \, d\epsilon \, d\Omega
\]  \hspace{1cm} (2.2)

where \( m^* \) is the electron effective mass in the semiconductor (\( m^* = 1 \) is assumed in the metal), \( e \) is the electron charge, \( h \) Planck's constant, and \( \epsilon \) is the electron energy (in this equation only). The function \( \pi(\epsilon, \Omega) \) is the single-electron transmission probability calculated for the entire potential structure, including the layered dielectrics and the silicon depletion region.\textsuperscript{4} The variable \( \Omega \) is the solid angle of electron incidence on the barrier and \( f_s, f_m \) is the Fermi function for the silicon substrate and metal contact, respectively.
2.2.1.2 Derivation details of the effective mass model

The k-space integration in Eq. 2.2 can be done in a straightforward way by using numerical methods, with special care taken with the integration over energy. For certain barrier combinations, the transmission resonances can be extremely narrow, while at the same time having enough spectral weight to dominate the total current. The Wentzel-Kramers-Brillouin (WKB) approximation is a well-known method for estimating tunneling through a barrier but it is not useful in our case because it does not reproduce the described resonant transmission effects, nor does it properly treat the transmission near the band edges or through propagating states. The numerical methods we use allow for the treatment of transmission that is dominated by such combined processes as thermionically-assisted tunneling.

By breaking the potential barrier into many exactly solvable square barriers, transmission can be calculated, within the independent-electron picture, to arbitrary precision. Essentially, this is a one-dimensional treatment, although parallel components of electron momentum are assumed. Those components are conserved since specular transmission is also assumed (no interface roughness or electron scattering).

In this model, values of effective mass and dielectric constant are assigned to each layer, and the potential structure is divided into a stack of thin square barriers. By matching the incoming and outgoing wavefunctions ($\psi_1$ and $\psi_2$) at each interface, using the matching conditions,

$$\psi_1 = \psi_2,$$

and
\begin{align}
\frac{1}{m_1} \frac{d\psi_1}{dx} &= \frac{1}{m_2} \frac{d\psi_2}{dx}, \\
\end{align}

we develop a recursion relation that involves only electron energy and the barrier heights and effective masses of adjacent slices. The final recursion relation yields the outgoing wave function amplitude and the transmission coefficient \( T \) through the entire structure:

\[ T = \left( \frac{v_{\text{out}}}{v_{\text{in}}} \right) |\psi_{\text{out}}|^2, \]

giving the overall propagating solution. Here \( v_i \) are the electron velocities in the source and destination electrodes.

These recursion relations can be summarized as follows. The potential structure is divided into \( n \) layers. For each layer \( j \), the recursion coefficients are given by,

\[ 
\alpha_j \equiv \left\{ \frac{m_{j-1} \kappa_j}{m_j \kappa_{j-1}} f_{j-1} - \frac{1}{f_{j-1} + 1} \right\}, \\
\beta_j \equiv \left\{ \frac{f_{j-1} + 1}{m_{j-1} \kappa_j} \right\} \beta_{j-1} e^{-\kappa_{j-1} \Delta x} \]

where \( f_j \equiv \left[ \frac{e^{\kappa_j \Delta x} + \alpha_j e^{-\kappa_j \Delta x}}{e^{\kappa_j \Delta x} - \alpha_j e^{-\kappa_j \Delta x}} \right] \)

and \( \alpha_0 = 0, \beta_0 = 1 \). Here, \( \Delta x \) is the layer thickness, \( \kappa_j = \left[ 2m_j^* / h^2 (V_j - E) \right]^{1/2} \) is the wave vector, and \( m_j \) is the effective mass. For layers in which the state is propagating, the wave vector is given instead by \( \kappa_j = i \left[ 2m_j^* / h^2 (E - V_j) \right]^{1/2} \). Thus each \( \alpha_j \) or \( \beta_j \) coefficient for layer \( j \) depends on the coefficients for the previous \((j-1)\) layer. The final wave function amplitude for the outgoing state is given by
\[ b_{n+1} = -\left( \frac{f_n + 1}{-im_n q_{out} f_n + 1} \right) \beta_n e^{-\kappa_n \Delta x} e^{-iq_{out} x_0}. \]  \hspace{1cm} (2.7)

Once all the coefficients are obtained, wave function amplitudes can also be calculated at any point in the potential. These can be used for simple calculations of charge density \( \sigma \):

\[ \sigma = e \iint |\psi|^2 \, dx \, dE. \] \hspace{1cm} (2.8)

By self-consistently solving the wave equation and Poisson’s equation in the presence of a steady-state charge distribution, the effect of charging on the potential is also included. We use Eq. 2.8 to determine the amount of charge that builds up in the triangular well. In all cases presented here, charging effects due to carrier accumulation in voltage-induced wells within the barrier structure were negligible (less than a 10 mV change in the potential).

### 2.2.2 Electrostatic model

Fig. 2.1(c,d) show the device geometry for the three-layer structure under consideration. It consists of layered dielectric materials that are deposited on silicon and a metal contact on top of the dielectrics. By varying the barrier heights of the materials relative to Si, the currents through the barrier are controlled, though the dielectric constants and thicknesses are the controllable parameters that directly affect the amount of barrier lowering. Using the definition of voltage

\[ V = -\int E \cdot dl \] \hspace{1cm} (2.9)

we can write
\[ V_1 = E_1d_1, V_2 = E_2d_2, V_3 = E_3d_3 \]  

(2.10)

for the voltage drop over each dielectric layer in Fig. 2.1(d).

Also, using the definition of electric field in terms of charge density

\[ \nabla \cdot E = \frac{\rho}{\varepsilon_0} \]  

(2.11)

and assuming there’s no surface charge \( \rho \), we find that

\[ \varepsilon_1E_1 = \varepsilon_2E_2 = \varepsilon_3E_3. \]  

(2.12)

By combining Eqs. 2.11 and 2.12, we can write

\[ E_1 = \frac{V}{d_1 + d_3 + d_2 \left( \varepsilon_1 / \varepsilon_2 \right)} \]  

(2.13)

where \( V \) is the applied voltage, \( E_1 \) is the electric field, \( d_i \) is the thickness, and \( \varepsilon_i \) is the dielectric constant in each region. The subscripts 1 and 3 in Eqs. 2.10 - 2.13 refer to the low band-offset layers on the outside of the structure while the subscript 2 refers to the high band-offset middle layer (see Fig. 2.1(d)). This relation indicates that to maximize the overall barrier lowering, the electric field through the first layer should be maximized. This means that the center barrier material should have a high dielectric constant and that the low band-offset barrier (first and third layers) material should have a low dielectric constant. However, it is challenging to find materials that meet these requirements, because most with high dielectric constants have low band-offsets and vice versa.\(^5\)

### 2.3 Materials requirements and options

There are several factors that need to be taken into account when determining the appropriate materials and structures to demonstrate the proposed barrier lowering. We
have focused on specific candidate structures by considering the barrier heights, dielectric constants, and thicknesses of amorphous dielectric media for which there is some fabrication experience for silicon-based devices. The total barrier thicknesses that are considered are between 10 and 20 nm. Ideal barrier heights for the center layer are in the range 2.5 - 3.5 eV, while the outside layers should be 1.0 - 1.5 eV. It should be noted that the barrier height has a larger influence on the tunneling characteristics than does the dielectric constant.

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric constant</th>
<th>Band gap (eV)</th>
<th>CB offset from Si (eV)</th>
<th>VB offset from Si (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al$_2$O$_3$</td>
<td>9$^8$*</td>
<td>8.8$^*$</td>
<td>2.8$^*$</td>
<td>4.9$^*$</td>
</tr>
<tr>
<td>BaZrO$_3$</td>
<td>43$^{9*}$</td>
<td>5.3$^{7*}$</td>
<td>0.8$^{7*}$</td>
<td>3.4$^{7*}$</td>
</tr>
<tr>
<td>CaO</td>
<td>12.0-12.2$^{9*}$</td>
<td>2.5$^{12*}$</td>
<td>1.8$^{13*}$</td>
<td></td>
</tr>
<tr>
<td>Gd$_2$O$_3$</td>
<td>14$^{11}$</td>
<td>6$^{7*}$</td>
<td>1.5$^{7*}$</td>
<td>3.4$^{7*}$</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>22$^{9}$</td>
<td>15-25$^{14}$</td>
<td>6$^7$</td>
<td></td>
</tr>
<tr>
<td>HfSiO$_x$</td>
<td>15$^{10}$</td>
<td>7$^{15}$</td>
<td>23$^{7}$</td>
<td></td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>20.8$^9$</td>
<td>6$^7$</td>
<td>2.3$^7$</td>
<td></td>
</tr>
<tr>
<td>MgO</td>
<td>9.8$^9$</td>
<td>8.7$^{10}$</td>
<td>1.7$^{16}$</td>
<td>1.7$^{19}$</td>
</tr>
<tr>
<td>Sc$_2$O$_3$</td>
<td>13$^9$</td>
<td>5.4$^{10}$</td>
<td></td>
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</tr>
<tr>
<td>Si$_3$N$_4$</td>
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<td>5.3$^{7*}$</td>
<td>2.4$^{7*}$</td>
<td>1.8$^{7*}$</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>3.9$^{3*}$</td>
<td>9$^{7*}$</td>
<td>3.5$^{7*}$</td>
<td>4.4$^{7*}$</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>25$^{17*}$</td>
<td>4.4$^{7*}$</td>
<td>0.3$^{7*}$</td>
<td>3$^{7*}$</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>80$^{3*}$</td>
<td>3$^{10}$</td>
<td>0$^{7*}$</td>
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<tr>
<td>Y$_2$O$_3$</td>
<td>13-17$^{21}$</td>
<td>5.5$^{10*}$</td>
<td>1.3$^{7*}$</td>
<td>3.6$^{7*}$</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>11.3$^9$</td>
<td>5.6$^{22}$</td>
<td>1.4$^{7*}$</td>
<td>3.3$^{7*}$</td>
</tr>
<tr>
<td>ZrSiO$_x$</td>
<td>12.6$^{23*}$</td>
<td>6$^{7*}$</td>
<td>1.5$^{7*}$</td>
<td>3.4$^{7*}$</td>
</tr>
</tbody>
</table>

Table 2.1. Values for dielectric constant, band gap, conduction and valence band-offsets for various dielectric materials.
Table 2.1 is a list of reported dielectric constants, band gaps, and experimental and theoretical values for the conduction and valence band-offsets of various dielectric materials on Si. These offsets are shown as a function of dielectric constant in Fig. 2.2. (The values used in the figure are indicated by an asterisk in the table. References are indicated by the superscript.) This figure enables us to determine promising materials to maximize the overall barrier height lowering in layered dielectric tunnel barrier structures. For electron tunneling devices, the approximately inverse relation between conduction band-offset and dielectric constant complicates the search for a material with low dielectric constant and low band-offset and for another with high dielectric constant and high band-offset. For hole tunneling devices, no clear trend emerges as indicated by the distribution of dielectric constants and band-offsets for hole tunneling shown in Fig. 2.2. This could be an advantage when choosing materials for such devices.
Fig. 2.2. Shows the relationship between the dielectric constant and band-offset from Si for various materials. The upper panel shows the conduction band-offsets and the lower panel shows the valence band-offsets. They are separated by a silicon band gap of 1.1 eV. Squares indicate theoretical band-offset values and triangles indicate experimental band-offset values. The dielectric constants given are from recent journal articles and vary slightly according to deposition method or other factors. The values used in this figure are indicated by an asterisk in Table 2.1.
2.4 *Simulation results*

Because an effective mass model was used, reasonable values of mass were chosen for the electrodes and barrier materials. Electrode masses are much less important, only contributing to the prefactors in the expression for tunnel current. For metal electrodes, $m^* = 1$ was used. For silicon, $m^* = 0.2$ was used for electrons (the transverse mass for the conduction-band minimum at the center of the interface Brillouin zone for a (100)-oriented substrate).\(^3\) Since all barrier materials were assumed to have zone-centered conduction-band minima, the other Si minima at large parallel wave vectors were assumed to contribute only weakly to total current. For the case of holes, an isotropic mass of 0.5 was used for the silicon substrate.\(^3\) For the Al\(_2\)O\(_3\) barrier layers, $m^* = 0.5$ was used; for Si\(_3\)N\(_4\), 0.2 was used. Effective masses for holes were taken to be 0.5 for all barrier layers, and all barrier effective masses were assumed to be isotropic. Because total current is an integral over energy, and because the conduction and valence band effective masses are only appropriate for energies near the band edges, it is not straightforward to pick an appropriate value for simulations. Overall, however, we have chosen values that should give reasonable relative tunneling currents.\(^{24}\)

In Fig. 2.3(a), tunneling electron density per unit energy is shown as a function of $E_x - E_f$ (difference between the normal component of electron energy and the Fermi level) for a 4 nm and 6 nm (3 eV height for both) barrier with a bias of 0.1 V. The curve for the 4 nm barrier (solid line) has a maximum that is about 1 eV above the Fermi level. The electron current is not directly from the Fermi level, but is being limited by the Schottky barrier caused by the silicon depletion region. For the 15 nm barrier (dotted line), it is
observed that the electron transport occurs at higher energies – an indication of thermionic emission.

Fig. 2.3. Tunneling current per unit energy (A / cm² / eV) as a function of $E_x - E_F$ (eV). The solid line in part (a) is for a 4 nm square barrier and the dotted line indicates a 3 eV, 15 nm square barrier at a bias of 0.1 V. Part (b) shows the analogous situation for a bias of 2.0 V, while part (c) shows the transport of electrons through three different three-layer tunnel barriers at 2.0 V as well. The solid curve indicates Si₃N₄ / Al₂O₃ / Si₃N₄. The dotted curve indicates ZrSiOₓ / Al₂O₃ / ZrSiOₓ. The dashed curve indicates an ‘ideal structure’ with barrier heights 1.0 / 3.0 / 1.0 eV and dielectric constants 7.5 / 9.0 / 7.5. The thickness of each individual dielectric layer is 6 nm. Part (d) shows the analogous cases for the tunneling of holes at 2.0 V.
Fig. 2.3(b) shows the analogous structure at a higher bias voltage of 2.0 V. For a 4 nm barrier (solid line), tunneling is still the dominant transport mechanism, though the maximum tunneling current is at $E_x - E_f = 0$, meaning that most of the transport occurs at the Fermi level. For the 15 nm barrier, the increase in voltage causes the maximum tunneling current to be shifted to lower energies as is shown by the dotted line in Fig. 2.3(b). The transport in this case is still dominated by thermionic emission – the shift to lower energy transport (compared with the 0.1 V case) is due to the lowering of the barrier maximum.

We have calculated the tunneling current density per unit energy vs. $E_x - E_f$ for three candidate three-layer structures due to their closer to ideal dielectric constant and band-offset properties: Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$, ZrSiO$_x$ / Al$_2$O$_3$ / ZrSiO$_x$, and an ‘ideal’ structure (meaning it shows a large current ratio) with barrier heights 1.0 / 3.0 / 1.0 eV and dielectric constants of 7.5 / 9.0 / 7.5. The results of these calculations are shown in Fig 3(c). The assumed barrier conduction band-offsets with respect to silicon are 2.4 eV for Si$_3$N$_4$ and 2.8 eV for Al$_2$O$_3$, and the dielectric constants for Si$_3$N$_4$ and Al$_2$O$_3$ are 7.5 and 9.0, respectively. ZrSiO$_x$ has a conduction band-offset of 1.5 eV and a dielectric constant of 12.6. The thickness for each dielectric layer in the structure is 6 nm and the applied voltage is 2.0 V. The dashed curve in Fig. 2.3(c) describes the ‘ideal’ structure, and shows such significant barrier lowering that the electrons can tunnel through the structure directly from the Fermi level. For comparison, the heterostructure that incorporates Si$_3$N$_4$ (the solid curve in Fig. 2.3(c)) shows a maximum in tunneling current at about 2 eV under the same applied voltage of 2.0 V. This behavior results from the relatively small difference in barrier heights for the two materials (only 0.4 eV) and
indicates that the barrier to electron transport at this applied voltage is effectively thicker than the ‘ideal’ structure, allowing electron transport only at higher energies to occur over the structure (thermionic emission). The ZrSiO\textsubscript{x} structure (dotted curve in Fig. 2.3(c)) shows an intermediate behavior with a smaller tunneling electron current directly from the Fermi level than for the ideal structure, but greater than for the Si\textsubscript{3}N\textsubscript{4} structure.

Fig. 2.3(d) illustrates the hole tunneling behavior in Si\textsubscript{3}N\textsubscript{4} / Al\textsubscript{2}O\textsubscript{3} / Si\textsubscript{3}N\textsubscript{4} and ZrSiO\textsubscript{x} / Al\textsubscript{2}O\textsubscript{3} / ZrSiO\textsubscript{x} heterostructures. The valence band-offset for Si\textsubscript{3}N\textsubscript{4} is 1.8 eV while the offset for Al\textsubscript{2}O\textsubscript{3} is 4.9 eV. ZrSiO\textsubscript{x} has a valence band-offset of 3.4 eV. In the Si\textsubscript{3}N\textsubscript{4} / Al\textsubscript{2}O\textsubscript{3} / Si\textsubscript{3}N\textsubscript{4} structure, the maximum hole transport occurs at energies that are just above the Fermi level of the silicon. This is due to the large differences in the valence band-offsets for the Si\textsubscript{3}N\textsubscript{4} and Al\textsubscript{2}O\textsubscript{3}. The maximum tunneling current occurs at higher energies for the ZrSiO\textsubscript{x} / Al\textsubscript{2}O\textsubscript{3} / ZrSiO\textsubscript{x} structure, though two steps in tunneling current can be observed (dotted curve). The first step in tunneling current indicates the change in electron transport from tunneling to thermionic emission over the first barrier, while tunneling remains dominant through the second barrier. The second step indicates that the electron transport is not limited by tunneling in any part of the structure and the electrons are being thermionically emitted over the entire barrier. To a lesser degree these steps can be observed in the Si\textsubscript{3}N\textsubscript{4} / Al\textsubscript{2}O\textsubscript{3} / Si\textsubscript{3}N\textsubscript{4} structure. Resonances can be observed and result from the potential wells formed between the layers when the bias is applied.

As described in Eq. 2.2, by integrating over all energies, the total current can be obtained. In Fig. 2.4, several simulated I-V curves for theoretical barrier structures are shown that closely approximate a perfectly graded barrier. These simulations allow us to clearly depict the advantage of layered barriers over a homogenous structure. A graded,
triangular barrier structure (2.5 eV maximum band-offset, 20 nm thick) is shown by the solid curve. A five-layer structure ($\Delta \varepsilon_c$: 1.0 / 1.6 / 2.5 / 1.6 / 1.0 eV, 4 nm individual layer thickness) is shown by the dotted line and its tunneling characteristics very closely approximate the continuously graded barrier. The dashed line shows a three-layer structure ($\Delta \varepsilon_c$: 1.4 / 2.5 / 1.4 eV, $t = 7 / 5 / 7$ nm) whose behavior still approximates the graded structure, but differs more than the five-layer structure. A square barrier ($\Delta \varepsilon_c$: 2.5 eV, $t = 8$ nm) is represented by the line with square symbols. Its tunneling characteristics are considerably different from the graded and layered barriers exhibiting an electron tunneling current density at $V = 4$ V, approximately $10^{11}$ times lower. Curves such as these emphasize the ability of layered structures to significantly increase the tunneling current ratios compared with the square barriers that are used in devices today. Though it may be very difficult to find materials to construct the five-layer barriers, it is interesting to see how closely they approximate the graded barrier.
The simulated current-voltage (I-V) curves for Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ and ZrSiO$_x$ / Al$_2$O$_3$ / ZrSiO$_x$ on n-type silicon are shown in Fig. 2.5(a). Under a 4.0 V bias, for the Si$_3$N$_4$ three-layer structure with 6 nm of each material, we expect a current ratio of $10^{31}$ while we expect a current ratio of $10^{25}$ for a single 6 nm homogeneous barrier of Al$_2$O$_3$, though most of the current is limited by the Schottky barrier in this case. The current ratio for the ZrSiO$_x$ layered structure, is larger ($10^{37}$) due to the greater difference in
barrier heights. For comparison, a 9 nm Al₂O₃ layer gives a current ratio of 10^{31} though the total electron tunneling current is lower for this case.

The differences between homogeneous barriers and layered barriers on p-type silicon are shown in Fig. 2.5(b). We again examine the results from a 4.0 V bias: for the 6 nm Al₂O₃ barrier, we see a current ratio of 10^{14}, whereas a 7.7 nm Al₂O₃ barrier gives a current ratio of 10^{16}. The ZrSiOₓ layered barrier gives a greater current ratio of 10^{23}. The simulated current ratio is quite dramatic for the Si₃N₄ layered barrier (10^{28}) because of the significant difference in the band-offsets compared to that of silicon for the two materials.
2.5 Materials nonidealities

Our simulations assume ideal materials, though ideal materials will of course not be available for experiment. Other fabrication issues to be considered include defect density and interface quality. Localized trap states within the barrier films might result in bias dependent leakage currents that could obscure the barrier lowering effect. Likewise, if an unwanted (e.g., silicon dioxide) film develops at the silicon-barrier interface, a spurious barrier with large barrier height and relatively low dielectric constant could cause the speed of the program/erase process to decrease.

Fig. 2.6 shows a three-layer structure with a number of non-idealities including transport through the Schottky barrier\textsuperscript{1} formed at the silicon / dielectric interface. The trap states cause leakage currents but can also result in effects such as Frenkel-Poole emission where trapped charge near the top of the dielectric conduction band can be emitted in an alternative type of transport.

In our analysis, we have focused on amorphous materials. Such materials are of particular interest because they are simple to fabricate on silicon compared with the growth of lattice constant matched crystalline materials.

\textsuperscript{1} A Schottky barrier is a rectifying barrier for electrical conduction across a metal-semiconductor interface. The magnitude of the Schottky barrier height generally reflects the mismatch in the energy position of the majority carrier band edge of the semiconductor and the metal Fermi level across the metal-semiconductor interface.
2.6 Conclusion

In summary, we have explored the performance of silicon-based layered tunnel dielectric barrier structures and have predicted the tunneling characteristics for various barrier physical parameters. Our model indicates the dominant current transport mechanism for different barrier structures and shows that five- and three-layer barriers closely approximate the perfectly graded barriers, giving promise for these structures to be integrated into silicon-based technology. We have comprehensively surveyed the dielectric constants and band-offsets for dielectric materials that are under investigation in recent literature. Based on this data, and our simulations, two real structures that could potentially demonstrate the barrier lowering effect are Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ and ZrSiO$_x$ /...
Al₂O₃ / ZrSiOₓ. Compared with similar devices that utilize homogenous tunneling barriers, layered barriers could improve both the speed and retention time of floating gate memory devices.

References

9. D. G. Schlom (private communication).


Chapter 3 Analysis of single-layer dielectrics:
Internal photoemission and materials characterization

3.1 Significance of band-offsets for dielectric materials

There is an urgent need to find alternative dielectrics to act as the gate insulator in MOS technology. Silicon dioxide is currently used, but the decreased SiO₂ thickness required to scale down transistors for faster operation will cause large leakage currents as the oxide gets below 1 nm. As was explained in Sec. 1.4, the alternative is to use a larger thickness of a higher dielectric constant (high-κ) material. However, compared with SiO₂, these new dielectrics have much lower band gaps and could have a different type of leakage problems due to Schottky emission of carriers into the band states.¹

There are many criteria for selecting suitable high-κ materials. These materials must be thermodynamically stable next to silicon to avoid the formation of interfacial SiO₂ and must have a low diffusion coefficient so that material components will not diffuse into silicon, ruining the semiconductor electrical properties, during high temperature processing. A high-quality dielectric/silicon interface is also necessary to avoid interfacial charge trapping which degrades device performance. Finally, the high-κ material must have a barrier for electrons and holes of at least 1 eV, in order to have sufficiently low leakage currents from Schottky emission.¹

Good device performance requires a sufficiently high band-offset for the high-κ layer on silicon, however, the band-offset is not well known or characterized for many materials of interest. Having reliable measurements of the band-offset is a critical
requirement for device design and is a primary motivator for my thesis work. In this chapter, I will introduce a valuable measurement method for dielectric/silicon band-offsets called bias-dependent internal photoemission and present our results for these measurements.

3.2 Sample preparation and fabrication description

3.2.1 ALD HfO₂, Si₃N₄, and Al₂O₃ from Agere Systems

Two sets of samples were obtained from Agere Systems. The first set of samples contained single-layer Si₃N₄ and Al₂O₃, as well as Si₃N₄ / Al₂O₃ heterostructures (from Brett W. Busch, Martin L. Green, 2001). The split sheet for these wafers is shown in Table 3.1.

The silicon wafer lot number for the Agere samples is Z010504 and the wafers are 200 mm in diameter. Before implantation, a 50 Å sacrificial SiO₂ layer was deposited on a lightly doped p-type wafer (~10¹⁵ boron atoms / cm³). Multiple implants were performed to make a uniform degenerate doping layer that is 1.5 µm deep. The n⁺-type implants (5x10¹⁹ atoms / cm³) are phosphorus: 2.2x10¹⁴ ions/cm² at 2keV, 7.1x10¹⁴ ions / cm² at 120 keV, 1.3x10¹⁵ ions / cm² at 300 keV, and 2.0x10¹⁵ ions / cm² at 550 keV. The p⁺-type implants are boron (5x10¹⁹ atoms / cm³): 4.2x10¹⁴ ions / cm² at 25 keV, 7.7x10¹⁴ ions / cm² at 75 keV, 8x10¹⁴ ions / cm² at 150 keV, and 1.3x10¹⁵ ions / cm² at 250 keV. After the implants, the wafers were annealed at 1050 °C for 900 seconds. An HF dip removed the sacrificial oxide layer, and after a standard oxide clean, the growth splits were begun.
The Si₃N₄ depositions were performed after a 60 second dip in dilute HF (1:100). The Si₃N₄ was grown by low pressure chemical vapor deposition (LPCVD) with dichlorosilane and ammonia precursors at 700°C at a 10 Å / min growth rate. Prior to Al₂O₃ growth, the nitride layers were dipped for 10 seconds in 100:1 HF to remove ambient SiO₂ which forms after the wafers are removed from the CVD furnace at 400°C. Ellipsometry measurements show that the amount of SiO₂ removed during this step is about 6 Å. The Al₂O₃ was grown by atomic layer deposition (ALD) with alternating cycles of trimethyl-aluminum and water at 300°C. The growth rate for Al₂O₃ was 0.87 Å / cycle.

The index of refraction for the ALD Al₂O₃ is 1.66. The LPCVD Si₃N₄ has an index of refraction of 2.0 as determined by Thermawave ellipsometry at Agere. Thermawave measurements were also used to determine the thickness of each layer (as shown in table 3.1). The targeted thicknesses were mainly 6 nm. Three-layer films with 4 / 4 / 4 nm layers were targeted as was a 6 / 12 / 6 nm film. The layers deposited on wafers 1, 4, 7, 8, 9, 10, and 12 were also deposited on lightly doped p-type silicon (~10¹⁵ boron atoms / cm³).

<table>
<thead>
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<th>layer 3 (nm)</th>
<th>doping</th>
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<td>-</td>
<td>n⁺</td>
</tr>
<tr>
<td>04</td>
<td>5.0</td>
<td>-</td>
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</tr>
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</tr>
<tr>
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<td>6.5</td>
<td>5.6</td>
<td>-</td>
<td>n⁺</td>
</tr>
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<td>-</td>
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<td>-</td>
<td>n⁺</td>
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<td>n⁺</td>
</tr>
<tr>
<td>11</td>
<td>6.2</td>
<td>11.4</td>
<td>6.2</td>
<td>n⁺</td>
</tr>
<tr>
<td>12</td>
<td>6.2 SiO₂</td>
<td>-</td>
<td>-</td>
<td>n⁺</td>
</tr>
</tbody>
</table>
The second set of samples from Agere included heterostructures of ALD Al$_2$O$_3$ and HfO$_2$ (from Munyee Ho, Martin L. Green, 2002). The Al$_2$O$_3$ was grown in the same method as described above for Table 3.1. The HfO$_2$ was grown by alternating hafnium tetrachloride and water. The final list of HfO$_2$ and Al$_2$O$_3$ heterostructures are listed below in Table 3.2. As was the case for the samples in Table 3.1, these layers were grown on the highly doped substrates listed as well as on lightly doped p-type monitor wafers.

<table>
<thead>
<tr>
<th>wafer</th>
<th>Layer 1 (nm)</th>
<th>layer 2 (nm)</th>
<th>layer 3 (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>6</td>
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<td>-</td>
</tr>
<tr>
<td>3</td>
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<tr>
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</tr>
<tr>
<td>18</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
</tbody>
</table>

Table 3.2. Second batch of Agere Samples (HfO$_2$ and Al$_2$O$_3$).
Heavily doped substrates were utilized to ensure ohmic contact with the metallic gate contacts that were later used for current-voltage (I-V) measurement. The samples grown on n+-type silicon showed electron tunneling characteristics, while the samples grown on p+-type silicon showed hole tunneling characteristics. Lightly doped substrates were chosen to act as monitor wafers for the dielectric deposition and to allow for capacitance-voltage (C-V) measurements with a significant depletion region.

Single-dielectric layers were fabricated to learn about the physical and electrical characteristics of the individual layers, in order to understand the multi-layer samples. Two-layer samples (with asymmetric band structure) are expected to have asymmetric electrical characterization characteristics which could easily demonstrate barrier lowering. The three-layer samples were later analyzed (see Chapter 4) to show barrier lowering by their I-V behavior. The structures were chosen after simulations such as those described in Chapter 2. The outer barrier materials were HfO2 (expected Si conduction band-offset of 1.5 eV) and Si3N4 (expected Si conduction band-offset of 2.4 eV). The inner barrier material was Al2O3 (expected Si conduction band-offset of 2.8 eV). The barrier for holes was expected to be 1.8 / 4.9 / 1.8 eV for Si3N4 / Al2O3 / Si3N4 and 3.4 / 4.9 / 3.4 eV for HfO2 / Al2O3 / HfO2. Schematics of the band-structures for these heterostructures are shown in Fig. 3.1.
It should be noted, that while many multi-layer samples were fabricated and listed in this section, their characterization will not be discussed until Chapter 4.

### 3.2.2 ALD HfO$_2$ and Al$_2$O$_3$ from Harvard University

A number of Al$_2$O$_3$ and HfO$_2$ dielectric samples were obtained from Harvard University (Damon B. Farmer and Roy G. Gordon, 2003). The dielectric samples are grown on degenerately phosphorous doped n-type silicon to minimize the voltage drop across the depletion region in the silicon, and enhance the accuracy of our measurement. The dielectrics obtained from Harvard are HfO$_2$ and Al$_2$O$_3$ grown by atomic layer deposition (ALD). Before deposition, samples were dipped in a 5% HF solution for 30 seconds followed by a 3 minute UV/ozone cleaning. HfO$_2$ films were grown using deionized water (DI H$_2$O) and tetrakis(diethylamido)hafnium (Hf[NEt$_2$]$_4$), while Al$_2$O$_3$ films were grown using DI H$_2$O and trimethylaluminum (Al[CH$_3$]$_3$). Nitrogen was used as the carrier gas, and the deposition temperature was 225°C.
3.3 Physical characterization

3.3.1 ALD HfO2, Si3N4, and Al2O3 from Agere Systems

We used transmission electron microscopy (TEM) to learn about the physical characteristics of our films. Due to the Z-contrast ratio (difference in the masses of the elements in each layer) TEM can give us information on the layer thicknesses and crystallinity of our single-layer and multi-layer structures. This section describes the TEM results for single-layer dielectric films from Agere Systems. The multi-layer films fabricated with the same materials will be discussed in the next chapter.

Two TEM images for Si3N4 from Agere are shown in Fig. 3.2. The unannealed Si3N4 showed excellent conformity and interface quality with a thickness of 6.4 nm (nominally 6 nm). After a high-temperature anneal at 1000°C, in Ar + 2000 ppm O2 for 15 minutes, the film was still very uniform, though a small amount of strain developed at the Si / Si3N4 interface. An aluminum cap was added after the annealing step. The film thickness remained remarkably constant after the high-temperature anneal and was found to be 6.6 nm.

![TEM images](image)

Fig. 3.2. TEM images of nominally 6 nm CVD Si3N4 from Agere. (a) the film before any annealing steps are taken. (b) the Si3N4 after a 15 minute anneal in Ar + 2000 ppm O2 at 1000°C.
The ALD Al\textsubscript{2}O\textsubscript{3} from Agere had good conformity, and the thickness of the unannealed film is quite uniform at 6.4 nm (nominally 6 nm). A TEM image for the unannealed Al\textsubscript{2}O\textsubscript{3} film is shown in Fig. 3.3. After a 15 minute anneal in Ar + 2000 ppm O\textsubscript{2} at 600°C, the film still had very good uniformity with a possible layer thickness increase to 6.7 nm as can be seen in Fig. 3.4(a). After 15 additional minutes of a 1000°C anneal in Ar + 2000 ppm O\textsubscript{2}, a significant interfacial layer developed (~3.5 nm) and some of the Al\textsubscript{2}O\textsubscript{3} layer was consumed, leaving a layer of 5.3 nm based on the TEM image in Fig. 3.4(b). Both of the films were capped by a 500 Å Al cap layer after the annealing step.

![Fig.3.3](image1.jpg)

**Fig.3.3.** Thin ALD Al\textsubscript{2}O\textsubscript{3} film from Agere before any annealing steps. Nominally 6 nm film is found to be amorphous and 6.2 nm thick with no interfacial layer. Silicon substrate is somewhat rough.

![Fig.3.4](image2.jpg)

**Fig. 3.4.** Thin Al\textsubscript{2}O\textsubscript{3} films (~6 nm) after annealing steps have been taken. (a) shows the film after a 15 minute, 600°C in Ar + 2000 ppm O\textsubscript{2}. The film appears to have increased slightly in thickness to 6.7 nm, and has a very thin visible interfacial layer (~1 nm). The film appears to have remained amorphous. (b) shows the Al\textsubscript{2}O\textsubscript{3} film after a similar anneal at 1000°C. The film has developed a thick interfacial layer (~3.4 nm). The film has not become crystalline, but appears to have developed striated layers. Both samples have a 500 Å Al cap layer.
The ALD HfO$_2$ from Agere had less ideal physical characteristics. Before any annealing, the film appeared to be quite rough as a result of the rough silicon surface on which it was grown. Also, traces of crystallinity were observed in the unannealed sample, while the thickness was fairly uniform at 6.1 nm (nominally 6 nm) with a possible interfacial SiO$_2$ layer of up to 3 nm. This film can be seen in Fig. 3.5. After a 15 minute anneal in Ar + 2000 ppm O$_2$ at 600°C, the film thickness appeared to increase somewhat to 6.5 nm, the amount of crystallinity increased and a significant interfacial layer was observed as shown in Fig. 3.6(a). With a 15 min anneal in Ar + 2000 ppm O$_2$ at 1000°C, however, the film appeared to be very damaged. The film was no longer uniform, is thicker (5.6 to 7.5 nm) and a large amount of strain with a thick interfacial layer was seen at the Si / HfO$_2$ interface in Fig. 3.6(b). Both of the annealed films had a 500 Å Al cap layer after the annealing step.

Fig. 3.5. Unannealed HfO$_2$ sample from Agere. The silicon / HfO$_2$ interface is found to be rather rough. The sample is semi-crystalline and ranges from 5.6 – 6.5 nm thick. A possible interfacial layer is < 3 nm thick.
3.3.2 ALD HfO$_2$ and Al$_2$O$_3$ from Harvard University

TEM images were taken of the single-layer Al$_2$O$_3$ and HfO$_2$ films that were grown at Harvard. Al$_2$O$_3$ can be seen in Fig. 3.7(a). It was found to be highly continuous and amorphous throughout its thickness of 15.7 nm. A thin interfacial layer (2.2 nm) was observed. HfO$_2$ can be seen in Fig. 3.7(b). It was found to be somewhat crystalline and rough, while being about 16.7 nm thick. A thin interfacial layer (2.2 nm) was observed. Both samples were annealed for 35 minutes in Ar + 2000 ppm O$_2$ at 600°C prior to TEM analysis.

Fig. 3.7. TEM images of single-dielectric layers from Harvard. (a) shows a nominally 15 nm Al$_2$O$_3$ film to be continuous, amorphous, and 15.7 nm thick. A thin interfacial layer can be seen and measures 2.2 nm thick. (b) shows a nominally 15 nm HfO$_2$ film to be slightly discontinuous, somewhat crystalline, and 16.7 nm thick. A 2.2 nm interfacial layer is observed. Each sample was annealed in Ar + 2000 ppm O$_2$ for 35 minutes at 600°C.
3.4 Electrical Characterization

3.4.1 Current-voltage measurements

Current-voltage (I-V) measurements were used to investigate the dependence of the electrical characteristics on the processing conditions. From I-V measurements we learn about the transport mechanisms and effective breakdown characteristics of the dielectric barriers.

I-V measurements were made using a Keithley 6430 Sub-femtoammeter. Front contacts were made by evaporating > 50 nm of aluminum through a bronze shadow mask. The gates were 0.6 or 1.2 mm in diameter. A portion of the dielectric on the front side was sputtered away with Ar\(^+\) ions in order to make back contact. The pressure during the sputtering process was ~1 x 10\(^{-4}\) torr. Generally, the cathode current on the Ion Tech 3 cm Kaufmann ion gun was kept at ~3 A while the discharge voltage was maintained at 55 V. The ion beam was perpendicular to the sample and sputtering was performed for about one minute to overetch the dielectric. The sample was immediately placed in the vacuum of the evaporator so that a native oxide would not form before the ohmic Al contacts could be made. I-V measurements between back contacts were made to verify that they were ohmic (< 20 Ω).

3.4.1.1 ALD HfO\(_2\), Si\(_3\)N\(_4\), and Al\(_2\)O\(_3\) from Agere Systems

The method for measuring the current-voltage (I-V) characteristics of the Agere samples was described in Sec. 3.4.1. As was learned in Sec. 3.4.1, Si\(_3\)N\(_4\) shows little physical change as a result of annealing. This was verified by electrical characterization. Fig. 3.8(a) shows three I-V curves for positive biases applied to the top gate contact. The
as-prepared sample was annealed for 15 minutes at 800°C and 900°C in N₂ + 10% H₂ and no significant changes in the I-V characteristics were observed. The hysteresis measured in the capacitance-voltage (C-V) curves shown in Fig. 3.8(b) is indicative of a significant density of defect states at the Si₃N₄ / Si interface corresponding to a charge trapping density of 1.2 x 10¹¹ / cm².

We fit the I-V curves with the effective mass model that was described in Chapter 2. The results are shown in Fig. 3.9(b). The best fit to our results indicates that the Si₃N₄ has a conduction band-offset of 4.2 eV and a thickness of 4.3 nm. Based on theoretical calculations in the literature, Si₃N₄ is expected to have a band-offset of 2.4 eV and we know from TEM that the thickness is ~6 nm. Despite the discrepancies such as these, which were found for each single-dielectric structure, the values obtained from I-V curves and the calculations can provide a lower bound on the thickness and an upper bound on the band-offset.
The electrical characteristics of Al$_2$O$_3$ from Agere were demonstrated to depend heavily on the anneal conditions. In Fig. 3.10(a), I-V curves for Al$_2$O$_3$ are shown for samples annealed at 800, 900, 1000, and 1100°C for 15 minutes in Ar + 2000 ppm O$_2$. The slopes of the I-V curves decrease with increasing anneal temperature, indicating an effective increase in dielectric thickness with increasing temperatures. Additionally, the breakdown voltage of the dielectric increases dramatically at higher temperature. While the unannealed sample shows significant leakage current, this can be greatly ameliorated through the proper annealing sequence. C-V curves for Al$_2$O$_3$ indicate that negligible charge trapping occurs in the annealed dielectric layer (see Fig. 3.10(b)).

Fig. 3.9. I-V data for 6 nm Si$_3$N$_4$ (blue curve) with effect mass model fit (red curve). Annealing conditions were 400°C in N$_2$ / 10% H$_2$ for 30 min. The best fit to the data was found to correspond to a 4.2 eV barrier that is 4.3 nm thick.
Further experiments were performed on the Al₂O₃ layers by varying the annealing ambient. As can be seen in Fig. 3.11, the symmetry of the I-V curves can be altered by adding a second annealing step in house N₂ (with 5% O₂). These annealing experiments demonstrate the need to standardize the processing conditions in such a way that a large interfacial layer is not created (see Sec. 3.3), but also emphasize the need to anneal to lower the leakage currents.

Fig. 3.10. Electrical characterization of 6 nm ALD Al₂O₃ from Agere. (a) shows I-V curves at various annealing temperatures. Anneals were done in Ar + 2000 ppm O₂ for 30 min. (b) shows C-V curves for the film with an anneal at 850°C in Ar + 2000 ppm O₂ for 15 min.
We fit the general symmetry of the Al\(_2\)O\(_3\) film that was processed with two annealing steps (700°C in Ar + 2000 ppm O\(_2\), 1000°C in N\(_2\)) and found that it corresponds to an effective double-layer structure as shown in Fig. 3.12(a). The barrier closest to the silicon substrate is found to be \(\sim\)2 nm and 2.9 eV tall, while the layer closer to the top gate contact is \(\sim\)2 nm and 6.6 eV tall. A schematic of this layered structure is shown in Fig. 3.12(b). The reverse symmetry would fit best for the annealing condition with only the Ar + 2000 ppm O\(_2\) step. The expected structure for Al\(_2\)O\(_3\) is a 2.8 eV barrier that is \(\sim\)6 nm thick. Explanations for the discrepancy include scattering or nonideal barrier structures which can clearly be seen by TEM (see Fig. 3.4). Interfacial layers (both above and below the Al\(_2\)O\(_3\) layer) were observed as well as morphology changes to the Al\(_2\)O\(_3\) itself.

![Graph](image-url)
HfO$_2$ was also studied under various annealing conditions in Fig. 3.13. The unannealed sample had very high leakage currents and an anneal was required in order to suppress this leakage. As was observed by TEM, this also grew a significant interfacial layer. I-V curves for 6 nm HfO$_2$ is shown in Fig. 3.13 at 400, 800, and 1000°C. The trends are similar to those observed for Al$_2$O$_3$ in Fig. 3.10, where the slope of the I-V decreased with increasing annealing temperature, indicating an effective increase in layer thickness. The breakdown voltage was seen to rise with increased annealing temperature, probably due to the growth of an interfacial layer such as that seen in Fig. 3.6(b).
The solid lines in Fig. 3.13 represent a fit of the effective mass model to the HfO$_2$ results. The fits show that the effective barrier increases with the annealing temperature. The barrier heights fit best for 2.5 eV and 4.0 eV (at 400°C and 1000°C) while the expected barrier height is 1.5 eV.$^1$ This is consistent with the observed growth of the interfacial layer seen by TEM (Fig. 3.6(b)). SiO$_2$ has a comparatively tall barrier height of 4.5 eV, which would account for the increase of the effective barrier height.$^5$ The simulation shows an effectively thin barrier which can be understood by the high leakage currents in the HfO$_2$ layer itself.

Clearly, there are many nonidealities in these samples. From these experiments we have learned that choosing an appropriate annealing temperature and ambient is critical to the performance of the dielectric barrier and that interfacial layers can be
controlled by the anneal temperature. Fitting the I-V curves with our effective mass model has produced limited success due to the difficulty in deconvoluting the transport mechanisms due to the barrier heights of each individual layer with each layer thickness. The failure to get quantitative band-off set measurements from I-V curves led us to develop internal photoemission measurements for accurate analysis of the barrier heights.

3.4.1.2 Temperature dependence of I-V measurements

Recently, it has been reported that, at room temperature, charge transport in high-quality HfO$_2$ is dominated by trap-assisted processes rather than by tunneling.$^4$ Additionally, it is well known that room temperature charge transport in Si$_3$N$_4$ is dominated by charge hopping or Frenkel-Poole emission.$^5$ In fact, there are three different types of transport that occur at different temperatures and electrical fields.$^6$ These can be seen in Fig. 3.14, which displays a plot of temperature vs. current density for Si$_3$N$_4.$$^5$
In Fig. 3.14, the current transport process described by $J_1$ (dominant at high temperatures and high fields) is associated with Frenkel-Poole emission, which is due to field-enhanced thermal excitation of trapped electrons into the conduction band and is defined by

$$J_1 = C_1 E \exp \left[ -\frac{q \left( \phi_b - \sqrt{qE/\pi\epsilon_f} \right)}{kT} \right],$$

(3.1)
where \( J_1 \) is the current density, \( E \) is the electric field, \( \phi_B \) is the barrier height (in eV), \( q \) is the charge on an electron, \( \varepsilon_i \) is the dielectric dynamic permittivity, \( k \) is Boltzmann’s constant, and \( T \) is the absolute temperature. \( C_1 \) is in terms of effective mass.

The transport process described by \( J_2 \) (dominant at high fields and low temperatures) is due to a Fowler-Nordheim tunneling process that is essentially independent of temperature. This tunneling behavior is described by

\[
J_2 = C_2 E^2 \exp \left( -\frac{E_2}{E} \right),
\]

where \( C_2 \) and \( E_2 \) are in terms of effective mass and barrier height.

The third transport process described by \( J_3 \) (dominant at low fields and high temperatures) is associated with thermally excited electrons hopping from one isolated state to another. This behavior, known as Schottky emission, is described by

\[
J_3 = A^* T^2 \exp \left[ \frac{-q \left( \phi_B - \sqrt{qE / 4\pi \varepsilon_i} \right)}{kT} \right],
\]

where \( A^* \) is Richardson’s constant, and the other variables are the same as defined for Eq. 3.1.

Low-temperature current-voltage measurements allow us to isolate standard tunneling effects from thermally-assisted transport mechanisms caused by trap states. Our model for barrier lowering assumes tunneling effects as the primary transport mechanism. A demonstration of barrier lowering at low temperatures would motivate the search for appropriate material stacks where tunneling is the dominant transport mechanism, assuring an increase in speed and retention time for room temperature devices.
Lack of access to a temperature-controlled I-V measurement station did not permit a full-scale study of I-V characteristics on temperature. However, we were able to make a brief comparison between Si₃N₄ and Al₂O₃ from Agere at room temperature and at 77K (or -196°C) by immersing the sample and probe in liquid N₂. The results in Fig. 3.15 indicate that these materials have limited thermal transport properties, due to the similarities of transport at 77K and at room temperature. For this reason, we can assume direct or Fowler-Nordheim tunneling (this will be described in Sec. 4.3) as the dominant electrical transport mechanism for these materials, making it likely that barrier lowering with heterostructures of these dielectrics can be observable at room temperature.

![Fig. 3.15. I-V curves of ALD films from Agere at room temperature and 77 K. (a) shows the result for 6 nm Al₂O₃. (b) shows the result for 4 nm Si₃N₄. No significant difference (or suppression) in transport is observed.](image)

### 3.4.1.3 I-V results for Harvard samples

I-V measurements on Al₂O₃ and HfO₂ from Harvard were performed to determine the leakage characteristics and breakdown voltages of these materials. Figure 3.16 shows
the results of these measurements. The films were each 6 nm thick and were annealed at 800°C for 15 minutes in Ar + 2000 ppm O₂. The breakdown voltages for Al₂O₃ were slightly higher than for HfO₂. The leakage currents for both these samples were found to be substantial for low voltages (µA), making it impossible to make useful fits with our effective mass model. As we will show in the next section, it is simple to determine useful information about the band-offsets of these materials at a wide variety of bias voltages using bias-dependent internal photoemission. Because very low leakage currents are required for internal photoemission measurements, we used thicker HfO₂ and Al₂O₃ films in the next section to determine the band-offsets of these materials.

3.4.2 Internal photoemission

3.4.2.1 Theory of internal photoemission

Internal photoemission spectroscopy is a simple optical method for gaining information about barrier heights, trap states and interface dipoles of a variety of materials. The advantages of internal photoemission were first demonstrated by Fowler.
in the 1930s. This powerful technique was later used in the 1960s to understand the Si/SiO₂, but was essentially forgotten until only recently, when it has seen renewed interest in order to gain information in high-κ dielectrics.

In internal photoemission, a bias is applied across a dielectric structure, while tunable monochromatic light shines on the sample. At a threshold photon energy, electrons from the substrate (or metal gate) are excited by internal photoemission over the dielectric barrier. This threshold energy corresponds to the barrier height of the dielectric. Using bias-dependent internal photoemission spectroscopy, a complete barrier height profile as a function of voltage can be obtained. By measuring the barrier height at both positive and negative voltages, band-offsets with respect to silicon (and also the metal gate) can be determined in addition to the flat-band voltage and barrier asymmetry at 0 V.

In order to obtain barrier heights for the semiconductor/dielectric interface, it is necessary to obtain the yield,

\[ Y = \frac{I \cdot \hbar \omega}{P} \]  

(3.4)

where \( I \) is measured current in amperes, \( P \) is the absorbed light power in watts, and \( \hbar \omega \) is the photon energy in eV, and \( Y \) is the yield in electrons/photon. Using Fermi-Dirac statistics, beginning with the number of electrons per unit volume, Fowler has derived an equation for \( Y \),

\[ Y \sim \frac{T^2}{\sqrt{E_x - \hbar \omega}} \left[ \frac{x^2}{2} + \frac{\pi^2}{6} \left( e^{-x} - \frac{e^{-2x}}{4} + \frac{e^{-3x}}{9} - \ldots \right) \right] \]  

(3.5)

where \( x \) is defined as
In Eq. (3.6) $k$ is Boltzmann’s constant, $T$ is temperature, and $\hbar \omega_o$ is the threshold photon energy. By considering only electrons with energy greater than $3kT$, $Y$ becomes

$$Y \sim (\hbar \omega - \hbar \omega_o)^2.$$  \hfill (3.7)

Taking the square root of $Y$ yields

$$\sqrt{Y} \sim \hbar (\omega - \omega_o).$$  \hfill (3.8)

When we substitute the barrier height $E_b$ for $\hbar \omega_o$ (the threshold photon energy), we find

$$\sqrt{Y} \sim \hbar \omega - E_b.$$  \hfill (3.9)

In the above equation, $E_b$ is the barrier height seen by the transported carriers coming from the metal. By plotting the square root of $Y$ versus the incident photon energy and extracting the linear region to the $x$-axis, a measure of the barrier height is obtained at the $x$-intercept. An example of this can be seen in Fig. 3.17.\footnote{Fig. 3.17. Plot of the square root of the quantum yield versus photon energy. Squares (blue line) and circles (red line) represent data obtained in this work for p- and n-type silicon specimens, respectively. The x-intercepts of each curve represent the barrier height. The triangles are data for photoemission from silicon into vacuum, and are shown to permit comparison of the thresholds for photoemission into vacuum and photoemission into SiO$_2$. From Ref. 13. Reprinted by permission of the American Physical Society.}
3.4.2.2 Image potential barrier lowering theory

As electrons approach a dielectric-metal or dielectric-semiconductor interface, image charges build up in the electrode. The potential associated with these charges reduces the effective barrier height. This barrier reduction is generally small compared with the barrier height itself. Nevertheless, it is not negligible, as will be demonstrated by our internal photoemission measurements. Figure 3.18 shows the resulting image potential barrier lowering for an electron that is nearing an arbitrary dielectric barrier.

![Image of barrier lowering](image.png)

Fig. 3.18. Energy-band diagram between a metal surface and a dielectric. The effective barrier height is lowered (from black line to dotted blue line) when an electric field is applied to the structure. The lowering is due to the combined effects of the field and the image force (solid blue line).

Our simulations for barrier lowering are based on a paper by J. G. Simmons.\textsuperscript{14} The image force was approximated as that of an insulator between two metallic electrodes. The silicon substrates used in our experiments are highly doped, so this is a valid approximation. The exact form of image lowering (in energy units) is given as

\[
V_i = \left( \frac{e^2}{4\pi\varepsilon} \right) \left[ \frac{1}{2x} + \sum_{n=1}^{\infty} \left\{ \frac{ns}{(ns)^2 - x^2} - \frac{1}{ns} \right\} \right]
\]

(3.10)
where $e$ is the charge of an electron, $s$ is the thickness, and $\varepsilon$ is the dielectric constant of the insulating layer. The distance of the electron from the first (source) electrode is $x$. When $x = s/2$,

$$V_i = -\frac{e^2}{2\pi\varepsilon s} \sum_{n=1}^{\infty} \frac{(-1)^n}{n} = -\frac{e^2}{2\pi\varepsilon s} \ln 2.$$  \hspace{1cm} (3.11)

As shown in Simmons, et al.,$^{14}$ a good approximation to the image expression in Eq. (3.10) is

$$V_i = -1.15\lambda s^2 / x(s-x) \hspace{1cm} (3.12)$$

where

$$\lambda = \frac{e^2 \ln 2}{8\pi\varepsilon s}.$$  \hspace{1cm} (3.13)

This approximation is used in the following the sections.

### 3.4.2.3 Experimental setup

In our experimental system, we utilize an Oriel 1000 W Hg-Xe lamp with an Oriel monochromator as our light source. We use a Keithley 6430 voltage source / femtoammeter to apply a bias across the sample and to measure the current at each bias. The system is computer controlled so that the light can be scanned from 1 eV to 6 eV at any bias and photon energy step size. A Newport multifunction optical meter 1835-C (with model 818-UV detector) is used to determine the lamp output spectrum to normalize the photoemission yield. Fused silica lenses are used to focus the light onto the top gold contact of the sample, which is held vertically. See Fig. 3.19 for a schematic of the sample setup.
Each sample that will be discussed in this chapter has a 12 nm gold top electrode (1.5 mm diameter), deposited by evaporation, which is sufficiently transparent so that the light source can photoexcite carriers in the silicon. Contact to this gate is made with a bent, springy piece of piano wire (Röslau, 4 mil) with 5 mm of gold wire (10 mil) at its end so the front gate will not be punctured. The ohmic “back” contact is a small amount of indium melted on the front side of the wafer. The sample is mounted vertically at the output of the monochromator and the exciting light beam is focused on the gold gate.

3.4.2.4 Internal photoemission experiments for single-layer dielectrics

3.4.2.4.1 Photon energy vs. current for thermally grown SiO₂

In order to verify that our experimental system and analysis were calibrated properly, we analyzed a thermally grown film of 15 nm SiO₂ on n-Si (1-10 ohm·cm doping). The current was measured as the photon energy was scanned at many voltages between -10 V and 10 V. Fig. 3.20 shows the raw current vs. photon energy spectra for a
variety of bias voltages (from -0.5 to +3.0 V). It is evident from these plots that the sign of the photocurrent depends strongly on the applied voltage, and the peaks in photocurrent correspond with the peaks in Hg-Xe lamp output (see Fig. 3.20 inset). For voltages from -10 V up to +0.7 V, negative currents were observed. At +0.7 V, the photocurrent switched signs and was positive for all higher positive voltages. We suggest that for positive photocurrents, collected electrons originate in the silicon, while the negative photocurrents indicate that electrons are mainly being generated in the metal gate contact. We determined 0.7 V to be the voltage where the currents from the metal matched those coming from the semiconductor. We expect this voltage to be close to flat-band for single dielectric layers.

Fig. 3.20. Current through 15 nm SiO₂ film as a function of incident photon energy. Inset: output spectrum of Hg-Xe light source.
3.4.2.4.2 Extracting the band-offsets of SiO₂ – comparison of models

As was described by Eq. (3.4) in Sec.3.4.2.1, each individual current vs. photon energy curve should be divided by the incident photon energy spectrum in order to calculate the yield. The square root, cube root, or 2/5 power of the yield are then plotted vs. photon energy, as shown in Fig. 3.21 for the 15 nm SiO₂ sample. The x-intercept is then extracted and is reported as the band-offset relative to the valence band of silicon. The literature is in general agreement that the square root is the appropriate power for intercept extraction when considering electrons emitted from a metal.\textsuperscript{12,15} However, when electrons are emitted from the semiconductor, there is still some debate about the correct power law. Semiclassical calculations suggest that taking a 2/5 power of the yield is correct\textsuperscript{16}, but a quantum mechanical correction to the theory predicts that the cube root is correct\textsuperscript{17}. In order to most thoroughly report the relevant results, we have computed offsets based on models assuming both the 2/5 power and the cube root of the yield for these situations.\textsuperscript{18}

![Fig. 3.21. Yield to the 1/3, 2/5, and 1/2 power vs. photon energy. A linear fit to these curves is extrapolated to the x-axis to provide the barrier height.](image-url)
3.4.2.4.3 Band-offset profile vs. photon energy for thermally grown SiO$_2$

After extracting band-offsets for each voltage, we obtain a barrier height profile as a function of voltage, as can be seen in Fig. 3.22 for 15 nm SiO$_2$. The points on the left of the vertical dotted line are for electrons emitted from the metal, the points on the right are for electrons emitted from the semiconductor. The band-offset varies greatly with applied voltage, and thus illustrates that it is of the utmost importance to report a corresponding bias voltage associated with a measured band-offset. We report our band-offsets as the point nearest to flat-band, where electrons are coming from the semiconductor, or in the case of our SiO$_2$ film, 4.13 ± 0.1 eV. When we subtract off the 1.1 eV SiO$_2$ band gap, we find that the Si/SiO$_2$ conduction band-offset is 3.03 ± 0.1 eV. Ultimately, our results for SiO$_2$ fit well to what is expected for a SiO$_2$ film with image potential barrier lowering (see Sec. 3.4.2.2). The image force was approximated as that of an insulator between two metallic electrodes. In general, the silicon substrates used in our experiments are highly doped, so this is a reasonable approximation. For SiO$_2$, we assumed an optical dielectric constant of 2.5.
Our successful measurement of the band-offset for Si/SiO₂ was important to validate our measurements of other high-κ dielectric material/Si band-offsets. These measurements will be discussed in the next sections as well as in Chapter 4 (for multi-layer materials).

3.4.2.4.4 Internal photoemission results for Agere samples

The amount of leakage occurring for the 6 nm Al₂O₃, 6 nm HfO₂, and 6 nm Si₃N₄ did not allow for internal photoemission experiments such as those performed for SiO₂ in 3.4.2.4.3. Because of greater flexibility in the growth parameters, we used thicker
dielectric samples grown at Harvard (in the next section) for our primary high-κ internal photoemission experiments.

3.4.2.4.5 Internal photoemission results for Harvard samples

Internal photoemission analysis similar to that shown for SiO₂ in Sec. 3.4.2.4.3 was completed for Al₂O₃ and HfO₂ on n-Si (0.0001 Ω·cm). The resulting photocurrent curves for the 15.7 nm Al₂O₃ sample shown in Fig. 3.7(a) are shown in Fig. 3.23. It can be seen that the dielectric layer has a low leakage current even at 4.0 V. Curves showing the square root of the yield at 3.5, 1.5, 0.0, -2.5 V are plotted in Fig. 3.24. The curves are very linear above a particular threshold voltage. Below the voltage at which the current switches sign (0.8 V in this case), a lower threshold voltage becomes dominant in the electron transport.

![Photocurrent spectra for Al₂O₃ from Harvard.](image)
The resulting photocurrent curves for the 15 nm HfO$_2$ samples in Fig. 3.7(b) are shown in Fig. 3.25. The sample has a significant amount of leakage above 0.7 V, likely due to the polycrystalline nature of the film. The leakage current is subtracted from the curves before the thresholds are calculated, but a larger amount of noise is observed in the resulting spectra for the higher positive voltages. Curves showing the square root of the yield at -1, 0.2, 0.9, 1.4 V are shown in Fig. 3.26. The curve for 0.9 V is not particularly linear as only a small amount of photocurrent is present in this case, giving small values for the calculated yield (current / incident lamp power). The smaller voltages are very linear, due to the large amount of signal and small amount of leakage. Larger positive voltages are noisier due to leakage (small signal to noise).
Fig. 3.25. Photocurrent spectra for 15 nm HfO$_2$ from Harvard.

Fig. 3.26. Curves showing the square root of the yield vs. photon energy for 15 nm HfO$_2$ from Harvard.
The resulting barrier height profiles and barrier height simulations for the Al₂O₃ and HfO₂ film are shown in Fig. 3.27. The measured barrier height (from the Si valence band) for 16.1 nm Al₂O₃ is $4.6 \pm 0.1$ eV (at 1.0 V). After subtracting the Si band gap (1.1 eV), the Al₂O₃ conduction band-offset is found to be $3.5 \pm 0.1$ eV (at 1.0 V), but this probably corresponds most directly to the interfacial layer than to the Al₂O₃ layer itself. For this reason, another quantity of interest is the Au / Al₂O₃ barrier, which is observed to be $3.5 \pm 0.1$ eV. The experimental literature reports conduction band-offsets of 2.78 eV and 2.15 eV for Al₂O₃, while theoretical calculations predict 2.8 eV.¹⁹,²⁰,²¹ The barrier height profiles for these two materials are not nearly as clear as for SiO₂ in Sec. 3.4.2.4.3. This is particularly true for HfO₂ – a result of leakage through the barrier and greater difficulty in extracting band-offsets from the yield curves. As we learned in 3.3.2 by TEM, interfacial SiO₂ layers were present between the dielectric and semiconductor. This interfacial layer could be attributed to the UV/ozone cleaning step during the substrate preparation or a post-deposition 600°C anneal in Ar + 2000 ppm O₂, and could account for the higher measured band-offsets compared with literature values, though the electrical characteristics of these layers are unknown. An area of additional interest is the asymmetry in the band-offset at the point at which the current switches signs (vertical lines in Fig. 3.22 and Fig. 3.27). Using a consistent set of parameters (Al₂O₃ $\kappa = 9$, SiOₓ $\kappa = 3.9$), this asymmetry can be understood to first order if we consider the charge that is generated in the metal compared with those originating in the silicon for the Au / Al₂O₃ / SiOₓ / Si barrier. The results for this simulation (accounting for Si depletion) are shown by the solid line in Fig. 3.27. The absence of the slope between 0 and 0.9 V is not well understood, but the fact that we can simulate the general shape of the profile and
accurately approximate the barrier heights for electrons coming from each electrode is very encouraging.

![Graph showing barrier height profile for HfO₂ and Al₂O₃ on n⁺-Si.]

**Fig. 3.27.** Barrier height profile for HfO₂ and Al₂O₃ on n⁺-Si. The data and image potential barrier lowering simulation curves on the left-hand side of the vertical dashed line represent negative photocurrents. The data and simulation curves on the right-hand side represent positive photocurrents. The open symbols and dashed lines are for HfO₂ while the solid symbols and solid lines are for Al₂O₃. Squares indicate data extracted from \( Y^{1/2} \) vs. energy curves (where \( Y = \text{yield} \)). Triangles correspond to \( Y^{2/5} \) data while circles correspond to \( Y^{6/5} \) data.

Similar analysis can be done for HfO₂ (open symbols in Fig. 3.27), but because of the degraded data quality attributed to leakage from the substrate, it is more difficult to verify our data by simulation. The dashed curve indicates an barrier lowering simulation for the HfO₂ barrier (HfO₂ \( \kappa = 22 \), SiOₓ \( \kappa = 3.9 \)). The data quality is quite good when the electrons originate from the metal (from -0.5 to 0.9 eV) and we can determine a Au /
HfO₂ barrier height of 3.6 ± 0.1 eV. Using the same reasoning as for Al₂O₃, based on our data, our best approximation for the Si / HfO₂ barrier height (from valence band) is 3.8 eV ± 0.2 eV. This corresponds to a conduction band-offset with respect to Si of 2.7 ± 0.2 eV. The experimental literature reports conduction band-offsets of 2.0 and ~1.2 eV for HfO₂, while theoretical calculations predict 1.5 eV.²²,²³,²¹ Further effects of barrier lowering in HfO₂ / Al₂O₃ heterostructures will be addressed in Chapter 4.²⁴

3.5 Conclusion

Two methods for determining band-offsets have been presented in this chapter: using I-V measurements to fit to an effective-mass tunneling simulation and using bias-dependent internal photoemission. It proved to be difficult to determine the band-offsets of single-layer dielectric materials due to the convolution of various parameters such as the effective thickness of the film and the barrier height. From our measurements, we learned that choosing an appropriate annealing temperature and ambient is critical to the performance of the dielectric barrier and that the formation of interfacial layers will greatly affect the electrical characterization. Fitting the I-V curves with our effective mass model produced limited success, prompting us to develop an alternative optical/electrical method called internal photoemission for more accurate analysis of the barrier heights.

Internal photoemission proved to be a better method for determining band-offsets for dielectric materials because it depends simply on the effective barrier energy, and is minimally affected by leakage or thickness of the film (as long as leakage is below a critical value (~pA). We combined our structural knowledge (TEM – Sec. 3.3) with the
electrical characterization results (Sec. 3.4) to help understand the band-offsets of single-layer deposited dielectrics. Using internal photoemission, we have been able to determine energy profiles as a function of voltage for SiO$_2$, Al$_2$O$_3$, and HfO$_2$. We have demonstrated the importance of knowing the voltage across the sample when reporting an effective barrier height, as the height depends heavily on the band-alignment of the sample.

In summary, we have employed a wide range of techniques to characterize the properties of single-layer dielectric films. We will utilize similar techniques in the next chapter to understand the properties of multi-layer dielectric films, to demonstrate barrier lowering in these structures, and we will then discuss the applications of these dielectric stacks in improving memory devices and in fabricating a tunable photodetector.

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References


Chapter 4  Optical and electrical characterization of layered tunnel barriers

4.1 Introduction

In Chapter 2, through simulations, the advantages of using layered tunnel barriers in memory devices were introduced. These advantages include improved speed and retention compared with standard Flash memory devices. Additionally, through literature searches and modeling, we determined the materials and heterostructures that would most likely demonstrate the desired effects (barrier lowering) when integrated in a device. In Chapter 3, using a number of materials characterization techniques, a better understanding of the properties of single-layer dielectric materials was gained. We used TEM, I-V characterization, and most significantly, bias-dependent internal photoemission to learn about single-layer dielectrics. In this chapter, a number of the same techniques will be employed to characterize the properties of layered structures of the dielectric materials characterized in Chapter 3. As will be shown, bias-dependent internal photoemission allows for definitive observation of barrier lowering behavior in dielectric heterostructures. This is the first demonstration of barrier lowering in the context of dielectric materials in conjunction with silicon and it confirms that this effect can be used in memory devices and also in a voltage-tunable detector application that will be discussed at the end of this chapter.
4.2 Characterization of heterostructures by TEM

TEM images of dielectric heterostructures were taken for definitive measurement of layer thicknesses. The results of these measurements will be discussed in this section.

4.2.1 TEM analysis of Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ from Agere

Materials analysis of the CVD Si$_3$N$_4$ and ALD Al$_2$O$_3$ films grown at Agere systems was described in Sec. 3.3.1. The heterostructures of these films were also analyzed. Figure 4.1 shows a bright-field TEM image of a Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ three-layer structure. Figure 4.1(a) shows the film with no annealing. Figure 4.1(b) shows the film with a 15 minute anneal at 1000°C in Ar + 2000 ppm O$_2$. The unannealed film shows thicknesses of 6.9 nm Si$_3$N$_4$ / 5.4 nm Al$_2$O$_3$ / 5.4 nm Si$_3$N$_4$ / n$^+$-Si while the annealed film seems to have decreased in total thickness to 5.3 nm Si$_3$N$_4$ / 3.9 nm Al$_2$O$_3$ / 5.4 nm Si$_3$N$_4$ / n$^+$-Si, though no interfacial layer has appeared. This is consistent with the observation in Sec. 3.3.1 that Si$_3$N$_4$ on Si forms no interfacial layer. The layers appear to be generally amorphous and uniform.

Fig. 4.1. TEM images for Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ heterostructures. (a) The film with no high-temperature anneal. (b) The film after a 1000°C anneal in Ar + 2000 ppm O$_2$ for 15 minutes.
Figure 4.2 shows a two-layer structure of Al$_2$O$_3$ / Si$_3$N$_4$ / Si. The film has been annealed for 15 minutes at 1000°C in Ar + 2000 ppm O$_2$. The film thicknesses were found to be 5.7 nm Si$_3$N$_4$ and 5.4 nm Al$_2$O$_3$. No interfacial layer was observed, even though an interfacial layer was observed in Sec. 3.3.1 for Al$_2$O$_3$ on Si. It can be concluded that Si$_3$N$_4$ acts as an O$_2$ diffusion barrier during the anneal.

4.2.2 TEM analysis of HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ from Agere

TEM analysis was also done for HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / n$^+$-Si grown at Agere and an image is shown in Fig. 4.3. The film was first annealed at 1000°C for 15 minutes in Ar + 2000 ppm O$_2$. A significant interfacial layer (~2.4 nm) was observed for this sample. The other layer thicknesses were found to be 5.6 nm HfO$_2$, 4.2 nm Al$_2$O$_3$, and 5.8 nm HfO$_2$. The interfacial layer is somewhat crystalline and the layers are not completely uniform. The top HfO$_2$ is fairly crystalline while the other high-κ layers are amorphous.
4.2.3 TEM analysis of HfO$_2$ / Al$_2$O$_3$ / Si and Al$_2$O$_3$ / HfO$_2$ / Si from Harvard

TEM analysis was performed on two films from Harvard. The first is Al$_2$O$_3$ / HfO$_2$ / n$^+$-Si. This film was annealed at 600°C for 35 minutes in Ar + 2000 ppm O$_2$. The resulting dielectric film is 16.1 nm Al$_2$O$_3$, 15.7 nm HfO$_2$, and 2.8 nm SiO$_2$ on Si and is shown in Fig. 4.4(a). The presence of an interfacial SiO$_2$ layer is not surprising because the wafer preparation at Harvard includes an ozone clean of the Si substrate directly before the dielectric deposition, as was discussed in Sec. 3.3.2. Some crystallinity is observed in the HfO$_2$ layer, though the Al$_2$O$_3$ appears to have remained amorphous. The films are not entirely uniform and some differences in the thicknesses of the layers are observed across the sample.

A TEM image of HfO$_2$ / Al$_2$O$_3$ / n$^+$-Si is shown in Fig. 4.4(b). The film was found to be composed of 13.8 nm HfO$_2$, 12.5 nm Al$_2$O$_3$, and 5.4 nm SiO$_2$ on Si.
4.3 Fowler-Nordheim analysis of layered barriers

4.3.1 Theory of Fowler-Nordheim tunneling

The injection mechanism for electrons to reach the floating gate in standard Flash memory (as shown in Fig. 1.1) is Fowler-Nordheim tunneling. To discharge the floating gate, a negative voltage is applied to the control gate, removing the electrons from the floating gate by the same mechanism. Fowler-Nordheim tunneling is what limits the speed of Flash memory.

Fig. 4.5. Conduction band diagram demonstrating Fowler-Nordheim tunneling. The black line represents the effective energy barrier for an electron with no bias applied. The blue dashed line represents the effective energy barrier for an electron with voltage V applied. In this case, the electron encounters a triangular barrier, the definition of Fowler-Nordheim tunneling.
When a large voltage is applied across a polysilicon / SiO₂ / silicon (floating gate / tunnel oxide / substrate) structure, its conduction-band structure will be influenced as indicated in Fig. 4.5. Due to the high electrical field present, electrons in the silicon conduction band will encounter a triangular energy barrier shown by the blue dashed line. This barrier has a width dependent on the applied field and a height dependent upon the conduction band-offset of SiO₂ on silicon. The current density in Fowler-Nordheim tunneling is given by\(^{123}\)

\[
J = \alpha E_{\text{inj}}^2 \exp \left[ \frac{E_o}{E_{\text{inj}}} \right]
\]

with

\[
\alpha = \pi m (e / h)^3 / \kappa_1^2
\]

and

\[
E_o = -2 \kappa \phi_b / e
\]

where \(E_{\text{inj}}\) = the electric field at the injection interface,

\(m\) = the mass of a free electron (9.1 x 10\(^{-31}\) kg),

\(e\) = the charge of a single electron (1.6 x 10\(^{-19}\) C),

\(h\) = Planck’s constant,

\(\kappa_1 = \kappa(\phi_b)\), the value of the imaginary wavenumber at the injection interface,

\(\kappa\) = average value of the imaginary wavenumber in the oxide barrier,

\(\phi_b\) = the energy barrier at the injection interface (3.2 eV for Si – SiO₂).
As can be observed in Eq. (4.1), the Fowler-Nordheim tunnel current density is exponentially dependent on the applied field. Plotting log\((J / E^2)\) versus \(1/E\), should yield a straight line with a slope that is related to the barrier height \(\phi_b\) in situations where Fowler-Nordheim tunneling dominates the current density.

### 4.3.2 Fowler-Nordheim plots

Based on the description in Sec. 4.3.1, by plotting log\((J / E^2)\) versus \(1/E\) from the I-V curves, we can learn about the effective barrier height of a structure by calculating the slope \(E_o\) (see Eqs. (4.1) and (4.3). Using this technique, we can compare the barrier heights of single-layer structures with those of multi-layer structures and determine the presence of barrier lowering by comparing the \(E_o\) values as a function of bias. Because of the heterogeneous nature of our barriers, it is not possible to extract an exact value for \(\phi_b\) because the value of the wavenumber throughout the structure depends on the particular material (see Eq. (4.3). We can compare the values for \(E_o\) (directly proportional to the barrier height) for different biases for a single sample, but not to other samples due to the difference in structure (and thus the effective wavenumber). An example of a Fowler-Nordheim plot for \(\text{Si}_3\text{N}_4 / \text{Al}_2\text{O}_3 / \text{Si}_3\text{N}_4\) is shown in Fig. 4.6.
4.3.2.1 $\text{Si}_3\text{N}_4 / \text{Al}_2\text{O}_3 / \text{Si}_3\text{N}_4$ samples from Agere

Figure 4.7 shows a summary of the results from the Fowler-Nordheim plots for $\text{Si}_3\text{N}_4$, $\text{Al}_2\text{O}_3$, and their three-layer heterostructure grown at Agere. The values of slope $E_0$ for these materials structures were determined from plots that are similar to Fig. 4.6. From the asymmetry in the slopes extracted for a single-layer of $\text{Al}_2\text{O}_3$ we can conclude that the $\text{Al}_2\text{O}_3$ does not have an inherently square shape, but is taller at the metal / $\text{Al}_2\text{O}_3$ interface. We have approximated this by drawing a triangular barrier for this structure under no bias. This is opposite to what would be expected based on the TEM results. In TEM (Fig. 3.3) we observed an interfacial layer between $\text{Al}_2\text{O}_3$ and the Si substrate that...
is presumably SiO₂. The SiO₂ at the interface would result in a taller barrier at the Al₂O₃ / Si interface. The Fowler-Nordheim plots, however, show that there is a strong effect at the Al / Al₂O₃ interface, possibly due to dipole layers at the Al surface or to an inherent asymmetry in the Fermi energies of the Al and the Si. On the other hand, under the two bias conditions, Si₃N₄ appears to have a very symmetric barrier. This is in fact consistent with the TEM results where no interfacial layer is observed.

<table>
<thead>
<tr>
<th></th>
<th>Al₂O₃</th>
<th>Si₃N₄</th>
<th>Si₃N₄, Al₂O₃, Si₃N₄</th>
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<td><strong>- bias</strong></td>
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<td></td>
<td>( E₀ = 1.5 \times 10^{10} )</td>
<td>( E₀ = 7.0 \times 10^{9} )</td>
<td>( E₀ = 8.9 \times 10^{9} )</td>
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<td><strong>+ bias</strong></td>
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<td><img src="image5" alt="Diagram" /></td>
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<tr>
<td></td>
<td>( E₀ = 4.4 \times 10^{9} )</td>
<td>( E₀ = 6.0 \times 10^{9} )</td>
<td>( E₀ = 1.7 \times 10^{9} )</td>
</tr>
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Fig. 4.7. Summary of results from Fowler-Nordheim plots for Si₃N₄, Al₂O₃, and the three-layer heterostructure grown at Agere. The values of slope \( E₀ \) are listed for positive and negative bias for each instance.

In the third column of Fig. 4.7, we have drawn a schematic of what is observed for a three-layer structure of Si₃N₄ / Al₂O₃ / Si₃N₄. By simply combining the results from the first two columns of Fig. 4.7, we can account for the asymmetry in the observed band-offsets (proportional to slope \( E₀ \)) for the three-layer structure, though there is no
specific reason to believe that the Al₂O₃ layer remains asymmetric because it is not in contact with Al in this case. However, the Fowler-Nordheim analysis indicates that this is indeed the case. The barrier the electrons encounter when coming from the silicon is smaller than that when electrons come from the metal. This can be attributed to the asymmetry of the Al₂O₃ barrier and the overall barrier lowering in the structures where the highest barrier (Al₂O₃) is limiting electron tunneling. In actuality, the results here are difficult to interpret as the wavenumber across the structure depends so much on the properties of each individual layer and the properties of the metal and silicon source electrodes.

As was discussed in Chapter 3, it is difficult to obtain useful information from standard I-V curves for single-layer samples, due to the difficulty of deconvoluting the layer thicknesses from the barrier heights and other nonidealities such as leakage and alternative transport methods. It is even more difficult to gain information from I-V curves for multi-layer samples such as Si₃N₄ / Al₂O₃ / Si₃N₄ yet we will show the result for this sample below. In Sec. 4.4, we will present results from bias-dependent internal photoemission, a much more efficient method for isolating information about the barrier heights of structures.

Shown in Fig. 4.8 are I-V curves for the three-layer structure 4 nm Si₃N₄ / 4 nm Al₂O₃ / 4 nm Si₃N₄ / n⁺-Si annealed at 200, 600, and 800°C for 30 minutes in N₂ + 10% H₂. As can be seen by the similarities in the I-V curves, the annealing conditions play a minimal role in determining the electrical characteristics. It appears that this three-layer sample is very stable.
Shown in Fig. 4.9(a) is an I-V curve for 4 nm Si$_3$N$_4$ / 4 nm Al$_2$O$_3$ / 4 nm Si$_3$N$_4$ / n$^+$-Si annealed at 850°C for 15 minutes in Ar + 2000 ppm O$_2$. Overlaid with this curve is a simulated I-V curve for a three-layer structure. Circled on this figure is the region of the I-V curve where we would observe barrier lowering. Indeed, we see a change in the slope of the I-V curve that could indicate barrier lowering. In Fig. 4.9(b), a schematic of the simulated barrier under negative bias is shown. The effective barrier found with our simulation is Si$_3$N$_4$ (4.2 eV, 2.7 nm) / Al$_2$O$_3$ (6.8 eV, 1.1 nm) / Si$_3$N$_4$ (4.2 eV, 2.7 nm). We conclude that these values are an upper bound on the barrier height and a lower bound on the layer thickness. The slope of the curve indicates that the film has more
leakage than an ideal sample would and this could account for the relatively low effective thicknesses. In Fig. 4.9(c), a schematic of the simulated barrier under positive bias is shown. The resulting three-layer fit is Si$_3$N$_4$ (4.2 eV, 2.7 nm) / Al$_2$O$_3$ (5.2 eV, 1.2 nm) / Si$_3$N$_4$ (4.2 eV, 2.7 nm). There is a slight asymmetry compared with the band-offsets under negative bias. We can attribute this to a difference in the Fermi level energies of the metal and semiconductor or to an asymmetry of an individual layer.

4.3.2.2 HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ samples from Agere

Figure 4.10 shows a summary of the results from the Fowler-Nordheim plots for HfO$_2$, and the two- and three-layer heterostructures with Al$_2$O$_3$ grown at Agere. The first
column shows a schematic for HfO$_2$, as determined by the $E_o$ values which are proportional to the barrier heights. It was found that the electrons coming from the Si substrate encounter a taller barrier than those coming from the Al gate contact. This is consistent with the interfacial SiO$_2$ layer observed by TEM for the HfO$_2$ / Si structure (see Fig. 3.5). For the multi-layer samples, we assumed the dielectric barrier heights would retain the barrier symmetry (or asymmetry) measured for the single-layer samples. The assumed symmetry only affects our schematic interpretation of the barrier height changes observed, not the measured $E_o$, which is proportional to the actual structure barrier height. The second column of 4.10 shows a schematic for a two-layer structure of Al$_2$O$_3$ / HfO$_2$ / Si. The two-layer structure shows clear asymmetry based on the source electrode and indicates barrier lowering is strongly occurring, as evidenced by the differences in the $E_o$ values. The $E_o$ values extracted from Fowler-Nordheim plots for the HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ structure (Fig. 4.10, column 3) yield additional evidence for barrier lowering, as demonstrated schematically. The overall barrier height indicated by the schematic in the third column agrees with the barrier information obtained from the one- and two-layer structures as well as with the calculated $E_o$ values.
Conclusions from I-V characterization

Using Fowler-Nordheim plots to analyze a single structure allows for direct comparison of barrier heights without interference of leakage effects (or effects based on sample thickness). In this section, Fowler-Nordheim plots were shown to be a useful method for understanding the effective barrier heights for a single sample under positive and negative bias. They have also demonstrated barrier lowering, showing particularly convincing and consistent evidence for the HfO$_2$ / Al$_2$O$_3$ structures (shown in Fig.10). I-V curves for Si$_3$N$_4$ / Al$_2$O$_3$ / Si$_3$N$_4$ were also presented in this section, but were not very conclusive due to the difficulty in deconvoluting the layer thicknesses from the barrier heights and other effects such as leakage and other transport nonidealities. As was shown
in Chapter 3, bias-dependent internal photoemission is a very good method for isolating information about the barrier heights of a structure provided the leakage currents are small. In the next section, bias-dependent internal photoemission measurements on multi-layer dielectric samples will be presented.

4.4 Internal photoemission analysis of layered barriers

4.4.1 Background

As demonstrated in Chapter 3, internal photoemission provides a reliable method for determining dielectric barrier heights and conduction band-offsets from silicon as a function of applied bias. Using the same methods as described in Sec. 3.4.2, we will analyze multi-layer dielectric samples. We utilize an electrostatic model (see Eqs. (2.9) – (2.13)) to calculate the electric field and subsequent voltage drops within each layer based on the dielectric constant and thickness of the individual layers. Doing this allows us to determine the barrier height of the dielectric layers in the heterostructures under all voltage conditions, based on the measured band-offsets in the high voltage ranges.

4.4.2 Analysis of HfO₂ and Al₂O₃ heterostructures from Harvard

4.4.2.1 HfO₂ / Al₂O₃ and Al₂O₃ / HfO₂ structures

As was shown by TEM in Sec. 4.2.3, the “two-layer” structures grown at Harvard are actually best described as three-layer structures due to the presence of an interfacial SiO₂ layer at the Si surface. The two samples that will be discussed in this section are 13.8 nm HfO₂ / 12.5 nm Al₂O₃ / 5.4 nm SiO₂ / n⁺-Si and 16.1 nm Al₂O₃ / 15.7 nm HfO₂ /
2.8 nm SiO$_2$ / n$^+$-Si. Internal photoemission data will be presented as well as consistent barrier height simulations based on the thicknesses and measured barrier heights for the individual layers.

### 4.4.2.1.1 Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si from Harvard

The barrier height profile as a function of voltage (as determined by internal photoemission measurement) for the 16.1 nm Al$_2$O$_3$ / 15.7 nm HfO$_2$ / 2.8 nm SiO$_2$ / n$^+$-Si sample grown at Harvard University is shown in Fig. 4.11. The analysis of this data is similar to that described in Sec. 3.4.2.4. The data on the left-hand side of the vertical dashed line represents the electrons excited from the metal electrode. On the right-hand side, the electrons are originating from the semiconductor. The squares on the right represent electrons coming from the valence band of the silicon (the two sets of symbols indicated values extracted from yield to the 2/5 and 1/3 powers). Additionally, we observed the presence of conduction-band emission as indicated by the circles on the right-hand side of Fig. 4.11. As was discussed in more detail in Sec. 3.4.2.4.2, we use yield$^{1/2}$ to calculate the band-offsets for the electrons coming from the metal. For the electrons coming from the silicon, we present results from both the yield$^{2/5}$ and yield$^{1/3}$.

The solid curved line in Fig. 4.11 represents a simulation based on electrostatics such as those described in Sec. 4.4.1. The simulation shown in Fig. 4.11 is derived from a consistent set of parameters for each layer: Al$_2$O$_3$ ($\kappa = 9$, thickness $s = 16.1$ nm, conduction band-offset (from Si) $\phi = 3.2$ eV), HfO$_2$ ($\kappa = 22$, $s = 15.7$ nm, $\phi = 2.7$ eV), and SiO$_2$ ($\kappa = 3.9$, $s = 2.8$ nm, $\phi = 2.7$ eV). The Si doping for each of the samples in this chapter is $2 \times 10^{21}$ atoms / cm$^3$. 
A barrier height profile for this sample is shown in Fig. 4.12. The y-axis represents the energy of the barrier in eV and the x-axis represents distance in Å. The lower set of curves shows the barrier under a variety of applied biases such that the electrons originate from the valence band of the silicon (the left-hand side). The upper set of curves shows the barrier under applied biases such that the electrons originate in the metal (also the left-hand side). The barrier height profile in Fig. 4.11 is derived from
individual voltage profiles such as those shown in Fig. 4.12. In each case, the effective barrier height is given by the maximum energy barrier to electron transport. The barrier to transport for electrons coming from the silicon is HfO₂, but as the voltage increases to above 2.0, the transport is completely dominated by the SiO₂ barrier (as indicated by the right-hand portion of Fig. 4.11). For electrons coming from the metal, the transport is primarily dominated by the Al₂O₃ barrier at all negative voltages (as is seen in the right hand portion of Fig. 4.11).

![Figure 4.12](image)

**Fig. 4.12.** Barrier height simulations for Al₂O₃ / HfO₂ / SiO₂ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). Each barrier height profile is for the indicated voltage. The overall voltage profile assumes that the highest point in the barrier limits the electron transport. The Schottky barrier height is 0.4 eV.
The raw current vs. voltage curves for this sample are shown in Fig. 4.13. The crossover voltage (from semiconductor to metal transport) is observed to be at 1.3 V, which is consistent with our simulations. Several curves showing the square root of the yield are shown in Fig. 4.14.

![Current vs. photon energy curves for Al₂O₃ / HfO₂ / Si.](image)
4.4.2.1.2 HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si from Harvard

The barrier height profile for 13.8 nm HfO$_2$ / 12.5 nm Al$_2$O$_3$ / 5.4 nm SiO$_2$ / n$^+$-Si is shown in Fig. 4.15. The observed profile under bias is different from that for the Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si sample in Sec. 4.4.2.1.1 as can be observed by the large peak at low voltages. The cause of this peak can be seen in Fig. 4.16.
Fig. 4.15. Barrier height profile as a function of voltage for HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / n$^+$-Si.

Fig. 4.16. Barrier height simulations for HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). The Schottky barrier height is 0.4 eV.
Fig. 4.16 shows the barrier profile at a number of applied voltages. The parameters for this simulation are: HfO₂ (κ = 22, s = 13.8 nm, φ = 3.6 eV), Al₂O₃ (κ = 9, s = 12.5 nm, φ = 3.6 eV), and SiO₂ (κ = 3.9, s = 5.4 nm, φ = 3.05 eV). When we analyze the barrier profiles with voltages above 0.45 V (the crossover voltage), the electrons are coming from the semiconductor. At 0.0 V (the black curve in Fig. 4.16), the electrons are being limited by the Al₂O₃ barrier. As the voltage is increased, due to the low dielectric constant of SiO₂, the voltage across this layer drops rapidly until the SiO₂ barrier (no longer the Al₂O₃ barrier) now limits the transport. This behavior accounts for the peak in Fig. 4.15. A similar situation is present for the case where the electrons come from the metal (upper set of curves), but because HfO₂ has a high dielectric constant, the drop across this layer is low and the barrier-lowering effect takes place across a wider range of voltages.

Fig. 4.17 shows the raw current vs. voltage curves for the HfO₂ / Al₂O₃ / SiO₂ grown at Harvard University. The crossover voltage is observed to be 0.5 V.
4.4.2.1.3 Summary of two-layer samples from Harvard University

The data for the HfO$_2$ / Al$_2$O$_3$ and Al$_2$O$_3$ / HfO$_2$ samples matches the simulated barrier height profiles remarkably well. We found that the conduction band-offsets from Si for Al$_2$O$_3$ and HfO$_2$ are very similar to each other (within 0.1 eV). The metal / HfO$_2$ barrier is found to be 3.6 eV, while the metal / Al$_2$O$_3$ barrier is found to be about 3.2 eV. The Si / SiO$_2$ barrier is somewhat different for each of the previous simulations, possibly due to nonstoichiometric films or silicate formation (HfSiO$_x$ or AlSiO$_x$). For the Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si sample, the conduction band-offset was found to be 2.3 eV. For the Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si sample, the conduction band-offset was found to be 2.65 eV.

The fact that we have been able to successfully match our experimental data with our electrostatic model in all voltage ranges for these two-layer samples is extremely encouraging and gives us confidence that the effects observed by our bias-dependent internal photoemission technique are real. In the next section, we will utilize similar techniques to analyze the three-layer structures from Harvard.

4.4.2.2 $HfO_2 / Al_2O_3 / HfO_2$ and $Al_2O_3 / HfO_2 / Al_2O_3$ structures

As was observed by TEM in Sec. 4.2.3, the deposited three-layer structures (HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / Si and Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ / Si) are in fact four-layer structures, caused by an interfacial layer between the Si and the bottom high-k dielectric layer. Due to low leakage in the samples, gathering the data for these samples proved to be easy, but fitting the data is more difficult, due to the extra layer parameter (compared with the samples in the previous section).
4.4.2.2.1 Al₂O₃ / HfO₂ / Al₂O₃ / SiO₂ / Si from Harvard University

The barrier height profile as a function of voltage for 15 nm Al₂O₃ / 15 nm HfO₂ / 15 nm Al₂O₃ / 2.5 nm SiO₂ / Si is shown in Fig. 4.18. The symbols represent the experimental data while the line represents a fit based on a consistent model that is discussed in the next paragraph. Two sets of yield¹⁄² data are shown in Fig. 4.18, corresponding to two thresholds that can be observed in the square root of the yield vs. energy data shown in Fig. 4.19. As shown by the dashed green dashed line in Fig. 4.19, two thresholds can be observed at voltages below -2 V, possibly corresponding to the hole and electron barrier to transport for carriers coming from the metal. The vertical line indicates the point at which the lower threshold begins to dominate as indicated by the arrows. A combination of the data from the two thresholds appears to correspond with the general form shown by our simulation in Fig. 4.18.

![Fig. 4.18. Barrier height profile as a function of voltage for Al₂O₃ / HfO₂ / Al₂O₃ / SiO₂ / n⁺-Si. Symbols are measurements from internal photoemission, the line is from an electrostatic simulation. The two sets of squares represent data extracted from two thresholds shown in Fig. 4.19.](image)

- 10 - 8 - 6 - 4 - 2 0 2 4 6 8 1 0

- 10 - 8 - 6 - 4 - 2 0 2 4 6 8 1 0

barrier height (eV)

Voltage (V)

1/2 fit between 4.1 and 4.5 eV
1/3
2/5
1/2 fit between 3.5 and 4.0 eV

upper threshold is strong

lower threshold is strong

Fig. 4.18. Barrier height profile as a function of voltage for Al₂O₃ / HfO₂ / Al₂O₃ / SiO₂ / n⁺-Si. Symbols are measurements from internal photoemission, the line is from an electrostatic simulation. The two sets of squares represent data extracted from two thresholds shown in Fig. 4.19.
Fig. 4.20 shows the simulated barrier profile at a number of applied voltages. The parameters for this simulation are:  \( \text{Al}_2\text{O}_3 \) (\( \kappa = 9, s = 13.5 \text{ nm}, \phi = 3.23 \text{ eV} \)), \( \text{HfO}_2 \) (\( \kappa = 22, s = 15.0 \text{ nm}, \phi = 3.3 \text{ eV} \)), \( \text{Al}_2\text{O}_3 \) (\( \kappa = 9, s = 15.0 \text{ nm}, \phi = 2.5 \text{ eV} \)), and \( \text{SiO}_2 \) (\( \kappa = 3.9, s = 2.5 \text{ nm}, \phi = 2.3 \text{ eV} \)). When we analyze the barrier profiles with voltages above 0.9 V (the crossover voltage), the electrons are coming from the semiconductor. At 0.0 V (the black curve in Fig. 4.20), the electrons are being limited by the \( \text{HfO}_2 \) barrier. As the voltage is increased, due to the lower dielectric constants of \( \text{SiO}_2 \) and the first \( \text{Al}_2\text{O}_3 \) layer, the voltage across this layer drops rapidly until the \( \text{Al}_2\text{O}_3 \) and then the \( \text{SiO}_2 \) barrier (no longer the \( \text{HfO}_2 \) barrier) now limits the transport. This behavior accounts for the peak in Fig. 4.18. In the case where the carriers come from the metal (upper set of
curves), the $\text{Al}_2\text{O}_3$ barrier nearest the metal limits the transport in almost all cases below the crossover voltage.

Fig. 4.21 shows the raw current vs. voltage curves for the Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ grown at Harvard University. The leakage through this sample is rather low up to voltages around 14 V. The crossover voltage is observed to be 0.9 V.

Fig. 4.20. Barrier height simulations for Al$_2$O$_3$ / HfO$_2$ / Al$_2$O$_3$ / SiO$_2$ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). The Schottky barrier height is 0.4 eV.
4.4.2.2 \( \text{HfO}_2 / \text{Al}_2\text{O}_3 / \text{HfO}_2 / \text{SiO}_2 / \text{Si} \) from Harvard University

The barrier height profile as a function of voltage for 15 nm \( \text{HfO}_2 / 15 \text{ nm } \text{Al}_2\text{O}_3 / 15 \text{ nm } \text{HfO}_2 / 2.5 \text{ nm } \text{SiO}_2 / \text{Si} \) is shown in Fig. 4.22. The solid symbols represent the experimental data while the line represents a fit based on the model that is discussed in the next paragraph. Generally, the simulation fits the data quite well, including the peak near the crossover voltage of 0.9 V.

Fig. 4.23 shows the simulated barrier profile at a number of applied voltages. The parameters for this simulation are: \( \text{HfO}_2 (\kappa = 22, s = 15.0 \text{ nm}, \phi = 3.7 \text{ eV}), \text{Al}_2\text{O}_3 (\kappa = 9, s = 135.0 \text{ nm}, \phi = 3.2 \text{ eV}), \text{HfO}_2 (\kappa = 22, s = 15.0 \text{ nm}, \phi = 2.6 \text{ eV}), \) and \( \text{SiO}_2 (\kappa = 3.9, s = 3.0 \text{ nm}, \phi = 2.6 \text{ eV}) \). When we analyze the barrier profiles with voltages above 0.9 V (the crossover voltage), the electrons are coming from the semiconductor. At 0.0 V (the black curve in Fig. 4.23), the electrons are being limited by the \( \text{HfO}_2 \) barrier farthest from the
silicon. As the voltage is increased, the voltage across the other layers drops rapidly until the Al$_2$O$_3$ and then the SiO$_2$ barrier (no longer the HfO$_2$ barrier) now limits the transport. This behavior accounts for the peak in Fig. 4.22. In the case where the electrons come from the metal (upper set of curves), the Al$_2$O$_3$ barrier nearest the metal limits the transport in all cases below the crossover voltage.

![Barrier height profile as a function of voltage for HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / n$^+$-Si.](image)

Fig. 4.22. Barrier height profile as a function of voltage for HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / n$^+$-Si.
4.4.2.2.3 Summary of three-layer samples from Harvard University

The three-layer samples grown at Harvard University displayed very low leakage, making characterization of their band-offsets via internal photoemission possible. Modeling the band-structure of these dielectric barriers was shown to be possible, yet due to the large number of parameters, more than one consistent solution for the barrier profile may exist. In these past sections, we have presented consistent models for the two structures. The fit for $\text{Al}_2\text{O}_3 / \text{HfO}_2 / \text{Al}_2\text{O}_3 / \text{SiO}_2 / \text{Si}$ matched the data at the high negative and high positive biases, and at more moderate voltages, there are indications that a combination of hole and electron transport is occurring. The fit for $\text{HfO}_2 / \text{Al}_2\text{O}_3 / \text{SiO}_2 / \text{Si}$ is represented in the following figure.

![Barrier height simulations for HfO2 / Al2O3 / HfO2 / SiO2 / Si.](chart.png)

Fig. 4.23. Barrier height simulations for HfO2 / Al2O3 / HfO2 / SiO2 / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). The Schottky barrier height is 0.4 eV.
HfO₂ / SiO₂ / Si successfully described our data in all voltage ranges. The general agreement of our simulations with the three-layer experimental data in these cases renders the presented results a success.

### 4.4.3 Analysis of Si₃N₄ samples from Agere

The barrier height profiles for the Si₃N₄ samples from Agere were measured. The Si₃N₄ / Al₂O₃ / Si₃N₄ / n⁺-Si sample (shown in Fig. 4.1) gave results that were difficult to interpret. The sample showed substantial charging, and subsequent energy scans at the same voltage gave different results due to this behavior. It was not possible to generate fits to this data. The Al₂O₃ / Si₃N₄ / n⁺-Si data, however, gave high-quality results and enable easy extraction of a barrier height at each voltage. The barrier height profile as a function of voltage for this sample is shown in Fig. 4.24. The parameters that were used in the barrier height simulation are Al₂O₃ (κ = 9, s = 13.8 nm, φ = 3.8 eV) and Si₃N₄ (κ = 7, s = 6.0 nm, φ = 3.7 eV) as seen in Fig. 4.25. Due to the low leakage and limited charging of the two-layer film, this is the first sample containing Si₃N₄ that we have successfully measured by bias-dependent internal photoemission. By subtracting the Schottky barrier height (0.4 eV), and the Si band gap (1.1 eV), we find that the conduction band-offset from Si to Si₃N₄ is 2.2 ± 0.1 eV, which corresponds well with the literature value of 2.4 eV (simulated). This value had not previously been measured experimentally.²
Fig. 4.24. Barrier height profile as a function of voltage for Al$_2$O$_3$ / Si$_3$N$_4$ / n$^+$-Si.

Fig. 4.25. Barrier height simulations for HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ / SiO$_2$ / Si. The upper curves represent the electrons coming from the metal (on the left). The lower curves represent the electrons coming from the silicon (also on the left). The Schottky barrier height is 0.4 eV.
4.5 Potential application: voltage tunable photodetector

As has been demonstrated in this chapter, total barrier lowering with applied voltage is indeed possible with multi-layer dielectric samples. As we described in Chapter 2, an application for these heterostructures is to use them as alternate tunnel barriers in Flash memory devices. These barriers should show enhanced performance compared with standard Flash memory through improved speeds and retention. However, an alternate application for these layered barriers exists.

We propose to use these bias-dependent heterostructures as a voltage-tunable photodetector. Our photodetector differs from other standard photodetectors because it doesn’t depend on the band gap of a given material, but rather on band-offsets of these materials from silicon. A schematic of the operation of this voltage-tunable photodetector is shown in Fig. 26. In Fig. 26(a), a layered barrier similar to that seen in Fig. 2.1(c) is shown, with no bias applied across it. Both high-energy (blue) and low-energy (red) photons are shown schematically shining on the sample. In this case, neither type of photon provides enough energy to the electrons in the metal to give transport and thus a measurable photocurrent. In Fig. 26(b), the same heterostructure is shown, this time with a voltage applied, giving an overall lower energy barrier. In this case, the high-energy photons transfer enough energy to an electron, such that a measurable photocurrent can be obtained. The low-energy photons do not result in a photocurrent. In this way, the barrier lowering effect that we have demonstrated can be used as a high-pass filter or a voltage-tunable photodetector.
Chapter 4 is the culmination of the work that has been presented in this thesis. The previous chapters were used to introduce the concept of layered tunnel barriers and to introduce techniques that can be utilized in order to characterize high-k dielectrics, including TEM, I-V measurements and Fowler-Nordheim plots, and finally bias-dependent internal photoemission, a valuable method for learning about conduction band-offsets with respect to silicon or the metal contact.

In this chapter, we have demonstrated by several methods, the presence of barrier lowering in multi-layer dielectric structures. First, we utilized I-V measurements and our effective model to understand the transport behavior of the heterostructures, yet it proved difficult to deconvolute the effects of the individual thicknesses of the layers from the effective barrier heights. Next, we utilized Fowler-Nordheim plots to compare the effective barrier heights of individual structures under positive and negative bias. This method showed indications that the interfacial layer observed by TEM at the Si interface,
played an important role in the electrical characteristics. This manifested itself in the asymmetry of slopes extracted from Fowler-Nordheim plots of Al₂O₃. The Fowler-Nordheim plots also gave consistent pictures when the results of HfO₂, Si₃N₄, and Al₂O₃, were combined to analyze the multi-layer structures.

However, we found that the best method for analyzing the effective barrier heights of multi-layer structures is voltage-dependent internal photoemission. Internal photoemission allowed us to focus directly on the barrier heights of the materials, rather than giving a convolution of the barrier height and the thickness of the materials. In this chapter, we have demonstrated barrier lowering effects for a number of heterostructures by analyzing the voltage profiles available from voltage-dependent internal photoemission. We were able to observe the effects of an interfacial layer at the Si surface and incorporated it into a model to understand our experimental data. In most cases, our model accurately describes our experimental data in all voltage ranges. Ultimately, barrier lowering was observed for HfO₂ / Al₂O₃ and Al₂O₃ / HfO₂ grown at Harvard University as well as for three-layer structures grown at Harvard and Agere Systems.

The described barrier lowering behavior is expected to improve the characteristics of Flash memory, including the speed of devices, the retention, and the reliability of the tunnel oxide. Also, in this chapter, a voltage-tunable detector has been introduced as an additional application of dielectric heterostructures and will utilize the barrier lowering behavior as a high-pass filter to detect the energies of the incident photons on the sample.
References


Chapter 5 Conclusion

The goal of this thesis has been to motivate and apply the idea of using layered tunnel barriers in standard nonvolatile memory devices (Flash). We have utilized a number of experimental and theoretical methods to analyze the physical and electrical properties of both single-layer and multi-layer dielectric barriers. Initially, we developed an effective mass model to simulate the current-voltage (I-V) characteristics of a number of dielectric heterostructures and used literature values for conduction-band-offsets and dielectric constants to design layered tunnel barriers that could exhibit barrier lowering behavior. We used TEM, I-V characterization, and developed bias-dependent photoemission to analyze single-layer dielectrics. We then used these techniques to analyze dielectric heterostructures. Finally, we simulated the effective band-offsets of our barriers as a function of voltage, and a comparison of our experimental and theoretical results confirmed the presence of barrier lowering.

5.1 Layered tunnel barriers: simulation and materials identification

Chapter 2 motivated our study of layered dielectric barriers and described our efforts in understanding and creating an ideal structure. In the context of improved memory characteristics, the concept of conduction band diagrams was introduced in order to intuitively compare layered barriers with homogenous ones and the intrinsic advantages of creating layered tunnel barriers. By choosing materials with appropriate varying band-offsets and dielectric constants, the overall barrier height seen by tunneling electrons across a tunnel barrier can be reduced by applying a voltage, improving both
the program and erase speed of floating gate memory devices without sacrificing their retention time.

Using an effective mass barrier transport model, calculated the current-voltage (I-V) characteristics that would optimize the layered tunnel barrier structure. Tunneling currents were calculated by numerical integration over energy and carrier angle of incidence and thus naturally include the transport mechanisms of thermionic emission, Fowler-Nordheim tunneling, direct tunneling, and tunneling through the Schottky barrier of silicon. An additional mathematical tool for studying the effects of layering dielectric materials and for an understanding of the amount of barrier lowering in an effective triangular tunnel barrier is to analyze the electrostatics of the structure.

The two mathematical methods that have been described give us some guidelines for picking appropriate materials to optimize barrier lowering. Namely, for a three-layer structure, the center layer material should have a high dielectric constant and a relatively high band-offset relative to silicon (2.5 to 3.5 eV). The material in the outer two layers should have a lower band-offset relative to silicon (1.0 to 1.5 eV) and a lower dielectric constant.

Though the number of measurements of band-offsets of high-κ materials in the literature is small, after a thorough literature search of both theoretical and experimental work, we were able to compile a complete list of high-k materials, their band-offsets, and their dielectric constants. This list enabled us to choose materials structures to study in more detail using our mathematical tools. The structures we chose to analyze in detail are: \( \text{Si}_3\text{N}_4 / \text{Al}_2\text{O}_3 / \text{Si}_3\text{N}_4, \text{ZrSi}_x\text{O}_y / \text{Al}_2\text{O}_3 / \text{ZrSi}_x\text{O}_y, \) and \( \text{HfO}_x / \text{Al}_2\text{O}_3 / \text{HfO}_2. \)
Through the simulations and literature searches in Chapter 3, we confirmed the potential advantages of layered barriers and have identified the structures that should result in the most improved characteristics in terms of a memory device.

5.2 Analysis of single-layer dielectrics: Bias-dependent internal photoemission and materials characterization

In Chapter 3, we used the knowledge gained from simulations presented in Chapter 2 to design and fabricate multi-layer dielectric samples. There are two main sets of samples. From Agere Systems, we obtained Si$_3$N$_4$ / Al$_2$O$_3$ and HfO$_2$ / Al$_2$O$_3$ heterostructures on silicon. From Harvard University, we obtained HfO$_2$ / Al$_2$O$_3$ heterostructures on silicon. The samples were grown on highly doped silicon to decrease the silicon depletion layer and enabled easy electrical analysis. Though multi-layer sample design was described in this chapter, only the single-layer samples were characterized. The characterization of the multi-layer samples was presented in Chapter 4.

A series of annealing studies was performed on single-layer with the purpose of diminishing the defect density and decrease leakage currents. Transmission electron microscopy (TEM) was used to study the materials structure as a function of the annealing conditions. In the single-layer Al$_2$O$_3$ and HfO$_2$ films, the annealing temperature was found to be highly correlated with the growth of interfacial layers between the dielectric and the silicon substrate.

Next, current-voltage (I-V) measurements were used to investigate the electrical characteristics of the dielectric films on processing conditions. These I-V curves were fit
by the effective mass model described in Chapter 2, allowing for the extraction of thicknesses and barrier heights of the materials. Because of the non-idealities observed in the film (also shown by TEM), it was difficult to deconvolute the effects of the high-k layer, possible interfacial layers, and the nonidealities caused by leakage currents, charging, and defects in the sample.

The difficulties in quantifying the properties of the dielectric barrier by I-V characterization led us to develop the technique called bias-dependent internal photoemission. Internal photoemission spectroscopy is a simple optical method that can be used to gain information about barrier heights of dielectric materials. In this method, a bias is applied across a dielectric structure, while tunable monochromatic light shines on the sample. At a threshold photon energy, electrons from the substrate (or metal gate) are excited by internal photoemission over the dielectric barrier. This threshold energy corresponds to the barrier height of the dielectric. We developed bias-dependent internal photoemission spectroscopy, a technique which enables us to determine a barrier height profile as a function of voltage. By measuring the barrier height at both positive and negative voltages, band-offsets with respect to silicon (and also the metal gate) were found in addition to the flat-band voltage and barrier asymmetry at 0 V. In Chapter 3, the results of our internal photoemission measurements were presented for single-layer SiO$_2$, Al$_2$O$_3$, and HfO$_2$. The barrier heights were extracted by this method and were compared with literature values.
5.3 Optical and electrical characterization of layered dielectric barriers

In Chapter 4, we brought together what we learned about layered tunnel barrier design in Chapter 2 with what we learned about characterization of band-offsets with respect to silicon in Chapter 3. We presented materials characterization results for Si₃N₄ / Al₂O₃ and HfO₂ / Al₂O₃ heterostructures. We utilized TEM and I-V characterization to analyze these samples. Additionally, we used Fowler-Nordheim plots based on I-V data to compare about the positive and negative bias-dependence within a single sample, giving us information on the barrier height and asymmetry. This analysis showed good evidence that barrier-lowering is indeed occurring within our multi-layer samples. It also enabled us to understand the effects the interfacial layers at the Si surface have on both the single-layer dielectrics and the multi-layer samples.

Finally, we utilized bias-dependent internal photoemission to construct a barrier profile for our multi-layer samples. Using this method, we have demonstrated the barrier lowering effect in a number of samples grown at Harvard University and Agere Systems. Additionally, we have developed a consistent model for the barrier height as a function of voltage for each heterostructure and find that our results agree with our experimental data, most notably for the HfO₂ / Al₂O₃ and Al₂O₃ / HfO₂ structures.

Barrier lowering in these heterostructures can be used in Flash memory devices, as has been discussed. In Chapter 4, we introduced a new application called a voltage-tunable detector that will utilize these layered dielectric barriers as a high-pass filter and will detect the energies of photons that are incident on a sample.


5.4 Device measurements and design

In Appendix A, we describe how to design and measure devices that integrate layered tunnel barriers. Capacitor structures that incorporate poly-silicon floating gates and layered tunnel barriers were fabricated and the characteristics analyzed. The results, however, are somewhat inconclusive without a more thorough study of devices with both single-layer, double-layer, and triple-layer dielectrics. To this end, we have described a complete method for fabricating a set of ring-gate transistors (and other devices) that can be used to easily compare the characteristics of standard Flash memory with memory devices that integrate layered tunnel barriers.

5.5 Future steps to be taken

The completion of the transistor measurements outlined in Appendix A will provide us with a wealth of knowledge about the performance of the Flash memory devices that integrate layered tunnel barriers and will potentially motivate the semiconductor industry to create state-of-the-art transistor technologies based on our research. An additional path for applied device research is to fabricate voltage-tunable photodetectors fabricated from layered dielectric barriers.

A more fundamental application of the work presented in this thesis would be to utilize our bias-dependent internal photoemission to analyze the band-offsets of a wider variety of dielectric materials including III-V materials, organic materials, or carbon nanotubes.
Appendix A  Device measurements and design

A.1 Introduction

Chapters 1-5 of this thesis have established the basis of our interest in layered tunnel barriers and have demonstrated the barrier lowering behavior that could improve the speed and retention of Flash memory devices. The ultimate goal of our work is to create a functioning memory device utilizing these new tunnel barriers and to demonstrate their improved performance. This appendix describes some preliminary measurements of MOS capacitors, outlines a complete method for fabricating ring-gate transistors, and gives details on specific device dimensions and processing procedures based on film stacks that will be fabricated at IBM in Yorktown Heights during the Spring/Summer of 2004.

A.2 Fabrication and design of MOS transistors from Agere samples

A.2.1 Description of gate stack

Four different wafers were used to form the MOS capacitors, and all were from Agere Systems as described in Chapter 2. The fabrication began on lightly doped p-type silicon (~10^{15} boron atoms / cm^3) and the general gate stack is shown in Fig. A.1. Four types of MOS capacitors were fabricated, differing in their tunnel barrier configuration:

1) 6 nm SiO₂,
2) 6 nm HfO₂,
3) 6 nm HfO₂ / 6 nm Al₂O₃, and
4) 6 nm HfO$_2$ / 6 nm Al$_2$O$_3$ / 6 nm HfO$_2$.

On top of these layers, 8 nm of poly-silicon was deposited through a silicon mask in the Atwater Group’s molecular beam epitaxy (MBE) system. Following deposition of this layer and an 800°C anneal, 15 nm of SiO$_2$ was deposited at International Wafer Service. The final metallization was performed in an Edwards evaporator at Caltech.

![Fig. A.1. Structure of an MOS capacitor. The tunnel oxide is typically an SiO$_2$ layer, but a layered tunnel barrier can also be integrated.](image)

### A.2.2 Materials processing details

The poly-silicon deposition step described in Sec. A.2.1 was performed at 3 x 10$^{-8}$ torr. The growth rate was about 0.5 Å / sec, and the final deposition thickness was 8 nm. The poly-silicon was deposited through a silicon mask that was fabricated at Lenox Laser. Holes of 1/4, 3/16, 1/8, and 1/16 inch diameter were made in a silicon wafer as shown in Fig. A.2, to form a mask for deposition of the floating gate. The resulting circular poly-silicon gates formed the floating gate where charge would be stored.
After the deposition of the poly-silicon, the wafers were annealed at 800°C in Ar + 2000 ppm O₂ for 15 minutes to crystallize the silicon layer and to free the film of defects. Next, a blanket SiO₂ layer was deposited at room temperature at International Wafer Service. The base pressure of the chamber was 2 x 10⁻⁸ torr.

The top metal contacts were deposited through a stainless steel mask with holes similar to those in Fig. A.2. However, each hole diameter was half the size of the corresponding hole in the Si mask for easy alignment (1/8, 3/32, 1/16, 1/32 inch diameter). The Al contacts were 50 nm thick, deposited in an Edwards evaporator at a rate of 2 nm/sec. The back contacts were made after scratching the back of the wafer with a diamond scribe so the blanket Al layer would penetrate the native oxide. The back aluminum layers were 50 nm thick.

**A.3 Device characterization**

The number of devices fabricated by this method was very limited, and only two of the four had low enough currents (low enough conductances) through the sample that proper capacitance-voltage (C-V) curves could be obtained. The two samples whose characteristics could be acceptably measured were the ones with the 6 nm SiO₂ tunnel barrier and the 6 nm HfO₂ / 6 nm Al₂O₃ / 6 nm HfO₂ tunnel barrier. The measurements
were made using a Keithley 590 C-V meter and Metrics ICS electrical characterization software. The useful measurements that can be performed on these types of devices include:

1) Charge storage: By reading off the capacitance of the device before and after high voltage is applied, and by observing the flat-band voltage shift ($\Delta V_{FB}$), we can learn whether the device can store charge.

2) Device speed: By using short, controlled voltage pulses, and observing $\Delta V_{FB}$, we can learn how quickly carriers can be transported across the tunnel. By comparing three-layer tunnel barrier structures with homogeneous tunnel barrier structures, we can learn whether barrier lowering allows for improved speeds.

3) Charge retention: By observing the flat-band voltage shift, we can also determine how well the layered tunnel barriers retain charge on the floating gate.

4) Endurance: By sequentially writing and erasing the device, information about the long-term performance of similar devices can be gathered.

The device measurements that were possible for our samples are described in the next section.

**A.3.1 MOS capacitor measurements: SiO$_2$ tunnel oxide**

C-V characteristics were performed on the SiO$_2$ tunnel oxide MOS capacitor sample described in Sec. A.3. The first experiment performed was a C-V scan from -3 V to 2 V to verify proper characteristics in which the doping of the silicon could be identified as well as the accumulation and depletion regions of the C-V sweep.

Following this verification, an experiment to determine the required programming voltage of the capacitor was performed and is shown in Fig. A.3. The C-V curves are
shown in Fig. A.3(a). The curve for the erased device has had a -3.2 V pulse applied for 20 seconds. The results for the programmed devices have had the specified voltage applied for 50 seconds and are indicated by the colored curves in Fig. A.3(a). As can be seen, a larger C-V shift can be observed for larger program voltages. Ultimately, the magnitude of this shift, the flat band voltage shift $\Delta V_{FB}$, can be plotted vs. programming voltage as is shown in Fig. A.3(b). It is clear from this graph that a significant amount of programming (0.5 V flat band shift) can be obtained for all programming voltages above 2.7 V.

After the necessary programming voltages had been determined, an experiment to determine the programming time of the capacitor was performed and the results are shown in Fig. A.4. The C-V curves are shown in Fig. A.4(a). The green sweep is considered to represent the erased device, i.e., a device that has had -3.2 V applied for 20 seconds. Following an erase pulse, the device had a single “program pulse” of 3 V applied for a specific length of time. As can be seen, a larger C-V shift can be observed
for longer pulse times. Ultimately, the magnitude of this shift, the flat band voltage shift $\Delta V_{FB}$ can be plotted vs. the programming pulse time as shown in Fig. A.4(b). The programming of the device is seen to be rather slow, with $\sim 15$ sec required to obtain a $\Delta V_{FB}$ of 0.5 V.

A third experiment performed on the MOS capacitors with the SiO$_2$ tunnel oxide was used to determine how long the charge remains in the device after programming. These results are shown in Fig. A.5. The black curve in Fig. A.5(a) shows the C-V characteristics for a programmed device after a 3.0 V, 20 second pulse. The colored curves represent the measured C-V results at specific times after the programming has been completed. As can be seen, the charge leaves the device rather quickly, a 0.5 V flat-band voltage shift being observed after $< 200$ seconds. Fig. A.5(b) shows the flat-band voltage shift as a function of time. A clear, continuous decrease in the stored charge is demonstrated in this graph.

Fig. A.4. Capacitance-voltage (C-V) characteristics based on program times for MOS capacitor with SiO$_2$ tunnel oxide. (a) shows the C-V data at different programming times at 3.0 V. The black curve represents an erased device (-3.2 V for 20 seconds). (b) shows the flat-band voltage shift as a function of programming pulse time.
Calculations were performed to determine the expected capacitance for the SiO$_2$ tunnel oxide device. The oxide capacitance was calculated as shown in Fig. A.6 using

$$C_o = \frac{C_c C_t}{C_c + C_t}, \quad (A.1)$$

with

$$C_c = \frac{\kappa_c \varepsilon_o A_G}{x_c} \quad \text{and} \quad C_t = \frac{\kappa_t \varepsilon_o A_G}{x_t}, \quad (A.2)$$

where $\kappa_c$ and $\kappa_t$ are the average dielectric constants of the control oxide and tunnel oxide, respectively, $\varepsilon_o$ is the dielectric permittivity of free space, $A_G$ is the gate area, and $x_c$ and $x_t$ are the thicknesses of the control oxide and tunnel oxide, respectively. The semiconductor capacitance was calculated using

$$C_s = \frac{\kappa_c \varepsilon_o A_G}{W}, \quad (A.3)$$

Fig. A.5. Capacitance-voltage (C-V) characteristics based on program times for MOS capacitor with SiO$_2$ tunnel oxide. (a) shows the C-V data at different times after an initial program voltage of 3.0 V for 20 seconds (shown by the black curve). (b) shows the flat-band voltage shift as a function of the amount of time after the initial program pulse.
where $\kappa_s$ is the dielectric constant of silicon, $\varepsilon_0$ is the dielectric permittivity, $A_G$ is the gate area, and $W$ is the depletion width of the silicon given by

$$W = \left[ \frac{2\kappa_s\varepsilon_0}{qN_A} \phi_s \right]^{1/2},$$  \hspace{1cm} (A.4)

with $N_A$ as the total number of acceptor atoms or sites per cm$^3$ and $\phi_s$ as the semiconductor surface potential.\(^1\) The depletion capacitance is determined by calculating the oxide capacitance and semiconductor capacitance in series,

$$C(\text{depI}) = \frac{C_oC_s}{C_o + C_s}.$$ \hspace{1cm} (A.5)

Using Eqs. (A.1) and (A.2), the expected value for the oxide capacitance was calculated to be 815 pF. From Eqs. (A.3) – (A.5), the expected depletion capacitance is calculated to be 232 pF. The actual measured oxide capacitance was 134 pF and the
depletion capacitance is 42 pF, as can be seen in Fig. A.1. Without better information on the individual layers of the gate stack, it is difficult to determine the reason for the low measured capacitances. It is possible that the layer thicknesses deposited are slightly different than the assumed values. Also, it is possible that we have an unintended series resistance in the circuit, such as between the measurement probe and the gate contact or from poor quality penetration of the native oxide on the backside of the wafer, both of which would give rise to a lower measured capacitance.

A.3.2 MOS capacitor measurements: HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ tunnel oxide

The next MOS capacitor structure we successfully analyzed was similar to the structure in Fig. A.1, but the tunnel oxide is a multi-layer structure of 6 nm HfO$_2$ / 6 nm Al$_2$O$_3$ / 6 nm HfO$_2$. We performed experiments similar to those described in the previous section in order to determine the programming and erase voltage and speed capabilities of these devices.

Figure A.7(a) shows the “program” characteristics compared with the fully erased device. The erase pulse used was 20 seconds at -3.2 V and is shown by the black C-V curve. The other colored curves show the C-V curves at a variety of voltages, all held for a period of 20 seconds. As can be seen in Fig. A.7(b), there is very little difference in the flat-band voltage shift (compared with the erased curve) at applied voltages of 2.2 – 3.0 V. In fact, the “programmed” curves for these voltages appear to be the same as the curve with no voltage applied (the purple curve). The difference between the erased device and the programmed device is clear, but it appears that we can’t program with
voltages higher than 3.4 V because the capacitor breaks down (indicated by flat C-V curves and high conductances).

Figure A.8 shows the results for short voltage pulses from the initial erased state (-3.2 V, 20 seconds). The C-V curves are shown in Fig. A.8(a) and a clear trend can be observed. This trend is shown more specifically in Fig. A.8(b) – the flat-band voltage shift generally increases with longer write times (from .5 to 20 seconds). However, as was observed in Fig. A.7, the shift to the “program” state is not significantly different from the relaxed or uncharged state. Fig. A.8 simply gives us an idea of how fast we can remove the device from its erased state.
Figure A.9 shows the results for an erase study of the device. The programmed device is shown by the black curve (3 V, 20 sec applied bias). Curves for a device erased for different periods of time (at -3.2 V) are shown by the colored curves in A.9(a). A summary of the results (referenced to the programmed curve) are shown in Fig. A.9(b) in terms of the flat-band voltage shift vs. the erase time. The erase times are clearly related to the flat-band voltage shift. It is observed that we can erase the device more fully with longer erase pulses.

Fig. A.9. Capacitance-voltage (C-V) characteristics based on erase times for MOS capacitor with an HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ tunnel oxide. (a) shows the C-V data for a device which has been erased at -3.2 V for varying times. The black curve represents a programmed device (3.0 V for 20 seconds). (b) shows the flat-band voltage shift as a function of erase time.
Finally, we observed the permanence of the erase state as a function of time. The fully erased C-V characteristics are represented by the black curve in Fig. A.10(a). The colored curves show the changes in the C-V characteristics after the initial erase pulse (-3.2 V, 20 sec). Figure A.10(b) shows the flat-band shift of theses curves compared with the erase curve as a function of time. As can be seen, the device quickly drifts back to its stable uncharged state within 30 seconds.

Following Eqs. (A.2) – (A.5), the expected capacitances for the HfO₂ / Al₂O₃ / HfO₂ tunnel oxide MOS capacitor can be calculated. The oxide capacitance is found to be 234 pF and the depletion capacitance is 136 pF. As was seen for the SiO₂ tunnel oxide sample, the measured capacitances for this sample are low, with the oxide capacitance being 188 pF and the depletion capacitance being 66 pF.
A.3.3 MOS capacitor result summary

In summary, while clear charged and erased states can be observed for both the SiO$_2$ tunnel oxide sample and the HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ tunnel oxide sample, a comparison of the results is inconclusive. The measured capacitances are lower than the predicted values for each sample structure, possibly due to poor contacting of the sample or other nonidealities in the samples which were discussed in more detail in Sec. A.3.1. The SiO$_2$ sample shows distinct program and erase curves, while the stable uncharged state lies in between. The charge can be stored or erased for short periods of time (30 seconds) but the device tends to drift back to its uncharged state. On the other hand, the HfO$_2$ / Al$_2$O$_3$ / HfO$_2$ sample shows a distinct erase curve but the programmed state is not obtainable before the capacitor breaks down. In order to draw better conclusions about the differences in speed between devices with single-layer tunnel oxides and multi-layer tunnel oxides, a more complete experimental design is required. In the next section, an experiment is outlined such that we can obtain a better comparison of the speed of transistors integrating a variety of tunnel oxides so that we can more clearly identify the advantages of using multi-layer structures that were described in Chapter 1.

A.4 ALD HfO$_2$ and Al$_2$O$_3$ gate stacks to be fabricated at IBM

A.4.1 Description of samples obtained from IBM

To determine the device structures that are most likely to demonstrate the barrier lowering effect, and thus improved electrical characteristics, we have simulated the tunnel current and the resulting volume charge density in complete MOS structures, with
the goal of designing MOS transistors. An example of these simulations is shown in Fig. A.11. The right-hand axis of the figure shows the barrier height relative to the Fermi level. The conduction band throughout the structure under a 0 V bias is indicated by the black solid line. The conduction band throughout the structure under a 4 V bias is indicated by the pink dotted line. The structure here consists of a silicon substrate (below 900 Å on x-axis), 3 nm HfO₂, 3 nm Al₂O₃, 5 nm undoped silicon floating gate, and a 12 nm SiO₂ control oxide layer, followed by an aluminum gate contact. Superimposed with this conduction band diagram is the volume charge density at each position of the barrier. This is indicated by the left-hand axis. The charge density under a 0 V bias is shown by the blue solid line, and the purple dashed line indicates the charge density under a 4 V bias. It can be seen that under bias, the charge density in the well can be increased by 15 orders of magnitude, yet the amount of charge that is transported through the entire structure is negligible. These simulations enable us to compile the list of desired structures shown in Table A.1.
Samples 1 – 19 in the Table A.1 are the MOS capacitor stack structures that will be fabricated at IBM (Evgeni Gousev, Yorktown Heights). Single-, double-, and triple-layer tunnel barriers are described. The single layers will demonstrate the effects of standard tunnel barriers and will provide a comparison for the double and triple-layered tunnel barriers where barrier lowering is expected. The double-layered structures consist of both HfO$_2$ / Al$_2$O$_3$ and Al$_2$O$_3$ / HfO$_2$. HfO$_2$ has a lower band-offset than Al$_2$O$_3$ and we expect to observe barrier lowering in only one bias direction for both types of devices. The double-layer samples are therefore useful to compare the amounts of barrier lowering in one direction for structures of otherwise identical composition and thickness.

Simulations show that the thinner tunnel oxides will result in a larger amount of charge being stored in the floating gate, yet a concern is that as the HfO$_2$ or Al$_2$O$_3$ layer becomes too thin, leakage paths will be present. For that reason a variety of sample
thicknesses are listed. Two types of floating gates (25 nm and 15 nm poly-Si) are being fabricated. It is expected that the 25 nm film will result in a continuous floating gate while the 15 nm film will be somewhat nanocrystalline, potentially mimicking the advantages of a nanocrystal memory. Each MOS sample will have 150 nm poly-silicon deposited to act as a gate contact.

Samples 20 – 23 are samples that will not be fabricated into MOS capacitors but will be used in current-voltage and internal photoemission experiments. Such experiments are extremely sensitive to leakage current, so thicker structures are required to obtain clear measurements of band-offset.

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Table A.1. Samples from IBM – MOS devices with HfO₂ / Al₂O₃ tunnel barriers.
A.4.2 Transistor design for IBM samples

Figure A.12 shows the MOS gate stack after the deposition steps have been completed at IBM. The next steps in the transistor design involve lithography and etching of the films. The chosen transistor design requires a two-step mask process. The first lithography step defines the gate stack for a wide range of devices, including ring-gate transistors, capacitors, and resistors. Each of the devices will be patterned using photolithography and will be etched down to the silicon as is shown in Fig. A.13. Next, the entire wafers will be implanted, both to make the poly-silicon gate contact and to form the source and drain of the ring-gate transistors as is shown in Fig. A.14. The n⁺-type implant will be of phosphorous. The dose will be $5 \times 10^{15}$ ions / cm$^2$ at 5 keV. A 1 minute anneal in nitrogen at 900°C will activate the dopants without having the phosphorous diffuse into the control oxide. The resulting doping should be about $3 \times 10^{15}$ based on simulations done usingATHENA processing software.

![Gate stack diagram](image)

Fig. A.12. Gate stack after deposition of films at IBM.
The final step for the processing is metallization using a second mask and photolithography step. Aluminum contacts will be deposited to contact each transistor, capacitor, and resistor using a lift-off procedure. All of the processing steps (following the depositions at IBM) including mask design, implant, lithography, and etching can be performed over the entire wafers at a company such as MEMs Exchange.

Fig. A.13. Gate stack after devices have been defined by etching.

Fig. A.14. Gate stack after implantation of phosphorous. The implant makes the poly-silicon control gate conductive while defining the source and drain.
A.4.3 Mask design details

We have worked out the dimensions for each individual device to be fabricated and the details follow.

Resistors: The resistor contact pads will be $250 \mu m^2$. There will be two types of transistors, with 500 squares and 100 squares. The squares will be $1 \mu m$ and $3 \mu m$ on each side, giving a total of four resistors.

Capacitors: The capacitors will be square, with 1000, 500, 250, 150 $\mu m$ on each side.

Transistors: Two types of transistors will be fabricated, embedded transistors (see Fig. A.15(a)) and offset gate ring transistors (Fig. A.15(b)). The total field size for the embedded transistor (the green portion) is $750 \times 750 \mu m^2$. The channel in Fig. A.15(a) is blue. The source is red and consists of a square in the middle (the contact pad) and a leg width that corresponds to the length of the channel in Table A.2.

![Fig. A.15. General schematics showing the transistors to be fabricated. (a) shows an embedded gate transistor. (b) shows an offset gate ring transistor. Blue represents the “active” channel regions under the poly-silicon control gate. Red represents the source region. Yellow represents the drain region. Green represents the “inactive” channel regions under the polysilicon control gate.](image-url)
Table A.2. Dimensions for embedded transistors.

The dimensions for the offset contact transistors shown in Fig. A.15(b) are shown in Table A.3, with a total of 42 permutations of transistor width, source size, and contact pad size.

<table>
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<th>Length of channel (µm)</th>
<th>Width of channel (µm)</th>
<th>Source (µm)</th>
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</table>

Table A.3. Dimensions for offset contact transistors.

The contact pads will be 150 µm squares. They will be deposited on each source (red in Fig. A.15) and each contact pad (green). There will also be at least 2 drain contacts (yellow) somewhere at the bottom of the field.

<table>
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<tr>
<th>Width (µm)</th>
<th>Source (µm)</th>
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The devices operate like the floating-gate memory devices described in Chapter 2. Voltages are applied to the control gate and also to the source and drain to generate carriers within the channel. At a particular gate voltage, electrons will be drawn toward the control gate and will be stored on the floating gate once voltages are removed. The stored charge can be measured by a threshold voltage shift.

**A.5 Conclusion**

We have measured MOS capacitors that incorporate SiO₂ and HfO₂ / Al₂O₃ / HfO₂ tunnel barriers. The SiO₂ sample showed good program and erase transients indicated by a flat-band shift of over 1 V, with program/erase voltages of ±3 V. However, the program and erase states are not stable over time, drifting back to the intermediate, uncharged state in a matter of seconds. The HfO₂ / Al₂O₃ / HfO₂ also showed an available flat-band shift of 1 V. The “erase” state was easily achievable by a short -3.2 V pulse, yet it drifted back to its uncharged state very quickly. A “program” state was not achievable with voltages up to 3.4 V, when the device broke down. We calculated the expected oxide and depletion capacitance values for each sample and our results were well within an order of magnitude, but did not correspond exactly with the simulated values. Because of this, in order to more fully understand the capabilities of layered tunnel barriers, we have designed a complete set of MOS transistors based on the high-k growth capabilities of IBM.

The MOS transistors that have been described are expected to have improved device characteristics. These devices will allow for the measurement of the actual stored charge on the floating gate of a transistor, rather than the inferred charge based on the
measured capacitance. All the deposition steps will be performed at IBM, and a wide variety of tunnel oxides have been proposed for easy comparison of the layered tunnel barriers with the single-layer tunnel barriers. All of the device fabrication steps can be performed by a processing service such as MEMs Exchange, based on the parameters and processing steps that have been outlined within this appendix.

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